A temperature stabilized CMOS VCO

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Abstract The established method of frequency drift compensation in voltage controlled oscillators (VCOs) resulting from temperature variance involves modulation of control voltage using a non-linear voltage internally generated. An innovative frequency drift compensation scheme for a VCO, based on amplitude control, is described in this paper. Two peak detectors are used to generate voltages representing positive and negative peaks of the sinusoidal driving an error amplifier. The amplifier output controls the delivery of transconductance accessible to the oscillator, thereby keeping the oscillation amplitude steady. Frequency stability has improved to 16 ppm/°C from an uncompensated value of 189 ppm/°C and is applicable where frequency stability requirements are not stringent, such as HS-USB and S-ATA. The temperature stabilized VCO at 2.4 GHz center frequency is prototyped using CMOS technology from ams AG (formerly austriamicrosystems AG). The result obtained from this study indicates that better frequency stability may be achievable if the traditional compensation scheme is preceded by amplitude control.

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Abbreviations

AAC	Automatic amplitude control
OTA	Operational transconductance amplifier
ppm	Parts per million
PSS	Periodic steady state
PVT	Process, voltage and temperature VCO
	Voltage controlled oscillator
ZTC	Zero temperature coefficient

1 Introduction

Frequency drift in voltage controlled oscillators (VCOs) resulting from temperature variance is a critical design problem for radio frequency applications such as transceiver circuits in communication networks, data link protocols, medical sensor networks and micromechanical resonators used in silicon. A popular method of frequency compensation is that of modulating the control voltage terminal of the VCO using an appropriately generated control voltage (V_{CNTRL}) as summarized in Table 1, selected from recently published articles on temperature compensation applicable to oscillators in general. The oscillation frequency of an LC VCO may be represented as [1]

$$\omega T( ) \sqrt{\frac{1}{L(C_f + C_v\ V_{CNTRL})}\left[1 - \frac{C_f R^2_L(T) + C_v}{V_{CNTRL}(\quad)\quad R^2_L L}\right]}$$

$$(1)$$

where L is the inductor, C_f, the fixed capacitance in the tank circuit, C_v the variable capacitance of a varactor controlled

Table 1 Comparison of temperature compensation based on modification of V_{CNTRL}, selected from recent journal articles

	[1] 2009	[2] 2007	[3] 2012	[4] 2010
Technology node	0.25 μm	0.6 μm	90 nm	0.18 μm
Frequency (MHz)	800	5.5	1,400	14
$\Delta f = \frac{\partial_f \times 10^6}{\Delta T \times f_r}$ (ppm/°C)	1.689	0.39	51.43	11.52
Oscillator architecture	LC	FBAR resonator	Ring VCO	RC

Fig. 1 A generalized schematic of negative g_m LC oscillator

by a voltage V_{CNTRL}, and R_L the losses in the inductor. As the temperature is increased, $V_{CNTRL}(T)$ increases in a corresponding manner such that the resulting change in C_v compensates for the frequency drift.

To the best knowledge of the authors, the current body of knowledge concentrates on generated error voltage as a means to compensate for frequency drift. However, the use of amplitude control as a technique for improving immunity against process, voltage and temperature (PVT) variations is widely reported [1], [5–7].

This paper presents the design of a temperature compensated VCO based on an amplitude control mechanism for frequency drift compensation. The principle is validated through prototyping using the 0.35 μm CMOS technology (ams AG). The remainder of this paper is organised as follows: Sect. 2 critically evaluates the origins of frequency drift as a result of temperature variance noted in recent journals. Implementation of amplitude control to reduce the temperature dependency is illustrated in Sect. 3, followed by circuit design in Sect. 4. Results and the discussion involving the prototyped IC are presented in Sect. 5. Conclusions are drawn in Sect. 6.

2 Origins of frequency drift over temperature

The threshold voltage of MOS devices reduce in relation to increase in temperature [8]. A negative increment in V_{th} causes increased transconductance in the VCO core that results in a higher oscillation amplitude. It has also been established that an increment in oscillation amplitude translates into a negative shift in frequency [9].

The expression for drain current in an n-channel MOS, derived for long channel operation, is [8]

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_{th} \right)^2 \qquad (2)$$

Equation (2) contains the mobility term μ_n and the threshold voltage V_{th}; both depend on temperature and both variables have a negative temperature coefficient (TC)[10]. Therefore it is possible to achieve a zero temperature
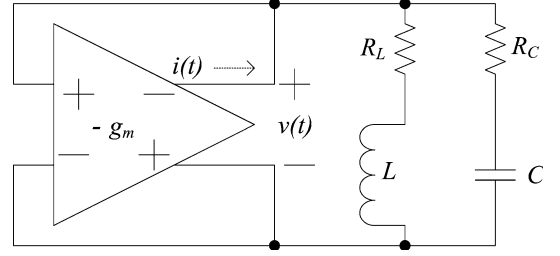
coefficient (ZTC) bias point, where any variation in temperature should not affect the bias current.

A generalized schematic of a negative transconductance (g_m) oscillator is provided in Fig. 1 [9]. The parasitic element is represented by R_L and R_C of the inductor and capacitors respectively. The natural resonant frequency of the resonator is

$$\omega_o = \sqrt{1/LC} \qquad (3)$$

Temperature and bias conditions affect the oscillation frequency in a predictable manner in an LC oscillator [1, 9].

The parasitic losses in the tank are overcome by the transconductance amplifier. From Fig. 1 the expression for oscillation frequency may be modified as

$$\omega_1 = \omega_0 \sqrt{\frac{L - CR_L^2}{L - CR_C^2}} \qquad (4)$$

Assuming the losses in the integrated capacitor are negligible compared to that of the integrated inductor, the oscillation frequency could be modified as

$$\omega_1 \approx \omega_o \sqrt{1 - \frac{CR_L^2}{L}} \qquad (5)$$

As the substrate resistance shows a positive TC, from (5) it is evident that an LC oscillator biased at ZTC still demonstrates a linear negative TC.

Furthermore, in a VCO, an increment in tail current, a power supply spike, or change in temperature leads to an injection of a current $i(t)$ with high harmonic content into the tank. Consequently, generated harmonics in the LC network are reconciled by reducing the frequency of oscillation. Equation (6) enables the prediction of oscillation frequency as a function of bias conditions [1, 9].

$$\omega = \omega_1 \left(1 - \frac{1}{2Q^2} \sum_{n=2}^{\infty} \frac{n^2}{n^2 - 1} h_{i(n)}^2 \right) \qquad (6)$$

where $Q = \omega_o L / \left(R_L + R_C \right)$ and $h_{i(n)} = I_n / I_1$ where I_n is the nth Fourier coefficient of $i(t)$.

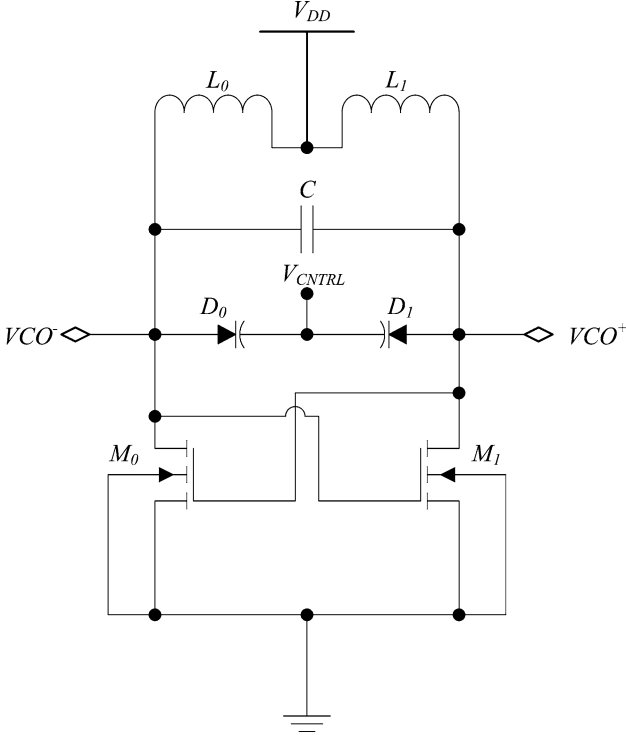Equations (5) and (6) confirm the argument that a positive increment in tail current results in a substantial

reduction of the oscillation frequency. An illustration of this effect is provided in [9]. Any further increment in bias current results in saturation. LC oscillators operated at this bias current demonstrate better frequency stability. Improved frequency stability is however in trade off with phase noise penalty [9].

From (3) it is clear that the effective inductance and the capacitance of the tank primarily determine the oscillation frequency. The current that passes through the inductor causes an image current in the substrate, which reduces the effective inductance. As the temperature increases, the substrate resistance increases. This increment in resistance reduces the image current and increases the effective inductance. In a spiral inductor, conductors are placed in close proximity to one another. Each segment induces eddy currents in other segments that cause series resistance to increase [11]. This phenomenon causes a further reduction in frequency according to (5). Effective capacitance constitutes the capacitance of the resonator as well as parasitic contributions from all reverse biased junctions shunting the inductor. However, the capacitance of the resonator displays a lower temperature dependency.

From this discussion it is evident that if an LC oscillator is operated at ZTC bias, negative frequency drift originates through modulation of net tank inductance L, or capacitance C, or net losses in the tank R_L, R_C, or harmonic content of bias current $i(t)$. Therefore it is concluded that the negative frequency drift resulting from a positive increment in temperature could be reduced, if the injection of harmonic content of bias current into the oscillator tank circuit is held constant. For a temperature induced frequency drift compensation the negative transconductor is biased using temperature independent current source. In this method to compensate for the coil loss induced drift, reactive compensation is suggested [9].

3 Temperature compensation using amplitude control

For LC VCOs, the amplitude of oscillation varies with the frequency of oscillation [6]. This implies that harmonic contents of the bias current or losses in the inductor induce a negative frequency drift resulting in a modified amplitude of oscillation. Therefore in order to prevent the frequency drift, this paper proposes to track down the amplitude of oscillation accurately, which is subsequently used for frequency compensation. An automatic amplitude control (AAC) is used for this purpose. Conventional AAC circuits utilize a single reference voltage; however for better noise and harmonic performance a dual AAC that generates two DC representing positive and negative peaks is proposed.

An AAC circuit generates two voltages, V^+ and V^-, representing the negative and positive peaks of the

Fig. 2 Temperature compensated VCO using AAC

oscillating waveform. Any harmonic component present in the peaks is suppressed by envelope detection. The operational transconductance amplifier (OTA) output controls the amount of transconductance available to the oscillator by limiting the bias current. As the frequency drift is captured from peak detection of the oscillating waveform, the presence of higher harmonics must be further suppressed. A band limited OTA with high common mode rejection must be utilized. The complete system design is illustrated in Fig. 2.

In the AAC circuit, V^+ is set higher than V^- to ensure the availability of bias current for the oscillator at start-up. Once the amplitude of oscillations is picked up, the OTA_{OUT} responds to the differential input voltage $V_{ID} = (V^+ - V^-)$ at the input. Thus closed loop action will force the V^+ and V^- to be closer, as the oscillations are established and a state of equilibrium is achieved. When any of the variables causes perturbations in the amplitude, the AAC output initiates the compensatory action by modifying V_{ID}, in turn controlling the conductivity of M_{CNTRL}.

4 Circuit design and layout

4.1 LC oscillator based VCO

In order to experimentally validate the key contribution of this paper, i.e. the amplitude control principle, a negative g_m architecture is chosen from the existing literature [6]. A differential cross-coupled LC oscillator topology such as Fig. 3 is selected since it is less sensitive to PVT, as well as to common-mode noise interferences [12, 13].
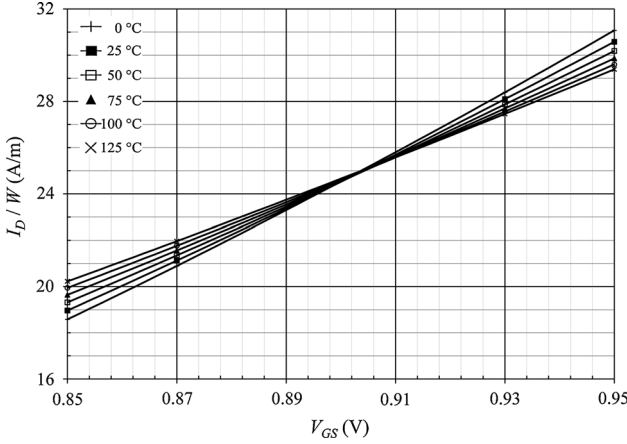
Fig. 3 Schematic of the LC VCO

Fig. 4 Illustration of ZTC bias point

An equal amount of bias is provided for both gates of the transistors. The ZTC bias current is selected for the oscillator design. A plot of transistor current density, I_D/W, against V_{GS} is depicted in Fig. 4.

In Fig. 4, the ZTC bias for NMOS transistors is observed when $I_D/W = 25$ and is chosen for designing the oscillator. In order to assist in further designing g_m/I_D versus I_D/W plots are derived using Cadence Virtuoso$^{®}$ employing Spectre Simulator. Transistors of minimum channel length are selected, as they deliver better unity gain frequency (f_t). All the simulations are performed using
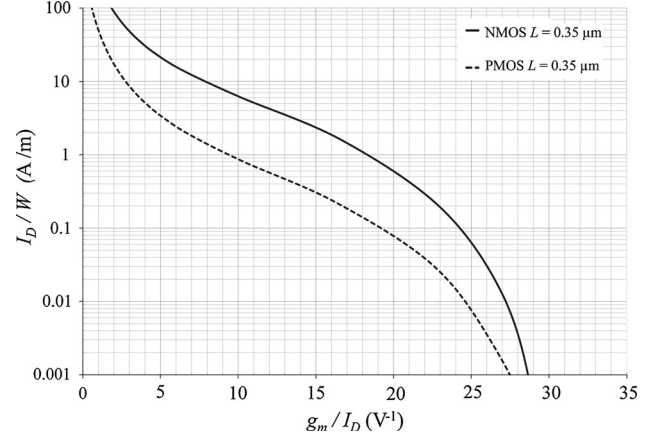
Fig. 5 A plot of g_m/I_D versus I_D/W for NMOS and PMOS transistors

transistors of $W = 10$ μm and $L = 0.35$ μm. Transistors with different widths and lengths are found to be overlapping, as reported in [14]. Resulting plots are shown in Fig. 5.

In order to vary the frequency of the oscillator, a varactor is to be included. The two different types of varactors available in the process are junction varactors and MOS varactors operated in the accumulation mode. It was observed that the accumulation mode MOS varactor offers performance much superior to junction varactors in terms of power consumption, phase noise and tuning range [15, 16]. An accumulation mode MOS varactor known as CVAR in the ams AG process is used in this work. There are four rows, and 12 columns are used to provide the required amount of capacitance.

4.2 Aac

From the sinusoidal generated by the oscillator, two voltages that represent the average positive peak (V^-) and the average negative peak (V^+) are formed by the AAC. Peak detectors are implemented differentially to improve noise rejection. Figure 6 shows the complete circuit diagram of the AAC. Transistors M_0 and M_1 conduct alternately at the corresponding positive peak of the sinusoidal, and charge the capacitor C_0. M_2 acts as the current source. The voltage across C_0 is then level shifted to V^- using transistor M_3. Similarly a negative peak detector is implemented using PMOS devices M_5, M_6, M_7 and a capacitor C_1. A positive increment in oscillation amplitude causes a rise in potential for V^- and a drop in potential for V^+. This action of the AAC results in reduced differential output voltage $V^+ - V^- = V_{ID}$, in response to an increase in oscillation ampli-tude. Similarly the AAC responds to a drop in oscillation amplitude by increasing the V_{ID}, forcing the M_{CNTRL} to increase the delivery of additional transconductance.
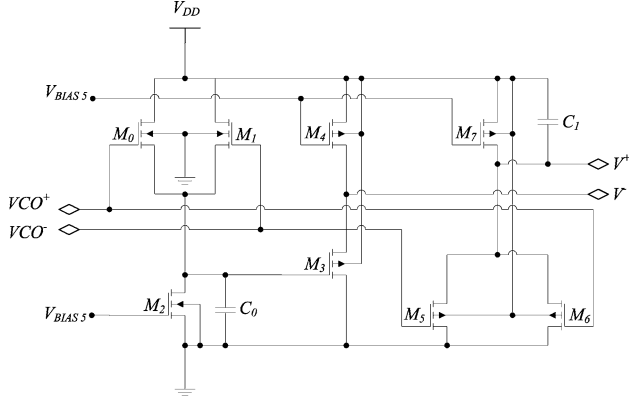
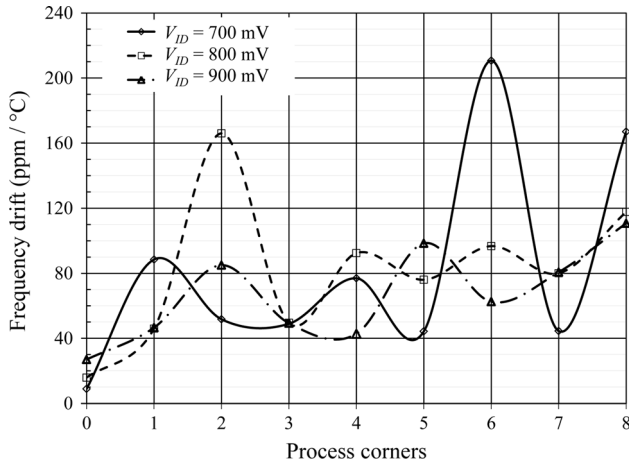**Fig. 6** AAC circuit schematic

Fig. 7 Frequency drift versus process corners for different V_{ID}

The set value of V_{ID} directly influences the amount of amplitude control achieved over the temperature range. Therefore it is imperative that AAC be characterized for different values of V_{ID}. Tighter amplitude control is expected to provide better temperature compensation but the effect of process variations needs to be accounted for. For a given oscillation amplitude $(VCO^+ - VCO^-) = V_{p-p} = 1$ V, the aspect ratio of level shifter M_5 is varied such that $V_{ID} = 0.7$ V, 0.8 V and 0.9 V. The resulting periodic steady state (PSS) simulation is performed at temperatures 0–125 °C in six steps. This simulation is again repeated at nine process corners containing combinations of typical mean (TM), worst case power (WP)—(fast NMOS– slow PMOS), worst case speed (WS)—(slow NMOS, fast PMOS) for transistors and capacitors. Further corners are identified for inductors in the form of 'high Q factor', and 'low Q factor' (LQ). Frequency drift in ppm/ ° C versus process corners is plotted in Fig. 7.

The best frequency compensation is observed for $V_{ID} = 0.7$ V, which at process corner zero (all TM corners)
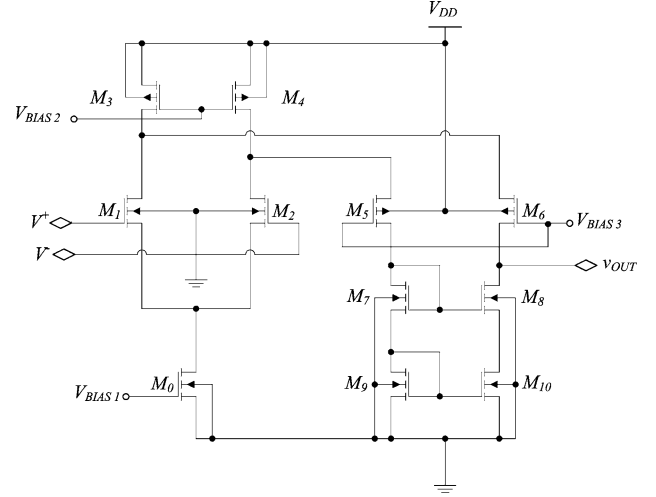
Fig. 8 Folded cascode OTA topology used

is 9 ppm/°C, but offers very high frequency drift of 200 ppm/°C at corner six (WS, WP, LQ for transistors, capacitors, inductors respectively). The worst result at a typical mean corner is observed for $V_{ID} = 0.9$ V, but provides a reduced maximum drift of 120 ppm/°C at corner eight. The best performance in a typical mean corner is always the best choice for any design, but as a design trade-off $V_{ID} = 0.8$ V is selected for this design.

4.3 Ota

An OTA is used as the error amplifier because of its high gain, reasonably large output signal swing and input dynamic range. One of the factors that could affect the gain of an op-amp is the short channel effect. This effect in turn modifies the square-law transfer characteristics in the saturation region to a more linear response. One of the short channel effects that contribute adversely to the gain of the op-amp is the reduced output impedance. Therefore, a longer channel length must be used. However, such lengths consume additional space on the silicon wafer. As a design compromise, a channel length of 1 μm is chosen. An OTA using folded cascode topology such as in Fig. 8, with a gain of 56 dB and the first pole at 300 kHz is designed.

The sub-systems that constitute a temperature compensated VCO are: an oscillator operated at ZTC; an AAC that generates two voltages, which represent the positive and negative peaks of the oscillation; an OTA that acts as an error amplifier, regulating the bias current to the oscillator; a bias voltage reference using MOS transistors as well as an output buffer designed in schematic and layout. The completed design is thereafter integrated in a single integrated circuit and subsequently prototyped in silicon at ams AG.

Figure 9 illustrates the layout of the temperature stabilized VCO and occupies an area of 675 μm × 1225 μm in

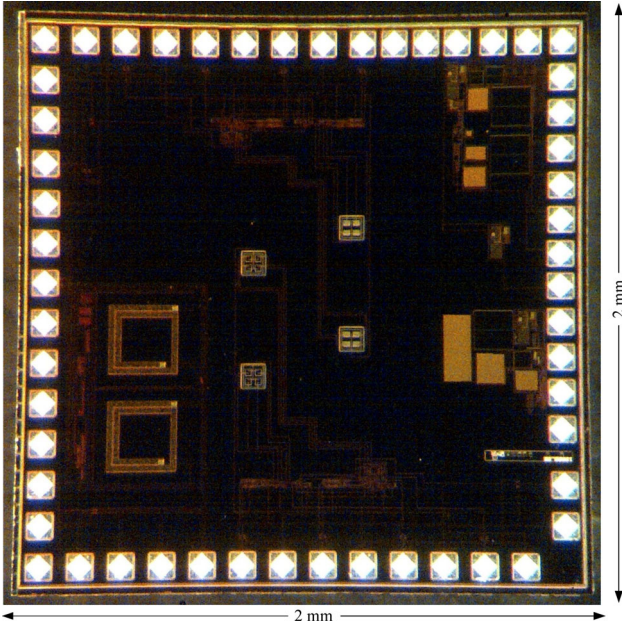**Fig. 9** Temperature stabilized VCO layout
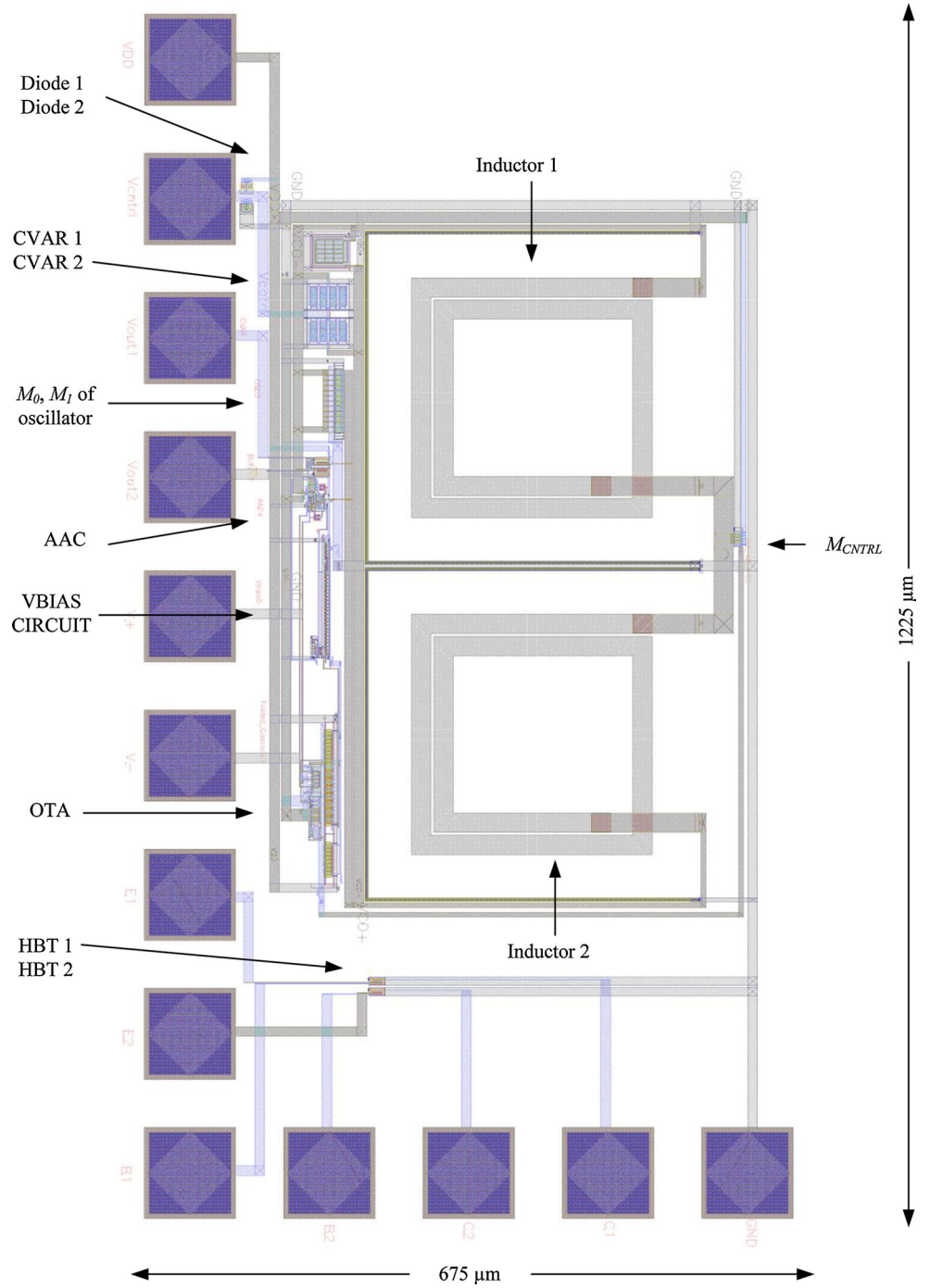
the multi project wafer. The chip microphotograph is depicted in Fig. 10.
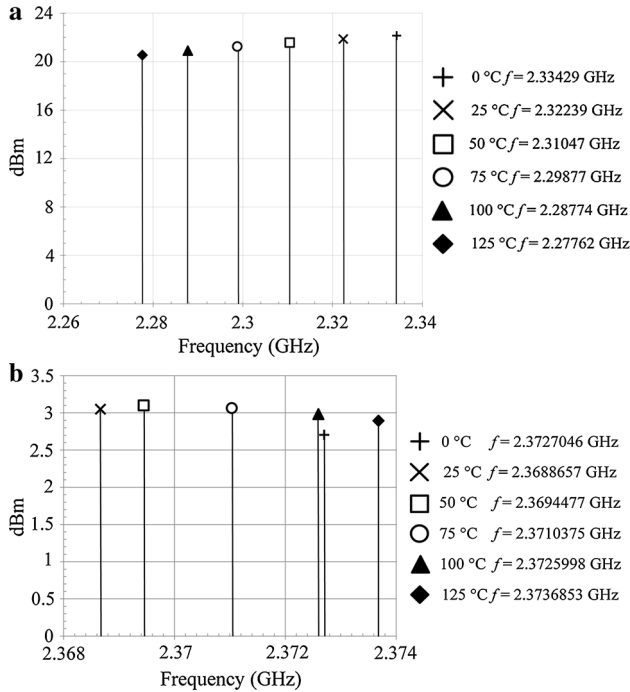
5 Results and discussion

In order to generate comparisons, an open loop VCO is simulated in PSS analysis available in Cadence Virtuoso. PSS simulations were first performed on an oscillator directly supplied by a 3.3 V power supply, and then the

same VCO was connected in a temperature stabilised loop such as in Fig. 2. The results of the PSS analysis with temperature as the parametric sweep variable at an interval of every 25 °C are presented in Fig. 11.

In Fig. 11(a) the frequency spread is 56.65 MHz for a temperature sweep of 0° C to 125° C. From Fig. 10(a) it may be observed that the frequency drift is in a negative direction in all temperature intervals. However, in Fig. 10(b) frequency spread has reduced to 4.82 MHz. The frequency drift is in a negative direction between the

Fig. 10 Chip microphotograph of the prototyped temperature stabilized VCO

Fig. 11 Frequency spread versus temperature, **a** in an open loop VCO supplied from a power supply, **b** in a temperature stabilized closed loop

Table 2 Frequency compensation observed in five temperature intervals of 25 °C

Temperature interval (°C)	Open loop VCO Δf (MHz)	Temperature stabilised VCO Δf (MHz)
0–25	−11.76	−3.839
25–50	−11.94	0.579
50–75	−11.77	1.593
75–100	−11.04	1.562
100–125	−10.14	1.086

Sect. 2. Table 2 compiles the results presented in Fig. 10(a, b) in five temperature intervals of 25 °C each.

In the case of an open loop, in every temperature interval there is a consistent frequency shift in a negative direction. The closed loop VCO demonstrates a reduced amount of frequency shift, as expected. For the closed loop VCO, in the first interval 0 and 25 °C there is again a reduced frequency shift of 3.839 MHz. This confirms that the closed loop action is effective in reducing the frequency drift. In the next four intervals of temperatures the negative frequency shift is greatly compensated for by this approach; it is in fact over-compensated for, resulting in a slight positive shift in frequency. It may also be argued from Table 2 that the amplitude control action is not fully effective in the temperature range of 0–25 °C. The amount of transconductance available to the VCO core at start-up is just sufficient to establish the Barkhausen criterion for self-starting the oscillations. As the oscillation amplitude is much smaller than gate source voltages of transistors in the AAC circuit, the amplitude control is inactive. For the rest of the temperature intervals the AAC is active and explains the improved temperature compensation.

Section 2 explains how three identified variables contribute to frequency drift. In Sect. 4, results display much better frequency stability, reconfirming that the AAC limits the injection of harmonic current into the tank. Therefore, it may be argued that by holding the oscillation amplitude to a constant value, the harmonic component of the bias current had in fact been suppressed. This also means that the first two variables, modulation of L, C, in the tank circuit, and the corresponding parasitic losses (R_L, R_C), are still contributing to frequency drift, but at much lower levels. Consequently, it may be reasoned that the contri-bution of losses in the tank to frequency drift is made indirectly through perturbations in oscillation amplitude, which is held moderately constant.

In comparison with recent journal articles on frequency drift compensation, listed in Table 1, the amount of frequency stability obtained in this work indicates that amplitude control is an effective way of controlling frequency drift.

temperatures of 0 and 25 °C. Between temperatures of 25 °C and 125 °C the compensatory action of the amplitude loop limits the transconductance available to the VCO core, thereby reducing the frequency drift, as described in

Improved frequency compensation presented here is based on reducing the injection of higher harmonic content rather than operating the oscillator at a much higher bias current that results in saturated operation as mentioned in [9]. However some phase noise penalty exists, as additional noise sources are present in the AAC circuit [17]. Phase noise reduction is however outside the scope of this paper.

6 Conclusion

A new and simpler approach for improving the frequency stability of an LC VCO based on amplitude control is described in this paper. The temperature stabilized VCO is implemented in a standard CMOS process. Simulation results indicate that frequency stability over temperature has improved to 16 ppm/°C using a combination of ZTC bias and amplitude control. It could thus be concluded and generalised that improved temperature compensation might be obtained if any compensation scheme should be preceded by amplitude control.

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