

# Design and performance of a wideband DRFM for radar test and evaluation

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The test and evaluation of modern radars using hardware in the loop (HIL) simulators requires the use of wideband, high fidelity, digital radio frequency memories (DRFM) in order to generate realistic target returns. This paper highlights important aspects of wideband DRFM design on printed circuit board (PCB) and also presents the architecture of the DRFM that was implemented using commercial-off-the-shelf (COTS) components. The spurious-free-dynamic-range (SFDR) of the DRFM was characterised as -47 dBc worst-case over an instantaneous bandwidth of 800 MHz. An experimental pulse-Doppler radar was used to compare the fidelity of the returns from the DRFM and an optical delay line (ODL).

*Introduction:* In the modern radar test and evaluation environment there is a need for HIL simulator systems able to simulate realistic target returns so that fewer aircraft flights are required to test the radar's performance. The HIL simulator captures the radar's transmit pulse by mixing it down and sampling it with a high-speed analogue-to-digital converter (ADC). In order to simulate a target at a specified range delay, the captured ADC information is transferred into memory and re-transmitted at the correct range via a high-speed digital-to-analogue converter (DAC) and RF up-conversion chain. This architecture is commonly referred to as a DRFM [1, 2].

Modern radars tend to have wide agile bandwidths and thus require the simulator system to have a wide instantaneous bandwidth to capture and recall frequency agile radar signals. The storage and recall of the radar pulse information also needs to exhibit high fidelity in amplitude and phase to provide a reliable return signal to the radar. The design focus should thus be on attaining the conflicting, wideband and high fidelity, characteristics simultaneously. The available data converter technology

provides less bits as the conversion frequency increases, thus providing less signal fidelity at higher instantaneous bandwidths than at lower instantaneous bandwidths. It is therefore critical to understand the aspects involved in a high-speed mixed-signal design that “push the boundaries” on all fronts in order to achieve exceptional performance.

*Important considerations:* It is not always feasible or cost effective to design and implement a complex, high performance, high-speed mixed-signal system like a DRFM on a single integrated circuit (IC), hence this research effort highlights the important aspects of the realisation of such a system on a PCB using COTS components.

As operating frequencies of systems increase, the physical size of circuits and devices being used becomes more important. The ratio of the physical length of the circuit or device,  $L$ , to the wavelength of the signal in the conductor,  $\lambda$ , is referred to as the electrical length,  $L/\lambda$  [3]. Ideally one should keep the electrical length of a circuit as small as possible since the circuit can then be treated as a lumped circuit and analysed using basic circuit theory. An electrical length of  $1/20$  is a conservative transition point from lumped to distributed circuit theory [3]. In order to achieve short electrical length circuits in the Gigahertz-domain on PCB, circuits need to be implemented in close proximity to one another, but caution must then be exercised regarding crosstalk. Fig. 1 shows current density in the reference plane of a stripline transmission line structure. The figure illustrates that the return current density is mostly kept underneath the signal trace and by doing so follows the path of least inductance. The return current density on the reference plane is described by [4]:

$$J_x = \frac{I}{\pi W} \left[ \tan^{-1} \left( e^{\frac{\pi x - w/2}{2h_1}} \right) - \tan^{-1} \left( e^{\frac{\pi x + w/2}{2h_2}} \right) \right]$$

where  $h_1$  and  $h_2$  are the distances between a signal trace and the lower and upper reference planes respectively.

The principle of return currents at high frequencies following the path of least inductance is an important one. If this path is provided by design, then the circuit becomes deterministic in terms of its electrical interaction with nearby circuits. In Fig. 1, it can be seen from the distribution of the return current in the reference plane, that if the distance ( $D$ ) between the aggressor and the victim traces can be increased, more isolation can be achieved between these two signals with respect to their return currents.

Another important design aspect in mixed-signal design is grounding. Data converter devices typically contain pins for both analogue and digital grounds. This sometimes creates confusion among circuit designers regarding ground plane splitting on PCB's. This research has shown that partitioning of analog and digital components in a mixed-signal design along with a moat and bridge approach on a single reference plane as advocated in [5], provides exceptional results. The key to success of the moat and bridge approach is to route all of the signals that cross between the analog and digital partitions over the bridge as illustrated in Fig. 2.

*Wideband DRFM design:* Fig. 2 indicates the specific data converters and field-programmable-gate-array (FPGA) that were chosen for this wideband DRFM design. This circuit required an 18 layer, controlled impedance PCB. The DRFM was designed to operate with a sampling clock of 2 GHz and to have a usable bandwidth of 800 MHz.

*Measured results:* A good measure of the fidelity of a DRFM is its SFDR which is shown in Fig. 3. The figure shows the measured SFDR of the ADC, DAC and DRFM as individual traces. A worst-case SFDR of -47 dBc was measured over the 100 to 900 MHz band. An equalizer was used on the output of the DRFM to compensate for

the  $\sin(x)/x$  amplitude slope. The DRFM was also tested against an experimental pulse-Doppler radar and its performance against the radar was compared with that of an ODL which produces a good approximation of an ideal target return to the radar. The results of these comparative tests are shown in Fig. 4 and Fig. 5. To the authors' best knowledge, this is the first publication of quantitative performance measurements of a high fidelity wideband DRFM against a pulse-Doppler radar.

*Conclusion:* A wideband, high fidelity DRFM was designed and characterised for its SFDR performance as well as tested against a pulse-Doppler radar. The test against the pulse-Doppler radar showed that even though quantisation effects of the DRFM are evident, the spurious levels are so low that it is unlikely that advanced electronic counter countermeasures (ECCM's) in the radar will be able to distinguish between a physical target return and one generated by the DRFM.

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**Figure captions:**

Fig. 1 Illustration of current density in the reference plane underneath a signal trace

Fig. 2 Schematic block diagram of the wideband DRFM showing implementation of moat and bridge approach on a reference plane

Fig. 3 Measured SFDR of the wideband DRFM

Fig. 4 Comparison of the radar's Range-Doppler map for the ODL target (upper plot) and the DRFM target (lower plot). The amplitude scale is in dB.

Fig. 5 Comparison of the radar's range responses (upper plot) and Doppler responses (lower plot) for the ODL and DRFM target.

Figure 1

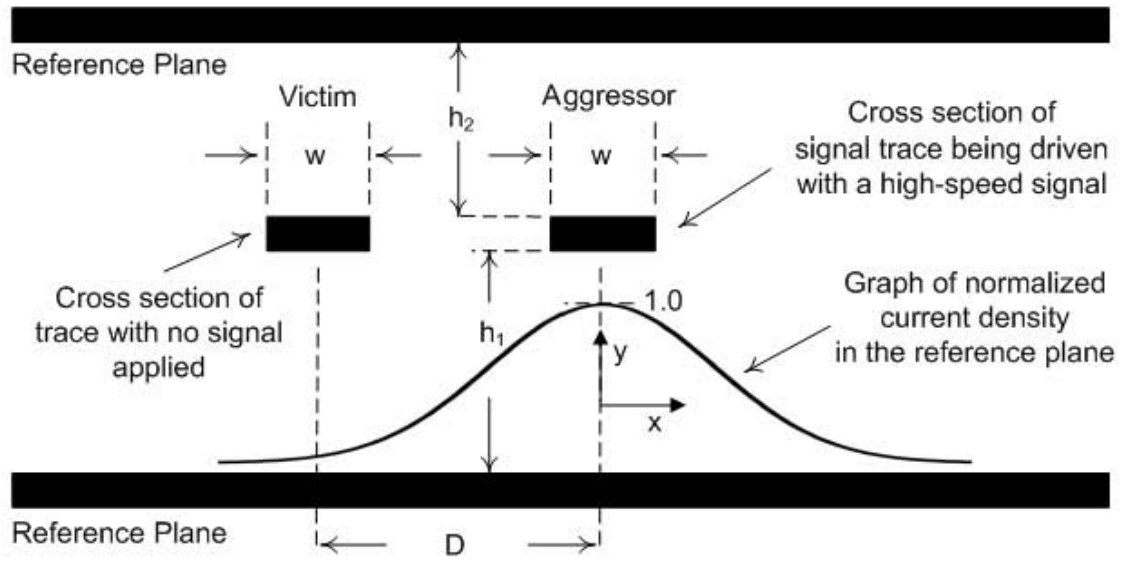


Figure 2

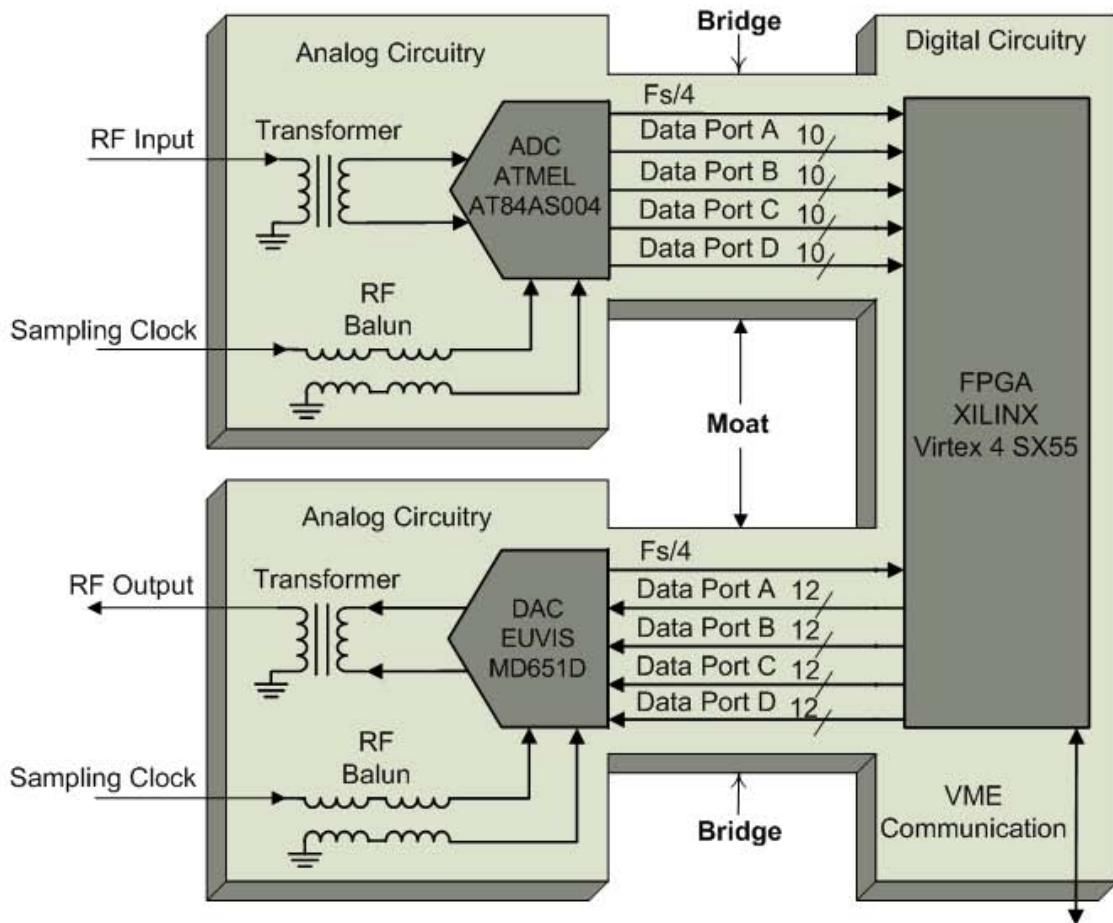


Figure 3

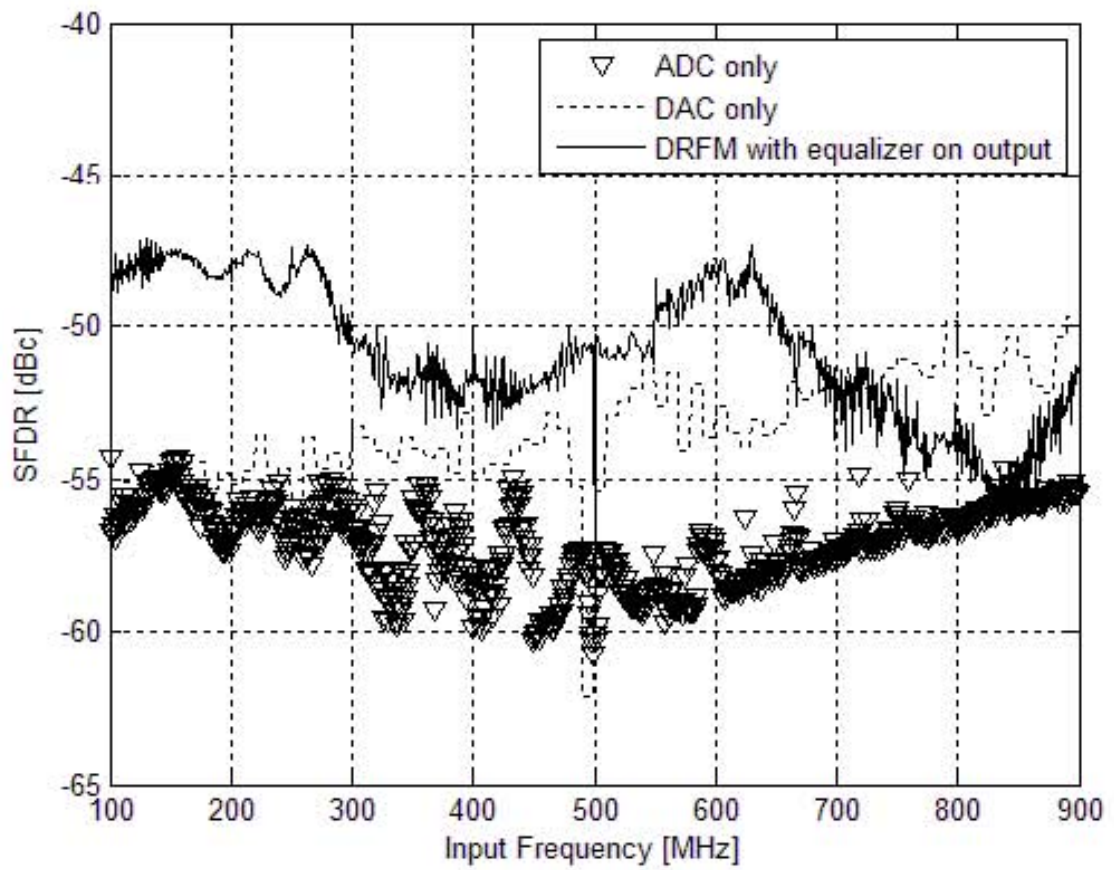
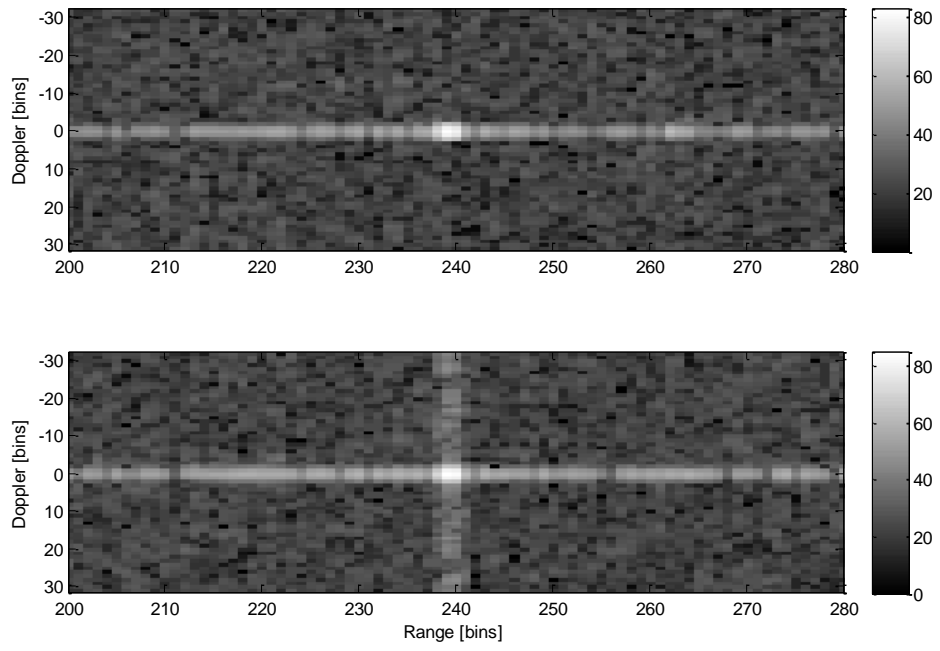


Figure 4



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Figure 5

