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Electrical characterization of sputter-induced deep levels in GaN thin films synthesized by electrodeposition

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ABSTRACT

This paper reports on the presence of deep-level defects in polycrystalline GaN thin films induced during the sputter deposition of Au Schottky barrier diodes (SBDs). The n-GaN films, with a thickness of approximately 300 nm were electrodeposited on (111) Si substrates using a low-cost method and a current density of 3 mA.cm^{-2} for 3 hours. Structural analysis by X-ray diffraction, scanning electron microscopy, and atomic force microscopy confirmed the polycrystalline nature and good quality of the films. Deep-level transient spectroscopy (DLTS) revealed a broad, asymmetric peak around 265 K in the as-deposited SBDs, indicating the presence of multiple defects. Laplace DLTS resolved four distinct defects with energies ranging between 0.40 eV and 0.60 eV. Thermal annealing between 450 - 500 K increased the reverse leakage current with only minor changes in the forward-bias characteristics. However, annealing at 550 K significantly reduced the leakage current by two orders of magnitude and improved the rectification ratio by one order of magnitude. All samples exhibited significant series resistance. Capacitance-voltage measurements revealed a reduction in the free carrier density near the surface, suggesting the sputter process introduced additional deep level defects. Furthermore, the deep-level energy (and therefore the likely defect composition) was found to be sensitive to the annealing temperature.

1. Introduction

III-V nitride materials, such as GaN, AlN, and InN, are highly suitable for high-power and high-temperature optoelectronic devices because of their wide direct band gaps and high saturation velocities [1]. Polycrystalline GaN offers several practical advantages over single-crystalline GaN, particularly for cost-effective, large-area applications. It can be grown on diverse substrates such as silicon, ITO glass, and metals using low-temperature, low-cost methods like sputtering or electrodeposition, avoiding the complexity and expense of epitaxial growth. Although polycrystalline GaN contains more grain boundaries and defects, these can enhance performance in gas sensors and photocatalytic devices by increasing surface activity and charge-transfer efficiency. Polycrystalline films also show strong adhesion and excellent chemical stability, enabling reliable operation under harsh conditions [2–10].

Importantly, the bandgap of GaN alloys can be modified between 0.69 eV and 6.3 eV by the substitution of Ga with either In or Al. For example, when alloyed with In, the bandgap of $In_xGa_{1-x}N$ ranges from 0.69 eV - 3.4 eV, whereas for $Al_xGa_{1-x}N$, bandgaps of 3.4 eV - 6.2 eV are possible.

Interestingly, GaN crystallizes into either zinc blend (cubic), rock salt (cubic) or wurtzite (hexagonal) crystal structures. Cubic GaN is metastable, whereas the hexagonal form is thermodynamically stable [11]. Moreover, intrinsic GaN is *n*-type, highly doped (~10^{18} cm^{-3}) because of the incorporation of residual donor impurities during crystal growth [12], whereas *p*-type GaN is difficult to grow. This is due to the absence of dopants with delocalized holes acting as shallow acceptors. For example, the hole of Mg (substituting Ga) is highly localized and therefore forms a deep acceptor in GaN. The selection of growth methods for GaN and its ternary alloys is based on the intended application, material quality requirements, and scalability. To this end, molecular beam epitaxy (MBE) and metal–organic chemical vapor deposition (MOCVD) are among the most widely used techniques for the growth of high-quality epitaxial GaN thin films [13–15]. These are, however, expensive techniques.

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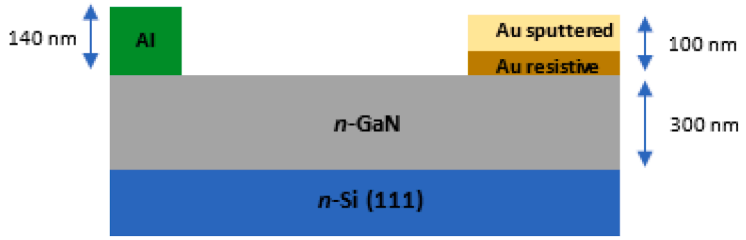


Fig. 1. The Au/n-GaN/Al SBD structures used in this study.

In this work, electrochemical bath deposition, an inexpensive growth technique, was used to grow polycrystalline GaN. Additionally, Schottky barrier diodes (SBDs) are fundamental to semiconductor device technology and are preferable to regular p-n junction diodes because of their fast switching, low forward voltage drop, and short reverse recovery time. For these reasons, SBDs are regularly used in high-frequency applications and microwave systems, as well as in power rectification and clamping circuits [16–18]. Moreover, high-quality SBDs are commonly fabricated on epitaxial GaN by sputter deposition, but little information is available on electrochemically deposited (ED) GaN. Some advantages of this technique, compared with resistive deposition, include the ability to deposit metallic compounds stoichiometrically and to deposit metals with high melting points at high deposition rates and improved adhesion [19,20]. The disadvantage, however, is that the high energy associated with sputtered atoms may, upon collision, dislodge atoms from their stable lattice position, causing a cascade of atomic displacements. These displacements cause perturbations in the periodic lattice potential, resulting in unintended states (defects) in the forbidden gap These lattice defects are, by and large, located in the near-surface region [20,21] where they significantly affect carrier dynamics and therefore the optical and electrical properties of the material and subsequently fabricated devices [22,23]. While defects in epitaxially grown GaN have been extensively studied, this research focuses on characterizing electrically active defects in polycrystalline GaN thin films grown by a cost-effective electrochemical bath deposition method. Additionally, the study examines how these defects respond to thermal treatment.

2. Experimental procedure

Electrochemical deposition was used to prepare polycrystalline GaN thin films on Si (111) substrates (1 cm × 1 cm) with a carrier concentration of 3.5 × 10^{15} cm^{-3}. The films were prepared at room temperature by mixing 0.034 mol/dm^3 $Ga(NO_3)_3$ and 0.025 mol/dm^3 of NH_4NO_3 in deionized water. Deposition of the GaN film on the Si was facilitated via a simple electrochemical cell consisting of a carbon anode and a Si cathode (the substrate), while the mixture, under continuous stirring, served as the electrolyte. The chemical reaction evolves as follows:

$$Ga(NO_3)_{3+}\ H_2O \rightarrow Ga^{3+} + 3NO_3^{1-}$$

$$NH_4NO_3 + H_2O \rightarrow NH_4^{1+} + NO_3^{1-}$$

$$NH_4^{1+} + NO_3^{1-} \rightarrow NH_3 + HNO_3$$

$$Ga\ (NO_3)_3 + NH_3 \rightarrow GaN + 3HNO_3$$

The current density during growth was maintained at 3 $mA.cm^{-2}$, and the growth period was 3 hours. The structural and microstructural properties of the resulting GaN films were investigated using X-ray diffraction (XRD) performed with a Bruker D2 Phaser diffractometer equipped with Cu $K\alpha_1$ radiation (λ = 1.54056 Å) operating in Bragg-Brentano (θ-2θ) reflection geometry. Surface morphology and microstructural features were examined using scanning electron microscopy (SEM) with a Zeiss Ultra Plus field-emission gun (FEG) microscope, while atomic force microscopy (AFM) measurements were carried out

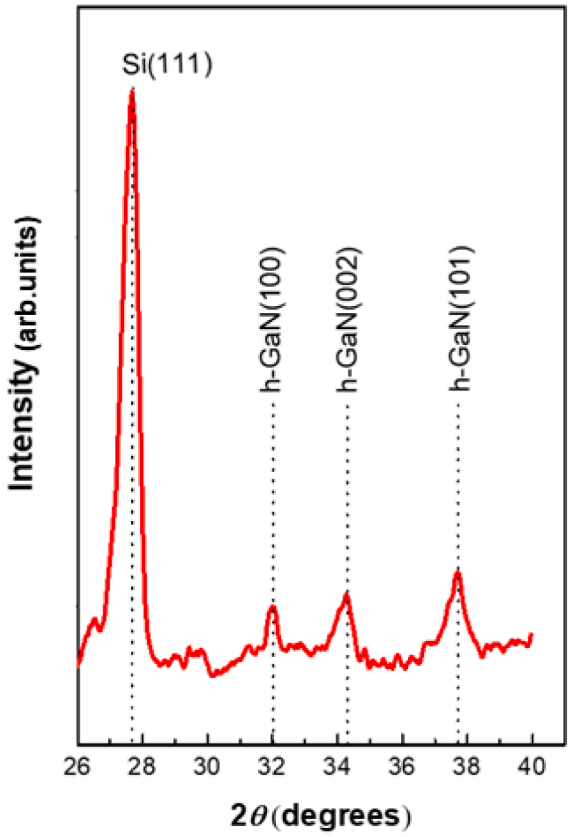


Fig. 2. XRD pattern of the h-GaN thin film electrodeposited on Si (111) using a current density of 3 $mA.cm^{-2}$. The growth period was 3 h.

using a Bruker Dimension Icon to further characterize the surface morphology of the deposited samples.

To form ohmic contacts, a 140 nm Al layer was deposited through a metal contact mask onto the GaN surface using resistive evaporation. No annealing was required to form a low resistance ohmic contact. Au SBDs were evaporated on the same surface next to the Al ohmic contact. Notably, Tang et al. showed that sputter damage could be limited during SBD fabrication by resistively evaporating a thin 20 nm gold layer before proceeding with sputter deposition [24]. The Au SBDs fabricated in this study were therefore deposited using a similar two-step process depicted in Fig. 1. Au dots, 10 nm thick and 0.6 mm in diameter, were resistively evaporated through a metal mask directly onto the GaN layer. No adhesion layer was needed. Next, an additional 90 nm thick Au layer was sputter-deposited onto the already established 10 nm Au/GaN/Al SBDs.

Sputter deposition was performed at a DC bias of 350 V and a discharge current of 0.05 A with an RF power of 20 W applied. The sputtering duration \ was 5 minutes. During the deposition the chamber pressure was maintained at 8 Pa and the target was positioned 50 mm above sample holder. The quality and basic electrical properties of the

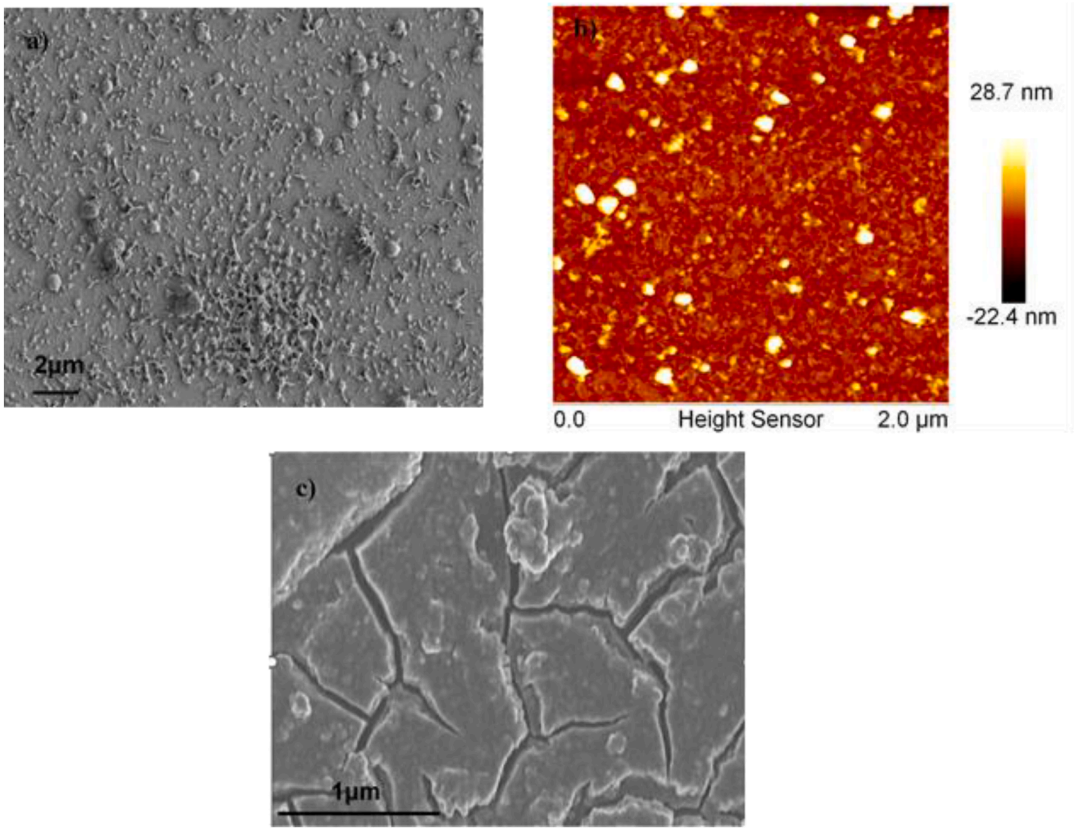


Fig. 3. (a) SEM and (b) AFM images of a 100-nm-thick electrodeposited GaN thin film grown in this study. For comparison, (c) shows an SEM image of a GaN layer grown for 30 minutes under similar deposition conditions [28].

GaN films were assessed using current–voltage *(I-V)* and capacitance–voltage *(C-V)* measurements, while the electrical characteristics of the sputter–induced defects were investigated using deep-level transient spectroscopy (DLTS) [25] and Laplace DLTS [26]. The *I-V* and *C-V* measurements were conducted at room temperature, using an HP 4140B pA meter/voltage source and an HP 4192 impedance analyser. Following the initial characterization, the samples were annealed at 450 K, 500 K and 550 K in N_2 gas for 10 minutes to evaluate the evolution and thermal stability of the sputter-induced defects.

3. Results and discussion

3.1. Structural characterization

X-ray diffraction (XRD) patterns of the ED GaN thin films grown at a current density of 3 mA.cm^{-2} for 3 hours are depicted in Fig. 2. These XRD patterns show a high degree of agreement with the JCPDS 50-0792 (Joint Committee for Powder Diffraction Standards) cards used to identify the phases present in the XRD patterns, which are commensurate with the structure of hexagonal (h) - GaN. The main peaks are observed at 32.05°, 34.30°, and 37.69°, confirming the hexagonal wurtzite phase of GaN for the films. The average crystallite size was calculated via Scherrer's formula [27]:

$$D = \frac{0.9\lambda}{\beta \cos\theta_B}, \tag{1}$$

where D represents the crystallite size, λ represents the wavelength of the incident X-rays (1.54 Å for Cu $K_{\alpha 1}$), θ_B represents the Bragg angle, and β corresponds to the full width at half maximum of the XRD peak. Importantly, owing to the relatively low intensity of the h-GaN peaks observed in the XRD pattern, only a rough estimate of the crystallite size could be obtained. By applying Scherrer's method, the average crystallite size for the sample was estimated to be approximately 20 nm.

Fig. 3(a) and (b) show the SEM (2 kV operating voltage) and AFM micrographs, respectively, of the GaN thin films grown for 3 h at a current density of 3 mA·cm^{-2}. This current density was selected because it resulted in optimum grain sizes, as reported in a previous study [28]. The polycrystalline GaN surface is uniform yet uneven, with a roughness of approximately 1.96 nm and consists of agglomerated particles, with a maximum height of ~30 nm, as confirmed by AFM. Fig. 3 (c) is included for comparison and shows a SEM micrograph of a similarly electrodeposited GaN layer deposited for 30 minutes at a current density of 3 mA.cm^{-2} [28]. As previously reported, the growth time strongly influences the morphology of the GaN layers [28]. Growth initiates with the nucleation of small clusters, which subsequently coalesce into larger islands that contain significant cracks (Fig. 3(c)) [28]. Extending the growth time (to 3 hours in this study) resulted in a rough but continuous layer. The layers become continuous, most likely because the cracks become covered as the islands increase in size and merge with prolonged growth.

3.2. Electrical characterization

I-V and C-V characteristics

The *I-V* characteristics of an SBD for which the current crosses the barrier, primarily owing to thermionic emission, are described by the following equation [29,30]:

$$I(V) = I_s\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right], \tag{2}$$

where V is the applied voltage, n is the ideality factor, q is the elementary charge and k is Boltzmann's constant.

Here, I_s, and the saturation current is expressed as [29,31]:

$$I_s = AA^*T^2\exp\left(-\frac{q\phi_{b,\,IV}}{kT}\right). \quad (3)$$

where A is the cross-sectional area of the SBD, A^* is the effective Richardson constant, and $\phi_{b,IV}$ is the zero bias barrier height.

In the region of the $log(I)$ *vs* V plot where the voltage drop due to series resistance is negligible (i.e., $V \gg IR_s$), Eq. (2) simplifies to:

$$I(V) = I_s\exp\left(\frac{qV}{nkT}\right). \quad (4)$$

The ideality factor and the saturation current, I_s, are obtained from the slope and y-intercept, respectively, of a linearized plot of Eq. (4), whereas the barrier height is extracted from Eq. (3). The series resistance, R_s, of the measured devices was determined by fitting Eq. (2) to the experimentally obtained $log(I)$ *vs* V plots.

It is instructive to note that a high series resistance, R_s, would affect the impedance of the complex series RC circuit which constitutes the SBD, Therefore, DLTS measurements may be influenced in several ways:

Since a SBD with notable series resistance acts as a voltage divider, the voltage drop ($\Delta V = I_{pulse}R_s$) across R_s will reduce the effective bias across the junction. This may lead to incomplete trap filling, particularly for traps located deeper in the depletion region or those with higher capture barriers. Because the transient current during the filling pulse varies dynamically, the instantaneous voltage drop across the SBD also changes, and may cause spatial non-uniformities in trap filling. However, since DLTS measures the average emission of charge from filled traps above the crossover point, this effect is not expected to alter the intrinsic defect emission rate. To accurately resolve a trap emission rate in DLTS, the junction RC time constant must be significantly shorter than the emission time constant of the defect; otherwise, the transient becomes distorted and no longer reflects the true trap kinetics [25]. Clearly, a significant R_s should introduce an additional time constant, $\tau = RC$, that can obscure the true trap emission rate and, therefore, may distort the measured capacitance transient. This could result in a broadening and temperature shift of the DLTS peaks. Moreover, when R_s is significant, the circuit impedance deviates from a purely capacitive response, leading to an underestimation of the actual junction capacitance and a corresponding reduction in DLTS signal amplitude.

In our case, the series resistance of our Schottky barrier diodes was measured directly from a fit of Eq. (2) to the forward-bias I-V characteristics. and was sufficiently small to assume that the effective bias across the depletion region remained essentially unchanged during the filling pulse. The applied pulse amplitude can therefore be considered accurate, with negligible impact on trap filling.

Additionally, DLTS measurements were performed at 1 MHz, where the influence of R_s on the junction capacitance is suppressed and R_sC was smaller than the emission time constant of the detected traps. These conditions confirm that significant distortion of the capacitance transient and the extracted emission rates due to R_s are unlikely. Accordingly, the recorded transients are considered to reliably reflect the intrinsic defect properties of the material, in agreement with that reported by [32].

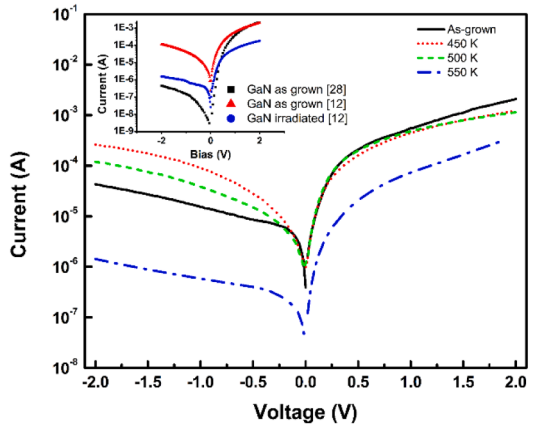
The capacitance per unit area of an SBD is given by [30]:

$$\frac{1}{C^2} = \frac{2}{\pm q\varepsilon_s\,(N_a - N_d)A^2}\left[\pm V_{bi} \pm V - \frac{kT}{q}\right], \quad (5)$$

where ε_s is the permittivity of (in this study) hexagonal GaN and where V is the applied voltage. Here, "+" and "-" refer to p-type and n-type materials, respectively. For the latter, $N_d > N_a$, $V_{bi} < 0$ and $V < 0$.

The x-axis intercept of an $1/c^2$ *vs* V plot gives V_i, which in turn is related to the built-in potential, V_{bi}, via the equation $V_i = -V_{bi} + kT/q$, where T is the measurement temperature. The C-V-derived barrier height, $\phi_{b,\,CV}$, is given by:

$$\phi_{b,CV} = V_{bi} + V_0 = -V_i + V_o + kT/q. \quad (6)$$



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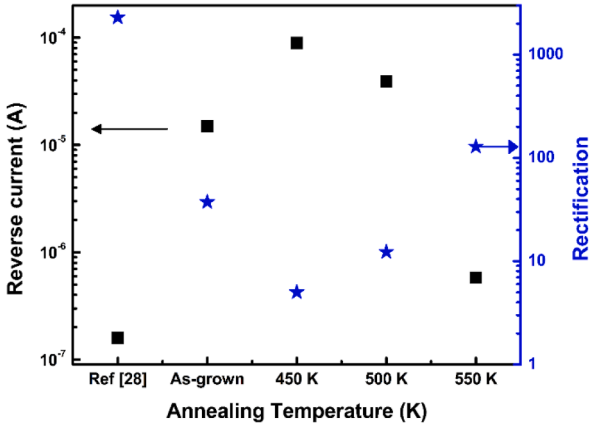

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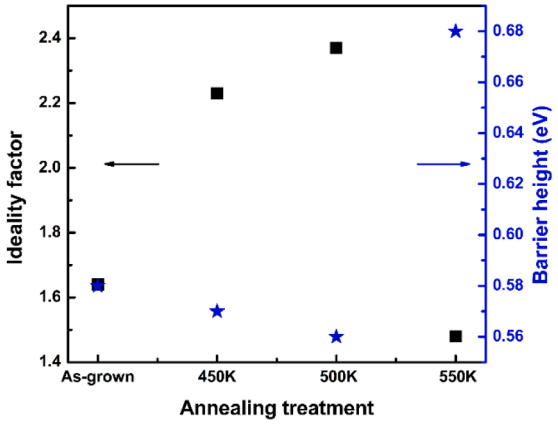
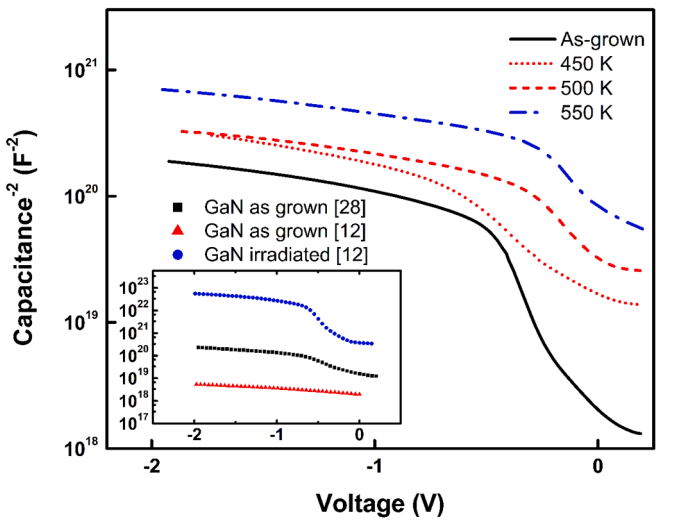


(c)

Fig. 4. Current-Voltage characteristics of the sputtered Au/GaN/Al SBD before and after annealing at different temperatures (a). The inset graph displays the I–V characteristics of resistively evaporated Au/GaN/Al SBDs on similar GaN films grown at 3 mA.cm^{-2} [28] and 1 mA.cm^{-2} [12], respectively. Leakage current and rectification ratio (b) and ideality factor and barrier height, derived from I–V measurements (c), as a function of the annealing after annealing at different temperatures. (Note: Stars represent barrier height and squares represent ideality factor).



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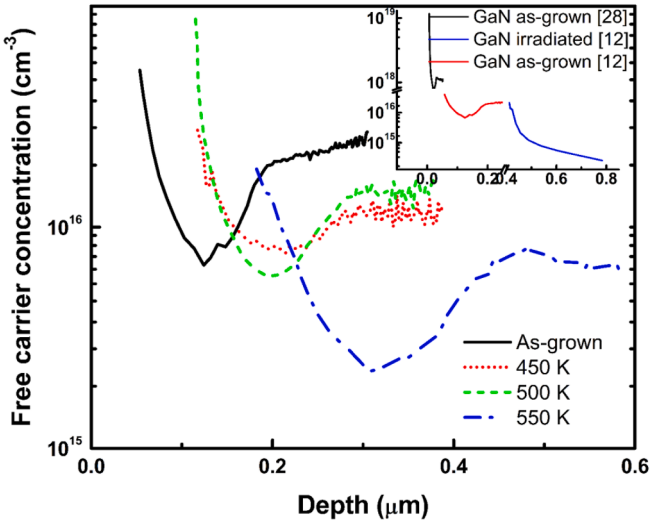


(b)

Fig. 5. (a). $1/c^2$ versus V plots of the sputter deposited Au SBD before and after annealing between 450 K and 550 K. The inset figures were obtained from resistively evaporated SBDs on similar n-GaN films grown at 3 mA.cm^{-2} [28] and 1 mA.cm^{-2} [12], respectively. Note the substantial change in the free carrier profile, especially near the surface, following alpha particle irradiation [12], Fig. 5 (b). Depth profiles of free carrier concentration in sputtered Au/GaN/Al SBDs before and after annealing. Insets show data from resistively evaporated on GaN films grown at 3 mA.cm^{-2} [28] and 1 mA.cm^{-2} [12].

$\phi_{b,CV}$, which is determined in this way, is the so-called flat band barrier height since it is determined from $1/c^2$ *vs* V, where $1/c^2 \rightarrow 0$. V_0 is related to the density of states in the conduction state,N_c and the free donor concentration, N_d and is given by:

$$V_0 = \frac{kT}{q} ln \frac{N_c}{N_d}. \tag{7}$$

The derivative of Eq. (5) allows the determination of the free carrier depth profile [29]:

$$\frac{dC^{-2}}{dV} = -2\left(q\varepsilon_s A^2 N_d\right)^{-1}, \tag{8}$$

Fig. 4(a) shows typical *semilogarithmic I-V* plots obtained at room temperature (RT) of the as-sputtered and subsequently annealed (450-550 K) Au/GaN/Al SBDs investigated in this study. The large reverse current is tentatively attributed to grain boundary conduction and/or barrier height inhomogeneity, which is expected considering the surface morphology of the GaN film surface. Notably, the reverse leakage current increases significantly with increasing annealing temperature between 450 K and 500 K and then drastically decreases following annealing at 550 K. The inset in Fig. 4(a) displays the *I-V* characteristics of resistively evaporated Au/GaN/Al SBDs on similarly grown GaN films at 3 mA.cm^{-2} [28] and 1 mA.cm^{-2} [12].

All the SBDs exhibited rectifying behaviour with significant series resistance. The rectification ratio decreases after annealing at 450 K but improves at 500 K and 550 K. This trend is evident from the plots of the series resistance and leakage current versus the anneal temperature.

To compare the leakage current and rectification ratio as a function of annealing temperature, the current for each diode was measured at ±1 V, as shown in Fig. 4(b). The leakage current reached a maximum after annealing at 450 K, but decreased to its lowest value following annealing at 550 K.

Fig. 4(c) presents the ideality factor and Schottky barrier height, extracted from the *I-V* characteristics, for both the as-sputtered and annealed Au SBDs. The barrier height remained relatively stable at an average of 0.57 eV for the as-grown sample and those annealed at 400 K and 500 K. However, for the sample annealed at 550 K, the barrier height increased to 0.68 eV, representing an enhancement of approximately 20%.

The series resistance is also strongly temperature dependent and increases from 456 Ω (sputtered) to 1861 Ω (sputtered and annealed at 550 K), most likely due to changes in the composition and structure in the near-surface region [33]. In comparison, contacts that were evaporate resistively (reported in an earlier study) have the lowest series resistances [12,28]. It is worth noting too that the ideality factor of the sputter-deposited Au/GaN/Al SBDs fabricated in this study is substantially lower (~ 44% on average) than that of the Au/GaN/SBDs resistively deposited on similar EC-grown h-GaN layers [12,28].

The results obtained from *C-V* measurements of the sputter-deposited Au/GaN/Al SBDs and their response to annealing are depicted in Fig. 5. In Fig. 5(a), the $1/c^2$ versus V plots show that the carrier concentration is nonuniform and increases sharply toward the surface. The decrease in capacitance following annealing indicates that the observed donor-type defects are annealed.

Fig. 5(b) shows the free carrier density depth profiles of the SBDs before and after each annealing step. In all measurements, the same bias range was used. The depth profiles clearly indicate that the depletion region extends deeper into the semiconductor after each annealing stage. Since the *I-V* characteristics suggest that the Schottky barrier height does not change significantly, this shift is attributed to the annealing of donor-type defects near the metal/semiconductor interface. These defects are located so close to the interface that they are not detectable through *C-V* depth profiling. Although a substantial number of defects anneal out at 450 K and 550 K, very little defect annealing is observed between 450 K and 500 K.

The evolution of the carrier density profiles near the surface further suggests the diffusion of donor-type defects into the bulk of the semiconductor, with the extent of diffusion increasing as the annealing temperature rises. The characteristic dip in the carrier concentration is observed to shift progressively deeper below the surface with higher annealing temperatures. Notably, because this feature consistently appears within approximately the same bias range, it is more plausibly attributed to interface-related states rather than a real reduction in the free carrier concentration [33–35]. The free carrier concentration of the sputter-deposited samples before annealing (measured at a depth of 0.2 μm) was approximately 2.0. × 10^{16} cm^{-3}. As the annealing temperature increased, a decrease in the free carrier concentration beyond 0.2 μm was observed, together with a clear drift of carriers away from the surface into the GaN film. For the sample annealed at 550 K, a minimum carrier concentration of 1.5 × 10^{15} cm^{-3} was recorded at a depth of 0.3

Table 1
I-V and *C-V* characteristics of the as-grown sputter-deposited and subsequently annealed GaN samples.

Sample	n	$\Phi_{b\ I-V}$ (eV)	$\Phi_{b\ C-V}$ (eV)	I_s (A)	R_s (Ω)	N_d-N_a (cm^{-3})
Sample *a* [28]	1.80	0.76	0.92	5.09×10^{-9}	416	1.20×10^{16}
Sample *b* [28]	2.30	0.60	0.71	2.43×10^{-6}	241	1.70×10^{16}
GaN as-grown [12]	2.4	0.58	1.18	1.20×10^{-6}	550	1.10×10^{18}
Irradiated GaN [12]	2.6	0.64	2.2	1.20×10^{-7}	7500	1.10×10^{16}
Sputtered sample	1.64	0.58	0.82	8.83×10^{-7}	456	2.70×10^{16}
Annealed at 450 K	2.23	0.57	0.63	1.66×10^{-6}	1032	1.42×10^{16}
Annealed at 500 K	2.37	0.56	0.94	1.98×10^{-6}	1313	1.57×10^{16}
Annealed at 550 K	1.48	0.68	0.98	6.50×10^{-8}	1816	6.96×10^{15}

μm, followed by an increase to approximately 7 $\times 10^{15}$ at 0.65 μm. Furthermore, it was observed that α-particle irradiation [12] produced a substantial modification in the free-carrier distribution, particularly near the surface.

The *C-V* derived barrier height $(\phi_{b,\ CV})$, except for that of samples annealed at 450 K, appears to increase with increasing annealing temperature and is, on average, as expected, greater than that obtained via *I-V* measurements, in which the value is ~ 40%. The large difference and inconsistency in $\phi_{b,\ IV}$ *vs* $\phi_{b,\ CV}$ are attributed to, among other factors, the drastic increase in carrier concentration close to the surface of the GaN films (see Fig. 5). Additionally, the two techniques are fundamentally distinct. The difference between the *I-V* and *C-V* barrier heights can be explained by considering how the variation in the barrier height across the surface of the diode influences the measurement in each case. In the case of *I-V* characteristics, regions with different barrier heights are effectively parallel, implying that the region with the lowest barrier height will dominate the current transport behavior. Therefore, for Schottky diodes with barrier height variations, the low barrier height regions are expected to control the *I-V* characteristics. This effect is enhanced by the exponential dependence of the current on the barrier height. With respect to *C-V* measurements, regions of a Schottky contact with different local barrier heights contribute different capacitances. The measured capacitance therefore represents a weighted average of these contributions, resulting in *C-V* measurements smoothing out, or averaging, spatial variations in the barrier height. As a consequence, barrier height inhomogeneities typically cause a larger reduction in the *I-V* derived barrier height than in the *C-V*-derived value. In addition, the reduced image-force lowering expected for materials with high free-carrier concentrations further influences the current transport dynamics in this system [33,36,37].

Table 1 lists the basic electrical properties obtained from the *I-V* and *C-V* measurements for the sputter-deposited Au/GaN/Al SBD before and after annealing. The ideality factor of the unannealed SBD was 1.64, which, following annealing, increased and reached a maximum of 2.37 at 500 K. Further annealing at 550 K resulted in an improvement in the ideality factor from 2.37 to 1.48. This improvement is attributed to the recrystallization of the GaN film and a commensurate decrease in the

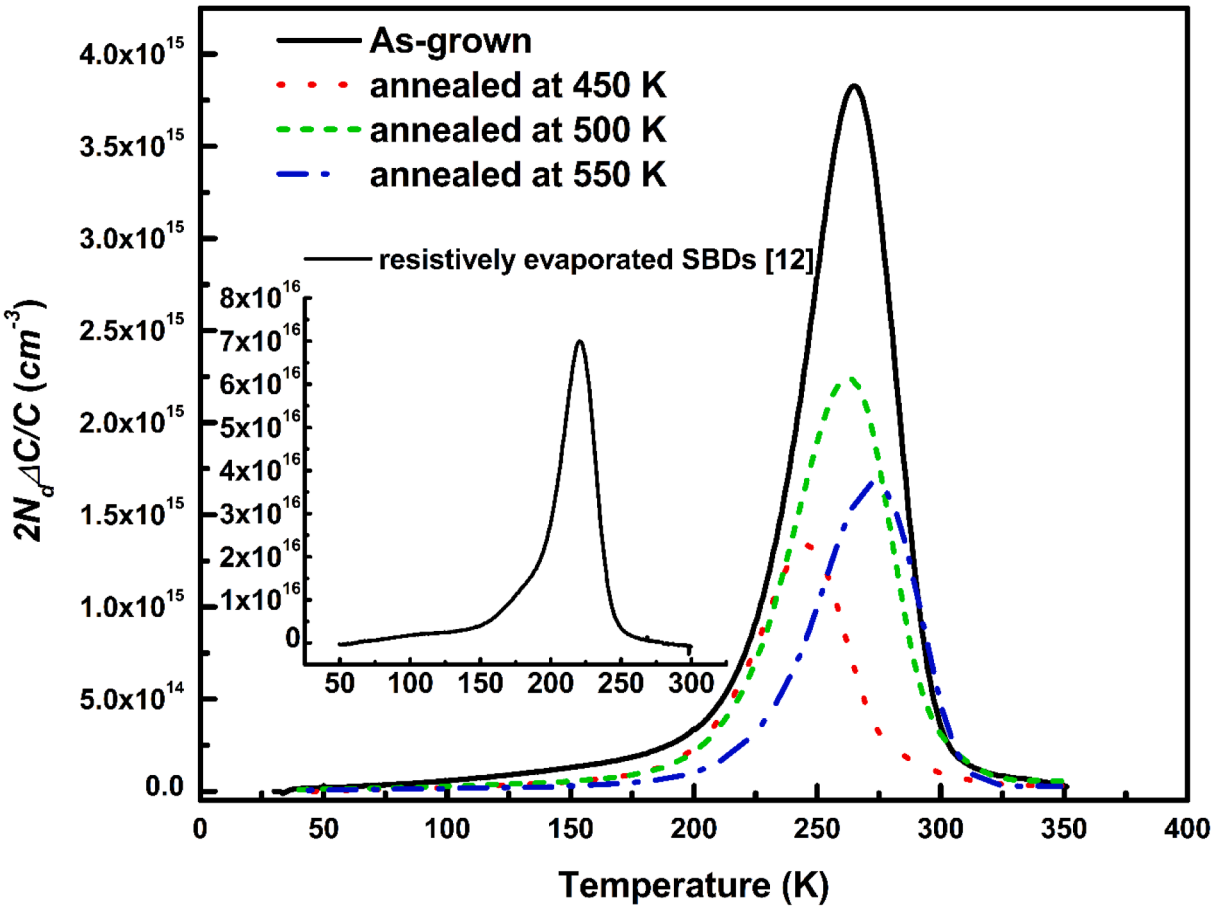


Fig. 6. The DLTS spectra of the sputtered SBDs before and after annealing. The spectra were recorded at a reverse bias of -2 V, a pulse of 2 V and a pulse width of 1 ms. The inset shows corresponding data for resistively evaporated contacts on GaN films grown at 1 mA·cm^{-2} [12]. The rate window was 80 s^{-1} for all samples.

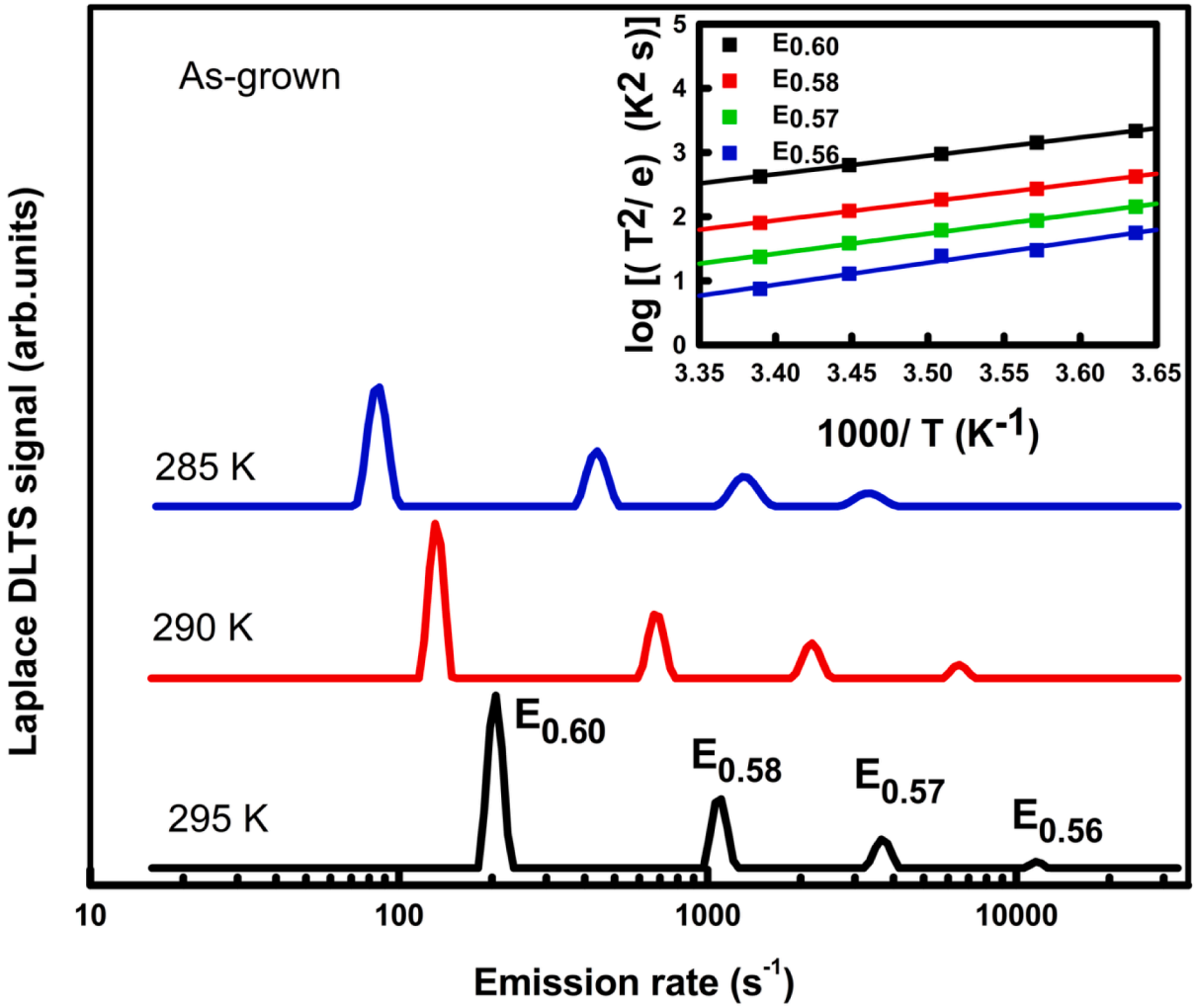


Fig. 7. Laplace DLTS spectra obtained from the unannealed sputter deposited Au/GaN/Al SBDs. The inset figure represents the Arrhenius plots for the defects detected in this sample.

surface state density.

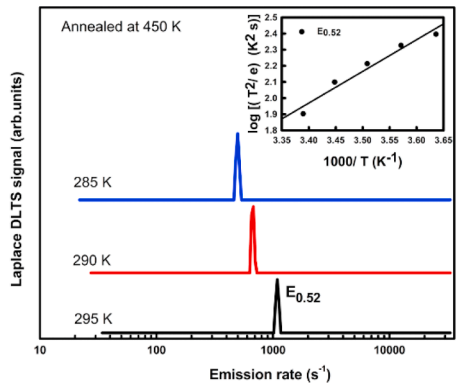
As is clear from the presented *I-V* and *C-V* results summarized in Table 1, the quality of the devices differs substantially from one annealing temperature to the next, and annealing (as is the case for the 550 K anneal) may result in significant improvement in some of the *I-V* characteristics of the SBDs. This improvement is attributed to the removal or migration of defects away from the active region of a device [34], enhanced crystallinity [35], a reduction in surface states (such as nitrogen vacancies, oxygen interstitials and Ga dangling bonds) [32], and stress relief in the material. Notably, the barrier height obtained from *C-V* measurements is greater than that derived from *I-V* measurements. This discrepancy arises because *I-V* measurements are more sensitive to interface states and barrier inhomogeneities. Additionally, significant series resistance reduces the apparent barrier height in *I-V* measurements compared with that in *C-V* measurements [29,30].

Fig. 6 shows conventional DLTS spectra obtained from the sputter-deposited Au/GaN/Al SBDs before and after annealing between 450 K and 550 K. As a rough approximation for DLTS, $N_T \approx 2N_d\Delta C/C$, where N_T is the defect concentration, N_d is the carrier concentration, ΔC is the change in capacitance and C is the capacitance. Therefore, $2N_d\Delta C\ /C$ is plotted on the vertical axis. The values for C and N_d (at -2 V bias) were taken from room-temperature *C-V* measurements, which are close enough to the temperature at which the DLTS peak was observed, to be reasonable approximations. Owing to the large change in carrier density (and subsequent change in capacitance), the region probed by the DLTS measurements differed from one sample to the other.

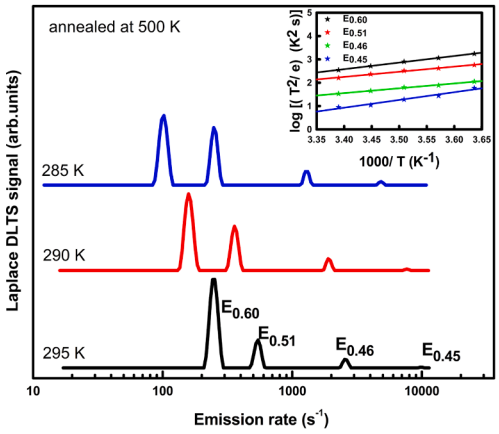
For the unannealed SBD, a broad asymmetric peak was detected at approximately 265 K, similar to that observed by V.R. Reddy et al. [1]. The asymmetry suggests that this peak is most likely composed of more than one defect. The capacitance transient should consequently be composed of several emission rates.

a. Annealing at 450 K led to a decrease in the peak intensity, indicating a reduction in the defect concentration by approximately 34% relative to the unannealed sample. The peak also shifted to 246 K, suggesting that deeper defect levels had annealed out, leaving primarily shallower states.
b. Annealing at 500 K caused an increase in the trap concentration to 58% of the as-grown peak height, accompanied by a shift of the peak to 262 K.
c. Annealing at 550 K resulted in a further decrease in the peak height to 43% of the original trap concentration, along with an additional upward shift of the peak position to 275 K.

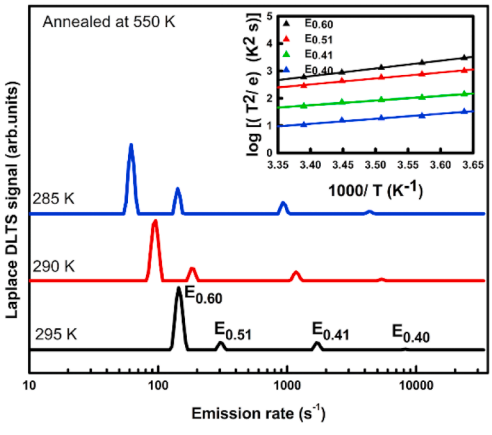
Since the carrier concentration changes after each annealing stage, the depth probed by DLTS also varies. After annealing at 550 K, the probed depth is significantly greater than that for the 450 K- and 500 K-annealed samples, which exhibit similar carrier concentration profiles. Therefore, the decrease in peak height observed after 550 K annealing could partly be attributed to a concentration gradient of the defects,



(a)



(b)



(c)

Fig. 8. Laplace DLTS spectra of Au/GaN/Al SBDs annealed at (a) 450 K, (b) 500 K, (c) 550 K, measured at -2 V reverse bias, 2 V pulse, and 1 ms width. Insets show Arrhenius plot of the detected defects.

decreasing with depth. A similar effect may occur after the 450 K annealing stage; however, because the change in carrier concentration is small, its impact is expected to be much less pronounced.

Overall, annealing modifies both the nature and the concentration of defects present in the GaN films. The DLTS peaks in all spectra, except for the sample annealed at 450 K, exhibit asymmetry, suggesting that the peaks arise from multiple defect states.

When DLTS is used, an electrically active defect is usually characterized in terms of its apparent capture cross section and activation energy, commonly referred to as its DLTS signature. The electron emission rate as a function of temperature is given by [38]:

$$e_n(T) = \sigma_n \langle \nu_n \rangle \frac{g_0}{g_1} N_c T^2 exp\left(-\frac{E_c - E_t}{k_B T}\right). \quad (9)$$

where σ_n is the apparent capture cross section, $\langle \nu_n \rangle$ is the average thermal velocity of the electrons, g_0/g_1 is the relative degeneracy of the defect before and after emission, N_c is the density of states in the conduction band, T is the temperature, and $E_c - E_t$ is the activation energy of the trap. The activation energy and apparent capture cross-section of the observed defects were determined from the slope and y-intercept of $e_n(T)/T^2$ versus T^{-1}, respectively. For each defect, Arrhenius plots are shown as inserts.

It should be noted that high electric fields within the depletion region can enhance electron emission rates from deep traps through field-assisted tunnelling or Poole-Frenkel effects, potentially causing shifts in the activation energies or emission rates observed in DLTS and Laplace DLTS. In our study, the reverse biases applied during DLTS measurements were limited to -2V producing an electric field equivalent to that used by Markevich et al for their low field limit [39].

Fig. 7 shows the Laplace DLTS spectra of the unannealed sputter-deposited SBD recorded at 285 K, 290 K and 295 K for the peak detected at 265 K in the conventional spectrum. These measurements used a reverse bias of -2 V and a filling pulse of 2 V with a pulse width was 1 ms. As expected, the asymmetric peak was resolved into multiple defect components with activation energies of 0.60 eV, 0.58 eV, 0.57 eV, and 0.56 eV in the as-deposited sample. The emission rates associated with each component increased systematically with temperature, confirming that the algorithmic separation of the peak into four constituents is reliable.

Interestingly, as shown in Fig. 8(a), upon annealing at 450 K, the conventional DLTS peak, apart from shifting downward in temperature, also displayed good symmetry, suggesting more closely spaced components. In agreement with this observation, the Laplace DLTS resolved only one peak, with an energy level of 0.52 eV. We therefore conclude that all the peaks except $E_{0.58}$ annealed out at 450 K. The slight discrepancy in the energy levels is probably due to the influence of the other nearby peaks. Fig. 9 compares the Laplace DLTS spectra recorded at 290 K after each annealing stage, clearly showing that $E_{0.52}$ and $E_{0.58}$ are observed at similar temperatures, providing further evidence that they are related to the same defect.

After annealing at 500 K, a set of four distinct peaks were present, as shown in Fig. 8(b) and listed in Table 2. The different positions on the Laplace DLTS spectrum, as shown in Fig. 9, indicate that these peaks are not related to the earlier peaks. We therefore conclude that these peaks are due to defects that diffuse from the interface. Annealing at 550 K leads to yet another set of four defects, as shown in Fig. 8(c). A comparison of the peak positions in Fig. 9 reveals that the peaks observed after annealing at 550 K are like those observed after annealing at 500 K. This shift could be explained by the lower carrier density after annealing at 550 K reducing the electric field in the depletion region, consequently shifting the peaks to lower emission rates.

The defects observed in this study have DLTS signatures similar to those in the literature [37,40–42]. More recently, theoretically and experimentally, this defect has been attributed to Fe_{Ga} acceptor state by D. Wickramaratne, et al. [43], M. Horita et al. [44] and P. Kruszewski et al. [45].

The results obtained from the *I-V, C-V* and DLTS measurements reveal that the defect states identified by DLTS are closely linked to

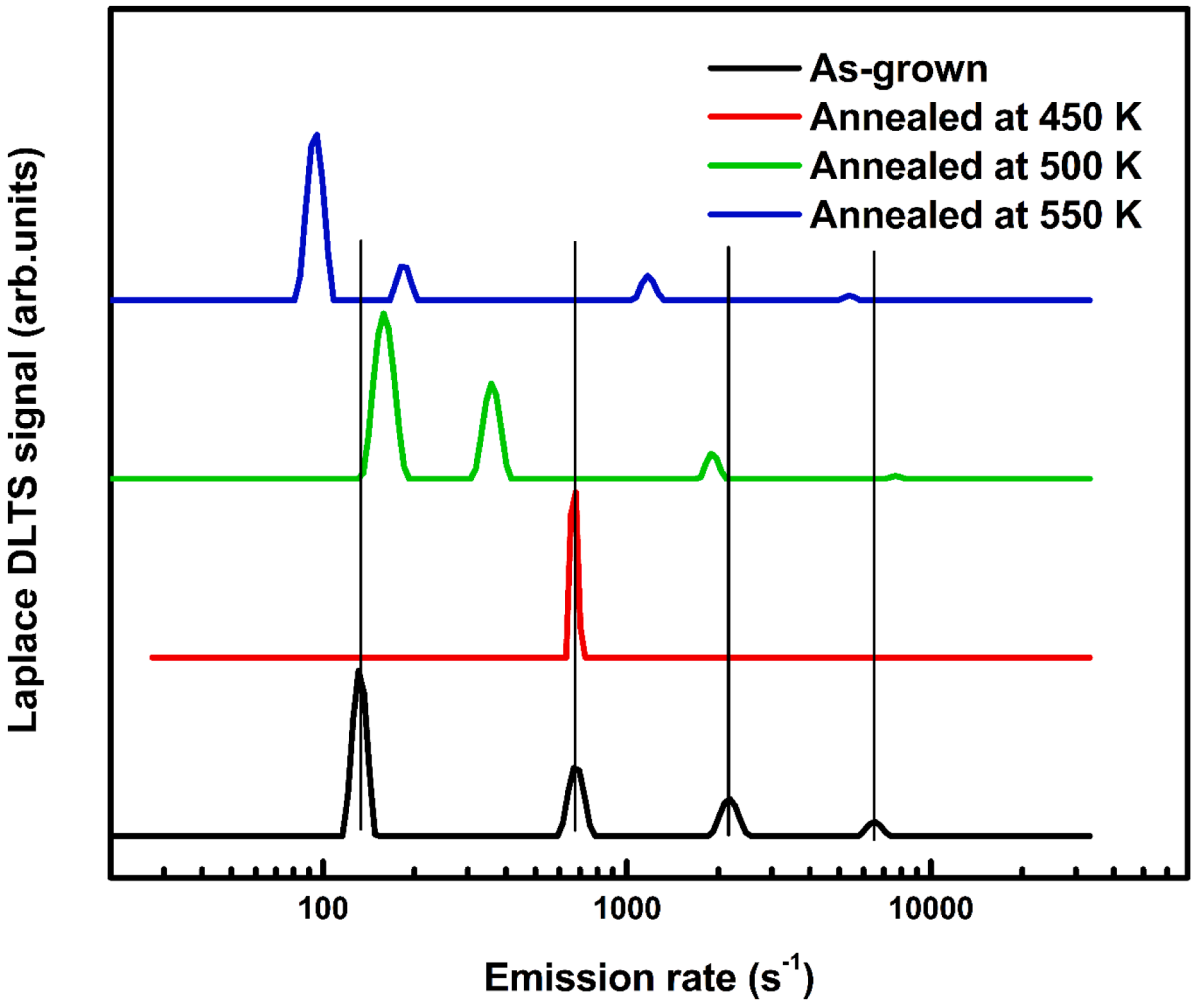


Fig. 9. Laplace DLTS spectra at 290 K obtained from the sputter-deposited Au/GaN/Al SBDs for all annealing stages.

variations in series resistance (*Rs*) and barrier height (Φ_b) obtained from *I-V* and *C-V*. The change in charge transport properties, reflected in N_d - N_a from *C-V,* aligns with trap levels detected in DLTS, indicating the influence of deep-level defects on carrier dynamics. Furthermore, annealing significantly alters defect states, leading to a marked shift in both deep-level and electrical characteristics.

This comprehensive relationship provides valuable insight into how defect states affect the overall electrical performance of a material.

The activation energies associated with each peak and their details are listed below in Table 2.

4. Conclusion

GaN thin films were synthesized on Si (111) substrates via electrochemical deposition. X-ray diffraction (XRD) confirmed the polycrystalline nature and hexagonal wurtzite structure of the GaN thin films. Scanning electron microscopy (SEM) and atomic force microscopy confirmed that the layers were continuous. Au Schottky barrier diodes were fabricated by sputtering Au on top of a 10 nm, resistively evaporated circular dot. The *I-V* and *C-V* results indicate that the ideality factor increased with increasing annealing temperature to 500 K but improved substantially upon annealing at 550 K. The barrier height remained approximately constant (0.58 - 0.56 eV) upon annealing at 450 K and 500 K. However, annealing at 550 K resulted in a ~14% increase in ϕ_b. Notably, the series resistance increased with increasing annealing temperature, most likely due to changes in the morphology and composition of the thin film in the near-surface region [33]. The *C-V* results revealed that the carrier concentration of the samples was inversely correlated with the annealing temperature. The *C-V* depth profiles suggest that the free carrier concentrations of these films are nonuniform and decrease sharply away from the surface region. Similar observations were made for all the layers for which the SBDs were resistively evaporated [12,28]. In conclusion, DLTS measurements revealed an asymmetric peak that could be split into four peaks by Laplace DLTS. After annealing, all but one of the components anneal at 450 K, where only a single peak is observed. This leads to the lowest defect concentration in the system. Annealing at 500 K introduced a set of 4 defects that differ from previously observed defects. After annealing at 550 K, the peak seemed to shift to a lower emission rate. A possible explanation would be a reduction in the electric field due to the lower carrier density.

CRediT authorship contribution statement

A.I.A. Ali: Writing – original draft, Software, Methodology, Investigation, Formal analysis, Conceptualization. **F. Taghizadeh:** Writing – original draft, Software, Methodology, Investigation, Formal analysis, Conceptualization. **P. J. Janse van Ransburg:** Software, Methodology, Investigation, Formal analysis. **W.E. Meyer:** Writing – review & editing, Supervision, Project administration, Investigation, Funding acquisition. **J.M. Nel:** Writing – review & editing, Supervision, Project administration, Investigation, Funding acquisition. **A. Venter:** Writing – review & editing, Supervision, Project administration, Investigation.

Table 2
Electronic properties of the sputter-induced defects in GaN before and after annealing.

This study				Similar defect observed in literature		
Sample	defect	E_a (eV)	σ_a (cm^2)	E_a (eV)	σ_a (cm^2)	Refs.
Resistive sample				$E_{0.32}$ = 0.32	1.9×10^{-17}	[12]
Sputtered sample	$E_{0.60}$	0.60	5.4×10^{-14}	Ec −0.61	9.5 × 10^{13}	[46]
	$E_{0.58}$	0.58		A_5 = 0.59		[47]
	$E_{0.57}$	0.57	2.0×10^{-13}	A_5 = 0.59	9.0×10^{-16}	[47]
	$E_{0.56}$	0.56		A_5 = 0.59		[47]
			5.0×10^{-13}		9.0×10^{-16}	
			6.6×10^{-13}		9.0×10^{-16}	
Annealed at 450 K	$E_{0.52}$	0.52	1.9×10^{-14}	A_5 = 0.59	9.0×10^{-16}	[47]
Annealed at 500 K	$E_{0.60}$	0.60	1.1×10^{-13}	Ec −0.61	9.5 × 10^{13}	[46]
	$E_{0.51}$	0.51		A_5 = 0.59		[47]
	$E_{0.46}$	0.46	7.0×10^{-15}	E_{T1}= 0.41	9.0×10^{-16}	[48]
	$E_{0.45}$	0.45				[48]
			5.2×10^{-15}	E_{T1}= 0.41	2.6×10^{-17}	
			1.5×10^{-14}		2.6×10^{-17}	
Annealed at 550 K	$E_{0.60}$	0.60	2.4×10^{-14}	Ec −0.61	9.5 × 10^{13}	[46]
	$E_{0.51}$	0.51		A_5 = 0.59		[47]
	$E_{0.41}$	0.41	5.0×10^{-15}	E_{T1}= 0.41	9.0×10^{-16}	[48]
	$E_{0.40}$	0.40				[48]
			3.7×10^{-16}	E_{T1}= 0.41	2.6×10^{-17}	
			8.4×10^{-16}		2.6×10^{-17}	

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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