Hot Carrier Degradation of Mixed-mode Polysilicon Light Emitting Diodes

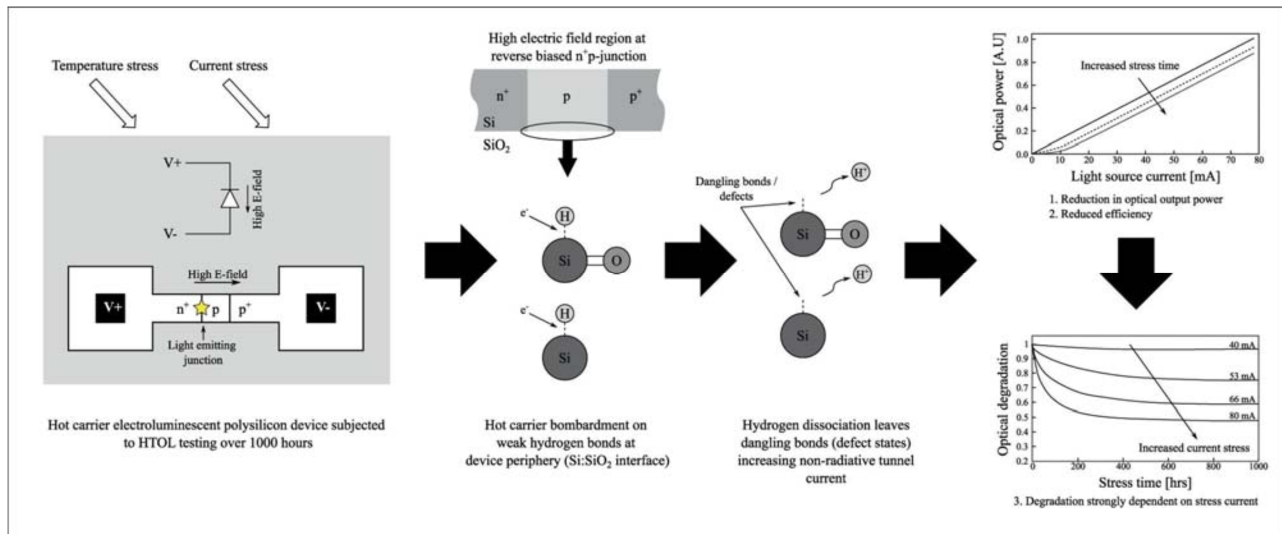
Marius E. Goosen[1,2,3], Petrus J. Venter[3], Nicolaas M. Fauré[3], Promise N. Msomi[3], Johan Schoeman[2], and Trudi-H. Joubert[2]

1. Corresponding author. Email: u04294106@tuks.co.za Phone: +2782 571 9346.
2. Department of Electrical, Electronic and Computer Engineering, University of Pretoria. Lynnwood road, Hatfield, Pretoria, 0063.
3. INSiAVA (Pty) Ltd. 19 Frikkie de Beer Street, Garston AH, Pretoria, 0063.

Highlights

- Mixed-mode polysilicon light emitting diode manufactured in standard 0.35 µm CMOS.
- Hot carrier degradation is noticed, caused by hydrogen dissociation in high E-field.
- Increased non-radiative tunneling is shown due to increased defect states.
- Degradation is strongly dependent on the stress current/hot carrier bombardment.

Graphical abstract



Abstract

This paper investigates the degradation and reliability of polysilicon light emitters implemented in a standard 0.35 μm CMOS process. A total of 48 identical hot carrier electroluminescent emitters were subjected to high temperature operating life tests. The results show the first reported degradation in reverse biased silicon light emitter intensity, consistent with hot carrier degradation. The degradation is shown to be strongly dependent on the stress current, while little to no dependence on temperature stress is noticed. With the device operating in a mixed-mode regime, it is postulated that hydrogen dissociation and generation of interface states through hot carrier stress increases the non-radiative tunnelling mechanisms reducing the optical intensity with increased stress. Degradation model parameters are extracted to predict light emitter lifetime and to provide long life design criteria for these polysilicon light emitters.

Keywords

Avalanche light emitting diodes, Hot carrier degradation, Hydrogen migration model, Silicon electroluminescence, Silicon light emitting device, Reliability.

I. Introduction

LIGHT emission from silicon has been a topic of much research since it was first noticed in 1955 [1]. Achieving an efficient light emitter in silicon has been called the holy grail of silicon photonics due to its integration potential and excellent spectral overlap with detection in silicon [2]. It remains paramount that standard manufacturing technologies are used for implementation and integration of systems containing silicon light emitters to capitalize on the vast investment made in silicon manufacturing technologies world-wide [3]. Target optical systems for complete CMOS integration include microdisplays [4], opto-isolators [5] and biosensors [6].

Silicon emitters based on avalanche electroluminescence remain inefficient due it's an indirect bandgap. Polysilicon as light emitting material was recently introduced in a CMOS-compatible process to improve the generation efficiency [7-9]. These devices make use of the additional defect centres present in the polysilicon material to enhance the efficiency. These devices showed a 2× factor of improvement in external power efficiency (EPE) compared to three-terminal devices presented in [10].

Only a few authors have studied the effect of degradation on silicon light emitters operating under high field conditions [11-14]. These authors agree that no clear net reduction in optical intensity is present after stressing. The hydrogen migration model (the formation of B-H complexes) has been

postulated to qualitatively explain the change in emission profiles noticed [11-14].

The degradation and operating life of polysilicon emitters need to be carefully considered and evaluated due to the introduction of additional defects states in the form of Si:SiO_2 interface and grain boundary states. Hot carrier degradation (HCD) has been shown to degrade polysilicon bipolar transistors, changing the base-emitter junction characteristics [15].

This work is motivated by the need to determine and understand the extent to which the possible efficiency improvement gained through defect centre exploitation, deteriorates the polysilicon light emitter performance over time. It is hypothesised that the hydrogen migration model cannot solely account for the degradation of polysilicon light emitters, and that the generation of interface states due to Si-H dissociation increases the non-radiative tunnelling component, degrading the light emitter performance over time.

II. Theory on HCD in Polysilicon *PN*-Junctions

HCD has been widely investigated in polysilicon-on-insulator MOSFETs [16-17] and polysilicon emitter BJTs [15][18] as a source of degradation that reduces the performance of the devices over time. In general, there are two main sources of the degradation due to hot carrier stress, 1) charges trapped in the oxide close to the metallurgical junction and 2) breaking of weak bonds at the Si:SiO_2 interface.

A. *Trapped charges in the oxide*

When the carriers are accelerated by the electric field in the depletion region, they attain sufficient energy to be injected into the field oxide via tunnelling. These "slow" states change the surface potential and the tunnelling and avalanche current along the perimeter of the device [19-20].

The accumulation of charge near the metallurgical junction shifts the localized breakdown point further from the device surface, increasing the depletion region width and the resulting reverse voltage (V_R). This effect reduces over time as the breakdown region is shifted deeper into the (poly)silicon and fewer carriers close to the device periphery have sufficient energy to tunnel into the oxide. At this point the trapping and releasing of electrons are in thermal equilibrium [21]. In this work, junction formation through ion-implantation and Boron out-diffusion from the *p*-region will shift the junction deeper into the polysilicon material, reducing the carrier energy at the surface before any stress is applied. The effect of junction walkout (the drift in V_R) is therefore unlikely to contribute significant degradation or change in junction characteristics in this work.

B. *Breaking of weak interface bonds*

In the processing of silicon devices and the formation of thermal oxides, hydrogen is readily available [22]. The available hydrogen by-products (from wet oxidation and pyrolyzing of silane to form polysilicon), as well as intentionally introduced hydrogen, bond and passivate the dangling Si bonds at the Si:SiO_2 interfaces and polysilicon grain boundaries.

These weak Si-H and SiO-H are bombarded by hot carriers when placed under high-field conditions, dissociating the hydrogen. The dissociated H^+ ions are free to diffuse within the device to either re-passivate newly formed defect states or to form new bonds such as B-H complexes (hydrogen bond model). The hydrogen ions will continue to diffuse away from the high field region with increased stress time.

The effect of the formation of B-H complexes was first introduced by [23-24] and results in a decrease in the acceptor doping concentration. Lowering the doping concentration of the *p*-type region will increase the V_R for devices with no field stop region to terminate the electric field. This drift in V_R was shown in [23] to be strongly temperature dependent. With the introduction of the field stop region [25], as is also done in this work, the V_R can be shown to reduce with decreased doping concentration due to the fixed location of the field stop region.

The complete encapsulation of the polysilicon light emitter in SiO_2 as introduced in this work, confines the dissociated hydrogen ions to within the thin polysilicon layer. Therefore, the hydrogen ions can only diffuse laterally, most likely compensating the p^+ field stop region with increased stress time. This will have little effect on the junction characteristics due to high p^+ doping concentration.

Although the temperature dependent hydrogen bond model (the formation of B-H complexes) cannot be completely discounted, it is postulated that the most likely source of degradation is the interface / defect states that remain due to the hydrogen-bond dissociation. These mid-band defects left behind after hydrogen dissociation and diffusion out of the high field region may introduce a trap-assisted tunnelling (TAT) current, in addition to the existing direct tunnelling current associated with operating voltages below $4E_g/q$ and in the transition region below $6E_g/q$ [25].

The rate of degradation is expected to decrease as the finite number of hydrogen bonds are depleted over time. Hydrogen dissociation and formation of defect states are expected to follow the form of a decaying exponential [25]. The same decaying exponential will also govern the reformation of B-H complexes. The decreased rate of degradation with stress time is confirmed in this work. The rate of interface state generation (dN_{it}/dt) can be expressed as [19]:

$$\frac{dN_{it}}{dt} = K(N - N_{it})J_{st}exp\left(-\frac{\varphi_{it}}{kT_e}\right) - \frac{BX_H}{D_H}N_{it}\frac{dN_{it}}{dt} \qquad (1)$$

where K and B are fitting constants, N is the total number of states that can be generated, N_{it} is the number of created states, J_{st} is the stress current density, φ_{it} is the critical energy required to induce bond breakage, k is the Boltzmann constant, T_e is the electron temperature estimated using an approximation based on the electric field and the scattering mean free path, and D_H and X_H are the effective diffusion coefficient and effective diffusion length of hydrogen, respectively.

The first term in equation (1) depicts the rate of state generation dependent on the stress current density and electron temperature. It is later shown in this work that the degradation rate is a strong function of stress current density. The second term in equation (1) depicts the healing due to formation of Si-H bonds from diffusive hydrogen (re-passivation of the dangling Si bonds). The reduced rate of degradation over time may be explained by 1) the interplay between the first (generation) term and second (healing) term in equation (1), and 2) the decaying number of bonds that are dissociated (N-N_{it}).

III. Methodology

A. Polysilicon light emitting devices

The polysilicon light emitters implemented in this work utilises electric field reach-through to maintain an operating voltage below 5 V, forcing the device to operate in a mixed-mode region with competing tunnelling and avalanche breakdown mechanisms [4].

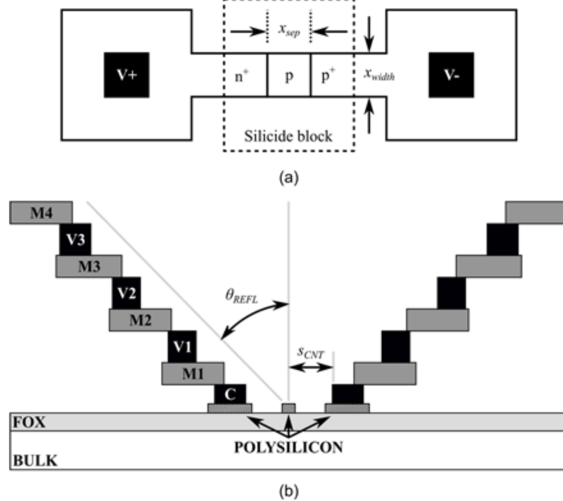


Fig. 1. Light emitter used for degradation and reliability analysis. (a) Polysilicon light emitting finger device. (b) Circular BEOL reflector used to direct the generated light to exit the chip surface.

Fig. 1 (a) depicts the implemented light emitter, with Fig. 1 (b) illustrating the cross-sectional view of the circular back-end-of-line (BEOL) reflector implemented to achieve a repeatable emission angle of 18.78±1.94° (sample size = 10 devices) and improve the light extraction efficiency.

The light emitter design parameters, x_{sep} and x_{width}, and the reflector design parameters, θ_{REFL} and s_{CNT}, are presented in Table 1. The light emitter design parameters were chosen based on the outcomes of an empirical study. The reflector design parameters were determined through a subsequent empirical study making use of the chosen emitter design from the first study and altering only reflector design parameters. The outcomes, properties and performance of the devices from the empirical studies are out of scope for this work and will be reported elsewhere. The best light emitter from the empirical studies was chosen for the degradation and reliability studies.

The single element emitter, together with a circular BEOL reflector, forms the fundamental building block with which a 1024 element parallel array was constructed.

The light emitting array was designed to be safely stressed with a DC current of up to 80 mA, with a typical operating current of 40 mA. The metal layers used to convey the stress current to the light emitting array were overdesigned by taking the foundry electromigration rules into account to isolate the degradation to only the light emitting array.

B. Experimental setup

A stress current and temperature stress were applied to the devices due to the unknown nature of the expected degradation of the polysilicon light emitters. The high temperature operating life (HTOL) tests were carried out according to the JEDEC standardized test method for temperature, bias and operating life [26]. The test parameters used are summarized in Table 2.

A total of 48 devices located on 24 chips were stressed at 12 unique stress points (4 stress current points and 3 stress temperature points). The DC stress currents were applied to each light emitting array using calibrated current sources.

Table 1. Design parameters of the light source and BEOL reflector used in the reliability study

Parameter	Symbol	Value
Separation distance	x_{sep}	200 nm
Finger width	x_{width}	650 nm
Reflector angle	θ_{REFL}	30 °
Contact spacing	s_{CNT}	2.25 µm

Table 2. Test parameters used in the HTOL tests

Parameter	Value
Number of elements	1024
Temperature stress conditions (N_T = 3)	100, 125, 150 °C
Current bias stress conditions (N_I = 4)	40, 53, 66, 80 mA
Unique stress points	$N_S = N_T \times N_I = 12$
Sample size	$4 \times N_S = 48$
Devices per chip	2
Number of chips tested	24
Measurement intervals (t_{stress})	0, 12, 36, 60, 84, 132, 196, 340, 508, 746, 1010 hours
Failure threshold	20% degradation in intensity

The temperature stress was applied using calibrated temperature-controlled ovens, accurate to within ±1 °C from the setpoint. The applied current and temperature stress were removed at the specified intervals, and its electrical and optical characteristics were determined, in accordance with the JEDEC standardised test method [26].

C. Analysis methods

In order to investigate the lifetime of the polysilicon emitters and to ascertain the dependence on applied stress conditions, Black's equation, conventionally used for failure modelling due to electromigration, was used to determine the mean time to failure (*MTTF*) [27],

$$MTTF = \frac{A}{J^N} exp\left(\frac{E_A}{kT}\right) \quad (2)$$

where, J is the stress current density, k the Boltzmann constant (8.617×10^{-5} eV/K), T the temperature (in K), E_A the activation energy (in eV), N a model parameter, and A a scaling constant. This equation is identical to the Eyring model for *MTTF* due to HCD in *n*-channel MOSFETs [28]. Two dataset types may be extracted using the presented experimental setup to distinguish the effect of applied current and temperature stress from each other. Taking the natural logarithm on both sides, the parameters N and E_A may be extracted by using datasets of constant temperature and constant current [29].

The polysilicon light emitter used in this work operates in the reach-through regime, where an EPE trade-off is introduced by weighing the operating voltage against the optical output power. However, reducing the operating voltage below $6E_g/q$ causes non-radiative field emission or tunnelling to be more pronounced [25]. When operating the emitters below this threshold voltage, the tunnelling and avalanche mechanisms compete for available carriers, hence operating in the so-called mixed-mode regime. Three methods will be used to investigate and quantify the change

in junction characteristics due to the shift in dominance between the tunnelling and avalanche mechanisms.

The first method used to investigate the mixed-mode operation is based on the assumption that only the linear avalanche current component (due to impact ionization) contributes to the measurable light emission [30]. The light generating current in the linear region (at higher operating currents) is extrapolated back to lower operating currents, from which the non-linear tunnel current may be extracted.

The second method used to investigate junctions operating in a mixed-mode regime is presented in [30-31]. This method determines the dynamic impedance of the device, $R = dV/dI$, to show the asymptotes of the dominant tunnelling and avalanche currents. The result of this illustration is a clear depiction of the transition between tunnelling dominant (low voltage, low current) and an avalanche dominant (high voltage, high current) operation. The asymptote that depicts the dependence of the dominant tunnel resistance (r_T) on the tunnel current (I_T) is expressed as [30]:

$$r_T = C_T {I_T}^{m_T} \tag{3}$$

where the model fitting parameters m_T and C_T may be extracted. The same equation is also used to extract the asymptote fitting parameters for the avalanche dominant current.

The last method utilised to investigate the mixed-mode junction's breakdown mechanisms entails a look into the change in the temperature coefficient (TC) of the light emitting device's electrical characteristics. Tunnelling is well-known to have a negative TC (in mV/°C), with avalanche having a positive TC [25].

IV. Results and Discussion

Fig. 2 shows the mean degradation in optical output power, measured at a stress temperature of 150 °C, over the total stress time of 1010 hours for different applied stress currents (I_{stress}).

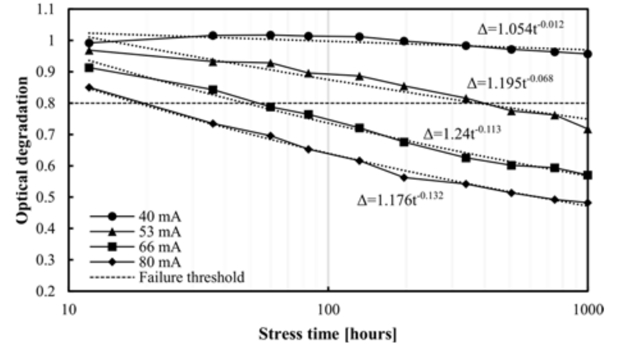


Fig. 2. The optical degradation of the polysilicon light emitters stressed at 150 °C, over the total measured stress time for the different applied stress currents. Power law fitted time dependence of degradation is shown. Sample size = 4 at each stress current.

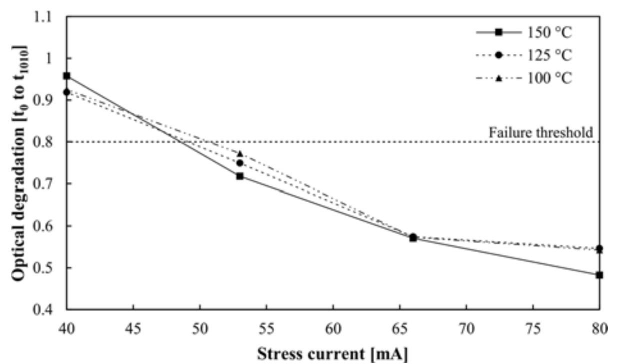


Fig. 3. The absolute optical degradation (from t_0 to t_{1010}) of the polysilicon light emitters at different applied stress current and stress temperatures (sample size = 4 at each stress temperature).

A failure threshold of 20% optical degradation from pre-stress performance is set to allow for lifetime extrapolation and model parameter extraction. Fig. 3 shows the mean

degradation in optical output power from t_0 (0 hours) to t_{1010} (1010 hours) at different applied I_{stress} and stress temperatures (T_{stress}), not to be confused with stress time, t_{stress}.

Three key traits are noticed from Fig. 2 and Fig. 3: 1) a strong dependence of the rate and absolute optical intensity degradation on the I_{stress}, 2) no clear dependence of the degradation on T_{stress} and 3) the rate of degradation decreases with increasing t_{stress} (linear dependence of degradation with $\log(t_{stress})$), with half of the degradation occurring in the first 60 hours.

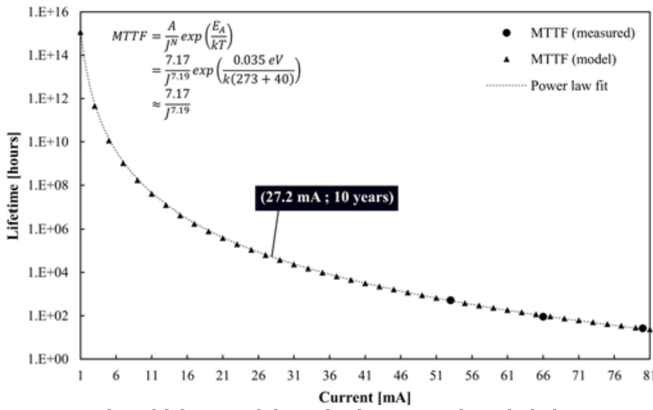


Fig. 4. Predicted lifetime of the polysilicon mixed-mode light emitters showing a maximum allowable bias current of 27.2 mA for a 10-year field life at a typical operating temperature of 40 °C.

The first trait is noticeable in Fig. 2 as a change in time dependence with I_{stress} (change in straight line slope with I_{stress}). This power law-like time-dependence has exponent values ranging from -0.012 to -0.132 for 40 mA to 80 mA stress currents, respectively. The remainder of this section is devoted to further explaining these three findings.

The possible increase in performance noted in Fig. 2 within the first 100 hours for I_{stress} = 40 mA fall within the accuracy of the current optical test setup (< 2.8%). This effect does however warrant a future investigation with an improved measurement setup.

A. Lifetime model and stress dependence

The extracted lifetime model parameters from equation (2) were determined as (E_A, N) = (0.035 eV, 7.19). These values show a weak dependence on temperature (low E_A value) and a strong dependence on stress current (high N value). The lifetime model based on the extracted model parameters is presented in Fig. 4. It shows the stress current that may be applied (at 100% duty cycle) to maintain the required performance level (less than 20% degradation in optical output power) over time at a typical operating temperature of 40 °C. The model closely matches that of a basic power law due to the high N and low E_A values. The E_A of 0.035 eV reduces the *MTTF* by ~10% due to an increase in temperature from 100 °C to 150 °C.

B. Temperature dependence of HCD

The temperature dependence of the degradation due to increased interface state generation as described in [19] is not seen in this work. From the first term of equation (1) the T_e is expected to introduce a noticeable temperature dependence of the degradation due to its exponential relationship with defect state generation. The maximum T_e value was calculated to be more than 3000 K for a device operating in strong avalanche [32], with the lattice temperature (at room temperature operation and no significant self-heating) approximately 10% of the electron temperature. This dependence of T_e on the lattice temperature or T_{stress} was not seen in this work. However, it was shown in [33] that the

temperature dependence of HCD is significantly more intricate than this and depends on the bond breakage mechanisms at play, the stress temperature as well as the operating voltage. Therefore, the model presented in equation (1) does not adequately capture the temperature dependence of interface state generation.

The Si-H bond breakage may occur through either a multiple-carrier process via multi vibrational excitation (MVE) or a single carrier process via anti-bonding (AB). The rate of the AB process is higher and more dominant at higher temperatures, whereas at lower temperatures the rate of the MVE process is higher and more dominant. The weak Si-H bonds are excited with an increase in temperature, lowering the typical threshold energy of 2.56 eV required for a single carrier bond breakage process, enhancing the AB process.

Scattering rates for surface scattering and electron-phonon interactions, increase at elevated temperatures, depopulating the high energy tail of the energy distribution function (EDF) more efficiently to reduce the rate of bond breakage and interface state generation [33]. At the same time the AB-process rate may increase with temperature due to electron-electron scattering, populating the high energy fraction again. This illustrates the strong interplay between bond breaking mechanisms with regards to temperature dependence of the HCD.

Higher healing and annealing rates at increased temperatures countering the increase in the AB-mechanism were shown to decrease the HCD in n-MOSFETs at 125 °C compared to room temperature operation [34]. The higher stress temperature utilised in this study may therefore suppress the HCD and the temperature behaviour thereof.

At higher operating voltages (and electric field), carriers attain more energy, populating the high energy tail of the electron EDF to increase the probability of single carrier (AB-mechanism) bond breakage. This may explain the increase in absolute degradation noticed at higher stress currents (and voltages). The temperature dependence of HCD, however, was shown in [33] to be dependent on the applied stress voltage. The strong coupling between single-carrier AB and MVE was shown to reduce the temperature dependence of the parameter degradation with increased operating voltage.

Therefore, it is argued that the absence of significant temperature dependence as seen in this work is due to the competing bond breakage mechanisms since the devices were 1) stressed at high temperatures (100, 125 and 150 °C) and 2) stressed at high currents with corresponding reverse voltages in excess of $V_R > 4$ V. A repeat reliability study over a wider temperature range (e.g. 25 °C to 125 °C) may enlighten the interplay between AB and MVE more clearly and provide more information on the temperature dependence of the degradation.

C. Current density dependence of HCD

The strong degradation dependence on stress current seen in this work is consistent with HCD typically associated with parameter degradation in *n/p*-channel MOSFETs, although

the lifetime model parameter, N, is higher than what is reported for n-channel transistors $2 < N < 4$ [28]. This higher N value suggests a narrower distribution of characteristic times for the bond dissociation process resulting from the convolution of the bond dissociation EDF and the carrier EDF. Further research and modelling are required to fully understand and explain the significantly increased N value.

The first term in equation (1) depicts the rate of state generation with a linear dependency on the applied stress current density, J_{st}. This linear dependency of interface state generation on applied stress current density does not translate to a linear performance degradation dependency with applied stress current when considering a mixed-mode light emitter. As shown in the next section, the newly formed interface states introduce more tunnelling, which lowers the junction potential, the electric field, and the electron temperature. This highlights the strong interdependence of the effect of stress current density on interface state generation and the change in junction characteristics.

It should be noted, that an increased I_{stress} also implies an increase in applied voltage stress. At higher reverse voltages, the electric field increases and in turn widens the carrier EDF. This widening of the carrier EDF with increased electric field is modelled in [3]. This widening implies that more, higher energy carriers are available to dissociate the hydrogen bonds. It may therefore be considered that the degradation is not solely dependent on the I_{stress}, but also on the applied voltage stress.

D. Change in junction characteristics

An in-depth look at the device junction characteristics is required to ascertain a clear understanding of the origin of the degradation. The raw measurement data for a light emitter array stressed at T_{stress} = 150 °C and I_{stress} = 80 mA, measured at the different t_{stress} intervals is shown in Fig. 5.

An operating point was arbitrarily chosen as the point at which 10% of the maximum optical output power (at t_0) is achieved to illustrate the change in junction electrical and optical characteristics. This operating point is depicted by the horizontal dotted line in Fig. 5 (a), and the corresponding points marked by '×' in Fig. 5 (b) and Fig. 5 (c).

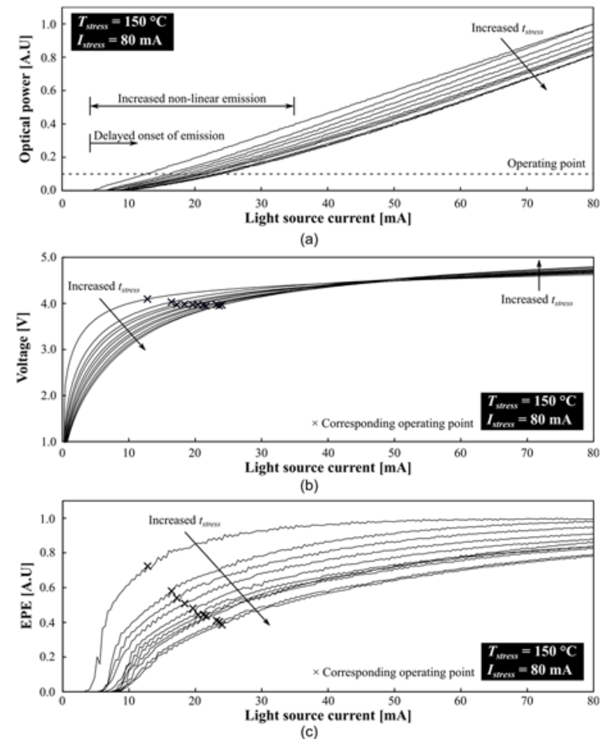


Fig. 5. Measurement data of a single light emitter stressed at T_{stress} = 150 °C and I_{stress} = 80 mA for different t_{stress} intervals. (a) Measured optical output power vs. current. (b) Measured electrical characteristics. (c) Reduction in EPE seen due to light emitter optical output degradation.

An increased non-linear slope in emission at low currents (0 – 40 mA) as well as a delay in the onset of the light

emission with increased stress time is noticed in Fig. 5 (a). This reduces the light generated at the same operating current after the applied stress.

The soft breakdown characteristic noticed in Fig. 5 (b) and the non-linear relationship of the optical output power versus current at low operating voltages in Fig. 5 (a), strongly suggest the presence of increased tunnelling [30]. The reverse voltage, V_R, of between $4E_g/q$ and $6E_g/q$ also indicates that the device is operating in a mixed-mode regime, with competing breakdown mechanisms of tunnelling and avalanche [25]. The light output becomes measurable (> 10 pW, when measured with a calibrated radiometer) with 3 V < V_R < 4 V, which corresponds well with the minimum value determined for the onset of impact ionization [30]. Fig. 5 (c) shows the effect that the reduction in light emission at the same operating current has on the EPE of the emitter.

At low operating voltages, the leakage current increases by more than a factor x10 with increasing t_{stress} (from Fig. 5 (b), at V_R = 2 V the leakage current increases from 200 μA to 3.6 mA for t_0 to t_{1010}). Although not shown here, the amount of leakage current at low voltages was also determined to be a strong function of applied I_{stress}, inline with the increased degradation noticed. An increased leakage current was reported in diodes after applying high temperature reverse bias (HTRB) stress [35]. The increase in the leakage current was attributed to conventional carrier generation-recombination in the diode body as well as tunnelling due to surface traps (band-to-band tunneling and band-to-defect tunneling) which are activated due to HTRB stress. An increased leakage current was also shown for devices manufactured with an intentional higher defect density [36]. It is therefore postulated that additional traps / defect sites are activated with increased I_{stress} and t_{stress} due to dissociation of weak hydrogen bonds, increasing the tunneling mechanisms. The increased contribution of tunneling is discussed next.

Field emission or tunnelling has been argued to be non-radiative in nature since the tunnel carriers due to direct tunnelling do not undergo band-to-band energy shifts [30]. A carrier may, however, tunnel into the high field region and be swept up by the high electric field if the depletion region width is larger than the carrier tunnelling distance.

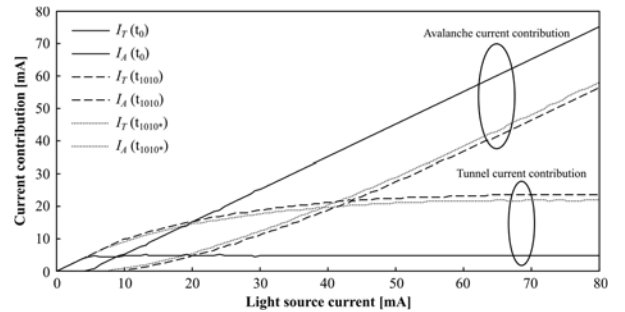


Fig. 6. Extracted tunnel and avalanche current using the method presented in [36] for unstressed (t_0), stressed (t_{1010}) and after-recovery devices (t_{1010*}). Data from the light emitter used in Fig. 5.

These swept up carriers may then proceed to impact ionize if the minimum threshold energy is reached and generate photons in subsequent transition and recombination events.

Therefore, it is hypothesized that an increase in non-radiative tunnelling takes place with increased stress. The suspected increased amount of non-radiative tunnelling with increased stress may explain the reduction in optical output power, the softer breakdown characteristic, the non-

linear light generation characteristic, and the delay in the onset of emission. The three methods introduced earlier to examine the mixed-mode junction breakdown are used to investigate this hypothesis. Fig. 6 shows the extracted tunnel and avalanche currents for unstressed (t_0), stressed (t_{1010}) and after-recovery (t_{1010*}) devices in accordance with the first method introduced [30].

Fig. 6 shows a 390% increase in the tunnel current component (increasing to 18.8 mA from 4.8 mA) with increased t_{stress}, reducing the avalanche current component responsible for the radiative mechanisms.

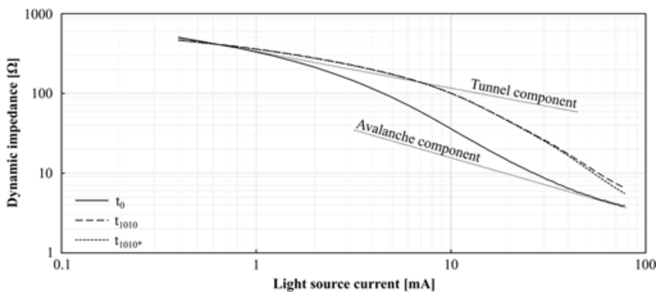


Fig. 7. Dynamic impedance versus reverse current for unstressed (t_0), stressed (t_{1010}) and after-recovery (t_{1010*}) devices. Data from the light emitter depicted in Fig. 5.

The reduction in operating voltage at lower currents, the delay in onset of light emission and the non-linear light generation at low voltages with increased t_{stress} are therefore attributed to an increase in tunnelling or field emission, with TAT the most likely candidate. Stressed devices which show partial recovery after being stored at room temperature for several months are also shown (t_{1010*}) and will be discussed later.

The dynamic impedance method [30-31] introduced earlier is used to show the transition from tunnel dominant to avalanche dominant regions for a non-stressed device (t_0) and a stressed device (t_{1010}), as illustrated in Fig. 7. The stressed device (t_{1010}) starts this transition from tunnelling to avalanche dominant regions only at higher operating currents, manifesting as a delayed onset of impact ionization.

The constants for the asymptotes in both the tunnelling dominant and avalanche dominant regions are extracted by using equation (3). Tunnelling dominant fitting values of $(C_T\,;\,m_T) = (14\text{ V}; -0.46)$ have been extracted from the measured data. The value of m_T is higher when compared to the silicon diode of [31]. The additional tunnelling mechanisms involved, as well as the difference in junction profiles between this work and [31], may justify the difference in m_T. The avalanche dominant fitting parameters of $(C_A\,;\,m_A) = (0.67\text{ V}; -0.7)$ have also been extracted using equation (3). The m_A value of -0.7 is larger than the ideal value of $m_A = -1.02$ determined for diffused junctions [31]. This is expected since the device still operates well below the $6E_g/q$ threshold at the maximum current of 80 mA, indicating that tunnelling is still involved and not completely avalanche dominant. Therefore, the m_A value does not capture a pure avalanche dominant region relationship where r_A is expected to be inversely proportional to I_A with an m_A value close to -1.

Additionally, the dynamic resistance values of more than 100 Ω in the Zener tunnelling region and less than 10 Ω in the avalanche region corresponds well to what was measured in [31]. The increase in operating voltage with t_{stress} at high

currents can be ascribed to the increase in dynamic resistivity, increasing from 3.8 Ω at t_0 to 6.5 Ω at t_{1010}. It is expected that the resistivity should increase due to the generation of additional defects, increasing the amount of scattering events, that in turn increases the effective resistance of the material.

The last method used to validate the hypothesis was to investigate the TCs of stressed and unstressed devices. Fig. 8 depicts the change in TCs for different amounts of applied stress.

For the unstressed device, the competing mechanisms' TCs cancel out at ~63.5 mA, transitioning from the tunnel dominant region into an avalanche dominant region. The stressed devices show more negative TC values and do not reach an equilibrium point within the measurement range.

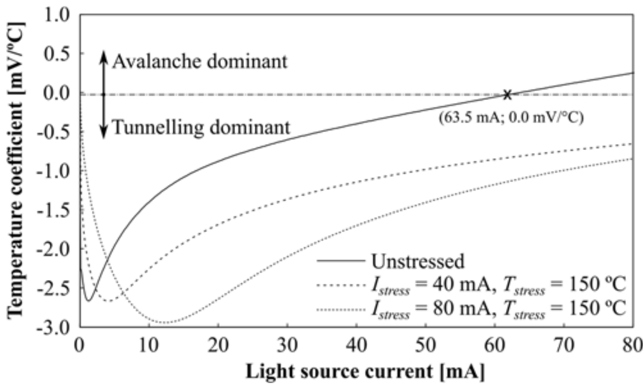


Fig. 8. Temperature coefficients of stressed (t_{1010}) and unstressed (t_0) light emitters showing the increased tunnelling component in the measurement range. Data from three different devices (I_{stress} = 80 mA from Fig. 5).

Comparing the traces with different applied I_{stress} (40 mA vs. 80 mA), also predictably shows an increase in the tunnel current component (more negative temperature coefficient) with higher I_{stress}.

E. Degradation recovery

Partial recovery of the degradation is noticed, presented in Fig. 6 and Fig. 7 (traces marked as 1010 hours*), after devices have been left at room temperature for several months. It is expected that any trapped charge in the oxide may escape over time due to thermal processes (walkout recovery), even if it is not the dominant degradation mechanism due to the absence of a field gradient in the oxide (no field plate). The reduction in charge accumulation close to the metallurgical junction due to recovery causes the surface potential to partially return to the pre-stressed value.

Additionally, the temperature-dependent reformation of Si-H bonds may also be responsible for the partial degradation recovery. As discussed, H^+ ions will diffuse away from the $Si:SiO_2$ interface having a higher concentration of hydrogen.

Table 3. Stress currents and junction properties of comparative work.

Reference	Junction type	Combined junction length (μm)	Stress current per unit length (mA/μm)
[11]	p^+n	47.6	0.21
[12]	n^+p	1500	0.014
[13] – low stress	n^+p	1500	0.016
[13] – high stress	n^+p	1500	0.023
This work	n^+p	665	0.06 – 0.12

This results in less unbound diffusive hydrogen available at the interface to heal the dangling bonds than what was originally created through dissociation under the high electric field, possibly explaining the small partial recovery seen over time. Fig. 7 illustrates a minor earlier transition from the tunnelling dominant region to the avalanche dominant region (less tunnelling, less interface states / defects) for the after-recovery device. Fig. 6 quantifies the recovery by showing a

6.8% reduction in the tunnel current component after recovery.

V. Comparison with Previous Reliability Studies

The most conclusive studies into silicon light emitter degradation to date were performed on the emitter-base junction of a 2N2222 transistor [12-13]. Both studies show changes in the light emission areas and patterns at low stress currents. However, no clear degradation is noticed when considering the total emission intensity. Light coalescence is observed, showing increased emission from certain sites, and diminishing emission at other sites due to the localized nonuniform breakdown along the junction. It was further shown that no light coalescence or degradation in light intensity is noticed at high stress currents [13].

The transistor junction device presented in [12] and [13] may not experience the same dominant degradation mechanism as presented in this work due to its implementation in the Si-bulk with less defects in the vicinity of the high field region. The hydrogen bond model and formation of B-H complexes was postulated to be the dominant mechanism that explains the behaviour of the bulk-based, long length 2N2222 base-emitter junctions.

Another, more recent reliability study was conducted on a p^+n bulk-based silicon light emitter implemented in a 65 nm CMOS technology [11]. No noticeable degradation in total intensity was observed when applying a stress current of 10 mA at 100 °C for 30 hours. The key parameters of this study and the previously mentioned transistor-based studies are depicted in Table 3 in relation to the work presented in this paper.

The studies presented in [12] and [13] did not stress the devices as severely as in this work or as in [11], which may explain why no degradation in optical output intensity was noticed with increased t_{stress} when considering the applied stress per unit length. The stress current used in [11] to stress the p^+n junction is almost double to what was used in this work, therefore suitably high to accelerate degradation due to hydrogen bond dissociation. These p^+n devices are less prone to changing electrical or emission characteristics according to the hydrogen bond model because the B-H bonds cannot form in the low doped *n*-type drift region. The B-H complexes may still form in the p^+ region, but this will not significantly affect the field profile or depletion region provided that the p^+ acceptor doping concentration remains much larger than the *n* donor doping concentration.

Implementing the light emitter in the polysilicon layer of a standard CMOS process causes the emitter to be fully encapsulated in SiO_2, creating additional Si:SiO_2 interfaces compared to equivalent bulk-based devices. This increases the amount of weak hydrogen bonds that can be dissociated from polysilicon devices upon bombardment by the hot carriers. The amount of available hydrogen bonds is further increased due to the presence of grain boundaries in the polysilicon material. Additionally, the Si:SiO_2 interface of bulk-based devices as presented in [11-13], contains fewer defects and weak hydrogen bonds. This bulk-Si:SiO_2 interface is critical for repeatable and reliable transistor

performance in a CMOS process, necessitating thin oxide formation by making use of dry thermal oxides. The reduced Si-H bond availability goes some way in explaining why other authors [11-13] do not see any significant degradation, either from the formation of B-H complexes or the increase in interface states.

Finally, all of the devices presented in [11-13] operate in strong avalanche, with V_R in excess of $6E_g/q$, where the avalanche current is expected to far outweigh the non-radiative tunnelling component even after degradation. This will result in negligible degradation in optical intensity due to an increase in tunnelling current.

VI. Conclusions and Outlook

Degradation in optical output power with increased stress has been noticed in polysilicon light emitters operating in a mixed-mode regime. In this work, a high dependence on stress current and a low dependence on stress temperature on the rate and amount of degradation are shown. The dissociation of hydrogen at the Si:SiO_2 interfaces and the formation of interface states are presented as a plausible mechanism to account for the increased non-radiative tunnelling component, and reduced radiative avalanching current measured in the light emitting devices.

Even though severe degradation has been noticed at high stress currents, a lifetime curve and model are presented allowing the design with polysilicon light emitters with performance over an expected lifetime in mind. The presented polysilicon devices are shown to able to be reliably implemented in a standard 0.35 µm CMOS process for operation at lower current densities, with a 10-year operating life expectancy at a 100% duty cycle current of 27.2 mA for the 1024-element parallel array used in this work.

In this work it is hypothesized that the number of defects or interface states increase due to hot carrier stress. A future investigation into the change in emission spectrum with hot carrier stress at high and low temperatures could possibly show this correlation. It would also be valuable to repeat this work in reciprocal p^+n type polysilicon light emitting devices, although not manufacturable in the 0.35 µm CMOS process utilized in this work.

Although not clearly notice in this work, the effect of time-0 variability or process variations could also be investigated by intentionally altering the design parameters, x_{sep} and x_{width}. These parameters strongly affect the initial amount of tunnelling present in the device operating in electric field reach-through, and may therefore also impact the rate and absolute amount of degradation.

These additional investigations may further reinforce the presented hypothesis that interface state generation due to hot carrier bombardment and the resulting increased tunnelling probability are the dominant mechanisms degrading mixed-mode polysilicon light emitter performance.

VII. Acknowledgement

The authors would like to thank INSiAVA (Pty) Ltd for providing access to equipment, experimental devices and data used to carry out this research.

VIII. Data Availability

The raw/processed data required to reproduce these findings cannot be shared at this time due to legal reasons. This may be provided on request.

References

[1] R. Newman, "Visible light from a silicon p-n junction," *Phys. Rev.,* vol. 100, no. 2, pp. 700–703, 1955.

[2] S. Dutta, V. Agarwal, R. J. E. Hueting, J. Schmitz and A. Annema, "Monolithic optical link in silicon-on-insulator CMOS technology," *Opt. Express*, no. 25, pp. 5440-5456, 2017.

[3] M. du Plessis, P. J. Venter and E. Bellotti, "Spectral characteristics of hot electron electroluminescence in silicon avalanching junctions," *IEEE Journal of Quantum Electronics*, vol. 49, no. 7, pp. 570-577, 2013.

[4] P. J. Venter and M. du Plessis, "A 128×96 pixel CMOS microdisplay utilizing hot carrier electroluminescence from junctions in reach through," *Journal of Display Technology*, vol. 10, no. 9, pp. 721-728, 2014.

[5] L. W. Snyman, H. Aharoni, A. Biber, A. Bogalecki, L. Canning, M. du Plessis and P. Maree, "Optical sources, integrated optical detectors, and optical waveguides in standard silicon CMOS integrated circuitry," *in Proc. SPIE 3953*, Silicon-based Optoelectronics II, 2000.

[6] K. Xu, Y. Chen, T. A. Okhai, and L. W. Snyman, "Micro optical sensors based on avalanching silicon light-emitting devices monolithically integrated on chips," *Optical Materials Express*, vol. 9, no. 10, pp. 3985-3997, 2019.

[7] K. Xu, L. Huang, Z. Zhang, J. Zhao, Z. Zhang, L. W. Snyman and J. W. Swart, "Light emission from a poly-silicon device with carrier injection engineering," *Materials Science and Engineering B*, pp. 28-31, 2018.

[8] H. Sun, K. Xu, J. Zhao, J. Zhang, Y. Zhou, L. Liu, J. Yuan, L. Huang, K. Zhu, L. W. Snyman, K. A. Ogudo, "A dependency of emission efficiency of poly-silicon light-emitting device on avalanching current," *Optical Materials*, vol. 88, pp. 711-717, 2019.

[9] K. Wu, J. Cheng, G. Huang, J. Yuan and K. Xu, "Poly-silicon light-emitting-device based electro-optical interfaces in standard silicon-CMOS integrated circuitry," *Optical Materials*, vol. 102, 2020.

[10] K. Xu, H. Liu and Z. Zhang, "Gate-controlled diode structure based electro-optical interfaces in standard silicon-CMOS integrated circuitry," *Applied Optics*, vol. 54, pp. 6420-6424, 2015.

[11] S. Dutta, G. J. M. Wienk, R. J. E. Hueting, J. Schmitz and A. Annema, "Optical Power Efficiency Versus Breakdown Voltage of Avalanche-Mode Silicon LEDs in CMOS," *IEEE Electron Device Letters*, vol. 38, no. 7, pp. 898-901, 2017.

[12] M. de la Bardonnie, D. Jiang, S. E. Kerns, D. V. Kerns, P. Mialhe, J.-P. Charles and A. Hoffman, "On the aging of avalanche light emission from silicon junctions," *IEEE Trans. on Electron Devices*, vol. 46, no. 6, pp. 1234-1239, 1999.

[13] A. Chatterjee and B. Bhuva, "Accelerated stressing and degradation mechanisms for Si-based photoemitters," *IEEE Trans. on Device and Materials Reliability*, vol. 2, no. 3, pp. 60-64, 2002.

[14] N. Toufik, F. Pelanchon and P. Mialhe, "Degradation of a light emitting silicon junction of a bipolar transistor," *Journal of Electron Devices*, vol. 1, pp.7-9, 2003.

[15] L. Vendrame, P. Pavan, G. Corva, A. Nardi, A. Neviani, and E. Zanoni, "Degradation mechanisms in polysilicon emitter bipolar junction transistors for digital applications," *Microelectronics Reliability*, vol. 40, no. 2, pp. 207-230, 2000.

[16] S. Banerjee, R. Sundaresan, H. Shichijo and S. Malhi, "Hot-electron degradation of n-channel polysilicon MOSFETs," *IEEE Trans. on Electron Devices*, vol. 35, no. 2, pp. 152-157, 1988.

[17] S. Bhattacharya, R. Kovelamudi, S. Batra, S. Banerjee, B. Nguyen and P. Tobin, "Parallel hot-carrier-induced degradation mechanisms in hydrogen-passivated polysilicon-on-insulator LDD p-MOSFET's," *IEEE Electron Device Letters*, vol. 13, no. 9, pp. 491-493, 1992.

[18] J. D. Burnett and C. Hu, "Modeling hot-carrier effects in polysilicon emitter bipolar transistors," *IEEE Trans. on Electron Devices*, vol. 35, no. 12, pp. 2238-2244, 1988.

[19] Y. Nitsu, K. Yamaura, H. Momose and K. Maeguchi, "Anomalous current gain degradation in bipolar transistors," *in 29th Annual Proc. Reliability Physics*, Las Vegas, NV, USA, pp. 193-199, 1991.

[20] E. Hackbarth and D. D. Tang, "Inherent and stress-induced leakage in heavily doped silicon junctions," *IEEE Trans. on Electron Devices*, vol. 35, no. 12, pp. 2108-2118, 1988.

[21] K. C. Saraswat, J. D. Meindl, "Breakdown walkout in planar p-n junctions," *Solid-State Electronics*, vol. 21, no. 6, pp. 813-819, 1978.

[22] G. S. May and S. M. Sze, *Fundamentals of semiconductor fabrication*, 1st ed., John Wiley & Sons, 2004.

[23] P. K. Gopi, G. P. Li, G. J. Sonek, J. Dunkley, D. Hannaman, J. Patterson and S. Willard, "New degradation mechanism associated with hydrogen in bipolar transistors under hot carrier stress," *Applied Physics Letters*, vol. 63, no. 9, pp. 1237-1239, 1993.

[24] D. Quon, P. K. Gopi, G. J. Sonek and G. P. Li, "Hot carrier induced bipolar transistor degradation due to base dopant compensation by hydrogen: theory and experiment," *IEEE Trans. on Electron Devices*, vol. 41, no. 10, pp. 1824-1830, 1994.

[25] S. M. Sze and K. K. Kwok, *Physics of semiconductor devices*, 3rd ed., John Wiley & Sons, 2006, pp. 102-114.

[26] Temperature, Bias, and Operating Life, JESD22-A108F, 2017.

[27] J. R. Black, "Electromigration - a brief survey and some recent results," *IEEE Trans. Electron Devices*, vol. 16, no. 4, pp. 338-347, 1969.

[28] Failure Mechanisms and Models for Semiconductor Devices, JEP122H, 2016.

[29] Method for developing acceleration models for electronic component failure mechanisms, JESD91A, 2003.

[30] M. du Plessis and P. Rademeyer, "Novel electroluminescence technique to analyze mixed reverse breakdown phenomena in silicon diodes," *Solid-State Electronics*, vol. 54, no. 4, pp. 433-438, 2010.

[31] H. Weinerth, "Silicon diode breakdown in the transition range between avalanche effect and field emission," *Solid-State Electronics*, vol. 10, no. 11, pp. 1053-1062, 1967.

[32] S. Dutta, R. J. E. Hueting, A. J. Annema, L. Qi, L. K. Nanver, and J. Schmitz, "Opto-electronic modeling of light emission from avalanche-mode silicon p+n junctions," *Journal of Applied Physics*, vol. 118, no. 114506, 2015.

[33] S. Tyaginov, M. Jech, P. Sharma, J. Franco, B. Kaczer and T. Grasser, "On the temperature behavior of hot-carrier degradation," *IEEE International Integrated Reliability Workshop (IIRW)*, pp. 143-146, 2015.

[34] A. Bravaix, D. Goguenheim, N. Revil, E. Vincent, M. Varrot, and P. Mortini, "Analysis of high temperature effects on performances and hot-carrier degradation in DC/AC stressed 0.35 μm n-MOSFETs," *Microelectronics Reliability*, vol. 39, no. 1, pp. 35-44, 1999.

[35] G. Barletta and G. Curro, "Junction leakage current degradation under high temperature reverse-bias stress induced by band-defect-band tunnelling in power VDMOS," *Microelectronics Reliability*, vol. 45, pp. 994-999, 2005

[36] G. Roll, M. Goldbach and L. Frey, "Leakage current and defect characterization of p+n-source/drian diodes," *Microelectronics Reliability*, vol. 51, pp. 2081-2085, 2011.

Marius E. Goosen is currently the Head of Engineering of the INSiAVA technical team, focussed on the development, productisation and commercialisation of INSiAVA's technology and products. He started his career as a part-time junior lecturer in the Department of Electrical, Electronic and Computer Engineering for the 2008 and 2009 academic year while pursuing his post-graduate studies. He subsequently joined the INSiAVA high-tech start-up team in 2010 as a research engineer, working on the research and development of silicon light emission technology. He was appointed in his current capacity in the latter half of 2015 to get the silicon light emission technology and other products to the market. Marius obtained his B.Eng degree (Electronic engineering, cum laude) from the University of Pretoria in 2007, B.Eng Honours degree (Microelectronic engineering, cum laude) in 2008 and M.Eng (Microelectronic engineering, cum laude) in 2011. He was awarded the Louis van Biljon Gold medal for best final year Electronic Engineering student in 2007 and was subsequently awarded the Carl and Emily Fuchs Foundation Fellowship in 2009.

Petrus J. Venter obtained his BEng in Electronic Engineering at the University of Pretoria in 2004, with distinction. He subsequently completed his BEng(Hons), specialising in Microelectronics, in 2005, his MEng in 2010 and his PhD in 2014. He developed the first fully CMOS microdisplay chip in 2009 and is the inventor and co-inventor of several patented inventions in the field of silicon light emission and CMOS integrated circuits. He joined the University of Pretoria in 2007 as lecturer, later senior lecturer, while contributing part-time to INSiAVA's research and development. He practiced as an ECSA registered professional engineer as consultant to private companies between 2008 and 2014. He obtained his Bachelor of Law (LLB) in 2014 with electives in intellectual property and international law. His engineering responsibilities include IC design and implementation, while in his capacity as CEO he is responsible for developing the company's commercial strategy, regulatory compliance, operational management, securing investment, managing stakeholder relations and guiding the company's intellectual property strategy.

Nicolaas M. Fauré is a senior IC design engineer at INSiAVA. He was employed as a research assistant in the Department of Electrical, Electronic and Computer Engineering for the first semester of the 2010 academic year while pursuing postgraduate studies. He joined the INSiAVA team mid-2012 and started working on demonstrator development and testing, before focussing on IC design. Nicolaas obtained his B.Eng degree in electronics in 2009 at the University of Pretoria and his B.Eng (Hons) degree in 2010 in the microelectronics department at the University of Pretoria. In 2015 he completed his M.Eng (Microelectronics, cum laude) degree in the field of high speed analogue to digital converters, also at the University of Pretoria.

Promise N. Msomi joined INSiAVA as electronic engineer in 2018 after obtaining her BEng degree in electronic engineering from the University of Pretoria. She is currently pursuing her BEng(Hons) in Microelectronics. She started her career as a part-time quality control and integration engineer at THALES SA during December 2010 for vacation work. She then worked part-time for ESKOM during December 2013 and December 2014 as a control plant maintenance assistant and a customer network centre engineer respectively. She subsequently worked part-time for CSIR: DSIDE ICT during June 2016, mainly focusing on ICT Coastal News watch data analysis and designing of a visualisation dashboard for geospatial events on South Africa's coastline from harvested data. Her academic interests include ink-jet printed thermal sensors integrated with a custom designed monolithic integrated circuit. Ms Msomi manages INSiAVA's laboratory facilities and is responsible for the testing, measurement and characterisation of integrated circuit devices and products. She is also responsible for designing printed circuit boards (PCBs).

Johan Schoeman received BEng (2001), BEng (Hons) (2002, Cum Laude), MEng (2009, Cum Laude) and PhD (2018) degrees in electronic engineering from the University of Pretoria, Pretoria, South Africa. He joined the Department of Electrical, Electronic and Computer Engineering, University of Pretoria as a part time assistant lecturer in the telecommunications group in 2002. He was offered a full-time position in 2003 as lecturer in the electronics and microelectronics group and has been a member of the Carl and Emily Fuchs Institute for Microelectronics (CEFIM) ever since. His recent research interest includes MEMS based sensor modelling and design for thermal imaging, digital signal processing algorithms and optimisation for FPGA and ASIC implementations, multi-aperture digital holographic microscopy approaches, and receiver design for satellite and radio astrology systems. He has published several research papers and have presented at numerous local and international conferences. He is a senior member of the IEEE and a registered professional engineer (PrEng) with the Engineering Council of South Africa (ECSA).

Trudi-H. Joubert is the Director of the Carl and Emily Fuchs Institute for Microelectronics (CEFIM) and an Assistant Professor at the University of Pretoria. She is registered as a professional engineer with the Engineering Council of South Africa (ECSA) and holds Senior Member status with the IEEE. She received both the BEng and MEng degrees in Electronic Engineering with distinction, and earned a PhD from the University of Pretoria, South Africa. Her core pursuit is CMOS and BiCMOS mixed signal circuit design, mainly in readout and signal processing for imaging arrays, biologically inspired electronic circuit applications, and specialized devices for analog IC design. Her most recent endeavour is printed electronics sensors and circuits, particularly for water quality monitoring, but also in point-of-use diagnostics. She is inventor on 3 patents, has published 22 journal papers, presented and co-authored 57 peer-reviewed conference proceedings papers, with 401 total citations at an h-index of 10 (Google Scholar). She has been a member of both the technical and the organising committee for several international conference events, and acts as reviewer for high impact factor journals. She has lectured short courses to industry in her field of specialisation, worked on 31 projects for the South African industry, writing 131 technical reports in the process, and contributing to 32 integrated circuit chips. The contributions of her work to the South African innovation system spans university teaching, applied research, and leading industrial development of prototypes and products.