A BLUETOOTH SINGLE-CHIP FREQUENCY SYNTHESIZER

by

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SUMMARY

A BLUETOOTH SINGLE-CHIP FREQUENCY SYNTHESIZER BY SAURABH SINHA

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Degree: M. Eng. (Micro Electronic)

The research conducted for this dissertation seeks to understand the issues associated with integrating a frequency synthesizer on to a single monolithic chip. The target application for the frequency synthesizer is Bluetooth wireless technology devices. Radios that comply with the Bluetooth wireless specification operate in the unlicensed, 2.4 GHz radio spectrum ensuring communication compatibility worldwide. These radios use a spread spectrum, frequency hopping, and full-duplex signal at up to 1600 hops/sec. The signal hops among 79 frequencies (2.402 - 2.480 GHz band) at 1 MHz intervals to give a high degree of interference immunity.

This research implements the required synthesizer by individually considering each sub-system and designing to meet the overall specifications for a dual-loop synthesizer. Such a dual-loop synthesizer consists of two VCOs: one operating at a higher frequency (with a narrow operating range) and another VCO operating at a lower frequency (with a wider operating range.) A LC based VCO is designed for the higher frequency loop, and the required inductor is implemented on-chip. The research considers the various issues related to on-chip inductor implementation, and also considers an active inductor as an option. The lower frequency loop is implemented with a ring-oscillator.

The design is completed for fabrication in a standard 0.35-µm CMOS process without any external components. The computed phase noise is -84 dBc/Hz at 1000 kHz offset from a 2.4-GHz carrier. With an active chip area of 3.8 mm^2, the simulated chip consumes about 100 mW.

Keywords: frequency synthesizer, phase locked loop (PLL), phase noise, spurious tones, voltage controlled oscillator (VCO), single sideband (SSB) mixer, ring oscillator, LC oscillator, loop filters, passive on-chip inductor, active on-chip inductor, pn-junction varactor.

SAMEVATTING

'N BLUETOOTH ENKELVLOKKIE-FREKWENSIESINTETISEERDER DEUR SAURABH SINHA

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Die navorsing wat vir hierdie verhandeling uitgevoer is, poog om die vraagstukke in verband met die integrasie van 'n frekwensiesintetiseerder op 'n enkele monolitiese vlokkie op te los. Die teikentoepassing vir die frekwensiesintetiseerder is Bluetooth-draadlosetegnologie-toestelle. Radio's wat voldoen aan die Bluetooth-draadlose spesifikasie werk in die ongelisensieerde 2.4 GHz radiospektrum wat kommunikasie-aanpasbaarheid wêreldwyd verseker. Hierdie radio's gebruik 'n spreispektrum, frekwensiespring- en volledige duplekse sein teen 1600 spronge per sekonde. Die sein spring tussen 79 frekwensies (2.402 - 2.480 GHz-band) teen 1 MHz-intervalle om 'n hoë graad van steuringsimmuniteit te lewer.

Hierdie navorsing realiseer die vereiste sintetiseerder deur elke substelsel individueel in ag te neem en te ontwerp om aan die oorhoofse spesifikasies van 'n tweelus-stelsel te voldoen. Sodanige tweelus-sintetiseerder bestaan uit twee VCO's waarvan die een teen 'n hoër frekwensie (met 'n nou reikwydte) werk en die ander teen 'n laer frekwensie (met 'n wyer reikwydte) werk. 'n LC-gebaseerde VCO is vir die hoërfrekwensielus ontwerp en die vereiste induktor is op die vlokkie gerealiseer. Die navorsing oorweeg die onderskeie vraagstukke in verband met op-vlokkie induktorimplementering en oorweeg ook 'n aktiewe induktor as 'n keuse. Die laerfrekwensie-lus wend 'n ringossillator aan.

Die ontwerp is voltooi vir vervaardiging in 'n standaard 0.35-µm CMOS-proses sonder enige uitwendige komponente. Die berekende faseruis is -84 dBc/Hz teen 1000 kHz vanaf 'n 2.4-GHz-draer. Met 'n aktiewe vlokkieoppervlakte van 3.8 mm^2 verbruik die gesimuleerde vlokkie ongeveer 100 mW.

Sleutelwoorde: frekwensiesintetiseerder, fasesluitlus (PLL), faseruis, ongewenste tone, spanningsbeheerde ossillator (VCO), enkelsyband(SSB)menger, ringossillator, LC-ossillator, lusfilters, passiewe op-vlokkie-induktor, aktiewe op-vlokkie-induktor, pn-koppelvaraktor.

ACKNOWLEDGEMENT

The research work of this dissertation would not be possible without the kind co-operation and support of many friends and colleagues. I would like to acknowledge and extend my appreciation to all those that have contributed indirectly or directly to the research conducted in this dissertation. The following names are worthy of a special mention:

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I would also like to acknowledge the excellent resources (human and financial) provided by the Carl & Emily Fuchs Institute for Microelectronics (CEFIM), University of Pretoria. During the course of this dissertation, I have also had the opportunity to serve on several IEEE committees (region 8) – as the dissertation progressed, I started to lack time to serve on some of the committees and withdrew: I would like to thank IEEE volunteers that kindly took over my roles in these committees and effectively fulfilled my initially promised tasks.

I would also like to extend my gratitude to my parents and friends for their kind support and understanding as this dissertation was concluded. In particular, I would like to acknowledge my close friends: Albert Chittenden, Nico Engelbrecht and Gregory Griffiths.

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CHAPTER 1: INTRODUCTION

1.1 Motivation

Commensurate with an explosive growth of the wireless communications market has arisen the demand for low-cost, low-power, small form factor transceiver units. To meet the needs associated with these requirements, highly-integrated monolithic solutions for the transceiver units need to be designed.

One of the key building blocks associated with any receiver or transmitter is a frequency generating or synthesizing device that creates a local oscillator (LO) signal used to shift down (down-convert) a received carrier signal spectrum to a lower frequency, or in the case of a transmitter, shift a signal spectrum up (up-convert) to a higher frequency band. The research conducted for this dissertation seeks to understand the issues associated with integrating the frequency synthesizer functions on to a single monolithic chip and to eventually implement a frequency synthesizer for Bluetooth[1] wireless technology devices. Figure 1 serves to illustrate the relevant position of a frequency synthesizer in a wireless transceiver.

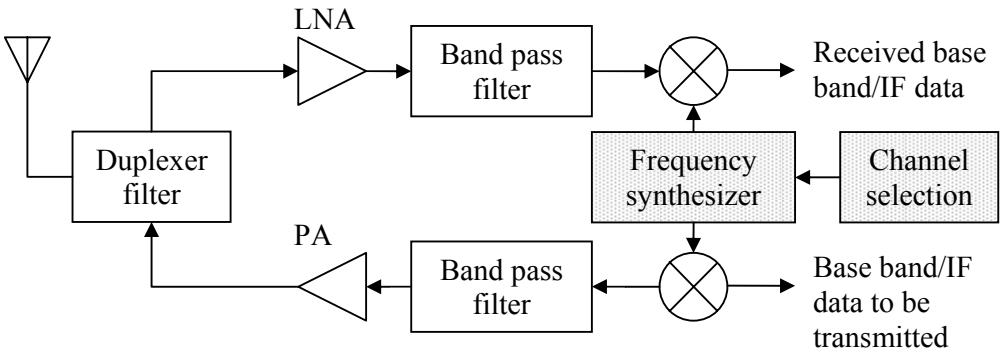


Figure 1.1. This figure shows a typical RF wireless transceiver, [1] to illustrate a typical use of frequency synthesis in tranceiver systems.

1.2 Context and contribution of work

Table 1.1 shows where this project fits in with reference to other similar works done globally. The research efforts (by some others globally) concentrate on narrow (single)

[1] The Bluetooth wireless applications website is located at http://www.bluetooth.com.

band frequency synthesizers and generate low frequency signals. However, as the 2.4-2.5 GHz range is becoming more popular for industry, scientific and medicine (ISM) applications, these frequency synthesizers cannot serve. It is, hence, desired to have a frequency synthesizer that can suffice this requirement. Other drawbacks are the power ratings of the synthesizers as well as the integration levels, [2].

As discussed in the next chapter, a dual loop series synthesizer will be used to achieve the more desired abovementioned specifications. However, this double-loop architecture requires effectively twice the circuitry as the standard single-loop phase-locked loop. This is also observed in typical dual-band synthesizers (partial integration level) on the market today. They utilize multiple PLLs with narrow band voltage-controlled oscillators that operate at different centre frequencies[2].

Source	Frequency range	Phase noise	Architecture	Technology	Power Supply	IC Level
[3]	1.4-1.6 GHz	-115 dBc/Hz @ 600 kHz	Single-loop (Switched tuning)	0.6 µm CMOS	3 V	Full
[4]	865-1000 MHz	-110 dBc/Hz @ 200 kHz	Single loop	0.5 µm CMOS	3.3 V	Off-chip filter
[5]	1.7-1.9 GHz	-123 dBc/Hz @ 600 kHz	Single loop	0.4 µm CMOS	3 V	Full
[6]	1.7-2.3 GHz	Not Reported	Single loop	0.5 µm BiCMOS	3 V	Off-chip filter
[7]	700-1000 MHz	-80 dBc/Hz @ 100 kHz	Single loop	0.8 µm CMOS	5 V	Off-chip filter
[8]	820-1560 MHz	Not Reported	Single loop	0.25 µm CMOS	1.8 V	Full
[9]	5-110 MHz	Not Reported	Single loop	0.8 µm CMOS	5 V	Full
[10]	1-150 MHz	-80 dBc/Hz @ 600 kHz	Translinear	0.6 µm BiCMOS	3 V	Full
[11]	0.3 –165 MHz	-94 dBc/Hz @ 10 kHz	Single loop (complex D/A control)	0.8 µm CMOS	3-5 V	Full
[12]	950-2150 MHz	Not Reported	Double loop	f_t = 9 GHz Bipolar	5 V	Full
This work	2.4-2.5 GHz	-80 dBc/Hz @ 10 kHz	Double loop	0.35 µm CMOS	3.3 V	Full

Table 1.1. The table places the contribution of this dissertation relative to others globally.

[2] Si4132 Product brief article (http://www.silabs.com/products/Si4132/index.html)

1.3 Organisation of dissertation

This dissertation is organised in the following manner:

 Chapter 1: Introduction

The chapter provides the research motivation for this dissertation. The chapter also serves to place the dissertation in context with other research conducted globally.

 Chapter 2: Synthesizer background

The chapter discusses the various approaches used in the implementation of a synthesizer. Synthesizer architectures directly or indirectly affect certain overall design specifications – the chapter aims to discuss such specifications. The chapter converges to show that a phase locked loop (PLL) based solution is ideal for the constraints of this dissertation.

 Chapter 3: General theory of PLLs

The chapter aims to provide a review of PLL theory. The chapter is written with a general approach kept in mind. Some of the critical specifications (of the previous chapter) are linked to mathematically quantify various trade-offs that apply to PLL design.

 Chapter 4: System level design

This chapter numerically quantifies the specifications of the synthesizer. The chapter provides the concept design (including sub-system specifications.) A simplified mathematical feasibility analysis is also accomplished (using MATLAB) to show that the sub-system specifications will serve (in theory) to meet the overall synthesizer specifications.

 Chapter 5: Sub-system level design & layouts

The chapter details the design (and simulation) of the various sub-systems conceptualized in the previous chapter. Sub-system integration is also accomplished, and design verification (by simulation) is demonstrated. The layout plan is also included in this chapter.

 Chapter 6: Inductor design

The previous chapter introduces an important component of oscillator design, viz an inductor. The implementation of an inductor has several practical implications from the perspective of on-chip design. This chapter discusses such effects, and includes the implementation for the inductors of the synthesizer aimed in this dissertation.

 Chapter 7: Conclusion

The conclusion serves to summarize (to synthesize) the design of this dissertation. Design shortcomings are also given as part of the conclusion.

The dissertation also includes two appendices. The first appendix serves to provide relevant layouts of the sub-systems (of chapter 5), and the second appendix serves to provide the mathematical (MathCAD) procedure for the inductor design (of chapter 6.)

CHAPTER 2: SYNTHESIZER BACKGROUND

2.1 Synthesizer approaches

Traditionally, there are two major ways of generating frequencies: direct and indirect approaches. The direct approach consists of generating a sine wave digitally (by storing the sine wave in a read-only memory (ROM), for example) followed by digital-to-analogue (D/A) conversion. Even though this approach enjoys the advantage of being mostly digital and is, therefore, easy to design, manufacture, and test, it needs a high-speed D/A converter, which can be the major bottleneck. Additionally, it tends to consume high power and hence is not considered further for this dissertation.

The focus of this dissertation will be the indirect way of generating frequencies: the use of a controlled oscillator. The general idea is to control the frequency of oscillation via some external control input (usually voltage); consequently, the resulting oscillator is called a voltage-controlled oscillator (VCO). Since the noise property and frequency stability of such a VCO is usually rather poor, it is typically put in a feedback loop to enhance these properties. Since the loop tracks the phase (and thus the frequency), it is called a phase locked loop (PLL), and so the approach is denoted as a PLL-based frequency synthesizer. This forms the fundamental basis of the approach for this dissertation.

For low system cost and portability, frequency synthesizers need to be integrated with an on-chip VCO. The difficulty of an integrated VCO lies in its poor frequency stability compared with an external high-Q resonator-based VCO. The phase noise of the integrated VCO also contributes directly to reducing the signal-to-noise ratio (SNR) of the receiver front end. The phase noise (defined in section 2.2) problem can be alleviated partially by broadbanding the PLL. Essentially, the feedback action allows the PLL to suppress the inband VCO phase noise by high-pass filtering it.

Several PLL-based frequency synthesizer architectures exist – the next three sub-sections (2.1.1-2.1.3) will discuss these architectures. As the PLL is an important building block of these frequency synthesizers, its operation principle and characteristics are examined in detail in the next chapter.

2.1.1 Integer–*N* PLL architecture

A simple PLL incorporating an integer-*N* programmable divider in the feedback path is shown in figure 2.1. The VCO output frequency is divided by the number *N* in the divider. The divided frequency is compared to the crystal reference frequency by the phase detector (PD). The low-pass filtered output of the PD provides the phase difference information to adjust the VCO output frequency to the more precise desired frequency.

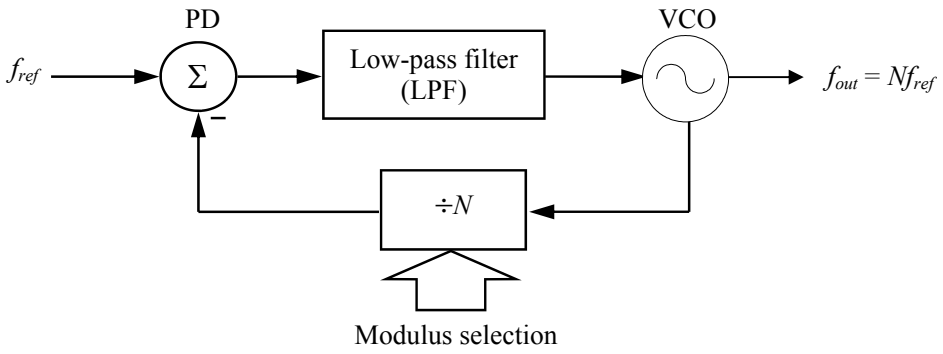


Figure 2.1. The figure shows the block diagram of an integer-*N* synthesizer, [13].

The PLL frequency synthesizer is suitable for integration in a standard IC process due to its low power consumption and reasonable chip area. This type of synthesizer is inherently slower than a digital direct synthesizer (DDS) due to the feedback action requiring time to acquire its steady-state operation. Larger loop bandwidth can attenuate the phase noise of the VCO for frequency offsets roughly within the loop bandwidth. Moreover, fast frequency change is only possible when the loop bandwidth is large. The loop bandwidth is typically limited to one tenth of the reference frequency [1] due to stability requirement.

In an integer-*N* synthesizer, the output frequency changes by only integer multiples of the reference frequency. As a result, the close channel spacing in a wireless communication system limits the reference frequency and the loop bandwidth. The periodic disturbance of the VCO control due to sampling action of the reference frequency in the PD creates unwanted sidebands in the VCO output and, to attenuate the magnitude of these reference spurs sufficiently, in many cases, it places further limitation on the loop bandwidth. Furthermore, the phase noise contributed from the reference source to the output is increased by approximately *N* times in the loop, which is large if the desired output

frequency is much higher than the channel frequency spacing. Therefore, many techniques have been proposed [14] to overcome the trade-off among frequency division ratio, loop bandwidth and reference frequency.

2.1.2 Fractional–*N* PLL architecture

In fractional-*N* synthesizer, the divider architecture is modified in order to obtain the frequency change by a fraction of the reference frequency, [15]. Therefore, the tradeoff in the PLL synthesizer with an integer divider does not apply to fractional-*N* synthesis. The fraction division is obtained by occasionally or periodically changing the division value of the divider and this can be done by pulse inserting, pulse removing and pulse interpolating or modulating the divider ratio. Figure 2.2 shows the block diagram of a fractional-*N* synthesizer with a dual-modulus divider as an illustration. For instance, if the VCO output is divided by *M* for *N* output pulses and by *(M+1)* for *P* output pulses, then the average equivalent divide value is equal to $[N / (N+P)] \times M + [P / (N+P)] \times (M+1) = M + [P / (N+P)]$. Thus, the division value can vary between *M* and *(M+1)*.

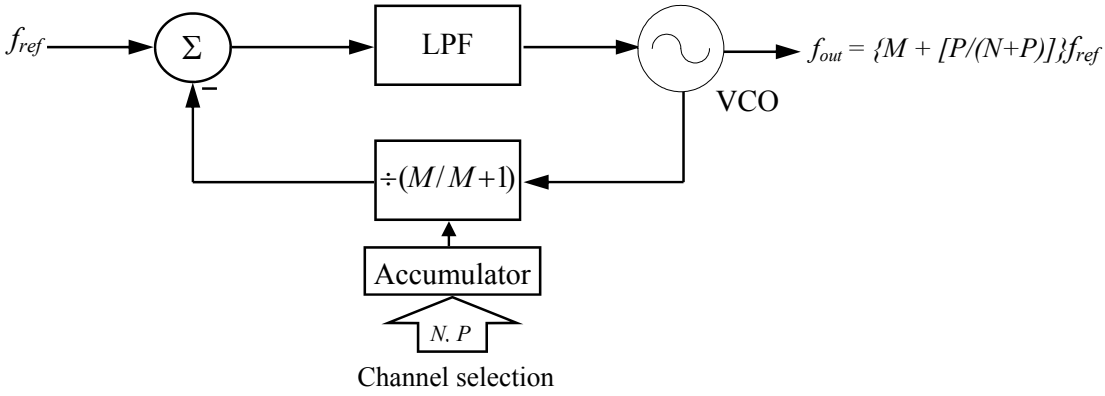


Figure 2.2. The figure shows the fractional-*N* synthesizer using dual-modulus divider[1].

The modification allows a larger loop bandwidth compared to that in the case of integer-*N* synthesizer under the same channel separation. Thus, it increases the locking speed of the synthesizer and provides more suppression of the VCO output phase noise close to the carrier. The drawback is the existence of large fractional spurs at the output and the locations of the spurs vary with the divide value. Many spur reduction methods, such as phase estimation by DAC and noise shaping by *S-Δ* modulation with multi-modulus divider, have been proposed in [1]. However, those methods make the design of fractional-*N* synthesizer more complicated.

[1] Delta-sigma fractional-N synthesizers web article (http://www.planetanalog.com/story/wireless/).

2.1.3 Dual loop architecture

Employing two or more loops can alter the relationship between the channel spacing and the reference frequency of integer-*N* synthesizers as discussed in [16]. There are mainly two types of dual-loop synthesizers as proposed in [14], which are combination of two PLLs by a single-side band (SSB) mixer in parallel and in series. Example of each type is shown in figure 2.3. The basic idea is to add a low variable frequency to a high fixed offset frequency. The frequency change of the synthesizer therefore only requires the change of the divide ratio in the low-frequency loop. In the parallel configuration, a fixed frequency is mixed with the changeable frequency by the SSB mixer at the output and therefore it suffers from large spurs during mixing. In the series configuration, a changeable frequency is added inside the loop. Although this configuration needs longer time to settle, the sideband from the mixer can be greatly attenuated by the loop.

The primary advantage of the dual loop architecture over integer-*N* topologies is that the loop bandwidth of the high-frequency loop chosen can be large. As the VCO in the high-frequency loop operates at a higher frequency, the phase noise performance is expected to be worse than that in a low-frequency loop. Therefore, a larger loop bandwidth can provide more reduction of the phase noise close to the carrier to compensate the phase noise performance of the high frequency VCO. Moreover, because of the fixed offset frequency, the division number of the divider is also reduced. The possible drawbacks are mainly the sidebands produced from non-ideal SSB mixing and probable larger power consumption than single loop synthesizers. In this dissertation, dual-loop architecture in series is chosen and more detailed merits and design will be discussed in chapter 4.

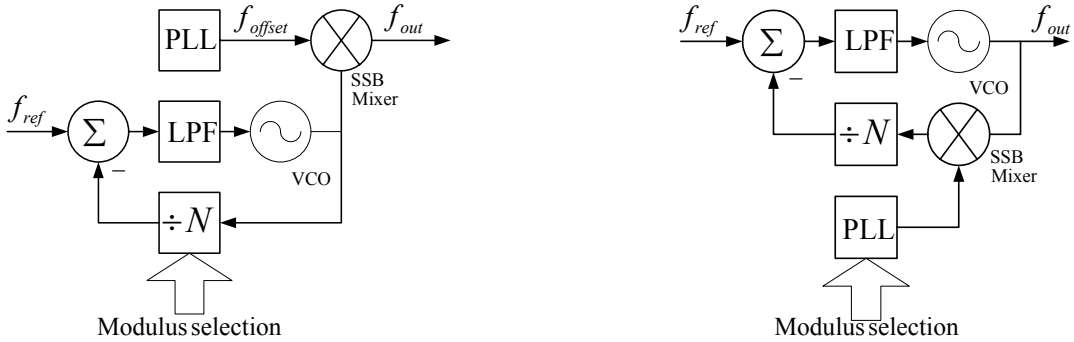


Figure 2.3. The figure [14] shows (a) parallel, and (b) series dual-loop architectures.

2.2 Frequency synthesizer design considerations

For an ideal oscillating source, a sharp impulse is expected in the frequency spectrum. However, due to random fluctuations in the oscillating source, expressed in term of phase noise, the spectrum exhibits "skirts" around the carrier. In order to quantify the phase noise, the noise power per unit bandwidth at an offset frequency ($\Delta\omega$) with respect to the carrier frequency, ω_o is compared with the carrier power, and this quantity is expressed in the unit of dBc/Hz. In contrast to phase noise, sidebands are deterministic non-ideal components in the output spectrum and have no harmonic relationship with the carrier. Sidebands are usually specified with their frequency and their magnitude relation to that of the carrier [1]. The plots of the phase noise and sidebands in the frequency domain are shown in figure 2.4.

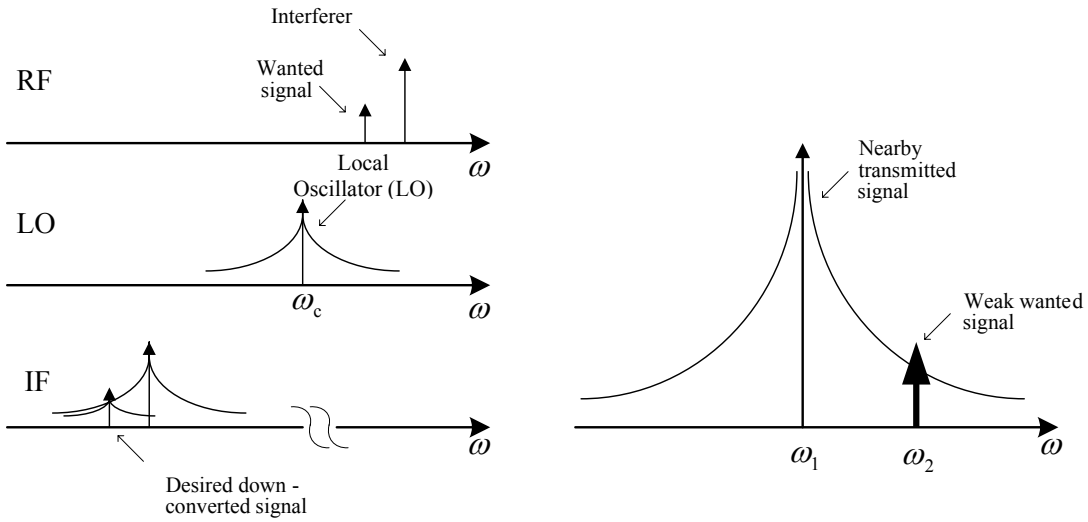


Figure 2.4. The figures show the effect of phase noise on the (a) receive, and the (b) transmit paths.

The effect of unwanted sideband is another problem in the receive path as shown in figure 2.5. Suppose the oscillator output consists of a carrier at ω_C and a sideband at ω_S, while the received signal at ω_{RF} is accompanied by an interference signal at ω_{IN}. If the difference between ω_C and ω_{RF} is equal to that between ω_S and ω_{IN}, the down-converted interferer falls into the desired channel as the wanted signal and corrupts the resulting intermediate frequency (IF) output. Typically, wireless communication systems require that spurs be approximately 60 dB below the carrier. Phase noise and spurious tones in the oscillator signal can limit the ability to receive a desired signal in the presence of strong

interferers and this ability is called "selectivity". The carrier frequency of oscillators in RF transceiver must also have very high absolute accuracy throughout a wide range of temperature and be stable for a long period of time. In a wireless communication system, the lower and upper edges of each channel can tolerate an error of no more than a few hundred Hertz.

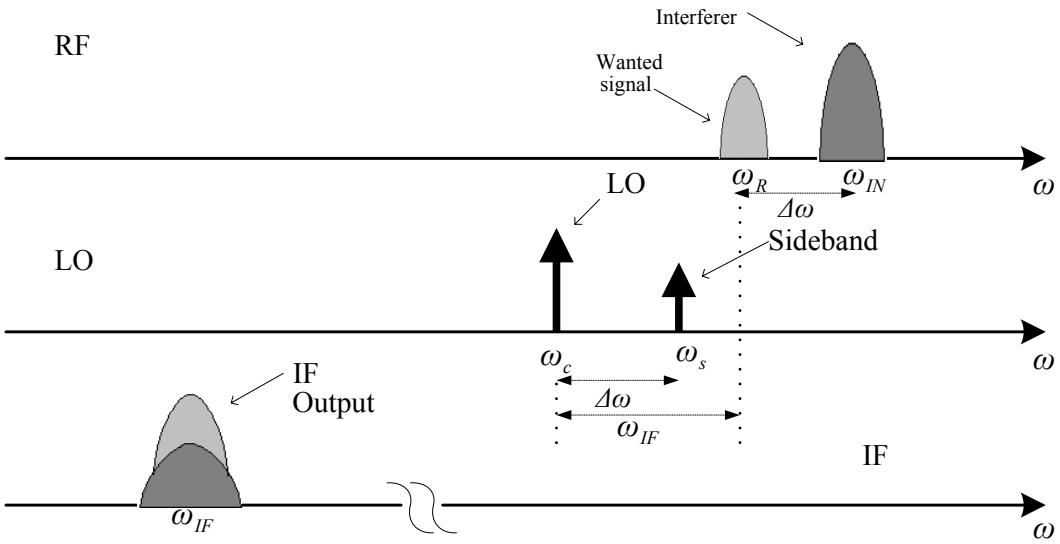


Figure 2.5. The figure shows the effect of sideband in a receiver.

In a wireless transceiver, to change from receive channel to transmit channel, the LO frequency may be required to vary by a few tens of megahertz, and the oscillator requires a finite time to establish the new stable frequency reference. The settling time of the timing source is a critical design parameter for some systems such as frequency-hopped spread-spectrum (FHSS) systems. The settling time required in a typical RF system varies from a few tens of microseconds to a few tens of milliseconds.

CHAPTER 3: PHASE LOCKED LOOP THEORY

The PLL is a fundamental part of radio, wireless and telecommunication technology. The goal of this chapter is to review the theory, design and analysis of PLL circuits. PLL is a simple negative feedback architecture that allows economic multiplication of crystal frequencies by large variable numbers. By studying the loop components and their reaction to various noise sources, it will be shown that the PLL is uniquely suited for generation of stable, low noise tunable RF signals for radio, timing and wireless applications.

Some of the main challenges fulfilled by PLL technology are economy in size, power and cost while maintaining good spectral purity. This chapter details basic loop transfer functions, loop dynamics, noise sources and their effect on signal noise profile, phase noise theory, loop components (VCO, crystal oscillators, dividers and phase detectors) and principles of integer-*N* and fractional-*N* technology. The approach will be mainly heuristic, with some illustrative examples. The examples are to illustrate the general PLL theory and do not necessarily cover the subsystems of this dissertation. The latter will be covered in the next chapter.

3.1 PLL motivation

Until DSP technology is capable of directly processing and generating the RF signals used to transmit wireless data, traditional RF engineering will remain a fundamental part of wireless communication systems design. As it stands, wireless transceivers must still be able to generate a wide range of frequencies in order to upconvert the outgoing data for transmission and downconvert the received signal for processing (as shown in Figure 3.1).

As discussed in the last chapter, there are a variety of frequency synthesis techniques; however, the PLL represents the dominant method in the wireless communications industry. Integrated PLL, like most wireless communication technologies, is relatively new and has only matured in the last two decades. The ability to execute all PLL functions on a single integrated circuit (IC) has created an economical, mass production solution to meet the needs of industry. Current PLL ICs are highly integrated digital and mixed signal circuits that operate on low supply voltages and consume very low power. These ICs require only an external crystal (Xtal) reference, voltage controlled oscillators (VCO), and

minimal external passive components to generate the wide range of frequencies needed in a modern communications transceiver. Although a proven technology, PLL is still changing and evolving to keep pace with the wireless revolution.

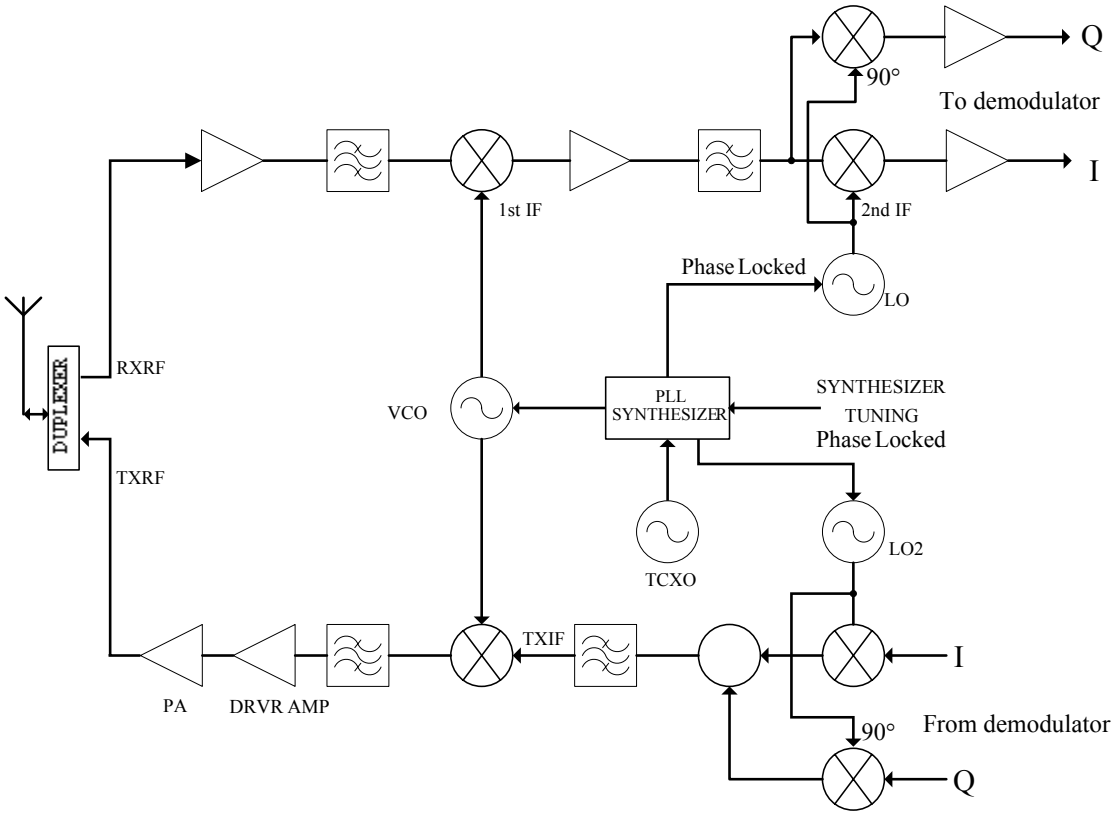


Figure 3.1. The figure shows a general transceiver block diagram. The figure is adapted from Stallings, [17].

The problems associated with operating a wireless communications system have become especially acute in the last few years with the advancement of cellular telephony and the emergence of wireless data networks. As there are more users now, most operating at progressively higher data rates, both interference and signal-to-noise-ratio (SNR) have become key considerations in system design. Phase noise and spurious emissions contribute significantly to both of these issues and are largely dependent on the performance of the PLL IC. Minimizing phase noise and spurs of the frequency synthesizer while staying within power consumption, size, and cost restraints serves as some of the engineering challenges of this dissertation. The purpose of this chapter is to illustrate practical PLL signal generation techniques, review PLL basic building blocks, and examine various phase noise sources and their measurement, and compare integer-*N* and fractional-*N* PLL technologies. The focus will be on basic principles, synthesis parameters, phase noise and its measurement, as well as design trade-off.

3.2 PLL Architectures

PLL synthesizer architectures have already been introduced in the previous chapter. The aim of this chapter is to complement the qualitative descriptions of the previous chapter.

3.2.1 Integer-*N* PLL

Figure 3.2 shows a typical block diagram of a PLL implemented with a TCXO reference.

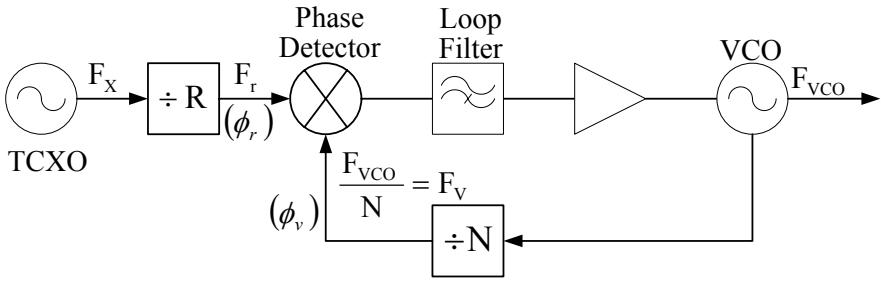


Figure 3.2. The figure shows the integer-*N* (classical) PLL block diagram.

This traditional PLL implementation will be termed "integer-*N*" to avoid confusion due to the addition of fractional-*N* technology. The PLL circuit performs frequency multiplication, via a negative feedback mechanism, to generate the output frequency, F_{VCO}, in terms of the phase detector comparison frequency, F_r.

$$F_{VCO} = NF_r \tag{3.1}$$

To accomplish this, a reference frequency must be provided to the phase detector. Typically, the TCXO frequency, F_x, is divided down (by R) "on-board" the PLL IC. The phase detector utilizes this signal as a reference to tune the VCO and, in a "locked state," it must be equal to the desired output frequency, F_{VCO}, divided by N.

$$\frac{F_{VCO}}{N} = \frac{F_x}{R} = F_r \tag{3.2}$$

Thus, the output frequency that the synthesizer generates, F_{VCO}, can be changed by reprogramming the divider N to a new value. By changing the value N, the VCO can be tuned across the frequency band of interest. The only constraint to the frequency output of

the system is that the minimum frequency resolution, or minimum channel spacing, is equal to F_r.

$$\text{Channel spacing} = \frac{F_{VCO}}{N} = F_r \tag{3.3}$$

When the PLL is in unlocked state (such as during initial power up or immediately after reprogramming a new value for N) the phase detector will create an error voltage based on the phase difference of the two input signals. This error voltage will change the output frequency of the VCO so that it satisfies (3.2). As long as the system is in a locked condition the VCO will have the same frequency accuracy as the TCXO reference. If the crystal accuracy is 1 part-per-million (ppm), the output frequency of the synthesizer will also be accurate to 1 ppm.

Specifically, if F_r = 30 kHz and N = 32000, the only way for this circuit to be in a stable state (locked) is when F_{VCO} = 960 MHz. If N were changed to 32001, a frequency and phase error will develop at the input of the phase detector that will, in turn, retune the VCO frequency until a locked state has been reached. The locked state will be reached when F_{VCO} = 960.03 MHz and, if the TCXO has an accuracy of 1 ppm, the output of the VCO will be accurate to $\approx\pm$ 960 Hz.

3.2.2 Fractional-*N* PLL

An unavoidable occurrence in PLL synthesis is that frequency multiplication (by N), raises the signal's phase noise by 20 log(N) dB [15]. The main source of this noise is the noise characteristics of the phase detector's active circuitry. As the phase detectors are typically the dominant source of close-in phase noise, N becomes a limiting factor when determining the lowest possible phase noise performance of the output signal. A multiplication factor of N = 30000 will add about 90 dB to the phase detector noise floor. 30000 is a typical N value used by an integer PLL synthesizer for a cellular transceiver with 30 kHz channel spacing. It would seem that the close-in phase noise of the system can be radically reduced by reducing the value of N, but unfortunately the channel spacing of an integer-N synthesizer is dependent on the value of N (as exhibited by (3.3.)) Due to this dependence, the phase detectors typically operate at a frequency equal to the channel spacing of the communication system.

Phase detectors are a form of comparator providing an output signal whose DC component is proportional to the difference in phase between the two input signals. Typically, $V_P = K_P(\phi_{i1} - \phi_{i2})$, where V_P is the output voltage, K_P is the phase detector gain and ϕ_{i1}, ϕ_{i2} are the phases of the input signals. To prevent any unwanted spurious noise, a filter at the output of the phase detector (called the loop filter) must be present and appropriately narrow in bandwidth. Unfortunately, as the loop filter bandwidth decreases, the time required for the synthesizer to switch between channels increases.

For a second order loop with natural frequency (loop bandwidth), ω_n and damping factor ξ, the switching speed, T_{sw} is proportional to the inverse of their product.

$$T_{sw} \propto \frac{1}{\omega_n \xi} \tag{3.4}$$

If N could be made much smaller, F_r would increase and the loop filter bandwidth required to attenuate the reference spurs could be made large enough so that it does not impact the required switching speed of our system. Once again, however, the upper limit of F_r is bound by our channel spacing requirements. This illustrates how the desires to optimize both switching speed and spur suppression directly conflict with each other.

A newly emerging PLL technology has made it possible to alter the relationship between N, F_r, and the channel spacing of the synthesizer. It is now possible to achieve frequency resolution that is a fractional portion of the phase detector frequency. This is accomplished by adding internal circuitry that enables the value of N to change dynamically during the locked state. If the value of the divider is "switched" between N and $N + 1$ in the correct proportion, an average division ratio can be realized that is N plus some arbitrary fraction, K/F. This allows the phase detectors to run at a frequency that is higher than the synthesizer channel spacing.

$$F_{VCO} = F_r\left(N + \frac{K}{F}\right) \tag{3.5}$$

where

F is the fractional modulus of the circuit (i.e. 8 would indicate a ⅛ fractional resolution) &

K is the fractional channel of operation.

3.3 PLL Parameters

There are several important parameters for signals generated by a PLL circuit.

Frequency range, or tuning bandwidth - the frequency band needed for the application. Most cellular applications are narrow band (covering 3-10 % bandwidth.) As an example USA cellular standards, AMPS, TDMA or CDMA, cover 25 MHz in the 900 MHz band.

Step size or frequency resolution - the smallest frequency increment possible. It is F_r for integer-N and F_r/F for fractional-N. In the USA cellular system, step size is 30 kHz. In China, Japan and the Far East it is 25 kHz. In Europe, the GSM cellular system requires a 200 kHz step. In FM broadcasting radio, the step size is 100 kHz.

Phase noise - an indicator of the signal quality. Phase noise and jitter are manifestations of the same phenomena (the former in the frequency domain, the latter in time domain.) Clean signals have low jitter, which results in much of their total energy being "concentrated" close to the center frequency of operation. Phase noise is specified in a variety of ways: time jitter (nsec rms), degrees rms, FM noise (Hz rms) or spectral distribution density, $L(f_m)$.

Spurious signal level - a measure of the discrete, deterministic and periodic interference "noise" in the signal spectrum. Spurious signals are part of the signal's "noise spectrum" and represent any discrete spectral line not related to the signal itself. Harmonics (and sometimes sub-harmonics) are usually not considered as spurious signals and are dealt with separately.

Loop bandwidth - a measure of the dynamic speed of the feedback loop. Since the PLL acts as a narrow-band tracking filter, this parameter indicates this filter's single sideband bandwidth. For many designers, this bandwidth is synonymous with the loop's natural frequency $\omega_n/2\pi$ or the frequency in which the open loop gain equals 1. ω_n is always a design parameter when optimizing for phase noise, switching speed, or spur suppression.

Switching speed - a measure of the time it takes the PLL circuit to re-tune the VCO from one frequency to another. This parameter usually depends on the size of the frequency step. As the synthesizer output frequency approaches the intended frequency asymptotically, switching speed is typically measured by the time it takes to settle to within a specified tolerance from the final frequency. Other parameters deal with size, power, supply voltage, interface protocol, temperature range and reliability.

3.4 PLL Components

The four basic components of a PLL circuit are the VCO, the phase-frequency detector, the main and reference dividers, and the loop filter. Typically, the PLL IC integrates the dividers and phase detectors onboard. In general, the reason for excluding the VCO and loop filter is to prevent the noise associated with the digital dividers and phase detectors from coupling with the VCO's active circuitry. This also allows the IC more flexibility in application.

3.4.1 Voltage controlled oscillators (VCO)

The VCO generates the output signal from the synthesizer. VCOs are positive feedback amplifiers that have a tuned resonator in the feedback loop. Oscillations occur at the resonant frequency, which is typically changed, or tuned, by varying the resonator capacitance. VCOs are oscillators whose resonant tank circuit can be tuned via a control voltage that is applied across a varactor in the tank circuit. In the cellular and PCS bands, most VCOs are "negative resistance" types, with a resonator in the transistor base or emitter. Though different designers have their own schemes, they are quite similar in structure. Figure 3.3 shows a typical VCO sketch.

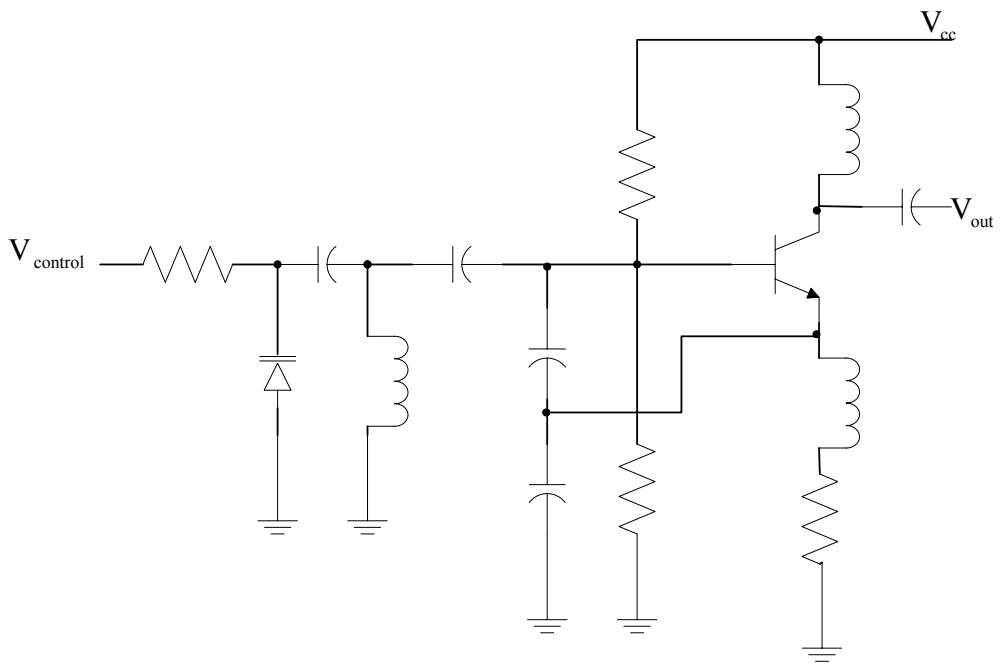


Figure 3.3. The figure shows a conceptual schematic of a *L*-Band VCO.

The theoretical transfer function of a VCO is given by $ks/(s^2 + \omega_o^2)$. In practice, the Q of the resonator must be finite and the transfer function poles will be slightly to the left of the imaginary axis on the complex plane (poles to the right or on the imaginary axis would yield a signal with infinite energy, which is not achievable.) Varying the DC voltage across the varactor diode, which is part of the tank circuit, controls the VCO frequency. The inductor and the varactor both limit the Q of the tank circuit.

Type of component	**Typical *Q***
Microstrip line on Fr-4	6-12
Air coil	20-50
Ceramic materials	50-200
Saw resonator	400-2000
Varactor (2-6 pF)	40-100

Table 3.1. The table shows the typical Q for inductors and varactors in the 800-2000 MHz range, [18]

A VCO can be specified by its tuning gain, K_v. This is the amount of frequency deviation (in MHz) that results from a 1-volt change in the control voltage. It is measured in units of MHz/V. The noise level on the VCO control line is determined by active devices and is not typically variable in a given application. Therefore, a lower K_v will generate a lower phase noise. For example, 1 mV of noise on the control line will generate 20 Hz FM noise for $K_v = 20$ but only 2 Hz FM noise for $K_v = 2$. Typically, if the Q of the tank circuit is raised, the phase noise characteristics will be improved (this can be achieved by reducing K_v (and ultimately the tuning bandwidth) of the VCO.) K_v linearity is also very important because of its effect on loop dynamics. As it will be seen in (3.6), K_v directly affects the loop transfer function, and therefore its bandwidth.

Oscillator design can be accomplished by analyzing either the open loop transfer functions, or the closed loop *s*-parameters. In the open loop analysis, oscillation will occur at the frequency where the open loop phase shift is 360° and the open loop gain is greater than 1 (see figure 3.4 and figure 3.5.)

A VCO will start to oscillate as a consequence of background noise in the circuit. This background noise is due to the noise figure of the amplifier, the resistors, and the finite Q of the resonator. When the VCO is initially powered up, noise that is present within the frequency band of the resonator is amplified until the circuit reaches saturation. When the

amplifier reaches saturation, the amplitude of the noise will stabilize and the oscillator will reach a steady state condition. If *G(s)* is the VCO transfer function, then the output spectrum will be given by:

$$S_o(f) = F(kT)\left|G^2(s)\right| \tag{3.6}$$

where:

k is Boltzman's constant,

T is the ambient temperature in Kelvin, and

F is the total noise figure.

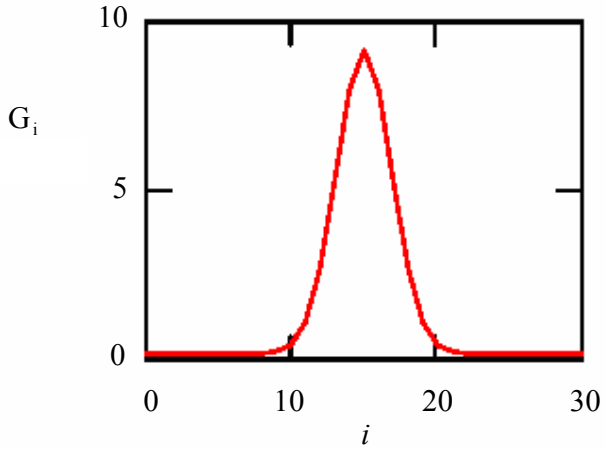


Figure 3.4. The figure shows the oscillator open loop gain model, [18]. The notation, *i*, is a variable used for the plotting (representing the frequency).

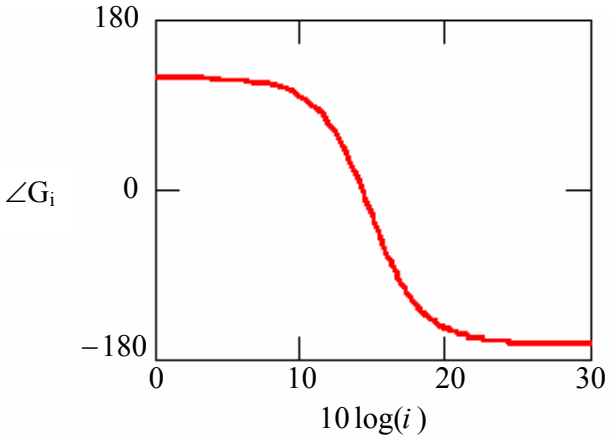


Figure 3.5. The figure shows the oscillator open loop phase model, [18].

The output spectrum of a VCO is therefore composed of bandpass amplified noise. The loaded *Q* of the resonator determines the "quality" of this noise (that is, how "narrow band" this noise is). For convenience, this noise signal is modeled as a sinusoid plus some arbitrary amount of noise. Almost all models use the Leeson approximation, [12].

3.4.2 Phase frequency detector (PFD)

The phase detector generates the error signal required in the feedback loop of the synthesizer. The majority of PLL ASICs use a circuit called a phase frequency detector (PFD) similar to the one shown in figure 3.6, [15]. Compared with mixers or XOR gates, which can only resolve phase differences in the ± π range, the PFD can resolve phase differences in the ± 2π range or more (typically "frequency difference" is used to describe a phase difference of more than 2π, hence the term "phase frequency detector.") This circuit shortens transient switching times and performs the function in a simple and elegant digital circuit.

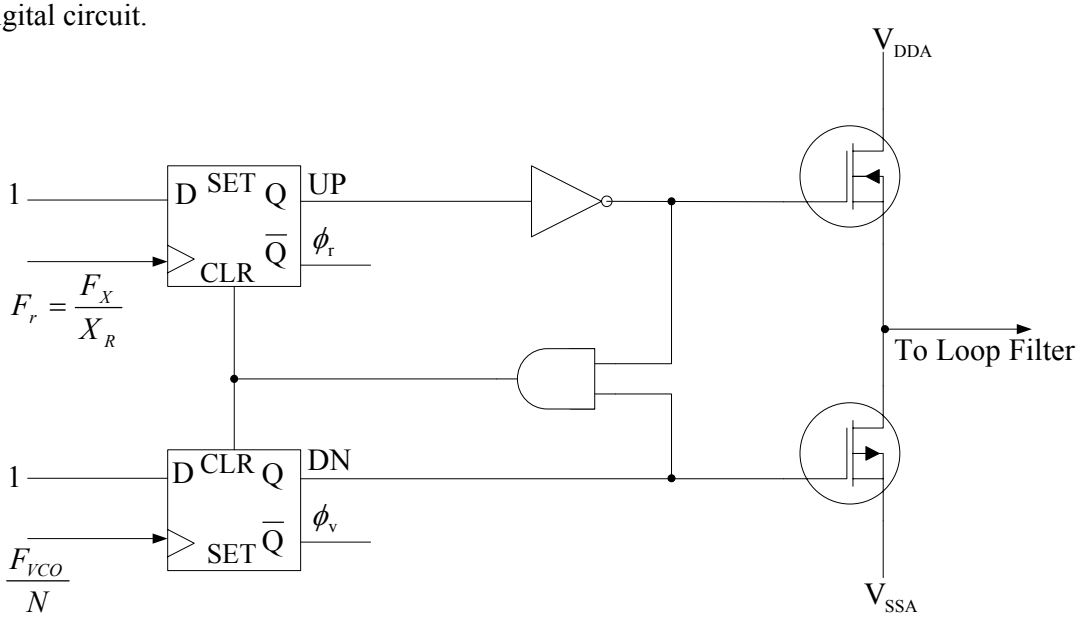


Figure 3.6. The figure shows the phase frequency detector schematic.

The PFD compares the reference signal, F_r with that of the divided down VCO signal (F_{VCO}/N) and activates the charge pumps based on the difference in phase between these two signals. The operational characteristics of the phase detector circuitry can be broken down into three modes: frequency detect, phase detect, and phase locked mode. When the phase difference is greater than ± 2π, the device is considered to be in frequency detect mode. In frequency detect mode the output of the charge pump will be a constant current (sink or source, depending on which signal is higher in frequency.)

The loop filter integrates this current and the result is a continuously changing control voltage applied to the VCO. The PFD will continue to operate in this mode until the phase error between the two input signals drops below 2π.

Once the phase difference between the two signals is less than 2π., the PFD begins to operate in the phase detect mode. In phase detect mode the charge pump is only active for a portion of each phase detector cycle that is proportional to the phase difference between the two signals (see figure 3.7.) Once the phase difference between the two signals reaches zero, the device enters the phase locked state (see figure 3.8.)

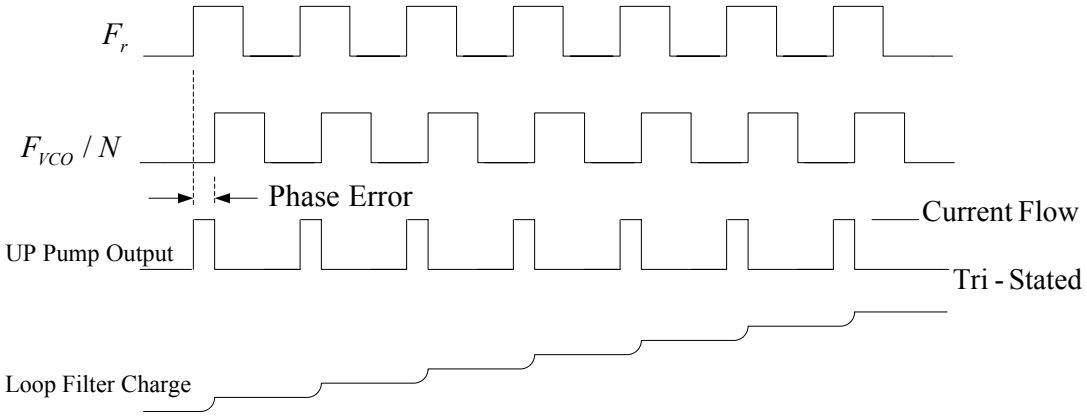


Figure 3.7. The figure shows the phase detector output (voltage, current) waveforms, for $F_{VCO}/N<F_r$.

In the phase locked state, the PFD output will be narrow "spikes" that occur at a frequency equal to F_r. These current spikes are due to the finite speed of the logic circuits (as shown in figure 3.8, D_{OA} blowup) and will have to be filtered so they do not modulate the VCO and generate spurious signals.

3.4.3 Dividers

Dividers constitute a main function in PLL circuits. A PLL circuit needs to cover a very wide range of continuous divisions for the crystal reference and for the VCO. Two types of dividers are used, high speed and low speed.

3.4.3.1 High Speed Dividers

For the high-frequency VCO's (200-2500 MHz), dual modulus dividers are employed to achieve a simple continuous division mechanism. For example, an AMPS phone needs to cover 25 MHz with 30 kHz steps. This requires the generation of about 850 contiguous *N* values.

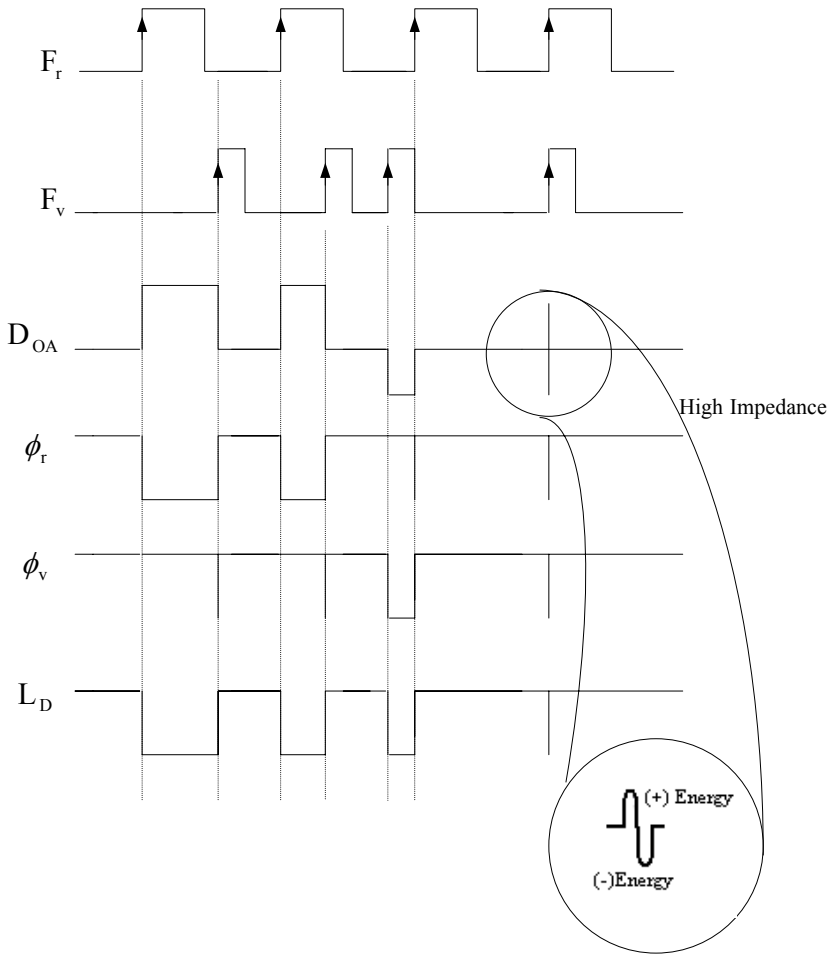


Figure 3.8. The figure shows the phase detector timing waveforms. Relevant input signals are defined in figure 3.2. D_{OA} and L_D are phase detector outputs for the cases shown.

A "*P*/(*P*+1)" dual modulus divider will divide by either *P* or *P*+1 based upon external command. It has a Modulus Control (MC) input port (typically TTL or CMOS) controlling the number of times to divide by *P* or *P* + 1. The lowest contiguous divide ratio for a dual modulus device is given by $P^2 - P$. Specifically, a 16/17 divider allows generation of contiguous divider values above $N = 239$.

Example

A divide value of $N = 960$ is accomplished by dividing the input signal by 16 a total of 60 consecutive times. Changing N to 961 requires that the signal is divided by 16 a total of 59 times and then divide the signal by 17 once, and so on. To generate divisions in the 100-150 range using a 16/17 device there will be some numbers that cannot be generated. A divide ratio of 100 can be gained by dividing twice by 16 and 4 times by 17 ($17 \times 4 + 16 \times 2 = 100$.) However, there is no combination of 16 and 17 that can generate the number 103. To generate contiguous division numbers in this range would require a lower dual modulus (8/9, 10/11, etc). Dual modulus devices typically employ bipolar technology due to current consumption and speed requirements. To run high division numbers and allow lower divisions (lower than P^2-P), tri-modulus and even quad-modulus circuits are used. One common configuration, 64/65/72, is used in a few PLL chips. For a tri-modulus $P/(P+1)/(P+R)$ divider, the minimum continuous divide number, N_{min}, is given by:

$$N_{min} = (P/R + R + 1) \times P + R \tag{3.7}$$

For a 64/65/72 divider $N_{min} = 1096$, compared with $N_{min} = 4032$ for a 64/65 divider.

3.4.3.2 Low Speed Dividers

The second type of divider is the regular programmable counter. These counters typically use CMOS technology, run at frequencies up to 100 MHz, and consume very low power. These counters are used as the reference divider and also as dual modulus control counters.

A complete PLL "N" divider is typically implemented using a dual modulus divider controlled by two programmable counters, usually described as the "A counter" which determines the number of times the input is divided by $P+1$ and the "M counter" which determines the number of times the input is divided by P. The total division ratio for the divider is given by: $N = P \cdot A + (P+1) \cdot (M-A)$.

Note that when A is incremented by 1, M-A decreases by 1 and the total division ratio, N, increases by 1. Note also that the minimum required bit size of the A counter is equal to the bit size of P. For 64/65, the A counter has to be of no more than 6 bits ($64=2^6$). A block diagram of a programmable divider using a dual modulus divider is shown in figure 3.9.

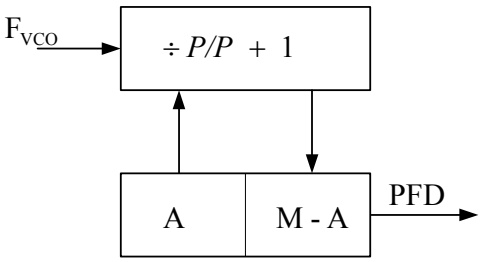


Figure 3.9. The figure shows the programmable divider using dual modulus, [12].

3.4.4 Loop filter

There are two types of loop filters, active and passive. Active loops use op-amps, are usually differential, and allow the synthesizer to generate tuning voltage levels higher than the PLL IC can generate on-chip. The op-amp itself provides the DC amplification necessary to develop a control voltage that is higher than the on-chip supply of the phase detector. Active loops are used in wide band applications that require wide DC voltages to control the VCO. Passive filters are mainly *R*, *C* (resistor, capacitor) elements that connect directly between the PLL ASIC and VCO. Most PLL ASICs use a current source for the output to generate the control voltage. This output is proportional to the phase error (for example: ± 1mA for ± 2π phase error). This "current source" loop filter configuration is the most popular for wireless, narrow-band applications.

3.5 PLL Mathematics

In this section, a short review of basic feedback loop principles and theory is presented, and transfer functions developed to study the effect of various noise sources on output noise. Firstly an important "principle" must be stated: "multiplication of a given frequency by *N* increases the signal's phase noise by *N* or 20 log(*N*)" [15]. Division, conversely, reduces the phase noise by this same factor. This effect can impact the communication system drastically. In the US AMPS or TDMA standard, multiplication by 30000 is required to generate signals in the 900 MHz range from a 30 kHz phase detector frequency. The signal's phase noise is therefore increased by 20 log(30000) ≈ 90 dB. To put this in perspective, the phase noise of the RF signal (compared to the reference signal) has increased by a factor of one billion.

The following example helps to visualize the mechanism of this effect: suppose that a 1 MHz signal has a time jitter (noise) of 1 psec rms. When this signal is multiplied 1000 times to 1 GHz, the output jitter (assuming noiseless counters) stays at 1 psec, but the signal time period has decreased from 1ms to 1ns. Thus, the period-to-jitter ratio has degraded 1000 times or 60 dB.

3.5.1 Feedback loop analysis

The loop equations can be derived by following the closed loop (figure 3.2) path in the Laplace domain as follows:

Let φ_r represent the reference phase (F_r) and φ_o the output phase (F_o). Assume that the loop filter network is denoted as $H(s)$. Then, the output of the phase detector is given by:

$E(s) = (\varphi_r - \varphi_o/N)\, K_d$ [Volts] (The phase detector has a gain, K_d [V/rad]) (3.8)

$\varphi_o(s) = E(s)H(s)K_v/s$ (VCO has a transfer function K_v/s) (3.9)

Solving for φ_o/φ_r, (the effect of the input on the output), results in

$$\varphi_o\varphi_r(s) = \frac{K_v K_d \dfrac{H(s)}{s}}{1 + K_v K_d \dfrac{H(s)}{sN}} = H_1(s) \tag{3.10}$$

For $K = K_v K_d$, the following is obtained:

$$H_1(s) = \frac{NKH(s)}{sN + KH(s)} \tag{3.11}$$

Generally, from linear feedback control theory, it is known that the transfer function for a specific input anywhere in the loop is given by the forward loop gain (from that input to the output point) divided by "1+ the open loop gain". The effect of different inputs (noise or modulation originating from anywhere in the circuit) can be calculated easily using these relations.

Example: If a signal E_ϕ is added after the phase detector to represent the phase detector additive noise, then its effect on the output can be obtained by noting that from this point to the output the forward gain is given by: $K_v H(s)/s$:

$$\frac{\phi_o}{E_\phi(s)} = \frac{K_v H(s)}{s + K\dfrac{H(s)}{N}} = H_2(s) \tag{3.12}$$

$$H_2(s) = \frac{NK_v H(s)}{sN + KH(s)} \tag{3.13}$$

The composite phase noise of the signal generated by the synthesizer can be easily calculated by the sum effect of all noise sources on the output.

Another function of interest is the error function, defined by $(\varphi_o - \varphi_r)/\varphi_r$, and given by:

$H_E(s) = \dfrac{sN}{sN + KH(s)} = 1 - H_1(s)$ and has "high-pass" characteristic.

Interpretation of the basic transfer function $H_1(s)$:

For low frequencies where $s << KH(s)/N$, $H_1(s)$ is approximately equal to N. The loop then behaves as a multiplier (by N) which is exactly what we wanted to achieve. However, when $s >> KH(s)/N$, the transfer function value diminishes, thus acting like a "low pass filter." Beyond a certain frequency which is the loop bandwidth, the output will not follow, or track, the reference phase, ϕ_r. This is an advantage which allows the designer to shape the output noise profile.

Generally, the transfer function H_1(s) has a spectral shape similar to a low pass filter, multiplied by N (see figure 3.10.)

The error function, H_E, implies that at low frequencies (relative to the loop bandwidth), the error will be low; the VCO will be "locked" to the reference. This is desirable since it is required for the VCO to acquire the stability of the reference frequency (crystal).

Overall, these transfer functions show that a PLL "locks" the VCO to the crystal (for accuracy and stability) while rejecting VCO noise close to the carrier. It does this by "shaping" the circuit noise in a low pass manner that decouples the VCO spectral profile from other noise sources.

For loop stability (an important issue in third and fourth order loops), it is necessary that at the frequency where the open loop gain is unity, there will be sufficient phase margin (> 45°) to prevent oscillations.

3.5.2 The Laplace and Fourier transform

The Laplace and Fourier transformations will be used throughout the analysis for the same reason as used in all electronics circuits: they turn differential equations into polynomials, and allow easy interpretation of circuits and their frequency response. The Fourier transform is used for calculating steady state ($s = j\omega$) and the Laplace transform is used for transient analysis.

Fourier transform definition:

$$F(\omega) = \int_{-\infty}^{\infty} f(t) e^{-j\omega t} dt \quad \Updownarrow \quad f(t) = \int_{-\infty}^{\infty} F(\omega) e^{j\omega t} dt \tag{3.14}$$

The steady state (Fourier) response of $H_1(s)$, for $H(s) = 1$ (indicating no loop filter), is calculated to be: ($s = j\omega$)

$$H_1(s) = \frac{K}{j\omega + \frac{K}{N}} \tag{3.15}$$

This is similar to a simple R/C circuit with a pole at $\omega = K/N$

Laplace transform:

$$F(s) = \int_{0}^{\infty} f(t) e^{-st} dt \tag{3.16}$$

Both transformations are linear.

3.5.3 Loop transfer function

The meaning of $H_1(s)$ is discussed here: no loop filter. The response is similar to a simple R/C circuit with a pole at $\omega = K/N$. (This is expected as there's only a single integrator in the loop, the VCO). The transfer function implies that while the (phase) frequency will be multiplied by N, the reference (φ_r) noise affects the output spectrum in a "controlled" way (figure 3.10.)

Example

Assume $K = K_v K_d = 28 \times 10^6$/sec, and the crystal has a noise density of -165 dBc at an offset of 0.1 MHz from the carrier. For $N = 1000$, the output noise at this offset due to crystal noise calculates to: -105 dBc/Hz. However, because of the loop's ability to filter this noise, it can be much better than -105 dBc/Hz. The loop starts to attenuate this noise above 4400 Hz ($K/N = 28 \times 10^6/(2\pi 1000)$) from the carrier at 6 dB/oct. At 100 kHz offset, the loop will attenuate this noise by more 26 dB to below -131 dBc/Hz. It can be concluded from this analysis that a PLL is a narrow band multiplier, having the characteristics of a tracking filter. The bandwidth of this filter, also known as the loop bandwidth can be easily controlled (as discussed in the next section.)

Viewing the error transfer function $H_E(s)$, shows that it has "high-pass" characteristics. Therefore, it can be concluded that the loop "resists" low frequency changes; it "tries to acquire" the characteristics of the reference source. If a signal is injected in order to modulate the VCO (say in FM applications), the loop will resist this disturbance, (see figure 3.10). Therefore, many FM systems, and especially those used in cellular applications, must use a very narrow band loop, so that the voice (300-3400 Hz) spectrum is significantly above the frequency where the loop has an effect (typical 20-30 Hz).

VCO noise can be modeled as additive; this noise will be rejected by the loop within the loop bandwidth.

It is seen that when there is no loop filter, $H(s) = 1$, the loop parameters were determined by K and N. This way, the control of the loop parameters is very limited and has already been set by K and N.

To gain complete control of loop parameters, (mainly bandwidth, noise characteristics and speed), the more common (second order) and in fact the most popular loop structure uses (at least) another integrator, having a transfer function given by:

$$H(s) = \frac{1 + sT_2}{sT_1} \tag{3.17}$$

where $T_1 = R_1 C$ and $T_2 = R_2 C$ (See figure 3.12.)

The new loop transfer function is given by:

$$H_1(s) = \frac{k\dfrac{(1+sT_2)}{T_1}}{s^2 + K\dfrac{(1+sT_2)}{NT_1}} \tag{3.18}$$

Defining: $\omega_n = K/NT_1$ and $\xi = \omega_n T_2/2$ then

$$H_1(s) = \frac{2s\omega_n\xi + \omega_n^{\,2}}{s^2 + 2\omega_n\xi s + \omega_n^{\,2}} \tag{3.19}$$

This is the most common loop transfer function in PLL theory. The loop is of second order (has two integrators) and enables control of its dynamic characteristics, bandwidth and damping, via T_1, T_2, resistors and capacitor. This structure, with minor modifications, is used in most frequency synthesizer designs.

3.6 Natural frequency and loop bandwidth

A normalized second order transfer function is shown in figure 3.10**,** ω_n is referred to as the natural frequency, and ξ is the damping factor, both terms borrowed from control theory.

For low values of ξ, the loop tends to oscillate. This is the reason for not using a pure integrator as a loop filter. Most designers use a damping factor between 0.7 and 2. The loop behavior is similar to many natural phenomena described by similar (second order) differential equations.

The solution of the denominator polynomial shows that:

$$s_{1,2} = -\xi\omega_n \pm \omega_n\sqrt{\xi^2 - 1} \tag{3.20}$$

For $\xi > 1$, settling to lock state will be asymptotic. For $\xi < 1$, it will be asymptotic with oscillation, or "ringing," occurring at a frequency of $\omega_n\sqrt{\xi^2 - 1}$.

The following is a review of the characteristics of this loop (see figure 3.10.)

The loop behaves like a low pass filter that is centered on the carrier instead of DC. (Actually, it is a bandpass tracking filter).

This filter's integrated bandwidth (also referred to as noise bandwidth), is given by:

$$B_L = \sqrt{\int \left| H_1^{\,2}(j\omega) \right| d\omega} = \frac{\omega_n}{2}\left(\xi + \frac{1}{4\xi}\right) \qquad (3.21)$$

This is illustrated in figure 3.10.

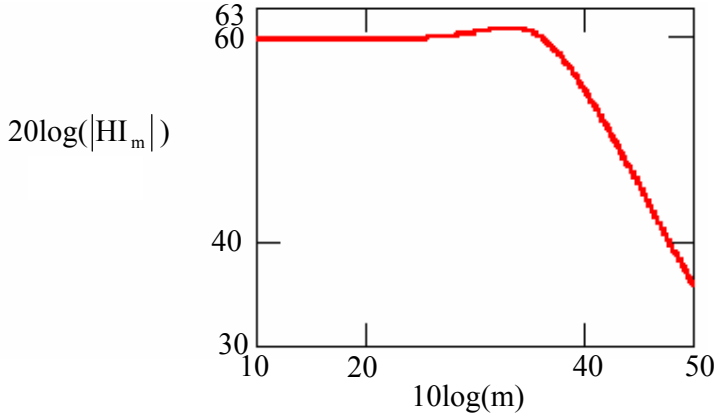


Figure 3.10. The figure shows a second order loop transfer function, $\xi = 0.7$

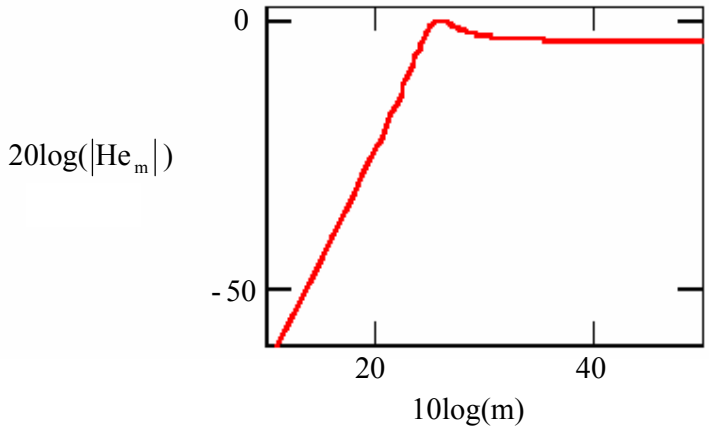


Figure 3.11. The figure shows a second order error transfer function, $\xi = 0.7$. The minimum value for this function is for $\xi = 0.5$ and $B_L = \omega_n/2$.

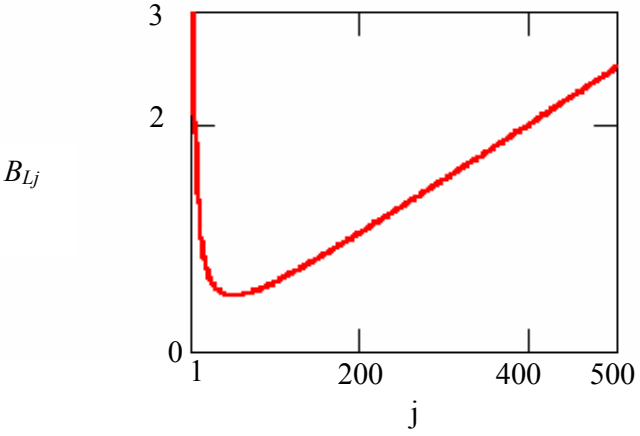


Figure 3.12. The figure shows B_L as a function of ξ (where $j = 100\xi$.)

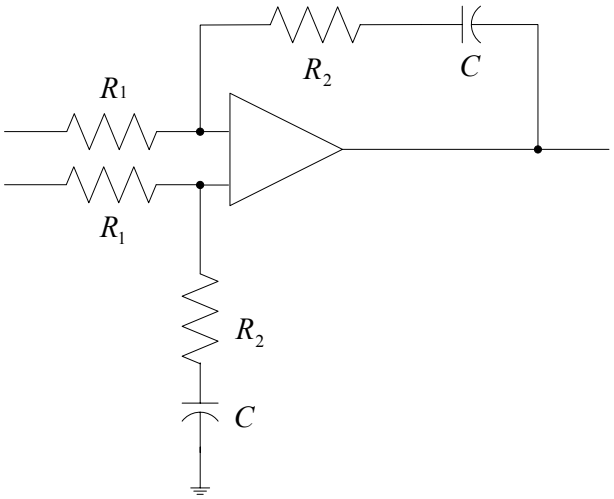


Figure 3.13. The figure shows an active second order loop filter.

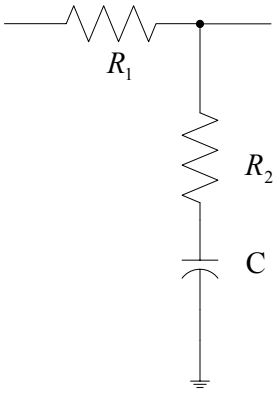


Figure 3.14. The figure shows a passive second order loop filter.

Though ω_n is the natural frequency (the frequency at which the critically damped loop will oscillate when disturbed from equilibrium), it is also an indication of the loop bandwidth; a measure of its dynamic ability to track and follow the carrier as well as reject noise sources. Many designers refer to $\omega_n/2\pi$ as the loop bandwidth. A more fundamental parameter, but not often used, is ω_p, the frequency in which the open loop gain equals 1.

The loop bandwidth also indicates loop dynamics and the speed with which it will lock. The speed relationship (asymptotic behavior) depends on how far the new frequency changed to is, as well as other parameters (among them phase detector characteristics, ξ). Generally, loops with higher ω_n will lock faster. Some of the speeds up mechanisms

actually increase ω_n for the duration of the lock up (acquisition) time, to speed up the acquisition process.

Note that when ξ is very large, the second order approximates first order characteristics as the effect of the capacitor is reduced (for very large R_2, the op-amp transfer function approximates R_2/R_1). This is used in timing circuits to reduce "peaking" in the response.

3.7 Passive loops and charge pump

In many applications, economics forbid the use of an active loop; also an active loop might not be necessary. For example, cellular synthesizers cover only 25 MHz, a 4 % bandwidth. With a VCO that has a K_v = 12 MHz/V, there is no need to use any active interface between the phase detector and the VCO. Passive loops are then used and take the form of a lead-lag network such as the one shown in figure 3.14.

The transfer function of this network $[(R_2+1/sC)/(R_1 + R_2 + 1/sC)]$ is given by:

$$H(s) = \frac{1 + sT_2}{1 + s(T_1 + T_2)} \tag{3.22}$$

As a consequence, the difference in the loop equations is as follows:

$$\omega_n{}^2 = \frac{K}{N(T_1 + T_2)} \qquad \xi = \frac{\omega_n}{2}\left(T_2 + \frac{1}{K}\right) \tag{3.23}$$

In high gain loops, $(1/K << T_2)$, the equations of the active and passive loops converge. Most common for wireless applications, the phase detector output is a current source (also referred to as charge pump) rather than voltage source. The design equations for the second order loop (shown in figure 3.14) are then given by:

$$\omega_n = \sqrt{\frac{K}{NC_1}}$$
$$R = 2\xi\sqrt{\frac{N}{KC_1}} \tag{3.24}$$

where

K_V is in Hz/V

K_D is in A/rad

$K = K_V K_D$ has dimensions 1/secΩ (Note: Ω.Farad = sec)

This network (R/C in parallel with an ideal current source) response is given by:

$$\frac{V_o}{I} = R + \frac{1}{sC_1} \tag{3.25}$$

Therefore, the current to voltage transfer function $Z(s) = V_o/I$, is given by $(1+sRC_1)/sC_1$ (perfect integrator) and the closed loop denominator takes the form:

$$s^2 + \frac{KRs}{N} + \frac{K}{NC_1} \tag{3.26}$$

Now ω_n and ξ (shown above) are easy to derive.

Most PLL ASICs use a current source output for reasons listed below.

- It is the most convenient way to generate the analog output function of the phase detector with digital three-state devices (current sources, charge pump structure).
- Assuming an ideal current source, the design has a real second integrator ($1/s$) in the loop, compared with the voltage passive network.
- Reference spurious signal attenuation by a third order loop structure is easily attained by the addition of a single capacitor, (C_2 in Figure 3.14.)
- A single ended filter structure provides economy, compared to a differential circuit, for active loops.

As mentioned, most practical designs add a shunt capacitor (C_2) between the current source output and ground (third order loop) to help attenuate spurious signals caused by reference spikes leaking out. The new network impedance transfer function is given by:

$$Z(s) = \frac{1 + sRC_1}{s^2 RC_1C_2 + s(C_1 + C_2)} \tag{3.27}$$

For third order loops, (and higher), the loop phase margin needs to be calculated, to ensure stability. (Note that second order PLLs are inherently stable, if $\xi > 0$). Fourth order loops add an extra R/C for additional spurious filtering.

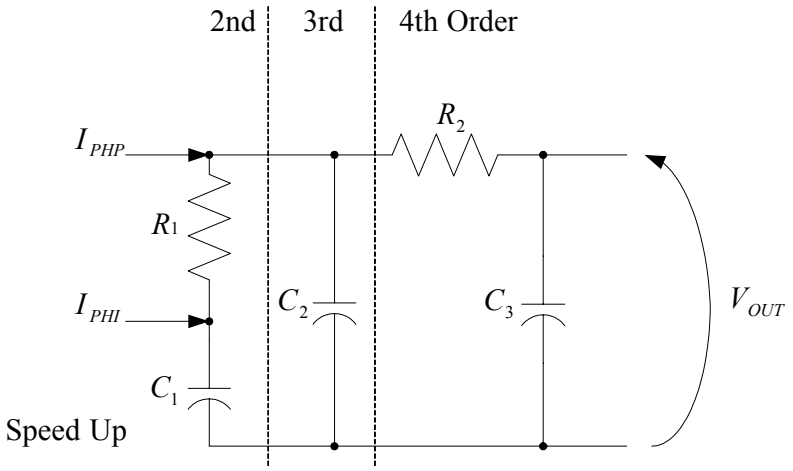


Figure 3.15. The figure shows a loop filter for current source (charge pump) phase detector.

3.8 Lock-up time and speed-up

3.8.1 Initial lock-up

Due to the importance lock time has gained in the last few years, special techniques and circuits have been devised to improve this parameter. A PLL circuit, being a feedback loop, theoretically never achieves steady state, but always approaches that state asymptotically. Thus lock time is usually defined by approaching the final state to within some defined margin (i.e. ± 1 kHz). In digital modulation applications, the receiving modem always has some frequency and phase tracking capability, so the frequency error tolerance is based on overall system performance requirements. In second and third order loops, it can be shown that switching speed depends on ω_n and ξ.

When hopping by "*dF*" Hz and settling to "*df*" Hz away from the new frequency, the system will asymptotically converge to zero error such that *df*/*dF* is proportional to $\exp(-t\omega_n\xi)$, thus the switching time, T_{sw}, is given by:

$$T_{sw} = -\ln(\xi\delta)/\omega_n\xi \qquad (3.28)$$

Example

Let: $df = 1$ kHz $dF = 20$ MHz $\xi = 1$

Then: $\delta = 1/20000$ and $T_{sw} = -\ln(1/20000)/\omega_n \approx 10/\omega_n$

The VCO will settle in $10/\omega_n$ seconds to within 1 kHz of the final frequency when hopping 20 MHz.

The speed with which the synthesizer can hop from one frequency to another is an increasingly important parameter. It is applicable as a diversity technique (narrow band signals suffer fading effects that are frequency dependant, hopping frequencies can attenuate this effect) as well as a networking protocol. Rather than operating in Frequency Division Multiplex mode in which each channel has a dedicated frequency, all channels are changed periodically in frequency to reduce the effects of multi-path and external interference.

3.8.2 Speed-up mechanisms

It is seen that the loop parameters, ω_n and ξ, determine speed. In most cases, the loop is designed for bandwidth and phase noise profiles. Sometimes, the outcome does not provide sufficient speed. To improve this parameter, simple and effective speed up mechanisms has been added to many ASICs. Improvements of up to 5:1 are possible using simple circuitry.

One speed up mechanism performs “pre-tune” of the VCO to the desired frequency. This will expedite the time it takes the VCO to slew up (or down) and will bring it to lock proximity, where the loop can start settle and lock fast. Another technique is to increase ω_n for a short time and speed up the “acquisition” time. This can be done by charging the largest capacitor in the loop filter directly, or even increasing the charge current in this short time, to expedite the charging process. One popular technique is to create a separate port that charges the capacitor in the transition. The “PHI (ϕ)” terminal of the TRF 2052 is a good example of this. Another method is implemented by an analog switch that bypasses the shunt resistor and allows charging of the capacitor directly. Terminal “SWM” in TRF 2020 is an example of this method. Speed up mechanisms can improve lock times by a factor of 1.5-5. Note that in the speed up mode, care must be taken to insure that the loop remains stable.

3.9 Loop order and type

Loop order is the number of poles in the closed loop equation denominator. Loop type is the number of poles at "0" in the open loop denominator. The third order loop filter is demonstrated in figure 3.16, has the open loop transfer function:

$$K\frac{(1+sT_2)}{s^2}(1+sT_1) \text{ and is of type 2 and order 3} \tag{3.29}$$

3.10 Loop stability and phase margin

Control theory shows that for stability, the open loop phase at gain = 1 (0 dB) must be in excess of 180°.

Since the feedback is negative, there is a feedback inversion of 180°. The two poles of the third order loop denominator shift the signal by another 180° $\{(j\omega)^2=-\omega^2\}$, for a total of 360°. Therefore an extra phase shift is necessary.

Careful location of the extra pole and zero $[(1+sT_2)/(1+sT_1)]$, will ensure stability. Phase margin is defined as the open loop phase difference from 180 degrees at the frequency at which the open loop amplitude gain is unity. To ensure loop stability, the usual requirement is that the system have at least 40-45 degrees of phase margin. If $C_2 < C_1/10$, this condition is easily met and is the reason this rule of thumb exists. The two controlling time constants are now $T_1 = R_1C_1$ and $T_2 = R_1C_1C_2/(C_1 + C_2)$. The open loop transfer function is:

$$H_{OL}(s) = T_1K(1 + sT_2)/[s^2 \cdot C_2N(1 + sT_1)T_2] \tag{3.30}$$

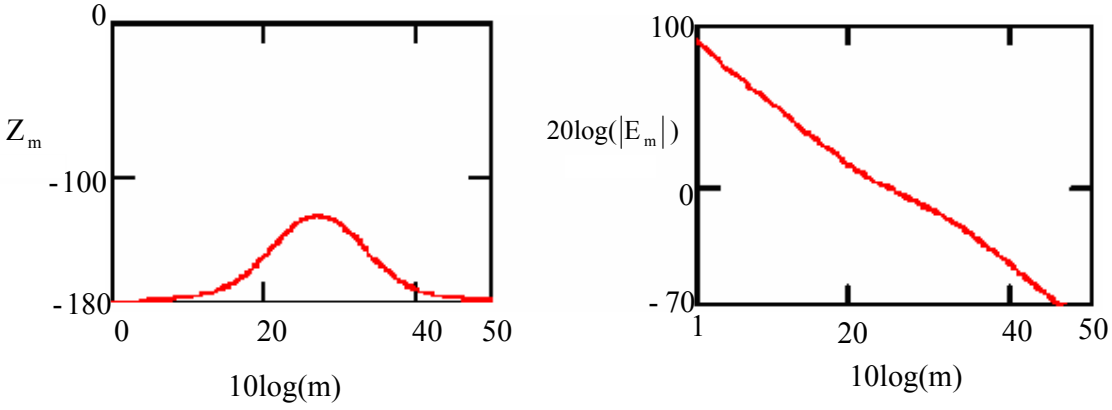
The phase margin is given by:

$$\phi_M = 180 + \arctan(\omega T_2) - \arctan(\omega T_1) \tag{3.31}$$

Sometimes, the third order structure does not provide sufficient reference spurious signal rejection. One option is to add an additional R/C circuit to further attenuate the reference spectral line. This will make the loop a fourth order type. Stability requires that the pole of this additional R/C structure be at least 10 times ω_n; thus requiring $1/(R_2C_3) > 10\omega_n$ (see figure 3.15). Following this rule ensures an additional phase shift of no more than 4-5°. A

simulation program is useful to calculate the total open loop transfer function and its phase shift before the design is implemented. This will insure that at the frequency where gain is 1 the phase margin is still at least 40-45°, including manufacturing tolerances. (3.32) shows the transfer function:

$$H_4(s) = \frac{T_1 K(1+sT_2)}{T_2 s^2 N(1+sT_1)(1+sR_2C_3)} \tag{3.32}$$



(a) (b)

Figure 3.16. The figure shows (a) the open loop phase of a third order loop, and (b) the open loop gain of the third order loop.

3.11 Active and passive loop summary

The following is a short summary of various loop structures and design procedures. When possible, passive loops are used for simplicity and economy; otherwise, active loops using op-amps must be employed. In most cellular and PCS applications, the overall bandwidth is narrow (3-5%) and the output voltage from the PLL chip is sufficient to cover the band (including manufacturing tolerances). These use passive third and fourth order loops. If wide-band synthesizers are necessary, (Satcom applications require 10-15 V for the VCO control) a larger (than PLL chip supply) control voltage must be generated and op-amp integrators are used. When using op-amps, differential connection is implemented. Low noise op-amps will not add significant noise to the PLL circuit.

For third order passive PLL design (most wireless applications):

Given K_v in rad/secV and K_φ in A/rad

$\omega_n = (K_v K_\varphi / N C_1)^{0.5}$ $\xi = 0.5 \cdot R_1 (K_v K_\varphi C_1 / N)^{0.5}$ and $C_2 < C_1/10$

T_{sw}, switching time for convergence to df for a dF excursion is given by:

$T_{sw} = -\ln(\xi df/dF)/\xi\omega_n$

If another R/C is required to further attenuate reference spurious signals, it should be ensured that: $R_2C_3 < 1/10\omega_n$

Phase margin for a third order loop: $\phi_M = 180 + \arctan(\omega T_2) - \arctan(\omega T_1)$

For second order active loop:

$$\omega_n = 0.5\frac{K_v K_d}{NT_1}$$

$\xi = \omega_n \cdot T_2/2$

Here, K_v is in rad/secV and K_d in V/rad.

3.12 Modulation

Amplitude Modulation (AM) and Phase Modulation (PM) are usually performed outside of the phase locked loop. AM is performed by multiplying the carrier, $\sin(\omega_0 t)(1+m\sin(\omega_m t))$, using mixers or other analog multipliers. PM is performed by complex multiplying, using quadrature modulators.
This yields: $\sin(\omega_0 t)R(t) + \cos(\omega_0 t)R_{\_}(t)$ [$R(t)$ and $R_{\_}(t)$ are the quadrature components of the base-band information.]

Generally, $R_{\_}(t)$ will be the Hilbert transform of $R(t)$. A variety of monolithic wide band quadrature modulators are available from various manufacturers. (The TRF 3040, soon from TI, is a fractional-N monolithic PLL ASIC with an on-board quadrature modulator). $R(t)$ and $R_{\_}(t)$ are usually generated from a ROM or other digital memory that calculates the exact values and generates the analog signal for modulation via a digital to analogue converter (DAC)

Frequency modulation (FM) can be performed by modulating the VCO directly. If a signal, V_{FM}, is injected after the loop filter on the input control line to the VCO, its transfer function is:

$$\frac{\varphi_o}{V_{FM}} = \frac{K_v / s}{1 + \frac{KH(s)}{sN}} = \frac{NK_v}{sN + KH(s)} = H_{FM}(s) \qquad (3.33)$$

For a second order loop, calculating (frequency) $df_0 = \mathrm{sd}\varphi_0/2\pi$.

$$sH_{FM}(s)/2\pi = s^2 G_L/(s^2 + 2\omega_n \xi s + \omega_n^2) \qquad (3.34)$$

where G_L is a constant.

Within the loop bandwidth, the modulating signal will be attenuated (s^2 in the denominator). Two options can be utilized to compensate for the loop attenuation, depending on the application:

- The loop bandwidth is made very narrow, as in cellular FM. Beyond the loop bandwidth the transfer function becomes G_L, (for $s >> \omega_n$, $s^2/(s^2 + 2\omega_n\xi s + \omega_n^2) \approx 1$) a constant, and will not affect the modulator. In FM cellular, the voice spectrum is greater than 300 Hz, and loop bandwidth in the order of 30-50 Hz.

If the loop bandwidth is kept somewhat wide (more than 15 - 20% of the modulating frequency), then the effect of the loop must be compensated. This can be done by passing the modulating signal through a network that compensates (pre-distorts) for the transfer function. Usually, this takes the form of an integrator. More complex schemes can be applied to improve low frequency response by modulating (injecting signals) at more than one point (VCO input and PFD output.)

3.13 Phase Noise

Phase noise is probably the major technical concern of frequency synthesis design. An overall radio specification will impose significant requirements on size, power dissipation, voltage requirements, cost and spectral purity. Of all the requirements, phase noise is the most challenging specification in synthesizer design. This section describes the definition of various interpretations of phase noise, derives the equations necessary to calculate various noise sources and offers techniques to reduce phase noise and its effect on communication channel performance.

3.13.1 Definitions and conversions

Ideal deterministic waveforms, expressed as $s(t) = A\sin(\omega_0 t)$, do not exist in the real world. All real signals are narrow band noise. Thus, phase noise is our method of expressing the signal's spectrum. An ideal signal has a spectral representation of $S(\omega)=A\delta(\omega-\omega_0)$; its total energy is concentrated in a single frequency. Real signals have a spectral distribution, and their energy is spread. The better the signal's quality, the more energy is concentrated close to the carrier.

Typically, let $S(t) = A(t)\sin(f(t))$. Amplitude noise, $A(t)$, can usually be contained to relatively low levels, with a noise density lower than -150 dBc/Hz. The more critical issue

is phase noise, $f(t)$. The terminology (-dBc/Hz) suggests that signal perturbations caused by noise have a statistical spectral density measured in relative power to the signal's total power. –150 dBc/Hz means that in 1 Hz bandwidth at specified offset (Hz) from the carrier, the (single sideband) noise power is 10^{-15} of the total signal power. Low frequency offset noise (from DC to 100 Hz offset from the carrier in wireless) is generally attributed to the crystal oscillator slow drift caused by aging, temperature and flicker factors. This is the "long term" noise, mostly caused by crystal stability and noise, which we deal with by temperature compensation, crystal aging or using higher tolerance crystals. This noise can be tracked by the receiving end, which is always equipped with some phase and frequency tracking capability. A more important concern is sometimes called "short-term" noise.

Short-term noise contains dynamic spectral characteristics that the receiver cannot deal with and thus becomes part of the communication system noise. Phase noise can also be viewed as a type of frequency modulation. When detected, there will be low and high frequency components. One can determine what threshold of FM noise can be tolerated simply by the communications application. In voice applications, frequency modulation less than 20 Hz is not audible so this can set the noise threshold at 20 Hz. Of course, if noise were to affect the communications system from a 1 Hz or even a 0.1 Hz offset, the requirements of signal purity would increase. The higher the signal purity, the more concentrated the signal energy is at the exact carrier frequency. In a statistical sense, a lower noise signal will have a lower standard deviation in frequency or phase perturbation.

The noise spectrum is characterized by its single side band (SSB) noise density, the function, $L(f_m)$. Note that since the noise spectrum is symmetrical around the vertical axis, the total noise is actually twice the single sided noise density. In the time domain, phase noise is expressed as jitter, and usually measured in radians, degrees, or seconds (psec) rms. FM theory provides an intuitive description of this effect. Suppose a signal is phase or frequency modulated by a sine-wave given by:

$$S(t)=\sin(\omega_0 t+ m\sin(2\pi f_m t))) \tag{3.35}$$

where ω_0 is the carrier,

f_m is the modulating frequency, and

m is the index of modulation ($m = df_{max}/f_m$).

The sideband (noise) power spectrum of such a signal is determined by Bessel functions and depends only on the index of modulation, m. When m is very small (< 0.1), the Bessel

coefficients of higher order (>1) become negligible. Then, the magnitudes of the two significant sideband spectral lines that appear around the carrier are $m/2$ (voltage) or $m^2/4$ (power) each.

The jitter of the carrier ω_0 can be calculated when corrupted by $m\sin(2\pi f_m t)$. Since m is the peak phase deviation level in radians, this will calculate to $\frac{1}{2}m^2$ rad^2 rms jitter. Note that the total power of the two sidebands, (showing at offset of $\pm f_m$ from the carrier, each being $m^2/4$), is $m^2/2$. So without laborious mathematics, it can be inferred that for small values of m, i.e. $m < 0.1$, the (integrated) power density of the noise is equal to its phase jitter in rad^2.

This can be extended from spectral lines to continuous spectral noise distribution with no loss of generality. The SSB phase noise density of the signal expressed by the function $L(f_m)$, is exactly what is measured on a spectrum analyzer when the signal spectrum is obtained (see Figure 3.17). Phase jitter can be computed by determining the area under the graph (integration).

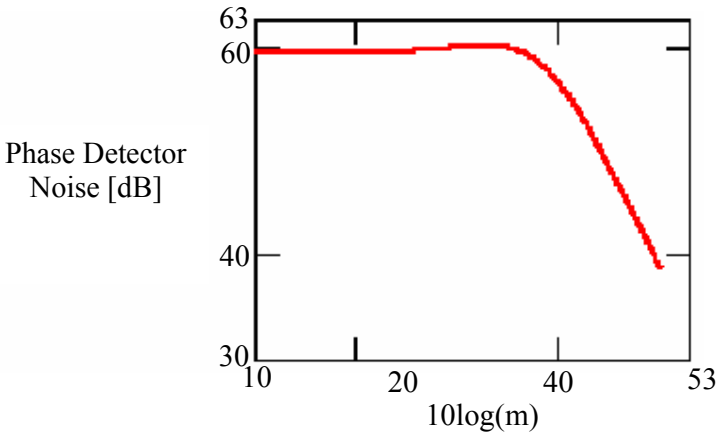


Figure 3.17. The figure shows a crystal phase detector noise transfer function, $N = 1000$

Example:

A 1000 MHz signal is FM modulated by a 10 kHz signal with peak deviation of 300 Hz

One can calculate the spurious signal level and the jitter directly:

Let $m = 300/10000 = 0.03$

$S(t) = \sin(2\pi\omega_0 t) + 0.03 \sin(\omega_m t)$ has a jitter of ± 0.03 radians peak. Therefore jitter is calculated as follows:

$$\varphi_N = \frac{0.03}{\sqrt{2}} = 0.021 \text{ rad rms}$$

The signal spectrum will consist of a carrier (1000 MHz) and two sidebands, at ± 10 kHz from the carrier, both with a relative level of:

$10 \log(m^2/4) = -36.5$ dBc

Total sideband noise is -33.5 dBc = 20log(0.021)

Thus it is inferred that for low m, the phase jitter can be calculated directly from the noise spectrum, phase noise or spurious signals.

Example:

If the carrier has 6 spurious signals at different offsets from the carrier, each at -40 dBc, one can calculate phase jitter as: $\varphi_N^2 = -40 + 10 \log(6) = -32.2$ dBc.

Therefore the rms phase jitter will be:

$\varphi_N = -32.2/2 = -16.1$dBc $\Rightarrow 10^{-1.61} = 0.0245$ rad or 1.4° rms.

Time jitter can be calculated from phase jitter as φ_N/ω_0.

3.13.2 The effect of phase noise on system performance

Phase noise is a critical wireless issue because of its effect on the total communication system and network performance. The following serves to summarise.

- Phase noise is part of the communication channel noise. Excess phase noise causes potential errors and adds to the channel noise.
- Channeling, accuracy and co-channeling are major considerations in wireless networks.
- Frequency re-uses and low mutual interference is the basis for all cellular telephony.
- Spurious signals and excess phase noise can cause interference with other users.
- Spectral density and the scarcity of bandwidth force government regulators and communications designers to open up higher frequency bands (an example is the PCS band in response to the crowded cellular band.) At these higher frequencies, the phase noise requirements are more difficult to achieve mainly due to the higher multiplication ratios.

3.14 Multi-loop design

Sometimes the simple single loop design will not be sufficient even with fractional-*N* technology. In this event using multiple loops becomes an option to reduce the division ratio, thus assisting to obtain even lower phase noise.

Very complex schemes can be employed to reduce the division ratio resulting in very substantial phase noise improvement. It is possible, at least in theory, to design the circuit to perform at a noise level equal to the noise level of the multiplied crystal (at 1 GHz, loss of no more than 40 dB if the reference is 10 MHz.) An example using the TI TRF 2050 is shown below (see figure 3.18.)

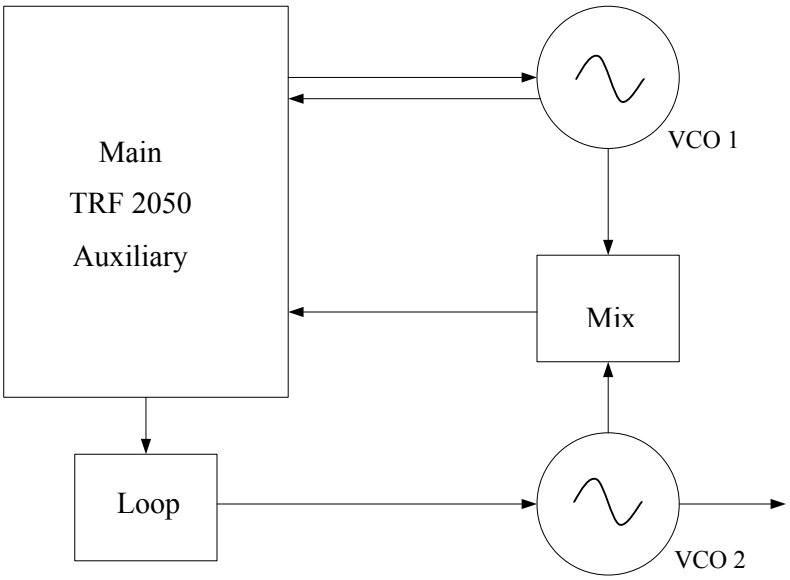


Figure 3.18. The figure shows a mix and count-down dual PLL, [18].

VCO_1 is an auxiliary, using the main PLL section and a high reference frequency, say, 480 kHz. The loop can be wide, and excellent phase noise performance can be achieved, some 15-20 dB better than with a lower reference. Then VCO_2, the one used to generate the output frequency, is mixed down with VCO_1 to generate a low frequency, say 9.6-10.05 MHz. The product then is connected to the Auxiliary input, where it is compared with F_r =30 kHz to produce a 30 kHz step in the output. If VCO_1 covers say, 960 (0.48 × 2000) to 979.2 (0.48 × 2040) MHz then the combined output will generate 969.6 to 989.25 MHz with 30 kHz step.

The division ratio of the main loop has been reduced to 2000 and the auxiliary loop to (320 - 335), significantly lower than a single loop (division will be in the 960/0.03 = 32000 range). Phase noise improvement will be in the 20 dB range. The price, of course, is an increase in complexity and cost. There are a variety of dual and multi-loop designs. This specific example is also referred to as “mix and count-down” architecture.

CHAPTER 4: SYSTEM LEVEL DESIGN

4.1 Bluetooth technology system specifications

Bluetooth technology allows for the replacement of the many proprietary cables that connect one device to another with one universal short-range radio link. Bluetooth radios are designed to operate in the unlicensed ISM band, approximately 2.4 -2.5 GHz. In order to minimize system degradation due to outside interference the system employs a frequency hopping scheme. In addition, the Bluetooth transceiver employs:

• Gaussian filtered binary FM modulation, GFSK,

• gross symbol rate is 1 Msym/s, and

• a time-division duplex scheme.

The synthesizer of this dissertation will eventually form part of a single chip transceiver system – this is a predominant requirement to reduce cost and size. As shown in figure 4.1, currently – ICs that are on the market often have capacitors & inductors placed external to the transceiver.

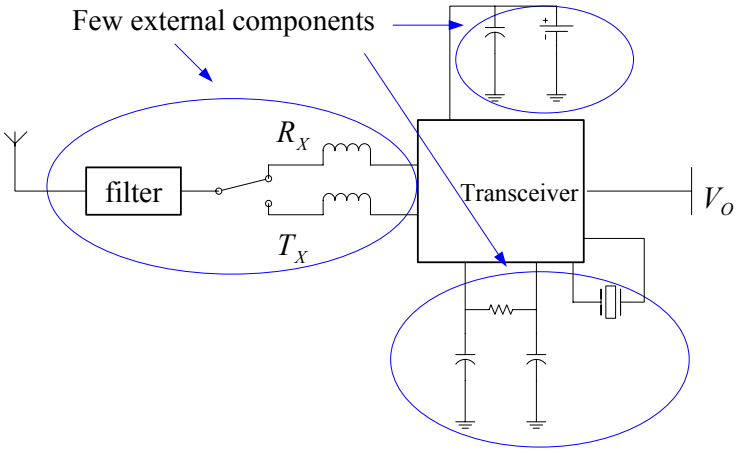


Figure 4.1. The figure shows the typical implementation of a Bluetooth transceiver. Traditionally, many components of the transceiver are placed external to the transceiver.

According to the Bluetooth specification, and in keeping with section 15.247 of the FCC rules, Bluetooth transceivers employ the following:

- 1600 hops/s,
- 79 (2.402 - 2.480 GHz band) channels depending on place of deployment, and
- 1 MHz spacing (220 μs switching time)

Bluetooth systems also utilize fast acknowledgment, FEC (Forward Error Correction) for improved reliability, and to allow for voice communication.

Bluetooth transceiver characteristics have similar regulations to the IEEE 802.11 standard. The frequency specifications cover all 2.4 GHz ISM bands, and are mainly used for short range communication (relaxed linked budget relatively to other low power narrowband ISM band transceivers) applications. As depicted in table 4.1, Bluetooth transceivers are categorized into 3 power classes.

Power class	Maximum output power	Minimum output power	Minimum output power*	Power Control
1	100 mW (20 dBm)	N/A	1 mW (0 dBm)	4 to +20 dBm
2	2.5 mW (4 dBm)	1 mW (0 dBm)	0.25 mW (-6 dBm)	-30** to 0 dBm (Optional)
3	1 mW (0 dBm)	N/A	N/A	-30** to 0 dBm (Optional)

*Minimum output power at maximum power setting.
**The lower range limit of -30 dBm is not mandatory and may be chosen according to application needs.

Table 4.1. The table shows the three Bluetooth transceiver classes.

Other specifications[1] that will be aimed for the synthesizer are listed below.

- As discussed in chapter 2, phase noise can lead to the corruption of the wanted signal by an effect called “reciprocal mixing.” The local oscillator system phase noise performance will be less than -80 dBc/Hz (with respect to the centre frequency) to reduce the “reciprocal mixing” effect.
- As also discussed in chapter 2, in addition to the phase noise, the output of the frequency synthesizer may contain sidebands. These can result in an interference signal that affects the desired signal. To reduce these effects, the sidebands must be approximately 60-70 dB below the carrier.
- The maximum supply current will not exceed 60 mA.
- Operation of the system will require a supply voltage of 3 to 5 V.
- The system lock-in time will be less than 1 ms. This is a typical requirement in communication systems that use FHSS.

[1] The Bluetooth specifications are listed at http://www.bluetooth.com/dev/specifications.asp.

4.2 Synthesizer architecture

In this dissertation, the dual-loop in series architecture approach is adopted. As discussed in chapter 2, this type of architecture offers excellent output spectrum purity and fast switching speed.

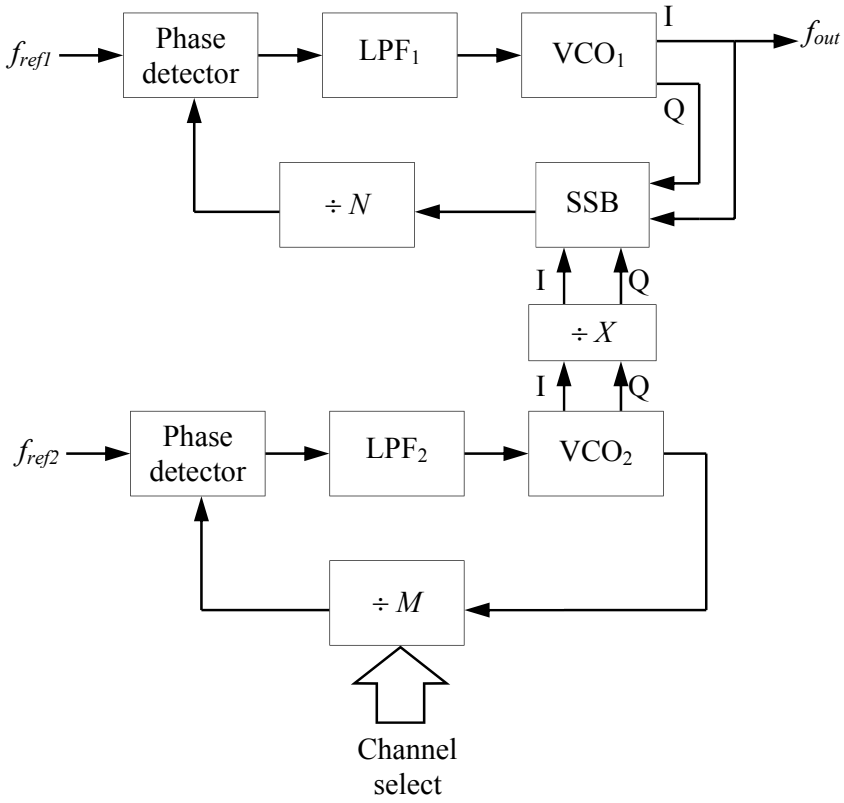


Figure 4.2. The figure shows the concept design of the dual-loop architecture, [1]. Counter X is added, [3].

The unwanted sidebands resulting from mismatches and non-linearities of the SSB mixing can be alleviated by placing the SSB mixer inside the feedback loop. The sidebands at the mixer output are suppressed by the low pass filter of the upper loop and the prescalar, N. The SSB mixer is used to subtract the output frequency of VCO$_2$ from that of prescalar, X and to suppress the unwanted sideband during mixing. The resulting output frequency can be calculated as follows:

$$f_{out} = f_{OFF} + M\frac{f_{REF}}{X} = Nf_{REF} + M\frac{f_{ref\,2}}{X} \tag{4.1}$$

The upper loop provides a large offset frequency $f_{OFF} = N \times f_{ref1}$ and hence it helps to reduce the division ratio in the programmable counter (M). The X-counter between the two loops is used to release the phase noise requirements of the VCO$_2$ with the expense of its

wider tuning range. It also helps to increase the reference frequency (f_{ref2}) of the lower loop. Each divide-by-2 counter can provide 6 dB reduction of phase noise of its output carrier comparing to its input and thus, the value of 4 in prescalar *X* can provide approximately 2 dB reduction of phase noise of the lower loop output signal, [3]. Moreover, the prescalar *X* also attenuates the sidebands resulting from the reference source of the lower loop. The phase noise performance of VCO_2 at the offset far from the carrier is further alleviated by the low-pass filter in the upper loop. The reference frequency (f_{ref1}) of the upper loop is 100 MHz and it is large enough to provide fast settling of the upper loop and enough suppression of the reference spurs by the upper loop filter.

The settling time of the synthesizer mainly depends on the settling of the lower loop and thus the lower reference (f_{ref2}). Very basic frequency planning shown in figure 4.6, the output frequency of the synthesizer can be tuned from 2400 MHz to 2500 MHz and the minimum required programmable value of counter *M* can change from 500 to 1000. The required tuning ability of VCO_2 is as large as 50 % with a 600 MHz center carrier while that of VCO_1 is only 1% with a 2450 MHz center carrier.

4.3 Frequency planning & sub-system level design

This section aims to summarize the requirements of each sub-system. The first concept design is shown in figure 4.2. To complete the design, each subsystem (represented by a block in the first concept design) is first realized. Appropriate input and output loading (for example using a capacitive output load of 10 pF) is used where it is anticipated that loading may affect performance. The next few sub-sections summarize the requirements of the various subsystems.

4.3.1 Digital Subsystem 1: Phase frequency detectors (PFD_1 & PFD_2)

Two phase detectors are required for the concept design shown in figure 4.3. As proposed, [19] identical phase frequency detectors (PFD) will be used in the two loops. The PFD will consist of a charge pump as an integral part of the design.

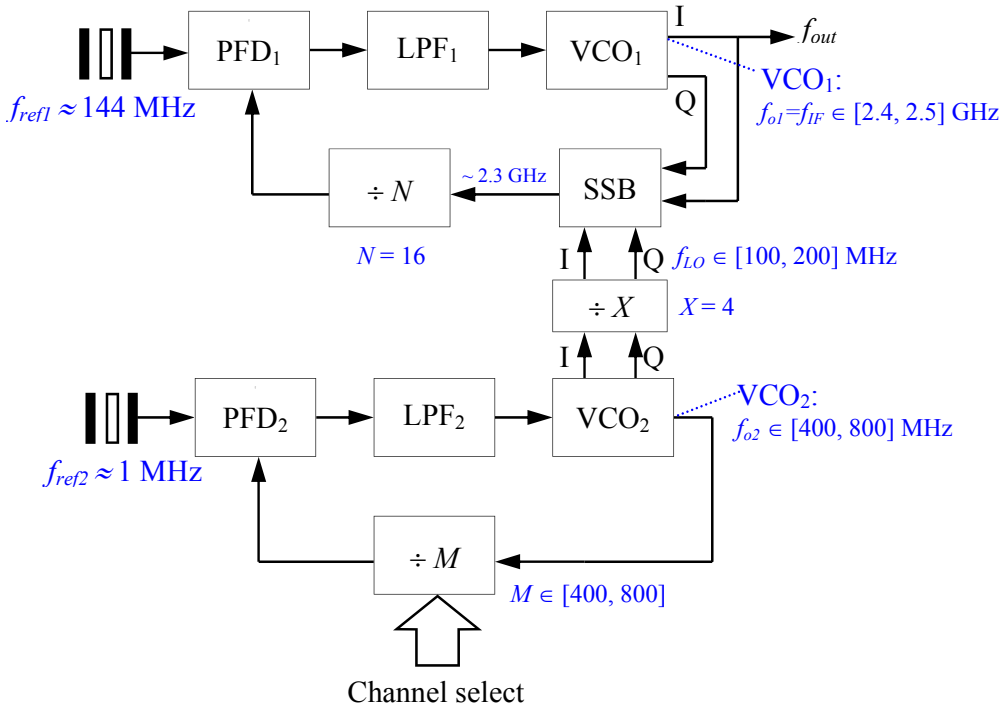


Figure 4.3. The figure shows the basic frequency planning of the figure 4.2.

4.3.2 Digital Subsystem 2: Fixed frequency divider (÷ *N* and ÷ *X*)

The divide by N subsystem can possibly be achieved by using two series divide by X subsystems. The input frequency to the divide by N subsystem is much greater than the divide by X subsystem. Thus, if the above series configuration of dividers is to be used then the dividers must be made to be able to accept high input frequencies.

4.3.3 Digital Subsystem 3: Programmable divider (÷ *M*)

The programmable divider will have an interface to the user. Either computer or manual (hence, a parallel programming interface) should be possible.

4.3.4 Analogue subsystem 4: Voltage controlled oscillator (VCO_1)

This VCO is part of the high frequency loop. With high frequency ($f_{o1} \in [2.4,2.5]$ GHz), a narrow tuning range of about 5 %, and a frequency range, $\Delta f = 100$ MHz is required. An LC oscillator may be used to best achieve the required narrow tuning range as well as the high frequency, [20]. Both in– and quadrature– phase output signals are required (as they eventually become the input to the SSB mixer).

4.3.5 Analogue subsystem 5: Voltage controlled oscillator (VCO_2)

This VCO is part of the low/tuneable frequency loop. With lower frequency ($f_{o2} \in$ [400, 800] MHz), a wide tuning range of about 50 %, and a frequency range, Δf = 400 MHz is required. A ring oscillator may be used to best achieve the required wide tuning range at lower frequencies, [20]. Both in- and quadrature- phase output signals are required (as they eventually become the input to the SSB mixer).

4.3.6 Analogue subsystem 6: SSB Mixer

This subsystem simply takes the signals from the two VCOs and "mixes" it. Traditionally, mixing produces two sidebands (upper and lower sidebands). However, as shown in figure 4.3, only one of the two sidebands are required. Hence, only a single sideband (SSB) is required. To generate SSB, firstly a DSB mixer using translinear principles is realized. Several techniques exist to convert DSB to SSB, [5]. The final mixer output should just be the lower sideband (LSB).

4.3.7 Analogue subsystem 7: Loop filter/Low pass filter (LPF_1)

The VCO is controlled from the LPF output. This output needs to be DC. The loop filter also serves to filter several high frequency signals that may be generated due to the highly nonlinear behaviour of the SSB mixer. The loop bandwidth is typically limited to one tenth of the reference frequency due to stability requirement, [1]. Either active or passive implementation can be done.

4.3.8 Analogue subsystem 8: Loop filter/Low pass filter (LPF_2)

All specifications are the same as LPF_1, except the cut-off frequency, which depends, among other factors, on the reference frequency of the lower PLL (PLL with the variable divider).

4.4 Mathematical modelling

As per the mathematics of the previous chapter, the loop was modelled for simulation in SIMULINK, MATLAB.

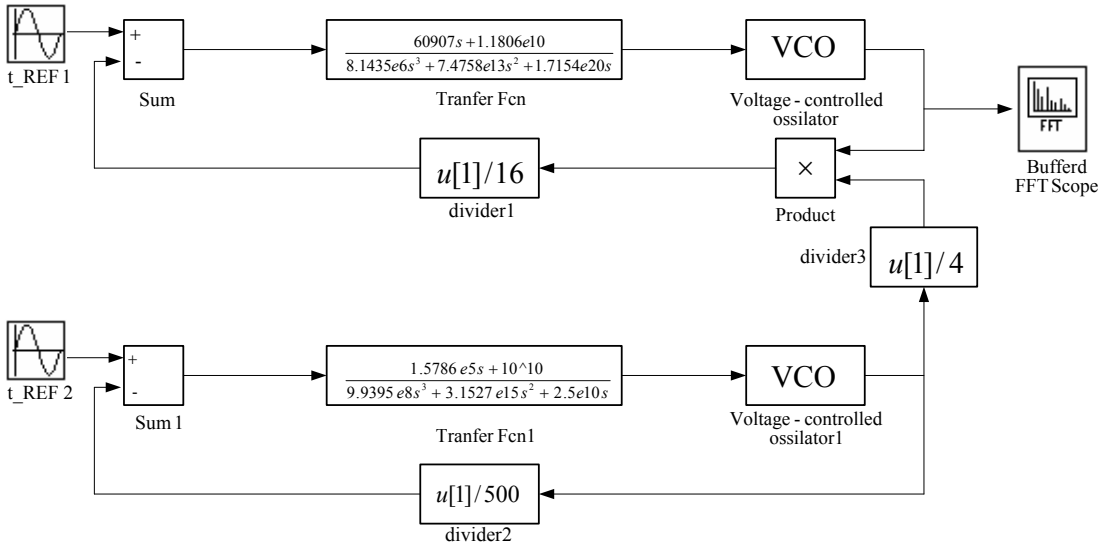


Figure 4.4. The figure shows the SIMULINK model of the synthesizer. This model was constructed using the signal communications toolbox provided in SIMULINK.

The dual loop architecture is simulated in MATLAB. The input of the primary VCO is shown in figure 4.5, the simulation result shows that the settling time improved to be less than 30 µs. The frequency domain analysis was also accomplished. Figure 4.5 shows the output as obtained on the FFT (Fast Fourier Transform) scope in figure 4.4. From this, it is clear that the desired frequency range, phase noise and sideband attenuation can be obtained.

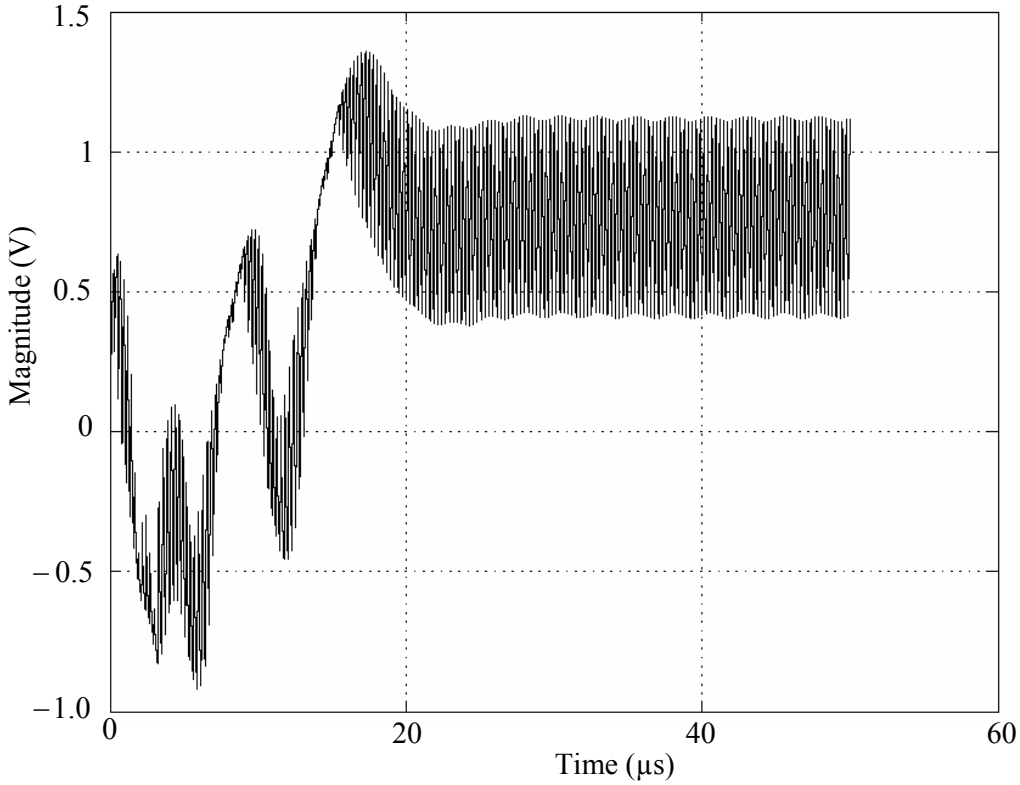


Figure 4.5. The figure shows the time domain simulation from figure 4.4.

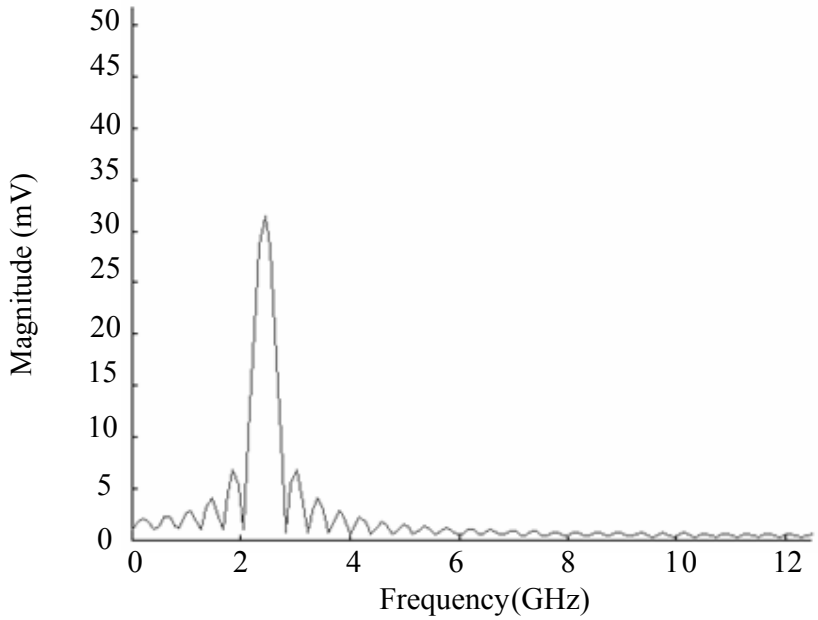


Figure 4.6. The figure shows the frequency domain simulation from figure 4.4.

CHAPTER 5: SUB-SYSTEM LEVEL DESIGN & LAYOUTS

5.1 Digital Sub-Systems

5.1.1 Phase Frequency Detector (PFD_1 & PFD_2)

PLL performance characteristics vary depending upon the type of phase detector (PD) used. The three most frequently used forms of PDs are the digital detector in which the output signal is restricted to two or three possible levels, the analogue mixer or multiplier, and the sampling PD. For high speed performance dual D flip-flop (FF) PD is preferred, [5]. PDs usually contain a charge pump as an integral part of the device: such a PD is a digital phase-frequency detector (PFD) with a charge pump output stage. Digital PFDs consist of two D flip flops and an AND gate.

The key characteristics for design are as follows:

- gain (associated with the output or charge pump stage),
- linearity, and
- steering characteristics.

The major difference between a PFD and other types of PDs is the existence of the third state (the advantages will be discussed in the following section.) The implemented PFD in this dissertation is depicted in figure 5.1. In the PFD, the output signal (of the PFD) depends not only on the phase error, θ_e, but also on the frequency error, $\Delta f = f_r - f_o$, before locking is acquired. The proposed PFD is built from two D flip-flops, whose outputs are denoted UP and DOWN, and whose state variable is denoted as d_{pd}. Since there are two storage elements, the d_{pd} has four states:

1. UP = 0, DOWN = 0
2. UP = 1, DOWN = 0
3. UP = 0, DOWN = 1
4. UP = 1, DOWN = 1

Since, only a tri-state device is needed, one of the states is unused (for instance, the fourth state (arbitrarily selected.)) To prevent lock-out (i.e. if the PFD accidentally selects this unused state), the approach used is to ensure that the PFD enters this stage, however, it will

then exit the state and arbitrarily enter one of the used states (this was selected as the first state (arbitrarily selected.)) This function is achieved by the AND gate of figure 5.1. The AND gate is also instrumental in determining the state transition. The state and d_{pd} are now defined as follows:

1. UP = 0, DOWN = 1, d_{pd} = -1
2. UP = 0, DOWN = 0, d_{pd} = 0
3. UP = 1, DOWN = 0, d_{pd} = 1
4. UP = 1, DOWN = 1, d_{pd} = inhibited

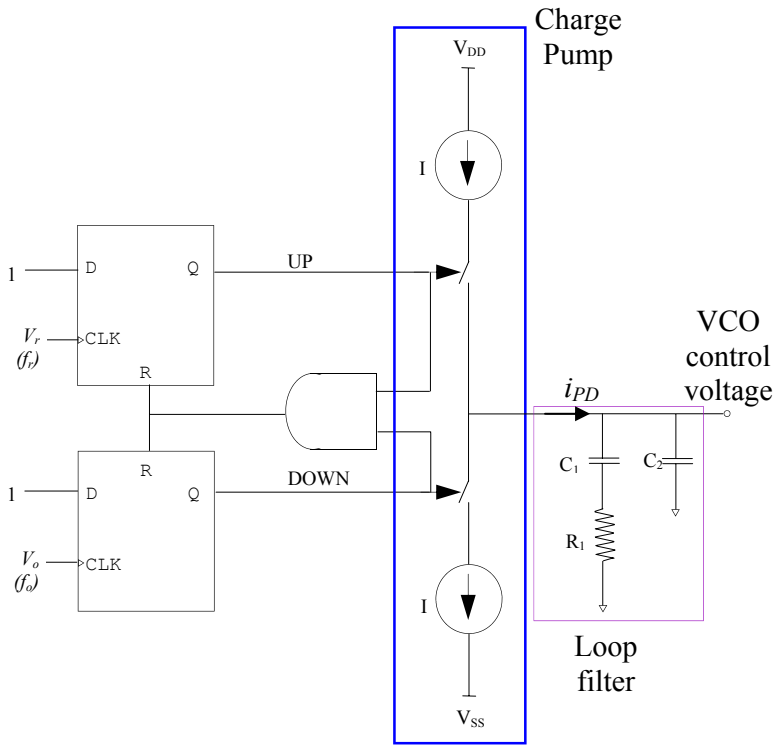


Figure 5.1. The figure shows a PFD, [6].

The actual state of the PFD is determined by the signals, V_r and V_o, applied to the two D flip-flops. Figure 5.2 is the state diagram that describes the operation of the circuit.

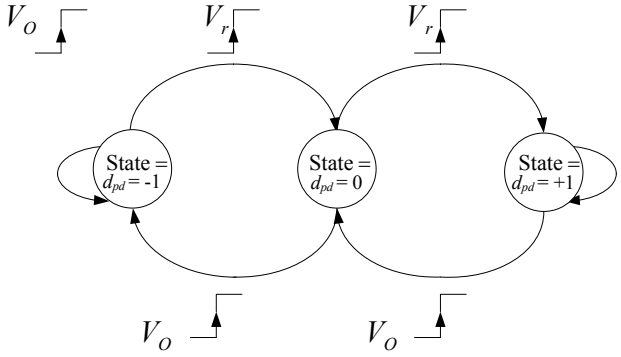


Figure 5.2. The figure shows the state diagram of the PFD.

The UP signal is high when the reference signal is operating at a higher frequency than the

feedback signal. The charge pump forces current into the loop filter when the UP signal is high. This causes the VCO control voltage to rise. This increases the VCO frequency and brings the feedback signal to the same frequency as the reference signal. The DOWN signal is high when the reference signal is operating at a lower frequency then the feedback signal. The charge pump forces current out of the loop filter when the *DOWN* signal is high. This causes the VCO control voltage to fall. This decreases the VCO frequency and brings the feedback signal to the same frequency as the reference signal.

The value of the charge pump current determines the phase detector gain, K_{PD}. Each reference cycle has duration of $2\pi/\omega_{ref}$ seconds. The time that the UP or DOWN signals are high determine the amount of current that gets delivered to the loop filter. Using the time that the UP and DOWN signals are high, given in equation (5.1), gives the average error current, i_e, over a cycle, [21]

$$i_e = \frac{t_{high}}{t_{cycle}}(\text{Charge pump current}) = \frac{I\theta_e}{2\pi} \tag{5.1}$$

This means that the phase detector gain is

$$K_{PD} = \frac{I}{2\pi}\left[\frac{\text{amps}}{\text{rad}}\right] \tag{5.2}$$

An example illustrating the operation of the PFD is shown in figure 5.3.

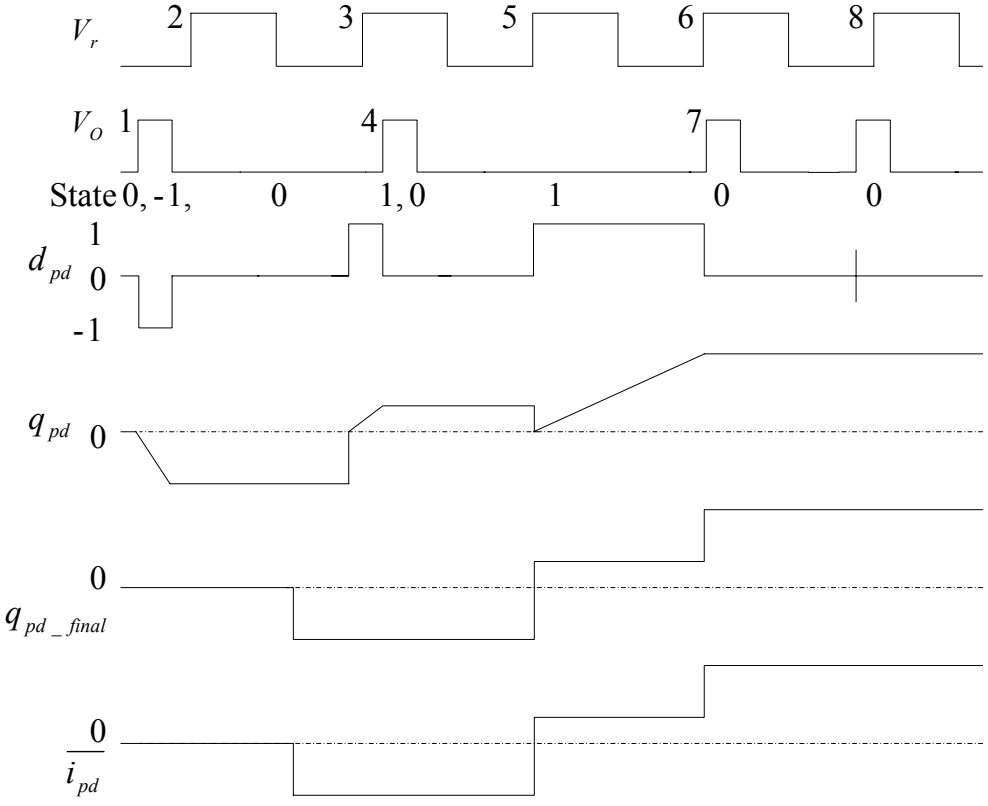


Figure 5.3. The figure shows an example illustrating the operation of the PFD.

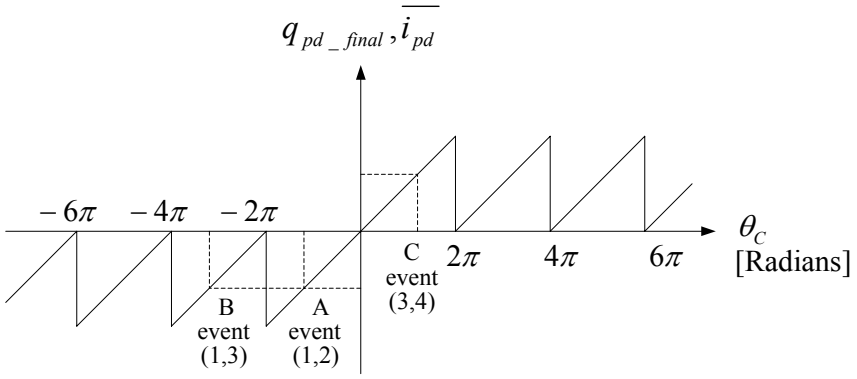


Figure 5.4. The figure shows a plot of the charge delivered and average current in a PFD versus phase error. The figure is derived from figure 5.3.

5.1.1.1 Charge pump

As discussed earlier, the PFD needs a logic to charge (current) converter or a charge pump. A generic model of the charge pump is incorporated in figure 5.1. Most of the time [5], the three output states are used with a PFD, but it is also possible to have combinatorial phase detectors with three-state logic outputs. These types of phase detectors, however, do not have the frequency-detection property of the PFD. A further unique feature of having a three-state output, like the one in the charge pump, is the existence of an idle state, which occurs when the PLL is in lock. This idling means that the output is zero, and ideally spurs should not exist. Therefore, the VCO is not modulated with spurs and V_o does not have side tones due to frequency modulation. Practically, voltage ripple can be expected – which causes spurs to occur at frequency, f_r. This is due to a small amount of charge that needs to be supplied to compensate for charge leaking away. The charge leakage is due to possible mismatches between the two current sources of figure 5.1.

Another feature of any charge pump is the time-varying properties. Due to the inherent switching of the charge pump, the PLL is a time-varying network, and is best analysed as a discrete time circuit. One complication in such an analysis is the non-uniform sampling operation of the PFD/charge pump. For example, the V_o's edge can arrive at the input to the PFD at any time (non-uniformly), in particular during the acquisition phase. When the system is locked, it becomes uniform, sampling only when the reference frequency is constant, which fortunately is the case in the present application. Hence, the PLL can be treated as a discrete time circuit with uniform sampling once it is in lock. Further simplification in analysis is possible, if the VCO control signal varies by a very small amount on each cycle of the reference signal (i.e. the loop bandwidth is small compared

with the reference frequency.) Consequently, the uniform time-varying operation can be averaged, and the discrete time circuit is transformed into a continuous time (time invariant) network, as in the subsequent analysis.

5.1.1.2 Spurs

Spurs are filtered by the loop filter (refer to figure 5.1.) However, though attenuated, the remaining spurs, if strong enough, when applied to the VCO will phase modulate the VCO and generate undesired side-tones. These side-tones can mix down unwanted adjacent channel interference (or other unwanted signals) to the same IF as the desired signal and corrupt the desired signal.

To illustrate the origin of spurs, refer to the circuit of figure 5.1, and the example of figure 5.3. If the steady state phase error is always positive, V_r is always on for a fixed period of time (before V_o is on.) One such example is event (3, 4) in figure 5.3. Here, it is seen that d_{pd} is 1 for the $\frac{\theta_e}{2\pi}T$ part of the period and 0 for the rest of the period. This part of the d_{pd} trace is re-drawn in figure 5.5 (a). The corresponding i_{pd} waveform is shown in figure 5.5 (b), where it is seen that the charge pump delivers a current $i_{pd} = I = I_{charge\_pump}$ for $\frac{\theta_e}{2\pi}$ fraction of a period T (where $T = f_r^{-1}$.) For the rest of the period, $i_{pd} = 0$. The current sources are normally implemented by single *n*-channel & *p*-channel transistors. Mismatch between the transistors lead to the steady-state phase error, θ_e. Assuming that $i_{pd}(t)$ has a duty cycle of $d = \frac{\theta_e}{2\pi}$, for a typical technology and transistor sizing, d turns out to be on the order of 0.1 %. A Fourier series expansion of $i_{pd}(t)$ reveals the discrete frequency components f_r apart, or the spurs. This is shown in figure 5.6. The envelope of these frequency components follows a sinc(f) function. The dc component is given by dc = $\overline{i_{pd}} = d \times I_{charge\_pump}$. The spur is represented by the frequency component closest to dc, as that component is most damaging. This is denoted as i_{spur} and is given by $A_{spur} \sin \omega_r t$. Since, f_r is close to dc, then $A_{spur} \cong \overline{i_{pd}}$. Consequently,

$$i_{spur} \cong \overline{i_{pd}}\ A_{spur} \sin \omega_r t \qquad (5.3)$$

The spur can be alternatively represented in the phase domain as:

$$\theta_{spur} \cong 2\pi d \sin \omega_r t \tag{5.4}$$

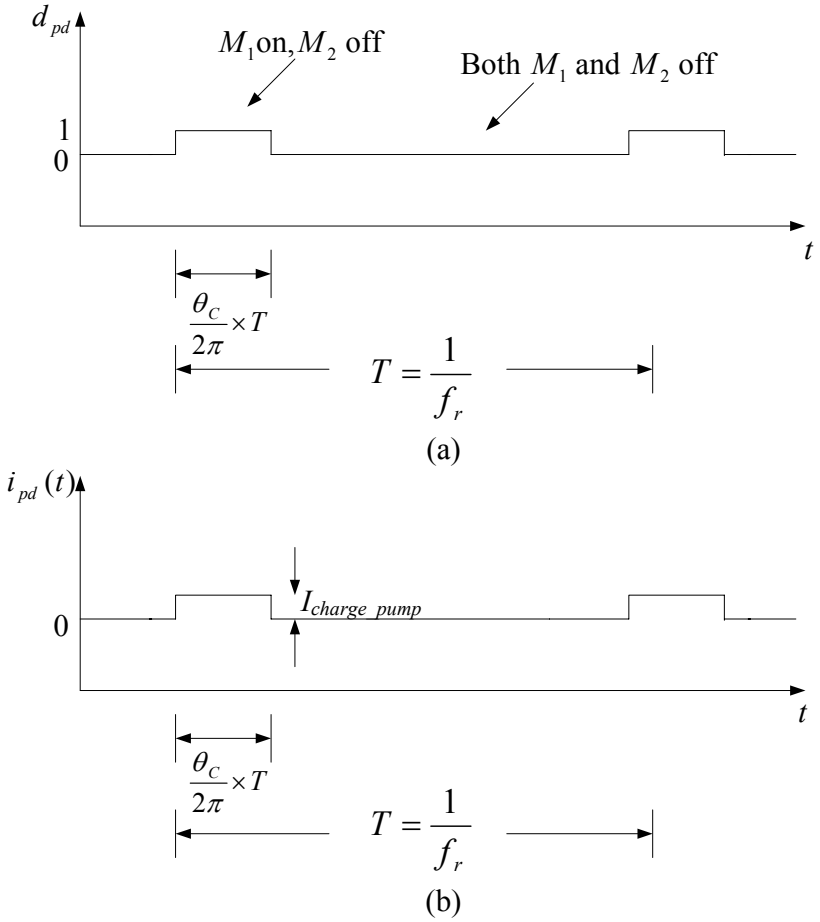


Figure 5.5. The figure shows (a) a plot of steady-state d_{pd} as a function of time, and (b) a plot of steady-state phase detector current as a function of time.

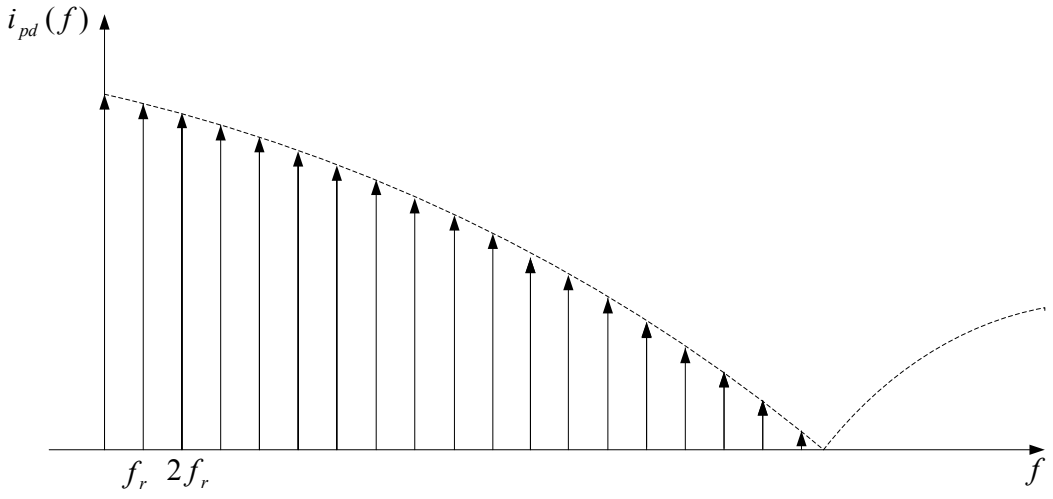


Figure 5.6. The figure shows the frequency spectrum of steady-state phase detector current.

5.1.1.3 PFD gain & phase noise

The PD/charge pump is characterised by its gain K_{PD} and $\overline{i_{pd}}$. The following considerations were taken into account for determining K_{PD}:

- K_{PD} should not be so large that the current source transistors become excessively large, and
- phase noise contribution (due to the phase detector.)

The phase noise contribution, [21] is:

$$S_{\theta\_pd} \propto \frac{1}{K_{PD}^{\ 2}} \tag{5.5}$$

Accordingly, K_{PD} should be selected to be large enough to make any output phase noise due to the charge pump insignificant when compared with other sources.

5.1.2 Dividers

Figure 5.7 serves to introduce the notation for the divider. This sub-section will serve to introduce divider architectures for the synthesizer developed in this dissertation.

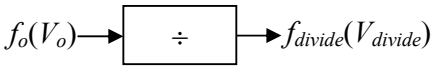


Figure 5.7. The figure shows a generic block depicting the divider operation.

This section covers various divider architectures prior to the chosen divider for this dissertation. Figure 5.8 illustrates the indirect divider (and the notation for discussion, thereafter.)

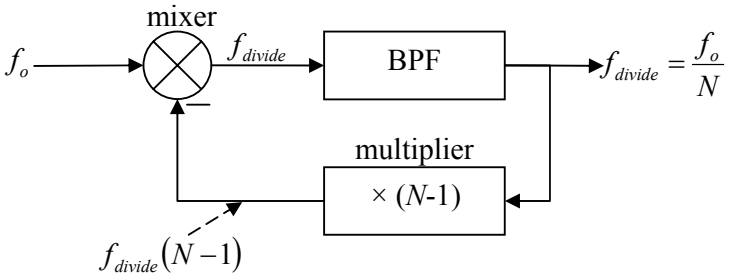


Figure 5.8. The figure shows an indirect divider, [5].

Assuming the output of the mixer has a frequency component, f_{divide}, the output of the band pass filter (BPF) will also have an output with frequency component, f_{divide}. After multiplication, this output becomes $f_{divide} \times (N - 1)$ – if this signal is applied to the mixer, the mixer output has a frequency component at $[f_o - f_{divide} \times (N - 1)]$, which was previously assumed to be f_{divide}. Equating these two expressions, $f_{divide} = f_o/N$. Due to feedback, this divider is slow.

As a higher speed divider is required, another topology (based on digital circuits) was considered. Figure 5.9 serves to introduce this topology. Operational discussion follows thereafter.

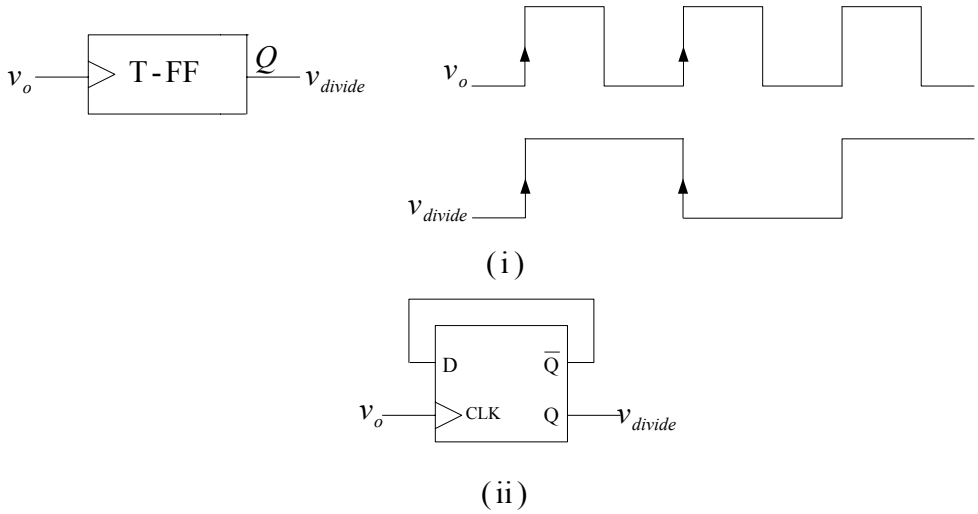


Figure 5.9. The figure shows (i) T-FF based divide-by-2 divider; and (ii) T-FF implemented using a D-FF, [5].

Assuming that the T-FF (toggle FF) is a positive edge-triggered FF, the FF has its output level toggled every time a positive edge arrives. For every two positive edge changes in the input waveform, there is one positive edge change in the output waveform, hence the number of positive edges is reduced by 2 (divide-by-2.) Figure 5.9 (ii) shows how the T-FF can be implemented by connecting the $\overline{Q}$ output of a D-FF back to itself. By cascading, a divide-by-4 (for example) divider could be implemented. In general, [5], feedback could also be deployed to achieve a non-binary division ratio.

Comparing the dividers of figure 5.8 and figure 5.9, it can be seen that the divider of figure 5.8 divides the input frequency by two, but the latter divides the input edges by 2. In general, for a frequency synthesizer the divider only needs to divide down the number of input edges, so the scheme in figure 5.9 is more general. In theory, it is not even necessary

to divide down the input edges uniformly. For example, a divider that divides according to figure 5.10 will also work.

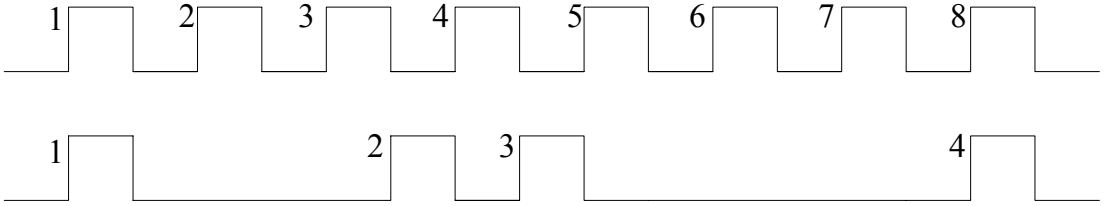


Figure 5.10. The figure shows the input and output waveforms of a generic divider that divides edges non-uniformly.

The divider of figure 5.10 produces output positive edges for eight positive input edges and therefore achieves a divide-by-2 operation, although in an average sense. To achieve a variable division ratio, the divider will be implemented as a programmable counter, as shown in figure 5.11.

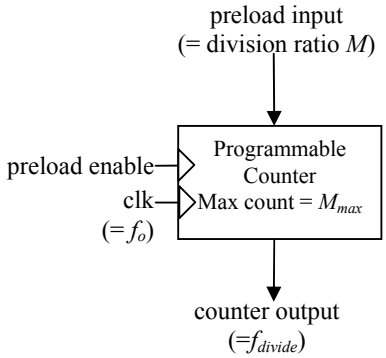


Figure 5.11. The figure shows a programmable divider, [22].

This divider is essentially a counter that counts from the preloaded input M to 0, thereby achieving a division of M. Here, $M \leq M_{max}$, the modulus of the counter, so the maximum division ratio is M_{max}. This counter can be implemented either as a ripple or a synchronous counter. The following paragraphs will serve to detail (the theory) two divider classifications: fixed divider and a programmable divider. The next sub-section will include implementation of the two types of dividers. A fixed divider is a divider for which the dividing ratio is fixed (for example, figure 5.9.) Such a divider has the inherent advantage that the configuration is fixed, i.e. the critical path is fixed and the speed can be optimized along the critical path. The earlier stage (if dividers of figure 5.9 are deployed in a cascade configuration) carries out division on the most significant bit (MSB), thus requires more current (with a direct implication on size and power) for a faster operation.

A programmable divider has a programmable divisor. This is achieved by using a programmable counter (as shown in figure 5.11): for a given speed requirement, a programmable divider is less power optimized (as with programmability, the critical path is dependent on the loaded value.) For example, in figure 5.11, the critical path is dependent on the value, M, and hence the design cannot optimize the transistor sizing a priori. In general, a frequency synthesizer requires a programmable division ratio while maintaining low power. To meet this challenge, the architectures (programmable & fixed dividers) can be combined (as shown in figure 5.12).

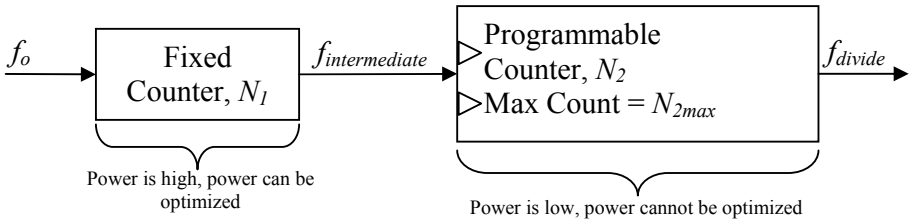


Figure 5.12. The figure shows a complete divider consisting of a fixed divider cascaded with a programmable divider.

In the divider (of figure 5.12), the output frequency, f_o is divided by a fixed counter at high frequency. Since the first counter is operating at high frequency, it consumes a lot of power (however, as discussed earlier, this can be optimized.) To make the entire division ratio programmable, the second counter must be programmable (however, as discussed earlier, this cannot be optimized.) However, the programmable divider operates at a lower frequency, hence, even without power optimization, the power consumption is not prohibitive. Selecting $f_{intermediate}$ involves a proper trade-off between the relative power consumption between the first and second counter.

Even though the aforementioned divider achieves better overall power consumption than a single programmable counter, it does reduce the resolution when compared with the single programmable counter approach.

Assume that the overall division ratio is:

$$M = N_1 \times N_2 \tag{5.6}$$

In the above equation, M is the complete divisor needed, N_1 is the divisor of the fixed divider, and N_2 is the divisor of the programmable divider. This implies that the overall

resolution of the divider is N_1 (as changing counter N_2 by 1 results in the overall division ratio changing by N_1). In general,

$$\text{Resolution}_{\text{complete\_divider}} = \text{Resolution}_{\text{programmable\_divider}} \times \text{division\_ratio}_{\text{fixed\_divider}} \quad (5.7)$$

The resolution of the complete divider may be improved if the fixed divider is also programmable. Since full programmability consumes too much power, the programmability can be restricted (by restricting the number of moduli that the divider can divide.) The simplest case would be to use the divider function as a dual modulus counter. A dual modulus counter can be further viewed as a fixed counter with a pulse swallower, which has the flexibility of counting one more pulse before generating an output or, equivalently, inserting one more pulse before generating an output. The concept is illustrated in figure 5.13 and figure 5.14.

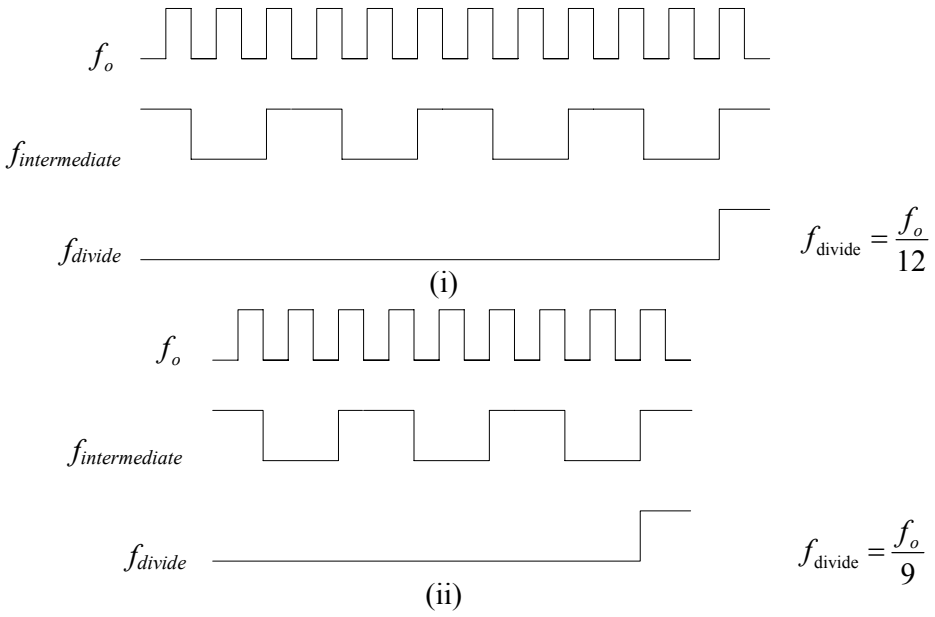


Figure 5.13. The figure shows (i) the waveform of the complete divider, $N_1 = 3$ and $N_2 = 4$; (ii) the waveform of the complete divider, $N_1 = 3$ and $N_2 = 3$.

In figure 5.13 (i), $N_1 = 3$, $N_2 = 4$, and $f_{\text{divide}} = \frac{f_o}{12}$. To illustrate the operation, if $f_{\text{divide}} = \frac{f_o}{11}$ is desired, a simple way will be to change M by 1 (in equation 5.6.)

The simple way is not possible here, since the only programmable counter is the second counter (as in figure 5.12.) If N_2 is decreased by 1, with N_1 remaining at 3, the result is as shown in figure 5.13 (ii) (where there are only nine f_o edges for one f_{divide} edge, so $f_{\text{divide}} = \frac{f_o}{9}$). To make up for the lost edges, the first counter is modified such that it

swallows pulses. The first counter is now called a pulse counter or an edge inserter. It works by swallowing one extra pulse (or inserting one extra edge) before generating an output. Figure 5.14 (i) serves to illustrate the output for a case when the first counter is turned on as a pulse swallower (edge inserter.) Hence the first counter, in the first cycle, counts four rather than three f_o edges before it generates an $f_{intermediate}$ edge. Assuming that in the subsequent cycles, the pulse swallower does not swallow a pulse, and therefore, it divides by 3. In this process, $f_{\text{divide}} = \frac{f_o}{10}$ is achieved. Hence, to still aim for $f_{\text{divide}} = \frac{f_o}{11}$, an additional edge should be inserted.

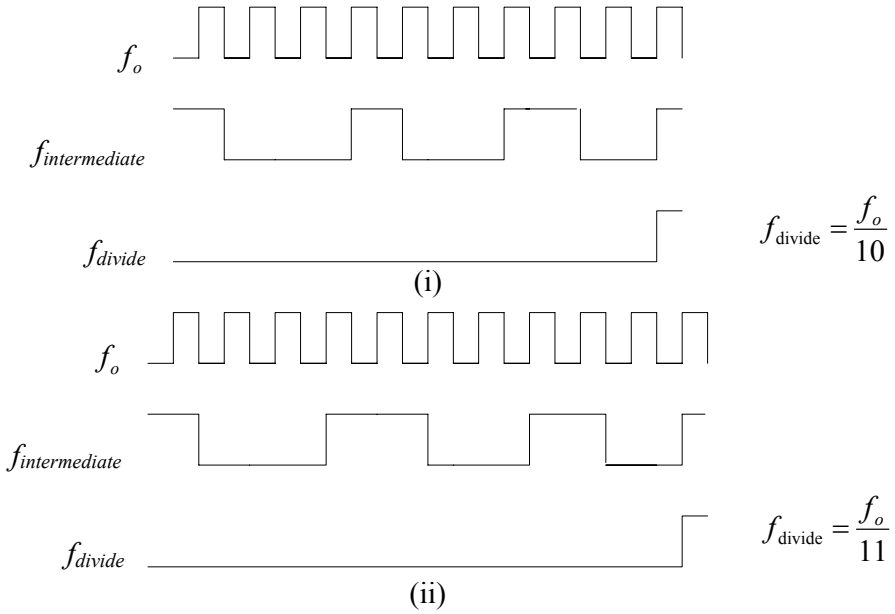


Figure 5.14. The figure shows (i) the waveform of the complete divider, with the fixed divider replaced by a dual modulus divider: $N_1 = 3/4$ and $N_2 = 3$ (i.e. $N_1 = 4$ for one N_2 cycle); (ii) the waveform of the complete divider, $N_1 = 3/4$ and $N_2 = 3$ (i.e. $N_1 = 4$ for two N_2 cycles.)

To continue the discussion, a restriction is posed by the first counter (which can only insert one edge (not two edges) per $f_{intermediate}$ cycle.) Hence, to achieve $\frac{f_o}{11}$, another edge needs to be inserted (as shown in figure 5.14 (ii)).

In this way, a resolution of 1 can be achieved, as f_{divide} can obtain all possible values between $\frac{f_o}{12}$ and $\frac{f_o}{9}$. This resolution is achieved by programming N_1 (setting the modulus) and also how many times the particular modulus should be used (i.e. how many times the edges are to be inserted.)

An overall restriction in choosing N_{2max} and N_1 is [22]:

$$N_{2max} \geq N_1 \tag{5.8}$$

The next two sub-sections will focus on the electronic/circuit level implementation of the dividers (based on the theory discussed above.)

5.1.2.1 Fixed frequency dividers (÷ N and ÷ X)

This section serves to implement the fixed dividers (as shown in figure 4.6.) Depending on the frequency and the amplitude of the input signals, different types of single-ended or differential structures for frequency dividers can be chosen. Figure 5.15 shows the block diagram of the divide-by-16 *N*-prescalar. The divide-by-4 *X*-prescalar is implemented using the same configuration as the ÷ 4 block of the divide-by-16 *N*-prescalar.

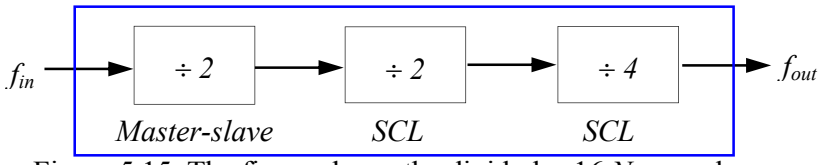


Figure 5.15. The figure shows the divide-by-16 *N* prescalar.

The source coupled logic (SCL) divide-by-2 circuit is based on a standard Master/Slave D-flip-flop and has a fully differential structure. As shown in figure 5.16, the half-speed SCL latch circuit consists of two main pairs. The first one is the sensing circuit, which is formed by M_1, M_3 and M_4. It is used to sense the differential signal at the D-input when the clock is high. The result will be stored to the subsequent latch stage, which consists of M_2, M_5 and M_6, when the clock is low. The current source in conventional SCL logic at the common source terminal shared by M_1 and M_2 is omitted in order to operate at a low voltage supply. However, omitting the current source requires a larger input signal swing to drive the input transistors, which is not a problem for the ring oscillator output as it is already maximized for low phase noise. Due to the limited output swing, a higher speed of the divider can be obtained compared to true single phase clocking (TSPC) dividers [23]. Moreover, the fully differential structure helps to avoid polluting of the substrate, which is a serious problem of TSPC logic. The circuit is used in the second divide-by-2 stages in the *X*-counter and *N*-counter.

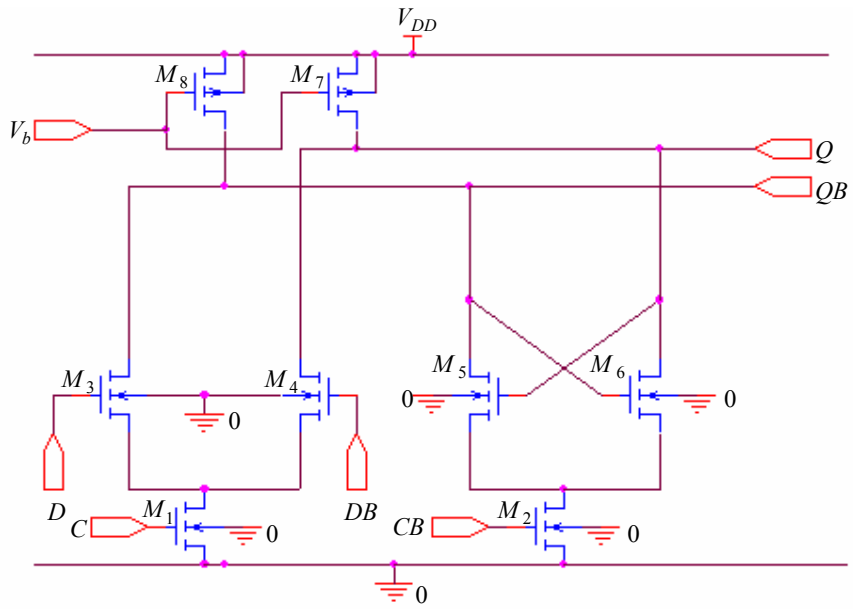


Figure 5.16. The figure shows the schematic of the half-speed SCL latch.

The full-speed SCL latch is also shown in figure 5.17. The only difference between the half-speed and the full-speed design is an additional pair of diode-connected transistors, M_9 and M_{10}, [9]. The transistors help to adjust the output common-mode voltage, to allow lower supply voltage and most importantly, to limit the output swing of the latch. By further limiting the output swing, reduction of the time required to switch from a low level to a high level is reduced and hence the speed of the circuit further increased. The circuit is used in the first divide-by-2 stage in the *X*-counter, which have maximum operation frequency around 1 Hz. The SCL latch cannot be fed back as the TSPC logic, and only a latch function is obtained because the sensing result directly appears at the output, [9]. Two SCL latches are to form the divide-by-2 circuit [24] and the divide-by-4 circuit is obtained by cascading two such divide-by-2 circuits as illustrated in figure 5.18.

Owing to the high-speed and small amplitude of the SSB mixer (as shown in figure 4.3) output signal, the divide-by-2 circuit shown in figure 5.19 is used for the first stage of the 2.3 GHz *N*-counter shown in figure 5.15.

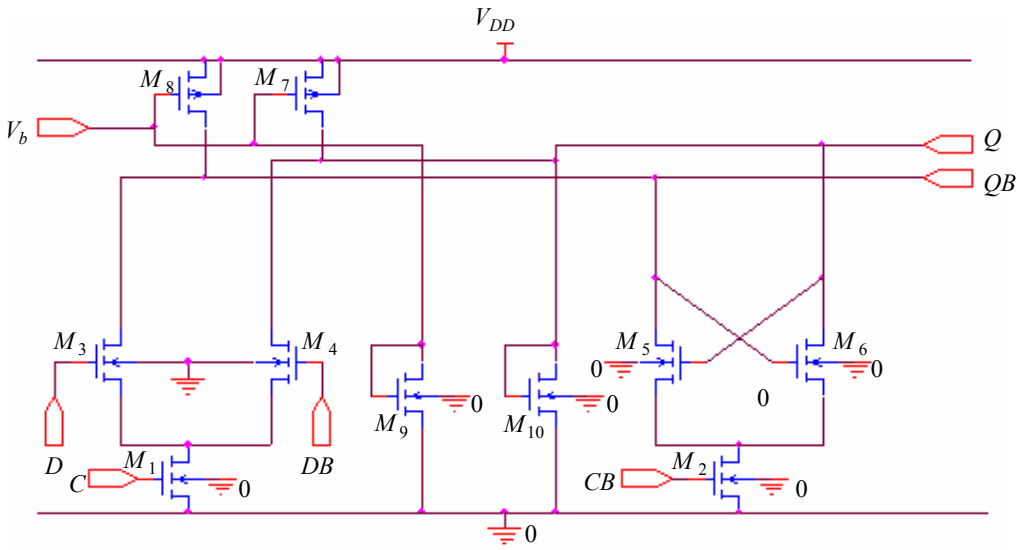


Figure 5.17. The figure shows the schematic of the full-speed SCL latch, [9].

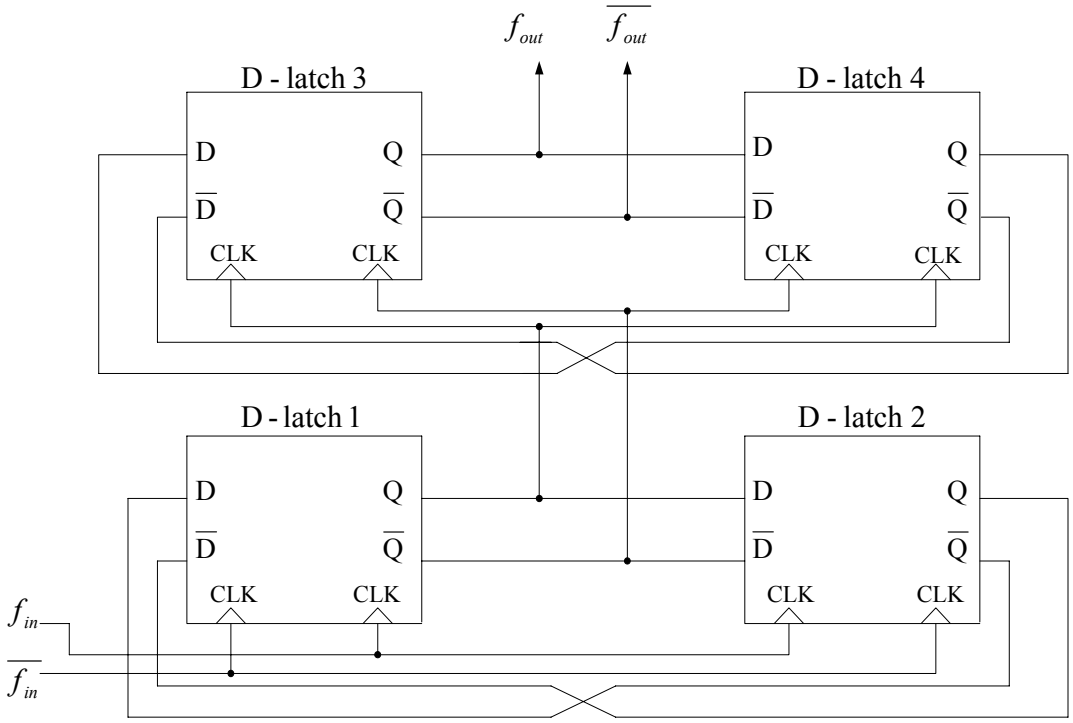


Figure 5.18. The figure shows the divide-by-4 circuit.

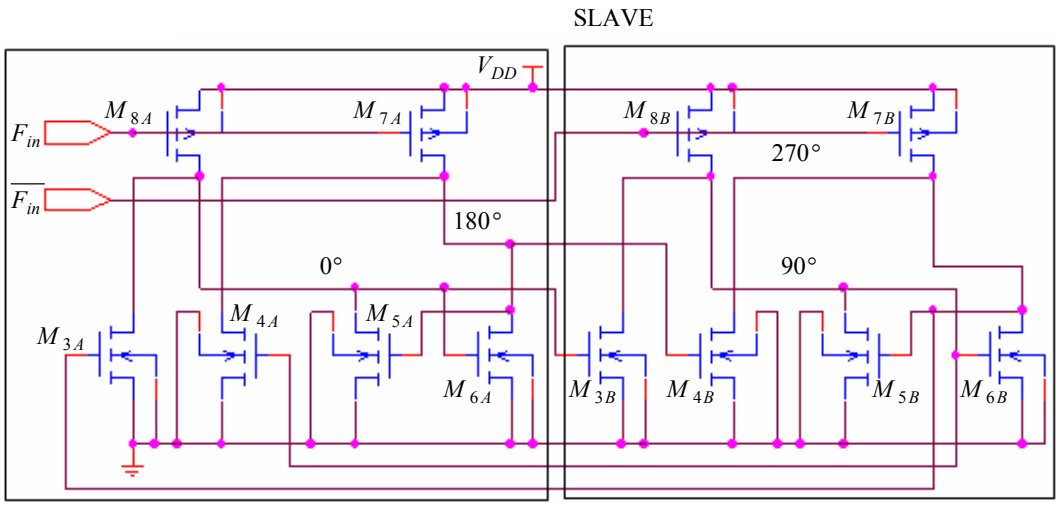


Figure 5.19. The 2.3 GHz divide-by-2 prescalar, [9].

The structure is essentially a Johnson Master and Slave counter that achieves high-speed operation by avoiding the stacking of the NMOS or PMOS transistor. The latch operates by using PMOS devices to drive current into its output nodes according to the clock signal, and the NMOS devices, M_3 and M_4, to selectively discharge the nodes according to signal levels of the other latch. When signal f_{in} is high, the master is in sense mode, while the slave is in store mode. When f_{in} goes low, the reverse occurs. The circuit can accept input signal as small as 0.25 V $V_{p\text{-}p}$ [9], while the divider oscillates if the input signal magnitude is too small. However, the divider is sensitive to the common mode voltage of the input and therefore an AC coupling stage could possibly be used at the divider input to improve performance. Proper DC bias can be applied through two resistors.

5.1.2.2 Programmable divider

As clear from figure 4.3, other than the fixed frequency scalars, there is a programmable multi-modulus counter in the low-frequency loop in order to adjust the desired channel in the synthesizer. Such a programmable divider is implemented as per the theory discussed earlier.

The counter employs the conventional design, which consists of a dual-modulus prescalar (DMP), a pulse (P) and a swallow (S) counter. The block diagram is shown in figure 5.20. The DMP initially divides the high-frequency input by $N + 1$ with the *Mode* signal being high. After the *S*-counter counts *S* output pulses from the DMP, it changes the *Mode* signal to low, and the DMP starts to count by *N*. The output from the DMP is also counted by the

P-counter simultaneously, and the *P*-counter resets the *S*-counter and itself after counting *P* output pulses. Therefore, the total counting number *M* is given by

$$M = P\left[(N+1)\frac{S}{P} + N\frac{P-S}{P}\right] = P.N + S \qquad (5.9)$$

In order to have a proper function of the counter, *S* should be smaller than *P* [22]. The numbers of *N*, *P* and *S* should be chosen carefully according to the maximum limitation of the allowable input frequency of the counters. In this design, *N* is 8 and hence the input frequency to the *S*-counter as well as *P*-counter is lower than 100 MHz. In the design, the *P*-counter has 7 bit binary inputs, and the *S*-counter has 4 bit inputs. Therefore, the maximum counting number of the frequency counter is 1031.

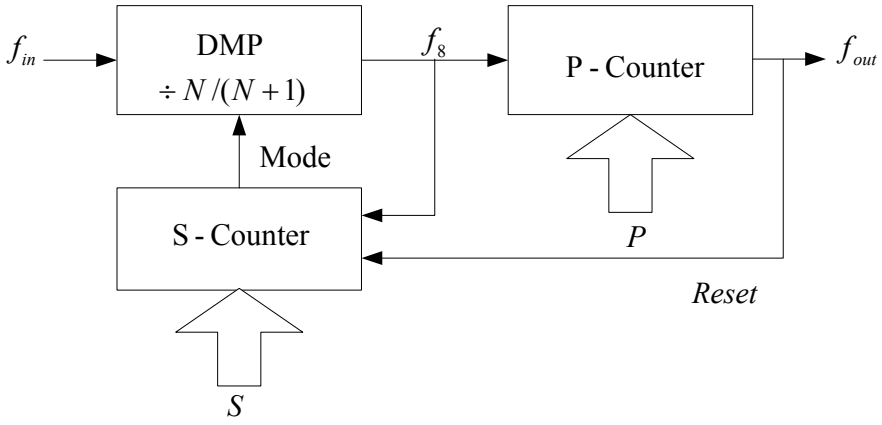


Figure 5.20. The figure shows the basic configuration of the programmable divider, [5].

The dual-modulus divide-by-8/9 prescalar is shown in figure 5.21. It is a critical building block of the programmable counter as its input stage is required to operate at a full speed. When the *Mode* signal is low, the second stage of the asynchronous divide-by-2/3 is disabled and the dual-modulus divider counts a number of eight. When the *Mode* signal goes high, the second stage of the synchronous divide-by-2/3 circuit is enabled on the every fourth count of the divide-by-4 stage and hence the counting number becomes nine instead of eight.

The asynchronous *S*-counter and *P*-counter are shown in figure 5.22 and figure 5.23, respectively. In both counters, a chain of TSPC flip-flops is used as the internal asynchronous ripple counters.

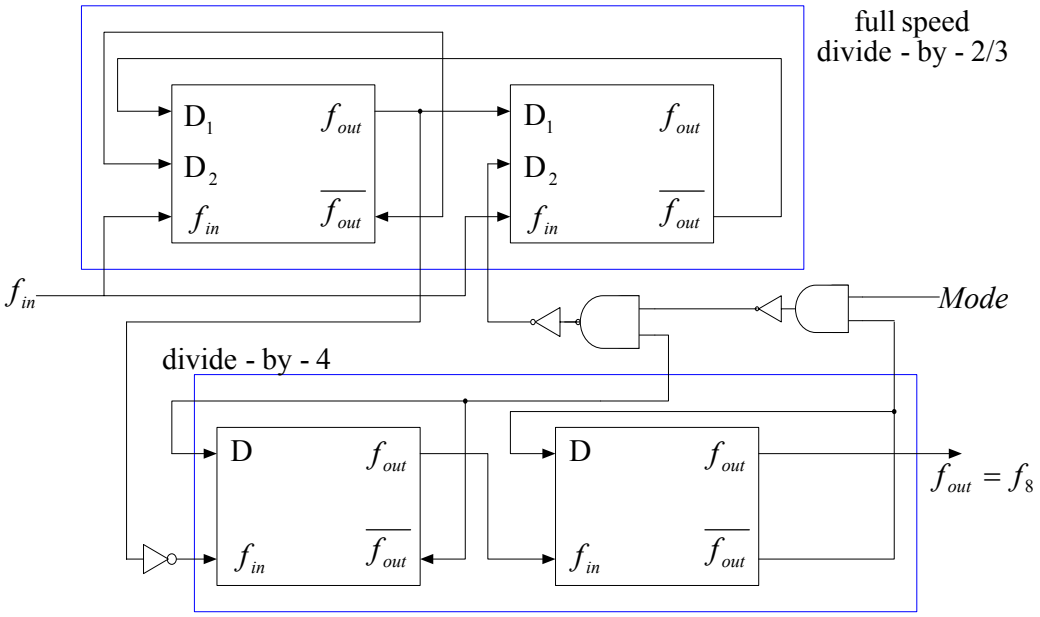


Figure 5.21. The figure shows the basic configuration of the dual-modulus divide-by-8/9 prescaler.

The output bits of the ripple counter are then compared with the input bits by the comparator. In the *S*-counter, a *D*-flip-flop after the comparator is used to obtain the *STOP* signal and *Mode* signal after *S* count of the input signal f_8, which is obtained from the DMP output. The ripple counter in the *S*-counter will stop its counting when signal *STOP* goes high until the *Reset* signal comes from the *P*-counter after *P* count of the input signal. The output signal of the *P*-counter is actually the output of the overall *M*-counter and resets both *P*-counter and *S*-counter when it goes high.

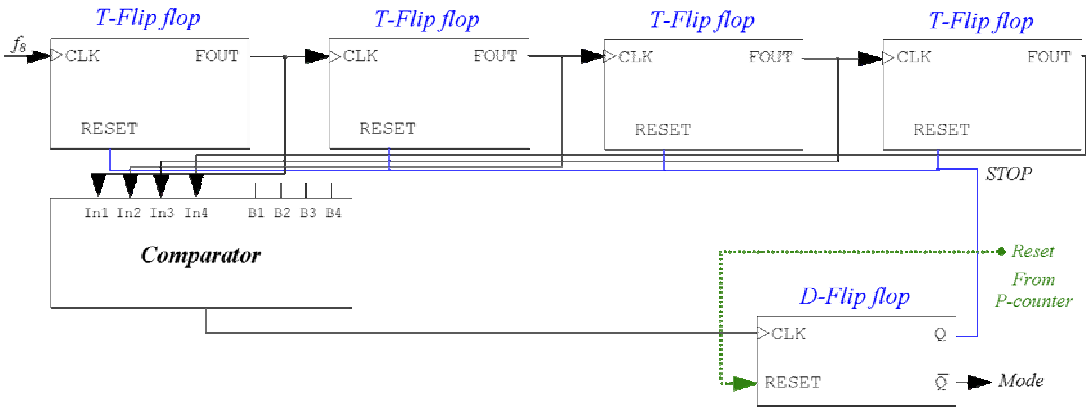


Figure 5.22. The figure shows the block diagram of the 4 bits *S*-counter, [9].

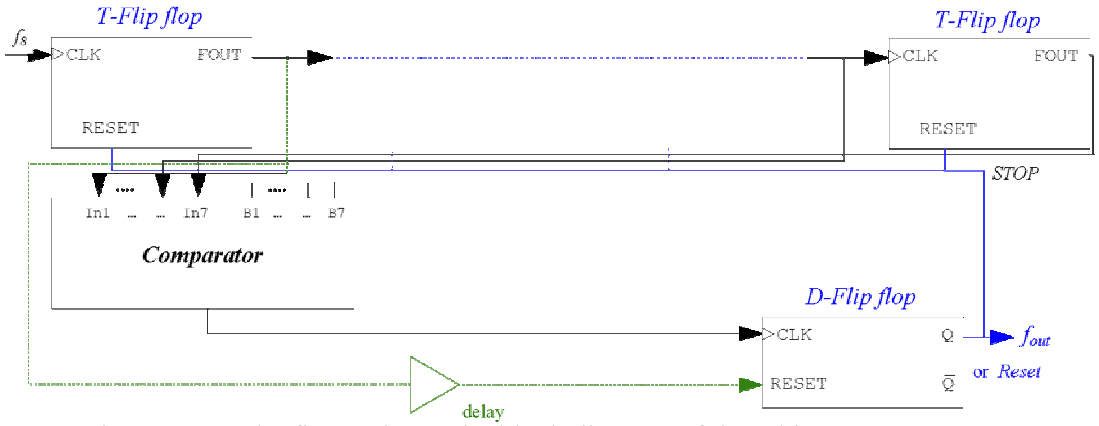


Figure 5.23. The figure shows the block diagram of the 7 bits *P*-counter, [9].

5.2 Analogue Sub-Systems

5.2.1 Voltage controlled oscillator (VCO)

This section will serve to introduce VCOs used in a frequency synthesizer. After coverage of general VCO types, the sub-sections will tend to focus on the VCOs directly applicable to this dissertation. VCOs can be categorized by method of oscillation into resonator-based oscillators versus waveform-based oscillators, as shown in Figure 5.24. Primary examples of each category are the LC oscillator and the ring oscillator, respectively. Each type has different ways of doing frequency tuning: current steering for ring oscillators and variable capacitor (or varactor) for LC oscillators. A relaxation VCO, another waveform based VCO, is usually not a good choice for the present application due to the huge amount of phase noise introduced as a result of positive feedback, [5].

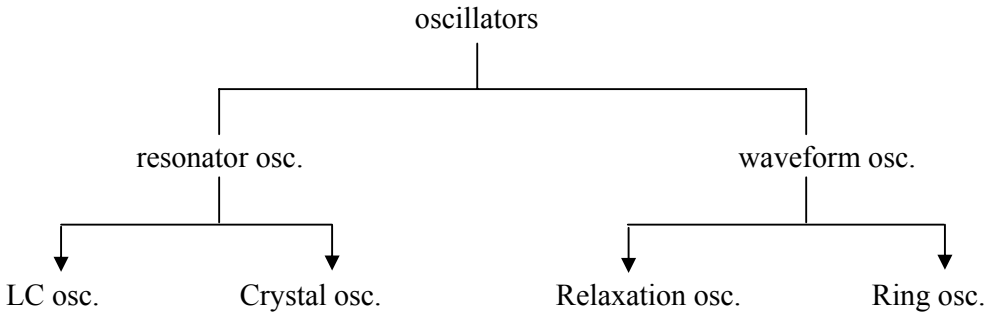


Figure 5.24. The figure shows the categorisation of VCOs.

There are two approaches to analyse resonator based oscillators: feedback approach and negative resistance approach. As resonator based oscillators can be modelled with small-signal analysis, the oscillators can also be described by a linear time invariant (LTI) system

using *s*-domain representation. For waveform oscillators, small signal analysis cannot be used, hence feedback theory does not apply. Thus, the next section will focus on reviewing the feedback theory from a perspective of resonator based oscillators.

5.2.1.1 Review: Feedback Theory

A feedback circuit in the *s*-domain is shown in figure 5.25. Some signal analysis will reveal:

$$\frac{S_o}{S_i} = \frac{a(s)}{1 + a(s)f(s)} \tag{5.10}$$

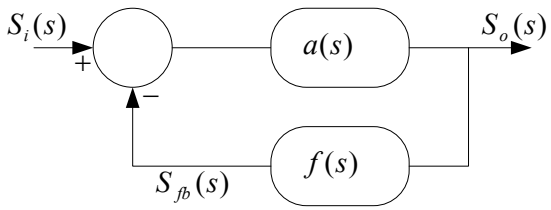


Figure 5.25. The figure shows the block diagram of a feedback circuit.

As an example, it may be assumed:

$$a(s) = \frac{a}{(1 + s\tau)^3} \tag{5.11}$$

It is further assumed that *f(s)* is negative (so overall feedback is positive), resistive, and constant. Then,

$$\frac{S_o}{S_i} = \frac{a(s)}{1 + a(s)f(s)} = \frac{k}{\left(1 - \frac{s}{s_1}\right)\left(1 - \frac{s}{s_2}\right)\left(1 - \frac{s}{s_3}\right)} \tag{5.12}$$

The transfer function consists of three poles, where the poles are roots of the equation:

$$1 + a(s)f(s) = 0 \tag{5.13a}$$

$$1 + \frac{af}{(1 + s\tau)^3} = 0 \tag{5.13b}$$

$$(1 + s\tau)^3 = -af \tag{5.13c}$$

$$1 + s\tau = \sqrt[3]{-af} \tag{5.13d}$$

To take care of the -1 (equation (5.13d)) inside the cube root, it is observed that

$$-1 = 1\angle 180^0 + n360^0 \quad \text{for} \quad n = 1, 2, 3 \tag{5.14a}$$

$$\sqrt[3]{-1} = 1\angle 60^\circ + n120^\circ \tag{5.14b}$$

$$= \text{-1, } 1\angle 60°, 1\angle \text{-}60° \tag{5.14c}$$

Substituting the cube root of -1 and normalizing $\tau = 1$, the poles of the transfer function can be obtained:

$$s_1 = -1 - \sqrt[3]{af} \tag{5.15a}$$

$$s_2 = -1 + \sqrt[3]{af}\ \angle +60^0 \tag{5.15b}$$

$$s_3 = -1 + \sqrt[3]{af}\ \angle -60^0 \tag{5.15c}$$

where af is the low-frequency loop gain. The root locus (as a function of af) is plotted in Figure 5.26.

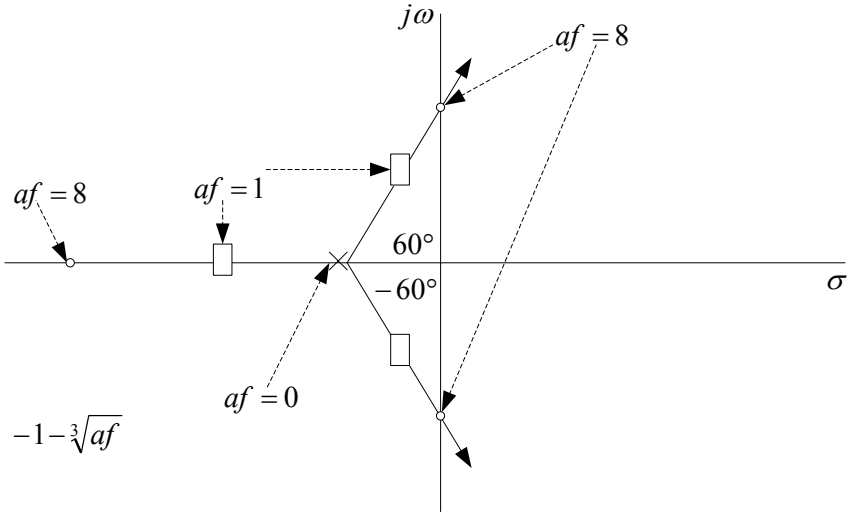


Figure 5.26. The figure shows the root locus of the example feedback circuit.

From the figure, it may be noted that when $af = 8$, two of the poles have just reached the imaginary axis. For $af > 8$ we have right half plane (RHP) poles, as shown in Figure 5.27.

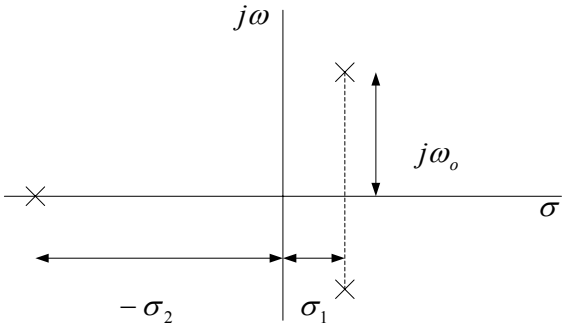


Figure 5.27. The figure shows the pole/zero diagram of the example feedback circuit.

To get a more complete picture of the behaviour of this transfer function (equation (5.12)), the Nyquist plot is used. The Nyquist plot is a plot of *af(jω)* in magnitude and phase on a polar plot using ω as the variable. In the present case, $af(j\omega) = \frac{af}{(1 + j\omega)^3}$, with $\tau = 1$.

For oscillation, the frequency where $\angle af(j\omega)$ = -180° is of interest. For $\omega = \sqrt{3}$, $\tau = 1$, $af(jw) = -\frac{af}{8}$. Two observations can be derived from this:

· feedback in this circuit is negative at $\omega = 0$, and

· feedback is positive at $\omega = \sqrt{3}$.

Furthermore, for oscillation, the loop gain ≥ 1:

$$\frac{s_0}{s_1}(j\omega) = \frac{a(j\omega)}{1 + af(j\omega)} \tag{5.16}$$

Substituting $\omega = \sqrt{3}$, $af(j\omega) = \frac{af}{8}$.

To set loop gain = 1, $af = 8$. Thus the transfer function with feedback applied is:

$$\frac{s_0}{s_1}(j\omega) = \frac{a(j\omega)}{1 + af(j\omega)} = \frac{a(j\omega)}{1 - 1} \to \infty \tag{5.17}$$

Hence, a loop gain at low frequency of 8 causes oscillation. This is verified by the Nyquist plot (where oscillation should occur when the Nyquist plot passes through (-1, 0)) of figure 5.28. This would happen at *af* = 8.

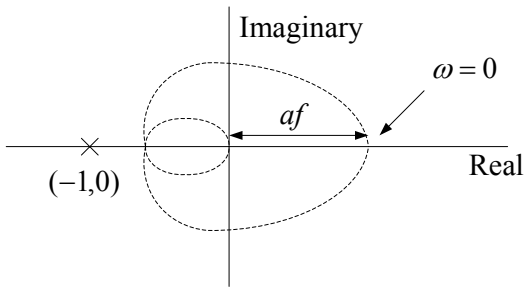


Figure 5.28. The figure shows the Nyquist plot of the discussed example feedback circuit scaled directly and linearly with the low-frequency loop gain, *(af)*.

From *S*-plane analysis, oscillation should occur when the root locus passes through the imaginary axis. From the plot (figure 5.26), this happens at *af* = 8. A result which is not obvious from the Nyquist plot is the case for a loop gain greater than 8. Mathematically, the number of times the Nyquist plot encircles (-1, 0) equals the number of RHP poles, but does not give further information. A plot of the overall gain, $\left|\frac{S_o}{S_i}(j\omega)\right|$, as *af* increases is

shown in figure 5.29. As af = 8, the gain approaches ∞, indicating a presence of RHP poles. The complete response of a circuit with RHP poles to any input is

$$S_o = f(input) + K_1 e^{-\sigma_2 t} + K_2 e^{\sigma_1 t} \cos \omega_0' t \,. \qquad (5.18)$$

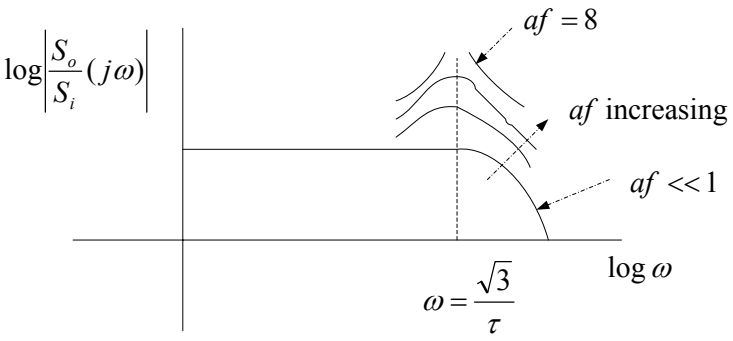


Figure 5.29. The figure shows the frequency response of the example feedback circuit discussed above.

It is noted that if *f*(input) is the forced response (amplifier response), $K_1 e^{-\sigma_2 t}$ is the decaying exponential natural response, and $K_2 e^{\sigma_1 t} \cos \omega_0' t$ is the oscillation (shown in the Figure 5.30.)

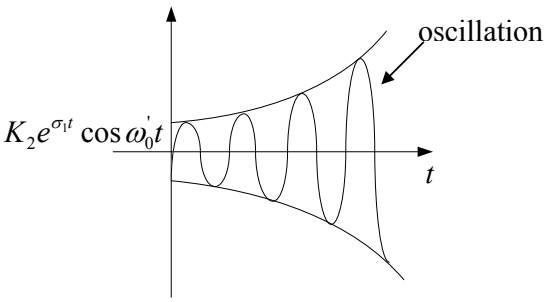


Figure 5.30. The figures shows the transient response of the example feedback circuit discussed above.

From Figure 5.30, it becomes clear that linear analysis is valid in the first part of the waveform. Hence, the zero crossing frequency equals ω_0' and is set by the RHP pole location. In the second part of the waveform, the effect of nonlinearity in active devices eventually dampens the growing exponential such that it has a steady-state waveform with constant amplitude. The zero crossing frequency is not necessarily ω_0'. Since a stable frequency of oscillation is desired, the circuit is not often used for oscillation. To summarise, for oscillation, positive feedback is desired such that phase shift of the loop gain is 180° and the magnitude of the loop gain is equal to or greater than 1 (while maintaining a stable and predictable frequency of oscillation.)

5.2.1.2 LC Oscillator

There are a few variations of oscillators, [5]. As discussed in section 4.3.4, an LC oscillator is used as the high frequency oscillator in this dissertation. Additional to the high frequency output, the oscillator should also have a good phase noise performance. This section will detail the design of such a LC oscillator.

5.2.1.2.1 Design variables

To design the LC oscillator, the following twelve variables are required:

- Spiral inductor: number of turns (n), turn width (w), turn spacing (s), and outer diameter (d_{out}). The next chapter details the design of the spiral inductor.
- Varactor: maximum value ($C_{v,max}$) and minimum value ($C_{v,min}$).
- Load capacitance: C_{load}.
- Transistors: width (W_n & W_p) and length (L_n & L_p).
- Bias current (I_{bias}): Since the thermal noise of the tail current source in the vicinity of the frequency of oscillation does not affect the phase noise of the oscillator due to its differential operation [25], I_{bias} is a design parameter rather than the bias transistor dimensions.

5.2.1.2.2 Evolution of LC oscillators (feedback theory)

This section serves to incorporate the theory discussed in section 5.2.1.1. The common source tuned amplifier is first considered in the development of an LC oscillator using feedback oscillator theory. Figure 5.31 shows the "tuned" stage, where an LC tank operates as the load. At resonance, the voltage gain is $-g_{m1}R_p$ (Note that the gain of the circuit is very small at frequencies near zero). As shown in figure 5.32, feedback is achieved by connecting the output to the input. Qualitative analysis reveals that at resonance, the total phase shift around the loop is equal to 180° (rather than 360°). Also, from figure 5.31, the frequency dependent phase shift of the tank never reaches 180°. Thus, the circuit will not oscillate. Further analysis reveals that if the stage is biased at a drain current, I_1 and the series resistance of L_p is small then the DC level of v_{out} is close to V_{DD}. If a small sinusoidal voltage is applied to the input, the output to the circuit can be expected to be an inverted amplified sinusoidal voltage (with an average value near V_{DD}) because the inductor cannot sustain a large DC drop. In other words, if the average value of v_{out} deviates significantly

from V_{DD}, then the inductor series resistance must carry an average current greater than I_1. Thus, the peak output level in fact exceeds the supply voltage, an important and often useful attribute of the LC load. With careful design techniques, the output peak-to-peak swing is ensured to be larger than V_{DD}.

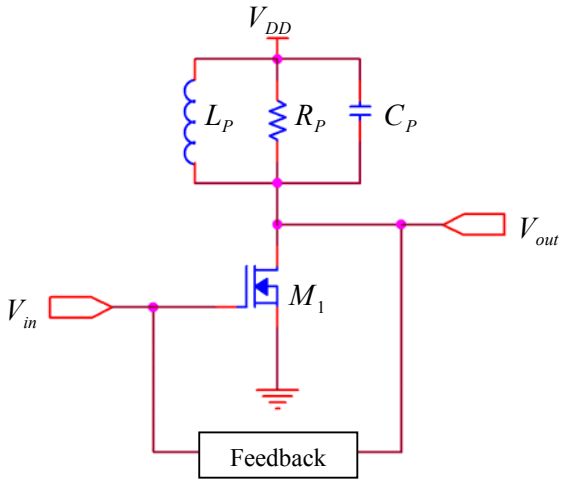


Figure 5.31. The figure shows a tuned gain stage in feedback.

Using two stages in cascade as shown in the configuration of figure 5.32, the configuration does not latch up because its low frequency gain is very small. Furthermore, at resonance, the total phase shift around the loop is zero because each stage contributes zero-frequency dependent phase shift. That is, if $g_{m1}R_P g_{m2}R_P \geq 1$, then the loop oscillates.

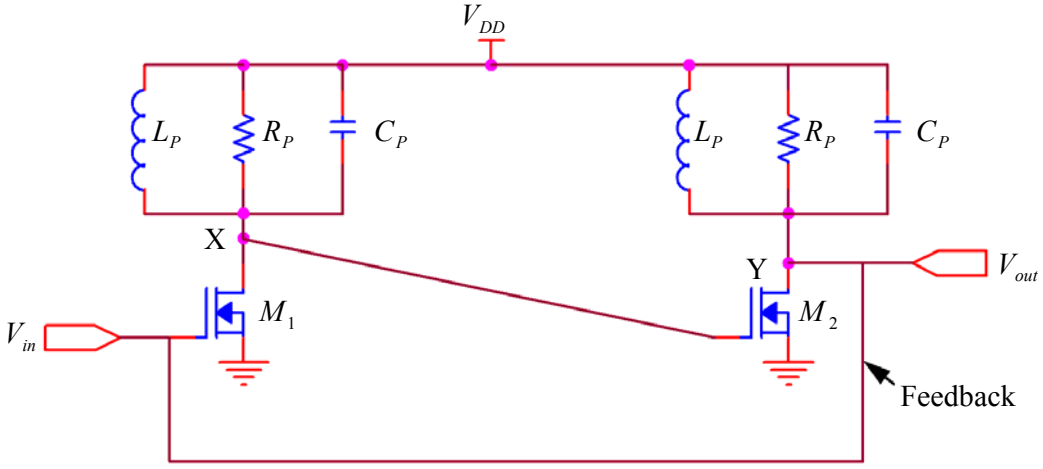


Figure 5.32. The figure shows two tuned stages in a feedback loop.

The drain currents of M_1 and M_2 and hence the output swings heavily depend on the supply voltage. The waveforms at X and Y are differential, hence M_1 and M_2 can be converted to a differential pair. This is shown in figure 5.33. A tail current source (total bias current), I_{SS} can be used to lower supply sensitivity. If the circuit begins with zero difference between V_X and V_Y, then $V_X = V_Y \approx V_{DD}$.

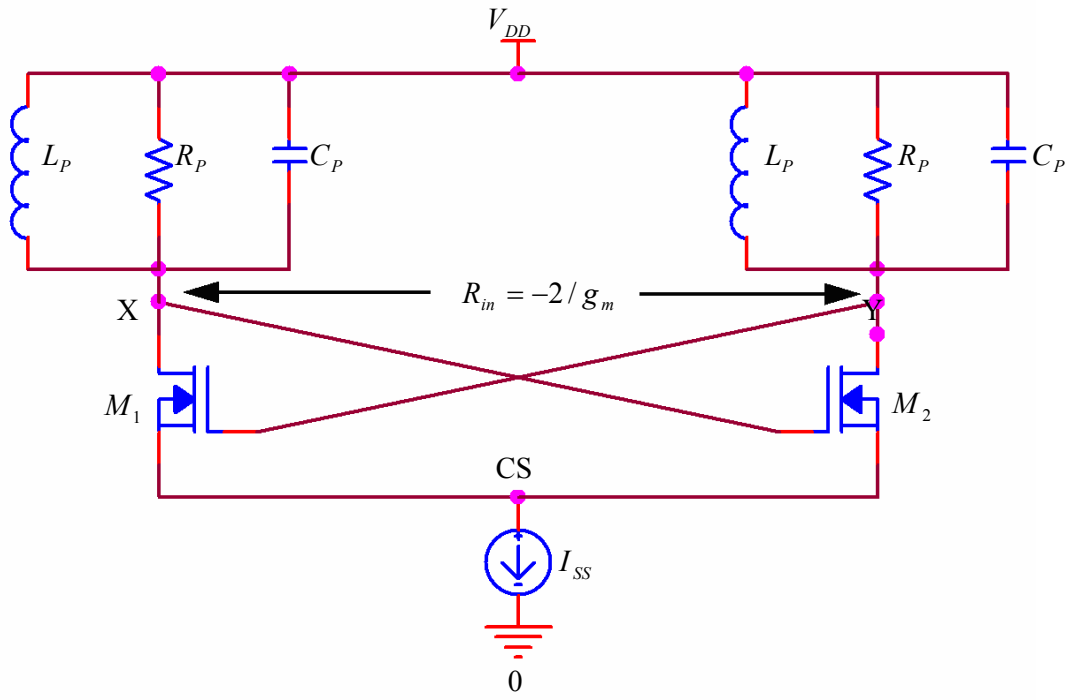


Figure 5.33. The figure shows a redrawing of the oscillator of figure 5.32 with addition of a tail current source, [26].

The transistors share the tail current equally. If $g_{m1}R_P g_{m2}R_P \geq 1$, where R_P is the equivalent parallel resistance of the tank at resonance, then noise components at the resonance are continually amplified by M_1 and M_2, allowing the oscillation to grow. The drain currents of M_1 and M_2 vary according to the instantaneous value of V_X - V_Y (as in a differential pair).

The oscillation amplitude grows until the loop gain drops at the peaks. If $g_{m1,2}R_P$ is large enough, the difference between V_X - V_Y reaches a level that steers the entire tail current to one transistor, turning the other off. Thus, in steady state, I_{D1} and I_{D2} vary between zero and I_{SS}.

The oscillator is constructed in fully differential form. The supply sensitivity of the circuit, however, is nonzero with perfect symmetry. This is because the drain capacitances of M_1 and M_2 vary with the supply voltage.

5.2.1.2.3 Evolution of LC oscillators (negative resistance theory)

This is an alternative theory used in the development of LC oscillators. It is based on the concept of "negative resistance". This can be first developed by considering a simple tank that is stimulated by a current impulse as shown in figure 5.34.

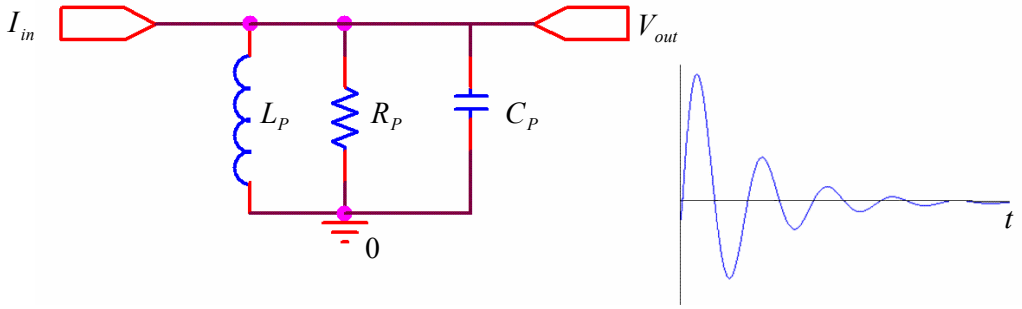


Figure 5.34. The figure shows the decaying impulse response of a tank.

The tank responds with a decaying oscillatory behaviour because, in every cycle, some of the energy that reciprocates between the capacitor and the inductor is lost in the form of heat in the resistor. If a resistor equal to $-R_P$ is placed in parallel with R_P (then the combined parallel resistance is infinite). Thus, if a one port negative resistance is placed in parallel with a tank, the combination may oscillate. Such a topology is called a one-port oscillator.

Feedback multiplies or divides the input and output impedances of circuits by a factor equal to one plus the loop gain. Thus, if the loop gain is sufficiently negative (the feedback is sufficiently positive), a negative resistance is achieved. As a simple example, the source follower of figure 5.35 is considered. If the feedback is implemented by a common gate stage and the current source, I_b is added to provide the bias current of M_2, then it is deduced in [26], that the input impedance will be negative as shown in equation (5.19). It is assumed that the two transistors are matched (have the same g_m) (for a first design).

$$R_{IN} = -\frac{2}{g_m} \tag{5.19}$$

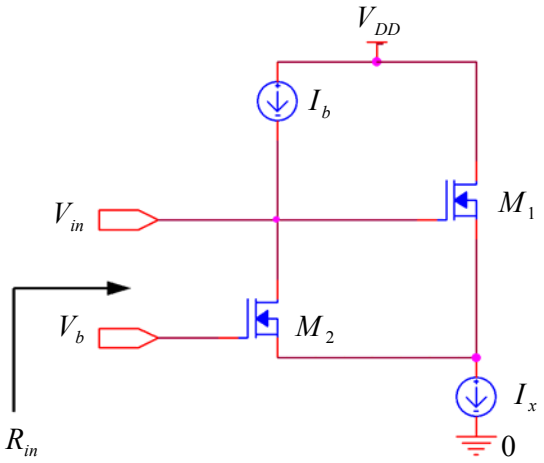


Figure 5.35. The figure shows a source follower with positive feedback to create negative input impedance, [26].

Negative resistance can be intuitively understood as an incremental quantity, that is negative resistance indicates that if the applied voltage increases, the current drawn by the circuit decreases. This can be qualitatively applied on figure 5.35. For example, if the input voltage increases, so does the source voltage of M_1, decreasing the drain current of M_2 and allowing an incremental part of I_b to flow to the input source (thus decreasing the current drawn by the circuit.) With a negative resistance available, an oscillator can be constructed. This is shown in figure 5.36.

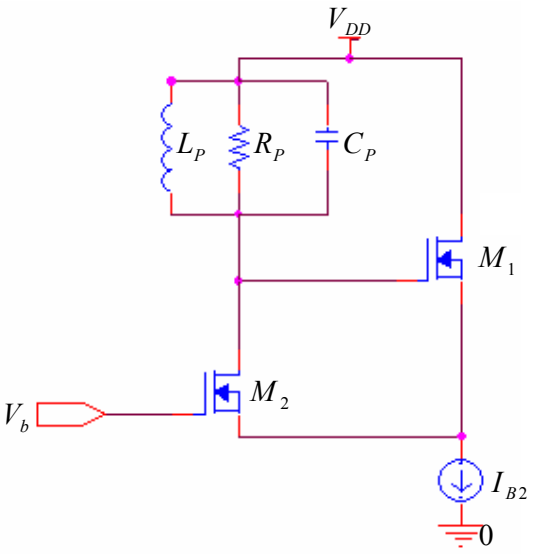


Figure 5.36. The figure shows an oscillator using negative resistance input resistance of a source follower with positive feedback.

In figure 5.36, R_P denotes the equivalent parallel resistance of the tank and, for oscillation build-up, R_P - $2/g_m \geq 0$. Note that the inductor provides the bias current of M_2, obviating the need for a current source. If the small-signal resistance presented by M_1 and M_2 to the tank is less negative than $-R_P$, then the circuit experiences large swings such that each transistor is nearly off for part of the period, thereby yielding an "average" resistance of $-R_P$.

If the drain current of M_1 flows through a tank and the resulting voltage is applied to the gate of M_2, the topology of figure 5.32 is obtained. It is noted that the cross-coupled pair must provide a negative resistance of $-R_P$ between nodes X and Y to enable oscillation. It can be shown that this resistance is equal to $-2/g_m$ and hence it is necessary that $R_P \geq 1/g_m$.

The circuit can be viewed as either a feedback system or a negative resistance in parallel with a lossy tank. This topology is also called a "negative-G_m oscillator."

5.2.1.2.4 In- and quadrature phase generation

The LC ring oscillator is a series of cascaded unit oscillators. It is not supposed to behave as a series of delay cells commonly found in conventional ring oscillators. Thus, the architecture should behave as a harmonious combination of N oscillators, and should produce the effect of cascaded bandpass filtering. One possible oscillator architecture with a ring type connection is shown in figure 5.37.

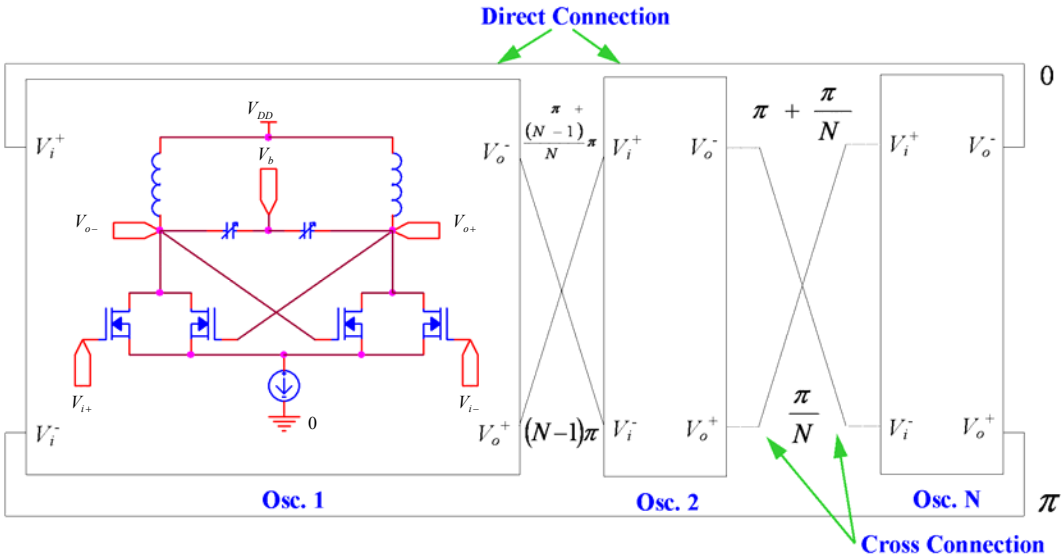


Figure 5.37. The figure shows the ring structure of cascaded LC oscillators, [27].

The ring architecture has one direct connection and (*N-1*) cross connections. Like the quadratic operation of two identical LC oscillators in [28], the cross coupling tries to force the following oscillator in-phase, while the direct coupling forces it anti-phase. In the beginning, V_{No+} and V_{1o-} become anti-phase through the direct coupling. Simultaneously, $V_{(i)o+}$ and $V_{(i+1)o+}$ ($i=1, \ldots, N-1$) become in-phase through the direct coupling. After the negotiation between the couplings, the unit oscillators connected by the cross between the couplings have π/N phase differences and the direct-coupled oscillators have $(N-1)\pi/N$ phase differences. The final phase distribution of the LC ring oscillator is shown in figure 5.37.

The oscillation can only sustain if the cross coupling transistors are on, that is when the sine goes through zero, so this means that the gate of the cross coupling transistor gets the maximum voltage from core 1 when core 2 is at zero, or a phase shift of 90° between both cores.

For $N = 1$, the resonance frequency, f_o is given by

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{5.20}$$

The general case (for a general N) is considered, for this the resonance frequency is given [27] by

$$f_o = \frac{1}{2\pi} \frac{\beta \frac{LG_m}{\sqrt{1+\beta^2}} + \sqrt{\frac{(\beta LG_m)^2}{1+\beta^2} + 4LC}}{2LC} \tag{5.21}$$

where G_m is the transconductance of M_{1-4}, N is the number of unit oscillators, and β is given by

$$\beta = \frac{1}{\tan\left(90^\circ - \frac{180^\circ}{N}\right)} \tag{5.22}$$

Taking the derivative of equation (5.21) and equating to zero (ceiling), it can be shown that the two-stage LC ring oscillator operates at the highest frequency (numerically, this is quite close to equation (5.20)). The resonance frequency of the other LC ring oscillator decreases as N increases thereafter, and it approaches that of the single stage given by equation (5.20). For $N = 2$:

$$f_o = \frac{1}{2\pi} \frac{\sqrt{(LG_m)^2 + 4LC}}{2LC} \tag{5.23}$$

5.2.1.2.5 Improved amplitude and phase matching

Coupled LC oscillators are known to provide good performance in terms of phase noise, signal amplitude, power consumption, and quadrature output signals. However, IQ amplitude and phase mismatches in these oscillators can be quite large due to the serious mismatch problem of large area inductors and varactors. A simple design modification of the coupled LC oscillators shows a significant improvement of the amplitude and phase mismatches.

LC oscillators can satisfy the strict requirements of phase noise, power and output swing. In order to generate quadrature phase outputs, many methods are used, e.g. RC-CR network, Havens' technique, and frequency division, but they suffer from inaccurate phase, amplitude loss, and double frequency operation [1]. By using two identical LC oscillators with four coupling transistors as shown in figure 5.38, even quadrature outputs can be obtained [28]. If the two oscillators are identical, they will oscillate at the same frequency with quadrature phase difference. However, as the mismatches in the two oscillators get larger, the amplitude will be deviated from each other, and phase difference will be further from 90º. If the mismatch is large enough, the two oscillators will eventually oscillate independently at different frequencies.

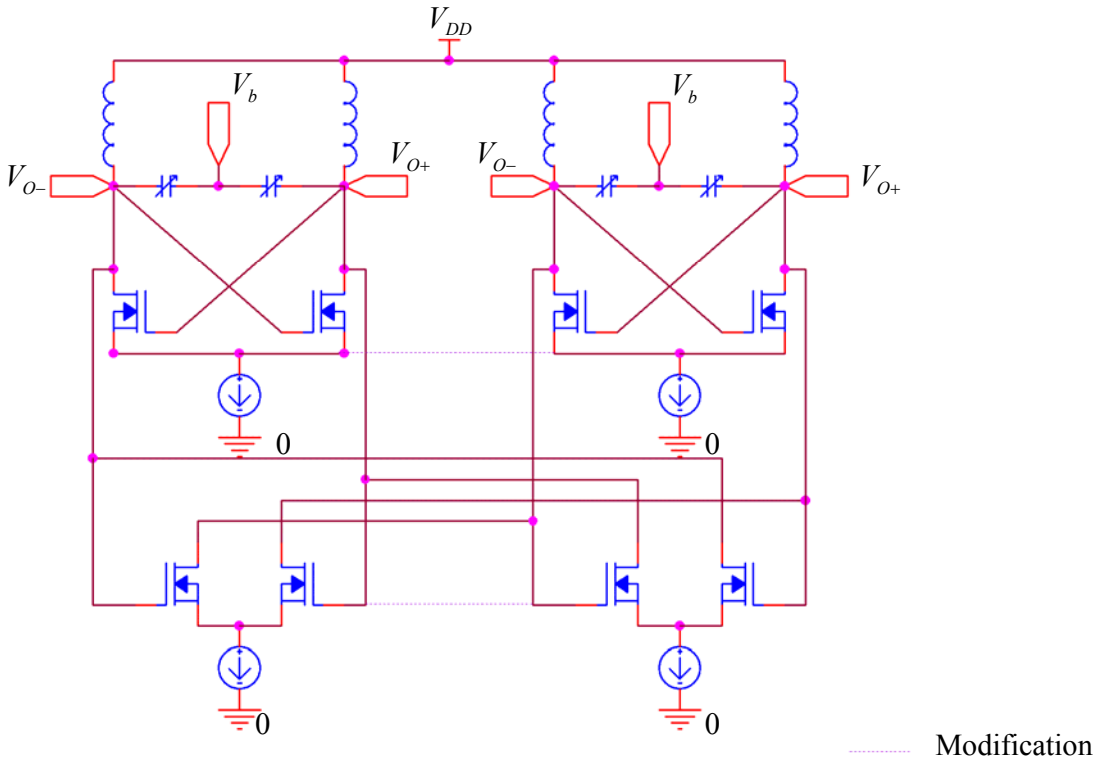


Figure 5.38. The figure shows the schematic of coupled LC oscillators with quadrature outputs, [28].

For LC oscillators, causes of mismatches include geometric error from the process, a large area of non-uniform substrate under the inductors and varactors, and nearby objects, which couple to the tanks both electrically and magnetically. Due to the large area of the LC resonant tanks, the mismatch problem of the two oscillators will be serious. Although larger coupling transistors with larger bias can force the two non-identical oscillations in a more quadrature way, they cannot control the output amplitudes of the two oscillations and will negatively affect the phase noise performance as well. Additionally, the coupling transistors can maintain the quadrature phase well only when two oscillations have same output amplitudes.

As the two oscillators are connected only by four transistors, more mechanisms are needed to maintain both amplitude and phase matching of quadrature outputs. Such a mechanism can be achieved simply and effectively by connecting the two bias current sources of the two oscillators together as shown in dotted lines in figure 5.38. This connection can provide an amplitude control, which is not available before, and enhance the phase control as well. About three times improvement in amplitude and phase matching is observed [29].

5.2.1.2.6 Amplitude control

Consider a single LC oscillator as shown in figure 5.33. A negative g_m cell is used to compensate the loss in the LC tank to maintain the oscillation. Typically, the common source of the two transistors of the differential pair is assumed to be a virtual ground. However, the assumption is no longer valid if the differential output signal becomes large. As one of two outputs of the oscillation is high and the other is low, one of the transistors is cut-off and the other becomes linear. The common source (node CS) of the two transistors will be pulled high by the linear transistor which acts as a small-value resistor. At this time, the cut-off transistor does not have transconductance gain, g_m, because it is off, and the linear transistor has a very small g_m gain because the source node rises with the gate voltage. This can be modelled as a transistor with source degeneration. The source degeneration reduces the g_m gain when the differential output is large as shown in the flatter part of transfer curve of the g_m cell in figure 5.39. As the oscillation can only occur when the average loop gain is larger or equal to one, the intersection point of the loop transfer function with the line of unity slope line determines the amplitude of oscillation. Since the transfer curve with degeneration cuts the line of unity slope at a point lower than the one without degeneration, the amplitude of the oscillation will be smaller than

expected. Ideally, the differential amplitude can be as large as the product of the bias current and the equivalent parallel resistance of one LC tank.

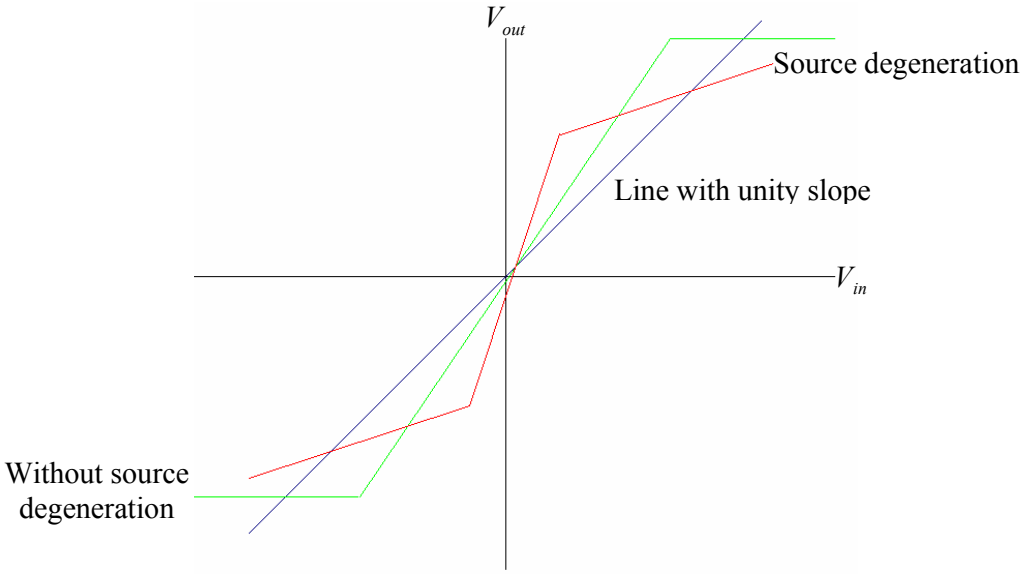


Figure 5.39. The figure shows the output-input voltage characteristic of a g_m cell, [29].

It is shown by [29] that a larger and closer-to-theoretical output amplitude, a "flatter" (as shown in figure 5.39) common source voltage, and a g_m cell current with extra current pulses can be observed by implementing the modifications shown in figure 5.38.

5.2.1.2.7 LC oscillator design

The final oscillator consists of two individual oscillators (as shown in figure 5.40), which are forced to have quadrature oscillation by the direct-coupling transistors (M_7 and M_8) and the crossed coupling transistors (M_5 and M_6). Each transistor in the coupling stages can provide 90º phase shift to the input signal. The quadrature outputs are required to drive the SSB mixer in order to obtain the image rejection function of SSB mixing. The transistors M_1, M_2, M_3, and M_4 of the negative transconductance pairs are used to compensate the loss in the LC tank in order to obtain oscillation. The oscillation frequency is given in equation (5.23). This can be rewritten as

$$f_o = \frac{1}{2\pi\sqrt{LC}} A_{loss} \tag{5.24}$$

where it is assumed that the Q-factor of the inductance dominates the overall Q and equivalent series resistance of the inductor is r_s. It is shown in [30] that

$$A_{loss} = \sqrt{1 - \frac{r_s^2 C}{L}} \tag{5.25}$$

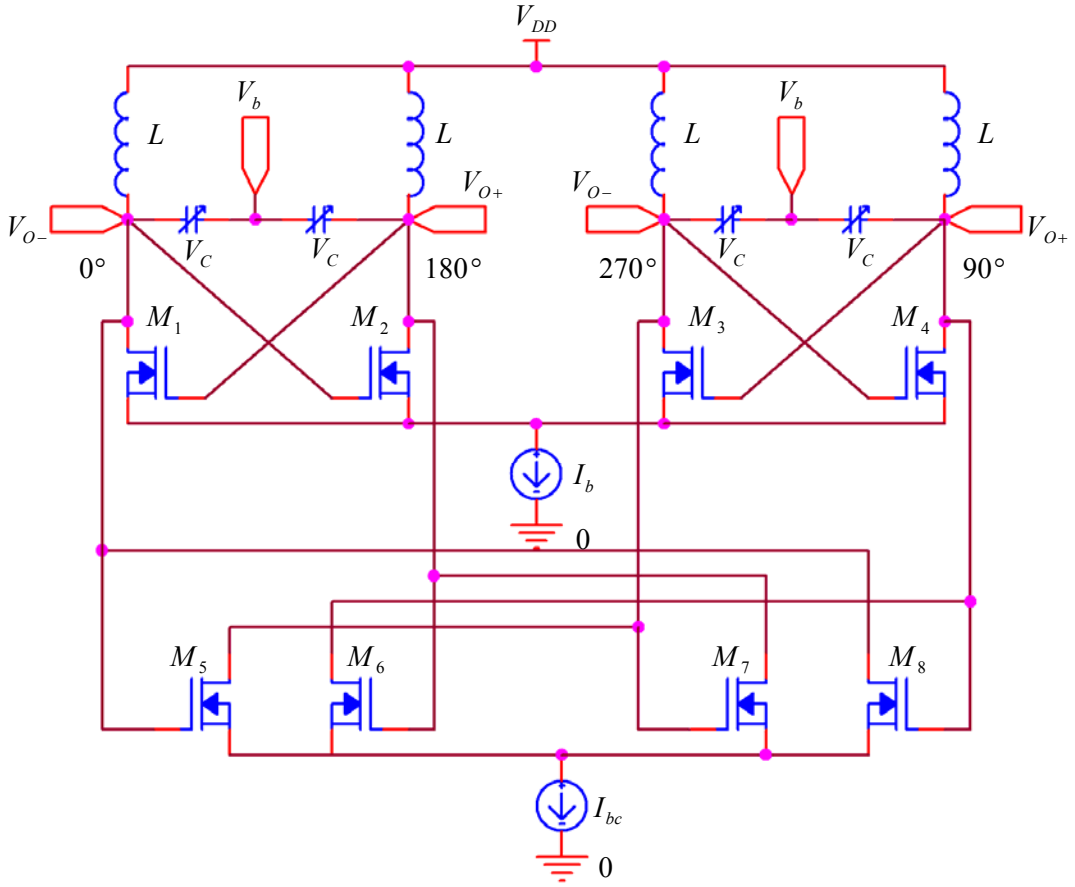


Figure 5.40. The figure shows the complete LC oscillator schematic with the required modifications to improve amplitude and phase matching.

The theory, design and simulation of the inductor (of value 10 nH (chosen for this case)) has been detailed in chapter 6 (and Appendix A). SONNET provides a SPICE model for the inductor; this is similar to the model obtained in 6.2. The Q_{IND} can be computed by

$$Q_{IND} = \frac{f}{\Delta f} = \frac{2\pi f_o L}{R_s} \tag{5.26}$$

The result (for different frequencies) has been graphed in figure 5.41 (theoretically) and figure 5.42 (using the more accurate simulations (5000 points & model obtained from SONNET)).

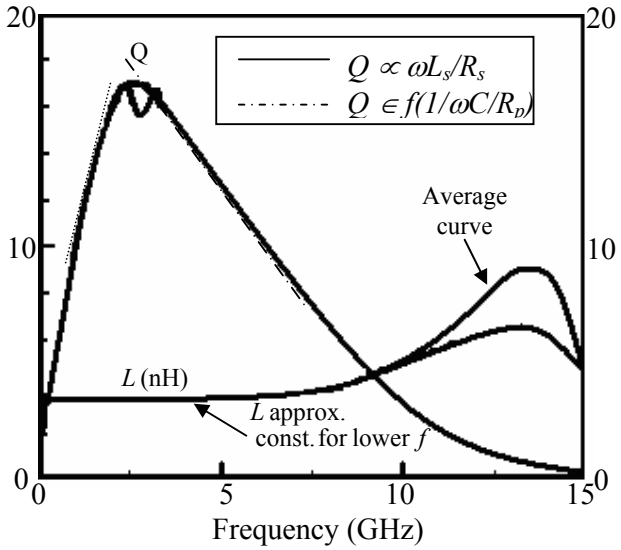


Figure 5.41. The figure shows the Q and L values as a function of frequency (GHz).

For test purposes, a copper inductor was also tested (by simulation) on an ideal substrate. The model was again obtained using the built-in SPICE conversion function in SONNET. The model obtained (as a netlist) was used instead of the ideal inductor, L_p in figure 5.33. Post-simulation results are shown in figure 5.42.

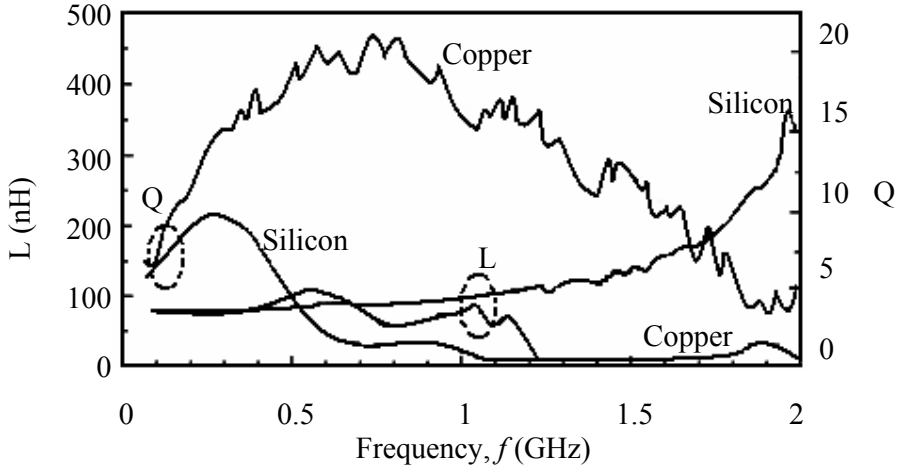


Figure 5.42. The figure shows the inductor quality factor, Q and the inductance value, L as a function of frequency (GHz) for a copper inductor on an ideal substrate.

5.2.1.2.8 Varactor design

Although the inductor dominates the overall Q-factor of the LC-tank, a good quality varactor is important to avoid further degrading the tank quality. In other words, the series resistance of the variable capacitor should be small. Commonly used varactors include the PN junction varactors, the PMOS varactors and the accumulation mode varactors. The structures of these varactors are shown in figure 5.43.

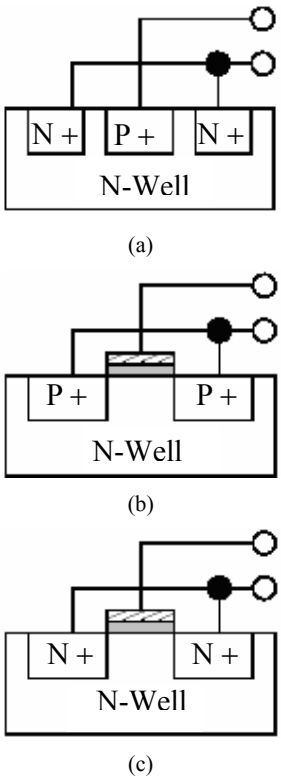


Figure 5.43. The figure [1] shows a) PN junction varactor, b) an PMOS capacitor varactor and c) an accumulation mode varactor.

The PN junction varactor consists of a P_+ and an N_+ region residing in an N-well. The depletion region is formed between the P_+ region and N-well. The tuning range provided by a PN junction varactor varies with the doping profile. Typical PN junction varactors provide a ±10 % tuning range. The PMOS varactor utilizes the gate capacitance of a PMOS transistor. While providing a wider tuning range than the PN junction varactors, the tuning range of the PMOS varactors is limited by the source and drain parasitic capacitance. In an accumulation mode varactor, the contacts replace the source and drain of a PMOS varactor. Accumulation mode varactors achieve a tuning range of ±30 % after the removal of the parasitic source/drain capacitance. As discussed in the section preface, a varactor with approximately ±5 % tuning range fulfils the basic requirements for the LC oscillator. Hence, a PN junction varactor is used for this project. This has additional advantages in that it is simple to design and implement. The varactor can be modelled as shown in figure 5.44.

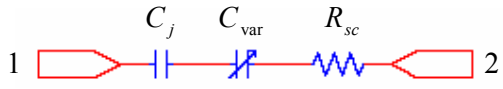


Figure 5.44. The figure shows a simplified model for a varactor.

The junction capacitances, C of an array of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage, V [46]. The junction capacitance per drawn area, C_J, the junction capacitance per unit area, C_{JSW}, the junction potential, P_B, the area junction grading coefficient, M_J and the sidewall junction grading coefficient, M_{JSW} are then extracted from

$$C_{\text{var}} + C_{fv} = \frac{WLC_J}{\left(1+\frac{V}{P_b}\right)^{MJ}} + \frac{2(W+L)C_{JSW}}{\left(1+\frac{V}{P_b}\right)^{MJSW}}, \tag{5.27}$$

where:

W: Junction width

L: Junction length

C_{JSW}: sidewall junction capacitance per unit area (0.53 fF/μm^2)

C_J: junction capacitance per drawn area

P_B: junction potential (0.53 V)

M_J: area junction grading coefficient (0.34)

M_{JSW}: sidewall junction grading coefficient (0.29)

As suggested [1], let $W = 2L = 145$ μm (to achieve a capacitance of about 1.48 pF). The other variables (above) are taken from the AMS process parameter document. The typical layout for the varactor is shown in figure 5.45 [33].

5.2.1.2.9 Frequency of oscillation

The oscillation frequency reduction factor A_{loss} (using equation (5.25)) is around 0.8 with the estimated r_s. The total capacitance, C of the node can be approximated by

$$C \approx (C_{var} + C_{fv}) + C_A + C_{coup} + C_L, \tag{5.28}$$

where

C_{var}: the variable capacitance provided by the varactor,

C_{fv}: fixed part of varactor's capacitance,

C_A: parasitic capacitance of the negative G_m cells,

C_{coup}: parasitic capacitance of the coupling transistors, and

C_L: capacitive loading of the subsequent stage.

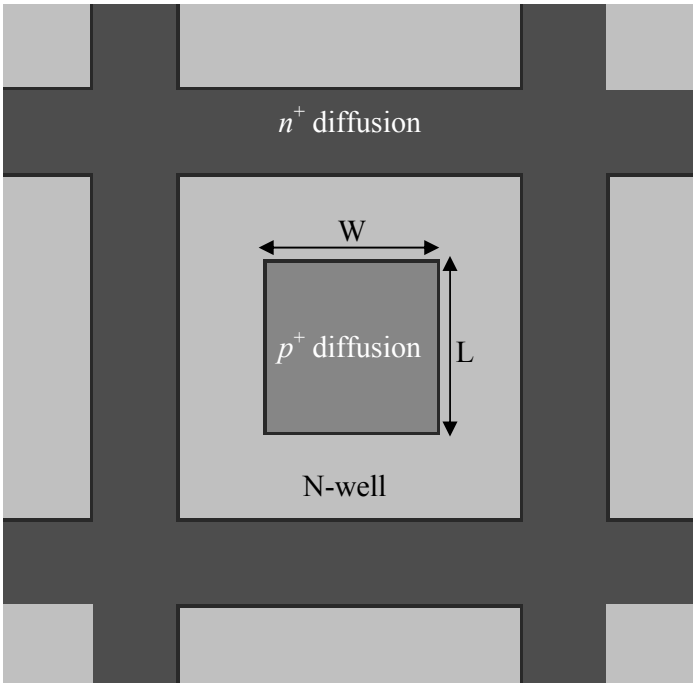


Figure 5.45. The figure shows the typical layout for the PN junction capacitor, [1].

Thus, the total capacitance consists of the fixed parasitic capacitance and a variable capacitance part provided by the varactor. The larger the inductance used, the smaller the capacitance required and lower power consumption can be obtained. However, in order to have large enough tuning range, the resulting C cannot be set to too small value. In this design, L is fixed to 10 nH and C is roughly 2 pF. The value of (C_{fv} + C_{var}) is around 1.48 pF. The overall effective single-ended series resistance of the LC tank can be calculated using [9]

$$R_{eff} = R_s + R_{sc} + \frac{1}{R_A (2\pi f_o C)^2}, \tag{5.29}$$

where:

R_s: effective series resistance of the inductor,

R_{sc}: effective series resistance of the varactor, and

R_A: impedance of the g_m cells.

In calculation the value R_s is double the value given in table 6.2 (and beneath the table) this in order to take the high frequency substrate loss into account. The Q factor of the varactor is assumed to be around 30 (computed by $1/\omega(R_{sc}(C_{fv}+C_{var}))$) and equivalently it is equal to R_{sc} of approximately 20 Ω for a varactor's capacitance of 1.48 pF. In this design, the resulted R_{eff} is approximately 31.5 Ω.

5.2.1.2.10 Transistor geometry specifications

The negative transconductance, g_m required can be calculated from

$$g_m = 2R_{eff}\left(\frac{\omega_o C}{2}\right)^2 = \frac{2R_{eff}}{(\omega_o 2L)^2}, \tag{5.30}$$

where

R_{eff}: effective single-ended series resistance of the LC tank (as in equation (5.29)),

C: total single-ended capacitance, and

L: single ended inductance of the LC tank.

The required g_m is around 11.3 mS but in order to ensure proper start-up of the oscillation, the transconductance value used (G_m) is double of this required value. The W/L ratio of the transistors in the negative g_m pairs are given [33]

$$\left(\frac{W}{L}\right)_{M_1} = \frac{G_m}{2\mu_n C_{ox}\left(V_{gs} - V_t\right)_{M_1}}, \tag{5.31}$$

where

C_{ox}: oxide capacitance (typical 2.3 fF/μm^2),

G_m: transconductance value (as above G_m = 22.6 mS),

V_t: threshold voltage (typical 0.5 V), and

μ_n: effective channel mobility (typical 400 cm^2/V/s).

As discussed earlier and in [28], the size of the coupling transistors must be the same as the size given by equation (5.31). Furthermore, the bias current is approximated by

$$I_b = \frac{G_m}{2}\left(V_{gs} - V_t\right)_{M_1}. \tag{5.33}$$

The realization of the current source (MOS) is discussed in the next sub-section. The latter configuration (of section 5.2.1.2.11.2) is used for output resistance advantages that the Wilson Current source provides.

5.2.1.2.11 Current Source

5.2.1.2.11.1 The simple current mirror

The simple current mirror is depicted in figure 5.46. The circuit supplies a constant current, I_{out}. The gate and drain of the transistor, M_1 are joined together. When the gate-source

voltage of M_1 exceeds the threshold voltage V_{T2}, it remains in the saturation region and draws constant current. The equation given (as part of figure 5.46) can be obtained by using Kirchhoff's laws in conjunction with simple transistor equations.

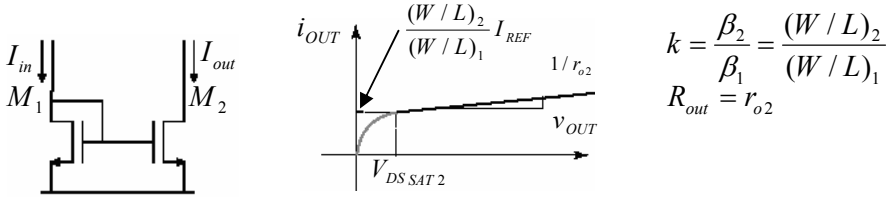


Figure 5.46. The figure shows the simple current mirror. The equation describing the reflection coefficient (gain) and the output resistance are also given, [34]. Note that $k = 1$ for identical transistors.

5.2.1.2.11.2 The Wilson current mirror

Figure 5.47 depicts the Wilson current mirror. The additional transistor M_4 is needed in order to have the same drain-to-source voltage for M_1 and M_2 and therefore to eliminate the effect of the finite output resistance of the bottom current mirror.

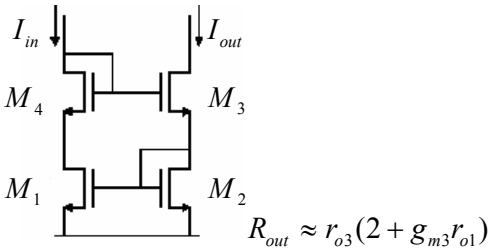


Figure 5.47. The figure shows the Wilson current mirror. The equation describing the output resistance is also given, [34].

5.2.1.2.12 Phase noise

The expected phase noise at 1 MHz offset can be [5] estimated by

$$L\{1MHz\} = \frac{kT(2R_{eff})(1+A)\left(\frac{f}{\Delta f}\right)^2}{\frac{V_A^{\,2}}{2}} \approx 135 \left[\frac{\text{dBc}}{\text{Hz}}\right], \qquad (5.34)$$

where

k: Boltzmann's constant, 1.38×10^{-23} W.s/K,

T: absolute resistor temperature in Kelvin, K (Assume about 300 K),

A: noise-amplifying factor of the amplifier, and

V_A: differential output amplitude (Assume about 3.3 V).

The factor A is roughly governed by the additional current used for the proper start up of the oscillation and it is around 2 in this design. Equation (5.34) shows that the phase noise is increased with the square of the centre frequency and decreased with the square of the oscillation amplitude. Figure 5.49 graphs the output power as function of the offset frequency.

5.2.1.2.13 Complete LC oscillator simulation

The basic LC oscillator is shown in figure 5.33. The complete circuit evolution is discussed in section 5.2.1.2.2 & 5.2.1.2.3. Simulation results in the frequency domain for the LC oscillator (for $V_b = V_{cont} = 1.56$ V (figure 5.36)) is shown in figure 5.48.

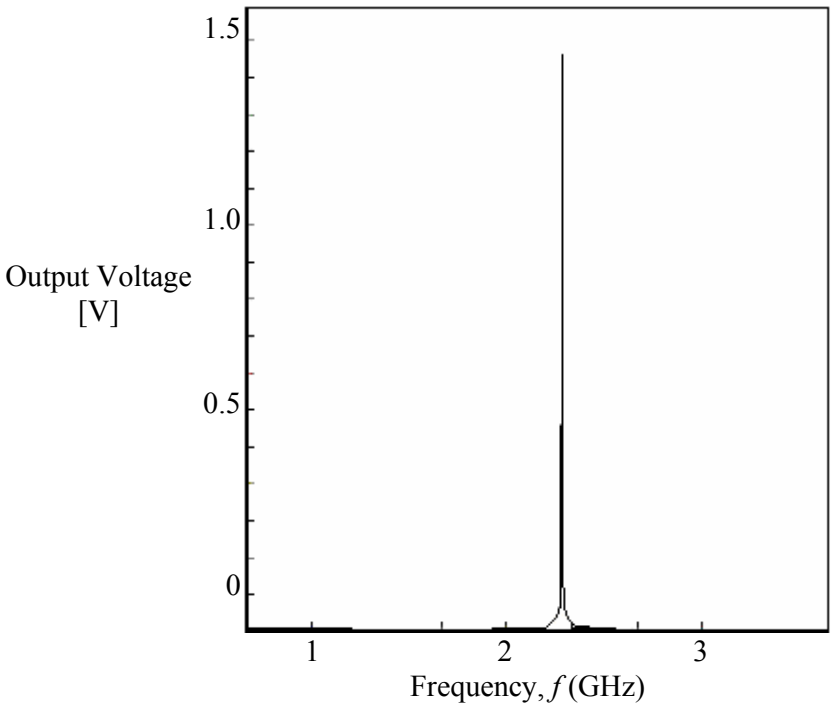


Figure 5.48. The figure shows the frequency domain simulation results from the complete LC oscillator.

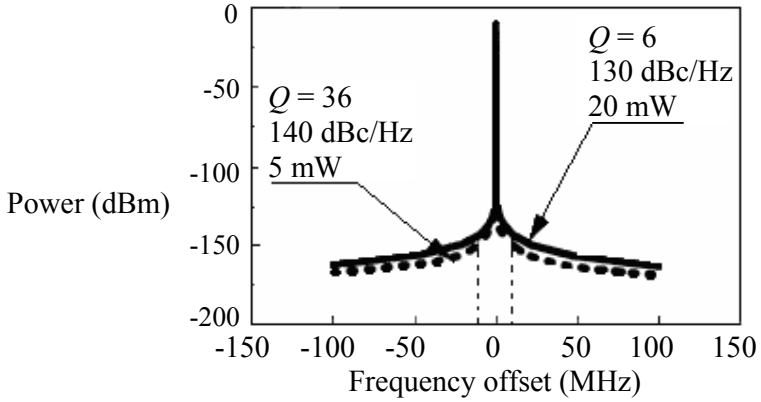


Figure 5.49. The figure graphs the output power as function of the offset frequency.

5.2.1.3 Ring oscillator

The requirements of the lower-loop oscillator include: having a centre frequency of 600 MHz and a tuning range around 400 MHz with the tuning voltage vary from 0 to 2 V. The phase noise should be smaller than –108 dBc/Hz at 1000 kHz offset from the carrier. In order to obtain such a large tuning range, a ring oscillator is used instead of a LC-tank oscillator, which has a typical frequency-tuning range limited to around 10-20 % [3]. The feasibility of a low noise CMOS ring oscillator is comparable with the performance of monolithic LC oscillators [61]. The block diagram of a ring oscillator is given in figure 5.50. The structure of the ring oscillator also employs positive feedback to achieve oscillation. However, as switching is involved, it can no longer be treated as an LTI system and all the results developed in subsection 5.2.1.1 are no longer applicable. Thus, the oscillator is analysed and designed (in the next subsections) using large signal time domain analysis.

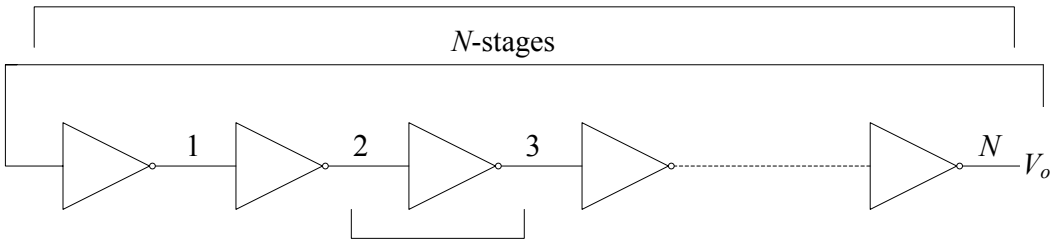


Figure 5.50. The figure shows the block diagram of ring oscillator.

Figure 5.51(a) depicts a *N*-stage ring oscillator realised using differential cells (which have complementary outputs). A source coupled pair (SCP) inverter will be a typical implementation. Assume that at time t_0 the output of stage 1 changes to logic 1 (denoted by edge a), as shown in figure 5.51 (b). When this logic 1 propagates to the end, it creates

a logic 1 at the *N*th stage, which, when fed back to the input of the first stage, creates a logic 0 in the first stage output. This is edge b. When this logic 0 is propagated through the chain again, it toggles the output of state 1 and triggers edge c. Notice that it takes two passes through the chain to complete a period. (Each pass generates an edge transition, and an up transition followed by a down transition is required to complete a period). Denoting t_p as the propagation delay through each state, then period $T = 2Nt_p$. For a single-ended output cell, N has to be odd, but for a differential cell N can be odd/even, to start an oscillation. The minimum value of N depends on the ω_0 and t_p available from a given technology. Assuming that 180º of phase shift is provided by the chain of N stages, each stage must provide $\frac{180^\circ}{N}$ of phase shift and sufficient gain (so that the overall gain is greater than 1) at ω_0. This also implies that the gain of each individual stage has to be greater than 1 as well.

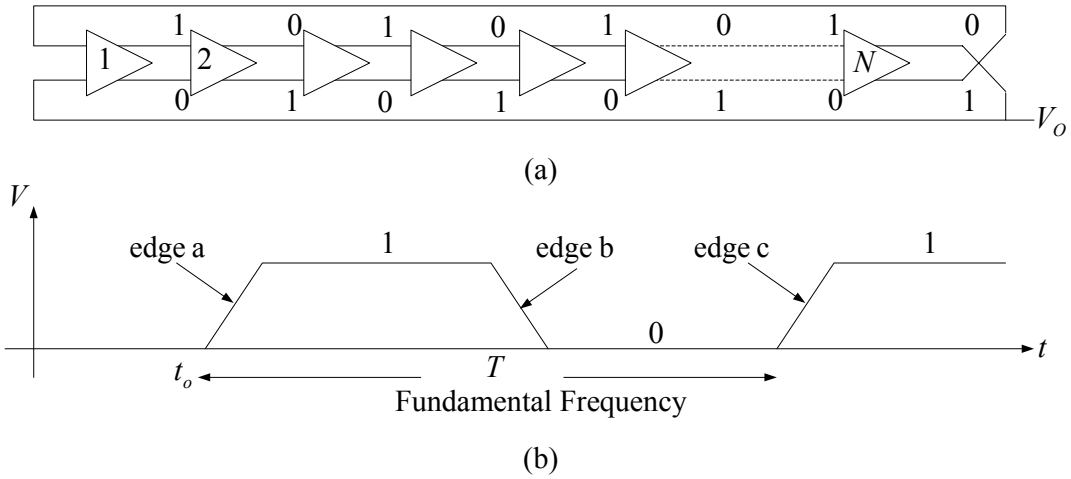


Figure 5.51. The figure shows (a) Differential implementation of ring oscillator, and (b) Corresponding waveform

5.2.1.3.1 Delay cells

There are many features that differentiate the delay cells used in a ring oscillator. The most important, perhaps, is the slew time. Contrary to popular belief, it is actually the slew time (a dynamic parameter), rather than the interstage gain (a static parameter), that determines the overall phase noise performance [62]. The delay cells used in ring oscillators can be categorized into three different types. The first type is a fast-slewing saturated delay cell [63]. This delay cell has fast rise and fall time. It also performs full switching and, therefore, belongs to the saturated class of delay cells. An example that

consists of one voltage-based inverter plus a Schmitt trigger and a buffer is shown in figure 5.52.

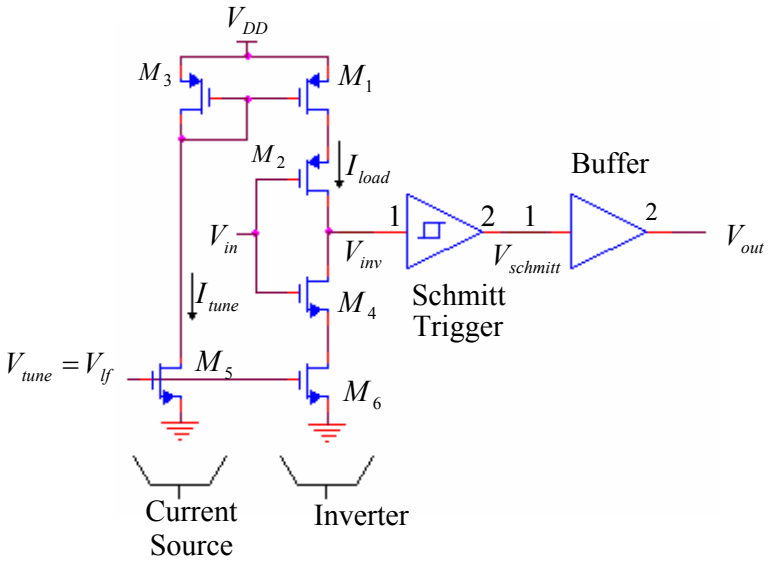


Figure 5.52. The figure shows a fast-slewing saturated delay cell, [63].

In figure 5.52, the delay time is determined by the amount of current supplied through the current source, the input capacitance, and the Schmitt trigger threshold. The current supplied is adjusted by the tuning voltage, V_{tune}. The Schmitt trigger gives the fast rising and falling. As shown, each PMOS and NMOS device of the input inverter completely turns off upon switching. Figure 5.53 shows the output voltage swings of three such adjacent delay cells.

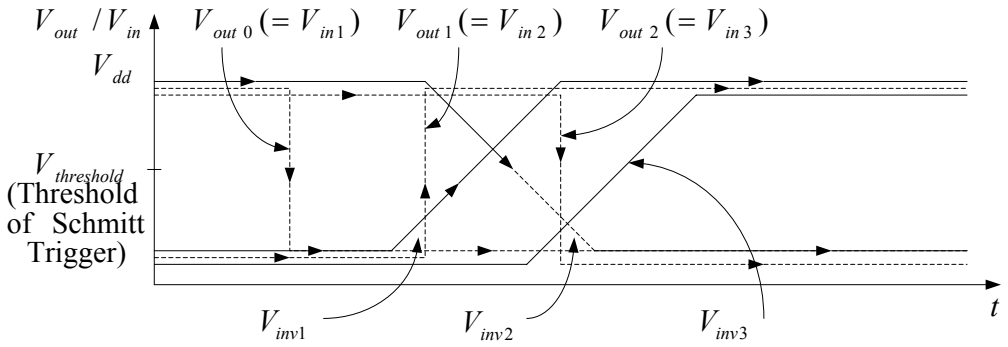


Figure 5.53. The figure shows the waveform of three cascaded fast-slewing saturated delay cells.

In figure 5.53, the three dotted lines are inputs V_{in1} - V_{in3} and the three solid lines are output of the input inverters, V_{inv1} - V_{inv3}. The figure can be discussed by starting from V_{in1} (the first dotted line) and assuming that it drops abruptly. The inverter takes time to change. Therefore, V_{inv1} (the first solid line) rises slowly. As soon as it hits the threshold of the

Schmitt trigger, $V_{schmitt1}$ rises abruptly, resulting in V_{out1} rising abruptly. Now this V_{out1} is connected to V_{in2} and so V_{in2} rises abruptly again (second dotted line). V_{in2} has the same steepness as V_{in1}, but is delayed from V_{in1} by a certain period. The process repeats itself, as V_{inv2} (second solid line) responds to V_{in2} and drops slowly. Therefore, V_{inv2} is delayed from V_{inv1} by the same delay as V_{in2} is from V_{in1}. Finally, the process is repeated for the third stage, whose input is V_{in3} (third dotted line) and whose inverter output is V_{inv3} (third solid line). In general, the following observations can be made:

1. V_{inv} changes slowly, whereas V_{in} changes abruptly.
2. From one stage to the other: V_{in} and V_{inv} change in the opposite direction.
3. V_{inv} starts to change when V_{out} from the previous stage hits the voltage rail (either V_{dd} or ground).
4. $V_{schmitt1}$ and, hence, V_{out} (and the next stage V_{in}) start to change when V_{inv} crosses $V_{threshold}$, the threshold voltage of the Schmitt trigger. Usually, the Schmitt trigger has two thresholds. To simplify this discussion, only one threshold was assumed.

This design is considered a fast-slewing delay cell due to rapid switching of V_{out} (made possible by the use of the Schmitt trigger.) Another variation of this type of delay cell consists of only one inverter without buffer.

The second type of delay cell is a slow-slewing saturated delay cell. An example of this type is shown in figure 5.54. Here, the inverter consists of a SCP and, hence, this is a current-based inverter. In this case, full switching also occurs. Therefore, this delay cell belongs to the saturated class of delay cells, just like the one described earlier (in figure 5.52.) The type of delay cell is called slow slewing as it has a longer gate delay. Due to the square law drain current characteristics, the delay is inversely proportional to the voltage swing. For a low-supply voltage, V_{dd}, the voltage swing is typically less than 1 V, making the delay much longer than the fast-slewing cell of figure 5.52. Another difference from the fast-slewing cell is that the load consists of resistors realised by biasing the transistor into the triode region. As this resistor is a function of the drain current (which is not true for a real physical resistor), the RC time constant, and hence the f_o can be tuned by varying I_{tune}.

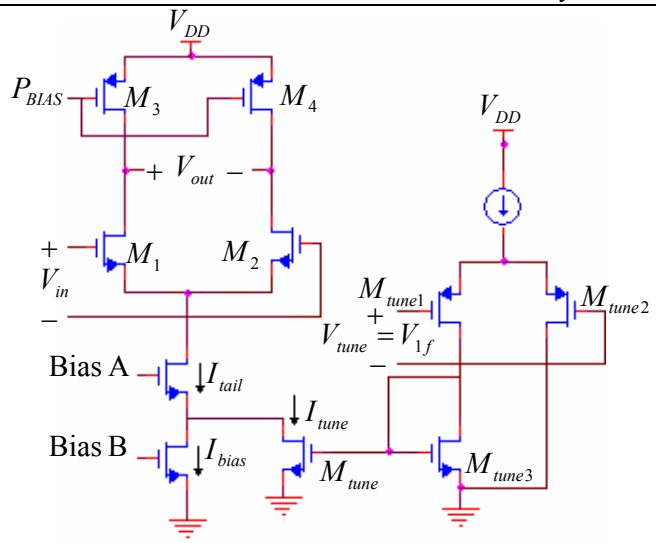


Figure 5.54. The figure shows the slow-slewing saturated delay cell, [64].

Figure 5.55 shows the output voltage swings of three such adjacent delay cells. Compared with the dotted lines of Figure 5.53 (which correspond to the outputs of the fast-slewing cells), the delay is longer and the rise and fall time is longer (due to the lack of the Schmitt trigger and the extra delay). Nonetheless, this delay cell is still saturated as the output goes all the way between V_{dd} and ground, which means that the devices are completely turned on/off.

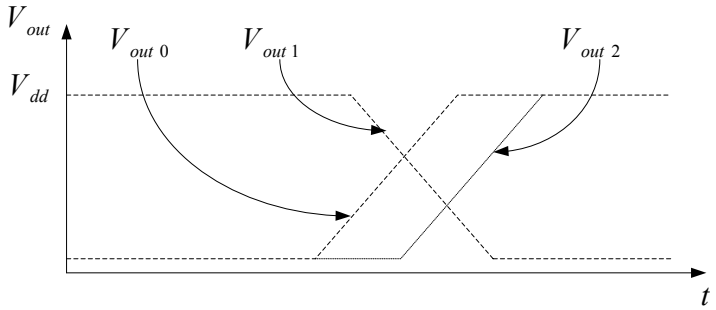


Figure 5.55. The figure shows the waveform of three cascaded slow-slewing saturated delay cells.

The third type of delay cell is the non-saturated delay cell [64] as shown in Figure 5.56. This is also a voltage inverter-based delay cell. Compared with Figure 5.52, it does not have a Schmitt trigger to enable fast turning on/off. Compared with both figure 5.52 and figure 5.54, the transistors M_1, M_2, M_3, M_4, M_6 and M_8 never fully turn on/off. As a result, as shown in Figure 5.57, the output waveforms V_{out0} - V_{out2} never reach V_{dd} or ground (thus, the type of delay cell is classified as non-saturated.)

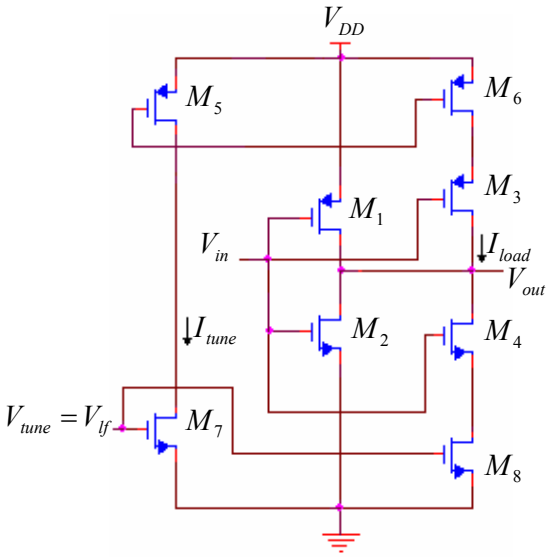


Figure 5.56. The figure shows a non-saturated delay cell, [64].

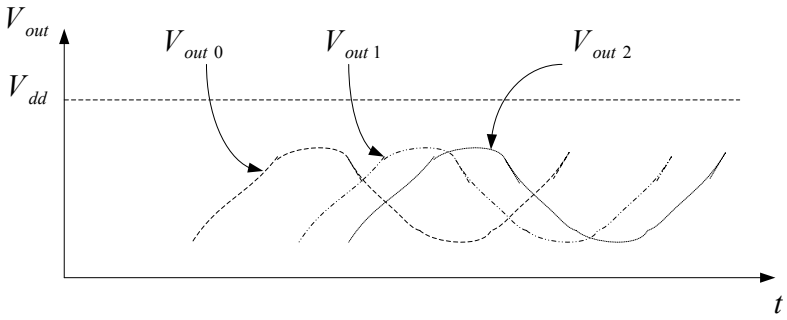


Figure 5.57. The figure shows the waveform of three cascaded delay cells.

5.2.1.3.1.1 Tuning

To calculate f_o:

$$f_o = \frac{1}{2Nt_p} \tag{5.35}$$

where N is the number of stages and t_p is the delay of each stage.

To calculate K_{vco} [5]:

$$K_{vco} = 2\pi \frac{df_o}{dV_{tune}} \tag{5.36}$$

To derive the parameters above, two classes of ring oscillators will be defined:

- a delay cell with an active load (for instance, figure 5.52); and
- a delay cell with a resistive load (for instance, figure 5.54).

The delay cells differ in the functional dependence of t_p on circuit components and tuning voltage.

5.2.1.3.1.2 K_{vco}: Delay cell with an active load

From figure 5.52 (as an example), at V_{inv} node,

$$I_{load} = C_l \frac{V_{swing}}{t_p} \tag{5.37}$$

where C_l is the load capacitor at V_{inv}, and V_{swing} is V_{inv}'s voltage swing.

Substituting (5.37) into (5.35),

$$f_o = \frac{I_{load}}{2C_l V_{swing} N} \tag{5.38}$$

Taking differentials on both sides yields

$$df_o = \frac{dI_{load}}{2C_l V_{swing} N} \tag{5.39}$$

From figure 5.52, $I_{load} = I_{tune}$ and so $dI_{load} = dI_{tune}$. Hence,

$$df_o = \frac{dI_{load}}{2C_l V_{swing} N} \tag{5.40}$$

Finally, substituting (5.40) into (5.36):

$$K_{vco} = 2\pi \frac{df_o}{dV_{tune}} = 2\pi \frac{dI_{tune}}{2C_I V_{swing} N dV_{tune}} = \frac{2\pi G_m}{2C_I V_{swing} N} \tag{5.41}$$

The last equality uses the definition $G_m = dI_{tune}/dV_{tune}$, where G_m is the transconductance of tuning transistor M_5 and M_6.

5.2.1.3.1.3 K_{vco}: Delay cell with resistive load

Figure 5.58 models the loads (M_3 and M_4) and device parasitic capacitances of figure 5.54 as R_1 & R_2 and C_1 & C_2, respectively. This dissertation considers the design with this kind of a delay cell. To derive f_o, t_p is required (as per equation (5.35)) [62]:

$$t_p = R_1 C_1 \ln 2 \tag{5.42}$$

It is further derived (using figure 5.58 & equations (5.35 & 5.36)) [62] that for figure 5.54, for a constant P_{bias},

$$K_{vco} = \frac{-2\pi f_o R g_{m_{Mtune1}}}{k_p (W/L)_3 (V_{GS3} - V_T - v_{DS3})^2} \tag{5.43}$$

For a constant V_{swing} ($= RI_{tail}$ ($R_1 = R_2 = R$)),

$$K_{vco} = \frac{2\pi f_o g_{m M_{tune1}}}{I_{tune}} \tag{5.44}$$

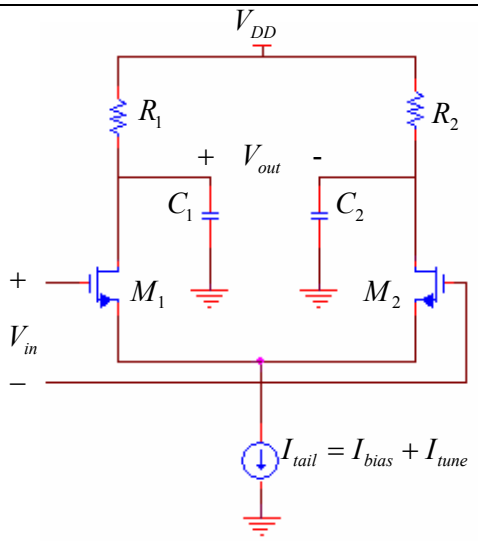


Figure 5.58. The figure shows the simplified slow-slewing saturated delay cell circuit schematic.

As with the K_{VCO} of an LC oscillator, K_{VCO} of a ring oscillator should be designed as small as possible [62], yet large enough so that f_o can span the whole frequency range.

5.2.1.3.2 Transistor geometry specifications

From the discussions in the earlier section, it is clear (for the design of figure 5.54), f_o depends on M_1, M_3, and M_1' (the next delay stage), [62] & K_{VCO} depends on M_3 and M_{tune1}. The following design steps are used to determine the transistor aspect ratios:

1. The load (M_3) is designed to satisfy low power requirements (say, less than 30 mW.)
2. The transconductance, g_m (M_1 & M_2) is designed to satisfy the f_o requirement.
3. Design the VCO gain, K_{VCO} to achieve the requirements set in the preface of section 5.2.1.3.

For N = 4, the following aspect ratios are obtained: $(W/L)_1 = (W/L)_2$ = 320/0.35 and $(W/L)_3$ = 35/0.35

5.2.1.3.3 Phase noise

The average noise contributed to the circuit from the switching thermal noise current sources of the MOS devices is approximated as proportional to the factor (t_{on}/T), where t_{on} is the on time of the transistors and T is the oscillation period. In this design, it is assumed

that this factor is equal to ½ due to turning off NMOS and PMOS devices half of the whole period. It is further assumed the worst case noise performance is at the highest operation frequency due to the trade off between phase noise and carrier frequency. The size of the latch is only half of the other device's size. Also, the g_m of the NMOS transistors, M_1 and M_2, and that of the PMOS transistors, M_3 and M_4, are adjusted to be the same. Thus, the total average noise can be written as follows:

$$\frac{i_n^{\,2}}{\Delta f} = \frac{t_{on}}{T}\left(\frac{i_{n,NMOS}^{\,2}}{\Delta f} + \frac{i_{n,PMOS}^{\,2}}{\Delta f} + \frac{i_{n,LATCH}^{\,2}}{\Delta f}\right) \tag{5.45}$$

where

$$\frac{i_{n,NMOS}^{\,2}}{\Delta f} = \frac{i_{n,PMOS}^{\,2}}{\Delta f} = 2\frac{i_{n,LATCH}^{\,2}}{\Delta f} \tag{5.46}$$

and,

$$\frac{i_{n,TRANSISTOR}^{\,2}}{\Delta f} = 4kT\gamma g_m \tag{5.47}$$

The noise is then calculated by assuming $\gamma = 0.8$ for short-channel devices. Finally, the phase noise in dBc/Hz at $\Delta\omega$ offset from the carrier can be calculated by [9]

$$L\{\Delta\omega\} = 10\log_{10}\left(\frac{2N}{2}\frac{\frac{i_n^{\,2}}{\Delta f}}{q_{\max}^{\,2}}\frac{\Gamma_{rms}^{\,2}}{2(\Delta\omega)^2}\right) \tag{5.48}$$

where $\Gamma_{rms} \approx 3/N^{1.5}$.

The $2N$ term is due to $2N$ nodes and thus $2N$ noise sources in the oscillator. The differential operation contributes the factor of 2 in the denominator. Using equation (5.48), the phase noise is predicted to be –90.2 dBc/Hz at 100 kHz and –112.4 dBc/Hz at 1000 kHz offset from the carrier. The differential output amplitude is from 1.92 V to 1.97 V.

5.2.1.3.4 Complete ring oscillator simulation

The ring oscillator implementation is obtained by incorporating the delay cell of figure 5.54 into the block diagram configuration of figure 5.51(a). A parametric sweep (with the bias voltage being the parametric variable) was done to verify if the desired frequencies can be obtained. The result is shown in figure 5.59.

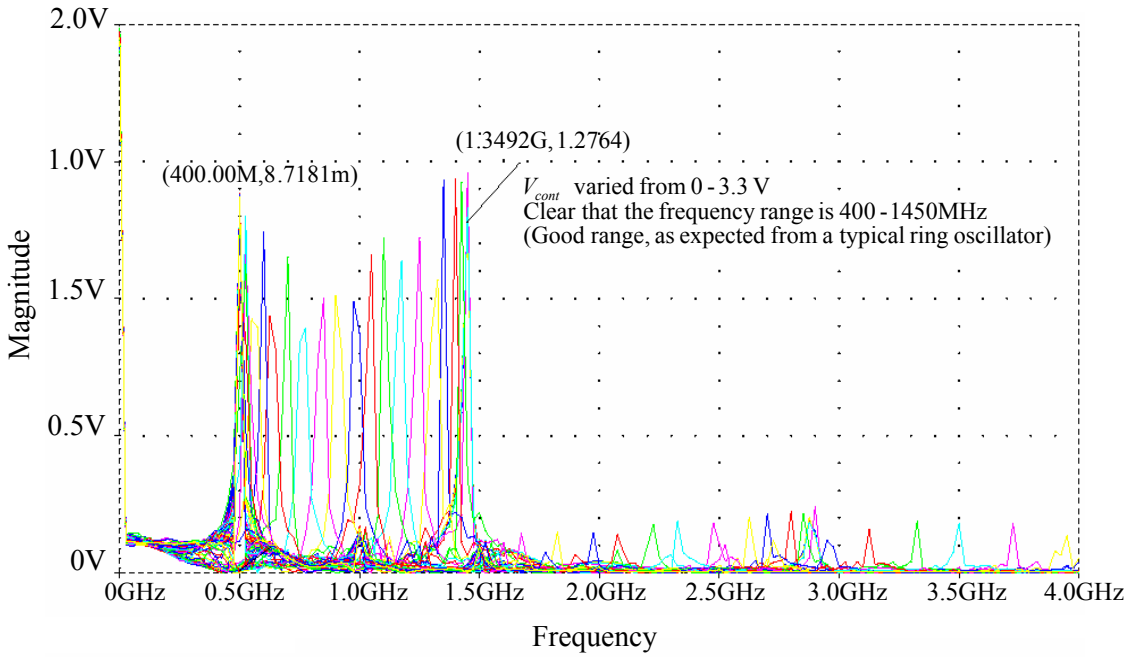


Figure 5.59. The figure shows the frequency domain results of the ring oscillator. Numerous curves are indicative of the wide spectra of signals that can be generated using this oscillator as required in the lower loop.

5.2.1.4 SSB mixer

In the upper-loop, a SSB mixer is needed to obtain the desired sideband for the high frequency prescalar output. Several methods are proposed to design a mixer [5]. The simplest method of achieving SSB is to implement a double side band (DSB) mixer using a Gilbert cell implementation. Thereafter, one of the bands can be filtered to obtain the desired frequency component. This is illustrated in figure 5.60.

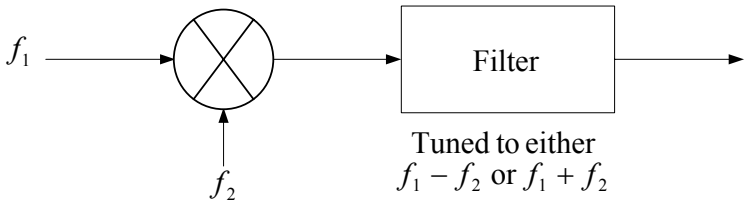


Figure 5.60. The figure shows a possible implementation for a SSB mixer.

However, the filter configuration shown in figure 5.60 is not practical for this project as the frequency components (f_1 - f_2) and (f_1 + f_2) are way too close, hence a very sharp filter would be needed, which would mean many more resistor and capacitor components. An alternative configuration, *I/Q* modulator configuration [2] will, hence, be used. The I/Q modulator configuration is shown in figure 5.61.

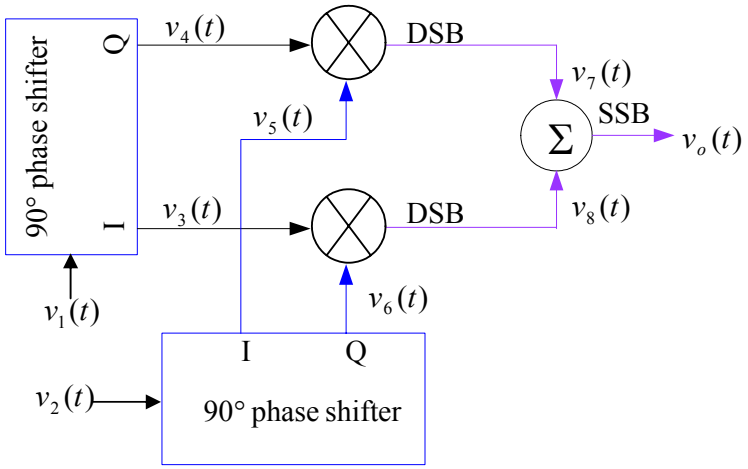


Figure 5.61. The figure shows the SSB mixer configuration using an *I/Q* modulator scheme.

The mathematical equations in figure 5.61 are defined as follows (assuming sinusoidal input waves):

$$v_1(t) = A_1 \cos(2\pi f_1 t) \tag{5.49}$$

$$v_2(t) = A_2 \cos(2\pi f_2 t) \tag{5.50}$$

$$v_3(t) = A_1 \cos(2\pi f_1 t + 90°) = -A_1 \sin(2\pi f_1 t) \tag{5.51}$$

$$v_4(t) = A_1 \cos(2\pi f_1 t) \tag{5.52}$$

$$v_5(t) = A_1 \cos(2\pi f_2 t + 90°) = -A_1 \sin(2\pi f_2 t) \tag{5.53}$$

$$v_6(t) = A_2 \cos(2\pi f_2 t) \tag{5.54}$$

$$v_7(t) = v_4(t)v_5(t) = -A_1 A_2 \cos(2\pi f_1 t)\sin(2\pi f_2 t) \tag{5.55}$$

$$v_8(t) = v_3(t)v_6(t) = -A_1 A_2 \sin(2\pi f_1 t)\cos(2\pi f_2 t) \tag{5.56}$$

$$v_o(t) = v_7(t) + v_8(t) = -A_1 A_2 \sin(2\pi(f_1 + f_2)t) \tag{5.57}$$

If the adding device in figure 5.60 was replaced by a subtract (difference) device, then the output would be as

$$v_o(t) = v_7(t) - v_8(t) = A_1 A_2 \sin(2\pi(f_1 - f_2)t) \tag{5.58}$$

The basic building block viz. the DSB mixers are implemented by a Gilbert cell. Translinear analysis [65] is used to simplify the circuit analysis. This is shown in figure 5.62. Results indicate that if I_2=I_5=*0*, then

$$I_o = I_1 I_4 \tag{5.59}$$

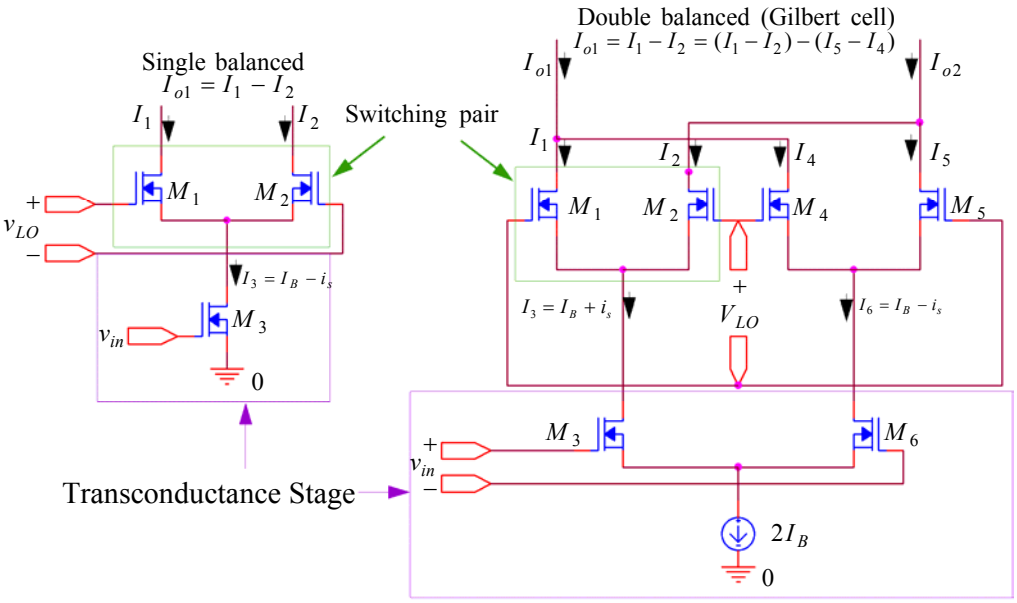


Figure 5.62. The figure shows the basic building block of the SSB mixer viz. the Gilbert cell.

The complete mixer is implemented by incorporating the Gilbert cell into the *I/Q* modulator shown in figure 50. The Gilbert cell is a "current multiplier" (hence nodal summation/difference is easily performed), hence PMOS transistors are used as resistors to convert to voltage. The complete schematic is shown in figure 5.63.

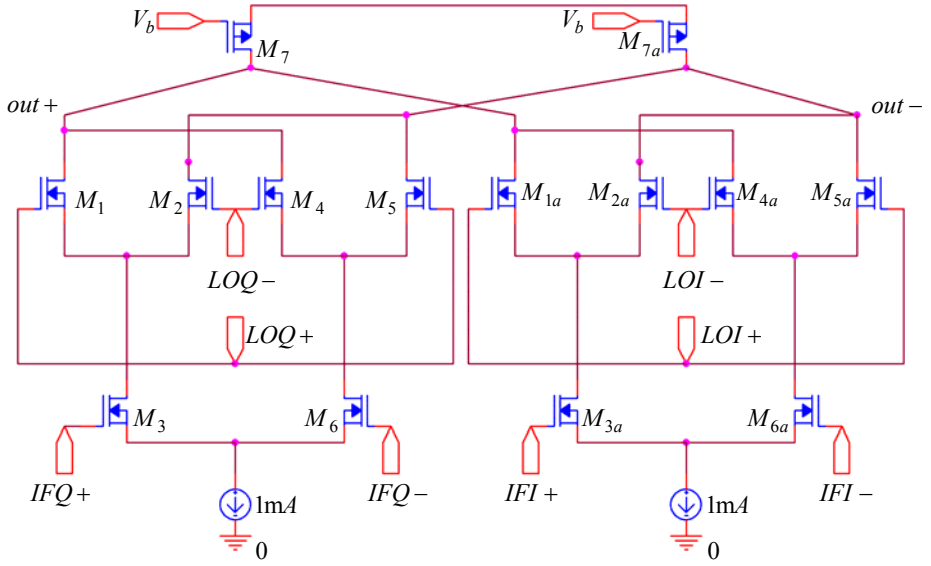


Figure 5.63. The figure shows the SSB mixer.

The LO terminals of the mixer are driven by the *I* and *Q* outputs of the ring oscillator and the IF terminals are connected to the *I* and *Q* outputs of LC oscillator. The resulting mixing currents are added together in the output nodes and convert to voltage by two linear transistors. In order to ensure a correct locking of the loop, the mixer should have small

gain and phase mismatch – this is achieved by careful symmetrical layout of both individual mixers. The linearity is not so important in this design because there is only a single dominant tone at the LC oscillator output. The current sources are implemented as discussed in section 5.2.1.2.11.

5.2.1.5 Loop filters

As the loop filter has been substantially discussed (mathematically) in sections 3.4.3-3.11, this will not be repeated in this section. This section will focus on the loop filter implemented for this dissertation. Briefly, the loop filter converts the charge pump error current, I_e, into the VCO control voltage V_c. Ignoring the smaller capacitor C_2 of figure 5.1, the loop filter has the following transfer function:

$$F(s)=\frac{V_c(s)}{I_e(s)}=\frac{R_1\left(s+\frac{1}{R_1C_1}\right)}{s} \tag{5.60}$$

The loop filter is the critical building block that determines the loop dynamics [6]. In a charge pump PLL, the natural frequency and the damping factor is set independently by the values of the components used in the loop filter. The capacitor, C_1, sets the natural frequency. The resistor sets the damping factor.

It is shown [1] that the PLL loop bandwidth has to be limited to a tenth of the input frequency. For simplicity [5], a passive filter implementation is used. A loop filter design software[1] is used to simplify the design process. For the complete loop filter shown in figure 5.1, the following transfer function is obtained.

$$F(s)=\frac{V_c(s)}{I_e(s)}=\frac{1}{s(C_1+C_2)}\frac{\frac{s}{\omega_z}+1}{\frac{s}{\omega_p}+1} \tag{5.61}$$

The poles and zeros of the shown transfer function are as follows:

$$\omega_z=\frac{1}{R_1C_1} \tag{5.62}$$

$$\omega_p=\frac{1}{R_1\frac{C_1C_2}{C_1+C_2}} \tag{5.63}$$

[1] The loop filter design software was obtained from www.national.com

Using the equations (of section 3.5-3.11) and (5.61)-(5.63), approximate values for the high-frequency PLL filter (LPF_1) zero and pole are at f_z = 20 kHz and f_p = 1 MHz, respectively. Likewise, for the low-frequency PLL filter (LPF_2) the zero and pole are f_z = 10 kHz and f_p = 300 kHz, respectively. The passive elements obtained from the loop filter design values are given in table 5.1

Parameters		Upper loop (LPF_1)	Lower loop (LPF_2)
Reference frequency	f_{ref}	144 MHz	1 MHz
Loop bandwidth	K_v	100 kHz	50 kHz
Charge pump current	I_c	1 µA	1 µA
Zero frequency	f_z	20 kHz	10 kHz
Pole frequency	f_p	1 MHz	250 kHz
Passive elements	R_1	20 kΩ	20 kΩ
	C_1	398 pF	796 pF
	C_2	8.1 pF	33.1 pF
Approximate chip areas	C_1	462790 µm^2	925580 µm^2
	C_2	9419 µm^2	38488 µm^2

Table 5.1. The table shows the basic frequency plan of the low pass filter. The passive element values obtained from the low pass filter software are also shown in the table. Approximate chip areas taken up by the passive elements are also indicated. These are obtained by using the AMS process parameters (*CPOX*: 0.86 fF/µm^2 and *RNWELL*: 1 kΩ/□).

The loop filter is fully integrated on chip by using poly2 – poly1 capacitors and a Nwell resistor as shown in figure 5.64. The key issue here is the silicon area associated with the filter components. Several contacts in parallel at both ends of the resistor allows the contact resistance to be effectively neglected.

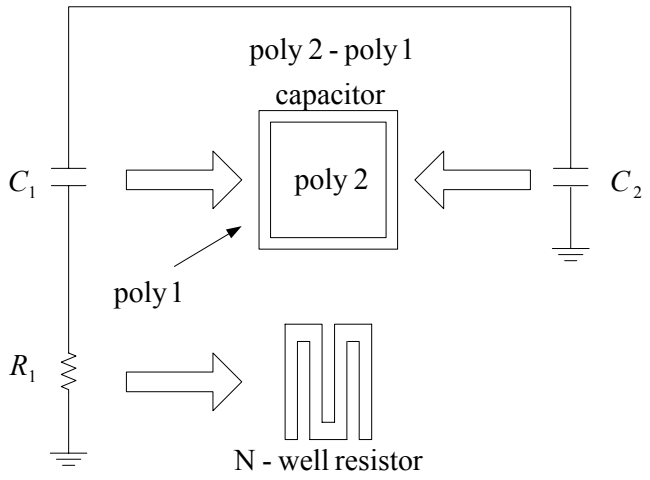


Figure 5.64. The figure shows the fully integrated loop filter.

5.3 Layout of the circuit

The synthesizer is basically laid out as per figure 5.65. Each block is placed as close to the previous block as possible in order to shorten the path of the signal passing through. It is extremely important for the high frequency signal paths. Some internal testing pads are added to examine the function of the building blocks. The power supplies of the circuits are separated so that individual blocks can be tested and there is less influence among the building blocks. In order to reduce the substrate noise coupling from the dividers and the ring oscillator to other circuits, guard rings are placed around these noisy circuits. Some large guard rings [3] are placed surrounding the inductors because it can absorb some amount of the eddy current (as discussed in section 6.4) induced under the inductors. In order to achieve better isolation of the noise, the ground of the guard rings is connected to a separated bonding pad. In the layout, the grounds of the loop filters, LC oscillator, ring oscillator and other digital circuits are connected to separate pads to minimize the problem of ground bounce. The digital ground and the analogue ground are also connected to the different DC bonding pads. Possible testing structures of the passive components included inductor, capacitor and varactor are included for high-frequency measurements and characterization.

Completed layouts for the LC VCO, the ring oscillator, the SSB mixer and the low pass filters are provided in Appendix B. For the digital subsystems, digital libraries (provided as part of the AMS 0.35 μm CMOS process) are used. The exact layout of the individual digital blocks provided by AMS is not accessible to clients (due to AMS proprietary regulations).

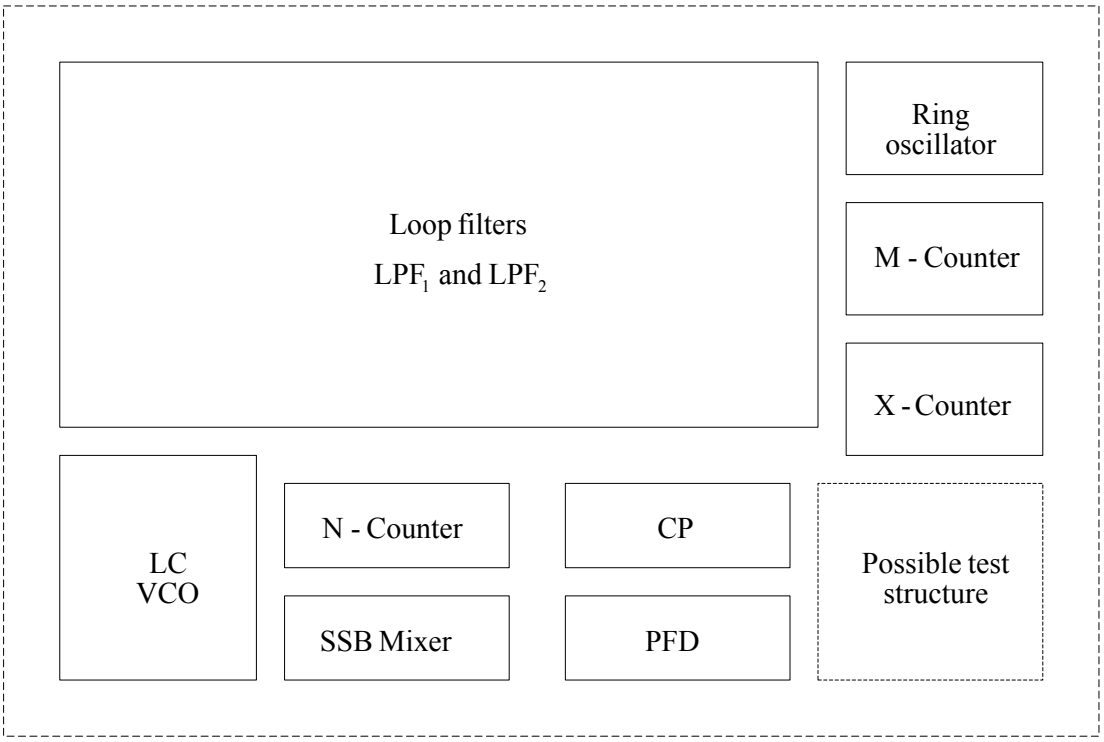


Figure 5.65. The figure shows the floor planning of the layout.

5.4 Models, simulation & verification

Several software (as mentioned in the preceding sections) have been used for the verification of the sub-systems. While some simulation results have already been provided in the preceding sub-sections, this section aims to completely provide relevant results obtained. Intensive simulations were done to ensure functionality of each subsystem prior to system integration. A subsystem is declared functional once it achieves all the subsystem specifications as provided in section 4.3. Technical performance is measured on successful verification of the complete system specifications (i.e. after integration of all the subsystems.) Most of these specifications for the CMOS implementation can be easily verified from the simulation results in ORCAD.

Each subsystem was modelled as a hierarchical block to simplify modelling and simulation. This was also necessary to save time (as there are a lot of basic digital blocks that are used more than once). The complete hierarchical model of the system is shown in figure 5.66. This figure shows one of the typical test settings used for the final post subsystem integration simulations. Test results are shown in the next sub-sections.

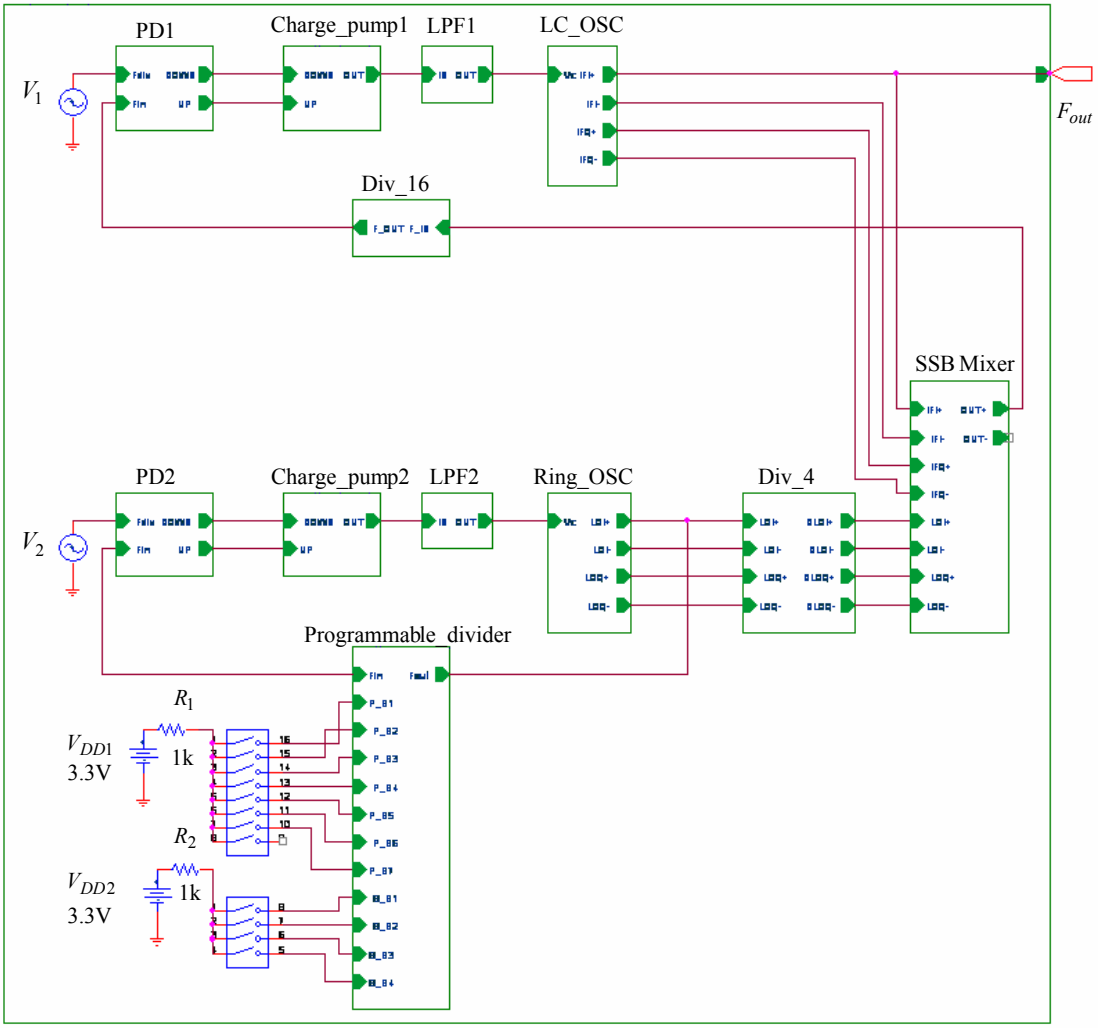


Figure 5.66. The complete hierarchical diagram of the complete frequency synthesizer. SPICE (Tanner Tools) automatically descends through the hierarchy to the lowest (transistor, resistor, capacitor, inductor, diode and power supply) levels during simulation.

The total number of devices used in the complete CMOS implementation: 2482 MOS (NMOS and PMOS) transistors, 12 capacitors, 7 resistors, 4 inductors, 4 varactors, and a common power supply of V_{DD} = 3.3 V.

5.4.1 Simulation results

In some instances, the simulation results have already been provided in an earlier sub-section of this chapter (in order to assist or substantiate a discussion.) Results that have not been provided earlier are provided in this section.

5.4.1.1 Digital subsystem 1: Phase-frequency detectors (PFD_1 & PFD_2)

Two arbitrarily inputs, V_r and V_o at 6.25 MHz and 9.375 MHz respectively are used for the simulation. The results at the corresponding *UP* and *DOWN* outputs are shown in figure 5.67. The charge pump is simulated by setting the *UP* and *DOWN* signals as ± 1.35 V (200 Hz) square waves. The results obtained at the output of the charge pump are shown in figure 5.68.

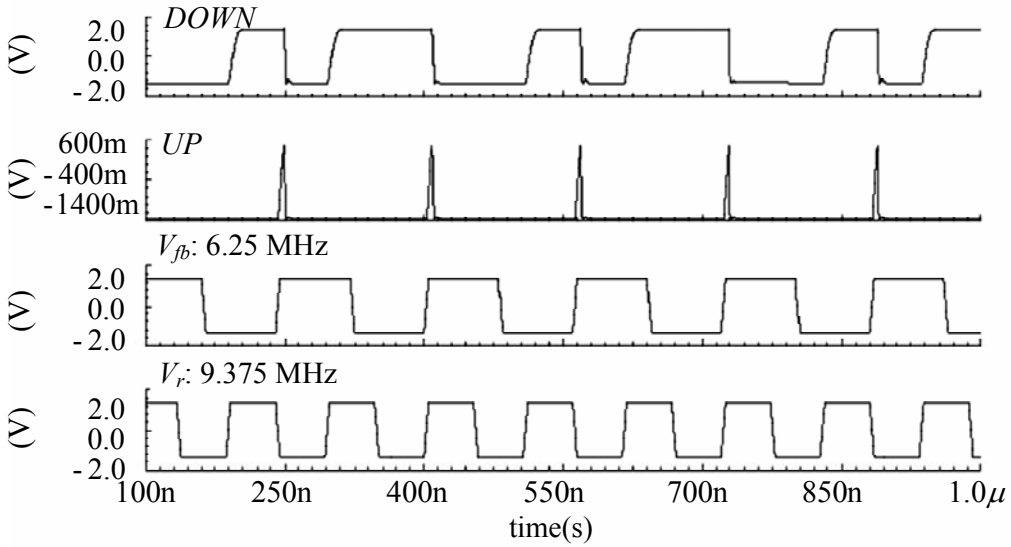


Figure 5.67. The figure shows the simulation results from the PFD of figure 5.1.

A rising edge on the V_r signal causes the *DOWN* signal to go high first. The *DOWN* signal stays high until a rising edge of V_o causes *UP* to go high. *UP* and *DOWN* are now both high for a short period. This causes the AND gate reset output to go high and force *UP* and *DOWN* low. This cycle is repeated with another rising edge of V_r. The overall effect of this is that with a significantly faster V_r signal the *DOWN* signal is high for a significant period of time. This will force the charge pump to discharge the loop filter and the VCO control voltage will drop. This will increase the VCO output's frequency and in turn the V_r signal's frequency. The simulation of the *UP* and *DOWN* signals are ±1.35V 200 Hz square waves. *UP* and *DOWN* are logic complements. A 10 nF capacitor loads the output of the charge pump. The charge pump positively charges the load capacitor with I_{UP} when *UP* is high and negatively charges the load capacitor with I_{DOWN} when *DOWN* is high. The output current will vary slightly with the output voltage level due to channel length modulation effects. The average output current is measured from the voltage slope over the ±0.8 V region of interest for the multi-band PLL system. When *UP* is high the charge

pump sources 24 µA of current into the loop filter. The charge pump sinks –25 µA of current from the loop filter when *DOWN* is high.

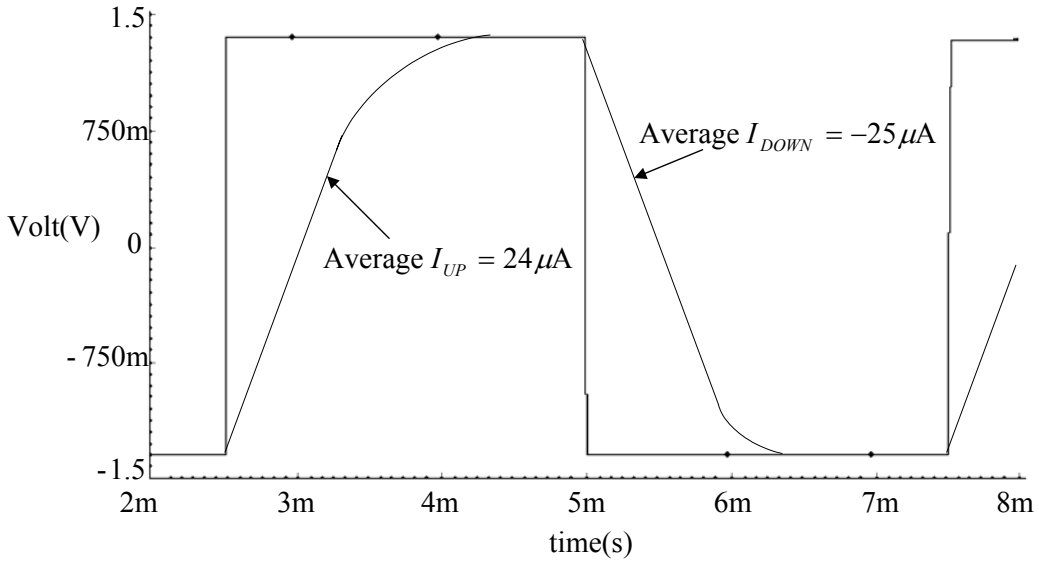


Figure 5.68. The figure shows the simulation result of the charge pump shown as part of figure 5.1.

5.4.1.2 Digital subsystem 2: Fixed frequency dividers (÷ X and ÷ N)

Figure 5.15 shows the fixed divider configuration. The system was verified by individually simulating each of the divider for an arbitrary high frequency input. Simulation results for the divide-by-4 configuration of figure 5.18, divide-by-2 configuration of figure 5.19 are shown in figure 5.69 and 5.70 respectively.

It is clear from the frequency spectrum that the high frequency division function on the square wave for both the counters is operational. However, certain noise components are also present. These can be cancelled by using differential outputs instead of single ended output. A basic differential to single ended converter [31] is used for this purpose. This schematic is incorporated as part of the hierarchical blocks shown in figure 5.66.

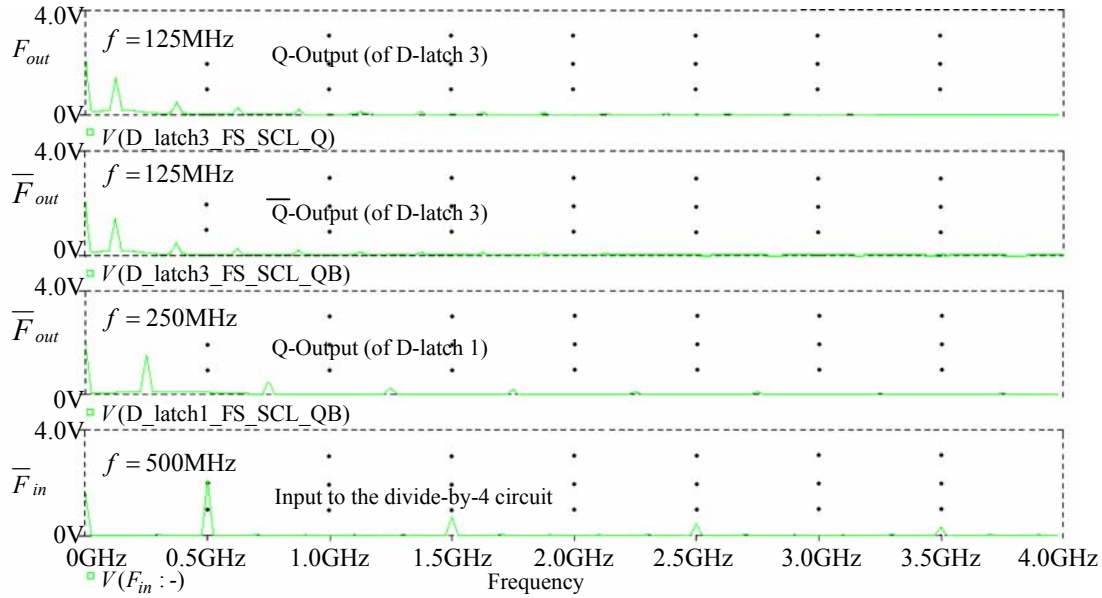


Figure 5.69. The frequency sweep performed on the divide-by-4 circuit of figure 5.18. This configuration is used as the ÷X counter as well as part of the ÷N counter as shown in figure 5.15.

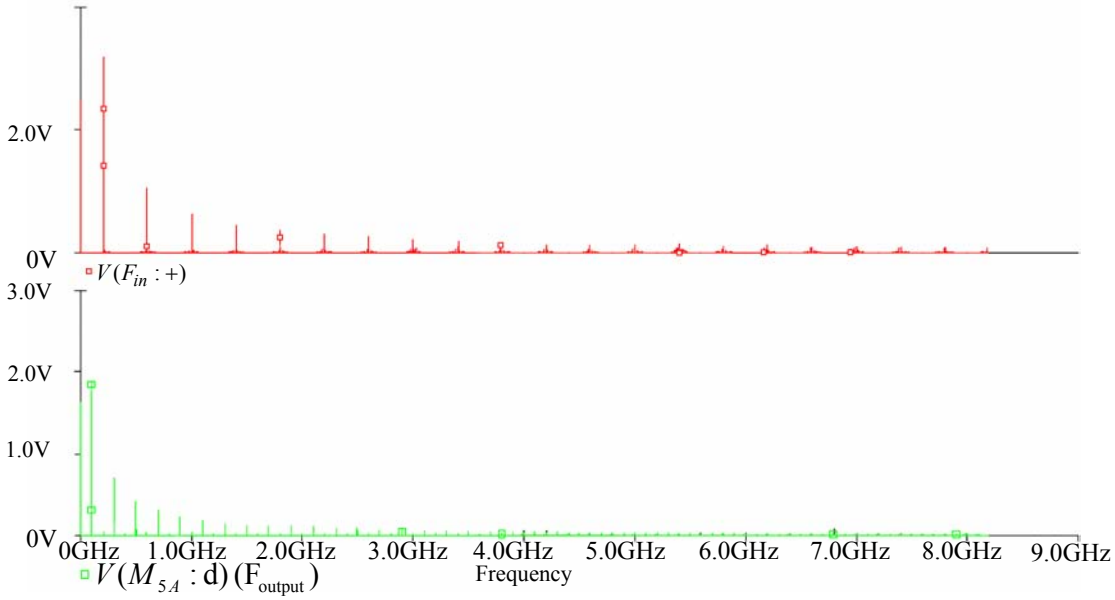


Figure 5.70. The figure shows the frequency sweep performed on the divide-by-2 circuit of figure 5.19. This configuration is used as part of the ÷N counter as shown in figure 5.15.

5.4.1.3 Digital subsystem 3: Programmable counter

The basic configuration used is shown in figure 5.71 (more detailed version of figure 5.20). Simulations were carried out for a range of settings. Firstly the *S*-input was set to 15 (all inputs set to high). Thereafter, *P* was varied from 0 to 127, by changing the input settings shown on figure 5.71. The frequency spectrum for $P = 64$ is shown in figure 5.72.

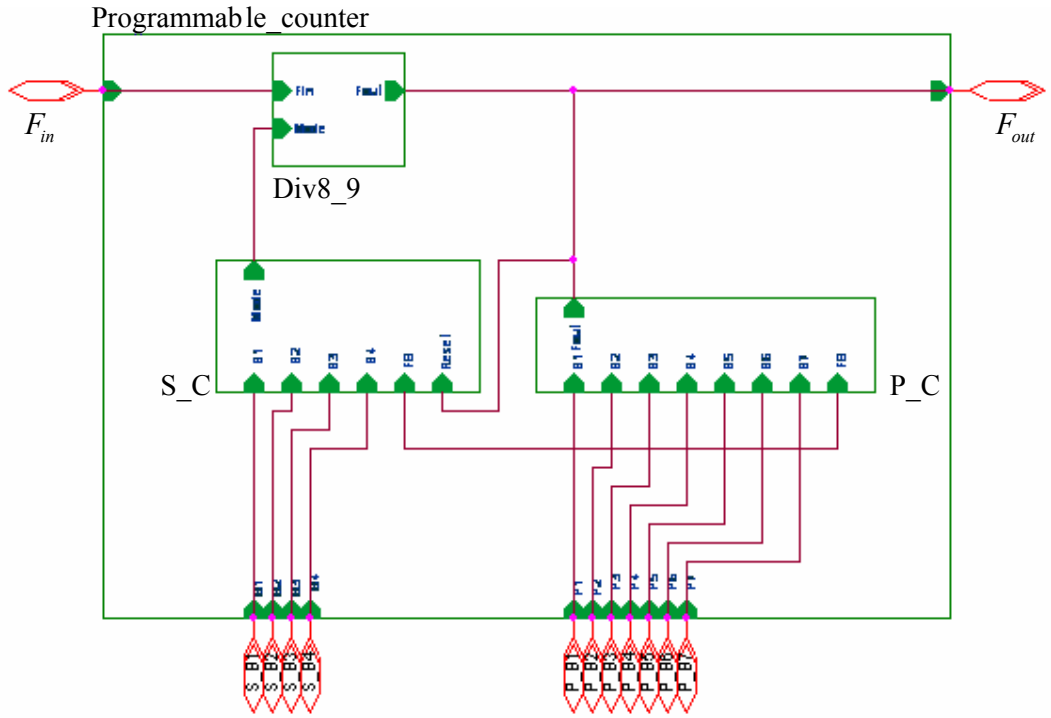
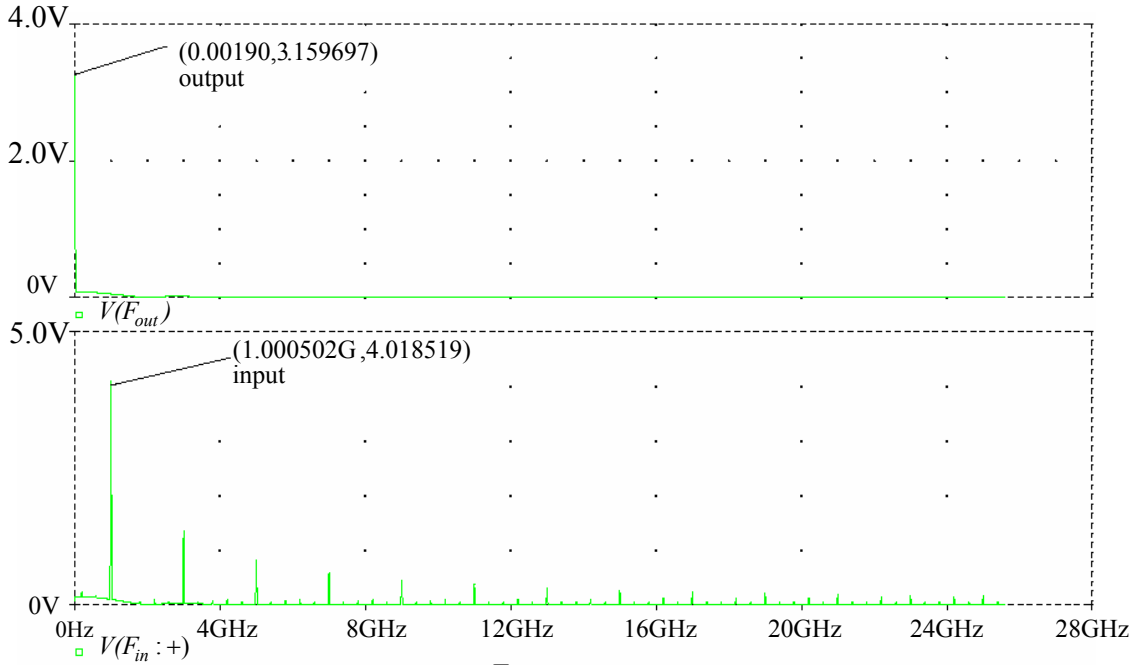


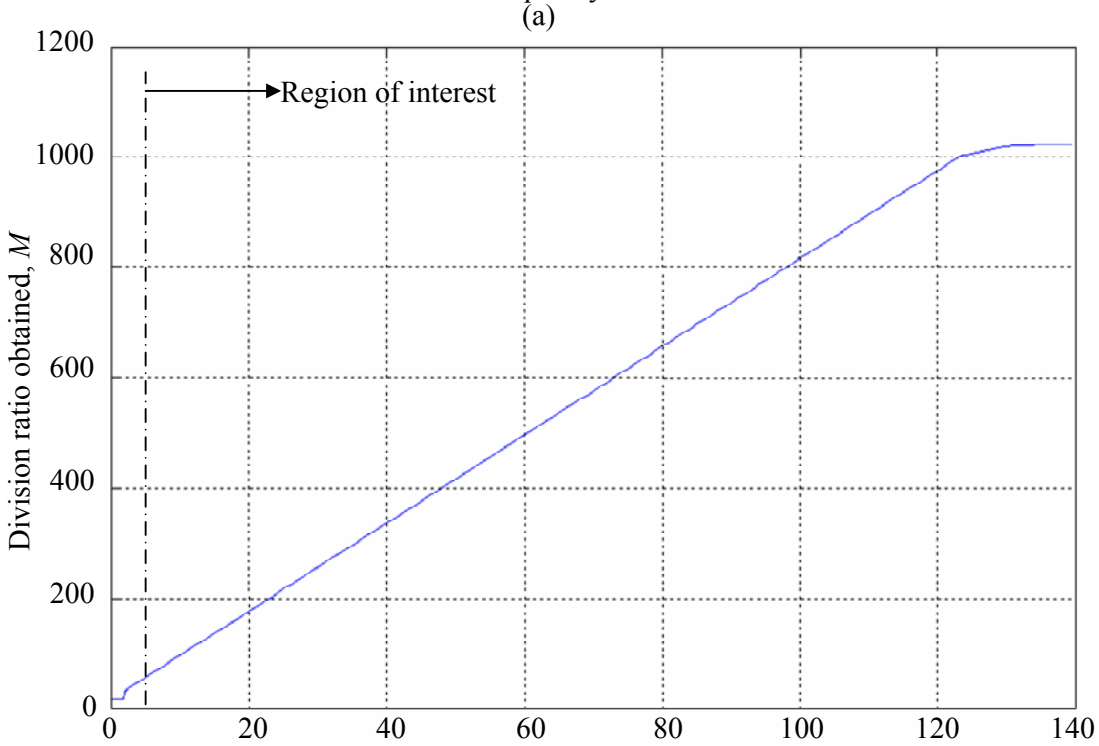
Figure 5.71. The figure shows the complete programmable counter. The figure is represented in terms of hierarchical blocks. During simulation, S-Edit descends down the hierarchy to transistor level simulations.

The input P was varied from 0 to 127. This is graphically shown in figure 5.72 (b). The "saturation" effect after $P > 127$ is attributed to simulation software errors, as the counter P has only 7-bit inputs, it cannot be to a division ratio, $M > 1031$. It was further seen that for $P < S$, i.e. $P < 15$, the counter cannot function. This result agrees with the inconsistent division problem [5]. Hence, the input P is limited between 15 and 127.

A typical programmable counter can fail at high frequencies due to delays in the signal path [6]. Optimizing the drive ratios of stages (blocks shown in figure 5.71) one through three can alleviate this problem. Furthermore, it is also discussed that the circuit can fail at low frequencies due to the discharge of the stages' output nodes. Increasing the output resistance of the stages alleviates this problem. However, as the frequency input into the programmable counter is from the ring oscillator with frequency range from 400 MHz to 800 MHz, it is seen that the programmable counter can operate in this range, and hence no further changes (in terms of transistor ratios) to that included in figure 5.71 is required.



(a)



(b)

Figure 5.72. The figure shows (a) the frequency domain simulation results performed on the programmable counter of figure 5.71, and
(b) the obtained division ratio, *M* as a function of the variable input, *P* to the programmable counter.

5.4.1.4 Analogue subsystems 4 & 5: LC VCO & ring oscillator

Figure 5.48 verifies the frequency and output voltage of the LC VCO. Figure 5.73 shows the verification that the required (by the SSB mixer) phases are indeed achievable. The results of the ring oscillator are provided in figure 5.59.

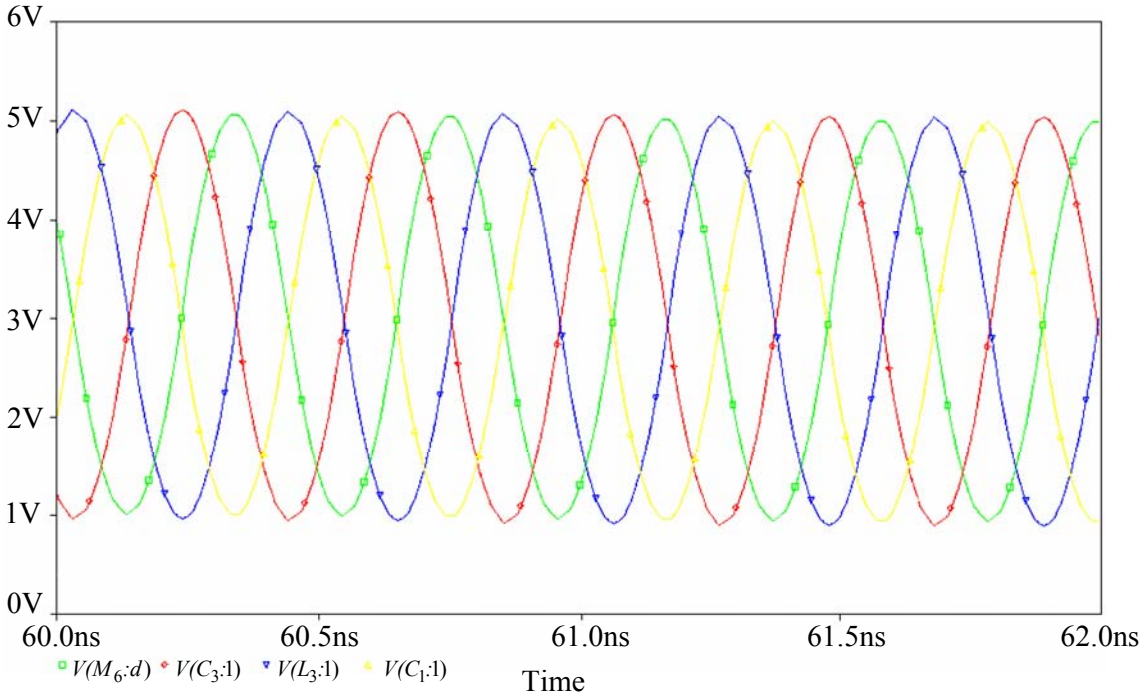
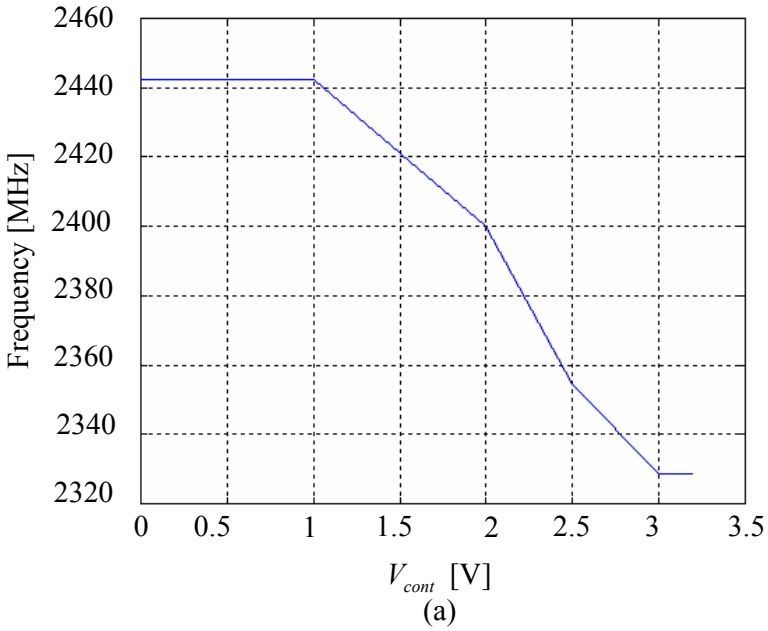
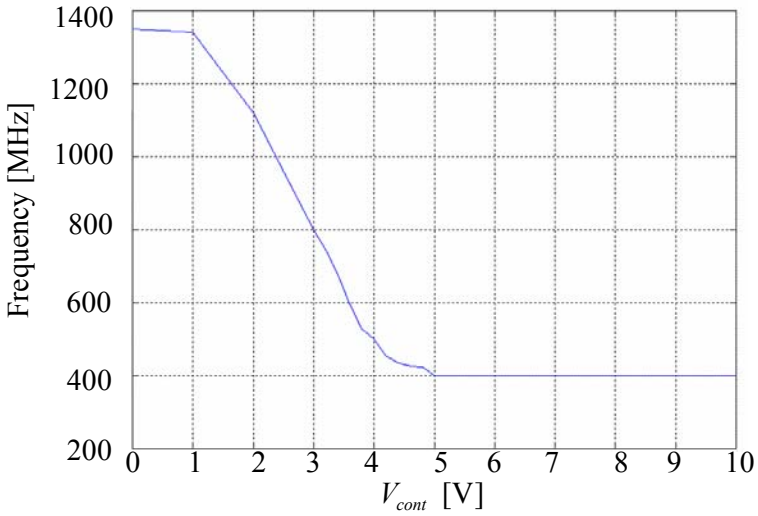


Figure 5.73. The figure shows the time domain simulation results from the LC oscillator.

A simple design modification (of connecting the bias current sources of the two oscillators), virtually at no cost, to the quadrature coupled LC oscillators has been used in figure 5.38. As seen from the simulation results of figure 5.73 and figure 5.48, this modification indeed provides an automatic amplitude-matching control which is not available in the original design and enhances significantly the quadrature-phase control [29]. With such a control, better amplitude and phase matchings can be obtained even in the presence of a large mismatch of the LC tanks. The tolerance of the LC tanks mismatches for a stable single frequency oscillation is much increased. Better phase noise is also expected due to the increase in amplitude and a more solid ac ground for the common source. The LC VCO transfer characteristic is shown in figure 5.74 (a). This was obtained by doing a DC voltage sweep on the extracted netlist from the LC oscillator layout. Simulation results (figure 5.59) show that the topology [11] for a high-speed ring oscillator is indeed suitable for multiphase signal generation. Parametric voltage sweep on the ring oscillator was used to achieve the VCO transfer characteristic (figure 5.74 (b)).



(a)



(b)

Figure 5.74. The figure shows the LC VCO transfer characteristic. An average gradient (for V_{cont} < 3.3 V) is accepted as the VCO gain. This value is approximately -55 MHz/V. (b) The figure shows the ring VCO transfer characteristic. An average gradient (for V_{cont} < 3.3 V) is accepted as the VCO gain. This value is approximately –196 MHz/V.

5.4.1.5 Analogue subsystem 6: SSB Mixer

The SSB mixer is tested by using two square signals (with amplitudes in the same range as that generated by the oscillators of section 5.2.1.2 and section 5.2.1.3 and input frequencies of the two square waves 200 MHz (LO inputs) and 2.3 GHz (IF inputs)). The basic circuit is shown in figure 5.63. For simulation purposes, the in- and quadrature-phases were

generated simply by using ideal sources. In practice, these inputs are from the VCOs. The resulting output is shown in figure 5.75.

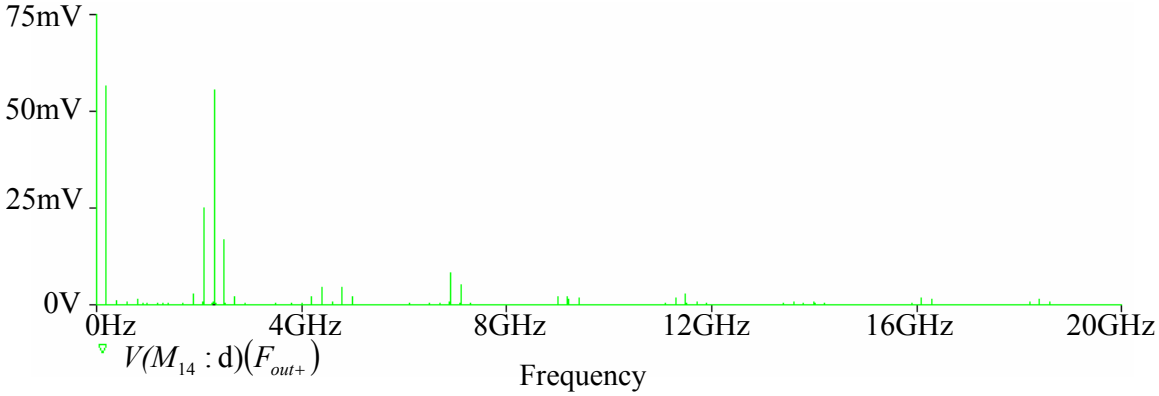


Figure 5.75. The figure shows typical frequency output obtained from the SSB mixer.

Simulation results indicate that the difference frequency term of the two input signals is obtained. This is consistent with the basic requirement for the SSB mixer as indicated in section 4.4. A differential-to-single-ended converter [31] is further used to cancel possible noise components.

5.4.1.6 Analogue subsystems 7 & 8: Loop filters

The basic loop filter circuit is shown in figure 5.64. A frequency sweep was performed, the corresponding bode plots (for the passive element values indicated in table 5.1) are shown in figure 5.76.

Simulation results show that the required filter bandwidths (indicated in table 5.1) are obtained. The loop filter involves a trade off between the reference sidebands and settling time [5]. This trade off differs from application to application. For full-chip synthesizer simulation, this loop filter is used. However, an option will be available to the user to either use the on-chip loop filter (by merely providing a short circuit to the loop filter designed) or an off-chip loop filter using external components [5]. The bandwidth of the loops is designed to be a tenth of the reference frequency for both stability and fast locking [1].

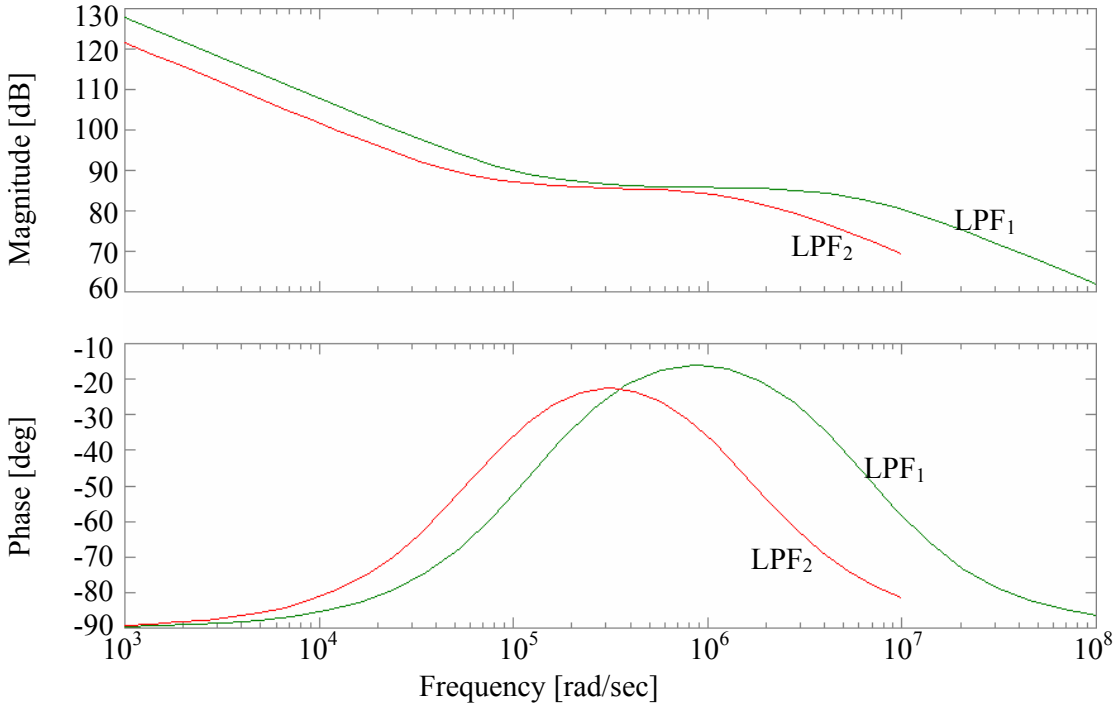


Figure 5.76.The figure shows the Bode magnitude plot for the two loop filters used in the system.

5.4.2 Overall results & Verification

The complete CMOS implementation of this dissertation is shown in figure 5.66. The relevant frequency domain results are shown in figure 5.77.

To determine the synthesizer switching time, the complete synthesizer in figure 5.66 was used. Timed (ideal) programming of the programmable counter setup was used; this was done by inverting the lowest-bit input on the *P* counter. The necessary time domain simulation required to determine the switching time is shown in figure 5.78.

From these simulations (and the earlier mathematical derivations of this chapter), it is shown that the implementation of this dissertation can be used in radios that utilize spread spectrum, frequency hopping, and full-duplex signal at up to 1600 hops/sec. The signal hops among 79 frequencies (2.402 - 2.480 GHz band) at 1 MHz intervals to give a high degree of interference immunity.

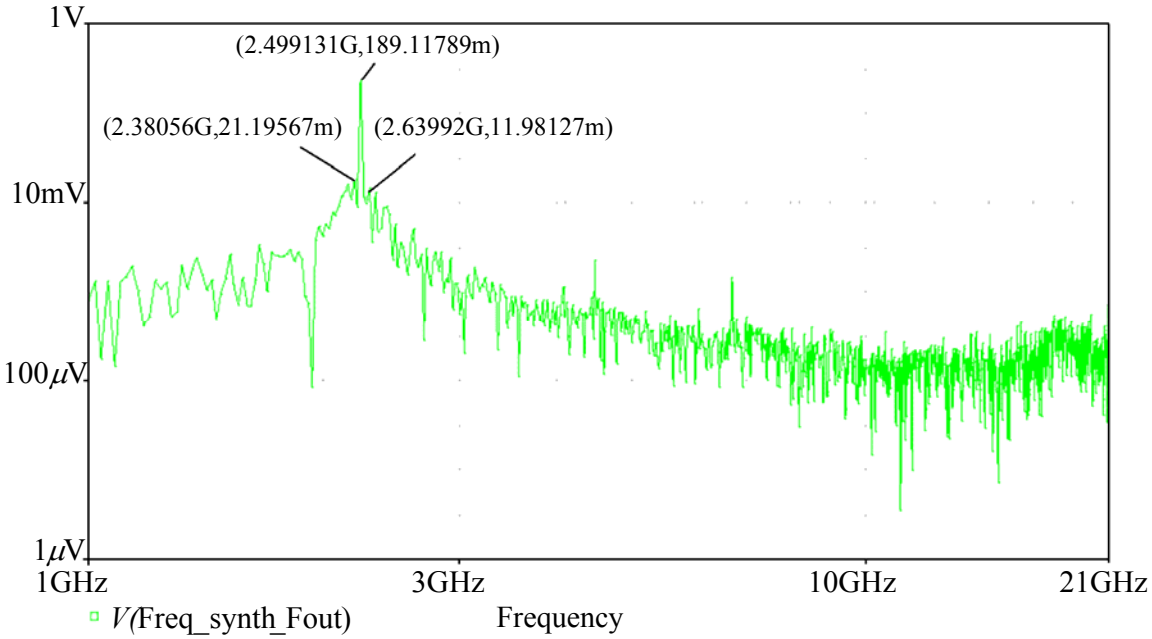


Figure 5.77. The figure shows the frequency domain results of the complete frequency synthesizer.

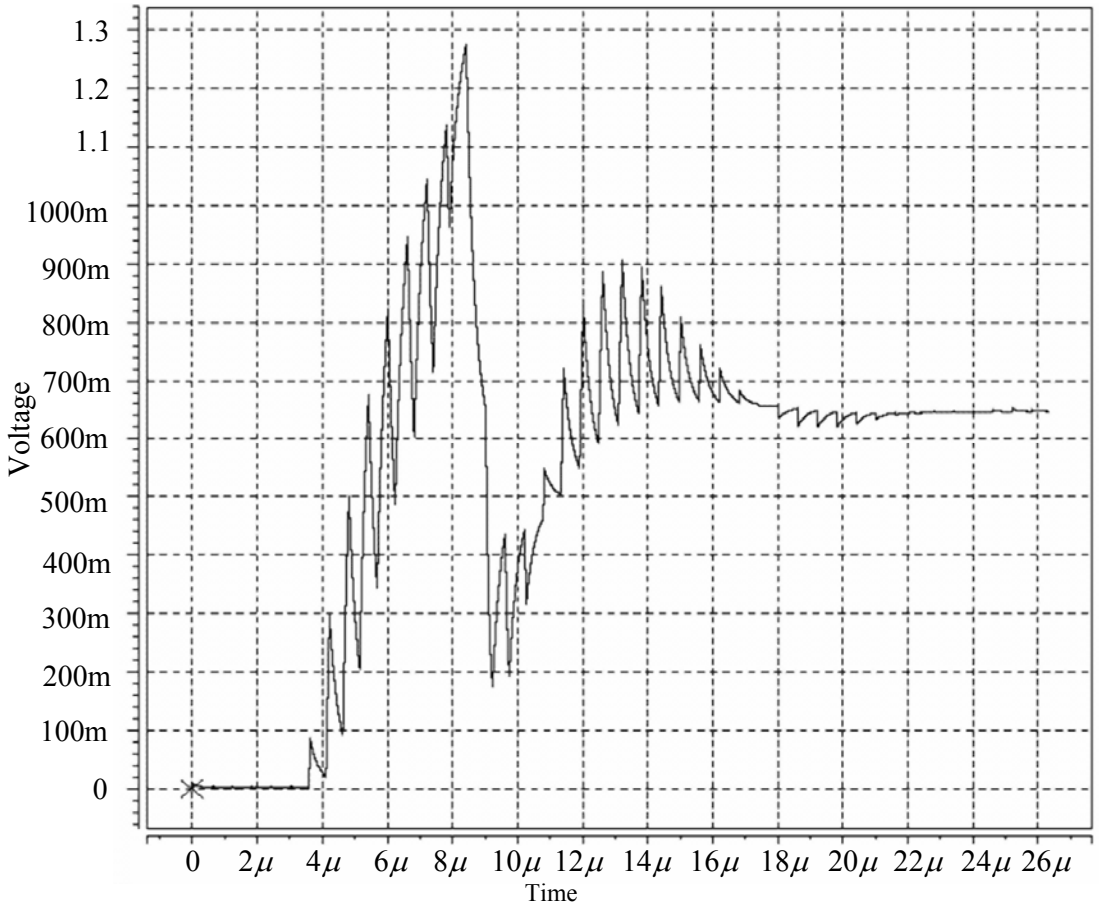


Figure 5.78. The figure shows the necessary time domain simulation to determine the switching time of the PLL frequency synthesizer.

Other specifications that have been achieved for this synthesizer are listed below.

• Phase noise: The noise originating in the VCO (oscillator noise) dominates for frequencies greater than the oscillator frequency (i.e. $\omega > \omega_c$), [5]:

$$S_{\phi_o} \approx S_{\phi}(\omega) \tag{5.64}$$

The oscillator phase noise is computed by [5].

$$\text{Relative phase noise} = \frac{1}{4Q^2}\left(\frac{\Delta\omega}{\omega_o}\right)^2 \frac{P_{noise}}{P_{carrier}} \tag{5.65}$$

Using equation (5.65), and SPICE output file, the total phase noise of the system is obtained to be about –84 dBc/Hz at an offset of 1000 kHz.

• Spurious frequency components: As seen in figure 5.77, the spurious frequencies can be located at about 5 GHz. It is clear that the spurious frequencies (side bands) are about 50 dB below the main carrier frequency. This can be improved by compensating the settling time of the system (or by using an off-chip external loop filter) as discussed earlier.

CHAPTER 6: INDUCTOR DESIGN

6.1 Introduction

The rapid growth of the wireless communication market has fuelled the demand for low-cost radio systems on a chip. Traditionally, radio systems are implemented on the broad level using a large number of discrete components. Silicon (Si) integrated circuit technology has progressed to offer device performance suitable for analogue operations up to several gigahertz and, thus, presents the potential for integrating radios on a chip. At the same time, a great deal of effort has been devoted to on-chip inductors as they are used extensively in radio frequency circuits.

Typical applications may include low loss inductors for input matching of low noise amplifiers (LNAs), inductively loaded pre-amplifiers, output matching networks for high efficiency switch-mode power amplifiers, and high quality (Q) factor tank circuits for low phase noise.

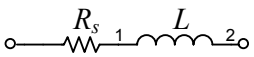


Figure 6.1. The figure shows a simplified model of an inductor.

Designs include higher conductivity metal layers to reduce the loss resistance, R_s (depicted in figure 6.1) of the inductor. The use of multi-metal layers increases the effective thickness of the spiral inductor and, thereby, reduces the loss. The connection of multi-metal layer spirals in series to reduce the area of the inductors, the low-loss substrates to reduce losses in the substrate at high frequency, and thick oxide or floating inductors to isolate the inductor from the lossy substrate.

The use of spiral inductors in Si IC was first reported by [31]. Since then, extensive research work has been published on modelling inductors [32-34] and on techniques to improve the Q [33-38]. For typical inductance ranging from 1 to 20 nH, conventional Si technologies can deliver Q's of about 5. Although on-chip inductors have Q's significantly lower than their discrete counterparts (typical Q's of about 50), they have been proven to be useful and essential in highly integrated RF systems [39 & 40]. In order to identify the

optimal inductor layouts and account for the inductors and their parasitic in circuit simulation, an accurate equivalent circuit model is necessary [41].

The following is a listing of motivation for the integration of inductors.

- Currently only hybrid circuits based on off-chip discrete inductors have sufficient performance for wireless applications.
- Integration of passive inductors onto a substrate that contains RF circuitry is desirable.
- If the passive inductors can be monolithically integrated with the same performance as hybrid components, it is possible to:
    - shrink the overall size,
    - decrease the packaging complexity,
    - give more flexibility in wireless transceiver system design, and
    - lower the total system cost.

Inductors may also be actively integrated. Various configurations have been developed to achieve this. One such configuration that has gained prominence is the generalized impedance converter (GIC), which can be used not only to simulate inductances, but also to synthesize frequency dependent resistances. The motivation for implementing active inductors is the increased tuneability, plus reduced chip area and processing cost, compared to on-chip passive inductor architectures.

This chapter deals with the investigation, modelling, design and simulation of integrated inductors for RF circuits that operate at the technology limits of Si CMOS. The development of such elements is an important step towards the realisation of the fully integrated (and ultimately single-chip) frequency synthesizer.

6.2 Typical inductor model

The spirals that are discussed in this chapter include single and multi-layered inductors. The simple case of a one-layer spiral is discussed first. A section view of a simple IC is shown in figure 6.2. The substrate, which is at the bottom (typically a few hundred microns), above which there may be an epi-layer of few microns thickness, depending on the process. The first layer of metal on which the inductor is made is separated from the epi-layer by an insulator. The insulator is usually silicon dioxide, SiO_2 with a relative

permittivity of 3.9. The figure also shows the capacitance from the turn to the epi-layer. The resistances represent the different paths that the current can flow.

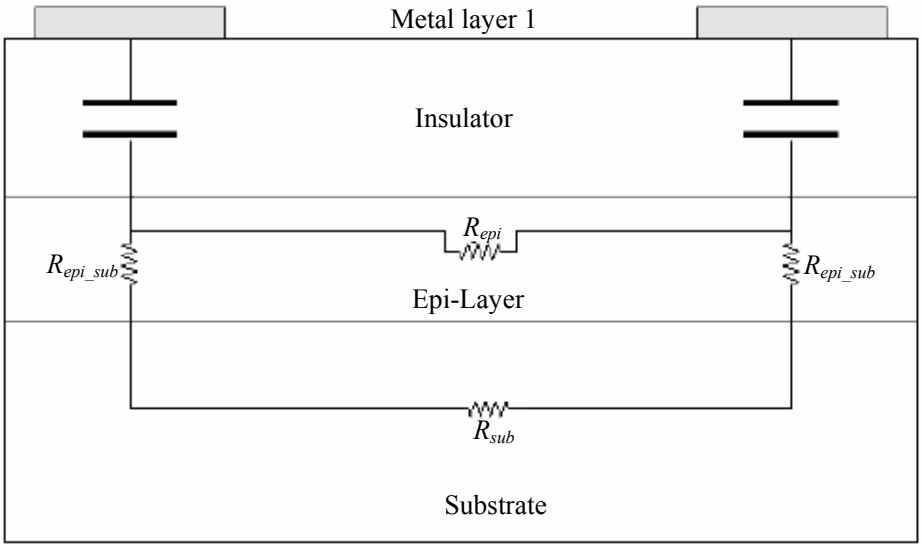


Figure 6.2. The figure shows simplified model of an IC showing the different resistances along with the turns-to-substrate capacitance, [43].

A series inductance and resistance represent the spiral for a turn. As the different turns are close to each other there is a mutual inductance between the turns. The mutual inductance and the coupling coefficients between the different self-inductances are calculated by finding the magnetic field inside the spiral. As shown in the figure 6.2, there is a capacitance that is associated from the traces of the spiral to the substrate. This is incorporated in the model, by calculating the capacitance from the trace to the substrate for half the turn and putting it on either side of it. The bottom plates of the capacitances are connected through the substrate by a resistance, R_{sub}. If there is an epi-layer, as in case of figure 6.2, there is also an epi-layer resistance that comes in parallel with the substrate resistance. The value of all these parameters can be calculated using basic device physics.

The simple model for a single turn of a spiral is shown in figure 6.3. Unfortunately, for a multi-turn and multi-layered spiral the model is not as simple (and further complicated when the different loss mechanisms are accounted for). The latter part of this section is devoted to the detailed modelled of a multi-turn and multi-layered spiral with the different loss mechanisms included.

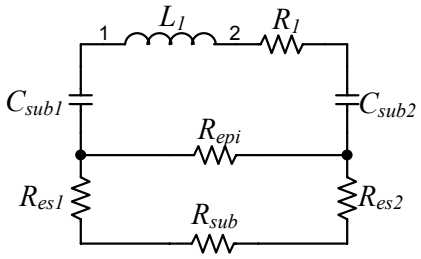


Figure 6.3. The figure shows a simple model for a turn showing the different passive components.

6.2.1 Model schematics and calculation of parameters

This sub-section explains the calculation of the different parameters mentioned in the previous section by considering a three-turn, 2-layered spiral inductor. Several modelling techniques are available [44], this chapter uses the finite element approach, which breaks up the spiral into individual turns. Several sections of this chapter are taken from [43].

The outer dimension is rounded to the closest multiple of the pitch of the spiral. The turns are assumed to have equal length on each side and this makes the calculations much simpler without compromising the results. Figure 6.4 illustrates the top view of three-turn spiral with the different parameters. The turns are separated into individual turns for calculations.

Figure 6.5 shows the perspective view of a three-turn, two-layer spiral with the two connection points represented as X and Y. The spiral is shown as spiraling in on the top layer and spiraling out on the bottom layer. The interconnection, shown by dotted lines, is made between the two layers using vias. Currently, in the model, the via resistance is not taken into account and is replaced by a perfect conductor. This is a reasonable approximation for most of the spirals as the total trace length is much greater than the via length.

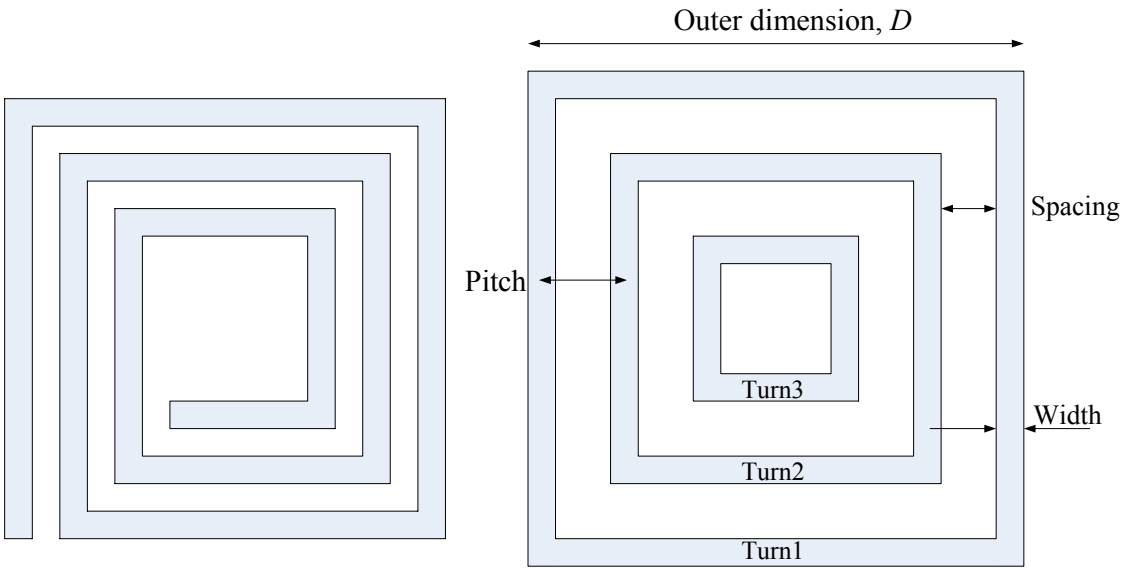


Figure 6.4. The figure illustrates the top view of a three-turn spiral showing some of the different parameters along with the closed turn approximation [45].

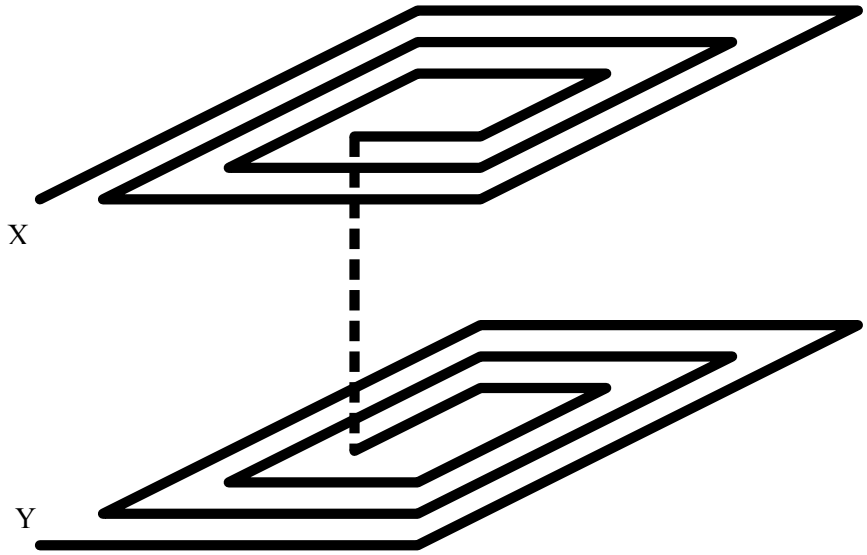


Figure 6.5. The figure illustrates the perspective view for a three turn two-layer spiral with via connection shown in dotted lines, [43].

A detailed model of the three turns, two layers spiral is shown in figure 6.6. All the different coupling coefficients (K_i) have not been shown, but have been discussed in the following subsections.

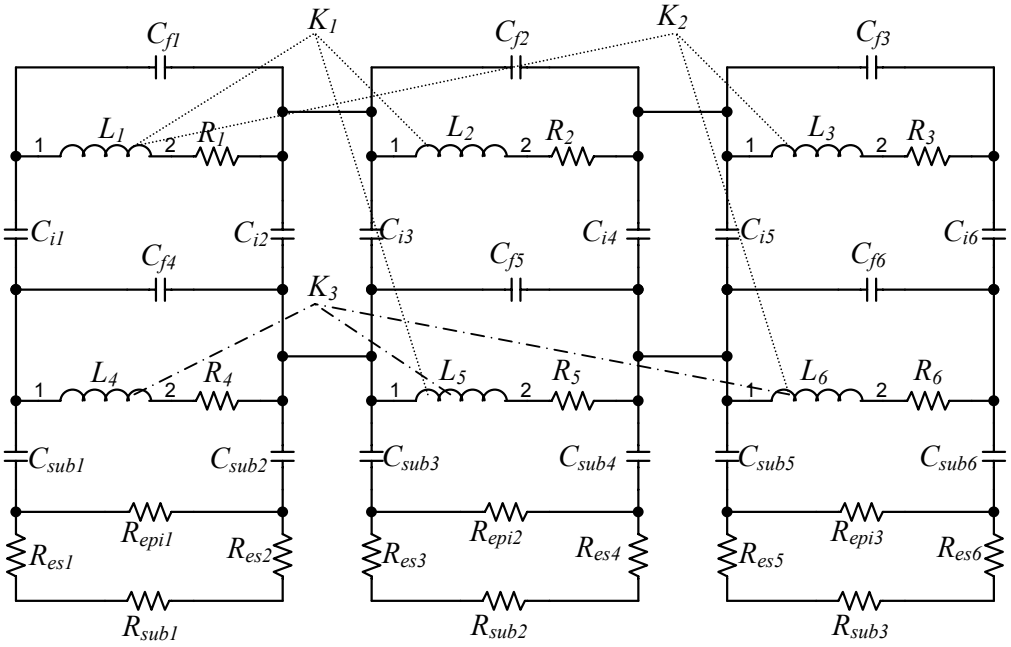


Figure 6.6. The figure shows a lumped model showing a two-layer, three turn spiral without a ground shield (all the coupling coefficients are not shown). The interlayer capacitance is also modelled and shown between the traces on the different layers as well as the sidewall capacitance between the traces of the same layer.

6.2.1.1 Series resistance

A series inductor and resistance are used to represent each turn in a layer. The value of series resistance is calculated using the metal sheet resistance, R_{sheet} of the layer and the size of the turn as

$$R = \frac{4LR_{sheet}}{W}, \tag{6.1}$$

where L is the length of each side of the turn, W is the width of the trace and R_{sheet} is the sheet resistance of the metal layer used. From figure 6.6, it can be observed that the different series resistances are R_1, R_2, R_3, R_4, R_5 and R_6. The resistances R_1, R_4 and R_3 represent the outermost turns, and R_6 represent the innermost turn. Using equation (6.1) it can be estimated that resistances decrease from R_1 to R_3 and R_4 to R_6.

6.2.1.2 Epi resistance

In typical IC processes there is a thin epi-layer on top of the substrate as shown in figure 6.2. This resistance is modelled as connecting between the bottom plates of the turns-to-

substrate capacitance. In many processes it may not be significant, but has been generically modelled. This epi resistance is calculated from

$$R_{\text{epi}} = \frac{\rho_{epi} L}{Epi_{thick} W}, \tag{6.2}$$

where the L is the spacing between the turns, W is the total length of the turn, Epi_{thick} is the epi-layer thickness and ρ_{epi} is the epi-layer resistivity.

6.2.1.3 Epi-substrate resistance

From figure 6.2, it can be observed that there is a resistance connecting the epi-layer to the substrate on both sides of the turn. It is usually very small compared to the substrate resistance but becomes significant in the case of very low resistivity substrates. It is calculated based on the thickness of the epi-layer and the area of the particular turn. R_{episub} can be computed from

$$R_{\text{epi}} = \frac{\rho_{epi} L}{A}, \tag{6.3}$$

where L is the epi-layer thickness, A is the area of the turn which is the product of width and length the turn, and ρ_{epi} is the epi-layer resistivity.

6.2.1.4 Substrate resistance

The substrate resistivity of most processes (for example AMS, [46]) lies between 0.02 – 20 Ω.cm and this contributes to substrate losses coupled through the turn-to-substrate capacitances. The substrate resistance, R_{sub} is modelled as connected between the ends of the turns [47] and computed by

$$R_{sub} = \frac{3\rho_{sub}}{8D}, \tag{6.4}$$

where ρ_{sub} is the resistivity of the substrate and D is the outer dimension of the turn (as shown in figure 6.4.)

6.2.1.5 Turn-to-substrate capacitance

There is a capacitance associated with each turn of the lowest metal layer to the substrate as shown in figure 6.6 and this is represented by C_{sub}. This capacitance can be visualized with the traces forming a parallel plate with the substrate and a layer of insulator separating

them. This capacitance can be calculated using the standard formula for a parallel plate capacitance

$$C_{sub} = \varepsilon_o \varepsilon_r \frac{wl}{d}, \tag{6.5}$$

where ε_o is the permittivity of free space, and ε_r is the relative permittivity of the insulator, l is the length, w is the width of the trace, and d is the distance of separation between the lowest layer to the epi-layer. In the case of absence of epi-layer, it is the distance to the substrate. This capacitance C_{sub} is split as $½C_{sub}$ and connected on each side of the turn for symmetry. The capacitance $½C_{sub}$ is the capacitance for half the turn.

6.2.1.6 Sidewall capacitance

There is a sidewall capacitance associated between adjacent turns on a layer. This is modelled only in terms of the sidewalls of the metal layers. The fringe effects of the sidewall capacitance have not been modelled. The capacitance can, again, be calculated using equation (6.5), where l is the length of each turn, w is the thickness of the metal layer, and d being the separation between the turns. In the case of innermost turns, there is no sidewall capacitance that can be represented in this model.

6.2.1.7 Interlayer capacitance

In the case of multi-layered spirals, the turns are broken down into individual turns on each layer. The lowest layer is modelled as explained above with the higher layers being connected to the next lower layer by the inter layer capacitances. The interlayer capacitance is calculated using equation (6.5), where l is the length of turn, w is the width of the trace, and d is the separation between the individual layers by the dielectric.

6.2.1.8 Turn inductances

The calculation of the inductances is more complicated than resistances. As mentioned earlier, there are a number of methods available to calculate it. In this chapter, a finite element based computation of the B field is used to calculate the inductance. This is discussed in section 6.4.

6.2.2 Pattern ground shield (PGS)

In the case of medium resistivity substrates, the displacement current coupled through the capacitance is a major factor degrading the Q of the spiral. To overcome this effect, a PGS is often used [36]. It essentially cuts down the losses, through capacitive coupling to the substrate, by putting a very low resistance path given by the sheet resistance (shown in figure 6.7) of the shield, R_s. The shield is patterned so that no eddy loops are generated in the ground plane. However, the PGS does not prevent the magnetic field from passing through the substrate, hence creating eddy current losses [47].

6.2.3 Complete model schematic

A typical case of two-layered, six-turn inductor is shown in figure 6.7 elaborating the different connections. As in the case of two-layered spirals, the inductor spirals in on the top layer and spirals out in the lower layer. In the case of more than two layers, the spiral alternates between spiralling in and out. It is seen in figure 6.7, the end of resistor R_3 is connected to resistor, R_6, with the polarities of the inductor adjusted. The two ends of the inductor would be ends of L_1 and L_4. The inductance of the spiral increases as factor of n^2, where n is the number of layers. However, it suffers from low self-resonant frequency, due to interlayer capacitances.

6.3 Optimal design procedures

As square spiral inductors are the most common in Si RF ICs. The target of this section will be achieved by designing a 10 nH (as discussed in section 5.2.1.2.7) square spiral inductor with a high Q. The solution is to find the number of turns and all dimensions of the square spiral inductor.

The inductance of a planar spiral square inductor can be calculated according to the Greenhouse theory. Basically, the spiral square inductor is split up into sections consisting of straight conductors, and the self-inductance of the sections is calculated and summed up. Beside the consideration of the self-inductance of each straight conductor, the mutual inductance (positive or negative) between parallel segments needs to be included for the calculation of the overall inductance. A simpler model to the one presented in the previous section will also be developed for design purposes.

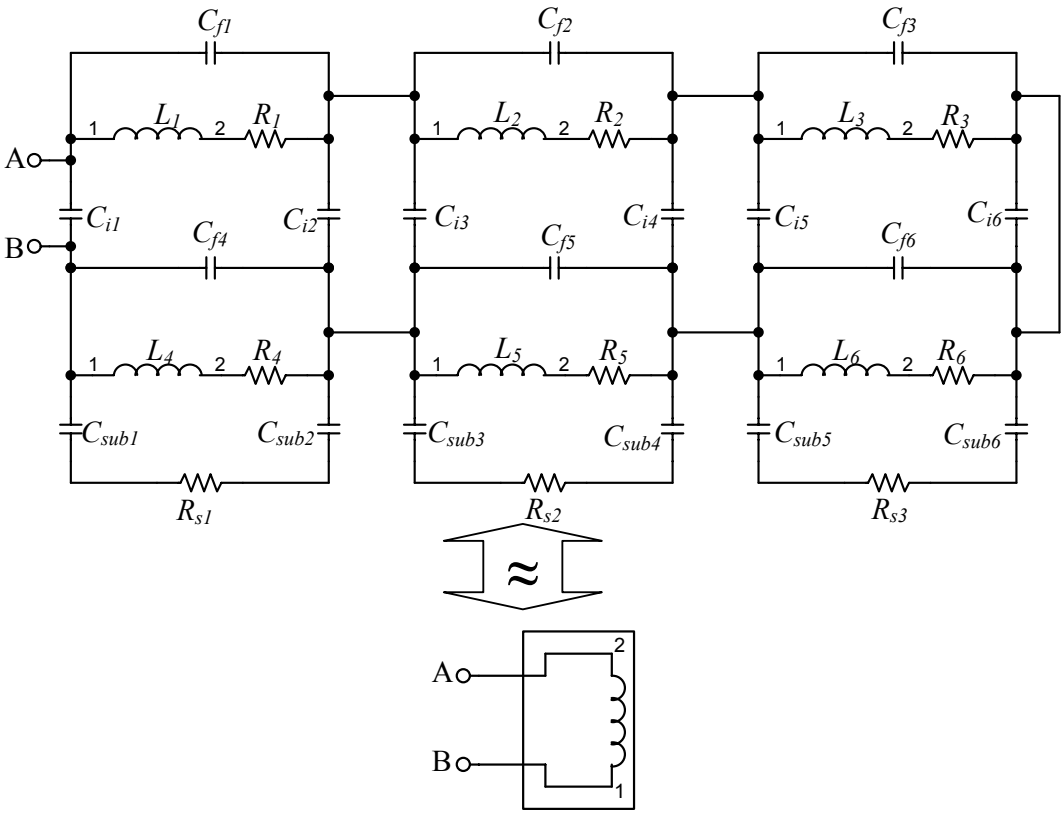


Figure 6.7. The figure shows an approximately complete model schematic for a six turn, two-layer inductor. The figure is an adaptation from figure 6.6 shown earlier.

6.3.1.1 Self inductance

The self-inductance for a straight conductor is approximately computed by [31]

$$L = 0.0021\left[\ln\left(\frac{2l}{GMD}\right) - 1.25 + \frac{AMD}{l} + \left(\frac{\mu}{4}T\right)\right], \qquad (6.6)$$

where L is the self-inductance in μH, l is the conductor length in cm, GMD and AMD represent the geometric and arithmetic mean distance, respectively, of the conductor cross section, μ is the conductor permeability, and T is the frequency correction parameter.

The GMD between two conductors is the distance between two infinitely thin imaginary filaments whose mutual inductance is equal to the mutual inductance between the two original conductors as shown in figure 6.8. The GMD is equal to 0.44705 times a side in the case of a square cross section.

The AMD is the average of all the distances between the points of one conductor and the points of another. For a single conductor, the AMD is the average of all possible distances within the cross section.

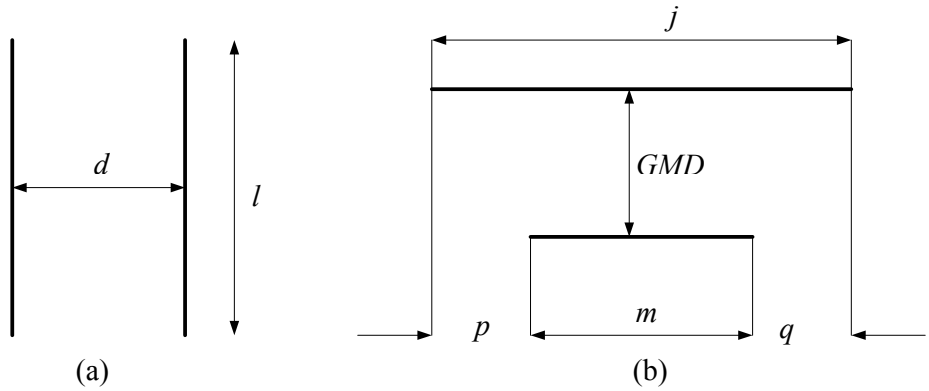


Figure 6.8. The figure shows (a) the layout of the current filaments, and (b) a two parallel-filament geometry to show the GMD.

If the top layer of metal is used for the layout of the spiral inductor, it can be considered as a thin-film inductor with rectangular cross section and equation (6.6) takes the form of equation (6.7) (The magnetic permeability, μ is 1, and the skin-depth phenomenon has little effect on thin film, T is approximately 1 for microwave frequencies.)

$$L = 0.0021\left[\ln\left(\frac{2l}{a+b}\right) - 0.50049 + \frac{a+b}{3l}\right], \qquad (6.7)$$

where a and b are the rectangular dimension of the cross section. This is shown in figure 6.9. This figure is described in more detail in the next sub-section.

6.3.1.2 Mutual inductance

In the case of an L-shaped thin-film inductor, the total inductance is equal to the sum of the self-inductance of the two straight segments, and less than the inductance of a single straight track of equal length. In the case of a rectangular or square planar coil, straight conductor segments are parallel to other straight conductor segments, and the mutual inductance between these parallel tracks contributes to the total inductance of the coil.

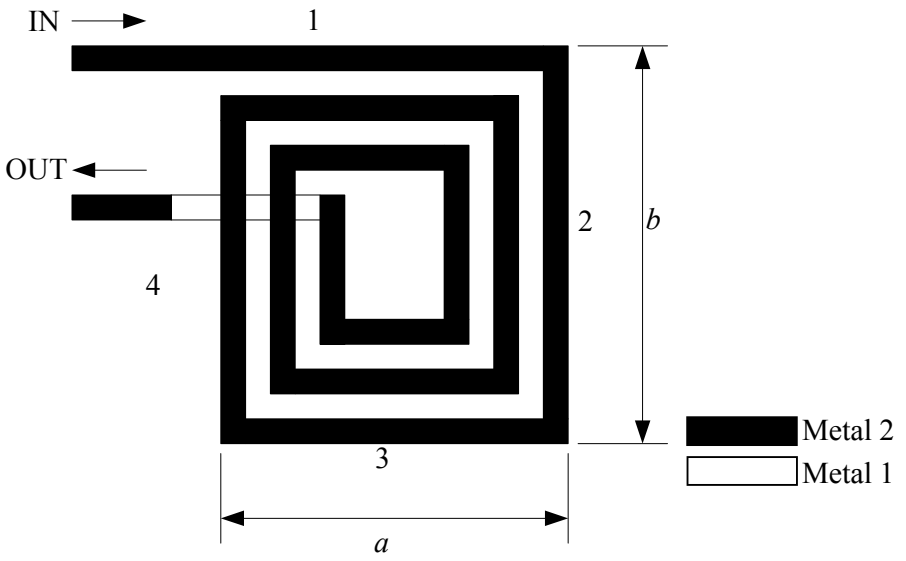


Figure 6.9. The figure shows the layout of a typical rectangular spiral inductor.

Value of T	Film thickness	Frequency (GHz)
0.9974	10000 Å	10
0.9986	0.0025 mm	1
0.9095	0.0075 mm	1

Table 6.1. The table shows the variation in frequency-correction parameter, *T* for thin films and microwave frequencies.

Figure 6.9 shows the top view of a 3-turn spiral inductor. For a typical process with two layers of metal, the top layer is used for forming the spiral inductor and the bottom layer for routing the inner turn outward. As the metal layer is separated from the substrate with an oxide layer, such that the top layer is used for the inductor layout hence increasing the oxide thickness from the ground, so that the substrate effect will be reduced thereby improving the self-resonant frequency. Further, the top layer has a thicker layer of metal, which helps to reduce both the dc and high frequency resistance so that inductor *Q* can be improved. The inductance of the spiral in figure 6.7 is equal to the sum of the self-inductance for each segment in the coil plus the mutual inductance, which are determined by the geometry and the phase relationship between the current carried by those lines. Figure 6.10 shows the model of two straight conductors carrying in-phase or out-of-phase current. There is a mutual inductance, *M* between the two conductors. For in-phase current such as the current in segment 1 and 5 of the inductor in figure 6.9, equations (6.8) and (6.9) govern the voltages and currents in the two conductors.

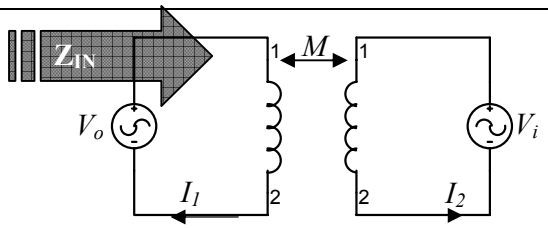


Figure 6.10. The figure shows a model of two conductors carrying in-phase and out-of-phase current.

$$V_o = I_1(j\omega L) + I_2\,(j\omega LM), \tag{6.8}$$

$$V_i = I_2(j\omega L) + I_1(j\omega LM), \tag{6.9}$$

For in phase current ($V_i = V_o$), it can be calculated that the impedance, Z_{in} (of segment 1) is

$$Z_{IN} = j\omega(L + M) \tag{6.10}$$

This implies that the inductance of the conductor increases by M, and M is the mutual inductance between the two conductors. Thus, parallel currents travelling in-phase can contribute positive mutual components of inductance. For the case of out-of-phase current, such as current in segments 5 and 7, the calculation of the impedance, Z_{in} is almost the same but now V_i = - V_o and will contribute negative mutual components of inductance. Thus, the inductance of a conductor can be expressed as

$$L = L_{self} \pm M \tag{6.11}$$

The mutual inductance between two parallel conductors is a function of the length of the conductors and of the geometric distance between them. In general,

$$M = 2lQ_k, \tag{6.12}$$

where M is the mutual inductance in nH, l is the conductor length in cm, and Q_k is the mutual inductance parameter calculated from [47]

$$Q_k = \ln\left[\frac{1}{GMD} + \sqrt{1 + \frac{l^2}{(GMD)^2}}\right] - \sqrt{1 + \frac{l^2}{(GMD)^2}} + \frac{GMD}{l}, \tag{6.13}$$

where GMD, the geometric mean distance between the two conductors, is approximately equal to the distance between the track centre. For two parallel conductors with lengths of j and m (figure 6.8), the total mutual inductance can be represented by equation (6.14).

$$2\,M_{j,m} = (M_{m+p} + M_{m+q}) - (M_p + M_q), \tag{6.14}$$

and the individual M terms are calculated using equation (6.12) and the lengths corresponding to the subscript given by equation (6.15).

$$M_{m+p} = 2l_{m+p}Q_{m+p} = 2(m+p)Q_{m+p}, \tag{6.15}$$

where Q_{m+p} is the mutual-inductance parameter, Q for GMD/($m + p$).

The total inductance of the spiral in figure 6.9, which neglects the extra routing segments, is the sum of the self-inductances of each of the straight segments ($L_1 ... L_n$) plus all the mutual inductances between the segments given by

$$L_T = L_0 + M_+ + M_-, \tag{6.16}$$

where L_T is the total inductance, L_0 is the sum of the self-inductances of all straight segments, M_+ is the sum of the positive mutual inductances and M_- is the sum of the negative mutual inductances.

6.3.1.3 Skin depth effect

The resistance of a metal segment will increase as frequency rises due to the skin depth effect. The skin depth of metal is given by equation (6.17).

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}, \tag{6.17}$$

where δ is the skin depth, f is the frequency, and μ is the permeability of free space, $4\pi \times 10^{-7}$ H/m. The skin resistance, R_s is approximately ρ/δ. For aluminium, the skin depth is approximately 1.2 μm at 5 GHz, roughly the thickness of metal lines in IC fabrication process. This implies that the series resistance of the spiral would not deviate much from its dc value up to 5 GHz. For this reason, the skin depth effect will be ignored in the design (of this chapter) considered in section 6.3.3.

6.3.1.4 Inductor quality factor, *Q*

The quality of an inductor is measured by its Q, which is defined by

$$Q = 2\pi \frac{energy\ stored}{energy\ loss\ in\ one\ oscillation\ cycle} \tag{6.18}$$

For an inductor, only the energy stored in the magnetic field is of interest. Any energy stored in the inductor's electric field, due to some inevitable parasitic capacitances in a real inductor, is a loss. Hence, Q is proportional to the net magnetic energy stored, which is equal to the difference between the peak magnetic and electric energies. An inductor is at self-resonance when the peak magnetic and electric energies are equal. Therefore, Q approaches zero at the self-resonance frequency. Above the self-resonance frequency, no net magnetic energy is available from an inductor to any external circuit.

The inductor Q can be mathematically represented by

$$Q = 2\pi \frac{energy\ stored}{energy\ loss\ in\ one\ oscillation\ cycle} = \frac{R}{\omega L}\left(1 - \left(\frac{\omega}{\omega_o}\right)^2\right), \qquad (6.19)$$

which equals zero at $\omega = \omega_0$, and is less than zero beyond ω_0. In terms of impedance, Q is equal to the ratio of the imaginary to the real part of the circuit impedance. The circuit impedance is inductive below ω_0, and antagonistically capacitive above ω_0.

In some simple RF circuits, Q can be found by

For parallel circuit: $Q = R_p/|X_p|$, and for a serial circuit, $Q = |X_s|/R_s$ (6.20)

6.3.2 Physical inductor model

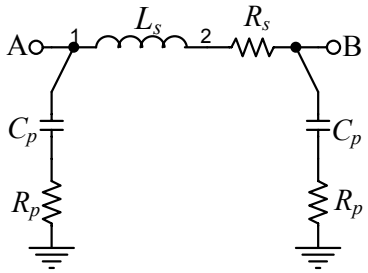


Figure 6.11. The figure shows an equivalent circuit of a spiral inductor.

Each segment of the inductor is modelled with a two-port network consisting of elements, as shown in figure 6.11. The geometry characteristics of interest are the track width, w of the spiral; the distance between two adjacent parallel tracks, s and the height of the metal track, t. The height of the Si substrate and the SiO_2 insulator are h_{Si} and h_{SiO2}, respectively. The main elements of the two-port are the series inductance, L_s, the resistance, R_s of the segment; and the capacitors, C_p formed by the insulating SiO_2 between the inductor and the Si substrate. Circuit parameters depicted in figure 6.11 can mathematically be approximated by equations (6.21) – (6.23), as also discussed in the section 6.2.

$$R_s = R_{sh}\frac{l}{w}, \qquad (6.21)$$

$$C_p = \varepsilon_o \varepsilon_r \frac{w}{h_{Si}}, \qquad (6.22)$$

$$R_{sub} = \rho_{Si}\frac{l}{wh_{Si}}. \qquad (6.23)$$

In the equations (on the previous page), R_{sh} is the sheet resistance of the metal track. All lengths are in cm, while inductance is in nH and capacitance in pF. In this circuit, L_s

models the self and mutual inductances in the second-metal segments, R_s is the accumulated sheet resistance, C_p models the parasitic capacitance from the second-metal layer to the substrate, and R_p represents the resistance of the conductive Si substrate. If one side of the inductor is grounded, the self-resonant frequency of the spiral inductor can be derived from the equivalent circuit. It is approximated by

$$\omega_r = \frac{1}{\sqrt{L_S C_P}} \sqrt{\frac{1 - R_s^2 \left(\frac{C_p}{L_S}\right)}{1 - R_p^2 \left(\frac{C_p}{L_S}\right)}}. \qquad (6.24)$$

Beyond the resonant frequency, the inductor becomes capacitive. C_p limits frequency, ω_r, which is inversely proportional to the oxide thickness between the second-metal layer and the substrate.

6.3.3 Design of the 10 nH square spiral inductor

This design is based on the background and equations that are introduced in section 6.3.2 and the previous section. In this design, a 0.35-µm process will be used to fabricate the chip. So, all the design specifications have been met for this process. The complete program (compiled in MathCAD) is given as part of appendix A. The results from MathCAD are shown in table 6.2.

Thickness, t (µm)	Space between segments, s (µm)	Width, W (µm)	Outer length, l_1 (µm)	Number of turns	Total inductance, L (nH)
1	4	6	213	7	10.02

Table 6.2.

The table shows the geometric values of square-spiral inductor from MathCAD.

The 5¼ turns (appendix A) means the square spiral inductor has 21 segments, as shown in figure 6.12. From appendix A, the two-port (AB) model shown in figure 6.11 will have the following values: R_s = 21.37 Ω, L_s = 10.02 nH, C_p = 0.7 pF, and R_p = 2.1 kΩ (ω_r = 38 krad/s).

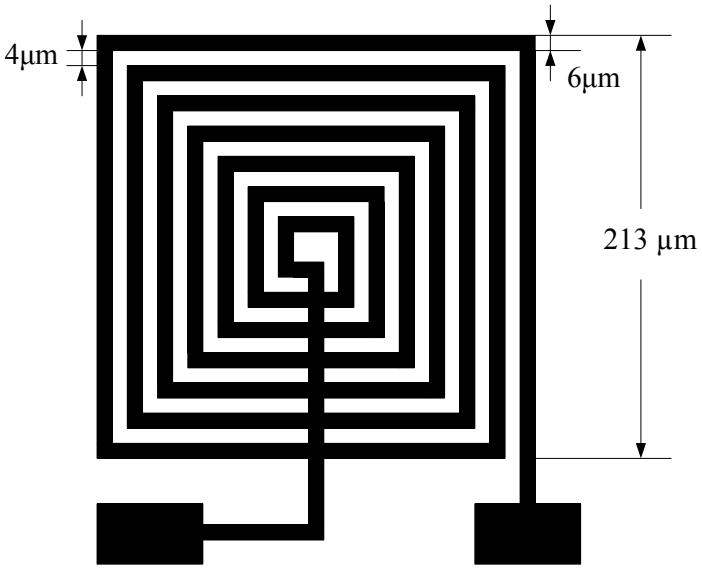


Figure 6.12. The figure shows the layout of the 10 nH inductor. Some of the dimensions are shown. These are obtained from appendix A.

The *Q* of this spiral inductor is changing as a function of frequency (mathematically shown in equation (6.19)), this is depicted in figure 6.13. The figure also shows that the quality factor, *Q*, in this case, has the maximum value of 5 at frequency 3.2 GHz. At high frequencies, when the substrate impedance is smaller than the inductive impedance of the spiral, the substrate loss dominates and the *Q* is a decreasing function of frequency (thus the peaking). This is important as the spiral inductor can be designed to have a peak *Q* at the frequency of interest.

6.4 Effects of Eddy Currents

The excitation currents flowing in the turns of the spiral generate a magnetic field that penetrates the substrate. Due to variations in the *B* field, eddy currents are formed which flow in the substrate. This is modelled as an inductor and resistor loop with appropriate coupling coefficients between the main turn inductor and the eddy inductor.

An important effect that is also modelled is the current crowding effect. It is a major contributor to losses at lower GHz range where skin effect is negligible [48-50]. Eddy currents are produced in the traces because of the *B* field of the adjacent turns, penetrating normal to the surface. This current actually adds to the current in the inside edges and

subtracts from the outside edges. The result is the increase in the effective series resistance. The next sections detail the device physics.

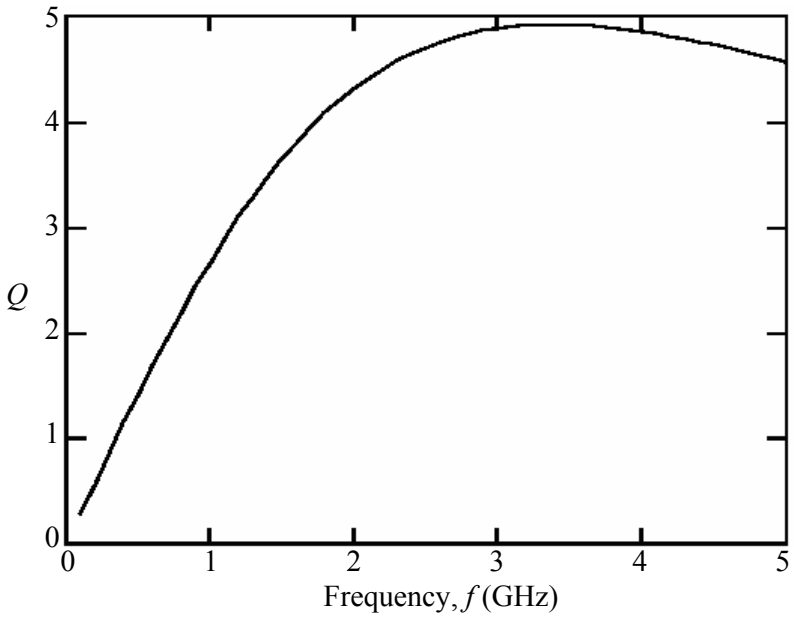


Figure 6.13. The figure shows the plot of the quality factor, Q as a function of frequency.

6.4.1 Substrate losses due to Eddy currents

In typical CMOS IC processes, the underlying substrate contributes losses to the Q of the spiral and its effects are not well understood [47 & 49]. To simplify modelling, several approximations will be made. A lumped element approach (like in section 6.2) is used to model these effects.

The excitation current passing through the traces of the spiral generates a magnetic field around it with directions given by the right hand rule. This magnetic field penetrates through the substrate and can be approximated as passing through a depth equal to one-sixth the outer dimension of the spiral [47]. There is a changing magnetic field in the substrate, and that causes the current flowing in it to be complex and three-dimensional. Using first order analysis and treating the currents circulating only under each turn, one can make a reasonable estimate of the current. Now, finding the sheet resistance of the substrate in which the magnetic fields are significant can be used to make a rough estimate of the losses in the substrate. Figure 6.14 shows that if the empty space in the centre of spiral is approximated, as $D/3$, then the spiral traces on each side would contribute $D/3$ each. Using this approximation, the thickness of the substrate through which the currents

are significant can be estimated to be one-sixth of the outer dimension of the spiral [47]. Thus, the sheet resistance can be calculated from

$$R_{sheet} = \frac{6\rho}{D}, \tag{6.25}$$

where ρ is the resistivity of the substrate, and D is the outer dimension of the spiral. Hence, R_{eddy} can be estimated from

$$R_{\text{eddy}} = \frac{LR_{sheet}}{W}, \tag{6.26}$$

where L is the total length of the each turn, and W is the width of the trace.

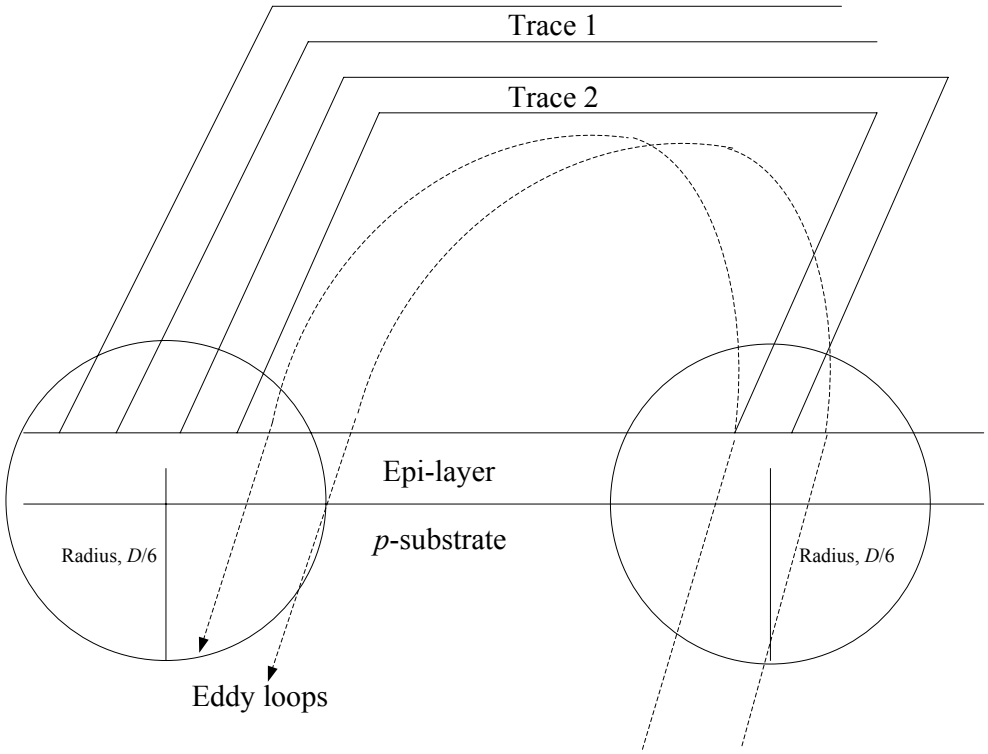


Figure 6.14. The figure shows an illustration showing eddy loops generated in the substrate and the estimation of substrate depth where the currents are significant.

Some special spiral geometries may have a large outer dimension with one or two thin traces. This makes the estimate of the width of the current flowing inaccurate. To get a better estimate for the width of the traces in all cases, the width is estimated by

$$Width = \frac{D}{2N}, \tag{6.27}$$

where D is the outer dimension, and the N is the total number of turns on a layer.

The coupling coefficients from the different series inductances to the eddy inductance can be calculated by finding the *B* fields contributed by each segment. This is detailed in the next sub-section.

6.4.2 *B* Field calculation

The sub-section briefs on the *B* field calculation method. This is used in finding the self and mutual inductance between the turns and the coupling coefficients. The outer dimension of the spiral is adjusted such that it is an integral multiple of the pitch. The whole spiral is then divided into squares the size of the pitch. A current element is assumed at the edge of each grid square, as shown in figure 6.15, and the *B* field generated by this current element is estimated at the centre of all other squares. The strength of the *B* field created by this current element is estimated at the centre of any other squares using the Biot-Savart law [51] and the direction by Maxwell's right hand rule:

$$B = \frac{\mu_o I\, d\,\bar{l} \times \bar{R}}{4\pi R^3}, \tag{6.28}$$

where μ_o is permittivity of free space, $I\, d\boldsymbol{l}$ the differential current element, and R the distance between the point and the current element.

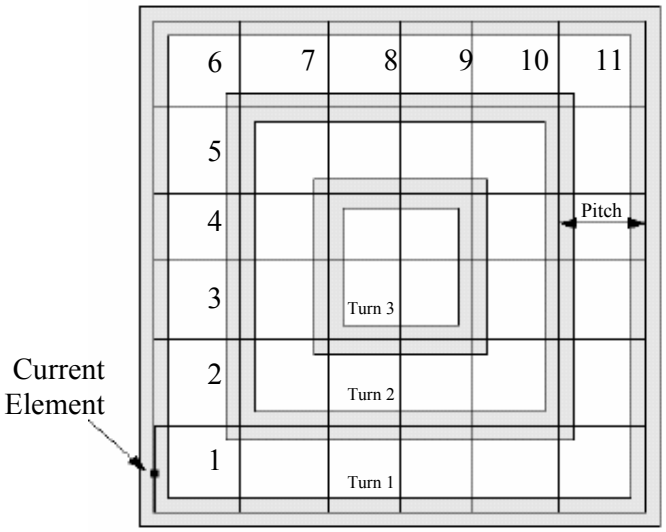


Figure 6.15. The figure illustrates the closed turn approximation and the grid for *B* field computations.

For instance, for the outermost turn (figure 6.15), the total *B* field due to the turn can be obtained at each individual square by considering the grid from squares 1...11 for the

whole turn and summing the *B* field in the centers of the squares. The total flux generated by the turn can be calculated using equation (6.29) [51].

$$\psi = \int_S \overline{B}.d\overline{S}\,, \tag{6.29}$$

where ***B*** is the magnetic field, and ***dS*** the infinitesimal area.

In this case the total flux would be the total *B* field in each square multiplied by the area of the square summed over all the squares inside the spiral. The self-inductance can thus be estimated from the total flux by equation (6.30) [51].

$$L = \frac{N\psi}{I}\,, \tag{6.30}$$

where N is the number of turns, ψ is the total flux inside the turn, and I is the current element.

It is evident that this estimation can be inaccurate and aggravated in the case of spirals, which have a thick trace width as the assumption of a current element for the race inside the grid becomes inaccurate.

6.5 Model simulation and testing

There are some software packages commercially available, which do electromagnetic simulation to characterize a spiral. Other software uses a lumped element model for similar simulation. Figure 6.16 shows some of the abovementioned software and compares them with respect to time required for simulation and the accuracy of the results (obvious Software Engineering trade-off, the closeness often comes with increased cost).

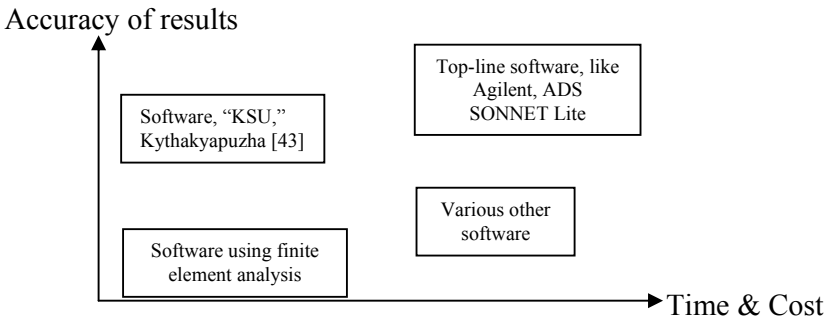


Figure 6.16. The figure shows commercially available software for simulation of the spiral inductor. The figure depicts the time, cost, and results accuracy trade-off.

For this dissertation, SONNET is used for the simulation. This is as a freely available student version (however, it is limited to simulate configurations that do not require more than 16 Mb of RAM). SONNET is a suite of products, which provides high-frequency planar electromagnetic analysis for different products. It uses a modified method of moments analysis based on Maxwell's equations to perform a true three-dimensional current analysis of predominantly planar structures. The electromagnetic engine, computes S, Y, or Z-parameters, transmission line parameters (Z_o and E_{eff}), and SPICE equivalent lumped element networks. The SPICE model (closely resembles the complete model accounting the Eddy current effects discussed in section 6.4) developed is, thereafter, used in the simulation of the LC VCO as shown in chapter 5.

6.5.1 Base-line inductor introduction & simulation

The basic characteristic of SONNET that makes it ideal for this problem is the accuracy with which conducting dielectrics are analysed. SONNET uses a FFT based analysis. As such, there is no accuracy degrading numerical integration. In addition, all fields in each layer are represented as a (large) sum of simple rectangular wave-guide modes (the side walls of the conducting box containing the circuit from the rectangular wave guide). Only the characteristic impedance and velocity of propagation of each wave guide mode needs to be changed - since these characteristics are known exactly for a rectangular wave guide, substrate conductivity is included with precisely the same accuracy as is seen in an equivalent lossless analysis. This is difficult to do in analyses based upon direct numerical integration of an underlying Green's function. Thus, the only problem to be overcome in analysing an inductor on silicon using SONNET Lite is to cast the problem into a form that satisfies the analysis constraints.

Figure 6.17 shows the base line inductor. To reduce the substrate loss, a coplanar inductor is used. The coplanar ground strips are the wide conductors in figure 6.17. Ground return current flows in these strips. Thus, the electric field from the signal line to ground need not pass through the entire silicon substrate. This results in lower loss. The inductor's dimensions are given in table 6.2, depicted in figure 6.12 as well as derived in appendix A.

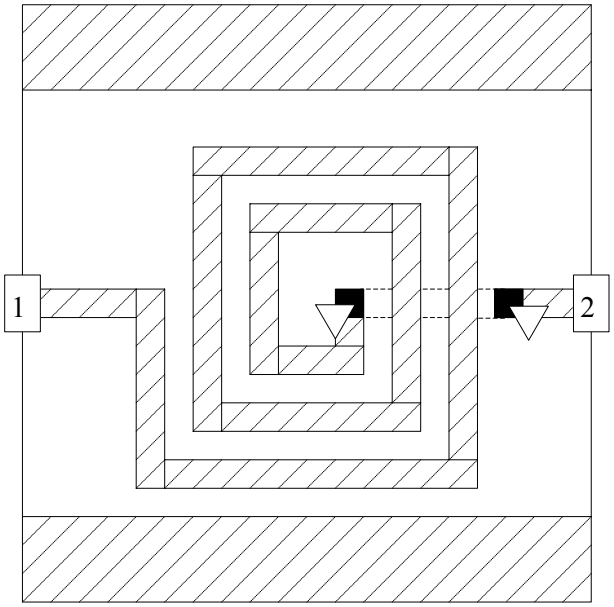


Figure 6.17. The figure shows the base line inductor (including coplanar ground return lines for lower loss). Note that the figure differs somewhat from the inductor designed in section 6.3, as it seeks to illustrate some of SONNET's capabilities.

The first task is to simplify the model of the inductor (figure 6.7) without significantly affecting accuracy. SONNET meshes only the metal surface and problem size increases rapidly with the number of subsections. Thus, it is desired to reduce the number of subsections as much as possible. The first way is by making the subsection size as large as possible. This does impact analysis error, but this is something quantified later. The other way to reduce the subsection count is by reducing metal area. The coplanar ground return lines are wide. It would be nice to eliminate them from the analysis. This is easily done as SONNET Lite places a perfectly conducting box sidewall at the edge of the substrate. By removing each ground strip and substituting a box sidewall in its place – the ground current flows in the box sidewalls rather than in the ground strips. Further, by placing the sidewalls from the inductor, as depicted in figure 6.18.

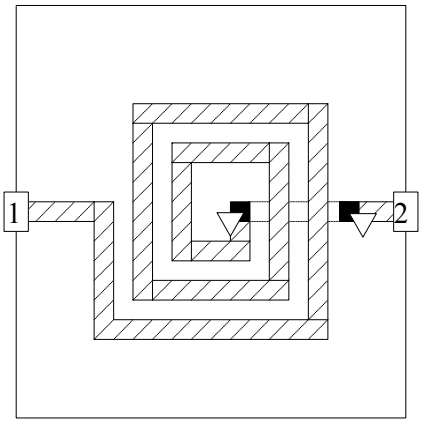


Figure 6.18. The figure shows the inductor of figure 6.17 modified so that the box sidewalls take the ground return current. Faster analysis can be obtained by removing the ground strips.

This is a major modification to the circuit - as an alternative to pointless hand waving. Figure 6.19 shows a comparison of the two approaches to this analysis. S_{11} is different by about 0.5 dB. S_{21} differences approach 2 dB, but only at high frequencies where S_{21} is down about 20 dB. It is assumed that these differences are small compared to requirements and proceed with the evaluation of the inductor of figure 6.18. On a 450 MHz Pentium the inductor of figure 6.18 analyses in 1 second per frequency and uses only 1 Mb of RAM.

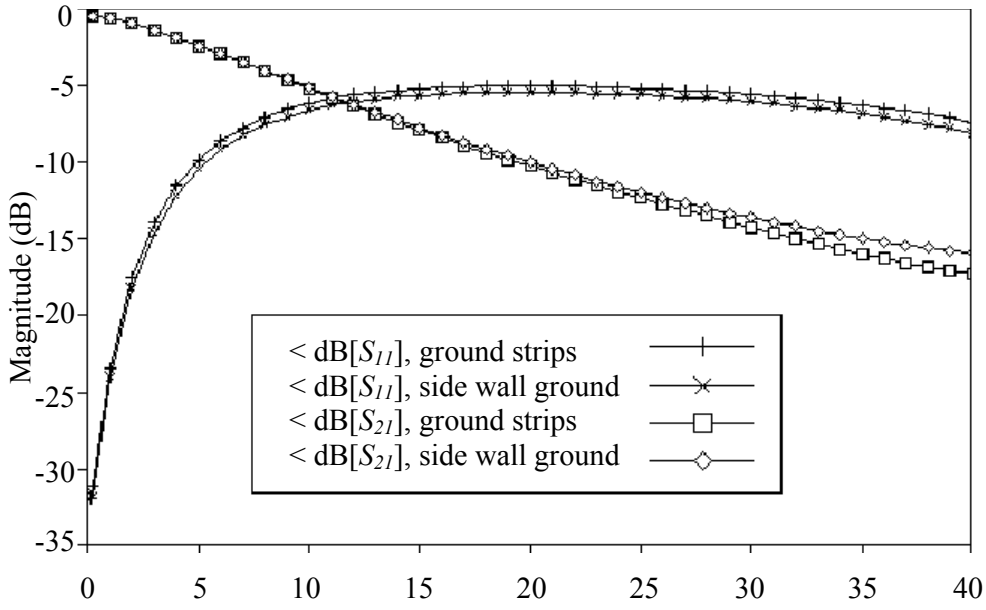


Figure 6.19.

The figure shows a comparison of analysis results from the inductor of figure 6.17 with the inductor of figure 6.18, by plotting ground strips versus sidewall ground return. S_{11} differences are about 0.5 dB. S_{21} differences approach 2.0 dB, but only at high frequency.

The original inductor requires 2 Mbytes and 2 seconds per frequency. While this is a small difference now, it becomes important later. If the half-dB difference is significant, trade-offs need be considered, as done using the inductor in figure 6.18. Once complete, then final performance analysis with necessary changes ("fine tuning") can be incorporated into the inductor of figure 6.17.

6.5.2 Error bounds

It is appropriate to determine the accuracy of the analysis. While all electromagnetic analyses are advertised as being accurate[1], a quantitative error analysis is also done. By comparing the estimated error with initial inductor specifications, the analysis done is justified. The error mechanisms for SONNET have been extensively investigated – in nearly all cases, the principal error source is error due to cell size. In addition, this error has the unique characteristic of reducing by half when cell size is cut in half (with a few well-understood exceptions). Error due to cell size is easily evaluated. If the cell size is cut in half and circuit analysed, then the error is also halved. From this information, the total error can be obtained. The results of just such a convergence analysis are shown in figure 6.20. The difference between the two curves is not easily seen, but is less than 0.15 dB nearly everywhere. This means that results obtained using double the cell size should be approximately ± 0.3 dB.

6.5.3 The lossless limit

Before loss reduction is attempted, it will be first assumed that loss is completely removed. Comparing a lossless analysis with the baseline lossy analysis gives an upper limit on how much the inductor can be improved. Under the loss-removal assumption, all loss (metal and substrate) from the inductor of figure 6.18 and analysing the resulting circuit: In figure 6.21, the lossless analysis is compared with the original lossy result. There is around 7 dB of loss in both S_{21} and S_{11} at 40 GHz. By comparing S-parameter data for the lossless case, the baseline case, and each case considered, the merits of each alternative can be quickly determined. It is noted that there is no need to calculate inductor Q, which, for the complicated equivalent circuits possible with planar spiral inductors, is neither uniquely defined nor simple to calculate.

[1] A study of the accuracy is mentioned at http://www.SONNETusa.com

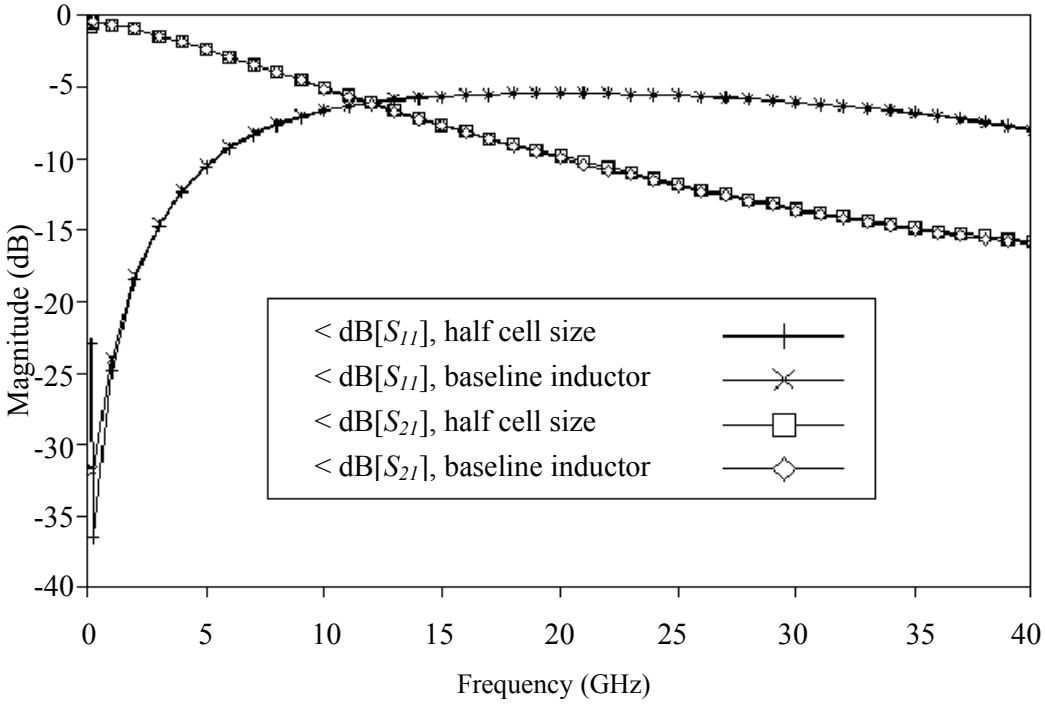


Figure 6.20. The figure shows error analysis by graphical methods - by cutting cell size in half, the error bounds can be determined for the analysis results.

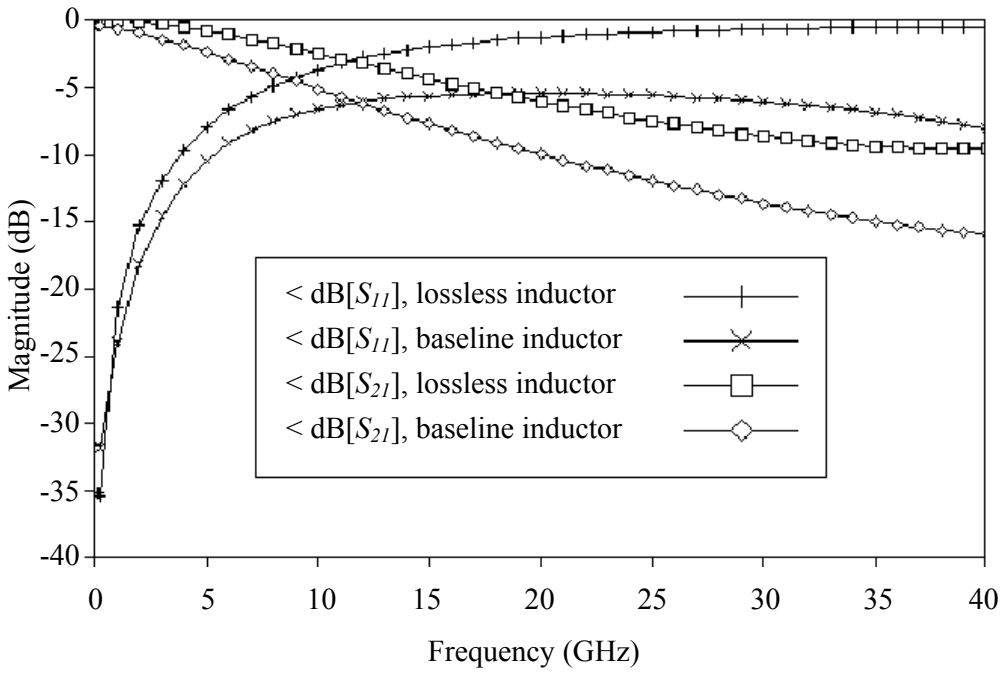


Figure 6.21. The figure shows a comparison between the baseline inductor (from figure 6.18) with the same inductor (but, with all loss removed). The results indicate a room for about 7 dB of improvement at 40 GHz.

6.5.4 Line width

Next, taking the baseline inductor of figure 6.18, the line width is increased. The reasoning being that taking a wider line width yields lower loss. Figure 6.22 shows the case of increasing the line width from 8 microns to 12 microns (4 micron cell size). The analysis result is shown in figure 6.21. The analysis now requires 11 seconds per frequency. Note that the loss has generally increased. While the effect of conductor loss has undoubtedly gone down, the effect of substrate conductivity has increased.

The loss drops unexpectedly around 40 GHz. The reason for this has not been investigated. It might be due to a resonance off the plot above 40 GHz. Since the wide lines failed, narrow lines are tired – this is shown in figure 6.21, i.e. the line width is decreased to 4 microns and figure 6.22 shows the analysis results (5 seconds per frequency). Loss has gone down substantially. If desired, one could continue until the optimum line width is found.

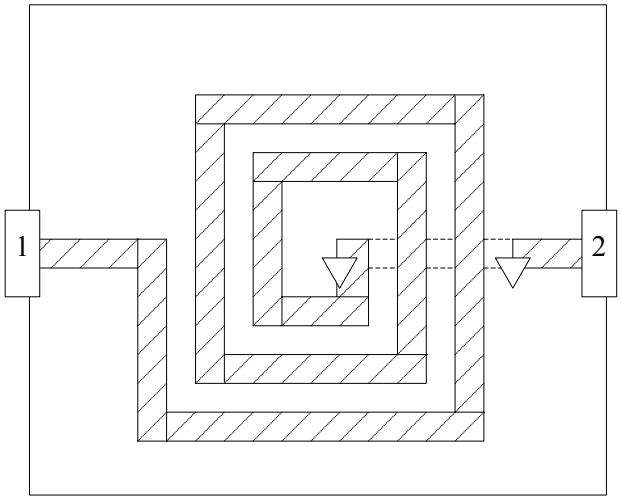


Figure 6.22. The figure shows the case when the line width is increased from 8 to 12 microns to investigate the effect on loss.

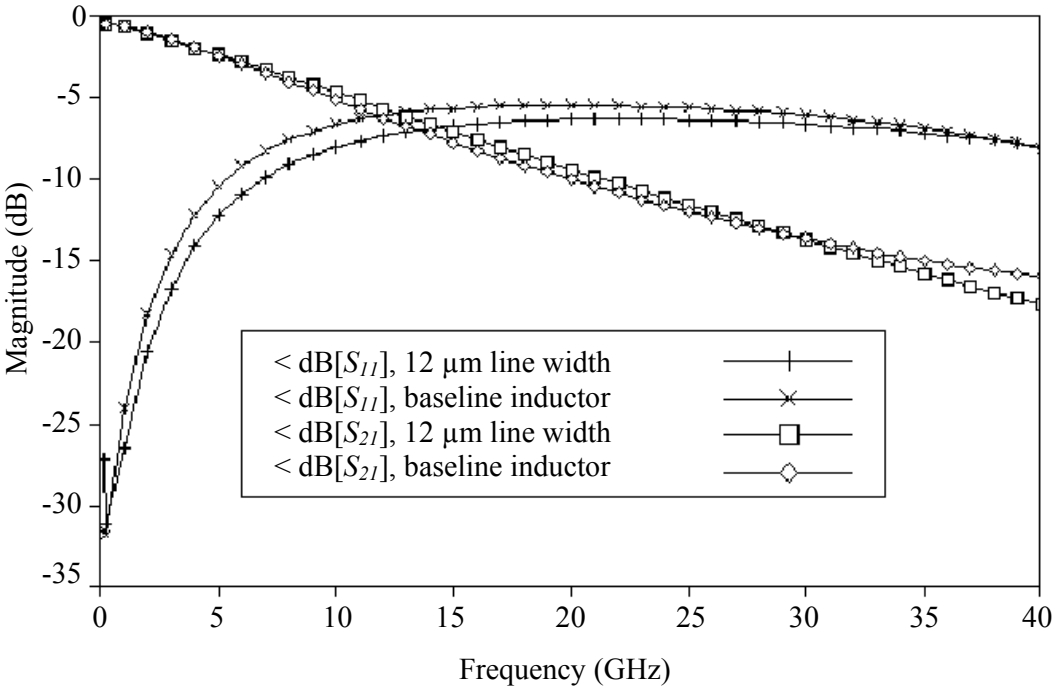


Figure 6.23. The figure shows the effect of increasing the line width from 8 to 12 µm unexpectedly increased loss.

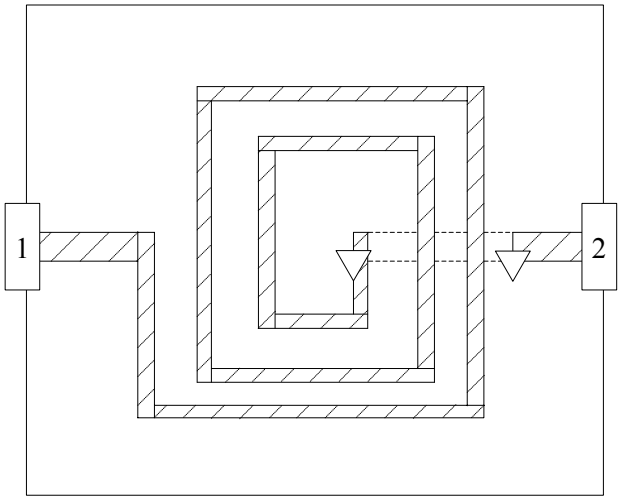


Figure 6.24. The figure shows the case when the line width is decreased from 8 to 4 microns to investigate the effect on loss.

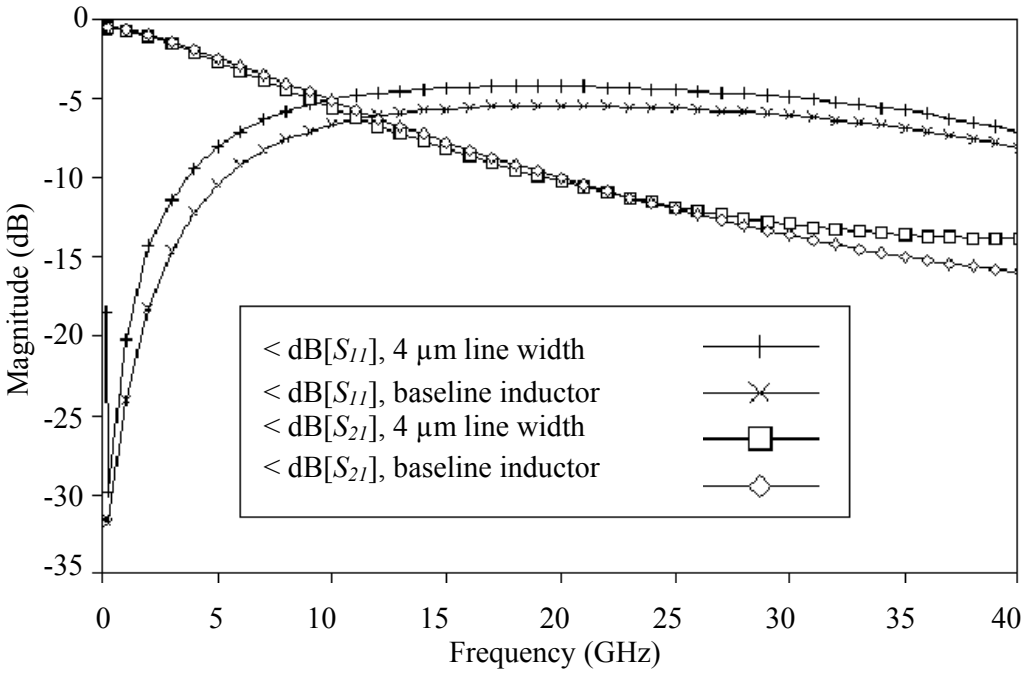


Figure 6.25. The figure shows the effect of decreasing the line width from 8 to 4 µm results in the desired decrease in loss.

6.5.5 Insulating layer thickness and dielectric constant

A spiral inductor on silicon usually has a thin insulating layers (for example, SiO_2) deposited underneath it. This reduces the effect of substrate conductivity, especially at low frequency. To reduce the loss, a thicker insulating layer can be used or choosing a material with a lower dielectric constant.

To investigate these alternatives, the insulating layer thickness is doubled. The result is shown in figure 6.26. Next, using the original layer thickness, the dielectric constant is halved. The result is in figure 6.27. Both actions substantially reduce inductor loss at all frequencies.

Now, with knowledge of the relative importance of each parameter with respect to loss, and with knowledge of manufacturing and design constraints, the chapter considers achieving a design to realize the lowest possible loss. To gain some further insight into this particular spiral inductor design, the spiral inductor of figure 6.18 with extremely small cell size is examined. The resulting current distribution from this is shown in figure 6.28.

Note that there is some disruption of the current distribution at the location of the underpass connection to port 2. This is common in underpass and overpasses situations and is real. It is not a numerical artifact. Port 1 is excited with a one-volt source at 40 GHz connected in series with a 50 Ω resistor. Port 2 is terminated in 50 Ω.

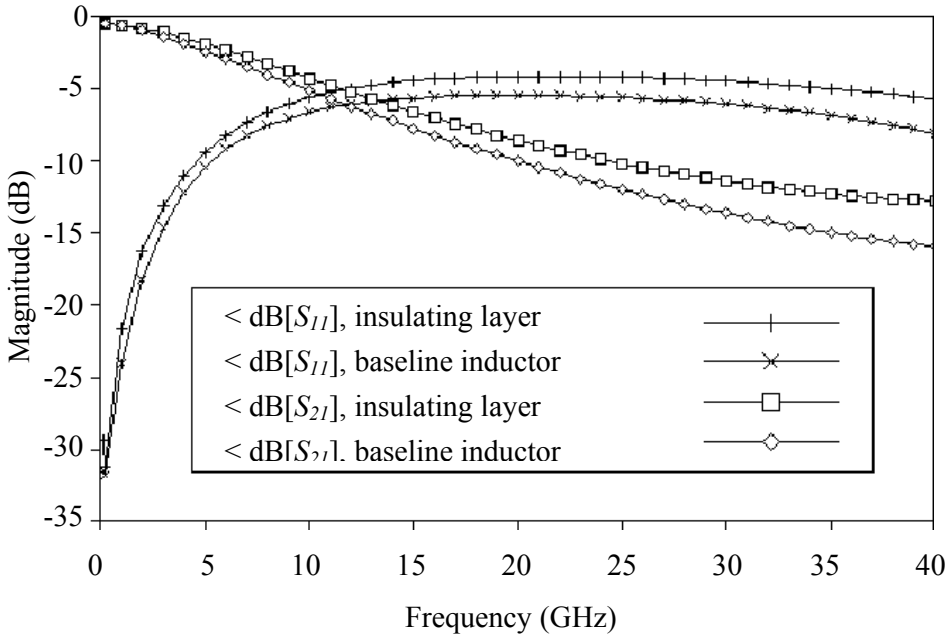


Figure 6.26. The figure shows the effect of insulating layer thickness. By doubling the thickness of the insulating layer on top of the silicon substrate, the inductor loss is reduced substantially.

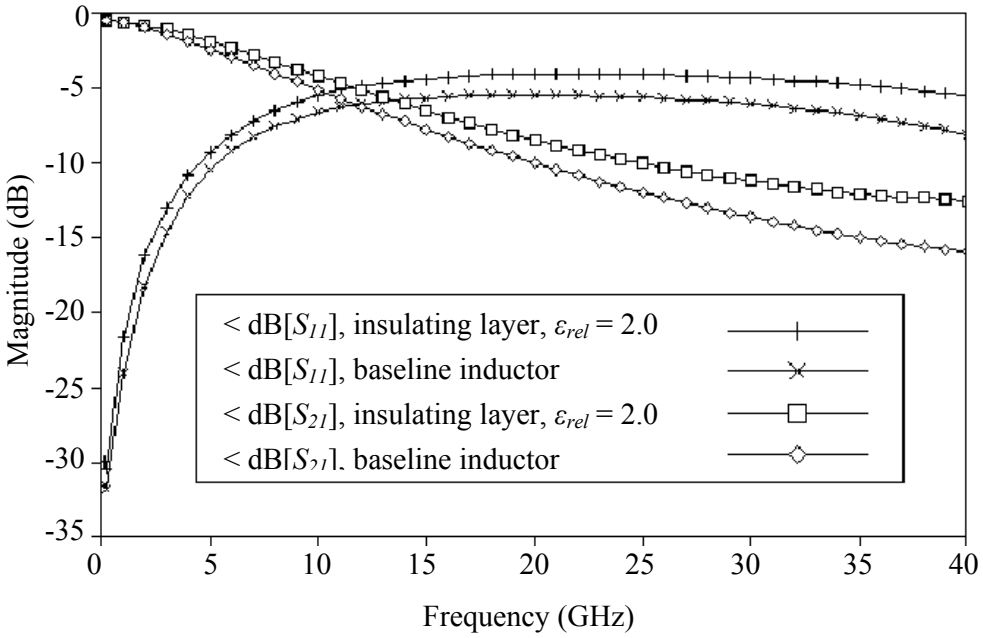


Figure 6.27. The figure shows the effect of insulating layer thickness. By halving the dielectric constant of the thin insulating substrate on top of the silicon substrate, the inductor loss is again reduced substantially.

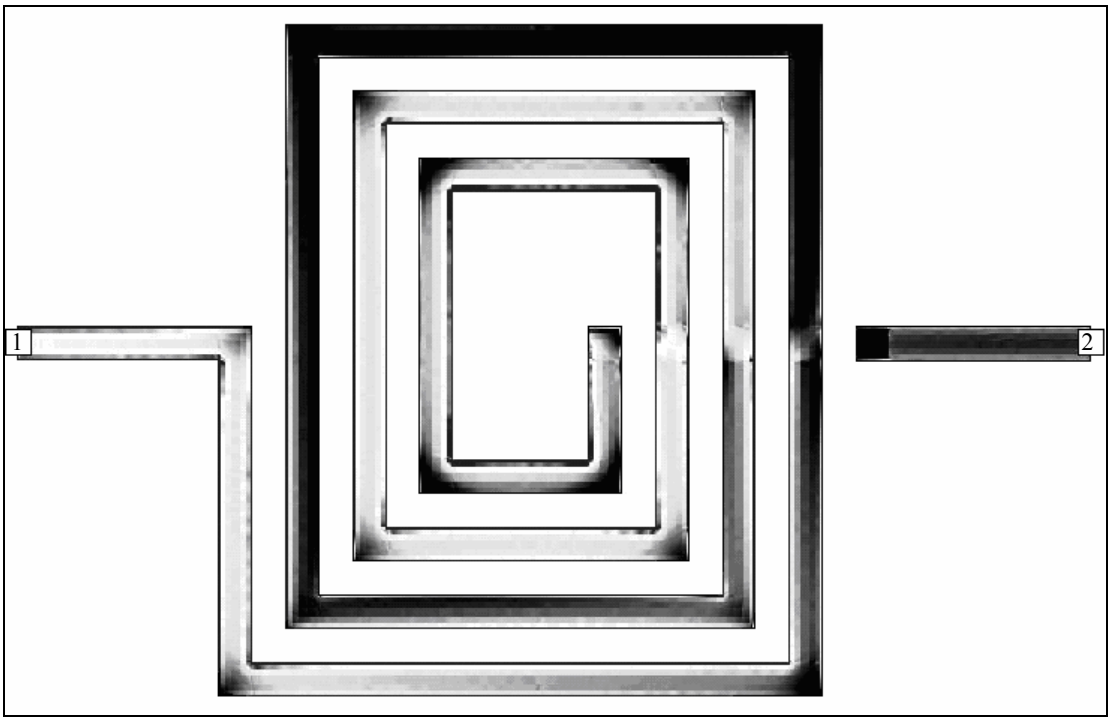


Figure 6.28. The figure shows the current distribution for the baseline spiral inductor analysed with a very fine 0.5 μm cell size. The disruption near the underpass connection to port 2 is real; it is not a numerical artefact.

6.5.6 Conclusions from SONNET Lite simulations

The earlier sections of this chapter, viz. sections 6.5.2- 6.5.5 demonstrate how SONNET Lite can be used to simulate a spiral inductor (on a conductive silicon substrate). In addition, it is shown how to modify the inductor so as to reduce inductor loss and how to characterize the analysis error quantitatively.

6.6 Incorporation and testing in a LC VCO

It is clear (from section 5.2.1.2.11 and section 5.2.1.2.12) that the inductor Q is critical for RF circuit performance. From chapter 5 & chapter 6, it is clear that spiral inductors on silicon are:

- feasible for inductance range between 0.5 to 100 nH (a 10 nH inductor is designed in section 6.3 of this chapter), and
- Q values up to 24 (Al) or 36 (Cu) can be obtained as indicated in figure 5.49.

Note that crosstalk was not considered as a major issue [30].

6.7 CMOS active inductors

This section investigates the development of analogue circuits which operate at the technology limits of silicon CMOS, suitable for implementing tuned oscillators (as discussed in section 6.7.2), particularly for use in wireless applications. The development of such circuits is an important step towards the realisation of a fully integrated (and ultimately single-chip) wireless communications receiver. The section aims (i) to develop high-frequency active inductor topologies for implementation in Si CMOS technology, and (ii) to develop these CMOS active inductor topologies into front-end bandpass filter circuits in the low microwave frequency range (as an additional test case.) Motivational factors for implementing active inductors include increased tuneability, plus reduced chip area and processing cost, compared to on-chip passive inductor architectures.

6.7.1 Active inductor implementation

The first phases consider the basic development of fully-integrated active inductor architectures. The main performance criteria is operation close to f_T, high Q, independent tuning of inductance and Q, acceptable dynamic range, low power supply voltage and low power consumption. Numerous alternative architectures were investigated both analytically and using simulation tools, namely OrCAD[2]. The most promising architectures are reported in this section.

6.7.1.1 Inductor simulation

The gyrator-C architecture is a classical approach for designing active inductors; this topology typically employs a gyrator (consisting of two transconductors connected in a feedback configuration) with an integrating capacitor. The performance of the active inductor is ultimately determined by the capabilities of the active transconductors. Complex linearised transconductors may be used at low frequencies to achieve good phase accuracy and high dynamic range, however such techniques are generally not suitable for frequencies approaching the f_T of the technology. At these frequencies, the performances of the gyrator and active inductor are demeaned by the high-frequency phase errors caused by the parasitic poles and zeros within these transconductors [52]. For high frequency operation, internal nodes within the circuit should be minimised to reduce the number of

[2] OrCad is an electronic simulation package from Cadence: http://www.orcad.com

parasitics, therefore it is more appropriate to implement transconductors by using as few devices as possible. An alternative strategy suitable for high-frequency operation is to make use of the intrinsic poles and zeros within the devices to implement the inductor characteristics [53-54]. Due to continuous improvements in CMOS technology, it is now typical for a sub-micron gate length CMOS device to exhibit an f_T in excess of 10 GHz. The intrinsic capacitance method should, thus, be capable of implementing CMOS active inductors operating in the wireless radio frequency range (0.8 GHz - 2 GHz). The next few sub-sections aim to discuss some designs of high-frequency CMOS active inductors (using the intrinsic capacitance approach).

6.7.1.2 Single-ended CMOS active inductor

An understanding of the work (passive inductor implementation in section 6.1-6.6) led to the development of the novel single-ended RF CMOS active inductor architectures capable of operating close to the f_T of the technology with high-Q values [55]. Applying gain-enhancement techniques based on cascoding, which extends the inductive range, reduces the inductor loss. Regulated and multi-regulated cascoding techniques further reduce the inductor loss (thus, increasing the Q), and provide the additional benefit that controlling bias currents can independently tune the inductance value and Q. The use of multi-regulated cascode structures preserves high frequency operation, as the additional "regulating" transistors are not within the signal path. Figure 6.29 illustrates the basic regulated and multi-regulated cascode active inductor topologies [56].

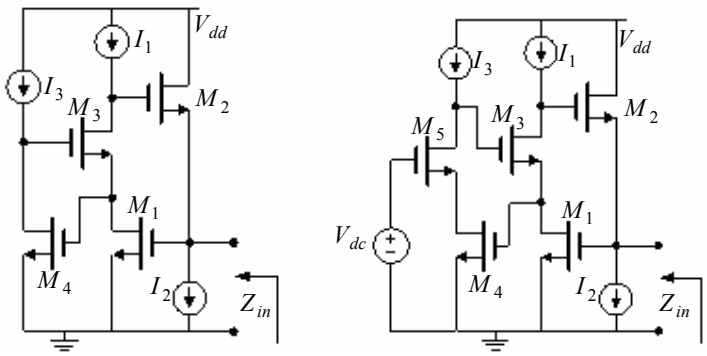


Figure 6.29. The figure shows regulated and multi-regulated cascode active inductors, [37].

The performance of these single-ended active inductor architectures has been evaluated by simulation using OrCAD with process parameters from a 0.6 μm CMOS process (AMS). The regulated cascode inductors achieve a bandwidth of over three decades and

self-resonant frequency up to 1 GHz, with an inductance value which can be tuned in the range of a few hundreds of nH, while the maximum obtainable Q value is in excess of 100 [57]. A simple RLC bandpass filter was simulated based on the active inductor, verifying that the centre frequency and Q of the filter can again be orthogonally tuned [58]. A maximum Q of 80 was obtained at a centre frequency of 0.5 GHz.

6.7.1.3 Differential CMOS active inductor

The performance of the single-ended active inductor is limited by the fact that it implements a grounded inductor only, and additionally the dynamic range is limited by the asymmetric "class A" operation. Due to these disadvantages, another implementation of a fully differential version of the active inductor is shown in figure 6.30, [59]. This fully differential architecture exhibits increased dynamic range, improved common-mode noise rejection and reduced even harmonic distortion when compared to the single-ended version [58]. The main drawback of a fully differential architecture is the need for common-mode control circuitry. Existing common-mode feedback control circuits could not be used as these were found to severely degrade the high frequency response of the active inductor. Thus, weak positive feedback (obtained by a negative resistance load circuit (as shown in figure 6.30)) was used to achieve the common-mode control without seriously degrading the frequency response.

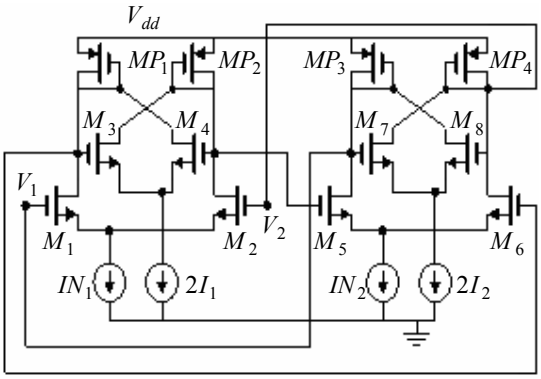


Figure 6.30. The figure shows a differential active inductor, [58].

6.7.1.4 Improved CMOS differential active inductor

The differential active inductor of figure 6.30 achieves high frequency operation with good linearity, however the penalty is increased power consumption compared to the single-ended version. As discussed earlier, a further disadvantage of this active inductor is the use of resistance cancellation to achieve Q enhancement is very sensitive to process tolerances. To circumvent these problems while maintaining the performance benefits of a differential structure, an alternative differential active inductor architecture has been implemented [60] which does not require additional negative resistance loads. This alternative architecture achieves very low series resistance by employing pole-zero compensation. In this approach, shown in figure 6.31, feedback resistors are connected between the two transconductors; these feedback resistors are implemented using MOS devices biased in the triode region, such that the resistor value can be fine-tuned by varying the gate voltage, V_Q. These resistors combine with the parasitic capacitance at the input of the second transconductor to provide positive phase compensation. The addition of these feedback resistors also allows the dc bias conditions of the two transconductors to be independently set, thus the input bias voltage of the second transconductor is set at a point which maximizes the dynamic range. The performance of this differential active inductor had been evaluated by simulation using OrCAD with process parameters from AMS 0.6 µm CMOS technology. Simulations indicate that a wide inductive range and orthogonal tuning of inductance value and quality factor are achieved with low power consumption [58].

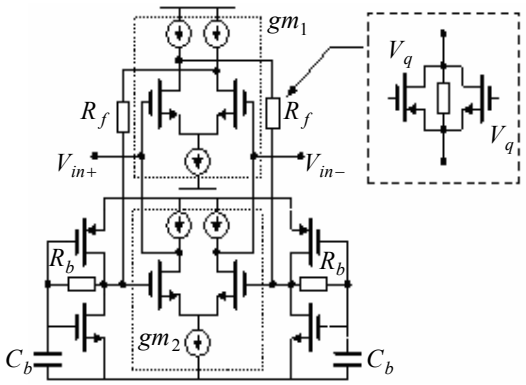


Figure 6.31. The figure shows a differential active inductor, [60]

6.7.2 Possible application of the active inductor – tuned oscillators

Tuned LC-oscillator architectures are preferable for high-performance applications (as discussed in chapter 5) due to their high-frequency capabilities and low phase noise characteristics when compared to ring oscillators [45]. Oscillators realised using an amplifier with passive LC tanks exhibit superior phase noise characteristics, however they typically require the use of a tuneable capacitance (for example a varactor or a MOS-capacitor) for frequency tuning. As a consequence, the tuning range of the oscillation frequency is usually limited, especially when on-chip varactors are used. The implementation of integrated amplifier-LC oscillators is also limited to frequencies in the GHz range (and beyond) because of the difficulty of integrating large inductor values.

An LC oscillator has been implemented by replacing the passive inductor in an LC tank with a differential CMOS active inductor [46]. Simulation results show that the resulting circuit is capable of producing high-frequency oscillation with low output distortion (less than 1 % for 0 dBm output power) under low power supply voltage. Additionally, the amplitude and frequency of the oscillation are electronically controllable which is necessary in post-fabrication tuning against component tolerances in the circuit. The oscillation frequency is tuneable from 400 MHz to more than 1.1 GHz. The main disadvantage of the actively tuned oscillator is the poorer phase noise characteristic compared to a passive LC tank (detailed in chapter 5); this is mainly caused by the noise of the active inductor. Consequently, larger capacitance value and power consumption are required to achieve low phase noise in an actively tuned oscillator. Nevertheless, the circuit exhibits a relatively wide oscillation frequency tuning range when compared to the previously (chapter 5) discussed passive LC-tuned oscillators, making it a good choice for implementation of wideband frequency synthesisers, where the oscillator phase noise at low offset frequencies is attenuated (high-pass filtered) by the PLL action.

6.7.3 Conclusions: active versus passive inductors

CMOS active inductor structures seem promising for the implementation of fully integrated resonant circuits due to their small area and inherent tuneability. The main alternative method (as discussed in section 6.1-6.6) for implementing integrated RF resonant circuits is to use an on-chip passive inductor. A passive inductor has the advantage that power consumption is negligible, and achieving high dynamic range. However, a high-quality integrated passive inductor often requires additional processing

steps, involving extra cost. Moreover, the inductance value is not tuneable, thus additional tuning circuitry is required. High inductor values are also not feasible due to the large chip area required, which also leads to high associated losses. Although high-Q, GHz-region bondwire inductors have also been demonstrated [59], the accuracy and reproducibility of these inductors is still questionable due to uncertainties in fabrication. Several RF resonant circuits have recently been realized in standard Si processes with the use of a negative resistance circuit to compensate for the inductor losses. As a consequence, the inductor Q is improved at the expense of increased noise figure and power consumption. The performance of Q-enhanced passive inductors, thus, becomes comparable to that achievable with an active inductor, while the active inductor has the additional advantage of reduced area and increased tuneability.

Although the active inductor has been investigated for this dissertation, a passive inductor has been used for the final synthesizer design (due to the higher frequency operation required by the LC oscillator.)

CHAPTER 7: CONCLUSION

7.1 Technical summary and contribution

This dissertation completes the design and implementation of an integrated frequency synthesizer for wireless applications. The dissertation also places various sub-system research issues in the context of the designed synthesizer, amongst others, the distinguishing technical features of the synthesizer implemented include:

- a dual loop architecture allowing a larger bandwidth (leading to lower phase noise [66]),
- a series SSB mixer integration (within the high frequency loop) allowing reduction of undesired sidebands as well as generating the required frequency increments,
- use of different VCO topologies, viz. a ring oscillator and LC oscillator (as per the different loop requirements, such as high frequency range and operation),
- a detailed investigation of different on-chip inductor implementations to provide high-purity signals for the LC VCO, and
- an investigation of high-speed dividers and their implementation.

Optimal integration of the above sub-systems (and associated design challenges and configuration choices related to the integration of a full on-chip synthesizer) serves as the main contribution of this dissertation. The following serves to list the technical specifications of the designed synthesizer (the design of this system was conducted at room temperature, however, several techniques for temperature stability was deployed):

- Carrier Frequency: 2.4 GHz
- Channel Spacing: 1 MHz
- No. of Channels: 79
- Process: AMS CMOS 0.35 µm
- Architecture: dual-loop
- Supply Voltage: 3.3 V
- Reference Frequency: 144 MHz & 1 MHz (refer to figure 4.3)
- Chip Area: 3.8 mm^2
- Loop Filter: on-chip
- Loop Bandwidth: 100 kHz and 50 kHz
- Phase Noise (at 1000 kHz offset): –84 dBc/Hz
- Power Consumption: 120.6 mW

7.2 Technical synthesis and future work

Phase noise and sideband suppression serve to be the major challenges of frequency synthesizer integration. Commercial synthesizer solutions seldom include the integration of VCOs on the same chip: in this dissertation, it is shown that a single-chip solution is possible, however, at the expense of phase noise performance. This dissertation does investigate some active inductor (with higher Q values) implementation, however, the final implementation does not include an active inductor (due to the high frequency limitation.) It has been shown [15] that a high frequency active inductor (with some alternative topologies) may be incorporated, and this could serve as a future improvement to the design of this dissertation.

Amongst other techniques used to reduce the abovementioned effects, the following can be noted.

- During noise analysis, it was found that the PMOS (in the delay cell) contributed to a large amount of noise to the ring oscillator. A future suggestion could be to incorporate frequency control with bias current.
- Another major source of noise is the bias transistor. For a given current, the noise current is inversely proportional to V_{DS}. With some modification, such as removing the cascode (in the current source), V_{DS} can be increased. A small increase (if at all) in common mode power supply sensitivity is expected since the differential pair pushes the current source into the triode region decreasing its effective resistance. The total area of the bias transistor is increased to decrease the flicker noise (which is inversely proportional to device area.)
- Noise currents in parallel with the control node of the VCO directly modulate the output signal and should be reduced. The charge pump circuit is scaled to minimize noise contributions that the charge pump may add.
- The SSB mixer requires very stringent high-frequency performance, which includes an output frequency of 2.4 GHz with both input frequencies of around 100 MHz and 2.3 GHz. One of the possible solutions to release such tough requirements is putting a high-frequency prescalar between the SSB mixer and the LC-oscillator, [67]. The prescalar can reduce the input frequency of the mixer RF input.
- A trade-off of the dual-loop architecture is the reduction of the low-frequency loop reference frequency due to the required channel spacing. In order to maintain the designed large loop bandwidths, a larger modulus number of the X-counter may be required to

compensate the change and at the same time, the tuning capacity of the VCO in low-frequency loop should be increased.

7.3 Further research work

This section serves to provide proposals that stems (indirectly) from this dissertation but could serve as proposals for further research work.

Noise related specifications serve as an important system specification for design of RF sub-systems. However, there is a current lack of accurate noise prediction methods (and simulators) for regenerative oscillators. Future works in this direction could also be applied to the design of high speed, low jitter prescalers [68].

In the present design, the LC VCO could operate at frequencies higher than 5200 MHz (ISM/HiperLAN applications [69]) when the supply voltage was increased past 3.3 volts. Future designs should be able to operate from a 3 (or even lower) volt power supply. The easiest solution would be to move to a faster technology such as 0.25 µm CMOS process [67]. If such a move was made, not only would it be possible to operate from a 3 volt power supply, but lower noise would also be achieved. A simple argument shows this: If, for example, the same bias current is used for the 0.25 µm oscillator as the 0.35 µm oscillator, the 0.25 µm oscillator would operate 30 % faster than the 0.35 µm oscillator. The 0.25 µm oscillator could be “slowed down” by increasing the size of the output swing, reducing the noise.

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APPENDIX A: MATHCAD ALGORITHM – INDUCTOR DESIGN

The following gives the MATHCAD routine used for the design of the inductor (chapter 5 & chapter 6).

$t := 0.0001\,cm \quad s := 0.0004\,cm \quad w := 0.0006\,cm \quad I_1 = 0.0213\,cm \quad N := 7$

$k := 4 \cdot N$

$r := 2..(2 \cdot N)$

$I_2 := I_1 \quad I_3 := I_1$

$I_{2r} := I_2 - (r-1) \cdot (w+s)$

$I_{2r-1} := I_1 - (r-2) \cdot (w+s)$

$$length := \sum_{y=1}^{k} I_y$$

$I_1 = 0.0213$

$I_2 = 0.0213$

$I_3 = 0.0213 \quad I_4 = 0.0203\,cm$

$length = 0.4274\,cm$

$y := 1..k$

$$L_y := 0.002 \cdot I_y \left[\ln\left[2\frac{I_y}{(w+t)} \right] + 0.50049 + \left(\frac{w+1}{3 \cdot I_y} \right) \right]$$

$$L_o := \sum_{y=1}^{k} 10^3 \cdot L_y$$

$L_o = 3.6982\,nH$

$$GMD1 := \left| \begin{array}{l} \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad \left| \begin{array}{l} \ln(n(s+w)) - \left[1 + \frac{1}{12\left[\frac{n \cdot (s+w)}{w}\right]^2} + \frac{1}{60\left[\frac{n \cdot (s+w)}{w}\right]^4} + \frac{1}{168\left[\frac{n \cdot (s+w)}{w}\right]^6} \right] \text{ if } (j+4 \cdot n) \le k \\ t_{j \cdot (j+4 \cdot n)} \leftarrow c \\ 0 \text{ otherwise} \end{array} \right. \\ t \end{array} \right.$$

$$Mlj := \left| \begin{array}{l} sum1 \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad \left| \begin{array}{l} suml \leftarrow suml + 2 \cdot I_j \cdot \left[\left[\ln\left[\frac{I_j}{GMD1_{j\cdot(j+4n)}} + \left[1 + \left[\frac{I_j}{GMD1_{j\cdot(j+4n)}} \right]^2 \right]^{0.5} \right] - \left[1 + \frac{GMD1_{j\cdot(j+4n)}}{I_j} \right]^2 \right]^{0.5} + \frac{GMD1_{j\cdot(j+4n)}}{I_j} \right] \\ 0 \text{ otherwise} \end{array} \right. \\ suml \end{array} \right.$$

$$\text{if } (j + 4 \cdot n) \le k$$

$$Mlm := \left| \begin{array}{l} summ \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad \left| \begin{array}{l} sumlm \leftarrow sumlm + 2 \cdot I_{j+4n} \cdot \left[\left[\ln\left[\frac{I_{j+4n}}{GMD1_{j\cdot(j+4n)}} + \left[1 + \left[\frac{I_{j+4n}}{GMD1_{j\cdot(j+4n)}} \right]^2 \right]^{0.5} \right] - \left[1 + \frac{GMD1_{j\cdot(j+4n)}}{I_{j+4n}} \right]^2 \right]^{0.5} + \frac{GMD1_{j\cdot(j+4n)}}{I_{j+4n}} \right] \\ 0 \text{ otherwise} \end{array} \right. \\ sumlm \end{array} \right.$$

$$\text{if } (j+4\cdot n) \le k$$

$$Mlp := \left| \begin{array}{l} sumlp \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad \left| \begin{array}{l} sumlp \leftarrow sumlp + 2 \cdot (I_j - I_{j+4\cdot n}) \cdot \left[\left[\ln\left[\frac{I_j - I_{j+4\cdot n}}{GMD1_{j\cdot(j+4n)}} + \left[1 + \left[\frac{I_j - I_{j+4\cdot n}}{GMD1_{j\cdot(j+4n)}} \right]^2 \right]^{0.5} \right] - \left[1 + \frac{GMD1_{j\cdot(j+4n)}}{I_j - I_{j+4\cdot n}} \right]^2 \right]^{0.5} + \frac{GMD1_{j\cdot(j+4n)}}{I_j - I_{j+4\cdot n}} \right] \\ 0 \text{ otherwise} \end{array} \right. \\ sumlp \end{array} \right.$$

$$\text{if } (j+4\cdot n) \le k$$

$$M1 := M1j + M1m - M1p$$

$$M1 := 12.5647 \text{ nH}$$

$$l2p := \left| \begin{array}{l} sum2p \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad \left| \begin{array}{l} sum2p \leftarrow sum2p + 2\cdot(I_j - I_{j+4\cdot n-2})\cdot\left[\left[\ln\left[\frac{I_j - I_{j+4\cdot n-2}}{2GMD2_{j\cdot(j+4n-2)}} + \left[1+\left[\frac{I_j - I_{j+4\cdot n-2}}{2GMD2_{j\cdot(j+4n-2)}}\right]^2\right]^{0.5}\right] - \left[1+\left[\frac{2GMD2_{j\cdot(j+4n-2)}}{I_j - I_{j+4\cdot n-2}}\right]^2\right]^{0.5}\right] \\ \text{if } 1+\frac{2GMD2_{j\cdot(j+4n-2)}}{I_{j+4\cdot n-2}} \text{ if } (j+4\cdot n-2)\le k \\ 0 \text{ otherwise} \end{array} \right. \\ sum2p \end{array} \right.$$

$$GMD2 := \left| \begin{array}{l} \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad \left| \begin{array}{l} \ln\left[I_{j+1} - n\cdot(s+w)\right] - \left[1+\frac{1}{12\left[\frac{I_{j+1} - n\cdot(s+w)}{w}\right]^2} + \frac{1}{60\left[\frac{I_{j+1} - n\cdot(s+w)}{w}\right]^4} + \frac{1}{168\left[\frac{I_{j+1} - n\cdot(s+w)}{w}\right]^6}\right] \\ u_{j\cdot(j+4\cdot n-2)} \leftarrow c \\ \text{if } (j+4\cdot n-2)\le k \\ 0 \text{ otherwise} \end{array} \right. \\ u \end{array} \right.$$

$$M2m := \left| \begin{array}{l} sum2m \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad \left| \begin{array}{l} sum2m \leftarrow sum2m + (2\cdot = I_{j+4\cdot n-2})\cdot\left[\left[\ln\left[\frac{I_{j+4\cdot n-2}}{GMD2_{j\cdot(j+4n-2)}} + \left[1+\left[\frac{I_{j+4\cdot n-2}}{GMD2_{j\cdot(j+4n-2)}}\right]^2\right]^{0.5}\right] - \left[1+\left[\frac{GMD2_{j\cdot(j+4n-2)}}{I_{j+4\cdot n-2}}\right]^2\right]^{0.5}\right] \\ \text{if } 1+\frac{2GMD2_{j\cdot(j+4n-2)}}{I_{j+4\cdot n-2}} \text{ if } (j+4\cdot n-2)\le k \\ 0 \text{ otherwise} \end{array} \right. \\ sum2m \end{array} \right.$$

$$2j := \begin{cases} sum2 \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad sum2 \leftarrow sum2 + 2 \cdot I_j \cdot \left[\left[\ln\left[\frac{I_j}{GMD2_{j\cdot(j+4n-2)}} + \left[1 + \left[\frac{I_j}{GMD2_{j\cdot(j+4n-2)}} \right]^2 \right]^{0.5} \right] - \left[1 + \frac{GMD2_{j\cdot(j+4n-2)}}{I_j} \right]^2 \right]^{0.5} + \frac{GMD2_{j\cdot(j+4n-2)}}{I_j} \right] \\ \quad 0 \text{ otherwise} \\ sum2 \end{cases}$$

$$\text{if } (j+4\cdot n-2) \leq k$$

$$M2 := M2j + M2m - M2p$$

$$M2 := 6.2397\ nH$$

$$Ltt := L_o + M1 - M2$$

$$Ltt = 10.0232\ nH$$

$$Rsh := 0.03 \frac{ohm}{sq} \qquad \varepsilon r := 3.9 \qquad \varepsilon o := \frac{10^{-9}}{36 \cdot \pi} \qquad \rho si := 0.1\ ohm \cdot cm$$

$$hsi := 0.03\ cm \qquad hsio := 0.0003\ cm$$

$$Rsub_y := \frac{\rho si \cdot I_y}{w \cdot hsi}$$

$$R_p := \sum_{y=1}^{k} Rsub_y$$

$$Rs := \frac{length}{w} \cdot Rsh$$

$$Rs = 21.37\ ohms$$

$$Rp = 2.3744 \cdot 10^3\ ohms$$

$$Cp := \varepsilon o \varepsilon r \frac{w}{hsi}$$

$$Cp = 6.8967 \cdot 10^{-13}\ F$$

APPENDIX B: SUB-SYSTEM LAYOUTS

This appendix serves to provide the relevant layouts (as mentioned in chapter 5.)

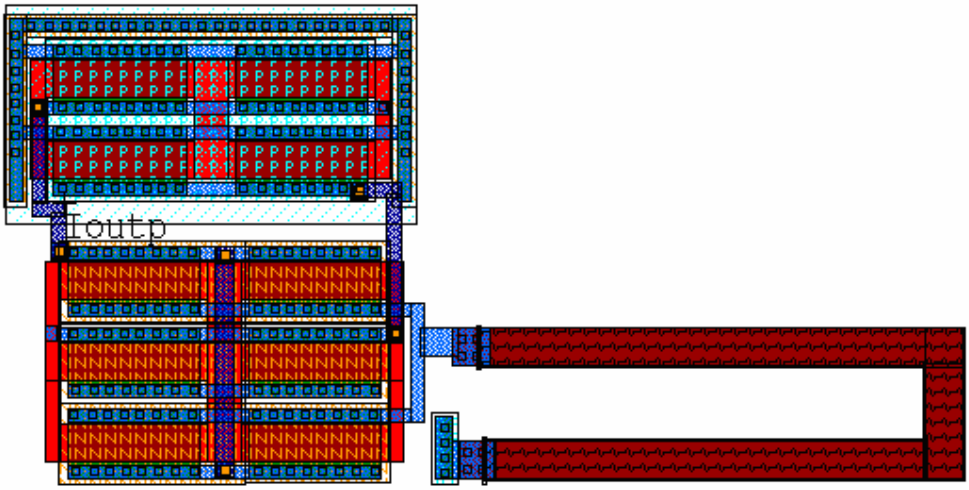

Figure B.1. The figure shows the charge pump layout.

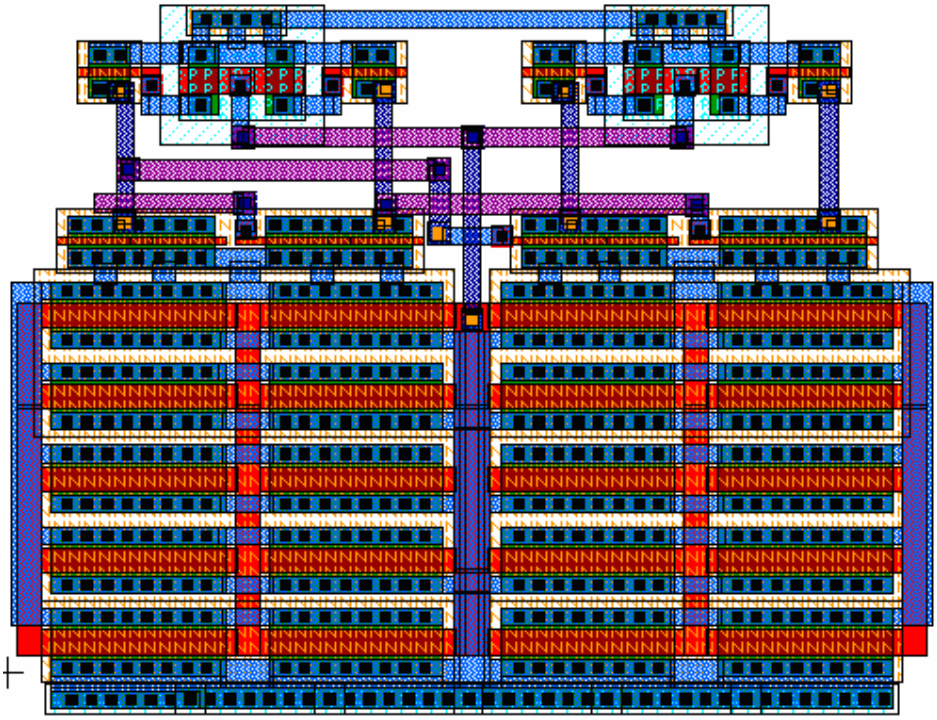

Figure B.2. The figure shows the phase detector layout.

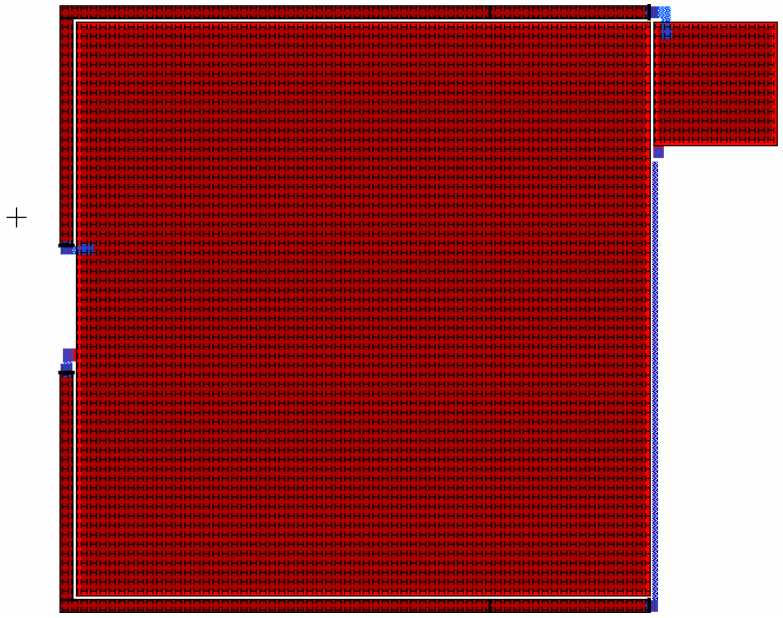

Figure B.3. The figure shows the loop filter layout.

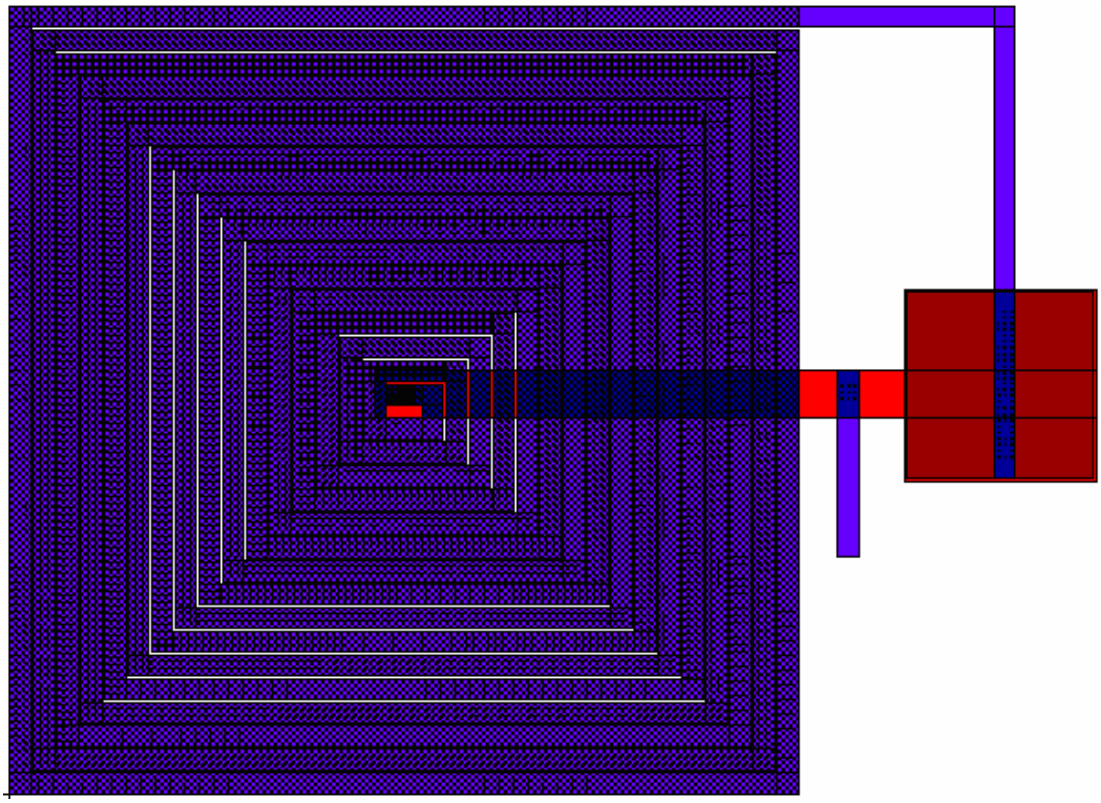

Figure B.4. The figure shows the LC oscillator tank circuit.

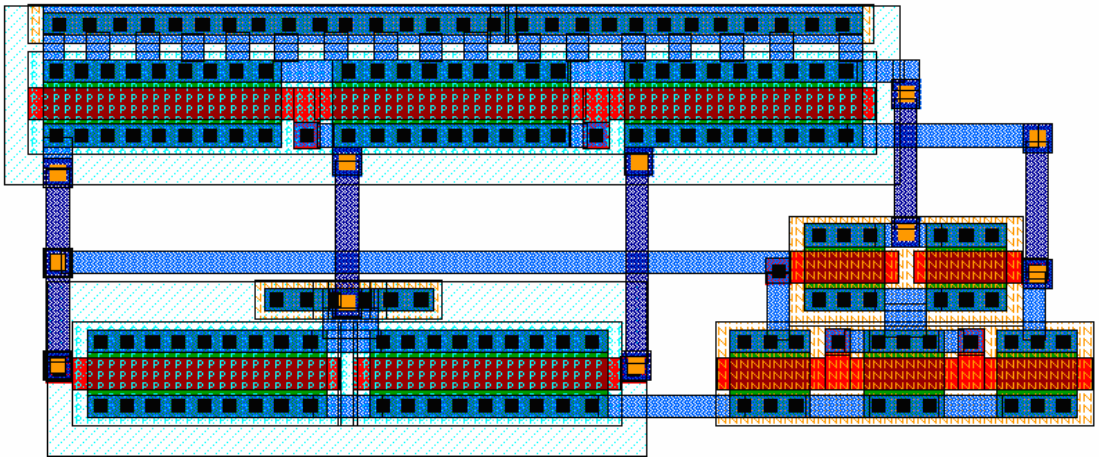

Figure B.5. The figure shows the fixed divider layout.

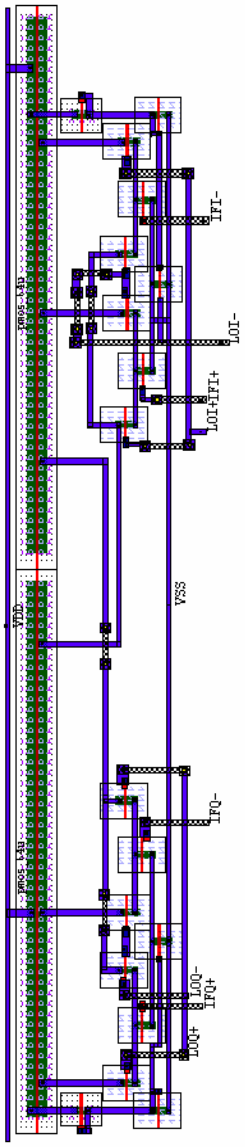

Figure B.6. The figure shows the SSB mixer layout.

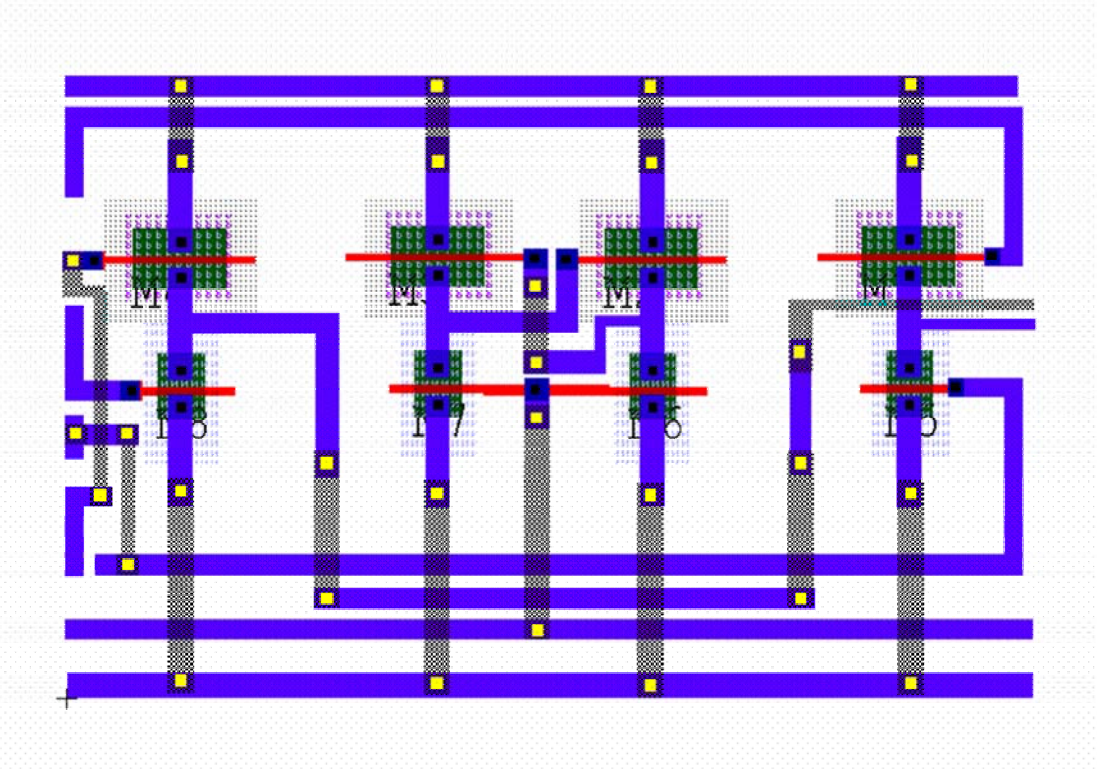

Figure B.7. The figure shows the ring oscillator layout.

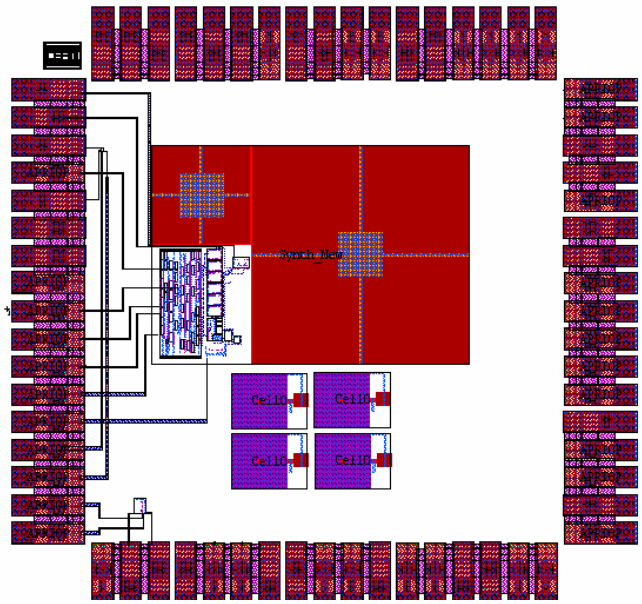

Figure B.8. The figure shows the complete synthesizer architecture.