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ORIGINAL RESEARCH

The effect of temperature variation on the transient response of RF PIN diode limiters for very high frequency applications

Cornelius Johannes Botha | **Tinus Stander**

Department of Electrical, Electronic, and Computer Engineering, University of Pretoria, Pretoria, South Africa

Correspondence

Cornelius Johannes Botha.
Email: u10690922@tuks.co.za

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Abstract

This work presents the effect of temperature change on the capacitance of silicon PIN diodes and the resulting change in performance of RF limiters at very high frequency (VHF). Device temperatures were varied between −25 ºC and 100 ºC, with small-signal parameters (including device capacitance) extracted at regular temperature increments and bias voltages from −20 Vdc to +3 Vdc using a multi-bias parameter extraction method. It was found that the junction capacitance of the four PIN diodes under investigation increases with temperature, as expected from carrier lifetime behaviour, while results also confirmed prior observations of an inverse relationship between forward-biased series resistance and temperature. Devices were subsequently tested in two different limiter topologies through high-power transient measurements. It was found that the combination of increased capacitance and decreased resistance with increasing temperature increases the transient spike leakage and decreases the flat leakage of a limiter. It was also concluded that, for VHF, an anti-parallel topology provides the best performance over a wide range of temperatures.

KEYWORDS

limiters, parameter estimation, p-i-n diodes, semiconductor device models

1 | INTRODUCTION

In modern communication systems, a single antenna is often used for both transmitting and receiving signals [1]. In high-power systems, such as very high frequency (VHF) radios used for military, signals can leak from the transmission path into the receiver path [2]. In other applications, such as mobile electronic warfare (EW) systems, a broadband receiver antenna is frequently found in very close proximity to a high-power transmitter antenna that occupies the same frequency spectrum [3]. A simplified superheterodyne communications receiver is shown in Figure 1. An RF limiter is a power attenuation device that is inserted between a source, such as an antenna, and sensitive components at the start of a receiver chain and is designed to prevent high-power signals from passing into the receiver, whilst allowing the receiver to function unprotected in the absence of such signals [2, 4–8]. The limiter has, since its invention in the 1960s, become a key component in modern receiver protector designs to provide electromagnetic protection to sensitive circuit components at the front-end of a receiver chain [4–6, 9–12].

Military communication and EW systems commonly use the VHF band (30–300 MHz) and are often used by personal and armoured vehicles that are deployed in harsh environments. Systems are exposed to extreme device temperatures during their service in the field. It is, therefore, critically important to understand performance variation due to ambient temperature variation.

PIN diodes, as depicted conceptually in Figure 2, are generally preferred to other solid-state alternatives such as Schottky diodes for RF limiters because of their power handling capability and slower response times (which ensures that solid-state switching follows the RF envelope rather than rectifying the RF signal). A PIN diode with a thick I-layer has more capacitance and a slower response and longer recovery time than a PIN diode with a thin I-layer but also has greater

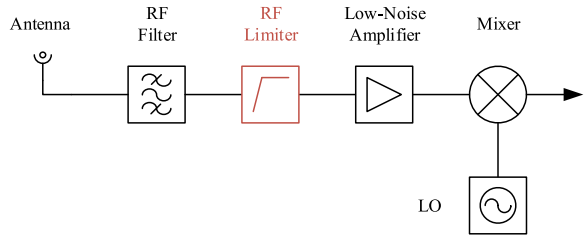

FIGURE 1 Simplified communications receiver.

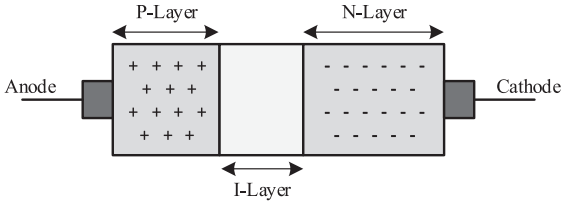

FIGURE 2 PIN diode layout.

power handling capability [13]. Studies that investigated the effect of ambient temperature on PIN diodes focused primarily on the change in diode resistance in the forward-bias state and at frequencies outside the VHF band [7, 8, 14–19], or changes due to self-heating rather than ambient variation [20]. It is, however, known that the spike leakage of a PIN diode limiter can be influenced by the response time of the PIN diode, as more energy can pass through the limiter before it provides sufficient limiting [3, 12]. Spike leakage is dependent on how fast a diode switches between the off and on state. The response time and recovery time of the PIN diode is directly related to the diode's carrier lifetime [1, 5, 11, 21], and the carrier lifetime is in turn influenced by temperature and the capacitance of the I-layer [8, 14, 22]. These effects are compounded in an overall response of higher transient spikes in diodes with thicker I-layers [23].

However, despite these known dependencies, there is no systemic study investigating the effect temperature has on the capacitance of PIN diodes and the resulting impact on a PIN diode limiter's transient performance, specifically for diodes in limiters used in applications that operate in the VHF band.

Recent literature on PIN diode and PIN diode limiters has focused on improved circuit or device design [24–26] (including integration with amplifiers [27, 28], filters [29, 30], or reflectionless balanced networks [31]), improved circuit modelling [32] or modelling by other means such as neural networks [33], the application of novel materials such as diamond [34], improved packaging [35–38], MMIC integration [39, 40], reliability studies [41], and advances in device modelling [42–45]. While the effect of incident power or pulse length [46] on self-heating of the device is often studied [47–51], as is changes in CW operation due to temperature variation [52–54], changes in transient behaviour due to ambient temperature variation are not. While spike leakage in VHF limiters was studied extensively in ref. [23], the impact of temperature on this leakage was not.

This paper aims to address this shortcoming in literature by providing, for the first time, explicit data on capacitance variation over temperature in PIN diodes, as well as studying the effect of temperature variation on the transient response of PIN diode-based limiters.

A brief review of a PIN diode's operation and known temperature dependencies is provided in Section 2. Section 3 outlines this work's methodology to PIN diode modelling, based on experimental measurements under temperature variation and presents the small-signal model variation of the selected PIN diodes at different bias points and temperatures. Section 4 presents the measurement setup and results of the transient operation at different temperatures, with the findings summarised in Section 5.

2 | REVIEW OF PIN DIODES AND MODELLING

While both the theory and techniques of PIN diodes and limiters are well-documented, a short overview is presented here for the sake of the later discussions.

2.1 | Review of structure and properties

PIN diodes can be considered as a bias-controlled variable resistor at RF and microwave frequencies [1, 6, 10, 55]. The P-layer (Figure 2) is a thin layer with low resistance and is heavily doped with p-type acceptor impurities (or holes), while the N-layer is heavily doped with n-type donor impurities (or electrons). The I-layer, or intrinsic layer, is an undoped layer containing very little impurities and, as a result, has a high resistivity. In commercial diodes, the intrinsic layer is rarely purely undoped but is often lightly doped with n-type impurities [1, 10, 11]. The I-layer can also be lightly doped with gold atoms to substantially reduce the minority carrier lifetime.

However, gold adds to the cost of the diode and increases the minimum resistance of the PIN diode [1].

The electrical characteristics of a PIN diode also depend significantly on the I-layer properties. These include the stored charge (which controls the resistance and capacitance), carrier lifetime (which governs the RF resistance and affects the response time, spike leakage, recovery time, and bandwidth), and power handling (through the thickness of the I-layer). For example, a PIN diode with a thick I-layer is expected to have high power handling capability but is too slow to be used in stand-alone RF limiter applications because of its long response time [7].

2.2 | Forward-biased equivalent circuit

A forward-biased PIN diode behaves as a current-controlled resistor that presents a linear resistance to the flow of RF current through the diode. It is this property that enables a PIN diode to be used as an RF power control element [55].

The equivalent circuit of a forward-biased, shunt-grounded, PIN diode is shown in Figure 3.

The only intrinsic steady-state diode property modelled is the forward-biased resistance, R_F, which is a function of the forward-bias current, I_F. The other parameters are the bond wire inductance and resistance, the package capacitances, and the diode grounding inductance, L_{paddle}. Package reactance have little effect on the diode's performance for frequencies below 1 GHz [7, 55].

2.3 | Reverse-biased equivalent circuit

The equivalent circuit of a reversed-biased diode in shunt configuration is shown in Figure 4, and consists of the shunt combination of diode capacitance, C_R, and diode resistance, R_R, in series with the parasitic inductance, L_{paddle}, which can also be neglected for frequencies below 1 GHz [7, 55].

C_R and R_R represent the reactance and net dissipative resistance of the depleted I-layer in the reverse-biased diode, respectively. C_R includes the junction capacitance, C_j. Similarly,

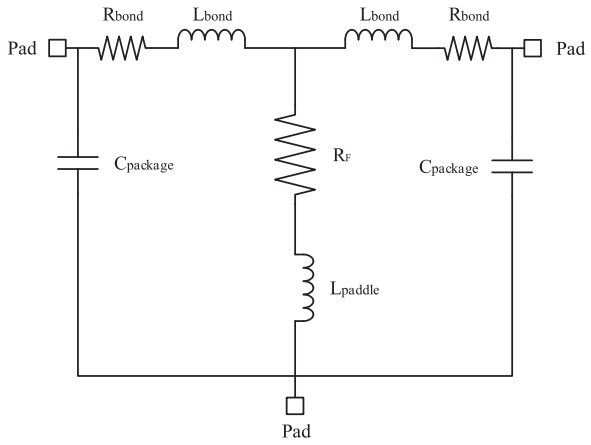

FIGURE 3 Forward-biased, shunt-grounded, PIN diode equivalent circuit. Adapted from [56].

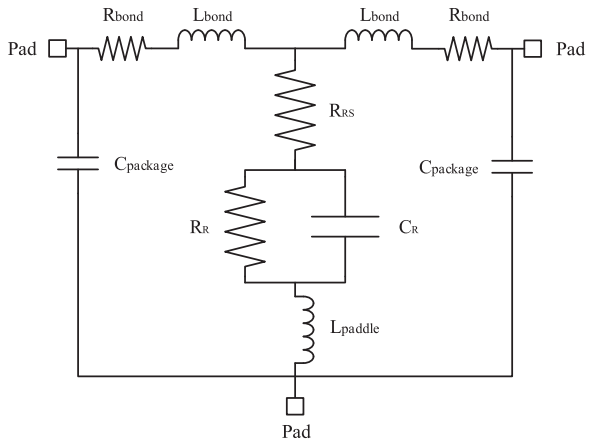

FIGURE 4 Reverse-biased PIN diode equivalent circuit. Adapted from [56].

the parallel resistance, R_R, is also affected by any series resistance in the semiconductor or diode contacts or package.

2.4 | Known thermal effects

Two main parameters of a PIN diode are strongly influenced by temperature, namely the I-layer ambipolar mobility, $\mu_a(T)$, and carrier lifetime, $\tau(T)$ [8, 14, 15]. Ambipolar mobility and carrier lifetime as a function of temperature are given as the following equations:

$$\mu_a(T) = \mu_a(T_{nom}) \left(\frac{T}{273 + T_{nom}}\right)^{-2.3} (°C), \quad (1)$$

and

$$\tau(T) = \tau(T_{nom}) \left(\frac{T}{273 + T_{nom}}\right)^{\tau_{coefficient}} (°C), \quad (2)$$

where $\mu a(T)$ is the ambipolar mobility as a function of temperature, $\tau(T)$ is the carrier lifetime as a function of temperature, T is the temperature in °C, T_{nom} is the ambient temperature in °C, T is the temperature in °C, and $\tau_{coefficient}$ is the carrier lifetime temperature coefficient.

Equation (2) shows that the carrier lifetime increases with increasing temperature, as confirmed in refs. [15] and [22], while $\tau_{coefficient}$ depends on the diode's surface passivation and I-layer capacitance [16], [19]. Ambipolar mobility in (1) decreases with increasing temperature [15].

Thermal capacitance is defined as the amount of energy required to raise the temperature of the I-layer of the diode by 1°C, in the absence of heat flow from the diode [1, 57]. Thermal capacitance is given by the following equation:

$$C_{Thermal} = \frac{\rho c_\theta}{V} (J/°C), \quad (3)$$

where $C_{Thermal}$ is the thermal capacitance in Joule per Celsius (J/°C), c_θ is the specific heat property of the diode material in cal/(g °C), ϱ is the density of the diode material in g/cm^3, and V is the volume of the I and N-layer.

Equation (3) suggests that a diode with a thick I-layer has greater heat capacitance and requires more energy to increase the temperature through self-heating.

Ambient temperature variations are expected to have less of an impact on diodes with thick I-layers, and more of an impact on diodes with a thin I-layer.

3 | SMALL-SIGNAL MODELLING AND MODEL VARIATION

To establish the effect of temperature change on device small-signal capacitance, it must first be extracted from temperature-varied small-signal S-parameter measurements of the PIN diode. The purpose of this test was to characterise each of the

PIN diodes in Table 1 individually by measuring the S-parameter data for each diode at different temperatures and bias voltages over a range of frequencies. Using the S-parameter data and through a parameter extraction process, the equivalent circuit models were determined.

3.1 | Measurement approach

The PIN diodes that were used for this study is given in Table 1. Four silicon PIN diodes from Skyworks Inc. were chosen to represent a selection of diodes with small, medium, and large I-layers, in terms of thickness. The PCB was manufactured on 0.5 mm thick Rogers RO4003C and devices fed by a grounded coplanar waveguide. A 30 mm launch distance was added to all the calibration standards and the DUT characterisation circuit to allow any higher-order modes from the connector to microstrip transition to attenuate.

The PIN diodes were soldered to the test fixture as shown in Figure 5. A Rohde & Schwarz ZNB20 vector network analyser was used, with the addition of a bench power supply and a digital multi-metre (Figure 6).

The small-signal measurement used a 5-point measurement average. An Agilent E3640A 20 V/1.5 A DC power supply and Keysight 34,465A digital multi-metre (Figure 6) were used to bias and measure the current through the DUT, respectively. The temperature range of interest (−25 °C to 100 °C) was divided into 25 °C intervals. A highly accelerated life test (HALT) chamber was used to control and vary the temperature to which the test jig was subjected. The measurement setup shown in Figure 7.

The test cables that were connected between the DUT inside the HALT chamber and the VNA on the outside would be subjected to changing temperature and were, therefore, selected for temperature stability. Multiple units of a specific PIN diode were available and were installed into the characterisation (Figure 5) and limiter circuits beforehand, therefore eliminating the need to move a single PIN diode between circuits.

The DC bias voltages were in 5 V steps from −20 V to −10 V, 1 V steps from −10 V to −1 V, and 0.1 V increments from −1 V to +3 V. This was done to achieve greater resolution in bias regions of fast model parameter variation. +3 V was selected as the maximum voltage because of the allowable current draw by the PIN diode through the VNA in the absence of a current-limiting resistor.

A two-tier calibration procedure was used. For the VNA cable calibration, the SOLT calibration standard was chosen, whereas TRM calibration standard was used to de-embed the test fixture. The SOLT calibration establishes a calibration plane at the outside of the HALT chamber where the temperature is constant, and the TRM calibration shifts the calibration plane to the inside of the HALT chamber and handles temperature variations (Figure 7). A two-tier approach was also done to allow large volumes of data to be captured in a reasonable amount of time.

3.2 | Circuit model parameter extraction

To investigate the effect of temperature variation on small-signal junction capacitance, the circuit model in Figure 4 can be fitted to measured reverse-biased small-signal parameters,

TABLE 1 PIN diode selection.

Diode name	I-layer thickness (μm)	C_j (pF)	Max CW (W)	Carrier lifetime, τ, (ns)
CLA4610	4.5	0.32 @ −6 V	8	20
CLA4608	7	0.6 @ −38 V	5	100
CLA4611	12	0.25 @ −38 V	10	300
CLA4609	20	0.6 @ −30 V	16	1100

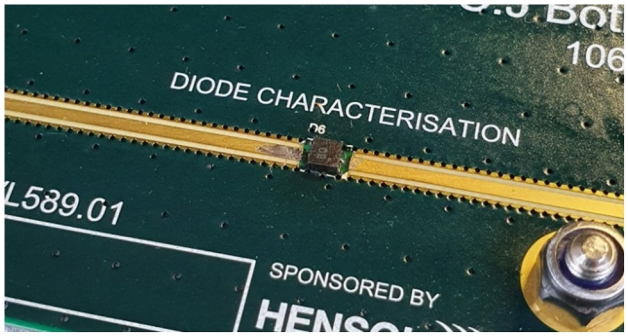

FIGURE 5 Test fixture with DUT.

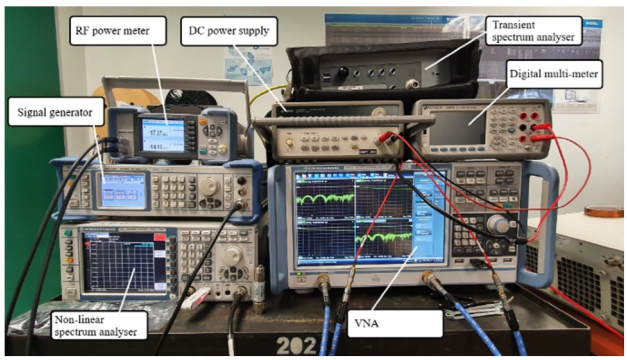

FIGURE 6 Measurement equipment.

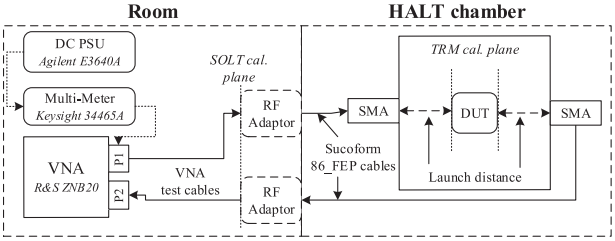

FIGURE 7 Small-signal measurement setup.

with some package parameters extracted using forward-biased measurements and the model in Figure 3. The equivalent T-circuit for both models can be presented as is shown in Figure 8.

The equivalent circuit neglects the effect of $C_{package}$. Parameters Z_1 and Z_2 represent the combined impedance of R_{bond} and L_{bond} in the series branch, whereas Y represents the admittance of the shunt branch. $C_{package}$ is neglected in the frequency range of interest.

The branch impedance and shunt admittance can be calculated from the ABCD parameters of the circuit using (4).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} (1+YZ_1) & (Z_1+Z_2+YZ_1Z_2) \\ Y & (1+YZ_2) \end{bmatrix}, \quad (4)$$

where the two-port ABCD parameters are calculated from the measured S-parameters.

Both direct-extraction and optimization-based algorithms for parameter extraction [58] must deal with the ill-conditioned nature of the extraction problem, which makes determining a unique equivalent model for a device challenging. This ill-conditioned behaviour of extraction is prevalent in parasitic elements such as lead or bond inductances, or package capacitances, due to the small effect they have on the measured data. Using a multi-bias approach that combines S-parameter data from multiple bias points into an integrated parameter extraction algorithm has demonstrated to be effective in extracting a distinctive set of model parameters [59]. In this study, the following heuristics are applied in extraction:

1. L_{padde}, R_{bond}, and L_{bond} are bias independent.
2. At low frequencies, C_R dominates the imaginary part of the shunt impedance.
3. When the PIN diode is forward biased, the junction capacitance in the shunt branch is negligible.
    1. At high frequencies, the shunt admittance is dominated by the reactance of L_{padde}.
    2. At low frequencies, the shunt impedance is dominated by R_F.

On the basis of these assumptions, the parameter extraction process started with the forward-biased model. Using the de-embedded S-parameter data, the forward-biased series and shunt branch impedances were calculated according to (4).

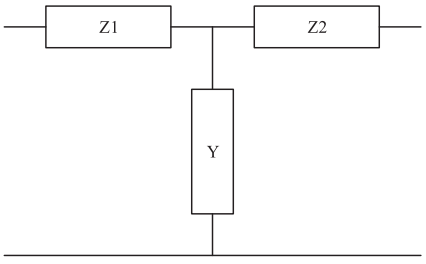

FIGURE 8 T-branch equivalent circuit.

The total shunt impedance for a forward-biased PIN diode at 3 V is given by (5), with the best-fit value of L_{paddle} extracted at the highest bias voltages using (6). The inductance was calculated at frequencies between 4000 and 6000 MHz where the inductive reactance is dominant.

$$Z_{3V} = R_F + j\omega L_{paddle} \quad (5)$$

$$L_{paddle} = \Im m(Z_{3V})/\omega \quad (6)$$

where Z_{3V} is the complex shunt impedance at 3V (Ω), and ω is the angular frequency.

The value of L_{paddle} was averaged across the three highest bias voltages to obtain a consistent value which was used as a constant to extract the value of reverse-biased parameters.

The total shunt impedance for a reverse-biased PIN diode is given by the following equation:

$$Z_R = R_{RS} + R_R \left\| \left(\frac{1}{j\omega C_R} \right) + j\omega L_{paddle}, \right. \quad (7)$$

where Z_R is the shunt impedance at a given reverse voltage (Ω), R_{RS} is the reverse-biased series resistance (Ω), R_R is the reverse-biased parallel resistance (Ω), C_R is the junction capacitance (pF), L_{paddle} is the previously calculated paddle inductance, and ω is the angular frequency.

Using the branch impedances, Z_1 and Z_2, the series resistance and inductance were calculated using the following equations:

$$Z_x = R_{bond} + j\omega L_{bond}, \quad (8)$$

$$R_{bond} = real(Z_x), \quad (9)$$

$$L_{bond} = \Im m(Z_x)/\omega, \quad (10)$$

where Z_x is the complex series branch impedance (Ω), and ω is the angular frequency.

3.3 | Reverse-biased capacitance versus temperature results

This section presents the capacitance versus temperature results for each diode and provides a comparison amongst the diodes and PIN diode models.

The variation of the capacitance, C_R, with temperature is shown in Figure 9, and would indicate a gradual increase with temperature. Table 2 summarises the results of Figure 9.

The nominal values of C_R correspond well with published datasheet values, featuring an irregular relationship between I-layer thickness and junction capacitance. The data would indicate that the diode with the thickest I-layer, CLA4609, exhibits less capacitance change over temperature than the diodes with a thinner I-layer thickness, as is suggested by (3), except for the CLA4610 diode. It is also interesting to note

that, for this device, most of the capacitance increase occurs between 75 °C and 100 °C.

3.4 | Reverse-biased resistance versus temperature results

The best-fit series resistance, R_{RS}, that was extracted at 0 V for various PIN diodes, is shown in Figure 10 and demonstrates a gradual increase in series resistance over increasing temperature.

The best-fit parallel resistance, R_R, extracted at 0 V versus temperature is shown in Figure 11. All the diodes show a sharp decrease in resistance from −25 °C to 100 °C, except for the CLA4609 diode which has a more gradual decline.

3.5 | Forward-biased resistance versus temperature results

The PIN diodes' forward resistance, R_F, at around 10 mA versus temperature is given in Figure 12 and would indicate that the diodes studied here have a carrier lifetime coefficient of greater than 2.3. The large variation in forward resistance below 0 °C could be due to inaccurate parameter extraction in a range where R_F is no longer expected to be a small value.

The change in resistance with temperature was discussed in a study by Caverly [15, 19], where it was shown that the forward-biased resistance of the PIN diode may increase ($\tau_{\text{coefficient}} < 2.3$), decrease ($\tau_{\text{coefficient}} > 2.3$), or remain constant ($\tau_{\text{coefficient}} = 2.3$) over temperature. While the manufacturer of the DUTs included in this study does not provide the required information to calculate the carrier lifetime temperature coefficient, the results shown in Figure 12 would indicate that the diodes studied here have a carrier lifetime temperature coefficient of greater than 2.3. This can further and readily be explained by decreased scattering due to an increase in lattice phonons, increased carrier mobility and decreased bandgap [51].

3.6 | Package parasitics versus temperature results

The branch inductance, Z_1 and Z_2 shown in Figure 8, versus temperature for each diode is shown in Figure 13. The results show a slight increase in bond-wire inductance, likely due to minor temperature elongation of the bond wire length.

The diodes' best-fit paddle inductance, L_{paddle}, extracted at the highest bias voltages using (6) is shown in Figure 14. The results show a negligible increase in inductance with increasing temperature. Differences in inductance between diodes, which were also observed in Figure 13, are likely due to small variations in the amount of solder used during installation.

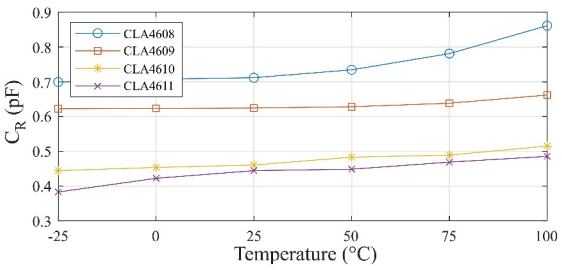

FIGURE 9 Capacitance versus temperature comparison at 0 V.

TABLE 2 Summarised change in capacitance per diode at 0 V.

PIN diode	I-layer thickness (μm)	C_R at −25 °C (pF)	C_R at 100 °C (pF)	$\frac{\Delta C_R}{125\ °C}$ (pF)
CLA4610	4.5	0.4448	0.5152	0.0704
CLA4608	7	0.6995	0.8615	0.162
CLA4611	12	0.3834	0.4856	0.1022
CLA4609	20	0.6229	0.662	0.0391

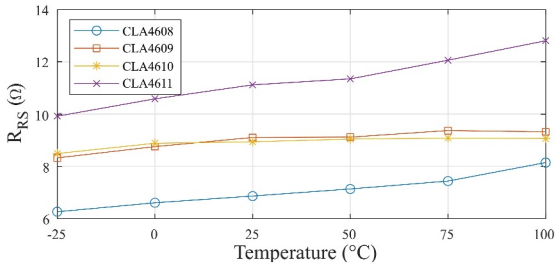

FIGURE 10 Series resistance versus temperature at 0 V.

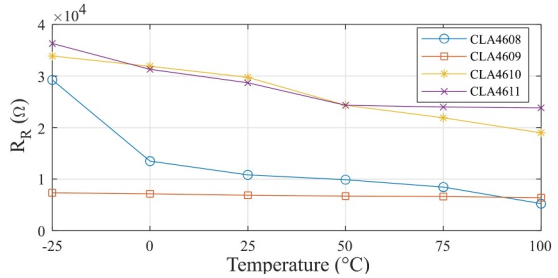

FIGURE 11 Parallel resistance versus temperature at 0 V.

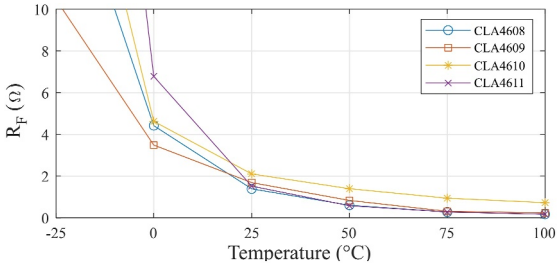

FIGURE 12 Forward resistance versus temperature at around 10 mA.

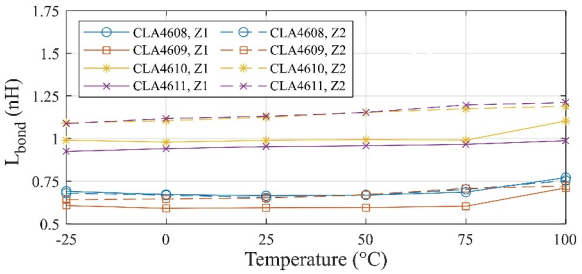

FIGURE 13 Branch inductance versus temperature at 3 V.

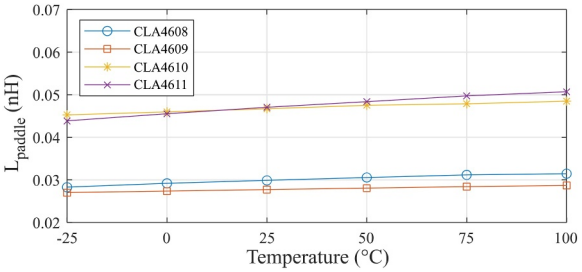

FIGURE 14 Paddle inductance versus temperature at 3 V.

4 | PIN DIODE LIMITER TRANSIENT CHARACTERISATION

This section presents the measurement setup and transient responses of each limiter topology at different frequencies and temperatures. The small-signal model discussed in Section 3 provides, conceptually, a good baseline for how a diode's capacitance will change with increasing temperature. Although the specific capacitance values may differ between the small-signal and large signal models, the trends over temperature can reasonably be expected to correspond and are used here to compare transient measurements.

From the discussion in Section 3, it is expected that the change in capacitance, C_R, and forward resistance, R_F, due to temperature will affect the transient response of a limiter in terms of the limiter's spike and flat leakage, since the flat leakage is dependent on how small the forward resistance of the diode becomes during its on state, whereas the spike leakage is dependent on the carrier lifetime, which is in turn influenced by temperature and the capacitance of the I-layer [8, 14, 22].

4.1 | Circuits under test

Two PIN diode limiter topologies were chosen to evaluate the effect of temperature variation on PIN-diode limiter response, namely the traditional PIN diode limiter, and the anti-parallel limiter. The traditional PIN diode limiter (Figure 15) is the simplest type of PIN diode-based limiter and is frequently featured in component datasheets.

The anti-parallel limiter circuit (Figure 16) does not require a DC bias choke and has been shown to have improved performance compared to the traditional limiter topology [60].

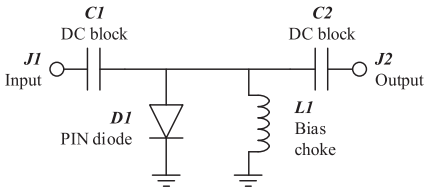

FIGURE 15 Traditional limiter circuit topology.

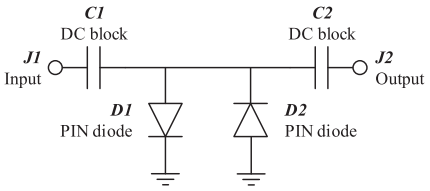

FIGURE 16 Anti-parallel limiter circuit topology.

The results for the CLA4608 and CLA4609 diodes are presented, as they provide variety in intrinsic layer width (7 vs. 20 μm) and carrier lifetime (100 vs. 1100 ns).

4.2 | Measurement setup

The purpose of this measurement was to measure the spike and flat leakage of the PIN diode limiter through transient analysis at different temperatures. The measurement setup is shown in Figure 17.

A pulse generator (Figure 18) was used to produce pulsed RF signals at 100 and 300 MHz, amplified to 100 W peak signal using a power amplifier. The results at 100 and 300 MHz are presented in Tables 3 and 4 in the following section. The limiter's response was measured using an Anritsu MS2090 A handheld spectrum analyser (Figure 6) configured in the zero-span (time domain) mode.

4.3 | Traditional limiter measurement results

Figure 19 shows the transient response for the traditional limiter using the CLA4608 and CLA4609 PIN diodes at 100 MHz at different temperatures.

For the CLA4608 diode, the results show a 0.7 dB decrease in the flat leakage from −25 °C to 100 °C. For the CLA4609 PIN diode, the limiter's flat leakage decreases with increasing temperature due to a decrease in the series resistance at higher temperatures shown in Figure 12. The results show a decrease in the flat leakage of around 0.6 dB from−25°C to 100°C.

The limiter's change in spike leakage with temperature shows that, at 100 MHz, the magnitude of the spike increases by approximately 1.2 dB from −25 °C to 100 °C for the CLA4608 diode, which, in combination with the decreasing flat leakage, increases the spike leakage. For the CLA4609 diode, the results show a significantly more pronounced (3.1 dB) increase in the spike magnitude, as well as a longer spike

duration, over increasing temperature. These increases can be attributed to the increase in the diode's carrier lifetime, which is influenced by temperature and the increase in capacitance of the I-layer, as was shown in Figure 9.

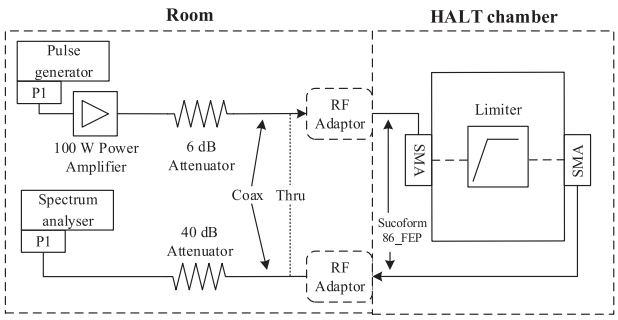

FIGURE 17 Limiter transient measurement setup.

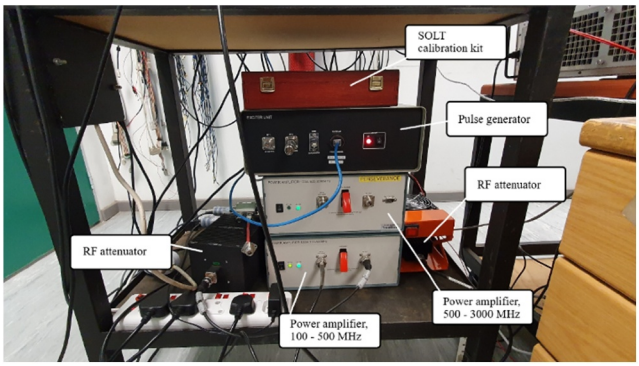

FIGURE 18 Transient measurement equipment.

4.4 | Anti-parallel limiter measurement results

Figure 20 show the transient response of the anti-parallel limiter with the CLA4608 and CLA4609 PIN diodes at 100 MHz for different temperatures.

Like the results in Figure 19, the anti-parallel limiter with the CLA4608 diode also exhibits a decrease in the flat leakage of about 0.6 dB from - 25°C to 100°C, whereas the response for the CLA4609 diode shows that the limiter's flat leakage decreases marginally with increasing temperature, with the results showing a decrease in the flat leakage of around 0.14 dB from −25 °C to 100 °C. An increase in both the magnitude and duration of the spike in the case of the CLA4609 diode is also observed, with the spike magnitude increasing by 6.8 dB from −25 °C to 100 °C.

The CLA4608 diode, with its thinner I-layer, was fast enough to respond to the incident RF pulse and did not present any significant spike leakage.

4.5 | Results summary

Table 3 shows a summary of the traditional limiter's performance at 100 and 300 MHz using the two different PIN diodes. The table shows a clear trend of increasing spike leakage and near-constant flat leakage with increasing temperature. The increase in spike leakage is more severe with the larger, CLA4609 PIN diode, at 100 MHz.

A summary of the anti-parallel limiter's performance at 100 and 300 MHz is given in Table 4. As was the case with the CLA4609 diode in the traditional limiter topology, the table

TABLE 3 Traditional limiter PIN diode comparison at 100 and 300 MHz.

		Spike leakage (nJ)		Flat leakage (dBm)	
Temp. (°C)	Freq. (MHz)	CLA 4608	CLA 4609	CLA 4608	CLA 4609
−25	100	0.1	24.33	15.17	16.7
25		0.12	48.24	15.33	16.28
100		0.17	83.75	14.46	16.1
−25	300	0.54	0	15.33	17.96
25		0.59	0	15.35	18.07
100		0.66	0	14.73	18.36

TABLE 4 Anti-parallel limiter PIN diode comparison at 100 and 300 MHz.

		Spike leakage (nJ)		Flat leakage (dBm)	
Temp. (°C)	Freq. (MHz)	CLA 4608	CLA4609	CLA 4608	CLA 4609
−25	100	0.01	12.93	14.55	16.1
25		0	30.27	14.1	15.94
100		0	97.9	13.49	15.96
−25	300	0.18	0.76	13.98	19.04
25		0.25	0.24	13.57	18.31
100		0.49	0.19	12.28	18.1

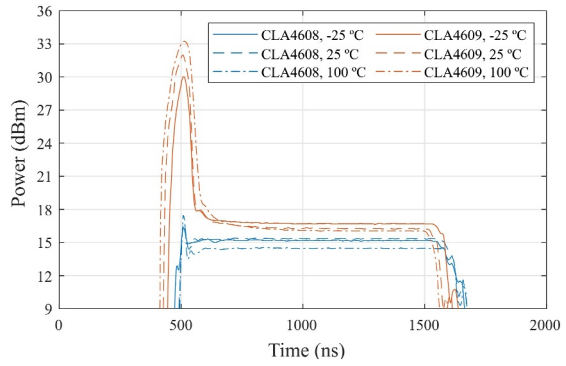

FIGURE 19 Traditional limiter's transient response versus temperature with CLA4608 and CLA4609 PIN diodes at 100 MHz.

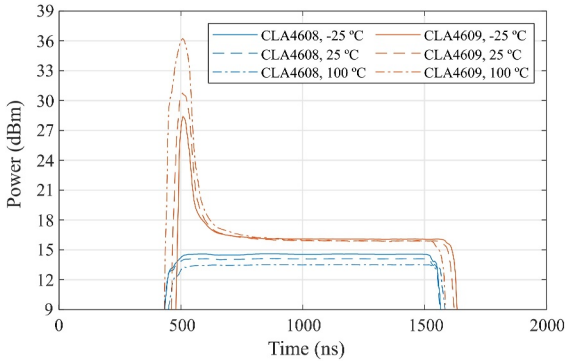

FIGURE 20 Anti-parallel limiter's transient response versus temperature with CLA4608 and CLA4609 PIN diodes at 100 MHz.

shows a clear trend of increasing spike leakage with increasing temperature at 100 MHz. This can be attributed to the increase in the diode's carrier lifetime which is influenced by temperature and the increase in capacitance of the I-layer, as was shown in Figure 9. The results further show a small decrease in the flat leakage at both frequencies for both diodes.

5 | CONCLUSION

This work presented, for the first time, explicit data on capacitance variation over temperature for silicon PIN diodes and studied the effect of temperature variation on the transient response of PIN diode-based limiters.

It is evident from Figure 9 that a PIN diode's capacitance, C_R, increases with temperature between −25 °C and 100 °C, mirroring the effect of temperature on capacitance in Schottky photodiodes [61]. The measured data also supports (3), which suggests that temperature variations will have less of an impact on diodes with thick I-layers, and more of an impact on diodes with a thin I-layer. The reverse-biased resistance results showed a gradual increase in series resistance series, R_{RS}, with temperature, where the parallel resistance, R_R, showed a sharp decrease in resistance with increasing temperature. It was also found that the forward-bias series resistance, R_F, decreases with temperature. It is concluded that the measured diodes have a carrier lifetime temperature coefficient, $\tau_{coefficient}$, of greater than 2.3, which is indicative of a negative resistance coefficient.

The transient results showed that the flat leakage decreases with increasing temperature for both the traditional and anti-parallel limiter topologies operating at VHF, while the spike leakage increases. The decrease in flat leakage with increasing temperature is due to the decrease in the forward-biased resistance that was shown in Figure 12. The increase in spike leakage with increasing temperature, a novel experimental observation of this work, can be attributed to the increase in the diode's carrier lifetime, which is influenced by temperature and the increase in capacitance of the I-layer. This observation is supported by the small-signal characteristics in Figures 9 and 12, where it is shown that C_R increases with increasing temperature, while R_F decreases. It can further be concluded that the increase in spike leakage at higher temperatures correlates with increasing device capacitance as influenced by carrier lifetime.

The increase in spike leakage was found to be more severe with the thicker CLA4609 PIN diode, which showed far greater spike leakage compared to the other diodes at 100 MHz. This can be attributed to the CLA4609 diode's increased carrier lifetime compared to the smaller CLA4608 diode, which is due to its thickness (20 μm compared to 7 μm). The result agrees with prior studies that found that diodes with a thin I-layer (less junction capacitance) have little spike leakage and that thick I-layer diodes (more junction capacitance) have much more spike leakage [13]. As discussed in Section II, the response time of the PIN diode is directly related to the diode's carrier lifetime, and the carrier lifetime is in turn influenced by temperature and the capacitance of the I-layer [11, 23].

Future work will extend the frequency range of the study to include X-band frequencies (8–12 GHz) or even 2–18 GHz for EW applications, building on a distributed multi-stage topology as shown in refs. [26] or [62]. This study will also be replicated for microelectronic integrated limiters, incorporating a wider variety of limiter topologies.

We further propose to extend the comparison of the single and anti-parallel diode topologies to other performance parameters, such as operating bandwidth, building on the prior work in ref. [63].

AUTHOR CONTRIBUTION

Cornelius Johannes Botha: Detail design, software development, experimentation, data curation, writing–original draft & editing. Prof. Tinus Stander: Conceptualisation, funding acquisition, supervision, writing–review & editing.

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CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

Data available on request from the authors.

ORCID

Cornelius Johannes Botha https://orcid.org/0009-0004-6089-9852

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