A novel CMOS Hall effect sensor

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Abstract

This paper reports on a new technique for sensing the Hall effect in an integrated CMOS device. Contrary to traditional Hall plates where sensor contacts comprise of highly doped, low ohmic contacts, the proposed sensor makes use of a parasitic vertical pnp bipolar junction transistor (BJT) to sense and amplify the Hall current caused by the Lorentz force in the presence of a perpendicular magnetic field. The Hall effect appears as a current through the emitter of the BJT. The BJT forward gain implies a direct gain of at least β+1 in the measured signal in comparison to traditional methods.

Keywords

Hall effect, CMOS, Hall current

1. Introduction

The state of the art method of sensing the Hall effect in Hall plate devices is through the use of highly doped low ohmic contacts [1, 2, 3, 4, 5, 6, 7, 8]. This method of sensing is primarily associated with the Hall voltage which in silicon can be very limited in magnitude. A typical silicon Hall plate has a sensitivity of 0.07 T^{-1} for both voltage mode and current mode of operation [9], and since the Hall voltage scales linearly with the applied DC voltage bias and magnetic field, this relates to a typical signal in the order of 25 mV at a DC bias of 1.7 V and a magnetic field of 200 mT. Taking the geometrical factor into account for a square plate, this signal can diminish further by up to 30 % in magnitude [9]. Replacing the n+ sense contacts in the n-well with p-type implants results in a parasitic pnp BJT formed vertically downward to the substrate through which the Hall current can be effectively measured, very similar to the BJT's used in a CMOS bandgap circuit [10]. This allows for a very simple measuring technique with built-in gain when compared to complex traditional amplification such as instrumentation amplifiers. . As CMOS technologies scale down to smaller geometries, combined with the high biasing voltages and currents required to maximise Hall sensitivities, traditional Hall plates are progressing toward the velocity saturation limits and increased Joule heating. For large geometries this is normally no problem but for µ-Hall devices this becomes a limiting factor [11]. For silicon velocity saturation occurs at approximately 30 $kVcm^{-1}$ and this corresponds to a minimum length of 1.5 µm for a voltage bias of 5 V [9]. In contrast with traditional sensing techniques which require high supply voltages, the technique is capable of attaining a wide dynamic range at very low supply voltages and hence can be applied in low power devices.

Our novel sensing circuit will induce substrate currents through the collector terminals of the vertical pnp BJT's and may require well-known layout techniques to avoid undesired latch up effects. Transistor mismatches, especially pnp transistor beta mismatches on chip, may require DC offset trimming techniques similar to that used in operational amplifier input stage designs.

This paper begins with a brief summary of the Hall effect physics applicable to the proposed design after which the Hall plate design, layout, experimental procedure and results are explained. The effect of noise and other limitations are then discussed followed by the concluding remarks and suggestions for further research on the topic.

2. The Hall effect

2.1 Hall voltage in long and short geometries

Fig. 1 illustrates a typical a) long and b) short Hall plate with dimensions length = *l*, width = *w* and thickness = *t* and four contacts at its boundaries, with *l* >> *w* for the long device and *l* << *w* for the short device. The long geometry in a) is very similar to the 2 × 9 cm sample used by Hall in his original experiment [12].

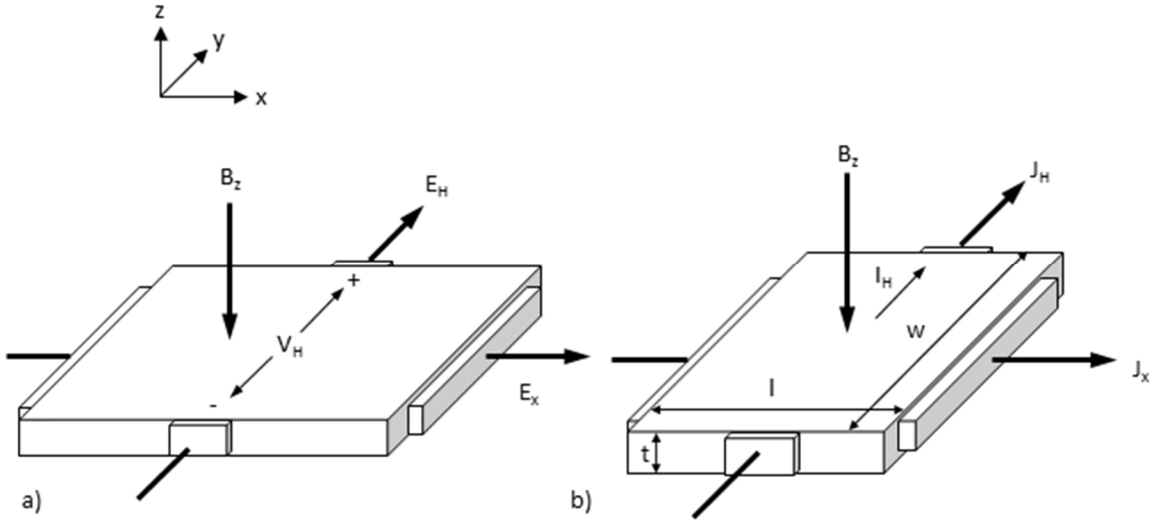

Fig. 1 Hall effect in a) long and b) short samples with applied electric field E_x or current density vector J_x, Hall electric field E_H or Hall current density vector J_H, magnetic field B_z, width *w*, length *l*, thickness *t* with resultant a) Hall voltage V_H or b) Hall current I_H

The Hall voltage and current deflection illustrated in Fig. 1 is a direct result of the Lorentz force. A Hall voltage occurs due to the boundaries of the long sample constraining the current flow down the length whilst in the short sample current deflection occurs as the current exits the sample without any boundary interaction. The resulting electric field opposing this force is given [9] by:

$$\boldsymbol{E}_H = \mu[\boldsymbol{E}_x \times \boldsymbol{B}_z] \qquad (1)$$

where $\boldsymbol{E}_H$ denotes the Hall electric field, μ the majority charge carrier mobility, $\boldsymbol{E}_x$ the externally applied electric field resulting from the voltage bias and $\boldsymbol{B}_z$, the perpendicular magnetic induction.

The Hall voltage V_H for a constant voltage bias in the long sample in Fig. 1 a) is given by [9]:

$$V_H = \mu \frac{w}{l} G_H V_{bias} B_\perp \qquad (2)$$

with G_H the geometrical correction factor, V_{bias} the voltage supplied to the plate and $B_\perp$ the perpendicular magnetic field. It can be seen from Eq. (2) that the Hall voltage is proportional to the voltage supplied as well as the intensity of the perpendicular magnetic field. Similarly then, the Hall current I_H for the short sample in Fig. 1 b) can be written [9] as:

$$I_H = \mu \frac{w}{l} G_H I_{bias} B_\perp \qquad (3)$$

and describes the transverse current due to the Hall effect with I_{bias} the Hall plate biasing current.

2.2 Offset

Probably one of the most studied Hall device characteristics is the offset usually described in terms of the offset Hall voltage V_{off} or offset Hall current I_{off}, or expressed in terms of an equivalent magnetic field offset B_{off}. B_{off} can be derived from the offset voltage or current in terms of the absolute sensitivity S_A with units VT^{-1} for a voltage mode operation and AT^{-1} for current mode operation as shown in (4):

$$B_{off} = \frac{V_{off}}{S_A} \quad \text{and} \quad B_{off} = \frac{I_{off}}{S_A}. \qquad (4)$$

The offset is one of the major deviations observed in a Hall device and is the DC signal measured in the absence of a magnetic field and thus cannot be distinguished from the quasi-static signal of interest [9]. Typically the offset as well as the offset drift of a conventional Hall plate is somewhat larger than the Earth's magnetic field [13]. The main causes for the appearance of an offset are process gradients across the chip, misalignment of masks and/or mechanical stresses resulting from fabrication as well as packaging [14, 15, 16, 17] and can also vary due to supply voltage and temperature [18]. Whereas absolute sensitivity S_A above describes how much the output of a sensor will change given a specific magnetic field input, the relative sensitivity is defined as the ratio between the absolute sensitivity and a bias quantity for the Hall voltage and current mode and is given [9] by:

$$S_{AV} = \mu \frac{w}{l} G_H V_{bias} \quad \text{and} \quad S_{AI} = \mu \frac{w}{l} G_H I_{bias}. \qquad (5)$$

Substituting (5) into (4) shows that the higher the mobility, the lower the equivalent offset. For a typical Hall plate in silicon with $l/w \approx 1$, an offset in the range of $B_{off} \approx 10$ mT can be expected [19].

2.3 Geometrical correction factor

The geometrical factor for a point contact rectangular Hall device can be approximated [9] by:

$$G_H \cong 1 - \frac{16}{\pi^2} e^{\left(-\frac{\pi l}{2w}\right)} \left[1 - \frac{8}{9} e^{\left(-\frac{\pi l}{2w}\right)}\right] \left(1 - \frac{\theta_H^2}{3}\right). \qquad (6)$$

Eq. (6) is true for $0.85 \leq l/w \leq \infty$ and $0 \leq \theta_H \leq 0.45$ with θ_H in radians. The Hall angle θ_H is given [9] by:

$$\tan \theta_H = \mu B. \qquad (7)$$

3. Design

Fig. 2 illustrates a cross section and top view of an n-well CMOS Hall plate. The cross section is shown midway along the length of the device. The vertical BJT forming between the p-type contacts in the n-well, through the n-well to the substrate can clearly be visualized. As can be seen in the figure, the base of the vertical pnp transistor is formed by the n-well and can be contacted by n+ contacts. Furthermore, all the vertical pnp transistors share a common collector, namely the p-type substrate.

It should be noted that a substrate current will flow through resistors R_{c1} and R_{c2} , and in order to prevent any problems like latch-up to occur as a result of voltages generated within the substrate, wide p+ substrate contacts should be placed as close to the p+ emitters as possible, as shown in the top view of the figure. It is possible to bias the Hall device such that the BJT becomes forward biased in the active region and in doing so, activate the inherent current gain of the transistor to amplify the Hall current into a useful signal via the emitters of the BJT.

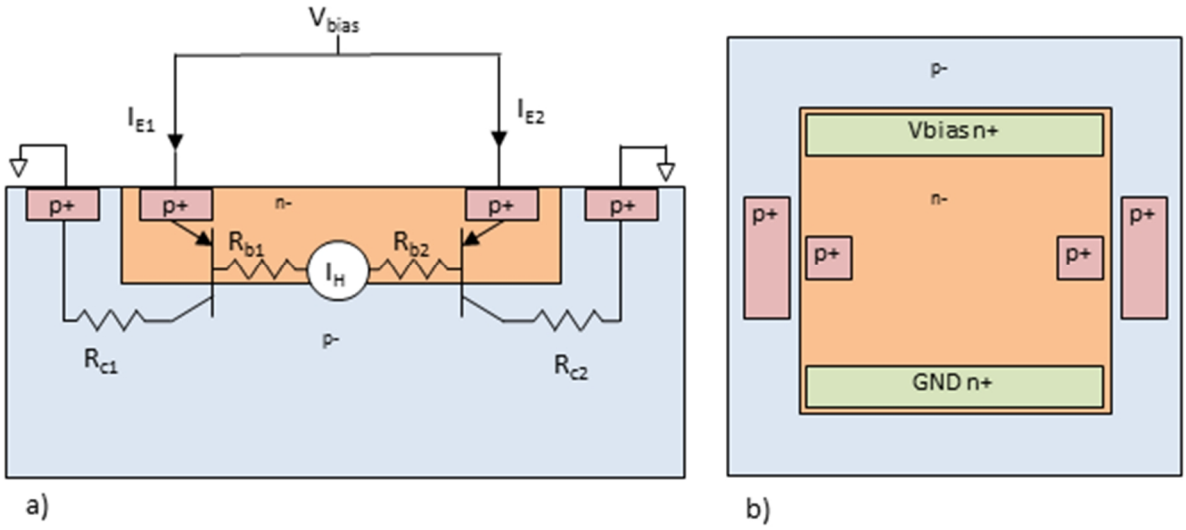

Fig. 2 (a) Cross section and (b) top view of n-well Hall plate showing the presence of the parasitic vertical BJT between the p-type node p+ forming the emitter, the n-well n- forming the base and the substrate p- forming the collector. I_E denotes the emitter current, I_H the Hall current and R_{b1}, R_{b2}, R_{c1} and R_{c2} the relevant parasitic resistances

Fig. 3 shows a schematic representation of the Hall plate which can also be used as a first order simulation model. The Hall current I_H is modelled as a current source whilst the Hall plate offset is modelled by adjusting R_d which represents the mismatch that occurs in the plate resistance R_{s1} and R_{s2} and ultimately the zero magnetic field Hall current. Under ideal conditions, $R_{s1} = R_{s2} = R_S$. Typically in the technology used in this study, it was found that R_d was in the order of 0.2% of R_S which translates to approximately 2 Ω. V_{bias} is used to set up the bias current I_{bias} through the Hall plate causing a voltage drop of V_{EB} across both R_{s1} resistors. For relatively low bias currents and magnetic fields, the voltages V_{Rs1} and V_{Rs2} across R_{s1} and R_{s2} will be equal and the base resistance will have a very small impact on the emitter Hall current. If however V_{bias} increases to such extent that $V_{bias}/2$ exceeds the forward voltage of the base emitter junction V_{EB}, the voltage across R_{s2} will increase at a faster rate than the voltage across R_{s1} and will become a source of non-linearity. Ideally I_B should be kept very small, such that the current through R_{s1} and R_{s2} are approximately equal. R_{c1} and R_{c2} can be minimized through proper layout design of the BJT. Biasing the transistors requires that the base to emitter voltage $|V_{BE}|$ be greater than 0 V with a biasing voltage V_{bias} across the Hall plate as given in Eq. (8) and thus:

$$V_{bias} \approx 2V_{BE} \approx 2V_{Rs1} \approx 2V_{Rs2}. \qquad (8)$$

Keeping V_{bias} as low as possible also reduces the consumed power and hence also the Joule heating in the Hall plate and is one of the major advantages of this technique. This does however come at the expense of sensitivity. Fig. 4 shows both the pnp transistor's forward voltage $|V_{BE}|$ and gain β versus the collector current I_C characteristics as simulated from foundry data. It can be seen that a collector current as low as 1 nA is sufficient to bias the transistor enough to get stable current gain. As the main aim was to illustrate a proof of concept, biasing the emitter at the same V_{bias} greatly simplified the setup. For this experiment, this bias point is indicated in Fig. 4 by the dotted black line

at approximately 2 mA. From Fig. 4 it can also be seen that the ideal biasing conditions for the Hall device would be for a collector current between 1 nA and 100 µA. This range yields a stable current gain factor Beta over many decades of collector current and will also yield a decrease in inter-chip variation as well as lower temperature dependencies.

Using the setup shown in Fig. 3 with V_{bias} = 1.7 V, the Beta for each BJT was calculated by measuring the emitter and collector current separately. The base current and hence the BJT's Beta could be deduced.

Table 1 below shows the measured Betas for ten samples used in this experiment which consist of the average of both BJT's per plate. It can be seen that the inter-chip variation is relatively good, matching within approximately ± 2.5%. This mismatch will however be larger between wafers and batches.

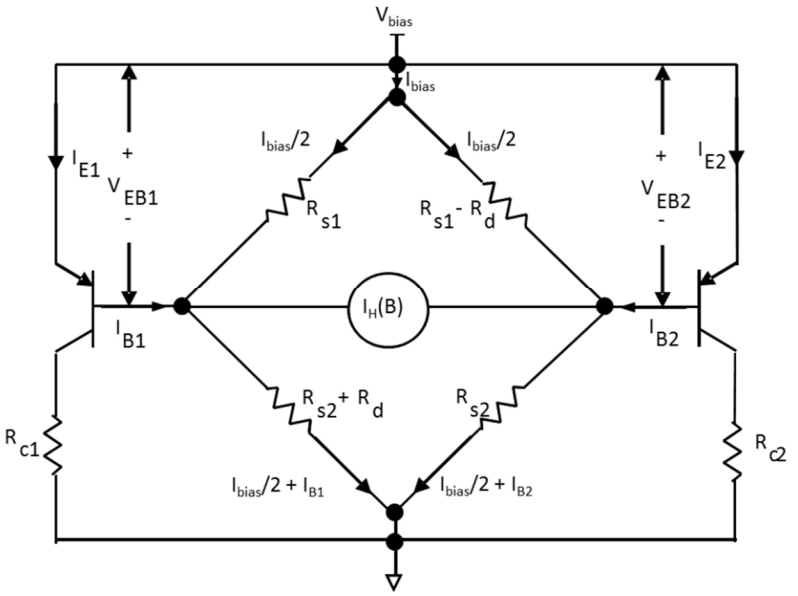

Fig. 3 Schematic representation of the Hall plate with integrated pnp transistors. I_{E1} and I_{E2} denotes the emitter current, I_{B1} and I_{B2} the base current, $I_H(B)$ the Hall current, R_{c1} and R_{c2} the collect parasitic resistances, R_{s1} and R_{s2} the Hall plate resistance, R_d the deviation component of the Hall plate resistance for modelling the offset effects, V_{EB1} and V_{EB2} the emitter to base voltages, V_{bias} the bias voltage and I_{bias} the resulting bias current through the Hall plate

Table 1 Summary of the measured vertical BJT emitter current I_E and collector current I_C used to calculate the forward gain β for a V_{CE} of 1.7 V

Device number	I_E (mA)	I_C (mA)	Calculated β
1	2.251	1.688	2.998
2	2.237	1.667	2.925
3	2.218	1.653	2.926
4	2.306	1.740	3.074
5	2.269	1.702	3.002
6	2.248	1.683	2.979
7	2.244	1.678	2.965
8	2.269	1.706	3.030
9	2.234	1.669	2.954
10	2.226	1.668	2.989
Average	2.250	1.685	2.984

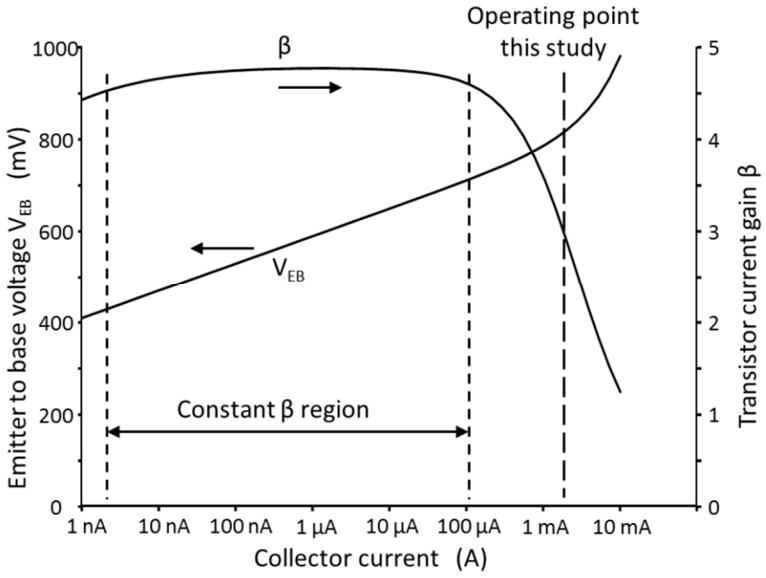

Fig. 4 BJT forward current gain β and forward base emitter voltage V_{EB} as a function of the collector current I_C for a similar sized BJT as modelled by the foundry

As we are most interested in how the emitter current translates into a measurable Hall effect parameter, it will be necessary to relate the emitter currents I_{E1} *and* I_{E2} to the effective Hall current ΔI_{EH} by measuring the difference between the emitter currents and is given by:

$$\Delta I_{EH} = I_{E1} - I_{E2}. \quad (9)$$

Rewriting ΔI_{EH} as a function of the base currents I_{B1} and I_{B2} results in:

$$\Delta I_{EH} = (\beta + 1)(I_{B1} - I_{B2}) \quad (10)$$

with β the forward current gain as defined in the technological electrical parameters. The potential gain this method offers is quite significant especially in more sophisticated technologies such as BiCMOS processes where a much higher β may be achievable.

4. Hall plate design

4.1 Hall effect characteristics

A standard Hall plate with an area of 100 µm × 100 µm was planned as a test structure based on the technological parameters of the 0.35 µm CMOS technology. Substituting these technological parameters into Eq. (2) through (7), it was possible to determine the expected theoretical performance of the plate. A summary of the expected performance of the plate at the proposed bias voltage of V_{bias} = 1.7 V can be seen in Table 2 against which the Hall plate performance could be compared.

Table 2 Summary of calculated Hall plate parameters @ V_{bias} = 1.7 V based on CMOS technology specifications

Parameter	Calculated	Unit
B_{max}	185	mT
V_{Hmax} @ B_{max}	23.24	mV
I_{Hmax} @ B_{max}	26.56	µA
S_{AV} *Hall voltage mode*	0.1256	VT^{-1}
S_{AI} *Hall current mode*	0.1436	mAT^{-1}
$S_V = S_I$	0.0739	T^{-1}
G_H	0.725	-
θ_{Hmax}	1.078	deg
Plate width w	100	µm
Plate length l	100	µm
Plate thickness t	2	µm

A width to length ratio of unity was chosen as a practical device to use as it approximately coincides with the best trade-off between voltage or current sensitivity and the geometrical correction factor

degradation [9]. According to [9], the maximum achievable voltage related sensitivity for a plate occurs for the shortest plate length. The mode of operation however changes from Hall voltage mode to Hall current mode once the plate becomes too short and thus for a very small Hall angle, the geometrical factor maximises at 0.742. The maximum achievable voltage related sensitivity S_{Vmax} for Hall voltage mode or current related sensitivity S_{Imax} for current mode is thus 0.0756 T^{-1}. The square Hall device is also a good choice as a test structure given it is very well documented in literature and simple to fabricate and study.

5. Layout

A layout was prepared according to the proposed design. The resulting Hall plate layout measuring 100 µm × 100 µm is illustrated in Fig. 5. The Hall device has n+ ohmic contacts connected to $\pm V_{bias}$ through which the plate will be electrically biased. Normally the GND and $-V_{bias}$ nodes will be at the same potential, but for test purposes they were not connected on chip. The n-type contacts stretch across the entire width of the plate to ensure an evenly distributed current flow through the device. The p+ emitters are located at the midway point of the plate and are connected to I_{E1} and I_{E2} and each measure 19.6 µm × 8.8 µm. Finally a p+ substrate contacts stretching around the entire plate are connected to the GND pad. Fig. 6 shows a photograph of the fabricated device.

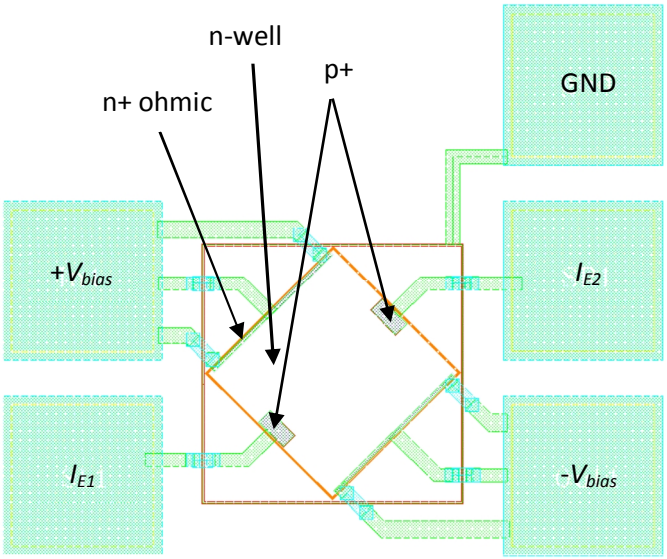

Fig. 5 Hall plate layout illustrating the biasing n+ ohmic contacts $\pm V_{bias}$, the p+ emitter contacts I_{E1} and I_{E2}, the n-well Hall plate and the collector formed by the GND substrate contacts

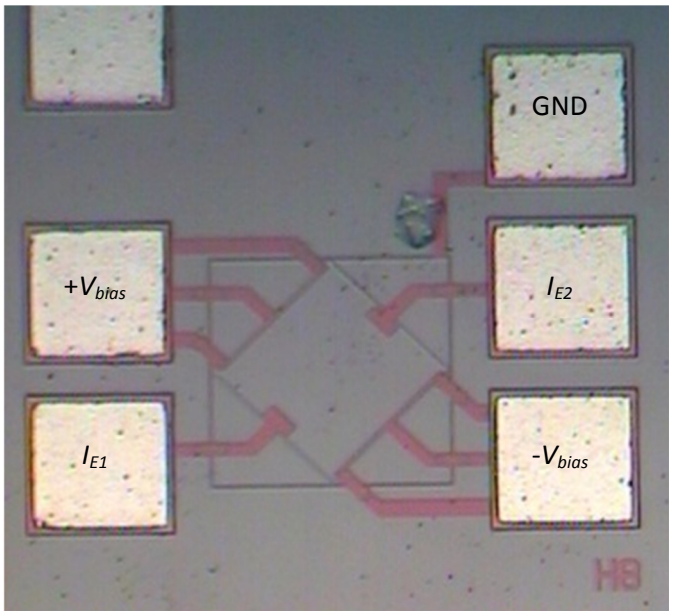

Fig. 6 Fabricated Hall plate

6. Experimental procedure and results

An A1302 linear ratiometric Hall sensor manufactured by Allegro was used as a reference for this experiment. The A1302 is a high precision linear Hall effect sensor that outputs a voltage that is directly proportional to the applied magnetic field. The A1302 was chosen as it has a very sensitive response of 1.3 mV/G. At a supply of 5 V, it provides for a very large dynamic range with high enough resolution for the intended aims of this study. Ten samples were manufactured and prepared for measurements. It was first required to measure the emitter and collector currents so that the active forward gain β for each Hall plate's BJT could be calculated. This was done by using a bias voltage of V_{bias} = +1.7 V applied to the Hall plate as well as the BJT emitters with ammeters between the emitters and the supply voltage. The calculated gains were averaged and the results reported in Table 3.

Table 3 Summary of BJT parameters at biased conditions as illustrated in Fig. 2 and Fig. 3

Parameter	Measured	Unit
V_{bias}	1.7	V
p-type *area*	1.72E-6	cm^2
I_C	1.67	mA
I_B	0.56	mA
I_E	2.23	mA
β_f	2.98	

Next the Hall plate resistances were measured such that the electron mobility for each individual sensor could be calculated. The measured results of the ten samples were then used to calculate the theoretical Hall current I_H for each individual plate according to Eq. (3). Using the electrical design in Fig. 3, a physical setup was built upon which the Hall plate integrated circuit was mounted such that the magnetic field from a rare earth magnet directly above it would intercept the plate perpendicularly. The magnet was then moved up and down with linear magnetic field strength steps and the emitter currents measured using a MASTECH® MS8218 digital multimeter with a resolution of 1 µA and hence also reflecting the uncertainty in the measurement. The measured differential emitter current thus consists of the differential base currents of the transistors multiplied by β+1 as indicated by Eq. (10). As with the Hall voltage, the Hall current appears positive through one of the BJT's and negative through the second, the sign reflecting the specific direction of the perpendicular field.

The differential emitter currents $\Delta I_{EH} = I_{E2} - I_{E1}$ for each device was measured individually. A comparison of a typical measured ΔI_{EH} current and the calculated elemental Hall currents I_H is plotted in Fig. 7. The magnetic field itself was calculated by using the A1302 output voltage as reference. The Hall plate was subjected to a maximum magnetic field of approximately ±185 mT at a bias voltage of V_{bias} = 1.7 V. From Fig. 7 it can be seen that a linear signal response is observed from the transistor circuit. The offset is in the order of 15 mT, which is not excessive, since no layout or circuit techniques were used to improve transistor matching. It can also be observed that the measured output current signal is significantly larger than the Hall current signal derived theoretically for the basic Hall element with no transistor readout. This is due to the current gain of the transistors.

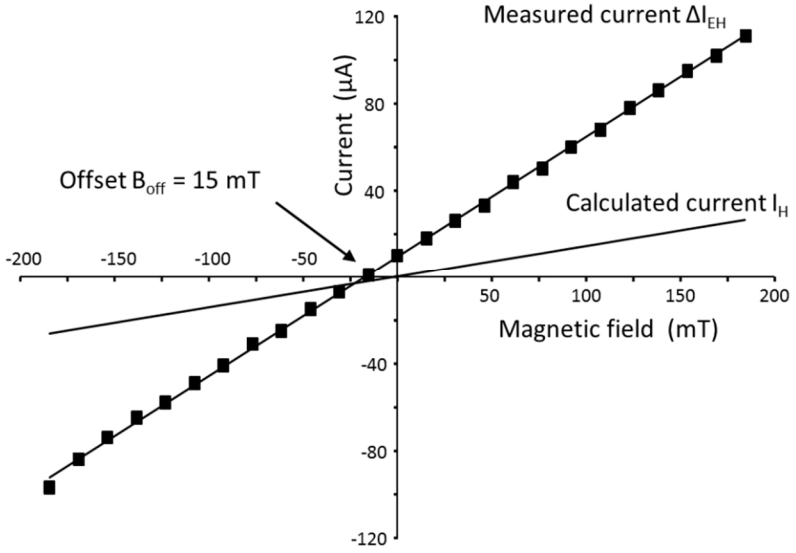

Fig. 7 Measured differential emitter current ΔI_{EH} of one Hall device compared to the theoretical Hall current I_H in µA versus the magnetic field B in mT

The average current gain of the ten BJT's was measured to be 2.98 which also compares well with the gain of 3 as illustrated by the simulation results in Fig. 4. It can thus be shown that the required sensitivity to measure 1 Gauss would be in the order of 150 nA, a feat easily achievable using very simple current mirroring techniques. Furthermore, by using high gain BJT's available in a BiCMOS process, significant gains can be made using this technique.

7. Noise analysis

Two noise sources are identified, namely i^2_{nR}, the noise contributed by the Hall resistive plate and i^2_{nT}, the input referred noise from the BJT.

The Hall plate noise i^2_{nR} is dominated by its thermal noise and *1/f* flicker noise and can be approximated by Eq. (11) if recombination-generation noise is excluded:

$$i_{nR}^2 = S_{nR} \cdot \Delta f = \left[\frac{4kT}{R_S} + \frac{\alpha}{n}\frac{1}{f} I^2\right] \Delta f. \qquad (11)$$

Current *I* is the bias current I_{bias} through the device, *n* the total number of charge carriers in the device, α is the Hooge parameter, a dimensionless value that may be associated with a specific device processing method and structure. Recently the Hooge parameter $\alpha \approx 10^{-5}$ has been determined for CMOS silicon Hall devices very similar to ours [20], and therefore we used this value in our calculations.

The input referred transistor noise i^2_{nT} has shot noise components as well as a flicker noise component, as shown in Eq. (12). Since two transistors are connected to the Hall plate, the transistor noise contributions should be twice that of a single BJT.

$$i_{nT}^2 = S_{nT} \cdot \Delta f = 2\left[2qI_B + \frac{2qI_C}{\beta^2} + \frac{KI_B}{f}\right] \Delta f \qquad (12)$$

The flicker coefficient *K* will determine the corner frequency of the BJT noise spectral density where the flicker noise equals the "white" shot noise. Most of the BJT spectra measured in a detailed study had corner frequencies in the range of 10 Hz to 10 kHz [21]. In our calculation a corner frequency of 1 kHz was assumed, a typical value for BJT devices.

The Hall noise current is i^2_{nH} and will be given by:

$$i_{nH}^2 = S_{nH} \cdot \Delta f = i_{nR}^2 + i_{nT}^2 \qquad (13)$$

The relevant noise spectral densities as calculated for our device are shown in Fig. 8. From this figure it can be seen that at low frequencies the transistor *1/f* noise is slightly larger than the Hall plate noise. The 100 Hz frequency noise values are tabulated in Table 4. From the slopes in Fig. 7, the absolute device sensitivities S_A could be determined for the plain Hall plate sensor, as well as the Hall sensor with BJT sensing devices.

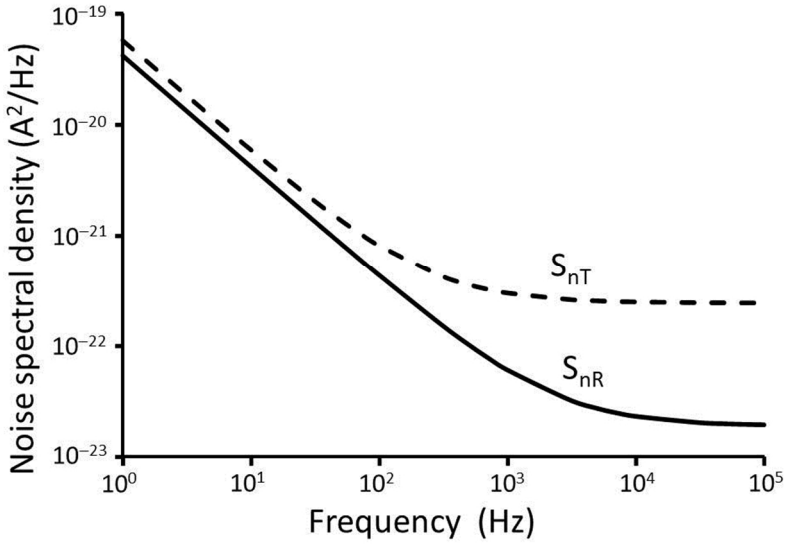

Fig. 8 Noise current spectral densities

Table 4 Summary of calculated noise contribution and minimum magnetic detection level at 100 Hz for i) a traditional plate without the integrated BJT's, and ii) the integrated BJT Hall device

	Absolute sensitivity S_A (A/T)	**Total input noise density S_{nH} (A^2/Hz)**	**Noise equivalent field (T/√Hz)**
Hall plate	140×10^{-6}	4.32×10^{-22}	0.15×10^{-6}
Hall plate + BJT	550×10^{-6}	12.4×10^{-22}	0.25×10^{-6}

From the above table the spot noise figure $NF = (SNR_{out})/(SNR_{in})$ of the BJT amplifier circuit can be determined as the ratio of the two input referred noise densities, giving us the value of NF = 4.6 dB at 100 Hz frequency. The noise figure can be lowered by reducing the BJT base current, although too low a base current will limit the dynamic range.

Measurements of CMOS Hall sensors with plate area 20 µm x 20 µm = 400 µm^2, layer thickness 1 µm and drive current 0.2 mA resulted in a measured noise equivalent field of 5×10^{-7} T/√Hz at 100 Hz [8]. The estimation of our Hall plate noise equivalent field is 1.5×10^{-7} T/√Hz at 100 Hz, which is in the same range.

Smaller area Hall plate devices will generate significantly higher *1/f* flicker noise than our quite large Hall plate. For µ-Hall devices electron drift velocity saturation may also become one of the main limiting factors and for silicon this occurs at an electric field of approximately 30 kVcm^{-1} [9]. For a bias voltage of 5 V for example, this corresponds to a minimum length of 1.5 µm. Scaling down the lateral dimensions, especially in present day deep submicron technologies, leads to an increase in noise on the Hall signal [8] and tends to dominate in smaller dimensions [11]. This is mainly due to the limited number of carriers available as well as other effects such as Joule heating. This makes the integrated BJT very suitable to integrate with µ-Hall devices whereby much lower power consumption results in lower biasing currents and consequently I^2R heating effects.

8. Limitations

8.1 Layout

As with the diode coupled BJT in a bandgap generator, care must be taken when currents flow through the substrate of an integrated device. The fundamental element that must be prevented in this case is latch-up. Latch-up occurs when adjacent structures form a pnpn structure that can be switched on when current flows through the substrate. By using well placed guard rails around the Hall plate, free carriers can be extracted from the substrate as soon as possible. The use of increased spacing to nearby devices is also a very effective method to reduce and even eliminate undesired latch-up scenarios. Typically an I/O should be able to withstand a minimum of 100 mA local substrate current according to the AEC-Q100-004 specification [22]. Using similar methods in our design should fairly easily ensure that substrate currents of a few mA can be tolerated.

8.2 BJT Beta variation

It is known that the current gain β is a function of temperature, collector to emitter voltage V_{CE} and collector current I_C. Fig. 9 illustrates this relationship using a standard foundry pnp BJT with similar area specifications. These variations in β will translate into an error in the gain of the Hall current signal and will especially affect high accuracy linear applications negatively. For this reason it will be necessary to measure and adjust the gain of each BJT by either trimming the bias current through the BJT or by adjusting V_{CE}. For simple binary applications the variations in β should be tolerable as

the switching points can include enough margin such that this variation has negligible effect. This can be done through stimulating the Hall plate with a known magnetic field with a given bias condition and measuring the output. The bias condition can then be changed by either using an adjustable operational amplifier to vary V_{CE} or by using adjustable current mirrors to vary the bias current through the Hall plate and implemented during wafer testing.

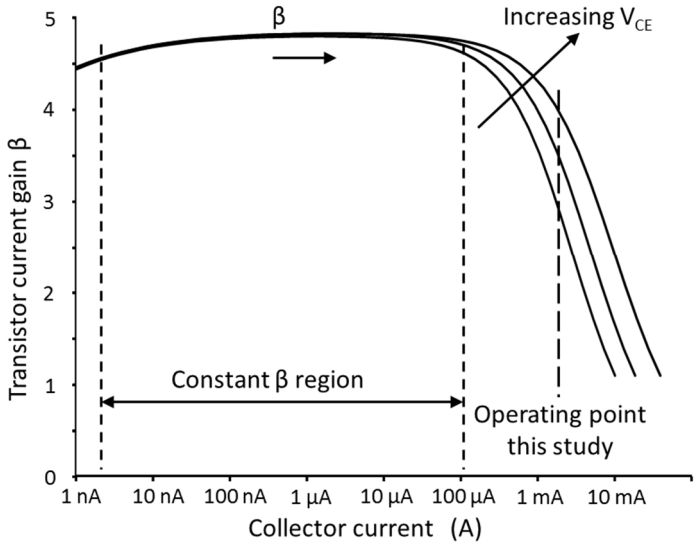

Fig. 9 BJT forward current gain β as a function of the collector current I_C as well as its dependency on the collector to emitter voltage V_{CE} for a similar sized BJT as characterised by the foundry

9. Conclusion

A novel solution has been presented for the measurement of the Hall current in standard CMOS Hall plate devices. Using p-type instead of n-type contacts at the sensing location results in the activation of the vertical parasitic BJT's through which the Hall current can be measured by measuring the difference in emitter current flowing through each BJT. Correctly biasing the Hall device and BJT's, results in a signal gain of β+1 times the Hall current. The method is well suited to µ-Hall devices to eliminate velocity saturation as well as to reduce Joule heating. The device was manufactured and shown to have very good correlation with the predicted theoretical results for a square Hall plate and also seems to be influenced by the geometrical factor in the same way traditional Hall voltage plates are. Future work will be focused on the design and implementation of a standalone sensor solution as well as dealing with the offset currents created by the biased BJT's.

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