The Effect of Temperature Change on the Performance Characteristics of RF PIN Diode Limiters for VHF Applications

by

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Submitted in partial fulfilment of the requirements for the degree
Master of Engineering (Microelectronic Engineering)

in the

Department of Electrical, Electronic and Computer Engineering
Faculty of Engineering, Built Environment, and Information Technology

UNIVERSITY OF PRETORIA

June 2023

SUMMARY

THE EFFECT OF TEMPERATURE CHANGE ON THE PERFORMANCE CHARACTERISTICS OF RF PIN DIODE LIMITERS FOR VHF APPLICATIONS

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Keywords: Capacitance versus temperature, de-embedding, flat leakage, parameter extraction, PIN diodes, RF limiters, spike leakage

In this dissertation, the effect of temperature change on the capacitance of a PIN diode and performance of RF limiters was investigated. The focus was on measuring the change in junction capacitance between -25 ºC and 100 ºC and determining the consequence thereof on the performance of different limiter topologies operating primarily in the VHF band. This was done through small-signal measurements of the PIN diode (that was soldered onto a printed circuit board (PCB)) between -20 V and 3V at different temperatures. Using de-embedding and parameter extraction techniques, important parameters, including the capacitance, could be extracted from the PIN diode. It was found that the junction capacitance of four Skyworks PIN diodes increases with temperature, whereas the forward-biased series resistance decreases with increasing temperature.

Each of the four PIN diodes were soldered into three different limiter topologies on the PCB and high-power transient and non-linear measurements were conducted on the various limiters. It was found that, because of an increase in temperature, the increase in diode capacitance influences the carrier lifetime of the diode and, along with the decrease in

forward-biased series resistance, increases the transient spike leakage and decreases the flat leakage of a limiter. It was further found that the increase in capacitance does not affect the non-linear attenuation of the limiter, but rather the decrease in resistance that is responsible for the increase in attenuation. From the measurements it was also concluded that, for VHF, an anti-parallel topology provides the best performance over a wide range of temperatures in terms of non-linear attenuation and transient spike and flat leakage.

LIST OF ABBREVIATIONS

AC	Alternating Current
CAD	Computer Aided Design
CSV	Comma Separated Values
CW	Continuous Wave
DC	Direct Current
DRC	Design Rule Check
DUT	Device Under Test
EW	Electronic Warfare
HALT	Highly Accelerated Life Tests
HASS	Highly Accelerated Stress Screening
LNA	Low Noise Amplifiers
LVS	Layout Versus Schematic
MMIC	Monolithic Microwave Integrated Circuit
PA	Power Amplifier
PCB	Printed Circuit Board
PIN	Positive-Intrinsic-Negative
RF	Radio Frequency
SCPI	Standard Commands for Programmable Instruments
SOLT	Short-Open-Load-Thru

STC	Sensitive Time Control
TR	Transmit/Receive
TRL	Thru-Reflect-Line
TRM	Through, Reflect and Match
TRM	Thru-Reflect-Match
VCO	Voltage-Controlled Oscillator
VHF	Very-High Frequency
VISA	Virtual Instrument Software Architecture
VNA	Vector Network Analyser
VSWR	Voltage Standing Wave Ratio

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CHAPTER 1 INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Context of the problem

In modern communication systems, a single antenna is often used for both transmitting and receiving signals [1]. In these systems, such as radar, high-power signals can leak from the transmission path into the receiver path [2]. In other applications, such as mobile Electronic Warfare (EW) systems, a broadband receiver antenna is frequently found in very close proximity to a high-power transmitter antenna that occupies the same frequency spectrum [3]. As a result, high-power incident signals delivered by the transmission antenna could enter the receiver antenna. A Radio Frequency (RF) limiter has, since its invention in the 1960s, become a key component in modern receiver protector designs to provide electromagnetic protection to sensitive circuit components at the front-end of a receiver chain [4] – [12]. A simplified communications receiver is shown in Figure 1.1.

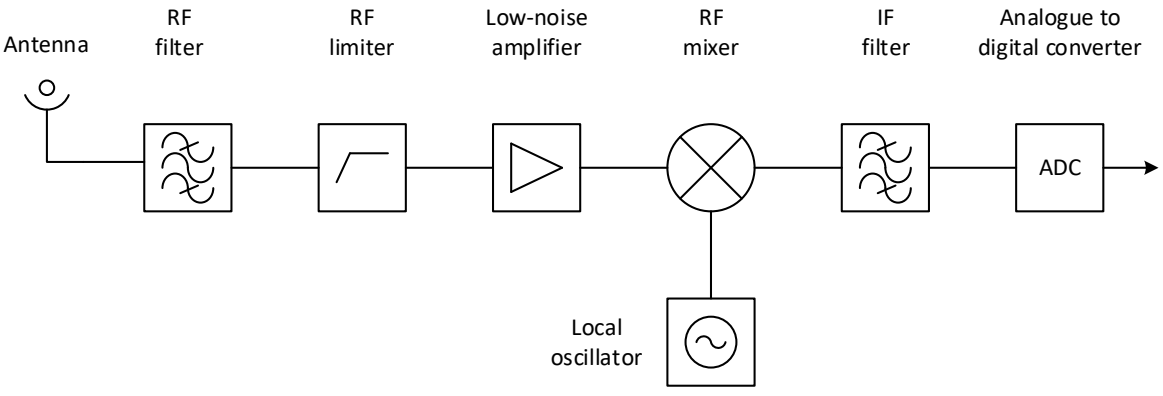


Figure 1.1. Simplified communications receiver.

Military communication and EW systems commonly use the Very High Frequency (VHF) band (30 – 300 MHz) to operate and are often used by personal and armoured vehicles that

are deployed in harsh environments. Electronic components, such as an RF limiter, used in these communication and EW systems are exposed to extreme device temperatures during their service in the field, which can cause their performance to show significant variation. It is, therefore, critically important to understand this behaviour and be able to model the performance of these components over a wide temperature range beforehand.

1.1.2 Research gap

Studies that investigated the effect of temperature on PIN diodes focused primarily on the change in diode resistance in the forward-bias state and at frequencies outside the VHF band [13] – [20]. It is known from the literature that the spike leakage of a PIN diode limiter can be influenced by the response time of the PIN diode, in that more energy can pass through the limiter before it provides enough limiting [3], [11]. The response time and recovery time of the PIN diode is directly related to the diode's carrier lifetime [1], [5], [10], [21], and the carrier lifetime is in turn influenced by temperature and the capacitance of the I-layer [14], [15], [22]. A PIN diode with a thick I-layer has more capacitance and a slower response and longer recovery time than a PIN diode with a thin I-layer, but also has greater power handling capability [23]. It is also known that the insertion loss and bandwidth of the limiter are related to the capacitance of the diode.

No research is available in published literature on what effect temperature has on the capacitance of PIN diodes and the result on a PIN diode limiter's performance, specifically for diodes in limiters used in applications that operate in the VHF band. The research gap that will be addressed with this work is the investigation and measurement of the effect of temperature change on device capacitance and the resulting performance characteristics both in the steady-state and transient response of an RF PIN diode limiter. The study can assist in the improvement of the durability of PIN diode limiter circuits in the VHF band.

1.2 RESEARCH OBJECTIVE AND QUESTIONS

The focus of this study is on the effect that device temperature variation has on the performance of a PIN diode limiter used in Electronic Warfare or military systems that operate in the VHF band because of a change in diode capacitance. The following research question is addressed:

- What effect does temperature variation have on the capacitance of an RF PIN diode?

Expanding on the primary research question, the following research questions were also addressed during this study:

- What effect does the change in RF PIN diode capacitance have on the transient behaviour of an RF limiter?
- What type of RF PIN diode-based limiter topology performs best in terms of transient behaviour under various temperature conditions, given change both in capacitance and resistance over temperature?
- What type of RF PIN diode-based limiter topology performs best in terms of steady- state behaviour under various temperature conditions, given change both in capacitance and resistance over temperature?

To answer the primary research question, the following hypothesis was formulated:

'*An increase in the device temperature of a PIN diode will increase the capacitance of the PIN diode. Because of the increased capacitance, the carrier lifetime of the diode will also increase which will increase the response time of the limiter and, therefore, increase the spike leakage.*'

1.3 APPROACH

An experimental approach was followed where simulation results was used as a reference to which experimental measurement results was compared against. For the simulation, a PIN diode and RF limiter circuit was simulated and analysed to determine the effect of device

temperature change on the capacitance and other small-signal parameters of a reverse-biased PIN diode and the subsequent change in RF limiter performance, specifically the transient performance. Characteristically different PIN diodes were used, the results of which were used as the reference results. The widely recommended PINDRC Caverly PIN Diode simulation model was used.

After the simulations, a physical test layout of a PIN diode and limiter circuit was constructed for measurement. A test fixture to house the DUT (device under test) was also designed along with a TRM (Through-Reflect-Match) calibration area, which assisted in the parameter extraction of the PIN diode. The different PIN diodes were first measured in isolation to determine the effect of temperature on their capacitance, before being integrated into the limiter circuit. A temperature-controlled oven was used to regulate the device temperature during practical measurements. The temperature range of interest was between -25 °C and 100 °C.

For both simulation and physical experiments, data were taken across the temperature range in 25 °C increments and at frequencies that include the VHF band. The measurements included small-signal S-parameters of the PIN diode under different bias conditions, as well as the steady-state and transient response of the limiter circuit to an incident RF signal. The S-parameters were measurement using a calibrated VNA, a variable power supply and digital multi-meter. Model parameters were extracted from the measured S-parameters. Performance characteristics such as the steady-state and transient response of the limiter circuits were measured using laboratory equipment such as a spectrum analyser, a high- power RF amplifier, an RF exciter unit (to generate a square-wave modulation on a high-power RF tone) and RF power meter.

1.4 RESEARCH GOALS

The objective is to determine the change in PIN diode capacitance as a function of diode temperature. Furthermore, the goal of this study is to link these changes, both in simulation

and measurement, to the change in RF limiter performance, both steady-state and transient, as a function of PIN diode device temperature within the VHF band.

1.5 RESEARCH CONTRIBUTION

The contribution of this study is the provision of both simulated and measured results for the change in capacitance and associated performance variation in an VHF-band PIN diode limiter. The resulting data can be used to better understand the impact of device temperature on the performance of an RF PIN diode limiter.

1.6 RESEARCH OUTPUTS

The following journal publication is in preparation from this research study:

> C.J Botha, C. van Niekerk and T. Stander, "The Effect of Temperature on the Capacitance of a PIN Diode used in RF Limiters", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2023 (in preparation).

1.7 OVERVIEW OF STUDY

The dissertation is organised as follows:

Chapter 2 provides a detailed theoretical and literature review of RF limiters and PIN diodes. The basic concepts and important performance characteristics of RF limiters are discussed first, followed by a comparison of several RF limiter technologies. The semiconductor operation of PIN diodes is discussed thereafter, including the effect of temperature on the PIN diode and how the diode compares to other common diodes. The final topic of the literature review focusses on diode limiters and a comparison between different topologies.

Chapter 3 describes the research methodology and test plan that was followed to complete this study. Choice of data points for the simulated and measured test are discussed and the

detailed design of the test fixture layout and limiter topologies are also provided. This chapter also presents the calibration and measurement setups that were used to capture the data. Finally, the methods used to derive mathematical models for diode's parameter extraction are discussed.

Chapter 4 documents the measured results for the various PIN diodes obtained from this study and a comparison to relevant simulation data and, where applicable, results from previous published studies. This chapter also highlights the modelling approach that was used. Main observations are provided and deviations from expected results are explained.

Chapter 5 discusses the measured and simulated results for the PIN diode limiters and gives a comparison between the topologies in terms of their performance characteristics. Where possible, results from previous published studies or manufacturer data were used as reference. As like before, main observations are provided and deviations from expected results are explained.

Chapter 6 summarises the study and draws concluding remarks about the work that was performed and provides suggestions for future work.

CHAPTER 2 LITERATURE STUDY

2.1 CHAPTER OVERVIEW

This chapter presents a review of the fundamental concepts and building blocks for PIN diodes and RF limiters. Section 2.2 provides a detailed review of PIN diodes like their forward and reverse biased equivalent circuits and how their operation can be influenced by temperature. The section further provides a comparison between PIN diodes and other common diodes. The following section, Section 2.3, gives an introduction into RF limiters and their function in a receiver system. Their on and off states are discussed and important metrics that characterise their performance are also explained. Different RF limiter technologies and their advantages and shortcomings are discussed in Section 2.4, including different operating architectures like active and passive limiters. Section 2.5 presents RF limiters that are based on diodes and some of the most common limiter topologies. The section also discusses research into the effect of temperature on diode limiters and their durability. Section 2.6 provides a conclusion to the literature study and final remarks.

2.2 PIN DIODES

PIN diodes are widely used in RF applications and can be considered as a bias-controlled, variable resistor at RF and microwave frequencies [1], [8], [9], [24]. In contrast to a varactor diode, which is a voltage-controlled device, a PIN diode is current-controlled. A PIN diode also differs from a conventional PN diode in the sense that it has three layers, hence the abbreviation, PIN. A simplified layout of a PIN diode can be seen in Figure 2.1.

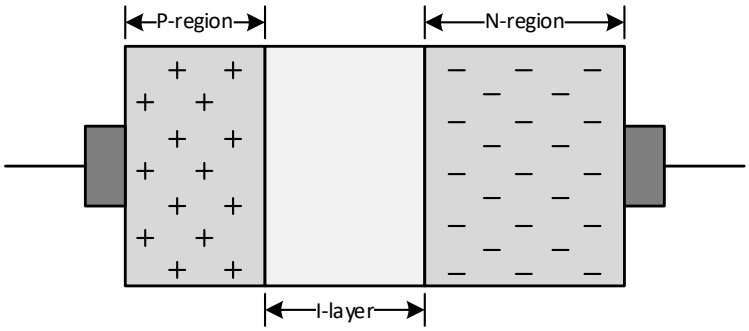


Figure 2.1. PIN diode layout.

The P-layer is a thin layer with small resistance and is heavily doped with p-type acceptor impurities (or holes). The N-layer is a layer that is heavily doped with n-type donor impurities (or electrons). It is also the thickest out of the three layers and a key element to the thermal impedance of the diode with a non-negligible resistance. The I-layer, or *intrinsic* layer, is an undoped layer found between the P and N-layers. Intrinsic silicon contains very little impurities and as a result, has a high resistivity. However, because of manufacturing processes, the intrinsic layer is rarely purely undoped but is often lightly doped with n-type impurities [1], [8], [10].

2.2.1 Intrinsic region characteristics

Because the presence of the intrinsic layer in a PIN diode is the cause for its exclusive properties, it is worth discussing this layer and the characteristics of a PIN diode that depend on it, such as the stored charge, carrier lifetime, and power handling, among others. By varying or choosing the dimensions and properties of this layer, certain trade-offs can be made for different applications.

The stored charge is increased when holes and electrons from the neighbouring regions are injected into the I-layer. The charge density of the I-layer determines the resistance of the diode, and when no bias is applied to the PIN diode, the resistivity of the I-layer can be a few thousand Ω/cm. The geometry and resistivity of the I-layer determine the minority carrier lifetime of the diode. Minority carrier lifetime, τ, is the time that a free charge carrier exists before recombination occurs. Carrier lifetime not only governs the microwave and RF

resistance of the device, but also affects the response time, spike leakage, recovery time, and bandwidth when used in an RF limiter. It is also related to the stored charge in the diode. The thickness of the I-layer determines the threshold level and power handling capability but is inversely proportional to the carrier lifetime of the diode [1], [5], [10], [21]. Thus, a PIN diode with a thick intrinsic layer has exceptional power handling capability but is too slow to be used in stand-alone RF limiter applications because of its long response time [13]. This relationship was confirmed by studies which report that the thickness of the I-layer of the PIN diode has a direct impact on both the magnitude and duration of the spike leakage and the threshold and limiting level of a PIN diode RF limiter [10], [25]. It was also found that the spike leakage increases with frequency for a given incident RF signal because the shorter RF wavelength does not provide sufficient time for charge carriers to transit the I-layer and combine [26].

The intrinsic layer can be lightly doped with gold atoms to substantially reduce the minority carrier lifetime. However, gold adds to the cost of the diode and increases the minimum resistance of the PIN diode [1]. Therefore, a trade-off must be made when choosing an intrinsic layer thickness: thin enough to have a low carrier lifetime and fast response and recovery time, but thick enough to meet power handling capability and threshold level.

2.2.2 Forward biased equivalent circuit

If an RF signal is incident on the PIN diode, its positive cycle injects charge carriers (holes and electrons) from the P and N-layers into the high-resistance I-layer where they combine, forward biasing the PIN diode. The charge does not recombine instantaneously, but instead has a finite lifetime, τ, in the I-layer before recombination occurs. When charge carriers combine within the I-layer it results in the lowering of the resistivity of the I-layer and enables current to flow across the layer. For RF signals above a lower frequency limit, f_T, the negative half-cycle of the incident signal is not sufficient to remove all the charge carriers in the I-layer, and thus the impedance remains low. This lower frequency limit is discussed later in this section. The quantity of stored charge, Q, is a function of the carrier lifetime, τ,

and forward bias current, and differs for Alternating Current (AC) and Direct Current (DC) forward biases. For an AC forward bias, the stored charge in the I-layer is given as

$$\frac{dQ}{dt} = i_f(t) - \frac{Q}{\tau}, \tag{2.1}$$

where

Q is the stored charge in Coulombs,

τ is the carrier lifetime, and

$i_f(t)$ is the time-varying forward bias current.

For a DC forward bias, the stored charge is the I-layer is given as

$$Q = \tau I_F\ (C), \tag{2.2}$$

where

Q is the stored charge in Coulombs,

τ is the carrier lifetime, and

I_F is the forward bias current [27].

A forward-biased PIN diode behaves as a current-controlled resistor that presents a linear resistance to the flow of RF current through the diode. It is this property that enables a PIN diode to be used as an RF power control element [24]. The equivalent circuit of a forward-biased diode is shown in Figure 2.2.

Figure 2.2. Forward biased PIN diode equivalent circuit.

The circuit consists of a series combination of parasitic inductance, L, and forward series resistance, R_F. R_F is a function of the forward bias current, I_F, whereas L depends on the

geometrical properties (such as the wire bonds or connector length and diameter) of the diode and has little effect on the diode's performance for frequencies below 1 GHz [13], [27].

The resistance of the diode's I-layer under forward-bias is inversely proportional to the stored charge, Q, given by (2.2), and can be expressed as [1], [24], [27]

$$R_F = \frac{W^2}{(\mu_n + \mu_p)Q}\ (\Omega), \tag{2.3}$$

where

R_F is the forward series resistance (Ω),

W is the I layer width in microns,

μ_n the electron mobility,

μ_p the hole mobility, and

Q is the stored charge.

Substituting (2.2) into (2.3), the expression for R_F as an inverse function of the forward bias current, I_F, is given as

$$R_F = \frac{\mathrm{W}^2}{2\mu_a \tau I_F}\ (\Omega), \tag{2.4}$$

where

μ_a is the ambipolar carrier mobility as

$$\mu_a = \frac{(\mu_n + \mu_p)}{2}. \tag{2.5}$$

At DC and very low frequencies, a PIN diode behaves as a rectifying diode where the series resistance of the diode is described by the dynamic resistance of the non-linear current-voltage, or I-V, characteristics at any bias point. Dynamic resistance defines the diode's resistive nature when an AC source is applied. It is measured by the ratio of change in voltage across the diode to the resulting change in current through the diode for a specific DC operating point. At these low frequencies, the series resistance decreases as the frequency is increased. PIN diodes that are designed to function in RF and microwave frequencies show

this decrease in resistance in the 1 – 10 MHz frequency range, although this may vary significantly depending on the characteristics of the diode [27].

The dynamic resistance point is only valid at frequencies well above the inverse of the carrier lifetime, τ, of the I-layer, which can mean significant deviations from the assumed resistance behaviour may be observed if operated at lower frequencies [20]. The frequency at which this occurs is called the transit frequency and can be considered as the lower frequency limit for which (2.4) applies. This is the point at which the diode starts to behave like a current-controlled resistor with a linear resistance curve. The lower frequency limit is primarily a function of the thickness of the I-layer. An estimate of the transit frequency is given as [24]

$$f_T = \frac{1300}{\mathrm{W}^2}\ (MHz). \tag{2.6}$$

2.2.3 Reverse biased equivalent circuit

When the diode is reverse biased, the impedance of the PIN diode is at its maximum, and ideally, there is no stored charge in the I-layer. However, there still exist some stored charge in the I-layer. When reverse biased, the diode appears as a capacitor with capacitance C_R shunted by a parallel resistance R_P to an RF signal. The equivalent circuit of a reversed biased diode is shown in Figure 2.3.

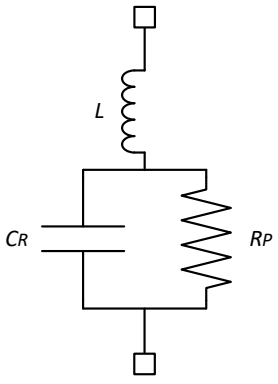


Figure 2.3. Reverse biased PIN diode equivalent circuit.

The equivalent circuit consists of the shunt combination of diode capacitance, C_R, and diode resistance, R_P, in series with the parasitic inductance, L, which can also be neglected for

frequencies below 1 GHz [13], [27]. C_R and R_P represent the reactance and net dissipative resistance of the depleted I-layer in the reverse-biased diode, respectively. C_R contains the junction capacitance, C_j, and the stray capacitance, C_{pkg}, because of the diode's package structure. For bare die packages, C_{pkg} is often ignored. Similarly, the parallel resistance, R_p, is also affected by any series resistance in the semiconductor or diode contacts or package. The capacitance C_R can be calculated as [1]

$$C_R = \frac{\varepsilon A}{d}\ (F), \tag{2.7}$$

where

C_R is the diode capacitance (F),

ε is the dielectric constant of the material comprising the I-layer,

A is the diode junction area, and

d the thickness of the I-layer.

From (2.7), the larger the diode's I-layer is, the more shunt capacitance it will have. To reduce the effect of shunt capacitance, diodes are often stacked in series. The capacitance of a diode influences device characteristics such as the insertion loss, recovery time and bandwidth [28]. The lowest frequency for which (2.7) is valid is related to the dielectric relaxation frequency of the I-layer, f_τ, which can be calculated as [27]

$$f_\tau = \frac{1}{2\pi\rho\varepsilon}\ (Hz), \tag{2.8}$$

where

ρ is the resistivity of the I-layer, and

ε is the dielectric constant of the material comprising the I-layer.

For frequencies below f_τ, the capacitance characteristics of the PIN diode behaves like that of a varactor diode [29].

Even if the diode is operated at zero bias, some charge may still exist in the I-layer, and so the diode behaves as a lossy capacitor, and a small voltage, which is called the *punch-*

through voltage, must be applied to the I-region to sweep out the finite immobile charge left in the I-layer [1], [24], [27]. PIN diodes also have a reverse breakdown voltage that is proportional to the I-layers' width. When the breakdown voltage is exceeded, the PIN diode will enter avalanche breakdown where the reverse current increases rapidly and can result in PIN diode failure.

2.2.4 Thermal effects

The serviceable life of a semiconductor device is exponentially reduced as its operating temperature increases. For this reason, the influence of temperature on a PIN diode is of extreme importance to its reliability and performance. Under normal operation, a diode will dissipate only a small portion of the incident RF power upon it. Over time, however, this can be appreciable.

There are two main parameters of a PIN diode that are strongly influenced by temperature: I-layer ambipolar mobility, $\mu_a(T)$, and carrier lifetime, $\tau(T)$ [14], [15], [16]. Ambipolar mobility and carrier lifetime as a function of temperature are given as

$$\mu_a(T) = \mu_a(T_{nom}) \left(\frac{T}{273 + T_{nom}}\right)^{-2.3} \text{ (°C)}, \tag{2.9}$$

and

$$\tau(T) = \tau(T_{nom}) \left(\frac{T}{273 + T_{nom}}\right)^{\tau_{\text{coefficient}}} \text{ (°C)}, \tag{2.10}$$

where

$\mu_a(T)$ is the ambipolar mobility as a function of temperature,
$\tau(T)$ is the carrier lifetime as a function of temperature,
T is the temperature in °C,
T_{nom} is the ambient temperature in °C,
T is the temperature in °C, and
$\tau_{\text{coefficient}}$ is the carrier lifetime temperature coefficient.

Equation (2.10) shows that the carrier lifetime increases with increasing temperature, an observation that was confirmed in [16] and [22]. Investigations of the carrier lifetime temperature coefficient, $\tau_{\text{coefficient}}$, have shown a wide range of coefficient values that are dependent on the diode's surface passivation and I-layer capacitance [17], [20]. It has also been established that ambipolar mobility shown in (2.9) decreases with increasing temperature [16].

Thermal capacitance, which is also referred to as heat capacity, is defined as the amount of energy required to raise the temperature of the I-layer of the diode by 1 °C, in the absence of heat flow from the diode [1], [30]. Thermal capacitance is given by

$$C_{Thermal} = \frac{\rho c_\theta}{V} \ (J/°\text{C}), \tag{2.11}$$

where

$C_{Thermal}$ is the thermal capacitance in Joule per Celsius ($J/°$C),

c_θ is the specific heat property of the diode material in cal/(g °C),

ρ is the density of the diode material in g/cm^3, and

V is the volume of the I and N-layer and is given by

$$V = \frac{\pi {r_I}^2}{d_I + d_N}, \tag{2.12}$$

where

r_I is the radius of the I-layer,

d_I is the thickness of the I-layer, and

d_N is the thickness of the N-layer.

Equation (2.11) would indicate that a diode with a thick I-layer requires more energy to increase the temperature of the diode from within and, therefore, it can be assumed that device temperature variations will have less of an impact on diodes with thick I-layers, and more of an impact on diodes with a thin I-layer.

Continuous Wave (CW) thermal resistance, $\emptyset_{jc}$, is a PIN diode parameter given by the manufacturer that indicates the temperature rise per Watt of power dissipated in the diode's junction and is given as °C/W. The thermal resistance equates to a resistor in an electric circuit, whereas the thermal capacitance is analogous to a capacitor. Together, the thermal capacitance and resistance create a thermal time constant that dictates the time the PIN diode's junction takes to increase in temperature. The thermal time constant, $\tau_{Thermal}$, is used to understand how the junction temperature of a diode changes over time and can be given as

$$\tau_{Thermal} = \emptyset_{jc} C_{Thermal}. \tag{2.13}$$

Heating at the junction of the diode limits the maximum average power that can be incident on a PIN diode because most of the power absorbed by a PIN diode is dissipated into the I and N-layers. Heat flow through convection and radiation is mostly negligible, and the conduction of heat through the PIN diode's bond wires is often small enough to be ignored [1]. To maintain safe operating conditions for a PIN diode, the maximum junction temperature, T_j, should not be exceeded. The maximum junction temperature is often given by diode manufacturers and is typically between 150 and 200 °C. Junction temperature, T_j, is given as

$$T_j(t) = T_{a/heatsink} + P_d \emptyset_{jc} (1 - e^{\frac{-t}{\tau_{Thermal}}}), \tag{2.14}$$

where

$T_j(t)$ is the junction temperature as a function of time,

$T_{a/heatsink}$ is the ambient or heatsink temperature,

P_d is the dissipated power,

$\emptyset_{jc}$ is the thermal resistance, and

$\tau_{Thermal}$ is the thermal time constant [1].

For a CW incident signal, the junction temperature rise reaches an equilibrium given by (2.14). For pulsed signals, the heating does not reach equilibrium immediately since the diode is only heated for a portion of the duty cycle.

2.2.5 Comparison to other diodes

This section is dedicated to the comparison of a PIN diode's operation and characteristics, which were discussed above, to those of other semiconductor diodes that are often used in RF limiter applications, the PN and Schottky diode.

The process of converting an alternating current into a unidirectional current is defined as rectification [24]. A rectifier device conducts current only in one direction. A rectifier PN junction diode is one of the simplest semiconductor devices and has the characteristic of passing current in only one direction only. The diode does not behave linearly to the applied voltage because of the non-linear current-voltage relationship. In a PN diode, a junction is formed between a p-type and n-type semiconductor, which creates a potential barrier voltage across the diode junction (approximately 0.7 V for silicon-based and 0.3 V for germanium-based diodes). The potential barrier voltage is also known as the forward voltage drop. A simplified layout of a PN diode can be seen in Figure 2.4.

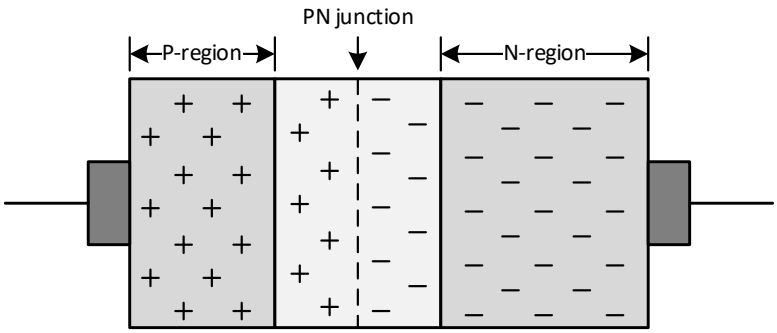


Figure 2.4. PN diode.

The junction region, known as the depletion region, has no charge carriers itself and has a physical thickness that varies with the applied bias voltage. When the diode is forward biased, the width of the depletion layer between the two regions decreases and mobile charge carriers (holes and electrons) are supplied with extra energy to overcome the potential barrier and cross the junction. When the diode is reverse biased, free charge carriers are pulled away from the junction which causes the width of the depletion layer to increase. The physical changes in the depletion layer's width are a result of the differences in the electrical properties of the two sides of the PN junction. Rectification is one of the results produced

by this physical change. Through forward or reverse biasing, the effective resistance of the diode's junction itself is decreased or increased, respectively, thus allowing (or blocking) current to flow through the diode. A PN diode is often used in clamping circuits for DC restoration and clipping circuits for wave-shaping.

The Schottky diode is a metal-semiconductor diode with a very fast switching speed and a forward voltage drop that is much lower than that of a conventional silicon PN-junction diode. Schottky diodes are constructed using a metal electrode bonded to an n-type semiconductor and has no depletion layer. A simplified layout of a Schottky diode can be seen in Figure 2.5.

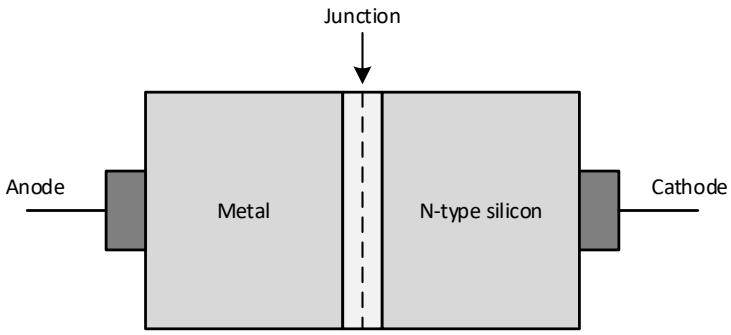


Figure 2.5. Schottky diode.

A common contact metal used for Schottky diodes is silicide, a highly conductive silicon and metal compound with a low ohmic resistance value allowing more current to flow, which produces a smaller voltage drop of around 0.3 to 0.5 V. When the diode is forward biased, electrons move from the n-type material to the metal contact allowing current to flow. Thus, the current through the diode is the result of the drift of majority carriers. Because there is no p-type semiconductor material and, therefore, no minority carriers (holes), the conduction stops very quickly and blocks the flow of current when the diode is reversed biased. Like a PN diode, a Schottky diode does not behave linearly to the applied voltage because of the non-linear current-voltage relationship. Schottky diodes are often used in applications that involve rectification, voltage clamping, signal conditioning and switching. Due mainly to their fast-switching speeds, they are also used in microwave and millimetre wave frequency applications such as mixers, detectors, and power limiters [31].

The major difference between the diodes is that silicon-based PN and Schottky diodes have a non-linear I-V curve, or non-linear resistance, which produce a rectified RF signal. PIN diodes behave linearly and exhibit low distortion over a range of input power, frequency, and bias conditions because of the presence of stored charge in the I layer, and thus, does not rectify the signal. However, at frequencies below that given by (2.6), a PIN diode behaves the same as a rectifier diode because of insufficient stored charge in the I layer to control to large RF current present. The differences in electrical performance between the rectifier and PIN diodes are most apparent in RF applications. When a PIN diode is operated within the correct conditions, it can switch large values of RF current with a small amount of DC bias current. PIN diodes perform a unique function for RF switches and attenuators, or limiters, that rectifier diodes cannot perform.

IMPATT and Tunnel diodes were not included in this comparison because both diodes have negative resistance characteristics, which make them favourable for applications like voltage-controlled oscillators (VCOs) and output amplifiers.

2.3 INTRODUCTION TO RF LIMITERS

An RF limiter is a power attenuation device that is inserted between a source, such as an antenna, and sensitive components at the start of a receiver chain and is designed to prevent high-power signals from passing into the receiver, whilst allowing the receiver to function unprotected in the absence of such signals [2], [4], [5], [8], [12], [13].

An RF limiter works by attenuating high-power signals which are above a certain power threshold through limiting the output power to a constant power level, but also allowing low-power signals below the power threshold to pass through uninterrupted to the receiver [8], [14]. The limiter reflects most of the input signal power to the source rather than dissipating it as heat, although in practice, some of the power is dissipated by the limiter itself. The reflected power is either re-radiated through the receiver antenna or is directed to be

dissipated into a resistive load [1], [8]. The input and output power threshold of an RF limiter greatly depends on the required application of the limiter.

An RF limiter can function in any one of three operating states based on the power level of the incident signal.

2.3.1 Large-signal state

In this state, the limiter is active, or on, and is protecting sensitive components against high-power signals that are above the power threshold level. The limiter is very poorly matched, and the output power is clipped to a constant power level. Important limiter performance metrics that are commonly used are, but not limited to, the following [2], [8], [32], [33]:

2.3.1.1 Threshold level

The limiting threshold level is defined as the incident power level at which point the output power is attenuated by 1 dB [34]. It is also known as the 1 dB compression point of the output. Above this level, the attenuation is not linear with the input power. The threshold level is illustrated in Figure 2.6.

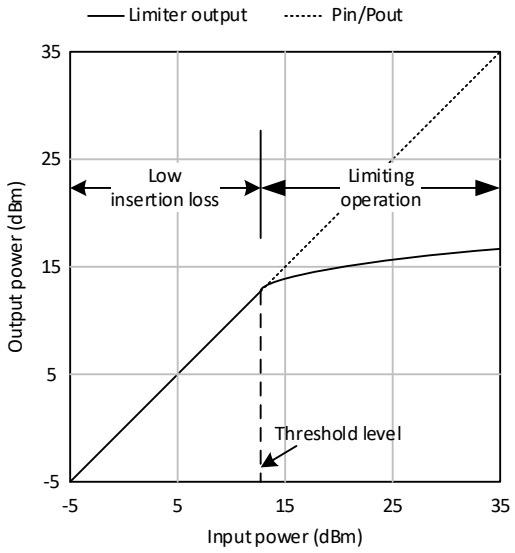


Figure 2.6. Threshold level.

2.3.1.2 Saturation level

This is the RF input power level for which the limiter is no longer able to protect the receiver. At this level, the output power can no longer be clipped and, once again, increases linearly relative to the input power. The saturation level is illustrated in Figure 2.7. For RF input levels above the saturation level, the limiter can become severely damaged or even destroyed.

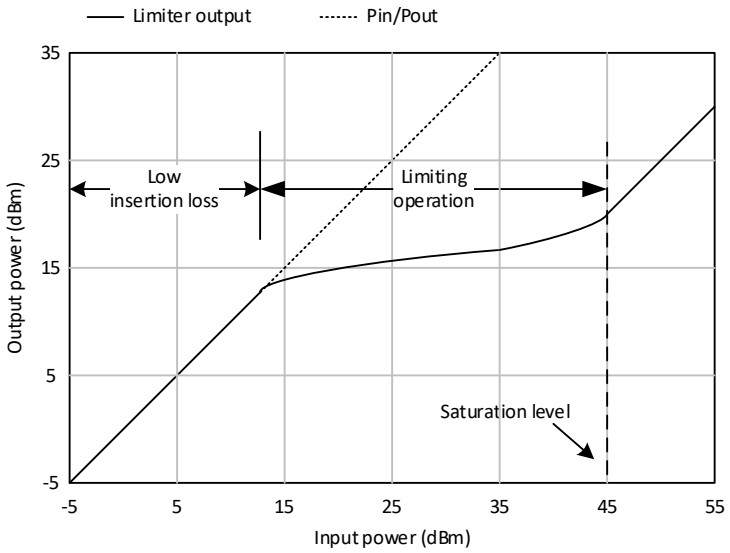


Figure 2.7. Saturation level.

2.3.1.3 Response time

Response time is the small amount of time it takes the limiter to react to a high-power incident signal and transition from the small-signal to the large-signal state. Generally, it is considered as the time taken for the limiter to provide 1 dB of attenuation and is usually in the sub-nanosecond to nanosecond range. The response time of a limiter varies depending on the limiter design and technology used and is inversely affected by the power handling capability of the limiter.

2.3.1.4 Spike leakage

Spike leakage can be defined as the total amount of RF energy from the leading edge of a high-power pulse or signal that passes through the limiter as it transitions from the small-signal to the large-signal state [23], [25]. A typical theoretical response of a limiter with a

high-power signal fed into the input is shown in Figure 2.8. Spike leakage is often referred to in units of energy, not power.

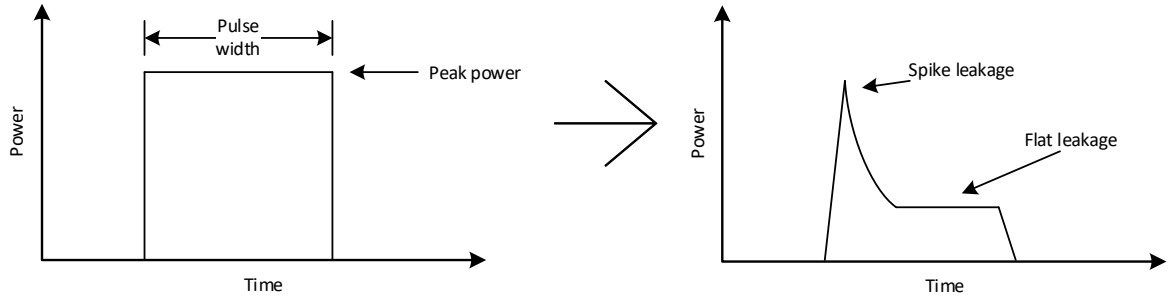


Figure 2.8. RF input/output comparison with spike and flat leakage.

2.3.1.5 Flat leakage

Flat leakage refers to the output power level of the limiter after it has transitioned to the large signal state. This power is not reflected to the source and instead propagates past the limiter into the receiver chain. Flat leakage is also shown in Figure 2.8.

2.3.2 Small-signal state

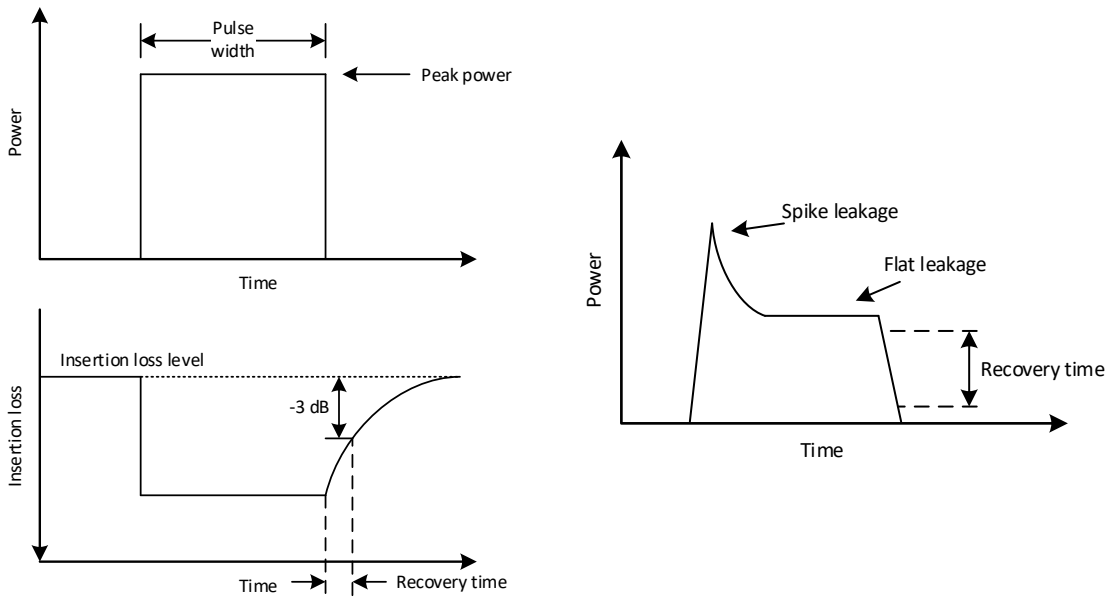
In this state, the limiter is off and is not providing any protection against incoming signals. The incoming signals are below the power threshold and pass with relatively low power loss, which would be the case when the receiver is *listening* for or *staring* at outside signals through the antenna. The limiter is ideally matched and provides minimum insertion loss to in-band signals to keep the noise figure of the receiver low in this state. It is common to define the insertion loss and VSWR performance metrics of the receiver during this state [8], [34]. To maintain a low insertion loss, components with small shunt capacitance are often preferred.

2.3.3 Recovery state

The recovery state is the period during which the limiter transitions from the large-signal state back to the small-signal state. During this transition state, the sensitivity of the receiver is momentarily degraded since received in-band signals that are of interest would be

attenuated. Therefore, during this transition, the receiver is, essentially, *blind* [1]. The duration of this state is often referred to as the recovery time of a limiter, and for certain applications, such as radar, communications, or EW systems, it is desired to have this duration as short as possible. The recovery time of a limiter constitutes an important characteristic of comparison between different limiter designs and technologies [8].

The standard industry definition is that recovery time is measured from the end of an incident signal up to the point where the attenuated output power has returned to within -3 dB of its quiescent insertion loss value, as illustrated in Figure 2.9 (a) [2]. Another experiment measures recovery time as the time for the output power to return to normal operating levels [35], whereas elsewhere it is defined to be the time between the 3 dB point of the trailing edge of a high-power incident signal to the time where the output reaches 90% of its small signal level [8], [12].



(a) (b)

Figure 2.9. Recovery time.
(a) -3 dB Recovery time. (b) 10/90 Recovery time.

However, because the insertion loss was not measured during the transient measurements, the 10/90 recovery time was selected for the performance comparisons, which is the time

interval it takes the signal to go from 10% to 90% of its final value and is illustrated in in Figure 2.9 (b).

It is relevant to mention the following regarding recovery time:

- The recovery time is related to the quiescent insertion loss value, and is, in general, a function of the incident power and pulse width. The higher the power and width of the pulse of the incident signal, the longer the recovery time [2].
- Recovery time is a fundamental measurement when choosing a limiter configuration for a specific application.
- Reduced recovery time can impede other requirements, such as threshold and saturation levels.

2.4 RF LIMITER TECHNOLOGIES

Various technologies can be used to create RF limiters. Some of these technologies are commonly used for most limiter applications, whereas others are more specialised towards a certain application. This section discusses some of these technologies.

2.4.1 Limiter operating architecture

An RF limiter can either operate as a passive limiter, an active limiter, or in some cases as a semi-active limiter, which is also known as *quasi-active* [2], [8], [36].

A passive limiter is self-activated and does not require external control logic to provide protection. The limiter is switched on by a high-power incident RF signal and is thus AC biased [8]. Passive limiters are commonly adopted as receiver limiters and are generally considered to be more reliable than active limiters because of their *always-on* protection. Other advantages of passive limiters include their minimalistic design with little to none additional components, such as DC bias or driver control circuitry [2], [3], [37]. Bias refers to the voltage potential across a device or component and can be one of three conditions: zero bias, reverse bias, or forward bias. Zero bias implies there is no external voltage

potential across the device, whereas reverse and forward bias refer to a negative and positive voltage potential across the device, respectively. The disadvantage of a passive limiter is the inverse relationship that exists between their power handling capability and response time [3], [11]. This inverse relationship means that a passive limiter with a high power-handling capability is slow to respond to an incident signal above the limiter's power threshold level. Similarly, a passive limiter with quick response time is incapable of handling a high-power incident signal. Because of this relationship, passive limiters are generally best suited for low to medium power applications.

Active limiters require a driver control signal or a DC bias network to provide protection. A limiter driver delivers a fast bias current injection to the limiter at an incident pulse's leading edge. In some cases a driver also provides a reverse bias spike at the trailing edge of the pulse, improving the limiter's reverse recovery time The advantage of using an active limiter is the ability to control the insertion loss of the limiter, and thus the threshold level, using an external control voltage/current or driver according to a detected input power level, therefore, providing *on-demand* protection [38]. This makes active limiters attractive for radar and sensitive time control (STC) systems where the control signal is synchronised with a transmitter pulse [2], [3], [37]. The disadvantages of an active limiter are the addition of control logic circuitry and components, increased complexity, and physical footprint. Additionally, if the control signal is not synchronous with the transmitter pulse, or fails for any other reason, there is no receiver protection. Active limiters are often used in applications that require medium to very high power-handling capabilities, a low threshold level, fast recovery time or extremely low spike leakage power [2]. It has been shown [39] that an active, or DC biased, PIN diode-based limiter provides significantly more isolation at high input power than a passive, AC biased, PIN diode.

In certain applications, passive and active limiters are combined to form a *quasi-active* limiter and provide receiver protection against low to high power signals. Such limiters provide passive, *always-on*, protection but also have circuitry that includes *on-demand* protection capability under normal or ideal operating conditions [36].

Table 2.1 shows a comparison between the advantages and disadvantages of the three limiter architectures:

Table 2.1. Limiter operating architecture comparison.

Architecture	Advantage	Disadvantage
Passive	Limits large in-band incident signals. The receiver is always protected, even when the receiver is off. No power supplies or driver required.	Slow reverse recovery time. Requires reverse DC bias to improve insertion loss and recovery time.
Active	Limits synchronous RF signals. Low losses and spike leakage. Faster response and recovery time.	Zero non-synchronous protection. DC power supply required for the driver circuit. Physical size. If the control signal fails, the receiver protector fails.
Quasi-active	Limits both synchronous and non-synchronous signals. Low loss and spike leakage. Provides protection even when the power is off.	DC power supply required for the driver circuit. Physical size.

2.4.2 Technological solutions

Technological solutions for RF limiters differ in various aspects. Some of the most common technologies are discussed below.

2.4.2.1 TR tube

The transmit/receive (TR) tube is a passive limiter with a single or multiple high-Q, parallel LC circuit, resonant filter section(s) constructed in a section of the waveguide which is sealed with waveguide windows at the ends [2], [40]. Truncated cones and irises, or posts, form the

capacitive and inductive elements, respectively. The waveguide is evacuated and filled with gas at below atmospheric pressure. In the absence of a high-power signal, the TR tube functions as a band-pass filter with characteristics determined by the spacing and dimensions of the LC elements. A high-power incident signal will create an arc between the capacitive cone gaps which ionizes the gas in the region and causes most of the signal power to be reflected. The layout of the TR tube is such that as the input power increases, the attenuation increases, which creates a constant flat leakage for increasing input power levels. TR tubes provide very good protection against both in-band and out-of-band frequencies and can have very-high power handling capability. TR tubes also have good dynamic operating power range and are forgiving should its power handling capacity be exceeded. However, TR tubes have slow recovery times and a limited operational lifetime because of the use of gas, although a gas reservoir can be installed to increase the operating life. Its power handling capability is limited by the temperature rise on the glass waveguide windows but can be increased by using ceramic windows. TR tubes can be unattractive for long-service or fast-response limiter systems but are often used in radar systems.

2.4.2.2 Pre-TR tube

The pre-TR tube is very similar to the TR tube and functions much the same way, with main differences being that the gas is stored in a quartz tube and a lower-Q circuit. This means that the pre-TR tube has better power handling capability since quartz has a higher melting temperature than glass. A pre-TR tube has very low insertion loss and because the gas is stored within a quartz cylinder, as opposed to body-filled TR tube, gasses with a much faster recovery time can be used. The disadvantages of pre-TR tubes are its low-Q circuit, which does not provide much in-band or out-of-band protection, and it also has limited operational life. It is well suited as a pre-limiter, hence the “pre” in “pre-TR tube” and is usually followed by either a TR-tube or other type of limiter [2], [41].

2.4.2.3 Solid-state limiter

Semiconductor-based limiters, such as diode limiters, are most prevalent and commonly used in modern receiver protection applications. Solid-state limiters are primarily based on PIN or Schottky diodes but can include MESFET transistors and rectifying PN diodes [24].

Solid-state limiters have advantages such as that it can be configured as either active or passive limiters, do not have a limit on its operational life, and can easily be designed as a multifunctional component or module to gain additional functionality, such as increased response time and power handling capability. The main characteristic exploited in these limiters is the change in the device's resistance as a function of the incident power. These devices have very high and low resistance for low and high-power incident signals, respectively. The disadvantage of this type of limiter is that a powerful enough incident signal will destroy or damage them [8]. Diode limiters are discussed in the following section.

2.4.2.4 Superconductor and smart material limiter

Superconductor-based limiters use superconducting materials that change between the conducting and semiconductor state with a rise in temperature. The operating principle is as follows: A super-conducting layer with very low resistance is inserted in series with the main transmission line. When the incident power is below a certain threshold, the temperature loss of the circuit is low. When the temperature increases, the superconductor behaves like a semiconductor and blocks the incident signal. This type of limiter has the advantage of quick response time, but a disadvantage of being difficult to realize as it requires cooling mechanisms and control of the ambient temperature to avoid a condition where external warming induces activation of the limiter and therefore a loss of useful signal. Smart materials are materials that exhibit varying electrical characteristics based on external effects such as temperature or light [8]. Vanadium dioxide is an example of a material used in a superconductor limiter which passes from the semiconductor to the conducting state according to a threshold temperature and have been explored for applications such as thermally actuated RF switching, tuneable metamaterials, and broadband limiting [2], [32].

2.4.2.5 Ferrite limiter

A ferrite limiter is a passive limiter with a permanently magnetised ferrite material mounted alongside one or more of its waveguide walls. In the active, or on, state, the in high-power signal is absorbed by the ferrite as the signal passes down the waveguide [42]. The absorbed RF energy is converted into heat energy. In the de-active, or off, state, the limiter looks like a dielectrically loaded piece of a waveguide to an RF signal and passes through freely. The

ferrite limiter has a very fast recovery time and an indefinite operational lifetime. The main drawbacks of the ferrite limiter are its low power handling capability, high insertion loss, high spike, and flat leakage (because of slow response time), its sensitivity to changes in ambient temperature and self-heating in the active state. This makes the ferrite limiter unattractive to systems that are exposed to severe temperature conditions and high-power requirements. This limiter is also normally installed as a pre-limiting device and followed by a higher-power capable limiter such as a diode limiter [2].

For comparison purposes and because of the widespread adoption of solid-state, diode limiters in front-end receiver protection, they are the preferred limiter technology for this study, with particular emphasis on discrete diode limiters that are based on PIN diodes.

2.5 DIODE LIMITERS

Diode limiters are most prevalent and commonly used in modern receiver protection applications. This section discusses diode limiters based on PIN and Schottky diodes, and a combination of the two.

2.5.1 PIN diode limiter

PIN diodes are generally preferred to other solid-state alternatives such as Schottky diodes for RF limiters because of their power handling capability, despite their slow response time. Because of this, discrete PIN diodes are the chosen diode for this study. A typical passive, single-stage PIN diode limiter is shown in Figure 2.10.

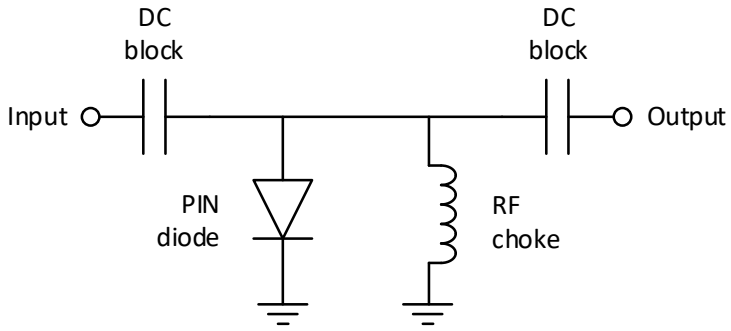


Figure 2.10. Simplified PIN diode limiter configuration.

Commonly, the PIN diode is mounted in shunt across the transmission line and is provided with a DC bias return [5], [6], [43]. A shunt PIN diode also has a convenient heat removal path to the ground plane or a heat sink. In this configuration, the limiting level and spike leakage are determined by the thickness of the PIN diode's I-layer. Spike leakage can be reduced by using a multi-stage limiter design, where a subsequent diode reduces the spike leakage from the first diode [23].

The operation of the limiter in this configuration can be described as follows: In the absence of a high-power signal, the diode appears as a capacitor with a small value to an RF signal, of which the equivalent circuit is shown in Figure 2.3. The insertion loss of the diode in this state is mainly the mismatch loss because of the capacitive reactance of the diode's junction capacitance.

The presence of a high-power incident signal will force charge carriers from the P and N-layer into the high-resistance I-layer during the positive half-cycle of the RF signal. This reduces the series resistance of the PIN diode from its maximum value to its minimum value, assuming the amplitude of the incident signal is sufficiently large. The series resistance of the PIN diode during the forward biased state is given by (2.4). Most of the charge carriers persist in the I-layer during the negative half-cycle and so current starts to flow in the closed-loop formed by the DC bias return. Thus, the diode limiter is biasing itself and momentarily forcing the impedance of the PIN diode to a minimum, causing an impedance mismatch and maximum insertion loss which reflects most of the input signal power to the source. Not all

the input signal is reflected to the source. Some of the energy propagates past the diode because the charge carriers that are forced into the I-layer from the P and N-layers by the incident signal does not recombine immediately. Spike leakage is the portion of the signal that passes the diode as it transitions from high impedance to low impedance. The power output of the diode after it has changed to its low impedance is the flat leakage. Spike and flat leakage were discussed previously and are visually presented by Figure 2.8 [7], [13], [29].

When the high-power signal is removed, and for a brief period thereafter, free charge carriers remain present in the I-layer and so the impedance remains at a minimum. After a short delay, known as the recovery time, the carriers in the I-layer recombine, the DC bias stops, and the impedance of the PIN diode reverts to its maximum value.

2.5.2 Schottky diode limiter

Schottky diodes are popular in limiter applications because of their fast response time but have the disadvantage of poor power handling and limiting capability [11], [33], [44]. Studies report that Schottky-diode based limiters have power handling capabilities in the region of 29 dBm to 33 dBm (0.8 W – 2 W) [3], [45]. A similar study experimented with high-power Schottky diodes that have been designed through the introduction of a diffused guard-ring structure at the edge of the Schottky diode, improving the saturation level of the diode to around 40 dBm (10 W) [33]. This design, however, was difficult to fabricate for diode geometries suitable for X-band frequencies and above. It also increased the total capacitance of the device, which increased the insertion loss of the diode limiter. For this reason, Schottky diodes are rarely used for single-diode limiter applications and instead find their application in Monolithic Microwave Integrated Circuit (MMIC) technology or multi-stage limiter configurations [11], [35], [44], [46], [47].

Schottky diode limiters and Low Noise Amplifiers (LNAs) are often used together in MMICs and are widely popular in commercial and military microwave systems. An advantage of integrated limiter/LNA circuits is the improved noise figure compared to

discrete solutions because the limiter's parasitic capacitance forms part of the LNA's input impedance matching network. Another advantage of limiter/LNA MMIC is its single-chip design that requires no additional components and assembly [35]. A Ka-band integrated limiter and low noise amplifier design that uses an antiparallel Schottky-diode limiter configuration, like the configuration shown in Figure 2.11, was presented in [45]. The study reports an overall noise figure improvement of between 0.3 to 0.35 dB to less than 2.9 dB across the band compared to a discrete solution, with a maximum input power of 33 dBm (2 W) and response and recovery time of 2 ns and 90 ns, respectively.

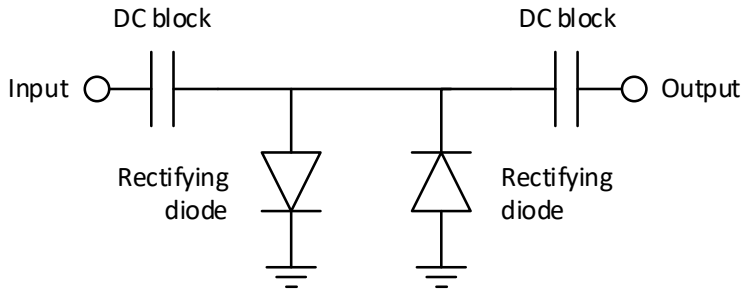


Figure 2.11. Anti-parallel limiter circuit.

Since Schottky diodes are rectifier diodes and only *clip* an RF signal, they are often installed in an anti-parallel configuration to limit the peak voltage of the positive and negative signal alternations, either referenced to ground or some other selected DC level. The limiter circuit as shown in Figure 2.11 is known as a Clipper circuit and is discussed in a later section.

Because of the Schottky diode's fast response time, they also find application alongside PIN diodes as detector elements in multi-stage limiters [1], [4]. A separate discussion on multi-stage diodes and PIN-Schottky limiters is presented in the next section.

2.5.3 Multi-stage diode limiter

The PIN and Schottky diode limiters that were discussed in the preceding sections are referred to as single-stage diode limiters. A single-stage limiter only has one diode *stage*, like the limiter shown in Figure 2.11, but can feature multiple stacked diodes within the stage

or make use of an anti-parallel configuration, like the limiter shown in Figure 2.10. In some cases, more isolation is required to protect sensitive components. For these cases, multi-stage limiters are used.

Multi-stage diode limiter designs employ more than one diode and are very popular topologies to achieve certain power requirements. Stages are usually separated by a quarter wavelength transmission line [13], because a quarter wavelength acts as an impedance transformer, transforming small impedances into large impedances, and vice-versa. Therefore, at least one diode will be on. Most practical limiters have 3 stages or less [1]. A two-stage PIN diode limiter topology is shown in Figure 2.12.

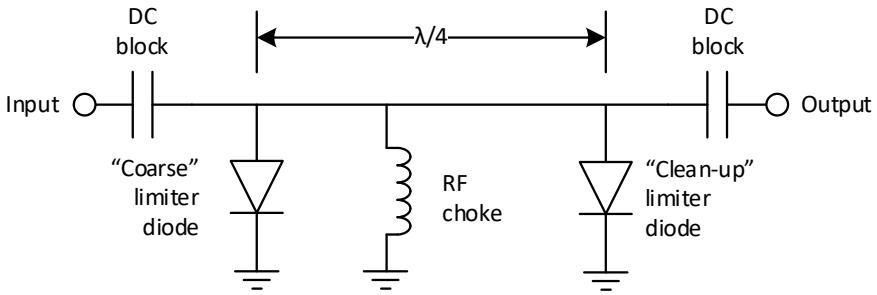


Figure 2.12. Two-stage limiter topology.

In a two-stage limiter topology, the first stage is closest to the input and is referred to as the *coarse limiter*. The second stage is known as the *clean-up limiter* [1], [48]. The two stages are spaced one-quarter wavelength apart, or an odd multiple thereof. A third or additional stage can be added in the middle if more power handling is required. The third stage would be known as the *intermediate limiter* and is also spaced one-quarter wavelength away from the adjacent stages. In a multi-stage limiter topology where all the diodes are PIN diodes, the coarse limiter normally has a thicker intrinsic layer compared to the other diodes and determines the limiting capability of the limiter. The coarse limiter also produces the insertion loss of the overall limiter. The clean-up limiter has a thin intrinsic layer and determines the threshold level and spike leakage of the overall limiter. The coarse limiter is used to limit the incident power to a level that the clean-up and subsequent limiter stages can withstand. The intermediate limiter has an intrinsic thickness anywhere in between the coarse- and clean-up limiter and provides additional limiting capabilities.

Passive two-stage limiters work as follows: With no or low-power input signals, all the diodes are in their off state with maximum impedance and the input signal passes through. With the arrival of a high-power signal, spike leakage is generated as some of the power passes through the limiter while the clean-up limiter transitions from maximum to minimum impedance first, because of its thinner I-layer. Since the coarse limiter is spaced a quarter wavelength away from the clean-up limiter, a voltage maximum occurs over the coarse limiter, forcing charge carriers from the P and N-layer into the I-layer thus reducing its impedance to a minimum. Once in the forward-biased state, the coarse limiter handles most of the overall limiting.

The Clipper limiting circuit that is shown in Figure 2.11 is a very basic topology and features two rectifier diodes (which could be PN junction or Schottky diodes). The two rectifying diodes limit the peak-to-peak voltage of an incident wave either to ground or a DC bias level. For diodes connected to ground, the peak voltage of the incoming signal must exceed the forward voltage drop to force the diode into conduction. Signals with a lower peak voltage will pass through the limiter, whereas signals above this voltage will be clamped to within a forward voltage drop of the potential to which the diode is connected. Since the clipped output signal is no longer sinusoidal, the input power is spread across the frequency band, which results in the input power still propagating past the limiter at higher frequencies. This circuit is well suited for low-frequency applications, but undesirable given its power-spread behaviour and therefore not considered any further.

PIN-Schottky diode limiters are an example of a multi-stage limiter and are discussed in the following section.

2.5.4 PIN-Schottky diode limiter

A PIN-Schottky diode limiter is, as the name implies, a multi-stage limiter utilising the power handling capability of a PIN diode and fast response time of a Schottky diode. The most common configuration for a PIN-Schottky limiter is having the PIN diode function as

the key signal-attenuating component, and the Schottky diode function as the signal detecting component. The Schottky diode is connected at the end (furthest from the source) of the limiter for this configuration [46], [47]. A typical PIN-Schottky limiter circuit is shown in Figure 2.13.

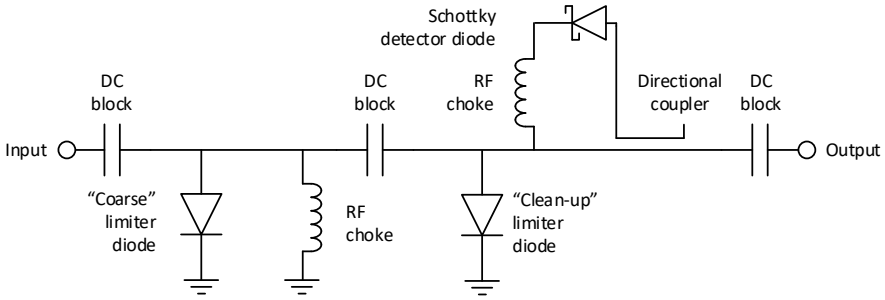


Figure 2.13. PIN-Schottky detector limiter circuit.

Active or semi-active multi-stage limiters often use a directional coupler with a Schottky diode to perform peak detection on incoming signals [1], [43]. The coupler samples the incident signal and compares it to a reference value which can be set depending on the desired threshold level or application. The current produced by the Schottky diode is applied as a bias current to the clean-up limiter via an RF choke.

A study that investigated a low-loss configuration for integrated PIN-Schottky diode limiters reports that a PIN-Schottky diode limiter provides better receiver protection than a PIN diode limiter because it has a limiting threshold that is 10 dBm (10 mW) less [47]. However, the extra diode in a PIN-Schottky limiter results in a higher insertion loss than a PIN diode-only limiter because of the diode's parasitic capacitances loading the signal path. This also negatively impacts the overall noise figure of the system since the limiter normally precedes the LNA. Aside from reducing the parasitic capacitance by stacking the diodes in series or though mesa construction, limiter loss can be reduced using circuit techniques. The improvements in the study are also attributable to the low-pass Pi configurations used in it. A Pi (Π) configuration integrates the PIN and Schottky diode's parasitic capacitances into a lowpass ladder network with a series inductor. The study found that at 1.8 GHz, the Pi configuration achieves a 13 dB lower return loss and 0.2 dB lower insertion loss than a conventional parallel PIN-Schottky control limiter.

A multi-stage PIN-Schottky diode limiter with a high degree of isolation and nanosecond response time was designed in [11] for RF front ends using multi-stage PIN and Schottky diodes. The design used a single shunt PIN diode with an intrinsic layer thickness of 10 µm as the coarse limiter, two PIN diodes with an intrinsic layer thickness of 5 µm each in an anti-parallel configuration for the intermediate limiter, and two 2.5 µm PIN diodes and two Schottky diodes. The study investigated the pulse characteristics of the limiter using modulated pulses with a 200 ns duration and a 1 GHz centre frequency. No information regarding the integration medium is provided. The study found that the design has a response time of less than 1 ns, a limiting capability of 34 dBm (2.5 W) with a 50 dBm (100 W), 30 ns duration microwave input pulse, and a voltage capability of more than 200 V with a 30 ns square input pulse that has a 1 ns rising edge.

A similar multi-stage limiter design was introduced by another study that verified the design and experimental methods of an active RF front-end limiter [43]. The design uses a single shunt PIN diode with an intrinsic layer thickness of 7 µm as the first stage, two PIN diodes with an intrinsic layer thickness of 4 µm each in an anti-parallel configuration for the second stage, and three, paralleled 2 µm PIN diodes for stages 3 through 5. The design also used an RF coupler at the front, preceding the first stage limiter, to detect and compare the incident RF signal to a pre-set threshold value and determines whether to DC bias stages 3 through 5. No information regarding the integration medium is provided, but from the figures shown in the study it was deduced that limiter module was an MMIC. The study also used a modulated signal with a 1 GHz centre frequency and pulse widths between 200 ns and 3 µs. The study reports that the power amplitude of the output RF signal was less than 0 dBm (1 mW) when the square pulse modulated microwave input signal power was 40 dBm (10 W). Although the response time of the active limiters of stages 3 to 5 was as short as 7 – 9 ns, because of the use of a coupler, an extra 10 ns was needed by the passive limiters of stages 1 and 2 before it was completely transformed from high-impedance state to low-impedance state.

Other PIN-Schottky diode-based studies focused on the recovery time [35], [49], the evaluation of device characteristics of GaN merged PIN-Schottky diodes [50], and a GaAs limiter designed for 8 – 12 GHz frequencies [51].

2.5.5 Temperature effect on PIN diode limiters

Understanding and predicting the effect of temperature on a PIN diode limiter is critical to a design engineer to maximise the durability and performance of the limiter.

A study by Caverly investigated the effect of temperature on a PIN diode's parameters and the impact it has on PIN diode attenuators [16]. The study consisted of a theoretical analysis of the behaviour of ambipolar mobility and carrier lifetime with temperature ((2.9) and (2.10), respectively). Measurements were then performed to determine the temperature dependence of a PIN diode's resistance and carrier lifetime, and its effect on a shunt diode limiter's performance. For a PIN diode, the study found that the type of material used to passivate the diode's surface and geometry (like I-region size) influences the temperature dependence of the carrier lifetime coefficient. It was found that a typical silicon dioxide passivated PIN diode has a carrier lifetime temperature coefficient ($\tau_{\text{coefficient}}$ from (2.10)) of around 1.7, reliant on the diode's capacitance. Depending on the temperature dependence of the carrier lifetime coefficient, the resistance of the PIN diode may increase ($\tau_{\text{coefficient}} < 2$), decrease ($\tau_{\text{coefficient}} > 2$), or remain constant ($\tau_{\text{coefficient}} = 2$) over temperature. The study reports that low capacitance (0.1 pF and smaller), silicon dioxide passivated diodes show a resistance change of between -0.1% and +0.1% per ℃. The PIN diode measurements were performed at 100 MHz and temperatures varying between 20 ℃ and 90 ℃. For the PIN diode attenuator (or limiter), the results indicate that the temperature dependence of the carrier lifetime is a good predictor of the temperature coefficient of a PIN diode's resistance and, therefore, microwave attenuation. The measurements were taken at frequencies between 1 and 2 GHz with temperatures varying between 35 ℃ and 125 ℃. The results showed that large capacitance diodes, such as diodes with a thick intrinsic layer and $\tau_{\text{coefficient}} > 2$, tend toward a negative resistance coefficient, indicating that shunt diode limiters will show an

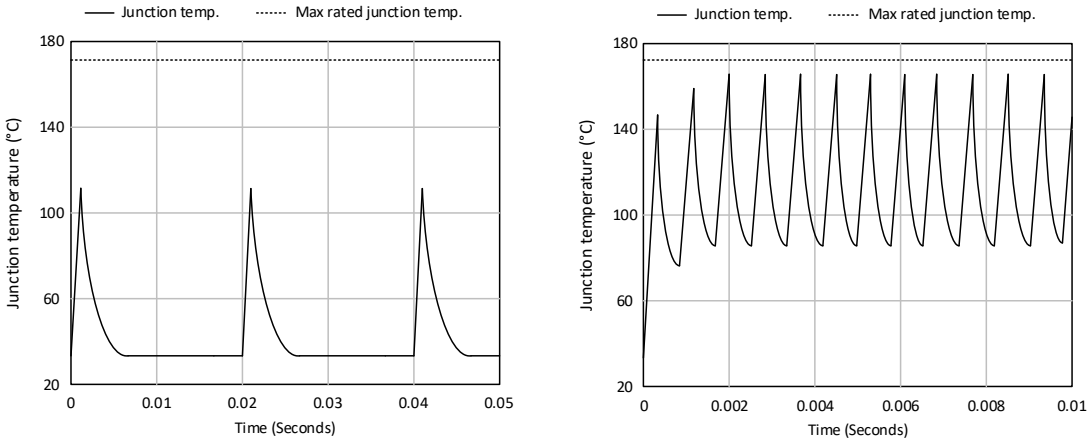
increase in attenuation with increasing temperature. Low capacitance diodes with $\tau_{\text{coefficient}} << 2$ exhibited little attenuation variation over temperature.

Results from [22] confirm the finding of Caverly in that the carrier lifetime is dependent on the ratio of the I-region area to I-region width. The study performed experiments to determine the effect of temperature on the carrier lifetime of a PIN diode. The diode temperature was controlled by airflow. Three gold-infused PIN diodes with different I-layer sizes and carrier lifetime values were used for the experiment. The results show a significantly steeper rise in carrier lifetime as a function of temperature for the diode with the largest I-layer and longest carrier lifetime compared to the diode with the smallest I-layer and shorter carrier lifetime, which showed a more gradual increase. Similar results are reported by another study [52]. The temperature range for the experiment was 25 ℃ to 200 ℃.

Another study by Caverly investigated the impact of temperature on the impedance of microwave and RF PIN diodes [20]. This study builds on the work previously completed in [16]. The results show that a PIN diode's resistance exhibit an increase with temperature for carrier lifetime temperature coefficients, $\tau_{\text{coefficient}}$, smaller than 2.3 (refined from a value of 2 found in [16]). The carrier lifetime temperature coefficient was again calculated using the stored charge. A significant increase in diode resistance was noted for carrier lifetime temperature coefficients of 1.5, whereas a modest decrease in resistance was recorded for coefficients greater than 2.3. The study also shows an increase in PIN diode reactance for the same carrier lifetime temperature coefficients discussed above. The measurements were performed at temperatures varying between 20 ℃ and 90 ℃ and frequencies between 10 MHz and 500 MHz.

It is evident from (2.11) that the physical properties of the diode determine its thermal capacitance and hence its thermal time constant. Assuming a constant input signal amplitude, a diode will not reach its steady-state temperature until approximately 6 thermal time constants, $\tau_{Thermal}$, have passed [1], [53]. As illustrated in Figure 2.14 (a), for pulsed input

signals of shorter duration, the junction temperature of the diode may reach a peak value that is less than the maximum junction temperature and that of a longer or more frequent burst, shown in in Figure 2.14 (b).



(a) (b)

Figure 2.14. PIN diode junction temperature for:

(a) Long pulses. (b) Short pulses.

For input signals or input pulses that are shorter than 6 thermal time constants, the junction temperature has time to recover as heat is transferred to a heatsink or analogue or chassis ground between pulses. For more frequent input pulses, the junction temperature does not have long to dissipate heat before the next pulse and so the junction temperature increases. Results from a study by Yi and Du [54] have shown that using repetitive microwave pulses, the maximum junction temperature of the PIN diode will rise, and that thermal burnout will inevitably occur. The results also showed that the thermal burnout power threshold of a PIN diode limiter can degrade with an increase in the number of input pulses. Caverly [15] found that a typical junction burnout temperature of 175 ℃ for a series PIN diode would occur at power levels of approximately 49 dBm (79.4 W). For power levels below 35 dBm (3.16 W), the temperature rise in the diode is minimal but increases rapidly for power levels above 40 dBm (10 W).

Ward, Tan, and Kaul [23] investigated spike leakage and burnout of silicon PIN diode limiters using a pulsed RF input signal. PIN diodes with I-layer thickness ranging from 0.5

to 50 µm were used. The study confirms that diodes with a thin I-layer have little spike leakage but are damaged at relatively low RF power levels, and that thick I-layer diodes can withstand higher levels of RF power but have much more spike leakage. This finding is supported by other similar studies [10], [25]. The investigation also found that for a PIN diode that is forward biased, the electric field is greater at the centre of the diode, and as such, the temperature build-up is a maximum there. Because the current density is uniform across the diode, heating will be proportional to the electric field. During reverse bias, the maximum fields are at the edge of the PIN diode, at the PI and IN junctions, and so the maximum temperature accumulates there. The study also found that spike leakage increases with frequency. RF pulses with a 1.5 ns rise time were used to test the spike leakage. The study reports that there exists a strong dependence between the burnout level of the diode and I-layer thickness, where a diode with a thicker I-layer is a higher damage threshold than a diode with a thin I-layer. Interestingly, the study also found that the damage threshold power decreases roughly linearly with RF pulse length.

2.5.6 Diode limiter durability

Limiter durability and reliability can be of great concern in nearly all limiter applications, especially in radar or EW systems. As discussed previously, limiters are occasionally exposed to harsh conditions, such as temperature, dust, and vibration, but should still reliably function as intended. This section will briefly discuss the reliability and durability of previous limiter studies.

An extensive study examining the reliability of high-power GaAs PIN diodes was performed in [55]. The study examined the continuous wave power handling capability of three X-band PIN diode limiters, each with different intrinsic layer thickness and topology (single-stage anti-parallel, two-stage anti-parallel and two-stage, double-row anti-parallel) at room temperature. From the results, the authors deduced an acceleration factor predicting the time-to-failure as a function of input RF power. A reduction of approximately 6 dB from the peak input power level is required to achieve $1x10^6$ hours of constant CW exposure at room temperature. The study also examined DC bias reliability and found that as current passes

through the PIN diode in the forward bias state, the series resistance of the diode starts to change. The change is a function of current density, and assuming a typical bias current of 5 mA, it would take 2.5 years for a 10% change in R_s. As discussed earlier, the insertion loss of a PIN diode is proportional to the series resistance, and the study found that a 30% change in R_s would only result in a 0.1 dB change in the insertion loss of the limiter. It should be noted that the study was performed two decades ago and both PIN diode and limiter technology has since changed rapidly.

Smith, Heston, and Allen conducted burnout experiments with PIN diodes of various intrinsic layer thickness in both single shunt and double, antiparallel configurations [28]. The authors concluded that a single and double diode configuration both experience destructive failure at approximately the same input signal level (40 dBm (10 W)) and, more importantly, a passive two-stage limiter configuration can be designed to maximize power handling capability and limiter bandwidth by reducing the number of diodes in the *clean-up* stage compared to the *coarse* stage and double stacking the diodes. By stacking the diodes, the shunt capacitance is reduced by a factor of 2. However, while stacking diodes does reduce the shunt capacitance, another study showed it adversely affects the threshold limit of the limiter and is a trade-off that should be considered [47].

Another study [56] investigated the damage accumulation in PIN diodes used in limiter applications due to microwave pulse injection. The study measured the insertion loss of a multi-stage PIN diode limiter after a defined amount of pulse injections to determine the degree of damage caused by the microwave pulses. The frequency, pulse width, repetition frequency and peak power of the microwave pulses were 5 GHz, 100 ns. 20 Hz and 2 kW, respectively. The results show that the damage accumulated by the limiter is not linear to the number of injected pulses. Instead, the insertion loss increases rapidly for the 40 pulse injections to 6 dB, then exhibits a slight decrease to 5 dB before remaining constant until 600 injected pulses, after which it increases again until the maximum 1000 pulse injections are reached at 15 dB. A dual-beam FIB Cross-Section Analysis of the coarse limiter (the limiter closest to the input) revealed an ablation burn hole at the P-I junction after 4 pulse

injections. After 15 pulses, the passivation layer was destroyed, and the I-layer showed signs of burnout. After 40 pulse injections, the complete burnout of the I-layer was observed. After roughly 600 pulse injections the authors speculate that the thick N-layer has burned out, which lead to the deterioration in insertion loss. The results are confirmed by a similar study [54], which concluded that increasing the pulse number or pulse repetition frequency can lower the thermal burnout power threshold of a PIN diode.

2.6 CONCLUSION

The literature relevant to the study of temperature dependence of PIN diode limiters has been introduced in this chapter. A detailed summary of published works in this field has been provided.

From the previous discussion of the thermal influence and temperature effects on PIN diodes, it was found that the carrier lifetime and ambipolar mobility is heavily influenced by temperature change. The carrier lifetime temperature coefficient is the primary parameter that dictates the resistance and reactance versus temperature of a PIN diode and depends heavily on the geometry and passivation of the diode. In a diode limiter, the resistance and reactance of the diode influences various parameters such as the spike leakage, response time, recovery time and attenuation. Various studies that investigated the effect of temperature on PIN diodes focused primarily on the change in diode resistance and limiter attenuation and at frequencies typically outside the VHF band [13] – [20] ([13], [14], [15], [16], [17], [18], [19] [20]). It was found that the resistance of a PIN diode increases with temperature for a carrier lifetime temperature coefficient, $\tau_{\text{coefficient}}$, smaller than 2.3. A typical silicon dioxide passivated PIN diode with a capacitance of 0.1 pF has a carrier lifetime temperature coefficient of around 1.7. Caverly's study does show that a PIN diode's reactance increases with temperature for carrier lifetime temperature coefficients also smaller than 2.3 [20]. However, the study neither specifies whether the reactance is capacitive or inductive, nor does it provide real capacitance values over temperature (only normalised values for the reactance were provided).

No published research documents the effect of temperature on the electrical capacitance of PIN diodes and the result on a PIN diode limiter's transient performance, specifically for PIN diodes in limiters used in applications that operate in the VHF band.

CHAPTER 3 RESEARCH METHODLOGY

3.1 CHAPTER OVERVIEW

The literature study presented in Chapter 2 provided a background on PIN diodes and their application in RF limiters. In this chapter, the research methodology used in this study is discussed. Section 3.2 gives an outline to visually represent and discusses the flow of the research procedure that was followed. The simulation and modelling software that was used is described in Section 3.3, followed by a detailed discussion of the schematic design, component selection, limiter topologies, and PCB layout in Section 3.4. Section 3.5 presents the measurement approach which includes the temperature control, measurement automation, calibration measurement hierarchy, test environment, and various measurement setups. Section 3.6 explains the layout and design of the test PCB that was used to measure the DUT. The method of extracting a small-signal model for a PIN diode, referred to as the parameter extraction process, is described in Section 3.7. A chapter summary is provided in Section 3.8.

3.2 RESEARCH PROCEDURE

The research procedure that was followed during this study is presented in Figure 3.1. The process began with a literature study, which was presented in Chapter 2, and theoretical review of all the aspects of PIN diodes and RF limiters and discussed the effect of temperature on both. The literature study presented various RF limiter topologies and the trade-offs that should be considered during the design stage. Chapter 2 also discussed how temperature influences a PIN diode and which diode properties are more susceptible to temperature variation.

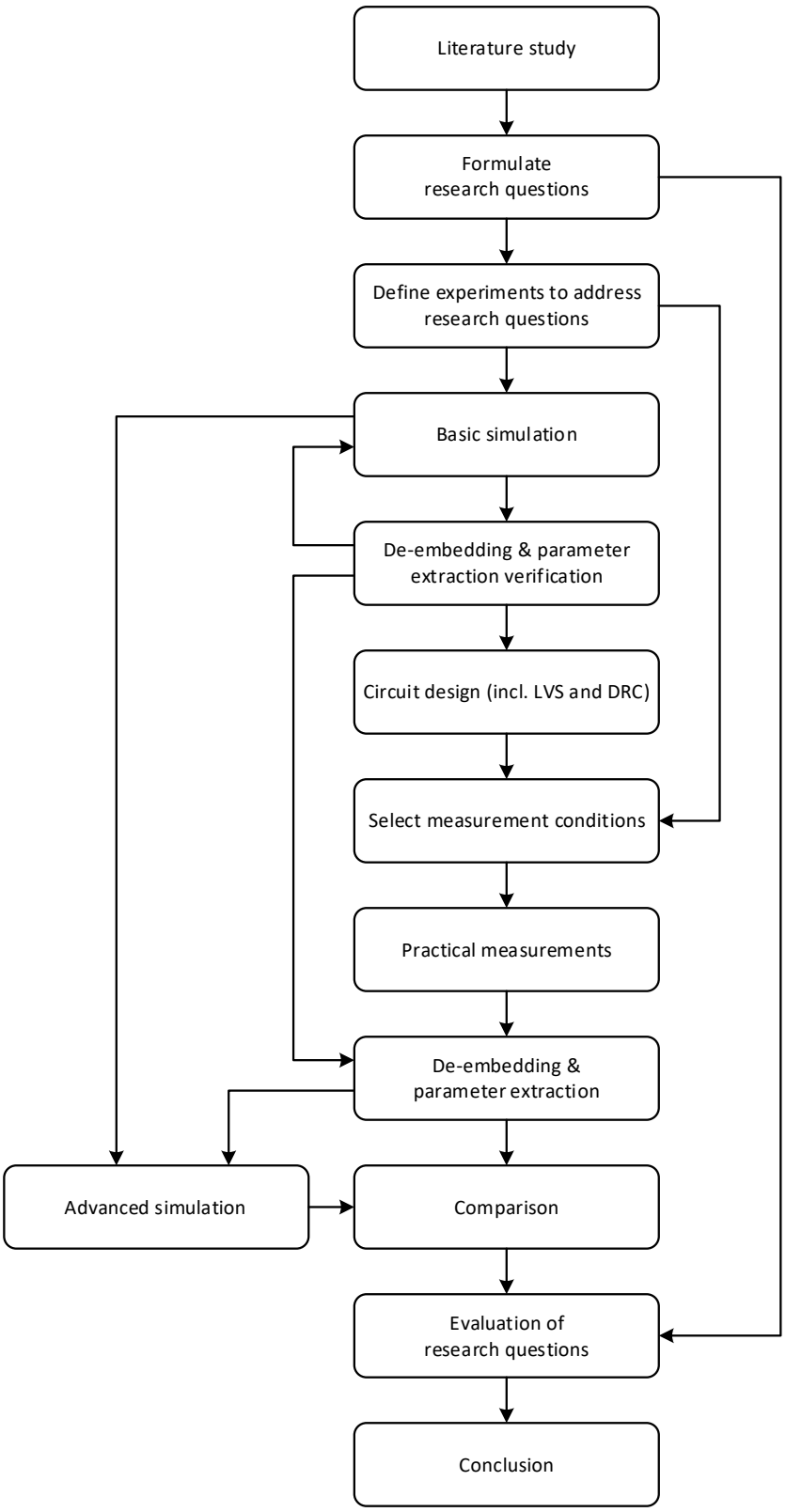


Figure 3.1. Research methodology flow diagram.

The literature study exposed research opportunities which were used to formulate the research questions for this study. Based on the research questions, suitable experiments were identified to address the research questions.

Ideal components and elementary circuit design were found sufficient for basic simulation of both the PIN diode and RF limiter circuits. This method enabled rapid testing and verification so that educated decisions could be made about best circuit design options and calibration setup. The basic simulation was also used to verify the de-embedding and parameter extraction process. This verification test was repeated until agreement was achieved between the extracted and known parameters of the simulation, and until the expected results matched those published in other studies and by manufacturers.

The circuit design was done based on the basic simulation's outcome of the best approach for layout options of the RF limiter, PIN diode and calibration area. The design was sent for manufacturing and components were ordered. The resulting PCB was assembled using the selected components. Measurements were taken at the various data points, which are discussed in the next section, and the data was stored.

Using the parameter extraction algorithm that was developed in conjunction with the basic simulation, the measured data could be processed. Parameters such as the small-signal capacitance, resistance, and inductance of the PIN diode could be extracted from the measured data and used for comparison. The extracted parameters were then used to update the ideal components of the basic simulation to create accurate components models that reflect the measured data. True comparisons were then made between simulated and measured results and the research questions were then evaluated based on the literature study, mathematical models, and simulation results.

3.3 SIMULATION AND MODELLING SOFTWARE

The implementation of this study required careful use of computer aided design (CAD) software to obtain accurate results to validate the hypothesis and provide meaningful results to the proposed research questions. The circuit design and simulation, parameter extraction algorithms and measurement automation scripts cannot be completed without CAD software. During this project, the software applications listed in Table 3.1 were used.

Table 3.1. CAD software.

Software	Application
Cadence's AWR Microwave Office	Used for the simulation (basic and advanced) and analysis of the PIN diodes and limiter circuits. The Robert Caverly PIN diode model, PINDRC, was used to model the PIN diodes.
Altium Designer	Schematic design and PCB layout. Altium was also used Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification.
MATLAB	Mathematical modelling and parameter extraction algorithms. Also used to create the graphs for the results sections.
Visual Studio Code	Used as an editor for the MATLAB scripts.
PyCharm	Used for the development of the measurement automation scripts.

3.4 CIRCUIT SIMULATIONS AND DESIGN

As was briefly described in Table 3.1, Cadence's AWR Microwave Office was used to simulate, evaluate, and analyse different limiter topologies and PIN diode circuit variations. Different types of simulations were done between the PIN diode and limiter circuits.

3.4.1 Simulation types

As discussed in Section 2.5.1, PIN diodes in limiter applications are typically mounted in a shunt configuration and, hence, the PIN diode was simulated as such. The following main simulations were done:

1. Capacitance vs frequency.
2. Capacitance vs bias voltage.
3. Capacitance vs temperature.
4. Forward and reverse resistance vs temperature.

In addition to the simulations above, a combination of these simulations was also done, e.g., keeping the frequency constant and varying the temperature. The objective of the simulations was to determine how the capacitance would change due to different parameters. For these circuit simulations, APLAC's harmonic balance solver was used. APLAC is a high-frequency circuit simulator that is built into the Microwave Office software. The PIN diode model that was used is an implementation of Robert Caverly's PIN diode model [57], PINDRC, which is also included in the Microwave Office software. AWR recommends the Caverly PIN diode model over their in-house model, PINDD, for all types of diode circuit design [58]. A drawback of the Caverly PIN diode model is that is requires many input parameters that are often not provided by the diode manufacturer.

For the limiter circuits, two main simulations were done:

1. Transient response vs temperature.
2. Non-linear response vs temperature.

From these two simulations, the performance characteristics, discussed in Section 2.3.1, of the limiter can be deduced. For the transient circuit simulations, APLAC's transient solver was used, whereas the harmonic balance simulator was used for the non-linear response. From the transient response, the spike leakage, flat leakage, and response time can be measured. From the non-linear response, the threshold and saturation level can be calculated.

The objective of these simulations was to determine how the performance characteristics of the limiter circuits change due to temperature.

3.4.2 Limiter topologies

Three different limiter topologies were selected for this study. The three topologies are the traditional PIN diode limiter, the anti-parallel limiter, and a modified version of a PIN-Schottky limiter. The traditional PIN diode limiter circuit was selected because of its minimalist design and frequent use by limiter diode manufacturers. The limiter schematic is shown in Figure 3.2.

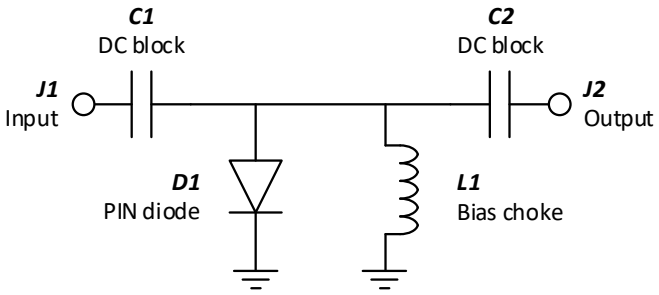


Figure 3.2. Traditional limiter circuit topology.

The anti-parallel limiter circuit was chosen because of its simplistic design which does not require a DC bias choke and improved performance compared to the traditional limiter topology [59]. The PIN diodes were placed as close to each other as possible. The limiter schematic is shown in Figure 3.3.

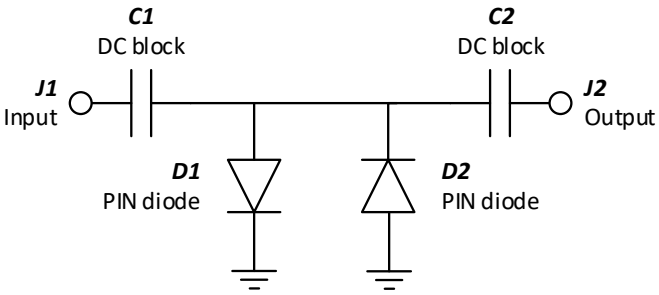


Figure 3.3. Anti-parallel limiter circuit topology.

A modified version of a typical PIN-Schottky limiter circuit shown in Figure 2.13 was chosen to utilise the reverse coupled signal's power to further bias the PIN diode. The limiter schematic is shown in Figure 3.4.

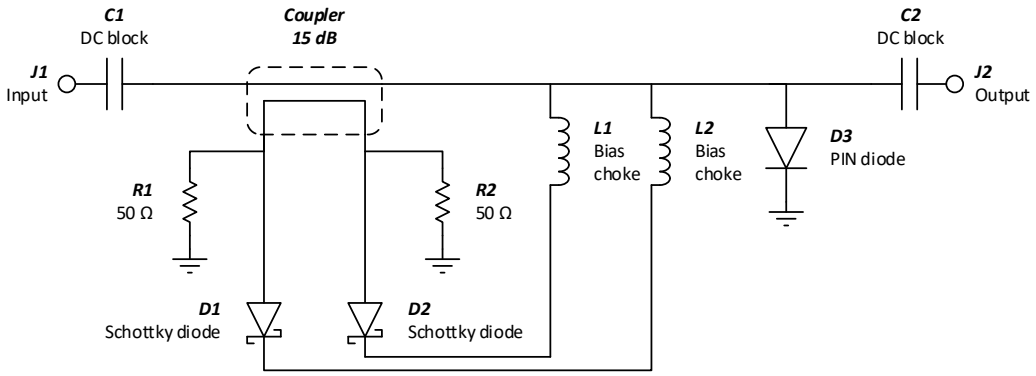


Figure 3.4. Detector limiter circuit topology.

3.4.3 Component selection

The PIN and Schottky diodes were carefully chosen for the purpose of this study. The following sections briefly discusses the component selection process.

3.4.3.1 PIN diodes

Careful attention was paid to the selection of the PIN diodes. A selection of PIN diodes with a high degree of similarity would create near identical results, making it difficult to evaluate the effect of device parameters on measured performance. The criteria for the PIN diode selection were:

1. Different intrinsic region width, W: As was discussed in Section 2.2.1, the intrinsic thickness of a PIN diode determines its response time, spike leakage, and recovery time. It also controls the power handling capability of the diode. Choosing diodes with different intrinsic region widths were essential.
2. Maximum input power: The diode should survive close to a 5-Watt, high-power CW signal in a limiter configuration.

Table 3.2 lists the packaged PIN diodes that were considered for this study.

Table 3.2. PIN diode selection.

Diode name	W (µm)	C_j (pF)	Max CW (W)	Carrier lifetime, τ (ns)
MA4L032	3	0.2 @ 0 V	4	15
MA4L101	13	0.15 @ 0 V	6.3	90
MADL-000301	20	0.2 @ 0 V	7	200
CLA4608	7	0.6 @ -38 V	5	100
CLA4609	20	0.6 @ -30 V	16	1100
CLA4610	4.5	0.32 @ -6 V	8	20
CLA4611	12	0.25 @ -38 V	10	300

The CLA4608, CLA4609, CLA4610 and CLA4611 diodes from Skyworks were chosen to represent a selection of small, medium, and large diodes. Choosing diodes that have the same package footprint was preferred because it simplified the PCB design by not having to accommodate different footprints.

3.4.3.2 Schottky diodes

For the detector limiter topology shown in Figure 3.4, the Schottky diodes are used to bias the PIN diodes through an RF choke. The selection criteria for the Schottky diodes were:

1. Large breakdown voltage, V_b: The breakdown voltage of the Schottky diode must be large enough to withstand the coupled and reflected power going to the PIN diode. The coupled and reflected voltage depends on the maximum expected input power.
2. Low forward voltage, V_f: A lower forward voltage will allow the Schottky diode to start conducting current at a lower input voltage. A low forward voltage was essential because of the diodes' use in conjunction with a coupler.
3. Small series resistance, R_s: A lower series resistance allows for more current to be injected into the PIN diode, which increases the turn-on time.

Table 3.3 lists the packaged Schottky diodes that were considered for this study.

Table 3.3. Schottky diode selection.

Diode name	V_b (V)	V_f (mV)	R_s (Ω)
SMS3923	20	310	10
SMS3924	70	490	11
HSMS-2800-TR1G	70	410	35

The SMS3923 diode, also from Skyworks, was the preferred Schottky diode because of its low forward voltage.

3.5 MEASUREMENT APPROACH

This section discusses the different measurement setups, the measurement procedure and the equipment used to gather the data. The measurement setup is divided into the four configurations below, each of which are briefly explained in their own section.

1. Equipment calibration
2. Small-signal diode characterisation
3. Transient
4. Non-linear

3.5.1 Temperature control

The temperature range of interest is -25 ºC to 100 ºC, which was divided into 25 ºC intervals. For temperatures above 100 ºC, common plastic materials start to melt and special attention must be paid to the RF test cables and connectors. For temperatures below -25 ºC, significant is required to sustain the cold temperature during measurements with little value to gain.

A Highly Accelerated Life Tests (HALT) chamber was used to control and vary the temperature to which the test jig was subjected. A HALT chamber, also referred to as a HALT/HASS (Highly Accelerated Stress Screening) chamber, is a test chamber designed

for the purpose of accelerated stress testing, specifically HALT and HASS. HALT and HASS uses temperature and vibration during the manufacturing process of components or products to compress the time normally required to identify design and process defects. The HALT chamber that was used for this study is shown in Figure 3.5.

Figure 3.5. HALT chamber at Hensoldt GEW Technologies.

All the test equipment, such as the VNA, spectrum analyser, signal generator and power amplifiers, was always kept outside the HALT chamber and at room temperature. Only the DUT was placed inside the HALT chamber and subjected to temperature variations. The test cables that were connected between the DUT inside the HALT chamber and the VNA on the outside will be subjected to changing temperature and are, therefore, of temperature resistant material. Multiple units of a specific PIN diode were available and were installed into the characterisation and limiter circuits beforehand, therefore eliminating the need to move a single PIN diode between circuits.

Because the availability of the HALT chamber is limited, all the measurements were taken at a specific temperature level since it is easier, quicker, and more effective to adjust the test equipment on the outside of the HALT chamber than to regularly adjust the temperature of the HALT chamber. Between each measurement setup, the HALT chamber was brought back down to room temperature before any setup changes are made.

3.5.2 Measurement automation

Numerous individual measurements are required to cover the selection of PIN diodes, limiter topologies and measurement data points, with a high risk of operator error. Therefore, some of the measurement procedures were automated using Python scripts. All the measurement equipment is controllable through a LAN connection, apart from the bench power supply which could only be controlled through a RS-232 serial connection. A LAN connection to the instruments was preferred over a serial connection because of the superior bandwidth, latency advantage, and ease of use (using common LAN cables and network switch compared to multiple specialised USB-to-serial adaptors). The Virtual Instrument Software Architecture (VISA) library was used to connect to the various instruments from a test computer, and Standard Commands for Programmable Instruments (SCPI) commands were used to configure, control, and read from the instruments. Although the VISA library was available in other software languages like MATLAB and C #, Python was preferred given the author's prior knowledge of the language. The automation of specific measurement procedures is discussed in the relevant sections below.

3.5.3 Calibration and de-embedding

3.5.3.1 Calibration

To extract the parameters of interest from the PIN diode, careful and precise measurements are required. Nonlinear models are derived from the linear equivalent circuit models which are extracted from linear S-parameters and various DC measurements. These S-parameters are measured using a vector network analyser, or VNA, which measures both the magnitude and phase of the complex S-parameters of a device for a specific bias condition. Such

measurements are also called small-signal measurements. Before the S-parameters of a device can be measured, however, a calibration process must be followed. Calibration ensures that the measurement reference plane is shifted to the ports of the DUT.

Calibration is performed as an accuracy enhancement procedure that removes systematic errors from the instrument hardware that can cause uncertainty when measuring a DUT [60]. Systematic errors include imperfect impedance and terminations at the ports of the VNA, reflections and losses caused by the VNA hardware, test cables and connectors, and any internal signal leakage between the VNA ports [61]. During calibration, the instrument measures known and well-defined calibration standards and mathematically compare the results with ideal models of these standards. Calibration is a very important step to achieve accurate and meaningful measurement results.

Because the DUT (the PIN diode) is installed onto a PCB or test jig and because of the difference in temperature that will occur between the outside room and inside the HALT chamber, a two-tier calibration procedure is required. A two-tier calibration procedure means that two calibration methods are required to move the measurement reference plane from the VNA to the DUT. An example of a two-tier calibration setup is shown in Figure 3.6. Common calibration methods for both connector and PCBs include short-open-load-thru (SOLT), thru-reflect-line (TRL) and thru-reflect-match (TRM) [62]. The SOLT and TRL techniques are frequently used for connectors and PCBs, respectively. However, for lower frequencies, the line standard of the TRL technique becomes infeasibly long as the wavelength increases. For frequencies inside the VHF band, the line standard's length would be impractical to manufacture on a PCB. For this reason, the TRM calibration standard was chosen. For the VNA cable calibration, the SOLT calibration standard was chosen because the calibration kits are readily available and are highly accurate up to and beyond 6 GHz, which make it sufficient for the frequency band required for this work.

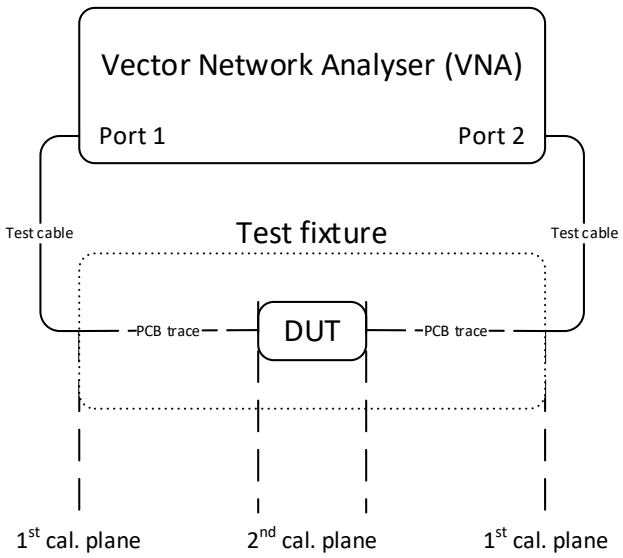


Figure 3.6. Two-tier calibration reference plane.

The first procedure is to move the reference plane to the end of test cable through calibration, and the second to move the reference plane to the DUT through a process called de-embedding.

3.5.3.2 De-embedding

De-embedding refers to the process of removing the effects of a test fixture around a DUT from measured data. During the de-embedding process, a model of the test fixture, such as the calibration standards (TRM in this case), are mathematically removed from the measurement network parameters. In its simplest form, the measured data can be represented as three cascaded networks using the (3.1):

$$[M] = [A][DUT][B], \tag{3.1}$$

where

$[M]$ are the measured network parameters,

$[A]$ represents the transmission parameters of the test fixture of port A,

$[DUT]$ are the DUT's network parameters, and

$[B]$ represents the transmission parameters of the test fixture of port B.

General matrix theory states that if a matrix determinate is not equal to zero, the matrix has an inverse. By multiplying any matrix by its inverse will result in the identity matrix. Therefore, by multiplying the transmission parameters of the test fixture by its inverse, as is shown in (3.2), the network parameters of the DUT can be determined.

$$[DUT] = [A]^{-1}[M][B]^{-1}, \tag{3.2}$$

where

$[M]$ are the measured network parameters,

$[A]^{-1}$ represents the inverse transmission parameters of the test fixture of port A,

$[DUT]$ are the DUT's network parameters, and

$[B]^{-1}$ represents the inverse transmission parameters of the test fixture of port B.

Equation (3.1) and (3.2) are simplified for the purpose of readability. The de-embedding process used for this study is based on a generalised TRM calibration theory developed in [63].

3.5.3.3 Setup

The two calibration reference planes are shown in Figure 3.7. The custom plate is omitted for clarity purposes.

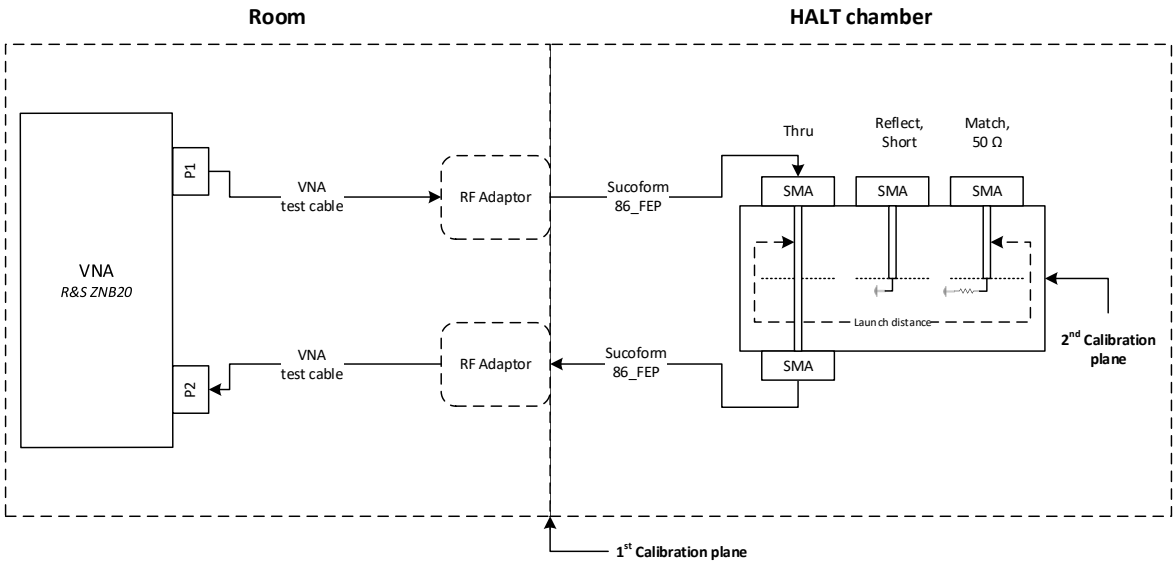


Figure 3.7. Calibration measurement setup and reference tiers.

The first reference plane is before the HALT chamber door at the end of the VNA test cables. The calibration method for the first tier is SOLT. A 3.5 mm, SOLT, precision calibration kit was used. The VNA and test cables are kept at room temperature throughout the test procedure and, therefore, is only be calibrated once.

The second reference plane is located at the pads of the DUT as shown in Figure 3.6. The test cables are connected to the VNA through RF barrel adaptors located on the outside the HALT chamber. Because the DUT and cables inside the HALT chamber are subjected to the different temperatures, calibration is required at each temperature interval.

3.5.3.4 Equipment

The VNA used for this measurement was the Rohde & Schwarz ZNB20 vector network analyser which is, amongst other measurement equipment, shown in Figure 3.8. The ZNB-20 was preferred over other available vector network analysers like the ZVL-13 because of its built-in bias-tees, which was useful during the instrument's calibration and diode's small-signal characterisation measurements.

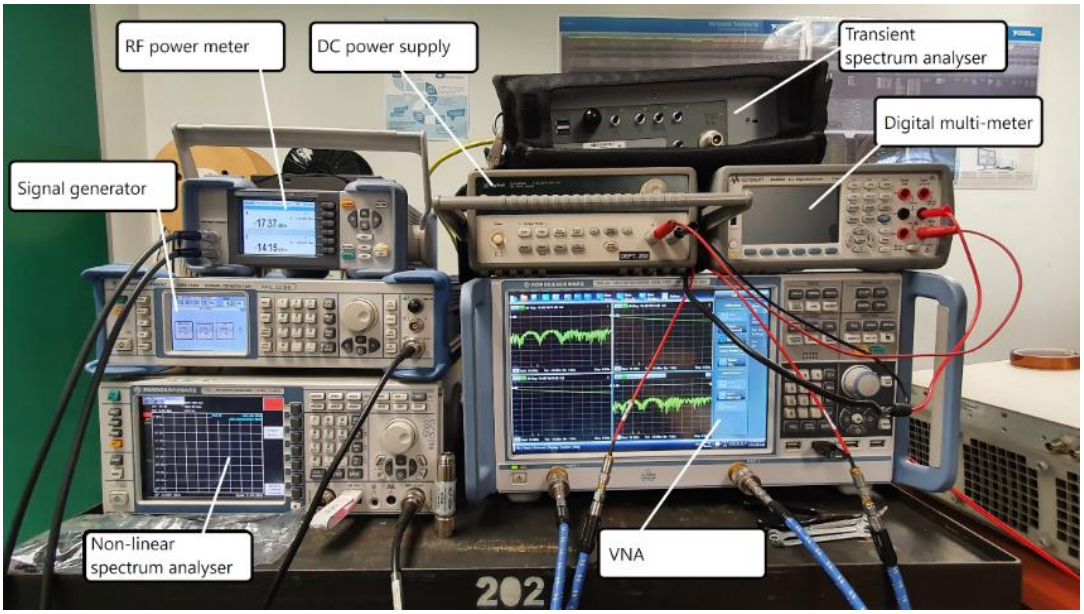


Figure 3.8. Measurement equipment.

3.5.3.5 Tier 1 calibration procedure (VNA)

Even though the frequency range for this study was primarily 30 – 300 MHz, for small-signal (S-parameter) measurements the VNA measurement range was increased to 10 – 6000 MHz. The additional frequency data can hold valuable information without any time penalty or additional setup. The frequency sweep points were increased from the default value to 1001 and the measurement bandwidth set to 1 kHz. A 1 kHz bandwidth presents a fair trade-off between dynamic range and measurement speed. An average was used for each measurement to prevent any outlier data points. The average was set to 5 and was cleared for each measurement iteration. After the VNA was configured, a full 2-port calibration using a SOLT calibration kit was performed.

3.5.3.6 Tier 2 calibration procedure (De-embedding)

The second tier TRM de-embedding calibration setup started with the thru calibration standard. Each calibration standard was measured at each temperature increment and the measurement saved as an S2P file. The standards were altered after a full temperature cycle. The measurements were conducted on the VNA using the same settings and prior to the diode's small-signal characterisation in the next section.

3.5.4 Small-signal measurements

3.5.4.1 Setup

The purpose of this test is to characterise each of the PIN diodes discussed in Section 3.4.3.1 individually in the configuration that will be used in the limiter circuit. The objective was to measure and capture the S-parameter data for each diode at different temperatures and bias voltages over a range of frequencies. Using the S-parameter data and through a parameter extraction process (which is described in Section 3.7) the capacitance versus reverse voltage and current versus voltage curves can be determined. The PIN diode small-signal measurement setup is shown in Figure 3.9.

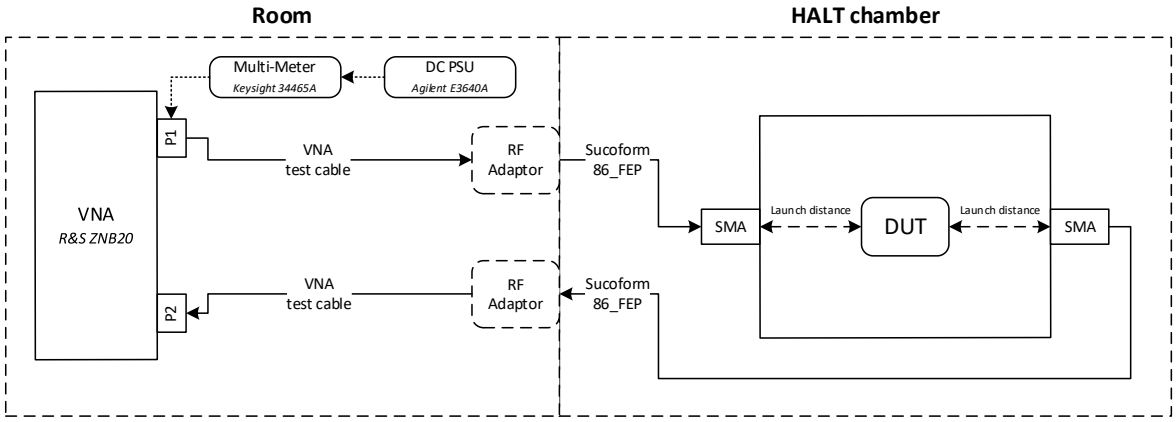


Figure 3.9. Diode small-signal characterisation measurement setup.

3.5.4.2 Equipment

The test setup uses the same Rohde & Schwarz ZNB20 vector network analyser as before, but with the addition of a bench power supply and a digital multi-meter. The small-signal measurement also used the 5-point average, which was cleared for each measurement iteration. For this measurement, an Agilent E3640A 20 V/1.5 A DC power supply and Keysight 34465A digital multi-meter was used. The bench power supply and digital multi-meter were used to bias and measure the current through the DUT, respectively. Both the power supply and multi-meter is shown in Figure 3.8. The power supply was connected to a BNC connector at the back of the VNA to supply voltage to the bias-tee through the multi-meter to measure the current.

The small-signal measurements used the same VNA settings that was discussed in Section 3.5.3.5. The DC bias voltages for the are given in Table 3.4. A large negative bias voltage is desired for capacitance extraction, whereas a positive bias voltage is used to determine the current-voltage (IV) curve, the forward resistance, and lead inductance of the PIN diode. The positive bias voltage is limited by the 250-mA port bias current fuse on the VNA. For simplicity, the voltages were divided into four sections. For the first section, -20 V to -10 V, a step voltage of 5 V is chosen since it was shown through simulation and literature review that there should be no significant change in capacitance between these voltages [64]. Between -10 V and -1 V, a step voltage of 1 V is chosen because the

capacitance is expected to start levelling out at the voltages. For voltages between -1 V and 3V, a step voltage of 0.1V is chosen because the model parameters vary rapidly as the diode transitions between the off and on state and, therefore, greater resolution is required.

Table 3.4. DC bias voltages for small-signal measurements.

Section	Start Voltage (V)	Stop Voltage (V)	Step Voltage (V)
1	-20	-10	5
2	-10	-1	1
3	-1	0	0.1
4	0	3	0.1

3.5.4.3 Procedure

The procedure was completed in the following order:

1. Set the temperature of the HALT chamber to the first index and allow the temperature to settle.
2. Set the DC bias voltage to the first index given in Table 3.4.
3. Measure the frequency response on the VNA and save the output as an S2P file. Clear the measurement average with each iteration.
4. Record the power supply voltage and current measured on the multi-meter.
5. Repeat step 3 and 4 for each DC bias voltage iteration given in Table 3.4.
6. Repeat steps 1 through 5 for each temperature iteration. With each iteration, allow the temperature to settle.
7. Bring the HALT chamber to room temperature and allow the temperature to settle. Power down the HALT system.
8. Repeat steps 1 through 7 for each diode discussed in Section 3.4.3.1.

3.5.4.4 Automation

The automation process for the PIN diode small-signal measurement procedure is shown in Figure 3.10. The program requires the user to select which diode is currently installed and should be measured. The program then asks the user to select the temperature at which the

measurements will be made. Before commencing with the measurements, the program prompts the user to verify that the power supply cables are correctly connected for either a positive or negative bias voltage, since failure to correctly connected the supply cables can damage the DUT or equipment. The program then proceeds to loop through all the DC bias voltages. It sets the voltage on the bench power supply, clears, and then waits for the average on the VNA before taking the measurement and saving the result to the test computer. Finally, it measures the current through the diode on the multi-meter and appends the result to the IV data file. The program will prompt the user again to alter the supply cables when transitioning between positive and negative bias voltages. Once finished with all the DC bias voltages, the program returns to the list of temperatures and waits for a user input. If all the temperatures are done, the program returns to the list of PIN diodes.

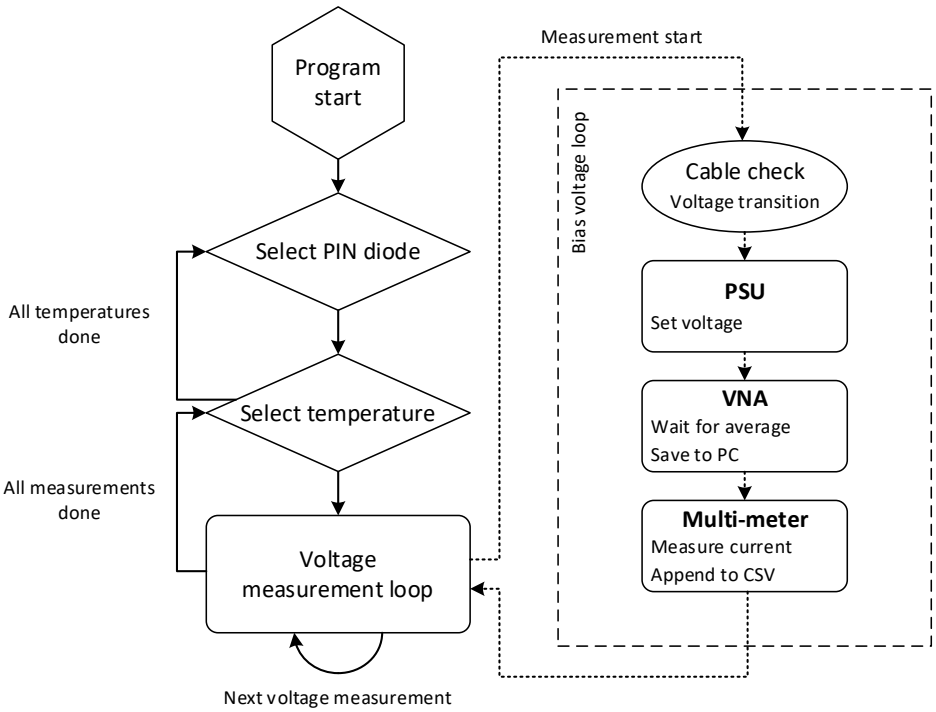


Figure 3.10. Diode small-signal characterisation measurement automation process.

3.5.5 Transient measurements

3.5.5.1 Setup

The purpose of this test is to measure the spike and flat leakage, and recovery time of the PIN diode limiter through transient analysis. The objective was to determine what effect temperature, incident signal frequency and limiter topology has on the spike leakage of a PIN diode limiter. The equipment that was used for this measurement and which are discussed in this section provided the data directly without the need to apply post-processing techniques. The test setup to measure the transient response of a limiter circuit is shown in Figure 3.11.

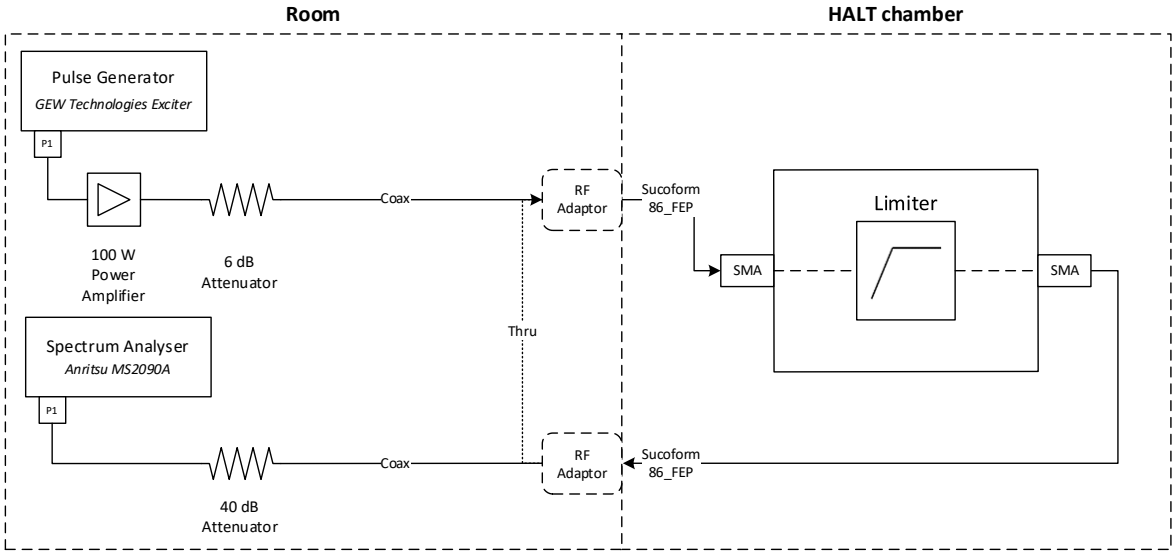


Figure 3.11. Limiter transient response measurement setup.

3.5.5.2 Equipment

A pulse generator, or exciter, provided by GEW Technologies was used to produce a continuous wave incident pulse. The pulse generator is, amongst other equipment, shown in Figure 3.12. Although the performance and characteristics of GEW Technologies' exciter is confidential, it uses DDS (direct digital synthesis) to produce an analogue waveform by generating a time-varying signal in digital form and then performing a digital-to-analogue conversion. Since the operation within a DDS device is mostly digital, it offers very fast switching between frequencies. The pulse generator was configured to produce a square

wave modulated sinusoid with an output power of 0 dBm. The pulse had a 1.2 µs duration which is long enough to allow the limiter circuit to start limiting.

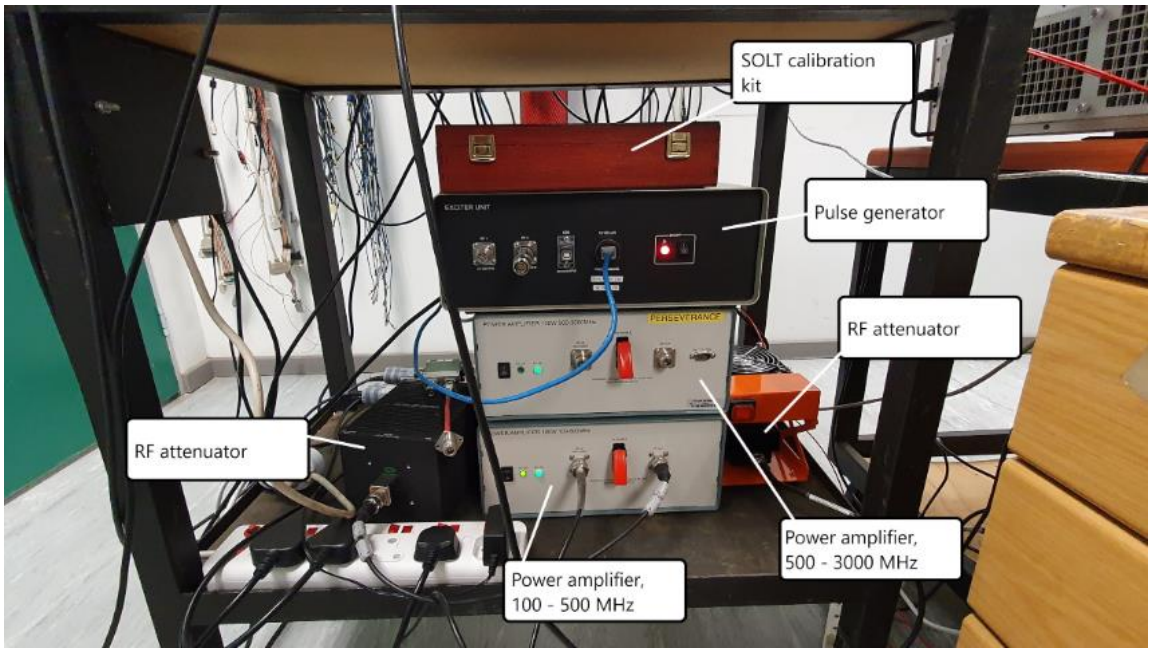


Figure 3.12. Measurement equipment continued.

The pulse frequencies were divided into two bands depending on the equipment. Equipment such as the RF power amplifiers (PAs) and couplers are frequency dependent and had to be changed depending on the frequency iteration to function optimally. The pulse frequencies are given in Table 3.5.

Table 3.5. Transient frequencies.

Frequency (MHz)	Band	Motivation
100	Band 1	VHF band
300		
500	Band 2	Intermediary frequency
1000		Manufacturer listed frequency
2000		The designed coupler was optimised at this frequency

To increase the power level of the RF signal generated by the pulse generator to a level sufficient to trigger the limiter circuit, RF power amplifiers were used. Two, 100-Watt (50 dBm) amplifiers were used that individually cover 100 – 500 MHz, and 500 – 3000 MHz. With reference to Table 3.5, the 100 – 500 MHz PA was used for frequencies inside Band 1, and the 500 – 3000 MHz PA was used for frequencies inside Band 2. The power amplifiers are RFcore™ modules that are fitted into custom boxes which were provided by GEW Technologies.

A 300-Watt, 6 dB RF attenuator shown in Figure 3.13 was placed after the power amplifier to protect the power amplifier against reflected signals when the limiter is active. To distinguish and measure the difference between the incident pulse and the limiter's response, first a thru measurement is done to record the incident pulse.

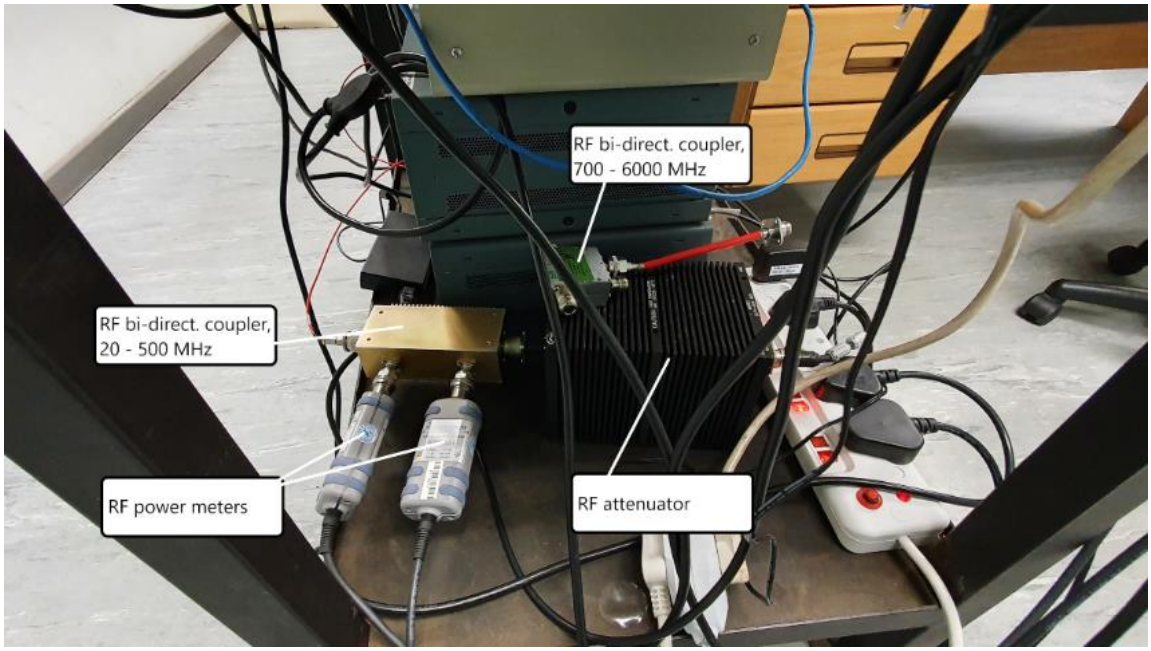


Figure 3.13. Measurement equipment continued.

The thru measurement was done at room temperature outside the HALT chamber. The limiter's response was measured on an Anritsu MS2090A handheld spectrum analyser that was configured in zero-span (time domain) mode. The spectrum analyser is shown in Figure 3.6. A 40 dB attenuator, shown in Figure 3.12, was placed before the spectrum analyser to

reduce the power level to a safe level to not damage the sensitive front-end of the spectrum analyser. The 40 dB attenuation is later mathematically added to the measured signal.

3.5.5.3 Procedure

The procedure was completed in the following order:

1. Set the temperature of the HALT chamber to the first index and allow the temperature to settle.
2. Set the frequency on the pulse generator to the first index given in Table 3.5.
3. Initiate the pulse on the pulse generator. On the spectrum analyser, save the output as an image and CSV file.
4. Repeat steps 2 and 3 for each frequency iteration given in Table 3.5.
5. Repeat steps 2 through 4 for each temperature iteration.
6. Bring the HALT chamber to room temperature and allow the temperature to settle. Power down the HALT system. Repeat steps 1 through 5 for each limiter topology discussed in Section 3.4.2.
7. Bring the HALT chamber to room temperature and allow the temperature to settle. Power down the HALT system.
8. Repeat steps 1 through 7 for each diode discussed in Section 3.4.3.1.

3.5.6 Non-linear

3.5.6.1 Setup

The setup to measure the non-linear output power response of a limiter circuit is shown in Figure 3.14. The purpose of this test is to measure the non-linear attenuation response of a limiter circuit to a high-power incident signal with varying power levels and frequency at different temperatures. The objective was to determine the input versus output power curve of the limiter circuit at different temperatures, and to compare the different topologies and PIN diodes.

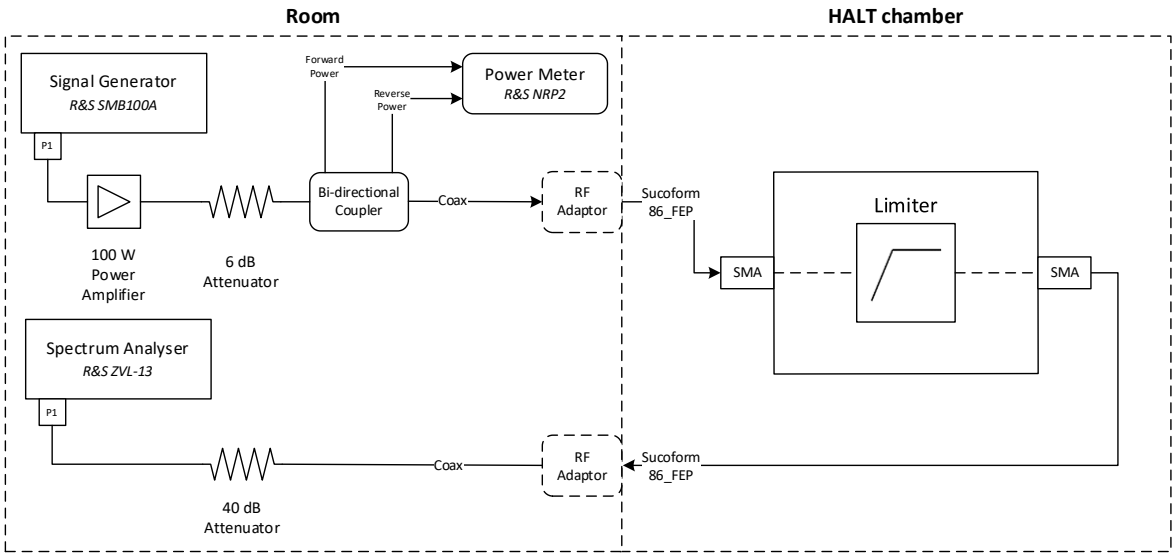


Figure 3.14. Limiter non-linear attenuation response measurement setup.

3.5.6.2 Equipment

A Rohde & Schwarz SMB100A signal generator, which is shown in Figure 3.8, was used to control the frequency and output level for the non-linear limiter measurements. The signal generator was configured with the same frequencies given in Table 3.5. The output power was set to -40 dBm at the start of each frequency iteration and increased in 1 dB increments to a maximum of 5 dBm. The same 100 W PAs units as the previous measurement were used during this measurement.

A 20 – 500 MHz, 200W, 40 dB Werlatone bi-directional coupler was used to sample the forward and reflected power for the frequency bands below 500 MHz. For frequencies higher than 500 MHz, a 700 – 6000 MHz, 250W, 40 dB Werlatone bi-directional coupler was used. A Rohde & Schwarz NRP2 power meter, shown in Figure 3.8, was used with two Rohde & Schwarz NRP-Z81 wideband power sensors, shown in Figure 3.13, to measure and record the forward and reflected power of the limiter circuit. The limiter's response was measured using a Rohde & Schwarz ZVL-13 vector network analyser, shown in Figure 3.8, in its spectrum analyser mode.

3.5.6.3 Procedure

The procedure was completed in the following order:

1. Set the temperature of the HALT chamber to the first index and allow the temperature to settle.
2. Set the frequency on the signal generator to the first index given in Table 3.5.
3. Set the centre frequency on the spectrum analyser to the current frequency iteration. Add a marker on the centre frequency.
4. Set the signal power level to the start level.
5. Note and record the peak amplitude as displayed by the marker.
6. Note and record the forward and reverse power on the power meter.
7. Repeat steps 4 through 6 for each signal power level iteration.
8. Repeat steps 2 through 7 for each frequency iteration given in Table 3.5.
9. Repeat steps 1 through 8 for each temperature iteration.
10. Bring the HALT chamber to room temperature and allow the temperature to settle. Power down the HALT system. Repeat steps 1 through 9 for each limiter topology discussed in Section 3.4.2.
11. Bring the HALT chamber to room temperature and allow the temperature to settle. Power down the HALT system.
12. Repeat steps 1 through 11 for each diode discussed in Section 3.4.3.1.

3.5.6.4 Automation

The automation process for a limiter's non-linear response measurement is shown in Figure 3.15. The non-linear program also requires the user to select which diode is currently installed and should be measured. The program then asks the user to select the current limiter topology that will be measured, followed by the temperature at which the measurements will be made. Before commencing with the measurements, the program prompts the user to verify that the equipment, such as the power amplifier and bi-directional coupler, is correctly connected for the frequency that is to be measured, since failure to connect the correct frequency-dependent equipment can result in degraded performance and, therefore,

inaccurate results. The non-linear automation program loops through the different frequency points and, within the frequency loop, loops through the signal generator power levels. Inside the frequency loop, the program sets the frequency on both the signal generator and spectrum analyser to the current measurement frequency and initiates the output power loop to the starting power level. Inside the power loop, the program sets the power level on signal generator to current loop value and after a short delay, measures the limiter's output power on the spectrum analyser and appends the results to the data file. The program also records the forward and reflected power level to and from the limiter on the power meter and appends the result to the same data file. To protect the DUT, the program checks if the forward power level is more than the absolute maximum power rating as specified by the diode manufacturer and aborts the power level loop if true. If false, the power level loop continues.

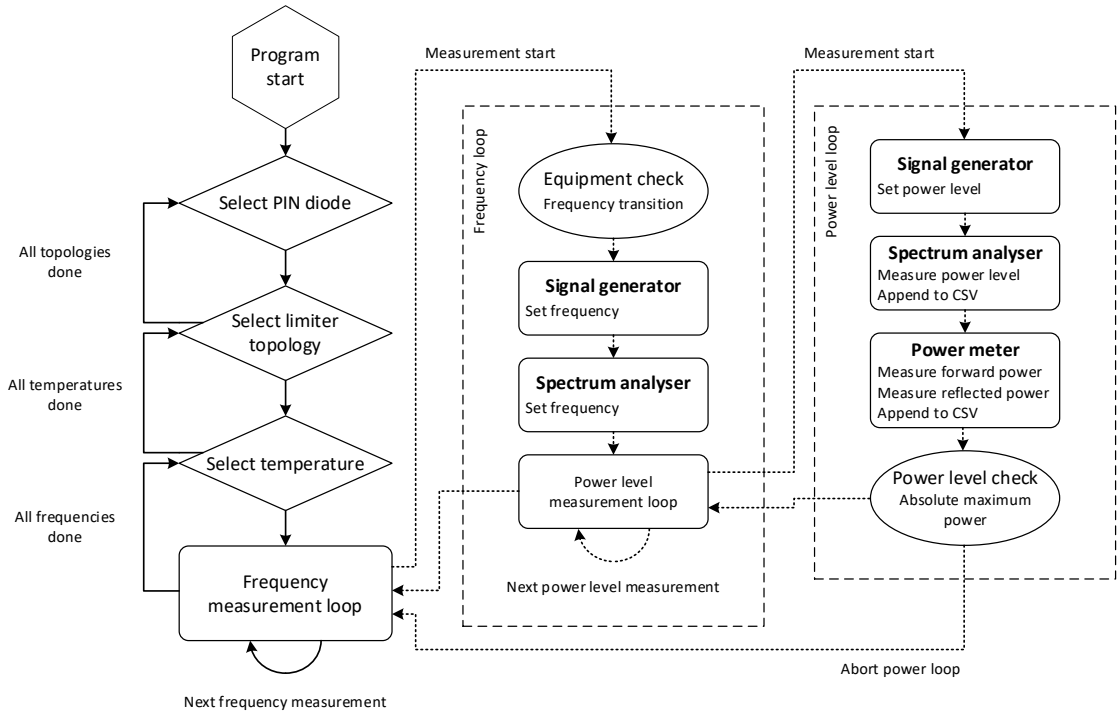


Figure 3.15. Limiter non-linear response automation process.

Once finished with the power level loop, the program returns to the frequency loop for the next frequency iteration. If all the frequencies are done, the program returns to the list of temperatures and waits for a user input. If all the temperatures are done, the program returns to the list of limiter topologies, after which it returns to the list of PIN diodes.

3.6 TEST PCB

The PCB was manufactured on a 0.5mm thick Rogers RO4003C. A 3D render of the PCB is shown in Figure 3.16. SMA connectors were used to transition between the test cables and PCB because they are affordable and perform well in the frequencies used during measurements. At the top of the PCB is the coupler that was designed for the detector limiter circuit topology that was discussed previously. The coupler characterisation area allows to easily measure and verify the performance of the coupler against the simulation. Below the coupler are the three limiter topologies. From top to bottom they are the detector limiter topology (which uses the designed coupler), the anti-parallel limiter topology, and traditional shunt PIN diode limiter topology.

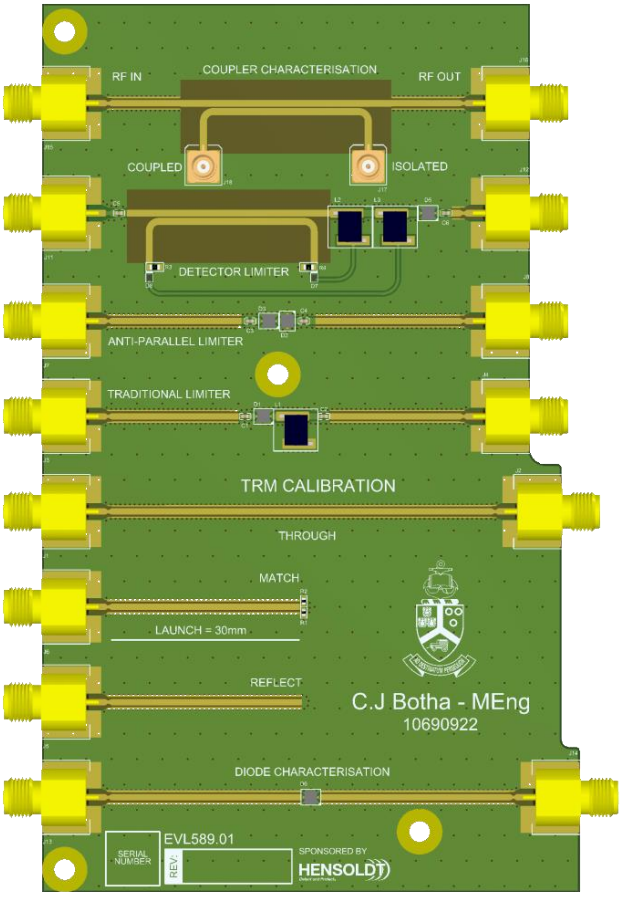


Figure 3.16. Rendered PCB layout in Altium Designer.

Below the limiter topologies are the TRM calibration standard. The TRM calibration standards were implemented as follow:

Thru: A zero-length thru was chosen to minimise reflections and losses.

Reflect: A short (to ground) was chosen as the high-reflection standard.

Match: The low-reflection standard was chosen to be 50 Ω (two 100 Ω resistors in parallel) to mimic the characteristic impedance of the microstrip line.

A 30 mm launch distance is added to all the calibration standards and the DUT characterisation circuit to allow any higher-order modes from the connector to microstrip transition to attenuate so it does not interfere with the calibration. The launch was not added to the coupler characterisation or limiter topologies since these circuits are not part of the de-embedded measurements for circuit modelling. At the bottom is the DUT characterisation circuit.

Mounting holes were added to the PCB so that the PCB can be mechanically fixed to a custom metal base plate. The PCB containing the DUT was mounted to the base plate, which forms the test jig shown in Figure 3.17, using standoffs and nuts to keep the PCB secure. The test jig allowed for easier handling of the PCB during setup changes. The test jig was placed in the HALT chamber and mechanically fixed to the HALT chamber floor using bolts for the duration of the test procedure.

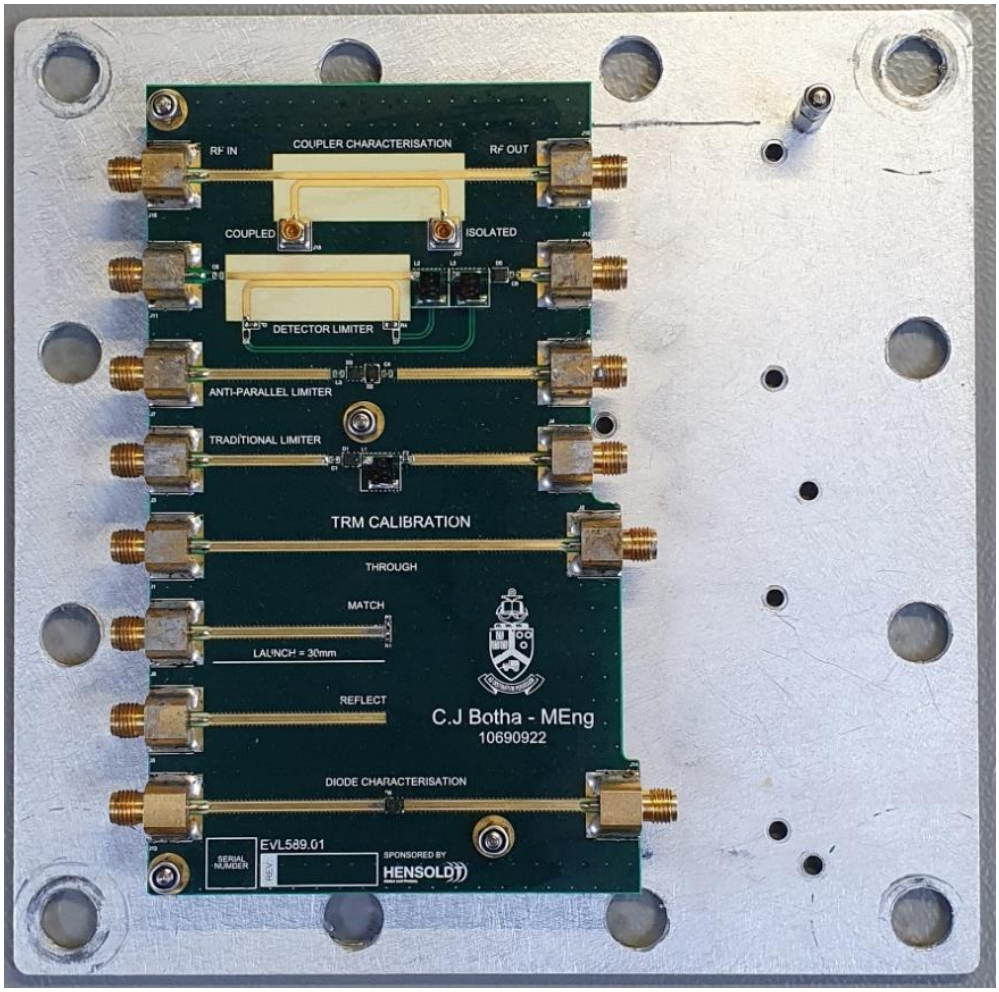


Figure 3.17. PCB test jig.

3.7 PARAMETER EXTRACTION

An important aspect of this study is to investigate the change in capacitance of a PIN diode due to temperature variation. This section is dedicated to a discussion on how the capacitance and other diode parameters were calculated using de-embedded S-parameter data and parameter extraction techniques. Parameter extraction is the process of finding appropriate values for the parameters of a circuit model such that the simulated and measured results correlate with one another.

Figure 3.18 shows the forward and reverse biased equivalent circuit models for a PIN diode that includes the package parasitic parameters. Equivalent circuit models in general are only an estimation of the physical component or device and, therefore, may differ in setup or simulation.

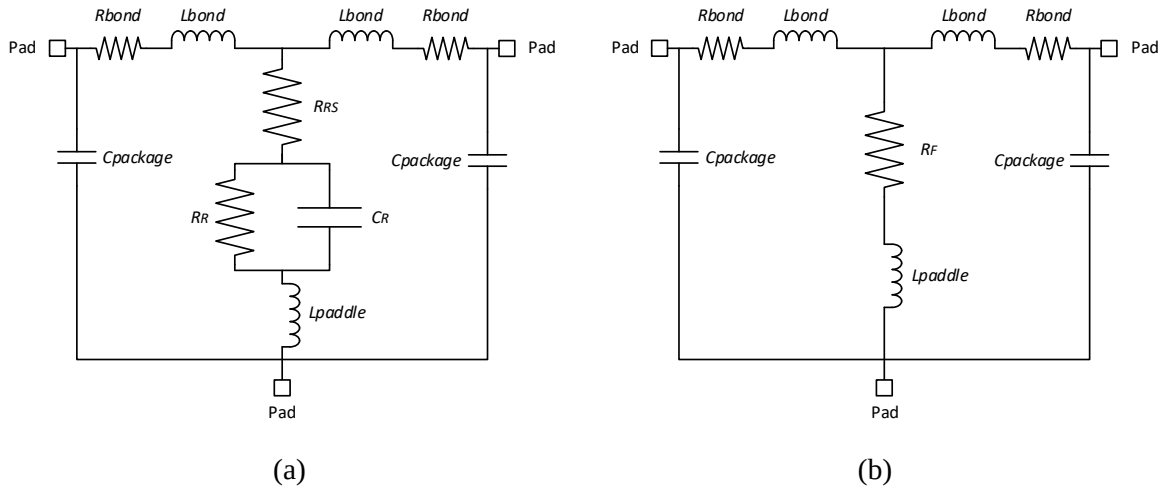


Figure 3.18. PIN diode equivalent circuits including package parameters.
(a) Reverse biased. (b) Forward biased.

Using parameter extraction, the equivalent circuit model of a PIN diode can be populated with accurate values. From the equivalent circuit model, the reverse biased capacitance, C_R, can be monitored.

The parameter extraction process work as follows. The TRM de-embedding standards and small-signal characterisation measurements from Section 3.5.3 and Section 3.5.4, respectively, are used to create the de-embedded DUT measurement. The de-embedding process is repeated for each small-signal measurement and uses the TRM de-embedding standards measurement for the relevant temperature point. The algorithm was developed using MATLAB.

Once the DUT's response has been de-embedded using (3.2), its de-embedded S-parameters are converted into ABCD-parameters using (3.3) through (3.6).

$$A = \frac{(Z_1^* + S_{11}Z_1)(1 - S_{22}) + S_{12}S_{21}Z_1}{2S_{21}\sqrt{R_1 R_2}}, \tag{3.3}$$

$$B = \frac{(Z_1^* + S_{11}Z_1)(Z_2^* + S_{22}Z_2) - S_{12}S_{21}Z_1Z_2}{2S_{21}\sqrt{R_1R_2}}, \quad (3.4)$$

$$C = \frac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{2S_{21}\sqrt{R_1R_2}}, \text{ and} \quad (3.5)$$

$$D = \frac{(1 - S_{11})(Z_2^* + S_{22}Z_2) + S_{12}S_{21}Z_2}{2S_{21}\sqrt{R_1R_2}}, \quad (3.6)$$

where

Z_1^* is the conjugate of the impedance of Port 1,

Z_1 is the characteristic impedance of Port 1 (Ω),

R_1 is the real part of the characteristic impedance of Port 1 (Ω),

R_2 is the real part of the characteristic impedance of Port 2 (Ω),

Z_2^* is the conjugate of the impedance of Port 2, and

Z_2 is the characteristic impedance of Port 2 (Ω).

For PIN diode circuits shown in Figure 3.18, the equivalent T-circuit can be presented as is shown in Figure 3.19. The parameters Z_1 and Z_2 represent the combined impedance of $C_{package}$, R_{bond} and L_{bond} in the series branch, whereas Y represents the admittance of the shunt branch. The package capacitance, $C_{package}$, is not provided by the diode manufacturer and could not be accurately calculated because of its small value. It was therefore assumed that $C_{package}$ is approximately 0.

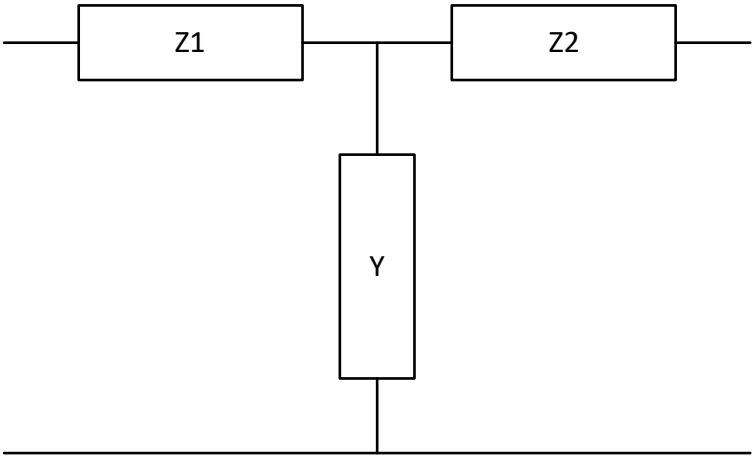


Figure 3.19. T-branch equivalent circuit.

The branch impedance and shunt admittance can be deduced from the ABCD parameters of the circuit using (3.7).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} (1+YZ_1) & (Z_1+Z_2+YZ_1Z_2) \\ Y & (1+YZ_2) \end{bmatrix}. \quad (3.7)$$

Using the shunt admittance, Y, the capacitance and other parameters were extracted from the data. Equally, using the branch impedances, Z_1 and Z_2, parameters like the series resistance, bond wire inductance and package capacitance were extracted.

Different parameter extraction techniques have been developed and ranges from direct extraction to optimisation-based algorithms [65]. However, both methods must deal with the ill-conditioned nature of the extraction problem, which makes determining a unique equivalent model for a device difficult. This ill-conditioned behaviour of extraction is prevalent in parasitic elements such as lead or bond inductances, or package capacitances, due to the small effect they have on the measured data. Using a multi-bias approach that combines S-parameter data from multiple bias points into an integrated parameter extraction algorithm has demonstrated to be effective in extracting a distinctive set of model parameters [66].

3.7.1 Multi-bias parameter extraction

For this study, a multi-bias approach was implemented. The parameter, L_{padde}, does not change with bias voltage and is, therefore, bias independent. Its value remains constant even when the PIN diode is reverse biased. However, when the diode is reverse biased, the diode's capacitance, C_R, dominates the imaginary part of the shunt impedance at low frequencies which makes it difficult to accurately determine the value of both C_R and L_{paddle}. When the PIN diode is forward biased, there exists little to no junction capacitance in the shunt branch of the diode and the paddle inductance dominates the imaginary component of the impedance at higher frequencies. For this reason, the parameter extraction process started with the forward biased model. Using the de-embedded S-parameter data, the forward biased series and shunt branch impedances were calculated according to (3.7).

In addition to using a multi-bias parameter extraction approach, a frequency-assisted approach was also implemented. This means that, instead of calculating the value of a specific parameter across the whole measured frequency range (10 – 6000 MHz), the frequency scope was focussed on where parameter is dominant. This led to less variation in parameter value across different bias voltages and a more accurate model.

3.7.2 Forward biased parameter extraction

The total shunt impedance for a forward biased PIN diode at 3 V is given by (3.8). The best-fit value of L_{paddle} was extracted at the highest bias voltages given in Table 3.4 using (3.9). The inductance was calculated at frequencies between 4000 MHz and 6000 MHz where the inductive reactance is dominant.

$$Z_{3V} = R_F + j\omega L_{paddle}, \tag{3.8}$$

$$L_{paddle} = imag(Z_{3V})/\omega, \tag{3.9}$$

where

Z_{3V} is the complex shunt impedance at 3V (Ω), and

ω is the angular frequency.

The value of L_{paddle} was averaged across the three highest bias voltages to obtain a stable value which was used as a constant to extract the value of reverse-biased parameters, like C_R, more accurately.

3.7.3 Reverse biased parameter extraction

The total shunt impedance for a reverse biased PIN diode is given by the following equation.

$$Z_R = R_{RS} + R_R||(\frac{1}{j\omega C_R}) + j\omega L_{paddle}, \tag{3.10}$$

where

Z_R is the shunt impedance at a given reverse voltage (Ω),

R_{RS} is the reverse biased series resistance (Ω),

R_R is the reverse biased parallel resistance (Ω),

C_R is the junction capacitance (pF),

L_{paddle} is the previously calculated paddle inductance, and

ω is the angular frequency.

Solving for (3.10) required various assumptions and frequency-specific parameter extraction algorithms. Values for the parameters were first calculated numerically, whereafter they were refined using MATLAB's nonlinear regression function. This combination proved to be the most accurate compared to using just the one or the other.

Looking into the shunt the branch, the series resistance, R_{RS}, dominates the real component of the total impedance since the parallel resistance, R_R, is much smaller than the impedance of the parallel capacitance, C_R. On the assumption that the parallel resistance is zero, the series resistance was initially calculated according to (3.11).

$$R_{RS} = real(Z_R). \tag{3.11}$$

With the knowledge of the paddle inductance and series resistance, the parallel capacitance, C_R, and resistance, R_R could be calculated as shown in (3.12).

$$R_R||(\tfrac{1}{j\omega C_R}) = Z_R - R_{RS} - j\omega L_{paddle}. \tag{3.12}$$

Inverting the impedance to admittance allows for easier parallel computation and capacitance calculation. The initial parallel capacitance, C_R, and resistance, R_R was then calculated using (3.13) through (3.15).

$$Y_R = {}^{1}\!/_{R_R||(\frac{1}{j\omega C_R})}, \tag{3.13}$$

$$C_R = {}^{imag(Y_R)}\!/_{\omega}, \text{ and} \tag{3.14}$$

$$R_R = {}^{1}\!/_{(Y_R - j\omega C_R)}. \tag{3.15}$$

The initial values were then refined using MATLAB's *nlinfit* function and by focussing the frequency on where the parameter is dominant. The values were refined in the following order:

1. Capacitance, C_R: By assuming a very large parallel resistance value and using the initial capacitance value as a starting point, the capacitance was refined between 250 MHz and 1000 MHz. For frequencies lower than 250 MHz, uncertainty and error in the calibration standards caused capacitance variations.
2. Series resistance, R_{RS}: Since the series resistance is the dominant parameter of the real component, it is calculated before the parallel resistance. Using the refined capacitance and initial parallel resistance, the series resistance was refined between 5000 MHz and 6000 MHz in the (assumed) absence of reactance.
3. Parallel resistance, R_R: Using the refined series resistance and capacitance values, the parallel resistance also refined between 5000 MHz and 6000 MHz.

3.7.4 Series parameters extraction

Using the branch impedances, Z_1 and Z_2, the series resistance and inductance was calculated using the following equations.

$$Z_x = R_{bond} + j\omega L_{bond}, \tag{3.16}$$

$$R_{bond} = real(Z_x), \text{ and} \tag{3.17}$$

$$L_{bond} = imag(Z_x)/\omega, \tag{3.18}$$

where

Z_x is the complex series branch impedance (Ω), and

ω is the angular frequency.

3.7.5 Experimental verification

To verify the de-embedding and parameter extraction process, a simulated test fixture with known parameter values and TRM calibration circuit was simulated. The top level of the simulated test jig is shown in Figure 3.20.

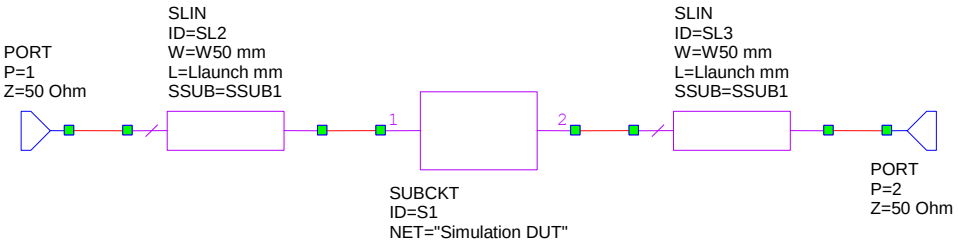


Figure 3.20. Simulated test jig top level.

The simulated calibration standards include the 3-meter, heat resistant Sucoform_86_FEP cable and connector-to-board transition. The simulated zero-length thru calibration standard is shown in Figure 3.21.

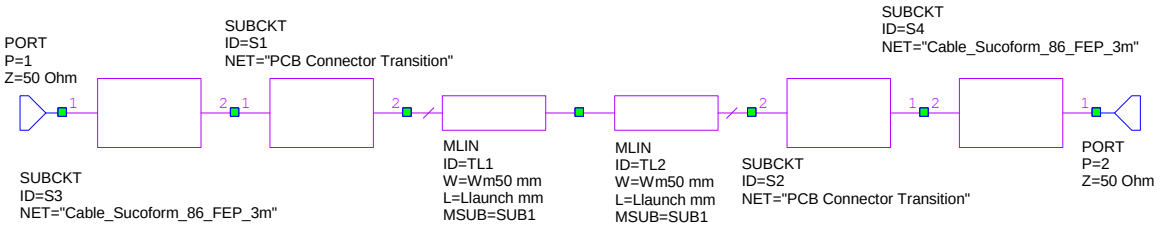


Figure 3.21. Simulated thru calibration standard.

The reflect calibration standard that was used during the verification process is shown in Figure 3.22.

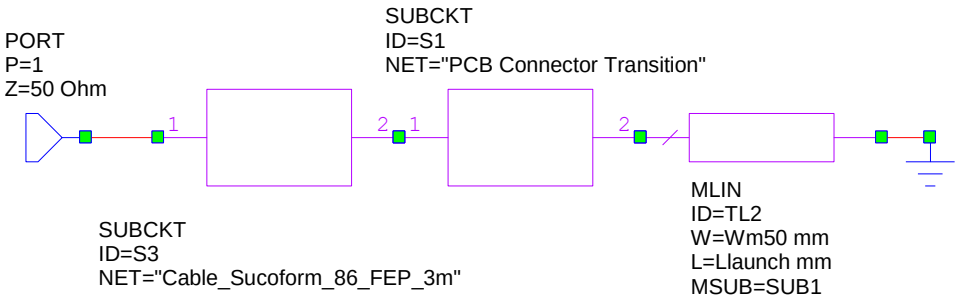


Figure 3.22. Simulated reflect calibration standard.

The 50Ω match calibration standard is shown in Figure 3.23.

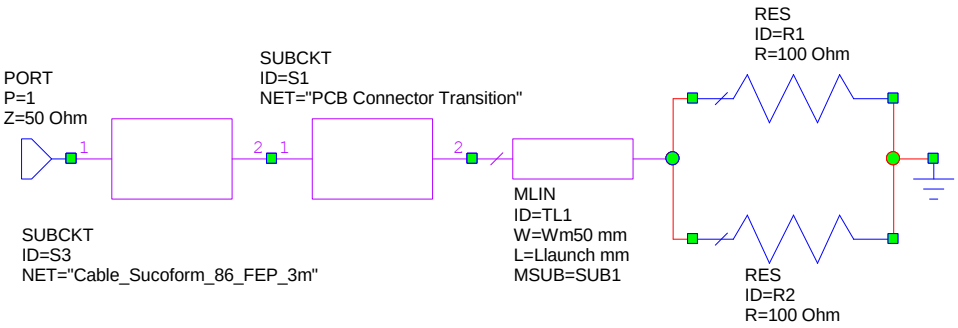


Figure 3.23. Simulated match calibration standard.

The simulated data was fed into the parameter extraction algorithm. The following sections briefly discusses the algorithm's results.

3.7.5.1 Forward biased

The simulated forward biased circuit is shown in Figure 3.24. For the shunt branch, a reasonable 2.3192 Ω forward series resistance was chosen and a paddle inductance of 0.0316 nH that was taken from the manufacturer datasheet.

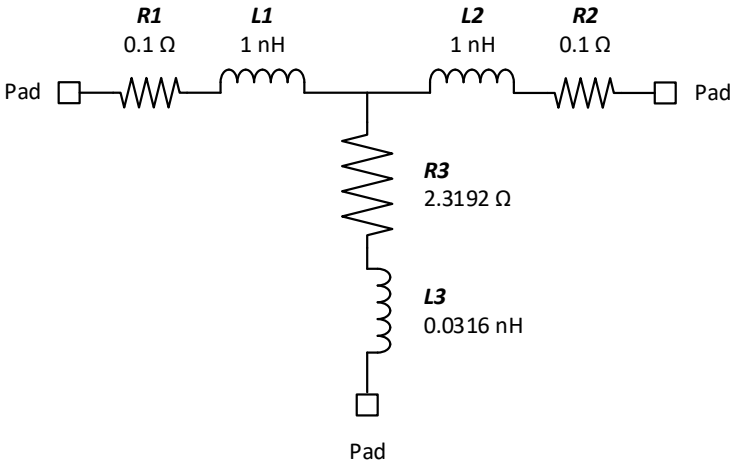


Figure 3.24. Simulated forward biased PIN diode.

The output from the parameter extraction algorithm is shown in Figure 3.25.

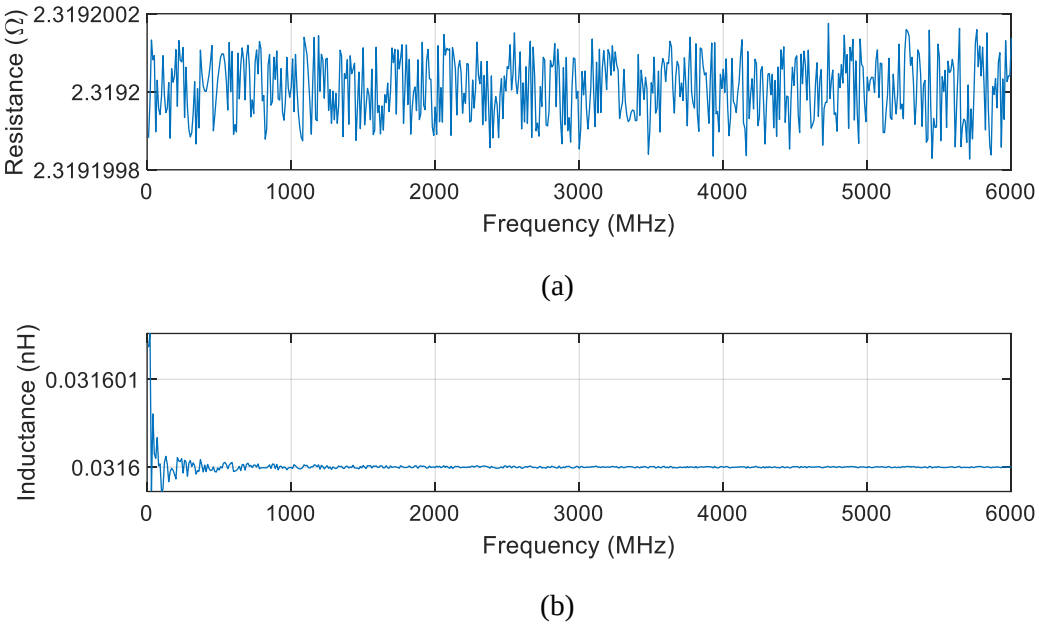


Figure 3.25. Simulated forward biased PIN diode results.
(a) Forward resistance. (b) Paddle inductance.

The algorithm correctly extracts the series resistance as 2.3192 Ω across the whole frequency range with miniscule variation. The paddle inductance was also correctly extracted as 0.0316 nH across the frequency range with very small uncertainty at lower frequencies.

3.7.5.2 Reverse biased

The simulated reverse biased circuit is shown in Figure 3.26. For the shunt branch, an 8.1943 Ω series resistance, a 1.672 pF parallel capacitance and a 214 kΩ parallel resistor was chosen based on typical datasheet values. The paddle inductance of 0.0316 nH was taken from the manufacturer datasheet.

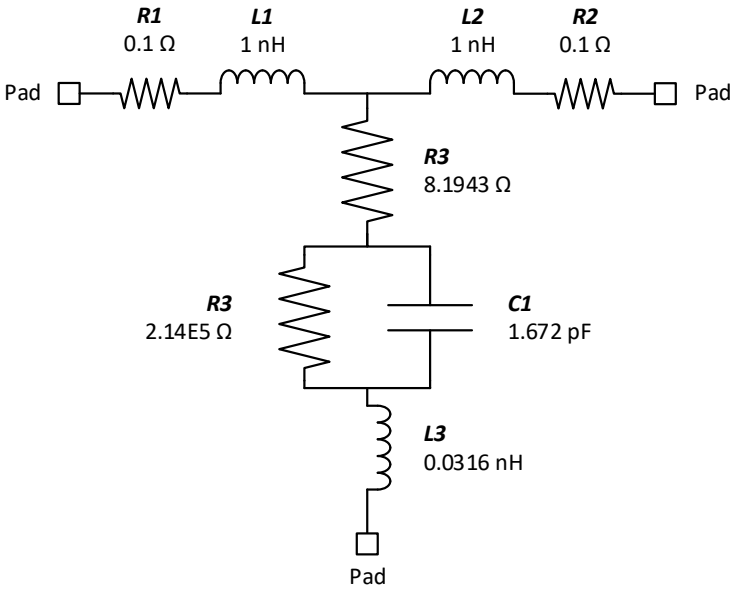
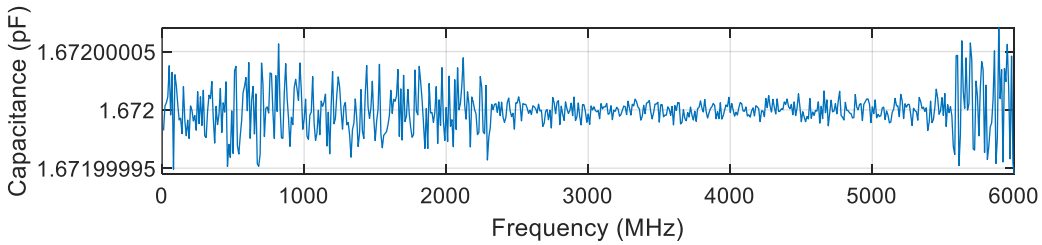
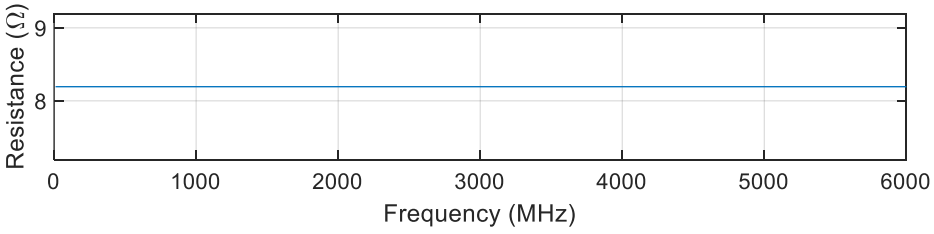


Figure 3.26. Simulated reverse biased PIN diode.

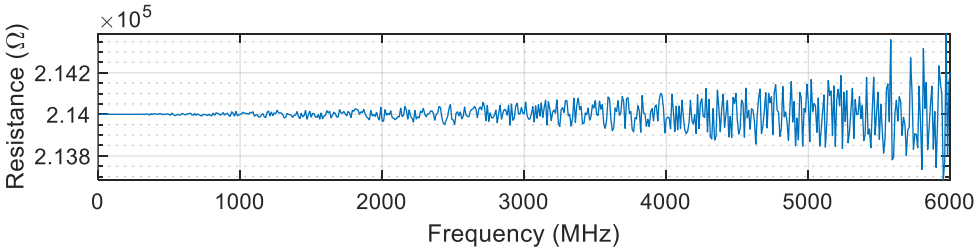
The output from the parameter extraction algorithm is shown in Figure 3.27. The algorithm correctly extracts the capacitance with nearly no variation across the whole frequency range. The series and parallel resistance of 8.1943 Ω and 214 kΩ are also correctly extracted, with the parallel resistance having some variation at higher frequencies.



(a)



(b)

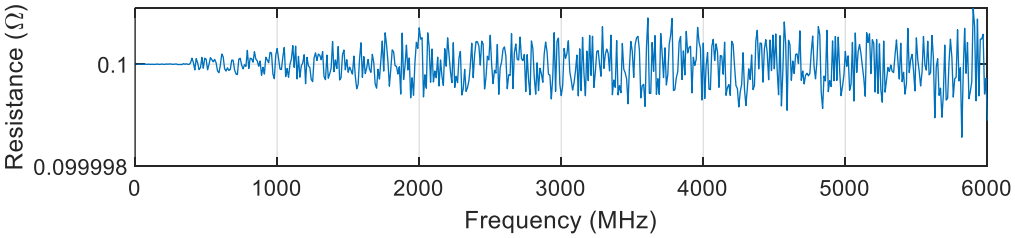


(c)

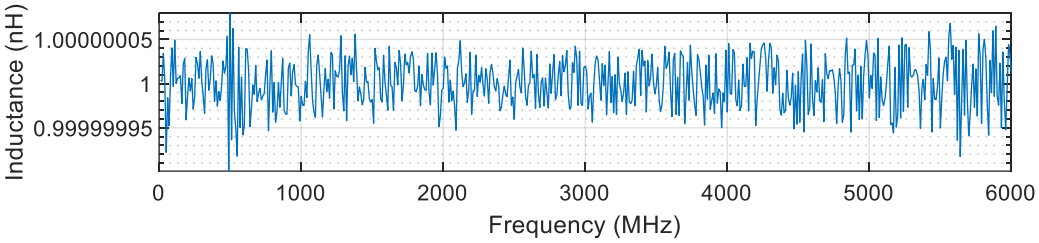
Figure 3.27. Simulated reverse biased PIN diode results.
(a) Capacitance. (b) Series resistance. (c) Parallel resistance.

3.7.5.3 Series branch

The simulated series branches of the PIN diode were shown in Figure 3.24 and Figure 3.26. For the series branches, a 0.1 Ω series resistance and a 1 nH bond wire inductor was chosen. The output from the parameter extraction algorithm for the series branches is shown in Figure 3.28. The algorithm correctly extracts the series resistance and inductance as 0.1 Ω and 1 nH, respectively.



(a)



(b)

Figure 3.28. Simulated series branch results.
(a) Resistance. (b) Bond wire inductance.

3.8 CONCLUSION

The research methodology that was used throughout this study has been presented in this chapter. The outline of the study was provided which showed how different aspects such as simulations, parameter extraction, and measurements are linked. The numerous simulation software tools and how they were used throughout this study was also given.

A section dedicated to circuit simulation and design discussed the different types of simulations that were done, including the which simulation solver was used for each type. It was further discussed why limiters based on discrete components were preferred above MMIC limiter modules. Circuit schematics for the different limiter topologies that were selected were given and the reason for their inclusion was provided. The PIN and Schottky diodes that were chosen for this study were also discussed, including the criteria that was considered for each.

A detailed section on the setup, equipment used, and procedure for each measurement was provided. The section included a discussion on how the temperature was controlled during measurements, how the equipment was calibrated for use, and an explanation on the process of de-embedding. The relevant data points and the equipment required for each measurement was given. The automation of repetitive measurements was also presented.

It was discussed how the de-embedded data is converted from S-parameters to an equivalent T-branch circuit. A thorough explanation of how the values of important equivalent-circuit parameters were calculated by using multi-bias parameter extraction techniques was then given. The parameter value refinement process was also explained.

By providing results from the simulated verification of the parameter extraction process, confidence is established that the results from the measured data are accurate.

CHAPTER 4 PIN DIODE MODEL PARAMETER EXTRACTION

4.1 CHAPTER OVERVIEW

This chapter focuses only on PIN diodes and discusses the extracted small-signal parameters for the reverse and forward-biased circuit models shown in Figure 3.18. The extracted parameter values were implemented into Robert Caverly's PIN diode model, PINDRC, in Cadence's AWR Microwave Office software. Using the model, the simulations were executed and compared to the data from the small-signal diode measurements. The different simulations were discussed in Section 3.4.1.

Section 4.2 presents the parameter values that were extracted under reverse-biased conditions, the populated PIN diode model, and its broadband validation against the measured data. The section further presents the effect of frequency, temperature, and bias on the value of the extracted parameters. Section 4.3 presents the extracted parameter values under forward biased conditions, its broadband validation against measured data and the effect of frequency, temperature, and bias on the value of the extracted parameters. Section 4.4 discusses the extracted parasitic paddle and branch inductances. Section 4.5 provides a conclusion to the chapter and summarises the data that was measured and simulated.

4.2 REVERSE BIASED

4.2.1 Extracted parameters

Figure 4.1 shows the equivalent circuit for a reverse biased PIN diode, including its package parameters.

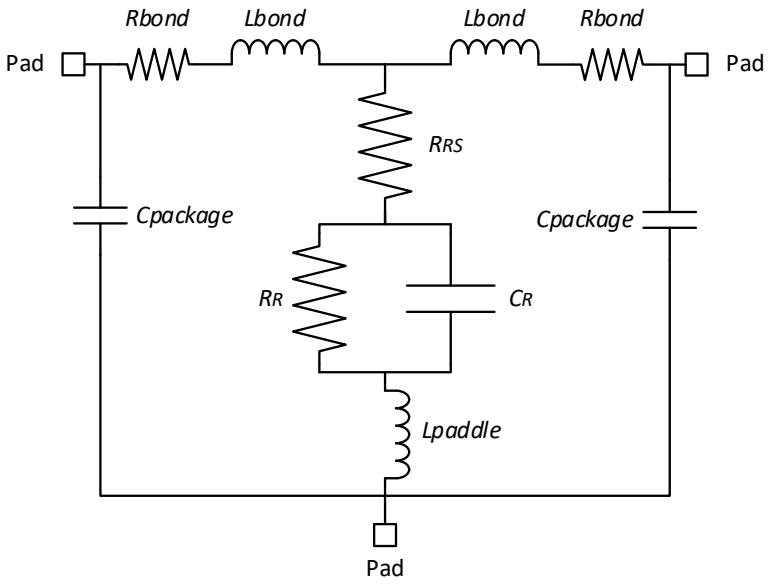


Figure 4.1. Reverse biased PIN diode equivalent circuits including package parameters.

The extracted parameters for the various measured PIN diodes are given in Table 4.1. The parameter values were extracted at the most negative voltage of -20 V, unless otherwise specified, and at a temperature of 25 ºC to enable comparison to the values provided by the manufacturer. The values that are listed are the best-fit, frequency-optimised, values for each parameter. The data given by the manufacturer was also measured at 25 ºC, with the capacitance value at 1 MHz listed. A blank entry in the manufacturer value column indicates that the parameter value was not available. Unless otherwise stated, the parameter values reported throughout this section are best-fit values.

Table 4.1. Extracted reverse-biased parameters at 25 ºC with a -20 V bias.

PIN diode	Parameter	Extracted value	Manufacturer value
CLA4608	C_R	0.6602 pF	0.6 pF @ -38 V
	R_R	12.83 kΩ	-
	R_{RS}	6.9716 Ω	-
	L_{paddle}	0.0299 nH*	-
	L_{bond}	0.6664 nH	0.3 nH**
CLA4609	C_R	0.5964 pF	0.6 pF @ -30 V
	R_R	8.68 kΩ	-
	R_{RS}	8.1326 Ω	-
	L_{paddle}	0.0277 nH*	-
	L_{bond}	0.6397 nH	0.3 nH
CLA4610	C_R	0.4014 pF @ -6V	0.28 pF @ -6 V
	R_R	16.63 kΩ	-
	R_{RS}	8.9953 Ω	-
	L_{paddle}	0.0466 nH*	-
	L_{bond}	1.1061 nH	0.3 nH
CLA4611	C_R	0.4093 pF	0.25 pF @ -38 V
	R_R	6.9787 kΩ	-
	R_{RS}	9.4493 Ω	-
	L_{paddle}	0.0470 nH*	-
	L_{bond}	1.0865 nH	0.3 nH**

* Calculated through multi-bias parameter extraction

** Assumed value

Table 4.1 shows that the extracted capacitance, C_R, closely resembles the data published by the diode manufacturer. For the CLA4608 and CLA4609 diodes, the capacitance is nearly

identical and is within 10 % of the expected value. For the CLA4610 and CLA4611 diodes, however, the capacitance value differs by 43 % and 56 %, respectively. This could be due to noise in the measurement data because of uncertainty in the two-tier calibration or parameter extraction process, which makes extracting such a small capacitance value difficult, even with a large negative bias. It is also likely that, with a larger negative bias, the extracted values could be closer to the manufacturer's data.

The extracted bond wire inductance, L_{bond}, differs by at least a factor of 2 compared to the manufacturer data. The bond wire inductance was not provided for all the PIN diodes. However, since the diode packages are all the same, it was assumed that bond wire inductance is the same for all the diodes. The bond wire inductance remained constant with bias voltage, only showing a slight deviation (± 0.01 nH) between the maximum and minimum bias voltage. Between the left and right branches, a maximum difference of 0.02 nH was observed. The large difference between the extracted and manufacturer value could be due to differences in the measurement setup. However, as it will later be shown, the extracted values better represent the measured data.

The reverse parallel and series resistance, R_R and R_{RS}, respectively, could not be compared to manufacturer data, but the extracted values correlate well with the measured data.

4.2.2 Populated PIN diode model

The extracted parameter values at 0 V and at a temperature of 25 ºC was used to populate the PINDRC diode model in AWR. The equivalent circuit of the PINDRC model in AWR is shown in Figure 4.2. It was found that, although the PINDRC model does have a minimum series resistance parameter, R_{LIM}, the parameter did not have any effect on the simulation results. This is because, internal to the PINDRC model, R_{LIM} is in parallel with the junction capacitance and not in series as expected. Therefore, a separate series resistor was added to the circuit to achieve the desired series resistance, with R_{LIM} set to 0 Ω. Furthermore, the PINDRC model has another parameter, "model internal diode series resistance", R_S, which is not shown in the equivalent circuit but did influence the behaviour of the forward-biased

simulations. It is not explained how this parameter differs from the "minimum series resistance" parameter. For reverse-biased simulations, the value of R_s was too small and, hence, the addition of a separate series resistor was still required. Because the model internal diode series resistance, R_s, influenced the model, it was preferred over the R_{LIM}. The PINDRC model also has a R_{EPI}, or "Epi leakage resistance", parameter. The function of R_{EPI} is not given. However, AWR states that R_{EPI} can be made low (~1 kΩ) without any effect on the simulation results, and that a low value of R_{EPI} facilitates convergence, especially in self-biased limiter circuits [58].

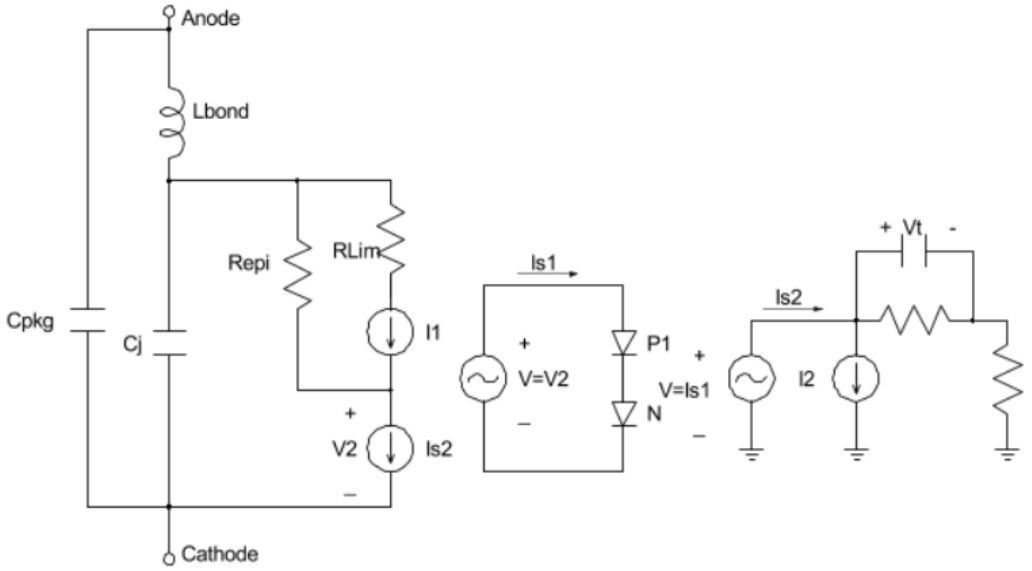


Figure 4.2. PINDRC diode equivalent circuit model in AWR [58].

The populated PINDRC diode model (including forward-biased parameter values) is shown in Figure 4.3. The addition of the series resistor, R_3 (R_{RS} shown in Figure 4.1) before the diode achieved the desired reverse-biased simulation results. The total series branch impedance (Z_1 and Z_2 shown in Figure 3.19) suggests that the entire branch is inductive, with the extracted bond resistance value either negative or near zero. Simulations showed that, for small values of R_{bond}, its effect is negligible. For this reason, the bond resistance (R_{bond} shown in Figure 4.1) is neither given in Table 4.1, nor shown in Figure 4.3 because its effect is negligible. The same argument holds for the package capacitance, $C_{package}$. It was previously discussed that the value of $C_{package}$ was assumed to be 0 because it is too

small to calculate from the available data and its effect on the simulations was found to be insignificant. It is, therefore, also omitted from Table 4.1 and Figure 4.3.

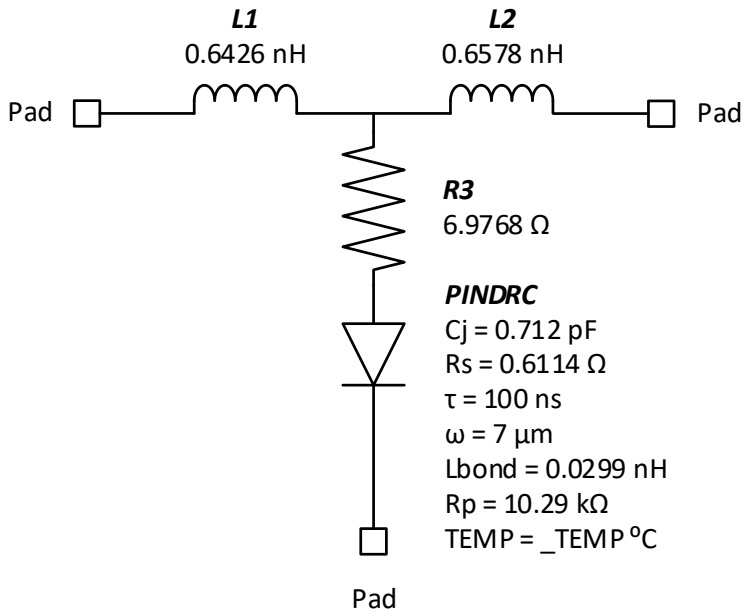
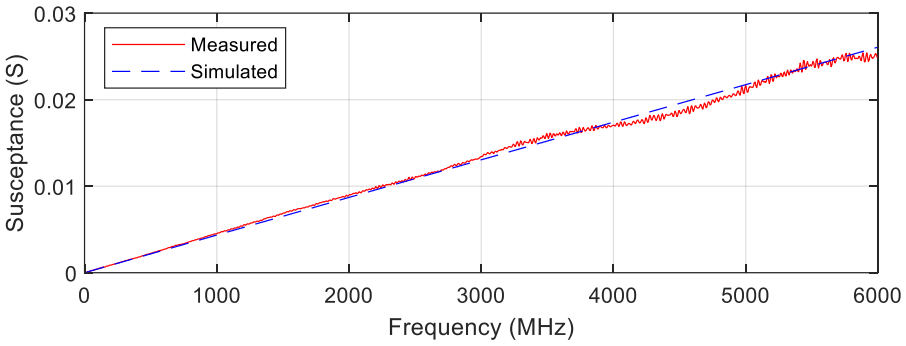


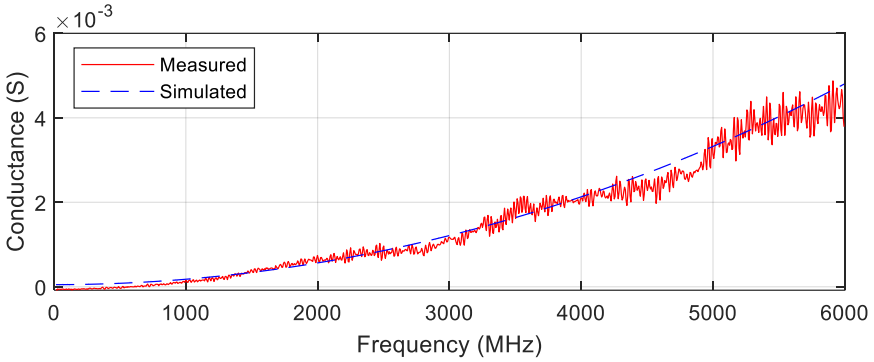
Figure 4.3. Populated PIN diode model with values at 25 ºC and 0 V.

4.2.3 Broadband model validation

The susceptance and conductance of the shunt admittance of the CLA4608 PIN diode is shown in Figure 4.4. The simulated data is compared against the de-embedded data of the PIN diode at 0 V and a temperature of 25 ºC. The simulated conductance in Figure 4.4 (b) closely follows the measured data, which indicates that the extracted reverse parallel and series resistance, R_R and R_{RS}, respectively, are accurate. Similarly, the simulated susceptance of the reactance in Figure 4.4 (a) matches the measured data, which follows a straight line with frequency. The positive straight line indicates that the susceptance is capacitive, which suggests that the extracted capacitance and paddle inductance, C_R and L_{paddle}, respectively, are correct.



(a)



(b)

Figure 4.4. De-embedded admittance comparison at 25 ºC and 0 V.
(a) Susceptance. (b) Conductance.

Overall, the results show that the parameters that were extracted from the DUT accurately predict its performance in simulation over a wide range of frequencies. A similar relationship between the simulated and measured data was observed for the other measured PIN diodes.

4.2.4 Capacitance

The following section discusses the variation in capacitance of the measured PIN diodes across different domains like frequency, temperature, and bias. Unless otherwise specified, the results shown are for the CLA4608 diode.

4.2.4.1 Capacitance versus frequency

Figure 4.5 shows the simulated and extracted capacitance versus frequency at 0 V and 25 ºC. The extracted capacitance remains within 10% of its nominal value at frequencies below 3000 MHz, whereafter a decline of approximately 0.05 pF is observed. The simulated capacitance shows a sharp increase at very low frequency before reaching the 0 V extracted capacitance value of 0.712 pF. As with the measured capacitance, a decline is observed at frequencies above 3000 MHz, although to a lesser extent.

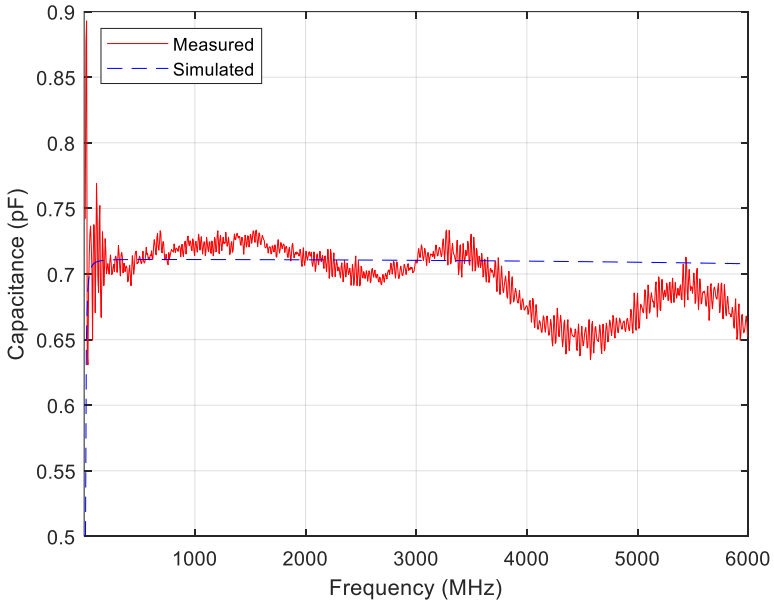


Figure 4.5. Capacitance versus frequency at 25 ºC and 0 V.

By analysing the capacitance's response over frequency, at low frequencies (f < 250 MHz) the parameter extraction process does not accurately determine the capacitance value due to uncertainty and error in the TRM calibration standards that is used for de-embedding. For this reason, the best-fit capacitance value, C_R, was extracted between 250 MHz and 3000 MHz. Extracting the capacitance at lower frequencies caused significant variation in the parameter value. The variation in the capacitance over frequency can also be caused by an incorrect paddle inductance value being subtracted from the total shunt susceptance. Like the capacitance, the paddle inductance is assumed to be constant over frequency, though in reality there may be small variation.

4.2.4.2 Capacitance versus temperature

The capacitance versus temperature is shown in Figure 4.6. The capacitance was simulated and extracted with a 0 V voltage. The simulated results do not report any change in capacitance with temperature. Neither the built-in AWR temperature variable, _TEMP, nor fixed temperature values yielded any change in the simulated PINDRC diode model. This was found to be a limitation for the PINDRC model in AWR. The measured results, however, show a gradual increase in capacitance with temperature of 1.296 fF / ºC.

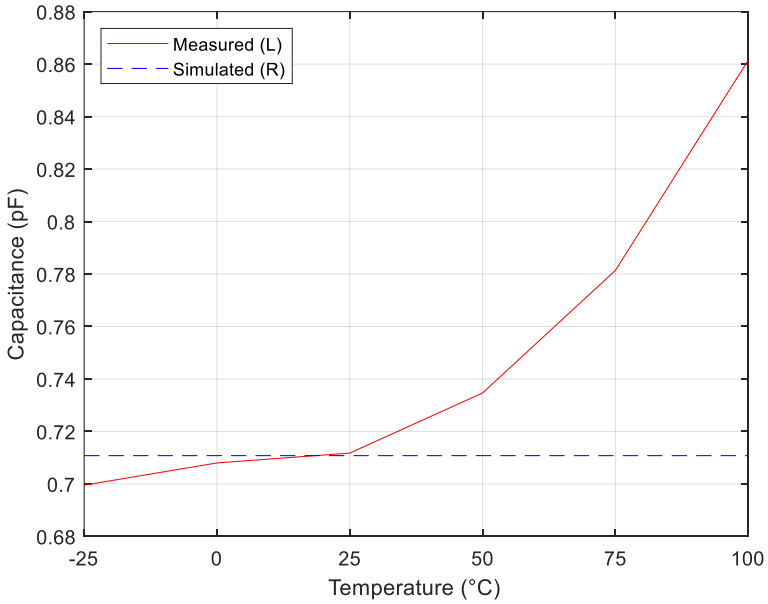


Figure 4.6. Capacitance versus temperature at 0 V.

Table 4.2 summarises the results of Figure 4.7. The summary indicates that, for all the measured PIN diodes, the capacitance increases, on average, at a rate of 0.7474 fF /ºC, though the increase is not linear over temperature.

Table 4.2. Summarised change in capacitance per diode at 0 V.

PIN diode	**Capacitance at -25** ºC (pF)	**Capacitance at 100** ºC (pF)	**Capacitance delta per 125** ºC (pF)
CLA4608	0.6995	0.8615	0.162
CLA4609	0.6229	0.662	0.0391

CLA4610	0.4448	0.5152	0.0704
CLA4611	0.3834	0.4856	0.1022

The increase in capacitance showed by the CLA4608 PIN diode was also evident on the other measured diodes. Figure 4.7 shows the change in capacitance for all the measured diodes at 0 V.

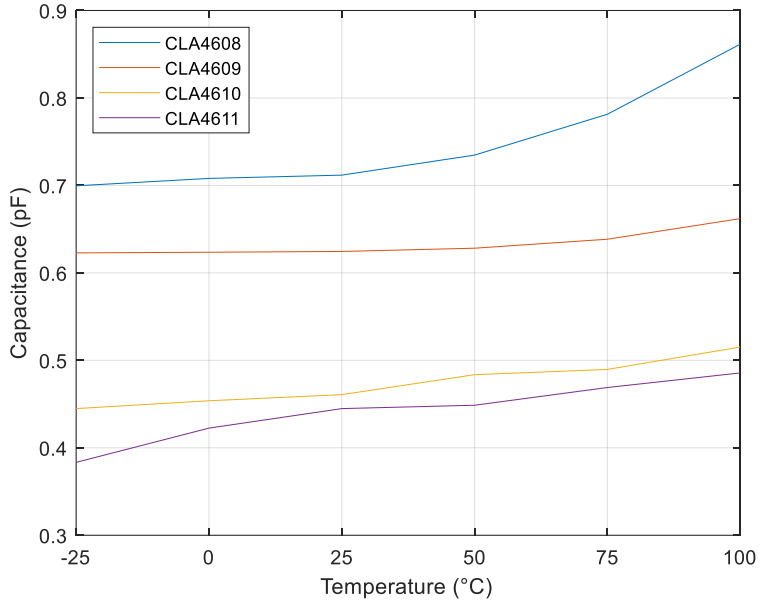


Figure 4.7. Capacitance versus temperature comparison at 0 V.

Table 4.2 also shows that the diode with the largest I-layer thickness, CLA4609, exhibits less capacitance change over temperature as the diodes with a thinner I-layer thickness, as is suggested by (2.11). This can be seen by the slope of the CLA4609 diode in Figure 4.7, which shows that most of the capacitance increase occurs between 75 ºC and 100 ºC.

A previous study showed that a PIN diode's reactance increases with temperature for carrier lifetime temperature coefficients also smaller than 2.3 [20]. However, the study neither specifies whether the reactance is capacitive or inductive, nor does it provide real capacitance values over temperature (only normalised values for the reactance were provided). Furthermore, the documented reactance was a PIN diode in the forward-biased state, and not reverse-biased. Another study that investigated the temperature and light induced effects on

the capacitance of Schottky photodiodes also found that the capacitance increases with temperature, with a higher dependence for low bias voltages [67]. Even though the study used Schottky diodes, a similar result is shown in Figure 4.8.

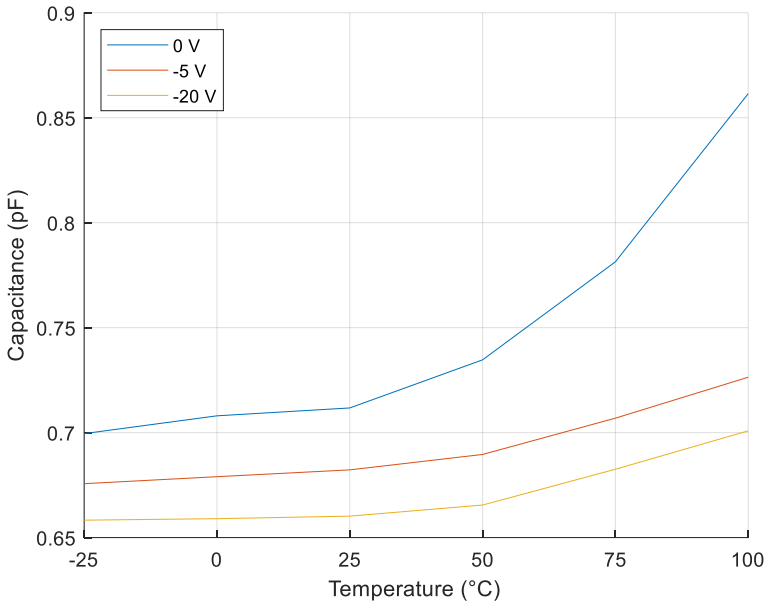


Figure 4.8. Capacitance versus temperature at different voltages.

The results show that for a smaller negative bias (0 V), temperature has more of an effect on the capacitance compared to a larger negative bias. However, for bias voltages smaller than -5 V, the rate of capacitance changer due to temperature remains the same.

4.2.4.3 Capacitance versus bias

Figure 4.9 shows the capacitance versus bias voltage graph at 25 ºC. The bias starts at 0 V and goes down to a minimum of -20 V. The results show that the simulated capacitance has no change in value with bias and remains constant at the best-fit value of 0.712 pF, whereas the measured results continue to decrease, as expected, to a minimum capacitance of 0.6602 pF. As it was discussed in Section 4.2.1, because the extracted capacitance shows a continuous decline in its value, it is likely that it would be closer to the manufacturer's reported value of 0.6 pF at -38 V.

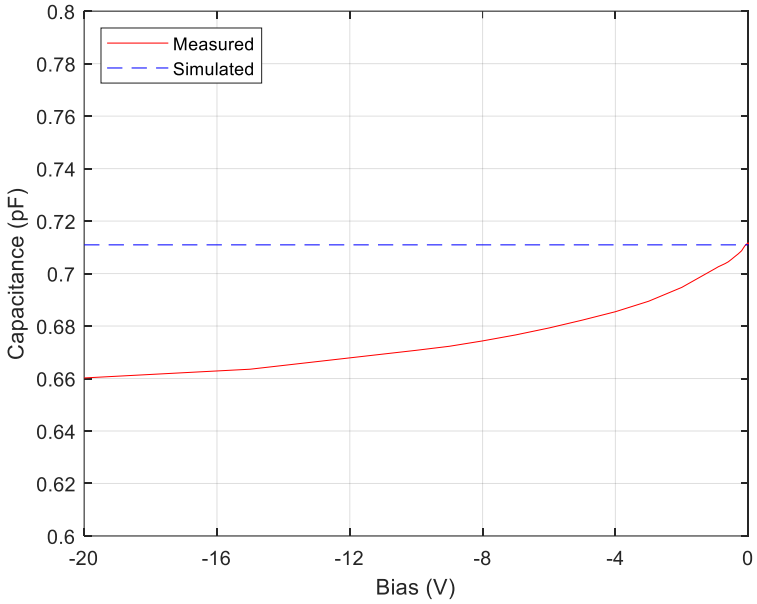


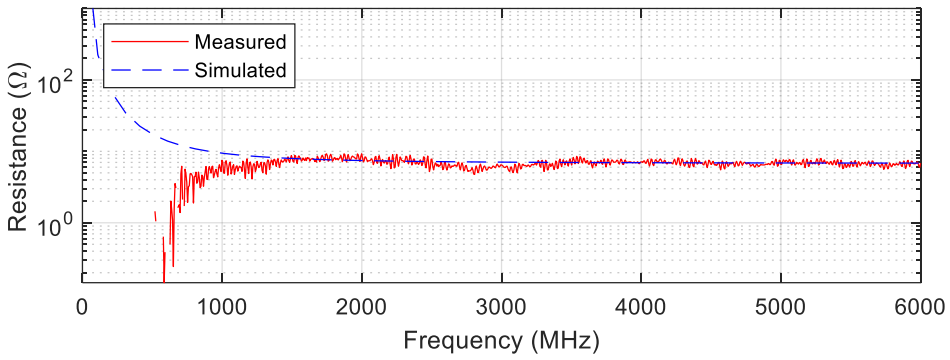
Figure 4.9. Capacitance versus bias voltage at 25 ºC.

4.2.5 Resistance

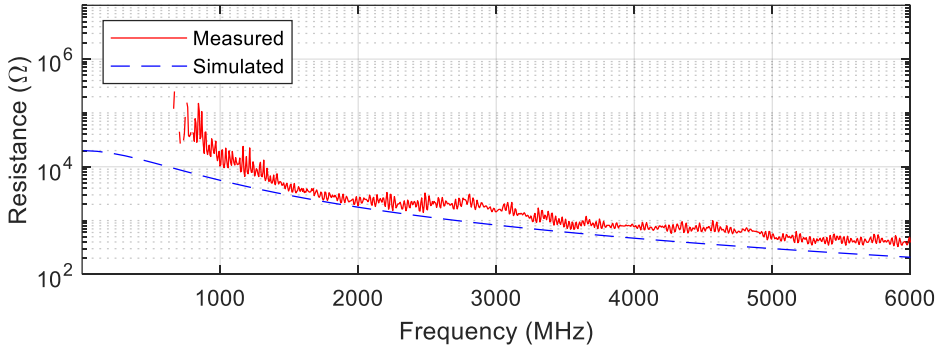
The following section discusses the reverse-biased series and parallel resistance results of the measured PIN diodes across like frequency, temperature, and bias. Unless otherwise specified, the results shown are for the CLA4608 diode.

4.2.5.1 Resistance versus frequency

Figure 4.10 shows the series resistance, R_{RS}, and parallel resistance, R_R, shown in Figure 4.1 at 0 V and 25 ºC versus frequency. As it was seen with the capacitance versus frequency results in Figure 4.5, the numerical parameter extraction process cannot determine either resistance accurately or reliably at frequencies below 1000 MHz, where the reactance is dominant. For this reason, the best-fit series resistance is calculated at frequencies between 5000 MHz and 6000 MHz where the reactance is considerably lower than the resistance and the total PIN diode impedance is dominated by the I-region resistance, as it was discussed in Section 3.7.5.2. The results show a good agreement between the measured and simulated series resistance for frequencies above 3500 MHz, with a best-fit series resistance of 6.9768 Ω at 0V.



(a)



(b)

Figure 4.10. Resistance versus frequency at 25 ºC and 0 V.
(a) Series resistance. (b) Parallel resistance.

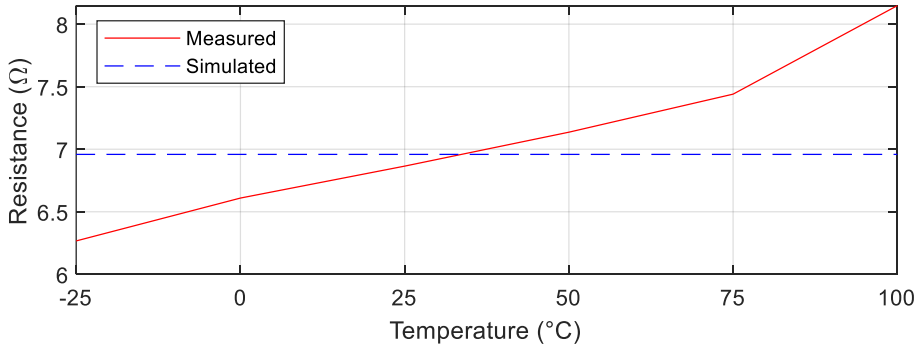
The equations for calculating the numerical parallel resistance and series resistance were presented in (3.11) and (3.15), respectively. The assumption was made that the series resistance remains constant over frequency. However, because the series resistance of the PIN diode is not truly constant and instead varies slightly over frequency, as can be seen from the data in Figure 4.10 (a), for some frequency points too much series resistance is deducted from the total impedance which results in a negative parallel resistance. Negative parallel resistance can be seen at low frequencies in Figure 4.10 (b), where the logarithmic y-axis does not display negative values, causing discontinuities in the results. This effect is pronounced at very low (-25 ºC) and very high (100 ºC) temperatures where the series resistance shows more variation. This was also observed between the different PIN diodes. Due to this, reliably calculating the parallel resistance proved to be difficult. The results

further show that for frequencies well above $1/\tau$ (10 MHz, τ = 100 ns for the CLA4608), the simulated and measured results indicate that both the series and parallel resistance decreases with frequency at a specific temperature. However, the series resistance exhibits much less change over frequency compared to the parallel resistance and remains more constant at higher frequencies.

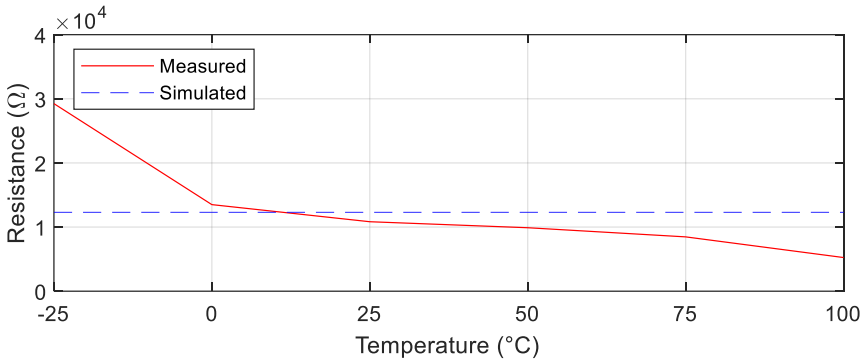
4.2.5.2 Resistance versus temperature

The best-fit series resistance, R_{RS}, that was extracted at 0 V versus temperature is shown in Figure 4.11 (a). The measured results show a gradual increase in series resistance from 6.27 Ω at -25 ºC to 8.11 Ω at 100 ºC, or a rate of 0.015 Ω / ºC, whereas the simulated results show no change in resistance over temperature as this dependency provoked no change from the PINDRC diode model. The increase in resistance with temperature was noted by the PIN diode manufacturer [53]. The increase was also observed in literature [20], though it should be noted that increase was for the forward-biased series resistance.

The best-fit parallel resistance, R_R, that was extracted at 0 V versus temperature is shown in Figure 4.11 (b). The measured results show a sharp decrease in resistance from 29.25 kΩ at -25 ºC to 5.25 kΩ at 100 ºC, or a rate of 0.192 kΩ / ºC, whereas the simulated results show no change in resistance over temperature.



(a)



(b)

Figure 4.11. Resistance versus temperature at 0 V.
(a) Series resistance. (b) Parallel resistance.

4.3 FORWARD BIASED

4.3.1 Extracted parameters

Figure 4.12 shows the equivalent circuit for a forward biased PIN diode, including its package parameters.

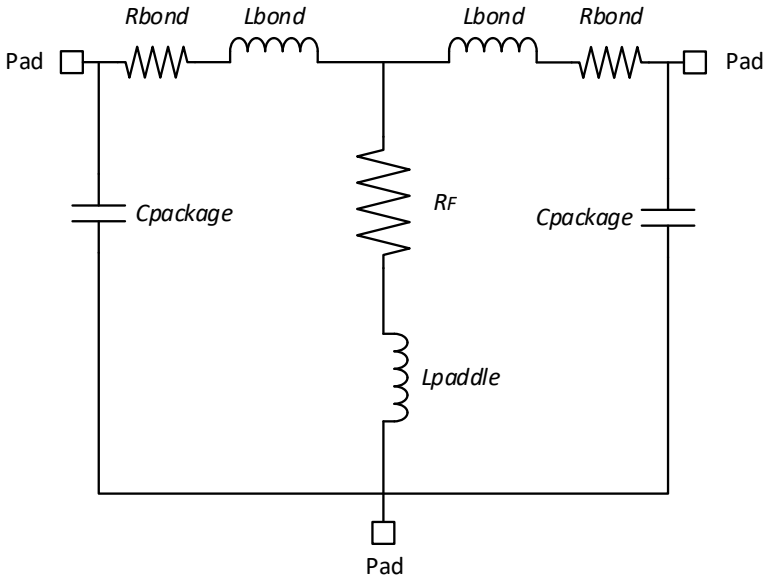


Figure 4.12. Forward biased PIN diode equivalent circuits including package parameters.

The extracted parameter values for a forward biased PIN diode are given in Table 4.3. The parameter values that are listed were extracted at 10 mA, unless otherwise specified, and at a temperature of 25 ºC. Where possible, Table 4.3 provides a comparison of the extracted parameter values to those provided by the manufacturer. The data given by the manufacturer was also measured at 25 ºC, with the resistance value at 10 mA listed. A blank entry in the manufacturer value column indicates that the parameter value was not available.

Table 4.3. Extracted forward-biased parameters at 25 ºC and 10 mA.

PIN diode	Parameter	Extracted value	Manufacturer value
CLA4608	R_F	0.6114 Ω @ 12 mA	1 Ω @ 10 mA
	L_{paddle}	0.0321 nH	-
CLA4609	R_F	0.7139 Ω	1.5 Ω*
	L_{paddle}	0.032 nH	-
CLA4610	R_F	1.9963 Ω	1.85 @ 10 mA
	L_{paddle}	0.0455 nH	-
CLA4611	R_F	0.7595 Ω @ 14 mA	0.75 @ 10 mA
	L_{paddle}	0.0508 nH*	-

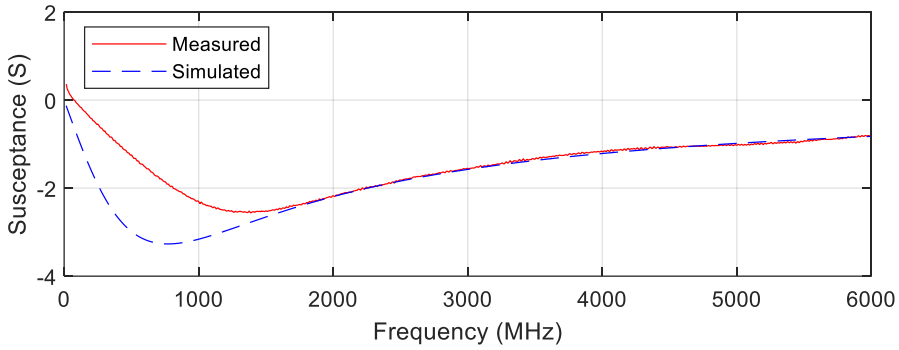
* Maximum value

The extracted forward resistance parameter data agrees well with the data provided by the diode manufacturer. The resistance for the CLA4610 and CLA4611 diodes are all within 5% accuracy of the listed value. It should be noted that the CLA4611's resistance was extracted at a current of 14 mA, compared to the manufacturer's 10 mA. The manufacturer does not provide a resistance value for the CLA4609 and instead only lists a maximum value of 1.5 Ω. Therefore, no comparison at 10 mA can be made. The resistance for the CLA4608 diode differs by 38.9 % (0.6114 Ω compared to 1 Ω), however, the measured resistance was extracted at 12 mA, and is expected to be lower.

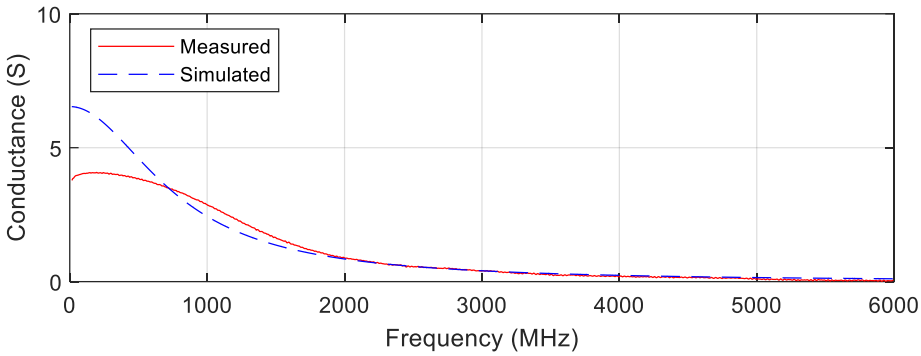
The paddle inductance was not provided by the manufacturer so no comparison could be made. However, given that the die is mounted directly on top of the cathode of the diode's package, it is expected that the paddle inductance be very small due to the absence of a bond wire. All the paddle inductances are between 0.03 nH and 0.05 nH, and the small differences could be due to amount of solder that was used when the PIN diode was installed onto the PCB. The extracted parameters given in Table 4.3 were also populated into the PINDRC diode model in AWR shown in Figure 4.3.

4.3.2 Broadband model validation

Figure 4.13 shows the simulated and de-embedded susceptance and conductance of the shunt admittance of the CLA4608 PIN diode at 25 ºC when forward biased with 1 V. A similar trend is seen with the conductance results, where the simulated data is around 3 siemens higher than the measured data before becoming identical at higher frequencies. Like the reverse-biased resistance, the results show that for frequencies well above $1/\tau$ (10 MHz), the forward-biased conductance and, therefore, resistance, also decreases with frequency. The reason for the measured and simulated results being identical at higher frequencies could be due to the best-fit resistance and paddle inductance parameter values that were extracted at frequencies between 5000 MHz and 6000 MHz. The results shown in Figure 4.13 suggests that the extracted forward-bias parameters are accurate.



(a)



(b)

Figure 4.13. De-embedded C-parameter comparison at 25 ºC and 1 V.
(a) Susceptance. (b) Conductance.

4.3.3 Resistance

The following section discusses the forward-biased resistance results of the measured PIN diodes across frequency, temperature, and bias voltage. Unless otherwise specified, all the results shown are for the CLA4608 diode.

4.3.3.1 Resistance versus frequency

The forward-biased resistance versus frequency is shown in Figure 4.14. The results are given at a temperature of 25 ºC and 12 mA, or 0.9 V for the CLA4608, which is the closest measurement to 10 mA. The results show a steady decline in the measured resistance over frequency, a result that was also found in [20] and [68]. The simulated results, however, shows a sharp increase in resistance with frequency with an initial resistance of 0.6114 Ω, which is the best-fit resistance value calculated from the measured data between 5000 MHz and 6000 MHz, most probably because of unconsidered reactance in the PINDRC diode model. It should be noted that for forward-biased measurements, R_3 shown in Figure 4.3 had to be omitted to enable the simulator to calculate the correct series resistance of the PIN diode.

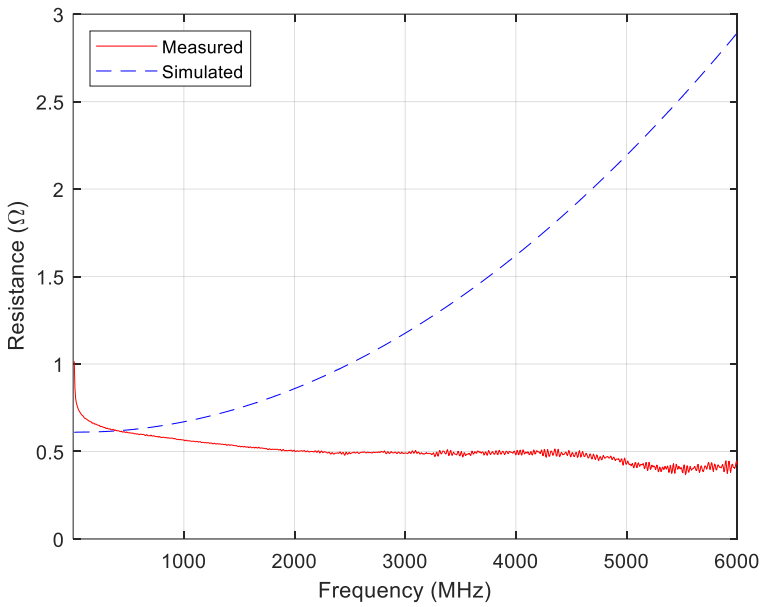


Figure 4.14. Forward resistance versus frequency at 25 ºC and 12 mA.

4.3.3.2 Resistance versus temperature

The PIN diodes resistance at 12 mA versus temperature is given in Figure 4.15.

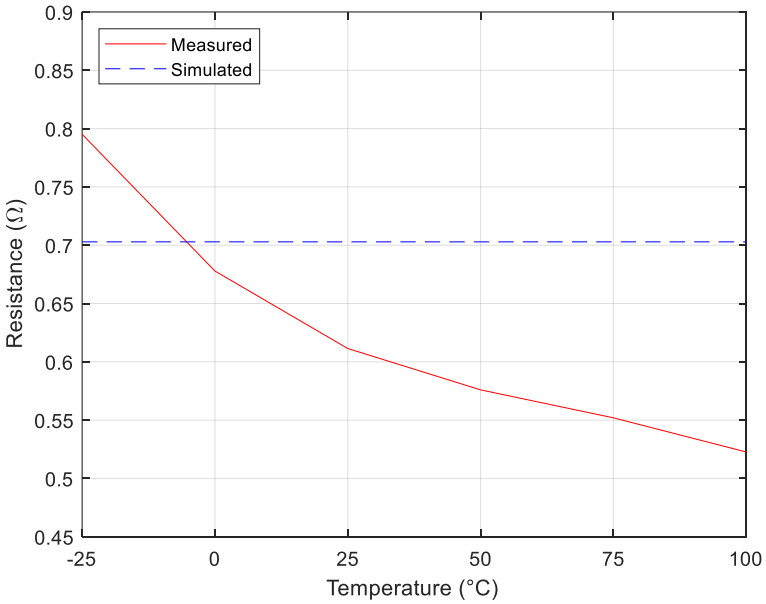


Figure 4.15. Forward resistance versus temperature at 12 mA.

The measured results show, however, that the forward resistance decreases with temperature at a rate of 2.492 mΩ / ºC. This result contrasts with the reverse-biased series resistance which showed an increase in resistance with temperature of 15 mΩ / ºC. The simulated results show no change in resistance as a function of temperature due to the limitations of the PIN diode model. The change in resistance with temperature was discussed in Section 2.5.5, where it was mentioned that, depending on the temperature dependence of the carrier lifetime temperature coefficient, $\tau_{coefficient}$, the resistance of the PIN diode may increase ($\tau_{coefficient} < 2.3$), decrease ($\tau_{coefficient} > 2.3$), or remain constant ($\tau_{coefficient} = 2.3$) over temperature. Unfortunately, the diode manufacturer does not provide the required information to calculate the carrier lifetime temperature coefficient. However, from the results shown in Figure 4.15, it can be concluded that the measured diode has a carrier lifetime temperature coefficient of greater than 2.3.

4.3.3.3 RF resistance versus bias

Figure 4.16 shows the forward resistance versus bias voltage at 25 ºC for voltages between 0 V and 3 V.

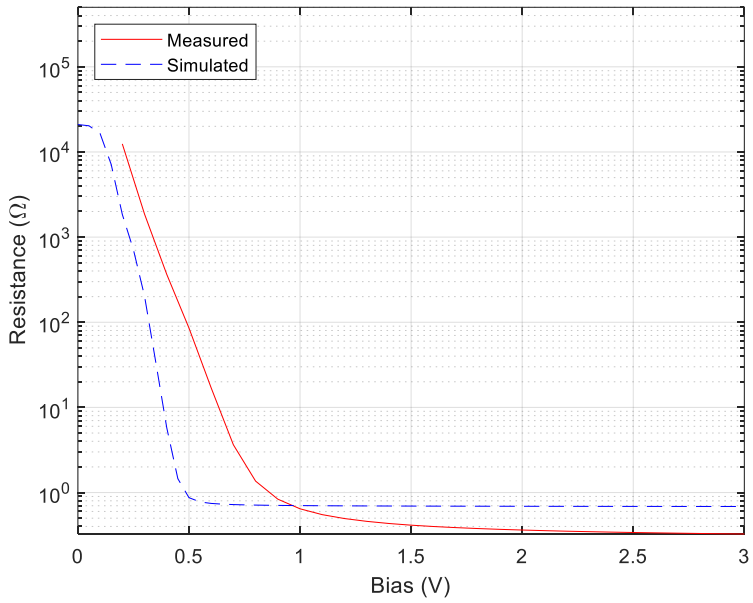


Figure 4.16. Forward resistance versus bias voltage at 25 ºC.

The simulated results show that the resistance reaches a minimum of around 0.68 Ω at 3 V with a knee voltage around 0.5 V as die diode transitions from the off to the on state. As per Table 4.1, the resistance peaks at 21 kΩ at 0 V bias. The measured results exhibit a more gradual decline in resistance as the bias increases compared to the simulated results, with a knee voltage of around 0.7 V and reaching a minimum of 0.2396 Ω at 3V. A maximum resistance of 12 kΩ is shown at 0.3 V. For voltages lower than 0.3 V, the parameter extraction process cannot determine a forward series resistance value as the circuit model is no longer valid. Similar gradual resistance slopes were observed for the other measured PIN diodes.

4.3.4 DC IV curve

In Figure 4.17, the CLA4608's DC IV curve is shown at 25 ºC. The figure shows the measured data compared to simulated data with and without the reverse-biased series resistance, R_{RS}, (R_3 shown in Figure 4.3). The addition of R_3 was discussed in Section 4.2.2. All the results indicate a turn-on or knee voltage of around 0.7 V, which is the typical turn-on voltage for silicon-based diodes.

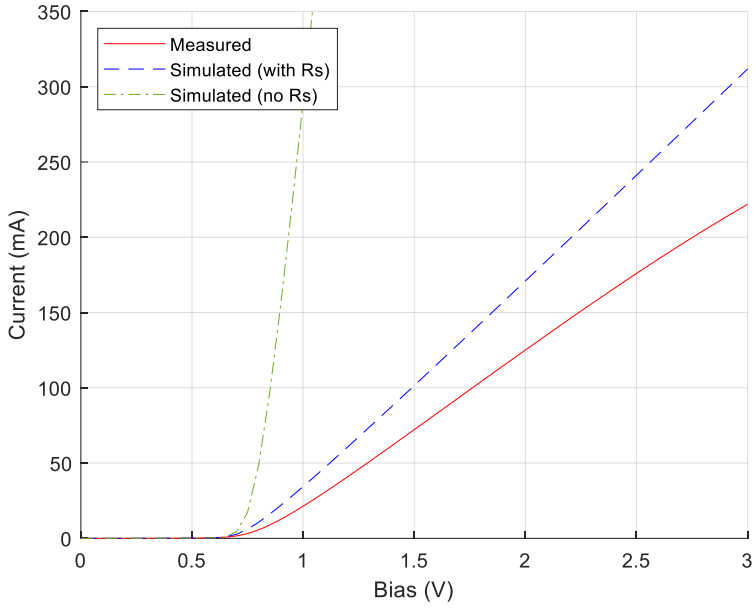


Figure 4.17. Forward current versus bias voltage at 25 ºC.

The simulated results which include the series resistor shows a better agreement to the measured data, confirming that the series resistance is present in the measured data. The difference between the simulated and measured results could be due to resistance internal to the VNA's bias-tee or unmodelled parasitic elements, for which the simulation does not account for. The measured IV versus temperature for the CLA4608 is shown in Figure 4.18. The results show that the knee voltage of the diode decreases with increasing temperature. This was also found in other experiments that investigated the temperature characteristics and dependence of different diodes [69], [70].

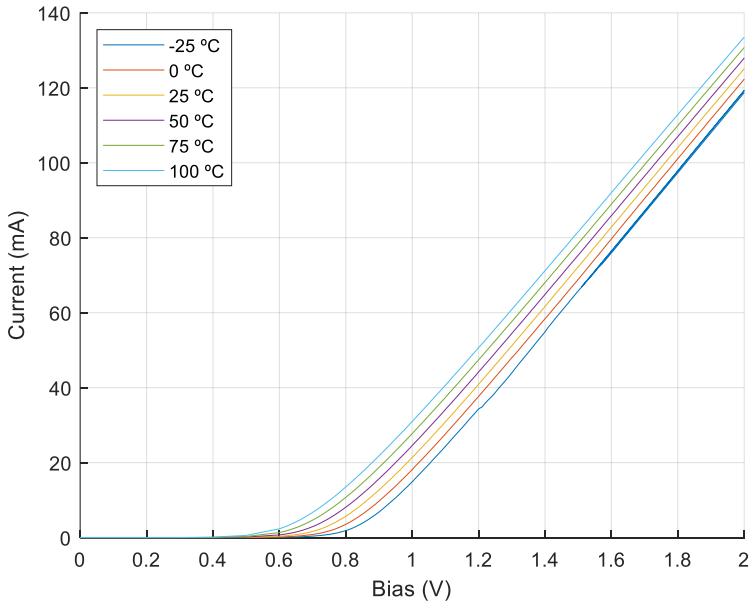


Figure 4.18. Forward current versus bias voltage versus temperature.

Table 4.4 shows a summary of the IV characteristics for each of the measured diodes. The voltage at 10 mA is given. It was found that the voltage decreases by an average of 1.34 mV / ºC across all four diodes.

Table 4.4. Summarised IV characteristics versus temperature per diode at 10 mA.

PIN diode	Voltage at -25 ºC (V)	Voltage at 100 ºC (V)	Voltage delta per 125 ºC (V)	Voltage per ºC (mV)
CLA4608	0.95	0.76	0.19	1.52
CLA4609	0.97	0.81	0.16	1.28

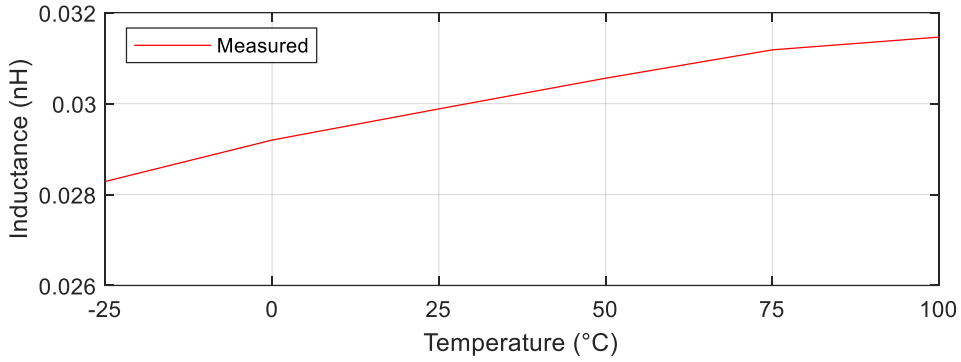
CLA4610	0.97	0.8	0.17	1.36
CLA4611	1.01	0.86	0.15	1.2

4.4 INDUCTIVE PARASITIC COMPONENTS

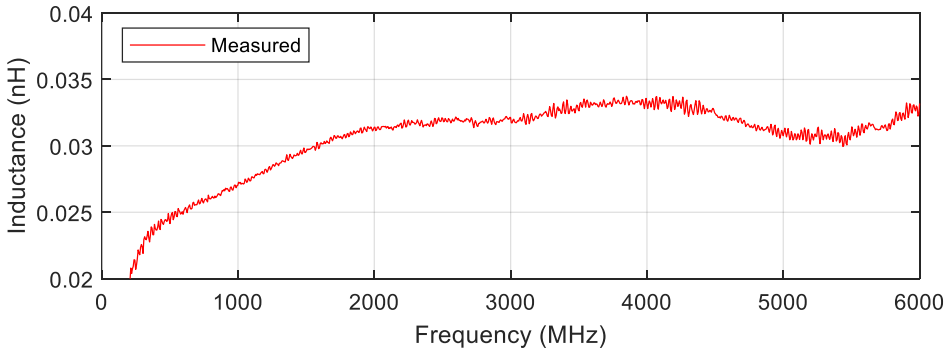
The following section briefly discusses the extracted paddle and branch inductances values for the CLA4608 PIN diode.

4.4.1 Paddle inductance

Figure 4.19 shows the paddle inductance, L_{paddle} shown in Figure 4.12, versus temperature and versus frequency at 3 V.



(a)



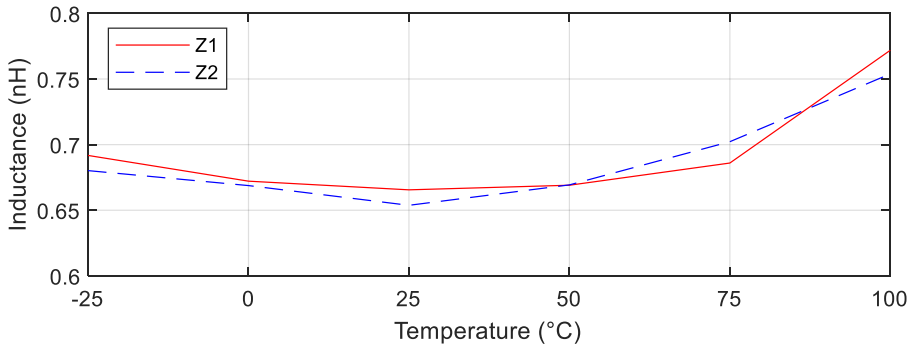
(b)

Figure 4.19. Paddle inductance at 3 V.
(a) Inductance versus temperature. (b) Inductance versus frequency.

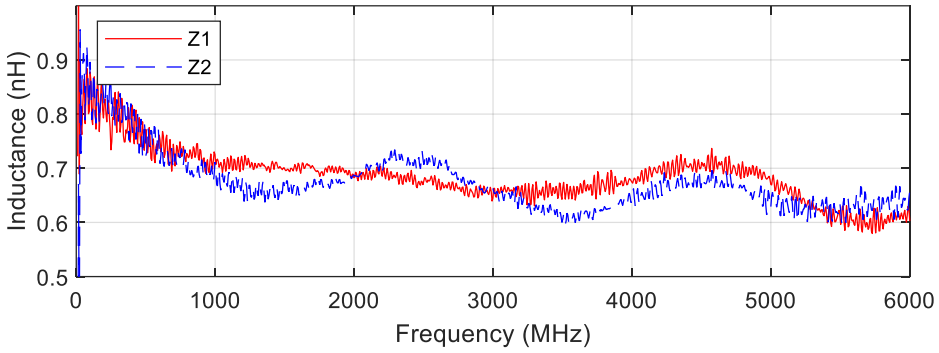
The temperature results show that the extracted shunt inductance increases from 0.027 nH at -25 ºC to 0.03 nH at 100 ºC – a negligible increase over such a large temperature range. Furthermore, the results show that the inductance has some variation in its value over frequency, especially at frequencies below 1000 MHz. Although the reactance at 3 V is predominantly inductive, at frequencies below 80 MHz, the reactance is negative. This would suggest that some capacitance is present at low frequencies, which could be indicative of un-modelled package capacitance. However, the calculated capacitance values are unrealistically high to be considered package capacitance. For this reason, the paddle inductance was only considered for frequencies higher than 2000 MHz. Similar paddle inductance results were observed for the other diodes, who all showed a small increase in inductance with temperature and minor variation in inductance over frequency.

4.4.2 Bond wire inductance

The branch inductance, Z_1 and Z_2 shown in Figure 3.19, is shown in Figure 4.20. The measured inductance versus temperature and the inductance versus frequency is given at 3 V. The frequency response of the inductance shows that both branches are nearly identical in value with some variation present across the frequency range. The inductance versus temperature result shows a decrease in extracted inductance for both branches between - 25 ºC and 25 ºC, before increasing between 25 ºC and 100 ºC, probably due to minor temperature elongation of the wire length.



(a)



(b)

Figure 4.20. Branch inductance at 3 V.
(a) Inductance versus temperature. (b) Inductance versus frequency.

4.5 CONCLUSION

The best-fit extracted parameter values given in Table 4.1 and Table 4.3 was used to populate the PINDRC diode model in AWR. The PINDRC model requires numerous parameter values that are not provided by the diode manufacturer to be configured properly. A simple simulation setup is not achievable. The lack of a series resistor for reverse-bias applications necessitated the use of a separate series resistor to achieve the desired frequency response. Otherwise, the model showed a good agreement with the de-embedded data during forward and reverse-biased simulations after the extracted parameters were loaded. It should be noted that for forward-biased measurements, the series resistance, R_{RS}, (R_3 shown in Figure 4.3), had to be set to 0 Ω (omitted) to enable the simulator to calculate the correct series resistance of the PIN diode. It was further found that the PINDRC model does not correctly apply changes in temperature to the parameter values. As a result, all the simulated temperature measurements did not show any change in the respective parameter value.

The reverse-biased results showed that the extracted capacitance remains stable at frequencies lower than 3000 MHz with some variation observed at higher frequencies which could be due to error in the calibration or unmodelled parasitic inductance. The simulated results showed a constant capacitance over frequency with a small decline at higher

frequencies, like the measured data. It was further shown that a PIN diode's capacitance increases with temperature between -25 ºC and 100 ºC. This agrees with the findings of a study that investigated the temperature and light induced effects on the capacitance of Schottky photodiodes [67]. Table 4.2 answers the primary research question of this study by presenting a summary of the change in capacitance that is shown in Figure 4.7 and shows that, for all the measured diodes, the capacitance increases with increasing temperature. It can, therefore, be concluded that the hypothesis that is presented in Section 1.2 is correct. The simulated data did not show any change in capacitance with increasing temperature. The measured data also supports (2.11), which suggests that temperature variations will have less of an impact on diodes with thick I-layers, and more of an impact on diodes with a thin I-layer.

The reverse-biased resistance results showed that both the series and parallel resistance decreases with frequency. The series resistance exhibited less decrease compared to the parallel resistance at higher frequencies (f > 2000 MHz). The measured results were in good agreement with the simulated results for frequencies higher than 1000 MHz. It was also found that the series resistance increases with temperature at a rate of 0.015 Ω / ºC between -25 ºC and 100 ºC. The simulated data did not show any change in series resistance with increasing temperature. It was demonstrated that using the best-fit series resistance to calculate the parallel resistance causes uncertainty in the parallel resistance value and, because of this, extracting a best-fit parallel resistance value proved difficult at low frequencies.

The forward-biased results showed that the extracted resistance decreases with increasing frequency, confirming previous published results [20]. The simulated resistance showed a sharp increase in resistance with frequency (probably due to unconsidered reactance), with an initial resistance value equal to the extracted best-fit value at 12 mA. The results further showed that the forward resistance of all the measured diodes decreases with temperature at a rate of 2.492 mΩ / ºC between - 25 ºC and 100 ºC. This contrasts with the reverse-biased series resistance, which was found to increase with temperature at a rate of 0.015 Ω / ºC in

the same temperature range. It can, therefore, be concluded that the measured diodes have a carrier lifetime temperature coefficient, $\tau_{\text{coefficient}}$, of greater than 2.3. The simulated data did not show any change in resistance with increasing temperature. Both the simulated and measured forward RF resistance versus bias presented a graph that is typical to PIN diodes. The simulated resistance reached a minimum resistance of around 0.68 Ω at 3 V, whereas the measured RF resistance displayed a continuous decline in resistance as the voltage increased, reaching a minimum of 0.2396 Ω at 3 V. It was found that the DC IV characteristics of the PIN diodes are also affected by the change in temperature. Table 4.4 summarised the change in voltage and shows that, at 10 mA, the voltage decreases by an average of 1.34 mV / ºC across all four diodes.

The branch inductance showed little variation in value over frequency and a minor increase in value with increasing temperature, probably due to temperature induced elongation of conductors in either the model or the measurement setup. The left and right branches showed near identical values, both over temperature and frequency. The paddle inductance results revealed that the inductance has some variation in its value over frequency, especially at frequencies below 1000 MHz, but increases almost linearly with temperature. This minor variation is, again, probably due to unconsidered parasitic reactance.

CHAPTER 5 PIN DIODE LIMITER RESULTS

5.1 CHAPTER OVERVIEW

The PIN diode simulation model that was setup in Chapter 4 using the extracted parameter values was implemented in the different limiter topologies that were discussed in Chapter 3. This chapter discusses the resulting PIN diode limiter performance characteristics that were obtained through simulation and measurements. This chapter focuses on the non-linear and transient response of the different limiter topologies to a high-power incident signal, investigating how the junction capacitance of a PIN diode that was established in the previous chapter influences the response. Where possible, comparisons to manufacturer and published data are also discussed.

Section 5.2 gives a brief discussion on the packaging and manufacturing of RF limiters and the reason for choosing limiter topologies based on discrete components. Section 5.3 describes the limiter topologies that were selected for tested and the reason for their inclusion. The simulated effect of varying the capacitance and series resistance of the diode model is discussed in Section 5.4. Section 5.5 highlights the limiter and custom coupler area on the designed PCB and gives a physical view of the limiter topologies that were described in Section 5.3. The custom coupler's results are presented in Section 5.6 and compared to the simulated results. Section 5.7 and Section 5.8 discusses the non-linear and transient, respectively, response results of the different limiter topologies at different temperatures and frequencies, and for different PIN diodes. Comparisons between the topologies are provided in terms of their performance at the various temperatures and frequencies. Section 5.9 concludes the section and provides a summary of the results.

5.2 PACKAGING AND MANUFACTURING

It is not uncommon for manufacturers to produce RF limiters based on MMIC technology. MMIC limiter modules are fully integrated limiter circuits packaged into a small plastic surface-mount package. These integrated modules can be any of a variety of the limiter topologies and often include supporting components such as DC blocking capacitors, biasing networks, and RF chokes. MMIC limiter modules are designed to simplify their application in a system but neither allows for the customisation of components nor for rapid and low-cost prototyping. Therefore, for this study, limiter topologies based on discrete components were chosen, as this would serve the same purpose in answering the research question as MMIC limiter modules. The selected PIN and other diodes can also easily be incorporated to allow for an easy comparison between topologies over temperature.

5.3 LIMITER TOPOLOGIES

The limiter topologies that were discussed in Section 2.5 highlighted some of the most common basic forms. The three topologies that were used for this study was discussed and shown in Section 3.4.2, but are repeated in this section for clarity. The topologies are the traditional PIN diode limiter, the anti-parallel limiter, and a modified version of a PIN-Schottky limiter. The traditional PIN diode limiter circuit was selected because of its minimalist design and frequent presentation by limiter diode manufacturers as an application circuit in PIN diode datasheets. The limiter schematic is shown again in Figure 5.1.

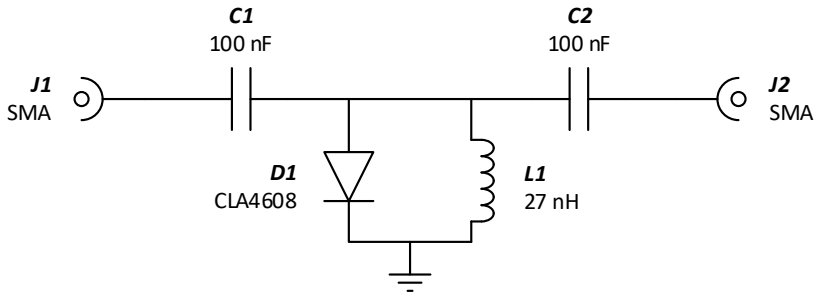


Figure 5.1. Traditional limiter circuit topology.

The anti-parallel limiter circuit was chosen because of its simple design which does not require a DC bias choke and improved performance compared to the traditional limiter topology [59]. The PIN diodes were placed as close to each other as possible. The limiter schematic is shown again in Figure 5.2.

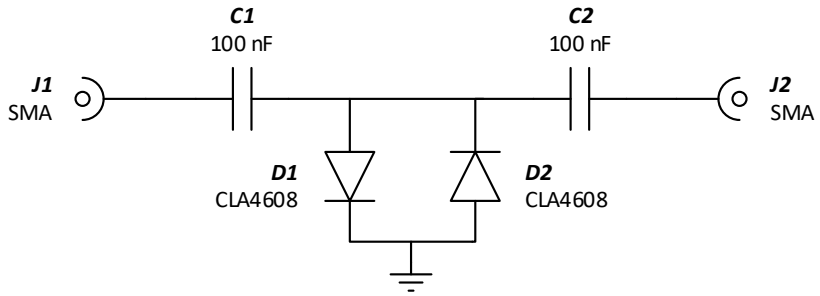


Figure 5.2. Anti-parallel limiter circuit topology.

A modified version of a typical PIN-Schottky limiter circuit shown in Figure 2.13 was chosen to utilise the reverse coupled signal's power to further bias the PIN diode. The limiter schematic is shown in Figure 5.3. The circuit includes two Schottky diodes that are connected to both the forward and reverse coupled ports of a bi-directional coupler, which is a novel contribution to the state-of-the-art. The drawback of using a bi-directional coupler is that it increases the complexity and physical size of the limiter. It further differs from the typical active PIN-Schottky limiter in that the coupler is placed at the input of the limiter, before the PIN diode, rather than after the PIN diode. The bi-directional coupler's purpose is to bias the PIN diode, through the Schottky diodes, using the high-power incident signal and the signal that is reflected to the source once the limiting commences.

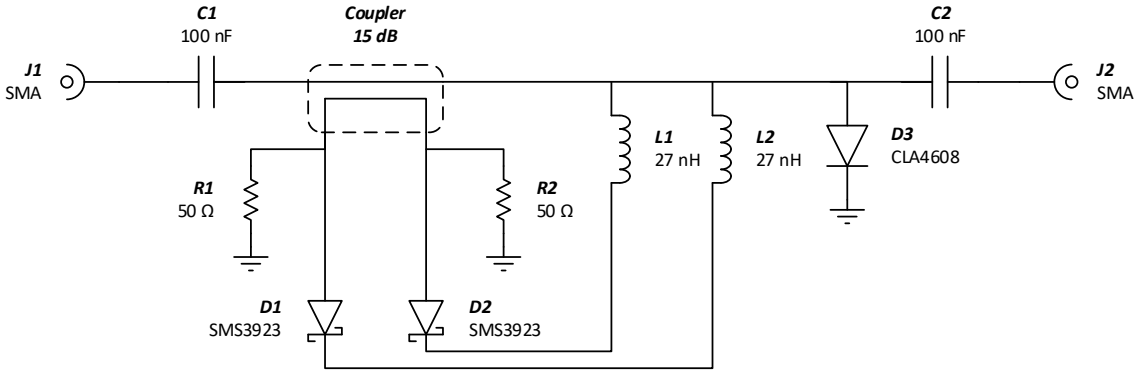


Figure 5.3. Detector limiter circuit topology.

5.4 SIMULATED EFFECT OF PARAMETER CHANGE

The following section discusses the simulated effect of varying the junction capacitance (C) and minimum series resistance (R_s) of the PINDRC model shown in Figure 4.3. The populated PINDRC diode models from the Section 4.2.1 were used to create the different limiter topologies in AWR. By varying these two parameters, their effect on the transient and non-linear response of the limiter can be determined.

The two parameters were varied independently of each other, thus ensuring that no other variable or parameter interferes with the simulation. The parameters were adjusted inside the PINDRC model, and their effect measured on the output of the limiter topology. It was shown in Figure 4.6 that a PIN diode's zero-bias junction capacitance increases with temperature, and its forward-biased series resistance decreases with temperature (shown in Figure 4.15). Therefore, the junction capacitance was varied with increasing values, and the series resistance was varied with decreasing values. Realistic values for both parameters were chosen based on Table 4.1 and Table 4.3 and varied in fixed increments. The junction capacitance was increased from 0.25 pF to 1.25 pF in 0.5 pF increments, and the series resistance was decreased from 1.25 Ω to 0.25 Ω in 0.5 Ω increments.

The temperature and frequency were kept constant in simulation at 25 ºC and 100 MHz, respectively. For the transient simulation, the square-wave modulated sinusoidal input signal had a rise time of 47 ns and a fall time of 32 ns, which resembles the measured signal, and a 50 dBm input signal was used and fed through a 6 dB attenuator. For the non-linear simulation, the power was increased linearly in 1 dB increments from 0 dBm to the maximum allowable as listed by the diode manufacturer. All cable losses were accounted for.

5.4.1 Transient results

Simulated transient responses are exported from AWR as continuous voltage versus time (in nanoseconds), which are converted to power (in milliwatts) in MATLAB on the assumption of

a 50 Ω load impedance. From the converted power response, the envelope is calculated. Using the envelope, the spike leakage is calculated by first determining the flat leakage level to use as reference. Any values preceding and higher than the reference is considered a contribution to spike leakage. Spike leakage is illustrated in Figure 5.4.

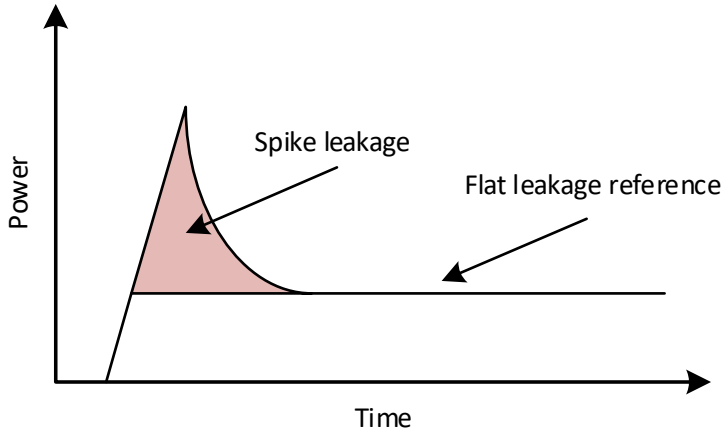


Figure 5.4. Spike leakage energy illustration.

The spike leakage is given as a unit of energy in nanojoules (nJ), which is equal to the power in watts (W) times the time duration in seconds referenced to the flat leakage value. The spike leakage was calculated using trapezoidal numerical integration to compute the approximate integral (area under the curve) of the spike leakage envelope. Since spike leakage is the amount of energy transferred, the duration of the spike is arguably more important than the magnitude of the spike itself.

Figure 5.5 shows the effect of the change in junction capacitance and minimum series resistance on the transient response of the traditional limiter topology at 100 MHz. The continuous power response is shown in blue; the envelope shown in red, and spike leakage shown in green.

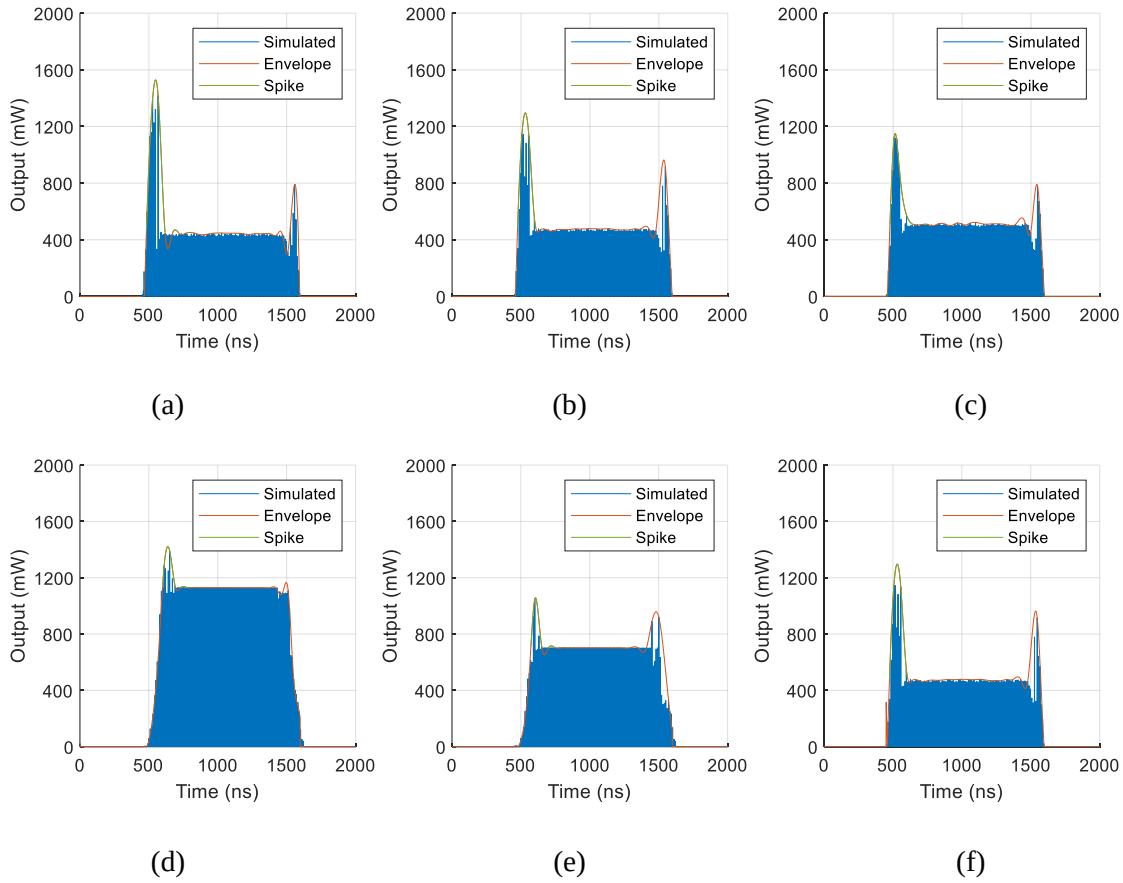


Figure 5.5. Effect of capacitance and resistance change on the transient response at 100 MHz. (a) C_j = 0.25 pF, R_s = 0.25 Ω. (b) C_j = 0.75 pF, R_s = 0.25 Ω. (c) C_j = 1.25 pF, R = 0.25 Ω. (d) R_s = 1.25 Ω, C_j = 0.75 pF. (e) R_s = 0.75 Ω, C_j = 0.75 pF. (f) R_s = 0.25 Ω, C_j = 0.75 pF.

Table 5.1 summarises the results from Figure 5.5(a) through Figure 5.5(c) and shows that an increase in capacitance will decrease the spike leakage of the limiter. This contradicts published literature which report that diodes with a thin I-layer (small junction capacitance) have little spike leakage, and that thick I-layer diodes (more junction capacitance) have much more spike leakage [23]. The flat leakage remains nearly constant as can be expected, since the capacitance of the diode has little effect on its power handling capability. An increase in recovery time is also expected with more capacitance.

Table 5.1. Summary of the effect of capacitance change at 100 MHz.

Capacitance (pF) R_s = 0.25 Ω	**Spike leakage (nJ)**	**Flat leakage (dBm)**	**Recovery time (ns)**
0.25	91.1	26.51	118
0.75	64.99	26.8	121
1.25	43.24	27.07	148

Figure 5.5(d) through Figure 5.5(f) shows that for a fixed capacitance of 0.75 pF, the spike leakage of the limiter increases, and the flat leakage decreases for decreasing resistance. For a series resistance smaller than 0.75 Ω, the spike leakage increases substantially. A decrease in flat leakage is expected since less resistance indicates that the diode is, essentially, more forward biased (as it was seen in Figure 4.16), providing more attenuation. The recovery time also increases as the resistance decreases. The reason for these changes is likely due to the lack of resistance to dampen the transient response, which increases the spike leakage and recovery time but also reduces the flat leakage (increased attenuation). The results are summarised in Table 5.2.

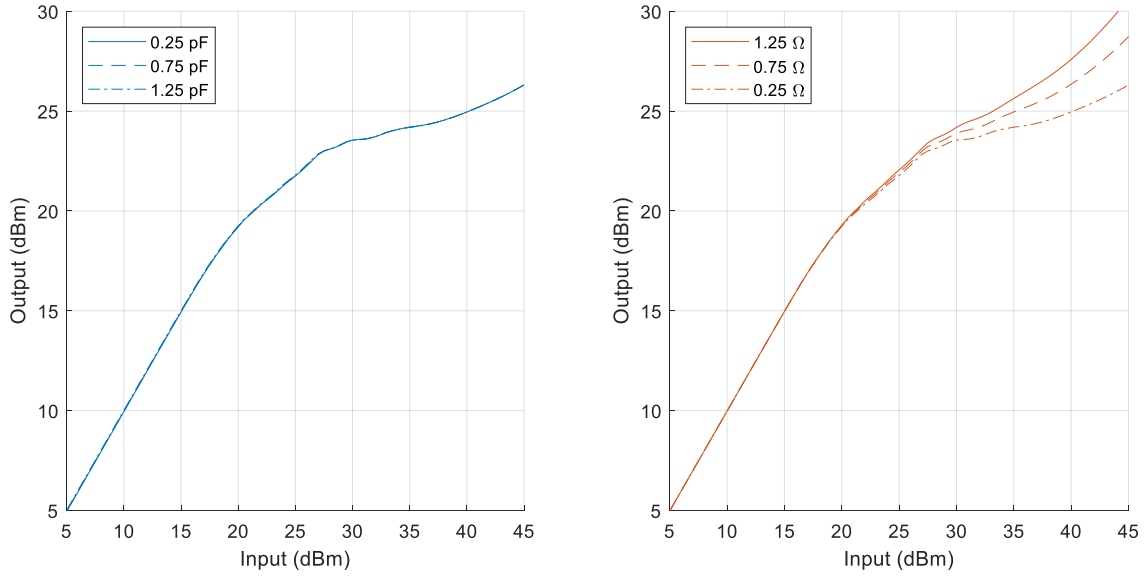
Table 5.2. Summary of the effect of resistance change at 100 MHz.

Resistance (Ω) C_j = 0.75 pF	**Spike leakage (nJ)**	**Flat leakage (dBm)**	**Recovery time (ns)**
1.25	16.99	30.53	58
0.75	17.29	28.46	80
0.25	64.99	26.8	121

5.4.2 Non-linear results

Figure 5.6 shows the non-linear response of traditional limiter at 100 MHz when the parameters are varied. Figure 5.6(a) shows there is no change in the attenuation when varying the capacitance of a diode for a series resistance of 0.25 Ω. This result agrees with the flat leakage result in Table 5.1, which shows no substantial change in flat leakage with increasing

capacitance. This is due to the slow application of the input power to the limiter which provides sufficient time for the charge carriers in the I-layer of the PIN diode to combine and reduce the resistance of the diode. Figure 5.6(b) shows that a decrease in the series resistance of a PIN diode increases the attenuation. It can, therefore, be concluded that any change in the non-linear response or flat leakage of a limiter because of a change in temperature is not due to a change in junction capacitance, but rather because of a change in series resistance.



(a) (b)

Figure 5.6. Effect of capacitance and resistance change on the non-linear response at 100 MHz. (a) Capacitance, $\boldsymbol{R_s}$ = 0.25 Ω. (b) Resistance, $\boldsymbol{C_j}$ = 0.75 pF.

Using Figure 5.5 and Figure 5.6 as a guide, the measured data in the following sections can now be interpreted to better understand the response with the goal of answering the research questions.

5.5 TEST JIG

The PIN diode limiter section is highlighted in Figure 5.7. At the top is the custom coupler that was designed for the detector limiter circuit. The coupler was designed and optimised for 15 dB coupling at 2 GHz. For frequencies lower than 2 GHz, the wavelength becomes too long which would have made the size of the coupler too large for the available PCB space. Below the

coupler is the detector limiter circuit that is shown in Figure 5.3. The resistors R_1 and R_2 are placed as close as possible to the output of the coupler and serves as a matched load for the coupled signal. This is required to prevent the coupled signal from reflecting between the forward and reverse coupled ports. The current produced by the Schottky diodes is applied as a bias current to the PIN diode via the respective RF chokes.

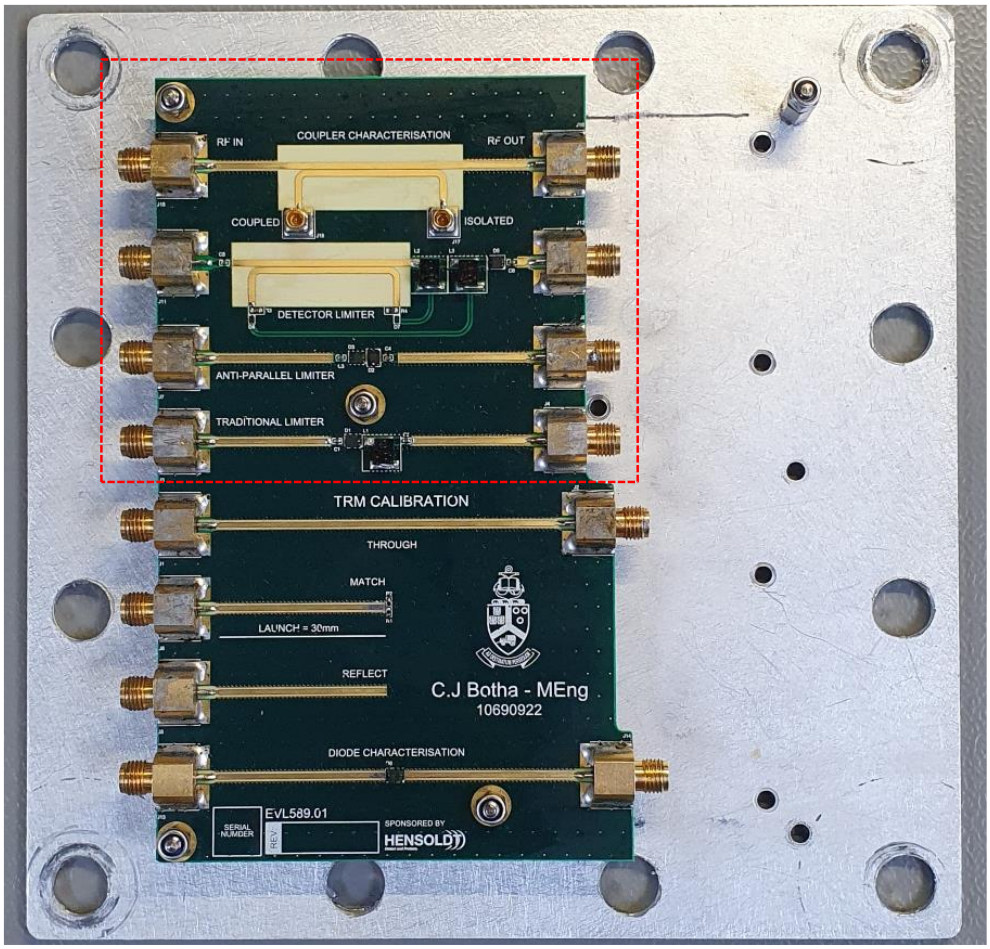
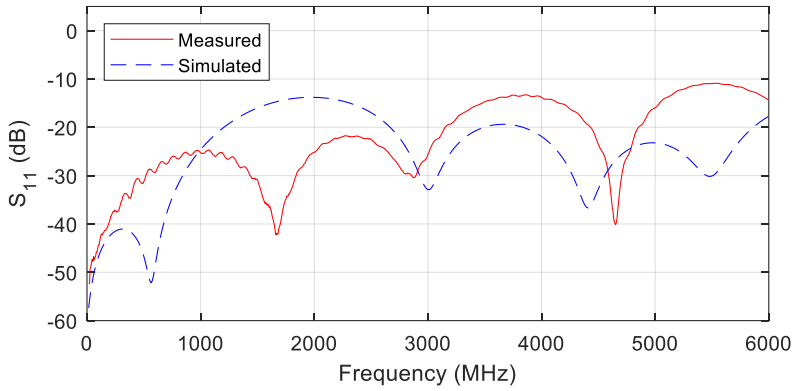


Figure 5.7. Limiter test jig.
From top to bottom: Custom coupler, detector limiter, anti-parallel limiter, traditional limiter.

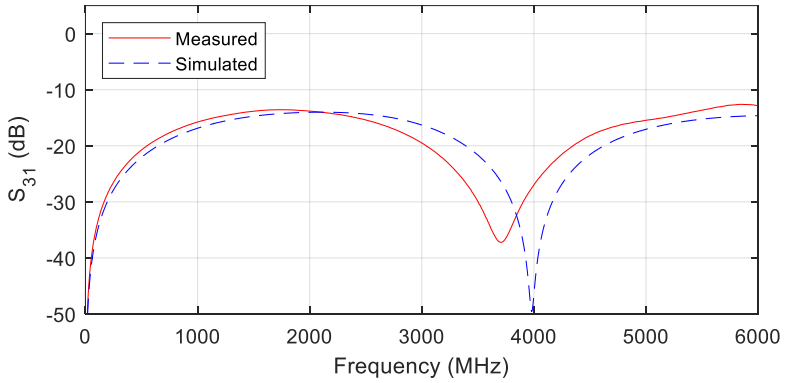
Below the detector limiter is the anti-parallel limiter circuit shown in Figure 5.2. Because the PIN diode is already shunt-mounted in its packaging, the second PIN diode is placed at a 90º angle to the first PIN diode. The two PIN diodes are placed as close to each other as possible. The traditional limiter circuit shown in Figure 5.1 is found below the anti-parallel limiter.

5.6 COUPLER RESULTS

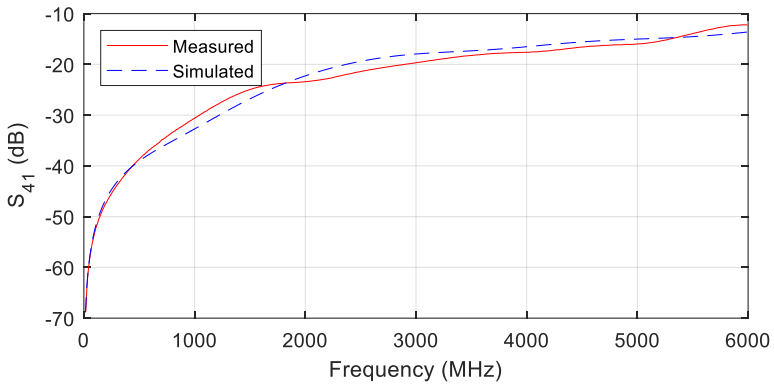
The S_{11} of the designed coupler is shown in Figure 5.8(a). The input reflection is lower than expected below 2000 MHz, which is the intended band of operation. Figure 5.8(b) shows the measured and simulated forward coupled (S_{31}) results of the coupler, indicating a 300 MHz shift in peak coupling frequency likely due to manufacturing tolerances. Two parameters that can influence the frequency in such a way is the dielectric constant, ε_r, of the PCB substrate, and the length of the coupler itself. Nevertheless, a coupling of 13.8 dB at 2000 MHz was still achieved, which is acceptable. The reverse coupled (S_{41}) results is given in Figure 5.8(c) and shows a good agreement with the simulated data.



(a)



(b)



(c)

Figure 5.8. Coupler results.
(a) S_{11}. (b) S_{31}. (c) S_{41}.

5.7 NON-LINEAR RESPONSES

The following section discusses the simulated and measured non-linear response of each limiter topology at different frequencies and temperatures. The simulated responses are given alongside the measured results. Unless otherwise stated, the results shown are for the CLA4608 PIN diode at 25 ºC. Each subsection also provides a comparison between the different PIN diodes in the relevant limiter topology. The different limiter topologies are compared to each other primarily at 100 MHz and 300 MHz and, for the detector limiter, 2000 MHz. Where possible, the results are also compared to the diode manufacturer's data. As was discussed in Section 4.3.3, R_3 (shown in Figure 4.3) again had to be omitted from the diode model to achieve relevant results.

5.7.1 Traditional limiter

5.7.1.1 Frequency

The measured and simulated non-linear responses of the traditional limiter topology is shown in Figure 5.9. The measured data is shown as a solid line, whereas the simulated data is shown with a dashed line. The limiter's schematic is shown in Figure 5.1.

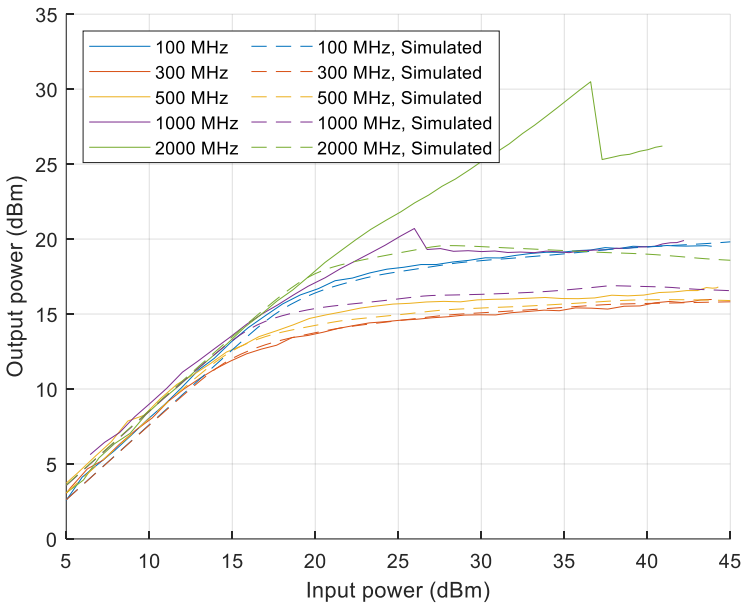


Figure 5.9. Traditional limiter response at different frequencies.

The results show a good agreement between the measured and simulated data. At frequencies below 1000 MHz, the simulated data is nearly identical to the measured data. For frequencies higher than 1000 MHz, the simulated results deviate from the measured results by following a predictable curve, rather than exhibiting a limiting *kink* as is seen in the measured data. This deviation may be attributed to unmodelled effects such as package parasitics and leakage around the package. The measured response at both 1000 MHz and 2000 MHz agrees with the manufacturer's data [71], which shows a similar kink at 24 dBm and 18 dBm input and output power, respectively, at 1000 MHz, and at 34 dBm and 29 dBm input and output power, respectively, at 2000 MHz.

The kink in the output power is likely the diode going into full forward-bias operation, where the I-region is filled with charge carriers and the diode’s impedance at its lowest. The kink seems frequency dependent, with lower frequencies not exhibiting this phenomenon. The output power kink was also observed in a study that compared the performance characteristics of single and dual stage MMIC limiters [72], and reports that the kink is not only repeatable from die to die, but also independent of the number of PIN diode pairs in a multi-stage configuration.

5.7.1.2 Diode

A comparison between the different diodes installed into the traditional limiter topology at 100 MHz and 300 MHz is given in Figure 5.10.

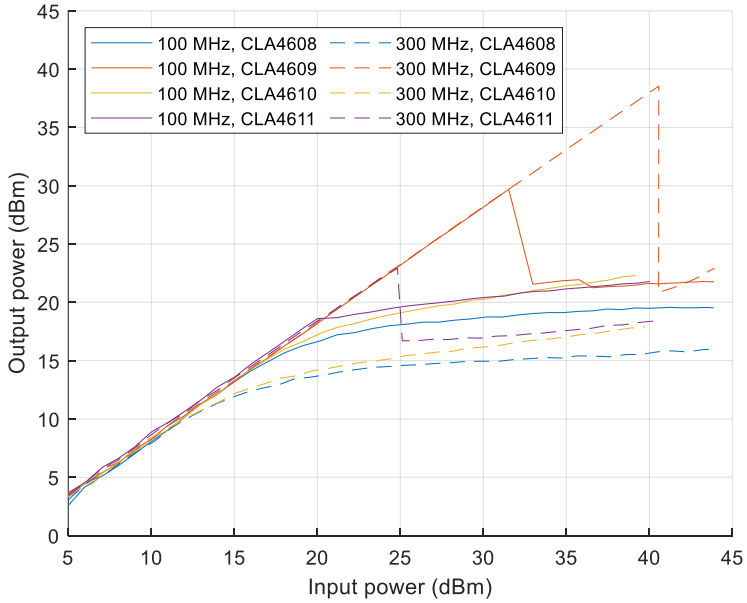


Figure 5.10. Traditional limiter PIN diode comparison at 100 MHz and 300 MHz.

Since the CLA4609 diode (marked in orange) has the thickest intrinsic region of all the diodes (20 µm), it is expected to start attenuating at a much higher input signal level compared to the other, smaller diodes, which can be seen from the measured results at both 100 MHz and 300 MHz. The second largest diode, CLA4611 (12 µm), starts attenuation at the second highest power level, which is also expected. The same kink in the output power that was seen previously with the CLA4608 diode at higher frequencies is observed with the CLA4609 diode at low frequencies.

5.7.1.3 Temperature

Figure 5.11 shows the non-linear measured and simulated response at 100 MHz and 300 MHz at different temperatures. The results show no change in the response due to temperature at lower input levels when the limiter is not activated. For input levels above 15 dBm, the results indicate that, at lower temperatures, the limiter attenuates less compared to higher temperatures. Attenuation is, therefore, increased with temperature. This result is to be

expected since it was shown in Section 4.3.3.2 that the measured PIN diodes have a carrier lifetime temperature coefficient, $\tau_{\text{coefficient}}$, of greater than 2.3, which is indicative of a negative resistance coefficient. It was concluded in [16] and [19] that diodes with a negative resistance coefficient will show attenuation levels increasing with temperature. This is further demonstrated in the simulation result in Figure 5.6(b) for decreasing series resistance.

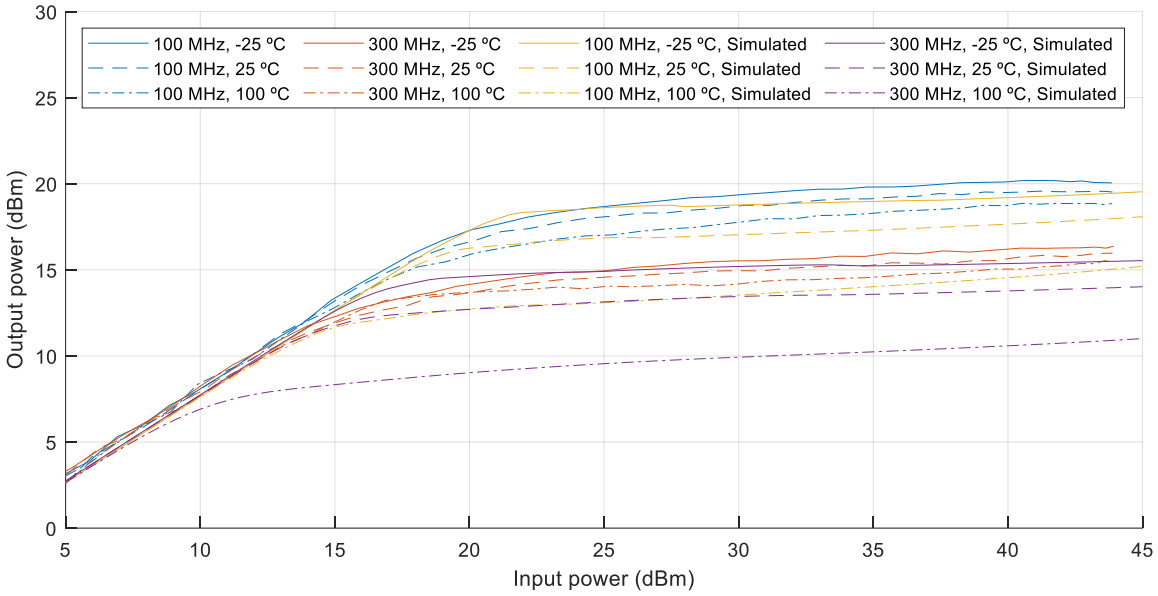


Figure 5.11. Traditional limiter response versus temperature at 100 MHz and 300 MHz.

This effect can clearly be seen at 100 MHz, where the difference in output power between - 25 ºC and 100 ºC at an input level of 30 dBm is around 1.6 dB, compared to a difference of 1.36 dB at 300 MHz. The simulated results show a similar trend, although with a much larger variation over temperature. In comparison to the measured response, the simulated response shows a difference of 5.2 dB at 100 MHz and 300 MHz between -25 ºC and 100 ºC at an input level of 30 dBm.

5.7.2 Anti-parallel limiter

5.7.2.1 Frequency

Figure 5.12 shows the measured and simulated non-linear responses of the traditional limiter topology at different frequencies. The measured data is shown as a solid line, whereas the simulated data is shown with a dashed line. The limiter's schematic is shown in Figure 5.2.

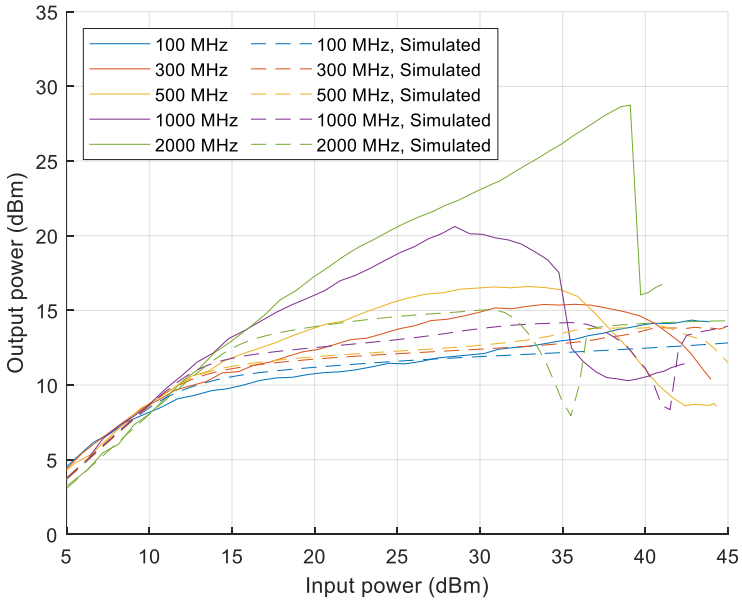


Figure 5.12. Anti-parallel limiter response at different frequencies.

As it was seen with the traditional limiter, the measured and simulated results show a good agreement up to around 15 dBm, after which the simulation shows a flat response for frequencies below 1000 MHz. For frequencies above this, however, the simulated response resembles a limiting *kink*, as it is seen with the measured response, but does not accurately predict the limiter's response. Comparing the simulated and measured response at 1000 MHz and 2000 MHz, the measured response shows a later (in terms of threshold level) and much steeper drop in output power at 2000 MHz than the simulated response, and an earlier and more gradual drop in power at 1000 MHz compared to simulated response. The diode manufacturer does not provide results for this topology.

As it was discussed in [72], the kink is independent on the number of PIN diode pairs, which is why the input power at which the kink occurs is roughly the same between the anti-parallel and traditional limiters (39 dBm compared to 37 dBm, respectively). However, because the anti-parallel configuration has two PIN diodes, the attenuation after the kink is much more compared to the traditional limiter. The simulation also does not consider parasitic coupling around the package at higher frequencies, which may contribute to higher leaked output power at higher frequencies.

5.7.2.2 Diode

Figure 5.13 shows a comparison between the different diodes installed into the anti-parallel limiter topology at 100 MHz and 300 MHz.

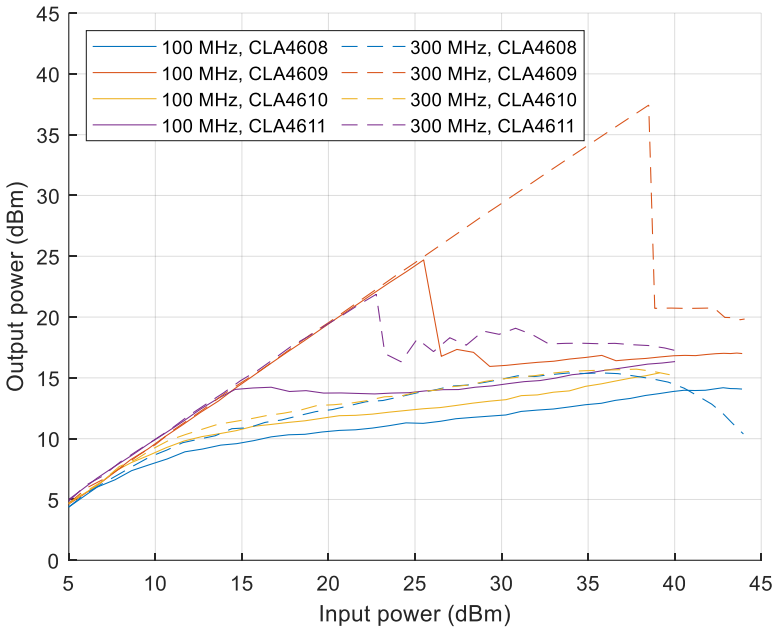


Figure 5.13. Anti-parallel limiter PIN diode comparison at 100 MHz and 300 MHz.

Like the traditional limiter's results, the CLA4609 diode starts attenuating at a much higher input signal level compared to the other, smaller diodes. The second largest diode, CLA4611, again starts attenuation at the second highest power level, which is expected. Both larger diodes also show a limiting kink at 300 MHz, as was seen with the traditional limiter in Figure 5.10.

5.7.2.3 Temperature

The measured and simulated response at 100 MHz and 300 MHz at different temperatures is shown in Figure 5.14. In contrast to what was observed with the traditional topology, the results show a bigger change in output power due to temperature variation at low input power levels (< 10 dBm). This is also seen for the simulated results. Like the traditional limiter, for input levels above 10 dBm, the results indicate that the limiter attenuates less at low temperatures compared to higher temperatures, though again this effect is exaggerated in simulation. For an input level of 30 dBm, the measured response at 100 MHz has a difference in output power of 0.75 dB from -25 ºC to 100 ºC, compared to a simulated difference of 4.1 dB at the same frequency. Between an input level of 15 dBm and 30 dBm, the response at 300 MHz shows the inverse, in that a lower temperature results in more attenuation. For input levels higher than 30 dBm, the response again agrees to those of the other frequencies.

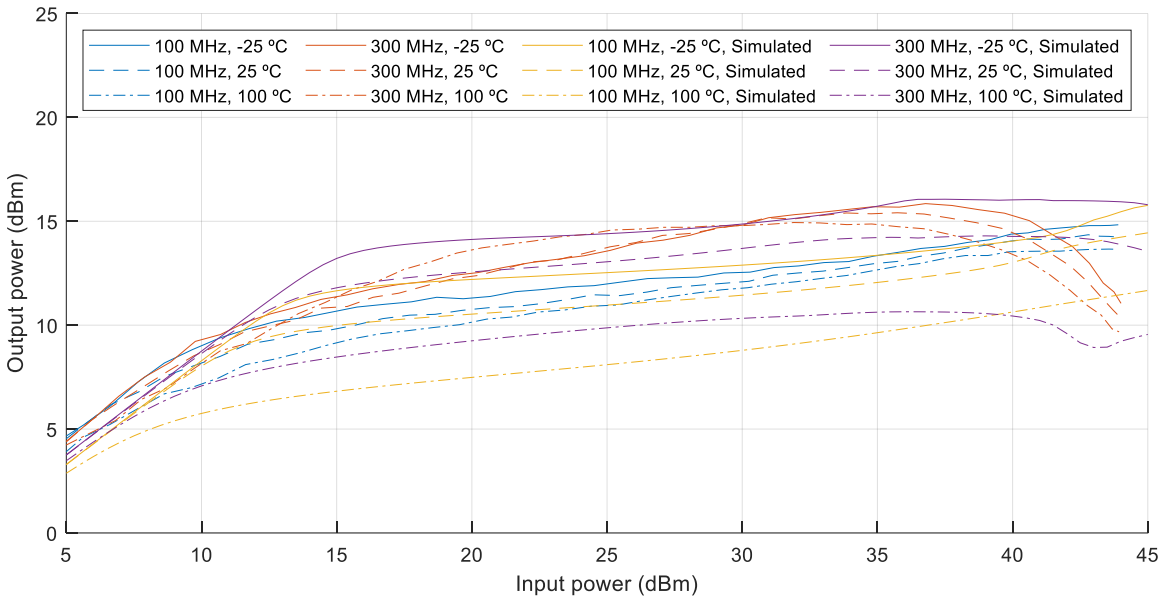


Figure 5.14. Anti-parallel limiter response versus temperature at 100 MHz and 300 MHz.

5.7.3 Detector limiter

5.7.3.1 Frequency

Because the limiter was not designed to function at VHF, only the measured and simulated responses at 1000 MHz and 2000 MHz are presented for this topology. Figure 5.15 shows the detector limiter's measured and simulated frequency response at 25 ºC.

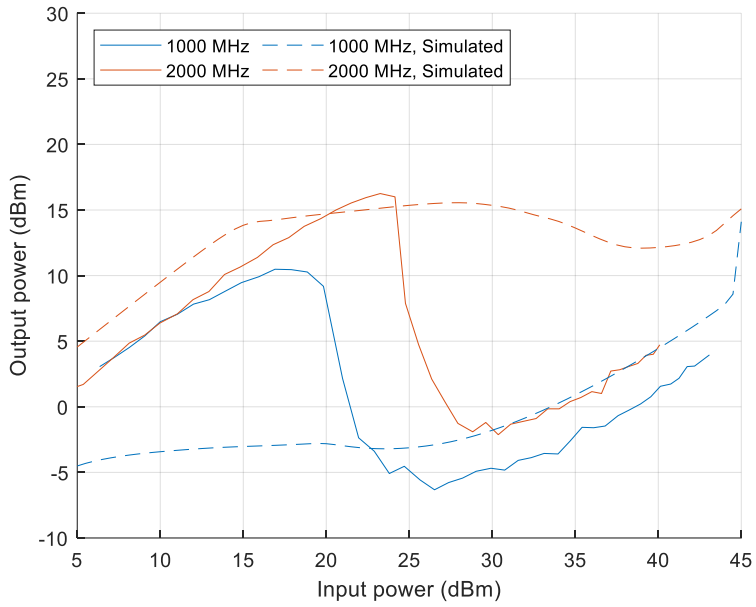


Figure 5.15. Detector limiter response at different frequencies.

At 2000 MHz, where the coupler is most effective, the measured response shows a sharp decrease in output power at an input power level of around 25 dBm. The sharp increase in attenuation can be explained as the incident power biasing the diode through the forward coupled port of the coupler, which causes the incident power to be reflected to the source, which further bias the diode through the reverse coupled port of the coupler. The simulated response does not show this sharp decrease and instead shows flat attenuation up to an input power of around 30 dBm. At 1000 MHz, the simulated response also does not agree well with the measured response, with the simulated response showing increased attenuation at very low input power levels. The measured response at this frequency shows a similar curve to the 2000 MHz response with a sharp decrease at an input power level of around 20 dBm.

5.7.3.2 Diode

A response comparison at 1000 MHz and 2000 MHz between the different PIN diodes installed into the detector limiter topology is shown in Figure 5.16. Because the PIN diode is biased through the coupler and not from the incident signal, the thicker diodes do not start attenuating at a much higher input signal level compared to the other diodes as it was seen with the previous topologies. Instead, the thicker diodes (CLA4609 and CLA4611) show similar attenuation curves to the smaller diodes at all frequencies.

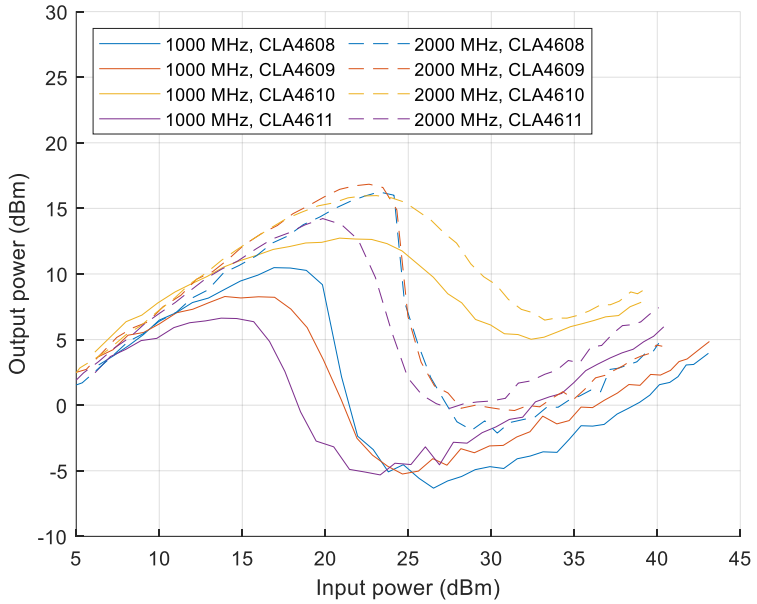


Figure 5.16. Detector limiter PIN diode comparison.

5.7.3.3 Temperature

The measured and simulated response of the limiter at 1000 MHz and 2000 MHz at different temperatures is shown in Figure 5.17. The temperature results show the same trend observed with the previous topologies, which is that at lower temperatures, the limiter attenuates less compared to higher temperatures. At 2000 MHz, the measured response starts to overlap at an input power level of around 30 dBm where the output power is less affected by change in temperature. This is observed at around 23 dBm at 1000 MHz. This could be due to both the forward and reflected coupled power more than sufficiently biasing the PIN diode such that the effect of temperature does not affect the forward resistance of the PIN diode to the extent where

a difference in attenuation can be seen. This is also seen for the simulated response, although the effect differs between 1000 MHz and 2000 MHz, with the temperature response at 1000 MHz showing more variation for lower input power (below 25 dBm), and the response at 2000 MHz showing more variation for higher input power (more than 15 dBm). In contrast, between an input power level of 15 dBm and 30 dBm, this effect of temperature is visible on the measured response as the limiter likely transitions between the off and on state.

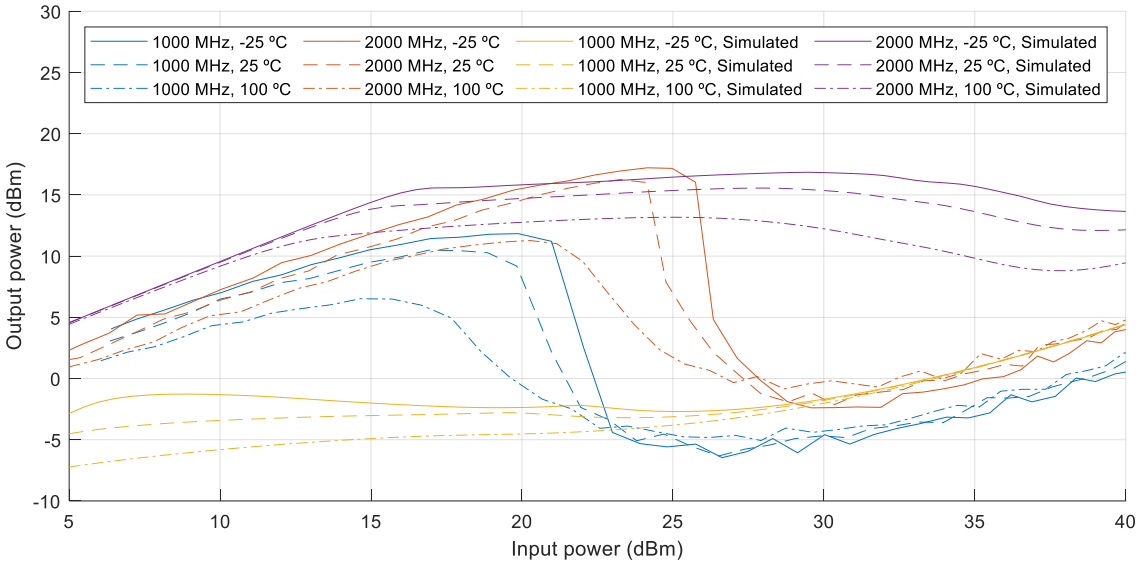


Figure 5.17. Detector limiter response versus temperature at 1000 MHz and 2000 MHz.

5.7.3.4 Comparison of typical and novel detector limiters

Figure 5.18 shows the simulated non-linear comparison at 25 ºC of the novel detector limiter to the typical PIN-Schottky detector limiter circuit shown in Figure 2.13. The results show that the custom detector design which utilizes both the forward and reverse coupled ports of the bi-directional coupler provide more attenuation at 1000 MHz and 2000 MHz than the typical, single port, design. This result was expected since the custom detector utilises the reflected power to further bias the PIN diode.

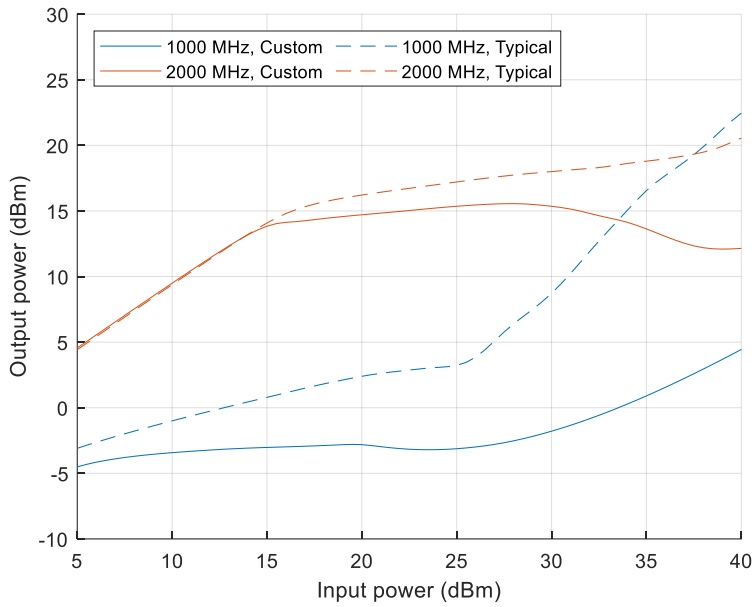


Figure 5.18. Detector limiter comparison to typical PIN-Schottky detector at 1000 MHz and 2000 MHz at 25 ºC.

5.7.4 Topology comparison

A temperature comparison between the traditional and anti-parallel limiter topologies for the CLA4608 diode at 100 MHz is given in Figure 5.19. The results show that the anti-parallel limiter outperforms the traditional limiter topology in terms of threshold level and temperature sensitivity.

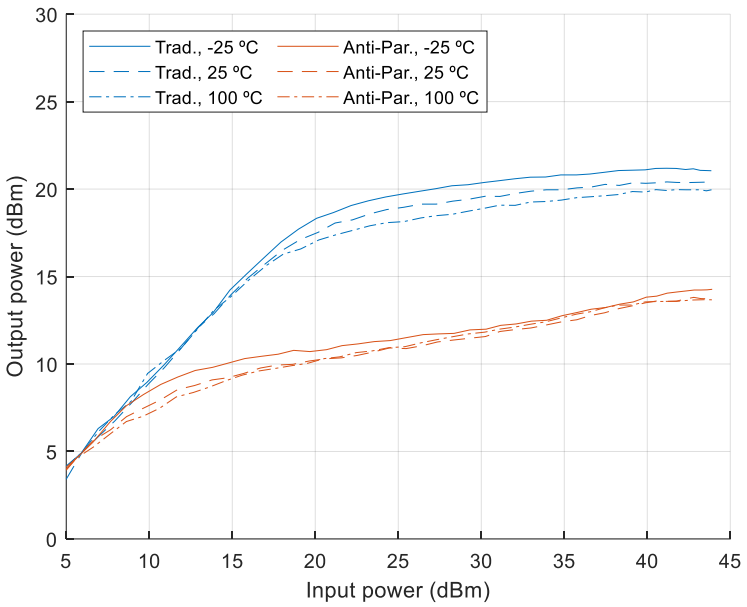


Figure 5.19. Limiter topology comparison at 100 MHz versus temperature.

The same comparison between the two limiter topologies at 300 MHz is given in Figure 5.20. The figure shows that the anti-parallel limiter again performs somewhat better than the traditional limiter, though the distinction is far less pronounced.

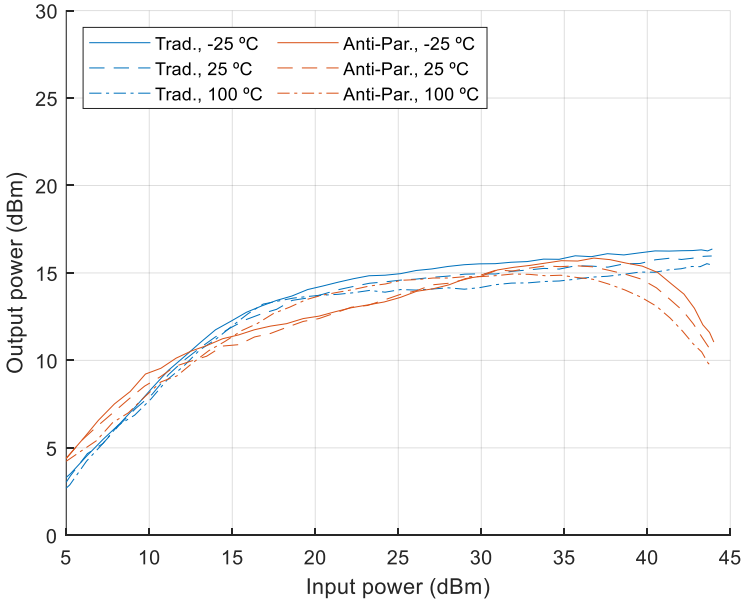


Figure 5.20. Limiter topology comparison at 300 MHz versus temperature.

Figure 5.21 shows the temperature comparison between the different limiter topologies at 2000 MHz. From these results the detector limiter outperforms the traditional and anti-parallel limiters in terms of its threshold level and attenuation (roughly 19 dB of attenuation compared to 6 dB and 12 dB for the traditional and anti-parallel limiters, respectively).

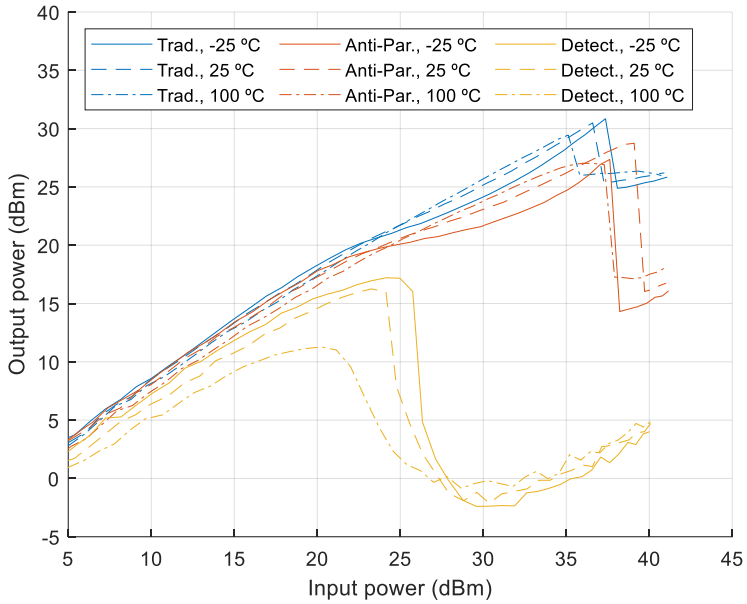


Figure 5.21. Limiter topology non-linear response comparison at 2000 MHz versus temperature.

This is no surprise since the detector limiter is optimised for this frequency. The traditional and anti-parallel limiters are nearly identical with regards to their attenuation with the anti-parallel limiter performing marginally better at input power levels higher than 25 dBm. Both the traditional and anti-parallel limiter has an inverted temperature response at input power levels higher than 25 dBm, showing that a higher temperature has less attenuation compared to a lower temperature at this frequency. The detector limiter does not exhibit this inverted temperature response. Once again, the high frequency of operation effectively negates the limiting action of the traditional and anti-parallel configurations.

Because it was shown in the previous section that the non-linear temperature performance of the limiter is affected by the change in series resistance, it can be summarized that the difference in attenuation observed for the limiters above are because of the decrease in the PIN diode's series resistance due to the increase in temperature, and not because of its capacitance.

5.8 TRANSIENT RESPONSE

The following section discusses the transient response of each limiter topology at different frequencies and temperatures. Unless otherwise stated, the results shown are for the CLA4608 PIN diode at 25 ºC. As in Section 5.7, each limiter topology subsection also provides a comparison between the different PIN diodes in the relevant topology. The different limiter topologies are also compared to each other at 100 MHz, 300 MHz and, for the purpose of including the detector limiter, 2000 MHz. Where possible, the results are also compared to published data. As was discussed in the non-linear section, R_3 (shown in Figure 4.3) had to be omitted from the diode model to achieve relevant results.

As discussed in Section 0, the measured transient responses were captured on an Anritsu spectrum analyser with a video and resolution bandwidth of 40 MHz. This translates to a transient resolution of 25 ns, which is more than sufficient to capture the response of a limiter to a fast incident signal. Furthermore, the spectrum analyser was configured in zero-span mode. Zero span is a mode of a spectrum analyser in which the local oscillator (LO) does not sweep, and instead remains fixed at a given frequency so the analyser becomes a fixed-tuned receiver. The bandwidth of the receiver is that of the resolution bandwidth. When a spectrum analyser is configured in zero span, the signal amplitude (or power) is displayed as a function of time.

5.8.1 Reference pulse measurement

Figure 5.22 shows the reference transient pulse that was used to measure the transient response of the limiter circuits. The figure shows the input pulse at various frequencies over time as measured in dBm. The duration of the pulse is around 1.2 µs. Depending on the frequency, the input pulse has a slightly different rise and fall time. This is due to the hardware that was used to generate the input pulse.

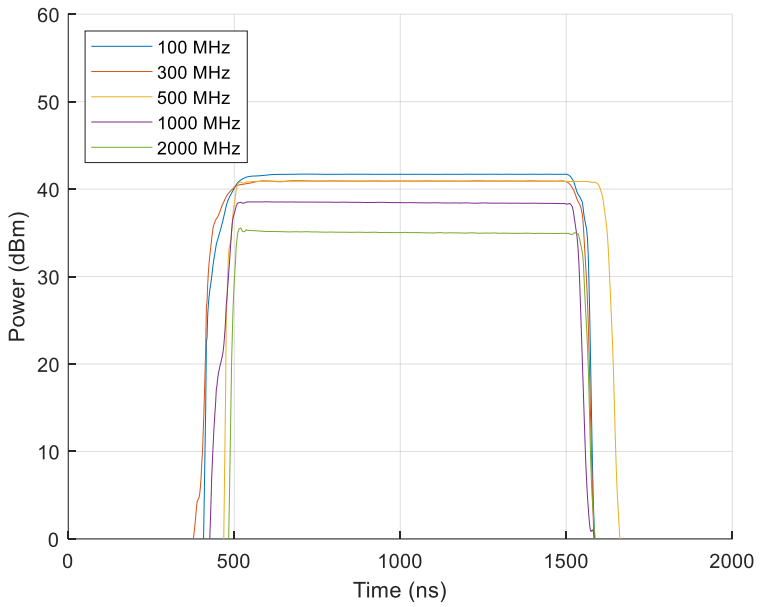


Figure 5.22. Transient thru measurement comparison.

The 10/90 rise and fall time are summarised in Table 5.3. The power level shown is the level measured at the input of the limiter.

Table 5.3. Input pulse characteristics.

Frequency	Rise time (ns)	Fall time (ns)	Power (dBm)
100 MHz	63	29	41.7
300 MHz	63	30	40.9
500 MHz	27	37	40.9
1000 MHz	62	34	38.5
2000 MHz	19	29	35

5.8.2 Traditional limiter

5.8.2.1 Frequency

The measured transient response of the traditional limiter topology is shown in Figure 5.23. The incident signals from Figure 5.22 were applied to the input of the limiter to evaluate the

efficacy of the limiter. The results show that the flat leakage at 100 MHz, 300 MHz, 500 MHz, and 1000 MHz are between 15 dBm and 17 dBm. The flat leakage at 2000 MHz is considerably higher than that of the other frequencies at around 27 dBm, which was also observed for the non-linear response measurements. This could be due to the frequency approaching the self-resonating frequency of the biasing inductor (3.2 GHz), or due to high-frequency parasitic leakage around the diode package.

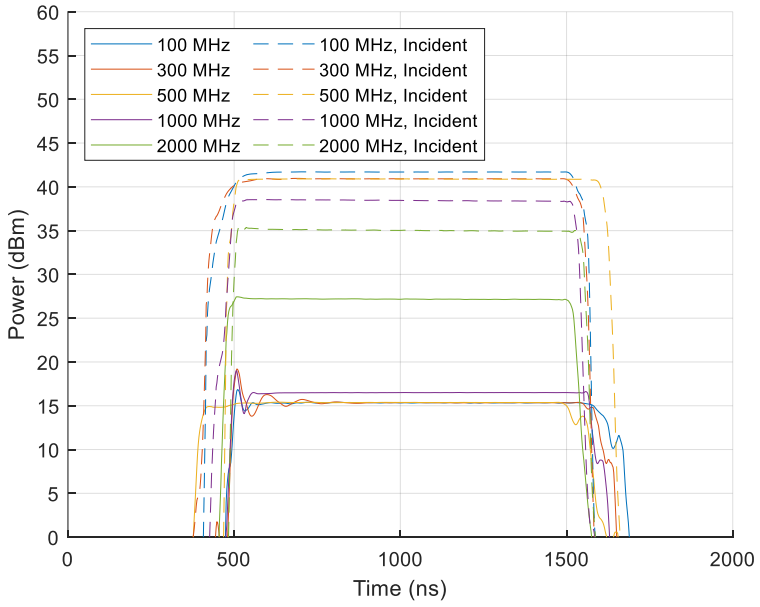


Figure 5.23. Traditional limiter's measured response at different frequencies.

The results further show that at 500 MHz and 2000 MHz, there is almost no spike leakage and, instead, a gradual limiting response is observed. In contrast, the response at 100 MHz, 300 MHz and 1000 MHz clearly shows both the spike leakage and ringing in response to the incident signal.

The simulated response is given in Figure 5.24. The response is divided into subfigures for each frequency and shows the simulated circuit envelope, spike leakage and measured response in milliwatts. The rise and fall time given in Table 5.3 was used to configure the incident pulse of the simulation. However, the measured response can appear shifted on the x-axis due to the measurement procedure. This has no effect on the comparison or performance values. The

simulated response shows spike leakage at 100 MHz, 300 MHz, and 1000 MHz, and almost no spike leakage at 500 MHz and 2000 MHz.

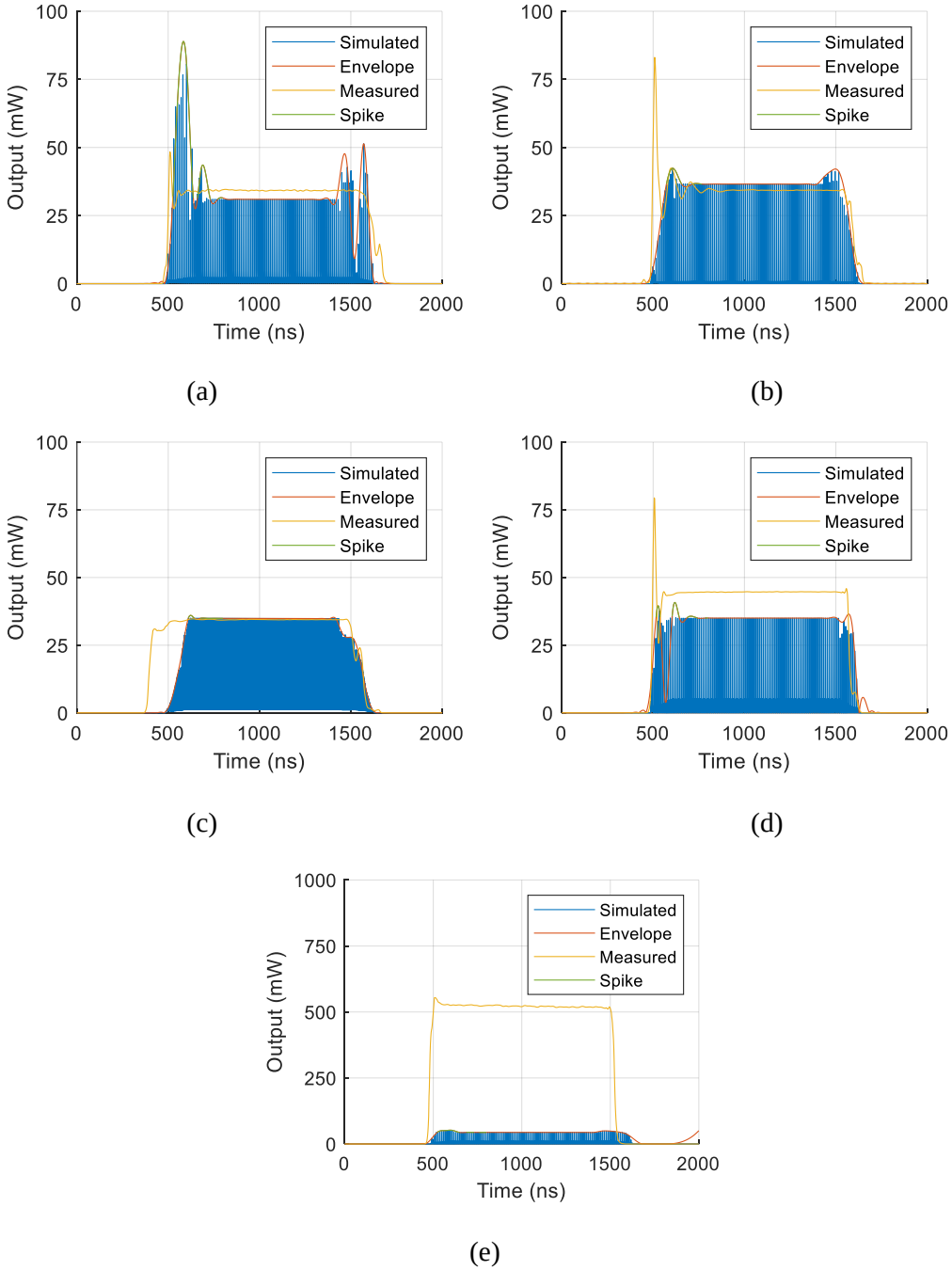


Figure 5.24. Traditional limiter's simulated response at different frequencies. (a) 100 MHz. (b) 300 MHz. (c) 500 MHz. (d) 1000 MHz. (e) 2000 MHz.

Except for the response at 2000 MHz, the simulated flat leakage of all frequencies agrees well with the measured response, with errors ranging between -21.65 % to 6.41 % in milliwatt.

A comparison between the simulated and measured responses in terms of the spike and flat leakage and 10/90 recovery time is given in Table 5.4. The reason for the discrepancy between measured flat leakage and the flat leakage predicted by nonlinear measurements is likely related to the pulsed input signal of the transient response compared to the continuous input signal of the nonlinear response. The absolute difference between the non-linear transmission and transient flat leakage values seems to differ with frequency. This inaccuracy was also observed for the other limiter topologies.

Table 5.4. Traditional limiter's performance versus frequency at 25 ºC.

Frequency	**Spike leakage (nJ)**		**Flat leakage (dBm)**		**Recovery time (ns)**	
	Measured	Simulated	Measured	Simulated	Measured	Simulated
100 MHz	0.1	4.2	15.3	14.61	46	44
300 MHz	0.66	0.59	15.36	15.6	44	67
500 MHz	0.01	0.03	15.37	15.4	42	164
1000 MHz	0.21	0.24	16.5	15.44	25	32
2000 MHz	1.17	0.29	27	16.42	23	98

5.8.2.2 Diode

A comparison between the different diodes installed into the traditional limiter topology at 25 ºC for 100 MHz and 300 MHz is given in Figure 5.25. Since the CLA4609 diode has the thickest intrinsic region of all the diodes (20 µm), it is expected to have significantly more spike leakage compared to the other, smaller diodes, which is evident from the measured nonlinear results at 100 MHz. The second largest diode, CLA4611 (12 µm), has the second most spike leakage at 100 MHz, which is also expected. The reason for the expected results is due to CLA4609 and CLA4611 diode's increased carrier lifetime compared to the smaller diodes. As it was discussed in Section 2.2.1, the response time of the PIN diode is directly

related to the diode's carrier lifetime, and the carrier lifetime is in turn influenced by temperature and the capacitance of the I-layer. Neither of these two larger diodes show any or significant spike leakage at 300 MHz.

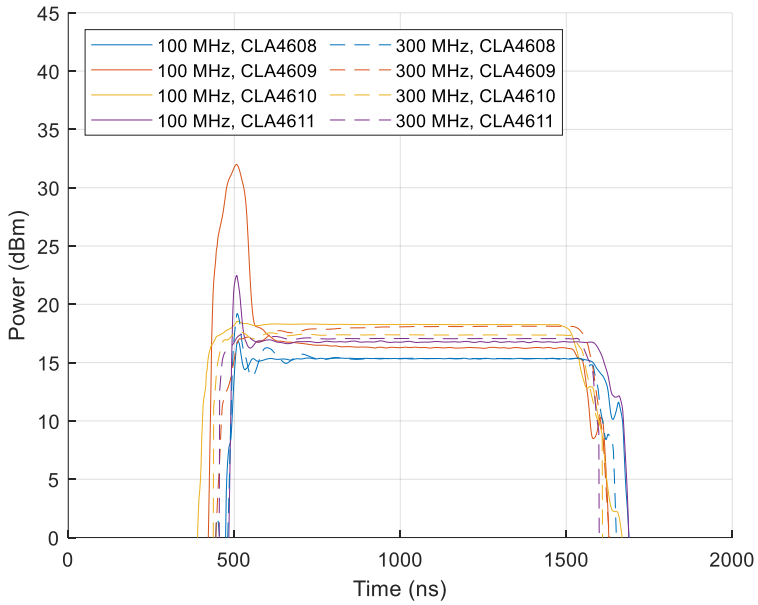


Figure 5.25. Traditional limiter PIN diode comparison at 100 MHz and 300 MHz.

A comparison between the different diode responses at the two frequencies in terms of the spike and flat leakage and 10/90 recovery time is given in Table 5.5.

Table 5.5. Traditional limiter's diode performance at 100 MHz and 300 MHz at 25 ºC.

Frequency	Diode	Spike leakage (nJ)	Flat leakage (dBm)	Recovery time (ns)	Carrier lifetime (ns)
100 MHz	CLA4608	0.1	15.33	46	100
	CLA4609	48.24	16.28	46	1100
	CLA4610	0.1	18.27	51	20
	CLA4611	1.38	16.73	42	300
300 MHz	CLA4608	0.66	15.36	44	100
	CLA4609	0	18.07	32	1100

	CLA4610	0.11	17.38	40	20
	CLA4611	0.11	17.07	26	300

5.8.2.3 Temperature

Figure 5.26(a) shows the measured transient response for the CLA4608 PIN diode at 100 MHz and 300 MHz at different temperatures. The results show a minor decrease in the flat leakage of the response of around 0.7 dB and 0.6 dB from -25 ºC to 100 ºC at 100 MHz and 300 MHz, respectively. The change in spike leakage with temperature is shown in Figure 5.26(b), and shows that, at 100 MHz, the magnitude of the spike increases by roughly 1.2 dB from -25 ºC to 100 ºC, which, in combination with the decreasing flat leakage, increases the spike leakage. At 300 MHz, the inverse occurs, and the magnitude of the spike exhibits a decrease of 0.9 dB from -25 ºC to 100 ºC. However, relative to the decreasing flat leakage at this frequency, the total spike leakage also shows an increase. At 100 MHz, the duration of the spike is also longer at lower temperatures, whereas the opposite is observed at 300 MHz.

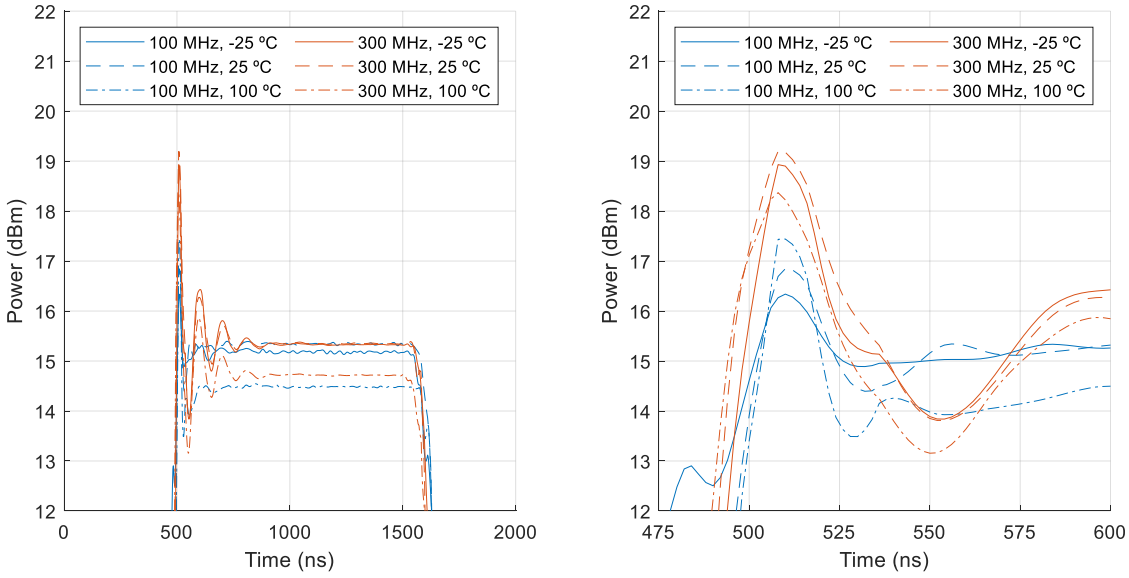


Figure 5.26. Traditional limiter's measured response temperature comparison at 100 MHz and 300 MHz.
(a) Flat leakage comparison. (b) Spike leakage comparison.

The comparison between the simulated and measured responses at 100 MHz and 300 MHz is shown in Figure 5.27(a) – Figure 5.27(c) and Figure 5.27(d) – Figure 5.27(f), respectively. The simulated response shows that the flat leakage decreases with increasing temperatures, while the measurement results exhibit the same trend, but to a far lesser extent.

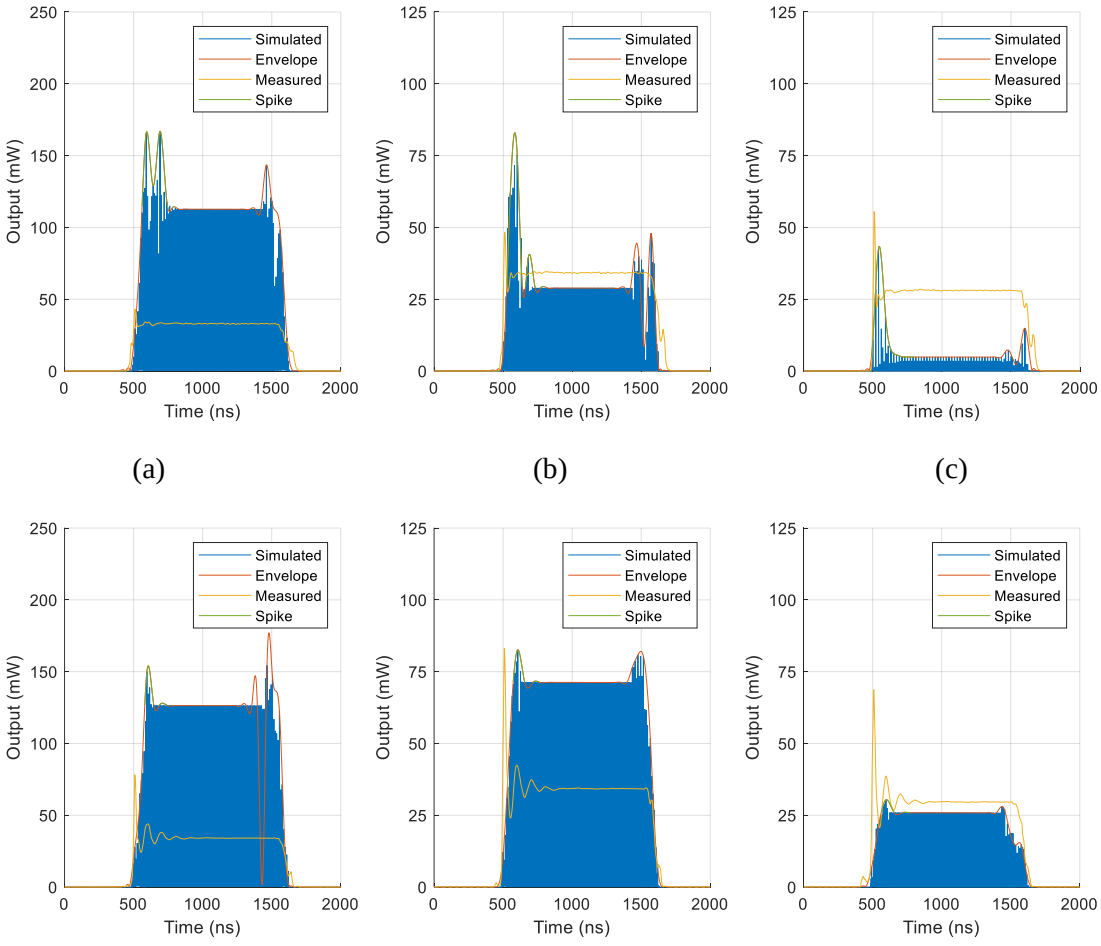


Figure 5.27. Traditional limiter simulated temperature response at 100 MHz and 300 MHz. (a) 100 MHz, -25 ºC. (b) 100 MHz, 25 ºC. (c) 100 MHz, 100 ºC. (d) 300 MHz, -25 ºC. (e) 300 MHz, 25 ºC. (f) 300 MHz, 100 ºC.

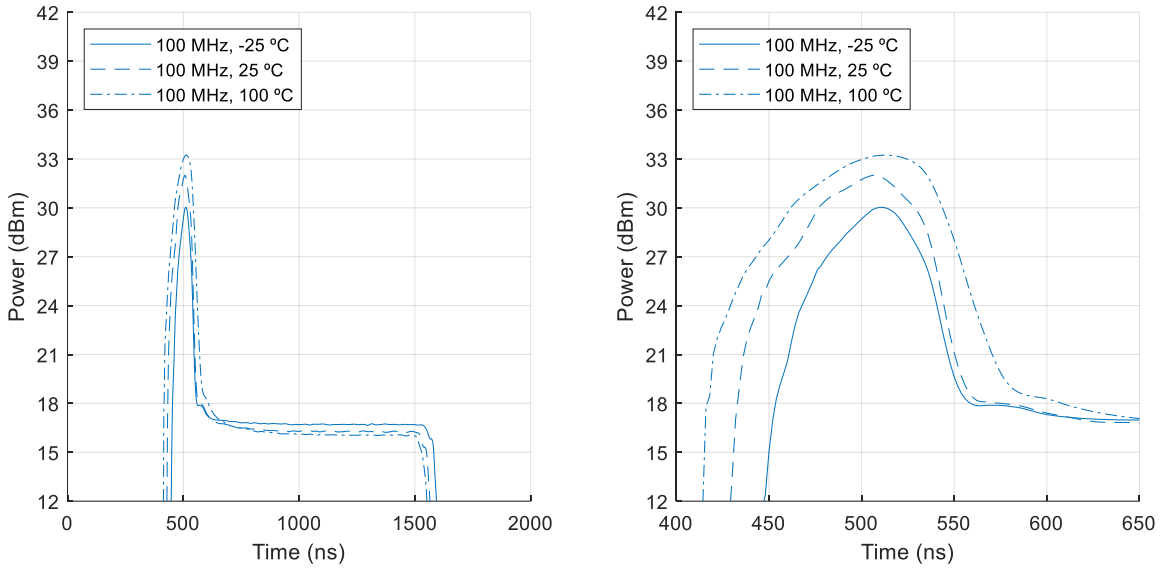
The simulated response shows a decrease in flat leakage between -25 ºC and 100 ºC of around 13.6 dB at 100 MHz, and 6.8 dB at 300 MHz. The model severely over-predicts the circuit's temperature sensitivity. The simulated response shows that the magnitude of the spike decreases with increasing temperature at both 100 MHz and 300 MHz, as opposed to increase like the measured response. Table 5.6 shows a comparison between the simulated and measured

responses at the different frequencies and temperatures in terms of the spike and flat leakage, and 10/90 recovery time. The increase in measured spike leakage is clearly seen, likely due to a decrease in the series resistance with temperature as suggested by Table 5.2, and a near-constant flat leakage. In comparison, the simulation shows a decrease in both spike and flat leakage. The measured recovery time also remains unchanged, compared to mixed results shown by the simulation.

Table 5.6. Traditional limiter's performance at 100 MHz and 300 MHz.

Frequency	Temperature (ºC)	Spike leakage (nJ)		Flat leakage (dBm)		Recovery time (ns)	
		Meas.	Sim.	Meas.	Sim.	Meas.	Sim.
100 MHz	-25	0.1	6.25	15.17	20.52	56	64
	25	0.12	4.2	15.33	14.61	46	44
	100	0.17	2.85	14.46	6.87	49	38
300 MHz	-25	0.54	1.17	15.33	21.02	41	46
	25	0.59	0.59	15.36	18.53	44	67
	100	0.66	0.27	14.73	14.13	43	151

Given the pronounced spike leakage shown by the CLA4609 diode at 100 MHz in Table 5.5, the effect of temperature on its performance in the traditional limiter was evaluated. Figure 5.28(a) shows that the limiter's flat leakage decreases with increasing temperature (more attenuation) due to a decrease in the series resistance at higher temperatures. The results show a decrease in the flat leakage of around 0.6 dB from - 25 ºC to 100 ºC. This result is like what was observed in Table 5.6 for the CLA4608 diode. Figure 5.28(b) clearly shows an increase in the magnitude of the spike leakage from -25 ºC to 100 ºC and, as a result, an increase in the total spike leakage. This can be attributed to the increase in the diode's carrier lifetime which is influenced by temperature and the increase in capacitance of the I-layer, as was shown in Figure 4.7.



(a) (b)

Figure 5.28. Traditional limiter's CLA4609 diode temperature response at 100 MHz. (a) Flat leakage comparison. (b) Spike leakage comparison.

Table 5.7 shows a summary of the limiter's performance shown in Figure 5.28. The table shows a clear trend of increasing spike leakage and constant flat leakage with increasing temperature. The recovery time of the limiter does not seem to be affected by the change in temperature and remains nearly constant at around 44 ns.

Table 5.7. Traditional limiter with CLA4609 PIN diode performance versus temperature at 100 MHz.

Frequency	Temperature (ºC)	Spike leakage (nJ)	Flat leakage (dBm)	Recovery time (ns)
100 MHz	-25	24.33	16.7	44
	25	48.24	16.28	46
	100	83.75	16.1	44

5.8.3 Anti-parallel limiter

5.8.3.1 Frequency

The measured transient response of the anti-parallel limiter topology is shown in Figure 5.29.

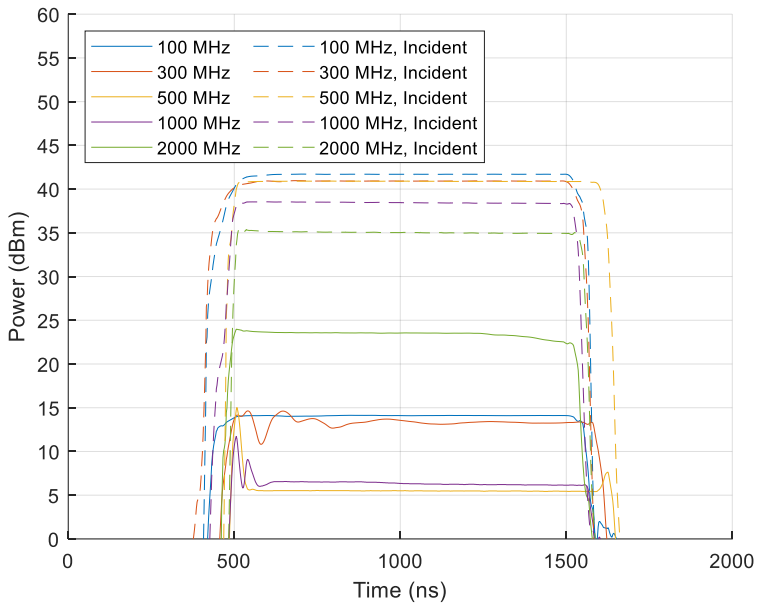


Figure 5.29. Anti-parallel limiter measured response at different frequencies.

The results show that the flat leakage at 100 MHz and 300 MHz are between 13 dBm and 14 dBm, whereas the flat leakage at 500 MHz and 1000 MHz are near identical at around 6 dBm. As with the traditional limiter topology, the flat leakage at 2000 MHz is also considerably higher than that of the other frequencies at around 23 dBm. This agrees with the limiter's non-linear response at 2000 MHz that was shown in Figure 5.12, where weak attenuation was also evident for input power levels below 38 dBm. The results further show that at 100 MHz and 2000 MHz, there is almost no spike leakage, whereas the response at 300 MHz, 500 MHz and 1000 MHz shows both the spike leakage and ringing in response to the incident signal.

Figure 5.30 shows the simulated transient response for the anti-parallel limiter. The responses at 300 MHz and 2000 MHz show multiple spikes which appears to be ringing before reaching flat leakage. This ringing is also seen at 300 MHz for the measured response. The simulated response at 100 MHz, 300 MHz and 2000 MHz agrees well with the measured response, unlike the response at 500 MHz and 1000 MHz, which greatly over and under simulates the response compared to the measured response at those frequencies.

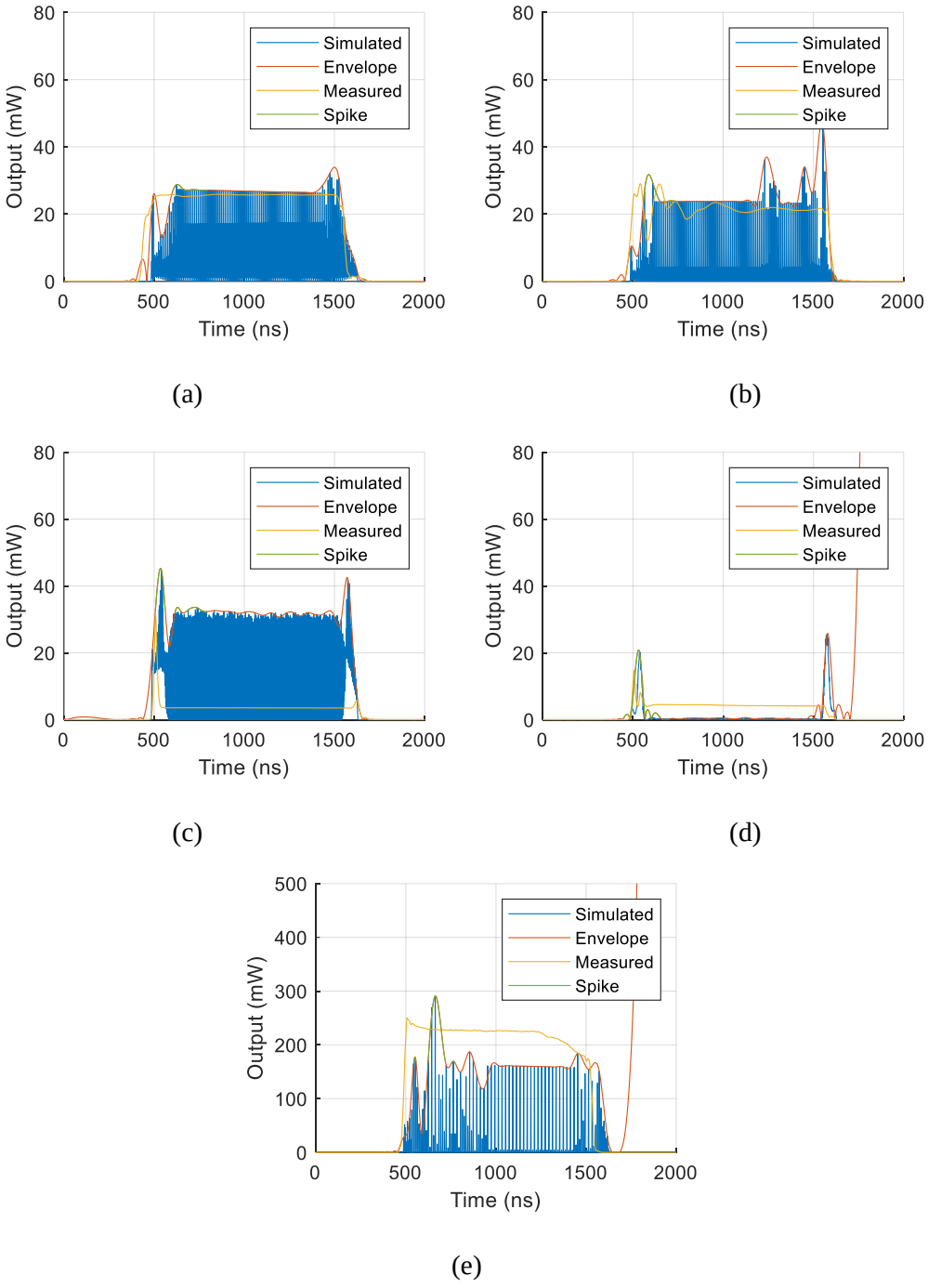


Figure 5.30. Anti-parallel limiter simulated response at different frequencies. (a) 100 MHz. (b) 300 MHz. (c) 500 MHz. (d) 1000 MHz. (e) 2000 MHz.

The performance values of the simulated and measured responses are given in Table 5.8. As it was discussed in Section 5.8.2.1, the measured and simulated flat leakage values does not

correlate well with the non-linear power transfer curve shown in Figure 5.12 at all frequencies, with large discrepancies seen at 500 MHz and 1000 MHz.

Table 5.8. Anti-parallel limiter's measured and simulated performance values.

Frequency	Spike leakage (nJ)		Flat leakage (dBm)		Recovery time (ns)	
	Measured	Simulated	Measured	Simulated	Measured	Simulated
100 MHz	0	0.13	14.1	14.29	22	87
300 MHz	0.25	0.42	13.57	13.76	25	22
500 MHz	0.28	0.61	5.5	15.06	23	126
1000 MHz	0.13	0.14	6.34	-2.56	28	76
2000 MHz	0.79	7.52	23.54	22.18	77	51

5.8.3.2 Diode

A comparison between the different diodes installed into the anti-parallel limiter topology at 100 MHz and 300 MHz is shown in Figure 5.31.

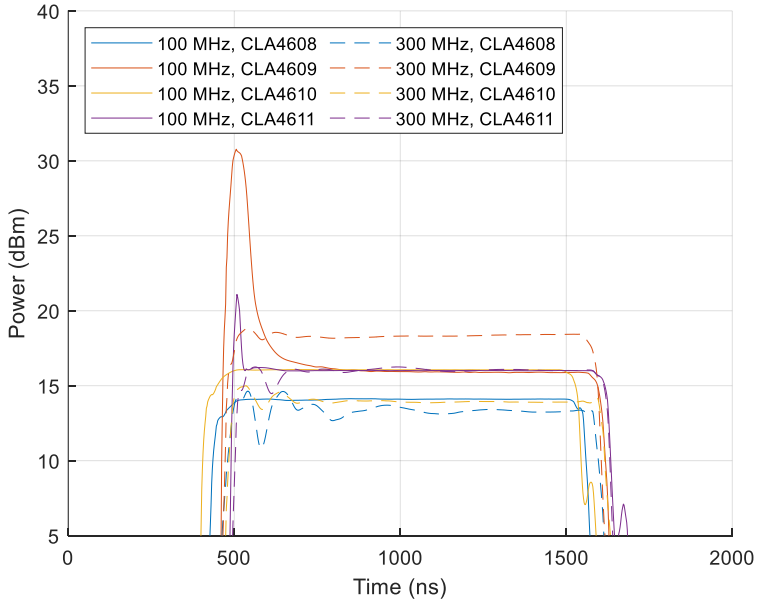


Figure 5.31. Anti-parallel limiter PIN diode comparison.

As it was seen in the previously topology, the CLA4609 and CLA4611 diodes have substantially more spike leakage compared to the other, smaller diodes, at 100 MHz, which again can be contributed to their longer carrier lifetime. However, both these larger diodes have a similar or higher flat leakage than both the smaller diodes. The magnitude of the flat leakage at 300 MHz corresponds to the non-linear response of the diodes given in Figure 5.13, which showed that the CLA4609 diode has the highest saturation level, followed by the CLA4611, CLA4610 and CLA4608, respectively The performance characteristics of the different diode responses at the two frequencies in terms of the spike and flat leakage and 10/90 recovery time are given in Table 5.9.

Table 5.9. Anti-parallel limiter's diode performance values at 100 MHz and 300 MHz.

Frequency	Diode	Spike leakage (nJ)	Flat leakage (dBm)	Recovery time (ns)	Carrier lifetime (ns)
100 MHz	CLA4608	0	14.1	22	100
	CLA4609	30.27	15.94	22	1100
	CLA4610	0.01	16.06	34	20
	CLA4611	0.77	16	19	300
300 MHz	CLA4608	0.25	13.57	24	100
	CLA4609	0.24	18.3	21	1100
	CLA4610	0.27	13.92	19	20
	CLA4611	0	16.25	24	300

5.8.3.3 Temperature

Figure 5.32 shows the transient response at 100 MHz and 300 MHz for different temperatures for the CLA4608 PIN diode. The results show a clear decrease in the flat leakage from -25 ºC to 100 ºC of 1.1 dB at 100 MHz, and around 1.7 dB at 300 MHz. Figure 5.32(b) shows the change in spike leakage with temperature at 100 MHz and 300 MHz. There is very little or no spike leakage to report on at both frequencies. However, at 100 MHz, the results show that the 'knee' power level reduces with increasing temperature, whereas a lot of ringing is seen at

300 MHz. Even though the flat leakage in Figure 5.32(a) decreases with temperature, the magnitude of the spikes remains roughly the same at between 14 dBm and 15 dBm from -25 ºC to 100 ºC, which increases the total energy through the limiter and, as a result, increases the spike leakage. The results shown in Figure 5.32 are summarised in Table 5.10.

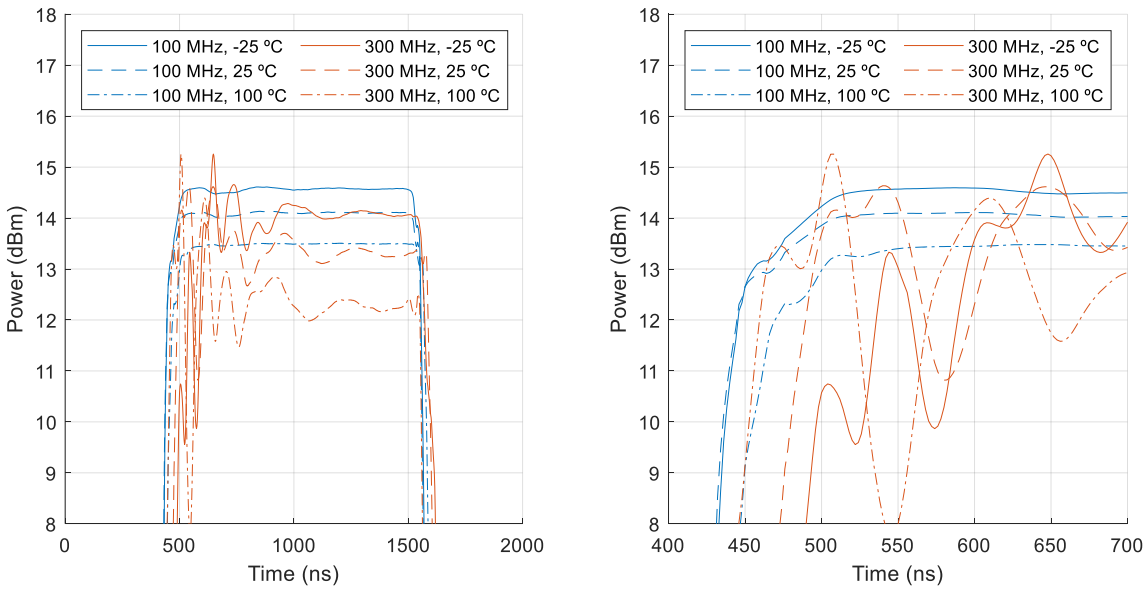


Figure 5.32. Anti-parallel limiter measured response temperature comparison at 100 MHz and 300 MHz.
(a) Flat leakage comparison. (b) Spike leakage comparison.

This decrease in flat leakage (though an over-estimation of it) is confirmed by the simulated responses shown in Figure 5.33, which shows a decrease of 3.87 dB and 7 dB at 100 MHz and 300 MHz, respectively. At 300 MHz, the simulation shows that significantly lower spike leakage is generated at higher temperatures (0.38 nJ), compared to lower temperature (2.06 nJ), whereas the measured response shows an increase in spike leakage with temperature. It is evident that the simulation struggles to accurately model the variation in spike leakage and flat leakage of the limiter circuit over temperature.

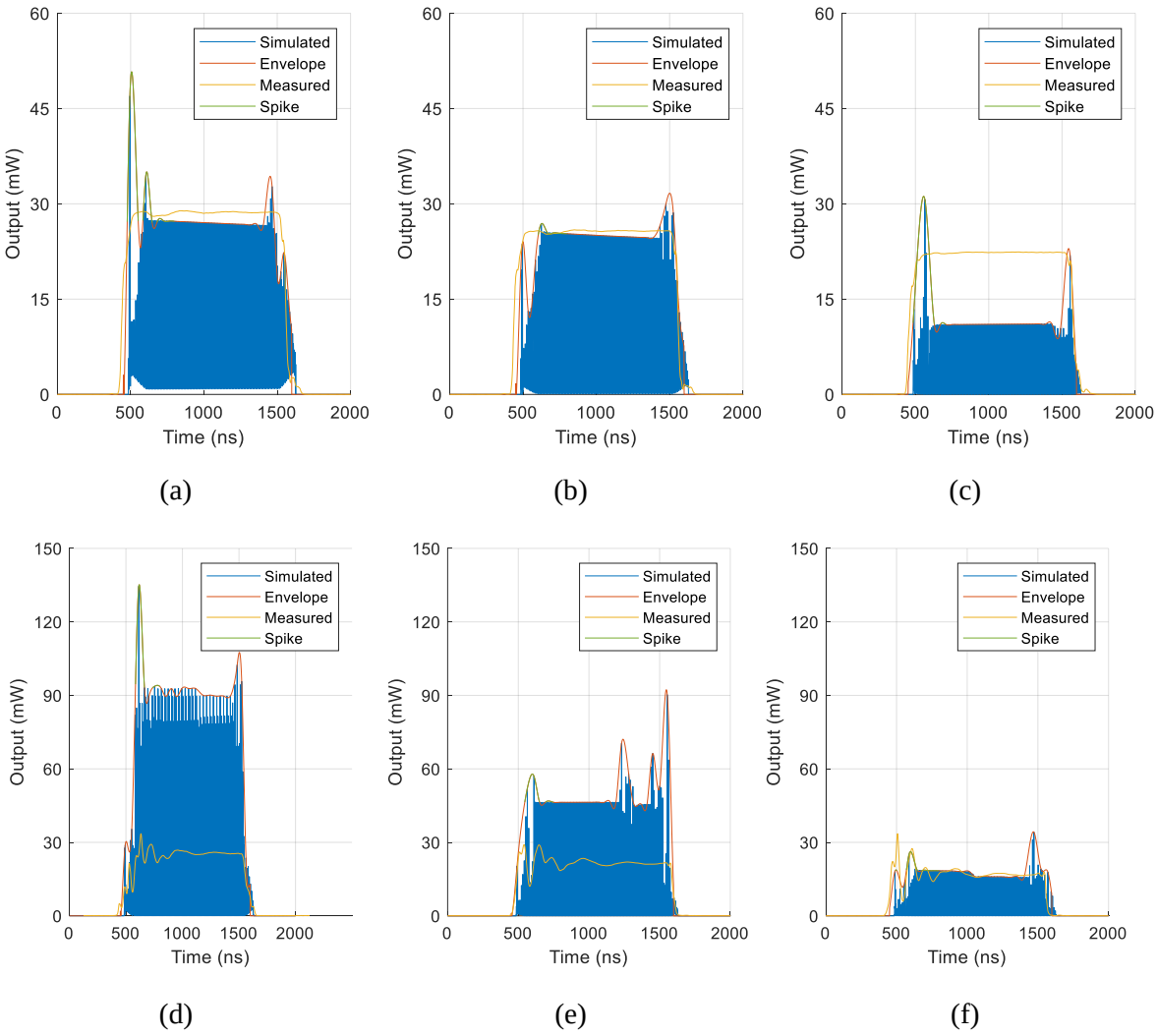


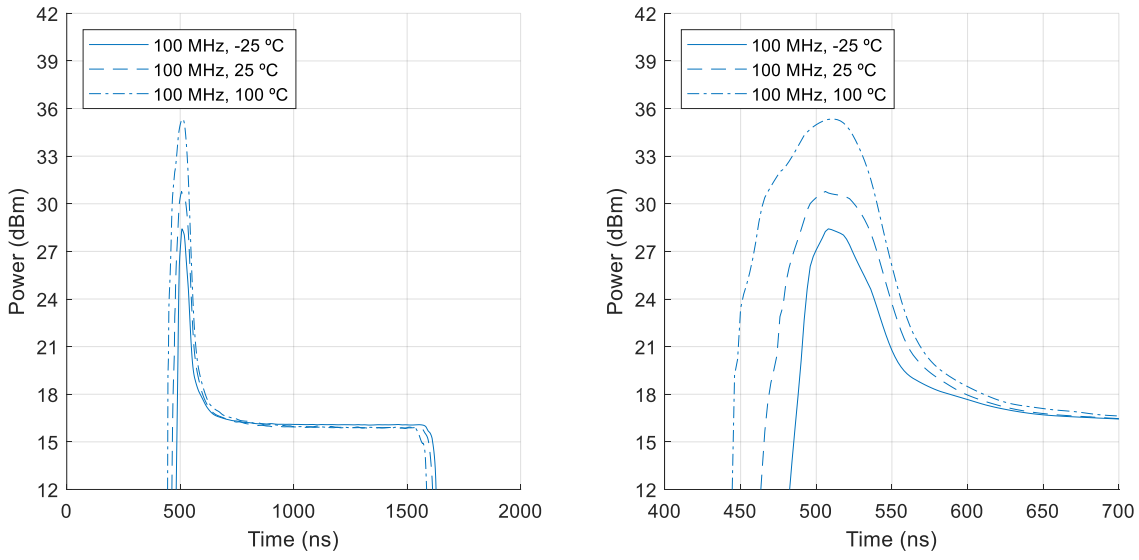
Figure 5.33. Anti-parallel limiter simulated temperature response at 100 MHz and 300 MHz. (a) 100 MHz, -25 ºC. (b) 100 MHz, 25 ºC. (c) 100 MHz, 100 ºC. (d) 300 MHz, -25 ºC. (e) 300 MHz, 25 ºC. (f) 300 MHz, 100 ºC.

Table 5.10 shows a summary of the simulated and measured performance characteristics of the limiter at the different frequencies and temperatures shown in Figure 5.32 and Figure 5.33 in terms of the spike and flat leakage and 10/90 recovery time. The decrease in flat leakage with increasing temperature is due to the decreasing series resistance of the diode as was predicted in Table 5.2.

Table 5.10. Anti-parallel limiter's measured performance values at 100 MHz and 300 MHz.

Frequency	Temperature (ºC)	Spike leakage (nJ)		Flat leakage (dBm)		Recovery time (ns)	
		Meas.	Sim.	Meas.	Sim.	Meas.	Sim.
100 MHz	-25	0.01	1.43	14.55	14.3	28	113
	25	0	0.12	14.1	13.99	22	57
	100	0	1.71	13.49	10.43	30	51
300 MHz	-25	0.19	2.06	13.98	19.68	17	67
	25	0.25	0.75	13.57	16.66	26	66
	100	0.49	0.38	12.28	12.65	11	62

The CLA4609 PIN diode again shows substantial spike leakage at 100 MHz in Table 5.9 compared to the other diodes, and the effect of temperature on its performance in the anti-parallel limiter was again evaluated. The performance of the anti-parallel limiter with the CLA4609 diode is shown in Figure 5.34.



(a) (b)

Figure 5.34. Anti-parallel limiter's CLA4609 diode temperature response at 100 MHz. (a) Flat leakage comparison. (b) Spike leakage comparison.

Figure 5.34 (a) shows that the limiter's flat leakage decreases marginally with increasing temperature (more attenuation), with the results showing a decrease in the flat leakage of around 0.14 dB from -25 ºC to 100 ºC. Figure 5.34(b) shows a clear increase in the magnitude of the spike leakage of about 6.8 dB from -25 ºC to 100 ºC and, as a result, an increase in the total spike leakage. A summary of the limiter's performance that is shown in Figure 5.34 is given in Table 5.11. As it was also seen with the CLA4609 diode in the traditional limiter topology, the table shows a clear trend of increasing spike leakage with increasing temperature. The results do show a small decrease in the flat leakage, but less than the traditional limiter topology. Considering Table 5.2, an increase in spike leakage and decrease in flat leakage would suggest that this is due the decrease in series resistance with temperature. This can also be attributed to the increase in the diode's carrier lifetime which is influenced by temperature and the increase in capacitance of the I-layer, as was shown in Figure 4.7. The recovery time of the limiter also does not seem to be affected by the change in temperature and remains nearly constant at 23 ns.

Table 5.11. Anti-parallel limiter with CLA4609 PIN diode performance versus temperature at 100 MHz.

Frequency	Temperature (ºC)	Spike leakage (nJ)	Flat leakage (dBm)	Recovery time (ns)
100 MHz	-25	12.93	16.1	23
	25	30.27	15.94	22
	100	97.9	15.96	23

5.8.4 Detector limiter

5.8.4.1 Frequency

The measured transient response of the detector limiter topology is shown in Figure 5.35. At 2000 MHz, for which the coupler is optimised, the measurement shows better performance in terms of spike leakage (0.02 nJ) compared to the response at 1000 MHz (0.04 nJ). The response at 1000 MHz has slightly better flat leakage performance compared to the flat leakage at 2000 MHz at -1.04 dBm and -0.54 dBm, respectively.

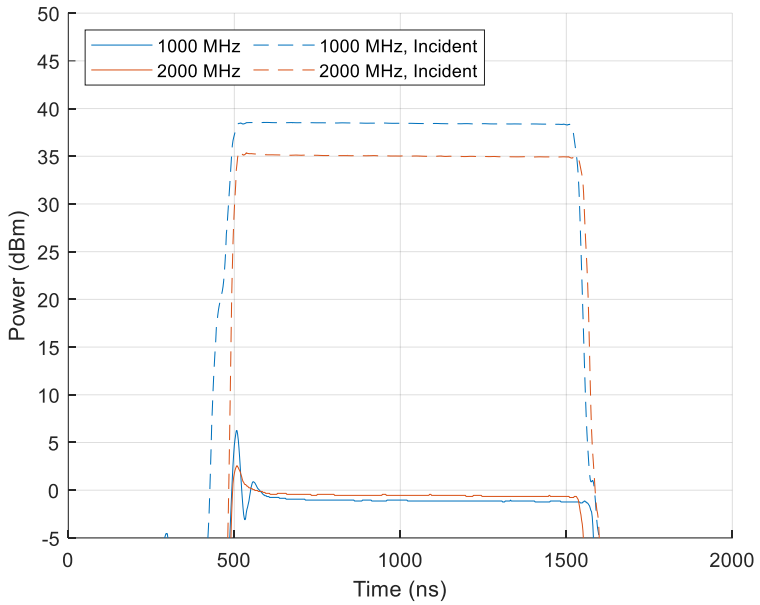


Figure 5.35. Detector limiter measured response at different frequencies.

Relative to the incident signal at the two frequencies, the detector limiter provides substantial attenuation with minimal spike leakage. The simulated response shown in Figure 5.36 shows higher spike and flat leakages at both frequencies compared to the measured response, with the response at 2000 MHz more significant. However, like the measured response, the simulated response does show that the flat leakage increases slightly from 1000 MHz to 2000 MHz.

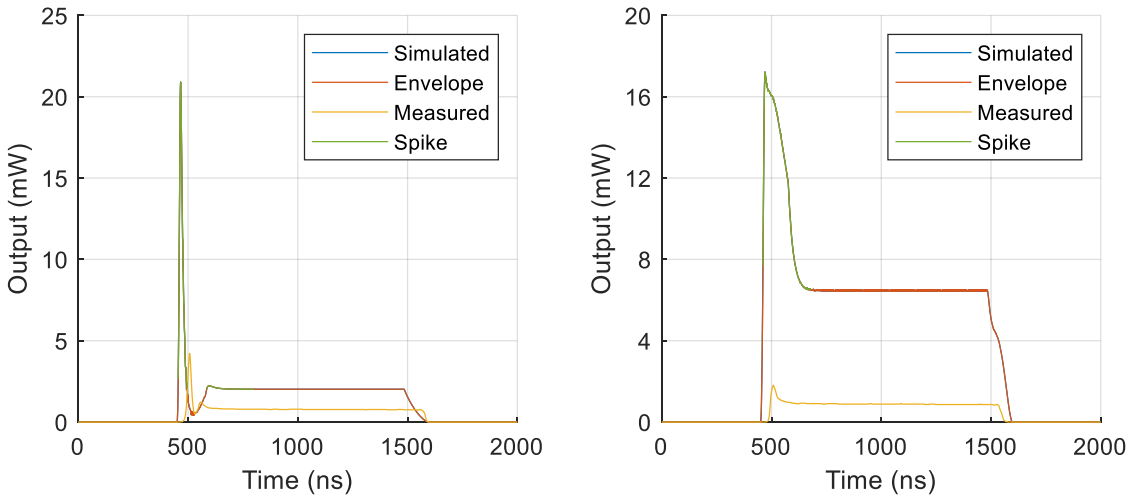


Figure 5.36. Detector limiter simulated response at different frequencies.
(a) 1000 MHz. (b) 2000 MHz.

The performance values of the simulated and measured responses shown in Figure 5.35 and Figure 5.36 are summarised in Table 5.12.

Table 5.12. Detector limiter's measured and simulated performance values at 25 ºC.

Frequency	Spike leakage (nJ)		Flat leakage (dBm)		Recovery time (ns)	
	Measured	Simulated	Measured	Simulated	Measured	Simulated
1000 MHz	0.04	0.32	-1.04	3.05	10	79
2000 MHz	0.02	1.06	-0.54	8.13	11	91

5.8.4.2 Diode

Figure 5.37 shows a comparison between the different PIN diodes installed into the detector limiter topology at different frequencies.

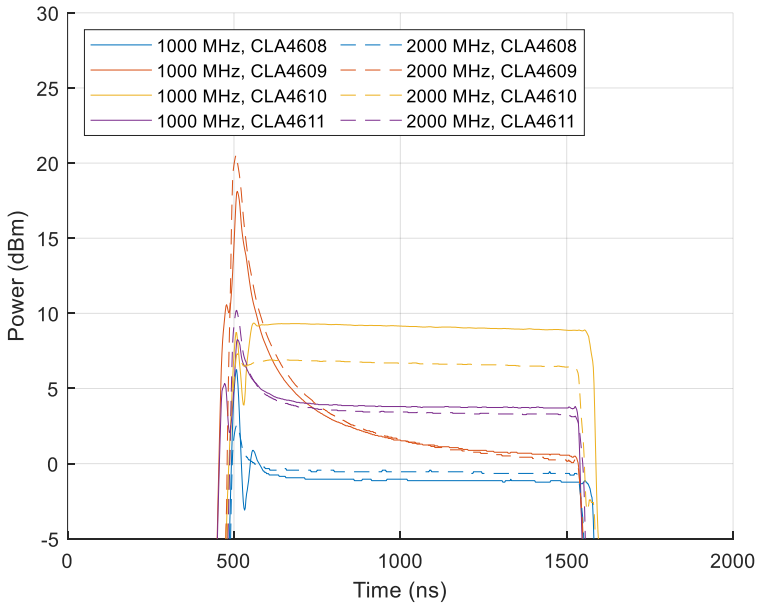


Figure 5.37. Detector limiter PIN diode comparison at 1000 MHz and 2000 MHz.

Like the non-linear response, the thicker diodes show more spike leakage at both frequencies compared to the smaller diodes but not significantly worse responses as was seen with the previous topologies. The CLA4609 diode shows a prolonged leakage period compared to the smaller diodes as the charge carriers must transit the entire intrinsic layer. However, their power

handling capability is better as seen in their lower flat leakage towards the end of the pulse when the diode is fully switched on. The performance characteristics of the different diode responses at the two frequencies in terms of the spike and flat leakage and 10/90 recovery time are given in Table 5.13.

Table 5.13. Detector limiter's measured diode performance values at 1000 MHz and 2000 MHz.

Frequency	Diode	Spike leakage (nJ)	Flat leakage (dBm)	Recovery time (ns)	Carrier lifetime (ns)
1000 MHz	CLA4608	0.04	-1.04	10	100
	CLA4609	1.43	1.57	38	1100
	CLA4610	0.03	9.15	14	20
	CLA4611	0.11	3.79	7	300
2000 MHz	CLA4608	0.02	-0.54	11	100
	CLA4609	2.26	1.63	38	1100
	CLA4610	0.03	6.68	26	20
	CLA4611	0.18	3.44	13	300

5.8.4.3 Temperature

The detector limiter's transient response for the CLA4608 PIN diode at 1000 MHz and 2000 MHz for different temperatures is shown in Figure 5.38(a). Between -25 ºC and 100 ºC, the flat leakage at 2000 MHz shows a slight increase in value from -0.65 dB to -0.13 dB, respectively. At 1000 MHz, the flat leakage decreases from -0.76 dB to -1.04 dB between -25 ºC and 25 ºC but increases very slightly from -1.04 dB to -0.94 dB between 25 ºC and 100 ºC. This result correlates with the limiter's non-linear response shown in Figure 5.17, which showed that for an input signal level higher than 30 dBm, the limiter has less attenuation at higher temperatures.

The change in spike leakage due to temperature is shown in Figure 5.38(b). At both 1000 MHz and 2000 MHz, the magnitude of the spike increases noticeably. This may be due to either

changes in the PIN diode itself, as it was seen with the previous limiter topologies, or changes in the PCB dielectric constant due to temperature, which negatively affects the coupling of coupler as the temperature increases, in turn causing more spike and flat leakage to occur at these temperatures.

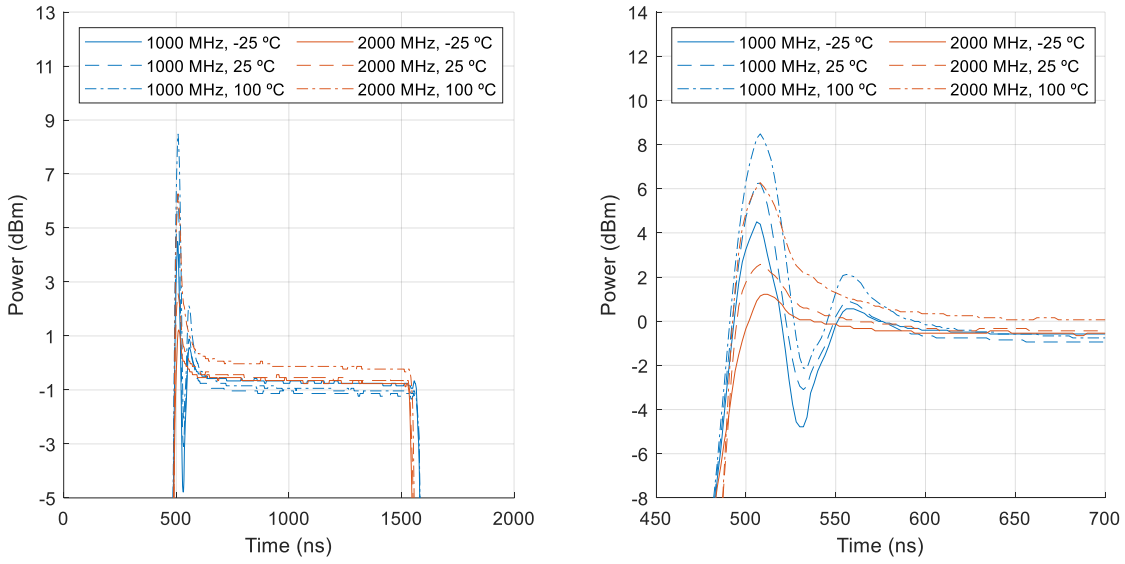


Figure 5.38. Detector limiter measured response temperature comparison at 1000 MHz and 2000 MHz.
(a) Flat leakage comparison. (b) Spike leakage comparison.

The simulated temperature response for 1000 MHz is shown in Figure 5.39(a) through Figure 5.39(c). The response shows a clear decrease in the magnitude of the spike leakage and an insignificant decrease in flat leakage from -25 ºC and 100 ºC, compared to an increase in the spike and flat leakage of the measured response. The simulated temperature response for 2000 MHz is shown in Figure 5.39(d) through Figure 5.39(f), and also shows a decrease in both the flat and spike leakage with increasing temperature, which also contrasts with the measured response which shows and increase in both the flat and spike leakage with increasing temperature. As with the previous limiter topologies, the simulation results predict a decrease in spike and flat leakage with increasing temperature, while the measured results indicate an increase in these metrics.

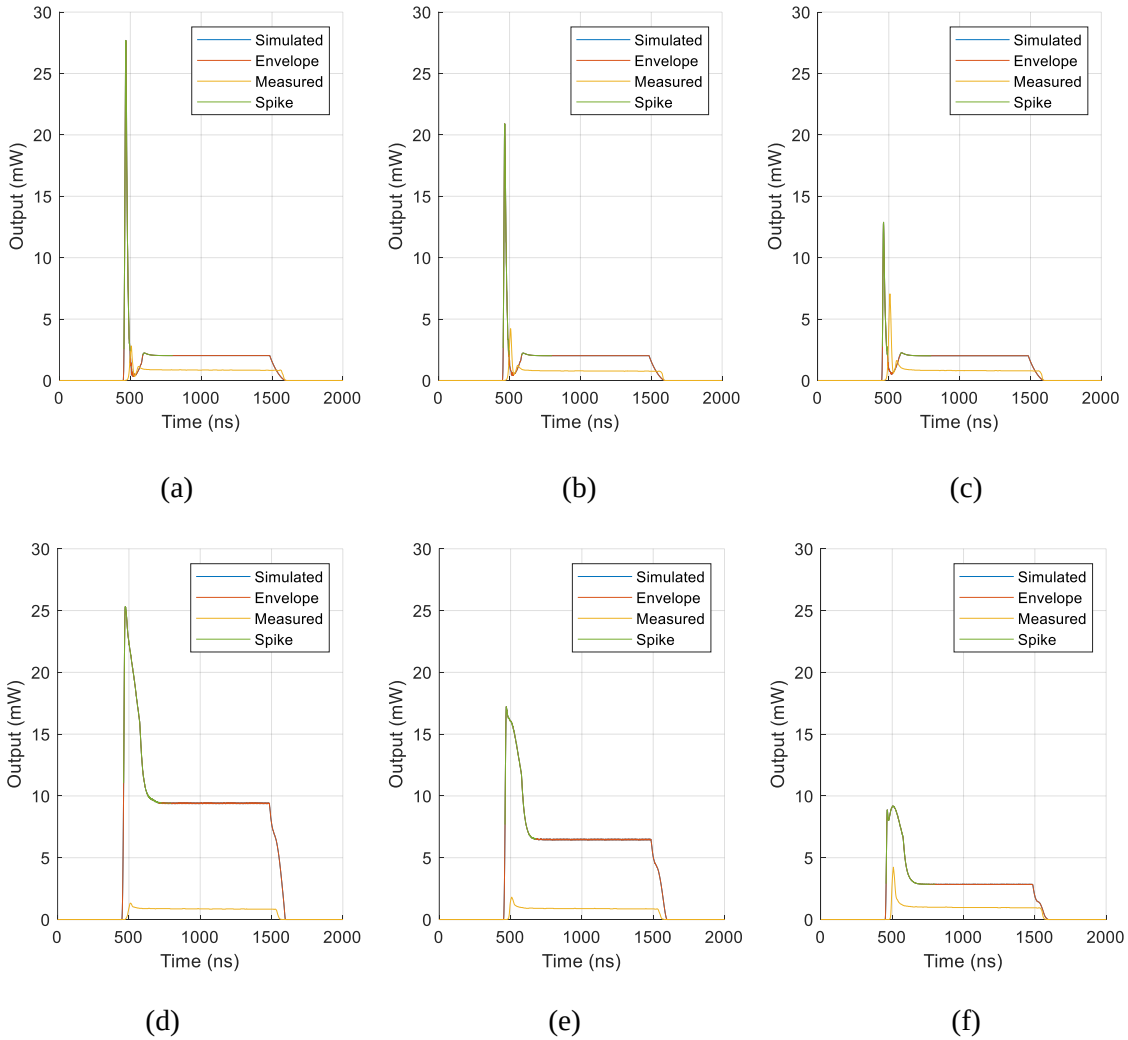


Figure 5.39. Anti-parallel limiter simulated temperature response at 1000 MHz and 2000 MHz. (a) 1000 MHz, -25 ºC. (b) 1000 MHz, 25 ºC. (c) 1000 MHz, 100 ºC. (d) 2000 MHz, -25 ºC. (e) 2000 MHz, 25 ºC. (f) 2000 MHz, 100 ºC.

Table 5.14 shows a summary of the simulated and measured performance characteristics of the results shown in Figure 5.38 and in Figure 5.39 at the different frequencies and temperatures in terms of the spike and flat leakage and 10/90 recovery time.

Table 5.14. Detector limiter's measured performance values at 1000 MHz and 2000 MHz.

Frequency	Temperature (ºC)	Spike leakage (nJ)		Flat leakage (dBm)		Recovery time (ns)	
		Meas.	Sim.	Meas.	Sim.	Meas.	Sim.
1000 MHz	-25	0.02	0.45	-0.76	3.07	11	79
	25	0.04	0.32	-1.04	3.05	10	79
	100	0.07	0.17	-0.94	3.04	10	78
2000 MHz	-25	0.01	1.4	-0.65	9.74	11	97
	25	0.02	1.06	-0.54	8.13	11	91
	100	0.05	0.73	-0.13	4.54	10	81

As it was seen with the traditional and anti-parallel limiter topologies, the size of the CLA4609 diode causes much more spike leakage in the detector limiter topology as well. The CLA4609 PIN diode shows more spike leakage at 2000 MHz in Table 5.13 compared to the other diodes, and, therefore, the effect of temperature on its performance in the detector limiter at 2000 MHz was investigated. Figure 5.40(a) shows that the limiter's flat leakage increases with increasing temperature (less attenuation), with the results showing an increase in the flat leakage at 1000 ns of around 3.8 dB from -25 ºC to 100 ºC. This increase was also observed with the CLA4608 diode shown in Figure 5.38(a) but differs from the traditional and anti-parallel topologies which showed a decrease in flat leakage with increasing temperature. Figure 5.40(b) shows a clear increase in the magnitude of the spike leakage of about 5 dB from -25 ºC to 100 ºC and, as a result, an increase in the total spike leakage.

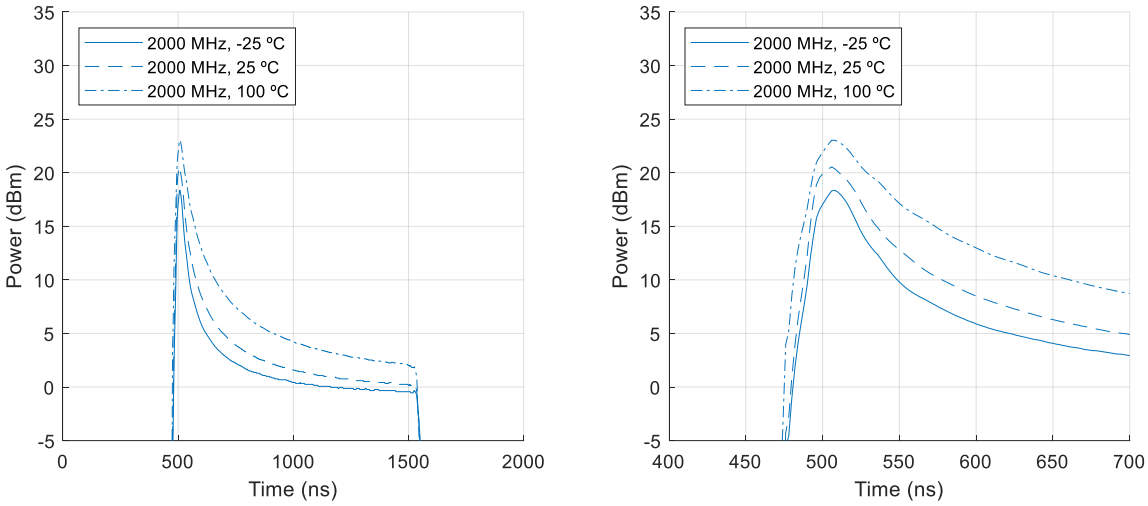


Figure 5.40. Detector limiter's with CLA4609 diode temperature response at 2000 MHz. (a) Flat leakage comparison. (b) Spike leakage comparison.

A summary of the limiter's performance that is shown in Figure 5.40 is given in Table 5.15. As it was seen with the CLA4609 diode in the traditional and anti-parallel limiter topologies, the table shows a clear trend of increasing spike leakage with increasing temperature. The recovery time of the limiter shows an increase with temperature, with a noticeable step observed from -25 ºC to 25 ºC.

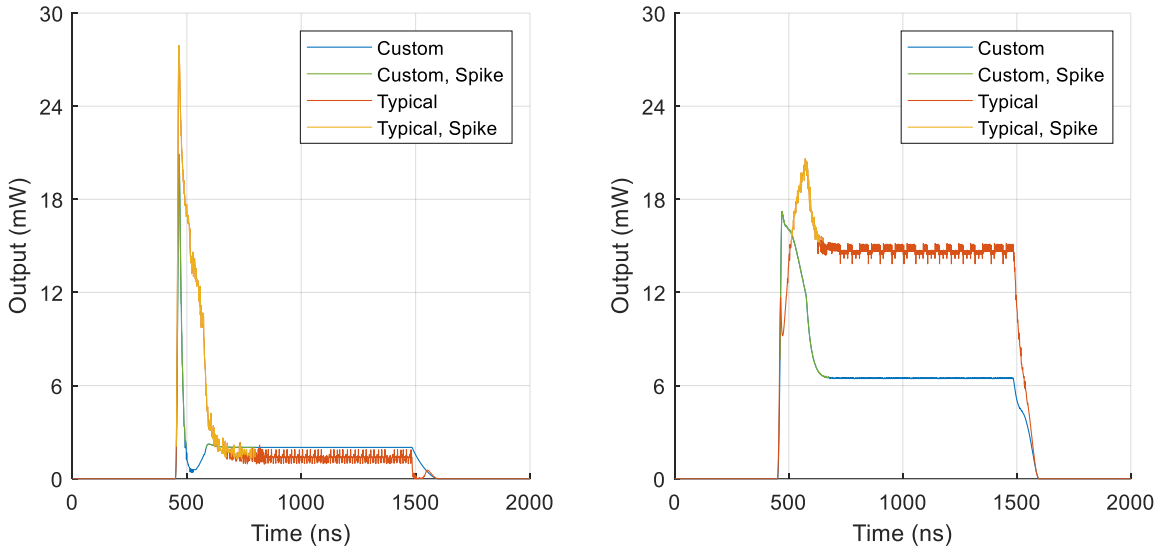
Table 5.15. Detector limiter with CLA4609 PIN diode performance versus temperature at 2000 MHz.

Frequency	Temperature (ºC)	Spike leakage (nJ)	Flat leakage (dBm)	Recovery time (ns)
2000 MHz	-25	1.24	0.43	39
	25	2.26	1.63	38
	100	5.01	4.26	35

5.8.4.4 Comparison of typical and novel detector limiters

The simulated transient comparison of the custom detector limiter to the typical PIN-Schottky detector limiter circuit (shown in Figure 2.13) is shown in Figure 5.41. The comparison is at

25 ºC. Both limiter topologies were simulated using the bi-directional coupler that was designed for this study at both frequencies.



(a) (b)

Figure 5.41. Detector limiter comparison to typical PIN-Schottky detector at 25 ºC. (a) 1000 MHz. (b) 2000 MHz.

The results show that the custom detector design has a lower flat leakage but more spike leakage at 2000 MHz, and less spike leakage but slightly higher flat leakage at 1000 MHz than the typical design. The performance values of both circuits are summarised in Table 5.16.

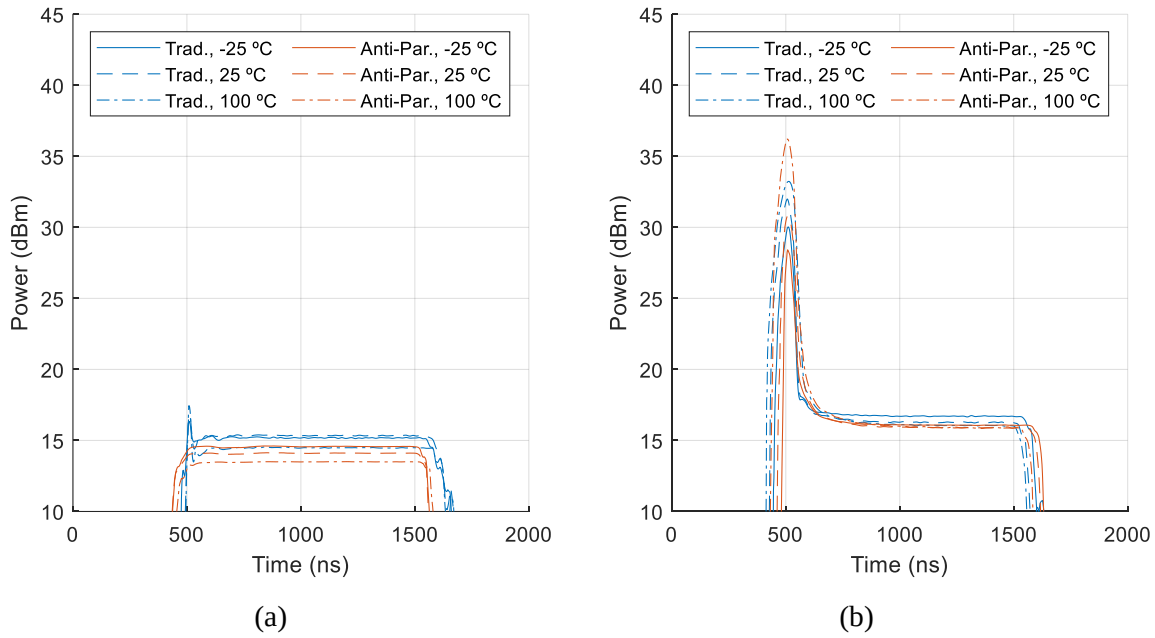
Table 5.16. Detector limiter comparison performance values at 25 ºC.

Frequency	**Spike leakage (nJ)**		**Flat leakage (dBm)**		**Recovery time (ns)**	
	Custom	Typical	Custom	Typical	Custom	Typical
1000 MHz	0.32	1.94	3.05	1.07	78	27
2000 MHz	1.06	0.33	8.13	11.79	69	46

At the coupler's optimal frequency, the use of both the ports does improve the performance compared to the typical design. It should also be mentioned that, even though the spike leakage is more at 2000 MHz, the magnitude of the spike is comparable to the flat leakage of the typical design. Both designs show similar recovery times.

5.8.5 Topology comparison

Figure 5.42 shows a comparison of the traditional and anti-parallel limiter topologies at 100 MHz at different temperatures for the CLA4608 (Figure 5.42(a)) and CLA4609 (Figure 5.42(b)) PIN diode. The CLA4609 PIN diode is included for comparison because it was seen in Table 5.5 and Table 5.9 that its spike leakage is considerably higher compared to the other diodes because of its size. The detector limiter is not evaluated at VHF given its frequency dependent design.



(a) (b)

Figure 5.42. Limiter topology response comparison versus temperature at 100 MHz. (a) CLA4608 PIN diode. (b) CLA4609 PIN diode.

At this low frequency, with the CLA4608 diode, the traditional limiter is outperformed by the anti-parallel limiter which does not show any spike leakage and has the least flat leakage. For the CLA4609 diode, both topologies show a clear increase in spike leakage and decrease in flat leakage (increase in attenuation) with increasing temperature at this frequency. The anti-parallel limiter has a lower flat leakage across all temperatures and less spike leakage at lower temperatures, but more spike leakage at 100 ºC. However, the traditional limiter has a much smaller increase in the magnitude of the spike leakage between -25 ºC and 100 ºC at 3.2 dB compared to 7.9 dB of the anti-parallel limiter. Considering the non-linear performance of these

two limiter topologies that was shown in Figure 5.19, it is evident that the anti-parallel topology provides better performance than the traditional topology for both PIN diodes at this frequency and temperature range.

Figure 5.43 shows a comparison of the traditional and anti-parallel limiter topologies at 300 MHz. The CLA4609 diode was not included for comparison at this frequency since it did not show any increase in spike leakage compared to the CLA4608 diode for either limiter topology. The traditional limiter has the worst flat leakage at 15.36 dBm at -25 ºC, and the most spike leakage of 0.6607 nJ at 25 ºC. Both limiter topologies have ringing before reaching flat leakage, with the anti-parallel limiter considered the most severe of the two, especially at -25 ºC. The results, including the temperature response, agree with the non-linear response that was shown in Figure 5.20, where the anti-parallel topology showed better attenuation than the traditional limiter for input levels higher than roughly 13 dBm.

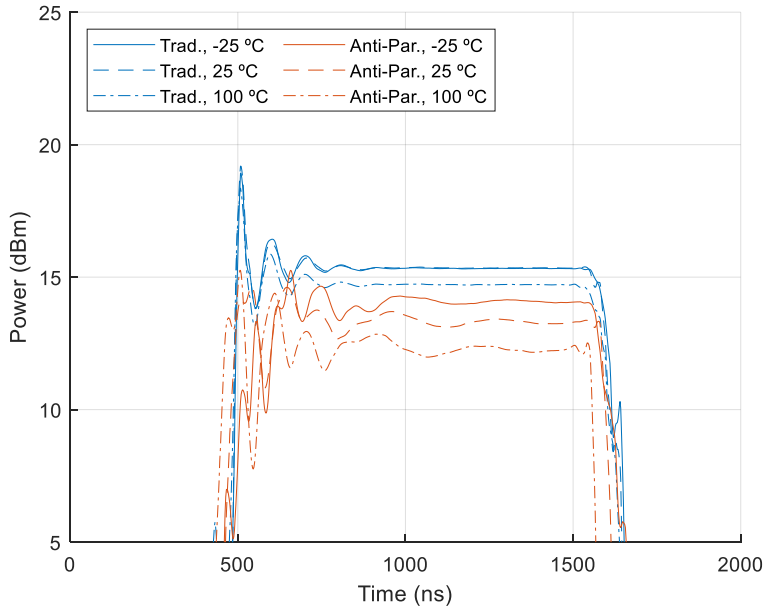


Figure 5.43. Limiter topology response comparison versus temperature at 300 MHz.

The limiter topology response comparison at 2000 MHz is shown in Figure 5.44. The CLA4609 diode is again included (Figure 5.44(b)) because of its increased spike leakage in the detector limiter topology compared to the other diodes that was seen in Table 5.13.

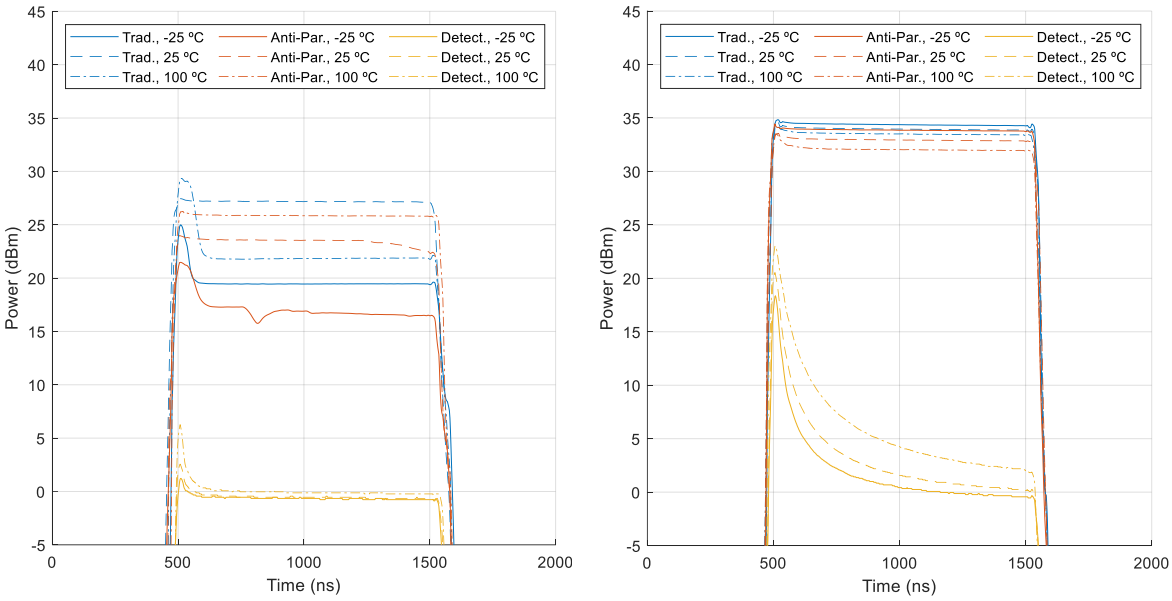


Figure 5.44. Limiter topology response comparison versus temperature at 2000 MHz. (a) CLA4608 PIN diode. (b) CLA4609 PIN diode.

For the CLA4608 diode, shown in Figure 5.44(a), at this frequency, the detector limiter has the best performance by far in terms of both spike (0.0095 nJ at -25 ºC) and flat leakage (-0.65 dBm at 25 ºC) compared to the traditional and anti-parallel limiters. The anti-parallel limiter again performs better than the traditional limiter, showing less spike (1.18 nJ vs. 23.23 nJ maximum at 100 ºC) and flat leakage (23.54 dBm vs. 27.16 dBm maximum at 25 ºC) at all temperatures.

For a thick diode such as the CLA4609 shown in Figure 5.44(b), the detector limiter exhibits a lot more spike leakage (compared to the CLA4608) but does not reach the spike or flat leakage level of either the traditional or anti-parallel limiter, who both shows poor performance at this frequency. The comparison clearly shows that the spike and flat leakage of the detector topology increases with increasing temperature, which is inverse from the response shown by the traditional and anti-parallel limiters. However, for the CLA4608 diode, both the traditional and anti-parallel limiters show an increase in spike and flat leakage with temperature, which was also observed in their non-linear response shown in Figure 5.21, but is the opposite to what was noted for VHF (and the CLA4609 response). It is also clear that neither the traditional nor the anti-parallel limiter offer substantial limiting at 2000 MHz, regardless of the PIN diode.

5.9 CONCLUSION

The different limiter topologies were shown on the PCB test jig along with the designed bi-directional coupler. The coupler's measurement response is in good agreement with the simulated design and any variation in the response is due to tolerances in the manufacturing process or differences in the RF laminate.

The measured non-linear results for the traditional limiter at both 1000 MHz and 2000 MHz show good agreement to the manufacturer's data [71], which shows a kink at 24 dBm and 18 dBm input and output power, respectively, at 1000 MHz, and at 34 dBm and 29 dBm input and output power, respectively, at 2000 MHz. This proved that the measurement methodology is accurate. No other frequency or topology could be compared to manufacturer provided data since it is not provided by the diode manufacturer.

The non-linear response of the traditional and anti-parallel limiter topologies shown in Figure 5.19 and Figure 5.20 for 100 MHz and 300 MHz, respectively, both showed that the attenuation of the limiter increases with an increase in temperature at VHF. This result was also found in [19], where it was reported that large capacitance diodes tend toward a negative resistance coefficient, which indicates that shunt limiters will exhibit increased attenuation levels with temperature. It was concluded in the previous section that the measured PIN diodes have a carrier lifetime temperature coefficient, $\tau_{\text{coefficient}}$, of greater than 2.3, which indicates a negative resistance coefficient.

The traditional and anti-parallel topologies' non-linear response at 2000 MHz, shown in Figure 5.21, indicates an inverse temperature response to VHF and shows that the attenuation level of the limiter decreases with an increase in temperature. The detector limiter also shows this inverse response and exhibits a decrease in attenuation level with increasing temperature for an input power level higher than 30 dBm. At this frequency, the detector limiter outperforms the traditional and anti-parallel topologies, which was expected. Figure 5.16 showed that the

detector limiter seems more accommodating towards thicker diodes because of its biasing method.

It was shown in Figure 5.6 that a limiter's non-linear response showed no difference in attenuation as a function of capacitance but did show an increase in attenuation for decreasing series resistance. It was also shown in Figure 4.15 that the measured PIN diodes have a decreasing series resistance with increasing temperature. Therefore, it can be concluded that the increase in attenuation because of an increase in temperature observed in the non-linear responses for the three limiter topologies are due to the decrease in their series resistance, and not because of the change in capacitance. Furthermore, at 100 MHz and 300 MHz, the anti-parallel configuration showed the best performance, with the least losses and most attenuation. Therefore, at VHF, the anti-parallel limiter topology has the best performance in terms of attenuation and losses.

The simulated non-linear response showed reasonable agreement to the measured data at low input power levels (< 10 dBm). However, the simulations did not accurately depict the measured response for higher input power levels and temperature responses, which often showed substantial differences in attenuation. Considering that the stand-alone PINDRC model showed good agreement with the de-embedded PIN diode data in the previous section, the extracted parameters are not suspected to be the cause for the poor simulation accuracy. The impeded simulation performance may be due to unmodelled parasitic elements, substrate coupling around the active components, or other circuit effects which are not evident in a linear or slow-varying nonlinear model. In some cases, like the traditional limiter's response at frequencies below 2000 MHz, the simulated response is nearly identical to the measured response. More complex circuit layouts like the anti-parallel and detector limiter seems difficult to simulate with the PINDRC model.

The input transient signals that are shown in Figure 5.22 were used to configure the RF pulse generator in AWR. The pulse was then used to simulate the transient response of the different limiter topologies. The simulated transient responses showed results that exhibited similar

trends to measured responses, even though the values could, in most cases, not directly be compared. The simulation also struggled to accurately model the spike leakage of the limiter topologies, likely due to the unmodelled parasitic elements discussed above. The simulation also struggled with the temperature response of the limiters, often wildly over-predicting the temperature dependency of the flat leakage. The simulated responses did show a decrease in the amount of spike and flat leakage with increasing temperature which, as discussed, is indicative of an increase in attenuation. Due to the problematic envelope fitting of the simulated response, confidently calculating the recovery time of the limiter was also difficult.

The measured transient results showed that the flat leakage decreases as the temperature increases for the traditional and anti-parallel limiter topologies operating at VHF. The limiter topologies also exhibited an increase in spike leakage with temperature from -25 ºC to 100 ºC. The detector limiter showed an increase in spike and flat leakage with increasing temperatures at 1000 MHz and 2000 MHz. The detector topology is the only limiter that showed an increase in flat leakage with increasing temperature. This could be due to either capacitance or resistance changes in the PIN diode itself, or because of degraded coupler performance due to small changes in the PCB dielectric constant or loss tangent due to temperature.

The increase in spike leakage was found to be more severe with the thicker CLA4609 PIN diode, which showed far greater spike leakage compared to the other diodes at 100 MHz and 2000 MHz, specifically. The reason for the more sever spike leakage is because of the CLA4609 and CLA4611 diode's increased carrier lifetime compared to the smaller diodes due to their thickness (20 µm and 12 µm, respectively, compared to 7 µm and 4.5 µm for CLA4608 and CLA4610 PIN diodes, respectively). As it was discussed in Section 2.2.1, the response time of the PIN diode is directly related to the diode's carrier lifetime, and the carrier lifetime is in turn influenced by temperature and the capacitance of the I-layer. This confirms the results found in other studies that reported that the thickness of the I-layer of the PIN diode has a direct impact on the magnitude and duration of the spike leakage [10], [25]. The CLA4609 PIN diode also exhibits the increase in spike leakage with increasing temperature to a larger extent than the thinner CLA4608 PIN diode. It was further found that, at VHF, the anti-parallel limiter

topology has the best performance in terms of spike and flat leakage, whereas the detector limiter showed superior performance at 2000 MHz.

Through simulation it was shown in Table 5.1 that an increase in the junction capacitance (with the series resistance kept constant) would decrease the spike leakage of a limiter but have a minimal effect on the flat leakage. However, the simulated results suggest the opposite to a study that found that diodes with a thin I-layer (less junction capacitance) have little spike leakage, and that thick I-layer diodes (more junction capacitance) have much more spike leakage [23]. The measured results would agree more with literature than the simulated results. Table 5.2 further showed that a decrease in the series resistance (with the junction capacitance kept constant) increases the spike leakage and decreases the flat leakage of a limiter.

The increase in spike leakage with increasing temperature can be attributed to the increase in the diode's carrier lifetime, which is influenced by temperature and the increase in capacitance of the I-layer. Therefore, since it was shown in Figure 4.7 and Figure 4.15 that the capacitance and resistance of the measured diodes increases and decreases with increasing temperature, respectively, it can be concluded that the increase in spike leakage and decrease in flat leakage with increasing temperature observed throughout this section and, more specifically in Figure 5.42(b) and Figure 5.44(b), is, at least partially, due to the increase in capacitance of the PIN diode, since it influences the carrier lifetime of the diode which governs the response time and, therefore, the spike leakage. This result would agree with the literature [10], [23], [25]. It is, however, evident that the performance of the limiter is dominated by the effect of the series resistance, which makes it difficult to accurately determine the effect of junction capacitance.

CHAPTER 6 CONCLUSION

6.1 CHAPTER OVERVIEW

This chapter concludes this research study by briefly summarising the results in Section 6.2 and presenting an analysis of the research hypothesis in Section 6.3. Section 6.4 proposes recommendations and suggestions for future work on this topic.

The objective of this study was to study the effect that device temperature variation has on the performance of a PIN diode limiter used in Electronic Warfare or military systems that operate in the VHF band, with a specific focus on the change in diode capacitance. By doing this the impact of temperature change on a PIN diode could be determined and its effect on the performance of certain limiter topologies analysed.

6.2 SUMMARY OF RESULTS

For this study, four different PIN diodes of different sizes were characterised at various temperatures and bias voltages and had their important parameter values de-embedded through the process of multi-bias parameter extraction. Parameters such as junction capacitance and resistance were then monitored across different domains.

The results that were presented in Chapter 4 showed that, for the measured PIN diodes, the reverse-biased junction capacitance, and reverse-biased series resistance both increase with temperature. It was further shown that the forward-biased series resistance of the diodes decreases with increasing temperatures. The de-embedded parameters were used to populate the non-linear PINDRC model in AWR. The model showed good agreement with the de-

embedded data during forward and reverse-biased simulations. For forward-biased measurements, R_3, shown in Figure 4.3, had to be omitted to enable the simulator to calculate the correct series resistance of the PIN diode. It was further found that the PINDRC model does not correctly apply changes in simulated temperature to the parameter values. As a result, all the simulated temperature measurements did not show any change in the respective parameter value, whereas the measured data did. This incorrect interpretation of simulation temperature was evident in Chapter 5 as well.

Chapter 5 presented the transient and continuous wave (CW) non-linear results of multiple PIN diode-based limiter topologies. It was shown through simulation in Figure 5.5(a) through Figure 5.5(c) that an increase in the junction capacitance (with the series resistance kept constant) decreases the spike leakage but has minimal influence on the flat leakage. This result agrees with Figure 5.6(a) which shows that the junction capacitance does not affect the non-linear response of the limiter. Figure 5.5 further showed that a decrease in the on-state series resistance (with the junction capacitance kept constant) increases the spike leakage and decreases the flat leakage of a limiter. This is supported by Figure 5.6(b) which shows that a decrease in series resistance (with the junction capacitance kept constant) decreases the flat leakage of a limiter and, therefore, increases attenuation.

The non-linear response of the traditional and anti-parallel limiter topologies both showed that the attenuation of the limiter increases with an increase in temperature for VHF, which agrees with the results found in [19]. The detector limiter topology showed an increase in attenuation at 1000 MHz and 2000 MHz for input power levels lower than 30 dBm, and a decrease in attenuation for input power levels higher than 30 dBm. It was concluded that the increase in attenuation because of an increase in temperature observed in the non-linear responses for the three limiter topologies are due to the decrease in their on-state series resistance, and not because of the change in capacitance.

The transient results showed that the flat leakage decreases (more attenuation) as the temperature increases for the traditional and anti-parallel limiter topologies operating in

VHF, with the spike leakage also showing an increase with increasing temperature. The detector limiter does not perform well at VHF but showed an increase in both the spike and flat leakage with increasing temperatures at 1000 MHz and 2000 MHz.

The increase in spike leakage was shown for thick (CLA4609) and thin (CLA4608) PIN diodes and was found to be more severe with the thicker CLA4609 PIN diode, which showed far greater spike leakage compared to the other diodes at 100 MHz and 2000 MHz, specifically. The thicker PIN diodes better exhibits the increase in spike leakage with increasing temperature due to their size, which confirms the results found in other studies that reported that the thickness of the I-layer of the PIN diode has a direct impact on the magnitude and duration of the spike leakage [10], [25]. This can be attributed to the increase in the diode's carrier lifetime which is influenced by temperature and the increase in capacitance of the I-layer with increasing temperature, as was shown in Figure 4.7. Considering the simulated results in Table 5.2, an increase in spike leakage and decrease in flat leakage would suggest that the increase in spike leakage could also be due the decrease in series resistance with temperature, as was shown in Figure 4.15.

Although Table 5.1 summarised that a simulated increase in junction capacitance will decrease the spike leakage of the limiter, a study reports diodes with a thin I-layer (small junction capacitance) have little spike leakage, and that thick I-layer diodes (more junction capacitance) have much more spike leakage [23], which agrees with the measured results. Therefore, it was concluded that the increase in spike leakage and decrease in flat leakage of the transient responses of the limiter topologies observed throughout Chapter 5 is, at least partially, due to the increase in capacitance of the PIN diode. However, the impact of the capacitance on the transient performance of the limiters is overshadowed by the effect of the series resistance.

It was also found that the simulated transient response greatly overestimated the effect of temperature on spike and flat leakage, adding to the incorrect interpretation of temperature

discussed previously, in addition to incorrectly simulating the effect of increasing capacitance on the spike leakage according to [23].

It was also concluded that for VHF, the anti-parallel limiter topology has the best transient and non-linear performance, whereas at 2000 MHz, the detector limiter topology showed superior performance due to its optimised bi-directional coupler.

6.3 EVALUATION OF HYPOTHESIS

The focus of this study was to investigate the effect that temperature variation has on the performance of a PIN diode limiter that is used in Electronic Warfare or military systems that operate in the VHF band because of a change in the diode's capacitance. The following research question was addressed:

- *What effect does temperature variation have on the capacitance of an RF PIN diode?*

It was found that the capacitance of the measured diodes increases with increasing temperatures, as was shown in Figure 4.7. Table 4.2 further showed that diodes with a largest I-layer thickness, like the CLA4609 diode (20 µm), exhibits less capacitance change over temperature as the diodes with a thinner I-layer thickness, as is suggested by (2.11).

Expanding on the primary research question, the following research questions were also addressed during this study:

- *What effect does the change in RF PIN diode capacitance have on the transient behaviour of an RF limiter?*

Although Table 5.1 summarised that a simulated increase in junction capacitance will decrease the spike leakage and increase the flat leakage of the limiter, the measured results contradicted this increase and decrease, respectively, and agrees more with a study which reports that diodes with a thin I-layer (less junction capacitance) have little spike leakage, and that thick I-layer diodes (more junction capacitance) have much more spike leakage [23]. The increase in spike leakage with increasing temperature can be attributed to the increase in the diode's carrier lifetime, which is influenced by temperature and the increase in

capacitance of the I-layer, which was shown in Figure 4.7. Therefore, it was concluded that the increase in spike leakage and decrease in flat leakage of the transient responses of the limiter topologies observed throughout Chapter 5 is, at least partially, due to the increase in capacitance of the PIN diode, since it influences the carrier lifetime of the diode which governs the response time and, therefore, the spike leakage. However, the impact of the capacitance on the transient performance of the limiters is overshadowed by the effect of the series resistance, for which a decrease with temperature, according to Table 5.2, greatly increases the spike leakage and decreases the flat leakage of the limiter.

- *What type of RF PIN diode-based limiter topology performs best in terms of transient behaviour under various temperature conditions, given change both in capacitance and resistance over temperature?*
- *What type of RF PIN diode-based limiter topology performs best in terms of steady- state behaviour under various temperature conditions?*

It was also concluded that for VHF, the anti-parallel limiter topology has the best transient and non-linear performance, whereas at 2000 MHz, the detector limiter topology showed superior performance due to its optimised bi-directional coupler.

To answer the primary research question, the following hypothesis was formulated:

'*An increase in the device temperature of a PIN diode will increase the capacitance of the PIN diode. Because of the increased capacitance, the carrier lifetime of the diode will also increase which will increase the response time of the limiter and, therefore, increase the spike leakage.*'

It was found that the capacitance of the measured diodes does increase with increasing temperatures, as was shown in Figure 4.7, agreeing with (2.10) that suggests that the carrier lifetime increases with increasing temperature, since the carrier lifetime is in turn influenced the capacitance of the I-layer of the diode. It was further found that the spike leakage increases in all the proposed limiter topologies with increased temperature and, more prominently, when using thick PIN diodes, therefore validating the hypothesis.

6.4 FUTURE WORK

Because most of the parameters required by the PINDRC model are not available from the manufacturer's datasheet, using third-party software models, like those provided by Modelithics, for the PIN diodes could improve the accuracy of the simulations. This will limit the options for choice of diode to what is provided by third-party suppliers but can greatly assist with the verification of and comparison between the measured data.

By either increasing the frequency band of interest or physical size of the test jig, the TRL calibration technique can be implemented and used for the purpose of de-embedding. The TRM calibration relies on a precise and predictable load standard that, if the assumption of a non-reflecting match standard is not fulfilled, can introduce extra residual errors into the calibration, which degrades the measurement accuracy. The TRL calibration standard is the most accurate method since it has the least requirement for precise calibration standards and lumped models. Using the TRL calibration technique might improve the accuracy of the parameter extraction.

The limiter-based measurements, both non-linear and transient, can be repeated using a bidirectional coupler with higher directivity. This could improve the measurements of the detector-based limiter. The discrete custom limiters presented in this study can be implemented on MMIC and their performance measured and compared.

The frequency range of interest (VHF) could also be extended or moved to include X-band frequencies (8 – 12 GHz) or even 2 – 18 GHz. X-band frequencies are another common military band and are used in modern radar systems and for air traffic control and defence tracking applications. The 2 – 18 GHz band is popular for electronic warfare receiver systems.

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