Hindawi
International Transactions on Electrical Energy Systems
Volume 2023, Article ID 3945160, 12 pages
https://doi.org/10.1155/2023/3945160

*Research Article*

# A Single DC Source Generalized Switched Capacitors Multilevel Inverter with Minimal Component Count

**Kasinath Jena,[1] Dhananjay Kumar,[2] B. Hemanth Kumar,[3] K. Janardhan,[3] Arvind R. Singh,[4] Raj Naidoo,[4] and Ramesh C. Bansal[4,5]**

[1]*Department of Electrical and Electronic Engineering, Arka Jain University, Gamharia, Jharkhand, India*
[2]*Department of Industrial Research Design and Development (IRDD), Aartech Solonics Ltd, Mandideep, Madhya Pradesh, India*
[3]*Department of EEE, Mohan Babu University (Formerly Known As Sree Vidyanikethan Engineering College), Tirupati, India*
[4]*Department of Electrical, Electronic and Computer Engineering, University of Pretoria, Pretoria, South Africa*
[5]*Department of Electrical Engineering, University of Sharjah, Sharjah, UAE*

Correspondence should be addressed to Arvind R. Singh; u17410411@tuks.co.za

Received 11 March 2023; Revised 9 May 2023; Accepted 23 May 2023; Published 3 June 2023

Academic Editor: Mahdiyeh Eslami



This paper presents a new single-source switched capacitor- (SC-) based multilevel inverter (MLI) design with a boosting potential of three times the supply voltage. To produce a waveform with seven output voltage levels, the suggested switching capacitor inverter consists of eight switches, single diode, and two capacitors. Because capacitors are inherently balanced, there is no need for a balancing circuit or sensor. The structure can be expanded using the provided generalized equations. In addition, the technique for switching control and loss analyses is explored. A fair comparison with the most recent SCMLI topologies has been conducted to demonstrate the merits of the proposed work. Furthermore, the proposed topology is evaluated using the MATLAB/SIMULINK tool, and experiments under both transient and steady-state situations are performed to demonstrate its feasibility. At dynamic-loaded situations, the performance of the proposed SCMLI with dynamic modulation index and switching frequency is tested.

## 1. Introduction

The multilevel inverter is becoming more popular in industrial and academic applications because of its enhanced power quality, efficiency, low losses, and total harmonic distortion (THD). The use of MLIs provides significant benefits in the fields of medium- and high-voltage applications [1, 2]. In comparison to conventional inverters, it has a better power handling capacity and a higher degree of modularity, and it requires a relatively smaller amount of filtering. Because of its flexible design, MLI can be used in many different fields of electrical engineering. Generally, there are three types of conventional MLIs such as flying capacitor (FC) MLI, diode-clamped (DC) MLI, and Cascaded H-bridge (CHB) MLI. They enclose some disadvantages in terms of voltage stress, the number of active-passive components, a capacitor's voltage maintaining its own self-balancing voltage, and voltage gain.

For example, DC MLI and FC MLIs have difficulties with capacitor voltage balancing and need multiple switching components for a multilevel voltage generation. The cascaded H-bridge MLI is one such device that receives extensive use in renewable energy integration system (REIS). The CHB MLI is one of the most popular topologies in the literature because of its simple and extensible design [3].

Numerous isolated sources (DC) are used in the MLI topologies proposed in [4–6]. As a result, it preserves to be used in either as asymmetrical or a symmetrical configuration. All of these MLI topologies feature a modular design, making it simple to add more basic cells or subcells to increase the output voltage. But each of these topologies requires a much higher amount of isolated DC sources at input and power components, which fallout in an increase in size. This, in turn, causes the circuit to be cumbersome and expensive. The problem is caused by the fact that there are several DC sources available. However, these are excellent

for locations that have access to a variety of input sources, such as renewable forms of energy. The output voltages are generated by a novel MLI topology in which voltage sources are connected in a series-parallel configuration. H-bridge makes it simple to combine numerous DC sources into a renewable energy system [7, 8].

The switched capacitor SC topologies in recent years have a great interest in the research field because of some excellent features such as (i) boosting the ability of the input voltage, (ii) multiple DC voltage sources can be replaced by capacitors, and (iii) inherent self-balancing property of capacitors. These factors reduced the weight, size, and costs. The series-parallel combination of the DC source and capacitor of the multilevel inverter has good modular structure features and capacitor voltage balancing without any external balancing circuit presented in [9–11]. Multiple sources advocated in [12, 13] have back-end H-bridge. Due to the fact that it comprises various sources, it becomes complicated and expensive. The authors in references [13–19] further describe an active NPC capacitor inverter in the midst of a similar principle with a voltage-boosting capability of $1.5V_{DC}$. The topology described in [20, 21] has a modular SC structure with a minimum number of switching components. Another generalized structure of the SC technique reduces the total standing voltage for generating seven voltage levels, but switching components is increased [22–26]. The topology proposed in [22] reduced the blocking voltage, i.e., the voltage stress is within the supply voltage but larger numbers of passive and active components are used. A cross-switched triple gain SC topology is presented in [27–29]. However, this topology suffers several drawbacks, such as it includes a larger number of switching components and higher discharging time compared to the charging time of capacitors. The preceding paragraphs inspire the development of a novel generalized SC-based topology with less active and passive components, boosting capability, and self-balancing capability.

In light of these concerns, this study proposes a unique compact SC inverter with the following noteworthy characteristics:

(a) The capacitors are self-balancing.

(b) Power supply voltage-boosting capabilities (i.e., three times the supply voltage).

(c) Less than 50% of switches operate for any level of voltage.

(d) Each fundamental cycle has an identical number of repetitions for both charging and discharging.

(e) The smallest possible number of switching components.

(f) The switching components are subjected to less voltage stress.

(g) The generalized structure of SCMLI is easily achievable.

The enduring sections of the article are structured as follows: Section 2 includes a description of the suggested topology, the operational principle of different states, the finding of the most optimal capacitance values, the inherent-balancing capability of capacitors, and the modulation scheme. Loss analysis of the SCMLI topology is presented in Section 3. Section 4 discusses the generalized structure. Section 5 discusses the simulation process as well as the interpretation of experimental results. The relative analysis is introduced in Section 6 to confirm the significance of the structural design. Discussion on findings and applicability are also presented. Finally, Section 7 concludes with the highlights of the suggested topology.

## 2. Proposed Seven-Level SC-MLI Topology

Figure 1 illustrates the suggested seven-level SC MLI topology's structural design. It is composed of two floating capacitors $C_2$ and $C_1$, a power diode $D$, and a direct current source $V_{DC}$. Two distinct types of eight-power semiconductor switch $S_x\,(x = 1, 2 \ldots 8)$ are described, as depicted in Figure 1. (a) IGBTs by antiparallel diode and (b) IGBTs not including antiparallel diode are considered. A threefold voltage-boosting capability is provided by the proposed topology $(0, \pm 1V_{DC}, \pm 2V_{DC}, \pm 3V_{DC})$. The capacitors, $C_1$ and $C_2$, are inherently self-balanced. It has four pairs of complementary switches (i.e., $S_1S_2.S_3S_4, S_5S_6, S_7S_8$) to evade the short circuit. The charging path of the capacitors and load is indicated by dotted red and black lines. Table 1 explains the conceptual topology's valid switching states. The "OFF" and "ON" states of the switches are represented by "0" and "1." Table 2 summarizes the stresses on the switches.

*2.1. Working Principle.* The operating concept of the suggested MLI is demonstrated with the help of the following states listed in Table 1 and the analogous circuit design illustrated in Figure 2.

(i) State-1 (output voltage $v_0 = 0$): This voltage level can be achieved in two ways, i.e., the switches $S_1$, $S_4$, and $S_7$ (or $S_2, S_4, S_8$) are ON. In both ways, capacitors $C_1$ are brought in parallel with the DC source and charged up to a voltage equivalent to 1 $V_{DC}$. The equivalent circuit representations intended for zero voltage level are displayed in Figures 2(a) and 2(b).

(ii) State-2 (output voltage $v_0 = 1V_{DC}$): In this state of operation, the switches $S_2, S_4$, and $S_7$ are activated simultaneously to achieve the output voltage $v_0 1V_{DC}$. During this state, the capacitors $C_1$ are charged to $1V_{DC}$. Figure 2(c) depicts the equivalent state of $V_{DC}$ voltage level.

(iii) State-3 (output voltage $v_0 = 2V_{DC}$): In this state of operation, the switches $S_2, S_3, S_6$, and $S_7$ are activated simultaneously to achieve this voltage $v_0 = 2V_{DC}$ level at the output. During this state, capacitor $C_2$ charges to $2V_{DC}$. The corresponding circuit of this state is presented in Figure 2(d).

(iv) State-4 (output voltage $v_0 = 3V_{DC}$): To obtain this output voltage level $v_0 = 3V_{DC}$, the switches $S_2, S_5, S_5$, are switched on simultaneously. During

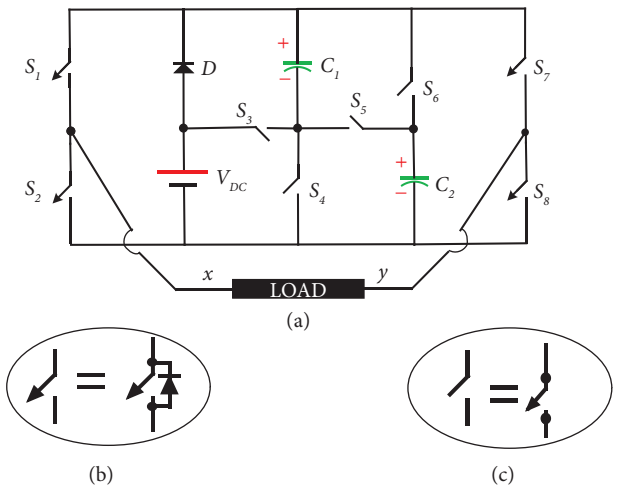


Figure 1: (a) The suggested seven-level SC inverter's structure. (b) IGBTs with antiparallel diode. (c) IGBTs without antiparallel diode.

Table 1: Proposed topology switching states.

| States | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | Output voltage |
|---|---|---|---|---|---|---|---|---|---|
| (i) | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| (ii) | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | $+1V_{DC}$ |
| (iii) | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | $+2V_{DC}$ |
| (iv) | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | $+3V_{DC}$ |
| (v) | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | $-1V_{DC}$ |
| (vi) | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $-2V_{DC}$ |
| (vii) | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | $-3V_{DC}$ |

Table 2: Voltage stresses of the switching components.

| Switching components | Voltage stress ($\times V_{DC}$) |
|---|---|
| $S_1, S_2, S_7, S_8$ | 3 |
| $S_3, S_5, S_6$ | 1 |
| $S_4$ | 2 |

this mode of operation, the capacitors, $C_1$ and $C_2$, discharge their stored energies to the load. Figure 2(e) shows the corresponding circuit diagram of this state.

(v) State-5 (output voltage $v_0 = -1V_{DC}$): To achieve the desired output load voltage, switches $S_1$,$S_4$, and $S_8$ are all turned on simultaneously. The capacitor $C_1$ is charged to $1V_{DC}$. Figure 2(f) shows the corresponding circuit diagram of this state.

(vi) State-6 (output voltage $v_0 = -2V_{DC}$): In this mode of operation, the output voltage $v_0 = -2V_{DC}$ can be achieved by activating the switches $S_1, S_3, S_4, S_8$ simultaneously. In this state capacitor, $C_2$ is charged to $2V_{DC}$. Figure 2(g) shows the corresponding circuit diagram of this state.

(vii) State-7 (output voltage $v_0 = -3V_{DC}$): In order to achieve the voltage level $v_0 = -3V_{DC}$ at the output terminal, the capacitors, $C_1$ and $C_2$, release their stored energy to the load. Figure 2(h) depicts the corresponding circuit diagram of this state.

*2.2. Design of Optimum Values of the Capacitor.* The capacitors get charged while they are connected in shunt fashion by way of an isolated DC voltage source ($V_{DC}$) and discharge their deposited energies to the output when connected with the supply source. The discharging values of capacitance are expressed as

$$\Delta Q_{c,i} = \int_{\theta_x}^{\theta_y} I_P \sin(\omega t - \varnothing) dt, \tag{1}$$

where $\theta_x$ and $\theta_y$ are the longest releasing time span, $I_P$ is the maximum load current values, and $\varnothing$ is the power factor angle.

The values of $\theta_x$ and $\theta_y$ can be measured as follows [26] from Figure 3(b):

$$\theta_1 = \frac{\sin^{-1} 1/3}{2 * \pi f}, \qquad \theta_2 = \frac{\sin^{-1} 1/3}{2\pi f}. \tag{2}$$

The optimal capacitance values are determined by the subsequent factors: (i) peak load current values, (ii) highest discharging period, and (iii) lowest voltage ripple ($\Delta V$) [17, 18]. As a result, the best possible capacitance values can be mentioned as

$$C_i \geq \frac{\Delta Q_{c,i}}{\Delta V_{c,i}}. \tag{3}$$

The maximum voltage spikes may be computed for pure resistive load

$$\Delta V_{c,1} = \frac{1}{\omega R C_1} \int_{\theta_1}^{\theta_2} V_{DC} dt + \frac{1}{\omega R C_1} \int_{\theta_2}^{\pi - \theta_2} 2V_{DC} dt, \tag{4}$$

$$\Delta V_{c,1} = \frac{V_{DC}}{\omega R C_1} [2\pi - \theta_1 - 2\theta_2], \tag{5}$$

$$\Delta V_{c,2} = \frac{1}{\omega R C_2} \int_{\theta_2}^{\pi - \theta_2} 2V_{DC} dt, \tag{6}$$

$$\Delta V_{c,2} = \frac{V_{DC}}{\omega R C_2} [2\pi - 4\theta_2]. \tag{7}$$

The details of self-balancing based on the parallel/series procedure of the switched capacitors as shown in Figure 2 make the capacitors self-balanced automatically [22].

*2.3. Modulation Strategy.* The suggested inverter is switched using a technique called phase disposition pulse with modulation (PDPWM). In this technique, a 50 Hz sine wave (u) is compared with eight constant signals (0+, 1/3, 2/3, 1, 0−, −1/3, −2/3, and −1), and the results are fed into a "AND" gate and a "Ex-OR" gate to yield the desired outputs

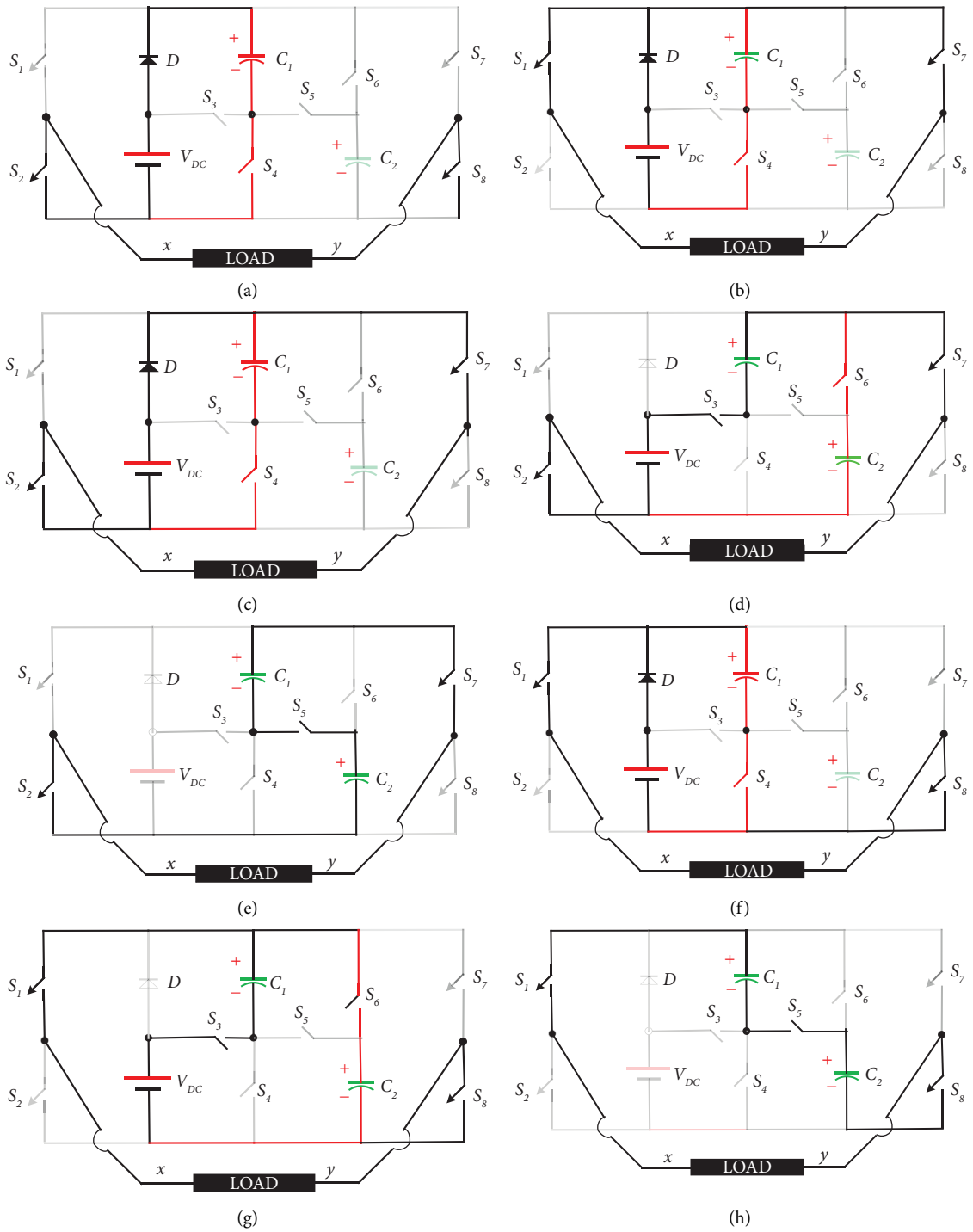


FIGURE 2: Equivalent circuit representation of different operating voltages. (a) $v_0 = 0$. (b) $v_0 = 0$. (c) $v_0 = 1V_{DC}$. (d) $v_0 = 2V_{DC}$. (e) $v_0 = 3V_{DC}$. (f) $v_0 = -1V_{DC}$. (g) $v_0 = -2V_{DC}$. (h) $v_0 = -3V_{DC}$.

$(P_1, P_2, P_3, P_{11}, P_{22}, \text{and } P_{44})$ as shown in Figure 3(a). In the second step, the sine wave is compared with six 1/3-height carrier signals $e_1, e_2, e_3, e_4, e_5$, and $e_6$ to produce the corresponding output signals $j_1$, $j_2$, $j_3$, $j_{11}$, $j_{22}$, and $j_{33}$, as shown in Figure 3(b) and graphically in Figure 3(c). Each of the signals $P_1, P_2, P_3, P_4, P_{11}, P_{22}, P_{33}$, and $P_{44}$, as well as their inverted counterparts, are fed into separate "AND" gates in the auxiliary circuit 2 of Figure 3(b), which in turn generate the corresponding outputs $x_1, y_1, x_2, y_2\, x_3, x_{11}, y_{11}\, x_{22}, y_{22}$ and $y_3$. Driving pulses for switches $S_1 - S_8$ can be generated

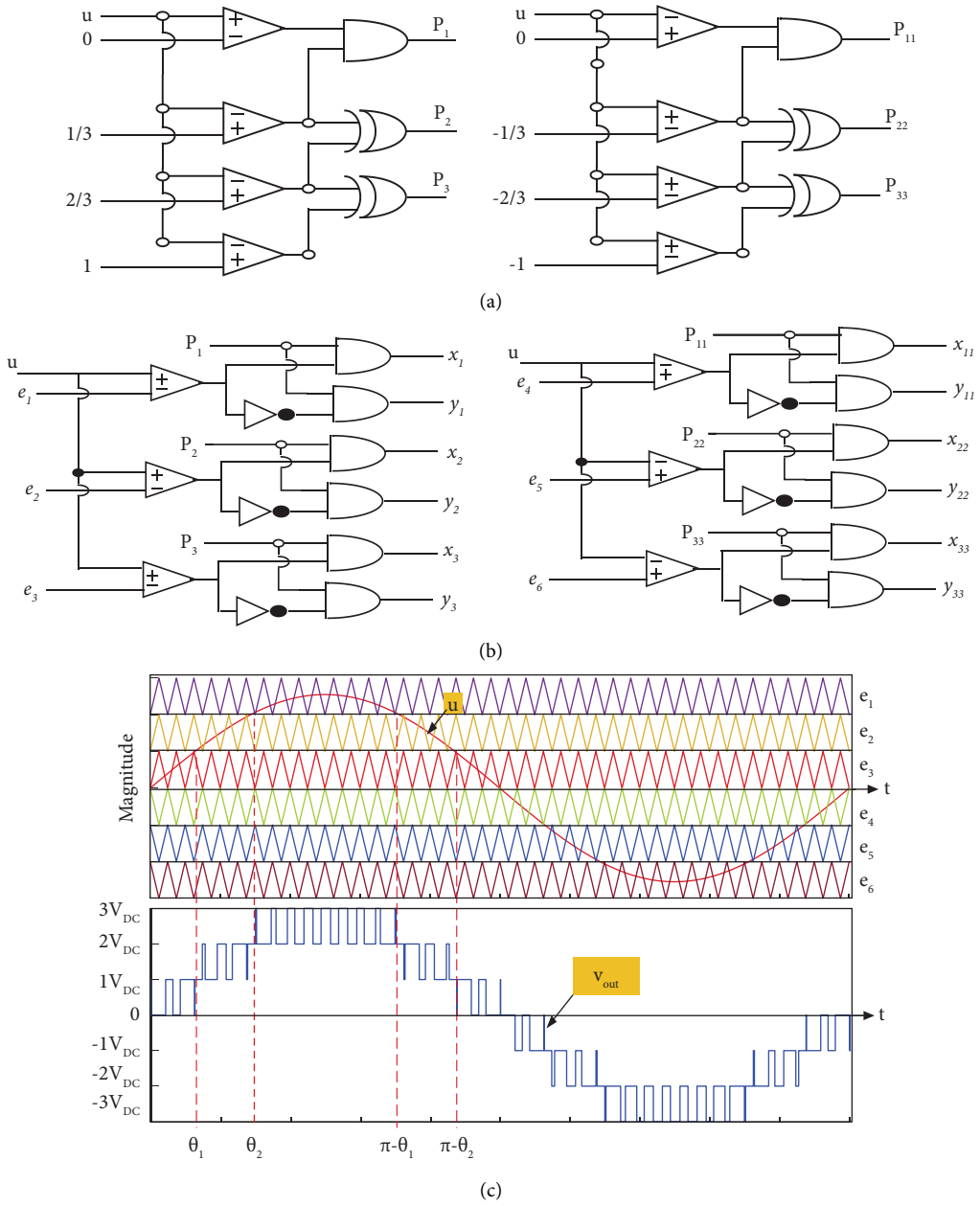


Figure 3: Control scheme: (a, b) simple logic-based switching scheme; (c) output voltage.

from the outputs of the auxiliary circuit 2 in Figure 3(b) using "OR" gates and the equations (8)–(14).

$$S_1 = x_{11} + y_{22} + x_{22} + y_{33} + x_{33}, \tag{8}$$

$$S_2 = y_{11} + x_1 + y_2 + x_2 + y_3 + x_3, \tag{9}$$

$$S_3 = x_2 + y_3 + y_{33} + x_{22} + y_3, \tag{10}$$

$$S_4 = y_1 + y_{11} + x_1 + y_2 + y_{22} + x_{11}, \tag{11}$$

$$S_5 = x_3 + x_{33}, \tag{12}$$

$$S_6 = x_2 + y_{33} + x_{22} + y_{33}, \tag{13}$$

$$S_7 = y_{11} + y_1 + x_1 + x_2 + y_2 + x_3, \tag{14}$$

$$S_8 = y_1 + y_1 + x_{11} + x_{22} + y_{22} + x_{33}. \quad (15)$$

## 3. Power Loss Analysis

This suggested topology has three sorts of losses. These losses are (a) conduction losses, (b) switching losses, and (c) ripple losses.

*3.1. Switching Losses ($P_{sw}$).* While switches are bowed ON and OFF, switching losses occur. The power losses in favour of every distinctive switch during ON and OFF are shown in Figure 4 [13].

Turn-ON power losses are

$$P_{on,sw} = \frac{1}{6} f_0 \left(V I_{on} t_{on}\right). \quad (16)$$

Turn-OFF power losses are

$$P_{off,sw} = \frac{1}{6} f_0 \left(V I_{off} t_{off}\right), \quad (17)$$

where $V$ is the voltage across the switches before and after activation. $I_{on}$ and $I_{off}$ are the current flowing through the switches once they are turned on. $t_{on}$ and $t_{off}$ are the switch's OFF and ON times. Thus, the proposed topology's total losses associated with switching ($P_{sw}$) is stated in

$$P_{sw} = \sum_{n=1}^{7} \sum_{m=1}^{8} \left(P_{on,sw,m} + P_{off,sw,m}\right), \quad (18)$$

where $n$ represents level count and $m$ represents switch count.

*3.2. Conduction Losses ($P_{con}$).* As a result of turning on the power switch, conduction losses are incurred. During the ON-state, the internal resistance of the power switch ($R_S$) and diode ($R_D$) wasted power.

In general, conduction losses are now the sum of the all switches and diodes power losses.

$$P_{con} = V_{s,on} I_{s,avg} + I_{s,rms}^2 R_{s,on} + V_{d,on} I_{d,avg} + I_{d,rms}^2 R_{d,on}, \quad (19)$$

where $V_{s,on}$ and $V_{d.on}$ are the ON-state voltage drop of the switch and diode, respectively.

$I_{d,rms}$, $I_{s,rms}$, and $I_{d,avg}$, $I_{S,avg}$ be the RMS and average current of the diode and switch, respectively.

So, the proposed SC-MLIs' overall power losses associated with conduction are given by

$$P_{con} = \sum_{i=1}^{k} \left( \sum_{j=1}^{n} \left(P_{con}\right) \right), \quad (20)$$

where $n$ and $k$ represent switch count and conduction paths, respectively.

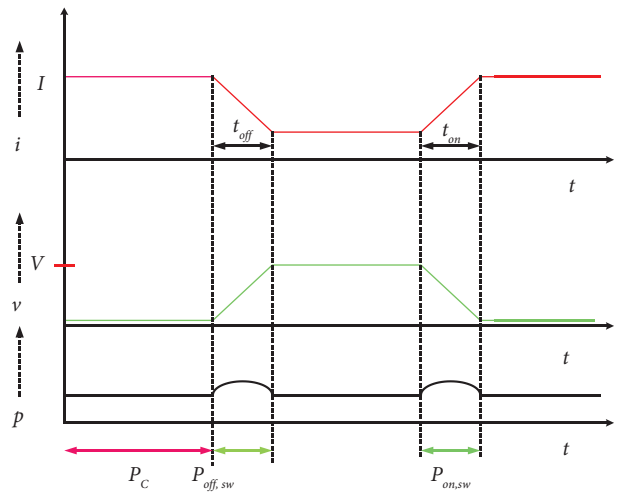


Figure 4: Typical switching turn-on/off.

*3.3. Ripple Losses ($P_R$).* The capacitor charges when a parallel connection is made between it and the power source. The capacitor's charging current creates ripple losses. So, the voltage ripple can be illustrated [25] from equations (5) and (7) as

$$\text{Ripple loss } (P_R) = \frac{f_0}{2} \sum_{i=1}^{2} \left(C_i \Delta V_{Ci}^2\right). \quad (21)$$

Therefore, the total power losses ($P_T$) are

$$P_T = P_{sw} + P_c + P_R. \quad (22)$$

## 4. Generalized Structure

Figure 1 shows a simple architecture that can easily be expanded to create a higher output voltage via simply adding SC cells or connecting them in series. By using a SC-based multilevel inverter, increasing the number of SC units increases the output voltage. Capacitors determine the maximum output voltage and serve as virtual sources. The 9-level output voltage is made achievable by including an additional SC unit in the suggested design. The generalised configuration of the proposed SCMLI topology for the expansion is depicted in Figures 5(a) and 5(b). The generalised arrangement of MLI with a SC unit is shown in Figure 5(a), and the generalised structure with a cascade tie is shown in Figure 5(b).

SCMLI's broad equation can be stated in terms of SCs. As a result, Table 3 lists the recommended SCMLI inverter switches, diode, and output level.

## 5. Comparative Assessment

The suggested SCMLI topology is compared to the seven-level SC topologies provided in Table 4 to assess its benefits. Among other criteria, the proposed architecture was assessed in provisos of maximum blocking voltage (MBV), gain, switch count per level, TSV, and cost function. The proposed and chosen topologies share

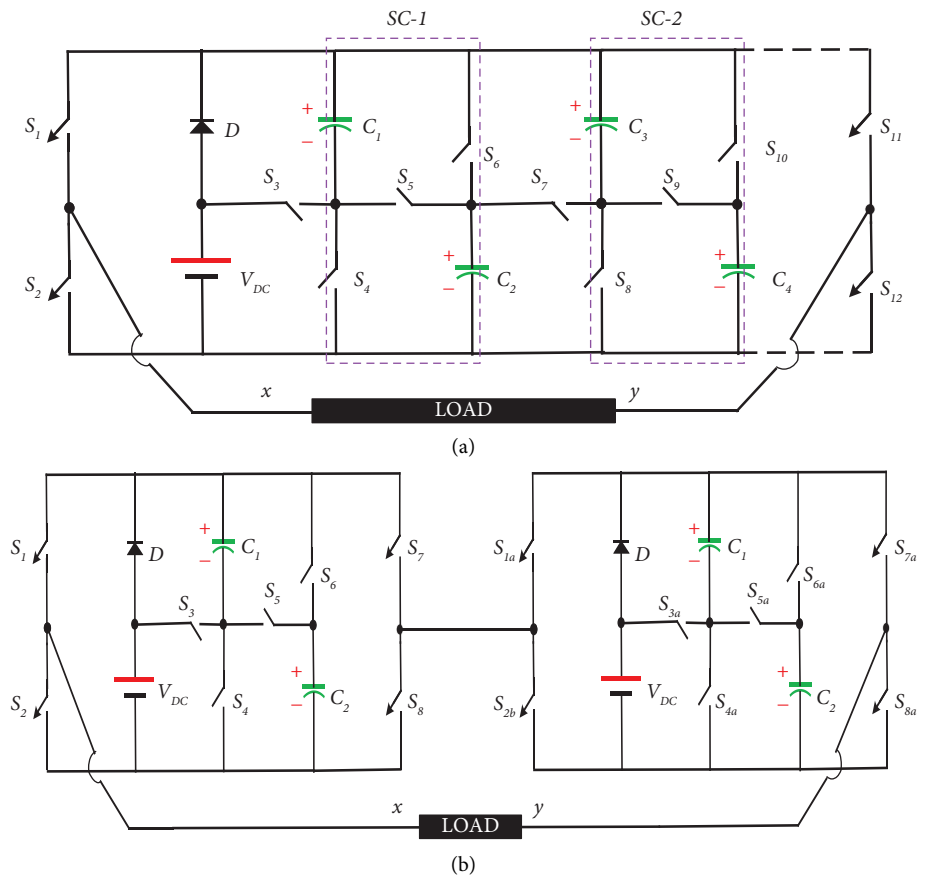


Figure 5: Generalized arrangement by (a) inserting SC unit and (b) cascade connection.

Table 3: Expressions used for the extension of SCMLI.

| Component | In terms of capacitor units ($n$) |
|---|---|
| Switch | $4n+4$ |
| Level | $2n+5$ |
| Capacitor | $2n$ |

a single-source and seven-level SC topologies. Furthermore, two parameters are evaluated to measure the cost-effectiveness of the structural design: component count per level and cost function. Switch count per voltage level ($F_{C/L}$) is defined as follows:

$$F_{C/L} = \frac{(N_S + N_{SW} + N_C + N_D)}{N_L}. \tag{23}$$

Cost function is defined as

$$CF = \frac{\left(N_{SW} + N_C + N_D + \alpha * TSV_{pu}\right) \times N_S}{N_L}. \tag{24}$$

The weight factor $\alpha$ will be near to unity and it completely depends on switching components' significance or the maximum load voltage. In the proposed architecture, this factor ($\alpha$) is "1", i.e., both switching components and $TSV_{pu}$ are equally important. As the name implies, $TSV_{pu}$ is the sum of all each switch voltage stresses divided by the maximum load voltage. These two factors ($F_{C/L}$, CF) decide the cost, size, and weight of the inverter. The proposed architecture is comprised of only 8 switches, one diode, and two capacitors in order to provide a 7-level output. It is noticed that the value of $F_{C/L}$ and CF of the anticipated topology is not as much as the recently proposed SCMLI topologies mentioned in Table 4 except the ones in [31, 32, 35]. However, the gain in [30–35] are less than the proposed one. This shows the said topology is associated with a smaller number of the driver unit, heat sinks, protection units, etc. Henceforth, the proposed converter's overall system cost, weight, and size are low among the state-of-the-art topologies. These features make the suggested topology more attractive and advanced. However, the topologies advocated in [16, 18, 22, 30–34] have a higher number of capacitor unit which means their stress and inrush current are very high, which degrades their reliability.

## 6. Results and Discussions

*6.1. Simulation Results.* A MATLAB/Simulink model of a seven-level SC inverter is constructed to test the viability of the proposed MLI. Table 5 displays the simulation parameters used in the analyses. The suggested inverter steady-state performance has been simulated under an R-L load (30 and 80 mH). Figure 6(a) depicts current and voltage waveforms.

Table 4: Comparative analysis with other seven-level existing SCMLI in literature.

| $A$ | [26] | [25] | [14] | [22] | [15] | [20] | [19] | [23] | [16] | [30] | [31] | [32] | [33] | [34] | [35] | ($P$) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $N_L$ | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 17 | 17 | 9 | 9 | 15 | 7 |
| $N_s$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 3 | 1 |
| $N_{sw}$ | 8 | 10 | 12 | 14 | 9 | 8 | 10 | 9 | 9 | 8 | 13 | 13 | 10 | 8 | 9 | 8 |
| $N_c$ | 2 | 2 | 2 | 2 | 3 | 2 | 4 | 2 | 3 | 3 | 4 | 4 | 4 | — | — | 2 |
| $N_D$ | 2 | — | — | — | — | 2 | — | 1 | — | 4 | 6 | 6 | 4 | 8 | 4 | 1 |
| B | 3 | 3 | 2 | 1 | 1 | 3 | 2 | 3 | 1 | 2 | 2 | 2 | 0.5 | 4 | 6 | 3 |
| G | 3 | 3 | 3 | 3 | 1.5 | 3 | 1.5 | 3 | 1.5 | 1.5 | 2 | 2 | 1 | 1 | 1 | 3 |
| C | 6 | 6 | 5.3 | 4.7 | 10 | 6 | 7.3 | 6 | 5.3 | 7.33 | 5.6 | 5.6 | 8.5 | 22 | 4.85 | 5.3 |
| $F_{C/L}$ | 1.8 | 1.8 | 2.2 | 5.6 | 1.8 | 1.8 | 2.1 | 1.8 | 1.8 | 2.28 | 1.41 | 1.41 | 2.11 | 2 | 1.06 | 1.7 |
| D | 2.6 | 2.6 | 2.7 | 2.9 | 3.2 | 2.6 | 3.1 | 2.6 | 2.5 | 3.19 | 1.68 | 1.68 | 2.95 | 8.44 | 3.57 | 2.3 |

$N_S$: number of sources, $N_L$: number of levels, $N_{SW}$: number of switches, $N_C$: number of capacitors, $N_D$: number of diodes, B: maximum blocking voltage, $F_{C/L}$: switching component per level, D: cost function (CF), A: parameter, $C$: per unit total standing voltage ($TSV_{pu}$), and G: gain, P: proposed topology.

Table 5: Simulations and experimental parameters.

| Parameter | Specification |
|---|---|
| Isolated DC source ($V_{DC}$) | 50 V |
| Output frequency (f) | 50 Hz |
| Switching frequency ($f_r$) | 200 Hz and 2 KHz |
| RL-load | $R = 30\,\Omega$, $L = 80$ mH |
| Capacitors $C_1$,$C_2$ | 1100 $\mu$F, 2200 $\mu$F |
| Modulation index (M) | 0.95 |
| IGBTs | FGW30XS65, FGW30XS65C |
| Diode | MBR20200CTG |
| dSPACE controller | RTI-1104 |
| Driver | TLP250 |

Each step's voltage is 50 V, and the highest output is 150 V. Due to the input source of 50 V, an increase gain of 3 is realized, which agrees with the theoretical notion.

The finding that the 2 capacitors are inherent-balancing with diminutive voltage ripples supports the investigation of balancing the capacitor voltage. The consequences of the rapid shift in load are shown in Figure 6(b). The findings show the inverter's ability to work across an extensive choice of loads, with a peak voltage of $3V_{DC}$ at a 7-level.

The proposed inverter can respond to variations in carrier wave frequency accurately. Figure 6 shows the voltage and current output vs. frequency (c). In all instances, it was discovered that the inverter exhibits a quick transient reaction (200 Hz to 2 kHz).The output voltage varies when the modulation index (M) amplitude varies, as seen in Figure 6(d). When $M$ lowers from 0.9 to 0.75 and subsequently to 0.2, the output voltage steps down from seven levels to five levels and then three levels, as shown in Figure 6(d). The speedy completion of the transient operations conveys the high transient performance of the proposed inverter. To investigate power losses, the proposed model was simulated using PLECS-based software, and the IGBTs datasheet was imported. The THD analysis of voltage and current is shown in Figures 6(e) and 6(f). Figure 6(g) depicts the power loss distribution for a purely resistive load. Overall, the proposed topology has an efficiency of around 96.2%.

*6.2. Experimental Results.* Experimentation with a research laboratory model is given here to authenticate the theoretical conclusions and reveal the viability of the suggested topology in both steady-state and dynamic circumstances.

The suggested inverter steady-state operation has been tested using an R–L load model (30 and 80 mH). Figure 7 depicts a voltage and current waveform (a). The maximum output is 150 V, with 50 V increments. With a 50 V input voltage, a boost gain of 3 is obtained, which is reliable through the theoretical expectation.

Figure 7 depicts the experimental waveform of the step change load's load voltage $v_o$, load current $i_o$, and voltage across the capacitors (b). When there is a sudden shift in load, the load voltage level remains constant. The waveform shows that when a step change in load is introduced, the voltage across the two capacitors is inherently balanced. Figure 7(c) also depicts experimental results for scenarios with a variable switching frequency (in this, i.e., 100 Hz and 5 kHz). It is vital to note that the output voltage level remains constant under these situations.

As seen in Figure 7(d), the output voltage varies as the modulation index amplitude changes. Furthermore, as seen in Figure 7(d), as $M$ falls from 0.9 to 0.5, then to 0.2, the quantity of output voltage steps lowers from seven to five, then to three. The maximum efficiency obtained from the experimental setup by the use of a power quality analyzer (Fluke 43B) is 97.16%. Finally, experimental results reveal that the proposed design performs adequately in both dynamic and steady-state circumstances.

*6.3. Discussions on Findings and Applicability.* The suggested design generates a seven-level waveform with three times the voltage gain, as shown by modelling and experimental results. It has been shown that the proposed topology reduces power loss in the switches. Based on a survey of the existing literature on SCMLIs, the following use cases have been identified for the proposed topology:

*6.3.1. High-Frequency AC Distribution.* Due to the significant reduction in the number of power conversion stages, the size of the transformer, and the size of the filter, a high-frequency alternating current (HFAC) power distribution system (PDS) has gained popularity in high-power density applications such as telecommunication [36, 37], spacecraft, and computer systems [38]. Another emerging field for HFAC PDS is its use in localised networks, such as

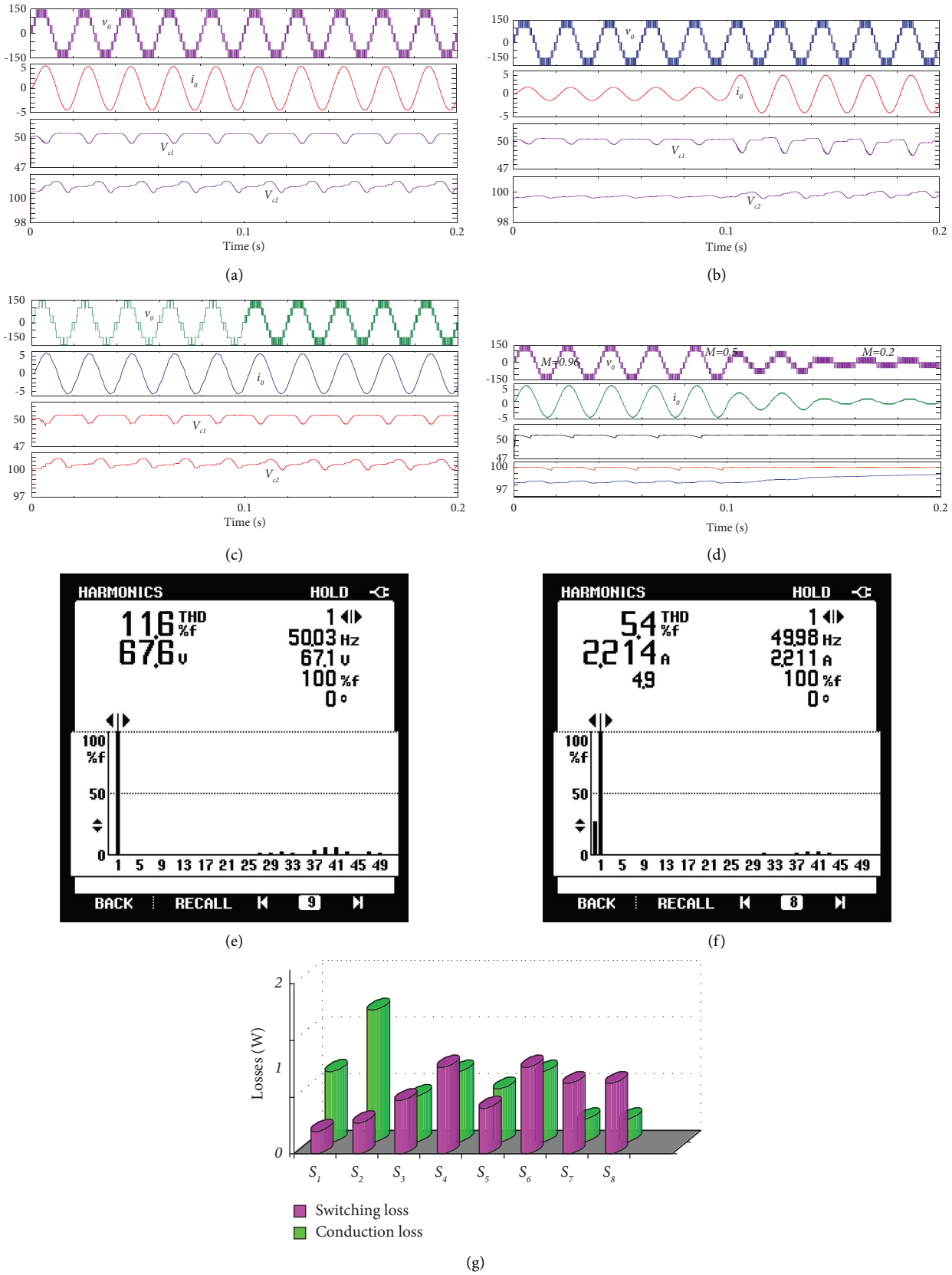


FIGURE 6: Simulation results: (a) wave of steady state, (b) step-in-load waveforms, (c) step-in-switching frequency waveforms, (d) waveform for modulation index steps of 0.95 to 0.5 and 0.5 to 0.2, (e, f) THD analysis of voltage and current, and (g) graphics of losses.

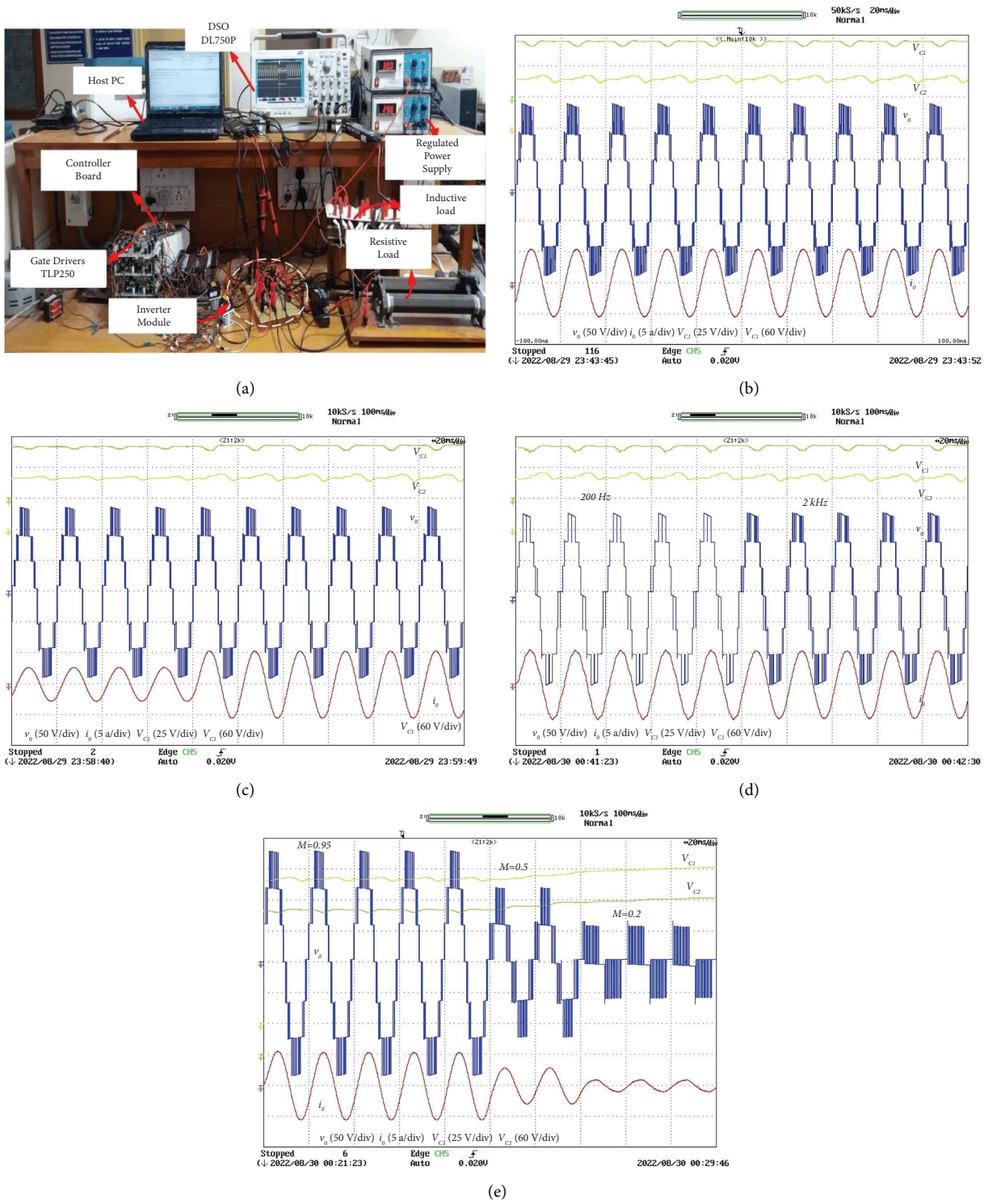


FIGURE 7: Laboratory results: (a) photograph of prototype, (b) steady-state profiles, (c) step-in-load waveforms, (d) step-in-switching frequency waveforms, and (e) waveform for modulation index steps of 0.95 to 0.5 and 0.5 to 0.2.

microgrids, buildings, and electric vehicles [39]. The use of magnetic circuits or dc-dc boost converters can be avoided in low voltage regions when SCMLI topologies are implemented.

*6.3.2. Photovoltaic- (PV-) Based Power Generation Systems and Electric Vehicle (EV) Traction System.* Renewable sources of energy, such as solar systems, have low power outputs. Cascading PV modules, a dc-dc boost inverter, or

a step-up transformer can all be used to increase the voltage. These methods raise the bar in terms of complexity, expense, footprint, and energy waste [40]. However, SCMLIs offer grid compatibility, a high-resolution waveform, reduced filtering needs, and increased voltage gain [41, 42]. Cascading the cells in EV systems is one way to get a high dc-link voltage, although charge balancing is a problem [43–45]. To circumvent these limitations of conventional EV drives, SCMLIs are being developed as a practical interface for converting low-voltage dc to high-voltage ac [45, 46].

## 7. Conclusion

This article describes a revolutionary SC-based boost-type seven-level inverter. The proposed SC-MLI topology's primary objective is to minimize switching components in order to achieve a high gain and with eight switching components and single isolated DC source seven levels are obtained in the output voltage profile. Additionally, the proposed converter output voltage is 3 times that of an input supply voltage, and capacitors are naturally self-balanced. The mathematical modelling of proposed topology is presented and validated with simulated results. Efficiency and loss investigation of the proposed MLI topology are presented and compared the same through the recent literature available on SC-MLI topologies. A brief comparative study has been carried out to check the superiority of other SC topologies in component count per level, MBV, and gain of the converter. This analytical comparison makes the proposed work more competitive and prominent. In the end, the experimental and simulated results for linear and nonlinear loads empower the findings of the study and reveal the practicality of the suggested design topology. Proposed SC-MLI topology performance was good at dynamic linear and nonlinear loads and with dynamic modulation index.

## Data Availability

No underlying data were used to support the findings of this study.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

## Acknowledgments

This work was supported by International Research: SA/China Joint Research Programme 2021, with Reference no. BCSA210303588702 and Unique Grant no. 148770.

## References

[1] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.

[2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—state of the art, challenges, and requirements in industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, 2010.

[3] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: a review," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135–151, 2016.

[4] M. Hosseinpour, A. Seifi, A. Dejamkhooy, and F. Sedaghati, "Switch count reduced structure for symmetric bi directional multilevel inverter based on switch diode source cells," *IET Power Electronics*, vol. 13, no. 8, pp. 1675–1686, 2020.

[5] D. J. Almakhles, J. S. M. Ali, S. Selvam, M. S. Bhaskar, and N. Sandeep, "Switched capacitor-based 13L inverter topology for high-frequency AC power distribution system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 5, pp. 5883–5894, 2021.

[6] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-Type) module: asymmetric multilevel inverters with reduced components," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7148–7156, 2016.

[7] R. Barzegarkhoo, H. M. Kojabadi, E. Zamiry, N. Vosoughi, and L. Chang, "Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple DC link producer with reduced number of switches," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5604–5617, 2016.

[8] K. P. Panda, P. R. Bana, and G. Panda, "A switched-capacitor self-balanced high-gain multilevel inverter employing a single DC source," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 3192–3196, 2020.

[9] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4614–4621, 2014.

[10] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 878–887, 2012.

[11] B. Hemanth Kumar, S. Prabhu, K. Janardhan, V. Arun, and S. Vivekanandan, "A switched capacitor based multilevel boost inverter for photovoltaic applications," *Journal of Circuits, Systems, and Computers*, vol. 32, no. 04, Article ID 2350057, 2023.

[12] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A step-up switched capacitor multilevel inverter with self-voltage balancing," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 12, pp. 6672–6680, 2014.

[13] S. R. Raman, K. W. E. Cheng, and Y. Ye, "Multi-input switched-capacitor multilevel inverter for high-frequency AC power distribution," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5937–5948, 2018.

[14] S. S. Lee, Y. Bak, S. M. Kim, A. Joseph, and K. B. Lee, "New family of boost switched-capacitor seven-level inverters (BSC7LI)," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 10471–10479, 2019.

[15] S. S. Lee, C. S. Lim, and K. B. Lee, "Novel active-neutral-point-clamped inverters with improved voltage-boosting capability," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5978–5986, 2020.

[16] B. Hemanth Kumar and M. M. Lokhande, "Investigation of switching sequences on a generalized SVPWM algorithm for multilevel inverters," *Journal of Circuits, Systems, and Computers*, vol. 28, no. 02, Article ID 1950036, 2019.

[17] J. Zeng, W. Lin, and J. Liu, "Switched-capacitor-based active-neutral-point-clamped seven-level inverter with natural

balance and boost ability," *IEEE Access*, vol. 7, pp. 126889–126896, 2019.

[18] S. S. Lee, "Hybrid 7-level boost active-neutral-point-clamped (H-7L-BANPC) inverter," *IEEE Transaction on Circuits and System II: Express Briefs (Early Access)*, vol. 67, no. 10, pp. 2044–2048, 2020.

[19] M. J. Sathik, N. Sandeep, and F. Blaabjerg, "High gain active neutral point clamped seven-level self-voltage balancing inverter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 11, pp. 2567–2571, 2020.

[20] Y. P. Siwakoti, A. Mahajan, D. J. Rogers, and F. Blaabjerg, "A novel seven-level active neutral-point-clamped converter with reduced active switching devices and DC-link voltage," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 10492–10508, 2019.

[21] B. H. Kumar and M. M. Lokhande, "An Enhanced Space Vector PWM for Nine-Level Inverter Employing Single Voltage Source," in *Proceedings of the 2017 IEEE Transportation Electrification Conference (ITEC-India)*, pp. 1–6, Pune, India, December 2017.

[22] S. S. Lee and K. B. Lee, "Dual-T-type seven-level boost active-neutral-point-clamped inverter," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6031–6035, 2019.

[23] W. Peng, Q. Ni, X. Qiu, and Y. Ye, "Seven-level inverter with self-balanced switched-capacitor and its cascaded extension," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 11889–11896, 2019.

[24] T. Roy, P. K. Sadhu, and A. Dasgupta, "Cross-switched multilevel inverter using novel switched capacitor converters," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 11, pp. 8521–8532, 2019.

[25] M. D. Siddique, S. Mekhilef, N. M. Shah, J. S. M. Ali, and F. Blaabjerg, "A new switched capacitor 7L inverter with triple voltage gain and low voltage stress," *IEEETrans:CirSyst: II Express Briefs*, vol. 66, no. 7, 2019.

[26] M. D. Siddique, J. S. M. Ali, S. Mekhilef, A. Mustafa, N. Sandeep, and D. Almakhles, "Reduce switch count based single source 7L boost inverter topology," *IEEE Trans:CirSyst: II Express Briefs*, vol. 67, no. 12, 2020.

[27] Y. Ye, W. Peng, and Y. Yi, "Analysis and optimal design of switched-capacitor seven-level inverter with hybrid PWM algorithm," *IEEE Transactions on Industrial Informatics*, vol. 16, no. 8, pp. 5276–5285, 2020.

[28] S. S. Lee, K. B. Lee, I. M. Alsofyani, Y. Bak, and J. F. Wong, "Improved switched-capacitor integrated multilevel inverter with a DC source string," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7368–7376, 2019.

[29] A. Taghvaie, J. Adabi, and M. Rezanejad, "A self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 199–209, 2018.

[30] A. Iqbal, M. D. Siddique, J. S. M. Ali, S. Mekhilef, and J. Lam, "A new eight switch seven level boost active neutral point clamped (8S-7L-BANPC) inverter," *IEEE Access*, vol. 8, pp. 203972–203981, 2020.

[31] S. Majumdar, K. C. Jana, P. K. Pal, A. Sangwongwanich, and F. Blaabjerg, "Design and implementation of a single-source 17-level inverter for a single-phase transformer-less grid-connected photovoltaic systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 4, pp. 4469–4485, 2022.

[32] S. Majumdar, B. Mahato, and K. C. Jana, "Analysis and implementation of a generalised switched capacitor multi level inverter having the lower total standing voltage," *IET Power Electronics*, vol. 13, no. 17, pp. 4031–4042, 2021.

[33] P. K. Pal, K. C. Jana, Y. P. Siwakoti, S. Majumdar, and F. Blaabjerg, "An active-neutral-point-clampedswitched-capacitor multilevel inverter with quasi-resonant capacitor charging," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14888–14901, 2022.

[34] S. Paul, K. C. Jana, S. Majumdar, P. K. Pal, and B. Mahato, "Performance analysis of a multimodule staircase (MM-STC)-Type multilevel inverter with reduced component count and improved efficiency," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 6619–6633, 2022.

[35] S. Majumdar, B. Mahato, and K. C. Jana, "Implementation of an optimum reduced components multicell multilevel inverter (MC-MLI) for lower standing voltage," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 4, pp. 2765–2775, April 2020.

[36] P. Jain, M. Pahlevaninezhad, S. Pan, and J. Drobnik, "A review of high-frequency power distribution systems: for space, telecommunication, and computer applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3852–3863, 2014.

[37] P. Jain and H. Pinheiro, "Hybrid high frequency AC power distribution architecture for telecommunication systems," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 35, no. 1, pp. 138–147, 1999.

[38] S. Luo and I. Batarseh, "A review of distributed power systems. Part II. High frequency AC distributed power systems," *IEEE Aerospace and Electronic Systems Magazine*, vol. 21, no. 6, pp. 5–14, 2006.

[39] S. Chakraborty, M. D. Weiss, and M. G. Simoes, "Distributed intelligent energy management system for a single-phase high-frequency AC microgrid," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 97–109, 2007.

[40] S. K. Kuncham, K. Annamalai, and N. Subrahmanyam, "A two-stage T-type hybrid five-level transformerless inverter for PV applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9510–9521, 2020.

[41] C. C. Antaloae, J. Marco, and N. D. Vaughan, "Feasibility of high-frequency alternating current power for motor auxiliary loads in vehicles," *IEEE Transactions on Vehicular Technology*, vol. 60, no. 2, pp. 390–405, 2011.

[42] S. Kouro, M. Malinowski, K. Gopakumar et al., "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, 2010.

[43] V. Gowri Shankar and C. Udhayashankar, "A new method for DC-AC conversion using simplified multilevel inverter - design and analysis using PSIM," in *Proceedings of the 2009 International Conference on Control, Automation, Communication and Energy Conservation*, pp. 1–7, Perundurai, India, May 2009.

[44] Y. C. Fong, S. R. Raman, Y. Ye, and K. W. E. Cheng, "Generalized topology of a hybrid switched- capacitor multilevel inverter for high- frequency AC power distribution," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2886–2897, 2020.

[45] J. O. Estima and A. J. Marques Cardoso, "Efficiency analysis of drive train topologies applied to electric/hybrid vehicles," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 3, pp. 1021–1031, 2012.

[46] B. Dong, Y. Li, and Y. Han, "Parallel architecture for battery charge equalization," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 4906–4913, 2015.