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ON-CHIP AND HYBRID LNA INTEGRATION AT MM-WAVE FREQUENCIES

by

Flavien Sagouo Minko

Submitted in partial fulfilment of the requirements for the degree
Philosophiae Doctor (Electronics)

in the

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Faculty of Engineering, Built Environment and Information Technology

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SUMMARY

ON-CHIP AND HYBRID LNA INTEGRATION AT MM-WAVE FREQUENCIES

by

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University:	University of Pretoria
Degree:	Philosophiae Doctor (Electronics)

Keywords:	Bipolar complementary metal oxide semiconductor (BiCMOS), Electromagnetic simulation, Electronic packages, Heterojunction bipolar transistors (HBT), Low-noise amplifier, Millimetre wave, Monolithic microwave integrated circuit (MMIC) design, Silicon germanium (SiGe), Total ionisation dose (TID).

This thesis presents a qualitative and quantitative comparison between an MMIC LNA packaged on PCB, and hybrid LNAs at V-band. This includes a quantitative study of the TID electron radiation on SiGe MMIC LNA at mm-wave as well as MMIC EM simulation protocol at mm-wave frequencies.

The MMIC LNA and the on-chip transistor were fabricated in the 130nm BiCMOS8HP process. The design configurations were adopted from literature for both the MMIC LNA and hybrid LNAs. The layout generated was subjected to RC parasitic extraction and 3D EM validation with both FEM and MoM. This was done to investigate the effect of on-chip parasitics on LNAs at mm-wave using SOTA methods, which confirmed the superior

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accuracy of the FEM approach but also revealed the value of RCPE for early design iterations.

The MMIC LNA was subjected to TID electron radiation, irradiated up to 15 Mrad/(Si) over 72 hrs. The device was measured for linear and noise figure performance over increasing total dose levels. It is found that the original gain of 14.84 dB and noise figure of 7.44 dB were degraded to 12.3 dB and 9.5 dB, respectively, with gradual degradation of gain, noise figure and operating bandwidth.

For the hybrid LNA, the on-chip transistors were bonded onto XT/Duroid 8100 soft substrate. The on-chip interconnection to the transistors, off-chip transmission lines and the interconnection to PCB were all modelled using 3D EM FEM. The resulting S-parameters were then used for circuit co-simulation. The MMIC LNA is mounted to PCB using flip-chip and wire-bond interconnects, while for the hybrid LNA, the transistors alone are mounted on the PCB using flip-chip and wire-bond, with the matching network off-chip. In addition, the RF coupling capacitors used coupled line bandpass filters also fabricated on PCB. These filters were then integrated as part of the matching networks. All off-chip passives were prototyped and characterized separately, including characterization of the substrate material itself.

The MMIC LNA had a simulated peak gain of 14.95 with NF of 7.66 dB, while each estimating an input 1 dB compression point of -15.6 dBm. The EM simulation revealed that insertion loss of less than 2.5 dB is expected for the on-chip transmission lines and flip-chip interconnects, while up to 6 dB can be expected for wire-bond transitions.

The MMIC LNA mounted on PCB by wire-bonding achieved a peak gain of 10.2 dB, with 12.2 dB expected when mounted by flip-chip bonding. In contrast, the hybrid LNA achieved 5.05 dB gain when integrating the transistors by wire-bonding and 10 dB when integrated using flip-chip bonding. This result is reflected in the NF as well, with the MMIC LNA achieving 7.66 dB NF in isolation, 9.74 dB when packaged on PCB using wire-bonds and 7.8 dB when packaged using flip-chip mounting. In contrast, the hybrid LNA using wire-bond integration achieves 10.4 dB of NF, while hybrid integration using flip-chip mounting

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achieves 7.9 dB. This data clearly illustrates the superiority of the MMIC LNA over its counterparts, despite a somewhat reduced -1 dB operating bandwidth.

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My grace is sufficient for you, for My strength is made perfect in weakness, 2 Corinthians 12:9. With that, I would like to give glory to my Lord Jesus Christ for the strength, wisdom, good health, and perseverance He has granted me throughout this research study.

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LIST OF ABBREVIATIONS

AED	Ansys Electronics Desktop
BEOL	Back-End-of-Line
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
BW	Bandwidth
CB	Common Base
CC	Common Collector
CD	Common Drain
CE	Common Emitter
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercially off-the-shelf
CPW	Co-Planar Waveguide
CS	Common Source
DK	Dielectric Constant
DRC	Design Rule Checking
DUT	Device Under Test
EM	Electromagnetic
ENIG	Electroless Nickel Immersion Gold
EPIG	Electroless Palladium Immersion Gold
ESCC	European Space Components Coordination
FEOL	Front-End-of-Line
FBW	Fractional Bandwidth
FEM	Finite Element Method
GFUS	GlobalFoundries United States
GSG	Ground Signal Ground
HB	Harmonic Balance
HBT	Heterojunction Bipolar Transistor
ISIG	Immersion Silver Immersion Gold

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ISS	Impedance Substrate Standard
LEO	Low Earth Orbit
LNA	Low Noise Amplifier
LVS	Layout Versus Schematic
MAG	Maximum Available Gain
MCM	Multi-Chip Module
MOM	Method of Moment
MMIC	Monolithic Microwave Integrated Circuit
MOS	Metal Oxide Semiconductor
NF	Noise Figure
PDK	Process Design Kit
PCB	Printed Circuit Board
QRC	Quantus RC
RCPE	Resistance and Capacitance Parasitic Extraction
SiGe	Silicon-Germanium
SOTA	State-of-the-art
TEC	Total Electron Content
TID	Total Ionizing Dose
VNA	Vector Network Analyser

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LIST OF VARIABLES

α	The total attenuation
α_C	The conduction attenuation
α_d	The dielectric attenuation
C_{pad}	The Pad capacitance
ENR	The error-to-noise ratio of the noise source
ε_r	The relative permittivity
F	The Noise factor
f_0	The Centre frequency
f_{max}	The Maximum oscillation frequency
f_T	The Transition frequency
G	The device Gain
IL	The insertion loss
k	The coupling coefficient
K	Rollet stability factor
L_E	Emitter degeneration inductance
L_g	The gate degeneration inductance
IP1dB	Input 1 dB compression point
OP1dB	Output 1dB compression point
Qu	The unloaded quality factor
r_b	The base resistance of a BJT
r_n	The noise resistance of the transistor
S_{opt}	The optimum reflection coefficient
Γ_L	The load reflection coefficient
Γ_S	The source reflection coefficient
μ	A unilateral stability criteria
Z_S	The Source impedance
Z_L	The Load impedance

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CHAPTER 1 INTRODUCTION

" The problem in this business is not to keep people from stealing your ideas; it is to make them steal your ideas". *- Howard Aiken*

1.1 INTRODUCTION

The last decade has seen increased efforts in measuring space weather effects, with solar flares being chief among these effects. The threats posed by solar flares range from short radio fadeout [1] to single event upsets [2], [3], and the triggering of magnetic storms [4]. These effects affect various ground-based and near-earth technologies. To mitigate damage associated with these effects, the scientific study of solar flare data is required to develop an effective service management plan. Such data could be obtained through the measurement of the energy spectrum of energetic particles during the impulsive phases of the flare [5] using mm-wave radiometry instruments. The present ground-based solar flare observatories (GBSFO) [6]–[9] suffer from various atmospheric and ionospheric variabilities as well as limitations in terms of the observation time due to the Earth's rotation [8]. These factors hinder the observation capacity of GBSFOs, resulting in discrepancies in their data. If these factors are to be mitigated by using a space-based system, new constraints would demand that the instrument be lightweight, compact, low-cost, preferably planar (especially for CubeSat integration), and resilient to ionizing radiation. System-on-chip (SoC) and system-in-package (SiP) system packaging satisfies the first two of these requirements. However, considering high parasitic loss at mm-wave frequencies in addition to limitations such as prototyping cost and long turnaround time [10]–[13], it is worth investigating for a better alternative. This project investigates the best integration (between a hybrid co-design of on-chip active and off-chip passives, versus full on-chip for mm-wave front-end technologies [14], [15]) and the best on-chip validation

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approach (between MoM, FEM and RC parasitic extraction) for mm-wave systems. To investigate these alternatives, emphasis is placed on mm-wave low noise amplifiers, because they are the most important component of mm-wave radiometer systems.

1.1.1 Background of the Research

The main motivation that drives heliospheric research is the study of solar event phenomena. Such studies help predict changes that these phenomena impose on the Earth's environment and how this affects life on Earth [16]. One of the most important of these phenomena is solar flare events. Solar flares are a sudden release of energetic charged particles observed in the form of brightness at the solar corona [17]. For many decades, studies have been conducted to investigate the impact of solar flares on near-earth technologies [18], spacecraft electronics [2], [3], [19], and terrestrial technologies such as electric power grids and communication lines [4]. These events are highly unpredictable which makes them "the most serious radiation hazard" in space [2]. This unpredictability is directly linked to a limited understanding of this phenomenon. By studying charged particles' origin, their acceleration mechanisms and their energy transport into the solar corona, solar flare events and related coronal mass ejection (CME) could be better understood [20]–[25].

In the studies conducted in [26] and [27], the observed data reveal the presence of mm-wave radio emissive electrons during non-thermal solar flare phases. This is confirmed in [5], where it is further stated that these energetic particles are the signatures of the impulsive phase of solar flares. In [26] it is further emphasized that the rise in temperatures around the plague areas on the solar disk is a consequence of energetic charged particles and can be detected several hours before the occurrence of the actual flare outburst. To study this effect, empirical models have been used to emulate solar particle behaviour [21], [27] to improve the understanding of solar flare events. In [21] and [22], however, the authors describe significant discrepancies between observed solar flare data and data obtained from empirical models.

Based on the above, there is a clear need for observed data to improve these models and to establish a comprehensive service management plan aimed at mitigating post flare damages. There have been several ground-based radio observatories in the frequency band ranging from

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microwaves (3-30 GHz), [28], [29] up to millimetre waves (30-300 GHz) [5], [30], [31]. Most of these observatories are no longer active today, and the remaining few (Big Bear Solar observatory, Owens Valley Solar Array, Mingantu Ultrawide SpEctral Radioheliograph)[28], [32] face significant challenges, including reduced tropospheric transmissivity [33], limited observation time as a result of Earth's rotation [8], and interference from ground-based transmitters, ground noise, buildings and mountains as depicted in Fig 2. Global positioning system (GPS) signals have also been employed to study solar flare events [7]. This method measures the ionization fluctuation in the ionosphere during the solar flare events, from which the diurnal quiet Sun total electron content (TEC) is deducted to determine the flare-induced TEC [6]. The problem with this approach, however, is that there is a need to know when the flare occurred, so that previous sidereal TEC data can be used to compute the flare-induced TEC. This process generally takes a few days, providing the results too late to take preventative action against energetic particles which arrive on Earth 1-2 days after ejection. On the other hand, solar flare EM radiation arrives within only 8 minutes after an event, making it more suitable for observation and timely data processing.

It is therefore clear that data needed to establish service management plans would only be relevant if they are obtained from mm-wave solar radiometers, as cm-wave observatories cannot observe higher frequency energetic charged particles [34] [35].

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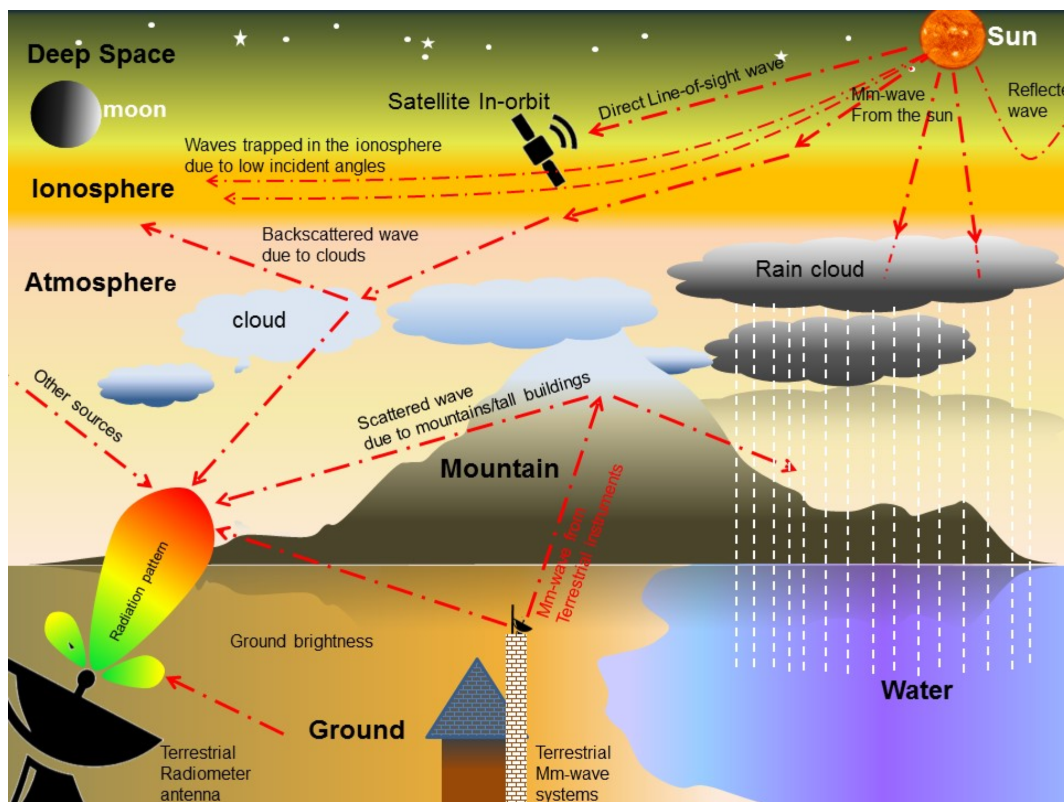

Figure 1.1. Graphical Representation of the Research Problem.

Based on all these considerations, placing an mm-wave solar radiometer in orbit would considerably eliminate the current observational limitations. A few studies have proposed such an instrument [8][36]–[38], but none have progressed beyond feasibility studies nor have any investigated an option of deployment on a low-cost CubeSat [39] mission using off-the-shelf components.

CubeSats (10x10x10 cm) have recently seen wide-scale adoption for a variety of space missions[40]–[42]. They are characterized by their use of commercially off-the-shelf (COTS) components, [34], [43], [39], novel design approaches, innovative packaging technologies, and novel integration techniques. The CubeSat standard's miniaturized volume (0.001m^3) imposes additional design constraints that necessitate the adoption of planar integrated systems as opposed to waveguide modules.

SoC and SiP are the two commonly used integration techniques. SiP is a complementary solution to SoC and offers alternatives where non-compatible die integration is required [44].

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Here, passives structures are implemented on low-cost off-chip mediums and then packaged together with on-chip active devices [13]. SiPs are manufactured at a reduced cost and the time-to-market is much shorter compared to SoC [45]. Although SiP is an interesting solution for multi-chip integration, some concerns remain w.r.t signal integrity, power delivery within the package, while at the same time requiring sophisticated verification tools [45]. Meanwhile, though SoC is less complex and less involved than SiP [46], the electrical performance of SoC is impeded at mm-wave frequencies by the low-quality back-end of line (BEOL) metallization in on-chip, a lossy silicon substrate and limited die size [47]–[50]. This lossy substrate and the proximity of on-chip structure increase on-chip parasitic elements which in turn degrade the performance of on-chip modules. The validation of layouts in the BEOL is equally complex, time-consuming and resource-demanding, especially when done outside the electronic design automation (EDA) tools [51]. This is because of the extreme aspect ratios, a multitude of thin dielectric layers, and dense via arrays that often lead to impractically large mesh sizes requiring major model simplifications [52] [53] [54]. All these simplifications, e.g. the segmentation of the model into small sectors [55], and the application of 2.5D geometry approximations [56] [57], lead to reduced simulation accuracy. While RC parasitic extraction tools such as Quantus RC [58], provides an alternative to EM solutions by offering faster simulation time within EDA tools as well as allowing for multiple iterations and optimization of first-pass design [59], the method is, however, limited to the extraction of R and C parasitics [60]. Therefore, a system integration between SiP and SoC is typically driven by the design goal, rather than optimized electrical performance, cost or size [44].

1.1.2 Research Gap

Based on several challenges of terrestrial mm-wave solar radiometers, placing a mm-wave radiometer in space is the preferred approach. This approach, however, would require a low-cost, lightweight radiometer; preferably small and light enough for the CubeSat platform. To achieve this, components on-chip need to be integrated with that off-chip in a planar off-chip medium with as little loss as possible. This would require the characterization of the electrical response of both interconnects (Figure 1.2) and lumped element parasitics of the on-chip module at mm-wave.

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These on-chip parasitics are a major impediment to mm-wave microelectronic circuits yet published studies generally do not present a pad-to-pad comparison of mm-wave LNAs, even though these MMIC LNAs cannot be deployed in isolation without packaging. The on-chip devices can only be probed in isolation; for any systematic performance evaluation, these devices need to be packaged (Figure 1.2) for system integration. Such integration presents parasitics that would influence the LNA's board-to-board performance significantly. To increase the first iteration accuracy of on-chip modules, parasitics need to be accounted for, through various post-layout validation tools such as 2.5D, 3D and RC parasitic extraction. Such a systematic comparison has not been found in the literature at mm-wave frequencies. In addition, the body of the literature does not address the impact of electron irradiation on SiGe LNAs at mm-wave frequencies. As a consequence, the survivability of mm-wave COTS LNAs or custom SiGe LNAs in orbit is unknown.

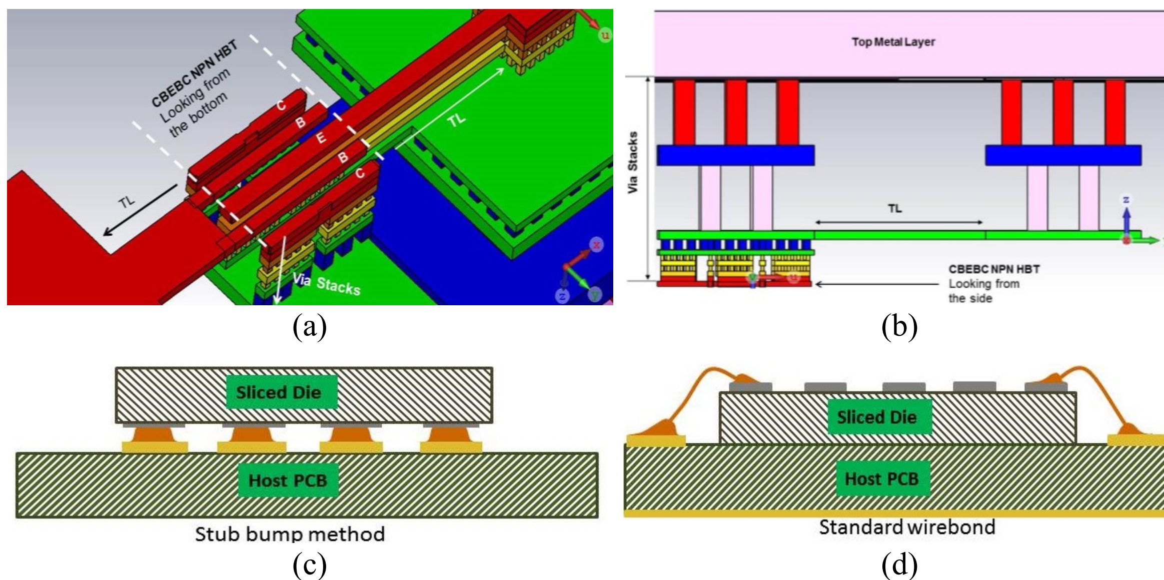

Figure 1.2. Interconnects that affect the performance of a BiCMOS HBT: a, b) On-chip transmission lines and vias between the pads and the BJT terminals, c) Flip-chip interconnect d) wire-bonding interconnect.

1.2 RESEARCH OBJECTIVES

The objectives of this research are to:

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- Establish a performance comparison between on-chip or off-chip matching of mm-wave LNAs integrated on PCB and Quantify the board-to-board difference in performance between on-chip LNA and its subsequent hybrid counterpart.
- Experimentally compare different approaches to EM modelling at mm-wave frequencies on-chip
- Quantify the effect of TID electron irradiation on the performance of V-band MMIC LNA in the SiGe process.

1.3 APPROACH

The approach adopted to meet the objectives stated are summarised as follows:

- A literature review focused on radiometers operation was conducted to establish the requirements for front-end components. This review identified the need for designing front-end mm-wave SiGe LNAs that can be characterised against TID electron radiation. The study also found the need to evaluate V-band LNAs for various types of integrations (Figure 1.3), to make the device readily integrable in a radiometry system at V-band. Through the literature review, MMIC LNAs topologies were identified [61], [62] as well as the method for MMIC-PCB integration [63], [64].

- A radiometer was designed [65] to establish typical performance requirements

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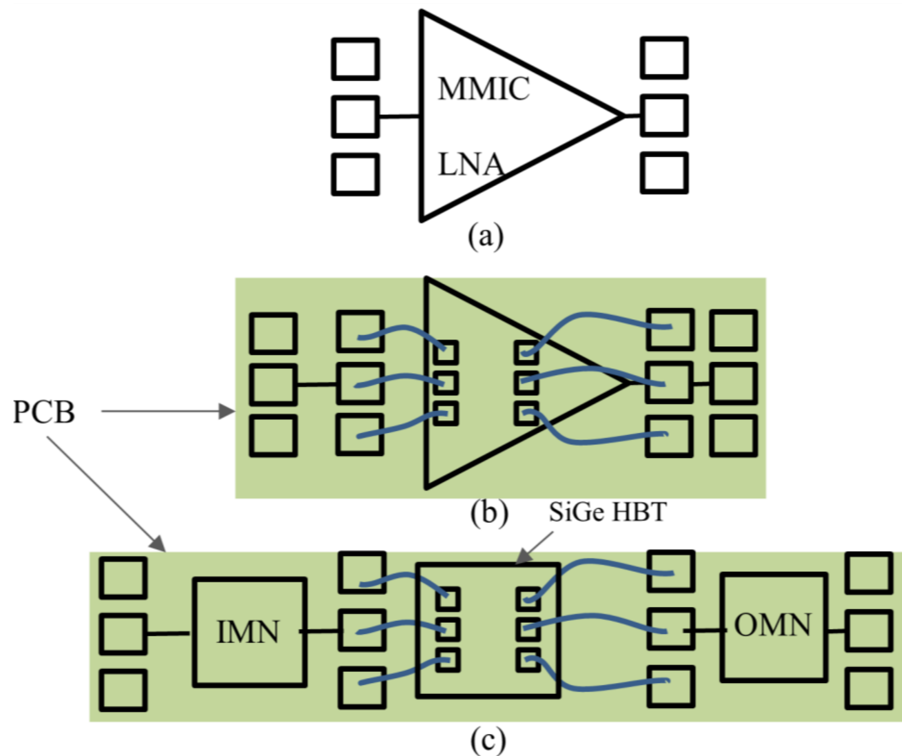

Figure 1.3. LNA integration approaches. a) MMIC LNA, b) MMIC LNA integrated into a PCB, c) hybrid with MMIC transistors matched off-chip on a PCB.

- The MMIC LNA architectures in [61], [62] were adopted and applied to meet typical V-band MMIC LNA requirements for a radiometer. The MMIC transistors were also designed in the same process, with the same dimensions as those used for the MMIC LNA. The schematic design was followed by an EM modelling of the layout transmission lines, as well as an RC parasitic extraction, before submitting it to GlobalFoundries US (GFUS) for fabrication.
- The hybrid LNA was designed simulated and prototyped. In this approach, the NPN HBT transistors on-chip was matched with off-chip passive on XT/Duroid 8100 substrate. The on-chip transistors were integrated into PCB via different approaches. The PCB was characterized through a wafer probing for both linear responses.

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- The on-chip LNAs was exposed to TID radiation using 2.28 MeV electron exposure from a Sr-90 strontium source. Both linear and noise figure measurements were conducted following consecutive iterations of radiation.

1.4 RESEARCH GOALS

The goals of this research are summarized as follows:

- To characterise microelectronic stack-ups through EM modelling and investigate the most suitable MMIC layout validation approaches at V-band between MoM, FEM, and RCPE.
- To establish the best design approach for V-band LNAs, between MMIC and hybrid MMIC/PCB.
- To quantify the performance degradation of SiGe HBT based mm-wave LNAs as a result of TID electron irradiation.

1.5 RESEARCH CONTRIBUTION

The study makes the following original contributions in the field of mm-wave engineering.

- A concept radiometer was designed to establish typical performance requirements [65].
- An experimental study that compares MoM, FEM and QRC parasitic extraction was conducted to validate the layout of an MMIC LNA at V-band [51]. This experiment found that the oversimplification in the MoM approach severely affects the S-parameters' response, making it the least accurate. Meanwhile, the FEM method, although the most accurate of the three, is extremely intricate, time-consuming and resource-demanding.
- The study of the stackups found that the front-end-of-line (FEOL) cannot be ignored when modelling on-chip passives, as this leads to significant deviation in both f_0 and S-parameters. Meanwhile, simplifications such as array vias to via blocks and the inclusion or exclusion of the etch factor do not significantly alter the simulation results, and can therefore be ignored to save time and resources [66].

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- V-band bandpass filters on PCB were designed, fabricated, and measured. This has not been in the literature at these frequencies, presenting a novel contribution to the state-of-the-art.
- A board-to-board comparison between an MMIC LNA to PCB integration and a board-to-board hybrid LNA was conducted for the first time. This found that the impact of the interconnect severely impedes the performance of an MMIC LNA integrated to PCB and in a hybrid approach. This was exacerbated in the case of wire-bond due to high interconnects insertion loss. The performance of the flip-chip LNA was proven to be a promising outcome for the mm-wave front-end.
- Electron irradiation data for V-band LNAs in SiGe is now available [67].

1.6 RESEARCH OUTPUT

Listed below are the research publications that have emanated from this study:

1.6.1 Peer-reviewed conference proceedings

- F. Sagouo Minko and T. Stander, 'LNAs integration comparison at V-band', International Conference on Electronics Packaging Technologies and Applications (ICEPTA), New York, United States, [Submitted].
- F. Sagouo Minko and T. Stander, 'EM Modelling Considerations for mm-Wave On-Chip Antennas,' *IOP Conf.* Ser. Mater. Sci. Eng., vol. 766, p. 012001, Mar. 2020.
- F. Sagouo Minko and T. Stander, 'A Comparison of BEOL Modelling Approaches in Simulating mm-Wave On-Chip Antennas,' in 2019 IEEE Radio and Antenna Days of the Indian Ocean (RADIO), Sep. 2019, pp. 1–2,
- F. Sagouo Minko, T. Stander and P. Cilliers. (2015). 'System Architecture for a Compact, Low-Cost 56-92 GHz Space-Based Solar Event Observation Instrument'. In 66th International Astronautical Congress. Israel, 11 Oct. 2015, pp. 2802-2811.

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1.6.2 Journal articles

- F. Sagouo Minko and T. Stander, 'The use of V-band bandpass filter on PCB as DC blocking capacitor in hybrid V-band LNA design', Int. J. Electron. Commun [Submitted].
- F. Sagouo Minko and T. Stander, 'Effect of TID electronradiation on SiGe BiCMOS LNAs at V-band,' *Microelectron. Reliab.*, vol. 112, p. 113750, Sep. 2020.
- F. Sagouo Minko and T. Stander, 'A comparison of three-dimensional electromagnetic and RC parasitic extraction analysis of mm-wave on-chip passives in SiGe BiCMOS low-noise amplifiers', *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 30, no. 2, p. e22019, 2020.

1.7 OVERVIEW OF THE STUDY

This thesis is organized as follows:

Chapter 2 introduces the research problem by providing the review of mm-wave LNAs as a critical component of solar radiometers. This looks into transistor processes as well as mm-wave LNA topologies. The study then focused on material and metalization processes, hybrid MMIC/PCB integration and SiGe devices' radiation tolerance at V-band.

Chapter 3 provides various methods and approaches that were followed. This includes the literature review approach that was adopted as well as the microelectronic design approach that considers the biasing, the matching, and the layout. The method for validating the stackups and for verifying the MMIC layout is also presented. Next, the methods adopted for characterising both the material and the interconnect are discussed leading to the hybrid LNA design discussion. The chapter concludes with a discussion on various measurement setups. This includes linear and noise figure measurements as well as TID radiation tolerance.

In Chapter 4, the MMIC LNA design is presented. This includes the DC and AC analyses, the schematic and layout designs, the full-wave EM and RCPE validation of the layout and

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subsequent simulation results. Finally, the measurement results of the MMIC LNA before and after the TID radiation experiments are also provided.

Chapter 5 presents the design of the hybrid LNA. First, the material and interconnects are characterised through simulation and experimentally. Next, the MMIC LNA integration into PCB is conducted. This is followed by a hybrid design, where MMIC transistors are matched off-chip using wire-bond and flip-chip transitions. The simulation results of MMIC LNA, MMIC LNA/PCB and the hybrid LNA integration are all compared. Then passive components design, and characterisation are discussed. This is followed by various LNA layouts and the discussion on measurements outcome.

Chapter 6 presents the overall conclusion of the study, details the challenges and limitations faced and offers recommendations for future works.

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CHAPTER 2 LITERATURE REVIEW

"Engineers like to solve problems. If there are no problems handily available, they will create their own problems." - *Scott Adams*

2.1 INTRODUCTION

This chapter provides a literature study on the state-of-the-art (SOTA) mm-wave LNAs, with an emphasis on MMIC and hybrid design approaches. The aim was to adopt a SOTA design approach for a V-band LNA for the radio front-end which would also serve as a test-chip in the study of the impact of RC parasitics and back-end-of-line (BEOL) modelling on MMIC LNAs at V-band. Furthermore, the chapter reviews the impact of various radiation mechanisms on the performance of mm-wave MMIC LNAs in SiGe technology, as well as the impact of on-chip/off-chip transitions in a hybrid V-band LNA design approach. This is because such transitions would be required both for integrating an MMIC on PCB as well as integrating MMIC transistors with the matching networks off-chip on a soft substrate in a hybrid approach. A process for the characterisation of both the interconnects and the host substrate material is also presented.

The chapter is structured as follows:

In Section 2.2, key parameters that affect the performance of a radiometer are discussed, justifying the criticality of LNAs with regards to the successful operation of radiometers. In Section 2.3, a review of SOTA MMIC LNAs is presented in order to isolate an MMIC LNA design topology to be adapted at V-band. Section 2.4 presents the review of SOTA integration topologies at mm-wave, with an objective to identify an integration technique suitable for MMIC LNA attachment onto a PCB, as well as for a hybrid LNA integration. Next in Section

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2.5, the materials and various processes are discussed, in relation to how interconnects are modelled, how materials are characterised and how to evaluate the impact of surface finishes on the performance of mm-wave LNA. In Section 2.6, MMIC layout verification methods are discussed in order to establish an approach that is the most effective at mm-wave, for an estimation of first-iteration accuracy of the protype. This is followed in Section 2.7 with a discussion on TID radiation tolerance of SiGe LNAs at mm-wave with the main focus on electron radiation. This is to establish how SiGe LNAs are perform under extremely harsh electron radiation conditions as found in low earth orbits. Finally in Section 2.8, a detailed summary of the chapter is provided.

2.2 MM-WAVE SOLAR RADIOMETERS

A radiometer is a receiver system that outputs a voltage level that is a linear relationship of the input's RF power [68]. The key parameter that ensures that a radiometer meets its goal is its sensitivity, sometimes quantified as the noise equivalent temperature difference (NETD) [68], [69]. In a general sense, a radiometer constitutes of the RF stage and the detector stage. The RF stage in most total power radiometers [68], [69] systems comprises an antenna directly followed by a low noise amplifier (LNA) that connects to a highly sensitive detector. In Dicke radiometers, however, this chain is broken with the inclusion of a Dicke switch as illustrated in [70]. The insertion loss of these switches needs to be as low as possible [71] so that the system noise temperature of the receiver chain is not compromised. According to the Frii's equation [72] in (2.1), the overall noise figure of the system is dictated by the first stage's noise figure. One can therefore conclude that to achieve a minimum NETD the LNA should provide the necessary gain while contributing as little noise as possible [73].

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_{N-1}}{G_1 G_2 G_3 \ldots G_{N-1}} \tag{2.1}$$

2.3 MMIC V-BAND LNAS

In this section, the SOTA of V-band LNAs is reviewed. This process seeks to identify current best practices for configurations for single-ended and differential LNAs, further improvements such as gain extension techniques, as well as matching techniques focusing on RF CMOS and especially in BiCMOS processes. To achieve this, the initial literature search was focused on

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V-band (50-75GHz). This resulted in a few resources which were deemed insufficient. The search was extended to include W-band (75-110 GHz) and resulted in a lot more resources.

2.3.1 Process technologies

High charge carrier mobility in III-V technologies such as GaAs and InP, makes them faster than silicon semiconductors [74], [75] for other similar process parameters. Silicon speed may be improved by using UHV/CVD techniques that grade germanium impurities to the silicon wafer [74], yielding silicon-germanium (SiGe) compounds that possess lower base resistance and are compatible with silicon processes worldwide.

The aggressive performance improvements of SiGe BiCMOS 130nm has opened possibilities for major applications at mm-wave [76]. These include a 77 GHz automotive radar [77], a 60 GHz, high data rate 100 Gbit/s telecommunication link [78], broadband amplifiers for optic receiver networks [79], and mm-wave multipliers [80], to name a few.

CMOS devices have also gained significant grounds as RF front-end devices [81]. In [82] for example, a 65 nm bulk CMOS LNA covering 55 to 64 GHz bandwidth is presented with a gain boosting technique. The final gain of the device is 12.8 dB with a competing NF of 3.8 dB.

Another breakthrough is FinFETs transistors [83]. These are high performing CMOS transistors in 22 nm with short channel effects. These transistors can achieve NFs of as low as 4 dB at V-band, with high f_T which, however, comes with lower f_{Max} [84] which can be improved by increasing the gate length of the transistor (e.g. 32 nm). In [85], however, high f_{Max} could be achieved by reducing the number of fingers which would improve the gate resistance [85]. Moreover, FinFET CMOS also suffers from self-heating, but this can be remedied by reducing the drain-source biasing voltage [83].

2.3.2 V-band and W-band LNA circuit topologies

2.3.2.1 Single transistor stage LNAs

In [86], a 53 to 117 GHz LNA is reported in a 28 nm FD SOI process using common source single transistor stages (Figure 2.1(a)). The topology is selected because of the low NF benefit that common source (CS) transistors offer. This is done by sizing the matching network to keep

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the NF as low as possible while sizing the transistor to maintain the bandwidth and increasing the stages to meet the gain requirement.

In [87] however, 90 nm SiGe BiCMOS is presented covering the 78-149 GHz spectrum, in a common emitter (CE) configuration (Figure 2.1(b)). Here, the bias is analysed to evaluate how it affects the gain, the NF and the matching. Inductive degeneration is included to increase the input resistance, which though it reduces the gain, facilitates simultaneous matching, and yields unconditional stability.

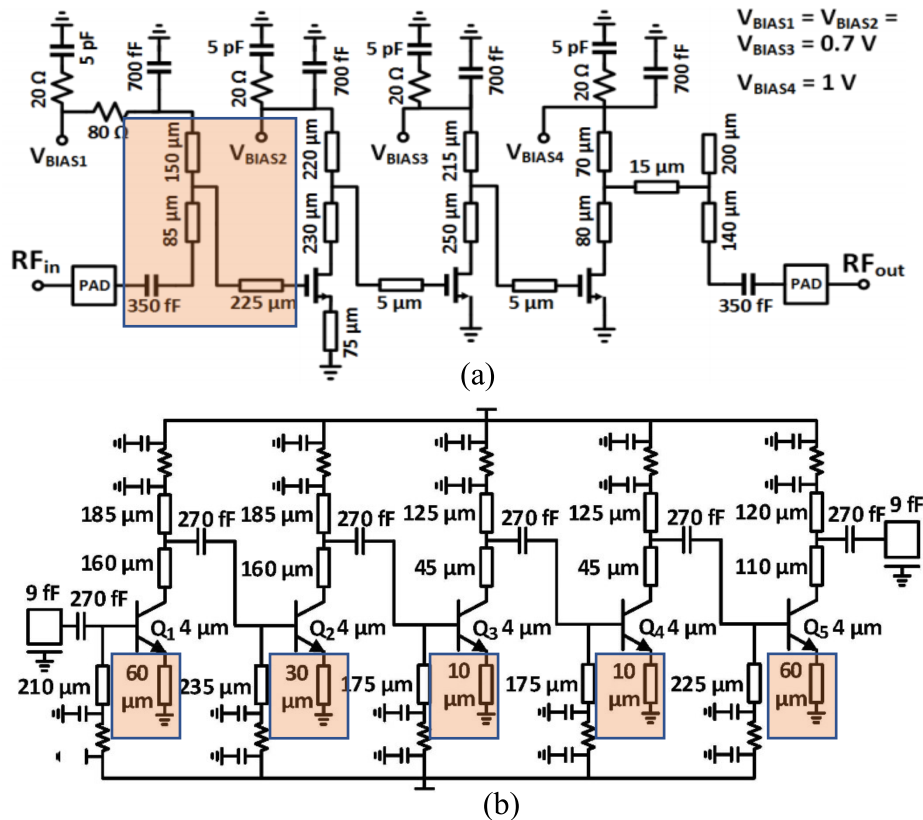

Figure 2.1. LAN with single transistor stages, a) three stages CS LNA, b) five stages CE LNA adapted from [86] and [87], © 2017 and 2014 IEEE.

2.3.2.2 Differential Amplifiers

Differential amplifiers are very popular in literature at mm-wave [88]–[91]. The main reason for avoiding single-ended LNAs is that they are sensitive to substrate noise and on-chip interference [92]. Furthermore, compared to single-ended designs, differential LNAs offer high

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gain, low noise figure, good linearity, and isolation. Differential amplifiers can be configured in a variety of ways (Figure 2.2) to optimize the occupied chip space, which is one of its dominant disadvantages.

In [88], the circuits are designed in 130 nm, and 250 nm BiCMOS processes with 3 µm top metal thickness. The circuit employs a T-matching and is biased through a current mirror (Figure 2.2(a)). The V and W-band LNAs achieve a maximum gain of 22.5 and 25 dB respectively including the insertion loss of the balun while having an NF of 7.2 dB and 7 dB respectively. In Figure 2.2(b), the circuit used a current source design for temperature compensation [91], and unlike the previous design, the inductive source degenerations are included in both stages to compensate for common-mode stability. In Figure 2.2(c) and d, transformers are used to provide differential biasing feeds, differential matching and also to provide for frequency selection by tuning the coupling factor *k* [93].

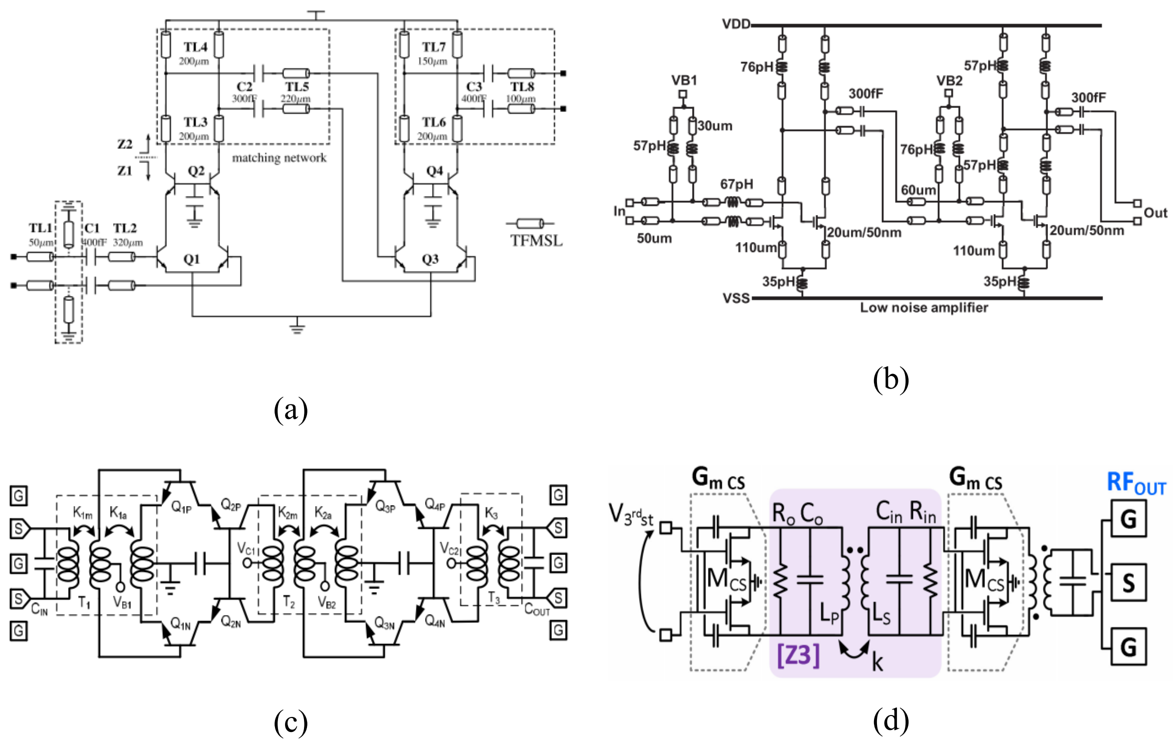

Figure 2.2. Mm-wave LNAs using transistors in differential mode. a) simplest approach, b) medium approach with source degeneration, c) using three winding transformers, d) using fourth-order interstage matching, and capacitive neutralization taken from [88], [90], [91], [93], © 2012, 2018 and 2013 IEEE.

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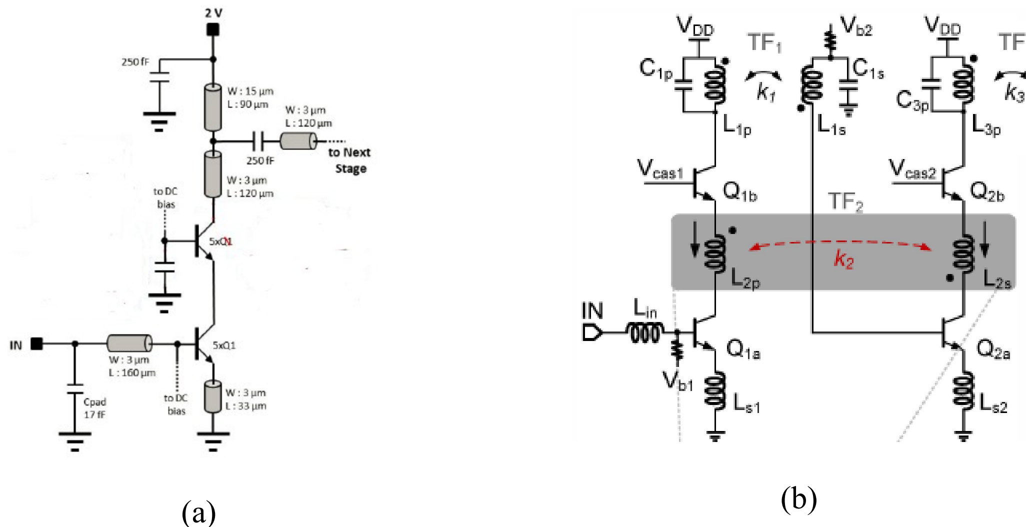
2.3.2.3 Cascode, Cascode common emitter, Cascode common source

A cascode pair is a combination where a CE/CS connects to a common base/gate (CB/CG) transistor (Figure 2.3). This provides better isolation, lower noise figure and a wider bandwidth [94] due to the reduction of Miller effects [95]. In the cascode configuration, the upper and the lower transistor can be matched to improve the noise figure, while the lower transistor can be degenerated to improve the linearity and stability.

A cascode pair stage could also be cascaded with either a CS or a CE stage as reported in [96] [97] (Figure 2.4 and Figure 2.5). The position of the cascode determines the desired targeted performance (gain, NF, and IP1dB). For example in [96], a 58-77 GHz LNA fabricated in 90 nm CMOS achieves 11.2 dB gain across the band with NF_{min} of 4.8 and IP1dB of -18.7 dBm, while the design of the 180 nm BiCMOS LNA covering 69-83.5 GHz in [97] achieves a peak gain of 14.5 dB with an NF of 7 dB, IP1dB of -11.4 dBm. CE/CS are well known to provide a lower noise figure as the first stage to the detriment of gain [86],[87].



(a) (b)

Figure 2.3. Mm-wave LNAs in a cascode configuration, a) conventional configuration no matching between the CE and CB, b) with inductively inter-stage matching, taken from [94], [95]. © 2009 and 2014 IEEE.

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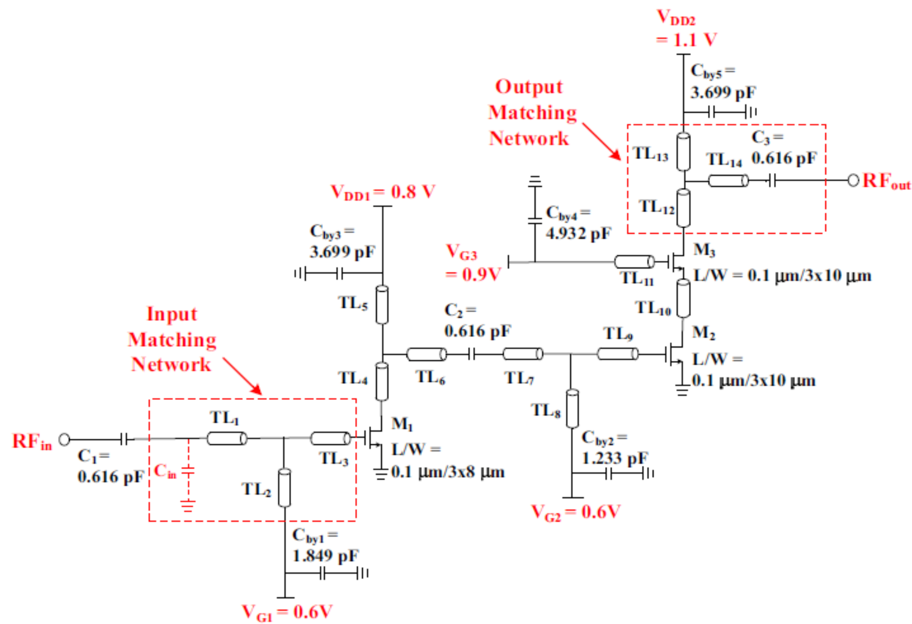

Figure 2.4. CS-cascode LNA in 90 nm CMOS, taken from [96]. © 2015 IEEE.

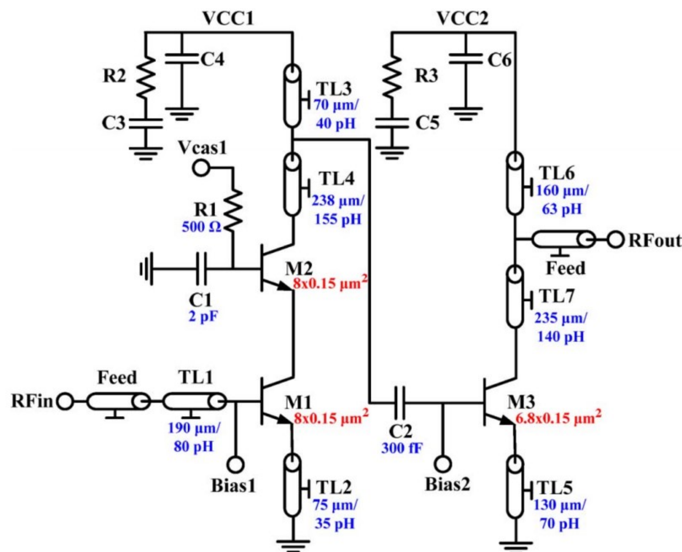

Figure 2.5. Cascode-CE LNA in 180 nm BiCMOS, taken from [97]. © 2010 IEEE.

2.3.2.4 Bandwidth extension

Extending the LNA's usable gain bandwidth can be achieved using the staggered gain method [98] or the neutralization method [99]. The staggered approach requires simultaneously tuned inter- matching network stages that create gain peaking, which is equalized across the band, as

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shown in Figure 2.6. The disadvantage of gain peaking is the ripple it creates as shown in Figure 2.6(b). The neutralization technique, however, is used to suppress the Miller capacitor [73] using an external capacitor or a transformer connected between the output and the input, mostly in differential designs [99], [73]. Though commonly used in differential designs, the neutralization technique can also be applied to single-ended using inductors [100].

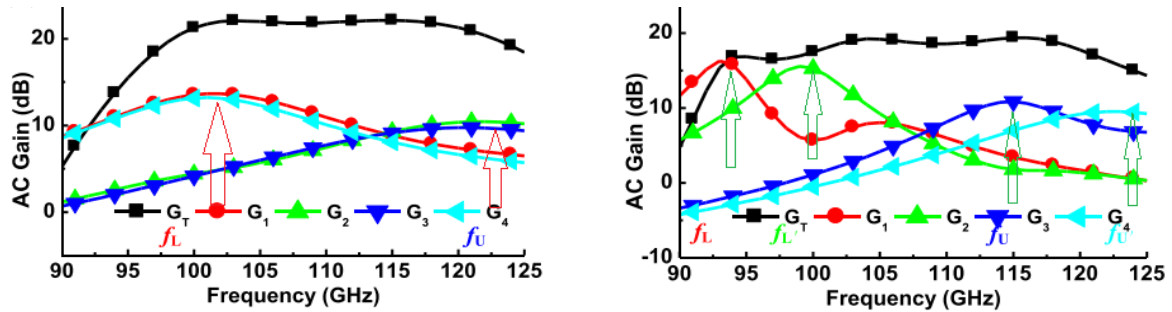

Figure 2.6. Tuning individual MN at different frequency points vs. two frequency points taken from [101], © 2016 IEEE.

2.3.3 Matching network approaches at V-band

2.3.3.1 L-matching

L-matching has been adopted in literature at mm-wave [98]. L-matching combined with source degeneration is a convenient approach to match the device while cancelling the parasitic effect of the pad capacitance C_{pad}. In practice, this would require a large inductance to achieve the same purpose when using other types of matching. By interstage matching the cascode transistor first, one would also achieve higher gain, improved isolation with a good noise figure [102].

2.3.3.2 T-matching

T-matching networks (as highlighted in Figure 2.7) have gained significant interest at mm-wave frequencies as they allow for tuning the Q-factor independently to achieve broadband operation [102]–[105]. Tuning the Q-factor of a T-matching optimizes the real part of the input impedance through a source degeneration inductors L_{s1}/L_{sh} as shown in Figure 2.7. The imaginary part of the impedance is compensated by the input inductor L_{g1} as indicated in Figure 2.7(a). The T-

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matching can be implemented using various inductors and capacitor configurations as shown in Figure 2.7.

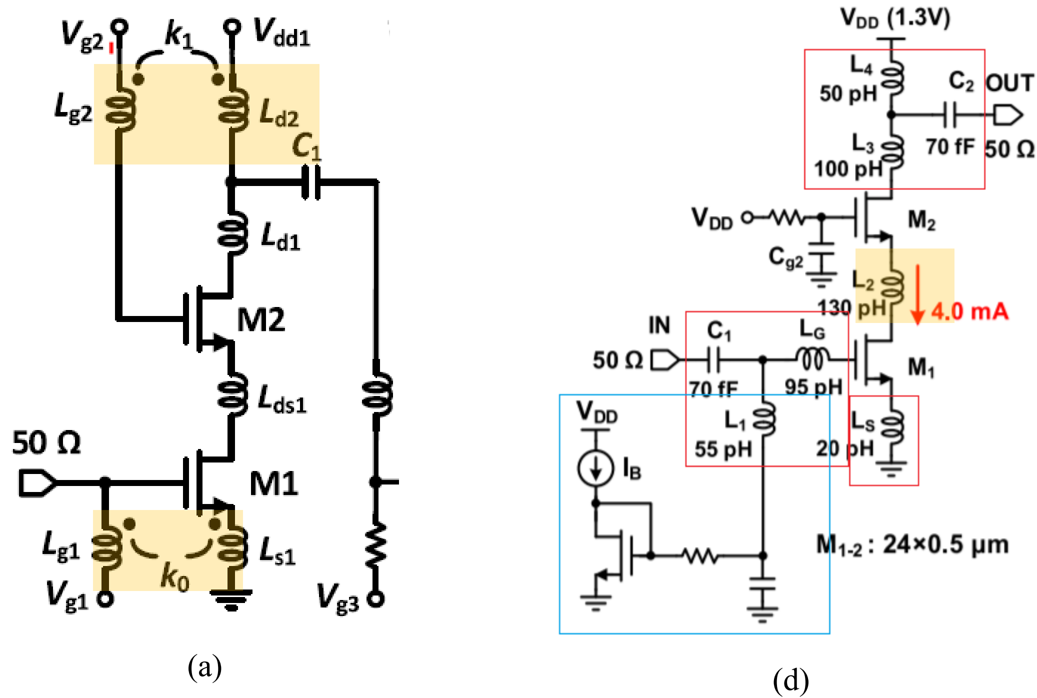

Figure 2.7. LNA with an emitter/source degeneration inductive and T-shaped matching, a) LNA topology that includes gate and source inductive degeneration, b) LNA topology that includes inductive degenerations and a current mirror adapted from [103] and [105], © 2020 and 2018 IEEE.

2.3.3.3 Transformer coupled matching

Transformer matching has also gained interest recently [93] [90], [106]. The design in [93] is fabricated in a 0.25 μm SiGe.C BiCMOS process using a three-winding transformer solution for broadband matching with different coupling coefficients to increase the real part of the input impedance R_{in}. This achieves $|S_{11}|$ of less than -10 dB in the passband with the gain of > 15 dB, NF of ±4.1 dB and the IP1dB of -22 dBm at 32 GHz. Low-k transformers have also been used in literature to optimize the occupied chip space by T-matching networks and improve the bandwidth of LNAs [107]. This, however, is not a viable option since high quality transformers are not readily available in the BiCMOS8P process.

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2.3.3.4 SOTA LNA comparison table

This section compares the state-of-the-art LNAs for the required frequency range. Table 2.1 presented does not aim at providing an exhaustive list, but rather to present the most relevant to the current study. From this list, it is evident that SiGe LNAs in 130 nm processes are very competitive as far as performance is concerned, with NF as low as 4 dB at V-band, competitive gains, and low DC power consumption as compared to their CMOS counterparts. These SiGe LNAs adopt a variety of matching network topologies ranging from series-shunt stub [87], LC tank [93], [94], [108], and T-type matching networks [61], [88]. Furthermore, due to the topologies adopted, the occupied chip area appeared less than those in other processes.

Table 2.1. Comparison of SOTA mm-wave LNAs

Properties	[86]	[87]	[88]	[90]	[93]	[94]	[96]	[61]	[108]
Technology	28-nm FDSOI	90 nm SiGe	250 nm SiGe	65 nm CMOS	250 nm SiGe	130 nm SiGe	90 nm CMOS	130 nm SiGe	130 nm SiGe
Topology	CS	CE	Diff	Diff	Diff	Cas	CS-Cas	Cas	Cas
Frequency (GHz)	53- 117	75-110	47-77	60-90	20-40	60	58-77	95-110	55-71
$\|S_{21}\|$ (dB)	17.7	25-34	22.5	21.8	29-37	12	11.2	20.5	13.5
NF (dB)	6	3.5-4.5	7.2	6.48	3.1-4.1	4.5*	4.8	4	4.4
S_{11} <-10 dB BW (GHz)	<- 10	<-12	<-14	70-82	24-40	58-62	60-80	<-10	59-71
P_{DC} (mW)	38.2	15.6	52	43.9	80	9.25	10	17	4.8
OP1dB (dBm)	1.5	8.5	-19 *	-	7	0	-18.7	-24	-5.5
Area (mm^2)	0.456	0.30	0.5	0.42	-	0.28	0.55	0.41	0.14

*Simulation results only

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2.4 HYBRID LNA

A few MMIC LNAs to PCB assemblies have been reported in the literature. In [109] for example, a 0.10 µm GaAs MMIC LNA is integrated through a multi-chip module (MCM) assembly method. Here, the LNA chip is attached to the PCB directly through 130 µm diameter solder balls. The NF and the gain data show a decrease of ± 1.5 dB and 0.6 dB, respectively, from those of the MMIC LNA. These findings are consistent with that which is reported in [110], whose assembly cross-section is shown in Figure 2.8.

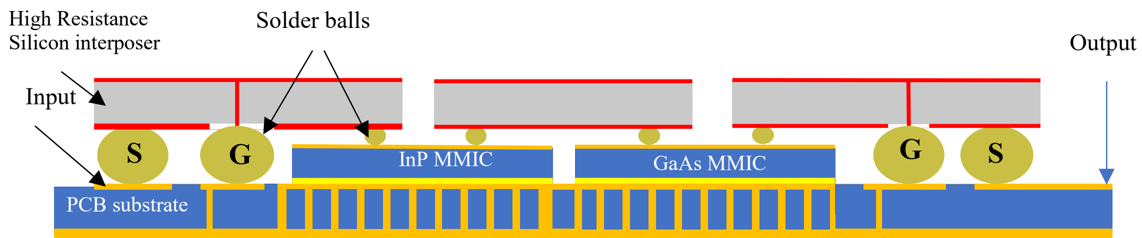

Figure 2.8. LNA in an MCM assembly approach adapted from [109], © 2014 IEEE.

In [49], a 0.5 µm SiGe BiCMOS, CE LNA is integrated with off-chip passives at 5 GHz. Here, wire-bond transitions are used between the on-chip active and the off-chip passive components. An improved gain and NF are reported compared to their MMIC LNA counterparts. This improvement, however, is because of minimal interconnect parasitic effect at low frequency, which becomes a major design consideration at mm-wave as discussed in [63]. Here, a liquid-crystal-polymer (LCP) material is used, where a 94 GHz 130 nm SiGe LNA is mounted in a flip-chip assembly approach (Figure 2.9). A non-negligible degradation is observed due to the transitions amounting to 1.6 dB in the gain and ± 1.3 in the NF reduction.

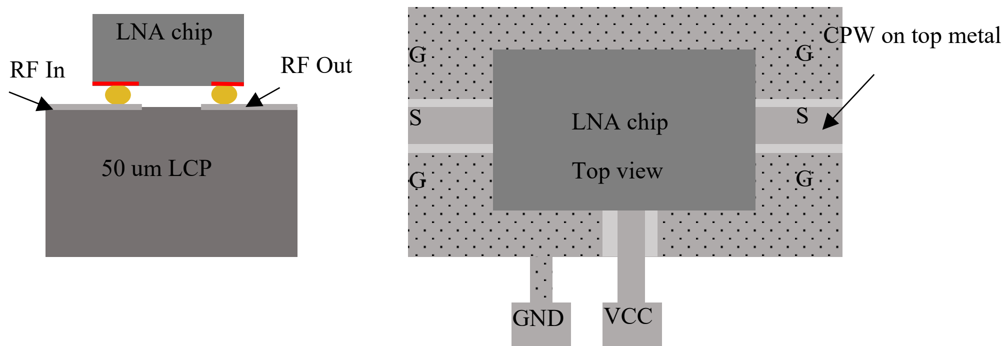

Figure 2.9. 94 GHz 130 SiGe LNA flip-chip to LCP adapted from [63], © 2013 IEEE.

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In some other designs, the die is sunk in a cavity [64] created on the PCB (Figure 2.10) to shorten the length of wire-bonds, which directly translates into a reduction in the interconnect inductance. The LNA chip itself is designed in the differential approach using 0.25µm SiGe transistors at Ka-band.

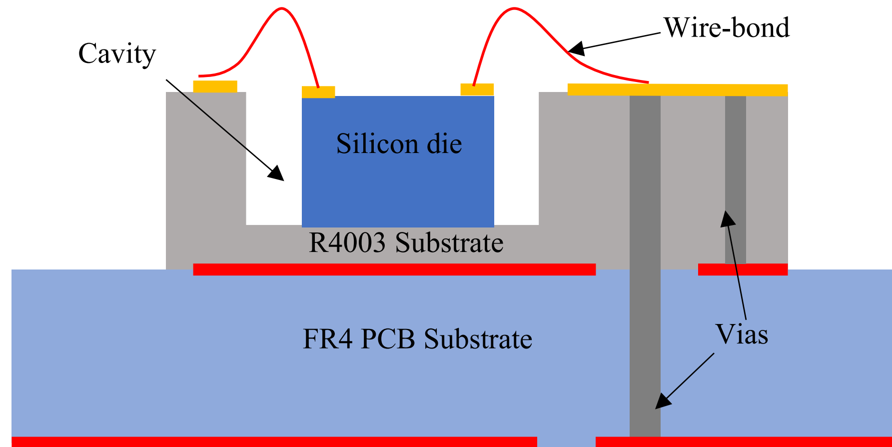

Figure 2.10. MMIC LNA-to-board assembly with the chip sunk in a cavity adapted from [64], © 2019 IEEE.

In [111], the packaging effect of flip-chip and wire-bond is evaluated. In this case, a CMOS MMIC LNA is first simulated and measured to establish the base of the study. Next, the chip-package co-design is done by extracting the package parameters in order to re-construct an equivalent network shown in Figure 2.11. The $|S_{21}|_{max}$ of 15 dB and NF of 3.5 dB are measured at an f_0 of 2.5 GHz. The chip to package $|S_{21}|_{max}$ of 14.8 dB and 13.6 dB are recorded for flip-chip and wire-bond transition respectively, while NF of 3.5 dB and 3.8 dB are also recorded, of which the flip-chip approach appears the most promising even at low frequency.

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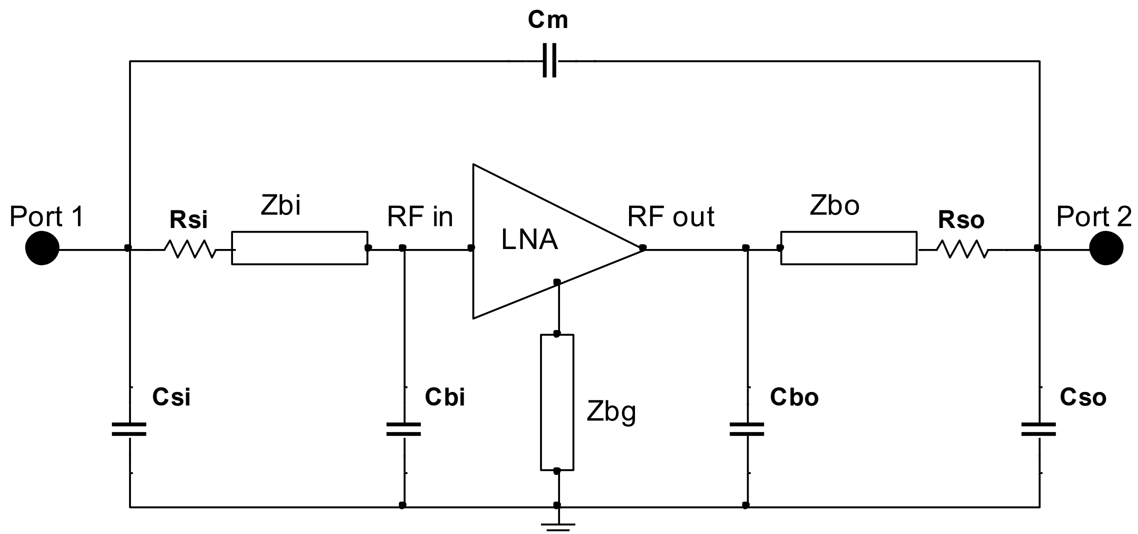

Figure 2.11. Chip-package equivalent circuit adapted from [111], © 2009 IEEE.

From these reviews, the MMIC LNA to package/board is very common in literature regardless of the processes, frequency bands and topologies. However, there is no reported literature on moving the entire matching network off-chip on PCB, while keeping SiGe transistors on-chip at V-band. Where such was demonstrated, it was below 10 GHz [112], [113], where interconnect parasitics have little to no effect on the performance of the LNA.

2.5 MM-WAVE MATERIALS AND PROCESSES

This section provides a review of various types of interconnects between MMICs and the host substrate material. In addition, the chapter also reviews various methods for substrate characterisation for hybrid mm-wave LNA designs.

2.5.1 Substrate Materials and Metallization Processes

Designing matching networks on-chip is a big challenge for RFIC designers due to high conductivity silicon substrate, and lossy on-chip passives which affect the quality factor required by these networks [112]. With rapid interest in high speed and high data rate systems for 5G technology and automotive radar, multi-chip assembly on high resistivity substrates has become an active research topic [114]. In this type of approach, heterogeneous systems are integrated into multilayer substrates using on-chip actives on silicon, with embedded passives

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[115]. These substrates can be based on laminated liquid crystal polymer (LCP) [116] or other PCB-type materials where multi-chips (LNAs, Mixers, PAs) are integrated using various integration means such as wire-bonds, ribbon bonds or flip-chips [117] as discussed in Section 2.4.3. This is commonly known as laminated multi-chip modules or simply MCM-L. Although a very popular and cost-effective packaging option, MCM-L can suffer from interconnection reliabilities issues leading to failures [118]. Contrary to MCM-L, co-fired ceramics multi-chip modules (MCM-C) use low temperature co-fired ceramics as a base substrate which provides a more stable dielectric constant up to high frequencies [119], with high-quality gold or silver metal layers. The process provides low dielectric loss, making it suitable for embedded passives such as high-Q, small size inductors, resistors, and capacitors [119] and substrate integrated waveguide bandpass filters at V, W, and D bands [120]. In many cases, benzocyclobutene (BCB) [114], [121] is used as the integration dielectric substrate in a deposited multi-chip module (MCM-D). This substrate in which modules are integrated may be mounted on top of a high-resistivity silicon (HR-Si) substrate [122]. In contrast to both MCM-L and MCM-C, MCM-D provides the highest connection density [123] but suffers from a higher fabrication cost [124]. MCM-D allows for the integration of other passives within the same substrate. The selection of the integration media is therefore not only driven by the performance, but also by cost [114] and the availability of processes worldwide, as that would impact the turnaround time and define the duration of a given project.

2.5.2 Interconnect approaches

Apart from the substrate materials and metallization options mentioned previously, the technology used to connect the die to the substrate also plays a vital part in the multichip system's operation. There are numerous options available today, including wirebond, flip-chip, ball grid arrays (BGAs), wafer-level packaging (WLP) and true silicon vias (TSVs) to name but a few [125]. Each of these packages has its requirements; for example, the BGA is recommended for packages with high I/O pin counts, while the flip-chip does not necessarily have to have such a high I/O density, but if required, the pitch can be reduced to meet such demand, while also offering a wider bandwidth [14]. Wirebonding on the other hand is currently the most popular integration type worldwide, however, because of its nature, the bonding pads

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must be at the periphery of the chip. The TSV and WLP are integrated vertically at the wafer level [126]. Based on the above requirements, and availability as post-processing packaging steps, the wire bonding and flip-chip are the only two viable options for this research study.

2.5.2.1 Wire-bond interconnects

A few studies in the literature have investigated the performance of wire-bond interconnects from DC up to mm-wave frequencies [127]–[129]. Wirebond inductance depends on the length of the wire as well as its profile [130]. In [131] and [127] approaches to reducing the wire-bond inductances are presented by the use of multiple wires or short travel loops instead of straight wires. Other methods absorb the equivalent LCL parasitic network into the matching network[130], turning the negative impact of the wirebond into a positive outcome. The effective inductance of the wires can be extracted via EM simulation data, and schematic simulated using the π-model representation described in [127], [131]–[133]. Here, the series resistance, the inductance and shunt capacitance could be computed using the two-port network's ABCD matrix.

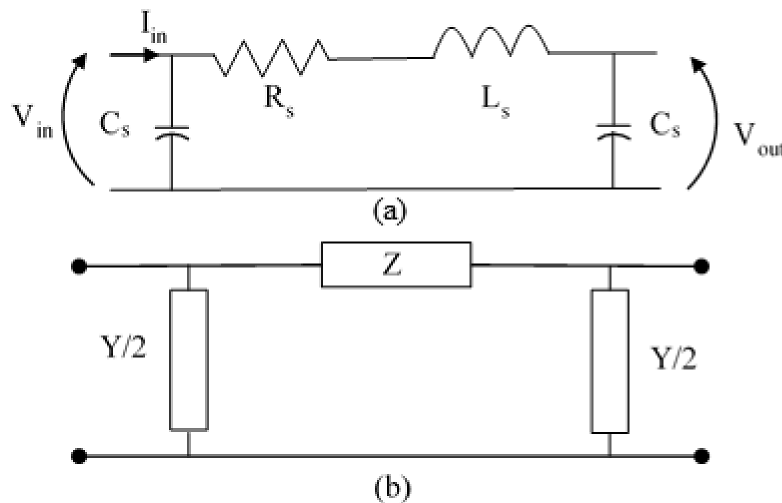

Figure 2.12. Equivalent circuits of wire bond interconnect

2.5.2.2 Flip-chip

The flip-chip technique entails attaching the die upside-down on a host substrate material with solder joints [133]. Flip-chip interconnects have become an increasingly attractive die

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attachment method especially at higher frequency [134]–[136]. This is due to the short interconnection length that it offers compared to wire bond interconnect, which suffer significant degradation as a result of a longer wire bond length [137], [135]. A π-model equivalent circuit of the interconnect provides a smaller inductance [132] and very low series resistance [133], [111] Due to the smaller size, which translates to a small interconnect profile, the performance variation of flip-chip interconnect is less noticeable, making it very attractive at mm-wave frequencies.

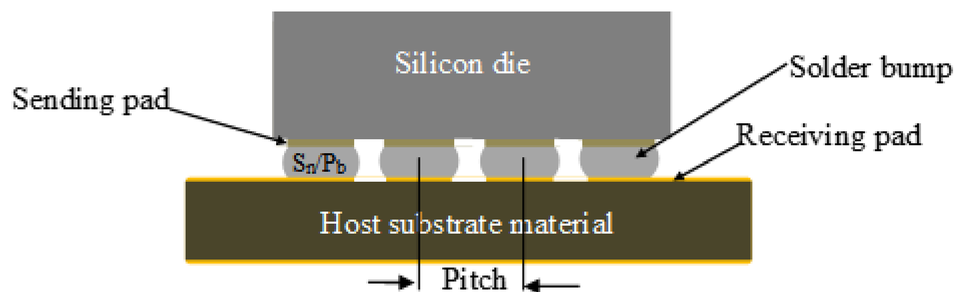

Figure 2.13. Flip-chip interconnect representation

A few studies that have looked at the assembly of V-band MMIC with passives on package using flip-chip are on GaAs HEMT [138] or GaAs PHENT [139]. On the CMOS process, the reported flip-chip LNA assembly is at W-band [140]. Here, reduced interconnect parasitics is reported at W-band due to compensated bump landing pads. Using simulation or measurement results, an ABCD matrix as provided in [111] can be used to extract the model parameters. It is evident that many works in the literature, as shown above, focus on the characterisation of the interconnection rather than the assembly.

2.5.3 Material characterisation

The performance of planar transmission lines at V-band is affected by many properties of the substrate material on which they are fabricated. The most important consideration here is the insertion loss, which reduces the Q-factor of the transmission line of matching elements. This loss impacts the NF of V-band LNA. It is, therefore, crucial to review factors that would impact various loss mechanisms of a transmission line.

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2.5.3.1 Resonator's characterisation

Resonators have widely been used to characterise substrate materials and transmission lines [141]–[144]. Regardless of whether the T-resonator in [143], the cavity resonator in [144], or the ring resonator in [141], [142] is used, the relative permittivity and the loss tangent are the primary common output parameters. Among the above approaches, the ring resonator appears to be the simplest approach [142]. This is because, in straight line resonators, the edge effect needs to be properly modelled as shown in [143] and [144]. It, therefore, appears that if the resonant peaks are identified, the dielectric constant and the Q-factor can be determined, assuming that the metal conduction loss and radiation loss are minor in comparison to the substrate loss.

2.5.3.2 Surface finishes

It has been shown from the literature [145], [146] how the various type of PCB finishes affect the performance of RF/MW circuits. These surface finishes are compared against bare copper which serves as a reference. In [146], the electroless nickel immersion gold (ENIG), the electroless palladium immersion gold (EPIG), the immersion silver immersion gold (ISIG) and copper masked with overlay (CU+CL) are studied up to V-band. It is found in [145] that besides bare copper, ISIG is the best option for RF circuits on V-band, while ENIG shows significant deviation from the bare copper performance.

2.6 MICROELECTRONIC LNA LAYOUT VERIFICATION

In this section, the review focuses on methods used to estimate the pre-production and post-production accuracy of MMIC LNAs at V-band. Of particular interest is EM verification using the 2.5D method of moments (MoM), 3D finite element method (FEM) and the RC parasitic extraction methods (RCPE).

2.6.1 2.5D and 3D EM verification

EM verification of large on-chip structures is a complex problem, to [52] [53] [54] due to the extreme aspect ratios and thin interlayer dielectric layers, both of which contribute to large mesh sizes. Modelling these structures using 2.5D or 3D EM is possible because of the short

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mm-wave wavelengths that enable the use of distributed transmission lines [147]–[149]. Feasible EM models, however, require major simplifications including the segmentation of the model into small sectors [55] and the application of 2.5D geometry [56] [57]. The direct impact of these simplifications [150] is the reduced first-iteration accuracy, with deviations of several hundred MHz in the resonant frequency (f_0) of resonant patch antennas above 60 GHz, for example. Another challenging factor in EM co-simulation is the interaction between microelectronic EDA tools and 3D EM tools [151]. This interaction adds to the longer design time already affected by EM simulation, which can vary from 50 seconds to 38 hours for on-chip capacitors alone [152]. Regardless of these challenges of EM simulation and long simulation time, EM modelling [106] [153] is useful in the extraction of the device parasitics including inductors and is effective in the estimation of the first-iteration accuracy of the mm-wave circuits [51].

2.6.2 RC parasitic extraction

Several algorithms have been proposed [58] for RC parasitic extraction on-chip. The software package that implements these is Quantus RC (QRC) which is a popular extension to the Cadence Virtuoso IC IDE [60]. This performs parasitic extraction through a 3D random walk field solver (RWFS) that detects RC parasitics on-chip. RCPE's limitation lies in the fact that it does not account for parasitic inductances and transmission line effects, which are crucial for MMMIC design compared to MMIC design [88]. RCPE has been successfully applied at Ka-band [154], where multiple optimization iterations were required to meet the targeted group delay in a 130 nm BiCMOS technology. At V-band, the use of RCPE led to a much-improved performance estimation of the LNA performance in 90 nm CMOS [155]. In [156], RCPE is successfully used to extract the capacitance of a modified capacitor with underlaid slow-wave structures on a 65 nm CMOS process. It is evident that RCPE is particularly commonly applied in RFCMOS and BiCMOS. This could be because most RCPE tools are created for CMOS EDA tools that aim for VLSI integration [157], while III-V design kits are typically created for RF circuit simulators such as Agilent ADS [158] [159] or NI AWR Microwave Office [160].

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2.6.3 FEM vs MoM vs RCPE

A direct comparison between EM solvers and RCPE tools has been attempted by a couple of studies [147], [161]. For example, in [161] the performance of a 2.4 GHz LNA are compared pre-production and post-production. It is found that the FEM-based EM solvers better estimate the measurement result than the RCPE method. This is confirmed in the study conducted at V-band in [51]. Meanwhile, in [147], 2.5D MoM appears most effective compared to RCPE at K-band, but when compared to FEM in [98], MoM presents a significant divergence in the estimation of f_0 and $|S_{11}|$ which is non-negligible. It can therefore be concluded that, while the FEM can be reserved for a final verification due to its long computational time, RCPE may be suitable for first-pass iteration.

2.7 RADIATION DEGRADATION OF SIGE BICMOS

SiGe is consistently a popular choice in literature even for applications in environments high in ionizing radiation such as the van Allen belt in low Earth orbits [162]. In such applications are found 60 GHz inter-satellite communications [163] and radiometers [164], [165] as well as high bandwidth communications in high energy particle experiments [166].

V-band front-end components required for these applications need a certain degree of ionizing radiation tolerance. To achieve this, SiGe devices have been exposed to gamma, neutron and proton radiation [162], [167], [168]. These studies have found that the exposure of SiGe devices to these mechanisms cause only minor atomic displacement and ionization damage at a device level. All of these studies have suggested a noticeable excess in the post-radiated base current due to particles trapped between the base and the emitter junction [169]. Another study has reported a degradation in the base resistance r_b and maximum oscillation frequency f_{Max} after neutron irradiation [167]. Equation (2.2) shows the relationship between r_b and f_{Max}, from which any variation in one of these two would affect the NF of the device.

$$f_{max} = \sqrt{\frac{f_T}{8\times\pi \, r_b C_{jc}}} \tag{2.2}$$

A few studies have reported TID effects on SiGe HBT LNAs at different frequencies. In [170], a bias tuning method is adopted to mitigate the effect of 63.3 MeV proton irradiation on $|S_{21}|$

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and NF in a 10 GHz LNA. According to [171], the increased NF in the reported 60 GHz LNA is due to increased r_b, following 63.3-MeV proton exposure. The data in [169] indicates up to 94 % reduction in $|S_{21}|$, following electron radiation exposure at S-band.

In [172], MIM capacitors exhibited an increase in capacitance as well as leakage current post-radiation. Based on this conclusion, it can be inferred that MIM capacitor damages would affect the passband of an LNA that uses them as both bypassing and decoupling capacitors.

It is important to note that V-band LNAs in 3rd generation 130 nm BiCMOS, which comprises both oxides filled shallow and deep trenches, are not included in these studies. These areas are particularly susceptible to trapped charges, which may alter the performance of an LNA [173]. Furthermore, there is non-existent data pertaining to the effect of electron radiation on SiGe LNAs at V-band explicitly, except for the work presented in [67].

This type of experiment could be conducted using a Strontium Sr-90 electron radiation source [23]. Such a source releases an electron having a peak energy of ± 0.58 MeV during the first decay, whose average is 210 keV, yielding a Yttrium-90. The second decay's peak energy is ± 2.26 MeV (average 980 keV) which yields a Zirconium-90 [24].

2.8 SUMMARY

The first part of this chapter explores why LNAs are integral parts of radiometers, by considering the sensitivity of radiometers known as NETD. These parameters are shown to be dictated by primarily the frontend LNAs based on the Friis equation.

It was reported that mm-wave LNAs are mostly fabricated in either III-V technologies or in silicon-based CMOS and SiGe. Group III-V technologies, although known to perform better at high frequencies, are far more expensive to prototype. On the other hand, CMOS processes are readily available worldwide and are cost-effective at expense of performance. Thanks to bandgap engineering, SiGe can compete with III-V technologies, and is compatible with silicon processes, making it a candidate for mm-wave systems [174].

Next, mm-wave LNA design topologies were discussed. Among the most popular topologies are the cascode topology in both the single and the differential configurations. This included many variations such as single-ended/cascode cascades for minimum noise performance,

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cascode/single-ended cascade for high gain, cascodes with transformer coupling for noise matching, and cascodes with source/emitter degeneration. These topologies are combined with various types of matching of which the T-matching approach and transformer matching emerged dominant. From this consolidated literature, it was found that designs based on 130 nm SiGe HBTs were the most competitive with regards to meeting performance parameters at V-band particularly, given the requirements for radiation hardiness.

To conclude this review, it was reported that EM methods are commonly used to verify the validity of layouts using 3D or 2.5D EM simulation. It was, however, found that 2.5D methods were less accurate than 3D methods, resulting in deviation in the S-parameters. Other studies preferred RCPE verification, which is less involved than full-wave methods but does not account for parasitic inductance. There was no published case study where all three methods were compared at V-band.

Furthermore, the other aspect that makes SiGe a candidate for many applications is the reported resilience to multiple radiation mechanisms. It is found, however, that there is no literature on how V-band SiGe LNAs' performance is affected by TID, especially when considering electron sources. The only literature that reported on this topic was conducted at S-band and recorded total S_{21} damage of up to 94%, but no post-radiation NF or power consumption data was reported.

Finally, various types of integrations techniques used in systems in/on-package were reviewed in the context of V-band hybrid LNAs. This review included the wire-bond, flip-chip, MCM-L, MCM-C and MCM-D, and looked at process availability, complexity, and process cost. From this review, it was found that, when comparing wire-bond with flip-chip interconnects, the latter provides better performance (lesser inductance) whilst the former is readily available and easier to apply. When comparing MCM-L, MCM-C and MCM-D, it is reported that MCM-C is the most popular among the three, providing a stable dielectric constant (DK), with high-quality metallizations which allow for embedded passives and high-Q inductors. In the case of MCM-L where PCBs are used, the review was extended to the material characterisation and the methods adopted in literature for that purpose. These include ring resonators, cavity resonators,

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and T-line resonators. Among these, the ring resonators were said to be the simplest, yet still effective in determining the DK and the quality factor and loss tangent of a substrate.

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CHAPTER 3 METHODOLOGY

"Design is not how it looks and feels like. Design is how it works."

-Steve Jobs

3.1 INTRODUCTION

In this chapter, the methods used to test the hypothesis described in Chapter 1 are presented. These include the design method of the V-band on-chip and the off-chip LNAs, as well as the approaches to EM verification to characterise the off-chip transitions. The chapter concludes with the description of radiation experiments and measurement approach of both devices to electron radiation to complement the study conducted by [175].

3.2 GENERAL APPROACH TO THE STUDY

The approach followed in this study was first to identify the problem, as was motivated by [8], [70], [176]. A component survey was conducted to evaluate the feasibility of integrating an mm-wave system in a CubeSat platform and how these could be integrated on a soft substrate, as well as the type of on-chip to off-chip transitions that would work. This was to identify the availability of die-based front-end components to allow for either flip-chip or wirebond integration. The study also identified the operating bandwidth of the components, the performance parameters and the die size. This process eliminated all waveguide components for their non-compliance with planar integration approach. Following this, single- and double-down-conversion receiver architectures were simulated in AWR VSS to check the feasibility of mm-wave system integration using COTS components. From the simulation process, it was found that neither wideband mm-wave mixers and synthesisers were readily available, nor were there any mm-wave bandpass filters off-the-shelf, making a system integration based on COTS

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highly improbable at mm-wave frequencies at this stage. Furthermore, the survey found that none of the proposed LNAs was space qualified. These needed to be characterized to check their radiation tolerance [177], [178]. To address these problems, a BiCMOS 130 nm process was selected to design a V-band LNA, characterise it under TID electron radiation to assess its resilience once in orbit. Next, on-chip active devices in the above process and off-chip passives were integrated into a hybrid configuration. Here, the flip-chip and wirebond transitions were evaluated, the off-chip substrate material was characterised as well as the PCB capacitors and other transmission lines. The performance of the full on-chip and hybrid LNAs are then compared.

3.3 LITERATURE REVIEW APPROACH

The literature review as presented in Chapter 2 was conducted using a systematic method [179]. Firstly, various V-band LNA topologies in the 130 nm BiCMOS process were identified. These were compared based on the achieved forward transmission gain, NF, OP1dB and the operating bandwidths. The limitations of each topology were also studied, looking mainly at the type of matching, the biasing networks, and the occupied chip size. The literature then focused on identifying V-band LNAs with hybrid integration (on-chip active components and off-chip passives). Of particular interest was the type of PCB materials used, the type of chip-to-PCB transitions, the effect of PCB surface finish and how all these variables affected the performance of hybrid LNAs. To conduct this study, the resources were collected from Google Scholar, IEEE Xplore, Science Direct and Scopus.

3.4 MICROELECTRONIC DESIGN APPROACH

In this section, the design approach applied in this study is discussed, as presented in [61], [180]. No novel contributions in the LNA design procedure is made.

3.4.1 DC and AC analysis

The BiCMOS8HP process, utilising 7 metallization layers and two stages of cascode configuration HBT [61] was used. Initially, the DC analysis was conducted in *SpectreRF* to establish the operational point of the transistors for a given dimension by tracing the I-V curve and plotting a quiescent point on the curve. Constant base currents were used to force the

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required collector current of I_C = 4.27 mA using a bias-tee schematic configuration, from which the S-parameter simulation was conducted to extract linear and noise figure parameters. The resulting S-parameters were used to determine the stability criteria of the circuit by calculating the Rollet stability factor K = 2.527 at f_0, the determinant of the S-matrix and the unilateral stability criteria μ = 1.47. These conditions indicated that the transistors were unconditionally stable under the selected bias point.

3.4.2 Matching Networks

3.4.2.1 Noise figure and Gain flattening

The unmatched S_{opt}, NF_{min}, the K-factor and R_n were extracted from S-parameter analysis in *SpectreRF*. To obtain the best compromise between S_{21} and NF_{min}, the bias conditions were adjusted by slightly shifting the Q-point to the left of the I-V curve (Figure 4.5) resulting in I_C = 4.30 mA, V_{CE} = 1.09 V. To improve the gain and NF flatness, base degeneration was adopted using a transmission line, where the length of the line was swept, and the optimal length was included in the design.

3.4.2.2 Input and output matching network

The device was matched to 50 Ω source and load. A broadband match was achieved using a T-matching network formed by two back-to-back L-matching networks [181]. The value of Γ_S was selected at the intersection between the constant gain and NF circle. This provided the best compromise between NF and gain, within stable regions. Using Γ_S, the load reflection coefficient, Γ_L was calculated from which the output impedance Z_{out} was obtained.

Using the transmission line impedance calculator in Cadence *SpectreRF*, the ideal components were converted into their equivalent transmission line *pcells* in *SpectreRF*. The RF blocking inductors were replaced by a quarter wavelength *rfline pcells* while all capacitors were replaced by *pcell* MIM capacitors. The pads were included in the schematic to account for their parasitic effects, as the pads were part of the design. The input and output pad used bondpads *pcells* with the estimated parasitics capacitor of 84 fF. To resonate out this parasitic capacitor, a shunt circuited stub was placed 26 µm away from the pad as it was impractical to place it next to the bondpad. The stub was terminated by a 17 fF capacitor to increase the stub's bandwidth.

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The DC analysis was used to fine-tune the bias point which would have shifted after all on-chip passive were placed. The S-parameter analysis was conducted to extract the linear and noise parameters of the device from 60 to 70 GHz. The next analysis was the harmonic balance (HB) simulation (using QPSS) which was conducted to obtain the device 1dB compression point OP1dB and the third-order output intercept point (OIP3). Matlab was used for the postprocessing of data.

3.4.3 Microelectronic layout

The LNA schematic was converted into the layout in Cadence Virtuoso where the schematic components were mapped to their equivalent layout models. This was done by exclusively using standard BiCMOS *pcells* in the schematic, with the HBT reliability option enabled to increase the current handling of the device. The final layout was created following BiCMOS8HP guidelines to reduce electromagnetic interference (EMI) and comply with the design rule check (DRC). All passives were in the BEOL, except the polysilicon resistors. An MQ-plane was drawn over the design area to ensure common global ground. The supply voltage was routed on a separate layer (M4) to reduce possible EMI.

3.5 SCHEMATIC-EM CO-SIMULATION

3.5.1 Validation of the microelectronic stack used in EM modelling

To ensure the credibility of the result obtained during the EM validation of on-chip layouts, three interpretations of the process stack were compared to establish their accuracy in the performance estimation of the on-chip prototypes [182]. The initial verification of the EM modelling approach is done using a microstrip patch antenna; although not directly related to the radiometer work, it is a conceptually simple one-port test device sensitive to a variety of modelling choices. The PDK provides a Momentum stack-up for their ADS clients labelled “B” in Figure 3.1. The next stack-up was created by compiling data provided in the BiCMOS8HP design manual, (stack “C”). These stack-ups were compared alongside with the BEOL-only stack-up (stack “A”), which omits the PEC termination representing the measurement chuck and a bulk silicon substrate of ε_r =11. In addition, this stack only comprises of one homogenous

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silicon dioxide fill (ε_r = ±4) in the BEOL. Stacks "B" and "C", on the other hand, include PEC termination and the bulk silicon substrate in the FEOL, with a heterogenous SiO_2 dielectric fill across the BEOL of various ε_r values and thicknesses. Where Stack "B" includes a thin layer of SiO2 in the FEOL above the bulk silicon, stack "C" includes a thin nitride layer of ε_r = ± 6.8. The impact of these discrepancies was investigated by prototyping a square patch antenna.

The antenna in Figure 3.2, was designed on the topmost AM metal layer of ±4μm thickness, suspended over the process recommend MQ ground plane (1070 × 938 μm) of ± 2μm thickness. The dielectric height between both layers was approximately 9.6 μm, with an ε_r = ± 4.5. The patch was fed with a microstrip line of width and length of 12.54 μm and 200 μm respectively, which is connected to 100 x 100 μm GSG probe pads with 150 μm pitch.

The GDSII files were imported into Ansys HFSS using the process stacks in Figure 3.1. The three imported files were simulated using the finite element method (FEM) approach with multiple variations listed below:

- Simplification of the via stack connecting top ground plane and the MQ ground
- The effect of the sidewall etch factor
- The choice of the solver (3D FEM and 2.5D Planar solver)
- The consolidated choices

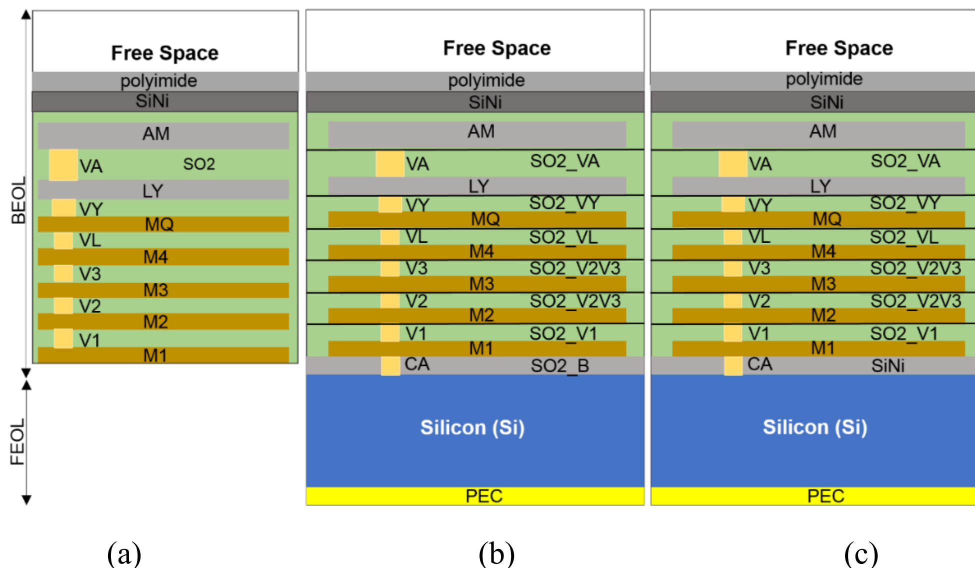

Figure 3.1: BiCMOS8HP Stackups EM simulation, (a) HFSS, (b) stack-up generated from the design manual, and (c) ADS Momentum stack-up.

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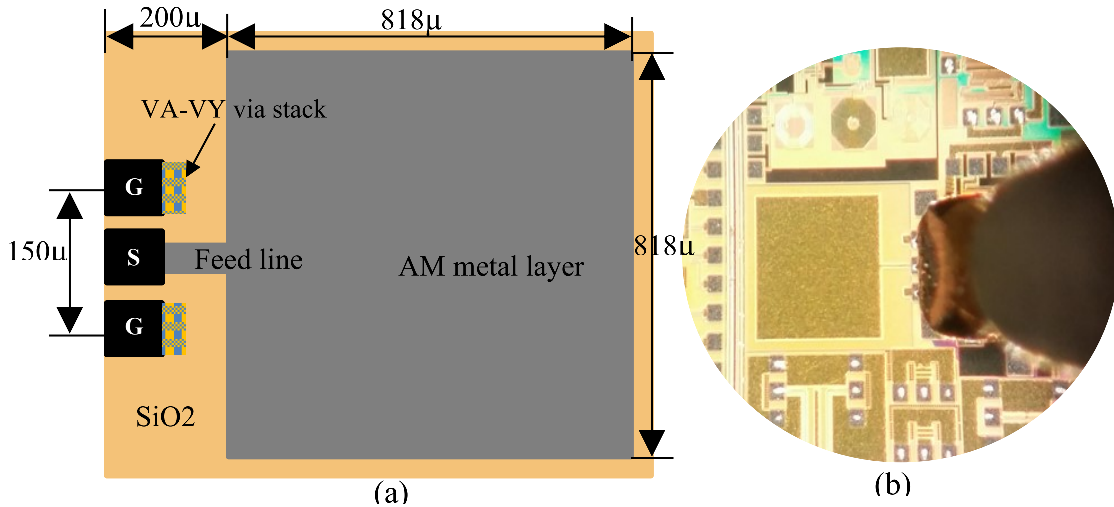

Figure 3.2. 88 GHz patch antenna, (a) design geometry showing dimension, (b) physical antenna under test

A square patch (Figure 3.2a) was initially fabricated in the BEOL and measured as shown in Figure 3.2b. First-tier line-reflect-match (LRM) and second-tier THRU-reflect-line (TRL) de-embedding were used to move the calibration plane to the probe tips, and then to remove the effect of pads parasitics.

The embedded and de-embedded measurements are presented in Figure 3.3. A minor calibration error in $|S_{11}|$ of ± 0.33 dB appeared as a result of a small discrepancy in the definition of THRU and REFLECT standard. Five different dies were measured, and the resulting data is displayed on the same figure, providing a range of measured f_0 between 87.72 to 88.6 GHz. Based on this measurement, f_0 variation of ±2% (1.76 GHz) outside of this range was still considered acceptable, but beyond this value, the simulation was considered inaccurate. The measured $|S_{11}|$ varies from -13.69 dB to -12.12 dB between the embedded and de-embedded measurement results. These measurement results provided a base for validating the stack-ups.

The three stack-ups were compared against the measurement results and are presented in Figure **3.4**. In this figure, the grey dashed lines are de-embedded measurements while the grey solid lines are the embedded measurements. In the same manner, all subsequent dashed lines and solid lines represent simulation results that include both the pads and those that do not, for (red)

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Stack “A”, (blue) Stack “B”, and (purple) Stack “C”. The results from these three 7ML BEOL stack-ups described above, show the following:

1) Significant discrepancies are evident between the simulation with and without pads of the Stack “A”, revealing an f_0 deviation of up to 2.5 and 5.2 GHz respectively. Being outside the measured f_0 range of 1.76 GHz as previously established, Stack “A” was discarded from subsequent simulations.

2) The frequency shift between Stack “B” and “C” is negligible, though Stack “C” is the closest to the measured f_0. This is true with and without pads. This difference reflects the difference in dielectric materials at the top boundary of the FEOL.

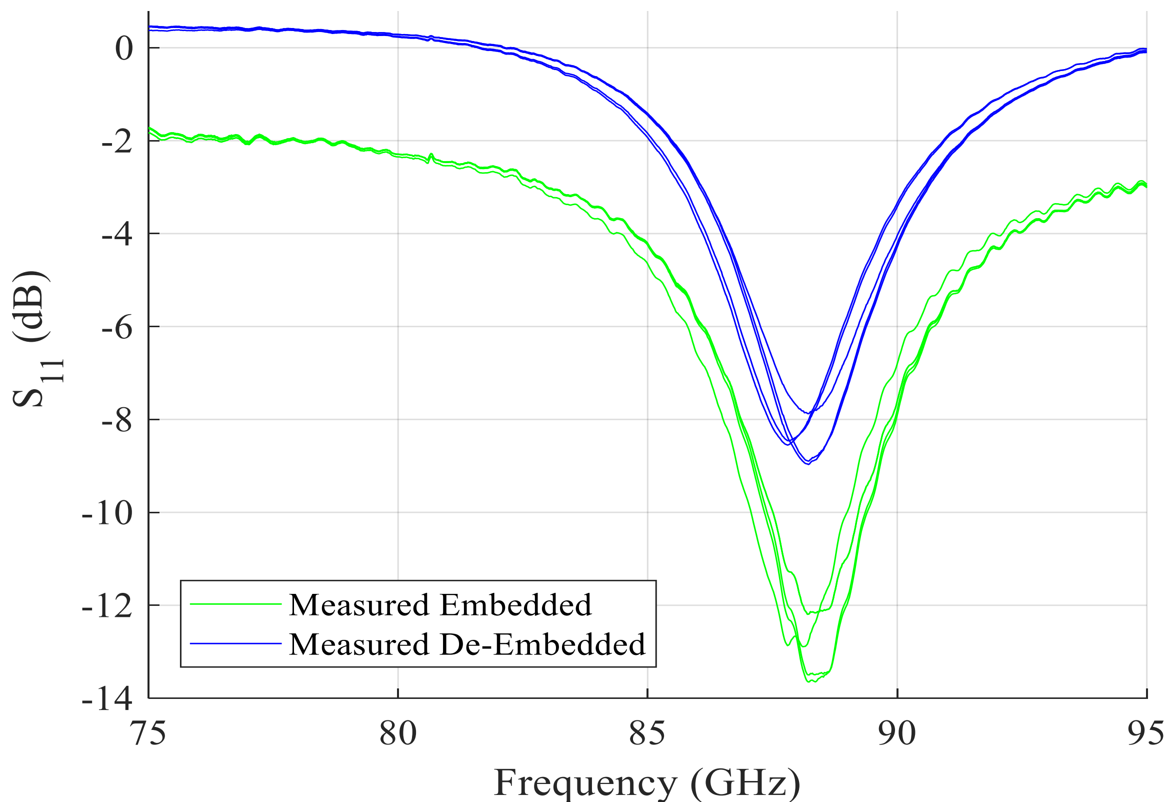

Figure 3.3. 88 GHz on-chip patch antenna measured results.

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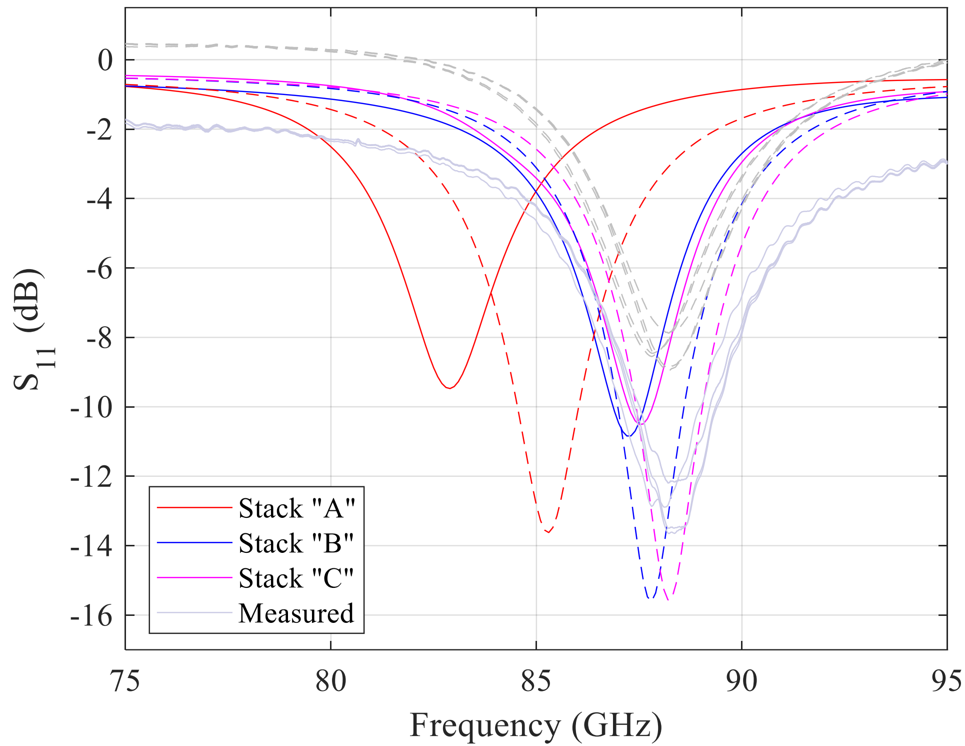

Figure 3.4. Comparison of the stack-ups against the measured data. De-embedded data shown with dashed lines.

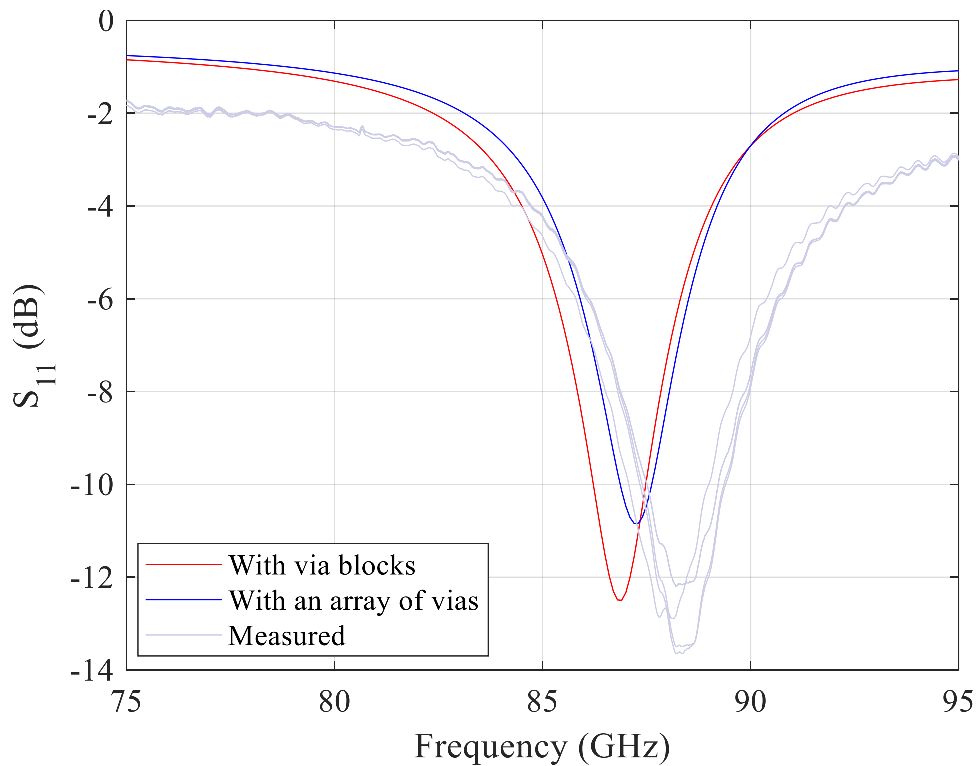

Figure 3.5. Comparison between an array of vias and solid via block.

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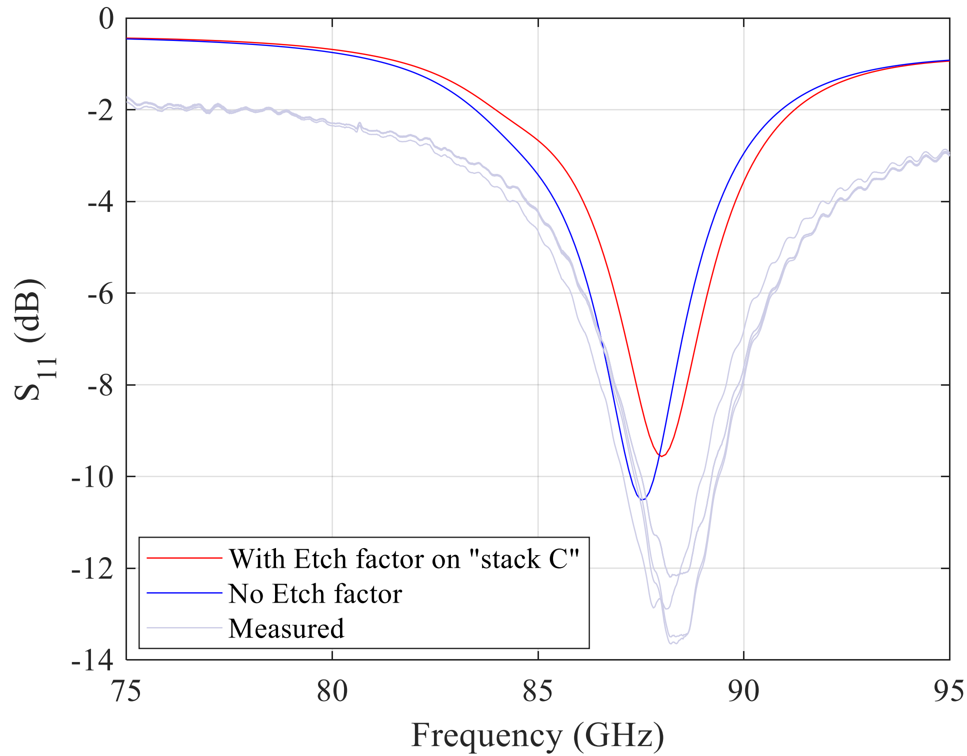

Figure 3.6. The analysis of the impact of the etch factor on the antenna at mm-wave.

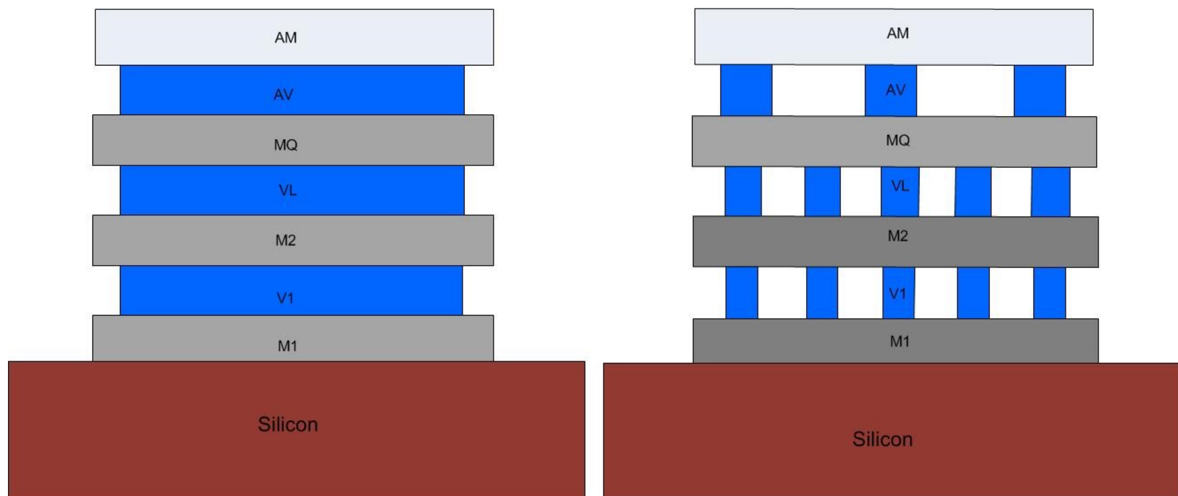

Figure 3.7. Via blocks vs. via arrays

Figure 3.5 represents the results based on the via consolidation simplification from the array to a single via block as illustrated in Figure 3.7. These results suggest a very moderate loss of accuracy in the estimation of either f_0 or $|S_{11}(min)|$. Here, the error in f_0 is increased by 87.3 MHz, while $|S_{11min}|$ = -12.49 dB which is 1.2 dB from embedded measurement results.

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This would indicate a possible change in the characteristic impedance of the feed transmission line as suggested in [183], as a result of the reduction in the effective area of that line. The inclusion of the etch factor did not influence the antenna's response significantly, as shown in Figure 3.6.

To evaluate the relevant solver for mm-wave layout validation FEM and MoM were compared using Stack "C". From Figure 3.8, significant inaccuracy can be seen and was consistent with findings previously reported in [51]. Here, it was found that the 2.5D planar solver was not only inaccurate at these frequencies and process nodes but also required an order of magnitude more processing time [51].

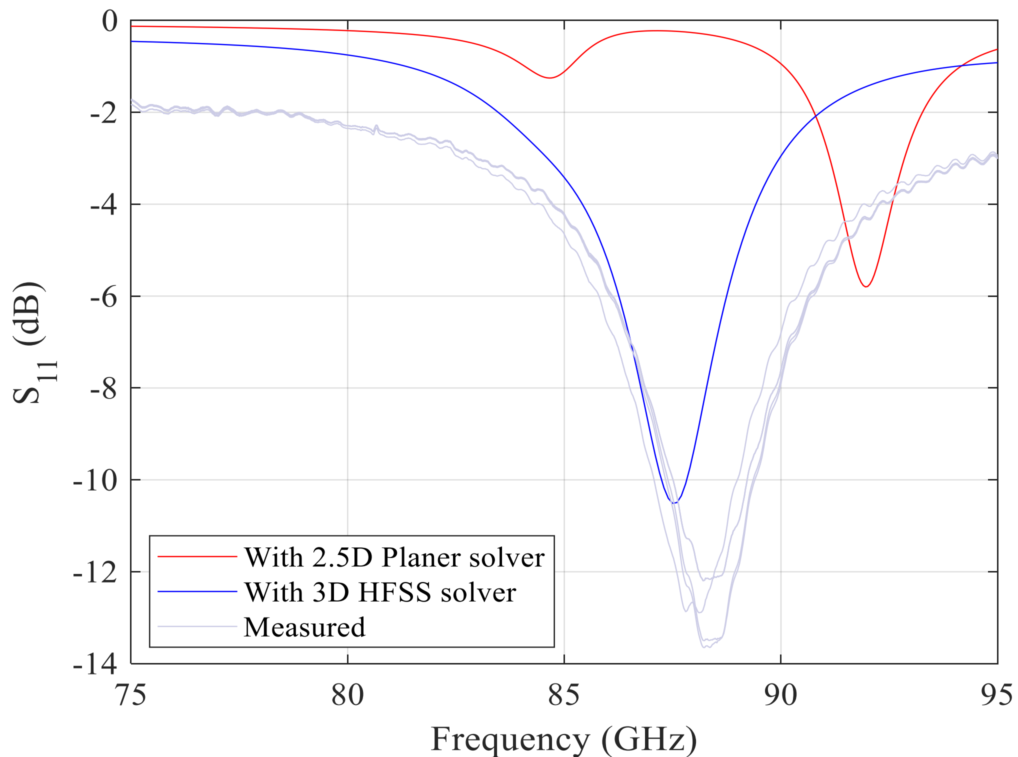

Figure 3.8. Selection of the solver.

With all these established, the best stack-up and simulation setup was used to provide the consolidated graph in Figure 3.9 and 3.10. These depict the minimal difference between the simulated and measured $|S_{11}|$ with ≈1.8 dB error in $|S_{11min}|$ estimation due to a slight underestimation of loss. This approach validated the subsequent 3D FEM validation modelling environment of the 60 -70 GHz mm-wave on-chip LNA.

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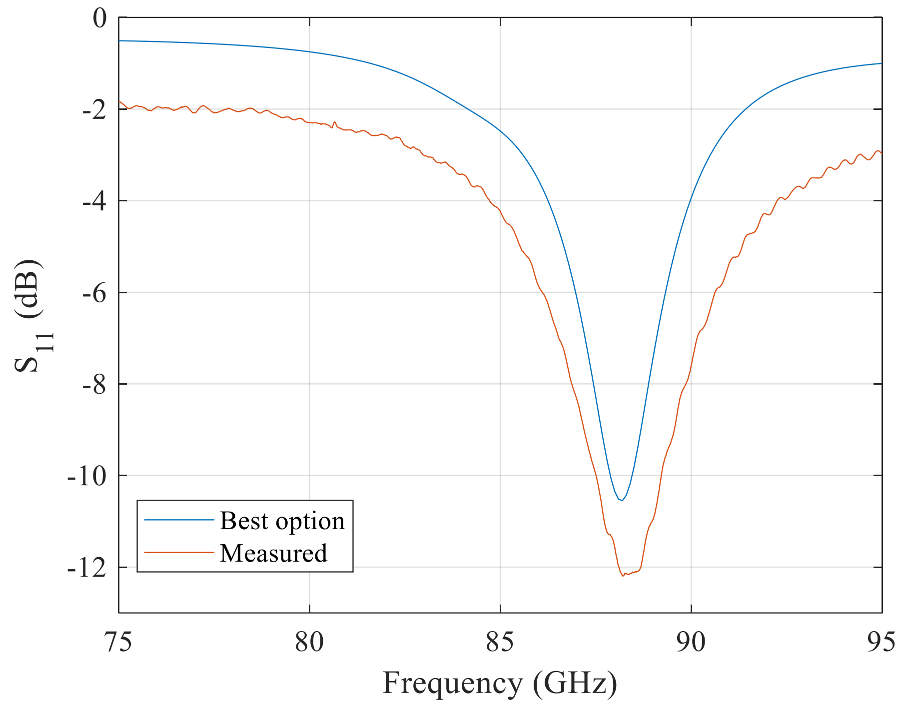

Figure 3.9. HFSS consolidated selection for on-chip 3D FEM validation.

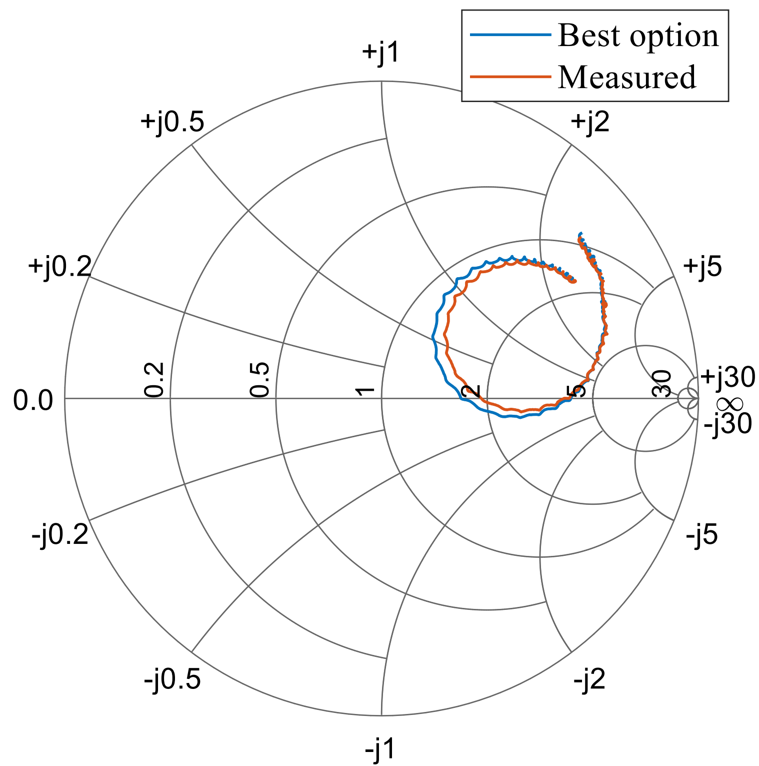

Figure 3.10. Smith chart representation showing insignificant phase difference (Z_0=50Ω).

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3.5.2 LNA layout EM validation

To validate the LNA layout, the GDSII file in Figure 3.11 was imported into Ansys HFSS [51]. Due to the high aspect ratio of the layout (structures ranging from 0.1µm to greater than 100 µm), exacerbated by multiple metals and dielectric layers, EM analysis of the complete layout was impractical as layout features led to extreme mesh ratios and large mesh sizes. To simplify the problem, the layout was divided into small segments and EM-analyzed independently as shown in Figure 3.12 and Figure 3.14. In Figure 3.12 a tee-bend discontinuity is analysed. The transmission line is modelled in a microstrip form where the AM layer was the signal layer and MQ the ground plane. In Figure 3.14, the AM transmission line was connected to the transistor on the M1 layer using vias of different sizes. In this case, one port was placed between the M1 level and to a ground strip used to shield the transistors. All of these ground strips were connected to MQ ground using V1-VY via stacks. The simulation was conducted using the FEM simulation as discussed in Section 3.5.2. The S-parameters were exported and re-imported as *SpectreRF* SnP blocks, and each replacing the original transmission line *pcells*. DC paths in the netlist were provided by bridging the SnP block with a 1nH ideal inductor and the ground pin through a 1pF capacitor as shown in Figure 3.13. Both the S-parameters and the HB analysis were repeated to obtain the linear and NF parameters of the FEM co-simulation as well as its OP1dB respectively.

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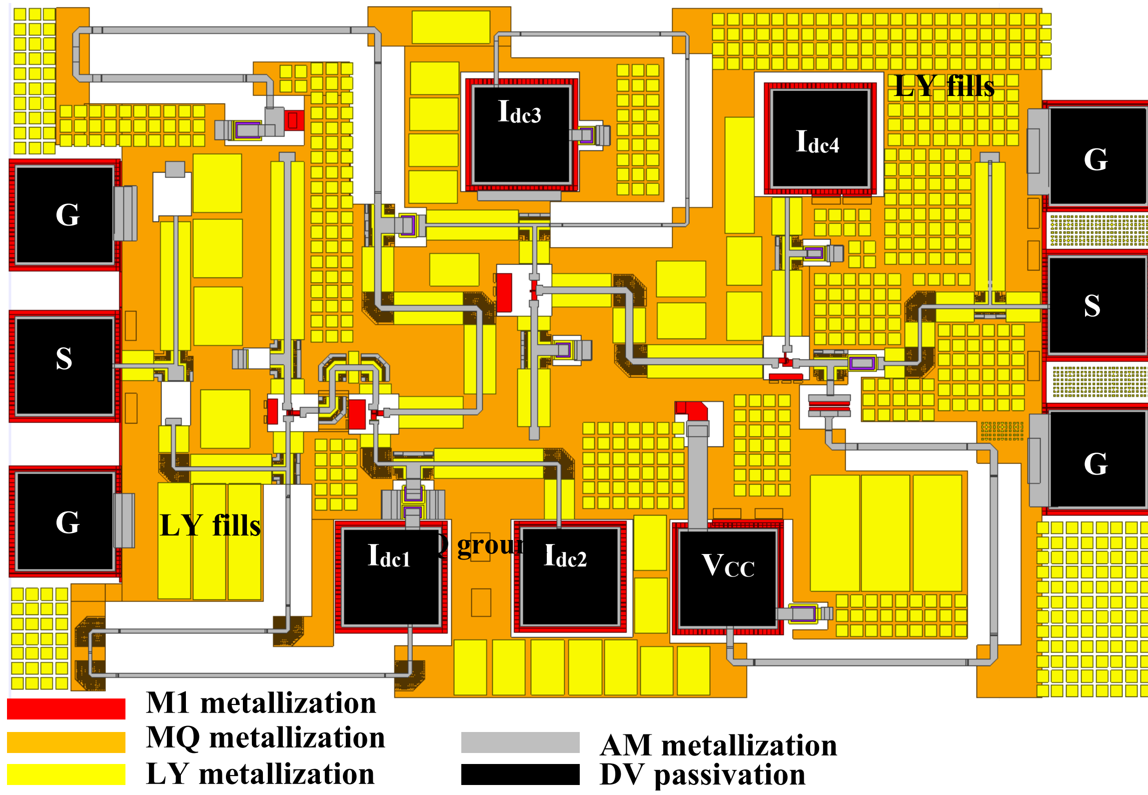

Figure 3.11. Imported GDSII file into HFSS.

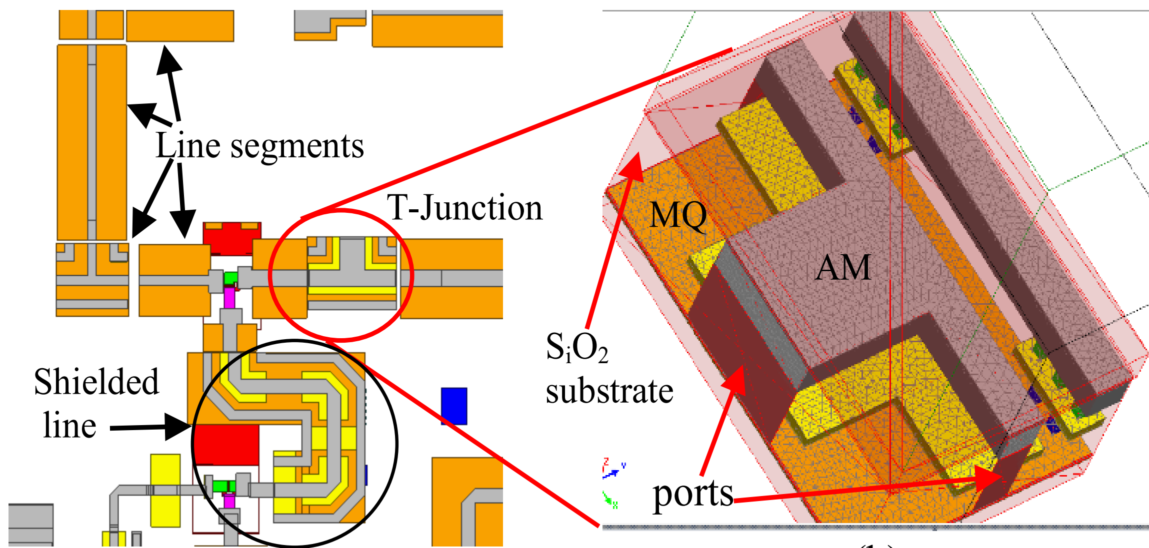

Figure 3.12. Port placement for a transmission line ending at AM layer.

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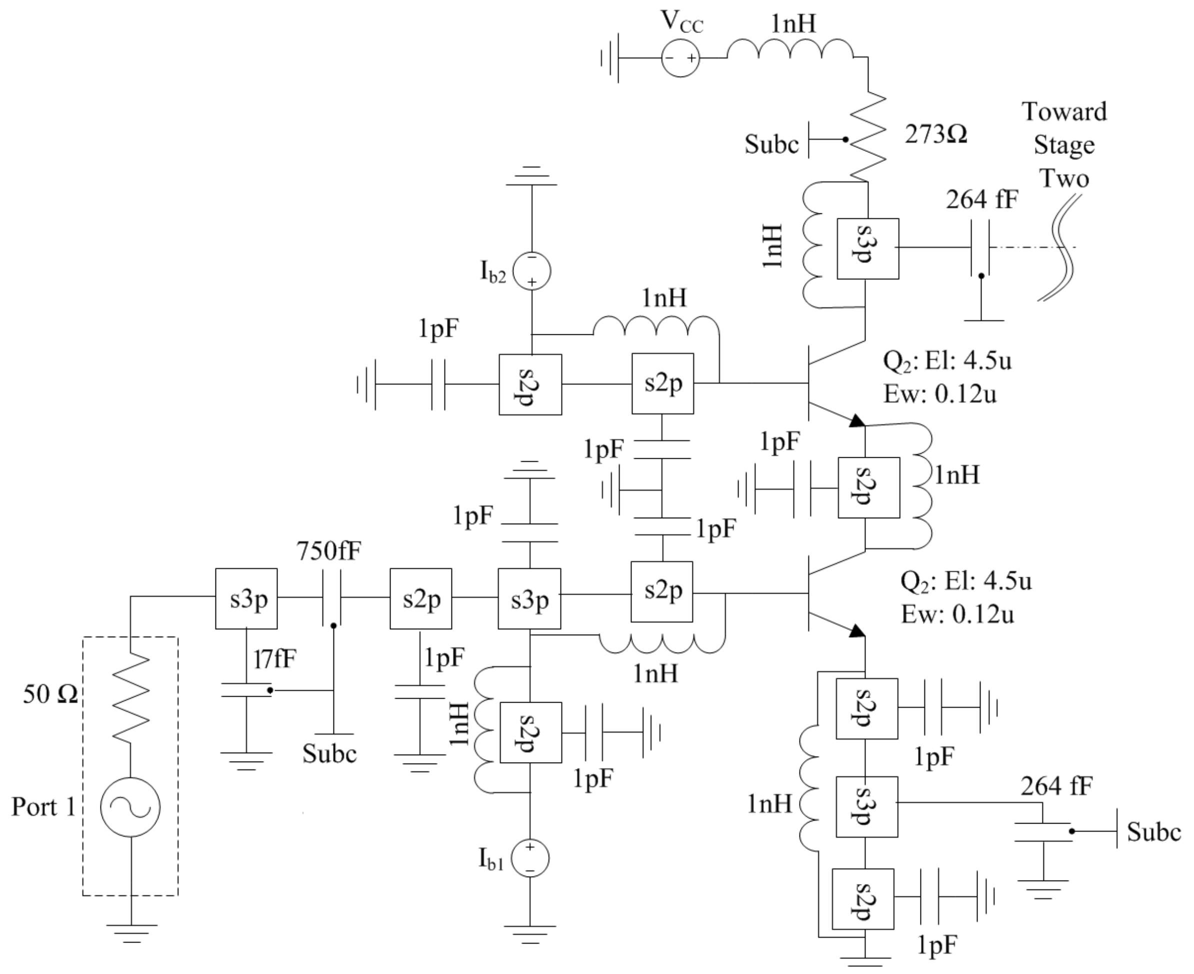

Figure 3.13. S-parameters based schematic diagram.

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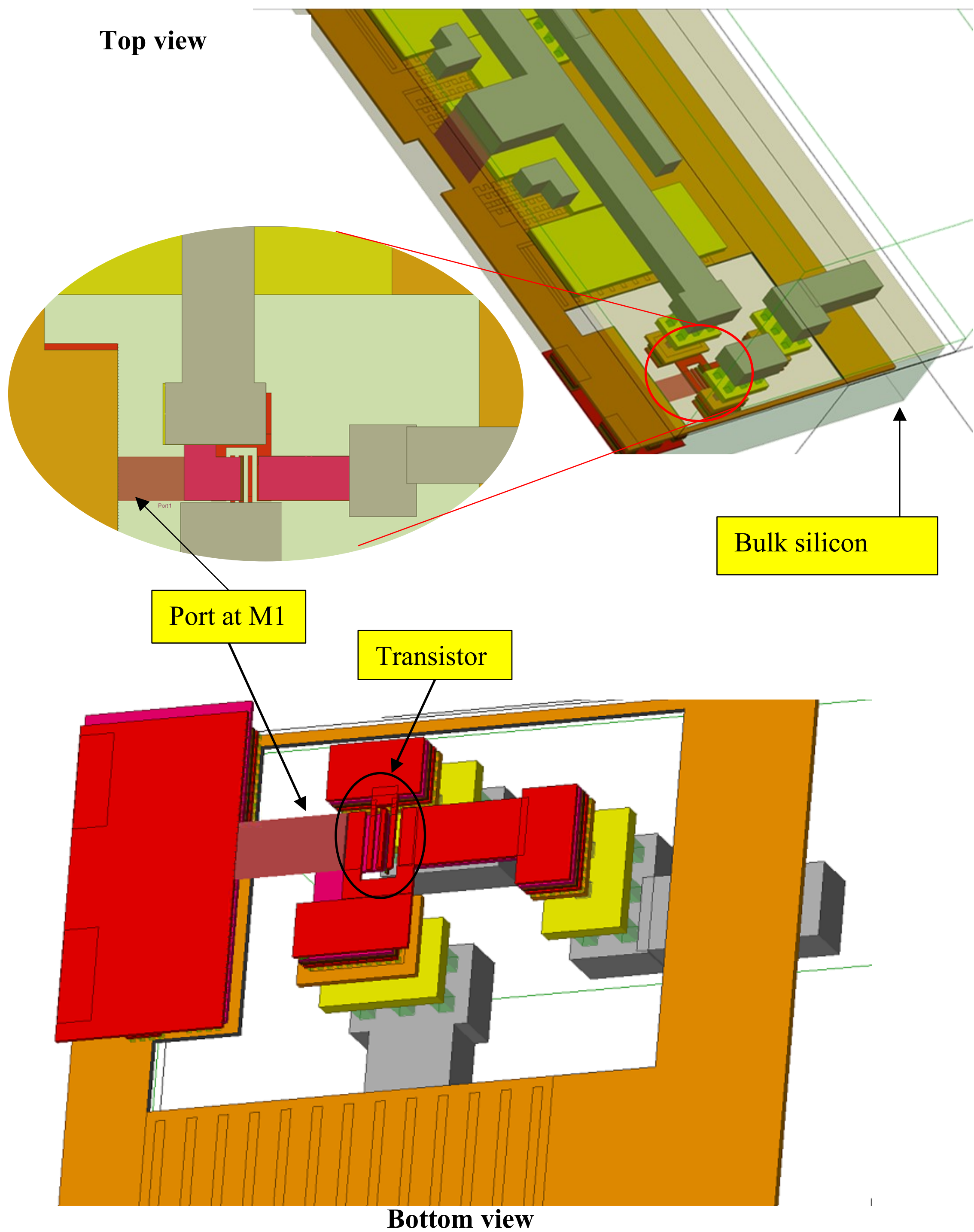

Figure 3.14. Simulation set up from M1 metal layer to AM including vias.

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3.5.3 LNA layout QRC validation

The design rule check (DRC) and the schematic vs. layout (LVS) were conducted to ensure compliance with the foundry rules. Following a successful LVS, RC parasitic extraction (RCPE) was conducted to compare with FEM co-simulation and *pcell* results. The results comparing the *pcell*, RCPE and FEM approaches are presented in Section 4.2.3 since these are compared with MMIC measurement results. The flowchart in Figure 3.15 illustrates the RCPE multiple iteration steps until the required S_{21}, S_{11}, S_{22} and NF were met.

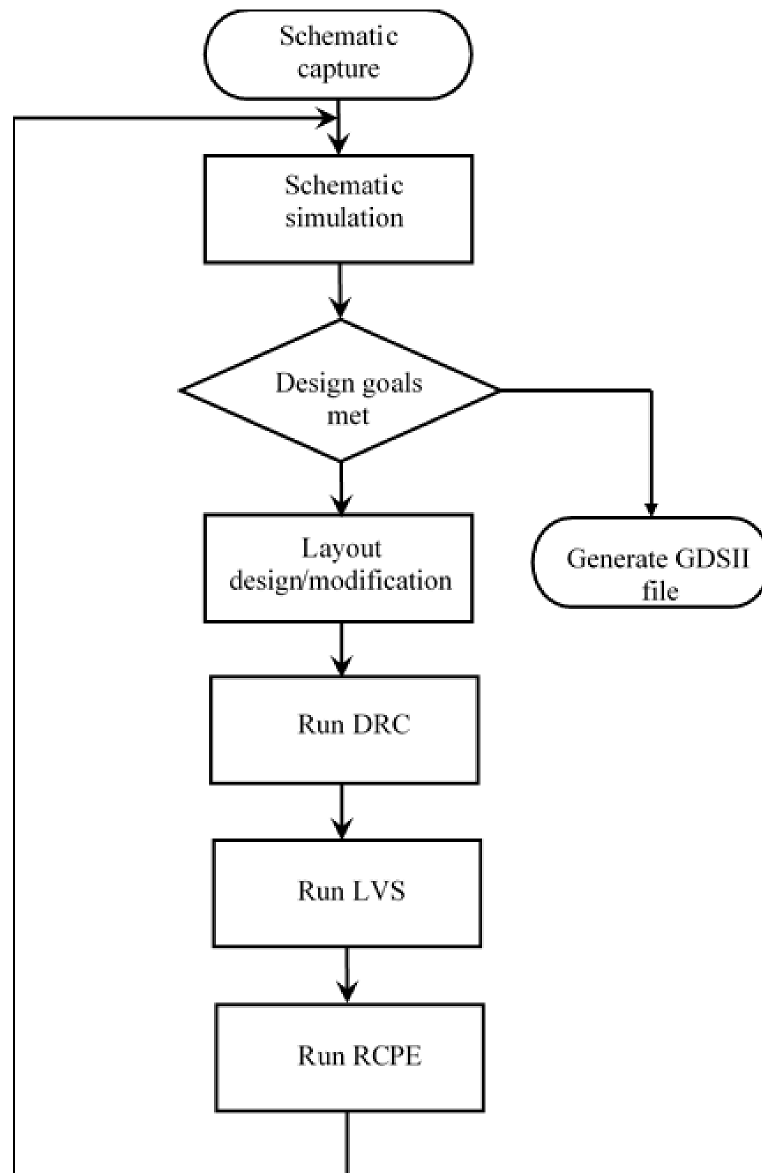

Figure 3.15. Parasitic extraction flow chart.

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3.6 HYBRID LNA

In this section, the approaches that were followed to design the hybrid LNA are discussed.

These include the EM modelling of on-chip transmission lines conducted in HFSS, the transitions between the on-chip transistors and the PCB, the EM modelling of off-chip passives and the LNA design topology and EM-schematic co-design conducted in ADS.

3.6.1 Substrate and interconnect characterisation

3.6.1.1 Interconnect characterisation

To quantify the effect of wirebond interconnections, an EM simulation was conducted in HFSS 3D to characterise three wirebond profiles available in HFSS 3D namely the Low, JEDEC 4-point and JEDEC 5 point as shown in Figure 3.16. The profile in Figure 3.16b was selected for the THRU experiment. The 3D FEM solver was selected to conduct this simulation because of its accuracy in the performance estimation of complex structures.

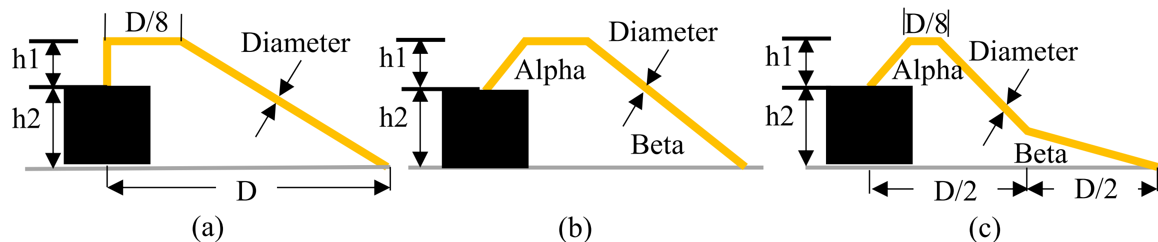

Figure 3.16. HFSS wirebond profiles: a) the low model, b) the JEDEC 4-point model, c) the JEDEC 5-point model.

To characterise the wirebond experimentally, a THRU standard experiment was conducted. Here, a λ/4 length CPW transmission line with 50 Ω characteristic impedance terminated in GSG pads arrangement, was implemented on the BEOL on the AMS C35 process. The transmission line was bonded on XT\Duroid 8100 with a published $\varepsilon_r = 3.38$ and tanδ of 0.0038. To comply with the PCB manufacturer's requirements for fabrication, the centre pad of the GSG pads were reduced to 60 µm to increase the gap on each side of the pad to 70 µm. Two methods were used to characterise the transitions.

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The first approach (direct measurement of the wirebond) was conducted by carefully probing on top of the wirebonds on the on-chip pads, with the other probe on the PCB as indicated in the diagram in Figure 3.17 by the letters R and L'.

The second method was to initially measure the THRU on-chip to obtain its characteristics in isolation. The THRU bonded onto a PCB using wirebond transitions were measured to obtain board-to-board (Figure 3.17 denoted by the letter R and L) measurement data. The wirebond transmission characteristics were obtained by de-embedding the isolated THRU measurement from the board-to-board measurement.

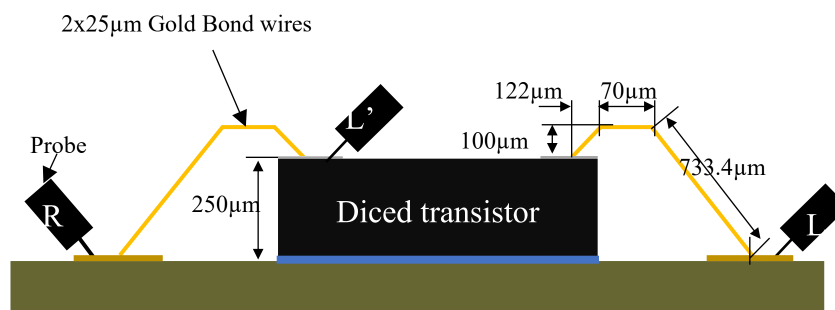

Figure 3.17. THRU experiment PCB layout.

3.6.1.2 Substrate characterisation

To evaluate the effect of surface finishing on the PCB, an end-coupled ring resonator shown in Figure 3.18 was designed and fabricated [184]–[187]. The aim was to extract the permittivity and loss tangent of the XT/Duroid 8100 post-fabrication using the ring resonators with the resonant frequencies at 20, 40, 60, 80 and 100 GHz. The ring resonator parameters and their respective fundamental-mode theoretical resonant frequencies are tabulated in Table 3.1.

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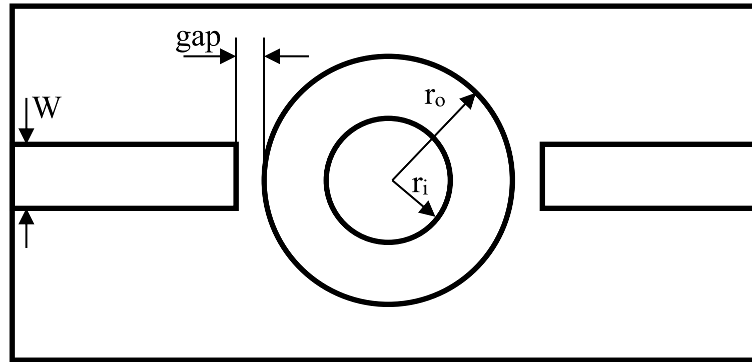

Figure 3.18. The end-coupled ring resonator

Table 3.1. Ring dimensions and respective resonant frequencies

Parameter	Mean Radius (mm)	Gap (mm)	f_0 (GHz)
Ring 1	1.300	1.09	20
Ring 2	0.650	0.547	40
Ring 3	0.433	0.365	60
Ring 4	0.325	0.274	80
Ring 5	0.259	0.219	100

The 50 Ω effective line width of 246 µm was calculated using the ADS line calculator *linCalc*. The effective dielectric constant was therefore calculated from the measured f_0 and the mean ring radius R_m as:

$$\varepsilon_{r,eff} = \left(\frac{nc}{2\pi R_m f_0}\right)^2 \tag{3.1}$$

The loss tangent of the substrate is therefore found as:

$$tan\delta = \frac{\alpha_d c\sqrt{\varepsilon_{eff}}}{\pi f} \times \frac{(\varepsilon_r - 1)}{\varepsilon_r(\varepsilon_{r.eff} - 1)} \tag{3.2}$$

where the expression for calculating the dielectric attenuation α_d is obtained by subtracting the conduction attenuation α_c [188] from total attenuation α [187]. Equation (3.3) was used to extract the unloaded quality factor Q_u, from measured S-parameters.

$$Q_u = \frac{\left(\frac{f_0}{Bw}\right)}{1 - 10^{\frac{S21(f_0)}{20}}} \tag{3.3}$$

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3.6.2 Coupled line PCB capacitors

The coupled line capacitors were designed using the design methods outlined in [189], based on 50 Ω characteristic impedance. The equivalent line width was synthesised using *lineCalc* tool in ADS.

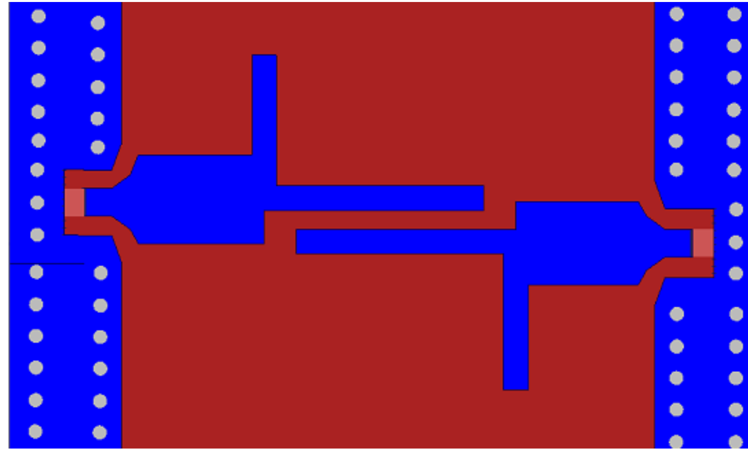

Figure 3.19. The layout of the coupled lines capacitor with open-circuited stubs.

Other PCB capacitors were also studied, such as the gap capacitor in Figure 3.20 and the interdigital capacitor, but the performance was found inferior. This was because the spacing required (10-20 μm) to achieve an effective coupling was much smaller than the capability offered by the PCB manufacturer (minimum 70 μm). A modified version of the gap capacitor in Figure 3.19 was therefore studied and analysed by FEM simulation in HFSS as shown in Figure 3.20, alongside the coupled line previously discussed.

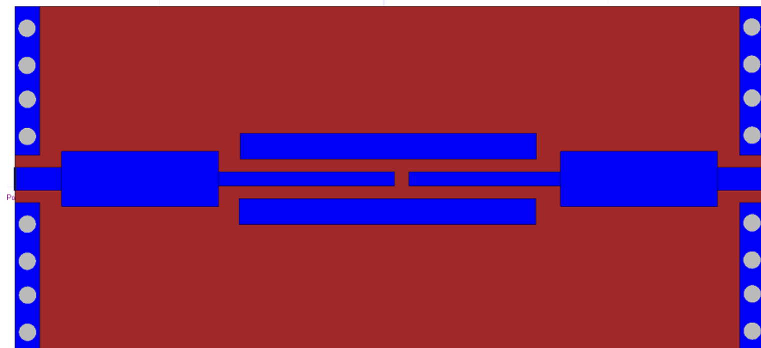

Figure 3.20. PCB layout of m a modified gap capacitor.

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3.7 HYBRID LNA DESIGN PROCEDURE

From the previous section, FEM modelling was conducted on all off-chip passives and transmission lines and was verified experimentally. In this section, the focus is on the approaches employed for the design of the hybrid LNA and how the results of the FEM modelling were used in off-chip layout validation.

3.7.1 Transistor selection

The transistor size ($L_E = 4.5$ μm $W_E = 0.12$ μm) was selected to match the MMIC design for a valid back-to-back comparison. A cascaded single transistor amplifier was therefore adopted for the design of the hybrid LNA due to the layout of the transistor on the die shown in Figure 3.21. The effect of the transmission lines between the transistor situated at M1 and the pad at AM were modelled using FEM simulation using wave ports placed as shown in Figure 3.22. The S-parameters of the transitions and those of on-chip transmission lines were all included in the schematic's solver for co-simulation.

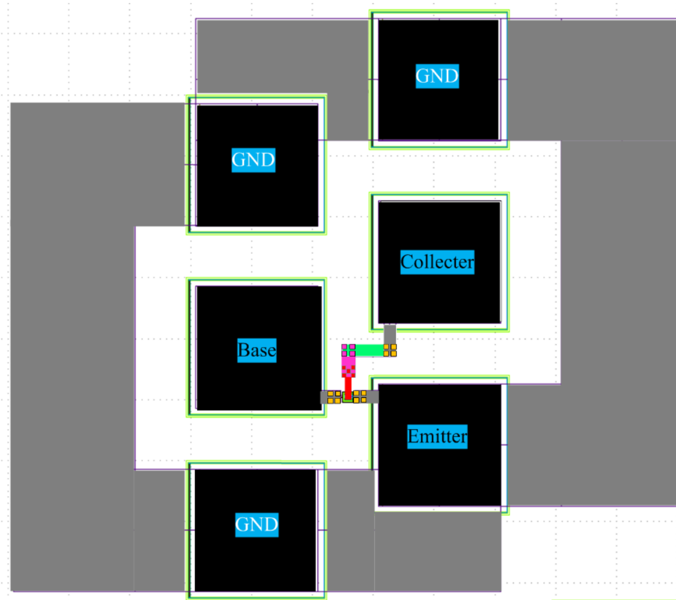

Figure 3.21. BJT transistor fabricated in BiCMOS 8HP process

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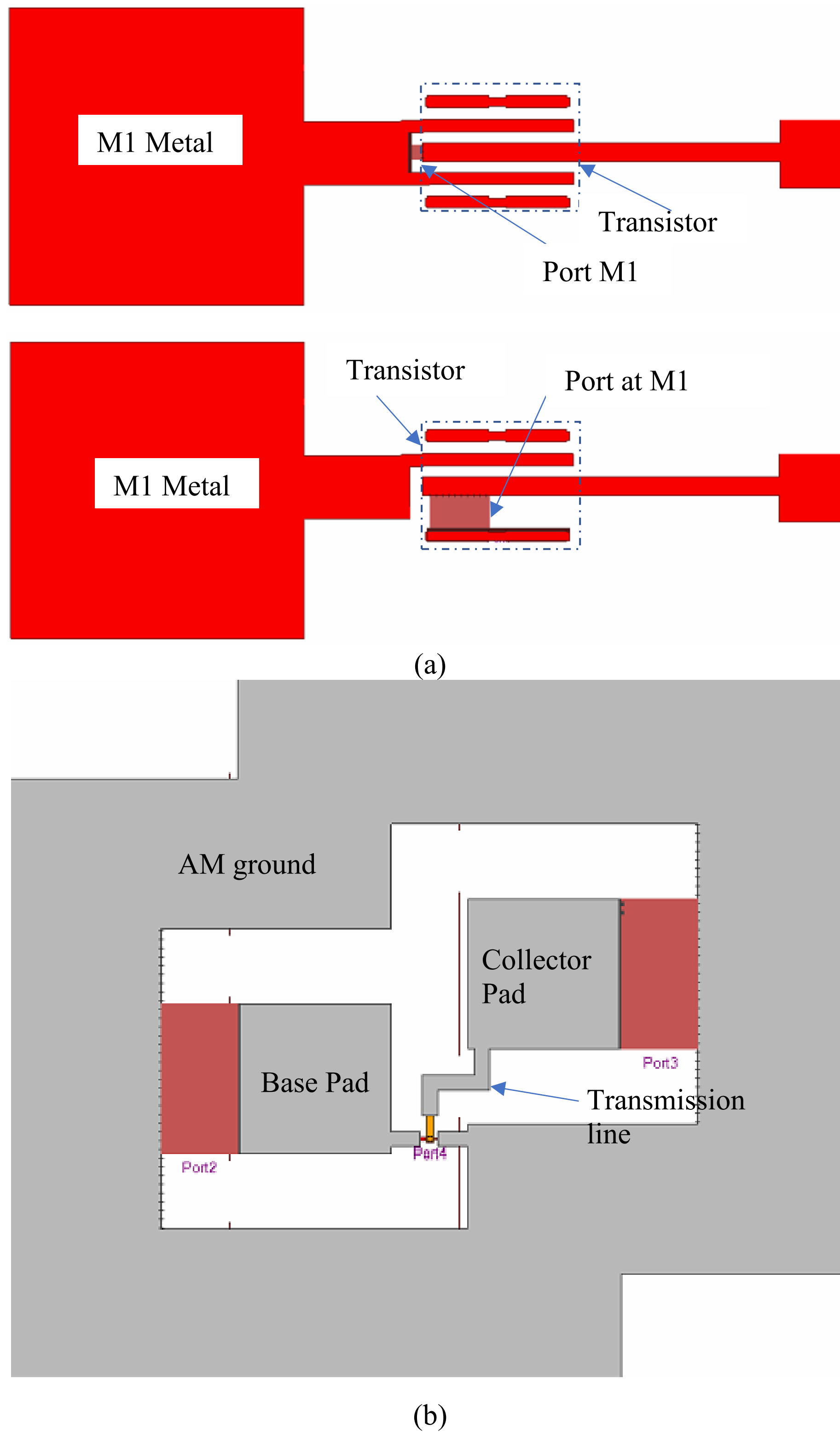

Figure 3.22. On-chip transistor transmission interconnects. a) with ports at M1 metal layer, b) with ports at AM metal layer.

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3.7.2 DC and AC analyses

The Hybrid LNA was designed in ADS using the built-in analogue library and BiCMOS8HP library which was accessed through the PDK file. The use of the BiCMOS PDK was mainly to use the HBT that matched the MMIC transistor.

3.7.2.1 DC analysis

The DC analysis was conducted using Figure 3.23 by sweeping the values of I_B and V_{CE} simultaneously. Here the MMIC transistor includes the measured SnP data of the HBT and 3D EM simulated SnP data of the on-chip transmission lines. This resulted in the Q-point of I_C = 3.9 mA and V_{CE} = 1.1V. This point was selected in the middle of the load-line to provide a symmetrical maximum AC swing at the output of the transistor.

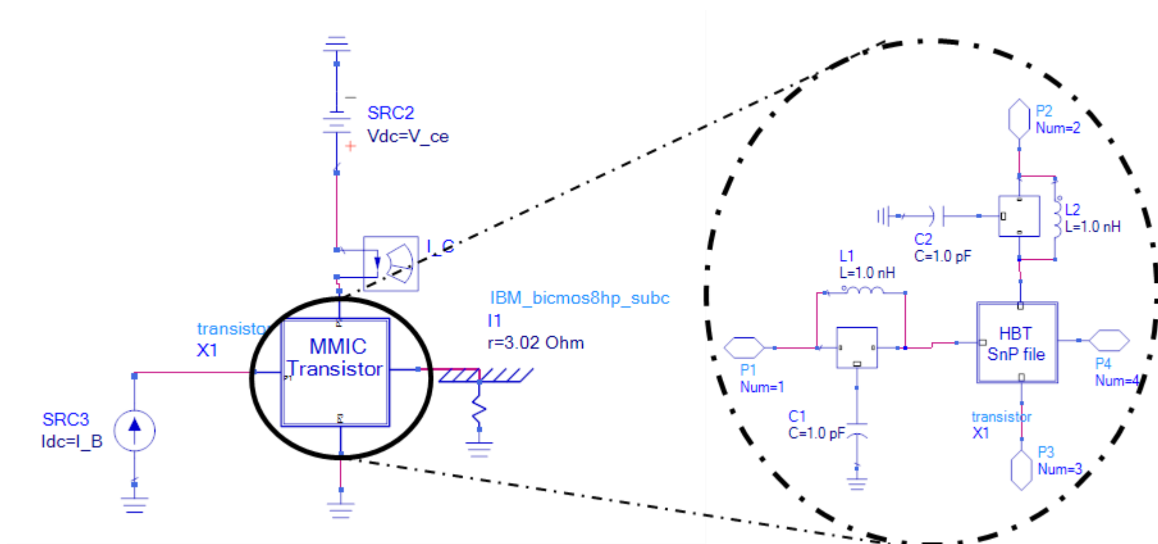

Figure 3.23. DC and AC analysis schematic.

3.7.2.2 AC analysis

The measured SnP file was used in ADS to extract small-signal parameters of the transistor. These parameters were used to analyse both the gain and the NF linearity. Base inductive degeneration was then applied to improve the flatness of both parameters mentioned above.

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3.7.3 Matching network

The HBT model of the transistor was used in ADS and the EM model of the on-chip transmission lines and that of the transitions were included. A combined S-parameters block was then extracted. Using the constant gain LNA design method [189], the Γ_L was selected on the Smith chart for the best possible compromise between the NF and MAG [190]. Using the selected Γ_L, the value of the Γ_S was calculated from which the device was matched using two elements L-matching.

3.7.4 PCB Layout

The schematic components were converted into the layout in ADS using the stackup shown in Figure 3.24 and the transmission lines were EM modelled using FEM in HFSS. The fabrication panel was prepared in layout 3D layout in Ansys Electronic Desktop and the required Gerber files were generated using LinkCad. The stack shows a cavity that was prepared to host the on-chip transistors to minimize the length of the wire-bonds.

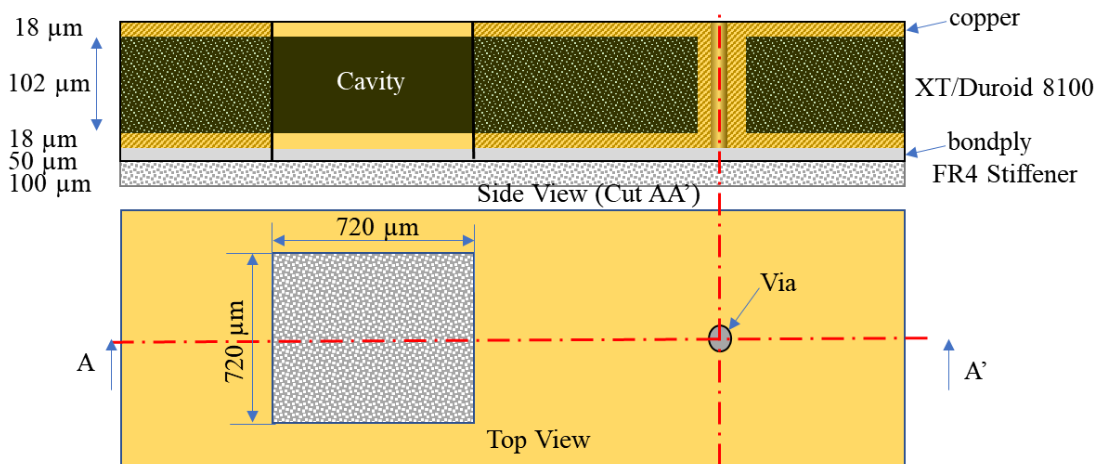

Figure 3.24. PCB stackup for fabrication purposes.

3.7.5 PCB assembly

To assemble the PCB, the transistors were first diced off from the die, using a computer numerical controlled (CNC) process. The diced transistors were then attached to the board using conductive epoxy to provide an electrical connection between the board and the die. The transistors were bonded using the JEDEC 4-point wirebond profile because it offers a shorter

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effective length. All the PCBs were designed to be measured using 110H Picoprobes which requires a pitch of 150 µm.

3.8 LNA MEASUREMENT METHODOLOGY

3.8.1 Probe Calibration

For the on-chip LNA, the probe-tip calibration was conducted on a ME7828A VNA using CS-5 impedance standard substrate (ISS). A single-tier de-embedding was conducted to shift the calibration plane to the probe tips. The second tier, which removes the effect of the pads, was not required because the pads were considered part of the DUT. The de-embedding method used a line standard of length 340 µm, a short-circuit standard as a reflecting standard and a 50 Ω matched load (LRM). For the ring resonators with f_0 above 50 GHz, an LRL calibration method was used with L_1 = 340 µm, L_2 = 1130 µm and the short circuit standard as a reflect standard. The LNA calibrations were conducted at -10 dBm input power, with 1kHz IF bandwidth and 10 points averaging. The measurements were taken over 1001 points between 60 to 70 GHz, at a steady room temperature of 23°C, while the passive measurements were done at a steady room temperature of 21°C with 100 Hz IF bandwidth to improve the VNA dynamic range.

3.8.2 Linear Measurement

The ME7828A VNA was used for the linear measurement with the device biased with an HP 16442A parameter analyser to supply the required base currents. The HMP4040 DC power supply provided the supplied voltage. All grounds were tied together, including grounds from the probe station, to avoid floating grounds. The output currents from the HP 16442A and the supply voltage from HMP4040 DC were supplied through DC needles as shown in Figure 3.25 and Figure 3.26.

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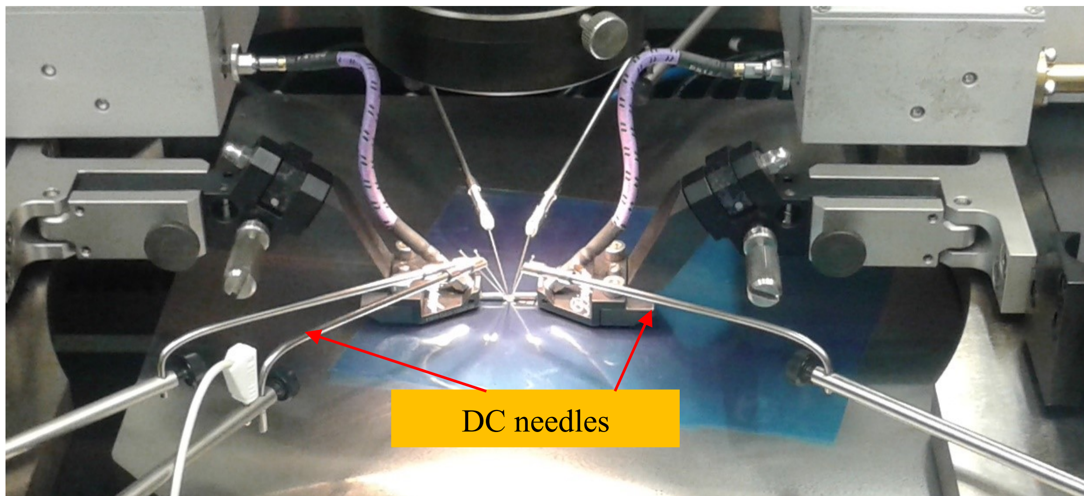

Figure 3.25. LNA under S-parameter measurement.

Figure 3.26. Micrograph of a probed LNA.

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3.8.3 Noise Figure Measurement

The STG-15-S1 low noise block downconverter was used with the R&S FSW50 with K30 measurement option, and an STZ-10-15-I1 noise source with a nominal ENR = 14 dB. The spectrum analyser (SA) was calibrated using a THRU transmission line on-chip. The measurement configuration is shown in Figure 3.27 and Figure 3.28 and shows the measurement process conducted just before the radiation experiment.

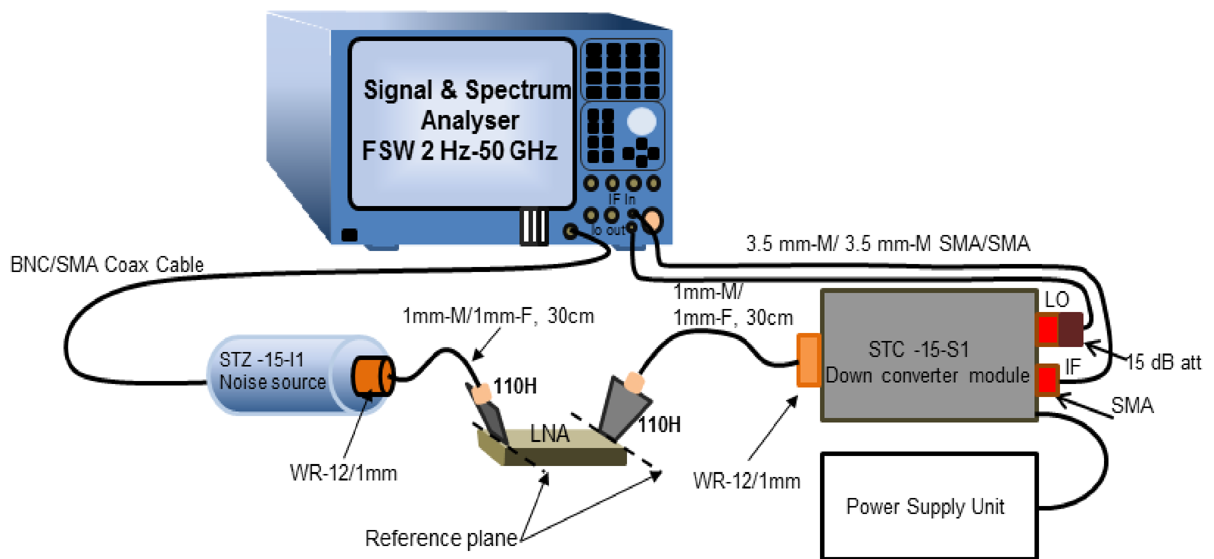

Figure 3.27. Noise figure measurement setup

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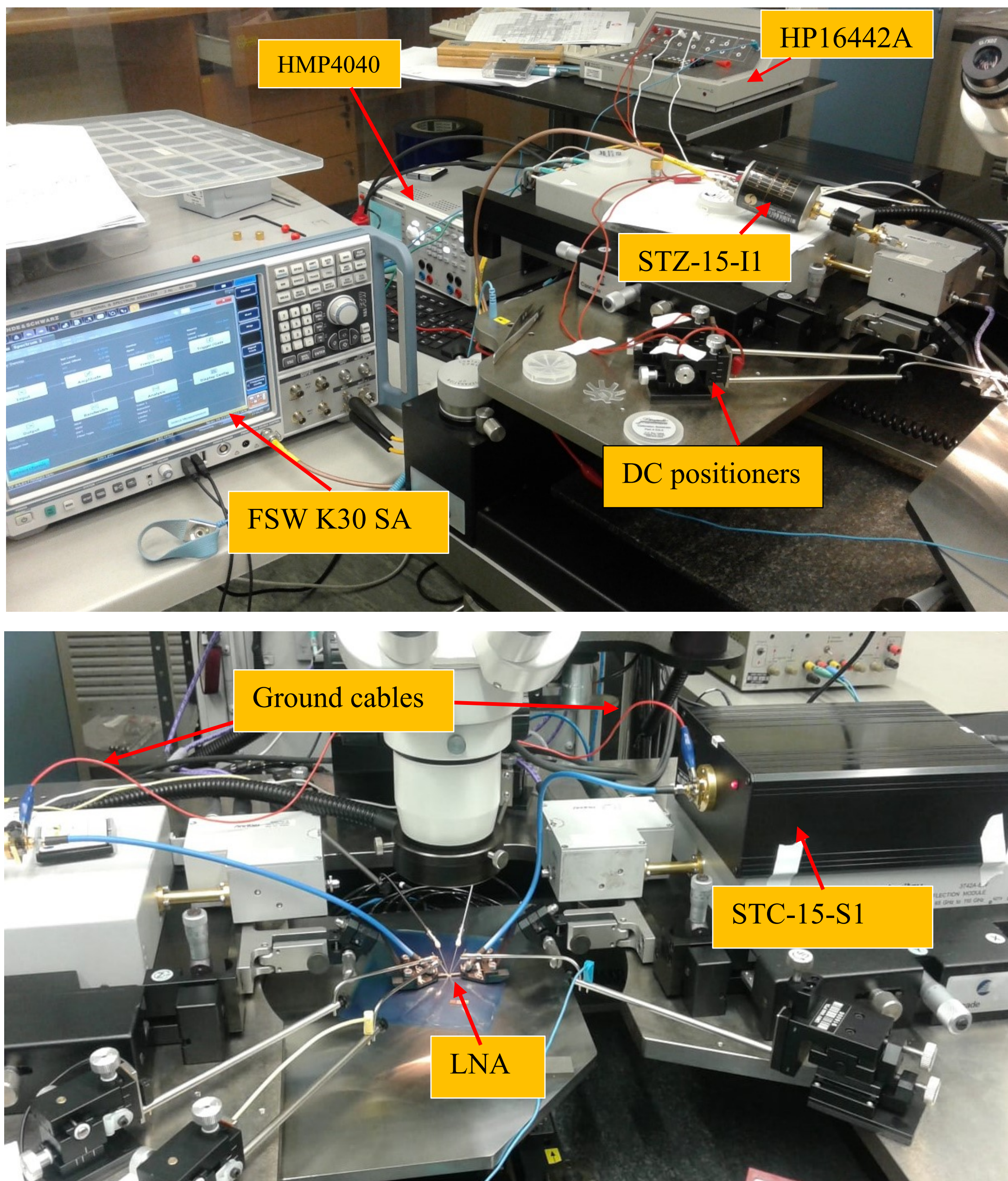

Figure 3.28. Noise Figure measurement.

3.8.4 LNA Radiation Testing

3.8.4.1 Setup description

To conduct the radiation experiment, the radiation probe station in Figure 3.29 was used. The probe was designed using a magnetic material as the base plate, onto which were welded four

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mounting bolts to sustain the radiation disk holder with a thickness of 25 mm. To accommodate the radiation source, the disk holder had one blind hole of ϕ18 mm and 20 mm at the end for which a through-hole of ϕ16 mm was drilled as shown in Figure 3.29. The height between the radiation source and the DUT was adjusted using the heights adjusting nuts. A more detailed description of the probe station, the type of material, and its properties can be found in [191].

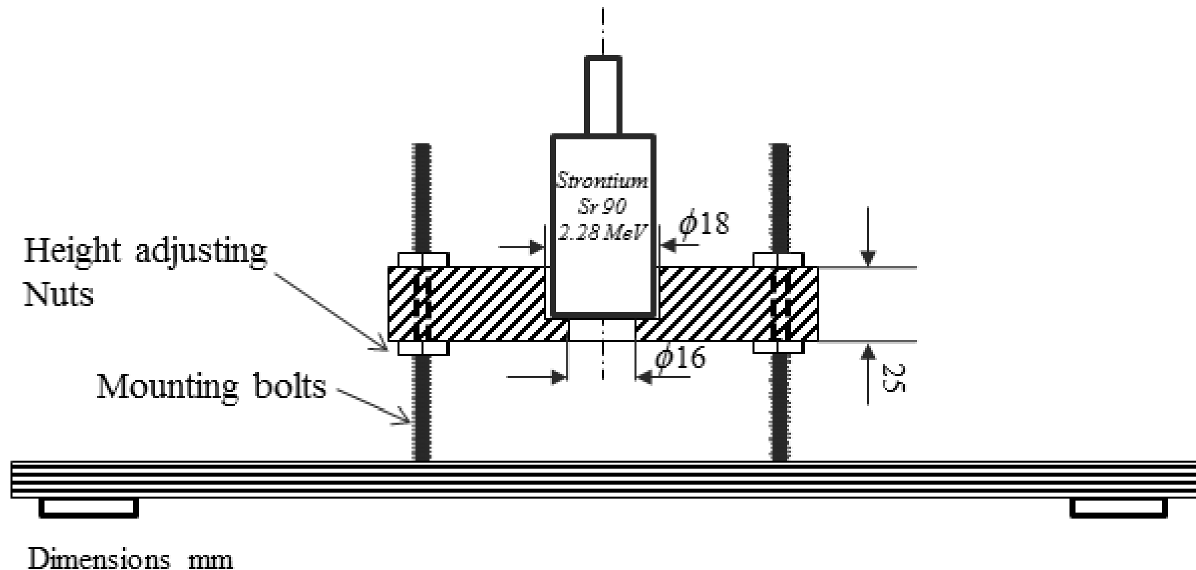

Figure 3.29. Radiation probe.

3.8.4.2 Experiment description

The radiation experiment was conducted in the radiation room in the Physics department at the University of Pretoria, where the facility is equipped with a 2.28 MeV Strontium electron radiation source. Five radiation iterations (1.5, 3.75, 7.5, 11.25 and 15 Mrad) were performed within 72 hrs. The radiation dose rate of 200 krad/(Si) as calculated in [192] was used resulting in the total cumulative dose of 15 Mrad/(Si). The dose rate was measured using GafChromic EBT3 film placed on the radiation station as shown in Figure 3.30. A 10% measured uniformity was achieved over the die area which was 0.4 cm below the radiation source. Once the die was placed on the probe station, a lead brick wall was constructed around the setup and after which the radiation source was placed. The samples were removed from the radiation room after each iteration, the linear and the noise figure measurements were conducted within 1 hr, and the samples were then returned to the radiation room for continued irradiation. In this study, the

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measurements were conducted ex-situ within 1 hour from the removal from the radiation exposure as discussed previously. A similar method was adopted in [193], but devices were only measured a few weeks after. Meanwhile, an in-situ approach was used in [162]. All these methods resulted in similar observations as far as the transistor parameters variations are concerned. Compared to [162], the method used in this study provides moderate complexity and the procedure is straightforward.

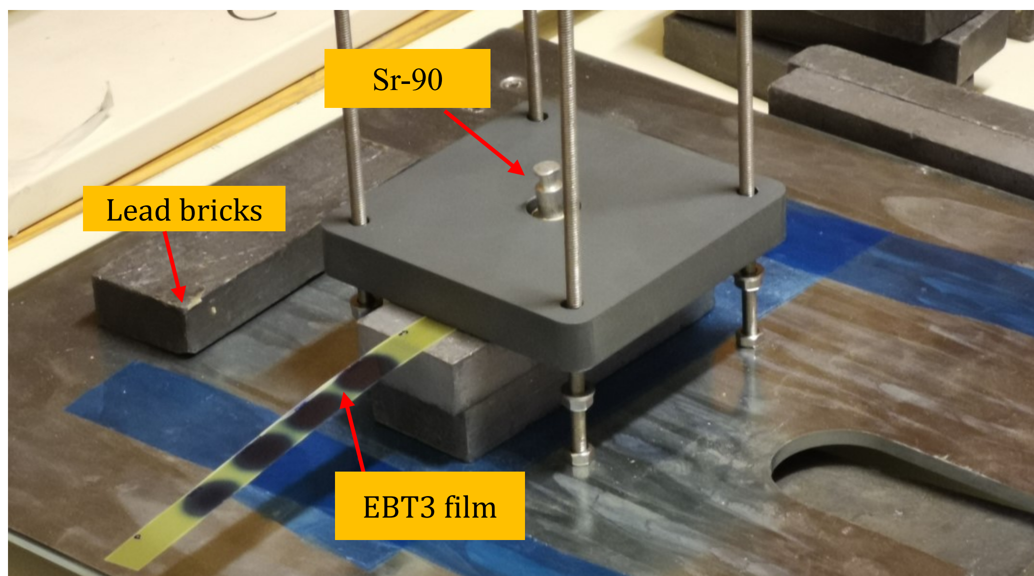

Figure 3.30. TID electron radiation setup.

3.9 SUMMARY

This chapter detailed the procedures used in this research study. In the first part of the work, a component survey was conducted in combination with the modelling of the receiver architecture in AWR VSS using both time-domain analysis and RF budget simulator engines, to identify mm-wave COTS components. The LNA was subsequently identified as a custom design requirement leading to the rest of the inquiry.

The LNA schematic was designed mostly in Cadence Virtuoso (RFspectre) where the DC, the S-parameters and the harmonic balance simulations were conducted to obtain the device performances. The layout generated was subjected to QRC for RC parasitic extraction and EM validation with FEM. This was done to investigate the effect of on-chip parasitics on LNAs at mm-wave using SOTA methods.

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The hybrid LNA used transistors bonded onto XT/Duroid 8100 soft substrate. The transmission lines leading to the on-chip transistors were modelled in 3D layout in AED and the S-parameters were used in ADS for co-simulation. The wirebond interconnects and all transmission lines in the schematic were also modelled in 3D layout and likewise incorporated in the schematic in ADS to account for their effects.

It is also shown how FEM was selected in favour of RCPE and MoM, as the preferred full-wave EM solver for this study. The steps followed to select an appropriate FEM representation of the 8HP process was also detailed and were novel contributions to the SOTA of MMIC EM design [51], [182].

The on-chip LNA was subjected to TID electron radiation where it was irradiated up to 15 Mrad/(Si) over 72 hrs. The device was measured for its linear and noise figure performance before and after the TID experiment using Anritsu ME7828A VNA and FSW50 measuring devices respectively.

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CHAPTER 4 MICROELECTRONIC LNA DESIGN

"No one wants to learn by mistakes, but we cannot learn enough from successes to go beyond the state of the art". *-Henry Petroski*

4.1 INTRODUCTION

This chapter presents the detailed design and measurement results of the V-band on-chip LNA fabricated in 130 nm SiGe BiCMOS. The EM validation of the LNA layout was conducted using FEM simulation. This was preceded by the validation of 7 metal layer microelectronics stack-ups presented in Section 3.5.1 and reported in [182]. The layout validation using RC parasitics extraction are also presented, along with a comparison with the aforementioned FEM simulations and measurements [51]. The chapter concludes with the experimental characterization of the TID radiation tolerance of the V-band SiGe LNA under electron radiation [67]. In this chapter, the design adopts the SOTA technique in [61], [180], to investigate the impact of RC parasitic and TID electron radiation on MMIC V-band LNAs, which are both novel contributions to the SOTA.

4.1.1 LNA DC analysis

To set the required collector current for the defined transistor dimension of 4.5/0.12 µm (the size of the transistor was selected for an optimum noise), the BiCMOS design manual recommends a current density limit for an NPN HBT of 15 mA/µm^2. The DC analysis was conducted based on Figure 4.1 using the PDK models to trace the I-V curve in Figure 4.2 from which the transistor's operational point (Q-point) was selected.

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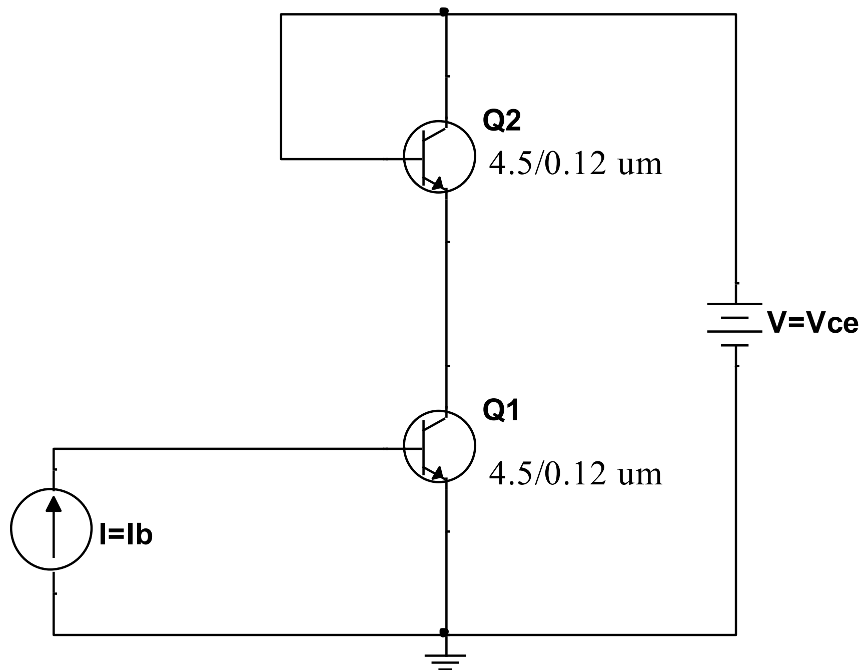

Figure 4.1. Schematic configuration for evaluating the DC operating point.

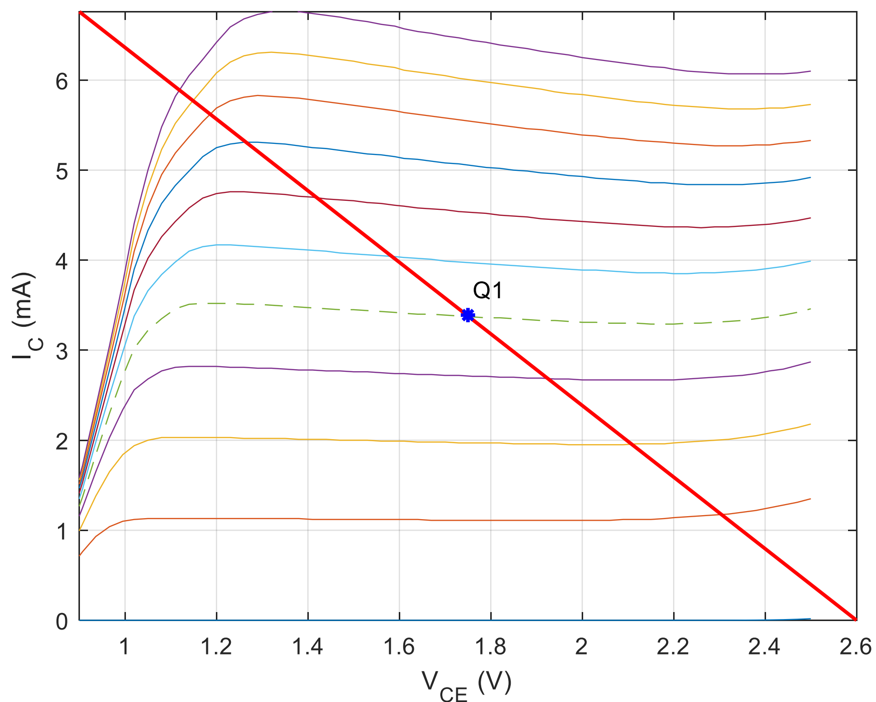

Figure 4.2. I-V curve of the cascode configuration.

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4.1.2 AC analysis

To extract the S-parameters and the small-signal hybrid model parameters of the HBT, the bias-tee configuration in Figure 4.3 was used to construct the AC-analysis in Cadence *SpectreRF* with the base currents as indicated to force I_C = 3.75 mA as per the first point (Q1-point). The transistors size of 4.5/0.12 µm was selected for an optimum noise figure as shown in Figure 4.4, which also depicts the stability factor *K*, noise resistor r_n, and the available gain. This was achieved by fine-tuning the bias point in *SpectreRF* which shifted the point to the second operation point (Q2-point) as indicated on the I-V curve in Figure 4.5. Using this point, the device's small-signal parameters were then extracted as shown in Table 4.1 to calculate the voltage gain of the device. To derive this, Figure 4.6 was used to evaluate the networks' voltage gain using constant base current biasing and the voltage divider biasing. The network in Figure 4.6(a) yielded the voltage again ($|A_v|$) of 9.16 dB using (4.1) and in Figure 4.6(b), $|A_v|$ = 14.83 dB using (4.2), for the voltage divider network and the constant base current bias, respectively. Based on these findings, a constant base current bias was adopted for the rest of the study, as it offered more gain than the voltage divider approach. Furthermore, it allowed for post-fabrication tunability, which is not possible with the voltage diver approach.

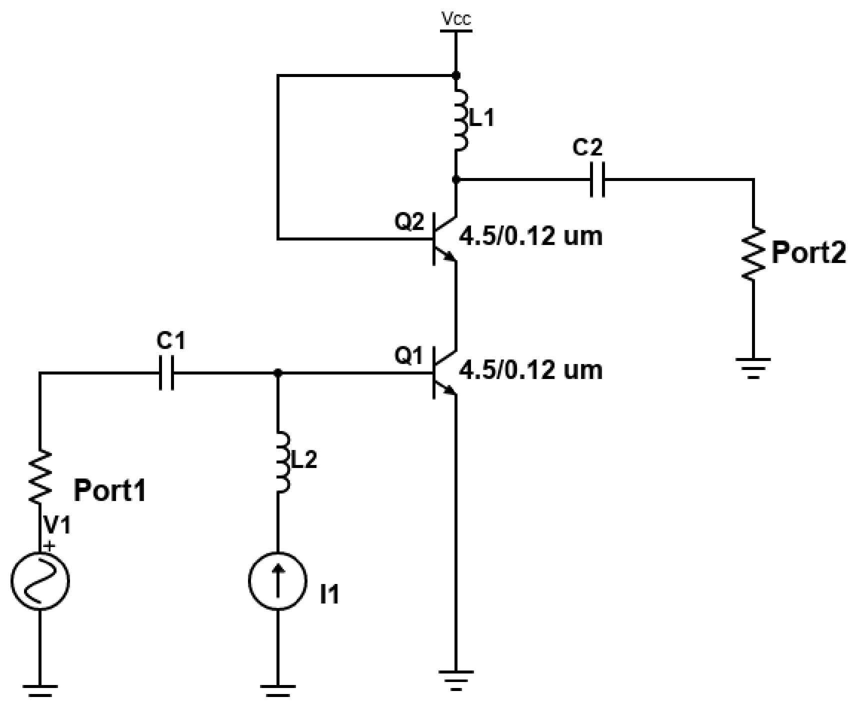

Figure 4.3. AC schematic configuration.

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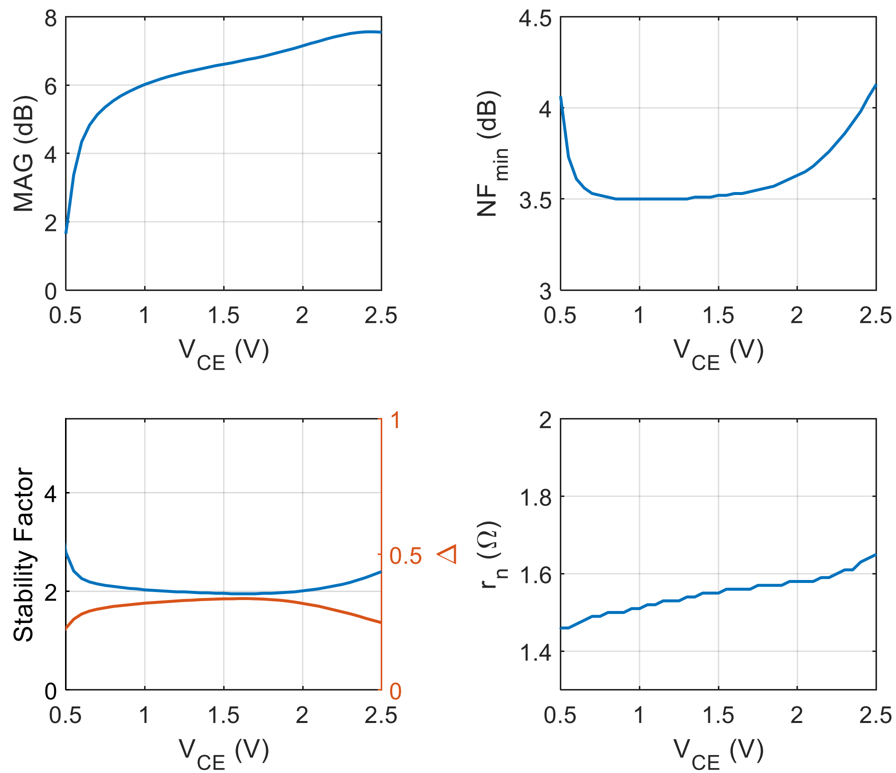

Figure 4.4. Unmatched transistor parameters of the first stage: The first quadrant is the maximum available gain, the second is noise figure, the third is the stability parameters, and the last is the normalised noise resistor.

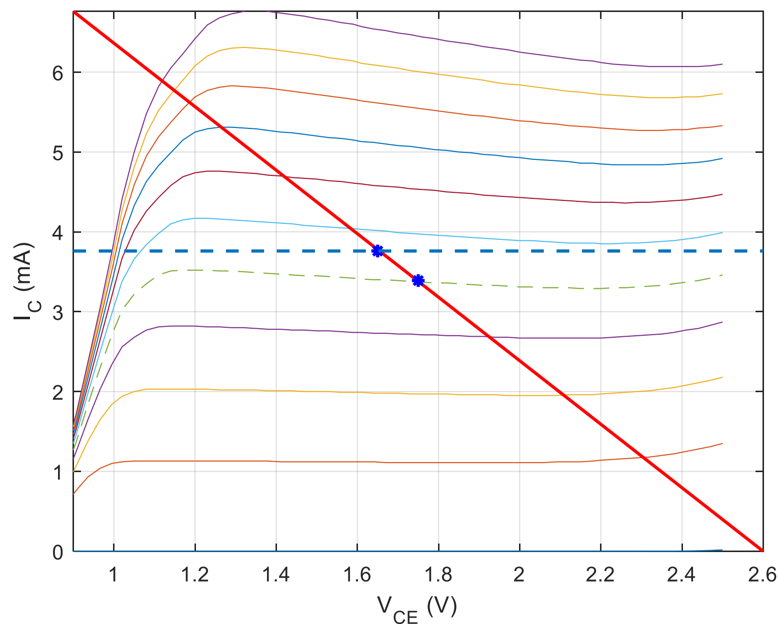

Figure 4.5. Adjusted bias point.

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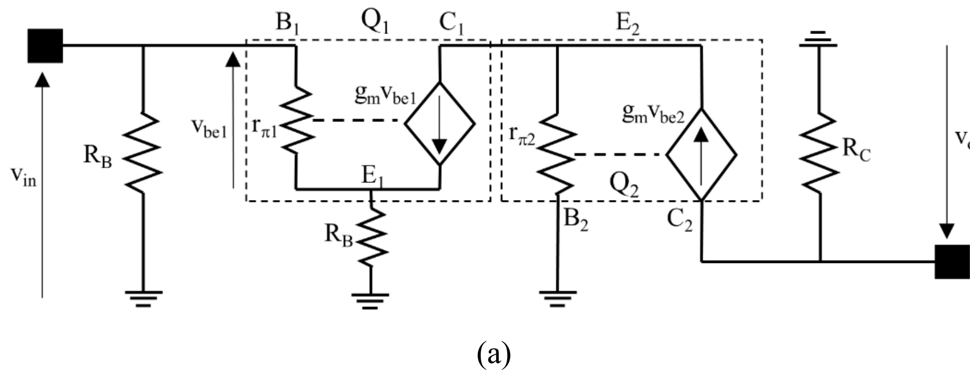
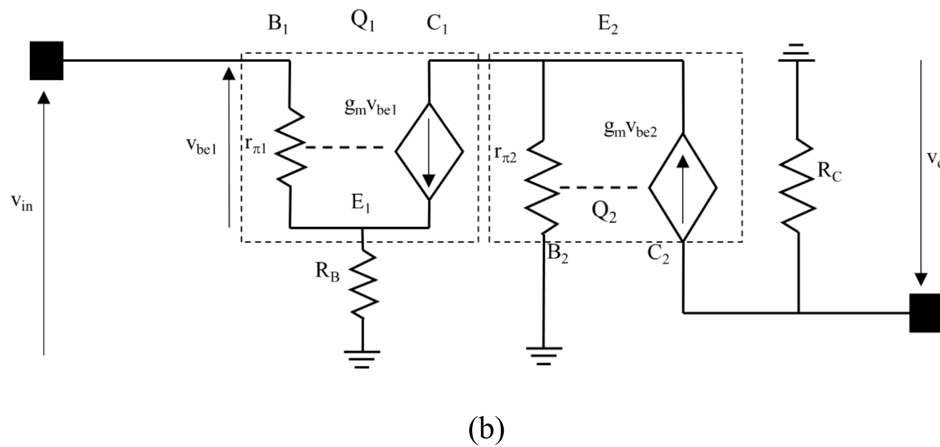
Table 4.1. Small signal parameters vs the bias voltages.

Parameters	r_π (kΩ)	C_π (fF)	C_{be} (fF)	C_μ (fF)	g_m (mA/V)	Beta	f_T (GHz)	V_{BE} (mV)	V_{CE} (mV)
Q1	49.8	62.6	82.65	6.30	125	269.7	192	864	1.93
Q2	57	122	133	12	133	241	120	892	363



(a)



(b)

Figure 4.6. Cascode small-signal model, a) for constant base current biasing, b) for a voltage divider resistive biasing.

$$|A_V|_{dB} = 20 \times log\left[-g_m \frac{(R_c \times R_L)}{R_c + R_L} \times \frac{r_{\pi 1}}{r_{\pi 1} + R_E}\right]_{R_E \ll r_{\pi 1}} \tag{4.1}$$

$$|A_V|_{dB} = 20 \times log\left[-g_m \frac{(R_c \times R_L)}{R_c + R_L} \times \frac{r_{\pi 1}||R_B}{r_{\pi 1}||(R_B + R_E)}\right]_{R_E \ll r_{\pi 1}} \tag{4.2}$$

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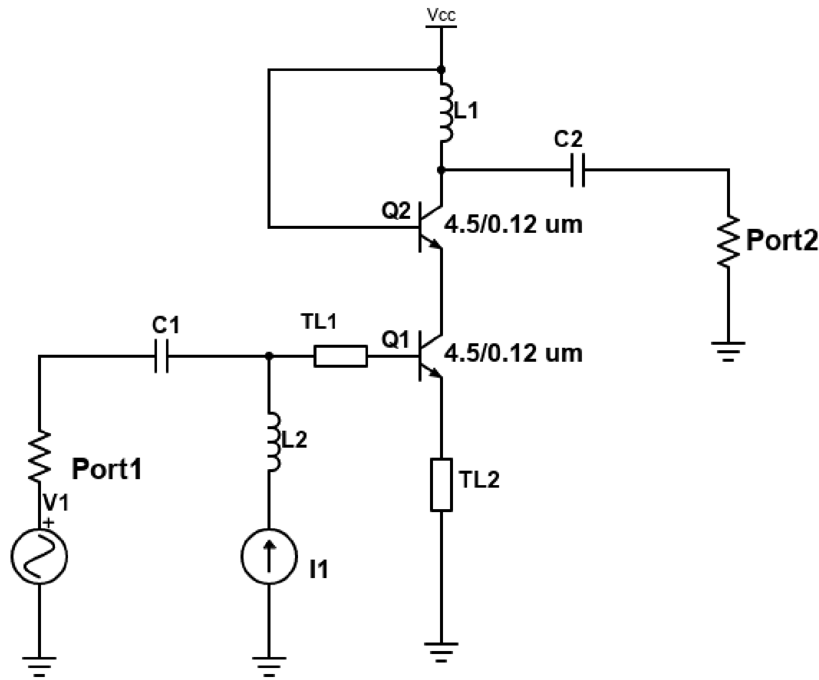

Figure 4.7. Base and Emitter degeneration.

To improve the gain and noise figure flatness, base degeneration shown in Figure 4.7 was employed where the length of the transmission line (TL1) was swept, resulting in the analysis in Figure 4.8. The optimum length of 99 µm was selected and was included in the final schematic diagram. A noise matching transmission line of 30 µm was inserted between the cascode transistors in the final schematic diagram in Figure 4.11, while an optimized transmission line (TL2) length of $\lambda/8$ was used as inductive degeneration at the emitter [61] to improve the stability and noise figure. The first step was to extract the S-parameters shown in Table 4.2. From these parameters the maximum available gain of 7.38 dB was extracted for the collector current of 4.32 mA when supplied by 2.3 V., This resulted in DC power consumption of ± 10 mW per stage, thus a total DC power of ± 20 mW. The stability parameters at f_0 are $|\Delta|$=0.285, K=2.527 and μ=1.470, all of which satisfy the criteria for unconditional stability.

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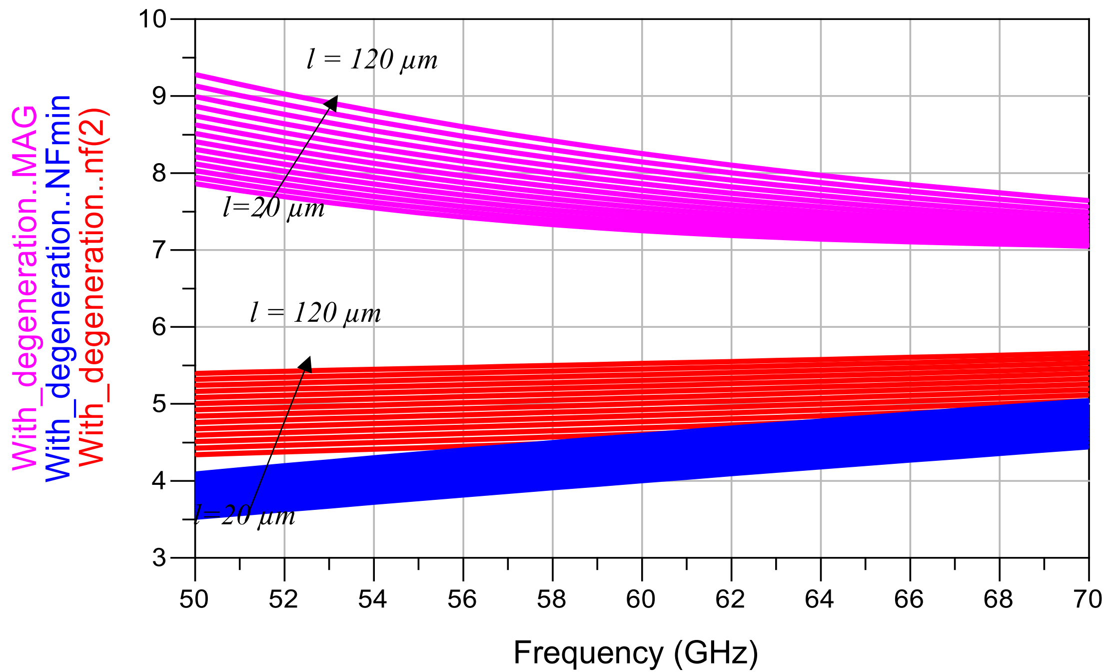

Figure 4.8. The impact of base degeneration on the cascode amplifier.

Table 4.2. One stage LNA' AC analysis parameters.

Freq (GHz)	**S_{11} (Mag/Deg)**	**S_{12} (Mag/Deg)**	**S_{21} (Mag/Deg)**	**S_{22} (Mag/Deg)**	**MAG (dB)**
65.00	0.528 / 2.285	0.063 / -72.952	1.668 / -28.509	0.522 / -19.338	7.38

4.1.3 Input and output matching network

The first stage of the LNA was deliberately matched for NF_{min} and the second stage for MAG. The first stage provided the MAG of 7.38 dB as per Table 4.2 while the noise figure parameters are given in Table 4.3.

Table 4.3. LNA noise parameters.

Freq (GHz)	**r_n (Ω)**	**Γ_{opt} *(MAG/Deg)***	**NF_{min} (dB)**
65.00	41.52	0.292 / -69.017	4.168

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r_n, Γ_{opt} and NF_{min} represent the noise resistor, the optimal reflection coefficient for the noise figure matching, and the minimum attainable noise figure of the device for a given biasing current. To obtain the best compromise between the NF and the gain, the MAG and the noise figure were computed and analysed in ADS using GsMax and NsCircle functions. Here, the MAG, NF_{min} and the number of points are passed as the arguments of the individual functions, resulting in Figure 4.9. From this graph, $\Gamma s = 0.169\angle 1.364$ was selected from which $\Gamma_L = 0.53\angle 21.44°$ was calculated as shown in [194] to be transformed to 50 Ω. This was achieved by using the ADS smart component tool for matching both the input and the output.

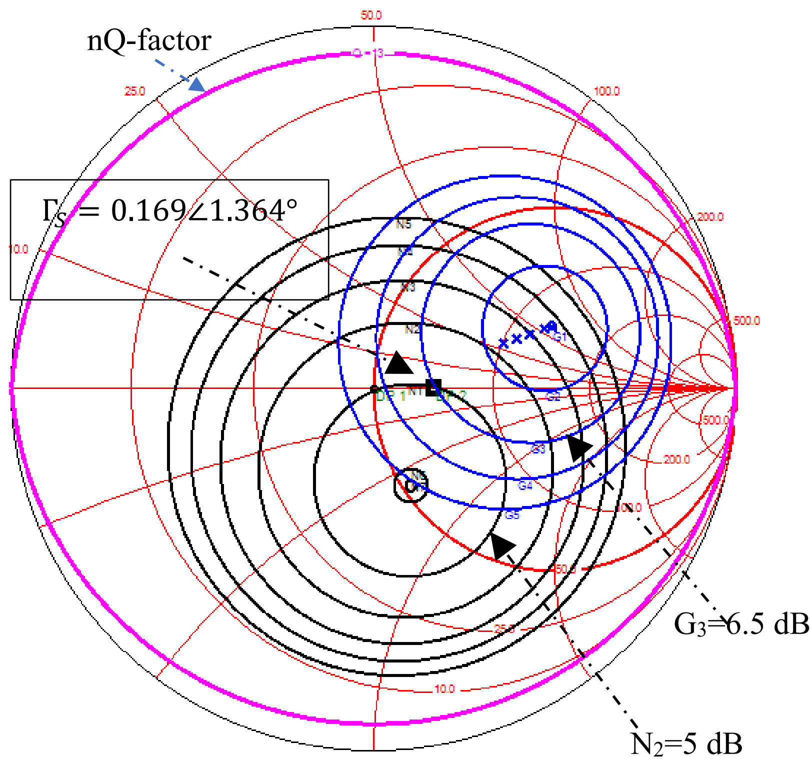

Figure 4.9. Noise figure, gain circle and source and load stability circles.

The input matching network in Figure 4.10 gives two back-to-back L-matching networks that provide a broadband match over the design bandwidth, while at the same time absorbing the pad parasitic capacitor and providing an electrostatic discharge (ESD) path to ground through inductor L_1. The output matching adopted a T-shape matching network as described in [61] to transform Γ_L to 50 Ω. The schematic diagram of the LNA is presented in Figure 4.11, where all

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ideal transmission lines and inductors were replaced with *single-wire* transmission lines *pcells* and the ideal capacitors were replaced by *pcells* MIM capacitors.

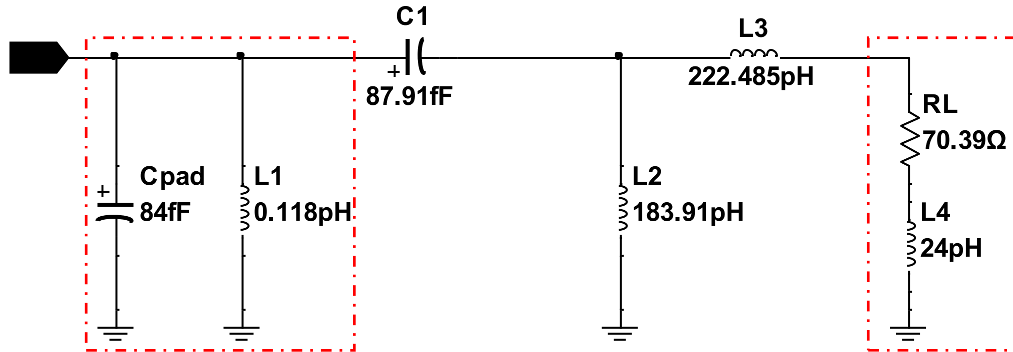

Figure 4.10. Equivalent input matching network.

A DC simulation was conducted again to finetune the biasing point after all the passive components were placed, after which the S-parameters and the HB simulation were conducted following the results presented in the next section.

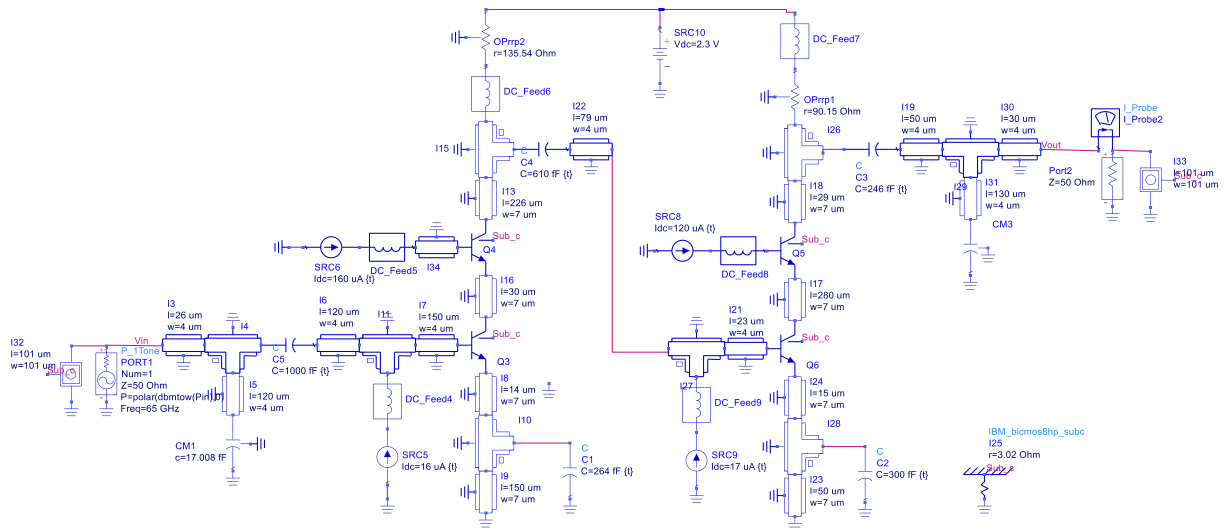

Figure 4.11. Complete LNA schematic constructed in Cadence Virtuoso.

4.1.4 LNA schematic results

The schematic simulation of the LNA exhibits a forward transmission coefficient $|S_{21}|$ and the NF as shown in the first row in Figure 4.12, where $|S_{21}|_{max}$ = 15.2 dB and NF = 7.25 dB at

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f_0 = 65 GHz for the collector current of 4.30 mA. The graph shows a 1dB gain flatness bandwidth > 6 GHz, with a flat NF over the frequency of interest. The reflection coefficients are plotted in the second row in Figure 4.12, width both $|S_{11}|$ and $|S_{22}|$ being below -10 dB over the frequency span. The LNA compression point from the harmonic balance simulation is shown in Figure 4.13, indicating IP1dB of -14.2 dBm.

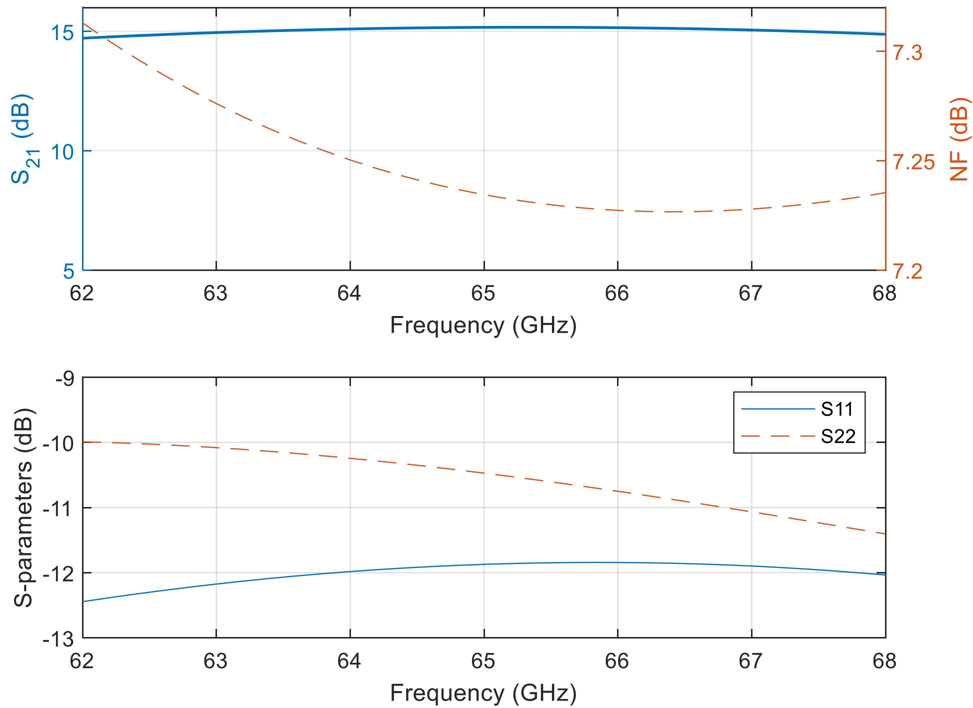

Figure 4.12. Schematic simulation: the upper row is S_{21} and NF, the bottom is for $|S_{11}|$ and $|S_{22}|$.

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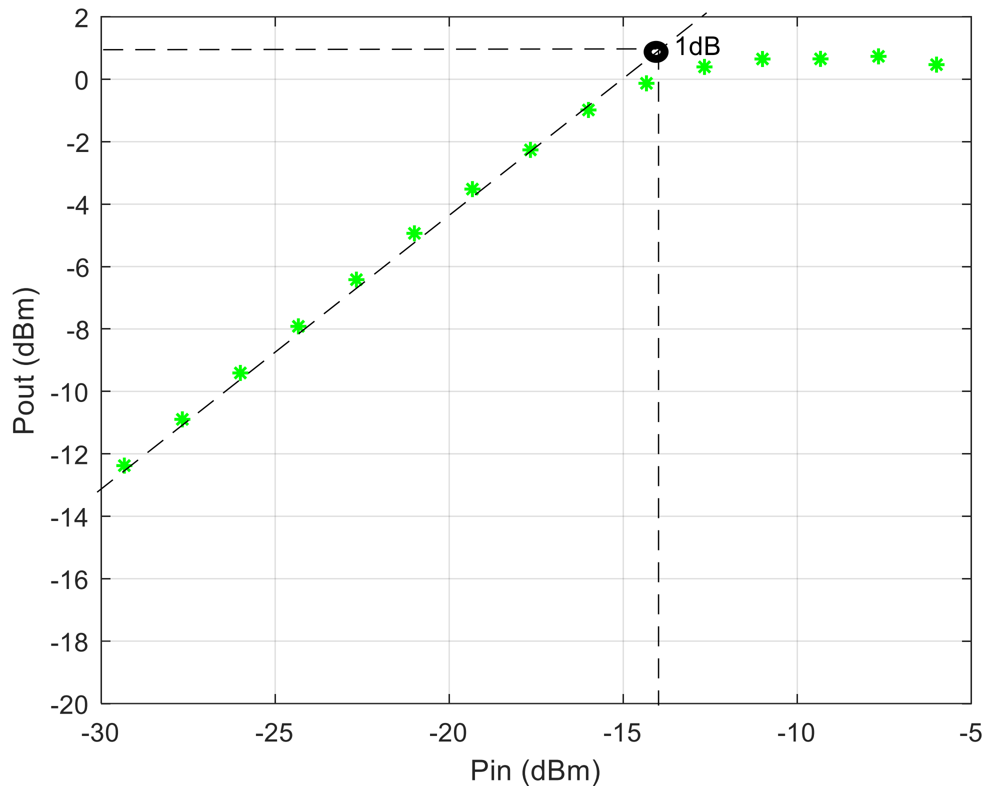

Figure 4.13. On-chip LNA compression point.

4.1.5 Layout

The conversion between the schematic and layout was facilitated by the associated layout model for each of the *pcell* schematic components. The layout in Figure 4.14 uses single-wire transmission line *pcells*, *rflines* for DC feeds and RF chokes. All lines use 45° bend chamfers. The components were placed with sufficient clearance to ensure DRC compliance. To ensure common grounding, an MQ ground plane was drawn over the entire design area and cut-outs were made at relevant locations to access devices underneath, as shown in Figure 4.15 LY dummy metal fills were placed as shown, to ensure that the required pattern density was met. Due to the discrepancy between the schematic simulation and the post-layout simulation, an EM validation was required.

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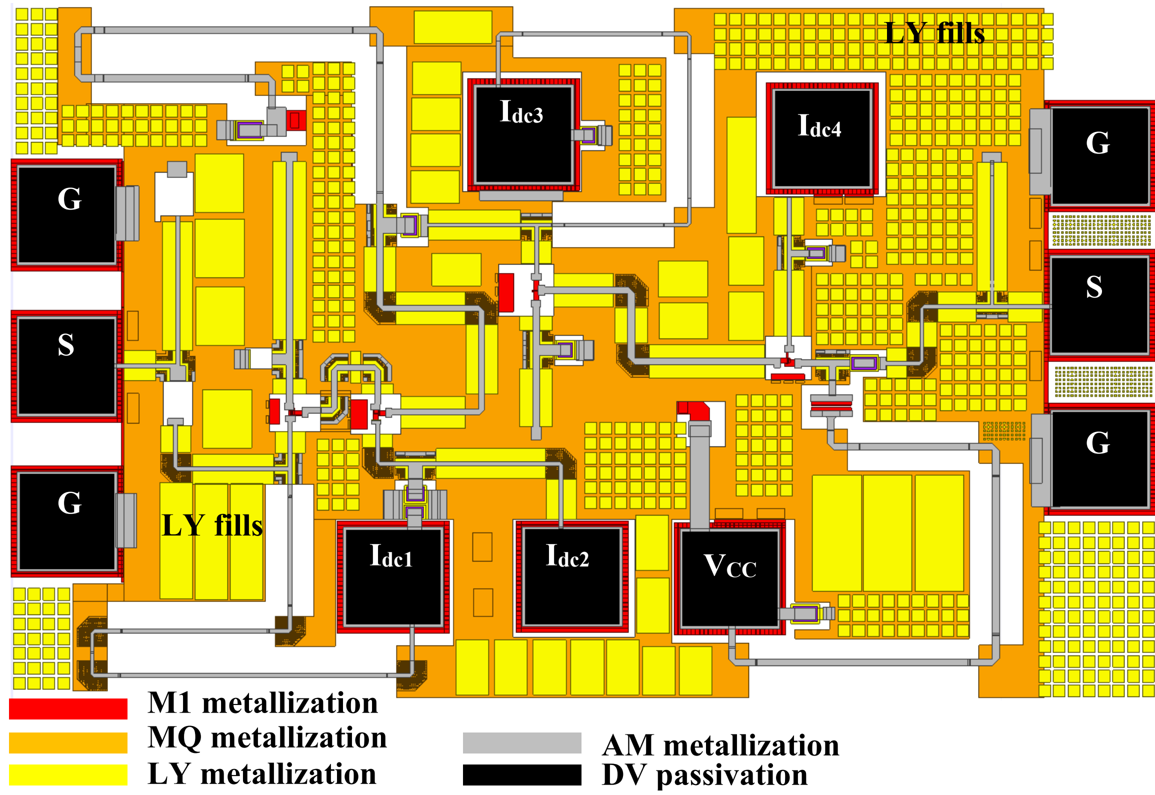

Figure 4.14. On-chip LNA complete layout.

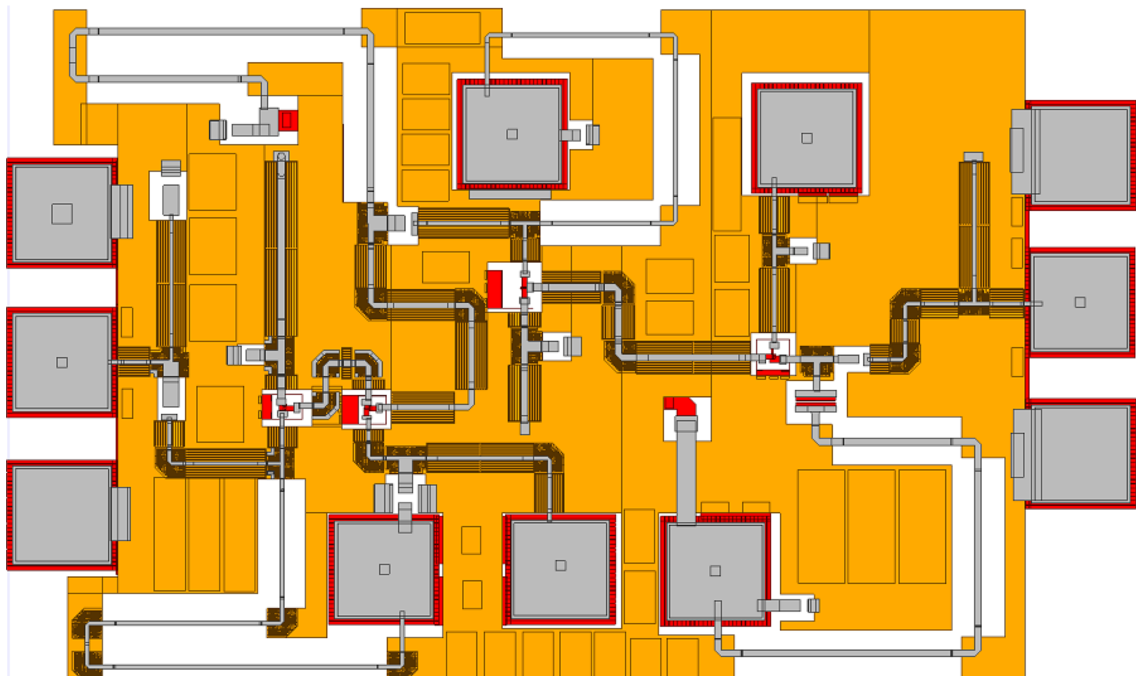

Figure 4.15. Layout showing cutouts through the MQ ground plane.

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4.2 MICROELECTRONIC LNA VALIDATION AND MEASUREMENT

This section discusses the on-chip layout validation methods that were adopted which include the EM validation, RCPE validation and TID electron radiation validation.

4.2.1 LNA post-layout simulation using 3D EM analysis

To validate the layout based on EM simulation, the GDSII file was imported and segmented in HFSS as discussed in Section 3.5.2 to facilitate the simulation process. Ports were placed between AM and MQ metallization layers. Using the FEM simulation engine, the resulting S-parameters from each transmission line were saved into individual folders, and a new schematic based on these files was generated and simulated in *SpectreRF* using previously used simulation tools.

The forward transmission coefficient and the NF are presented in Figure 4.16. Of particular interest is the 1dB gain flatness bandwidth, which reduced from >6 GHz to 4 GHz in the case of *pcell* based schematic simulation. This suggests a more comprehensive interpretation of parasitics elements with 3D EM analysis compared to the *pcell* based schematics. As far as NF is concerned, it is shown that the difference between the simulated *pcells* alone and FEM-schematic co-simulation, is more significant (increased of 0.6 dB) at the lower frequency cut-off. From Figure 4.16, it is evident that $|S_{22}|$ is reduced by ± -2 dB from the *pcell* based schematic $|S_{22}|$ while $|S_{11}|$ remains well matched across the bandwidth. Figure 4.17 indicates a reduction in linearity as well. The estimated input 1dB compression point is -16 dBm yielding to OP1dB of -1.2 dB.

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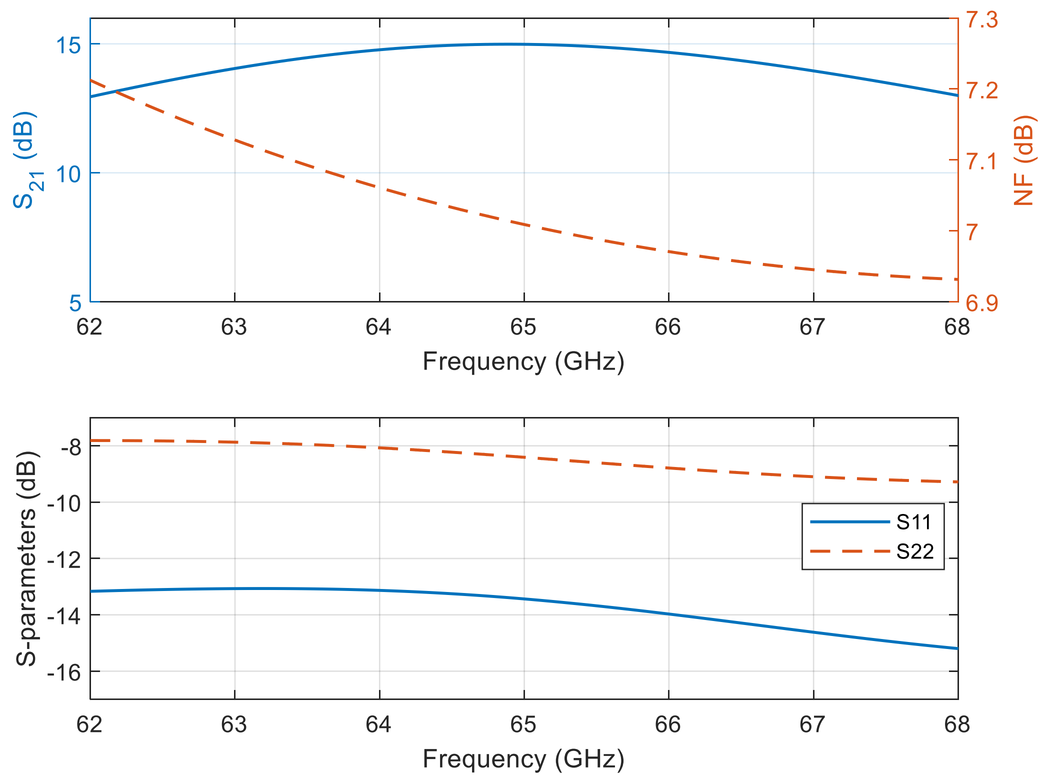

Figure 4.16. LNA simulation with EM-simulated layout.

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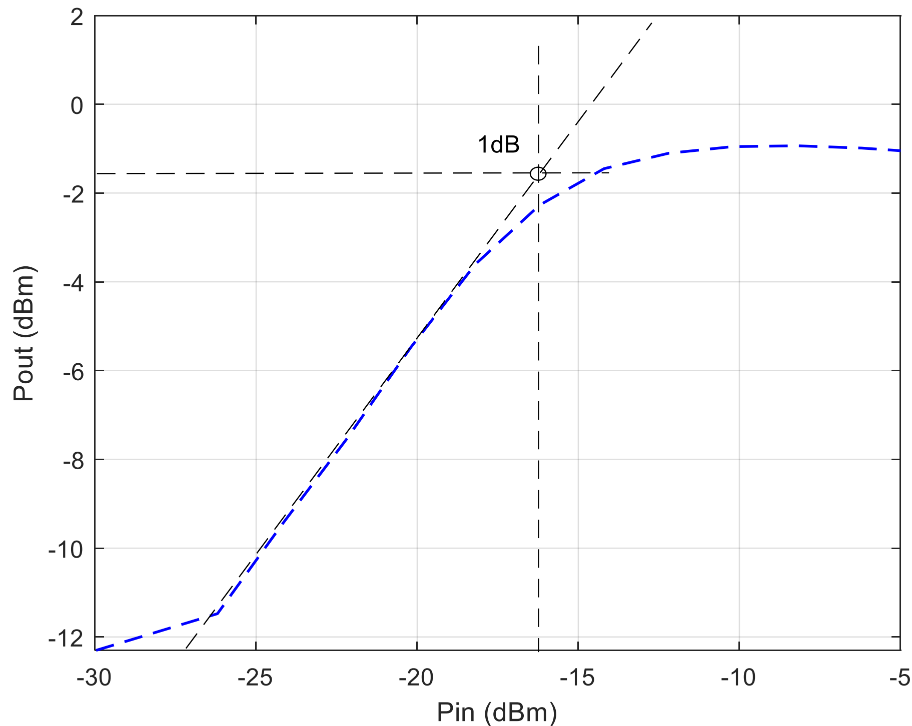

Figure 4.17. Microelectronic LNA compression point after EM simulation.

4.2.2 LNA post-layout simualation based on RC parasitic extraction

The DRC and LVS compliances were first validated on the layout before RCPE was performed using Quantus QRC. The RC parasitic extraction method was discussed in Section 3.5.3, with the result of each iteration of layout optimization and re-simulation saved.

Figure 4.18 to Figure 4.22 depicts improvements from the first iteration to the final iteration of each simulated parameter. Of particular interest, is a further reduction in 1dB gain flatness bandwidth to 2.5 GHz compared to 6 GHz and 4 GHz for the *pcell*-based schematic and FEM-schematic co-simulation, respectively. Likewise, a further degeneration in $|S_{22}|$ to -6 dB is shown in Figure 4.20, as opposed to -10 dB and -8.3 dB for the *pcell*-based schematic simulation and FEM- schematic co-simulation respectively.

It is important to note that the output MIM capacitor and the shunt stub capacitor played important roles in the observed degradation. For example, it was found that increasing the MIM capacitor's vias significantly improved the performance of the MIM capacitors, thereby improving the output matching. Furthermore, the space around the capacitors needed to be

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increased, which reduced stray capacitance. These, in addition to what was discussed in Section 3.5.3, resulted in an improvement of the response of the LNA which is shown by the fifth iteration. This final layout was then used for EM validation previously discussed. The NF in Figure 4.22 also shows a progressive improvement following each iteration until no more changes were observed with further layout changes.

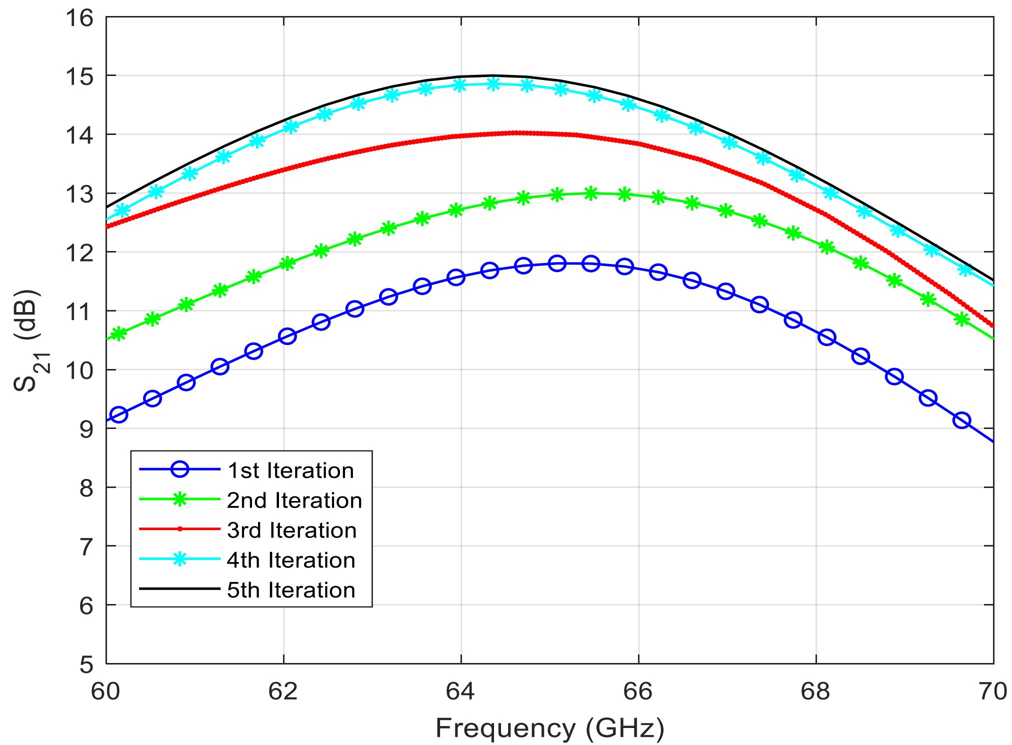

Figure 4.18. Post RC extraction S_{21} following each iteration.

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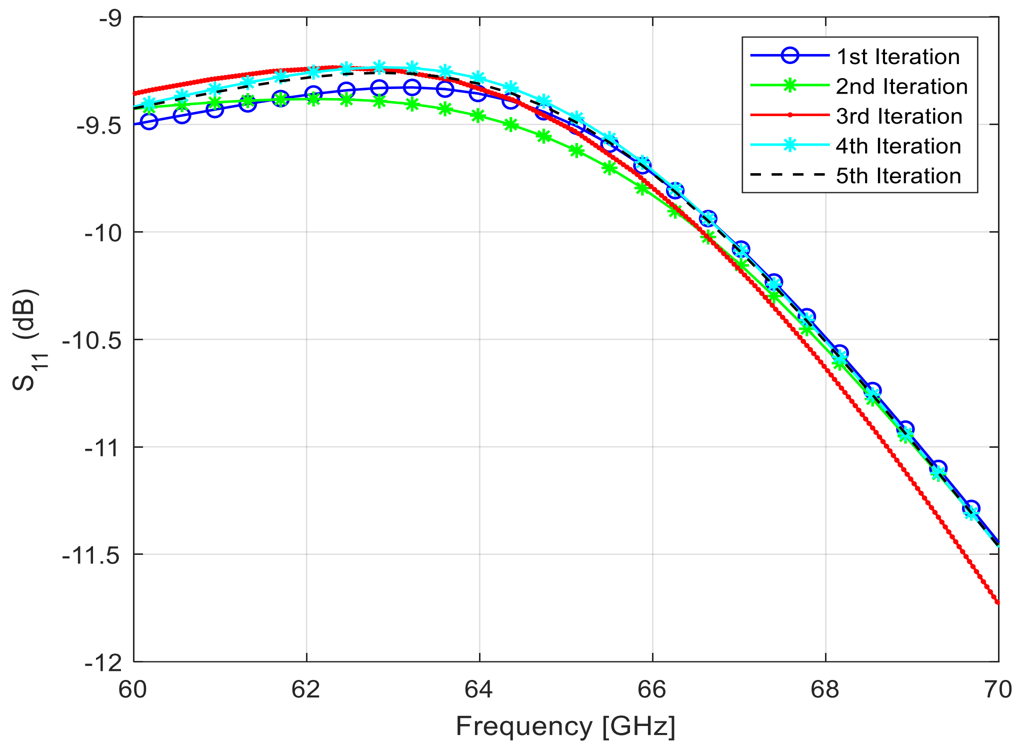

Figure 4.19. Post RC extraction S_{11} following each iteration.

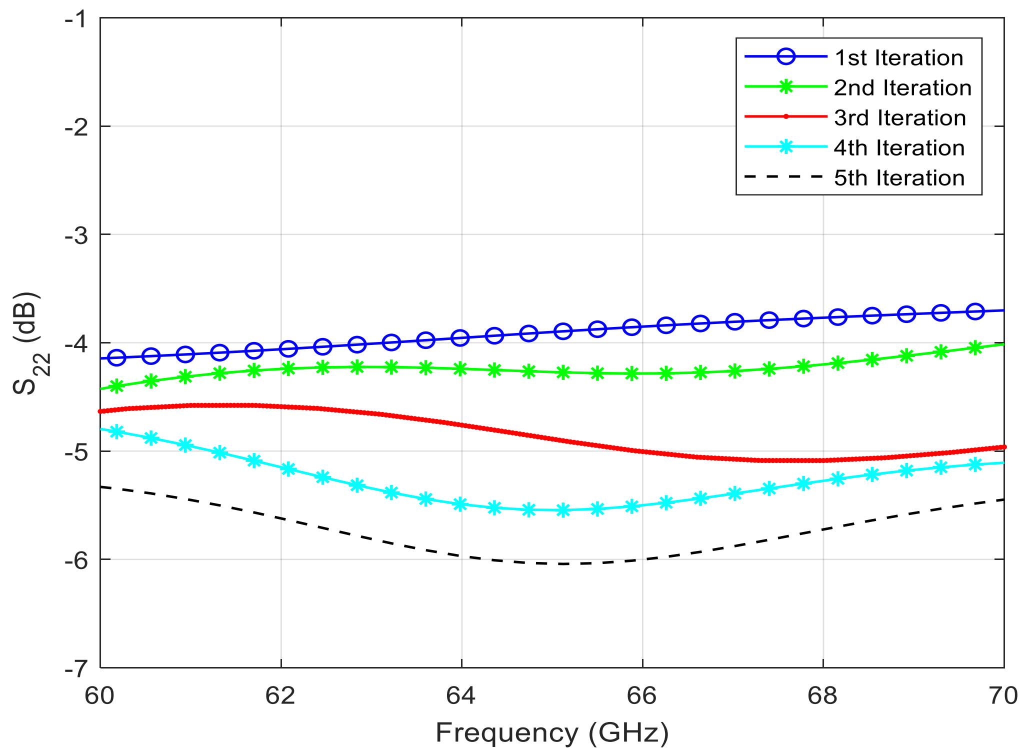

Figure 4.20. Post RC extraction S_{22} following each iteration.

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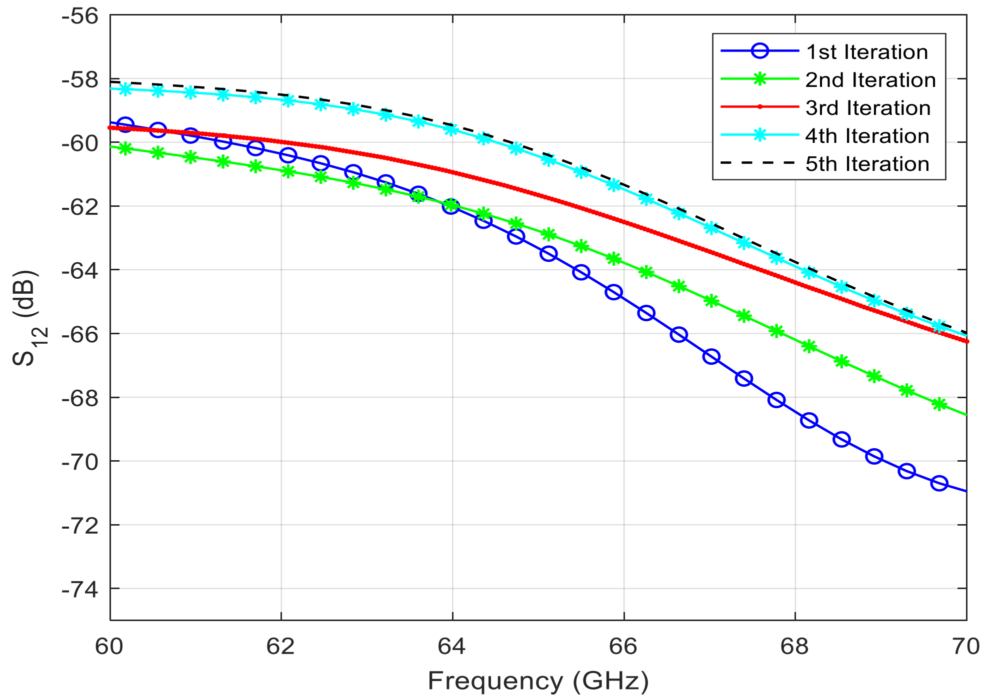

Figure 4.21. Post RC extraction S_{12} following each iteration.

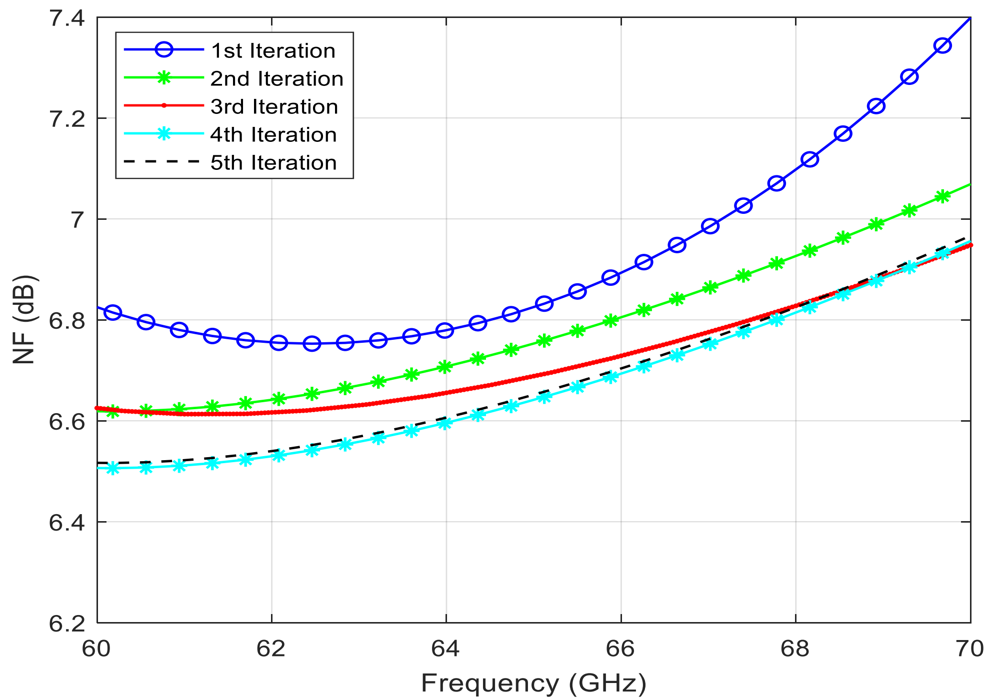

Figure 4.22. Post RC extraction NF following each iteration.

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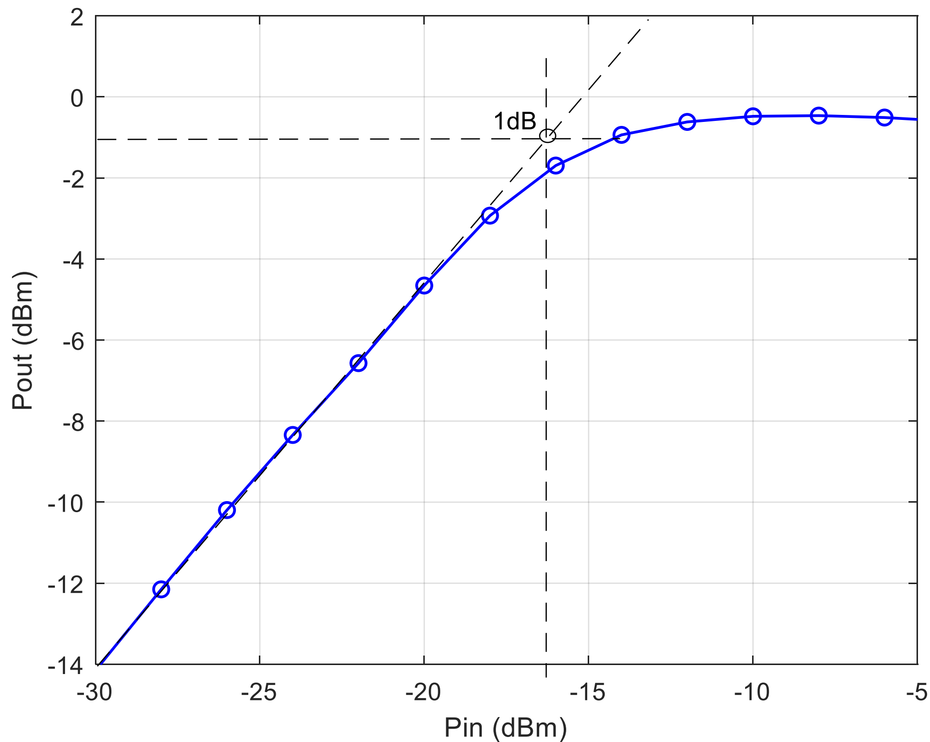

Figure 4.23. 1 dB compression point of RC extraction final iteration.

4.2.3 Microelectronic LNA Measurement

The linear measurements were conducted using Anritsu ME7828A VNA with the measurement frequency set from 55 GHz to 75 GHz. The VNA was calibrated using a single-tier LRM calibration using a CS-5 impedance standard substrate (ISS) on a wafer and the GGB 110H GSG probes. The calibration power level was set at -10 dBm, 1kHz IF bandwidth with the averaging enabled. Second-tier calibration was not necessary because the pads were part of the experiment. An external constant base current supply was done through an HP 4155B parameter analyser and applied to the circuit through four DC needles, forcing a collector current of 4.5 mA from 2.3 V supply (due to process variation the bias point was tuned from I_{CQ} = 4.3 mA to 4.5mA during measurements).

The RF power was initially swept from -30 dBm to -5 dBm and measured at the output of the LNA using a power meter whose values were logged to a computer. From this measurement, the compression point of the LNA was determined after which a THRU calibration update was conducted just prior to linear measurements.

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The Noise figure measurements were conducted on a Rohde & Schwartz FSW50 signal analyser (SA). A Sage Millimetre STG-15 external mixer was used for frequency extension from 50 GHz to 75 GHz since the SA operational frequency is limited to 50 GHz. For the noise figure measurements, the THRU calibration was performed as mentioned in Section 3.8.3, followed by a noise source (STZ-15-I1) calibration whose ENR values (11 to 13.5 dB) were stored in the SA for reference. The measured data were then exported and post-processed in Matlab.

The measured IP1dB and OP1dB shown in Figure 4.24 were -16.2 dBm and -2 dBm respectively. A linear gain of 14.84 dB at f_0 and a 1dB gain flatness bandwidth of ±3 GHz are evident in Figure 4.25. The measured midband NF from Figure 4.25 is 7.44 dB, with less than 1 dB variation across the band of interest. Both the measured input and output reflection coefficients are presented in Figure 4.26, indicating $|S_{11}| \approx$ -14.7 dB and $|S_{22}| \approx$ -11.2 dB.

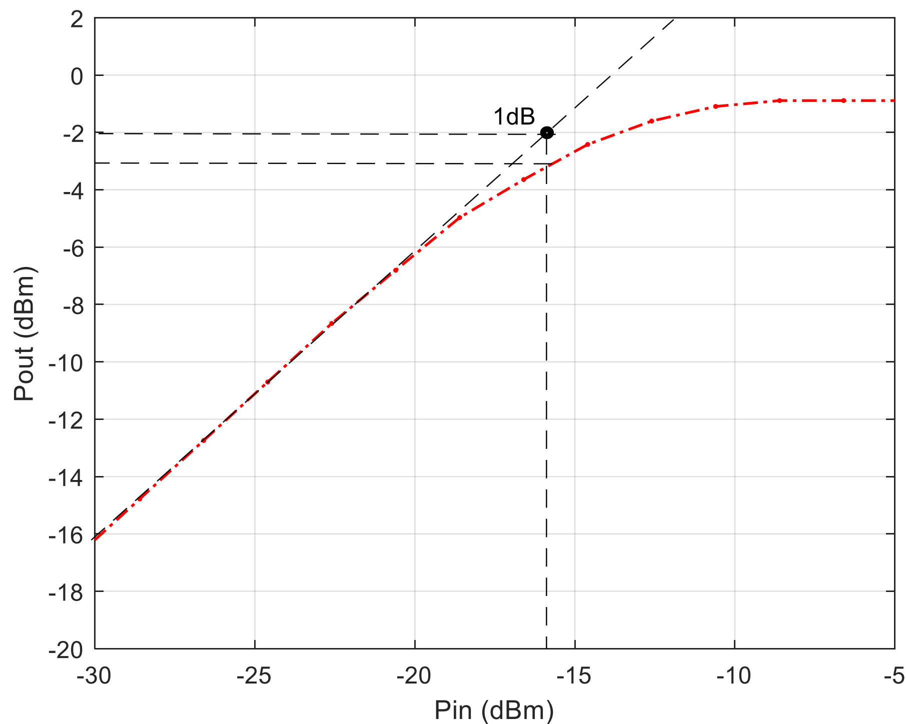

Figure 4.24. Measured 1 dB compression point.

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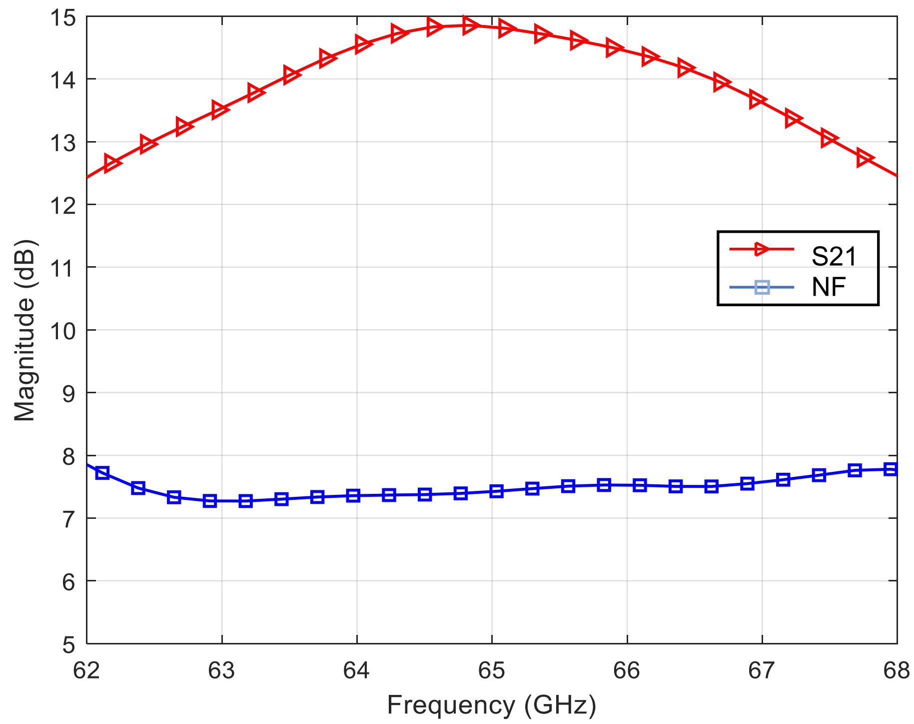

Figure 4.25. Measured $|S_{21}|$ and NF for the V-and LNA.

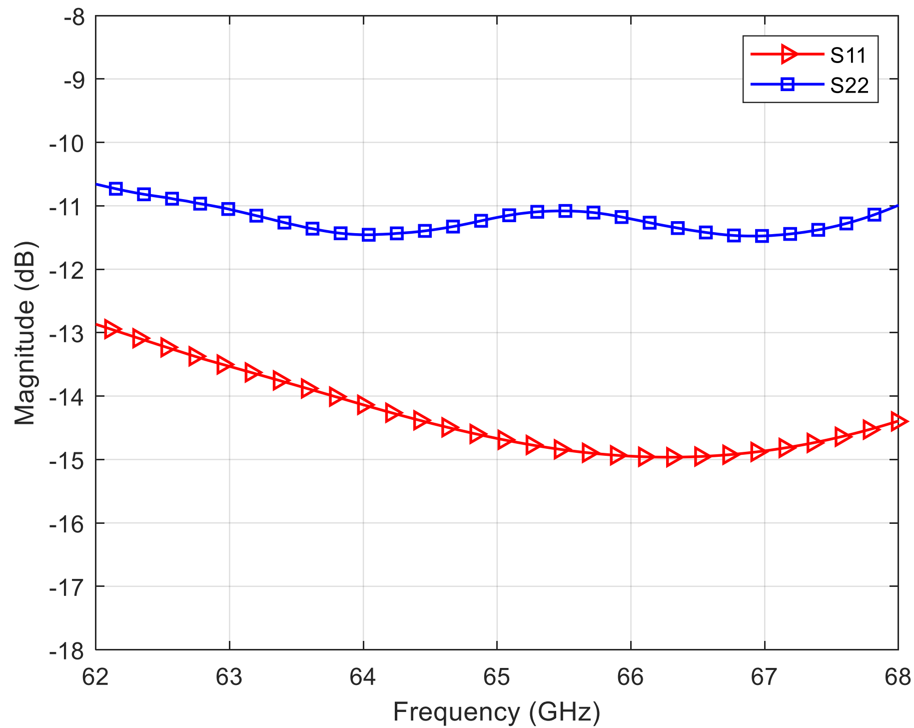

Figure 4.26. Measured $|S_{11}|$ vs. $|S_{22}|$ of V-band LNA.

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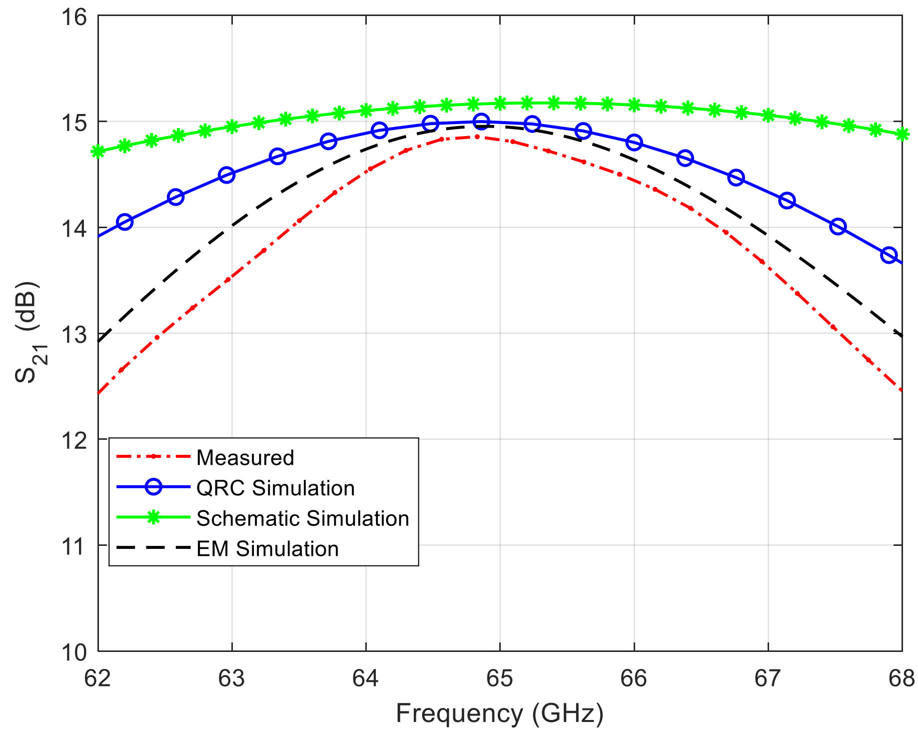

Figure 4.27. Comparing the measured $|S_{21}|$ against all simulated $|S_{21}|$.

To compare the three validation approaches, all the major LNA parameters are plotted alongside each other from Figure 4.27 to Figure 4.31 in order to compare simulated and the measured results. These are summarized in Table 4.4.

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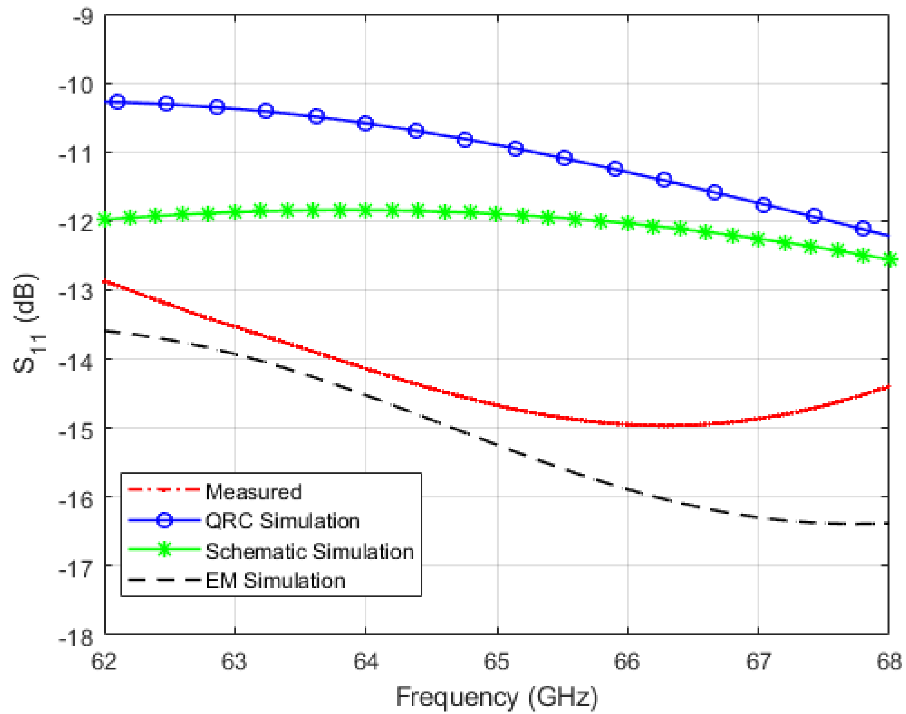

Figure 4.28. Comparison between the measured $|S_{11}|$ and all simulated $|S_{11}|$ values.

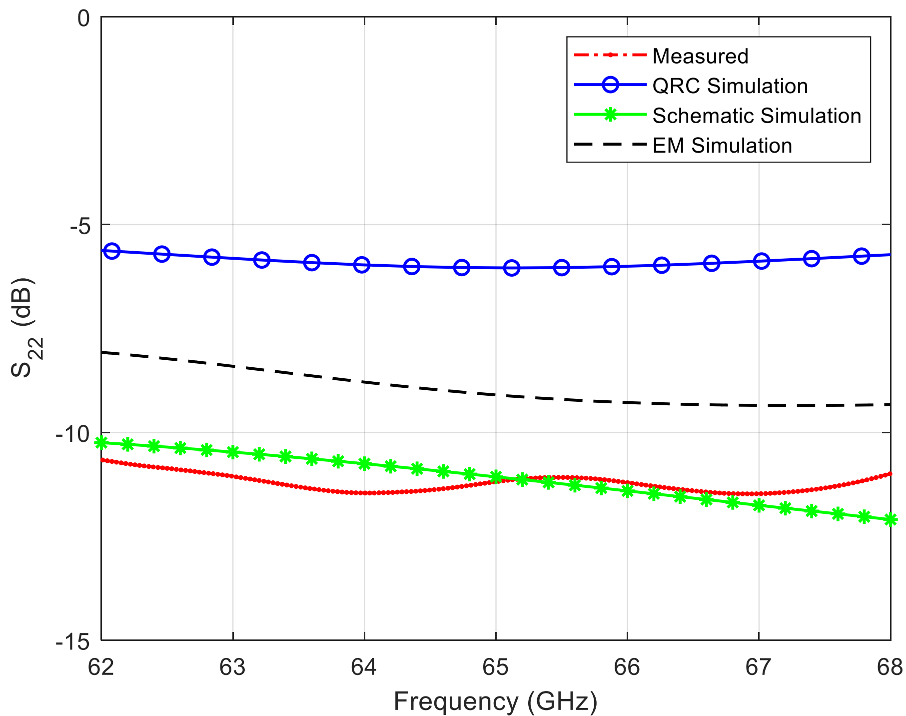

Figure 4.29. Comparison between the measured $|S_{22}|$ and all simulated $|S_{22}|$.

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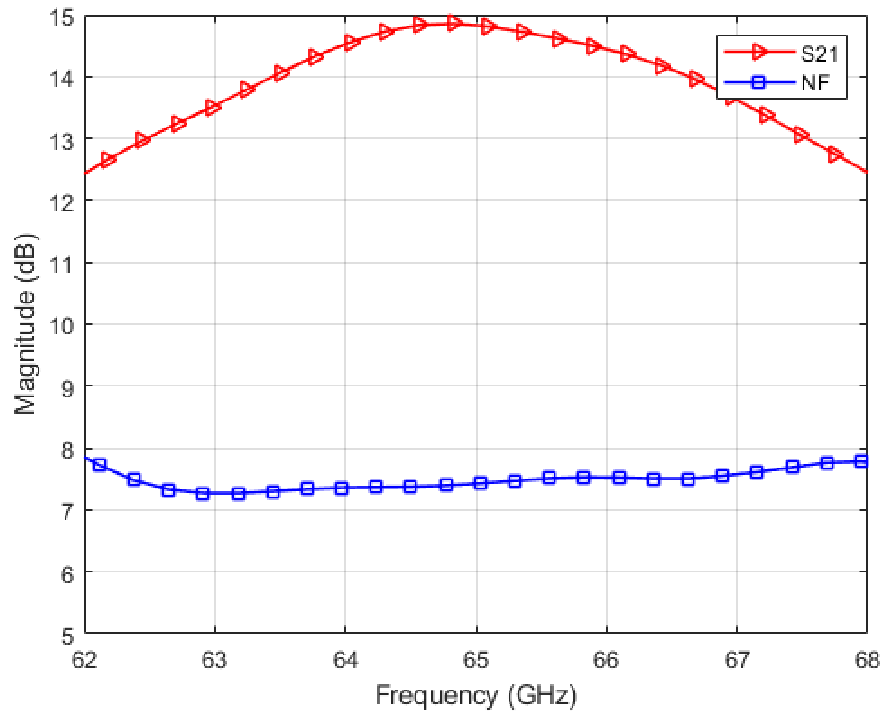

Figure 4.30. Comparison between the measured NF against all simulated NF results.

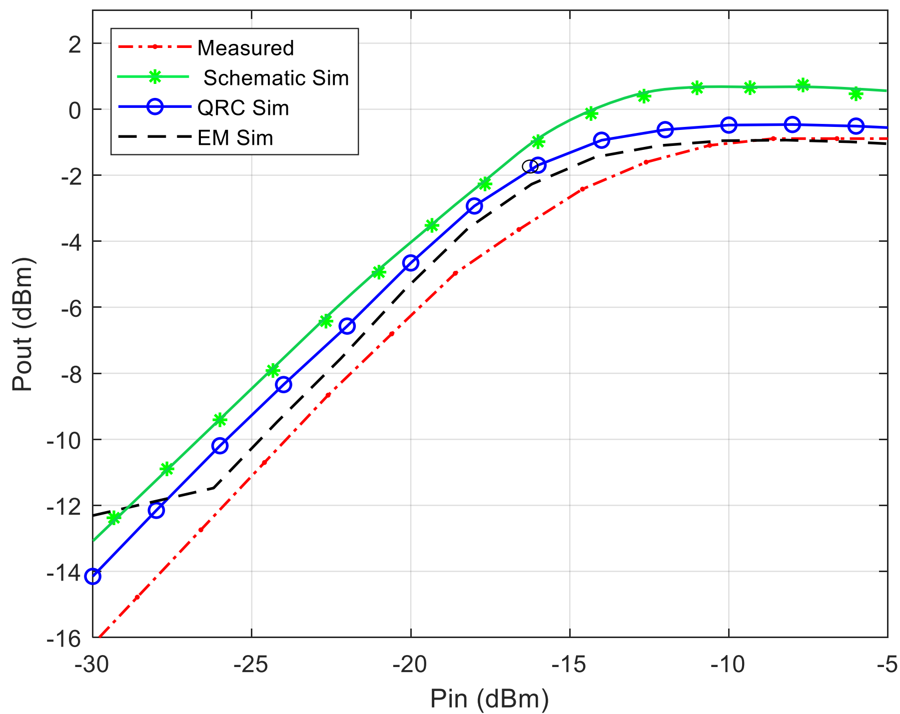

Figure 4.31. Comparing the 1dB compression point of the measured results against all simulated results.

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As shown in Table 4.4 the FEM co-simulation agrees with measurement results within 0.11 dB of maximum gain error, 0.18 dB of NF error and 0.6 dBm in P1dB error as opposed to 2.6 dB in maximum gain, 0.1 dB in NF, 2.2 dBm in P1dB for the *pcell*-based schematic simulation and 1.55 dB in maximum gain, 1.15 dB in NF, 0.8 dBm in P1dB for schematic with RC-parasitic extraction. These results are consistent with [147], [161] and [195] although the latter did not evaluate the RC parasitic extraction.

Table 4.4. Comparing the three validation approaches with SOTA.

	Frequency (GHz)	Approach	$\|S_{21}\|$ @ f_0, (dB)	$\|S_{21}\|$ error @ f_0, (dB)	1dB GFBW (GHz)	Gain BW error (GHz)	NF @ f_0, (dB)	NF error @ f_0, (dB)	P1db @ f_0, (dBm)	P1db error @ f_0, (dBm)
*	65.2	Pcell schematic	15.2	0.36	>6	>2.44	7.25	0.19	-14	-2.2
	65	Pcell schematic + QRC	15	0.14	5.7	2.14	6.95	0.49	-15.4	-0.8
	65	3D EM co-sim	14.95	≈0.1	4.03	0.47	7.66	-0.23	-15.6	-0.6
[147]	24	3D EM co-sim	8.2	-1.6	4.4	-1.4	-	-	-	-
	23.7	Schematic + RC	4.8	1.8	1.4	1.6	-	-	-	-
[161]	2.5	3D EM co-sim	21.8	4.2	0.2	-0.2	2.3	-	-	-
	2.3	Schematic + RC	24	2	0.5	0.1	2.5	-	-	-
[195]	0-11	Schematic sim	17.2	-0.2	>10	-2.5	-			
	0-11	3D EM co-sim	16.2	0.8	>6	1.5	-	-	-	-
[196]	33	3D EM co-sim	21.1	2.5	≈2.9	≈1.6	4.58	0.32	-8	-

*This work

4.2.4 Radiation experiment of microelectronic LNA

The results of the radiation experiment described in Section 3.8.4 are presented here. Figure 4.32 illustrates a gradual reduction of both $|S_{21}|$ (from ±15 dB to ± 12.3 dB) and 1dB gain flatness bandwidth (from ±4.5 GHz to ±3 GHz), with an increased radiation dose. This reduction in the bandwidth is evident at both the upper and lower cut-off frequencies. These may be associated with damaged MIM capacitors [172] used as coupling and bypass capacitors, and increases in the intrinsic parameters R_{be} (R_b+R_e) and C_{be} [191]. These effects, combined, would ultimately reduce the passband with increased radiation dose [197].

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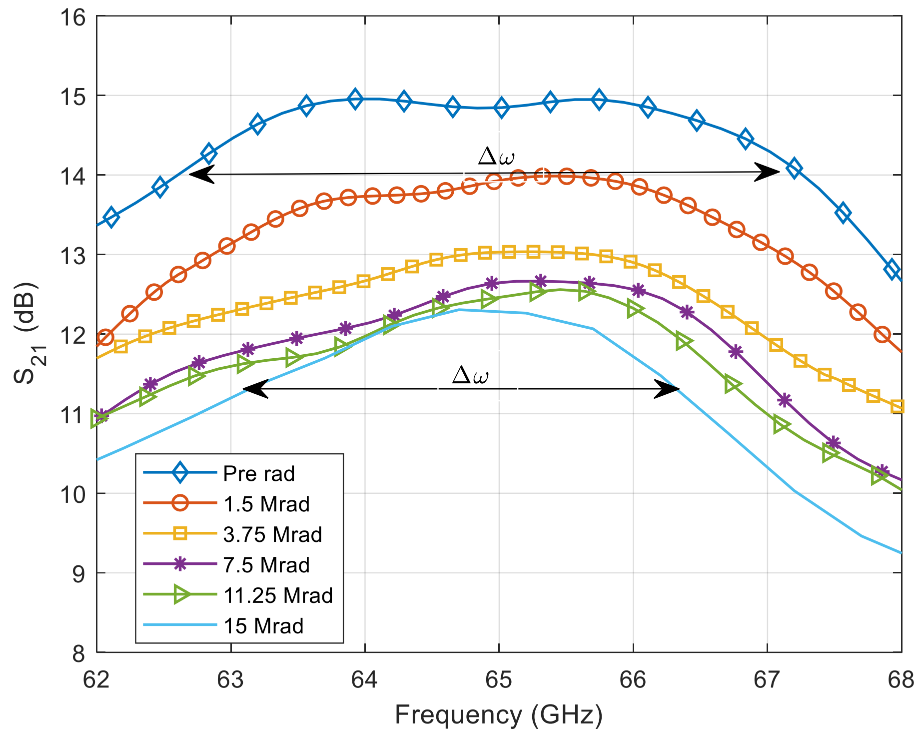

Figure 4.32. S_{21} damage following each radiation iteration.

Figure 4.33 and Figure 4.34, show an increase in the return loss, indicating a further change in the base-emitter capacitance C_π and resistance r_π assuming the π-model, thereby impacting both $|S_{21}|$ and NF. Figure 4.35 validates this hypothesis, indicating increases in the input resistance and capacitance with increasing radiation dose. These observations agree with those reported in [198], [191] and [199]. In these cases, electron radiation is linked with TID damage to R_{be} and C_{be}. The increase in the base thermal noise would further degrade the NF. This phenomenon is due to the increase in R_{bi} as reported in [200] and documented in [191]. Since the collector current I_{CQ} contributes to collector shot noise, an increase in the former would increase the latter [200].

The measurement results indicate a degradation across most parameters. These changes may also be modelled explicitly in simulation as described by [191], however, this method does not provide for scaling the model with device bias or device size (nor do any models exist with which this is possible). To implement the exact model in the simulation would require that the small-signal be pre-characterised for each of the LNA transistors under the exact bias condition.

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This was impossible, because the transistors were not available and, as a result, the model could not be adapted to a specific radiation dose.

Figure 4.36 shows a sudden increase in the collector current from the first radiation iteration which stabilizes after a further increase in the radiation dose despite the adoption of constant base currents topology. This may be due to an increased effective base current as a result of trapped charges between the emitter-base junction [167] [169], which would account for the increased P_{DC} in Table 4.5. This sudden increase in I_{CQ} under moderate damage, however, diverges from the gradual degradation observed in other performance parameters. This phenomenon might suggest a leakage path created by a radiation-induced defect, possibly in one of the large 264 fF MIM capacitors used for RF grounding [25] in the layout. This may also be attributed to an increased collector current density, which increases with TID but plateaus at values above ≈ 1 MRad for TID under gamma irradiation in [199].

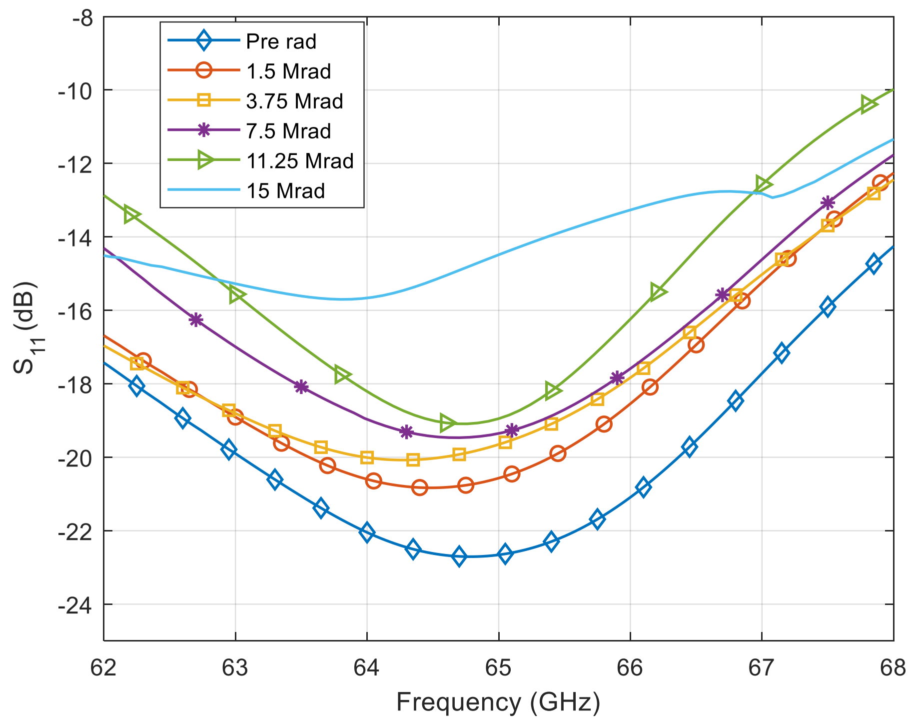

Figure 4.33. Input matching variation following each radiation iteration.

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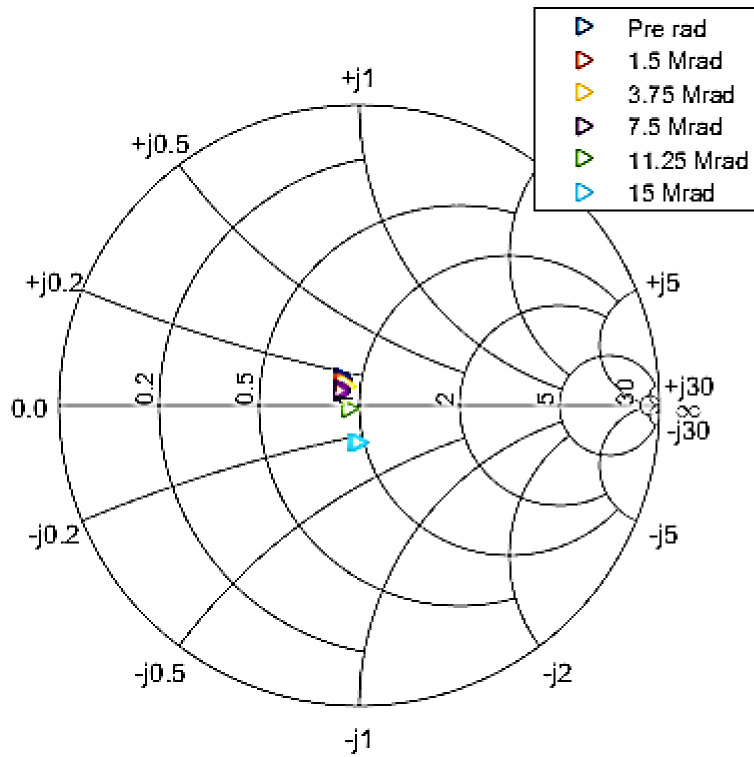

Figure 4.34. Input matching variation following each radiation iteration.

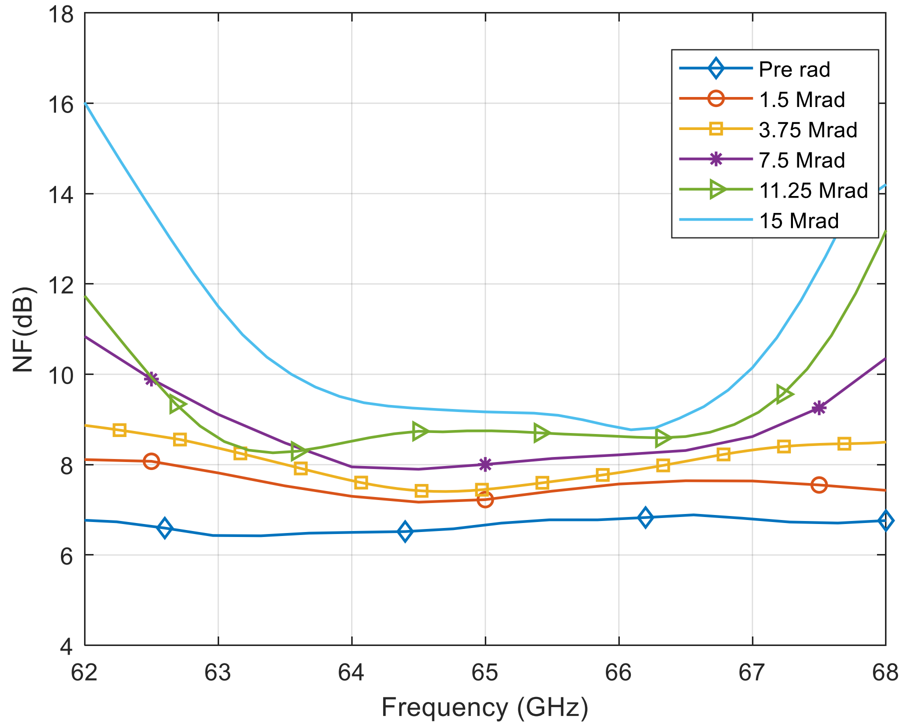

Figure 4.35. NF following each radiation iteration.

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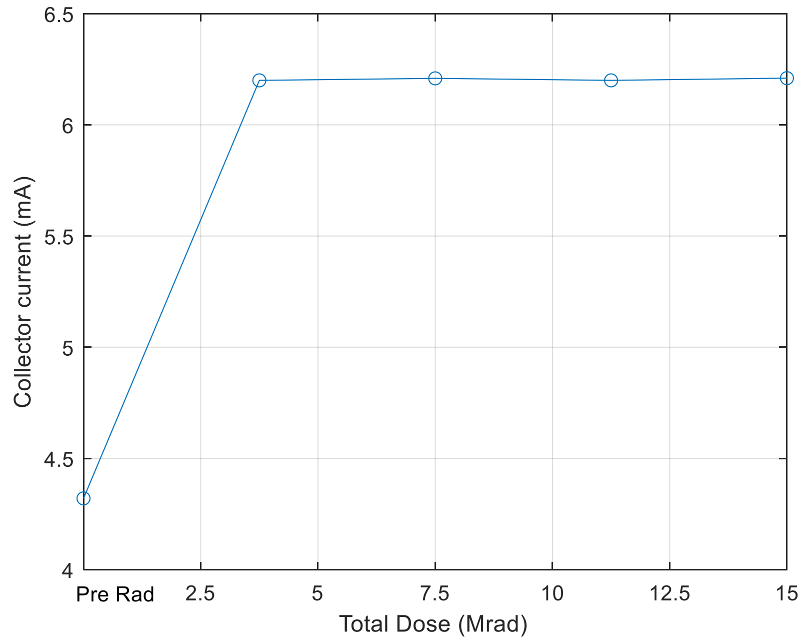

Figure 4.36. I_C vs. total dose for each iteration.

Table 4.6 presents a comparison of TID induced degeneration in this study with other TID studies in the literature on SiGe. The data would indicate very limited open-source literature in electron radiation effect on mm-wave LNAs. In [169], where electron irradiation is investigated, NF degradation data is not provided, nor is the figure of merit (FoM). It is, however, interesting to note the severe gain degradation observed under electron radiation > 10 Mrad(Si), both in this work and in [169], while SiGe's resilience to irradiation in [19] is only discussed in terms of gamma, neutron and proton radiation.

Table 4.5. LNA parameters Post-RC parasitic extraction.

Parameters	**Pre-Rad**	**1.5 Mrad**	**3.75 Mrad**	**7.5 Mrad**	**11.25 Mrad**	**15 Mrad**
P_{DC} (mW)	9.89	15.87	14.26	14.28	14.26	14.3
FoM	1.98	0.9	0.87	0.66	0.47	0.35
Z_{in} (Ω)	43+j5	43.5+j3.5	43.56+j2	43.7+j0.35	44+j0.002	44-j9.45
$\|S_{21}\|_{(max)}$ (dB)	14.8	13.93	13	12.62	12.4	12.3
NF (dB)	6.64	7.2	7.42	8.2	9.1	9.5
BW (GHz)	4.8	4.45	4.24	4.2	3.85	3.25

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Table 4.6. SiGe LNAs radiation tolerance comparison.

Reference	[169]	[171]	[170]	**This work**
Radiation type	Electron, 3 MeV	Proton, 63.3 MeV	Proton, 63.3 MeV	Electron, 2.26 MeV
f_0 (GHz)	2.5	62	12	65
Total dose (Mrad(Si))	25	0.134	2	15
Pre-rad $\|S_{21}\|_{(max)}$ (dB)	20.9	14.2	17.5	15
Post-rad $\|S_{21}\|_{(max)}$ (dB)	7.5	13.6	17.3	13.7
Pre-rad NF (dB)	-	3	5.85	6.5
Post-rad NF (dB)	-	3.5	5.63	7.72
Pre-rad I_C (mA)	-	8	3.5	4.32
Post-rad I_C (mA)	-	8	3.5	≈6.22

4.3 SUMMARY

This chapter presented the design of a V-band microelectronic integrated LNA. The LNA was designed and simulated in Cadence Virtuoso and was fabricated in a 130 nm BiCMOS8HP process, under a multi-project wafer program. The design was based on two cascaded stages of cascode pairs which were validated through DRC, LVS, QRC and 3D FEM. The simulated gain and NF were 15.2 dB and 7.44 dB, while the measured values were 14.84 dB and 7.44 dB respectively when I_{CQ} was 4.5 mA. Prior to RC parasitic extraction, the DRC and LVS were conducted to ensure an error-free design. It is found that FEM simulation best estimate the performance of the microelectronic LNA compared to the RCPE method and schematic using the *pcell* components alone. Meanwhile, the MoM significantly underestimates the performance of microelectronic devices leading a severe deviation in f_0 [182].

Preceding the FEM validation, microelectronic stacks were first simulated to validate the method using an 88 GHz patch antenna as discussed in Section 3.5.1. The simulation result revealed the impact of omitting the bulk silicon from the stackup and suggests such omission leads to the worst performance degradation as opposed to other effects. These effects include

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simplifying the vias, including etch factor or even changing between SiO2 and SiNi substrate at the boundary between FEOL and BEOL. The simulation also revealed that 2.5D MoM in HFSS was the least accurate as opposed to 3D FEM, in estimating the performance of on-chip complex stacks at mm-wave.

By comparing *pcell* based schematic simulation, *pcell* simulation with QRC extraction, and post-FEM schematic simulation against the measured results, it was shown that FEM best estimated the measurements compared to the other methods at these frequencies. This was true for the *NF*, S-parameters and 1dB compression points.

Finally, the LNA was exposed to TID electron radiation, a total dose of 15 Mrad(Si) under optimal bias currents of $I_C = 4.30$ mA. The newly measured $|S_{21}|$ and NF at this bias point were 14.8 dB and 6.64 dB. Parametric damages were noticeable, with reductions in gain, 1dB gain flatness bandwidth and an increase in the NF. These support previous results obtained with proton, neutron, and gamma radiations [171].

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CHAPTER 5 HYBRID V-BAND LNA

"Projects we have completed demonstrate what we know - future projects decide what we will learn." *- Dr Mohsin Tiwana*

5.1 INTRODUCTION

MMIC LNAs cannot be deployed into systems in isolation without packaging. By presenting a pad-to-pad comparison between the MMIC LNA (as packaged on the PCB) and the hybrid LNA integrated onto PCB,system designers a provided with data to guide their design decisions. Wirebond and flip-chip interconnections are used for this study because of the low I/O pin counts requirements, their low assembly cost and availability of low volume prototyping facilities compared to other technologies. XT/Duroid 8100 substrate material was used as the host medium based on its low and stable dielectric constant at high frequencies. This chapter, therefore, presents the design of the hybrid LNA which includes the designs and experimental data of all off-chip passives (the filters used as the DC blocks, the transmission lines, the wirebond interconnects, the radial stub and the chip capacitors). The chapter also includes the design and characterisation of the resonators used to characterise the XT/Duroid 8100 substrate material, as well as the experimental data for the transistors used in the hybrid designs. Further in the chapter, the integration of the MMIC LNA on PCB as well as the discrete transistors with off-chip matching are presented, including their subsequent simulation results.

5.1.1 Wire-bond characterisation

The wire-bond transitions were characterised through EM models in AED and experimental analysis. First, the GDSII file of the transistor layout was imported into Ansys Electronics Desktop (AED). Using the stackup builder in AED, a double-sided PCB stackup was generated

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and the AED wire-bond tool was then used to create the transition. No additional transmission line was added so that the result reflects the performance of the interconnect exclusively. Figure **5.1** depicts the π-model of the transition that was used to extract the RLC parameters in Table 5.1. The EM models included single wire, two-wire and three wires-bonds as shown in Figure 5.2. Waveguide ports were drawn explicitly as the edge ports could not be used since the ports are inside the simulation boundary box.

Figure 5.3 and Figure 5.4 provide the simulated S-parameters results of the interconnect. Of particular interest is the high insertion loss incurred by transitions (up to ± 5 dB *IL* at the designed f_0). Figure 5.4 also shows a significant deviation between different wire-bond profiles, where one wire-bond profile appears to have a much larger insertion loss (*IL* = -6.5 dB) than the two other profiles at f_0. In Figure 5.5, the wire-bond measurement geometry is presented, from which the two variants in Figure 5.6 were derived.

In Figure 5.6(a), a pad-to-pad measurement on PCB is highlighted, while in Figure 5.6(b), one probe is positioned on top of the wire-bond on the chip pad, and the other probe on the PCB. This method was found to be the most accurate. Once the transmission line on the PCB is de-embedded from the measurement, the remaining data directly reflect the interconnect.

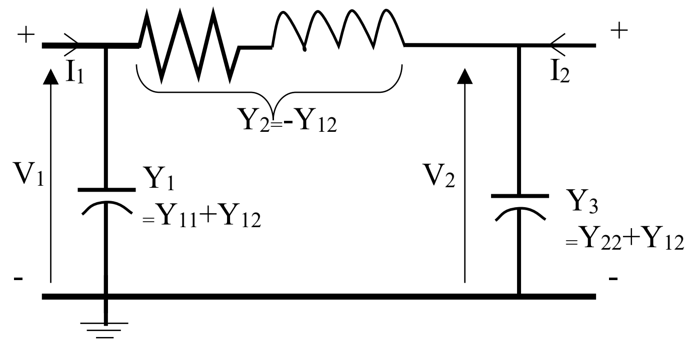

Figure 5.1. RLC π-model of wire-bond interconnect.

Table 5.1 provides the extracted RLC parameters of the transition using the method outlined in [201], while the measured S-parameters are presented in Figure 5.7. A significant increase in insertion loss is observed at the design f_0 (S_{21} ± 13 dB), which is more than double that simulated. In addition, the equivalent capacitance also appears significantly larger. These variations could be attributed to increased contact resistance and cross-coupling between the

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parallel lines respectively, which were not modelled in the model in Figure 5.1 or the EM simulations.

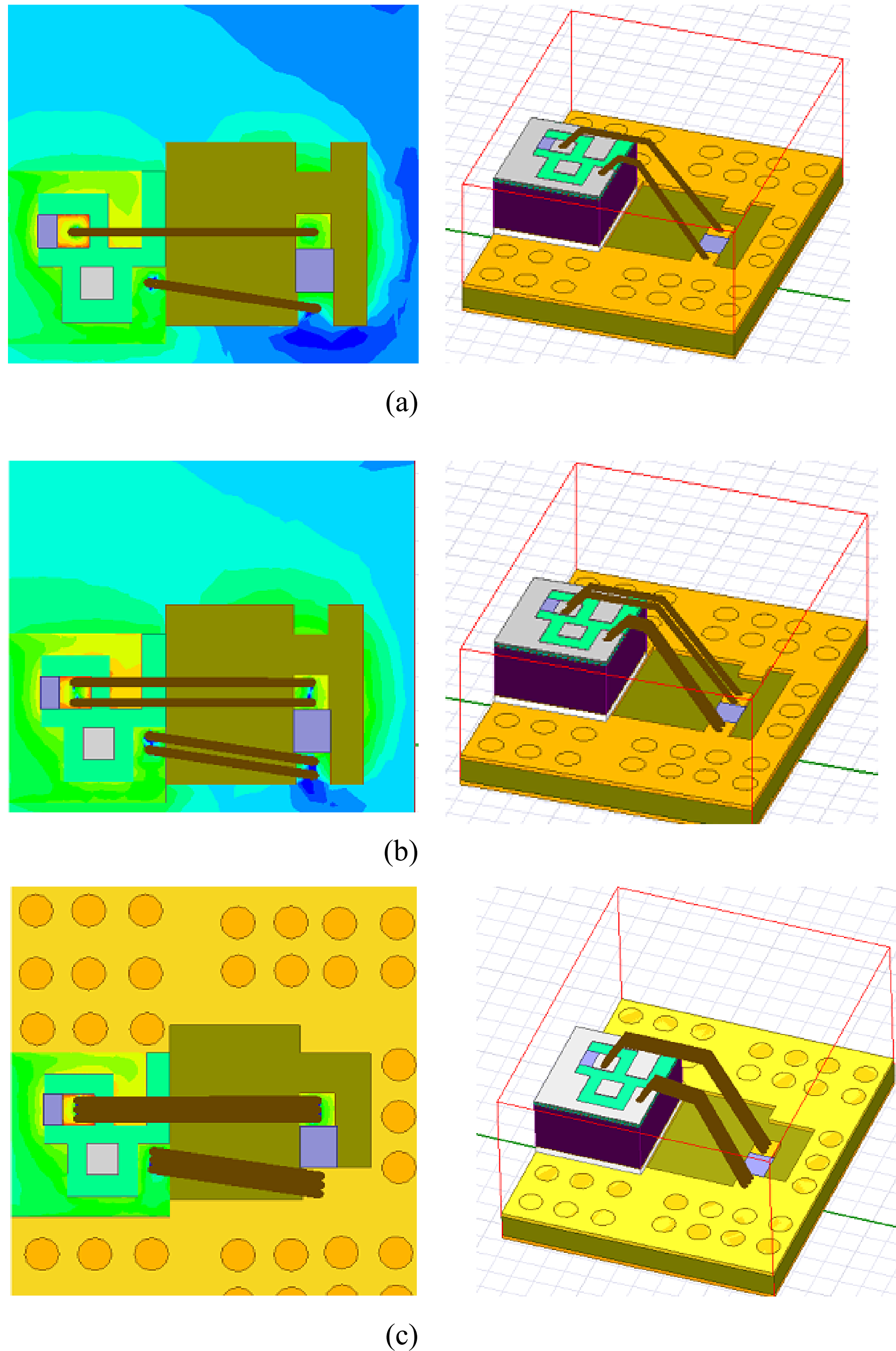

Figure 5.2. Wire-bond models and equivalent radiation field in AED, a) one wire-bond, b) two wire-bonds, c) three wire-bond.

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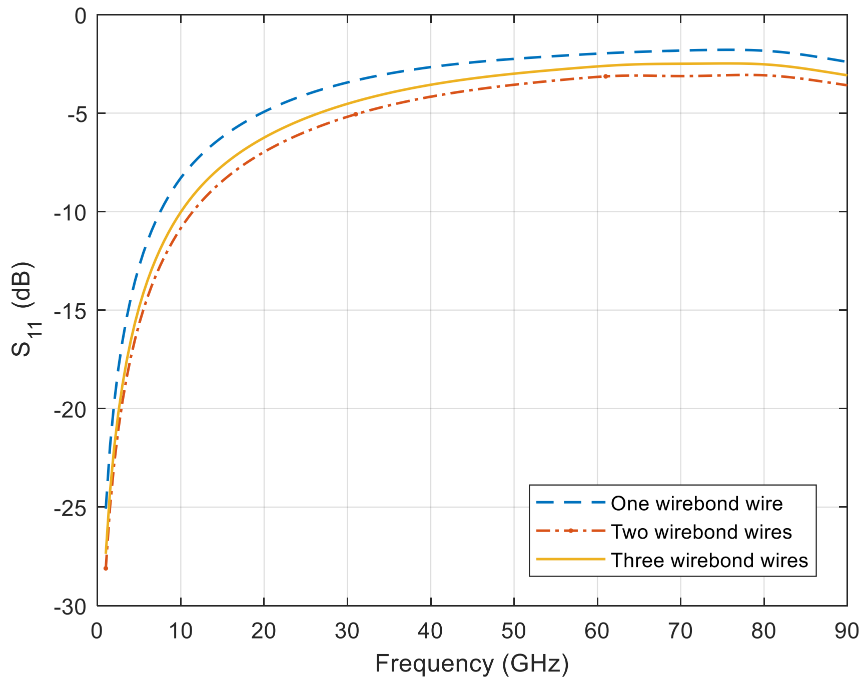

Figure 5.3. Simulated $|S_{11}|$ of the three wire-bond profiles.

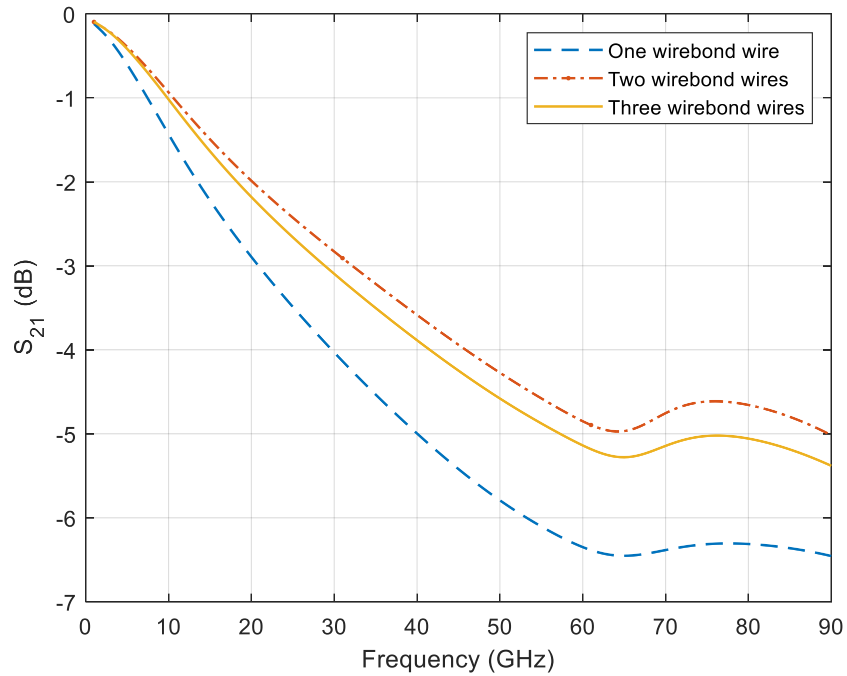

Figure 5.4. Simulated insertion loss of the three wire-bond profiles.

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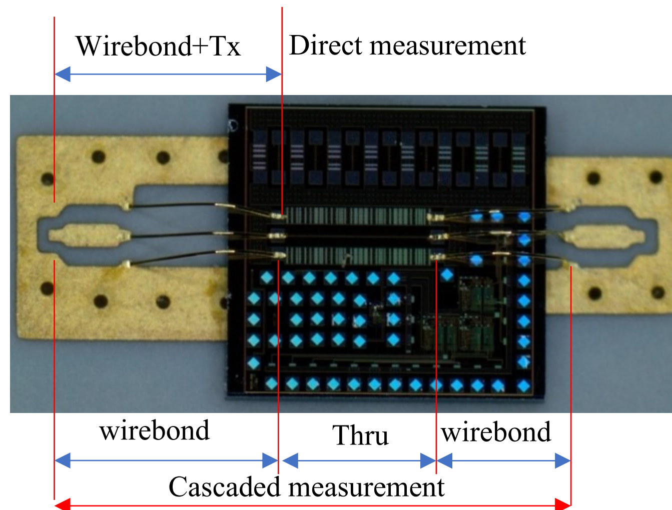
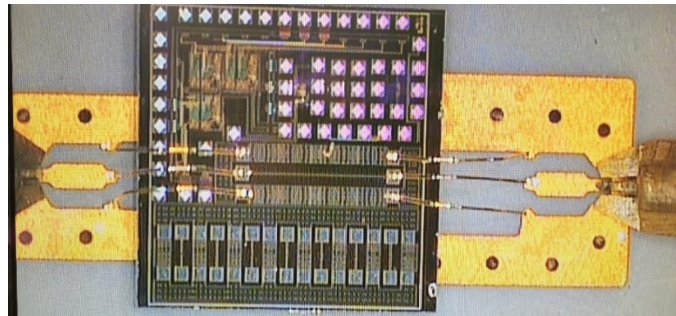
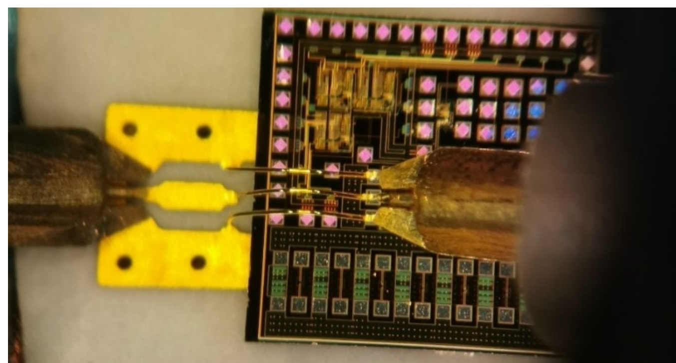


Figure 5.5. Wire-bond characterisation geometry.



(a)



(b)

Figure 5.6. Wire-bond experiment setup, a) PCB-to-PCB measurement, (b) chip-to-PCB measurement.

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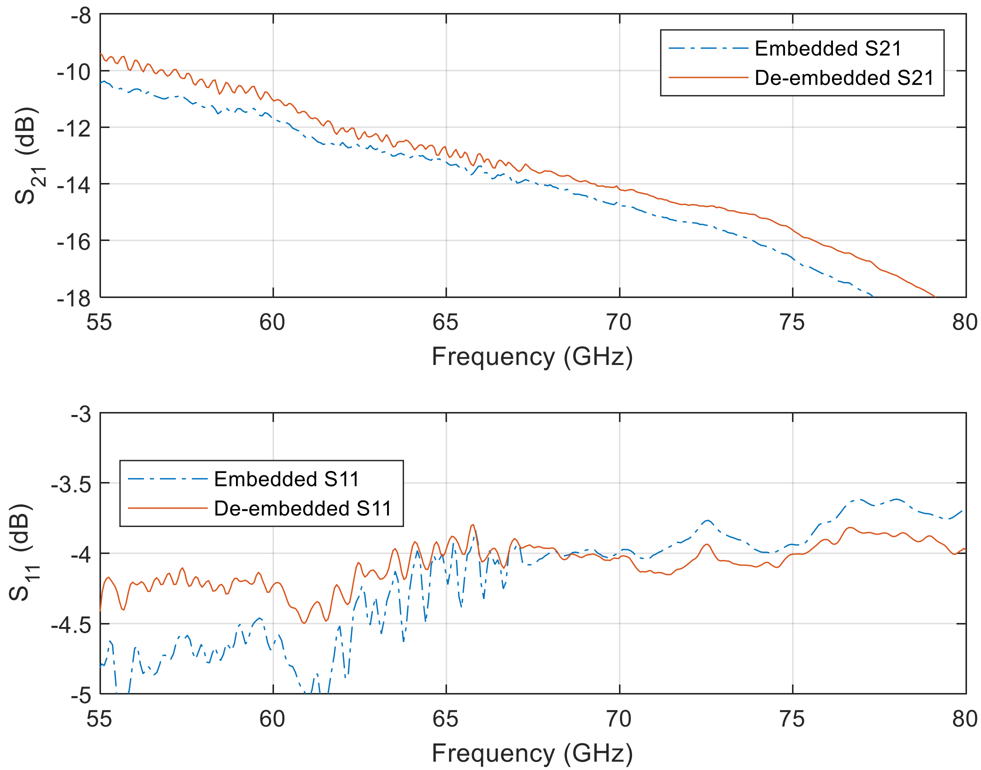

Figure 5.7. Experimental results of the wire-bond transition.

Table 5.1. Comparing RLC from single, double, and triple wire-bond transition at f_0.

Approach	***R*** **(Ω)**	***L*** **(nH)**	***C*** **(fF)**
Single wire (sim)	3.203	0.36	25.03
Double wire (sim)	4.075	0.27	29.2
Triple wire (sim)	2.96	0.29	30.29
Single wire (meas)	9.732	0.34	45.37

5.1.2 Flip-chip characterisation

The flip-chip transition was modelled using the Tin/Silver alloy characteristic for the bumps in AED's material library. For the 3D model of the flip-chip shown in Figure 5.8, a simplified model of the solder balls assumes the shape of the bumps to be reduced to a cylindrical shape

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as reported in [202], [203]. The profile used the solder ball with 60, 50 and 40 µm radius and heights (Figure 5.8). Figure 5.9, Figure 5.10 and Figure 5.11 depict the S-parameter simulation results and the extracted RLC parameters are tabulated in Table 5.2. It can be seen that the flip-chip transition offers much-improved input and output reflection coefficients as opposed to the wire-bond transition in Figure 5.3. Furthermore, the insertion loss of the transition is -1.5 dB to 2 dB between 60 GHz and 70 GHz which was possible by minimizing the bump-to-pad area, as described in [204]. W.r.t the RLC parameters in Table 5.2, it is seen that the effective resistance of the flip-chip transition is much lower than what was obtained by the double wire-bond transition. As a smaller flip-chip interconnect provides improved performance, this could also be due to an increased gap between the solder bumps which reduce mutual coupling. However, the interconnect resistance seems higher than in the case of wire-bond, consistent with the findings in [132] and is relative to the measured resistance of the wire-bond. As a conclusion, the high resistance could therefore be further attributed to the thickness of bumps.

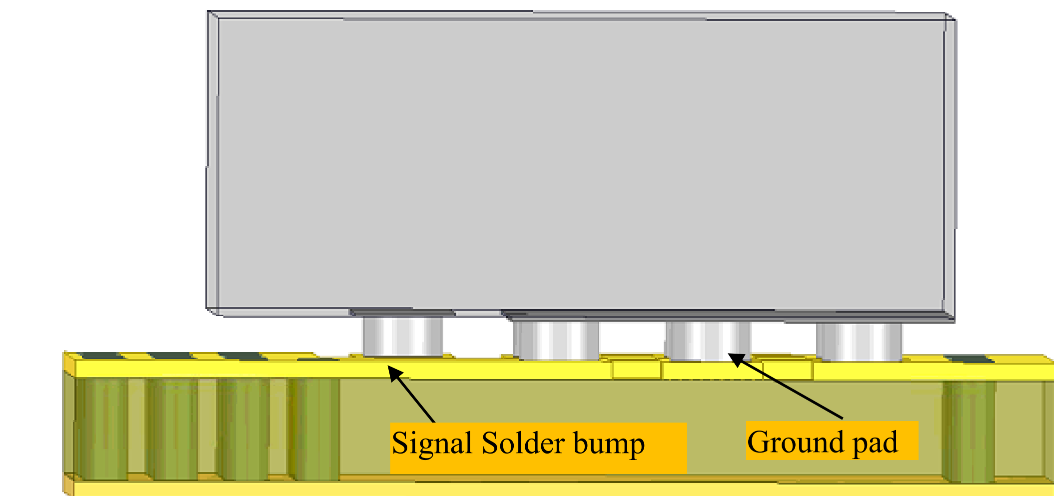

Figure 5.8. EM model of the flip-chip interconnect.

The experimental data of the flip-chip transition is not available due to the unavailability of low volume flip-chip assembly services worldwide. This is attributed to the high cost associated with the process. Many service providers were approached to request their services w.r.t the flip-chip assembly but the effort was unsuccessful multiple times.

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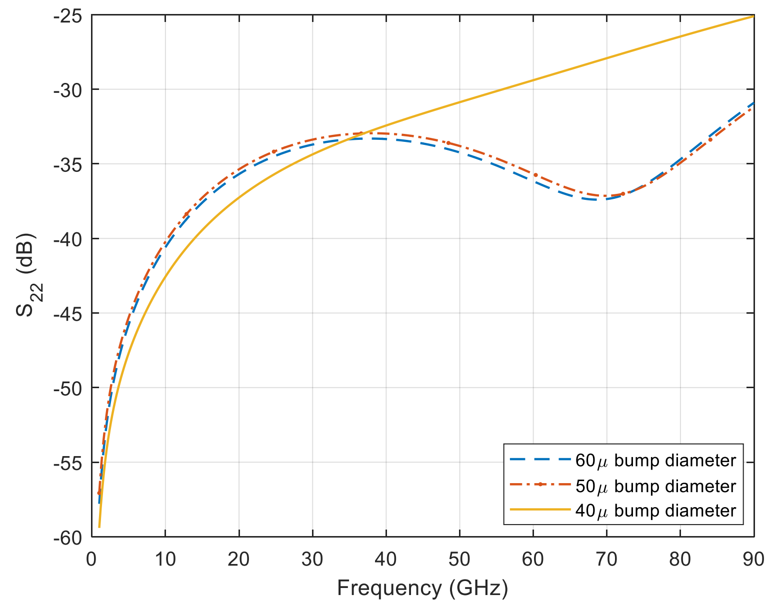

Figure 5.9. Simulated $|S_{22}|$ of the flip-chip transition.

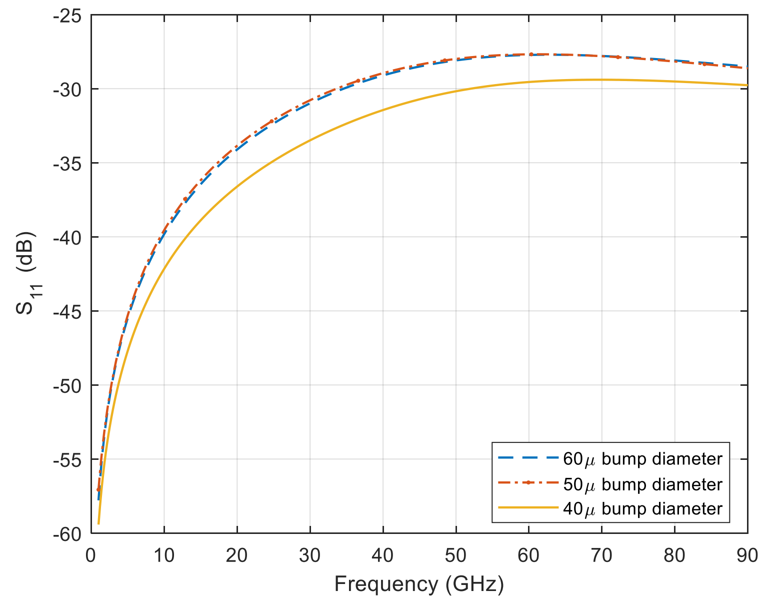

Figure 5.10. Simulated $|S_{11}|$ of the flip-chip transition.

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Table 5.2. Flip-Chip extracted RLC parameters.

Approach	*R* (Ω)	*L* (nH)	*C* (pF)
Simulation (60 µ)	7.051	0.107	27.27
Simulation (50 µ)	7.01	0.106	27.3
Simulation (40 µ)	7.28	0.102	25.87

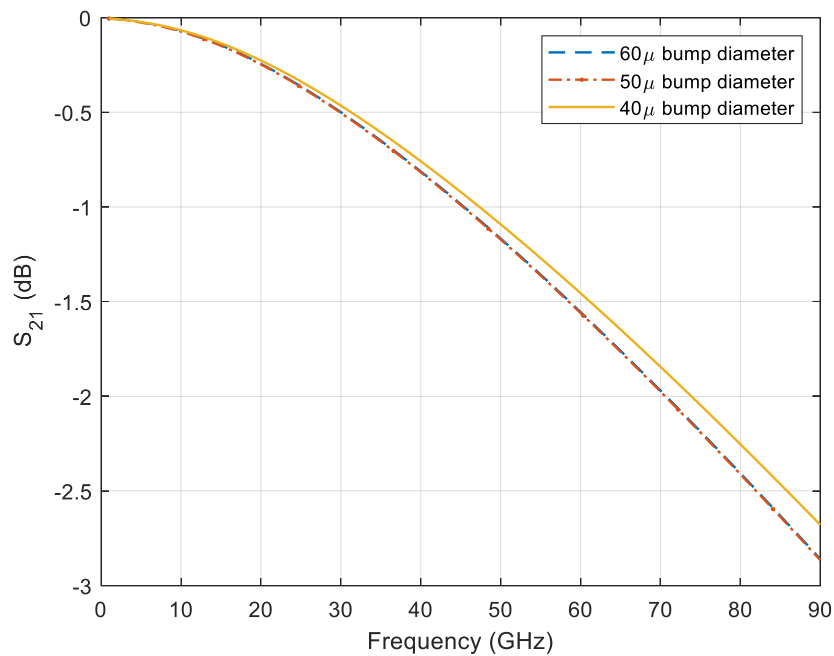

Figure 5.11. The insertion loss of the flip-chip transition.

5.1.3 Ring resonators

Ring resonators were used to characterise the PCB material. The resonators were designed using the design equations as provided in Section 3.6.1.2. The EM model in Figure 5.12 was constructed and simulated in AED. The smallest resonator is for the highest frequency and the largest, for the lowest resonant frequency.

The EM simulation and the experimental results are depicted in Figure 5.14 through to Figure 5.18. The measured S-Parameters results show a slight f_0 shift toward lower frequency, which

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could be due in part to change in the dielectric constant given in 3.1. The 25 µm thick coating of ISIG surface finish used should not affect results significantly, as ISIG is comparable to copper [145], [146]. The variation in the ε_r is reflected in the extracted parameters in Table 5.3, showing an average decrease in the measured ε_r of ± 0.19. The second probable cause of the shift in the f_0 could be the slight increase in the effective radius of the rings as shown in Table **5.3**, due to process tolerance.

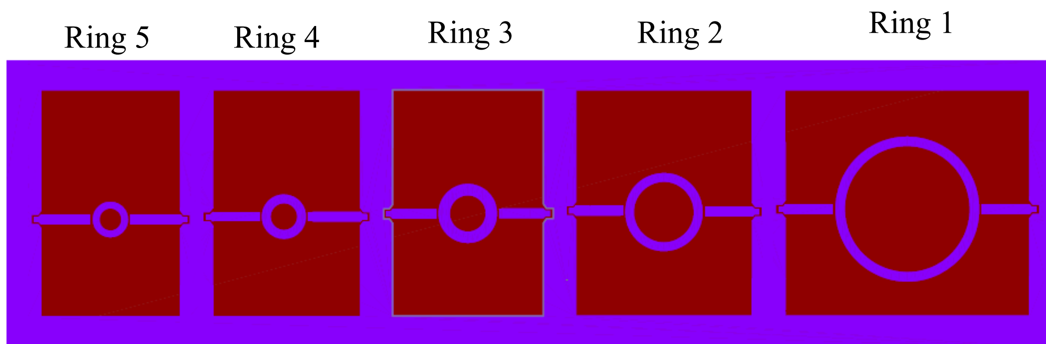

Figure 5.12. The layout for 100, 80, 60, 40, 20 GHz ring resonators.

Table 5.3. Ring resonator experiment summary.

Rings	Radius (µm)		f_0 (GHz)		BW(-3dB)		εr		QL	Qu
	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.	Meas.	Meas.
Ring 1	1300	1353	20	19.8	0.45	0.53	3.372	3.326	66.33	67.00
Ring 2	650	676	40	39.2	1	0.9	3.372	3.149	43.33	44.21
Ring 3	433	467	60	58.7	4	3.5	3.378	3.034	16.77	17.71
Ring 4	325	338	80	78.8	4	2.45	3.323	3.214	31.2	33.39
Ring 5	259	290	100	105.3	9.5	3.3	3.398	3.178	31.91	34.34

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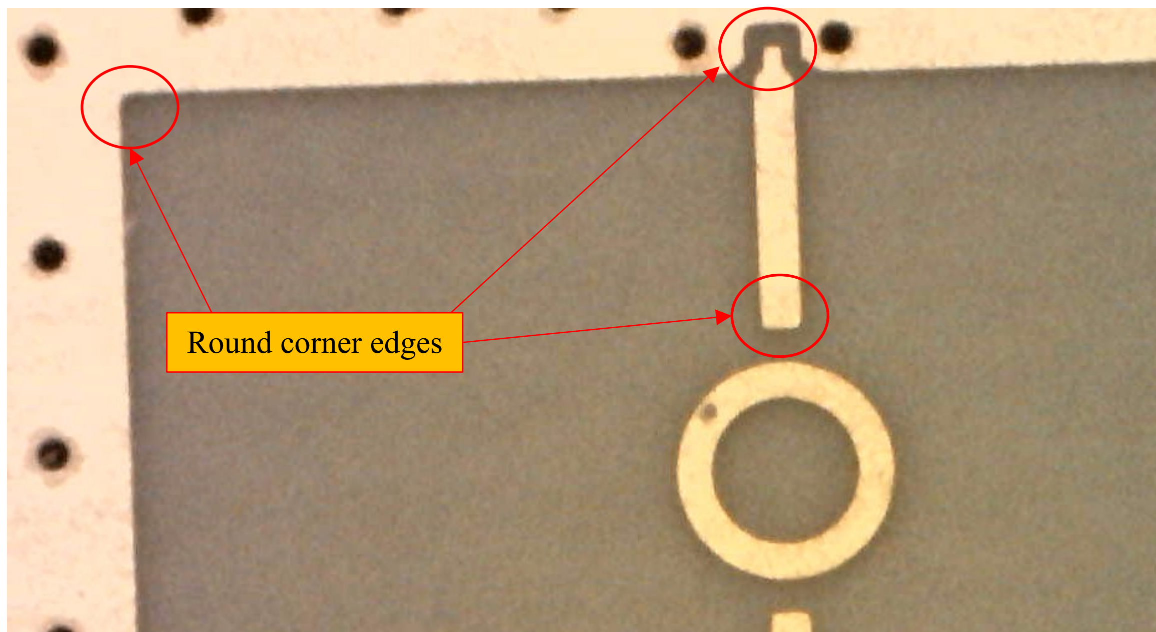

Figure 5.13. Post-fabrication imperfection.

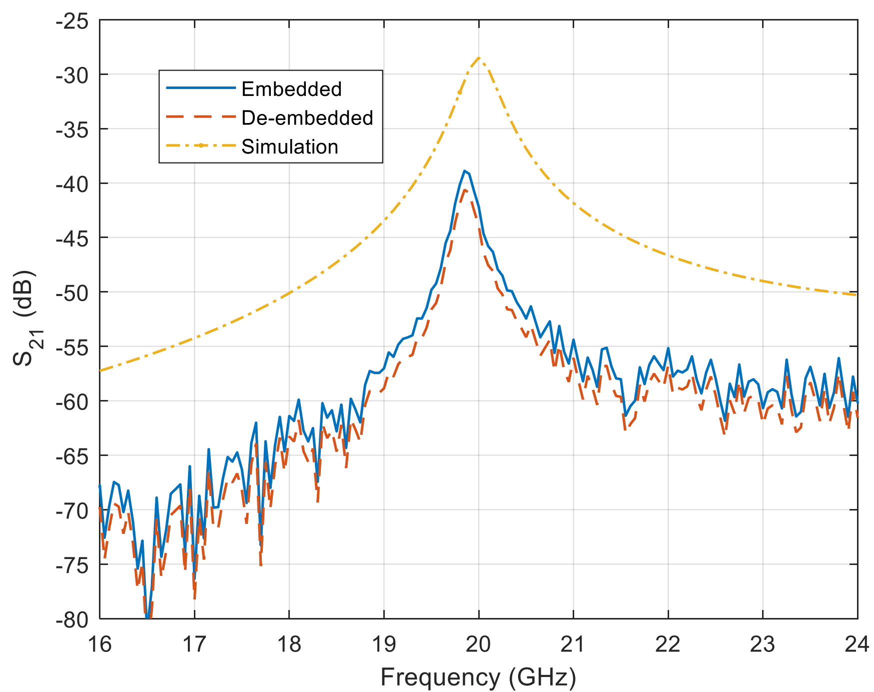

Figure 5.14. 20 GHz ring resonator response.

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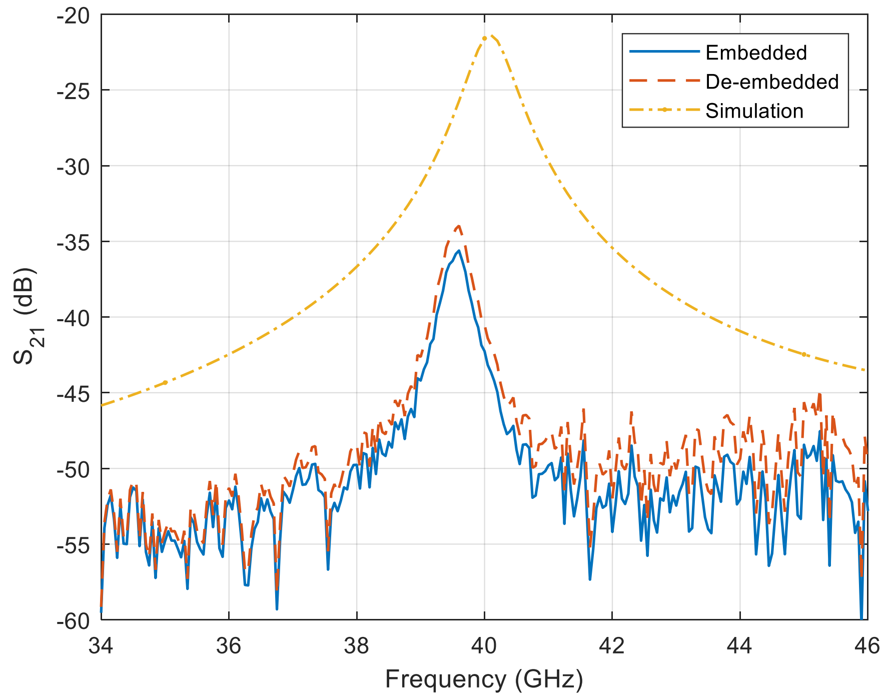

Figure 5.15. 40 GHz ring resonator response.

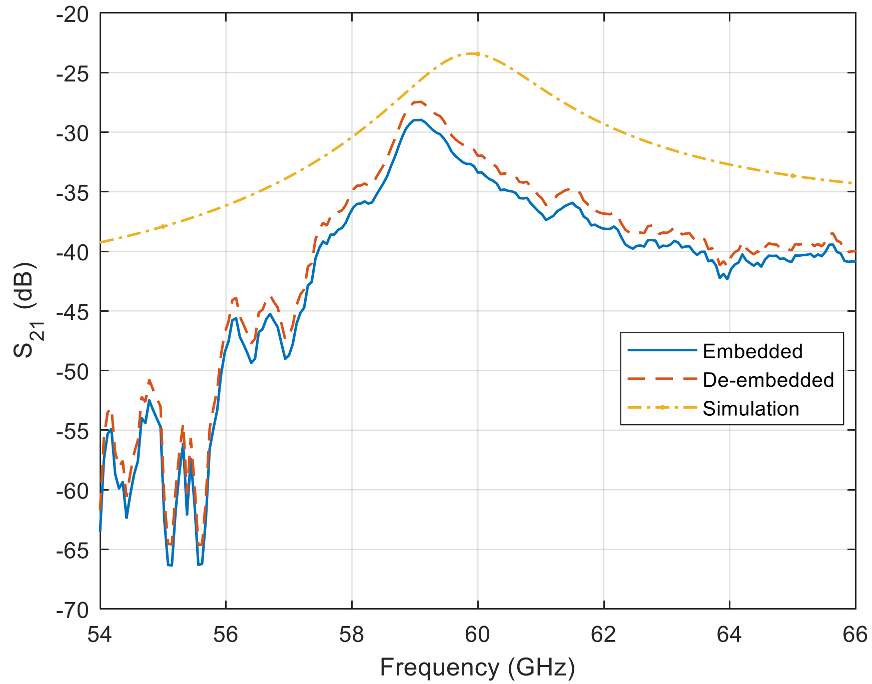

Figure 5.16. 60 GHz ring resonator response.

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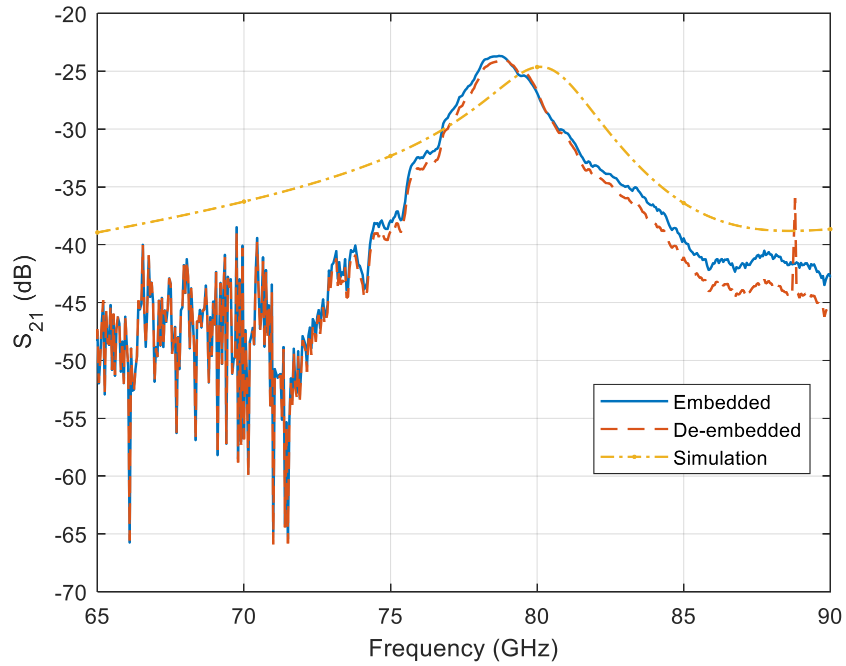

Figure 5.17. 80 GHz resonator response.

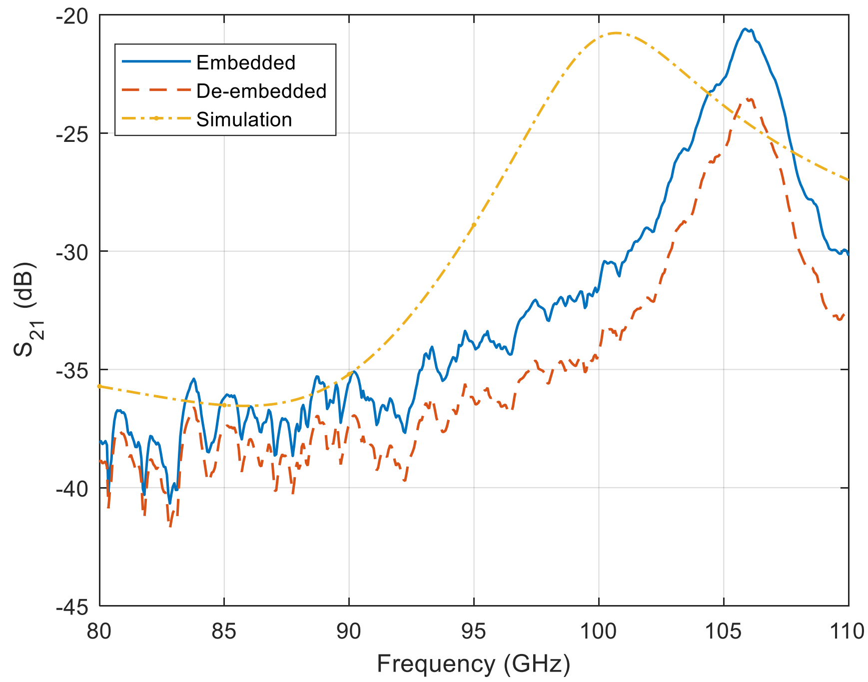

Figure 5.18. 100 GHz ring resonator's response.

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5.1.4 Extraction of the attenuation and the propagation constant

In this section, the attenuation and the propagation constant of the microstrip transmission line are extracted experimentally using the method outlined in [205], as they could not be extracted from the resonators measurements. This is because the attenuation and propagation constants are properties of the transmission line, and not only material parameters as demonstrated in [205], [206]. First, the width of a 50 Ω microstrip transmission line was determined using the Keysight ADS *lineCal* tool. The transmission line was then modelled in AED where the length of 1.776 mm was used. The simulation frequency was selected to cover V-band as shown in Figure 5.20. The measured attenuation constant alpha (α) is 0.6 dB/mm, while a minimal variation is observed between the simulated and the measured phase constant beta (β). A variation of ± 5.46 Ω is observed in Z_0. This could be due to the reduction in the width of the transmission lines during the etching process. The simulated and measured S-Parameters results are presented in Figure 5.20 where the line resonance effect is observed around 60 GHz.

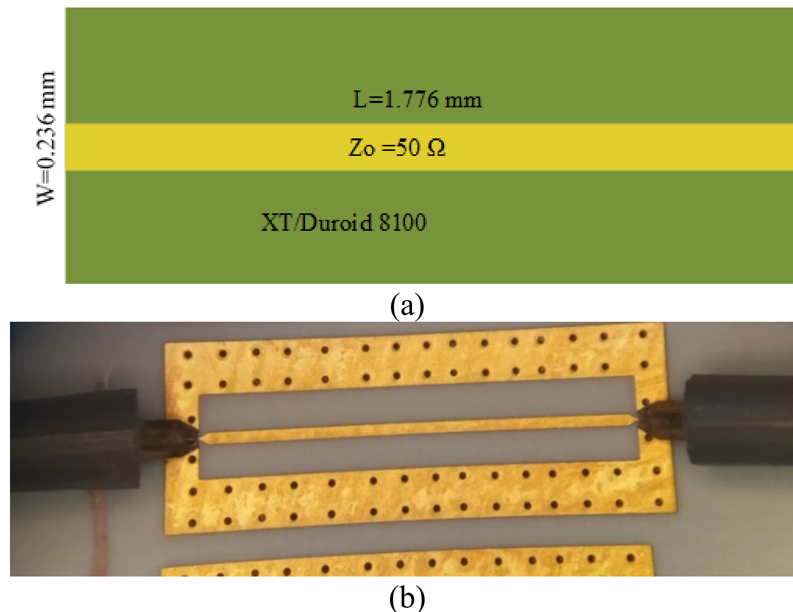

Figure 5.19. Microstrip transmission line. a) simulation model, b) wafer probe measurement of the model.

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Table 5.4. Transmission line parameters.

Parameter		Attenuation constant	Propagation constant	Characteristic impedance
Value at f_o	Sim	0.5 dB/mm	225°/mm	48.5 Ω/µm
	Meas	0.6 dB/mm	223°/mm	53.96 Ω/µm

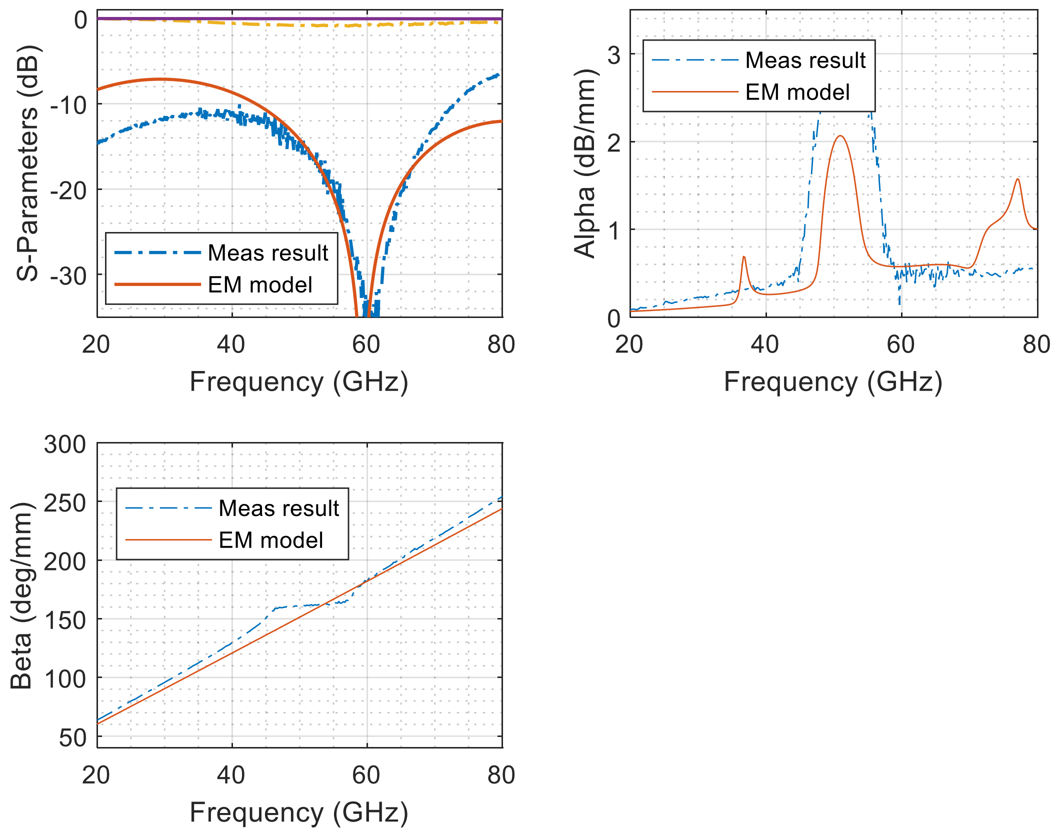

Figure 5.20. Extracted microstrip transmission line parameters.

5.2 MMIC INTEGRATED ON PCB

The MMIC LNA schematic in Figure 4.11 (inside the red area in Figure 5.21) was packaged onto an XT/Duroid 8100 PCB material (indicated within the dashed line in Figure 5.21) in the circuit schematic simulation, using the wire-bond and the flip-chip S-parameters from the EM model simulated in Section 5.1.1 and Section 5.1.2 respectively. The transmission lines from

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the interconnection landing pads on the PCB to the probe pads (see the dashed-dotted line in Figure 5.21) were optimised to improve the input and output reflection.

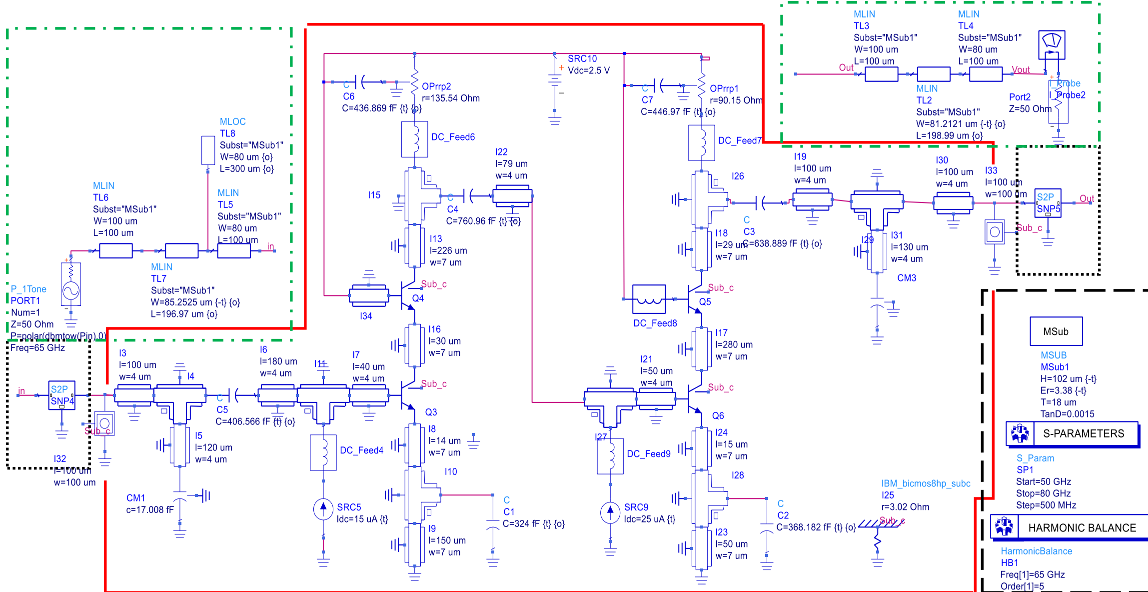

Figure 5.21. Schematic diagram of MMIC-PCB integration.

An additionally opened circuit stub of 300 μm was required at the input of the circuit to absorb wire-bond transition inductance, while a 150 μm line length was required to improve the matching in the case of flip-chip interconnection. All of these designs were done using the optimization tool in Keysight ADS. It is observed in Figure 5.22 that the centre frequency shifts lower in frequency in the case of the flip-chip interconnection.

A reduction in the S_{21} peak of ≈ 3 dB is also observed and is attributed to the interconnect insertion loss. All of these culminate in an increase in NF to ≈ 7.8 dB and an increase of ± 0.55 dB from the MMIC LNA schematic simulation result, using *pcells* alone. Meanwhile, in Figure 5.23, the peak S_{21} is ≈ 10.2 dB. Here, as the length of wire-bond transition $l >> \lambda_g$, the impact on the noise figure was to be expected. Furthermore, the additional stub added at the base further exacerbated the degradation as NF of ≈ 9.74 dB is obtained. Besides the shift in f_0 using flip-chip transitions, 1dB gain flatness bandwidth of ≈ 9 GHz is achieved, while ≈ 5 GHz is achieved in the case of wire-bond transitions.

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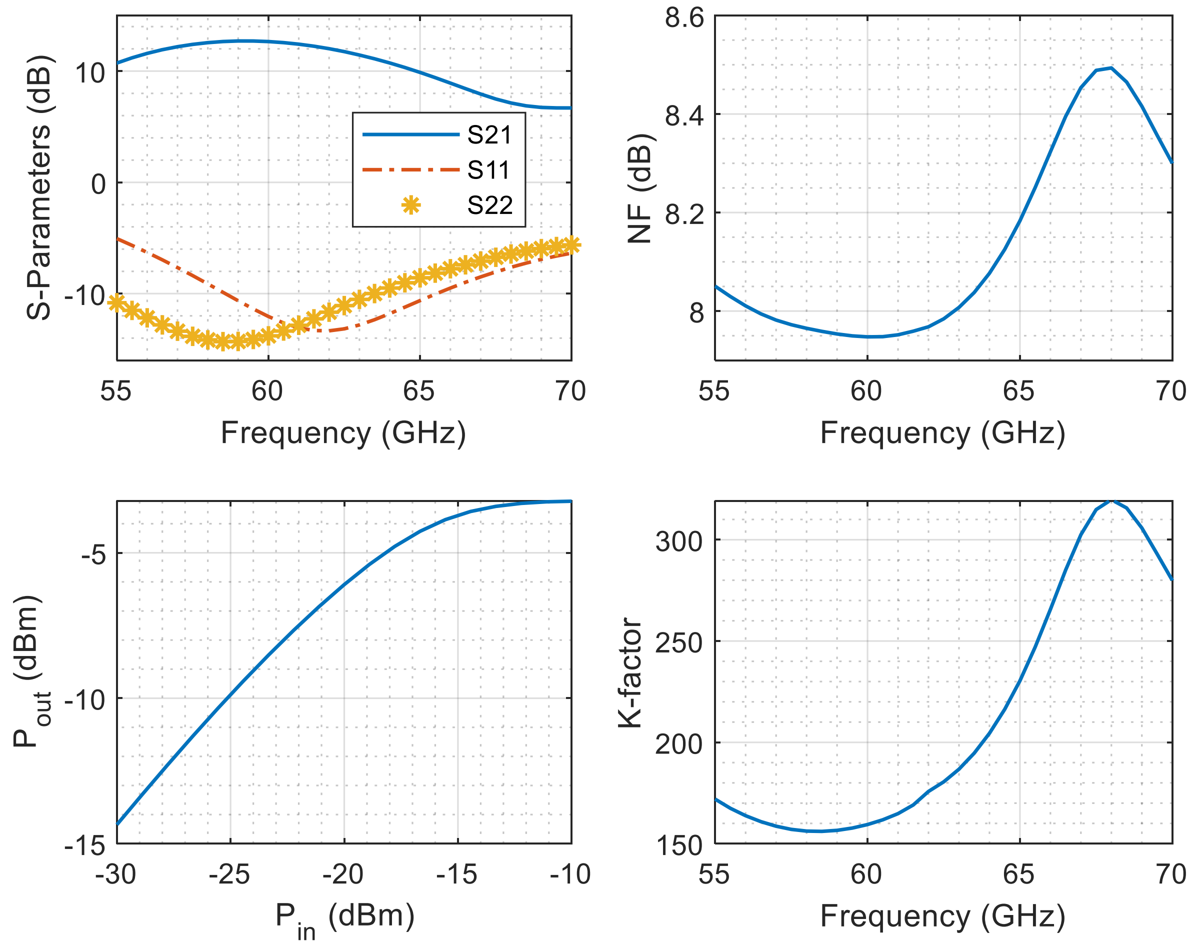

Figure 5.22. Simulation results of the MMIC LNA on PCB with flip-chip interconnects.

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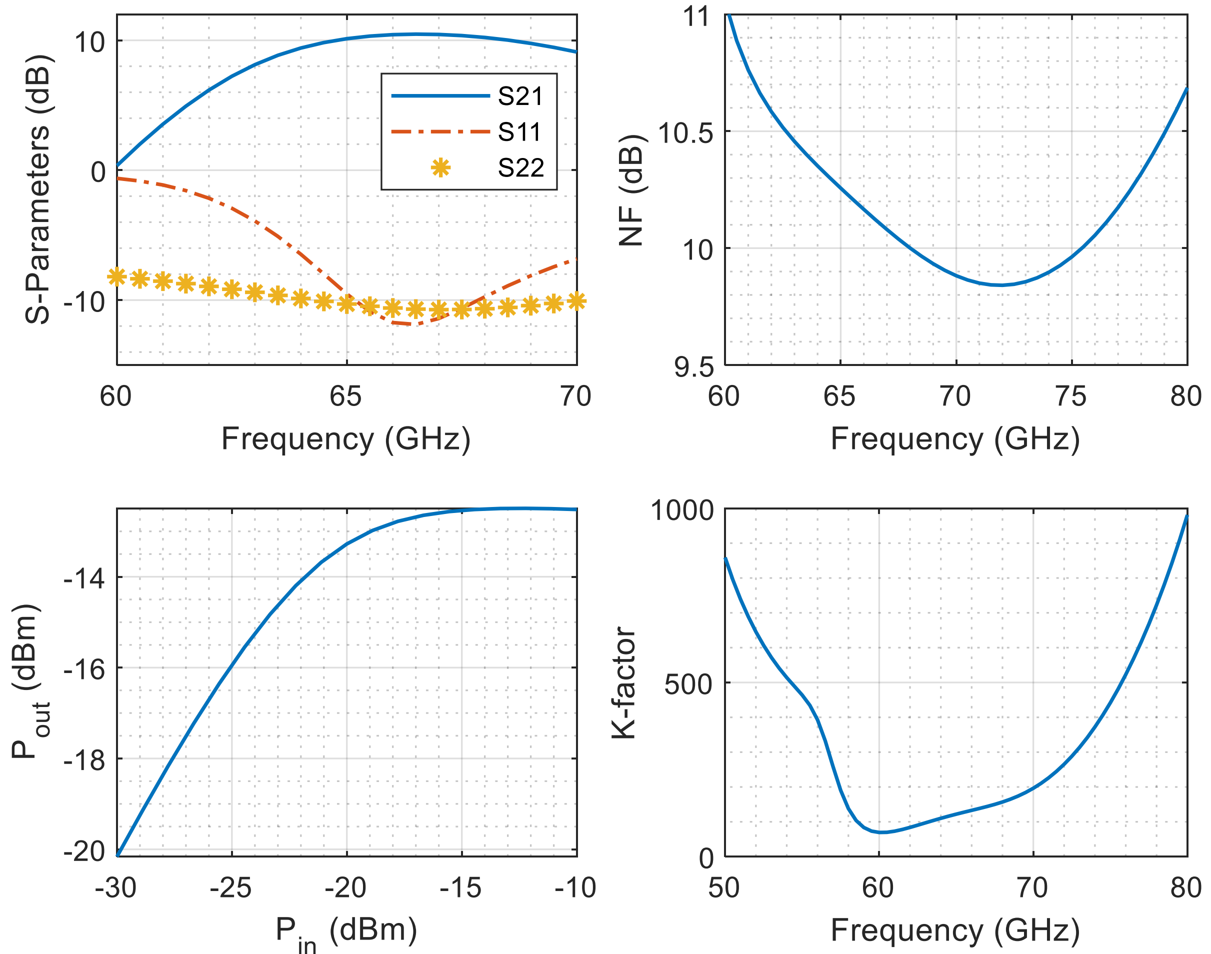

Figure 5.23. Simulation results of the MMIC LNA on PCB with wire-bond interconnects.

5.3 HYBRID LNA DESIGN

5.3.1 Modelling of MMIC transistor transmission lines

For an all-inclusive design, the bond pads and transmission lines leading to the transistors from the pads on-chip were modelled in Ansys Electronics Desktop. The graphs in Figure 5.25 and Figure 5.26 present the responses of the on-chip transmission line leading to both collector and base of the transistor. The IL < 2.5 dB up to 90 GHz, and reflection coefficient of ≈7.5 dB highlighting the necessity of including these lines in the modelling process.

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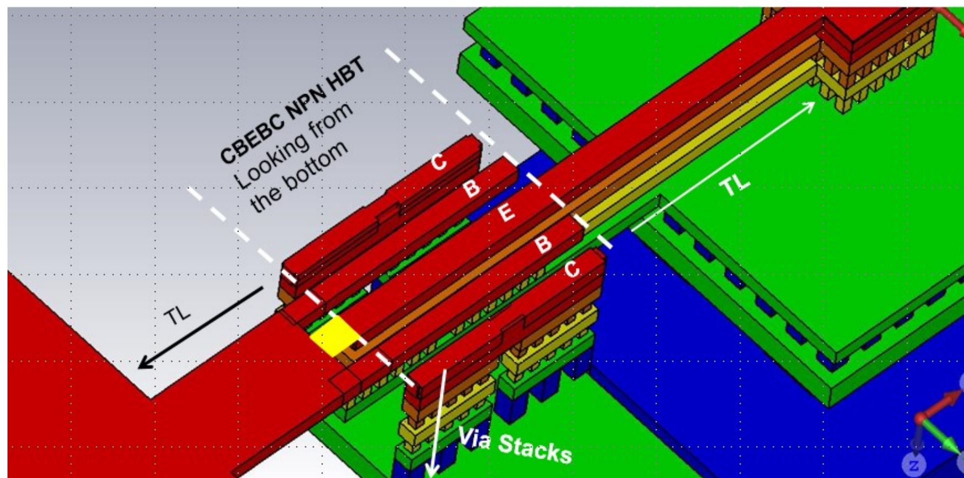

Figure 5.24. Modelling of on-chip transmission lines.

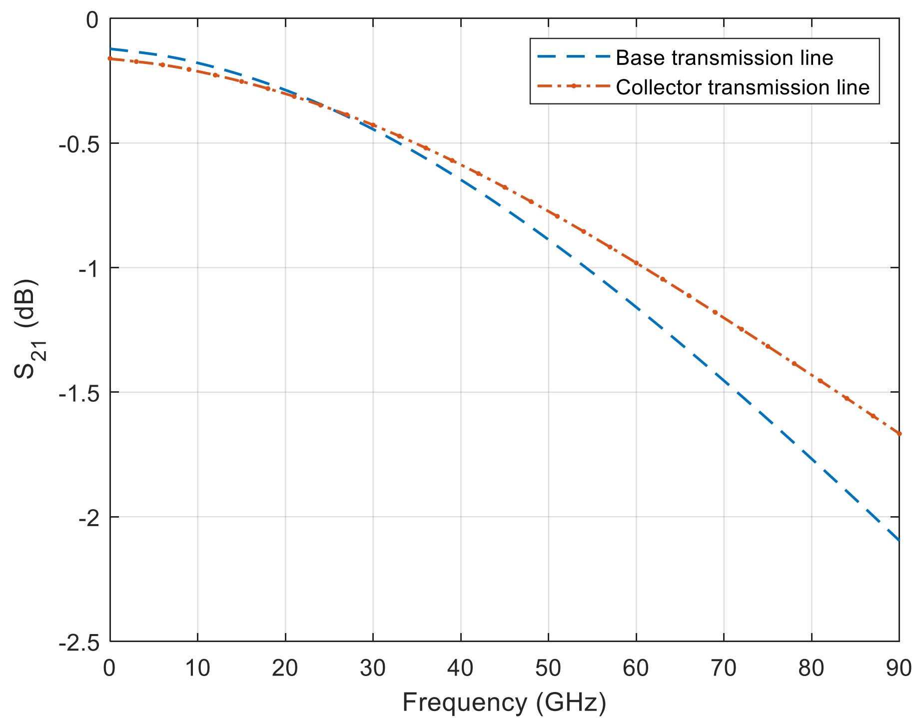

Figure 5.25. Simulated S_{21} of the MMIC transistor's transmission line.

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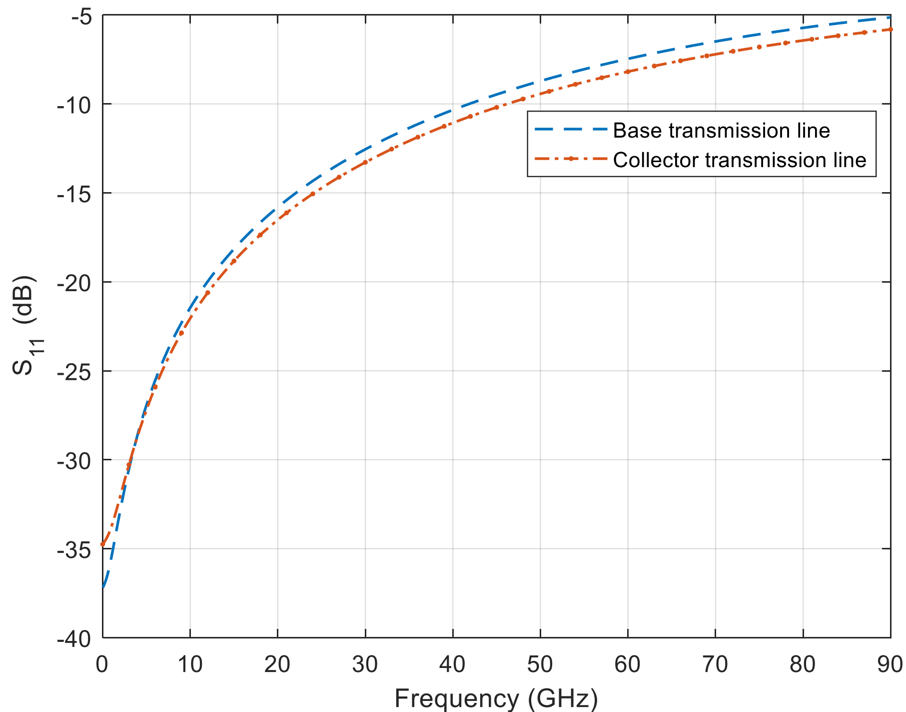

Figure 5.26. Simulated S_{11} of MMIC transistor's transmission line.

5.3.2 Transistor specifications

The transistors used are HBTs fabricated in BiCMOS8HP having an emitter length L_E =4.5 µm and the emitter width $W_E = 0.12$ µm and the DC forward gain of $\beta_{DC} = 450$. The collector-base-emitter-base-collector (CBEBC) configuration was used to provide greater reliability as opposed to the single finger collector base-emitter (CBE) configuration.

5.3.3 Schematic-EM co-design

The layout of the transistor is shown in Figure 3.21 and its subsequent S-parameters were measured in isolation under various bias conditions. From the layout, it can be observed that the emitter of the transistor is directly connected to the on-chip ground which makes it impossible to implement a cascode configuration. A CE design configuration was therefore adopted instead.

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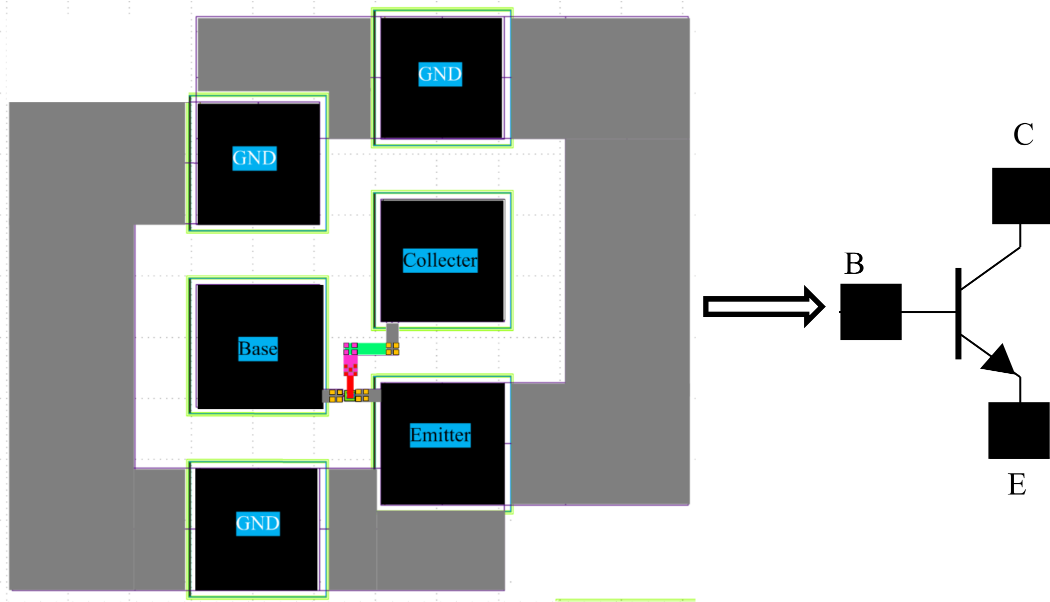

Figure 5.27. BJT transistor fabricated in BiCMOS 8HP process.

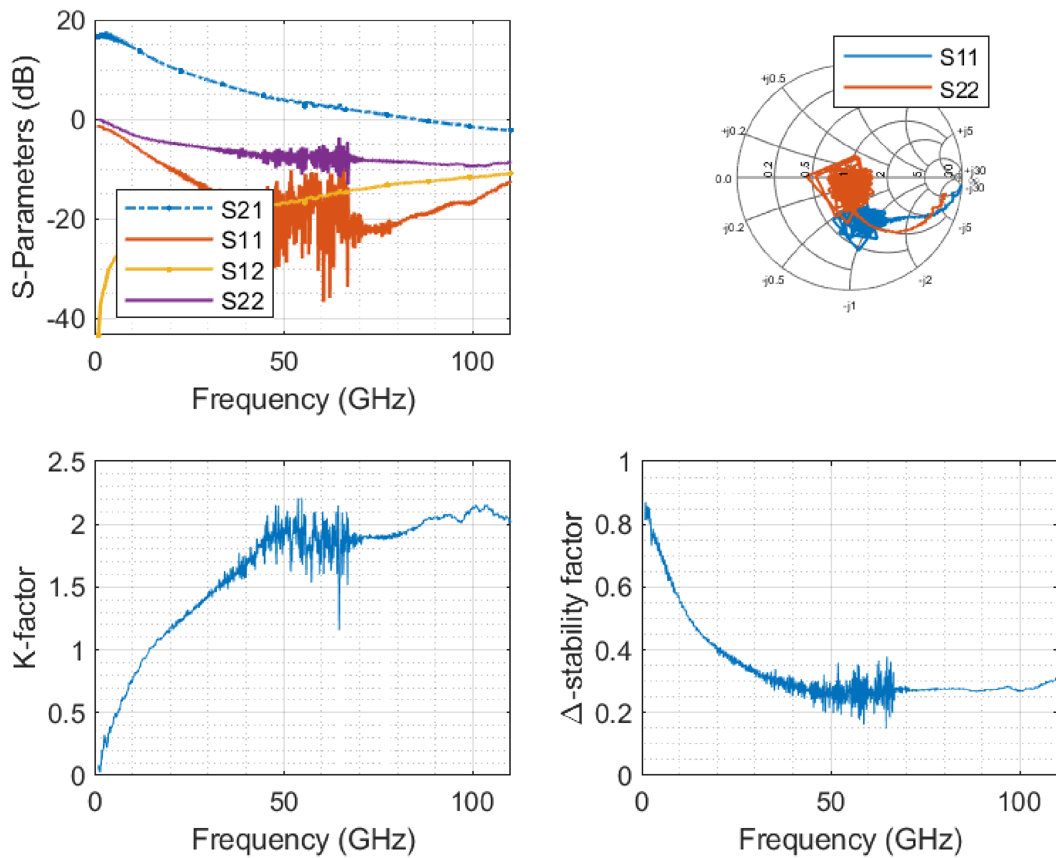

Figure 5.28. S-parameters of the 4.5/0.12 µm HBT.

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5.3.3.1 DC analysis

To ensure that the simulated DC operating point matches the measurement's, I_B was swept against V_{CE} and the point $I_B = \pm$ 11uA and V_{CE} = 1.1V results in the collector current $I_C = \pm$ 3.9 mA as shown from the I-V curve in Figure 5.30. This value is relatively close to $I_C = \pm$ 4.1 mA obtained from the measurements. The model of the transistor in Figure 5.29 includes the on-chip pads and the interconnections from the pads to the transistor's terminals. These are represented by the SnP blocks around the transistor. The inductor across the blocks provides the path for DC, while the capacitor prevents DC from shunting to ground in simulation.

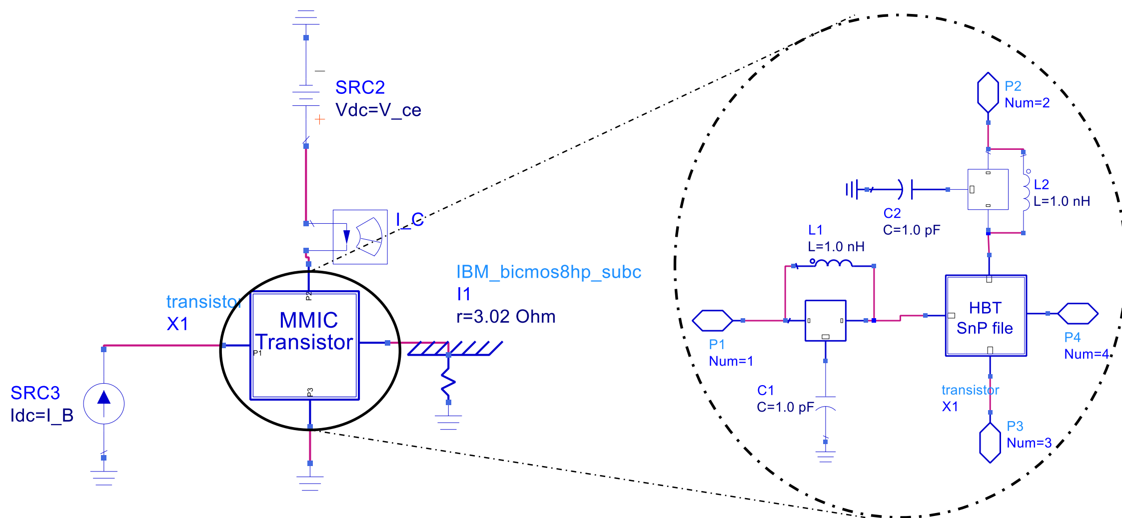

Figure 5.29. Transistor circuit for the DC verification.

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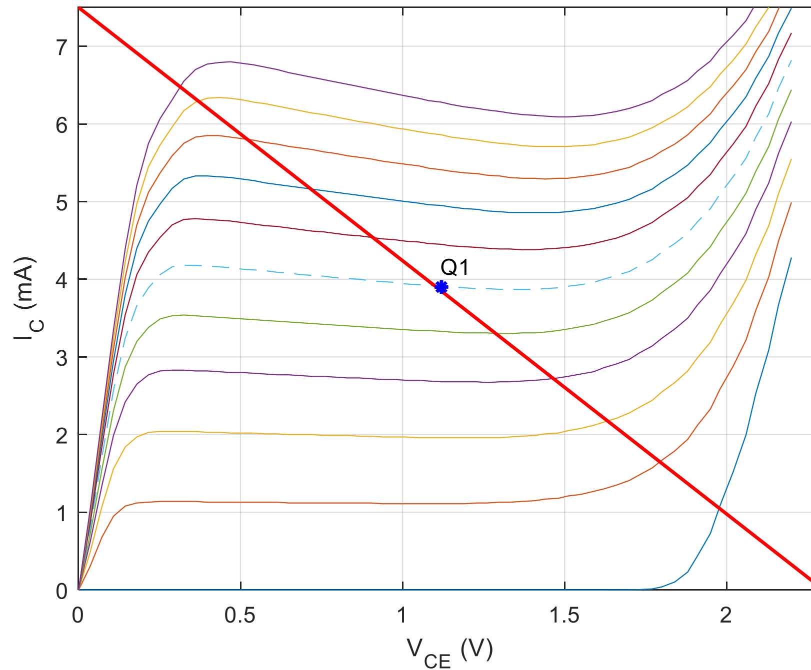

Figure 5.30. Hybrid LNA HBT I-V curve.

5.3.3.2 AC analysis

The MMIC transistor's small-signal results are presented in Table 5.5 for a transistor with a perfect interconnection, with flip-chip connection and wire-bond interconnect. This table reveals significant degradation in the small-signal parameters from flip-chip to wire-bond. For example, the noise figure is degraded from 4.8 dB to 6.12 dB for flip-chip and from 4.8 dB then to 8.4 dB, for wire-bond attachments. A similar trend is observed for other parameters as well.

Table 5.5. Simulated unmatched hybrid LNA parameters.

Parameters	Original design	With Flip-Chip	With Wire-bond
MAG	9.93	5.1	4.66
NF_{min}	4.816	6.124	8.4
S_{11}	-8.92	-9.41	-3.43
S_{22}	-4.72	-12.33	-4.75
Γopt	0.23/48.58	0.15/128.6	0.63/64.94

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5.3.4 Schematic simulation

The inclusion of the wire-bond or flip-chip S-parameters into the LNA schematic simulation drastically affected the performance of the LNA.

In the case of the wire-bond LNA, the source reflection coefficient was selected from MAG/NF Smith chart as Γ_S =0.71/ 81.99°. From this value, the load reflection coefficient of Γ_L = 0.70/ 65.15° was calculated resulting in Z_S=19.25 + j53.82Ω and Z_L=28.28+ 70.45Ω. Three element matching was attempted; however, it was difficult to match S_{11} above 63 GHz without causing instability.

In the case of flip-chip, the source reflection coefficient Γ_S = 0.26 / 74.6° (Z_{in} = 49.5 + j26.3Ω) was selected. This yielded Γ_L = 0.48 / 89.59° (Z_L=31+ j38.99 Ω). The input matching was achieved using a series LC network shown in Figure 5.36.

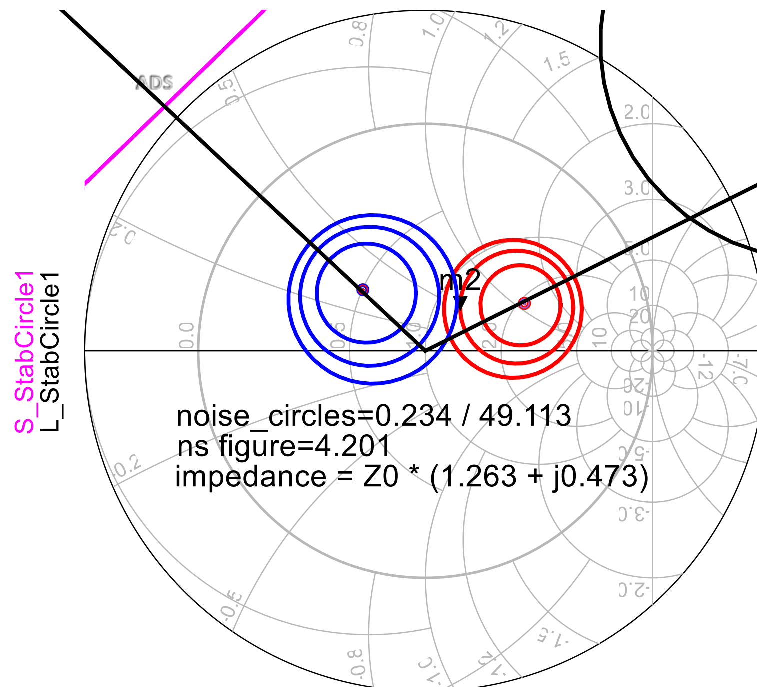

Figure 5.31. MAG, NF_{min}, source and load stability circles for the LNA without any interconnects.

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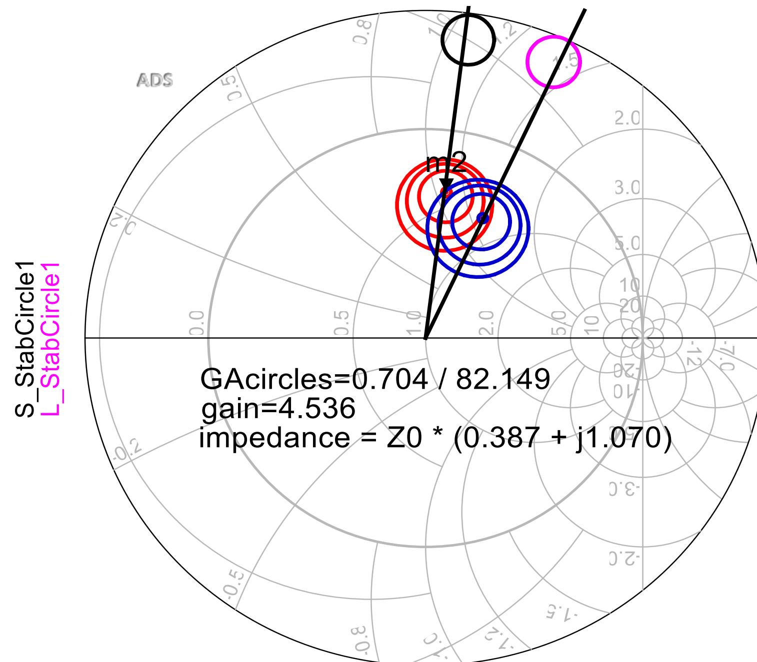

Figure 5.32. MAG, NFmin, source and load stability circles for the LNA with wire-bond interconnects.

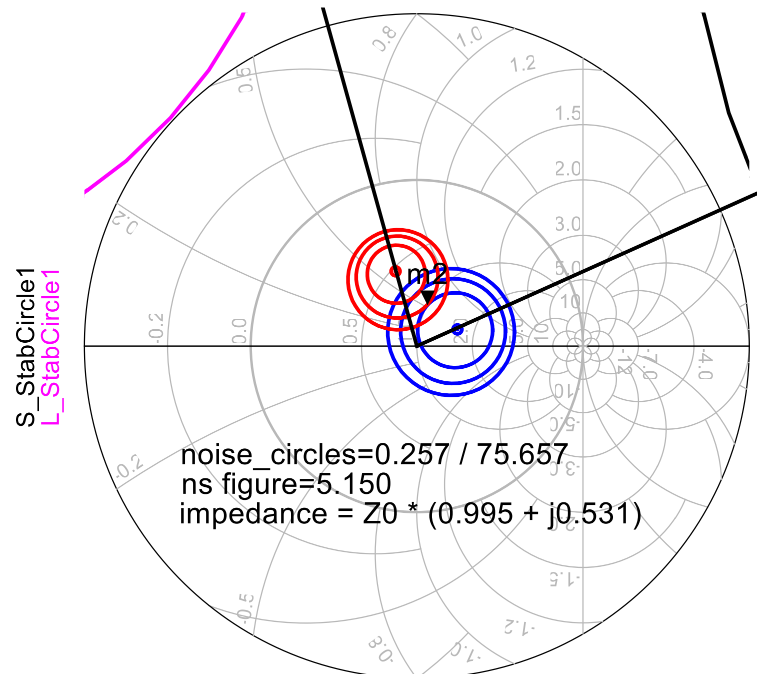

Figure 5.33. MAG, NF_{min}, source and load stability circles for the LNA with flip-chip interconnects.

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Figure 5.34 shows the V-band LNA on PCB using the MMIC transistor's S-parameters, with perfect interconnect and ideal components. The S-parameters and the harmonic balance simulations were conducted to establish the overall performance of all the LNAs. From Figure **5.37**, an NF < 6 dB and the gain > 14 dB with S_{11} and S_{22} below -10 dB across the band is observed. Based on these designs, the circuits in Figure 5.35 and Figure 5.36 were constructed by including the S-Parameters of the wire-bond and flip-chip transitions to the schematics respectively. The circuits were then re-matched with these components in place. Three element matching was used for the wire-bond hybrid LNA. This was transformed into a bandpass network that provided DC decoupling and provided a matching network. The flip-chip topology, on the other hand, used two-element matching. This was implemented with a bandpass network using coupled transmission lines. The component values are as indicated in Figure 5.35 and Figure 5.36, and the simulation results are shown in Figure 5.38 and Figure **5.39** respectively. The wire-bond LNA achieves an S_{21} peak of ≈ 5 dB, NF_{min} of 10.42 dB with < -10 dB S_{11} bandwidth of 3 GHz. The flip-chip LNA achieves S_{21} peak of ≈ 10 dB, NF_{min} ≈ 7.52 dB with < -10 dB S_{11} bandwidth of > 10 GHz.

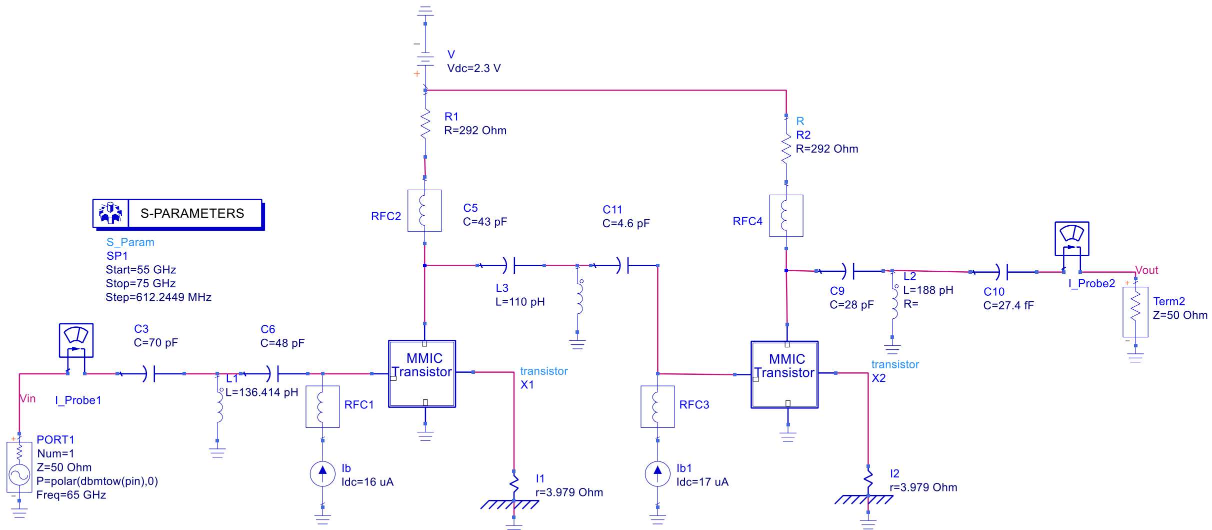

Figure 5.34. LNA matched with ideal components using on-chip HBT's SnP file with perfect transitions to off-chip.

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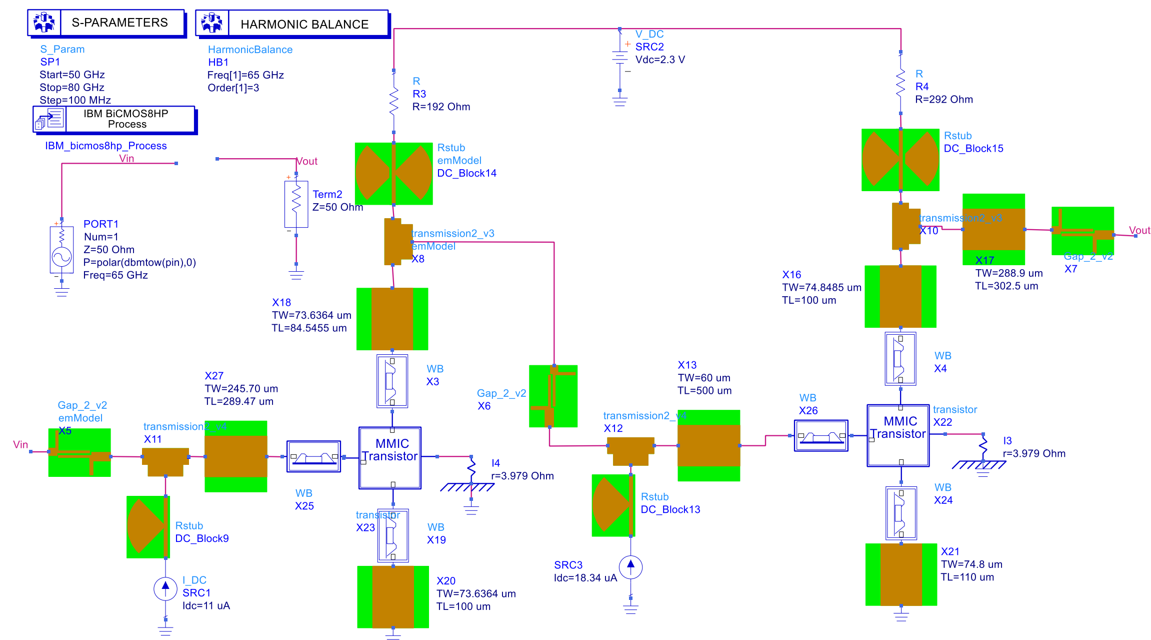

Figure 5.35. LNA with EM model of distributed components using wire-bond transitions and on-chip's HBT SnP files.

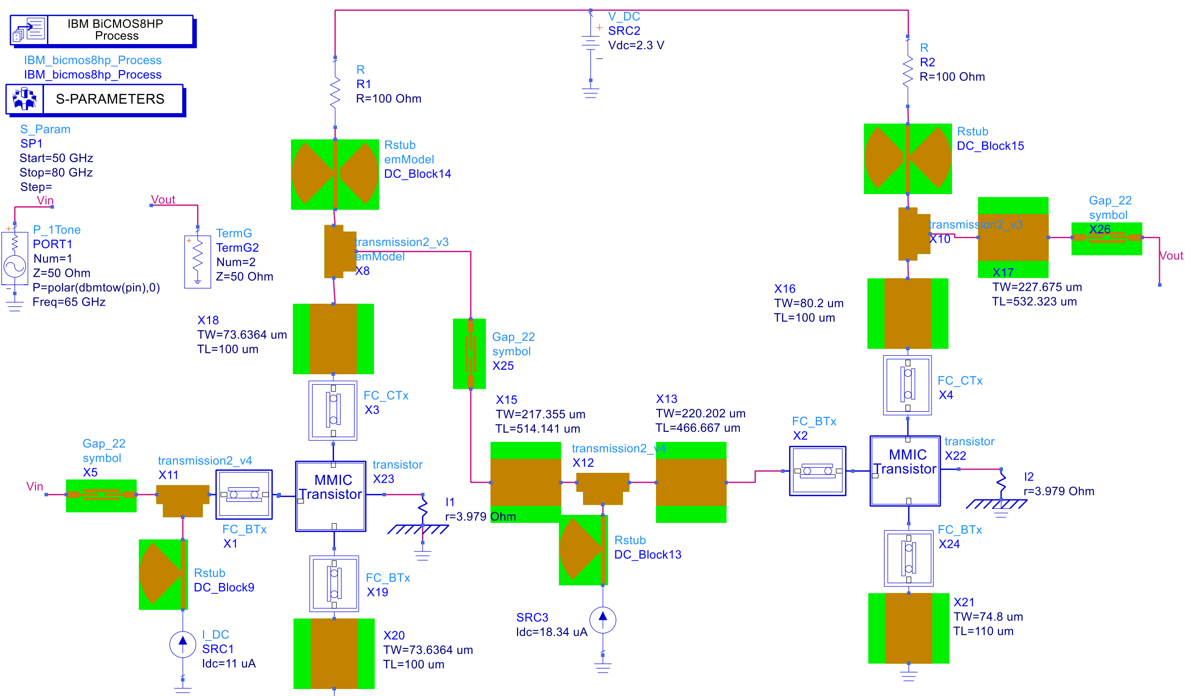

Figure 5.36. LNA with EM model of distributed components using flip-chip transitions and on-chip's HBT SnP files.

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The ideal components in both cases were replaced with the EM model transmission lines, PCB capacitors and radial stubs, as shown. This inclusion further exacerbated the performance degradation of wire-bond LNA, which was already poor due to the S-parameters of the wire-bond interconnect. As a result, the broadband S_{11} match in the frequency of interest was not possible as shown in Figure 5.38. Table 5.6 provides a parametric comparison of these three LNAs.

It can be observed that flip-chip interconnect performs better at mm-wave frequencies compared to wire-bond interconnects in both the MMIC attachment to PCB and the hybrid LNA. This is consistent with findings reported in [138], even though GaAs transistors were used instead of the SiGe ones used in this study.

Of particular interest is the noise figure degradation (9.74 dB and 10.4 dB for wire-bond LNAs), which could be attributed to the high insertion incurred by the wire-bond transitions. It is important to note that MMIC LNA performs better compared to either integrated LNA, but the MMIC LNA with flip-chip attachment has a better 1dB gain flatness bandwidth overall its counterparts.

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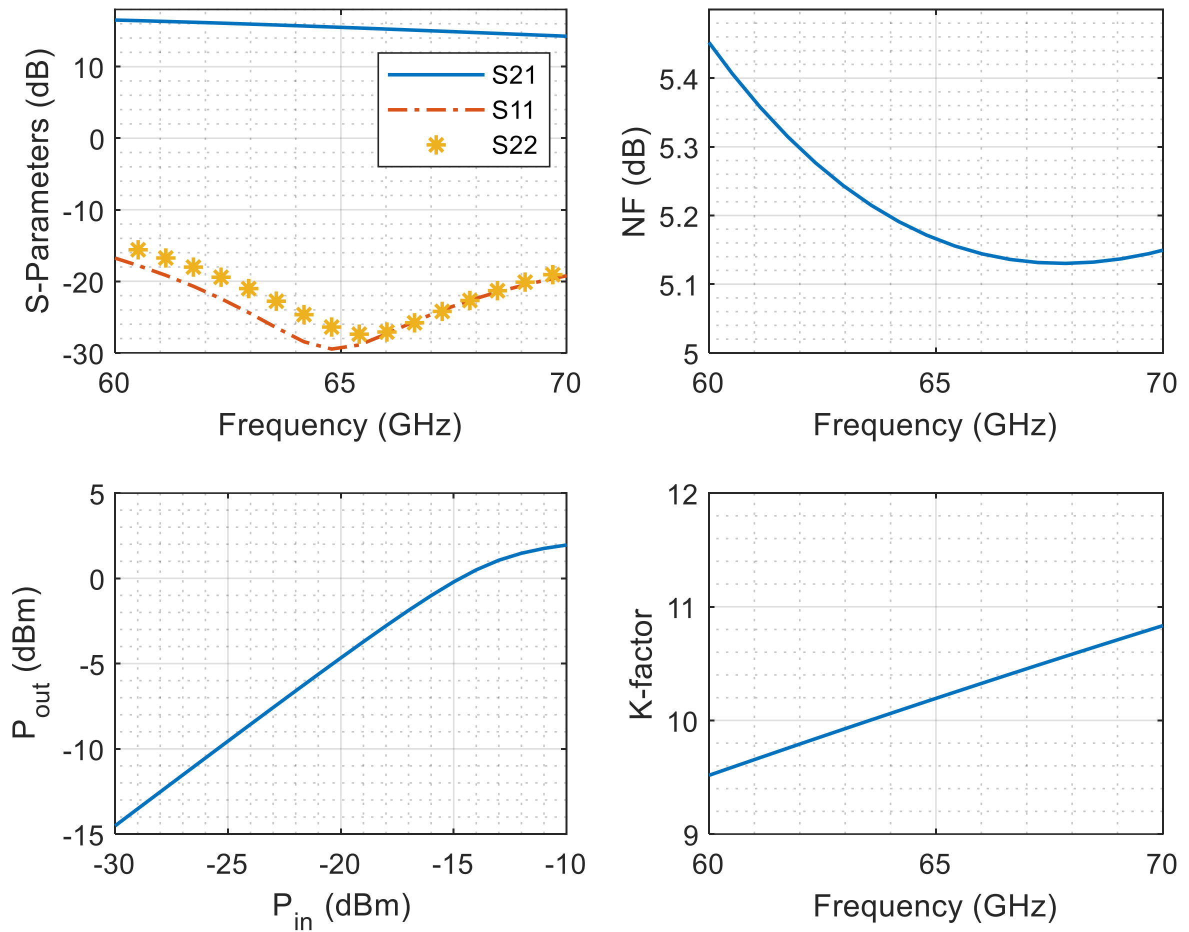

Figure 5.37. The simulation results of the hybrid LNA with perfect interconnects.

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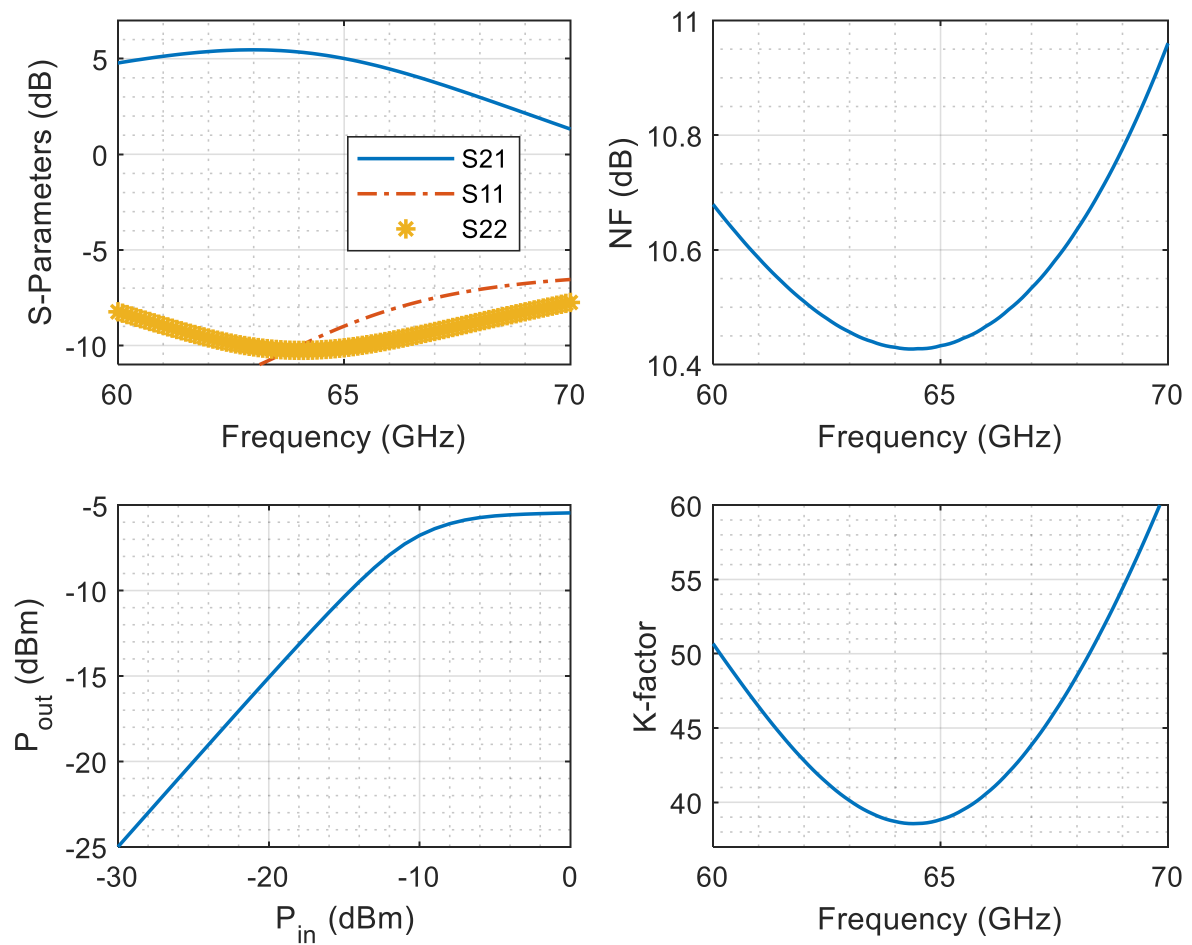

Figure 5.38. The simulation results of the hybrid LNA with wire-bond interconnects.

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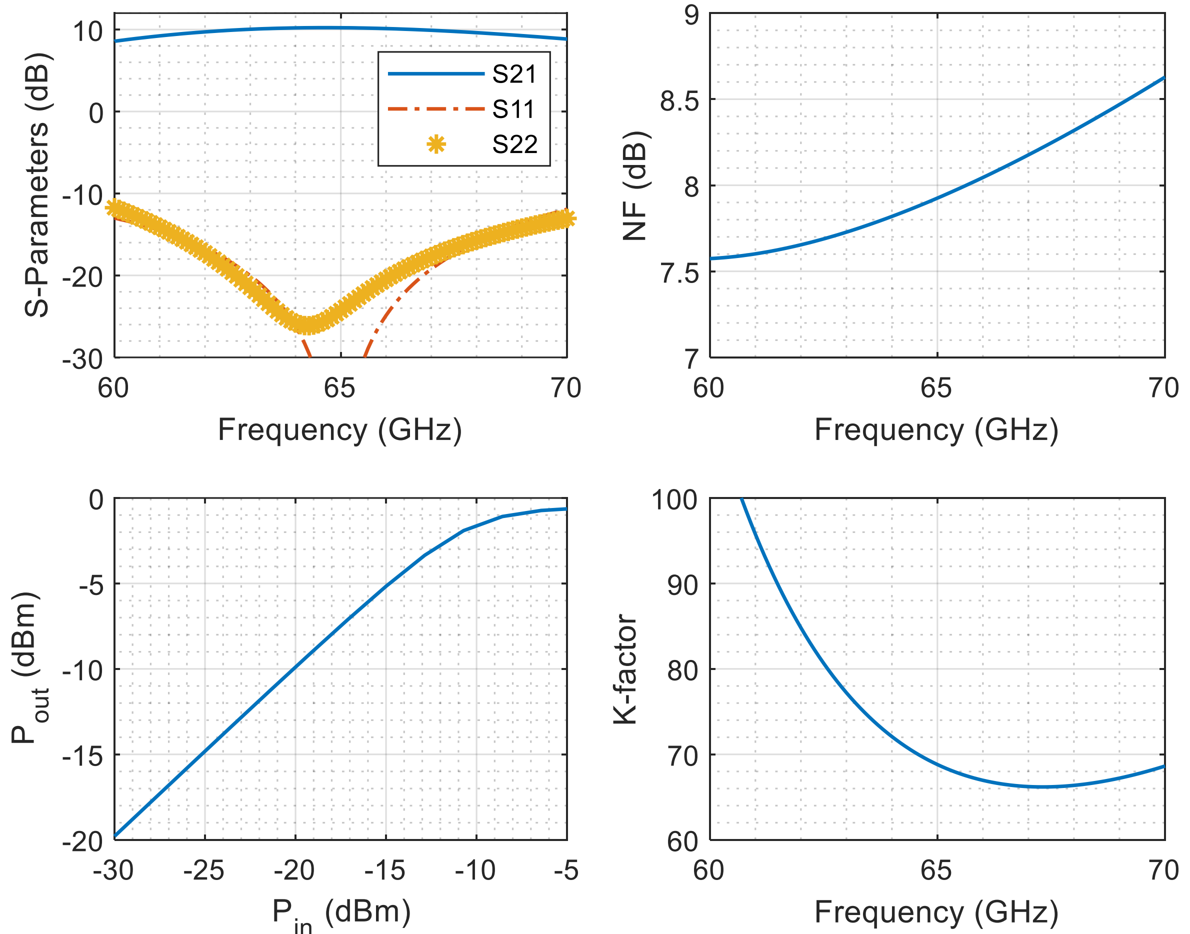

Figure 5.39. The simulation results of the hybrid LNA with flip-chip interconnects.

These are also consistent with the finding in [109], regardless of the process technology and the integration medium. It can therefore be concluded that the flip-chip interconnection is a promising solution for mm-wave hybrid designs. In the case of LNAs for example, once the first stage is optimized for noise figure, more gain stages could be cascaded to increase the gain. A shorter turnaround time is a major advantage of this approach, as it allows for multiple iterations within a short time as compared to MMIC prototyping turnaround. Furthermore, this solution provides the option of reworking / repair in case of component failure, unlike having to discard the device altogether as in the case of the MMIC.

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Table 5.6. Comparison between MMIC LNA, MMIC LNA/PCB, and hybrid LNA.

Integration	**MMIC LNA**	**MMIC LNA on PCB**		**Hybrid LNA on PCB**	
topology	***pcell* alone**	**wire-bond**	**flip-chip**	**wire-bond**	**Flip-chip**
Frequency	60 – 70	60 –70	60 –70	60 –70	60 –70
f_0 **(GHz)**	65.2	66.5	60	63.2	64.5
$\|S_{21}\|$ **@** f_0 **(dB)**	15.2	10.2	12.2	5.05	10
$\|S_{11}\|$ **@** f_0 **(dB)**	< -12	-12	< -12	-10	< -20
NF @ f_0 **(dB)**	7.25	9.74	7.8	10.4	7.9
1dB GFBW	> 6	± 5	±8	± 5.5	>10
IP1dB (dBm)	-14	-22	-17.3	-10	-10

5.3.5 Off-chip passive devices

This section discusses the modelling, simulation, and results of the passive components off-chip. These include decoupling and bypassing PCB capacitors, the radial stubs, and the chip capacitors samples from the American Technical Ceramics (ATC).

5.3.5.1 PCB capacitors

A few PCB capacitors were investigated from the interdigital and gap capacitors discussed in [207]. These capacitors require extremely small gaps to increase their capacitance, which was a challenge based on PCB process limitations. A coupled transmission line structure in Figure **5.41** was first investigated as a solution. In this case, a λ/4 coupled line was used and tuned such that the resonance occurs near the designed f_0. To obtain a bandpass response, two opened circuited (OC) stub resonators were added at each end of the coupled line (Figure **5.41**(a)). Each of the stubs introduced a pole [208] centred at 62 GHz and 68 GHz. Good input and output matching to 50 Ω was achieved by adjusting the width of the stubs. The required width of the input stub (TL4) was 100 µm which result in Zc = ±74 Ω. The output stub (TL3) width was synthesised to be 74.37 µm, translating to Zc = ± 84 Ω. The bandwidth of the passband was optimized by tuning the length of the stubs, the width and the separation of the coupled line.

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The schematic and EM model of the structure shown in Figure 5.41 were constructed in Keysight ADS and Ansys Electronics Desktop respectively. The subsequent simulation and measurement results are shown in Figure 5.42. An *IL* below -1 dB is achieved with 21.58% fractional bandwidth (FBW) based on the EM model. The measurement result shows a good agreement with the EM model achieving an *IL* of -1.3 dB and -3dB FBW of 25%.

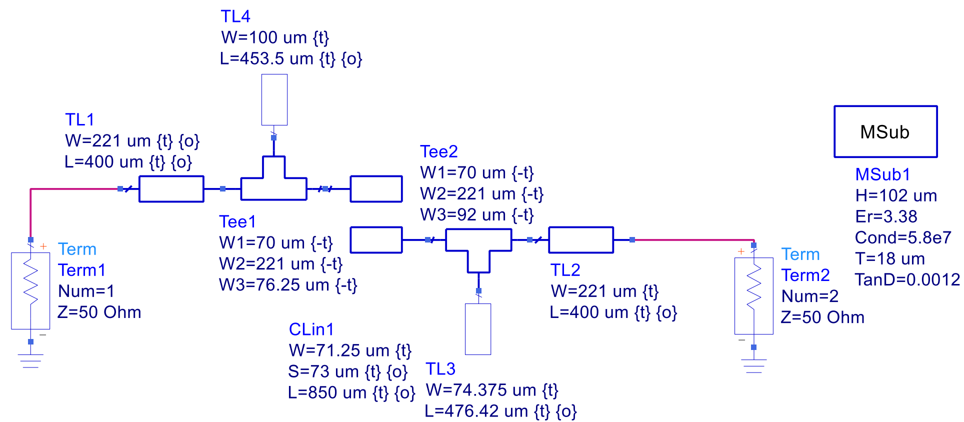

Figure 5.40. Schematic diagram of the coupled line capacitor with OCS.

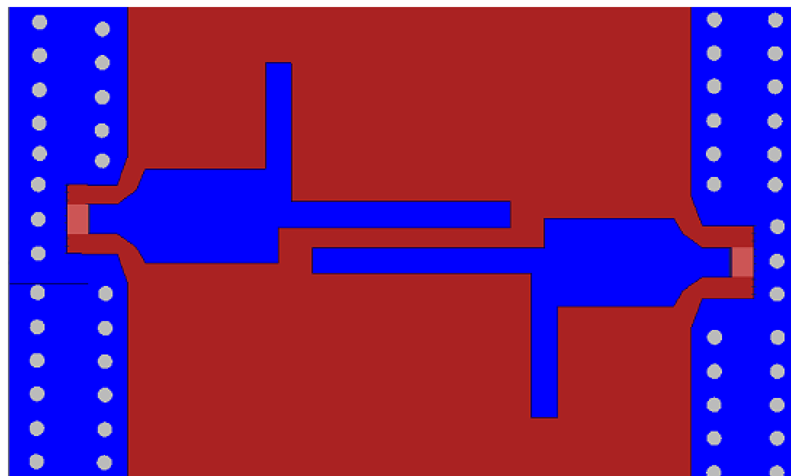

Figure 5.41. EM model of the coupled line capacitor with OCS.

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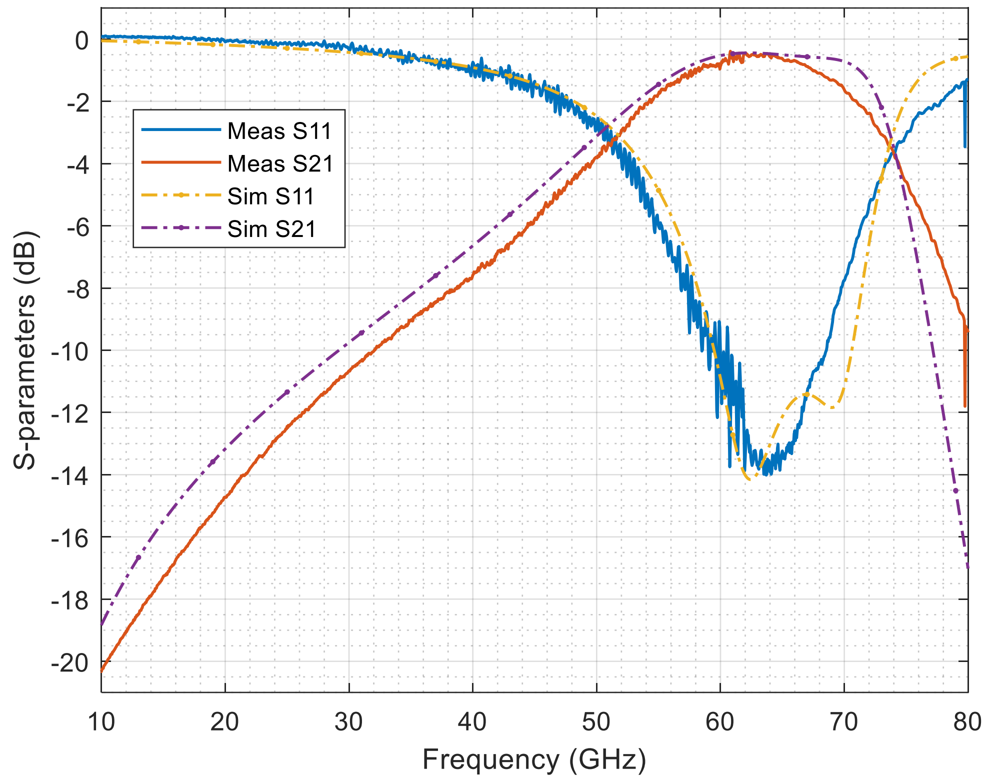

Figure 5.42. The measured result of the coupled line resonator with OC stubs.

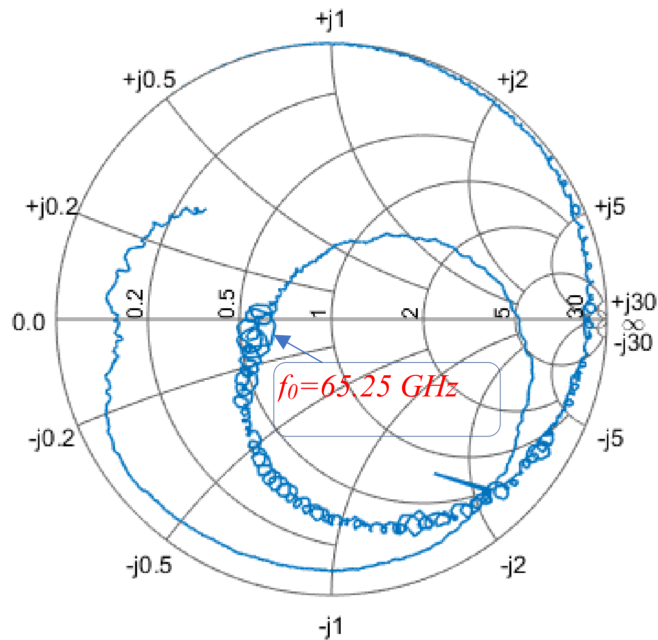

Figure 5.43. The measured S_{11} on the Smith chart.

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A modified version of the structure in Figure 5.41 is provided in Figure 3.20. The two ≈ λ/4 stubs are removed, and the middle transmission lines are shielded with floating structures. The two floating structures are not grounded; thus, the input signal couples to these two structures and then to the output transmission line. The magnitude of the coupling is controlled by adjusting gap2. The positioning of the transmission pole is adjusted by tuning the length of the shield structure and gap1. This can easily be achieved by parameterising the structure and running an optimization in Keysight ADS. The width of Tx is 221 μm, to match to 50 Ω, gap1 = 175 μm, gap2 and 3 = 87 μm, the length of the shield line = 1.57 mm and the OC lines are ≈ λ/4 each (final optimized value = 790 μm). Figure 5.45 shows a close agreement between the simulated and measured results. The simulated and measured are *IL* = - 0.5 dB and -1.3 dB respectively. The -3 dB FBW are ± 16.35% and 17.92% respectively with S_{11} below -10 dB from 62 to 68 GHz. The Smith charts in Figure 5.43 and Figure 5.46 suggest larger capacitance within the band of interest, making them ideal for dc blocking and bypassing capacitors at these frequencies.

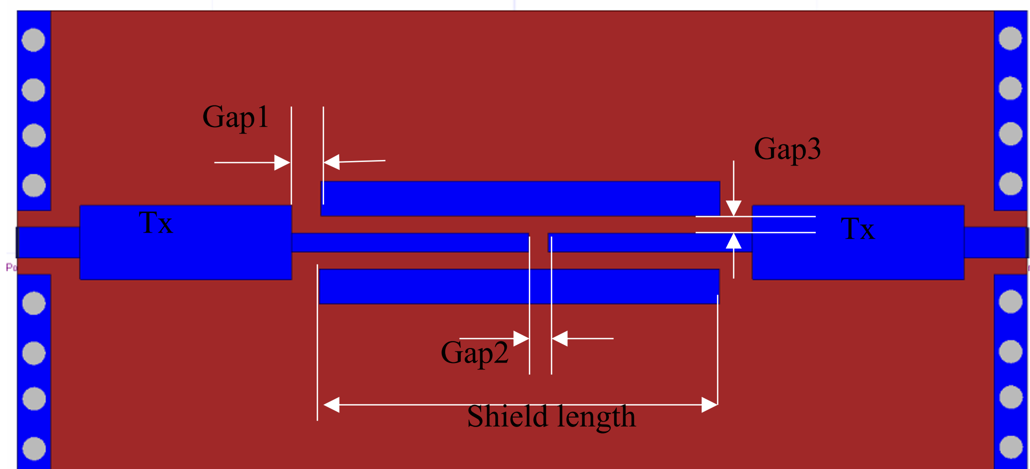

Figure 5.44. PCB layout of m a modified gap capacitor.

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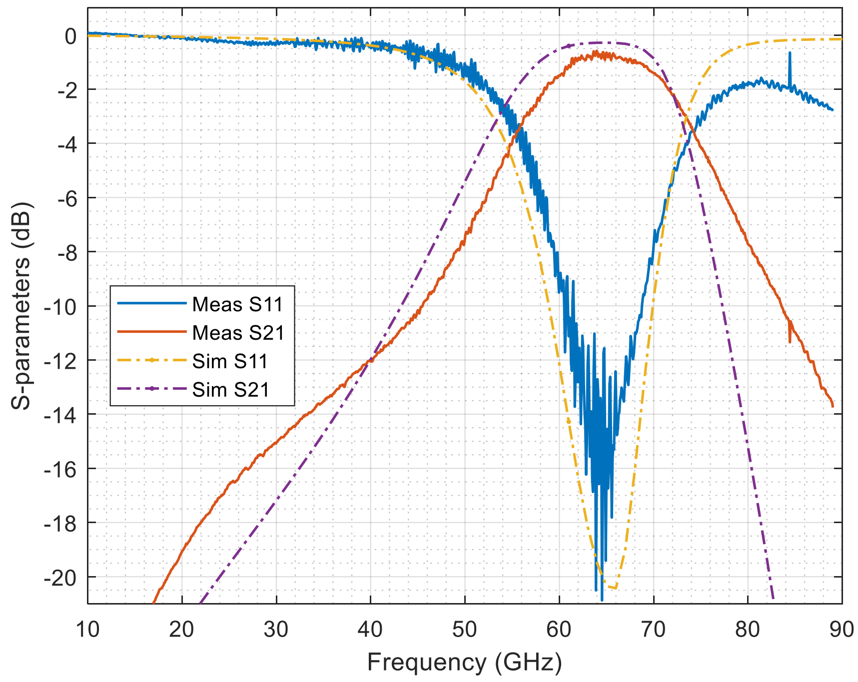

Figure 5.45. Coupled line with a stub measurement result.

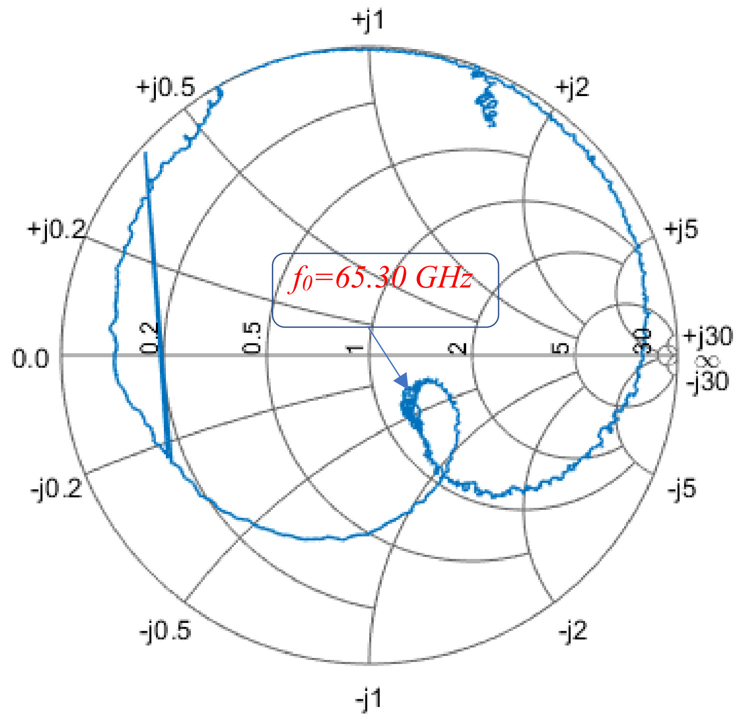

Figure 5.46. The measured S_{11} on the Smith chart.

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5.3.5.2 Radial stubs

To achieve biasing on PCB, an RF choke is required. A radial stub in Figure 5.48 was designed and fabricated to block RF between 60 to 70 GHz so that no RF is leaked into the DC power supply. The dimension of the stub is as shown on the schematic in Figure 5.47. The EM model in Figure 5.48 was simulated in Ansys using FEM simulation. The EM and the measurement results are shown in Figure 5.49, which indicate isolation of -34 dB which is sufficient to attenuate any RF from leaking to the DC lines.

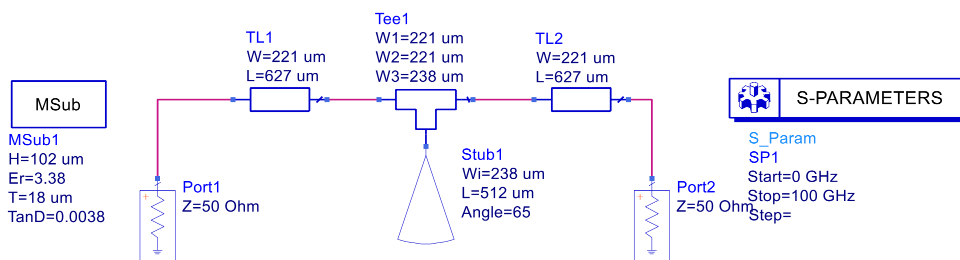

Figure 5.47. Schematic diagram in Keysight ADS.

Figure 5.48. Radial stub layout in AED.

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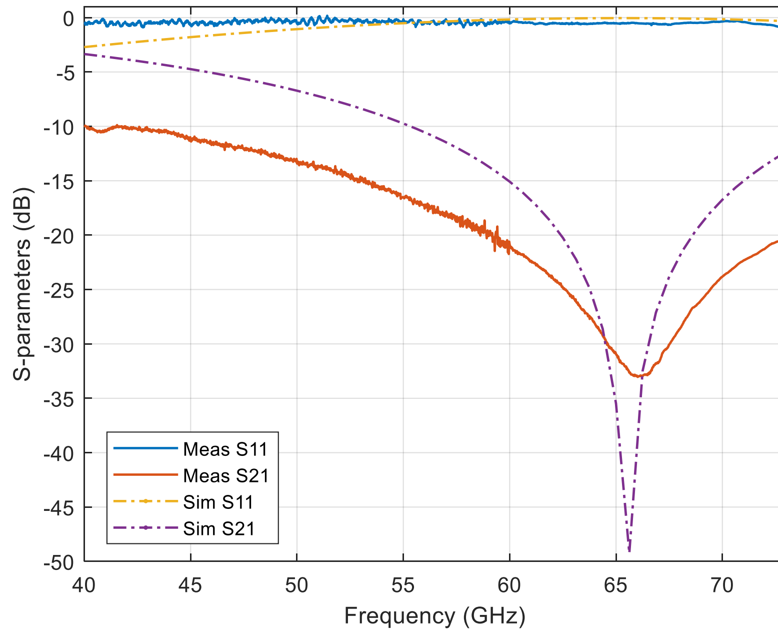

Figure 5.49. The simulation and measurement result of a V-band radial stub.

5.3.6 Chip capacitors

A few chip capacitor samples were obtained from ATC which included 0.1 pF, 0.25pF and 0.5pF. These were tested up to V-band (Figure 5.51) to verify their validity at mm-wave frequencies. Figure 5.52 presents the S-Parameters measurement of ATC 100 A 0.1 pF capacitor. The capacitor's equivalent circuit obtained according to [207] is given in Figure 5.50. To extract the capacitance, a second-tier (LRM and TRL) de-embedding was conducted to remove the effects of pads and those of the connecting transmission lines. The capacitance value was obtained by computing the ABCD matrix of the circuit and extracting the series capacitance value of 0.23 pF at 65 GHz. A deviation of 1.3pF is observed and could be attributed to mounting, or an incomplete circuit model of the measurement at mm-wave frequencies.

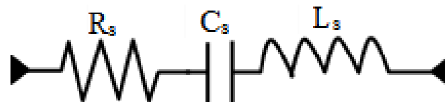

Figure 5.50. Equivalent circuit of a series-connected capacitor. Adapted from [207].

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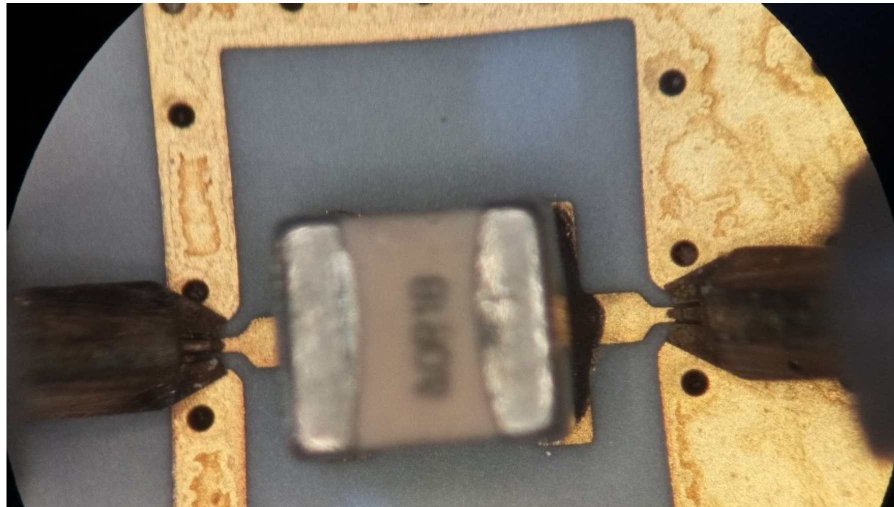

Figure 5.51. Chip capacitor measurement.

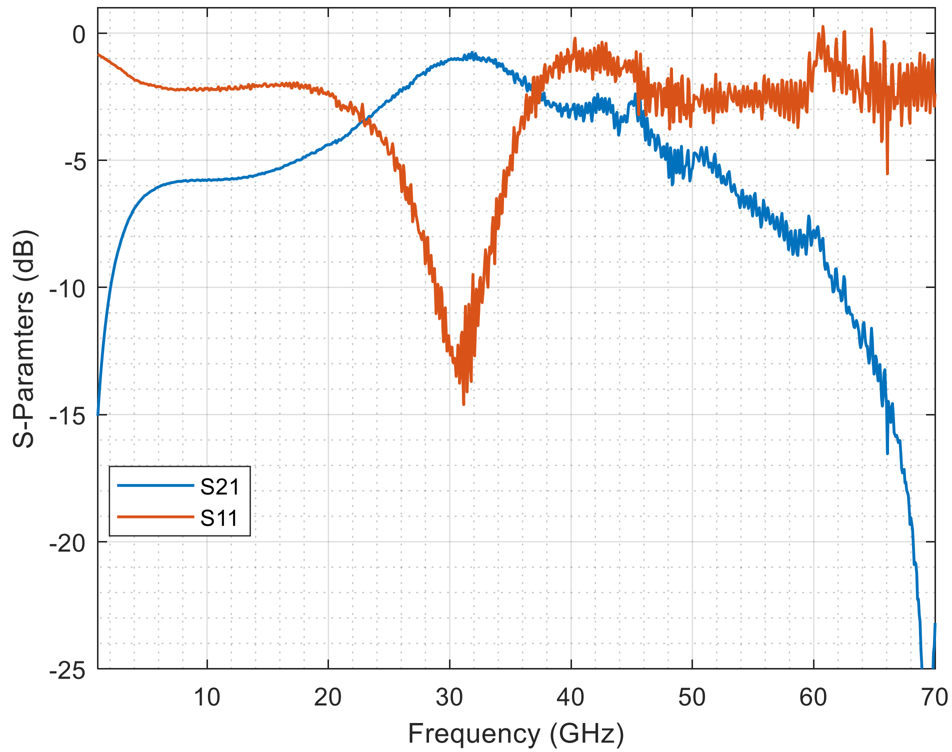

Figure 5.52. Forward transmission coefficient S_{21} of a chip capacitor.

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5.3.7 Layout and PCB assembly

5.3.7.1 Layout

The PCBs were designed to meet the PCB manufacturer production requirements (≥ 70 µm for structure widths and gaps). The pad structures were adjusted as shown in Figure 5.53. This adjustment leads to probe positioning difficulties during measuring due to uneven contacting surface plane contacting on the substrate.

An attempt to reduce the wire-bond length was done by creating a cavity as shown in Figure 5.53 as discussed in [64]. The depth of the cavity is 188 µm, such that only 134 µm of the die thickness protrudes out. The effective inductance of the wire-bond was reduced from 826 pH (961.1 µm) to 732 pH (871 µm).

The stackup in Figure 5.53 is double-sided, with the top layer used for routing and the bottom used as the ground plane. The finish is immersion silver immersion gold (ISIG) of thickness 25 µm over 18 µm copper. A 100 µm thick high-performance FR-4 was added to stiffen the overall PCB.

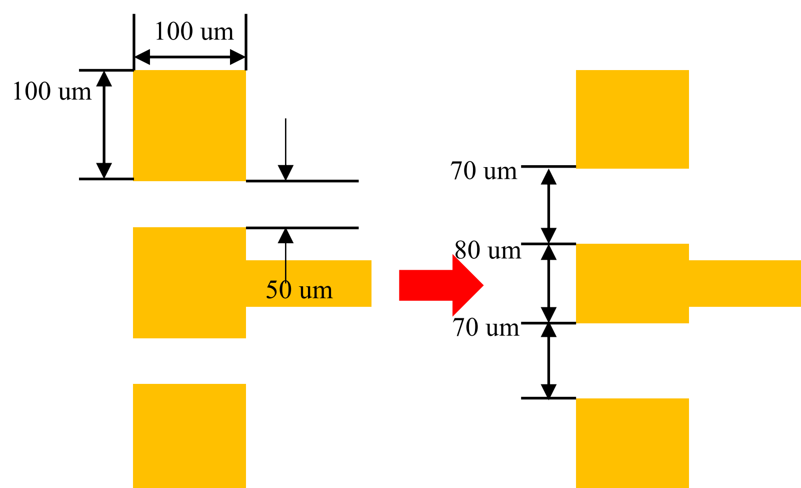

Figure 5.53. GSG pads on PCB with reduced widths and increased spaces.

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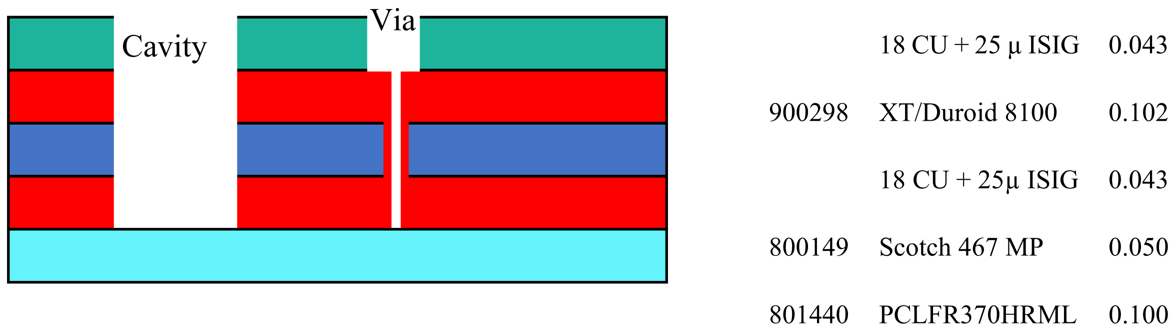

Figure 5.54. PCB Stackup.

5.3.7.2 PCB Assembly

The transistors were first diced from the die as depicted in Figure 5.55 before they were bonded onto the PCB. The dicing (Figure 5.56) and wire-bonding of the transistors were both conducted at DETEK, a division of Denel Dynamics. The dicing process was a complicated endeavour as it used a Computerised Numerical Control (CNC) process, and a few transistors were washed away by water in the process.

Besides losing a few transistors (as shown in Figure 5.56(a)), many others were successfully separated from the die (Figure 5.56(b)) and were wire-bonded to the PCB. The assembled PCBs are presented from Figure 5.57 through to Figure 5.60. Figure 5.57 and Figure 5.58 have transistors mounted on the top copper, while in Figure 5.59 and Figure 5.60, the transistors are sunk in the cavity.

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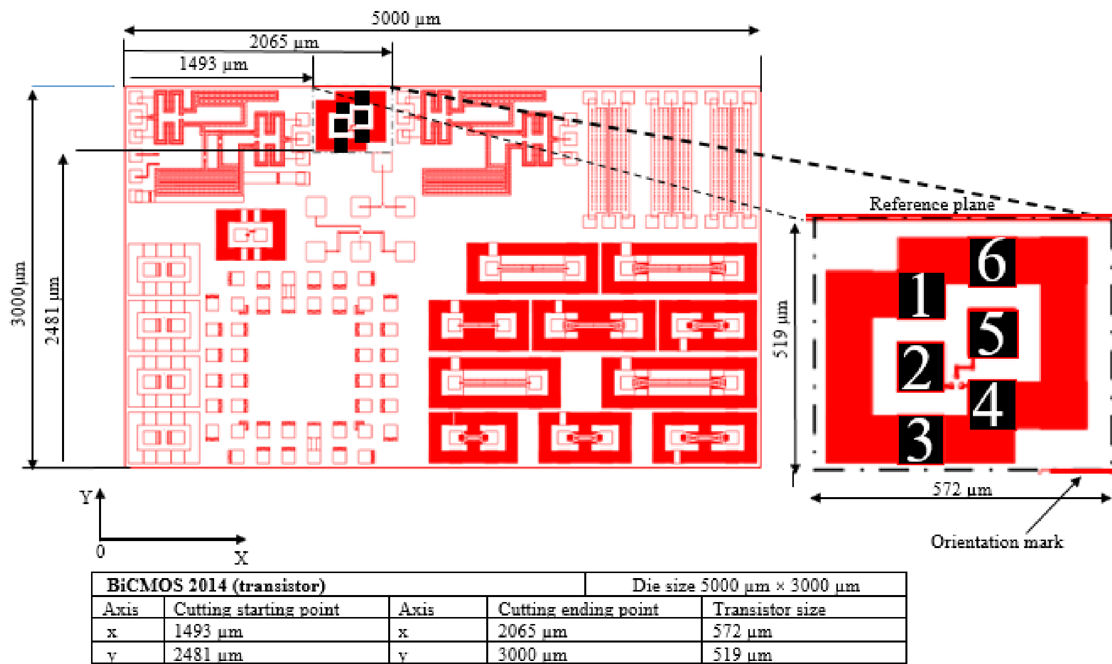

BiCMOS 2014 (transistor)			Die size 5000 µm × 3000 µm	
Axis	Cutting starting point	Axis	Cutting ending point	Transistor size
x	1493 µm	x	2065 µm	572 µm
y	2481 µm	y	3000 µm	519 µm

Figure 5.55. The transistor coordinate on the die.

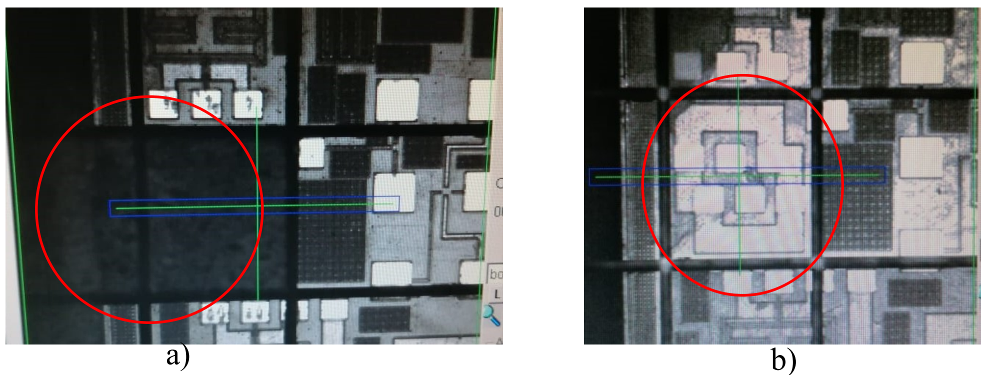

Figure 5.56. The dicing process of the transistors.

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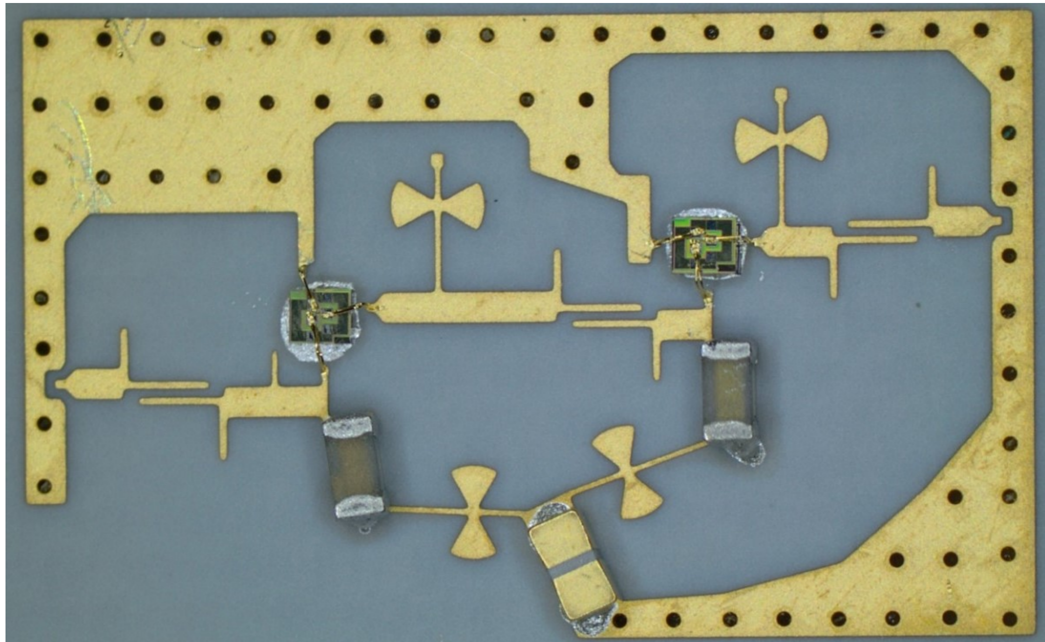

Figure 5.57. LNA with coupled lines capacitor with opened circuited stubs.

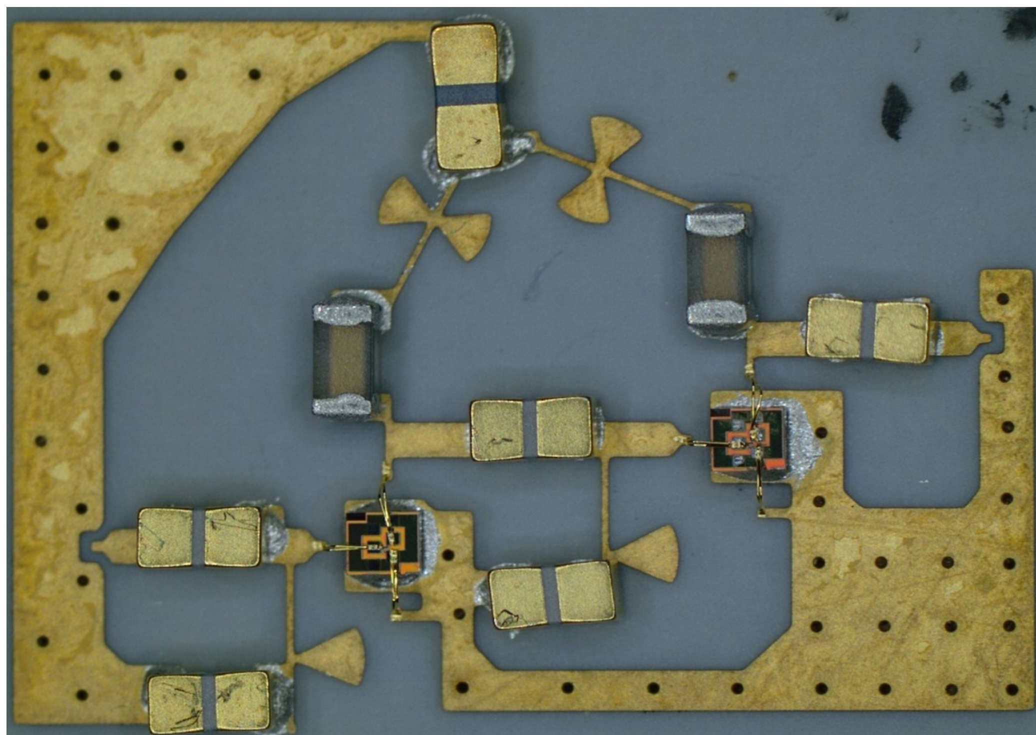

Figure 5.58. LNA with chip capacitors.

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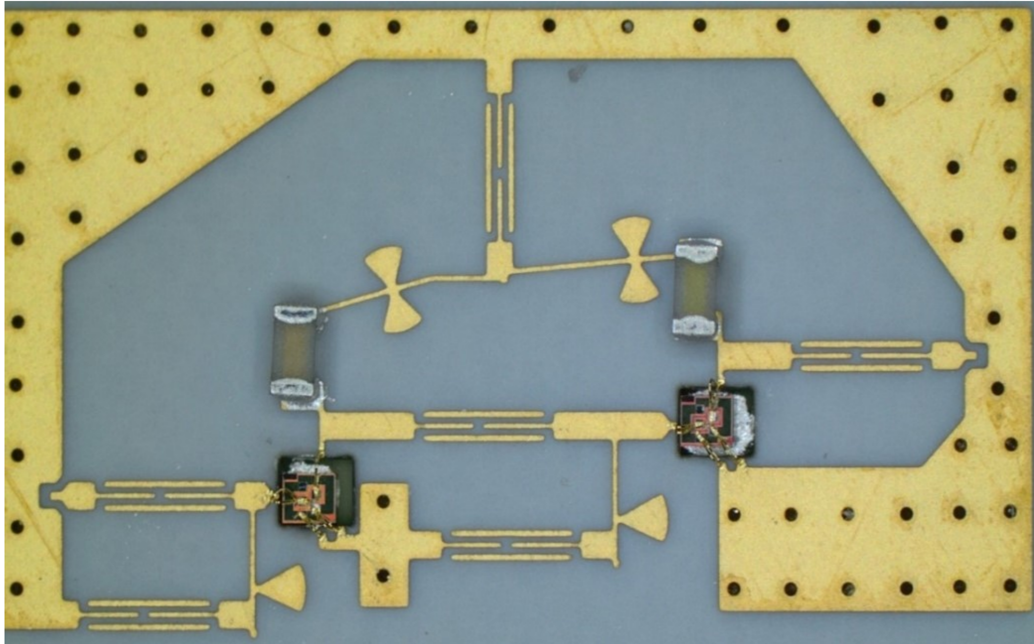

Figure 5.59. LNA with coupled line capacitors and the transistors sunk in the cavity.

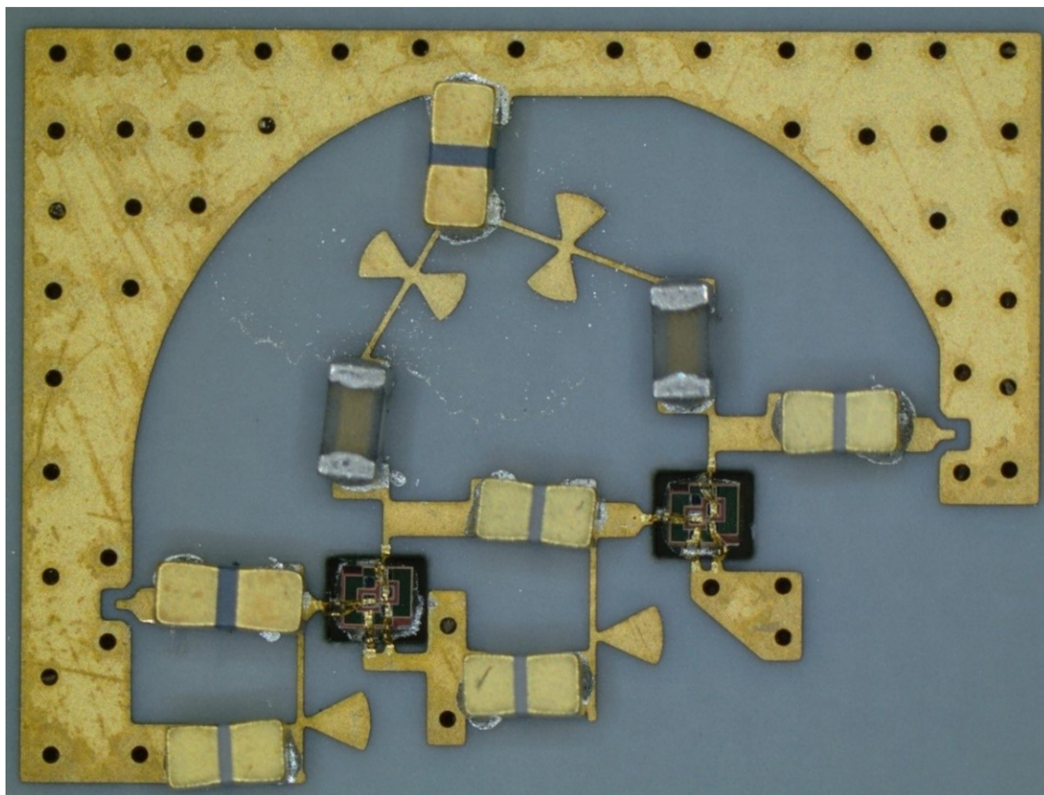

Figure 5.60. LNA with chip capacitors and the transistors sunk in the cavity.

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5.3.7.3 Hybrid LNA measurement

The linear measurements were conducted as per Section 4.2.3 using Anritsu ME7828A VNA. The measurement frequency was set from 55 GHz to 75 GHz. The calibration method and the power level setting were also in accordance with Section 4.2.3. The HP 4155B parameter analyser was used to supply the required independent biasing current to the LNA stages. Figure **5.61** shows the positioning of the probes and the DC needle contacts. The results obtained suggested that the transistors were not adequately biased. After ensuring that the HP 4155B provided the correct biasing voltage by disconnecting the DC needles from the circuit, a continuity test was followed. From this test, some portions of the circuits exhibited short circuit characteristics (very little voltage but over 70 mA current). In other portions, no current while the required biasing voltage was present. These were confirmed by conducting a visual inspection using the probe station's microscope. Figure 5.62 shows a few of these irregularities with wire-bonds disconnected from the pads in Figure 5.62(a) and (b). The conductive epoxy was also seen in a larger area around the MMIC transistors and could have been the cause of the short circuits observed during the DC test.

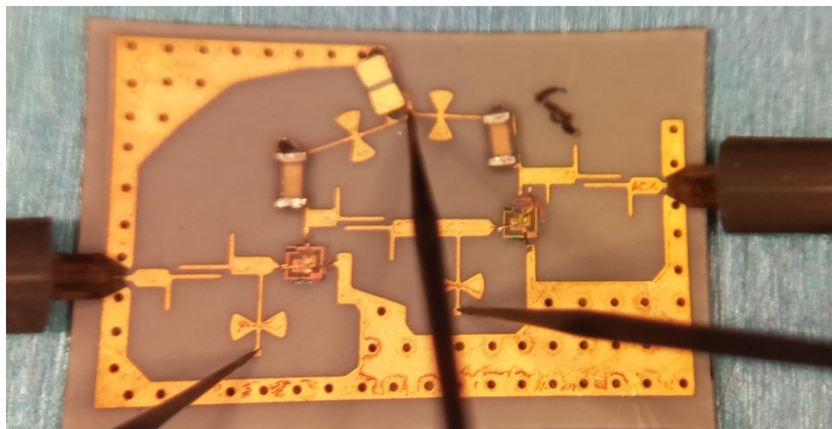

Figure 5.61. Hybrid LNA measurement with wire-bond interconnect.

After troubleshooting and isolating the faults discussed above, it was determined that components needed to be disassembled and the PCB needed to be washed to clear the epoxy, then re-assembled. This was not possible because all the transistor dies from the 8HP run were used, and there were no more funds and time to pursue re-prototyping or any re-work.

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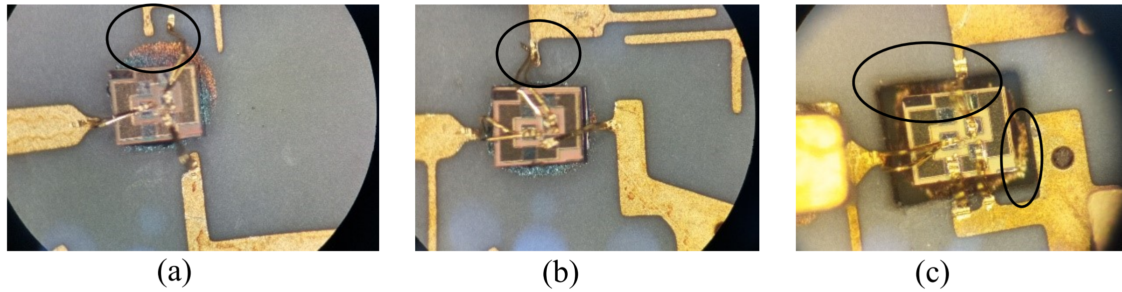

(a) (b) (c)

Figure 5.62. Faulty wire-bond interconnects and smeared conductive epoxy.

Based on the simulation results, a single wirebond has more than -10 dB return loss, since the length of the wire is much longer than 0.033 λ (which is ≥ 152 µm at 65 GHz) [129]. Therefore, the flip-chip remains the only viable solution. However, as discussed earlier, a large prototyping volume is required for consideration by commercial assembly houses, which constitutes a major challenge.

5.4 SUMMARY

In the first part of this chapter, the wire-bond and flip-chip interconnections were EM modelled. It was found that the insertion loss of the wire-bond transitions is significantly high at mm-wave. IL of ± 6 dB was obtained for a single wirebond. The insertion loss of the flip-chip on the other hand was found to be considerably lower between 1.5 to 2 dB.

Next, the ring resonators and the microstrip transmission line were used to characterise the XT/Duroid 8100 at V-band. The experimental results indicated an increase in the dielectric constant between 2.95% and ± 16% using the ring resonators method. On the other hand, the attenuation constant increased from 0.5 dB/mm to 1.2 dB/mm. These increases were attributed to the use of the ISIG surface finish.

PCB capacitors were designed, fabricated and measured. The measurement result of the coupled line with OCS bandpass filter provided an IL of -1.3 dB and -3dB FBW of 25%. The coupled lines filter exhibited IL = 1.3 dB. The 3 dB FBW of 17.92% with S_{11} below -10 dB from 62 to 68 GHz was also obtained. Both these filtering DC blocks are novel contributions to state-of-the-art as no PCB bandpass filter has been reported at these frequencies. The radial stub used as RF chokes was also characterised experimentally showing isolation of -34 dB. The on-chip

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transmission interconnects of the HBT used for the hybrid integration were also EM characterised, and the resulting S-Parameters were used for EM-schematic co-design.

The MMIC LNA integrated into PCB was evaluated through simulation. It was found that the insertion loss of the transition was a determining factor in how the LNA would perform. As a result, flip-chip LNAs performed better compared to the wire-bond LNAs. This was consistent also in the case of the hybrid design. It was thus concluded that the flip-chip approach was a viable candidate for hybrid frontend designs at mm-wave. To vary these findings experimentally, various experimental approaches were planned, the prototypes were fabricated, and the PCBs were assembled. However, due to the assembly problems, none of the prototypes was successful.

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CHAPTER 6 CONCLUSION AND FUTURE WORK

This chapter presents an overall summary of the research based on the findings in Chapters 4 and 5. These are analysed and evaluated on whether they address the research objectives set in Chapter 1. The chapter then concludes with challenges and limitations that were encountered and provides recommendations for future works.

6.1 TECHNICAL SUMMARY AND CONTRIBUTIONS

6.1.1 EM modelling approach for MMICs at V-band

To establish the suitable EM modelling method for MMIC LNA layout validation, microelectronic stackups needed to be validated first in order to establish a simulation algorithm in AED. Here, various simulation variables (the simulation engine, the bulk silicon, the vias and the etch factor) were evaluated.

The study established in Section 3.5.1 that the bulk silicon cannot be omitted from the stackup, as this would lead to significant performance deviation both in the shift of f_0 and in S-parameters degradation. The 3D FEM simulation discrepancy between the Momentum stackup and derived stackup from the BiCMOS8HP design manual were found to be tolerable and within acceptable margins *vis-a-vis* the measurement data. In addition, by simplifying the vias from array to via blocks, the results were still within the acceptable margins. Similarly, by omitting or including the etch factor from the model in AED, the results did not reveal any considerable deviation in both f_0 and S-parameters. This finding was validated subsequently by other researchers [209].

Using the consolidated approach to EM simulate the MMIC layout, the results of the post-layout EM-schematic co-simulation of the MMIC LNA in Section 4.2.1 were found to be in better agreement with the measurements than the *pcell*-based schematic simulation. This

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indicates that the approach for segmenting the structures and analysing them separately to save both time and resources is sufficient for the first-pass accuracy. The QRC extraction approach, which was the other layout validation method that was investigated, was found to be the fastest method but was less accurate than the FEM-based approach.

6.1.2 SiGe LNA radiation tolerance at V-band

To quantify the effect of TID electron radiation on SiGe HBT LNA, the device was exposed to Sr-90 source over 72 hrs. After a total cumulative dose of 15 Mrad(Si), it was found that a gradual degradation in the NF and S_{21} bandwidth were observed as discussed in Section 4.2.4. In addition, an increase in the collector current was recorded from the pre-radiation value of I_C = 4.30 mA to its plateau at ± 6.3 mA (3 Mrad(Si)). This phenomenon was also observed in the study conducted in [199] but plateaued at above 1 Mrad(Si). At the highest radiation dose of 15 Mrad(Si), the LNA still presented a gain of ± 12.3 dB and NF of ± 9.3 dB, consistent with results in [169]. This indicates the SiGe LNA's resilience to electron radiation at such a high radiation dose at mm-wave frequencies. This finding was in line with the proton, neutron and gamma radiation studies reported in [210].

6.1.3 LNA integration methods at V-band

To compare the MMIC to PCB packaged LNA and hybrid LNA with wire-bond and flip-chip interconnects, the MMIC LNA was used as the comparison reference. It was found in Section 5.1.1 that the EM modelling of the interconnects lead to up to an *IL* of ± 6 dB for a single wirebond at V-band, while the flip-chip interconnect resulted in an *IL* < 2.5 dB at V-band.

The experimental results of the resonators in Section 5.1.3 indicate that dielectric constant XT/Duroid 8100 varies between 2.95% to ± 16% from the simulation result to measurement values. The simulated dielectric constants were consistent with the manufacturer's datasheet provided by Rogers Corporation. Using the transmission line method, the attenuation constant was extracted in Section 5.1.4, also indicating an increase from 0.5dB/mm for the simulation

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model to 1.2 dB/mm from the experiment. These increases were attributed to the effect of the ISIG surface finish at mm-wave.

The measurement result of the bandpass filters used for coupling in Section 5.1.5.1 indicates an *IL* of 1.2 dB and a -3dB FBW of 25% for the stub version and *IL* = 1.5 dB for the version without the stubs. This latter indicates -3 dB FBW of 17.92% with S_{11} below -10 dB from 62 to 68 GHz. The radial stub used as an RF choke was also characterized experimentally showing isolation of -34 dB. The on-chip transmission interconnects of the HBT used for the hybrid integration were also EM characterised and the resulting S-Parameters were used for EM-schematic co-design.

The MMIC LNA integrated into PCB was evaluated through simulation. It was found that because of high wirebond insertion loss, the gain of the LNA was significantly reduced. This was valid for both the MMIC/PCB LNA and hybrid LNA. These two LNAs had comparable NF of ± 9.74 and 10.4 dB respectively while the gain degraded from 10.2 to 5 dB, respectively. Based on this finding, the wire-bonding MMICs on PCB for wideband LNAs is not found to be feasible at mm-wave frequencies. On the other hand, for the flip-chip options, the NF of 7.8 and 7.9 dB was obtained for the MMIC/PCB LNA and hybrid LNA, while gain of 12.2 and 10 dB were obtained, respectively. As a result, flip-chip transitions are the better candidate for mm-wave front-end integration. While it is true that the MMIC LNA performs better than either of the two-hybrid integrated LNAs one needs to consider the turnaround time. This is one week in the case of PCB fabrication and one week for assembly, compared to several months in the case of an MMIC.

6.2 EVALUATION OF THE RESEARCH OBJECTIVES

The first objective of this study was to establish a performance comparison between on-chip or off-chip matching of mm-wave LNAs integrated on PCB and quantify the board-to-board difference in performance between on-chip LNA and its subsequent hybrid counterpart (Section 4.2.3) although such a comparison may be biased somewhat toward the MMIC LNA, as it allowed for the use of cascode stages which the discrete design did not. Despite the fact that the hybrid prototypes were unsuccessful, this objective was met partially in a simulation study. By comparing the EM results of the MMIC LNA (which closely matched the experimental results)

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with those of the hybrid LNAs (Section 5.3.4), it is established that on-chip matching performs better than matching off-chip for a microelectronic HBT. From post-layout EM data at the design f_0, the MMIC LNA (which achieves 14.95 dB gain when measured on-chip) mounted on PCB by wire-bonding achieves peak gain of 10.2 dB, and 12.2 dB when mounted by flip-chip bonding. In contrast, the hybrid LNA achieves 5.05 dB gain when integrated by wire-bonding and 10 dB when integrated using flip-chip bonding. This result is reflected in the NF as well, with the MMIC LNA achieving 7.66 dB NF in isolation, 9.74 dB when packaged on PCB using wire-bonds and 7.8 dB when packaged using flip-chip mounting. In contrast, the hybrid LNA using wire-bond integration achieves 10.4 dB of NF, while hybrid integration using flip-chip mounting achieves 7.9 dB. This data clearly illustrates the superiority of the MMIC LNA over its counterparts, despite the reduced 1 dB FBW.

The second objective was to experimentally compare different approaches to EM modelling at mm-wave frequencies on-chip. This objective has been met and was validated by subsequent researchers as discussed in Section 6.1.1. This revealed that 3D EM method was the most accurate post-layout MMIC validation method at mm-wave frequencies. The study also provides relevant implications to speed up the simulation without affecting the simulation outcome. These are critical findings to the RFIC community and are now available for the first time in literature.

To quantify the effect of TID electron irradiation on the performance of V-band MMIC LNA in the SiGe HBT process, the electron source and the setup discussed in Section 3.8.4 were adopted. The most impacted LNA parameter as a result of radiation is the 1dB BW. Though a reduction in the gain and NF was observed, the LNA could still achieve a peak gain of 12.3 dB and NF of 9.3 dB revealing the strong radiation tolerance of SiGe LNAs at mm-wave frequencies to electron irradiation. This data is now available in literature for the first time.

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6.3 THE CHALLENGES AND LIMITATIONS

6.3.1 Challenges

None of the hybrid prototypes worked. After troubleshooting, it was discovered that the conductive epoxy used to attach the transistors to the PCB smeared over unexpected areas creating shorts in some parts of the LNA circuits.

Some of the bond wires were disconnected from the PCB peeling off the thin layer of ISIG used as surface finish and needed to be reworked. This was not possible because the stock of transistor dies had been depleted and there were no more funds and time to pursue microelectronic re-prototyping.

It was impossible to adhere to all ESA-ESCC 22900 guidelines due to the test being conducted in two different facilities distanced from each other and due to unavailable equipment for in-situ measurement. However, by adhering to the prescribed test criteria for the dose rate and particle energy, it is anticipated that similar results will be obtained by a formal ESA-ESCC 22900 test.

6.3.2 Limitations

It was impossible to conduct flip-chip bonding because the process was not available at the post-processing facility, and also due to a shortage of available dies. Many assembling facilities had initially been consulted, but all of them declined to quote on a small volume processing.

The ring resonators could not be printed with different conducting inks as initially planned due to the unavailability of the equipment, so only the ISIG surface finished was used in this study. For this reason, it was impossible to establish the exact contribution of the ISIG as a bare copper experiment could not be produced on the same run. However, by extrapolating to ε_r provided by Rogers Corporation with simulation results, it was observed that both agreed well.

6.4 RECOMMENDATIONS AND FUTURE WORK

In this research the MMIC transistor was connected to the on-chip ground, making it impossible for other LNA design configurations other than CE configuration. The design flexibility could

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be increased as shown in Figure 6.1. This would allow for cascode configuration off-chip with the ground pads used for mechanical support of the die in a flip-chip configuration. Alternatively, cascaded single-stage designs could be compared both on MMIC and on a hybrid integration approach.

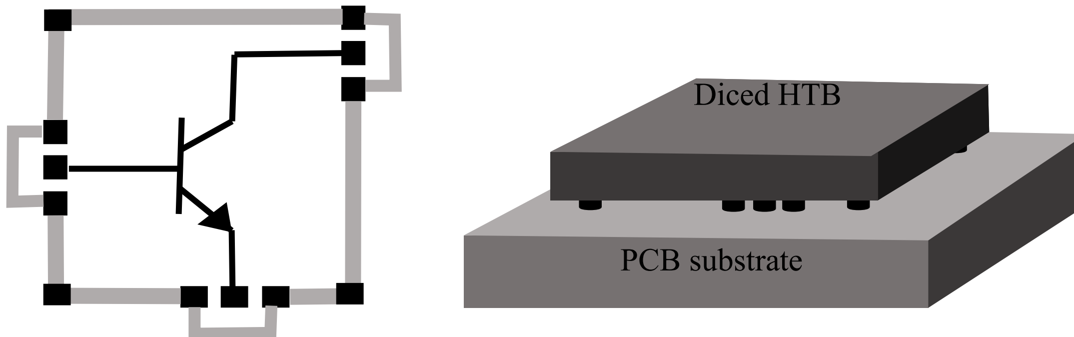

Figure 6.1. Recommended transistor configuration for hybrid integration.

The diced transistors should be tested after the dicing process to ensure that they are still functional. This will ensure that no damaged transistors are used for the LNA assembly. In addition to this, various transistors sizes should be fabricated, to allow for different transistors sizes in different stages.

In this work, the transistor and wire-bond interconnect were measured in isolation. The measurement of wire-bond was the most delicate measurement to conduct as the probes needed to be carefully positioned on top of the sending pads on-chip. Due to the risk of damaging the probes, from this type of measurement, it is recommended to first bond the transistor to PCB, then characterise the hybrid combination as shown in Figure 6.2. As part of the process, the on-chip pads would have to be placed at the die edge (Figure 6.2), which was not always the case in this study.

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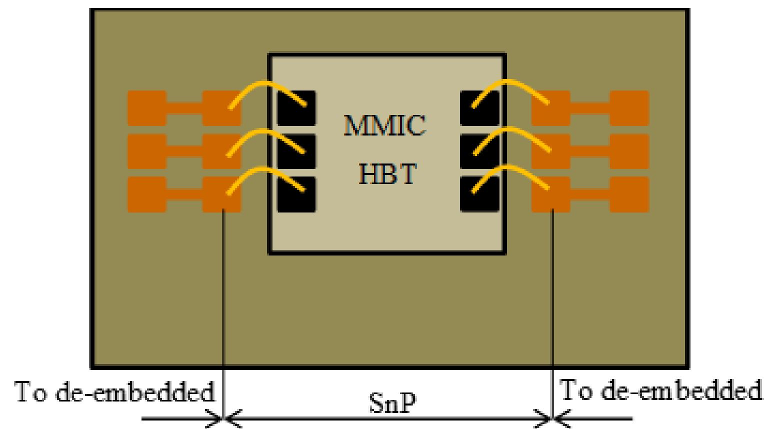

Figure 6.2. Transistor and wire-bond forming part of the SnP file.

It was shown in this work that wirebond interconnects significantly degrade the LNA's performance. It is therefore crucial that the parameters of the MMIC LNA be optimum to anticipate the degradation due to the transitions for the MMIC LNA to PCB attachment. This means minimising the NF in the first stage and maximising the gain through additional stages. This could mean combining the CE/CS in the first stage with cascodes in subsequent stages [211]. This combination has proven effective since CE/CS stages have lower gains but provides very low NF. Furthermore, this arrangement will also improve the 1dB compression point, because the low gain from the first stage will not easily drive the subsequent stages into compression. A cascode in the second stage will improve the bandwidth and gain.

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