A Millimeter-Wave Second-Order All-Pass Delay Network in BiCMOS

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***Abstract*— Analogue signal processing (ASP) is a promising alternative to DSP techniques in mm-wave technologies such as 5G, with second-order all-pass networks a key building block in ASPs. We present an active on-chip mm-wave second-order all-pass network in a 130 nm 280 GHz f_{max} SiGe BiCMOS process with an effective bandwidth of 40 GHz, peak delay of 62 ps at 36 GHz, delay Q_D-value of 3.6 and a magnitude ripple of 1.4 dB. A layout-focused design methodology incorporating layout parasitics and process tolerances is followed. This is the first reported mm-wave bandwidth second-order all-pass network, and the first monolithic microwave integrated all-pass network with a Q_D-value greater than 1.**

***Index Terms*—All-pass networks, analogue signal processing, group-delay engineering, millimeter wave integrated circuits, ultra-wideband technology.**

I. Introduction

DATA traffic of future 5G telecommunication systems is anticipated to increase 10 000-fold compared to current rates, necessitating wideband mm-wave front-haul links [1]. One possible mitigating approach to processing wideband data in real-time is to replace some baseband DSP blocks with ASP equivalents at RF [2].

Two fundamental building blocks of ASPs are dispersive first- and second-order all-pass networks [3] (as opposed to flat delay used in true time delay networks [4], [5]) for which both passive and active implementations have been proposed [6]–[11]. In many applications, a large band-pass delay Q-value (Q_D) [2], [6] is required. Real-time spectrum analysis [6] requires $Q_D > 0.79$ for frequency discrimination, while $Q_D > 3.5$ and $Q_D > 10$ results in a resolution of ~$0.4f_0$ and ~$0.2f_0$, respectively. In frequency scanning antenna arrays, a Q_D of 2 has been shown to result in a mapping of 60°/GHz [6], with higher Q_D required for finer spatial resolution. In M-ary pulse-position modulation (PPM), a Q_D of 3.14 is required to create a maximum delay of one pulse width. Increasing Q_D however, also increases the insertion loss of the network at resonance, which is exacerbated by low attainable on-chip inductor Q-factors (typically less than 10) [11]. In response to this, active implementations of all-pass networks have been proposed [7]–[11], but none achieve Q_D-values larger than 0.2.

A suitable single transistor second-order all-pass network with inductor Q-factor enhancement was proposed in [12], but the published synthesis method relies on zero length interconnects and ideal components. In MMICs, the circuit's design would be complicated by layout RLC parasitics and finite component Q-factors.

In this work, we present an MMIC second-order all-pass response with a Q_D-value larger than 1 for the first time, through augmentation of the procedure in [12] with an optimization-based, layout-focused design methodology which incorporates accurate device models as well as layout-specific RC parasitic extraction. The effects of component tolerances on the group delay and magnitude responses are further investigated. The proposed design is prototyped in a 130 nm SiGe BiCMOS process as proof of concept.

II. Design Procedure and Simulation

The single-transistor second-order all-pass network (based on [12]) is shown in Fig. 1. A single HBT npn transistor (L_e = 6 µm, W_e = 120 nm, multiplicity = 4) is used with emitter parameters as shown. Transmission lines T_1 and T_2, each placed over a deep trench, act as inductors connected in series with capacitor C_1 to form a resonant LC tank. Interconnects over the shielding ground plane are explicitly modelled from the foundry PDK pcells as inductive elements T_3 and T_4. This approach models potential distributed inductance in long interconnects with foundry-qualified PDK pcells, negating the need for FEM modelling of the layout. The V_{DD} bias connection is modelled as a 5 nH inductor, though the circuit's performance is found largely insensitive to this choice. A decoupling capacitor is included as C_3, with a gain-enhancement capacitor C_2 added to extend the bandwidth of the network. Further RC layout parasitics (as opposed to device parasitics and inductive interconnects included in foundry PDK pcell models) are further extracted and included in the final layout-ready simulation as demonstrated later.

The following design procedure is followed:

(i) Design equations from [12] are used for initial component values neglecting layout parasitics ($C_3 \to \infty, C_2 \to 0$)

(ii) An optimization is performed in simulation using the foundry PDK and initial values. C_3 is minimized without compromising decoupling, while C_2 is optimized to reduce high-frequency peaking.

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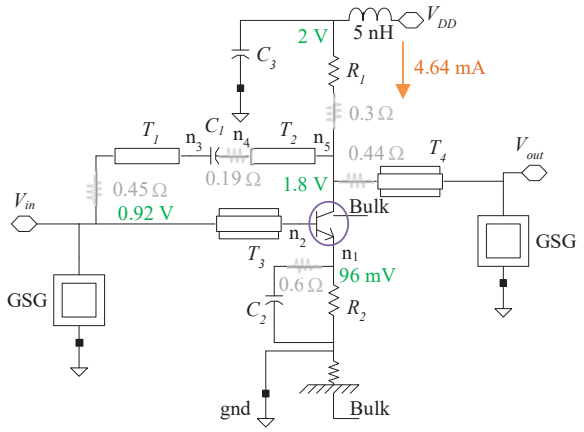

Fig. 1. Schematic of the single-transistor second-order all-pass network. Parasitic resistances extracted from the final layout are shown.

(iii) Using the values obtained in *(ii)*, a layout is constructed. RC layout parasitics are extracted with an automated tool, while inductive parasitics T_3 and T_4 are explicitly included in the schematic from pcells.

(iv) A second optimization is performed, this time including all parasitics (T_3, T_4, and extracted RC).

(v) The layout is updated to reflect the optimized changes.

A. Theoretical calculations

The ideal second-order all-pass voltage transfer function of Fig. 1. can be written as:

$$T(s) = K \cdot \frac{s_n^{\,2} - s_n / Q_D + 1}{s_n^{\,2} + s_n / Q_D + 1}, \tag{1}$$

where $s_n = s/\omega_0$, $Q_D = \Delta\tau\omega_0/4$ is the delay Q-value, $\omega_0 = 2\pi f_0$ is the center frequency of the second-order all-pass delay function and $\Delta\tau$ is the corresponding peak-to-nominal group delay. Equating similar terms in (2) with those in [12] leads to:

$$\frac{1}{\omega_0^{\,2}} = LC_1, \tag{2}$$

$$\frac{1}{Q \cdot \omega_0} = \frac{C_1}{G_2 - G}, \tag{3}$$

where L is the combined inductance of T_1 and T_2, $G_2 = 1/R_2$, and G is the combined parasitic conductance in parallel with T_1, T_2 and C_1. Conductance G_1 is chosen as detailed in [12] to meet the all-pass condition.

Applying step *(i)* of the design procedure using (1) – (3) and [12], we set $\Delta\tau = 38$ ps, $f_0 = 30$ GHz, $G = 0.04$ S, $G_2 = 0.086$ S. As the proposed network is designed to operate as a voltage-mode device, 50 Ω impedance matching and return loss are not considered as goals. This results in in $G_1 = 0.025$ S, $C_1 = 136$ fF and $L = 207$ pH. Initial values for C_2 and C_3 are chosen as 60 fF and 75 pF respectively. Using these values, the circuit schematic of Fig. 1 (excluding layout parasitics and interconnects) is simulated using the foundry PDK. The results are shown in Fig. 2 (blue trace). The effect of non-idealities is clear from the initial transmission magnitude variation of 7 dB and delay peak offset of 4 GHz.

B. Application of layout-based optimization

The first optimization is now performed to account for the device non-idealities (step *(ii)* of the procedure), where f_0, $\Delta\tau$ and passband magnitude variation are set as gradient-based optimization goals with C_1, C_2, L, R_1 and R_2 chosen as variables. The resulting magnitude and group delay responses in Fig. 2 (red trace) indicate that the passband magnitude variation is improved to 0.8 dB, with f_0 and $\Delta\tau$ goals met.

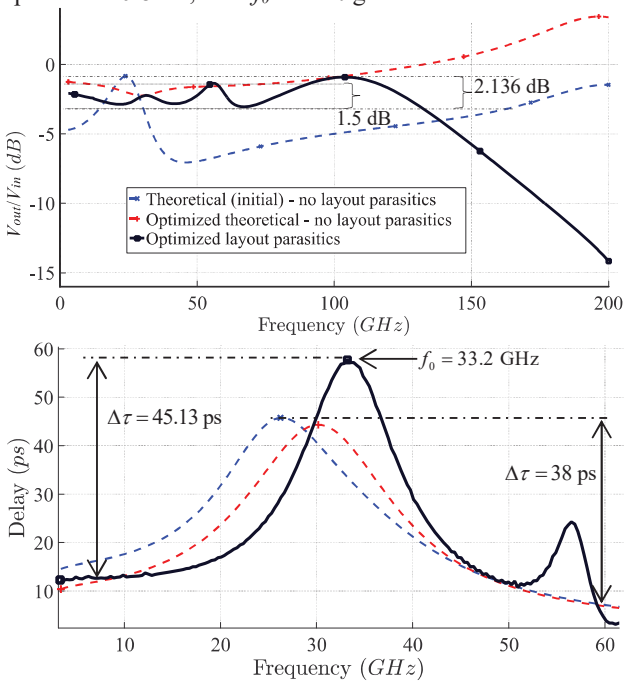

Fig. 2. Transmission magnitude and delay responses (voltage transfer).

Next, in step *(iii)*, a layout is drawn as shown in Fig. 3 and layout parasitics extracted. T_3 and T_4 are included explicitly, as these were assumed zero in step (ii).

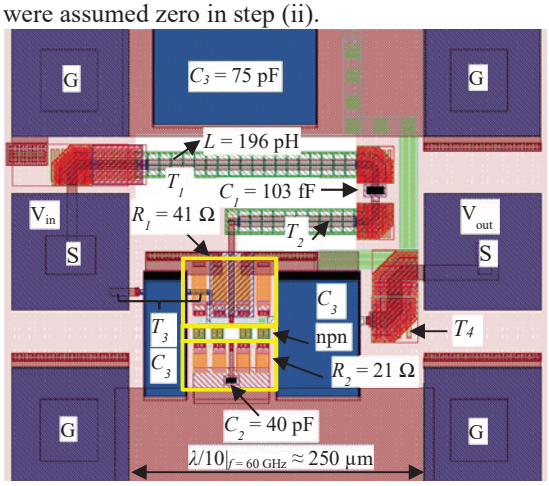

Fig. 3. Camera-ready layout of the BiCMOS second-order all-pass network.

146 parasitic capacitors and 35 parasitic resistors are extracted from the layout, with the dominant layout parasitic resistors indicated in Fig. 1. The sum of layout parasitic capacitances at each node are comparable to some component values (e.g. C_1) justifying the RC extraction and layout-based approach. Another optimization is performed (step *(iv)*) using the same optimization goals and variables, but now including the extracted RC layout parasitics. The resulting responses are shown in Fig. 2 (black trace).

It is found that the initial optimization parameters do not offer sufficient variation to meet all the pre-defined goals whilst maintaining pass-band variation of below 1.5 dB. This is a known trade-off in designing high-Q_D networks [2], [3]. The final achieved values of $f_0 = 33.2$ GHz and $\Delta\tau = 45.13$ ps with magnitude variation of 1.5 dB (2.14 dB including peaking) represent a fair trade-off between passband flatness and deviation from desired $\Delta\tau$ and f_0. The network's bandwidth is limited to 50 GHz by a spurious second delay peak at 56 GHz. An average output noise of 0.69 nV/√Hz is simulated over the band.

III. Measurement Results

The design is prototyped in the GlobalFoundries US 8HP 130 nm SiGe BiCMOS process, and measured with 150 µm pitch GSG wafer probes (Fig. 4, insert) on an Anritsu ME7828A VNA, with a single DC bias needle supplying V_{DD}. The network consumes 9.3 mW. The measured S-parameters are converted to ABCD parameters and the voltage transfer is extracted as shown in Fig. 4, with substantial dispersion observable down to ~ 20 GHz. A magnitude response ripple of 1.4 dB over a bandwidth of 40 GHz is measured. The obtained $\Delta\tau$ of 62.4 ps is larger than the simulated value of 45 ps, and f_0 is offset by 6.23 GHz. The poor absolute tolerances of on-chip TaN resistors (also shown in Fig. 4) may partially explain the magnitude ripple and $\Delta\tau$ discrepancies, but Fig. 2 would indicate that discrepancy in f_0, is, more probably, the result of unmodeled parasitics.

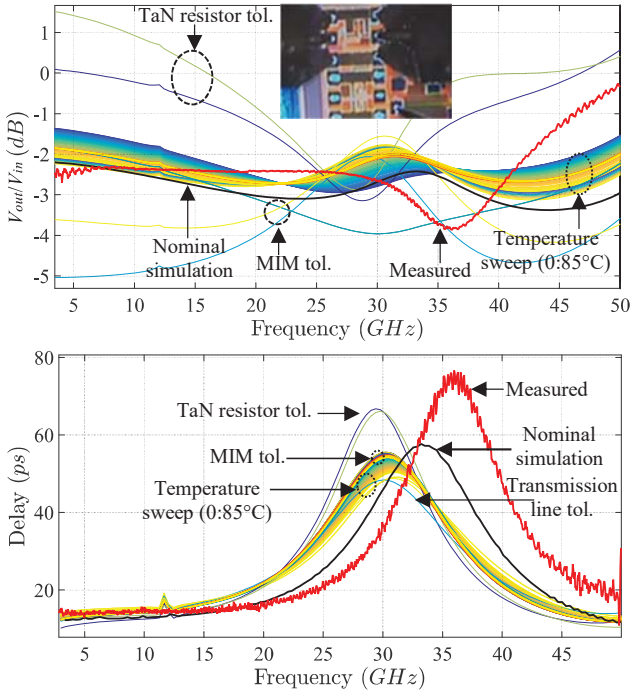

Fig. 4. Measured magnitude and delay responses (voltage transfer).

P1db is measured at 36 GHz as -6.7 dBm. The performance is compared to other state-of-the-art designs in Table I.

TABLE I
Comparison with measured 2nd order networks above 4 GHz.

	Q_D	f_0 (GHz)	-3dB (GHz)	Technology	Size (mm^2)	Power (mW)	Δ $\lvert T \rvert$ (dB)**
[*]	3.6	36	40	0.13 µm SiGe	0.0625	9.3	1.4
[4]	0^	0	12.2	0.16 µm CMOS	0.07	90	~ 1.4
[5]	0^	0	4.38	0.18 µm CMOS	0.0512	7.88	-
[7]	0.19	3	4	0.25 µm CMOS	0.085	< 95	~ 1.5
[8]	0.04	7	13	0.13 µm CMOS	0.0627	18.5	~ 0.5
[9]	0.098	7	16.5	0.09 µm CMOS	-	< 27	< 1
[10]	0.049	6.3	12	0.13 µm CMOS	-	16.5	~ 1.5
[11]	0.047	6	7.5	0.25 µm SiGe	0.49#	121	~ 1

*This work. ^Cascaded two first-order sections (no complex pole/zero). #Including pads. **T represents either a power or voltage transfer function.

IV. Conclusion

An optimization-based, layout-focused design procedure is applied to produce the first dispersive active on-chip mm-wave second-order all-pass network with a delay Q_D-value of 3.6, which enables various ASP applications for the first time. Future work will focus on synthesizing higher-order delay functions by cascading multiple second-order all-pass sections, introducing post-production tuning mechanisms for f_0 and $\Delta\tau$, and including impedance matching for 50 Ω system integration.

References

[1] A. Ghosh *et al.*, "Millimeter-wave enhanced local area systems: a high-data-rate approach for future wireless networks," *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 6, pp. 1152–1163, 2014.

[2] S. Gupta, A. Parsa, E. Perret, R. V. Snyder, R. J. Wenzel, and C. Caloz, "Group-delay engineered noncommensurate transmission line all-pass network for analog signal processing," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 9, pp. 2392–2407, 2010.

[3] P. J. Osuch and T. Stander, "A geometric approach to group delay network synthesis," *Radioengineering*, vol. 25, no. 2, pp. 351–364, 2016.

[4] S. K. Garakoui, E. A. Klumperink, B. Nauta, and F. E. van Vliet, "Compact cascadable gm-C all-pass true time delay cell with reduced delay variation over frequency," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 3, pp. 693–703, 2015.

[5] Y. W. Chang, T. C. Yan, and C. N. Kuo, "Wideband time-delay circuit," in *European Conference In Microwave Integrated Circuits*, 2011, pp. 454–457.

[6] C. Caloz, S. Gupta, Q. Zhang, and B. Nikfal, "Analog signal processing: a possible alternative or complement to dominantly digital radio schemes," *IEEE Microwave Magazine*, vol. 14, no. 6, pp. 87–103, 2013.

[7] X. Lin, J. Liu, H. Lee, and H. Liu, "A 2.5- to 3.5-Gb/s adaptive FIR equalizer with continuous-time wide-bandwidth delay line in 0.25-µm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1908–1918, 2006.

[8] P. Ahmadi, B. Maundy, A. S. Elwakil, L. Belostotski, and A. Madanayake, "A new second-order all-pass filter in 130-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 3, pp. 249–253, 2016.

[9] M. Maeng *et al.*, "0.18-um CMOS equalization techniques for 10-Gb/s fiber optical communication links," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3509–3519, 2005.

[10] P. Ahmadi, M. H. Taghavi, L. Belostotski, and A. Madanayake, "10–GHz current-mode 1st and 2nd order allpass filters on 130nm CMOS," in *IEEE 56th International Midwest Symposium on Circuits and Systems*, 2013, pp. 1–4.

[11] M. Hamouda, G. Fischer, R. Weigel, and T. Ussmueller, "A compact analog active time delay line using SiGe BiCMOS technology," in *2013 IEEE International Symposium on Circuits and Systems*, 2013, pp. 1055–1058.

[12] H. Rubin and R. Even, "Single-transistor all-pass networks," *IEEE Transactions on Circuit Theory*, vol. 20, no. 1, pp. 24–30, 1973.