A SLOW-WAVE CMOS DELAY LINE FILTER FOR MM-WAVE APPLICATIONS

by

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SUMMARY

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The standardisation of the 60 – 80 GHz band by the IEEE802.15.3 task group 3C offers prospects for high speed gigabit wireless applications. This mm-wave band can be used to achieve high data rate transmission in high definition television processing and mobile data applications. Electronic devices utilising the 5^{th} generation cellular standard will begin to use such transceiver chipsets. Nanoscale complementary metal oxide semiconductor (CMOS) technologies have enabled complete mm-wave systems-on-chip (SOC) containing distributed passive, RF active, and CMOS logic circuits. This approach offers the advantage of lower cost, reduced size and lower power consumption. Front-end filters are, however, typically omitted from this system integration due to the low achievable *Q*-factors of the constituent resonators, which results in high insertion loss and reduced selectivity. There is, therefore, a need for on-chip RF pre-select filters with low insertion loss that are immune to this *Q*-driven degradation.

This research is aimed at the realisation of a miniaturised high performance passive filter in a CMOS technology for mm-wave technologies. Research questions have been formulated where the research outcomes result in a mm-wave passive filter topology. Firstly, the delay line filter is identified as a possible solution for implementation at mm-wave frequencies. Research has been conducted into CMOS planar transmission lines and their associated effects to identify the best suited geometry. Secondly, it is found that the delay performance of a transmission line can be improved by means of introducing geometrical shielding structures. The performance of the CMOS delay lines is evaluated using the quality factor (*Q*-factor) and group delay as a measure of importance.

The delay lines are implemented within a delay line filter topology. The filter is synthesised and simulated in a circuit solver, after which the delay line and complete filter are simulated in a 3D full-wave electromagnetic (EM) simulation tool. The artwork of the complete design is exported, from the integrated circuit (IC) design tool, into the full-wave EM simulator to evaluate and verify the performance of the filter. Three slow-wave coplanar waveguide (CPW) delay lines and a passive mm-wave filter are designed and prototyped using the 0.13 µm bipolar complementary metal oxide semiconductor (BiCMOS) process from GlobalFoundries US as part of the experimental process. The best performing delay line, based on simulation results, has been implemented in a passive filter. The experimental verification confirms the 3D full-wave EM simulation results and answers the proposed research questions.

Three CMOS CPW transmission lines have been manufactured and tested. Shielded CPW structures with narrow and wide strip spacings were manufactured to understand the slow-wave mechanism. A third fabricated CPW with no shielding structures was used for comparison purposes. Slow-wave geometries have previously been studied, but this research focuses on the *Q*-factor and delay performance of the slow-wave CPW. Simulation and measured results demonstrate that the narrow strip spacing CPW achieves the greatest group delay at 70 GHz. The narrow strip spacing, wide strip spacing and no strip spacing lines achieve *Q*-factors of 38.3, 33.64 and 24.9 at 70 GHz respectively, with the narrow strip spacing showing a 34.9 % improvement in *Q*-factor compared to the no strip spacing CPW. The filter demonstrates a centre frequency of 70.05 GHz, a -3dB bandwidth of 20.74 GHz, a passband attenuation of 5.83 dB and a *Q*-factor of 4.82. The slow-wave filter compares well with recent literature published on CMOS mm-wave filters.

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LIST OF ABBREVIATIONS

BEOL	Back end of line
BGA	Ball grid array
BiCMOS	Bipolar complementary metal oxide semiconductor
CPW	Coplanar waveguide
DC	Direct current
DUT	Design under test
EM	Electromagnetic
FEM	Finite element method
FET	Field effect transistor
FIT	Finite integral technique
GSG	Ground-signal-ground
HBT	Heterojunction bipolar transistors
IC	Integrated circuit
ISS	Impedance standard substrate
LVS	layout-versus-schematic
MEMS	Micro-electromechanical system
MMIC	Monolithic microwave integrated circuits
MOSFET	Metal oxide semiconductor field effect transistor
NMOSFET	N-type MOSFET
PEC	Perfect electrical conductor
SDL	Switched delay line
SOC	System on chip
SOI	Silicon on insulator
SOTL	Short-open-through-load

SPDT	Single pole double throw
SPICE	Simulation program with integration circuit emphasis
SPST	Single pole single throw
TRL	Thru-reflect-line
VNA	Vector network analyser

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CHAPTER 1 INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Context of the problem

Millimetre-wave (mm-wave) transceivers have received a significant amount of interest and have experienced a rapid development boost due to the standardisation of the 60 – 80 GHz band by the IEEE802.15.3 task group 3C [1]. The mm-wave band can allow for data rates of up to 1.6 Gb/s per 2.16 GHz channel band [1]. IEEE 802.11ad applications make use of the 60 – 80 GHz band to achieve high data rate transmission in high definition television (HDTV) processing and transmission applications. As the cost and power consumption of embedded devices decrease, many other electronic devices utilising the IEEE 802.11ad and 5th generation cellular standard will begin to use such transceiver chipsets in order to reach higher data speeds.

Complementary metal oxide semiconductor CMOS is the dominating technology for digital circuits and is consequently cost effective and reliable for high volume production. The System-on-chip (SOC) technology presents the advantage of all components being integrated on the same chip and therefore prevents off-chip interconnect losses, which are prevalent at mm-wave frequencies. Transceivers consist of several building blocks such as input and output stages, power amplifiers, low noise amplifiers (LNAs), mixers, oscillators, filters and matching networks [2]. These building blocks typically consist of individual integrated circuits (ICs) within a common medium [3]. It would be an attractive alternative to use a common technology to design a complete system and thereby realise an SOC integration which will reduce size and cost as well as increase reliability. Silicon-germanium (SiGe) CMOS technologies allow for the realisation of heterojunction bipolar transistors (HBTs), culminating in devices that can reach transition frequencies (f_T) in excess of 200 GHz. Such transistors are desirable in front-end building blocks such as

LNAs due to the improved noise performance associated with the high current gain (β), and low base resistance (r_B) [4].

An integrated CMOS filter is therefore needed to support the mm-wave frequency band as discussed in the previous paragraphs. State-of-the-art long term evolution (LTE) and 5th generation transceivers use mm-wave filters to eliminate out-of-band interfering sources. Coupled resonator filters [5] - [8] adopt the technique of tuning the resonant frequency by varying the properties of the reactive elements within the resonator. Coupled resonator filters, however, provide narrow passbands and may not cover multiple bands or standards [9]. Intrinsic resistances and dielectric losses within the reactive elements degrade the performance of a filter. The parasitic effects associated with active filter designs at mm-wave frequencies outweigh the buffering and size advantages.

Analogue integrated delay lines have important applications in signal processing and RF front-end applications [9] due to their broadband frequency properties and are attractive to use in RF CMOS applications. Delay line filters can be used to create non-resonant filters [10]; however, such research has not been conducted on-chip and at mm-wave frequencies. IC designers are further faced with the challenge of length and area restrictions, particularly within the high frequency band.

1.1.2 Research Gap

High performance filters with low insertion loss, high selectivity and wide stopband properties are important for wireless data applications within the 70 GHz band. These filters are presently realised by means of E-plane waveguides [11]. They are bulky and have high associated manufacturing costs. Planar guided structures such as microstrip, stripline and coplanar waveguide (CPW) filters are common other choices in this frequency range for off-chip applications, but their efficiency is restricted by their poor selectivity as a result of a limited quality (Q)-factor caused by loss and radiation[12]. Active filters are not feasible at mm-wave frequencies due to the additional noise introduced by the active element [13]. Passive filter designs are therefore proposed due to their stability, wide operating power regions, low cost and linearity. These passive filters are used in many applications [13]; however, it is not possible to realise lumped network filters with high Q-factors at mm-wave frequencies, since the associated wavelengths are

comparable to the actual dimensions of the circuit elements [13]. Miniaturisation and SOC technologies have shown that on-chip filter can be implemented, where the wavelengths associated with the lumped elements are no longer comparable with the dimensions of a typical on-chip circuit equivalent. The ongoing miniaturisation of monolithic microwave integrated circuits (MMICs) has resulted in a drive towards passive on-chip filter topologies [14].

Passive delay line based filters [10], [15] have been implemented for the L-band utilising a Rogers RT 6010 substrate. Tuning is achieved by means of configuring the delay line length without introducing active elements, which would subsequently lead to additional losses. Such designs have not been attempted on-chip and at mm-wave frequencies to date. It is therefore necessary to realise a miniaturised filter, implemented on-chip, and that can operate at mm-wave frequencies. This serves as the identified research gap for this research.

1.2 RESEARCH OBJECTIVE AND QUESTIONS

This dissertation investigates specialised design considerations and techniques required to realise a CMOS based mm-wave delay line for implementation within a mm-wave filter topology while still taking into account the on-chip length and area restrictions. Subsequently, this research further focuses on improving the area limitation currently involved with the design of passive mm-wave CMOS filters.

Passive filter designs are proposed to be used for mm-wave applications due to advantages listed in the above section. It is necessary to understand mm-wave delay lines and to identify the best solution in order to achieve the best filter. It is therefore essential to determine the propagation characteristics of the transmission delay lines. These properties are to be studied, quantified and analysed in order to effectively model them. The said properties are thereafter implemented within a circuit simulation and design model.

The following research questions are constructed from the problem statement and research gap:

- How can integrated mm-wave CMOS delay lines be realised?
- How can a delay line filter be miniaturised?
- How can a mm-wave delay line filter be realised on chip?

1.3 APPROACH

The approach followed to investigate the research questions consisted of a thorough literature study on fundamental transmission line theory, the various geometries of transmission lines and how certain geometrical parameters influence the characteristic properties of the respective structure at mm-wave frequencies. The fundamental propagation mode theory, lumped-element models and shielding structures of CMOS transmission lines were investigated. A study of the delay line filter operation, the mathematical model, the key building blocks that make up the filter and how each may be constructed in a CMOS process was conducted. An ideal circuit model was designed in software to understand the key parameters that influence the characteristics of the filter. A theoretical filter synthesis is used to calculate the transmission line time delay needed by each element in order to achieve the required conventional filter parameters. The delay line structures are thereafter modelled in 3D full-wave EM simulation software. The simulation is used to determine the parameters that influence the characteristics of CMOS transmission lines. Thereafter, a delay line network utilising the slow-wave propagation mode principle is modelled in full-wave 3D EM simulation software. The simulation model was used to optimise the design and to investigate the related research questions highlighted in the previous section. The optimised transmission line structure was implemented within a delay line filter and simulated at a schematic and at a 3D full-wave EM level. The layout entries of the slow-wave delay lines and filter were modelled in the EM software. The designs were sent for fabrication and prototyping. The fabricated IC was measured for practical performance and used to validate simulation results. The design methodology description can be found in Chapter 3.

1.4 RESEARCH GOALS

The goal of this research is to understand slow-wave transmission line theory and how it can be implemented within CMOS technology in order to achieve a mm-wave delay line. Firstly, it was necessary to investigate how planar transmission line structures could be realised on-chip using the slow-wave propagation technique. Once complete, the research focused towards implementing a mm-wave delay line filter using slow-wave delay lines. The criteria for the proposed filter had to include the capability of performing in the E-band with competitive efficiency compared to similar CMOS filter technologies. The thesis aims at validating the research questions posed in the above sections. It is envisaged that the study will encourage future research initiatives using CMOS based slow-wave transmission lines for mm-wave applications.

1.5 RESEARCH CONTRIBUTION

The contribution of the research is, firstly, an investigation into CMOS slow-wave CPWs and the provision of an optimal design for use as an on-chip delay line. Secondly, a novel CMOS passive filter design is presented using the on-chip slow-wave delay lines. By realising the filter design, this research also demonstrates that EM modelling can effectively characterise an on-chip mm-wave structure. By achieving the research goals, this dissertation demonstrates one of the first CMOS passive mm-wave on-chip delay line filter designs utilising slow-wave transmission line theory.

1.6 OVERVIEW OF STUDY

The outline of the dissertation is as follows:

- Chapter 1: Introduction

  This chapter serves as an introduction to the research problem and poses the motivation for passive CMOS filter implementation. It also establishes the research questions, goals and contributions. A brief introduction into the research approach is presented.

- Chapter 2: Literature Review

  This chapter is divided into two sections. The first section introduces transmission line and delay line theory. It explores the role of the slow-wave propagation mode in the CMOS technology. The second section discusses filter designs and identifies the delay line filter theory and sub-circuits which can be implemented within a CMOS technology process.

- Chapter 3: Research Methodology

  The research methods used in order to design, simulate and measure the functional circuit are presented in this chapter. The chapter further discusses the experimental setup used to evaluate the research questions. Software design packages, measurement equipment and the measurement setup used to test the prototype IC are discussed.

- Chapter 4: Design and Simulation

  This chapter is divided into two sections. The first section discusses the design, modelling, simulation and implementation considerations of the mm-wave slow-wave CMOS delay lines. Three variants of the slow-wave delay line have been prototyped in order to study how the transmission line performance relates to the floating metal dimensions. The second section discusses the delay line filter, including detailed considerations of the power splitter in conjunction with the slow-wave delay lines. Simulation results of the mm-wave filter are presented.

- Chapter 5: Layout and Fabrication

  The layouts of the slow-wave delay lines, power splitter, switching devices and filter topologies are presented. The process specific design consideration and layout limitations are also discussed, as well as the design and layout of the calibration standards.

- Chapter 6: Results and Discussion

  The measurement results of the slow-wave transmission lines and filter are presented in this chapter. The experimental results for each circuit are de-embedded in order to remove measurement parasitics. The prototyped measurement results are

compared to simulations and the correspondences are discussed. Several setbacks and problems relating to the switching device are highlighted. An interpretation of the experimental results concludes the section.

- Chapter 7: Conclusion

  This chapter summarises the research work conducted on CMOS slow-wave delay lines and the passive filter design. The chapter provides critical evaluation of the research questions and findings from the simulations and experimental results. The chapter discusses the limitations of the study and future areas of research.

CHAPTER 2 LITERATURE REVIEW

2.1 CHAPTER OBJECTIVES

Microwave delay lines represent an important component in delay line filters and phase shifters which are used in phased array and radar system applications. Conventional printed circuit board and coaxial delay lines suffer from high insertion loss. They occupy a large area and therefore are difficult to integrate, given the shrinking dimensions of mm-wave circuits. Monolithic integrated circuits could serve as a viable medium for realisation of delay line based circuits that are able to operate at mm-wave frequencies. The integration of delay lines with high speed CMOS devices allows for the realisation of complete SOCs.

The first part of this chapter focuses on transmission lines and planar guided medium theory. The line modelling theory is critical in implementing on-chip delay line networks. The section investigates the various types of planar transmission lines, the trade-offs of each and their associated operating principles. The transmission line best suited for IC implementation is chosen based on a comparative study. The slow-wave transmission mode is explored as a mechanism to reduce the group velocity of a transmission line, consequently shrinking electrically long elements and reducing required on-chip area. Several slow-wave delay line networks utilising shielding are discussed in this section.

The second part of this chapter discusses different fixed and frequency agile filter designs at mm-wave frequencies and identifies the delay filter theory and topology which can be implemented in a CMOS technology process. This chapter further discusses various mm-wave switching elements.

2.2 PLANAR TRANSMISSION LINES

Metal strips placed on a dielectric substrate form a Transverse Electromagnetic (TEM) planar transmission line which is used in MMICs photolithographic manufacturing [16]. TEM and quasi TEM planar transmission lines are broadband, which can easily be adapted to hybrid fabrication technologies, and can be constructed using low cost CMOS and printed circuit board (PCB) processes.

2.2.1 Circuit model

Planar transmission lines can be analysed as a variant of a two-wire transmission line [16]. The time domain descriptions for the voltage and current on a point in the line are known as the *telegrapher's equations* and are defined by distributed parameters *R*, *L*, *C* and *G* which represent the frequency dependant resistance, inductance, capacitance and conductance of the transmission line, respectively [16]

$$\frac{dV(x)}{dx} = -(R + j\omega L)I(x) \tag{2.1}$$

$$\frac{dI(x)}{dx} = -(G + j\omega C)V(x). \tag{2.2}$$

The current *I(x)* can be calculated by solving the differential Equations from (2.1) and (2.2) as

$$I(x) = \frac{\gamma}{R + j\omega L}\left[V_o^+ e^{-\gamma x} - V_o^- e^{\gamma x}\right], \tag{2.3}$$

where $\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$. V_o^+ and V_o^- represent the respective positive and negative *x*-directed voltage wave magnitudes. The ratio of voltage amplitude to current amplitude of each of the travelling waves can be calculated from (2.3) and is known as the characteristic impedance of the transmission line.

$$Z_0 = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.4}$$

The wavelength (λ) of the transmission line and the phase velocity (v_p) are given by

$$\lambda = \frac{2\pi}{\beta} \tag{2.5}$$

$$v_p = \frac{\omega}{\beta} = \lambda f. \tag{2.6}$$

For TEM waves, the phase velocity can be expressed as

$$v_p = \frac{c}{\sqrt{\mu_r \varepsilon_r}}, \tag{2.7}$$

where ε_r and μ_r are the respective relative permittivity and relative permeability of the propagating wave mediums and c is the speed of light in free space. In some media the phase velocity varies with frequency and therefore the same phase relationship is not maintained. Such an effect is called dispersion; it allows the faster travelling waves to lead the slower waves and results in the original phase front being gradually dispersed as the wave propagates along a transmission line. TEM waves are classified as non-dispersive while Transverse electric (TE) and Transverse magnetic (TM) waves demonstrate dispersion. The group velocity (v_g) of a signal can be described as the velocity of a narrowband (ω_o) signal with insignificant dispersion across the signal band [16] and can be quantified as the rate of change of transmission phase angle with respect to frequency

$$v_g = \left(\frac{d\beta}{d\omega} \right)^{-1} \Bigg|_{\omega=\omega_o}. \tag{2.8}$$

Group velocity is the speed at which electromagnetic information travels while the group delay of a transmission line is the length of this line divided by the group velocity. From (2.8) it can be further calculated that group velocity is inversely proportional to that of phase velocity

$$v_g = \frac{c^2}{v_p}. \tag{2.9}$$

2.2.2 Stripline

A stripline consists of a metal strip oriented between and lying parallel to two wide conducting metal ground planes. The region between the ground planes is filled with a

uniform dielectric. The structure can be approximated by two parallel planes [17] if the strip width, *W* is much greater than the spacing *b* and if the two planes are grounded or at the same potential. The electric and magnetic field lines are perpendicular to the wave propagation.

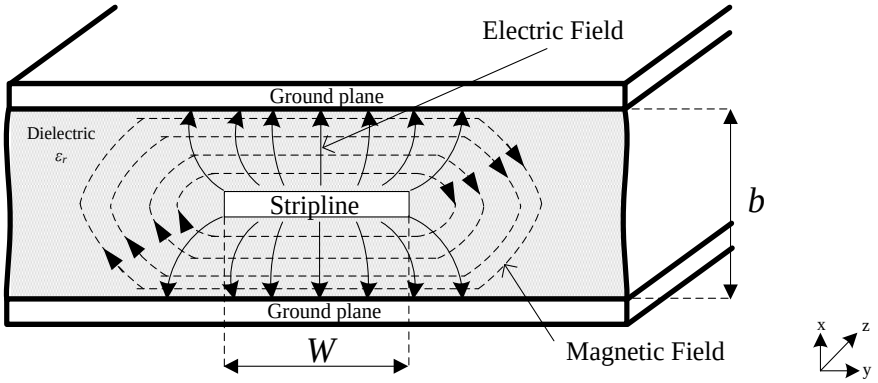


Figure 2.1. Cross section of a stripline with electric and magnetic field lines.

2.2.3 Microstrip

Microstrip lines are the most common form of planar transmission line due to the fact that they can be easily fabricated and can easily be integrated with other passive and active integrated devices. A microstrip line consists of a single conducting strip of width *W* lying on top of a grounded dielectric of thickness *b* with a conducting backplane present on the opposite side.

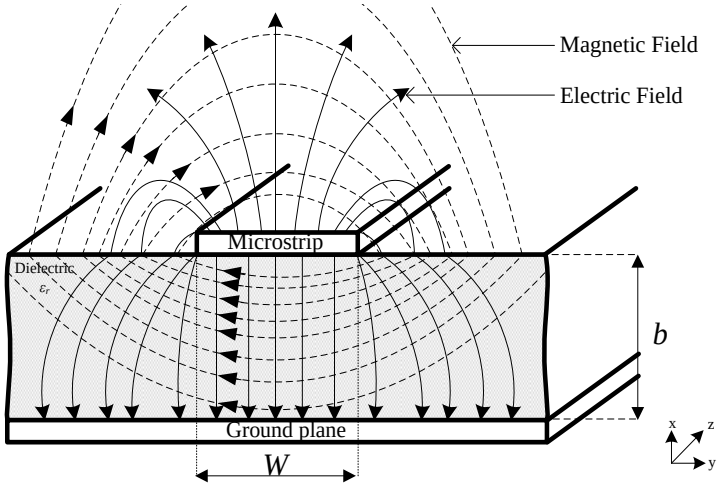


Figure 2.2. Cross section of a microstrip with electric and magnetic field lines.

The electric and magnetic fields of a microstrip do not all lie within the dielectric region due to the fact that the dielectric does not cover the region above the microstrip. The

majority of the field lines occupy the region between the microstrip and ground plane, with some of the field lines occupying the air region above the microstrip. This field distribution complicates the analysis of the microstrip as it does not support pure TEM wave propagation since the phase velocity of the wave in the dielectric is different to the phase velocity of the wave in the air. The fields can be described as quasi-TEM [16]. Microstrip transmission lines have been used for mm-wave applications; however, findings have shown attenuation in the vicinity of 2 dB/cm when used in standard RF CMOS [18].

2.2.4 Coplanar waveguide

CPW structures are an effective alternative compared to microstrip lines and are capable of achieving characteristic impedances around 50 Ω on-chip [19]. The structure consists of a conducting strip of width *W* separated by a distance *S* from a pair of ground planes which are all on the same dielectric surface of thickness *b*. It has the advantages of easily integrating with active devices since it is mounted on the top of the dielectric and does not require parasitic discontinuities in the ground plane [20] to connect to the lower front end of line circuitry. A CPW can operate in frequencies in excess of 100 GHz [20]. It supports quasi-TEM modes due to the non-homogenous dielectric in the transverse plane of the structure.

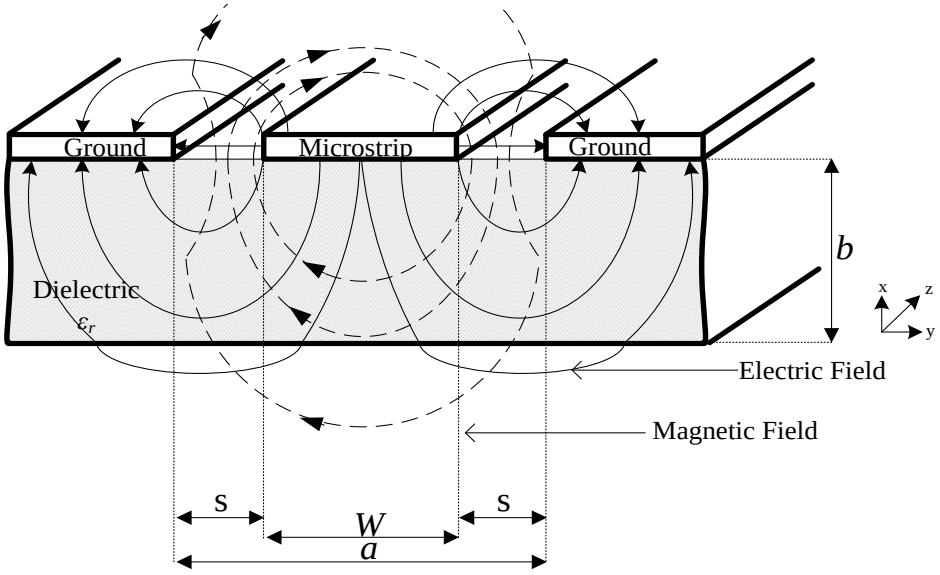


Figure 2.3. Cross section of a CPW with electric and magnetic field lines.

The characteristic impedance can be well approximated by [17]

$$Z_0 = \begin{cases} \dfrac{1}{\pi\sqrt{\varepsilon_e}} \ln\left(2\sqrt{\dfrac{a}{W}}\right) & \text{for } W/a < 0.173 \\ \dfrac{\pi}{4\sqrt{\varepsilon_e}} \left[\ln\left(2\dfrac{1+\sqrt{W/a}}{1-\sqrt{W/a}}\right)\right]^{-1} & \text{for } W/a < 0.173 \end{cases} \tag{2.10}$$

where the effective dielectric constant is defined as: $\varepsilon_e = \dfrac{\varepsilon_r + 1}{2}$

2.3 BACK END OF LINE (BEOL) PROCESS

The BEOL is the secondary process within IC fabrication where the individual active devices, doped resistive and MOS capacitive wafer components are interconnected by means of planar wiring [21]. The BEOL fabrication phase consists of dielectric layers, metal routing layers, vias and final passivation layers with windows for probing or bonding. BEOL processes can accommodate up to fifteen metal layers to allow for high integration density. The bottom metal layer is referred to as 'the local interconnect layer' and is typically used to connect active devices. The top or global metal layer has the thickest and widest metal interconnects resulting in the least resistance and is typically used for power and clock distribution in digital ICs.

2.4 DELAY LINES

Table 2.1 lists typical fixed delay line implementations and their corresponding characteristics to show the context of this CMOS based research. Piezoelectric and RF-micro-electromechanical systems (MEMS) delay lines have not been demonstrated to operate in the mm-wave frequency spectrum, as they typically occupy a large surface area and are difficult to integrate with miniaturised mm-wave elements. CMOS offers the advantage of low fabrication cost and the potential of monolithic SOC integration for mm-wave applications.

Table 2.1 Comparison of passive delay line implementations.

Technology	**Piezoelectric [22]**	**RF-MEMS [23]**	**CMOS [24], [25]**
Frequency	30 MHz – 1 GHz	0 – 10 GHz	Up to 80 GHz [24] , [25]
Insertion loss	10 dB at 1 GHz	0.6 dB at 10 GHz	0.65 dB at 60 GHz [24] 1.6 dB at 60 GHz [25]
Fabrication cost	Medium	High	Low
Size	Large	Large	Small

2.5 SLOW-WAVE TRANSMISSION LINES

Slow-wave transmission lines aim to reduce the group velocity of a transmission line by means of artificially increasing the effective dielectric constant [26]. They are useful in miniaturising large elements, and can operate within the mm-wave frequency band.

2.5.1 Propagation

Three propagation modes exist for a microstrip lines placed on a Si - SiO_2 substrate: the dielectric quasi-TEM, skin effect and slow wave modes have been identified [27].

The dielectric quasi-TEM mode is prominent when Si acts as a strong dielectric. The quasi-TEM mode closely resembles the TEM mode if the signal wavelength is much larger than the combined thickness of the SiO_2 and Si [27]. The skin-effect mode propagates when the substrate conductivity is large, causing little EM field penetration into the substrate. It therefore behaves as a lossy conductor. At high frequencies the skin effect propagation mode suffers from severe dispersion.

The slow-wave mode occurs in-between the first two modes where the Si substrate acts neither as a dielectric nor a conductor. A strong interfacial polarisation occurs and gradually increases as a result of the SiO_2 thickness being much less than the Si thickness [27]. This results in a non-uniform distribution of the electric and magnetic fields between the Si and SiO_2 layers and hence an artificial dielectric is created. As a result the propagation velocity slows down and hence a slow-wave is realised. The slow-wave mode

demonstrates lower attenuation compared to a conventional microstrip line [27]. It is clear that the propagating wave becomes a function of the substrate. The intrinsic impedance (η) and skin depth (δ) of the Si substrate therefore determines the propagation mode of a planar Si transmission line [28]. The intrinsic impedance and skin depth are defined as

$$\eta = \sqrt{\frac{j\omega\mu}{\sigma + j\omega\varepsilon_0\varepsilon_{r,Si}}} \tag{2.11}$$

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}. \tag{2.12}$$

2.5.2 Slow-wave CPW lumped-element modelling

The slow-wave CPW can be expressed as a *RLCG* model of an integrated transmission line [29]. The *RLCG* parameters are expressed in terms of the parameters

$$\begin{aligned} L_{eq} &= \frac{\mathrm{Im}(Z_c \cdot \gamma)}{\omega} && \text{[H/m]}, \\ C_{eq} &= \frac{\mathrm{Im}(\gamma / Z_c)}{\omega} && \text{[F/m]}, \\ R_{eq} &= \mathrm{Re}(Z_c \cdot \gamma) && \text{[}\Omega\text{/m]}, \\ G_{eq} &= \mathrm{Re}(\gamma / Z_c) && \text{[S/m]}. \end{aligned} \tag{2.13}$$

where γ is the propagation constant and ω is the angular frequency. If the slow-wave effect is taken into account, the CPW *RLCG* model can be expressed as [29]

$$\begin{aligned} L_{eq} &= \frac{\mathrm{Im}(Z_c \cdot \gamma)}{\omega} && \text{[H/m]}, \\ C_{eq} &= \frac{\mathrm{Im}(\gamma / Z_c + G(f)_{subs})}{\omega} && \text{[F/m]}, \\ R_{eq} &= \mathrm{Re}(Z_c \cdot \gamma) && \text{[}\Omega\text{/m]}, \\ G_{eq} &= \mathrm{Re}(\gamma / Z_c + G(f)_{subs}) && \text{[S/m]}. \end{aligned} \tag{2.14}$$

$G(f)_{subs}$ is the CPW per-unit-length admittance which models the slow-wave effect between the high loss Si and SiO_2 insulator.

$$G(f)_{subs} = \frac{-2 \cdot S_{11}(f \to 0)}{l \cdot 50 \cdot (1 + S_{11}(f \to 0))}. \tag{2.15}$$

The equivalent *RLCG* model of the slow-wave CPW is shown in Figure 2.4. The *Z* -element, which consists of the *L* and R components, is obtained from the original CPW structure and the Y-element, which consists of the *G* and *C* components, also originates from the original CPW structure. The equivalent non-physical model exhibits good agreement between simulated and measured results [29] .

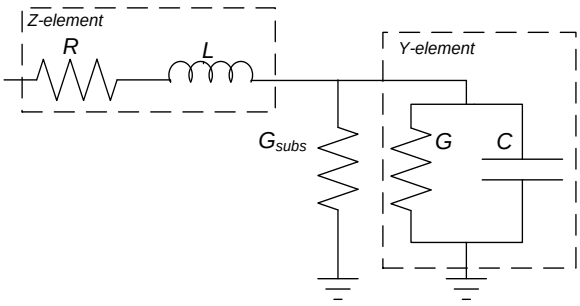


Figure 2.4. *RLCG* model of a slow-wave transmission line.

2.5.3 CPW shielding

Periodically floating metal shield strips can be placed beneath a transmission line in order to provide substrate shielding and affect the slow-wave propagation mode [26]. Parasitic inductances and capacitances coupled from the neighbouring digital circuitries and interconnects make it difficult to realise an on-chip ground reference. Voltage variations on a grounded shield under a CPW therefore lead to current flow and dissipation of energy [26]. Floating metal shield strips however are immune to such variations. The shielded slow-wave transmission line can be implemented in a CMOS BEOL to achieve a slower propagation velocity and without excessive substrate loss .

A reduction is the phase velocity results in the reduction in wavelength at a chosen frequency. The wavelength can however be reduced by means of introducing periodic floating metal strips, as shown by Figure 2.5, that increases the relative permittivity of the dielectric medium, thus creating an artificial dielectric [26]. If the length of the floating strip is short compared to the wavelength then slow-wave CPW can be modelled as two

segments. Segment A can be modelled as a section above a shield line and Segment B can be modelled as a section on top of an open slot [26].

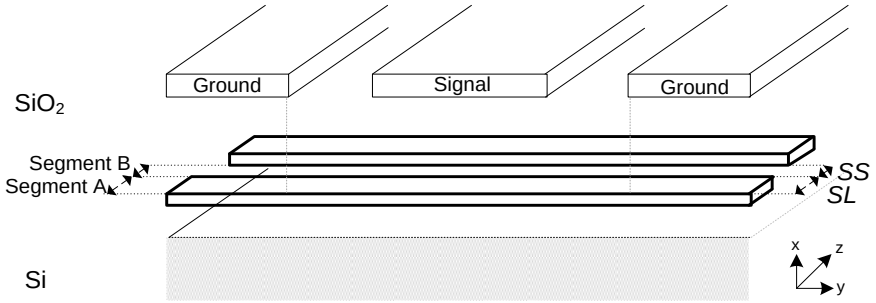


Figure 2.5. Slow-wave CPW with floating metal strips.

Figure 2.6 shows the EM filed distribution for Segment A and Segment B. The electric field in Segment A starts from the signal line, couples to the floating strips and terminated on the coplanar ground conductors [26]. Thus the EM fields are concentrated in the region between the floating strip and CPW. In Segment A the CPW the EM fields penetrate into the Si substrate.

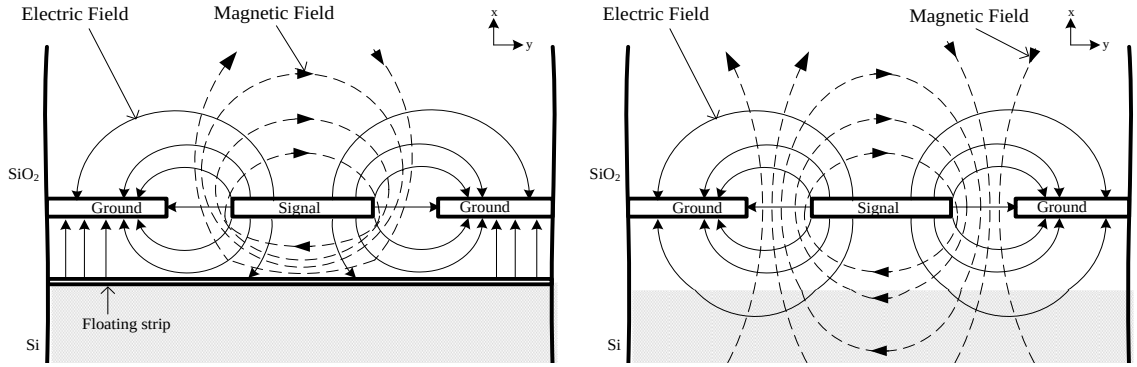


Figure 2.6. Electric and magnetic field distribution of slow-wave CPW. (a) Section of EM field at Segment A. (b) Section of EM field at Segment B.

Each segment can be modelled by an inductance and shunt capacitance per unit length. The slot density ratio R is defined as

$$R = \frac{SL}{SL + SS}. \tag{2.16}$$

Segment B can be modelled as a series inductance and shunt capacitance and Segment A can be modelled as the same, however with an increased shunt capacitance value due to the presence of the floating metal strip. The increased capacitance ratio between Segment A

and Segment B is referred to as *n*. The phase velocity of the slow-wave CPW can be defined as

$$V_p = \frac{c_o}{\sqrt{\varepsilon_r \mu_r}} = \frac{1}{\sqrt{LC(nR)}}, \tag{2.17}$$

and it can be seen that the phase velocity if the CPW decelerated by a factor of $\sqrt{nR}$ as a result of the floating metal strips [26].

2.5.4 CPW losses mechanisms

CPWs typically suffer from high attenuation in the mm-wave band comparable to microstrip losses. This limits the performance of such transmission lines. Attenuation is strongly dependent on CMOS process parameters, material properties and the transmission line geometry.

2.5.4.1 Substrate loss

The resistivity of Si typically varies from 0.00001 Ω-m to 100 kΩ-cm, depending on the doping intensity. EM energy is converted into heat within Si as a result of its conductive nature. Capacitive, inductive and EM induced substrate loss are the three main loss mechanisms associated with the substrate. Free carriers at the Si-SiO_2 interface within CMOS locally increase the substrate surface conductivity and therefore result in additional losses. EM induced losses also occur when the device size approaches the wavelength of the propagation frequency within CMOS.

2.5.4.2 Metal loss

Non-ideal conductivity characteristics of metal components and interconnects lead to resistive losses. DC and high frequency losses are the typical metal loss mechanisms in CMOS. DC losses are dependent on the cross-sectional area and resistivity of a conductor as it is assumed that the electric current is uniformly distributed within the latter. Surface roughness becomes significant when the roughness becomes of the order of the skin depth, resulting in attenuation.

2.5.4.3 Dielectric loss

Dielectric loss relates to the energy loss associated with the dissipation of an EM field within a dielectric material. A varying EM field in a dielectric medium is converted into heat. It is characterised by the loss angle δ, or loss tangent tan (δ).

2.5.4.4 Radiation loss

Radiation loss is the energy within a circuit that is lost by radiating away from the circuit into the surrounding environment. EM induced radiation loss occurs when the physical dimensions of the device approach the free space wavelength at the frequency of operation.

2.6 TUNEABLE SLOW-WAVE CPW DELAY LINE

A tuneable phase shift can be realised on CMOS [30]. The control is achieved by means of the floating metal shield structures being connected to the drain and source of an N-type metal oxide semiconductor field effect transistor (NMOSFET) implemented in 0.13 µm CMOS. The NMOSFET acts as a variable resistor and when the gate voltage is varied, the drain-source resistance is tuned. In so doing, the coupling of the electric and magnetic fields between the shields and CPW is varied and consequently, the permittivity of the artificial substrate can be altered. This results in an integrated delay line which is tuneable by the gate voltage of the NMOSFET. The experimental results indicated that the controllable delay line can be used for applications up to 110 GHz [30]. The structure demonstrates a low attenuation, of between 3.2 and 5.5 dB, for a 520 µm length transmission line. The device operates in the 63 – 98 GHz band with characteristic impedance of between 30 and 55 Ω.

2.7 FREQUENCY FILTERS

Both passive and active filter designs can be implemented on-chip. Table 2.2 summarises the key performance indices of mm-wave filters and compares these to similar published designs. CMOS mm-wave filters typically achieve a *Q*-factor between 3.28 and 7.7 when operating between 60 GHz and 80 GHz. The *Q*-factor of the filter is defined as the centre frequency divided by the -3 dB bandwidth of the filter.

Table 2.2 Comparison of passive mm-wave filters in CMOS.

Reference	Process	f_c (GHz)	-3 dB Bandwidth (%)	Passband Attenuation at f_c (dB)	Q-factor
[31]	0.18 µm CMOS	64	18.76	4.9	3.41
[32]	0.13 µm CMOS	60	18.28	2.56	3.28
[33]	0.18 µm CMOS	66	19.05	3.10	3.46
[34]	0.18 µm CMOS	77	10	9.3	7.7

Reconfigurable or agile filters are defined as filters where the design parameters can be switched between discrete states. Tuneable filters refer to filters where the design parameters can vary continuously. Table 2.3 compares the various frequency agile and tuneable filter topologies.

Table 2.3 Comparison of mm-wave reconfigurable and tuneable filters.

Filter type	Advantages	Disadvantages	f_c (GHz)	-3 dB Bandwidth	Size (mm^2)
Reconfigurable quartz CPW filter with MEMS switches. [35]	• Good stability	• High cost • Large area	50 GHz	17 GHz	5.40
			20 GHz	8 GHz	
Reconfigurable quartz filter with Niobium MEMS switch. [36]	• Process stability • Reliable actuation	• High cost • Large area	20.7 GHz	500 MHz	7.7
			23.25 GHz	700 MHz	

Filter type	Advantages	Disadvantages	f_c (GHz)	-3 dB Bandwidth	Size (mm^2)
Reconfigurable CMOS inductively coupled filter with MEMS switched capacitor. [37]	• Good channel isolation	• High cost • Large area	60 GHz	3 GHz	15.35
Tuneable MEMs Si integrated cavity filters. [38]	• High Q factor • Good tuning ratio • Immune to MEMS contact based failure	• High cost • Large area	6.1 GHz - 24.4 GHz	228.75 MHz	10
Tuneable liquid crystal based filter. [39]	• Low bias field • Low power consumption	• Large area • High insertion loss due to lossy material	33 GHz	1.3 GHz – 5.3 GHz	3.84
Off-chip tuneable rectangular waveguide filter with Fabry–Perot resonator. [40]	• 100 – 140 GHz operation	• High cost • Large area • Non-standard process	110 GHz – 140 GHz	10 GHz	1040

It is evident that the state-of-the-art mm-wave filter designs are predominantly implemented using MEMS technology. The smallest filter occupies an area of 3.84 mm^2. MEMS designs present the advantage of an increased performance per wafer area, but are costly to fabricate. A switched delay line (SDL) reconfigurable filter proposed an alternative topology and can be implemented in the CMOS process without the need for a MEMS switching mechanism [10].

2.7.1 Delay line filter

A switched delay line (SDL) element is shown in Figure 2.7. The structure consists of a power splitter, delay line structure and multi-pole switch. The input signal is divided by means of a power splitter between two opposite ends of a delay line. The delay line network generates standing wave patterns, the magnitude of which is sensed at the multi-pole switch; θ_1 and θ_2 represent the phase of the respective delay paths. The transmission response of the SDL element is determined by the phase relationship between the two delay paths [10]. Therefore, by toggling the multi-pole switch to the appropriate location, the stopband and passband characteristics of the filter may be adjusted. Unlike coupled resonator filters, the non-resonant network avoids high surface currents and strong absorption associated with resonance [4].

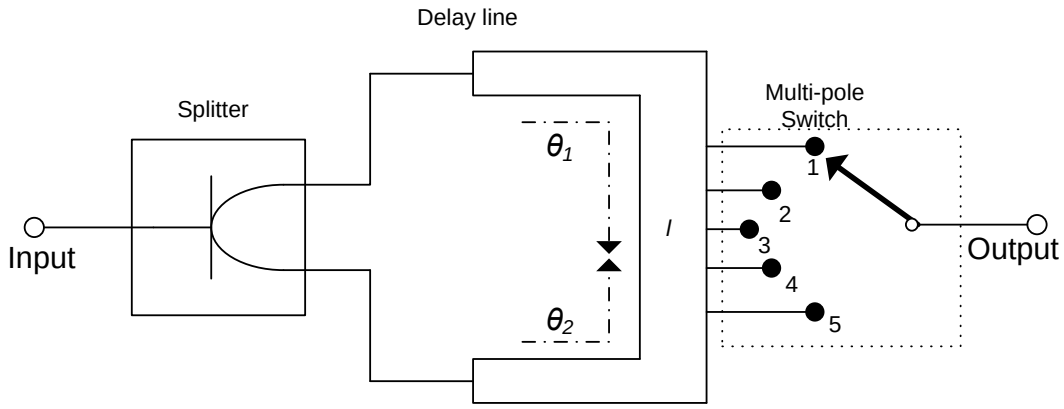


Figure 2.7. SDL element.

2.7.1.1 Chebyshev II filter response

A two-stage filter can be achieved by cascading the two delay line element with a second element with a delay twice that of the first. The transfer function of the structure in Figure 2.8 can be expressed by [10]

$$\left|S_{21}(\omega)\right|^2 = \cos^2\left(\frac{\theta}{2}\right)\cos^2(\theta), \tag{2.18}$$

where

$$\theta = \theta_2 - \theta_1.$$

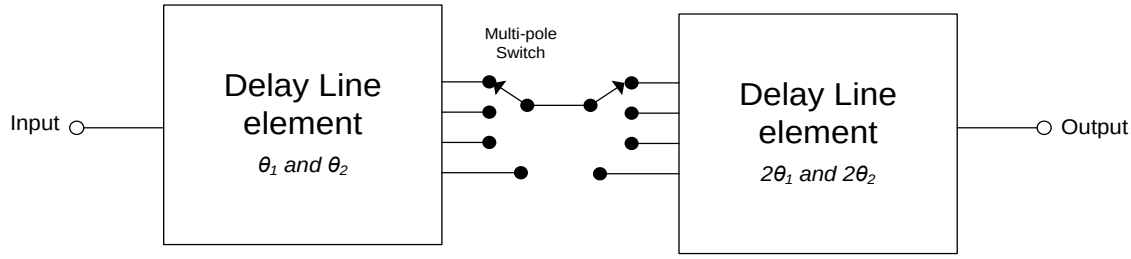


Figure 2.8. Chebyshev II delay line filter.

An N stage filter achieves an Chebyshev II response where additional zeros can be expressed by [10]

$$|S_{21}(\omega)|^2 = \left| \prod_{r=1}^{N} T_r \cos\left(\frac{\theta}{2}\right) \right|^2 . \tag{2.19}$$

where T_r represents the Chebyshev polynomial coefficients and N is the order of the filter. The passband bandwidth is established by the second switch delay-line network [10]. The stopband ripple of a two stage SDL Chebyshev II filter can be calculated using (2.19) by finding the zero crossing derivative. The maximum stopband ripple level of the filter is given by [10]

$$Ripple(dB) = 10\log\left(\frac{1}{|S_{21}(\theta)|^2}\right). \tag{2.20}$$

A unit element (UE) can be introduced between the two delay line resonators in order to improve the bandwidth and stopband rejection. The quarter wave transmission line UE is used to improve passband and stopband rejection [10] as shown in Figure 2.10.

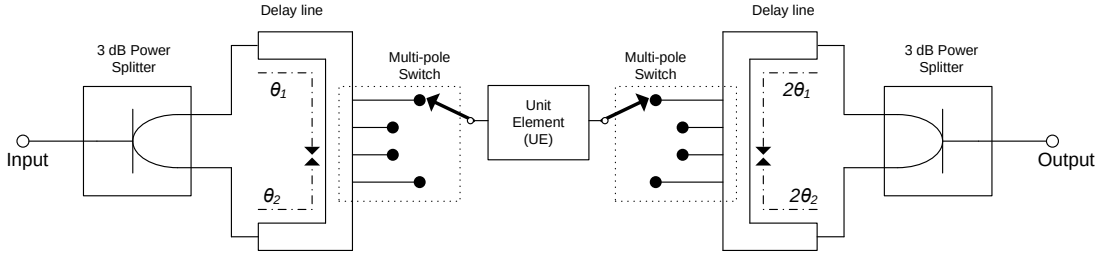


Figure 2.9. Chebyshev II SDL filter with unit element.

A control term $A(\omega, Z)$, defining the UE, is introduced to calculate the bandwidth and stopband ripple without influencing the zeros and poles of the filter. The transfer function of the filter can now be expressed as [10]

$$\left|S_{21}(\omega)\right|^2 = A(\omega, Z)\left[\cos^2\left(\frac{\theta}{2}\right)\cos^2(\theta)\right], \tag{2.21}$$

where

$$A(\omega, Z) = \frac{4\left[1+\tan^2\left(\frac{\pi\omega}{2\omega_o}\right)\right]}{4+\left(Z+\frac{1}{Z}\right)^2\tan^2\left(\frac{\pi\omega}{2\omega_o}\right)}.$$

If $f = 2 f_o$, then $A(\omega, Z) = 1$ and therefore a transmission pole is obtained for $T_r = 1$ for all Chebyshev polynomials. The cut-off frequency (ω_{3dB}) of the SDL filter can therefore be derived as

$$\omega_{3dB} \approx \left(\frac{4Z\omega_o}{\pi(Z^2+1)}\right), \tag{2.22}$$

and the stopband ripple as

$$Ripple \approx \left(\frac{2Z}{Z^2+1}\right)^2. \tag{2.23}$$

The cascaded series-coupled two-stage delay line filter [10] exhibits low stopband rejection of 11 dB and a passband of 14%. A parallel coupled SDL is therefore used to

combat this limitation [15]. The coupling section is achieved by means of a quarter-wavelength coupled open circuited line section as shown in Figure 2.10.

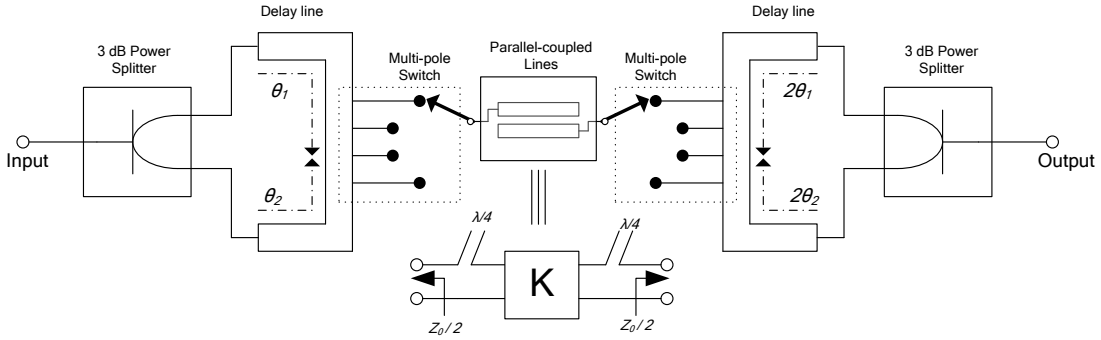


Figure 2.10. Parallel coupled SDL filter.

The parallel coupled line yield half the characteristic impedance of the UE structure which improves the stopband rejection ratio and passband reconfigurability. The transfer function can be expressed as [15]

$$\left|S_{21}(\omega)\right|^2 = K\left[\cos^2(\theta)\cos^2(\theta)\right], \tag{2.24}$$

where K is the transmission coefficient of the coupled line. The bandwidth of the filter can further be varied by scaling the impedance of the switched delay line structure. This may be achieved by introducing an inverter between the parallel delay lines. The parallel coupled SDL filter with inverter tuning achieved a tuning range of 45 % around the centre frequency of 1.6 GHz. Importantly, the filter does not suffer from power saturation effects which commonly occur in varactor loaded filters [15].

2.8 MM-WAVE SWITCHES

A switch is required to tap the delay line at different points in order to obtain various phase relationships between the two branches of the switched delay line filter network. RF and microwave switches are differentiated into two groups: MEMS and solid-state switches. Solid-state switches are typically more reliable, have a longer lifespan, require lower control voltages and can achieve faster switching speeds compared to MEMS [41]. GaAs field effect transistors (FETs) are the most commonly used RF switch due to their manufacturing repeatability, broadband operation and good drain-to-source resistance control advantages. Silicon on insulator (SOI) FET switches present improved cut-off frequencies and are comparable to GaAs devices. The choice of switch is dependent on the

application, switching speed, linearity and operating frequency. Table 2.4 compares the various switch fabrication technologies that are able to operate at mm-wave frequencies.

Table 2.4 Comparison of mm-wave switches [41].

	RF MEMS	**CMOS**	**CMOS SOI**
Insertion loss (dB)	0.1– 5	1.2	0.3 – 2.5
Isolation (dB)	> 30	> 32	> 30
Power handling (W)	< 10	< 5	< 50
Power consumption	Low	Low	Low
Linearity	Good	Good	Good
Switching speed	ns - µs	ns	ns - µs
Size	Small	Small	Small
Cost	Medium	Low	Low

2.8.1 MEMS switches

MEMS switches have proven to be an effective switching mechanism [41]. These switches are categorised into two groups, namely ohmic contacts and capacitive contacts. In ohmic switches, two metal electrodes are brought together to form a low resistance contact while capacitive switches utilise a thin membrane which is pulled over a dielectric to form a capacitive contact. The switch is actuated by means of electrostatic force and features high linearity and low loss compared to FET switches. Disadvantages of MEMS switches include that their switching speed is much slower compared to FETs, that they typically need higher control voltages, and they are more costly to fabricate due to a number of intricate components and processing steps associated with the design.

2.8.2 CMOS switches

A solid state switch is realised in its simplest form when a voltage is applied to the gate terminal of an MOS transistor. The transistor operates in a triode mode when switched on, allowing a low resistance connection between the drain and source terminals of the device. The on-mode resistance of most transistors is equal to $1/g_m$ at the edge of saturation. A large resistance is exhibited between the drain and source of the device in an off-mode

condition; therefore, no conduction can take place. At mm-wave frequencies when the MOS device is operating close to its f_T limit when biased, the off-state impedance of the device is comparable to that of the on-state, resulting in leakage. This is a primary limitation for CMOS mm-wave switches, and certain design techniques need to be adopted to address this issue. A switching structure with the least number of transistors is desired at mm-wave frequencies in order to reduce parasitic effects. An in-line device may also introduce additional loss. Traditional shunt switches occupy a large area as a result of utilising a quarter wavelength transmission line. A lumped component switching circuit is therefore advantageous. Table 2.5 compares literature relating to mm-wave solid state switch topologies. An explanation and discussion of each is shown below.

Table 2.5 Comparison of mm-wave solid state switch topologies.

	[42]	**[43]**	**[44]**	**[45]**
Process	130 nm CMOS	90 nm CMOS	50 nm mHEMT	65-nm triple-well CMOS process
Frequency (GHz)	57 – 66	50	87.8 – 98.2	60
Insertion loss (dB)	4.5 – 5.8	3.4	1.2	2.8
Isolation (dB)	24.1 - 26	13.7	30 - 33	20
Supply voltage (V)	1.2	1	4	-1.4 and 2
Area (mm^2)	0.221	0.004	0.9375	0.42

A single series transistor and two shunt transistors are utilised to form a shunt single pole double throw (SPDT) TX/RX switch [42]. The L-configuration makes use of only one series transistor to limit the induced parasitic losses prevalent at mm-wave frequencies. The topology decreases the amount of off-state leakage, but also increases the on-stage insertion loss. This loss can however be further reduced by choosing transistors with a large gain, increasing W/L and keeping $V_{gs} - V_{TH}$ as large as possible. The SPDT switch operates between 57 GHz and 66 GHz.

A lumped element transformer based SPDT switch topology using shunt transistors in [43] can be realised. Miniature transformers are used to replace the quarter wavelength transmission lines of a conventional shunt switch. The input is connected to the primary winding while the ends of the secondary winding are connected to each output with an

NMOS transistor shunted to ground. Parasitic capacitances are shunted to ground and therefore do not undergo feedback between the input and output terminals. The transformer based SPDT switch demonstrates low insertion loss; however, the input signal undergoes a 180° phase shift. This shift will influence the phase delay of the delay lines and consequently is not suitable for use within a SDL filter topology.

A transmitter topology focused on optimising the transistor drain efficiency [44] consists of an oscillator and an amplitude modulator based on a high speed single pole single throw (SPST) design. The circuit is manufactured in a 150 nm mHEMT process and achieves a normalised on-resistance of 0.35 Ωmm. The RF output signal achieves a dynamic range of 14.5 dB and an insertion loss of 1.2 dB.

A CMOS SPDT switch implemented in a 65 nm triple-well CMOS process used the triple-well floating body technique is used to improve the performance of the switch in the GHz operation band [45]. This is achieved by means of embedding the deep N-Well layer in order to separate the body of the transistor from the p-type substrate as shown in Figure 2.11. Biasing of the p-well and deep n-well is done by means of resistors R_B and R_{DNW}. This configuration results in an increase in the substrate resistance, leading to a reduction in capacitive coupling to the lossy substrate which is prevalent at higher frequencies. The SPDT switch [45] uses a non-ideal triple well CMOS process which drives up fabrication and prototyping costs.

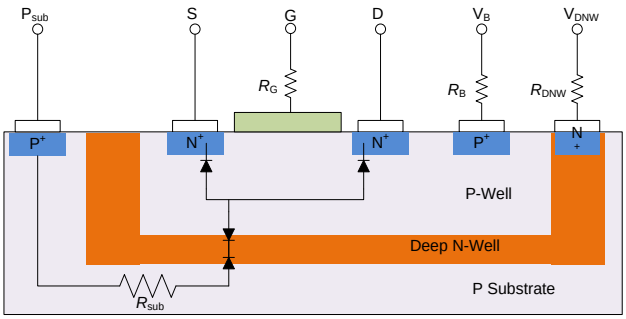


Figure 2.11. Cross section of triple-well nMOSFET.

A slow-wave CPW line connecting two symmetrical branches to a 50 Ω quarter-wave antenna is used to demonstrate the performance of the SPDT at 60 GHz [45]. The SPDT

displays an insertion loss of 2.8 dB and isolation of 20 dB at 60 GHz. It is claimed that the switch operates over a wide bandwidth from 17 GHz to 100 GHz.

2.8.3 SOI switches

SOI devices present less substrate loss and RF coupling effects compared to standard CMOS by stacking FET devices [46]. The device also allows for an equal voltage distribution and therefore presents high linearity. Improvements in SOI devices have resulted in less harmonic and inter-modulation distortion. SOI technology can be used for RF switch applications [47]. The power handling, $R_{on} \times C_{off}$ product and linearity of this improved SOI switch are comparable to those of GaAs and silicon-on-sapphire (SOS) devices.

2.9 CHAPTER SUMMARY

This chapter identifies relevant concepts relating to the design and manufacturing of a mm-wave filter on-chip. Firstly the CPW transmission line was found to be a suitable solution for mm-wave implementation when comparing it to conventional planar transmission lines such as the microstrip and stripline. Slow-wave transmission line theory was thereafter explored [19] and the slow-wave CPW is identified is a suitable solution to realise an mm-wave CMOS delay line. The structure uses floating metal strips placed under the CPW create an artificial dielectric, hence creating a slow-wave. The slow-wave technique also provides effective substrate isolation. A comparison of transmission lines showed that CMOS transmission lines using the slow-wave theory can operate at frequencies up to 80 GHz. Based on previous research, the slow-wave transmission line is expected to achieve attenuation between 1.6 dB and 2.2 dB at 60 GHz.

It was found that CMOS mm-wave single pole filters typically achieve a bandwidth between 18.28 and 10 GHz when operating between 60 GHz and 80 GHz, as reported by Table 2.2. Reconfigurable filters were also compared, and it was found that the state-of-the-art mm-wave filter designs are predominantly implemented using MEMS technology. MEMS technology, however, is very cost intensive. The delay line filter [10] was identified as a solution which can be implemented on CMOS at mm-wave frequencies. The filter makes use of the in-phase and out-of-phase combination of two unequal phase length propagation paths to create a frequency-selective transmission. Unlike coupled resonator

filters, the non-resonant network avoids high surface currents and strong absorption associated with resonance. A comparison of mm-wave switches is presented and it was demonstrated that SDST and SPDT switches can be implemented on CMOS at mm-wave frequencies. This research investigates CMOS switching mechanisms; however, its implementation falls outside the scope of this study.

CHAPTER 3 METHODS

3.1 INTRODUCTION

This chapter presents the method followed in order to address the research questions. This includes information on the EM modelling, the simulation tools used, the process followed to create the full-wave EM circuit models, the layout design, post layout simulations and measurement equipment used to test the research questions.

3.2 METHODOLOGY OUTLINE

The following approach was undertaken for the research and design on the proposed topic of mm-wave delay line filter design.

The literature study conducted in Chapter 2, investigated filter design topologies. The advantages and disadvantages of each were closely studied to find a suitable filter topology for mm-wave CMOS implementation. The delay line filter topology was chosen; thereafter, an investigation was conducted on possible design techniques for miniaturised on-chip mm-wave delay lines. Thereafter, a theoretical filter model was analysed to determine the key design parameters that influence the characteristics of the filter. The analytical model was analysed, which led to the implementation of a circuit model. It is evident from the literature, [19], [25] and [48], that 3D full-wave EM modelling is required at mm-wave frequencies to model the electrical behaviour of the structure, as opposed to 2.5D or circuit solvers. The various subsections of the filter were therefore analysed in 3D full-wave EM software. Once satisfactory results were achieved, the full filter design was simulated in the same 3D full-wave EM software. Several EM simulation tools were also investigated and a suitable tool was chosen. An iterative 3D full-wave simulation approach was subsequently followed for the layout of the delay line filter, and it was also used to compare the results with the theoretical model.

After successful 3D full-wave EM simulations were conducted, experimental verification by means of a fabricated prototype measurement was performed, which allowed for the testing and characterisation of the filter. Taking into account that the design is intended to operate in the E-band, considerations such as floor planning, BEOL tolerances, pad selection, pad placement and ground planes of the prototype had to be taken into consideration in order to ensure that unaccounted tolerances and parasitics did not influence the performance of the device. Measurement equipment was calibrated and the measured results were also de-embedded. The prototype IC allowed for the collection of the necessary data to confirm the research questions and also to suggest further improvements to this work. A flow diagram of this research methodology is shown in Figure 3.1. It is divided into five main sections: research fundamentals, implementation, experimental setup, experimental results and analysis. Each section is further segmented into its sub-sections.

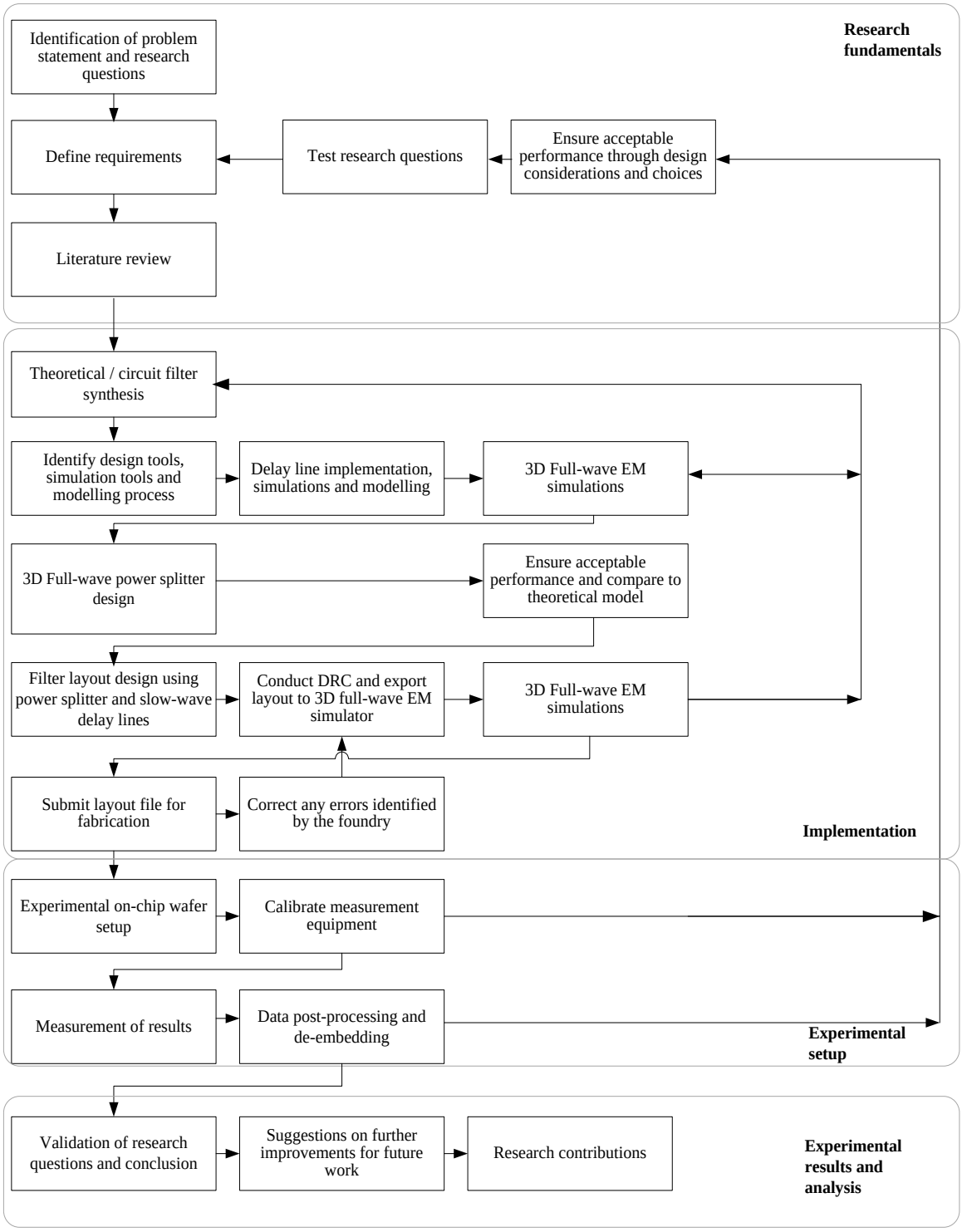


Figure 3.1. Flow diagram of research methodology.

3.3 RESEARCH PROCEDURE

The following list describes the research procedure undertaken to design and prototype the delay line filter:

- *Research fundamentals* – A study was conducted on the operations of the SDL filter and into how this topology could be implemented within a CMOS process. In order to arrive at an mm-wave CMOS delay line filter, an in-depth study was firstly performed on the geometries and slow-wave propagation mechanisms in planar transmission lines and how they influence the characteristic properties of those respective structures. The primary focus was to obtain a delay mechanism which could be implemented in CMOS BEOL. CMOS losses are particularly high and therefore an understanding of the loss mechanism was acquired. Secondly, the delay line filter theory was studied in order to understand the key design parameters that influence the characteristics of the filter. By grasping how to adjust the centre frequency and bandwidth, it was possible to create a delay line filter for operation at 70 GHz. The 70 GHz band was chosen because of the standardisation of the 60 – 80 GHz band by the IEEE802.15.3 task group 3C [1]. The 70 GHz to 80 GHz band is also provisioned for next generation cellular standards. The CMOS transmission line miniaturisation technique of slow-wave propagating modes studied in Chapter 2 was used to implement the filter.

- *Mathematical and software modelling* – Mathematical modelling and software design were used to investigate the performance of the slow-wave delay lines and filter. Several numerical tools such as MATLAB, AWR Microwave Office[1], CST Microwave Studio[2], and ANSYS HFSS[3] were used to plot the numerical, circuit and EM simulations of the delay line filter. The analytical response was investigated in MATLAB based on the theoretical filter equations [15]. An ideal circuit model was built and simulated in AWR Microwave Office to determine the

[1] AWR Corporation is an electronic design automation (EDA) software tool.
http://www.awrcorp.com/products/ni-awr-design-environment/microwave-office
[2] CST is a specialist tool for the 3D EM simulation of high frequency components.
http://www.cst.com/Content/Products/MWS/Overview.aspx
[3] HFSS is a commercial finite element method solver for electromagnetic structures from Ansys.
www.ansys.com/Products/Electronics/ANSYS-HFSS

filter delay line requirements. The slow-wave delay lines and power splitter were implemented in HFSS, a 3D full-wave solver, based on the requirements obtained in AWR Microwave Office. The sub-structures were then incorporated to create the delay line filter. The full-wave synthesis results obtained from HFSS were used to implement the layout of the transmission lines and filter in Cadence Virtuoso[4]. The IC artwork was then re-imported back into HFSS to verify the design by means of 3D full-wave EM simulation.

- *Low-level design* – The filter was prototyped in the 0.13 µm BiCMOS process from GlobalFoundries US[5]. This section of the research procedure includes the final IC layout, with the design rule check (DRC) verification, and includes simulation results. The interface of the wafer probe and CPW was also included in the simulation.

  The experimental setup was subdivided into stand-alone slow-wave CPW delay lines and a filter in order to address the research questions identified in Chapter 1.

  - Slow-wave CPW delay lines – Three CPW slow-wave transmission lines was prototyped independent of the SDL filter in order to identify and characterise the best solution for an mm-wave delay line. The three variants utilise different floating metal strip spacings and dimensions.

  - *Filter* – The passive filter was prototyped in order to demonstrate the performance abilities of CMOS based mm-wave filters without taking into consideration the parasitic and non-linear limitations associated with introducing an active switching element into the circuit.

On-chip measurements were conducted by means of a Vector Network Analyser (VNA) and wafer probing station. The laboratory setup is also capable of applying DC voltages to the wafer, which may be used for biasing the active switching elements in the SDL filter

[4] Cadence Virtuoso from Cadence design systems is the software package used to construct the low level design.
[5] GlobalFoundries is a semiconductor foundry headquartered in Santa Clara, California, United States. http://www.globalfoundries.com/

topology. The measurement equipment and measurement setup are discussed in sections 3.5 and 3.6.

3.4 DESIGN METHODOLOGY

The slow-wave line design in [19] is followed to achieve a miniaturised delay line network capable of operating at mm-wave frequencies. The design methodology describes how the characteristic impedance, phase velocity and effective dielectric constant can be controlled. A further investigation was conducted into the group delay of the slow-wave delay line by varying the strip widths and spacing dimensions. This was done in order to find a possible technique to improve the delay performance of a slow-wave transmission line. The most suitable slow-wave delay line was thereafter implemented in the delay line filter topology.

3.4.1 EM simulation solvers

CST and HFSS have 3D full-wave EM modelling capabilities and therefore are able to estimate the behaviour of the proposed structures. They were used to investigate the key characteristics such as loss, phase response and transmission characteristics. CST and HFSS were both utilised at the start of this research. CST employs the finite integration time domain (FITD) for its time domain solver and is best suited for broadband simulations. CST also uses the finite element method (FEM) for its frequency domain solver. HFSS employs the FEM solver and was preferred over CST because of its better performance when solving high bandwidth, inhomogeneous geometric problems [49]. FEM also performs well in fine mesh geometries within limited boundaries. HFSS was preferred over CST because it allowed for the GDS layout file to be directly imported from Cadence Virtuoso [50].

3.4.2 Modelling, layout and process

The mathematical model was investigated in MATLAB, based on the theoretical filter presented by (2.18). An ideal circuit model was constructed and simulated in AWR Microwave Office to determine the behaviour of the sub-elements and filter. Thereafter, the slow-wave delay lines were implemented in HFSS. Three delay lines were implemented in HFSS (the narrow strip spacing CPW, wide strip spacing CPW and no strips CPWs) to study the performance of each and to identify the geometry best suited for

implementation with the filter. The Wilkinson power splitter was also simulated in HFSS to evaluate its performance. The chosen slow-wave CPW and power splitter geometries were then implemented in the filter as part of the layout design in Cadence Virtuoso[6]. The Assura DRC was conducted in the Cadence Virtuoso layout editor in order to confirm process compliance with the design fabrication standards. The layout-versus-schematic (LVS) check was not conducted due to the absence of a circuit schematic describing the EM passives' connectivity. Once complete, the IC artwork was re-imported back into HFSS via a Touchstone file, and simulated in the 3D full-wave EM environment. This allowed for previously unmodelled components such as vias and process specific metal layers to be modelled within the EM environment; thereby providing an accurate simulation of the design. The EM simulation was compared to the ideal model created in AWR Microwave Office.

The accuracy enhancement technique [51] for on-wafer passive components has been used in HFSS to conduct the 3D full-wave simulation. This technique employs the ground ring approach of modelling the actual wafer measurement setup condition where the ground-signal-ground (GSG) probe tips excite the structure as seen in Figure 3.2. The modelled GSG probes consist of a perfect electrical conductor (PEC) bridge which connects two ground conductors with a lumped excitation port in the middle. Probe pads were not included in the simulations because they were de-embedded as part of the measurement process.

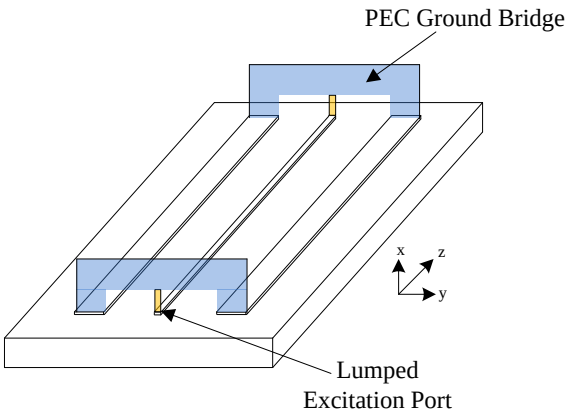


Figure 3.2. HFSS simulation setup with PEC bridge.

[6] Cadence Virtuoso from Cadence Design Systems is the software package used to construct the low level design.

The GlobalFoundries US 0.13 µm BiCMOS process is chosen for the fabrication of the prototype IC [52]. The author and University are bound by a non-disclosure agreement with GlobalFoundries US/MOSIS and therefore the details regarding the fabrication process parameters are not included in this dissertation. Material properties and layer maps of the process were used in the 3D full-wave EM simulation in order to model the passive structures.

3.5 MEASUREMENT EQUIPMENT

Wirebonds, ball grid arrays (BGAs) or flip-chip packaging interconnects do not form a controlled impedance transition; as a result, impendence mismatch commonly occurs when using them for conducting CPW measurements. The design is therefore characterised through wafer probing and is not placed into an IC package. A Cascade Microtech PM300 wafer probing station[7] was utilised in conducting all wafer measurements. The specifications for the probing station are given in Table 3.1.

Table 3.1 Cascade Microtech PM300 wafer probing station specifications.

Parameter	Specification
Coarse adjustment	300 mm x 300 mm
Fine adjustment	10 mm x 10 mm
Load strike	10 mm
Theta travel	8°

The PM300 wafer probing station is used to lower the Cascade Microtech Infinity[8] GSG contact probes as seen in Figure 3.3, contacting with the aluminium probe pads of the

[7] The PM300 probe system is suitable for tests on 300 mm wafers and substrates. https://www.cascademicrotech.com/products/probe-systems/300mm-wafer/pm300

[8] High frequency performance Infinity Probe®. https://www.cascademicrotech.com/products/probes/rf-microwave/infinity-probe/infinity-probe

prototype. The specifications for the Microtech Infinity Probes are given in Table 3.2. The probe presents a low loss connection between the die and the VNA.

Figure 3.3. GSG probe by Cascade.

Table 3.2 Cascade Infinity probe specifications.

Parameter	Specification
Frequency	70 kHz – 110 GHz
Configuration	GSG
Tip	Non-oxidising nickel alloy
Pitch	8°
Typical contact resistance	< 0. 05 Ω on Al, <0.02Ω on Au

The Anritsu ME7828A VNA is used for S-parameter measurements as shown in Figure 3.4. The specifications for the VNA are given in Table 3.3. Mm-Wave extension modules are linked to the VNA to conduct measurements from 65 GHz to 110 GHz. The Cascade Microtech calibration substrate was used for calibration of the VNA up to the probe tips. Cascade Microtech's WinCal XE, installed on a PC linked to the VNA, was used for the

calibration of the VNA and recording measurements. A description of the calibration process is detailed in Chapter 6.

Figure 3.4. Anritsu ME7828A VNA.

Table 3.3 Anritsu ME7828A VNA specifications.

Parameter	Specification
Frequency range	70 kHz – 110 GHz
Dynamic range	75 dB at 65 GHz
Measurement speed	120 ms for 201 points
Calibration stability	0.1 dB over 24 hours

3.6 MEASUREMENT SETUP

Mm-Wave probe positioners lower probe contacts onto a design under test (DUT) at both input and output ports. Square bond pads governed by the process parameter were placed on both ports of all designs in the GSG format with a pitch of 150 µm. A two tier calibration approach was used in the measurement process which is discussed further in this section.

The calibration of the VNA was achieved by means of an impedance standard substrate (ISS) by Cascade Microtech. The thru reflect line (TRL) calibration method is used.

Calibration was done from 30 GHz to 90 GHz. The measured TRL error terms from the calibration standards were thereafter programmed to the VNA by WinCal XE. On-chip TRL calibration standards were also fabricated on the same wafer. The fabricated TRL calibration standards were measured and subsequently used for de-embedding the measured wafer results which are discussed in Chapter 6.

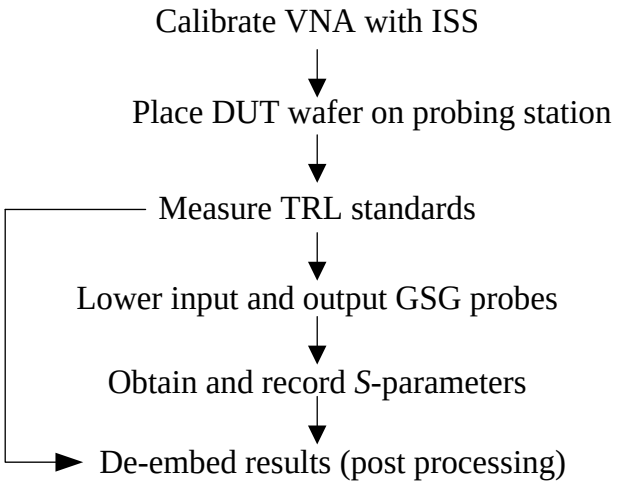


Figure 3.5. VNA measurement methodology.

Figure 3.5 shows the VNA measurement methodology used for the setup. The die was placed on a single sided adhesive material and thereafter placed on the vacuum base of the probing station's 300 mm chuck. The vacuum ensures that the adhesive material is kept in place while probing the wafer. The TRL calibration standards were measured on the wafer as indicated by step three. The GSG probes were lowered onto the DUT input and output port. Any skating of the probes needed to be taken into account when placing the GSG probe. The probe tips travel perpendicular to the probing pad. However, the angular orientation of the probe body forces the probe tip to scrape across the pad, which is known as skating. Skating is necessary to break through the aluminium oxide layer which forms on the probing pads. The S-parameters of the DUT were subsequently measured and recorded by the VNA once proper probing connections were established.

3.7 CHAPTER SUMMARY

This chapter provides an overview of the research methodology used within the project and dissertation. The chapter also describes the software used for the theoretical, EM, circuit

schematic, circuit layout and 3D EM verification of the design. The steps involved with the design, simulation and prototyping of the slow-wave delay line filters are discussed. The measurement equipment and laboratory testing procedure, as experienced, are also discussed.

CHAPTER 4 DESIGN AND SIMULATION

4.1 INTRODUCTION

The chapter commences with an analysis of the GlobalFoundries US BEOL process parameters and how CPW transmission lines can be designed to achieve the required group delay. Full-wave 3D EM simulations were used to analyse the CPW lines. Further to this, an analysis was done on three CPW structures to understand how the geometric properties of the floating metal strips influence the performance of the delay lines. The simulated S-parameters and derived group delay, propagation constant and transmission line *Q*-factor were used to compare the three structures.

A circuit model was designed as a preliminary evaluation of the filter and to understand how the delay lines influence the characteristics of the filter. The circuit model was employed to design the filter according to the design requirements which are discussed later in this chapter. The required delay line lengths were extracted from the model by combining the per-unit length delay from the EM simulation with the required delay from the circuit model. Thereafter the best suited slow-wave CPW geometry was used in the layout of the filter. The artwork generated in Cadence Virtuoso was imported back into HFSS, a full-wave 3D EM simulation tool, to verify its performance. This step is an iterative process; consequently the geometry needed to be altered several times in order to agree with the ideal circuit model.

The chapter concludes with the visual illustration of the EM fields of the slow-wave CPW, the verified 3D full-wave filter simulation results and a proposed frequency agile filter topology.

4.2 PROCESS PARAMETERS

The GlobalFoundries US 8HP [52] process was chosen for the implementation of the delay lines and CMOS filter. A free GlobalFoundries US run was provided by MOSIS as part of the MOSIS education program[9]. As discussed in Chapter 2, the BEOL process parameters govern the characteristic properties of a slow-wave CPW and consequently the delay line filter. Therefore, it was necessary to understand these process parameters prior to commencing with the geometrical designs.

The process consists of five copper (Cu) layers (M1, M2, M3, M4 and MQ) and two thick layers of aluminium (Al) (LY and AM). The seven metal layer stack (7ML) has a thicker dielectric layer stack than the 5ML process and was therefore chosen in order to allow for a larger electric field region. Although Al has a higher resistivity than Cu, as recorded in Table 4.1, the thickness of Cu in the 8HP BEOL process results in higher ohmic losses. The technology parameters and BEOL layout are summarised and shown in Figure 4.1. The relative permittivity of Si is 11.9 and the bulk average permittivity of the SiO_2 along the metal layer stack is 4.10 [52].

Table 4.1 Al vs. Cu comparison.

Metal	**Electrical resistivity at 20°C (μΩ-cm)**	**Thermal conductivity ($W.m^{-1}.K^{-1}$)**
Cu	1.7 – 2.0	401
Al	2.7 – 3.0	237

[9] MOSIS Educational Program. https://www.mosis.com/you-are/academic-institutions

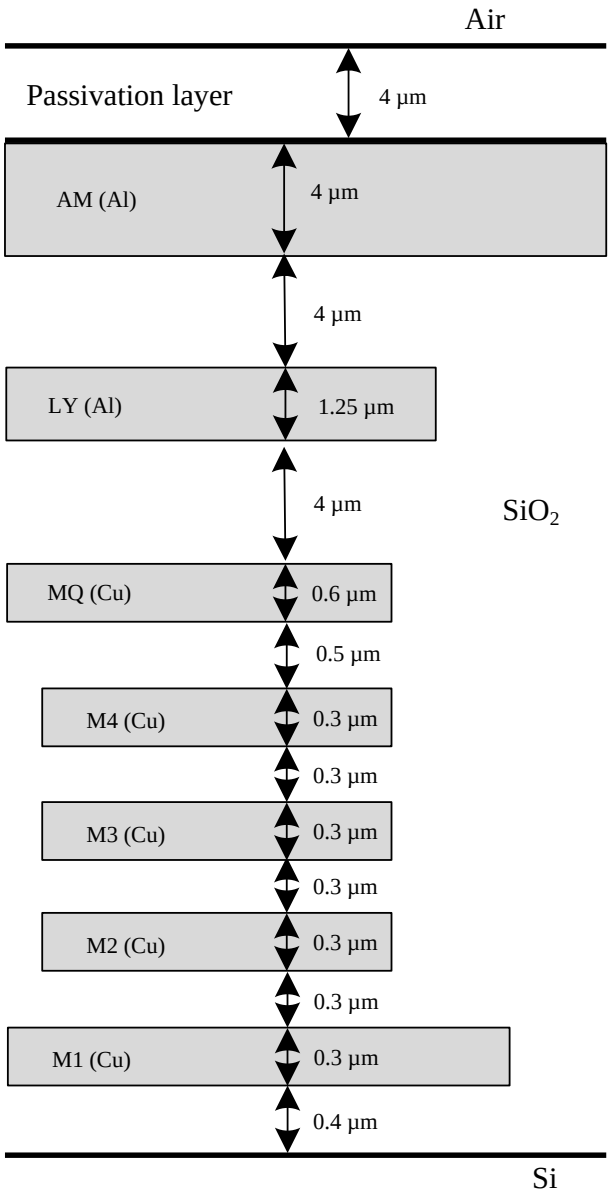


Figure 4.1. Metal parameters for the GlobalFoundries US 8HP process.

4.3 SLOW-WAVE TRANSMISSION LINE DESIGN

4.3.1 Transmission line geometry

A 50 Ω CPW line was designed using the 8HP BEOL. The BEOL was studied in order to understand how different metal layers influence the performance of a CPW at 70 GHz. This was achieved by creating simulation models of both an LY and an AM CPW transmission line. Figure 4.2 shows a CPW implemented on the top metal layer (AM) of the 8HP process. It can be seen that the transmission line is surrounded by the SiO_2

dielectric and the passivation layer. A similar model was created for a CPW implemented on the LY metal layer. The 50 Ω CPW was designed using the TX-LINE[10] synthesis calculation tool. From the tool a signal line width of 7 µm and a ground spacing of 10 µm were calculated for an Al CPW within a SiO_2 substrate.

Figure 4.2. CPW on AM layer.

CST Microwave Office was used for initial simulations; however, the simulation outcomes did not yield satisfactory results and as a result all further simulations were conducted in HFSS. An 840 µm length CPW transmission line was simulated in HFSS using the process parameters. A comparison of the AM and LY CPW is shown in Figure 4.3 and Figure 4.4. The $|S_{21}|$ of the structures is portrayed in Figure 4.3. For the chosen frequency range the insertion loss varies from 0.08 dB to 0.48 dB for the AM layer CPW and from 0.24 dB to 0.79 dB for the LY layer CPW. The AM layer CPW has an insertion loss of 0.4 dB at 70 GHz and the LY layer CPW has an insertion loss of 0.68 dB at the same frequency.

[10] TX-LINE is a free Windows-based interactive transmission line calculator for the analysis and synthesis of transmission line structures. http://www.awrcorp.com/products/additional-products/tx-line-transmission-line-calculator

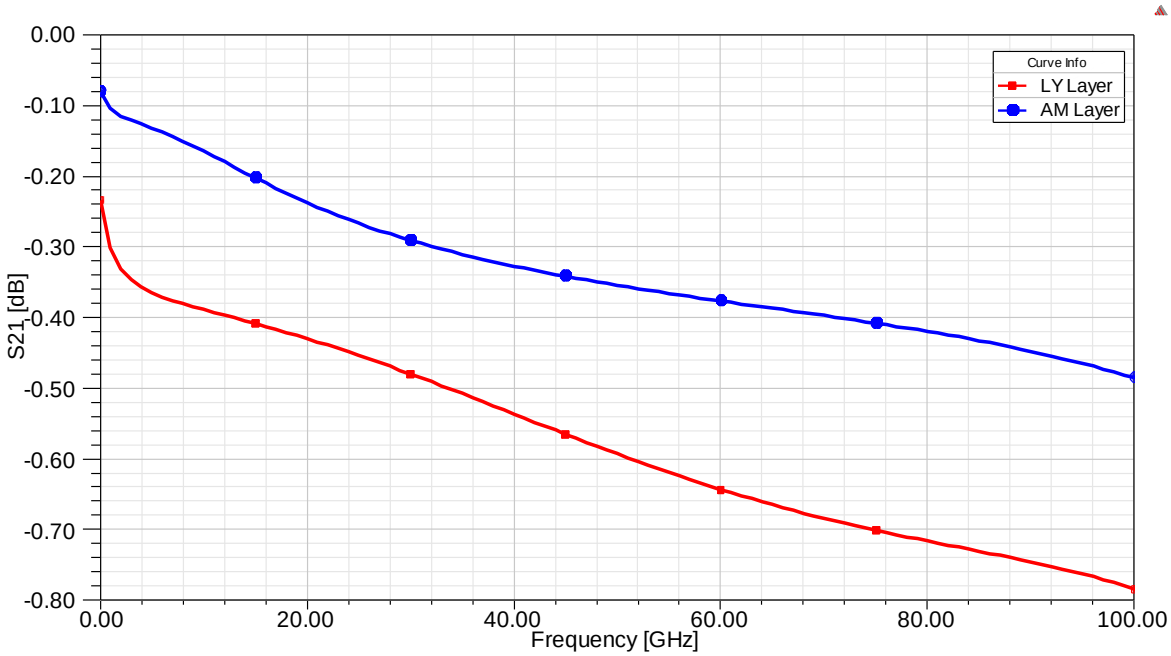


Figure 4.3. Magnitude of S_{21} of the AM and LY layer CPW.

The group delay of the two structures is shown in Figure 4.4. The group delay of the AM layer CPW recorded a 5.54 ps at 70 GHz while the LY layer CPW showed a group delay of 5.24 ps.

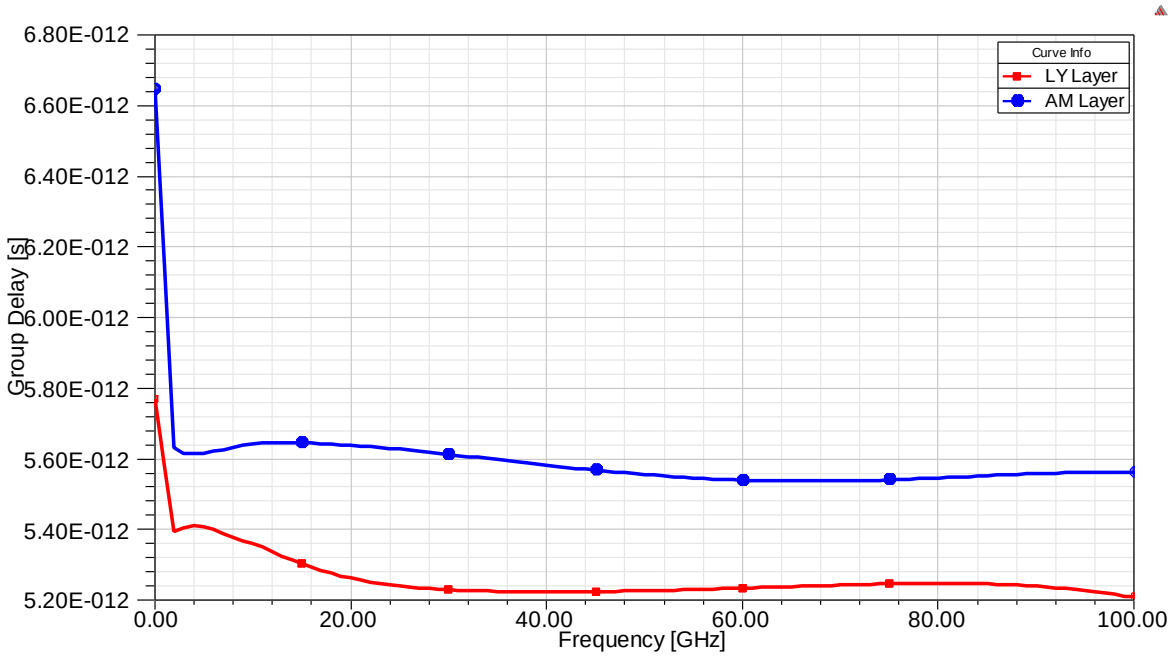


Figure 4.4. Group Delay of the AM and LY layer CPW.

Based on the above analysis it was concluded that the AM layer CPW provided more delay with lower insertion loss and was consequently a better choice than the LY layer CPW. This is due to the AM layer being further away from the substrate and hence lower

insertion loss is achieved. The AM layer CPW was therefore used for all further simulations.

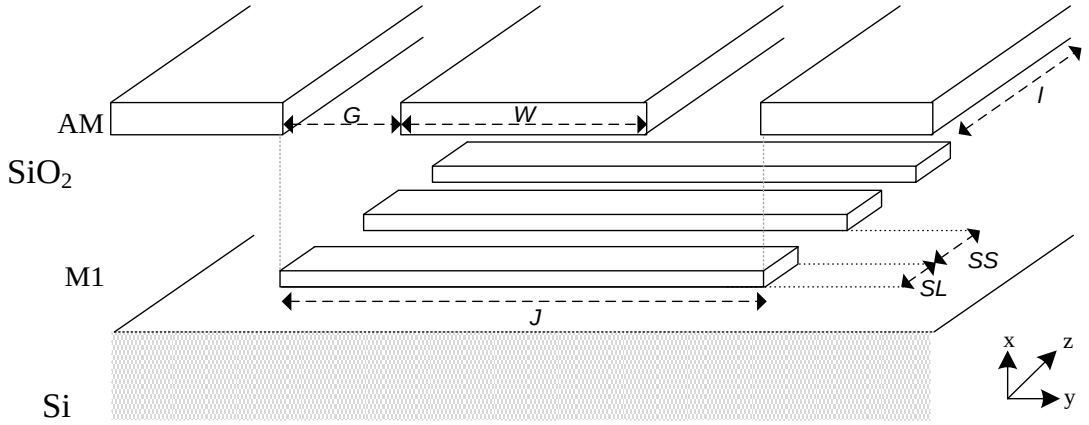


Figure 4.5. Slow-wave CPW with metal shielding.

Floating metal strips [19], [53] , as seen in Figure 4.5, are introduced below the CPW. The strip spacing (*SS*) varies from 1.6 µm to 6 µm, and is introduced to create the slow-wave effect and also to reduce attenuation loss and the effects of eddy currents at mm-wave frequencies. A wide strip spacing (*SS* = 6 µm) causes increased insertion loss because the electric field leaks into the Si substrate. By placing the floating metal strips closer together (*SS* < 2.5 µm), it is possible to reduce the electric field leakage and to create the slow-wave transmission line.

The following mathematical approach [26] was utilised to model the shield behaviour. The floating metal shield strip density (*R*) is expressed as

$$R = \frac{SL}{SL + SS}. \tag{4.1}$$

The propagation constant and attenuation of the structure can be varied by means of varying the widths of *SL* and *SS* while still maintaining the ratio (*R*) of shield strip density and spacing [26]. The unit section of *SL* and *SS* is modelled as a series inductance of $L(R\Delta z)$ and a shunt capacitance of $(nC)(R\Delta z)$ where *n* is the multiplication capacitance factor realised as a result of mutual coupling between the floating metal strip structures and CPW transmission line [26]. Consequently, the phase velocity of the slow-wave transmission line can be expressed as

$$V_p = \frac{c_o}{\sqrt{\varepsilon_r \mu_r}} = \frac{1}{\sqrt{LC(nR)}}. \tag{4.2}$$

The group delay (*GD*) of a length (*l*) transmission line can therefore be expressed as

$$GD = l\sqrt{LC(nR)}. \tag{4.3}$$

It can therefore be shown from (4.2) and (4.3) that the group delay can be increased by increasing *R* and subsequently increasing *n*. The increased capacitance between the transmission line and floating metal strips results in a larger group delay.

The 50 Ω slow-wave CPW was designed according to the above approach. The CPW was placed on the AM metal layer as explained in the above section. The AM layer is more than three times thicker than the LY layer and therefore has lower ohmic series resistance. The upper metal layer is also least affected by substrate losses, due to it being the furthest metal layer from the substrate. It also provides more routing flexibility since the lower metallisation layer may now be used to connect the various sub-circuit elements without having to introduce discontinuities in the shielding. The floating copper strips were placed on layer M1 to create the largest separation distance from the CPW. Extending the shields underneath the ground planes of the CPW would result in unshielded areas at the 90° degree bends of the delay line network in the filter topology. For this reason the shields were not extended underneath the ground planes of the CPW, sacrificing additional capacitance and the enhanced slow-wave effect. Table 4.2 summarises the geometry of the CPW.

Table 4.2 Geometric parameters of CPW.

Parameter	**Dimension (µm)**		
Signal width (*W*)	7		
Signal to ground spacing (*G*)	10		
Transmission line length (*l*)	840		
	No strips	Narrow	Wide
Strip spacing (*SS*)	NA	2	5
Strip length (*SL*)	NA	1.6	4.8

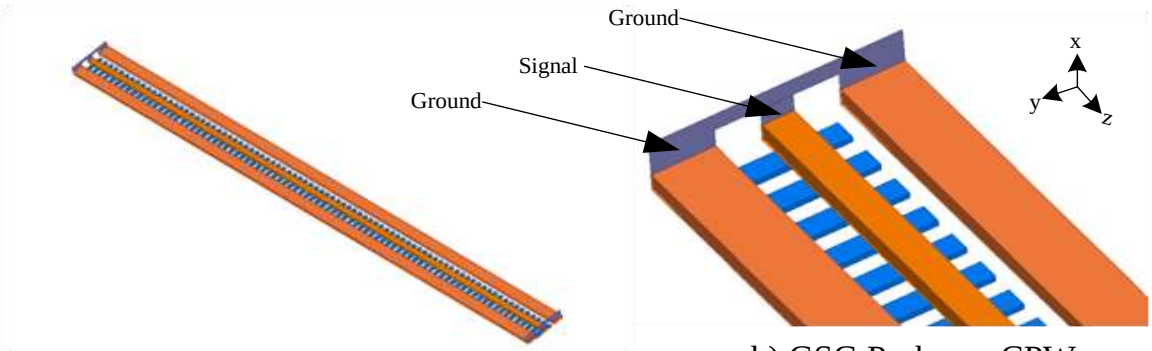
4.3.2 Parametric study of slow-wave CPW

Three transmission lines were simulated to study the effects of the delay line geometry. For the purpose of this dissertation the naming convention below is used to describe the three transmission lines. The naming convention is consistent throughout this dissertation and links back to the diagram shown in Figure 4.5.

a) (No Strip) A CPW transmission line with no shielding mechanism
b) (Narrow Strip Spacing) A slow-wave shielded CPW transmission line containing floating metal strips with dimensions *SS* = 2 µm and *SL* = 1.6 µm
c) (Wide Strip Spacing) A slow-wave shielded CPW transmission line containing floating metal strips with dimensions *SS* = 5 µm and *SL* = 4.8 µm.

SS and *SL* were chosen in order to maintain *R*, but still allows one to analyse the delay response of the various *SS* and *SL* geometric parameters. The geometric parameters for the slow-wave CPW structures are summarised in Table 4.2.

An analysis of the insertion loss and group delay was conducted to find the best performing delay line at 70 GHz. The selected geometries were implemented in the slow-wave delay lines. Figure 4.6 shows the narrow strip spacing slow-wave delay lines as explained above. The PEC bridge GSG probe discussed in section 3.4.2 has been used for all CPW simulations.



a) Narrow Strip Spacing CPW b) GSG Probe on CPW

Figure 4.6. Simulated CPW artwork.

Figure 4.7 shows the simulated $|S_{21}|$ for the three CPW structures. The results indicate that the no strip CPW shows the least insertion loss throughout the frequency band. At 70 GHz

the no strip CPW exhibits an insertion loss of 0.4 dB. The wide and narrow strip spacing CPWs demonstrate an insertion loss of 0.51 dB and 0.58 dB, respectively.

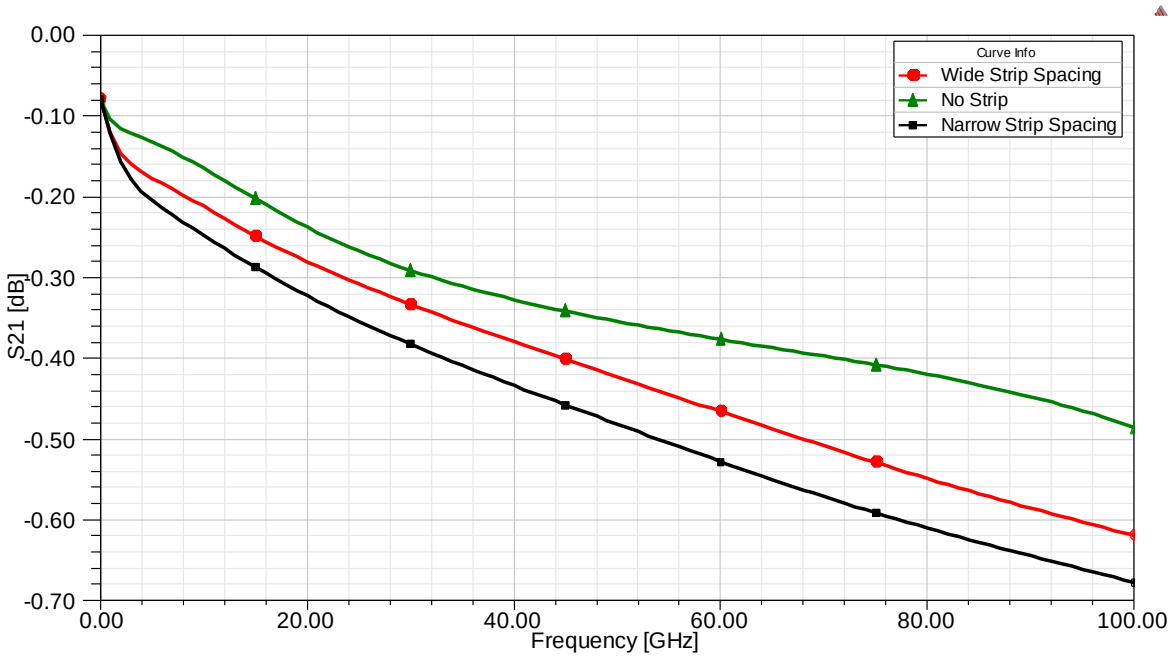


Figure 4.7. Simulated S_{21} magnitude response of the CPW structures.

The simulated group delays of the various structures are shown in Figure 4.8. The group delay is used to determine which structure features the most delay for the given length in the 70 GHz band. As expected, the shielded slow-wave CPWs demonstrated a greater group delay from 0 GHz to 100 GHz. At 70 GHz the no strip, wide and narrow strip spacing CPWs demonstrate a group delay of 5.24 ps, 5.51 ps and 5.60 ps respectively. The narrow strip spacing CPW has a 0.36 ps improvement in group delay compared to the other two CPWs. The narrow strip spacing CPW group delay of 5.60 ps at 70 GHz is considered satisfactory to be used within a mm-wave delay line. All three transmission lines maintain a group delay of 0.21 ps or better, which relates to within 3.88 % from 10 GHz to 100 GHz.

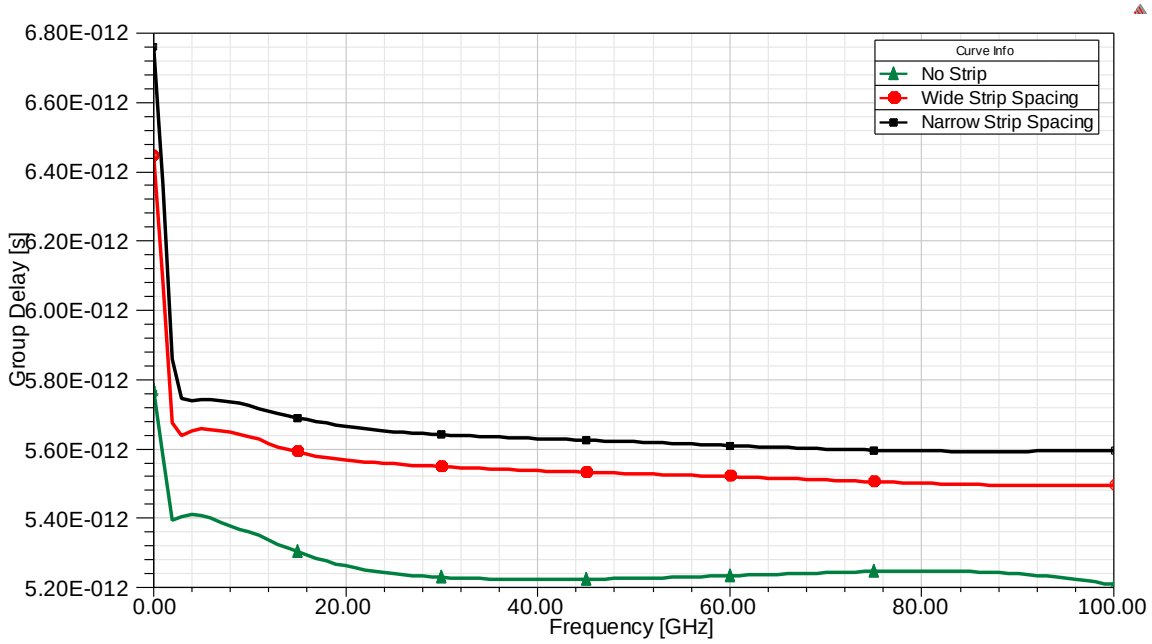


Figure 4.8. Simulated group delay of the CPW structures.

Figure 4.9 shows that the simulated characteristic impedances of the three CPWs structures change with the introduction of the floating metal strips. At 70 GHz, the no strip, wide and narrow strip spacing CPWs demonstrate an impedance of 52.52 Ω, 47.64 Ω and 47.02 Ω respectively. The introduction of the floating metal strips increases the loading capacitance between the strips and the CPW conductor which therefore decreases the characteristic impedance. All three transmission lines maintain a 50 Ω impedance to within 17.1 % from 1 GHz to 100 GHz.

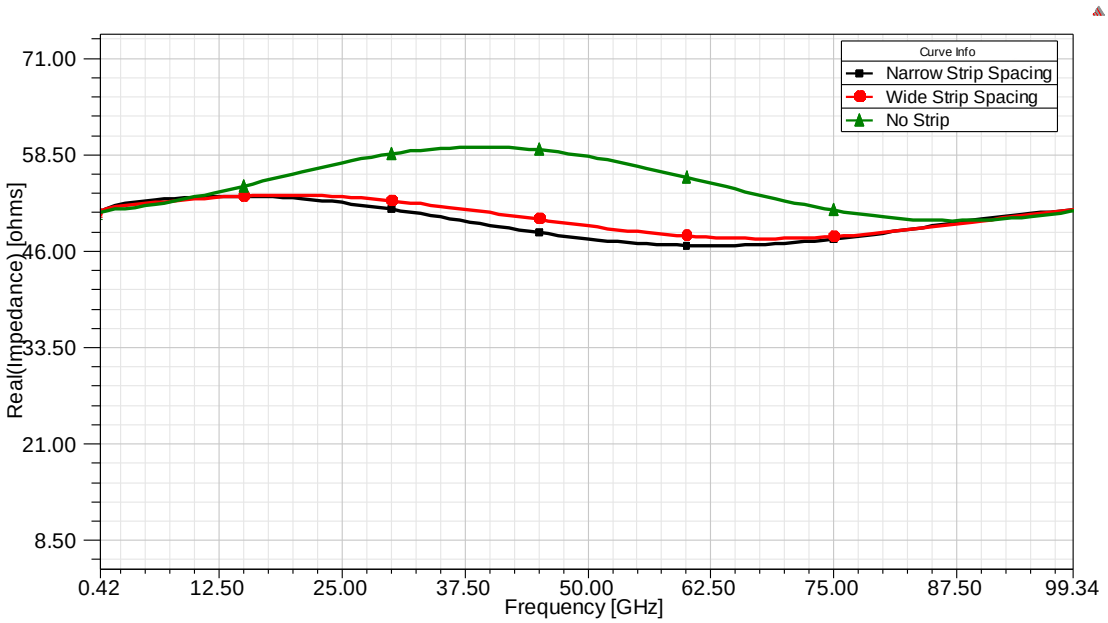


Figure 4.9. Simulated characteristic impedance of the CPW structures.

The attenuation constant (α) and phase constant (β) are simulated to find the transmission line *Q*-factor for the three simulated CPWs. The respective graphs are shown in Figure 4.10 and Figure 4.11. The attenuation constant increases with frequency. At 70 GHz the no strip, wide and narrow strip spacing CPWs demonstrate a loss of 0.52 dB/mm, 0.68 dB/mm and 0.75 dB/mm respectively. The narrow strip spacing slow-wave CPW achieves the highest attenuation constant which corresponds to the highest insertion loss of the three structures as highlighted by Figure 4.7.

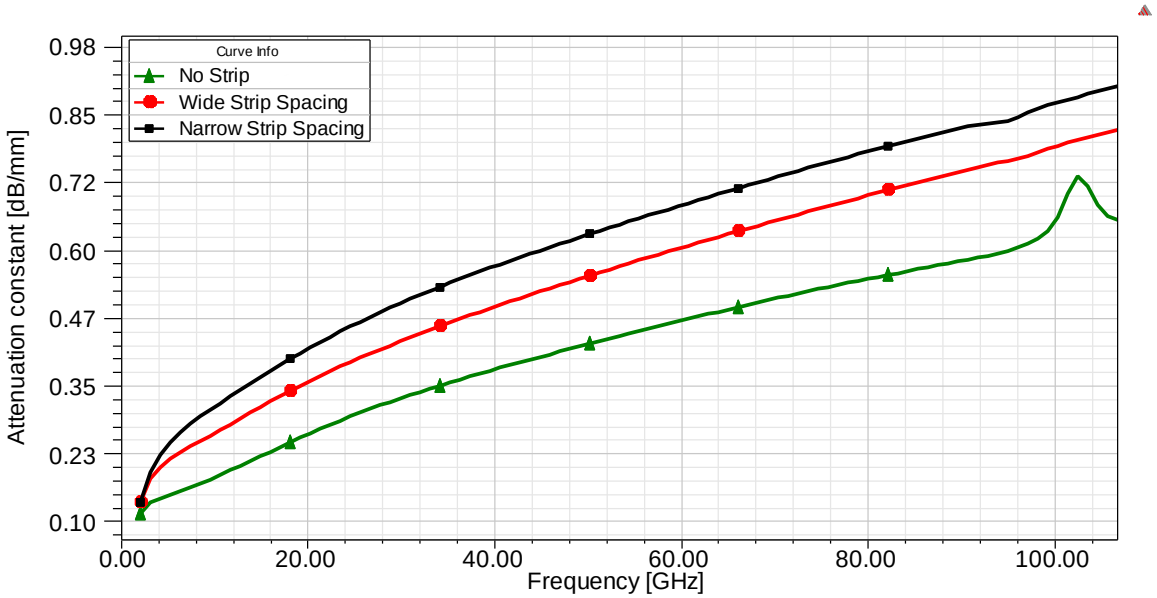


Figure 4.10. Simulated attenuation constant of the CPW structures.

The phase constant of the three structures is highly linear as shown by Figure 4.11. An increase of 0.5 rad/mm is noticeable by the introduction of the floating metal shield structures. At 70 GHz the no strip, wide and narrow strip spacing CPWs demonstrate a phase constant of 7.25 rad/mm, 7.66 rad/mm and 7.81 rad/mm respectively. The narrow strip spacing CPW achieves the highest phase constant of the three structures.

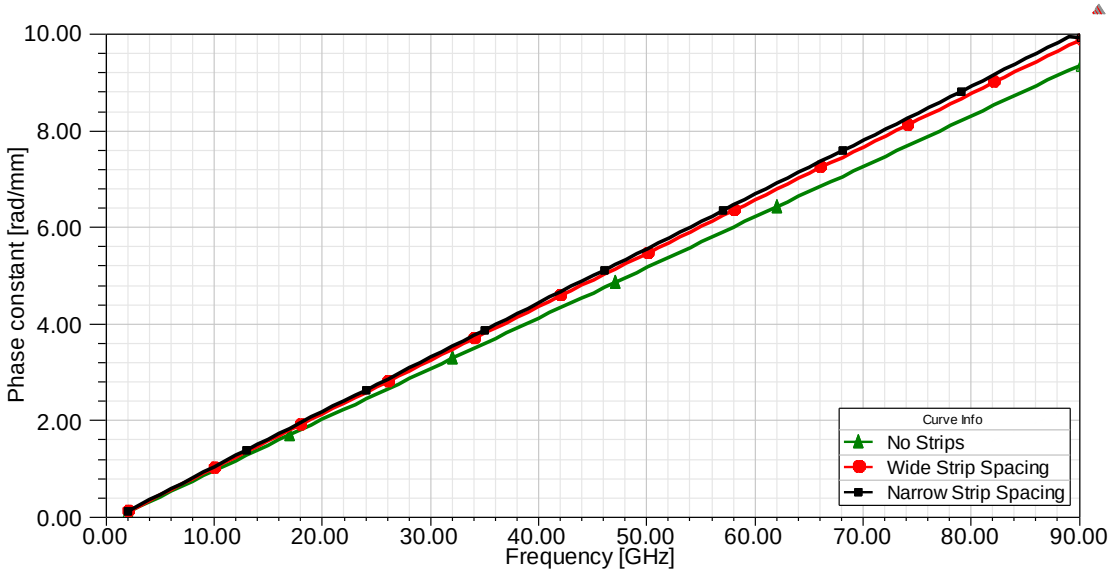


Figure 4.11. Simulated phase constant of the CPW structures.

The *Q*-factor is calculated using the relationship given by

$$Q = \frac{\beta}{2\alpha}, \tag{4.4}$$

where the attenuation constant in dB/mm is converted Np/mm and β is in rad/mm. The *Q*-factor of the three CPWs is shown in Figure 4.12. It is evident that the narrow strip spacing CPW achieves the highest *Q*-factor of 38.3. The narrow strip spacing CPW *Q*-factor is attributed to the highest phase constant of the three structures. At 70 GHz the no strip, wide and narrow strip spacing CPWs demonstrate *Q*-factors of 24.9, 33.64 and 38.30 respectively.

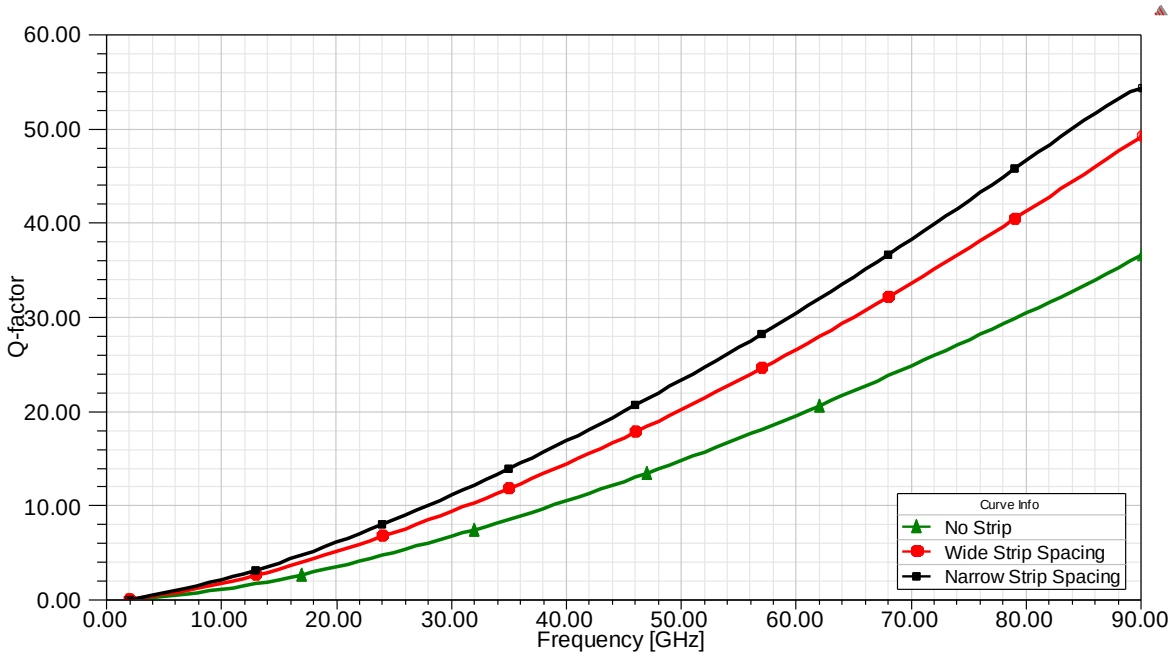


Figure 4.12. Simulated *Q*-factor of the CPW structures.

It is interesting to note that the narrow strip spacing CPW showed the highest insertion loss, but also the greatest group delay. The *Q*-factor of the narrow strip spacing CPW is also the highest. It is important to identify the purpose of the transmission line before deciding on geometry. It is evident that the line with the most per-unit length delay does not necessarily mean that it has the least insertion loss for a given required phase delay.

Taking the above into consideration, the narrow strip spacing CPW has the best group delay and *Q*-factor compared to the other two structures. Based on the above findings it is concluded that the narrow strip spacing slow-wave CPW was better suited for implementation within the filter topology.

4.3.3 Electric field distribution

The electric field distribution is observed to study the field distribution on the substrate, CPW and floating metal strips. Figure 4.13 shows the geometrical layout of the narrow strip spacing slow-wave CPW which is simulated at 70 GHz. A section at X = 35 µm is chosen to visualise the effects of the floating metal strips. The figure shows the electric field distribution between the CPW and floating metal strips caused by the GSG excitation of the CPW. Regions of yellow and green indicate a strong electric field whereas areas of

blue indicate a weak electric field. The simulation model also incorporates the passivation layer.

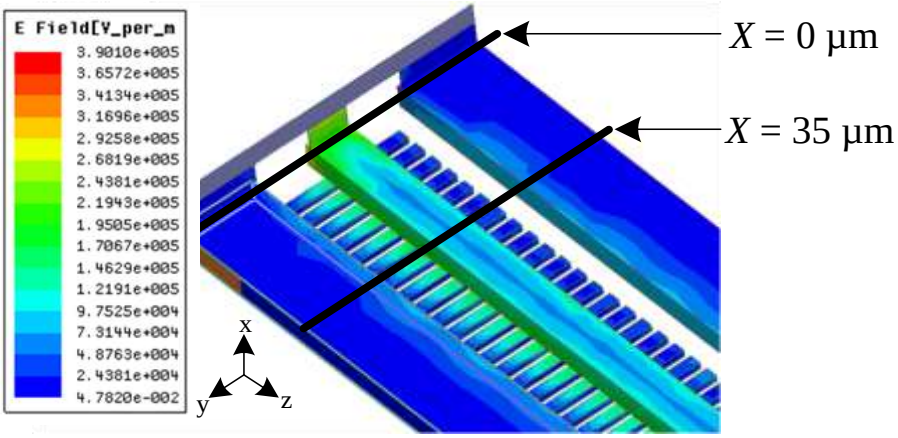


Figure 4.13. Electric field distribution at X = 35 µm of narrow strip spacing slow-wave CPW.

Figure 4.14 shows a cross-section view of the electric field distribution. The introduction of the floating metal strips effects the electric field concentration between the CPW and floating strips. The floating metal strips assist in reducing coupling between the substrate and signal conductor. From the figure it is evident that the floating metal strips limit the electric field penetrating into the substrate. In [54] is it shown that mutual coupling exists between the floating metal strips and the ground conductors when the floating metal strips are extended under the ground lines on either side. In an ideal situation, the floating metal strips would be extended under the CPW ground planes. As stated previously, the floating metal strips are not extended underneath the ground lines of the CPW in this study, to permit greater signal routing flexibility.

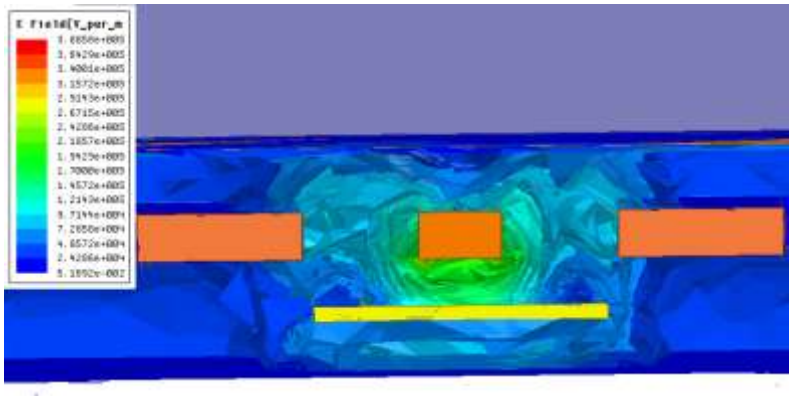


Figure 4.14. Electric field distribution of narrow strip spacing slow-wave CPW.

4.4 SLOW-WAVE FILTER DESIGN

The delay line filter is initially designed using a circuit model as detailed by the methodology shown in Figure 3.1 (Chapter 3). The E-band was identified as the band of interest based on the research questions and literature survey conducted in Chapters 1 and 2 respectively. The filter is aimed at full-band applications and therefore it was designed for a 15 % or 10.5 GHz bandwidth. The bandwidth of the filter is defined as the frequency difference between the two -3 dB transmission points either side of the centre frequency. The passband attenuation of the filter is aimed to be below 5 dB as compared to recent research [31]. It is necessary to obtain an out of band suppression of greater than 10 dB to suppress other mm-wave sources [31]. Table 4.3 details the filter design requirements.

Table 4.3 Filter design requirements.

Parameter	Requirement
Centre frequency (f_c)	70 GHz
Bandwidth percentage	15 %
Bandwidth in GHz	10.5 GHz
Gain	0 dB
Passband attenuation	< 5 dB
Out of band suppression	>10 dB

4.4.1 Circuit design

A synthesis of the delay line filter was performed in AWR Microwave Office to establish the required delay line lengths of the filter. Figure 4.15 shows the schematic of the circuit model implemented in AWR Microwave Office. A variable was created for θ_1 and θ_2 which allowed for the values to be varied. These were varied in order to investigate how the phase delay of the transmission lines influences the parameters of the filter. The link line is defined as the connection line with a phase delay θ_{ll}.

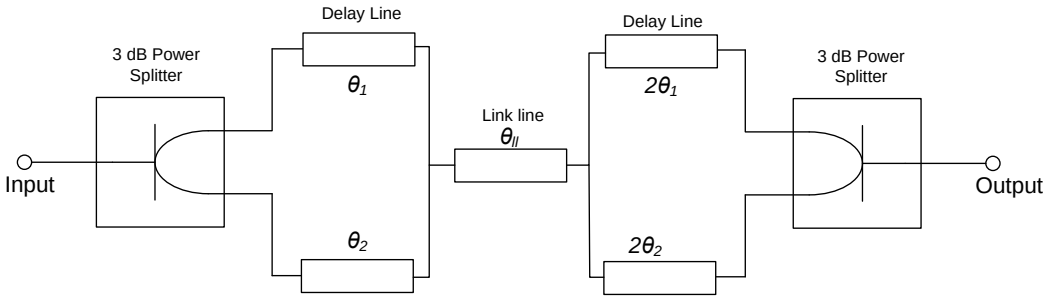


Figure 4.15. Delay line filter model.

From [15] the delay line filter is expressed as

$$\left|S_{21}(\omega)\right|^2 = \cos(\theta_{ll})\cos^2\left(\frac{\theta}{2}\right)\cos^2(\theta) \tag{4.5}$$

where

$$\theta = \theta_2 - \theta_1.$$

The parametric analysis of (4.5) for a varied θ_1 and θ_2 is shown in Figure 4.16. It can be seen that by varying the phase delay of θ_1 and θ_2 the centre frequency and bandwidth of the filter can be selected. Choosing smaller values of θ_1 results in a smaller bandwidth as demonstrated by the 60 GHz, 44 GHz and 45 GHz filter. This confirms that the parameters of the filter can be designed by selecting the delay line lengths of θ_1 and θ_2 as described in [10]. θ_{ll} is not taken into account in the Figure 4.16, as it is assumed to be much shorter than θ_1 and θ_2.

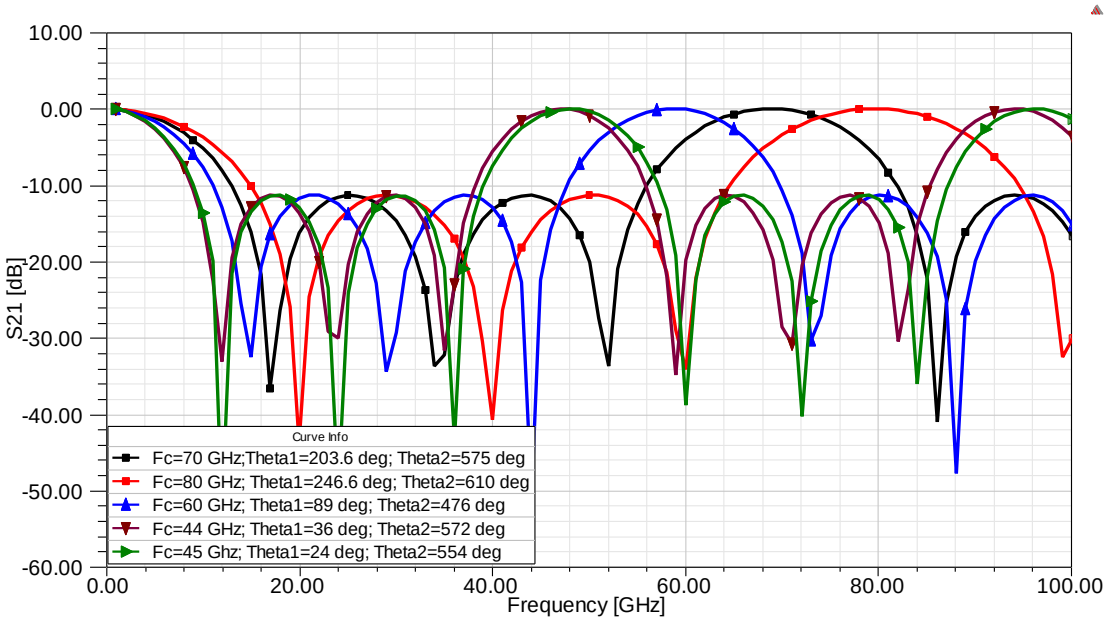


Figure 4.16. Parametric analysis of delay line length on ideal filter.

θ_{ll} is incorporated into the circuit model for all further measurements as represented by Figure 4.17 to account for the finite length of the link line between the two delay line networks. For a θ_1 phase delay of 30.5°, a θ_2 phase delay of 720.2° and a θ_{ll} of 6.2°, a filter with a centre frequency of 69.8 GHz and a bandwidth of 15.75 % or 11.03 GHz is achieved. An out of band suppression of 10.85 dB is achieved. The ideal circuit simulation shown in Figure 4.17, compares well with the design requirements of a 70 GHz centre frequency, 15 % bandwidth filter and an out of band suppression of more than 10 dB.

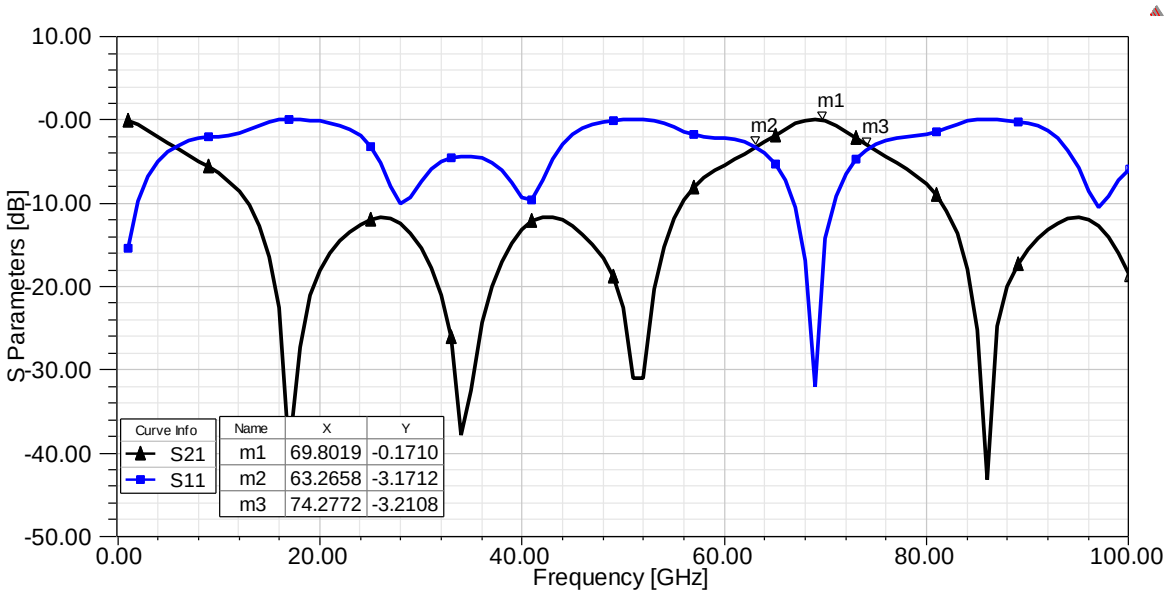


Figure 4.17. Simulated S_{21} and S_{11} magnitude response of the ideal filter.

4.4.2 Power divider

Limitations such as poor isolation and impedance mismatch need to be considered on the CMOS substrate. To model these effects, GlobalFoundries US have supplied designers with process specific RF power divider design and associated scalable models for simulation and layout. The power dividers provide a high degree of isolation between the two outputs such that a short to one of the outputs would have little effect on the other output and would only cause a 3:1 or worse voltage standing wave ratio (VSWR) mismatch [55].

The process uses a Wilkinson power divider to achieve equal power division and isolation between the output ports. The structure consists of two uncoupled λ/4 CPW transmission lines which are fed in parallel. The two inputs are kept as far apart as possible to prevent coupling. The input and output impedances have equal line impedances of $\sqrt{2}\,Z_0$ as shown in Figure 4.18 and are accompanied by a shunt load of $2Z_0$ for simultaneous port match and isolation.

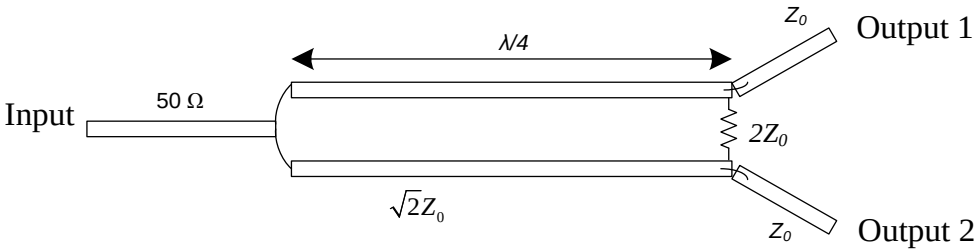


Figure 4.18. Wilkinson power divider.

The four metal stack *Powerdivx1* model [52] refers to a set of parameterised three-port, symmetric and reciprocal models for the Wilkinson power divider provided by the 8HP process design kit. The structure can be designed to have scalable characteristic impedances [52]. The model is valid from DC up to 120 GHz. The *Powerdivx1* model supports the five metal stack configurations with the signal path being on the AM metal level. The lower metal layers of the structure are used for return paths which depend on the metal stack. Metal layers M2, M3, M4 or MQ are used for these return paths. The model also supports a metal width from 4 μm to 50 μm. It also has side shields from 4 μm to 20 μm to assist with signal isolation.

The sub-circuit model is a hierarchal model which calls on the process reserved “T”, KQ metal resistor, bend, single wire and meanderline models. The meander shape of the *Pcell* layout is chosen to reduce the overall substrate area of the design without appreciable signal degradation [55]. The three port model is scalable and the characteristic impedance is set to 50 Ω. To validate the performance of the model, Figure 4.19 shows the simulated S-parameters of the *Powerdivx1* model. The model is simulated in a full-wave solver. The resistor is modelled as a Tantalum Nitride material in HFSS. The divider achieves an insertion loss of 0.90 dB at 70 GHz. The simulated isolation for $|S_{32}|$ and $|S_{23}|$ is -6.80 dB at 70 GHz. $|S_{11}|$ is found to be -10.64 dB at 70 GHz. The input impedance match and low insertion loss was found suitable for filter implementation, whilst the low isolation was inconsequential to pass-band operation, as ports 2 and 3 are excited symmetrically at this frequency.

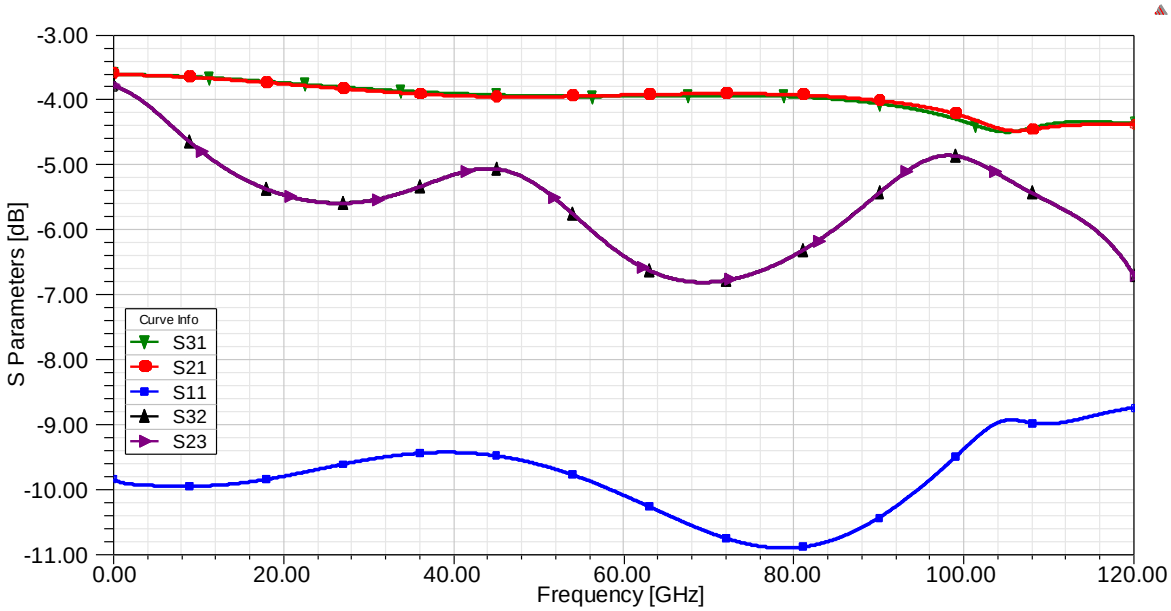
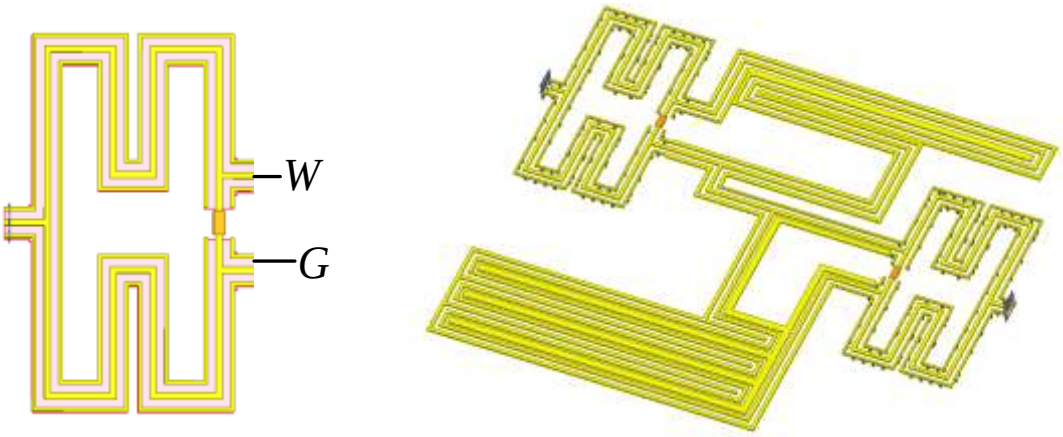


Figure 4.19. Simulated $S_{21,}$ S_{31} and S_{11} magnitude response of the *Powerdivx1* Wilkinson divider.

4.4.3 Filter design

In order to integrate the *Powerdivx1* model [52] into the delay line filter, the output width of the power divider ($w_{splitter}$) is matched in width to that of the delay line network in HFSS as shown in Figure 4.20. The *Powerdivx1* model was designed with a signal width (W) of 7 um and a signal to ground spacing (G) of 10 um.



Powerdix1 model Integration into filter

Figure 4.20. Artwork of filter.

Section 4.4.1 indicated that a phase delay (θ) of 30.5° is required for θ_1 and 720.2° is required for θ_2. In section 4.3.2 it was concluded that the narrow strip spacing CPW achieves the greatest group delay and was therefore best suited for use in the slow-wave delay line filter. The narrow strip spacing CPW has a *SS* = 2 µm and *SL* = 1.6 µm. The line length for θ_1 and θ_2 are calculated using

$$l = \frac{\theta \times \lambda}{360}, \tag{4.6}$$

where the wavelength of the simulated narrow strip spacing CPW is used. Table 4.4 indicates the delay line length required for θ_1 and θ_2 in order to achieve a centre frequency of 70 GHz and a 15 % bandwidth as determined by the circuit model detailed in Section 4.4.1. In addition to using the above equation, each delay line length was simulated in HFSS to confirm that the narrow strip spacing CPW length achieved the required phase delay.

Table 4.4 Delay line length.

Parameter	**Line Length (*l*) (µm)**
θ_1	114.50
θ_2	2705.00

These delay line lengths were refined, based on an iterative process between the artwork layout in Cadence Virtuoso and the 3D full-wave EM simulations in HFSS. In order to reduce chip area, a meander delay line was implemented. The meander structure is detailed in Section 5.2.1. The complete filter artwork design was thereafter imported from Cadence Virtuoso into HFSS to verify its performance prior to fabrication. Figure 4.21 shows the HFSS artwork which was created in Cadence Virtuoso. A link line of length 26.8 µm for θ_{ll} = 6.2° was constructed. A zero link line cannot be created in the artwork and hence it was incorporated into the circuit model to accurately predict the behaviour of the circuit.

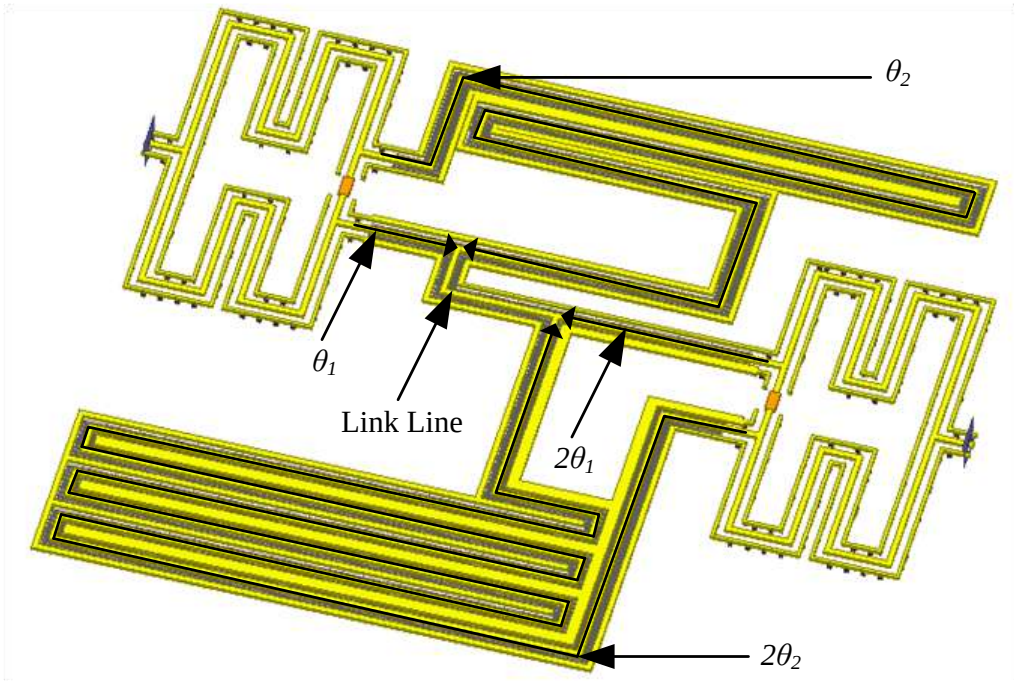


Figure 4.21. Simulation model of passive delay line filter.

The S-parameters of the full-wave, final simulated slow-wave delay line filter artwork are shown in Figure 4.22. The simulation is performed from DC to 120 GHz. It can be observed that the filter has a centre frequency of 70.2 GHz and a bandwidth of 14.21 GHz as marked by marker M2 and M3 which corresponds to a 20.24 % bandwidth. An insertion loss of 4.21 dB is noted at the centre frequency. $|S_{11}|$ indicates a return loss of 15 dB from 69.03 GHz to 71.91 GHz. The insertion loss of 4.21 dB can be attributed to unmodelled material properties such as surface roughness and heat dissipation mechanisms. The simulation accuracy is limited by the medium size mesh that is chosen for simulations to allow for a manageable mesh size and reduces simulation time. The floating metal strips

drastically increase the size of the mesh and therefore a coarse mesh has to be used. A finer meshed structure would result in a more accurate response.

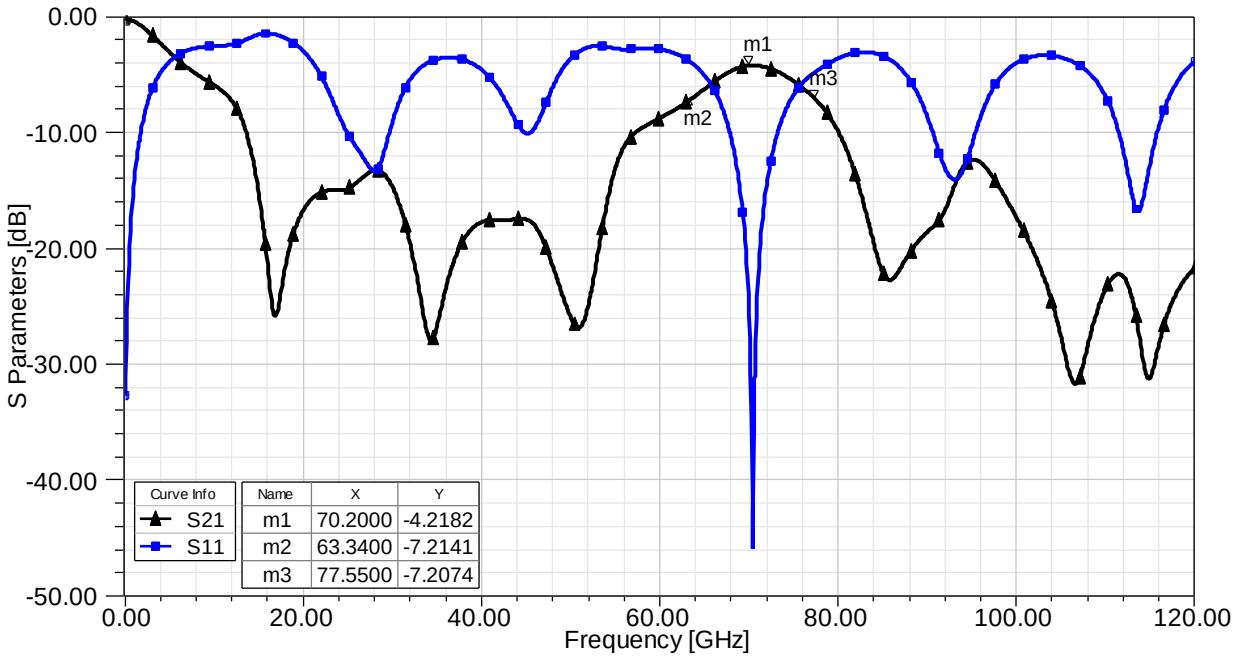


Figure 4.22. Simulated S_{21} and S_{11} magnitude response of the artwork filter.

A comparison between the ideal circuit filter and simulated artwork filter is shown in Figure 4.23. The $|S_{21}|$ graphs of the two waveforms show good agreement. The centre frequencies of the ideal and simulated filters are measured to be 69.8 GHz and 70.2 GHz respectively. The $|S_{11}|$ graphs show good agreement as well. The centre frequency of the ideal and simulated artwork filters varies by 0.4 GHz. The bandwidth of the ideal and simulated artwork filter is measured to be 15.8 % and 20.24 %. The Q-factor of the filter is expressed as

$$Q = \frac{f_c}{BW}, \tag{4.7}$$

where f_c is the filter centre frequency and BW is the bandwidth of the filter. Table 4.5 summarises the Q–factor of the ideal filter and simulated artwork filter.

The $|S_{21}|$ intercepts the $|S_{11}|$ at 34 GHz and 92.5 GHz. At these points there is an equal amount of transmitted and reflected energy. The dielectric is however modelled with the referenced material properties in HFSS and therefore resistive losses are taken into account in the simulation results which can be a cause of the two intercept point.

Table 4.5 Comparison of ideal and simulated artwork filter.

Filter	f_c (GHz)	*BW* (GHz)	*BW* (%)	*Q*-factor	Insertion loss (dB)
Ideal Filter	69.8	11.03	15.8	6.32	0.22
Simulated Artwork Filter	70.2	14.21	20.24	4.94	4.21

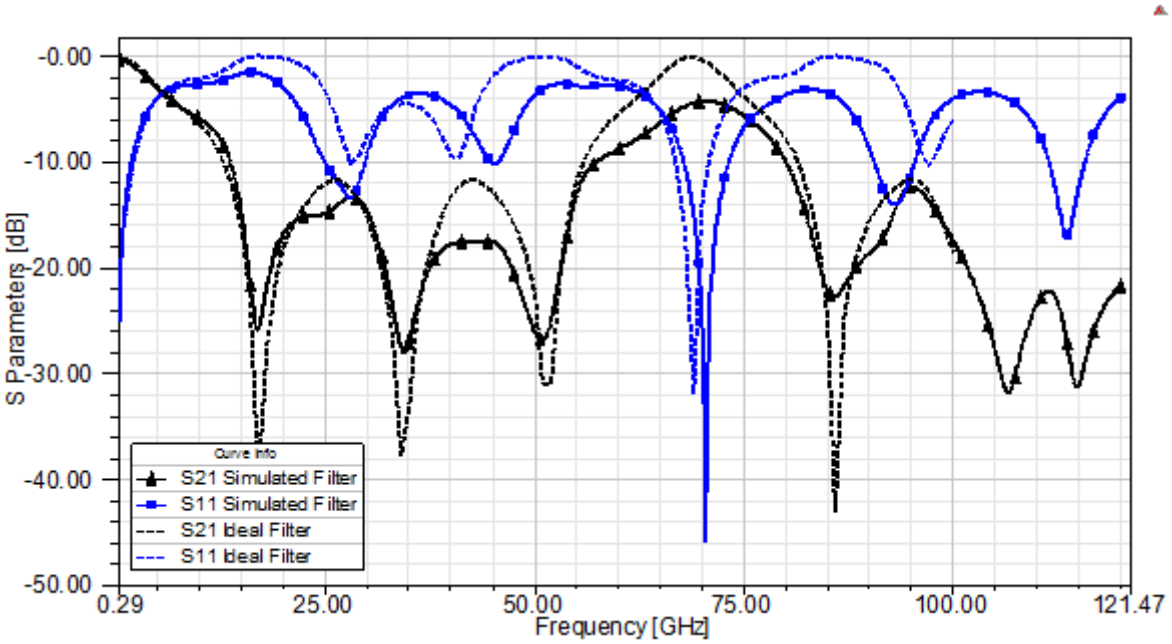


Figure 4.23. Simulated S_{21} and S_{11} magnitude response of the ideal and artwork filter.

4.5 SWITCHED DELAY LINE FILTER

A frequency agile SDL filter is achievable by introducing multiple tapping points and in-line switching elements as shown by Figure 4.24, thereby moving the short-circuit connection points between the two delay lines. A variation of 30 ° could result in an 8.5 GHz variation in centre frequency.

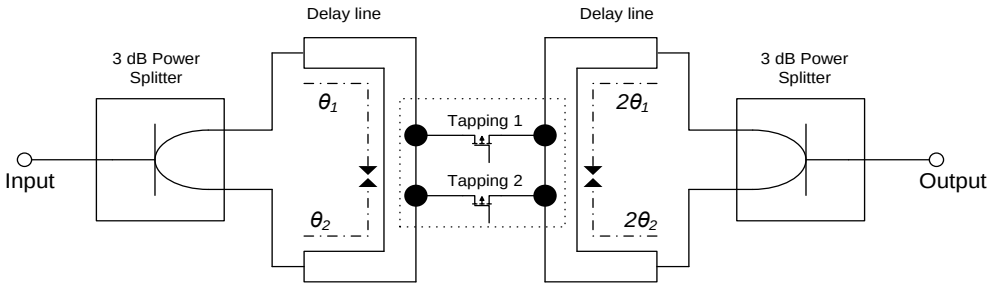


Figure 4.24. SDL filter.

The SDL topology uses two tapping points on the delay line network. By selecting between two points, the effective values of θ_1 and θ_2 are varied. CMOS NFETs serve as a cost effective and reliable method to design the switch. Each of the transistors is connected to a point on the CPW delay line network. The GlobalFoundries US process has supplied designers with process specific RF FET transistors which can operate up to 120 GHz [55]. The RF FET model supports have a minimum channel length of 0.12 µm which supports an operating voltage between 1.2 V and 1.5 V [55]. In principle, the RF FET can be implemented as a switch as detailed by this process; however, designing an RF switch at these mm-wave frequencies is complex and does not form part of the scope of work detailed in this dissertation.

4.6 CONCLUSION

The simulations and modelling in the above section are based on the GlobalFoundries US process. It was found that a CPW implemented on the AM layer demonstrated a greater group delay than one implemented on the LY layer. All CPWs were therefore implemented on the AM layer. Floating metal copper strips were placed on the bottom metal layer in accordance with the process guidelines and rules to achieve the slow-wave mechanisms. A no-strip CPW, narrow strip spacing CPW and wide strip spacing CPW were studied. The narrow strip spacing CPW demonstrated the highest insertion loss, but also the greatest group delay. The *Q*-factor of the narrow strip spacing CPW was also the highest. Based on the above findings, it is concluded that the narrow strip spacing slow-wave CPW is better suited for implementation within the filter topology.

A 70 GHz delay line filter based on a delay line topology [10] was designed. An ideal circuit model was simulated to investigate how the delay line lengths influenced the

characteristics of the filter. It was found that the centre frequency and bandwidth can be selected by choosing the appropriate values of θ_1 and θ_2 in the ideal circuit model. A representative geometry of the delay line filter model was then drawn in Cadence Virtuoso, for the chosen θ_1 and θ_2 values, and imported into HFSS for full-wave 3D EM simulations. The ideal model and 3D full-wave simulations showed good agreement. The ideal filter model had a centre frequency of 69.8 GHz, bandwidth of 11.03 GHz, percentage bandwidth of 15.8 % and a *Q*-factor of 6.32. The simulated artwork model had a centre frequency of 70.2 GHz, bandwidth of 14.21 GHz, percentage bandwidth of 20.24 % and a *Q*-factor of 4.94. The simulated artwork filter compares well with the ideal circuit model filter. Chapter 5 discussed the layout of the manufactured IC.

CHAPTER 5 LAYOUT

5.1 INTRODUCTION

This chapter discusses the layout of the powers dividers, slow-wave CPW delay lines and delay line filter in the selected microelectronic process. On-chip probe pads were placed on the fabricated die for measurement purposes. An analysis of these probe pads is also presented. The fabricated IC was not wire bonded in a package or placed on a PCB to avoid losses and parasitic inductances.

5.2 CHIP FLOORPLAN

The design is fabricated in the 0.13 µm 8HP BiCMOS process from GlobalFoundries US. The layout and fabrication of the IC formed part of the academic prototyping run sponsored by the MOSIS Educational Programme and is shown in Figure 5.1 and Figure 5.2. Three devices: the on-chip slow-wave delay lines, a passive delay line filter and an SDL filter were fabricated on the die. An SDL filter was fabricated to investigate the performance of the RF FETs as switching elements. The results of the SDL filter do not form part of this dissertation as there was an error in the biasing layout of the switching transistors. Cognisance of the pad placement, layout and pitch had to be taken to ensure that on-chip measurement could be conducted using the available GSG probes. Calibration standards are prototyped on the same die. The standards included a short thru and line (STL) standard manufactured on the AM layer. These calibration standards are used when de-embedding the measurement results as discussed in Chapter 6.

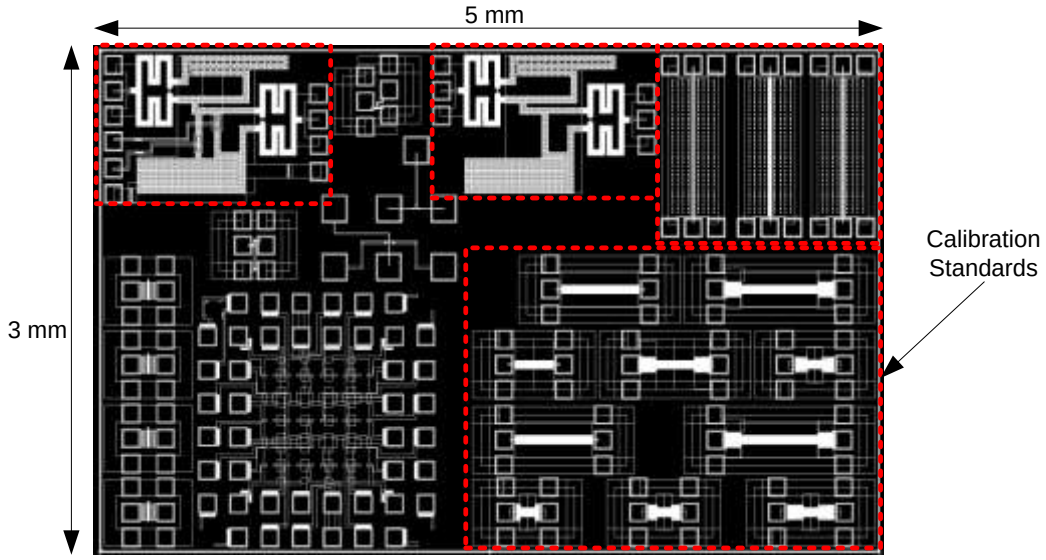


Figure 5.1. IC layout showing the slow-wave delay lines, passive delay line filter and a SDL filter.

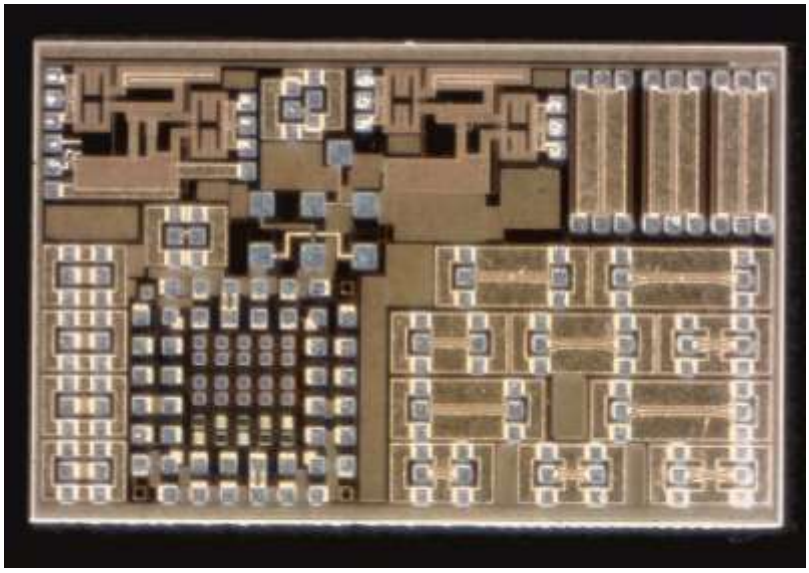


Figure 5.2. Micrograph of prototype die.

5.2.1 Probe pads

The pitch of the GSG probe pads has been matched to the pitch of the available Cascade Microtech Infinity probes. The probe pads therefore have a pitch of 150 µm (centre to centre). The pads are sized 115 µm x 115 µm to provide sufficient space for the probe to skate on the pads and make contact. The probe pads are on the AM layer of the BEOL. The pads were positioned to allow for simple placement of the probes and DC needles

when conducting measurements. The pad sets were therefore placed opposite each other in all cases. The orientation and placement of the pads are detailed in Figure 5.3.

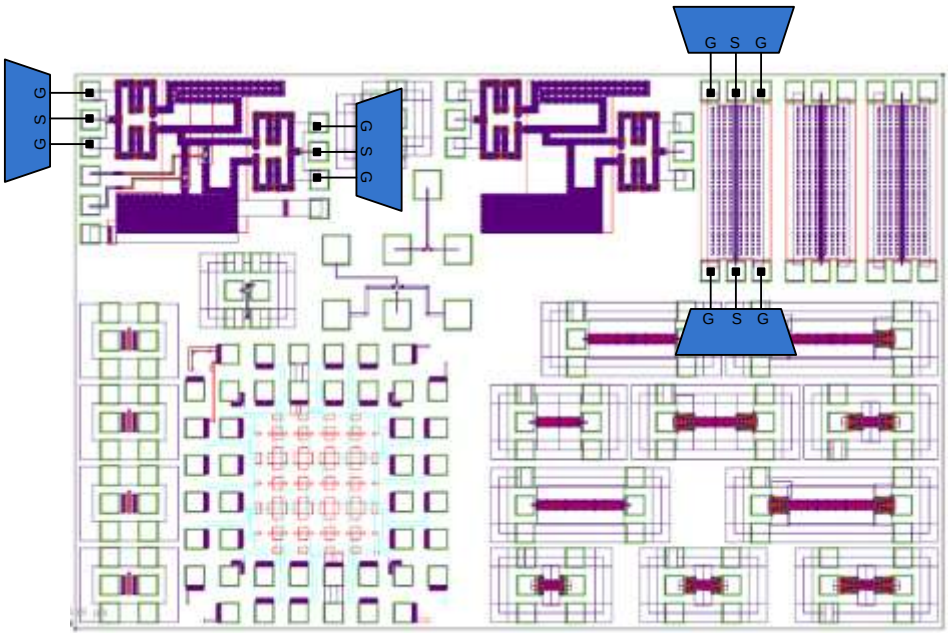


Figure 5.3. Layout of die and pad placement.

5.2.2 Slow-wave delay line layout

The slow-wave coplanar delay lines with varying floating metal strip spacings were fabricated to verify their respective simulation results. Three transmission lines were fabricated, comprising:

a) (No Strip) A CPW transmission line with no shielding mechanism
b) (Narrow Strip Spacing) A slow-wave shielded CPW transmission line containing floating metal strips with dimensions *SS* = 2 µm and *SL* = 1.6 µm
c) (Wide Strip Spacing) A slow-wave shielded CPW transmission line containing floating metal strips with dimensions *SS* = 5 µm and *SL* = 4.8 µm.

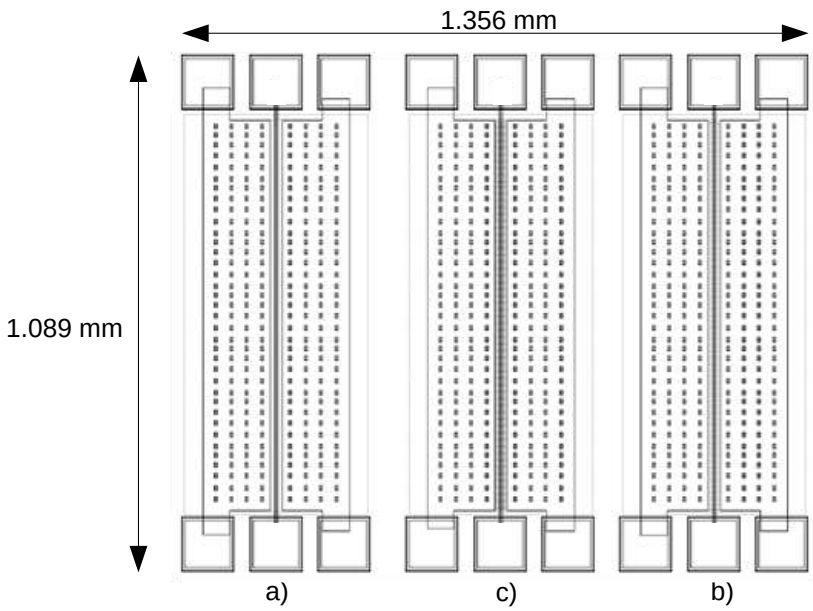


Figure 5.4. Layout of three slow-wave coplanar delay lines. a) No strip CPW. b) Narrow strip spacing CPW. c) Wide strip spacing CPW.

The CPW structures have a physical length of 840 µm. Additional CPW structures could not be fabricated due to the limited chip area. A physical length of 840 µm was chosen for all HFSS simulation and for the fabricated transmission lines. The same electrical length was used for simulations and measurements to accurately determine the agreement between HFSS simulations and measured results. The layout was generated in Cadence Virtuoso and subsequently imported into HFSS as discussed in Chapter 3 and Chapter 4. Probe pads are used to place the GSG probes of the VNA in order to perform on-chip measurements.

5.2.3 Power splitter layout

The layout of the *Powerdivx1* model is shown in Figure 5.5. Table 5.1 summarises the selected parameters of the model. The meander shape of the power splitter is used to reduce the overall area of the structure.

Table 5.1 Geometrical properties of power splitter model.

Parameter	Property
Signal width (W)	7 µm
Signal to ground width (G)	10 µm
Port length	50.0 µm
Signal to ground separation	100 µm
Number of metal levels	7
Signal layer	AM
Shield layer	MQ
CPW span	200.28 µm
Resistor width	12.92 µm
Resistor resistance	100.8046 Ω

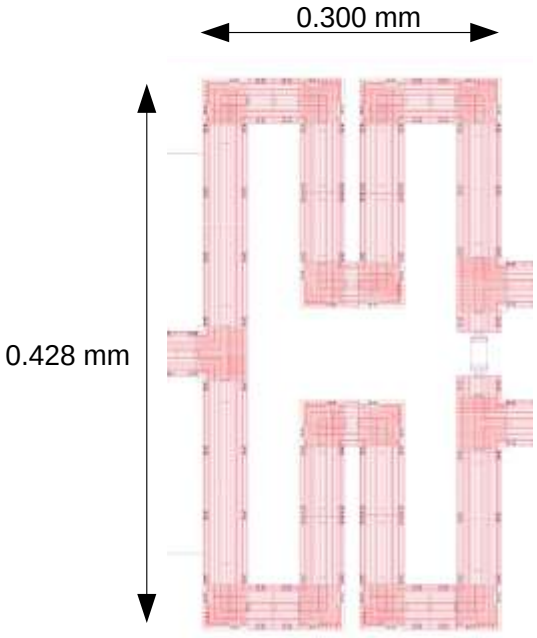


Figure 5.5. Layout of *Powerdivx*1 model.

5.2.4 Filter topology and layout

Two filter topologies were fabricated as part of the fabrication run conducted under MOSIS. The first design is a passive filter topology with a single centre operating frequency of 70 GHz. The second filter topology is a switched delay line network where either of two centre frequencies can be selected. The active filter topology contained switching transistors. The result of the active SDL filter does not form part of the research conducted in this dissertation. The narrow floating metal strip slow-wave CPW is used with the delay line network of the structures. Both filter topologies consist of the same geometric properties, BEOL layer selection, slow-wave floating metal strip dimensions and spacing.

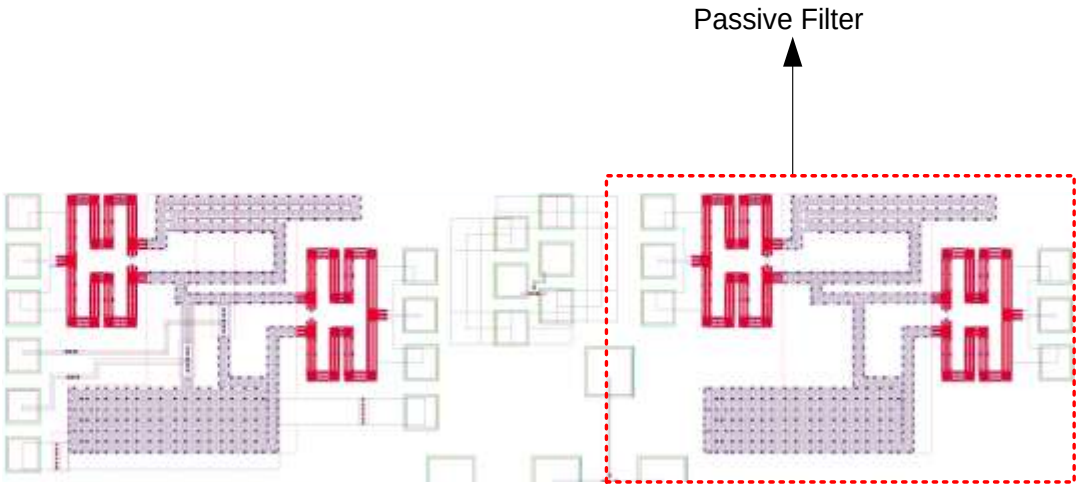


Figure 5.6. Layout of fabricated filters.

5.2.4.1 Passive filter layout

The passive layout is shown in Figure 5.7. The filter input and output are connected to GSG probe pads at each side. The slow-wave delay lines were constructed in a meander pattern to allow the design to fit within the allocated spacing. It can also be seen from Figure 5.7 that the signal width and signal to shield spacing of the power splitter is equal to that of the slow-wave CPW delay line network. The lengths of the delay lines, θ_1 and θ_2, were discussed in Chapter 4. Each section and non-zero bend of the meander delay line were taken into account.

The exact delay line lengths could not be achieved when drawing the artwork because of the bends introduced by the meander delay line. The end point of the meander line was not in the exact physical position required when integrating it with the other sub-element; therefore an approximate value was used. Simulation results however confirmed that the artwork achieved the requirements and therefore the artwork was not further optimised. Table 5.2 shows the calculated and measured artwork delay line lengths.

Table 5.2 Delay line length.

Parameter	Calculated Delay Length (*l*) (µm)	Fabricated Artwork Length (*l*) (µm)
θ_1	114.50	116.70
θ_2	2705.00	2715.43
$2\theta_1$	229.00	230.12
$2\theta_2$	5410.00	5399.00

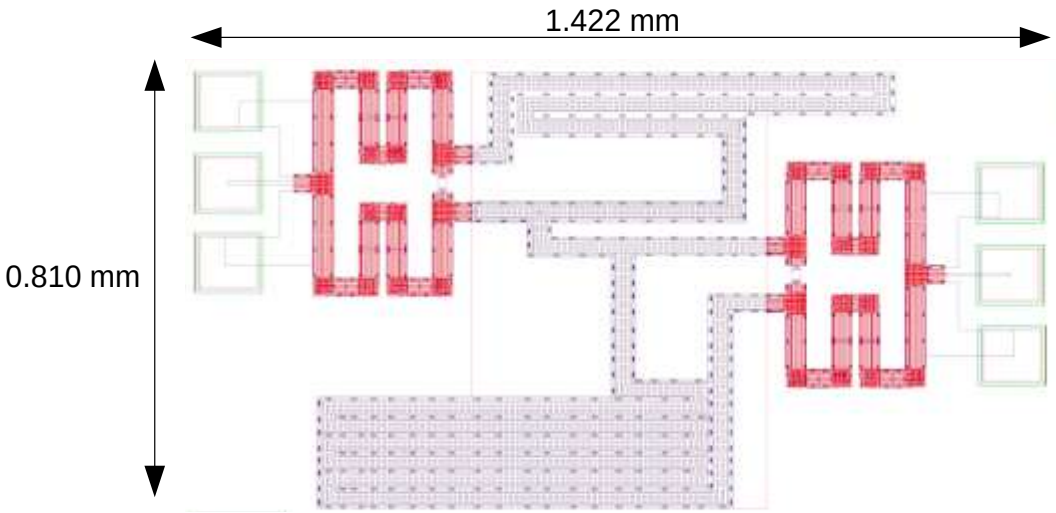


Figure 5.7. Layout of fabricated passive delay line filter.

5.3 EFFECTS OF PROBE PADS

Figure 5.8 shows the electric field of the fabricated narrow strip spacing CPW with probe pads. The GSG excitation method was once again used as shown in Figure 5.8 that a high electric field concentration is prevalent under the signal or centre probe pad.

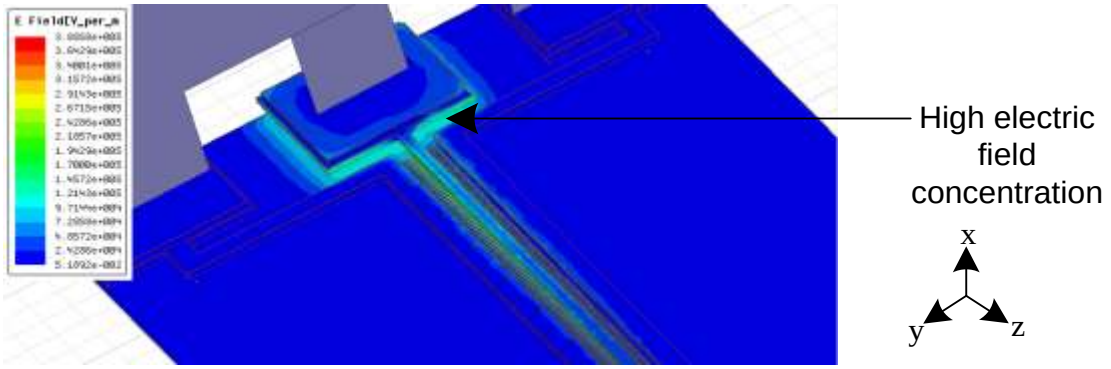


Figure 5.8. Electric field distribution of fabricated narrow strip spacing slow-wave CPW.

Figure 5.9 shows the $|S_{21}|$ of the three fabricated CPWs with the probe pads. The region below 50 GHz corresponds well with the simulated CPWs without probe pads. The second region occurs between 50 GHz and 88 GHz. This region demonstrates a drastic increase in loss. The third region demonstrates a local minimum in transmission for the three CPWs at 90 GH. The liner loss introduced into the circuit in the first region may be attributed to parasitic capacitances; however in the second and third region a resonance is present; which is supported by the strong electric field shown in Figure 5.8. An introduction of a shunt capacitor in conjunction with a series inductor as the probe pad shall counteract the resonant effect introduced by the probe pad. Figure 5.9 therefore highlights the importance of accurately calibrating the VNA and also de-embedding the measured results which are discussed in Chapter 6.

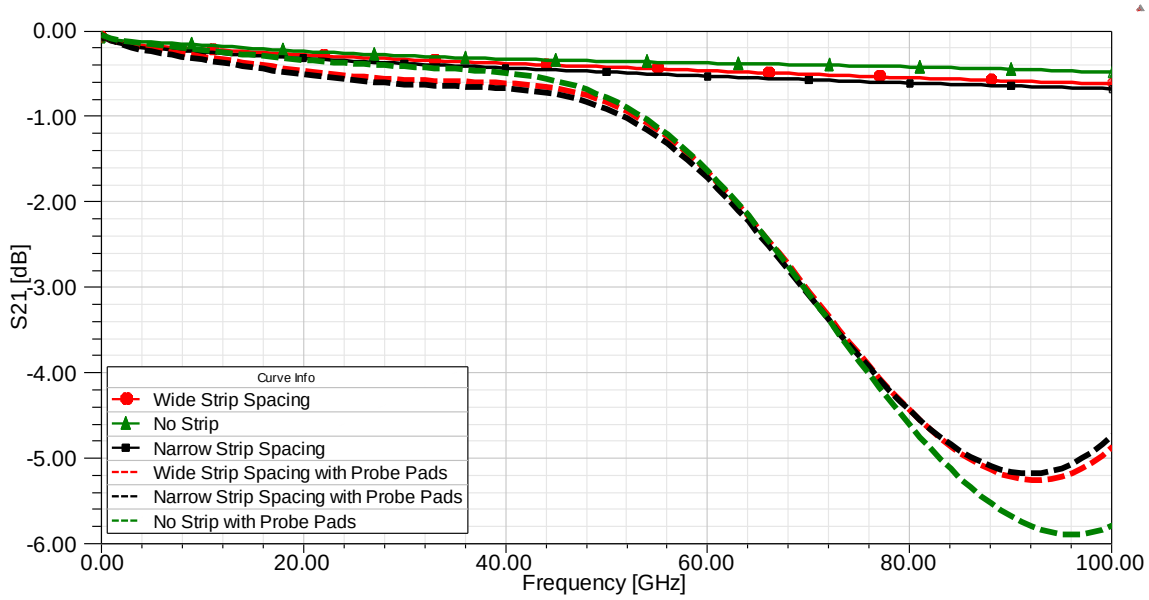


Figure 5.9. Simulated S_{21} magnitude response of the CPW structures with and without probe pads.

5.4 CONCLUSION

This chapter discussed the layout of the slow-wave CPW delay lines and elements which make up the delay line filter. The placement of the probe pads to conduct on-chip measurements was also highlighted. The effect of probe pads on the slow-wave transmission lines was furthermore investigated. It is noted that the probe pads may introduce additional losses; for this reason it is essential to de-embed the measured results. Chapter 6 discussed the measured results of the manufactured IC.

CHAPTER 6 RESULTS

6.1 INTRODUCTION

This chapter presents the measurement results obtained for the fabricated slow-wave CPWs with various strip spacings and the slow-wave mm-wave filter. On-chip measurements are conducted by means of the wafer probing and a VNA. This chapter further highlights the need for de-embedding the S-parameters of the slow-wave delay line structures and filter. The performance of the slow-wave CPW delay lines and filter, as well as the shortcomings and layout design limitations, are presented. The chapter concludes with an interpretation of measurement results and findings.

6.2 TEST SETUP

A photograph of the wafer probe station used to complete the on-chip measurements is reproduced in Figure 6.1. The connection in the figure shows the probes positioned for measurement of the passive slow-wave delay line filter. The VNA provides a single tone response measurement from 70 kHz to 110 GHz. The chuck has a vacuum base for the DUT to be held in place during measurements. The vacuum hole pitch of the chuck is, however, too large and could not hold the 15 mm^2 DUT in place. A single sided adhesive film was therefore used in order to hold the DUT. The adhesive film was placed on the vacuum chuck. A high performance microscope and viewing screen was used to view the probe tips and DUT, to facilitate probe alignment and ensure that an adequate connection between the DUT and probe was established.

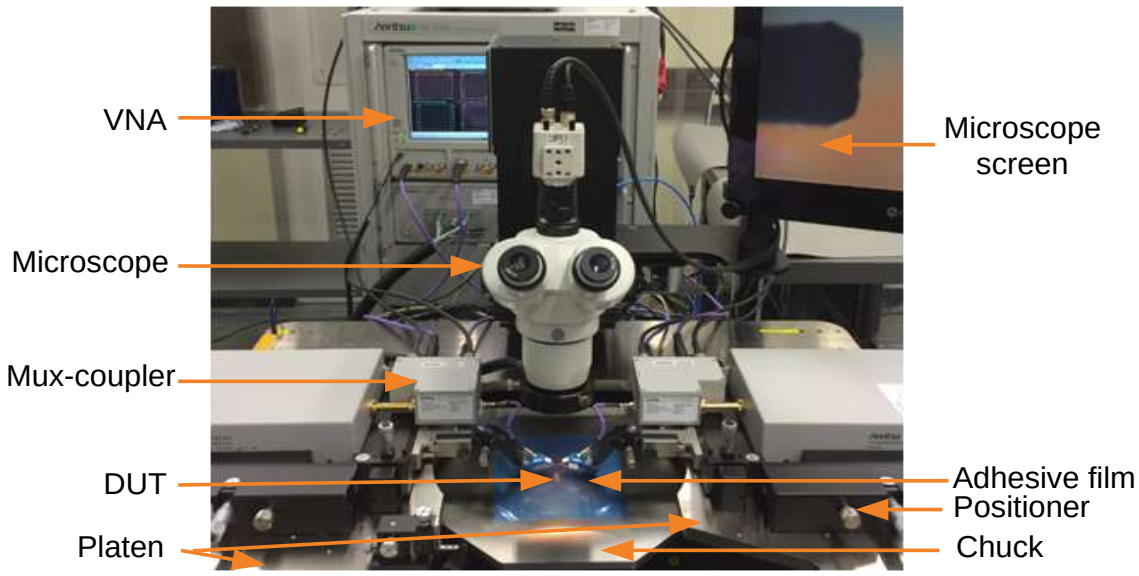


Figure 6.1. Photograph of probe station taken at the Carl and Emily Fuchs Institute for Microelectronics (CEFIM).

6.3 VNA CALIBRATION

The calibration of the VNA is important to ensure that interconnect loss and mismatch are interpreted as part of the measured results of the DUT. The VNA measures vector ratios of transmitted and reflected power at a plane inside the equipment. It is therefore important to move the reference plane to the edge of the DUT. The reference plane for wafer measurements is located at the probe connected to the VNA port. A two-tier calibration approach is used by means of taking into account the errors introduced by the non-ideal nature of cables or probes as well as the internal characteristics of the VNA.

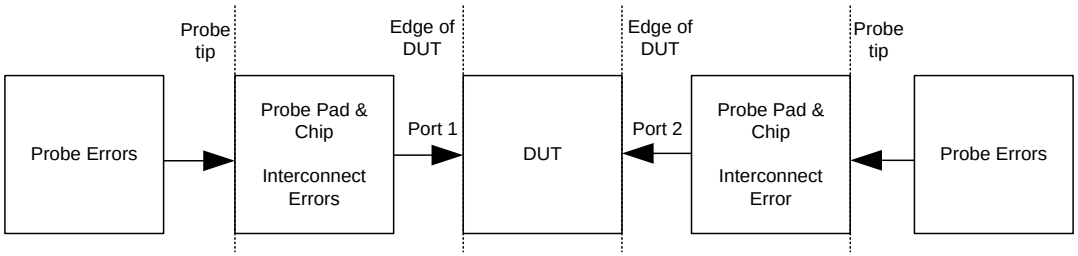


Figure 6.2. Two-tier measurement setup.

An impedance standard substrate (ISS) was provided by the probe manufacturer and was used to calibrate the VNA up to the probe tips. The ISS SOTL calibration standards were

measured from a PC connected to the VNA, the error terms calculated, and thereafter error correction applied on the VNA using the Cascade Wincal XE Software. The VNA stores the error model with several terms for each frequency point. This approach was utilised to calibrate the VNA before all measurements were conducted. All measurement results were recorded within six hours, using the same calibration setup.

6.4 DE-EMBEDDING MEASUREMENTS

The block diagram of a network analyser measurement two-port model is shown in Figure 6.3. The TRL calibration scheme is used for mathematically de-embedding the measured results from the probe pads' response. The three parameters allow for errors to be characterised. These errors are thereafter subtracted from the measured parameters in post-processing.

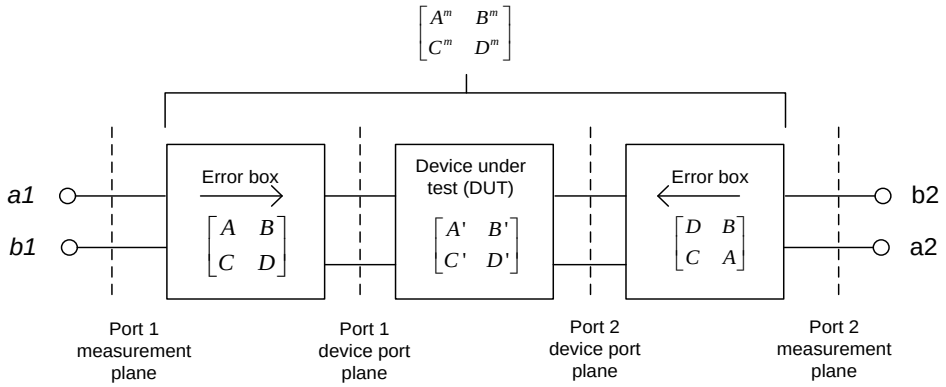


Figure 6.3. Two-port device model of VNA.

The measured S-parameters of the DUT are corrected by means of the TRL error box technique [56]. *ABCD* parameters are used to represent the solution as they offer a simpler method to cascade and remove the 2-port parameters. Assuming symmetric error boxes, the parameter of the network in Figure 6.3 can be expressed as [56]

$$\begin{bmatrix} A^m & B^m \\ C^m & D^m \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} \begin{bmatrix} D & B \\ C & A \end{bmatrix} \tag{6.1}$$

The parameter of the DUT (*A' B' C' D'*) of the DUT can therefore be expressed as [56]

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} \begin{bmatrix} A^m & B^m \\ C^m & D^m \end{bmatrix} \begin{bmatrix} D & B \\ C & A \end{bmatrix}^{-1} \tag{6.2}$$

The de-embedding procedure detailed in (6.1) has been analytically performed by means of a Python script.

6.5 DE-EMBEDDED TRANSMISSION LINE MEASUREMENT RESULTS

The measured S-parameters for the narrow, wide and no strip spacing slow-wave CPW structures are shown in Figure 6.4 to Figure 6.7. The graphs show the simulated, measured and de-embedded $|S_{21}|$ results of each structure. The simulated results were generated by 3D full-wave EM simulation in HFSS.

Figure 6.4 shows the simulated, measured and de-embedded measurement results of the wide strip spacing CPW. It can be observed from the figure that the three $|S_{21}|$ results are within 1.75 dB at 70 GHz. The de-embedded results indicate lower loss throughout the frequency band compared to the raw results. This is due to the fact that the de-embedded results remove the un-modelled parasitic effects of the probe pads on the transmission line structure. The de-embedded and simulated results are within 0.11 dB at 70 GHz.

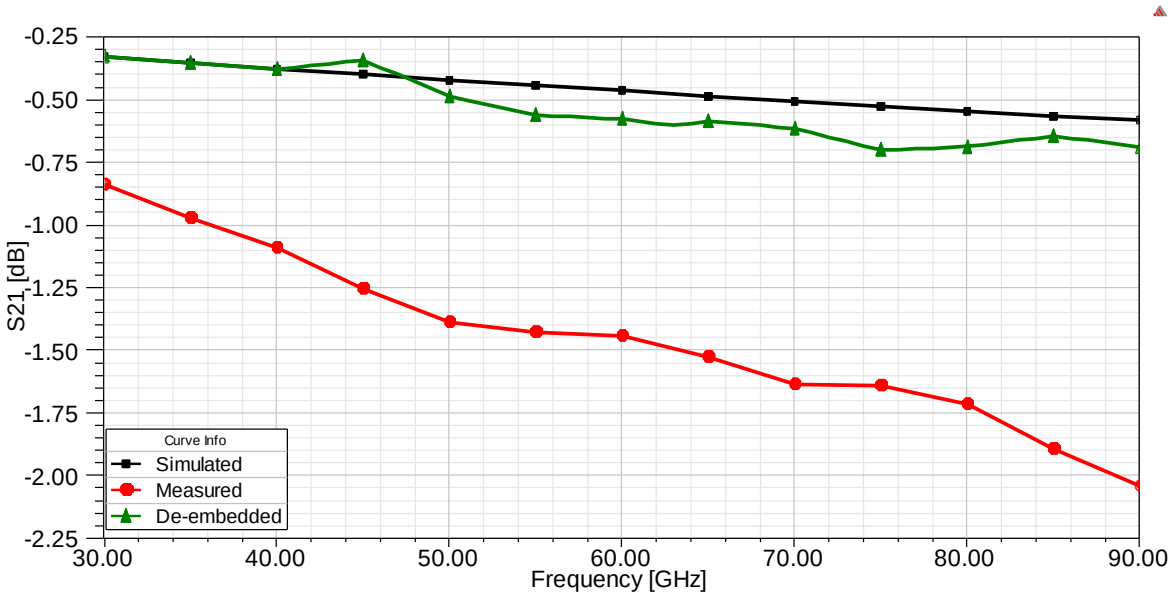


Figure 6.4. Simulated, measured and de-embedded $|S_{21}|$ of the wide strip spacing CPW.

The $|S_{21}|$ of the narrow strip spacing CPW is shown in Figure 6.5. The simulated and de-embedded results correspond well from 30 GHz to 90 GHz. A similar response to that of the wide strip spacing CPW is observed. The raw measured result once again demonstrates the effect of the probe pads. The de-embedded and simulated results are within 0.42 dB at

70 GHz. The de-embedded results vary by a maximum of 0.47 dB from 30 GHz to 90 GHz.

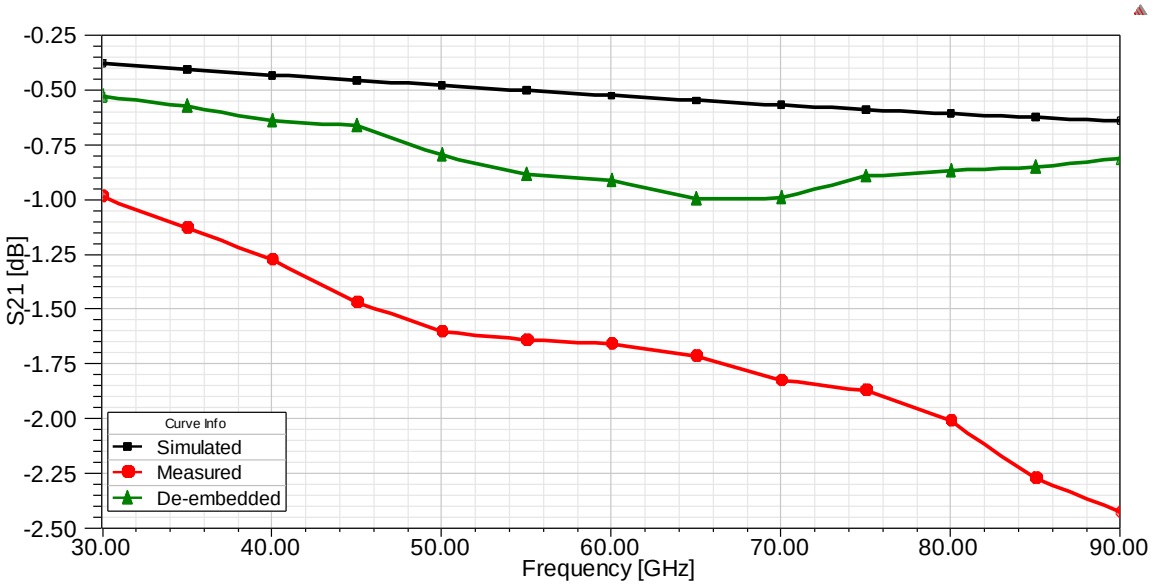


Figure 6.5. Simulated, measured and de-embedded $|S_{21}|$ of the narrow strip spacing CPW.

The $|S_{21}|$ of the no strip spacing CPW is shown in Figure 6.6. The simulated, measured and de-embedded results follow similar trends when compared to the wide and narrow strip spacing CPW results. The de-embedded and simulated results are within 0.48 dB at 70 GHz. The de-embedded results vary by a maximum of 0.44 dB from 30 GHz to 90 GHz.

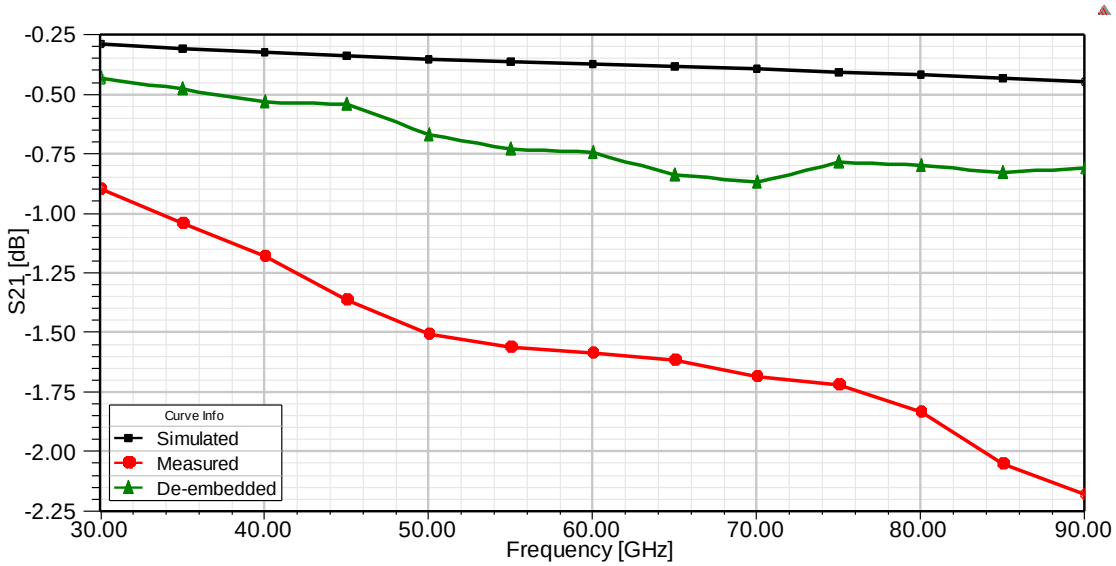


Figure 6.6. Simulated, measured and de-embedded $|S_{21}|$ of the no strip CPW.

A comparison between the de-embedded and simulated results of the narrow, wide and no strip spacing slow-wave CPW structures is presented in Figure 6.7. In both sets of results the narrow strip spacing CPW has the highest insertion loss of the three lines. The wide

strip spacing CPW shows the least insertion loss in the de-embedded results at 70 GHz; however, simulation results indicate that the no strip CPW has the least insertion loss. Table 6.1 summarises the electrical performance of the three CPWs. The variation in the insertion loss of the no strip and wide strip spacing CPWs could be caused by the large shielding ratio which effectively shields the CPW. It can also be observed that the narrow strip spacing CPW demonstrated the largest group delay in simulation and measured results.

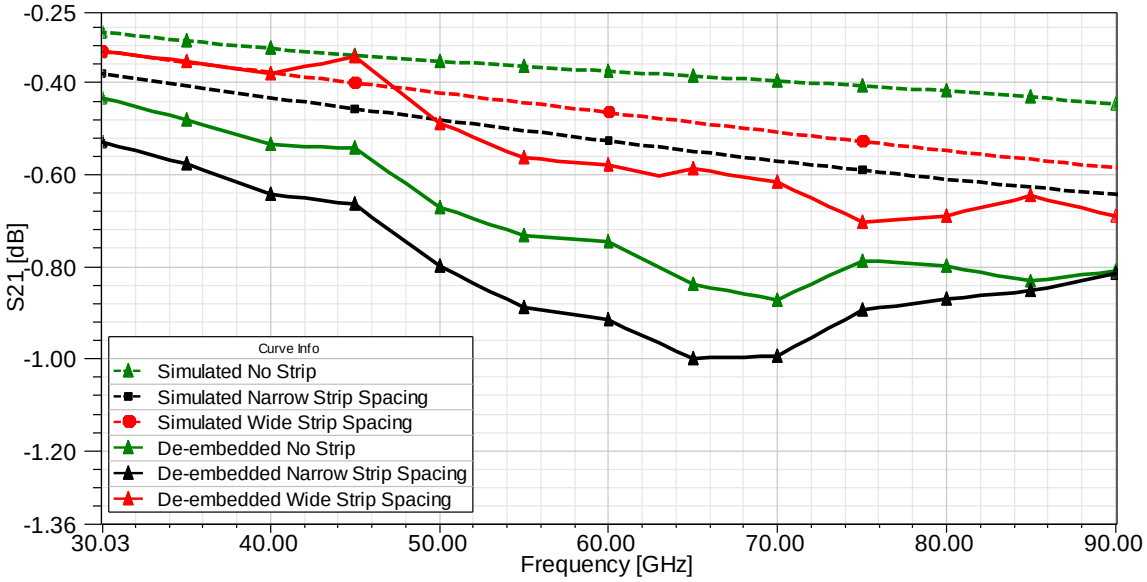


Figure 6.7. Simulated and de-embedded $|S_{21}|$ of the CPW structures.

Table 6.1 Electrical performance of the three CPWs.

Transmission Line Type	SL (µm)	SS (µm)	Delay Line Length (µm)	$\|S_{21}\|$ at 70 GHz (dB)		Measured Group Delay at 70 GHz (ps)	
				De-embedded	Simulated	De-embedded	Simulated
No Strip CPW	No shielding		840	-0.87	-0.39	7.050	5.235
Narrow Strip Spacing CPW	1.6	2	840	-0.99	-0.57	7.593	5.610
Wide Strip Spacing CPW	4.8	5	840	-0.62	-0.51	6.894	5.521

Figure 6.8 shows the characteristic impedance of the simulated and de-embedded measurement results of the lines. At 70 GHz the no strip, wide and narrow strip spacing

CPWs demonstrate an impedance of 46.33 Ω, 50.69 Ω and 43.49 Ω respectively. The narrow strip spacing has the lowest characteristic impendence, which can be attributed to the increased loading capacitance of the floating metal strips.

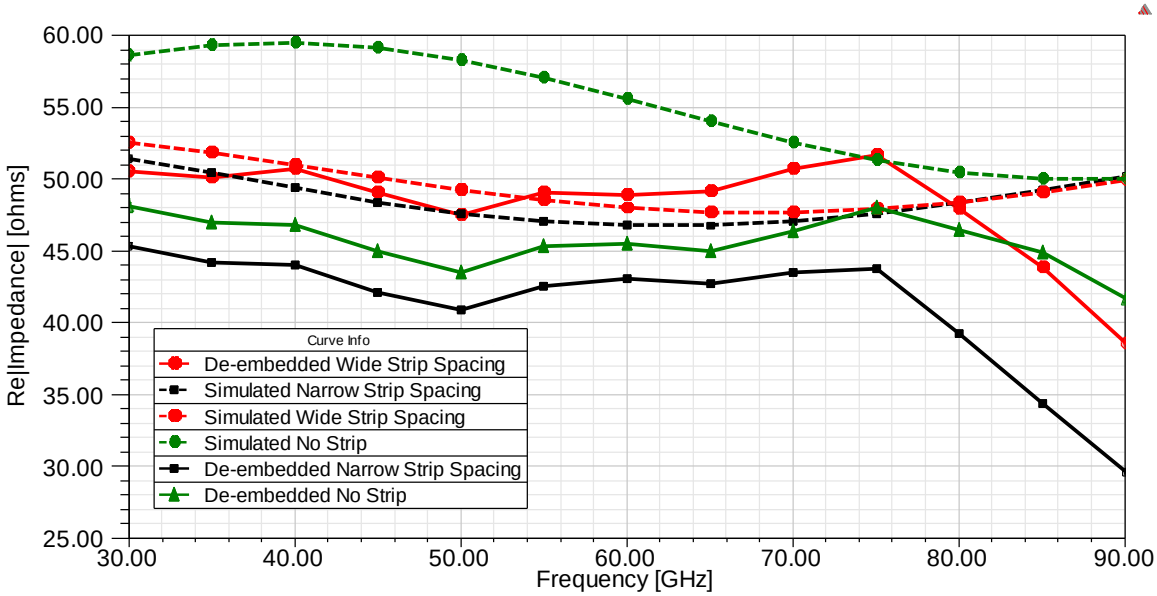


Figure 6.8. Simulated and de-embedded characteristic impedance of the CPW structures.

The attenuation constant is shown in Figure 6.9. At 70 GHz the no strip, wide and narrow strip spacing CPWs have a measured attenuation constant of 0.71 dB/mm, 0.56 dB/mm and 0.86 dB/mm respectively. Since the narrow and wide strip spacing CPWs have the same transmission line width, length and ground spacing; it is evident that the floating metal strip dimensions do affect the effective dielectric of the CPW. Subsequently, the strip length and spacing do also influence the EM field distribution. Having established that the de-embedded results appear to have more loss than the simulation results, it is evident that the simulation results to not take into account the unmodelled effects such as surface roughness loss present in CMOS transmission lines.

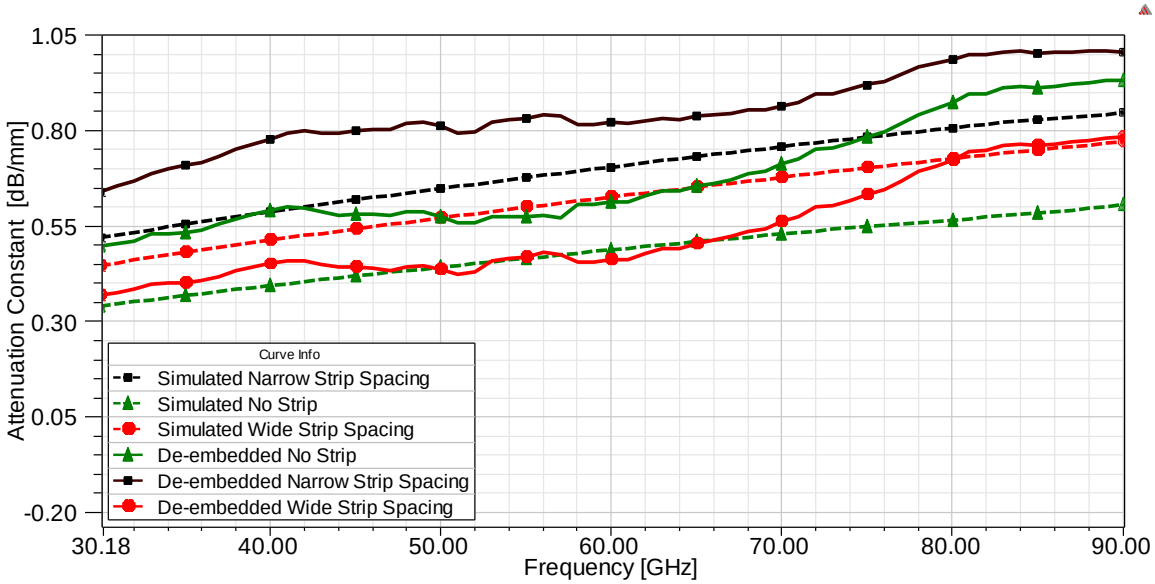


Figure 6.9. Simulated and de-embedded attenuation constant of the CPW structures.

The phase constant is extracted from the simulated and de-embedded measured results and portrayed in Figure 6.10. The narrow strip spacing achieves the highest phase constant in both data sets. At 70 GHz the no strip, wide and narrow strip spacing CPWs have a measured phase constant of 5.91 rad/mm, 5.73 rad/mm and 6.07 rad/mm. The variation between the measured and simulated phase constant values can be attributed to unmodeled simulation material properties as compared to the measured results which demonstrate the results from the real propagating medium.

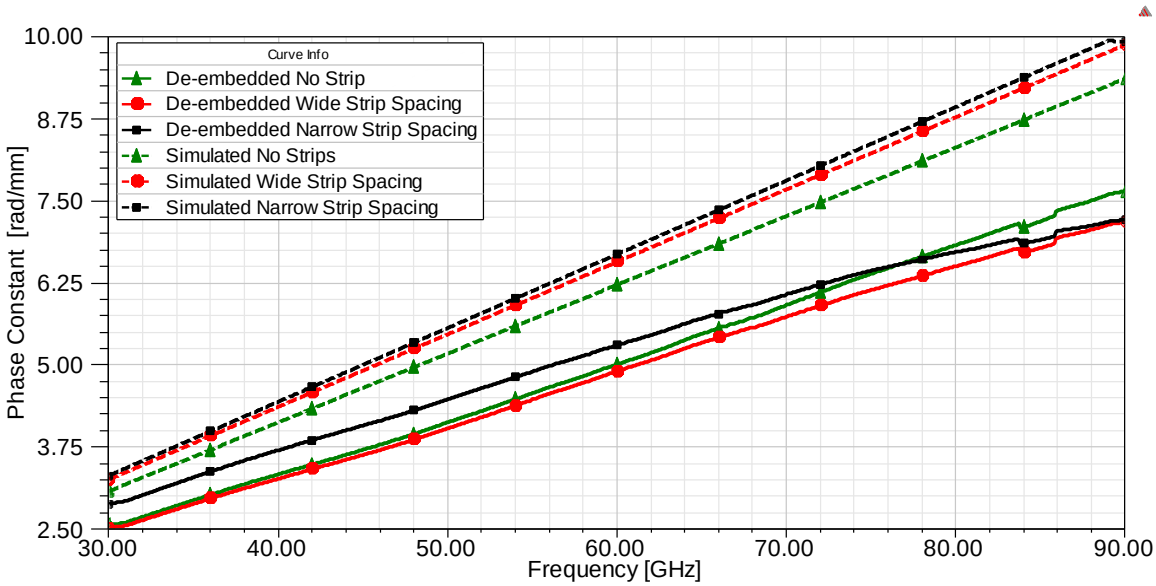


Figure 6.10. Simulated and de-embedded phase constant of the CPW structures.

The *Q*-factor for the simulated and de-embedded results is calculated and shown in Figure 6.11. The calculated values from the de-embedded results are lower than the simulation values which is primarily caused by the higher measured attenuation constant. At 70 GHz the no strip, wide and narrow strip spacing CPWs have measured *Q*-factors of 13.12, 15.38 and 25.78 respectively.

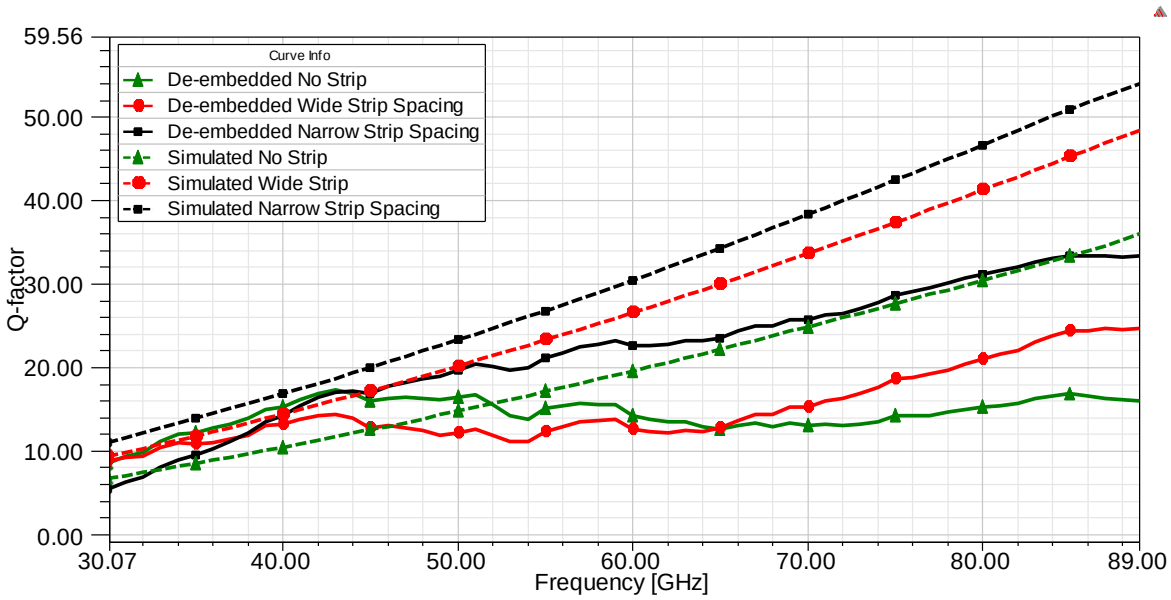


Figure 6.11. Simulated and de-embedded *Q*-factor of the CPW structures.

Table 6.2 and Table 6.3 compare the simulation and measured results of the three CPW lines. The measured results indicate that there is a difference of approximately 10 between the simulated and measured *Q*-factor of the three CPWs. The narrow strip spacing still, however, achieves the highest *Q*-factor. The attenuation constant shown in Figure 6.9 shows higher attenuation compared to the simulated results. The difference between the measured and simulated results could be caused by unmodelled surface roughness which has proven to introduce loss [57]. The increased attenuation reduces the *Q*-factor of the measured transmission line. The phase constants of the three lines are very similar across the frequency band. The narrow strip spacing demonstrates the highest phase constant at 70 GHz. Even though there is some disagreement between the simulated and measured results, it is evident that the narrow strip spacing possesses the greatest group delay and highest *Q*-factor at 70 GHz in measurement. This confirms the research question that the narrow strip spacing CPW is best suited for implementation in the filter topology. In Section 6.6 the results of the delay line filter utilising the narrow strip spacing CPW are presented.

Table 6.2 Attenuation and phase contact of the three CPWs.

Transmission Line Type	Attenuation Constant at 70 GHz (dB/mm)		Phase Constant at 70 GHz (rad/mm)	
	De-embedded	Simulated	De-embedded	Simulated
No Strip CPW	0.92	0.52	5.91	7.25
Narrow Strip Spacing CPW	0.86	0.75	6.07	7.81
Wide Strip Spacing CPW	0.56	0.68	5.73	7.66

Table 6.3 *Q*-factor and characteristic impedance of three CPWs.

Transmission Line Type	Characteristic Impedance at 70 GHz (Ω)		Q-factor at 70 GHz	
	De-embedded	Simulated	De-embedded	Simulated
No Strip CPW	52.52	46.33	13.12	24.90
Narrow Strip Spacing CPW	47.02	43.49	25.78	38.30
Wide Strip Spacing CPW	47.64	50.69	15.38	33.64

6.6 FILTER MEASUREMENTS

The measurements of the slow-wave filter are presented in this section. Measurements are conducted on the same setup used to measure the performance of the slow-wave CPW transmission line structures utilising the VNA. All on-chip measurements were also conducted within six hours using the same calibration setup in order to prevent invalidation of the calculated error terms.

6.6.1 Passive filter measurements

The graphs below indicate the $|S_{21}|$ and $|S_{11}|$ of the ideal, simulated, measured and de-embedded measurement responses. It can be noted from Figure 6.12 that the $|S_{21}|$ results agree well over the frequency band. The centre frequencies of the ideal, simulated and measured results are within 0.4 GHz, or 0.57 % fractional bandwidth. The de-embedded data displays lower attenuation compared to the measured results and shows the effects of the removal of the attenuation and shunt capacitances of the probe pads. The de-embedded passband attenuation of 5.83 dB at a centre frequency of 70.05 GHz differs by 1.62 dB from the simulated attenuation of 4.21 dB at 70.2 GHz. The variation in the measurements might be caused by the unmodelled surface roughness of the CPW. The variation of 1.62 dB is nonetheless acceptable, taking into consideration that the measurements are conducted at 70 GHz. As discussed in Chapter 4, the bandwidth is calculated as the frequency difference between the two -3 dB transmission points around the centre frequency. The bandwidths of the ideal, simulated, measured and de-embedded filter results are calculated to be 11.03 GHz, 14.21 GHz, 13.98 GHz and 14.53 GHz respectively.

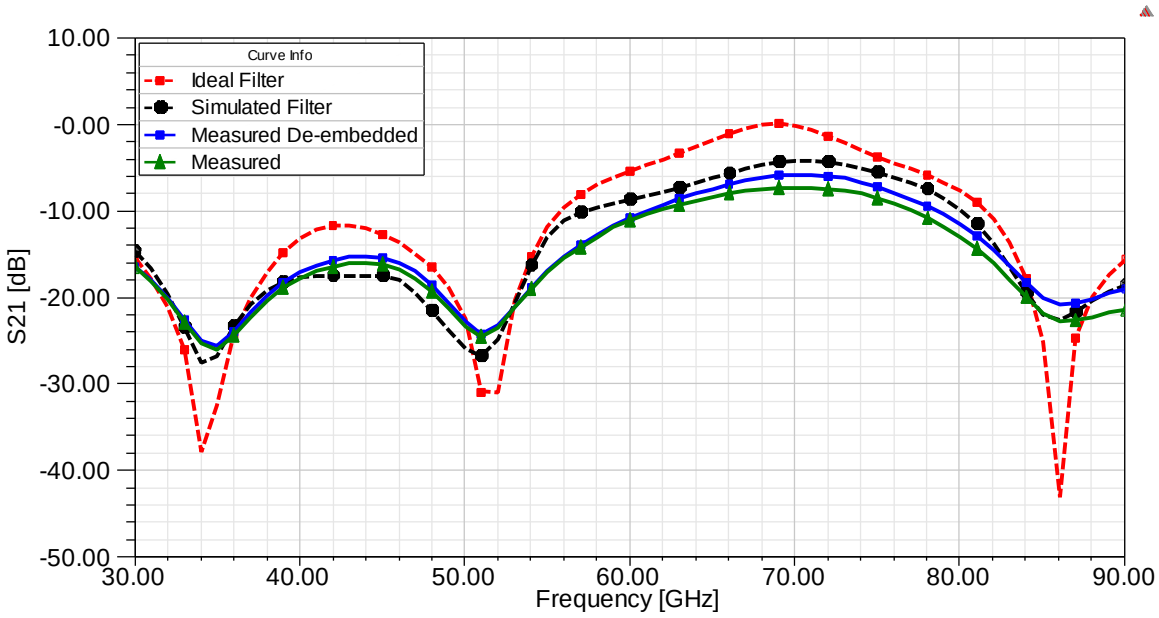


Figure 6.12. Ideal, simulated, measured and de-embedded $|S_{21}|$ of the slow-wave filter.

The input reflection coefficient for the passive filter is shown in Figure 6.13. The measurements agree with one another throughout the band of interest. The ideal, simulated, de-embedded and measured input reflection minima are measured to be -31.93 dB, -25.25

dB, -16.46 dB and -20.72 dB respectively. The local minima in reflection are found at 69 GHz, 70.2 GHz, 72.2 GHz and 72.2 GHz respectively.

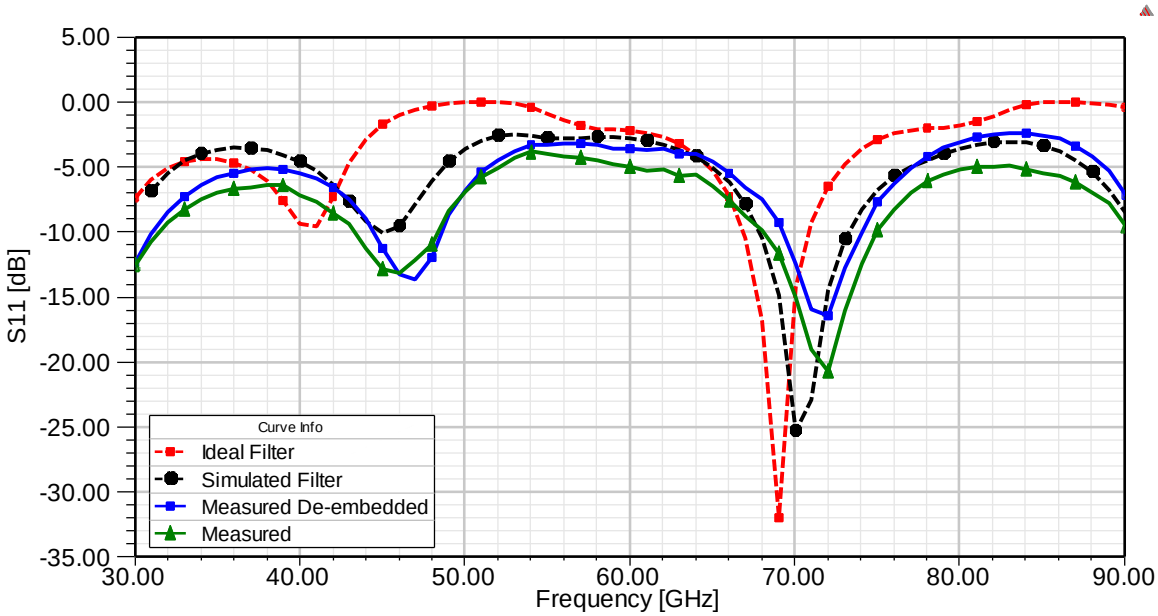


Figure 6.13. Ideal, simulated, measured and de-embedded $|S_{11}|$ of the slow-wave filter.

Table 6.4 summarises the electrical properties of the ideal, simulated and de-embedded measurement results. The centre frequency, bandwidth and *Q*-factor of the ideal, simulated and de-embedded filter agree well. The centre frequencies of the measurements are within 0.4 GHz, the bandwidth is within 3.5 GHz and the *Q*-factor within 1.5 as evident from the comparison shown in Figure 6.14.

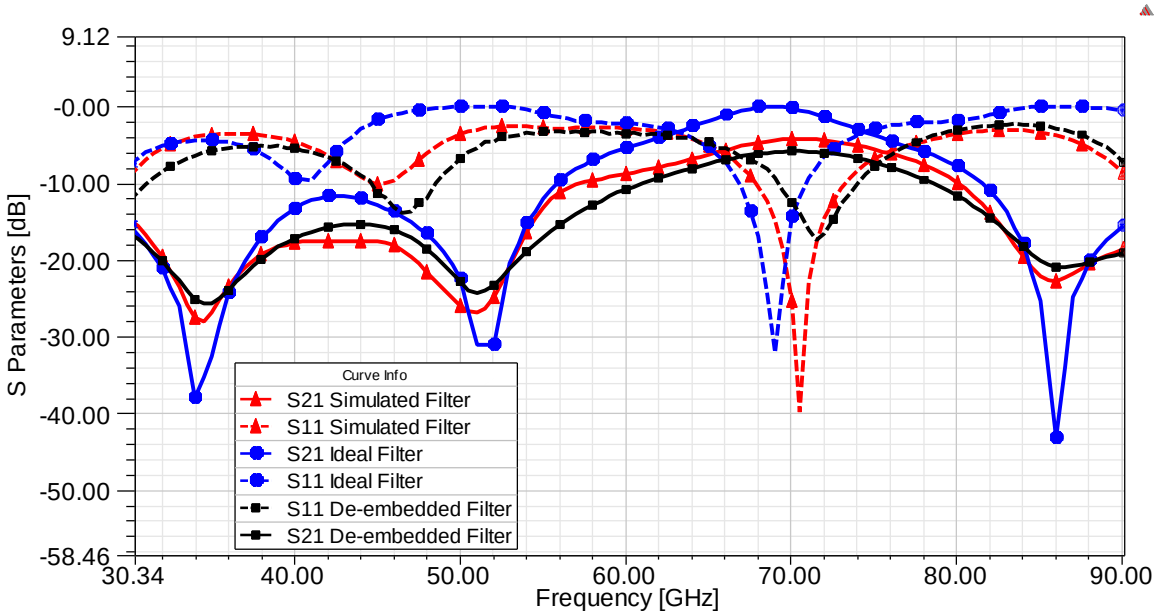


Figure 6.14. Ideal, simulated and de-embedded $|S_{11}|$ and $|S_{21}|$ of the slow-wave filter.

Table 6.4 Comparison of ideal and simulated artwork filter.

Filter	f_c **(GHz)**	***BW* (GHz)**	***BW (%)***	***Q*-factor**	***Passband Attenuation at*** f_c ***(dB)***
Ideal Filter	69.8	11.03	15.8	6.32	0.22
Simulated Filter	70.2	14.21	20.24	4.94	4.21
De-embedded Filter	70.05	14.53	20.74	4.82	5.83

The above further assists one in proving that the design methodology used to simulate the artwork is effective and satisfactorily approximates the performance of on-chip designs well into the mm-wave frequency band. It is therefore possible to design full passive networks in CMOS BEOL and analyse the behavioural model of the artwork using a 3D full-wave EM simulation tool such as HFSS.

6.7 CONCLUSION

The measurement data from the slow-wave CPW, passive filter and active SDL filter are presented in this chapter. The slow-wave delay line simulation approximates the measured result well. The narrow strip slow-wave delay line exhibits the largest group delay of 7.593 ps. This confirms the decision that it be used within the filter topologies.

The simulation results agree well with the measured results for the passive filter throughout the frequency band. A passband attenuation of 5.83 dB at the centre frequency of 70.05 GHz is achieved. The measured -3 dB bandwidth of 14.53 GHz is within 2.2 % of the simulated result. A good agreement between simulation and measurement results affirms the necessity for modelling mm-wave CMOS artwork in a 3D full-wave EM simulation tool. The measured filter has a *Q*-factor of 4.82 and a 20.74 % bandwidth. Chapter 7 presents the conclusion of the research.

CHAPTER 7 CONCLUSION

7.1 INTRODUCTION

This chapter provides a final conclusion of the research and data gathered in this dissertation in order to offer a critical analysis of the research questions.

Chapters 1 and 2 presented the research questions and a thorough literature review which investigated miniaturised CMOS delay lines design techniques and their application in mm-wave filters. The research focussed on the fundamental understanding of the slow-wave propagation mode and its application towards designing a CMOS delay line filter. Chapter 3 focussed on the research methodology followed in order to investigate the research questions. Chapter 4 highlighted the circuit design, modelling and simulation results that led to Chapter 5, which documented the IC layout and fabrication process. Chapter 6 discussed the results of the experimental measurements, which provided an assessment of the delay line and filter performance in order to answer the research questions.

7.2 TECHNICAL SUMMARY AND CONTRIBUTION

The following list details the main aspects of this research:

- Simulation results were conducted in HFSS. The good approximation, from 30 GHz to 90 GHz, between the simulated and measured sets of results is attributed to the accurate and effective modelling of the designs in full-wave EM software. Further to this; the ground ring approach of modelling the GSG probe as a PEC bridge in a full-wave EM software package also assisted in improving the accuracy of the simulation results. The use of full-wave 3D EM software proved to be an accurate method to model mm-wave CMOS delay lines.

- Floating metal shield strips placed under a CPW transmission lines achieved the slow-wave effect and proved to be the preferred choice to realise a delay line for mm-wave frequencies.

- The floating metal shield strips provide the benefits of:
    1. Artificially increasing the effective dielectric constant of the substrate.
    2. Slowing down the propagation velocity of the travelling wave and in turn reducing the length of the transmission line needed to achieve a specific group delay.
    3. Simulation and measurement results which show that a narrow strip spacing geometry achieves greater group delay than a wiser strip spacing geometry.

- A CMOS filter was designed in order to demonstrate the application of slow-wave delay lines in mm-wave applications. The delay line filter topology was miniaturised by means of introducing floating metal strips under a CPW, thereby realising a slow-wave structure which occupies less space compared to one with conventional delay lines. Simulation results of the passive filter approximate the measured results within 0.32 dB in the passband. The filter achieves a passband attenuation of 5.83 dB at a centre frequency of 70.05 GHz. The measured -3 dB bandwidth of 14.53 GHz is within 2.2 % of the simulated result. Several mm-wave filter topologies have been investigated, but according to the author's knowledge, the slow-wave CPW delay line filter topology has not previously been implemented in a microelectronic process or at any frequency above 5 GHz.

- It was demonstrated that mm-wave distributed passive devices may be realised in BEOL CMOS processes. This consequently demonstrates that CMOS is a feasible medium to achieve mm-wave SOC integration.

- A research paper presented in [58] at a peer reviewed conference and a submitted letter presented in [59] allows for exposure and for fellow researchers to further improve and create innovative research solutions in this field.

Table 7.1 summarises the key performance metrics of the slow-wave delay line and compares it to similar published designs.

Table 7.1 Comparison of slow-wave CMOS transmission line designs.

Reference	Slow-wave mechanism	Attenuation Constant (dB/mm)	*Q*-factor
[60]	Floating metal strips under a CPW	0.5 at 60 GHz	30 – 50 at 60 GHz
[30]	Floating metal strips with active control under a CPW	5.5 dB (Insertion loss)	Not measured
[61]	Floating metal strips under a coplanar stripline	0.6 at 20 GHz	27 at 20 GHz
[62]	Floating metal strips under a CPW	0.15 at 60 GHz	38 at 60 GHz
[63]	Floating metal strips under a CPW	0.5 at 40 GHz	20 at 40 GHz
[25]	Floating metal strips under a CPW	1.6 at 60 GHz	Not measured
[48]	Floating metal strips under a CPW	0.8 at 60 GHz – 28 nm ST 0.64 at 60 GHz – 0.35 µm AMS 1.1 at 60 GHz – 0.13 µm IHP	50 at 60 GHz (Q-Max)
[19]	Floating metal strips under a CPW on porous silicon substrate	4.4 at 100 GHz	17 at 100 GHz
This work	Narrow floating metal strips under CPW in BiCMOS 7 metal layer process	0.86 at 70 GHz	38.3 at 70 GHz
This work	Wide floating metal strips under CPW in BiCMOS 7 metal layer process	0.56 at 70 GHz	33.6 at 70 GHz
This work	No strips under CPW in BiCMOS 7 metal layer process	0.92 at 70 GHz	24.9 at 70 GHz

Table 7.2 summarises the key performance metrics of the slow-wave filter and compares these to similar published designs.

Table 7.2 Comparison of mm-wave filters.

Reference	Process	f_c (GHz)	-3 dB Bandwidth (%)	Passband Attenuation at f_c (dB)	*Q*-factor
[31]	0.18 µm CMOS	64	18.76	4.9	3.41
[32]	0.13 µm CMOS	60	18.28	2.56	3.28

[33]	0.18 µm CMOS	66	19.05	3.10	3.46
[34]	0.18 µm CMOS	77	10	9.3	7.7
This work	0.13 µm CMOS	70.05	20.74	5.83	4.82

7.3 LIMITATIONS AND ASSUMPTIONS

Geometries ranging from striplines to shielded CPW delay lines were investigated. The dissertation focussed on shielded floating metal strip CPWs; hence other topologies were not considered due to the lack of area availability on the IC. Furthermore, the filter design consisted of the power splitter, delay line network and link line; however, these elements could not be individually tested due to the lack of die area.

7.4 FUTURE WORK AND POSSIBLE IMPROVEMENTS

The technique applied in this dissertation to realise CMOS mm-wave slow-wave designs can be applied to many different topologies, technologies and circuits. The full-wave simulation took several hours to compile per run and resulted in an extended design period. Further research and work may be focussed on optimising the design process and reducing simulation times in HFSS.

The floating metal strip line CPW has been implemented in this dissertation. Future research may focus on adapted CPW transmission line geometries such as the grounded comb or periodic CPW transmission lines and their associated performance when implementing a delay line filter. The dissertation discusses the miniaturisation of delay lines using the slow-wave principle; however, unique floating metal strip geometries, such as a honeycomb or criss-cross, can now be implemented in the latest CMOS processes. This could prove to be an interesting study when implemented in the form of a shielded CPW structure. By investigating different feed methods it may be possible to improve the accuracy of simulation and measurement results. As discussed in Chapter 6, the variation between results may be caused by unmodelled surface roughness. Further research may therefore be focussed on obtaining accurate surface roughness values.

More extensive research and analysis on mm-wave switching elements could be conducted to achieve a frequency agile filter. Future research may focus on the most suitable RF MOSFETs or heterojunction bipolar transistors (HBTs) switching topologies which could

be implemented in a BiCMOS process and the necessary conditions that need to be met to successfully bias the devices at mm-wave frequencies. Further research may also focus on implementing a SPDT switch in a triple-well CMOS process which can be used in an SDL filter. The associated active switching noise and parasitics effects induced by the SPDT in the filter pose interesting research questions.

A recent conference publication [30] has shown that the delay of a transmission line may be altered by means of applying a voltage to the gate of a MOSFET connected across the floating metal strip configuration. The MOSFETS act as varactors that vary the capacitance of the shield. This technique may be used to vary the delay of the delay line and, in turn, realise a frequency agile filter.

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