NON-DESTRUCTIVE STRUCTURAL ANALYSIS OF THE HEAT CONDUCTING PATH IN POWER ELECTRONICS AND SOLID STATE LIGHTING BY THERMAL TRANSIENT TESTING

Farkas G.[1*], Sarkany Z. [1], Szel A. [1], Rencz M[1,2].
[*]Author for correspondence
[1]Mentor Graphics, MAD,
[2]Budapest University of Technology & Economics, Dept. of Electron Devices,
Budapest, Hungary
E-mail: gabor_farkas@mentor.com

ABSTRACT

Thermal transient testing is a tool for examining structural details of a heat conducting path composed of heat conduction and heat convection sections. Using the change of inherent heat in electronics, temperature transients provide a characterisation technique where using x-ray or acoustic microscopy would be troublesome and time-consuming.

A complete toolkit for the accurate dynamic characterisation of subassemblies and cooling mounts is described in the paper. After giving the theoretical background, it is shown that the methodology can directly generate a valid and detailed structural equivalent from a single transient measurement.

The descriptive thermal functions such as time constants and structure functions are demonstrated in practical examples, the capability of the structure functions for validating cooling concepts and detecting assembly problems is shown.

Recognising the fact that systems with multiple energy transport such as electric energy converted to heat and light exhibit special features; the concept of structure functions has been modified for applications in solid state lighting.

INTRODUCTION

With the dramatically growing *power level* in electronic systems (e.g. electric cars, locomotives) and *power density* (e.g. mobile phones producing watts in a tight case with no ventilation) the characterisation of the heat removal capability is of primary interest already in the design phase, and then in manufacturing and eventual failure analysis.

It is often forgotten that measurement and simulation are always accompanied with an inherent *modelling* step. Measuring the size of an object and claiming its length, width and height is equivalent to replacing it by a single block model and describing it by these three parameters. In thermal analysis a deeper model is expected, of course.

A primary quantity for examining a system design is the temperature elevation at certain powering. In engineering, we often simplify the thermal model to an R_{th} *thermal resistance*, that is total temperature change divided by power change.

The transient techniques enable measuring partial thermal resistances and subpart capacitances. In its fully developed form, the descriptor called *structure function* helps identifying parts, eventually failure locations in a complex cooling system. Furthermore, the degradation of structural elements in an operating system can be observed continuously, in a non-destructive way. Using the *change* of inherent heat in electronics, temperature transients provide a characterisation technique where using x-ray or acoustic microscopy would be troublesome and time-consuming.

Below we restrict our treatise on systems with a single heat source. Systems of multiple heat sources are discussed in [10].

THERMAL TRANSIENT MEASUREMENTS

In power electronics and solid state lighting the source of the heat is typically a semiconductor die, more precisely a thin dissipating layer within the die. In many cases this is a forward biased p-n junction in the device, so the heat source is traditionally called "junction". As all parameters of a semiconductor device are temperature dependent, the junction can also be used as sensor. This way we can record the temperature change of the hottest point in the structure.

Although any power profile in time can induce temperature transients, typically a power step, a sudden change between two power levels is used as excitation for its simplicity. Because of the above mentioned temperature dependence of the parameters producing steady power is a demanding task in electronics, while constructing a steady current source is more feasible.

A rather precise power change can be created by *switching down* from a stabilised high I_{DRIVE} heating current to a low I_{SENSE} current level (Figure 1).

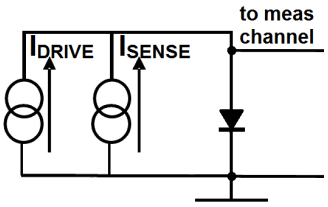

Figure 1 Powering scheme for a thermal transient

The sensor current maintains a forward voltage on the device, at nearly zero power. This voltage can be mapped to junction temperature in a *calibration* step, that is recording the voltage in a thermostat at different external temperatures.

Many details of the powering and sensing principles are given in [5].

Example 1. We chose a high power SCR module mounted on cold plate for analysis. In order to distinguish between the portions of the heat conducting path belonging to the device and to the cooling mount, we followed the thermal transient measurement standard JEDEC JESD 51-14 [3], fixing the samples first on a dry surface and then on the plate wetted by standard thermal grease.

With trial measurements we found that steady state can be reached within one minute by cold plate cooling.

Selecting 40A heating current and 2A sensor current we experienced crisp, noise free thermal transients (Figure 3). At the end of the heating when the device voltage stabilised, the current caused 44W power dissipation.

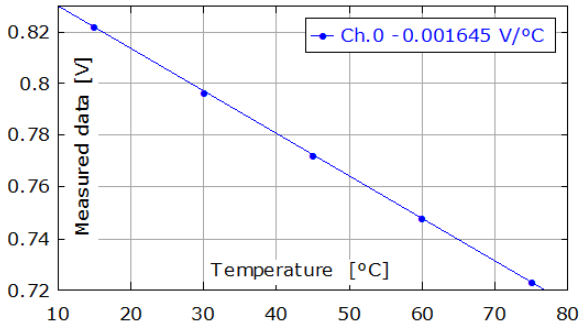

Figure 2 Voltage to temperature mapping at sensor current

The calibration showed that the temperature dependence of the forward voltage is quite linear at the sensor current (-1.64mV/K), although this is not a requirement for a valid mapping (Figure 2). This mapping scales the temperature axis of Figure 3.

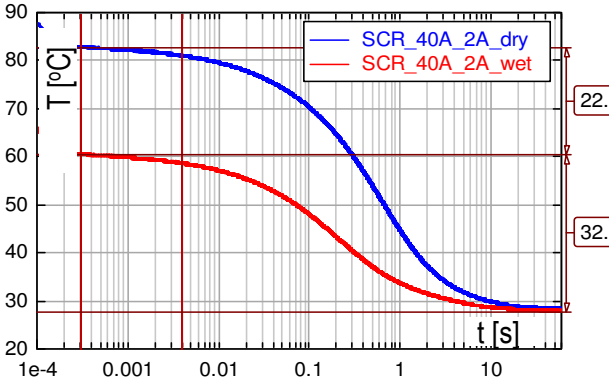

Figure 3 Measured cooling transients on the SCR with different boundary conditions

Figure 3 reveals that 44W heating power causes approximately 54 ºC temperature elevation at the "dry cold plate" boundary. The thermal grease fills the air gap beneath the device and diminishes the temperature change to 32 ºC.

THE LINEAR ADVENTURE

The cooling plot of Figure 3 already yields a lot of useful information. Usually the *time axis is logarithmic*, this helps analyse the thermal behaviour of different heat conducting portions. We see the *early time details*, which characterise the chip and package region, and later we can identify the cooling mount and the broader measurement environment.

Still, this plot is very specific; it describes the component behaviour on cold plate, at 44W power step only. We want to find descriptive functions, which predict the component behaviour at *different boundary, different power waveform* etc.

Reducing the cooling curves to temperature *change* only and fitting them at their hottest point (Figure 4) we find that the

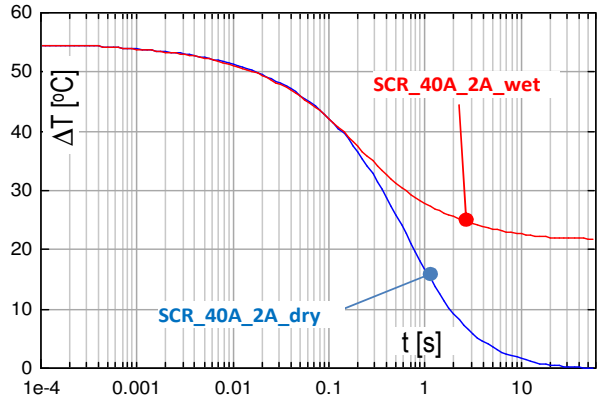

Figure 4 Component on high and low conductance boards, cooling curves fit at hot point

cooling is *not influenced by the actual boundary condition* until 0.2 s, the curves coincide perfectly. This can be easily explained stating that until 0.2 s the heat propagates inside the package, we still did not reach the air/grease thermal interface.

A beautiful world of powerful description tools can be entered assuming that *the behaviour of our thermal systems is linear*. Luckily, the material parameters of the components show only low dependence on temperature and radiation plays no important role at typical component temperatures. Nonlinearity in the *electric* domain plays no role, the temperature calibration makes it disappear. Handling thermal nonlinearity is treated in [4].

Zth curves

The first evident step to generalise our temperature measurement result is *normalising* it by the applied power. This normalised temperature transient is called Zth curve.

A fairly accurate temperature transient for any power step can be gained multiplying each time point in the Zth by the power. Figure 5 comes from Figure 4 dividing it by –44 W.

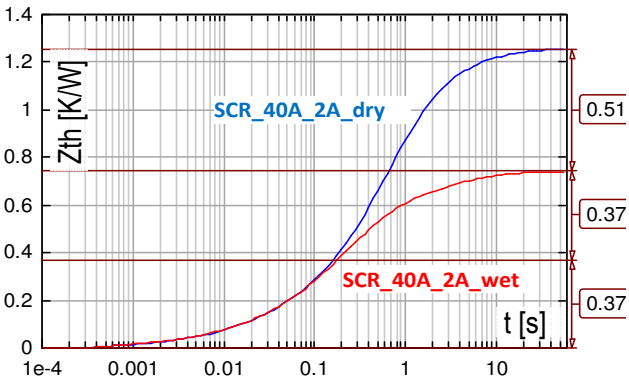

Figure 5 Zth curves, component on cold plate with different thermal interface

We can observe in the plot that until 0.37 K/W we proceed in the internal structures of the device, the Zth curves coincide. The arrangement shows 0.74 K/W total thermal resistance with the "wet" and 1.25 K/W with the "dry" thermal interface.

Experiments show that the Zth curves are always of "bumpy" nature. Two rational questions arise: *why* and *in which manner*? The next two sections formalise some answers.

Time constants

The presence of bumps is natural, at heating we can observe how we first heat up the chip, then internal package elements, afterwards the package body, the heat sink etc.

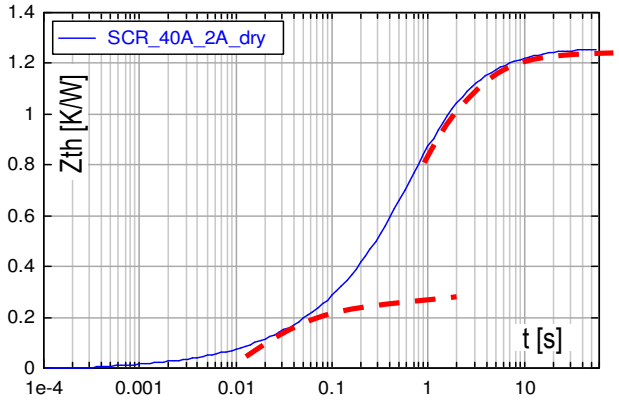

Figure 6 Zth curve and some of its exponential components

Such a curve can always be interpreted as a sum of exponential components (Figure 6). This exponential composition automatically yields a simple one-dimensional model, a chain of serial thermal resistance – capacitance pairs.

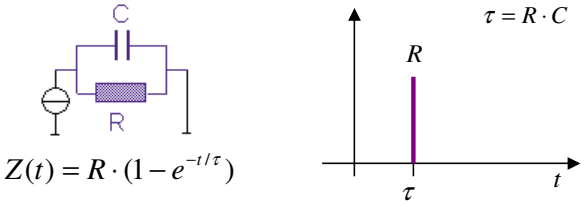

Figure 7 The simplest dynamic thermal model – a parallel thermal resistance and thermal capacitance

In the simplest case our system can be represented by a single thermal resistance expressing heat conductance and a parallel thermal capacitance expressing heat storage (Figure 7).

Applying power on this equivalent network the temperature quickly grows until $t=R \cdot C$ time, then gradually stabilises at $T=P \cdot R$ value following the $T(t) = PR \cdot (1 - e^{-t/\tau})$ time function. (In the analogous electric network power is replaced by current, temperature by voltage.) At 1W power we get the $Z(t)$ curve.

Composing now a Zth curve like the one in Figure 6 we have to sum up such exponential heating curves:

$$T(t) = \sum_{i=1}^{n} PR_i \cdot (1 - e^{-t/\tau_i}) \qquad (1)$$

The addition of temperatures corresponds to the chain model of Figure 8, the same power ("current") flows along the chain, and the total temperature ("voltage") is calculated as the sum of the components.

We could quantitatively describe the chain model with a large table of R_i and C_i pairs. For the visual representation it is practical to give the R_i and $\tau=R \cdot C$ values instead, because R gives direct information on the magnitude of the given component, and τ on the place of the "bump" along the time axis.

R_i and τ_i values are typically plotted in quasi – continuous

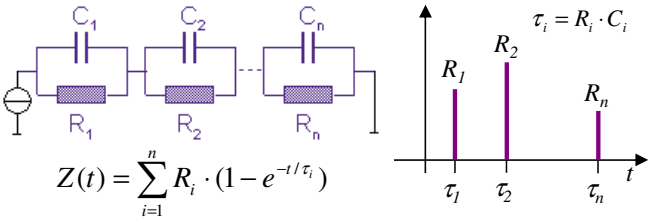

Figure 8 Chain model of parallel thermal resistance and thermal capacitance stages

graphs (*time constant spectrum*). This model is an important intermediate result but has no direct physical meaning.

With this methodology, as detailed in [1], we can create an RC network, which responds on an excitation just like the actual physical object. Theory of linear networks says that this network is not unique; many equivalent networks with different topology and RC values exist.

Structure functions

For building a physical model of the structure, we have to consider first the heat flow through a small portion of material.

As shown in Figure 9 there will be a temperature drop *between* two surfaces of the material. If the material has λ thermal conductivity and P power flows through the a and b surfaces they will have T_a and T_b temperatures, measured from the ambient. We can say that, if the slice has a small dx length and A surface, we see R_{th} thermal resistance between the a and b faces:

$$T_a - T_b = PR_{th} = P\left(\frac{1}{\lambda}\frac{dx}{A}\right), \qquad R_{th} = \left(\frac{1}{\lambda}\frac{dx}{A}\right) \qquad (2)$$

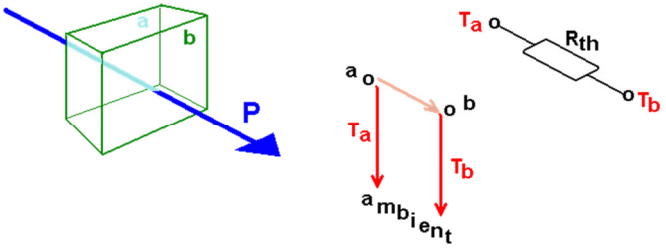

Figure 9 Heat flow through a material slice

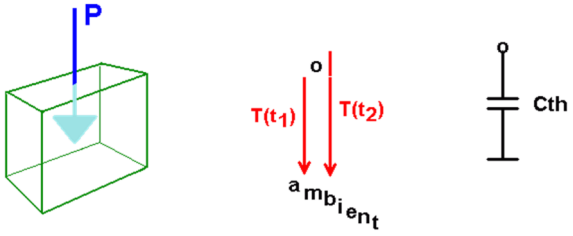

Figure 10 Heat flow into a material slice

On the other hand, the same material slice can store thermal energy (Figure 10). If we have a heat flow *into* the material then in a short $dt = t_2 - t_1$ time interval the energy change is

$$dQ = Pdt = C_{th}(T_2 - T_1) \qquad (3)$$

where $T_1 = T(t_1)$ is the temperature of the material at t_1 time and $T_2 = T(t_2)$ is the temperature of the material at t_2 time.

As T_1 and T_2 temperatures are again measured from the ambient (3) defines a C_{th} thermal capacitance between a point representing the material portion and the ambient. C_{th} can also be expressed through material parameters:

$$C_{th} = c \cdot m = c \cdot \rho \cdot dx \cdot A, \qquad C_{th} = c_V \cdot V = c_V \cdot dx \cdot A \quad (4)$$

(m – mass, c – specific heat, ρ – density, c_V – volumetric specific heat capacitance).

Building the heat conducting path of thin slices we create a ladder of lateral thermal resistances between two thermal nodes and thermal capacitances between a node and the ambient.

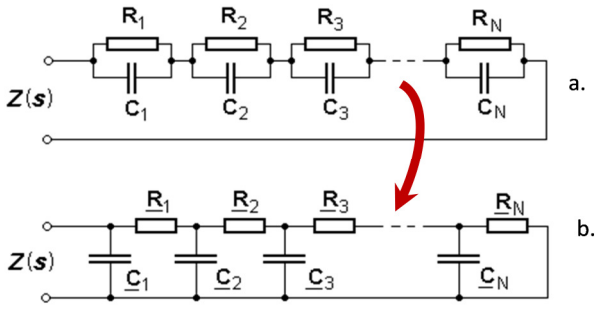

Figure 11 Foster network (a) to Cauer network (b) transformation: the way to a physical equivalent

Serial RC chains (Figure 8, Figure 11 a) can always be converted to RC ladders (Figure 11 b) by the Foster – Cauer transformation known in linear theory [1]. Doing these two processes; the exponential composition and the Foster – Cauer transformation in sequence we have a direct synthesis method for transforming measured transients into a one-dimensional physical compact model of the complex thermal system.

Instead of providing R and C values in tabular format we prefer again a graphic representation, the *structure function* (Figure 12). In this chart we sum up the thermal resistances in the ladder, starting from the heat source (junction) along the x-axis and the thermal capacitances along the y-axis.

This plot is an excellent graphic tool to analyse the heat conductance path. In *low gradient sections* a small amount of material having low capacitance causes large change in thermal resistance. These regions have *low thermal conductivity* or *small cross-sectional area*. *Steep sections* correspond to material regions of *high thermal conductivity* or *large cross-sectional area*. Sudden breaks of the slope belong to material or geometry changes.

Thus thermal resistance and capacitance values, geometrical dimensions, heat transfer coefficients, material parameters can be directly read on structure functions.

CASE STUDIES

Example 2. Converting the Zth curves of Figure 5 to structure functions we gain Figure 13.
Until 0.37 K/W we can see the sandwich-like internal structural details (die, solder, DBC). Physical dimensions, volumes and distances can be read in the chart knowing some material parameters, or thermal conductivity and specific heat can be determined knowing the geometry. After the junction to case separation point we see the heat spreading in grease and cold plate.

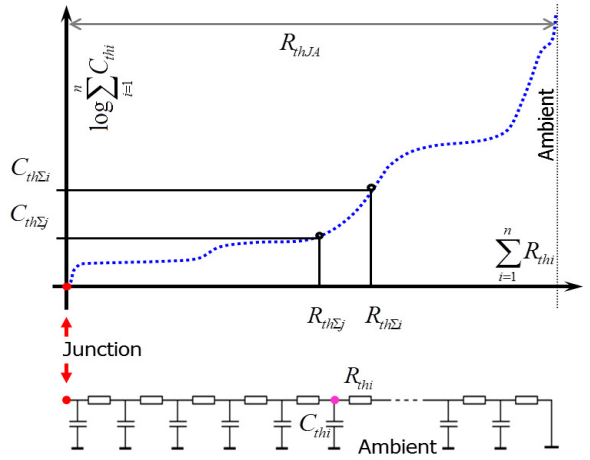

Figure 12 Structure function: the graphic representation of the thermal RC equivalent of the system

The air gap on dry surfaces adds 0.51 K/W to the junction to ambient total thermal resistance.

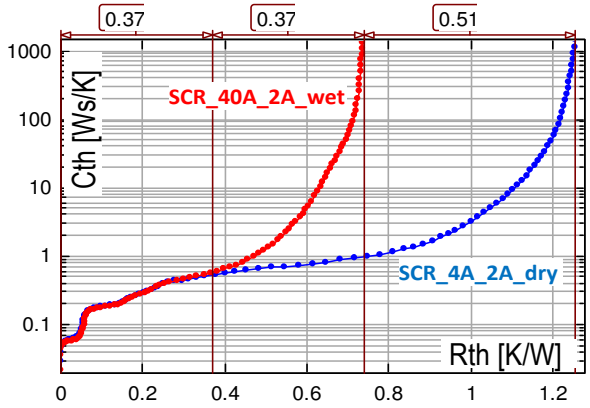

Figure 13 Structure functions: SCR at different boundaries

Example 3. Applying a soft thermal paste on the outer surface of the DBC we experience a significant improvement compared to the "dry" case. Repeating the power pulses of 60 s length, we see a continuous improvement (run-in) of the TIM layer (curves TIMA.01 to TIMA.30). After 20 cycles the layer stabilizes, we reach approximately the "wetted by thermal grease" boundary (Figure 14). Similar cases are treated in [8].

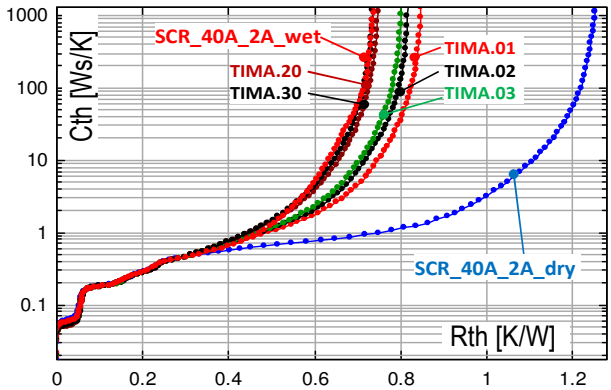

Figure 14 Run-in effect of a soft thermal paste

Example 4. In a desktop computer the Intel CPU is cooled by a large heat sink and a fan. The structure functions measured at three different fan speeds are illustrated in Figure 15.

After the steep early section belonging to the CPU package we can identify the TIM layer representing 0.12 K/W, to which the aluminium heat sink adds 0.28 K/W thermal resistance.

Three fan speeds are depicted (curves S1, S2, S3), the chart suggest that at a speed higher than S3 no further significant improvement can be expected, the convective section of the chart starts already from 94 J/K which corresponds to the full 38000 mm^3 volume of the heat sink.

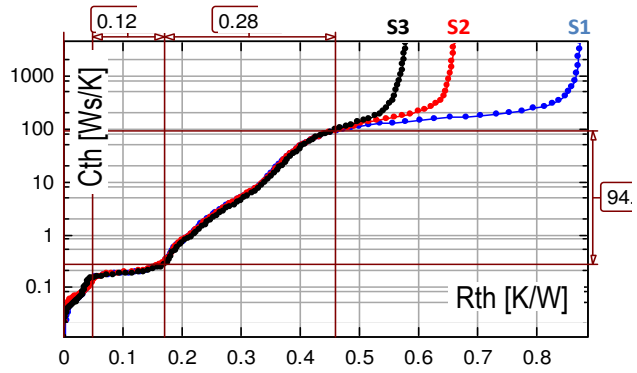

Figure 15 Structure function of a fan cooled CPU assembly at different rotational fan speed

STRUCTURAL ANALYSIS OF SOLID STATE LIGHTING APPLIANCES

Up to date lighting solutions are based on LED light sources which offer high reliability and long lifetime. However, good cooling is a principal requirement for these constructions because their excellent efficiency quickly diminishes at higher temperatures, unlike incandescent or fluorescent luminaires.

As all parameters of these light sources such as luminous flux, colour temperature, etc., are temperature and current dependent it is unavoidable to develop automated measurement arrangements for a complex characterization of the appliances in the electric, thermal and optical domain ([6][7]).

In these arrangements, first heating is applied by I_D current

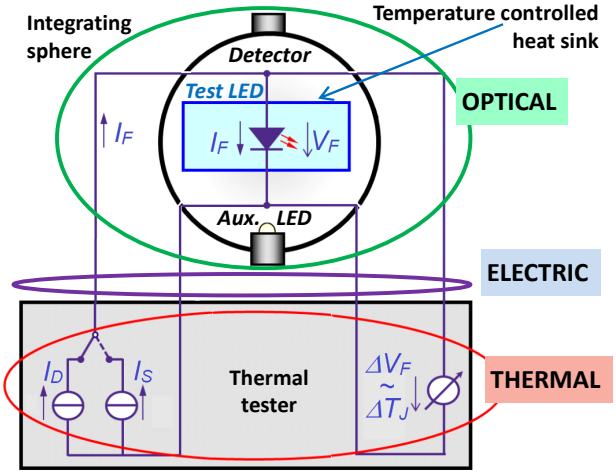

Figure 16 Combined thermal and radiometric/photometric test

and the optical parameters are stored after reaching steady state. Then a cooling transient (V_F~T_J) is recorded at I_S sensor current (Figure 16).

Due to the multiple energy transport in these devices (electric energy to heat and light), the data collected after heating correspond to the model shown in Figure 17.

As discussed in detail in [13], the standard diode model is split into a part depicting the carrier recombination process resulting in emitted photons ("left green diode") and another part generating heat ("right red diode").

The "left" diode outputs Φ_e light energy, also called radiant flux. The "right" diode produces $P_H = V_F \cdot I_F - \Phi_e$ heating power. The model in Figure 17 also considers the Joule heat in the diode and outer parts of a luminaire (R_S).

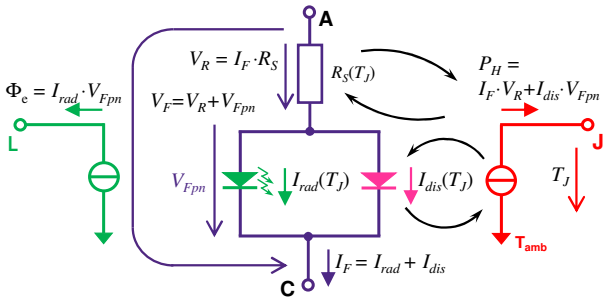

Figure 17 The multi-domain LED model proposed in [13]

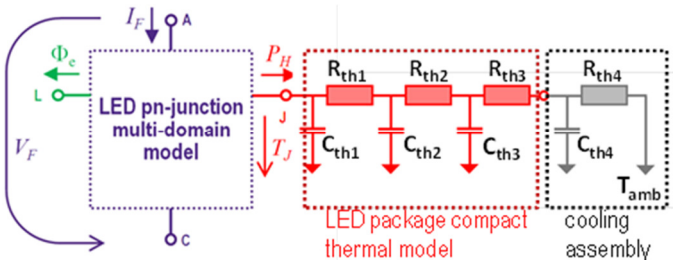

Figure 18 Heat conducting path of a LED assembly

The transient recorded after switching off the light source yields the compact RC model (Figure 18) of the LED and the cooling assembly, using the steps highlighted in previous sections. When producing Zth and the structure functions, only the residual P_H heating power has to be applied, of course.

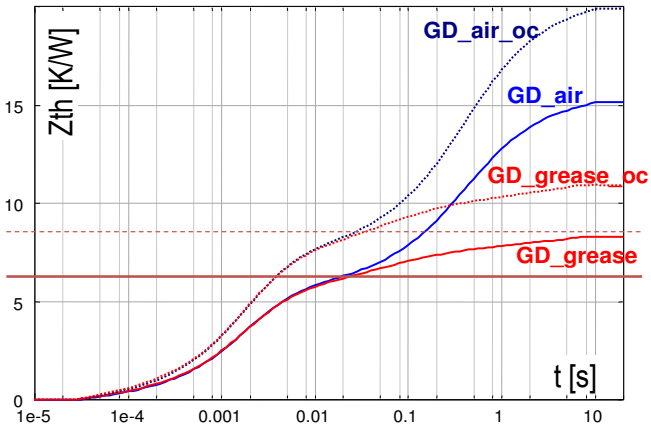

Figure 19: Z_{th} curves at two boundaries, with and without correction for the emitted optical power

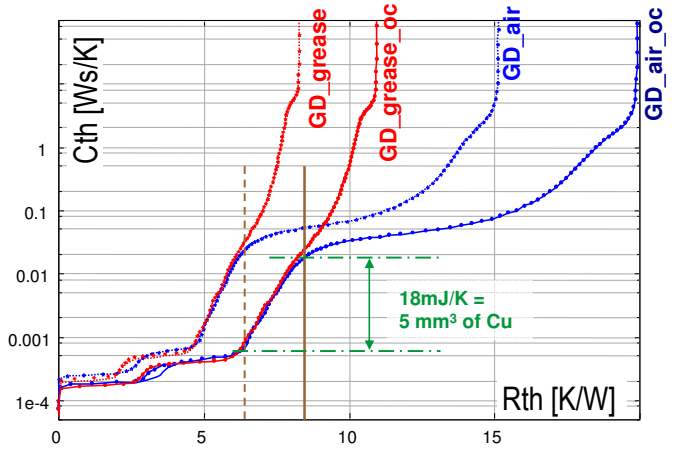

Figure 20: Structure functions, LED at two boundaries, with and without optical correction

Reducing the power by Φ_e is generally known as *optical correction* [11].

This correction is illustrated in the Zth curves of Figure 19 and structure functions of Figure 20. The charts were generated from a measurement of a high power LED on cold plate, with "dry (air gap)" and "wetted by grease" thermal interface.

The structural elements can be identified with their real resistance and size in the corrected charts only (dotted curves).

The junction to case thermal resistance can be read in both plots as 7.5 K/W. The steep section in the structure function corresponding to the cooling slug of the LED is 18 mJ/K long, equivalent to 5 mm^3 of copper, based on its specific heat.

CONCLUSION

In power electronics the classical concept of *Rth* thermal resistance is insufficient to describe a complex system. However, thermal transient measurement techniques can directly generate a valid and detailed structural equivalent from a single transient, including partial thermal resistances and subpart capacitances.

With the structure function technology, one can identify parts or failure locations. Moreover, the degradation of structural elements in a running system can be observed continuously, in a non-destructive way.

The transient measurement can record the temperature of the hottest point in the system ("junction"). The measured quantity can be any temperature dependent parameter of a semiconductor, e.g. a forward voltage.

A calibration step maps this voltage to junction temperature recording its value at different external temperatures.

For typical electronics with heat conduction and convection cooling, it is a sound assumption that the behaviour of the thermal system is linear. More precisely the material parameters of the components show only low dependence on temperature, and radiation plays no important role at typical component temperatures. Electric nonlinearity plays no role, the temperature calibration makes it disappear.

An equivalent behavioural model of a linear thermal system can be built of serial RC chains. The stages in the chain can be constructed by an exponential decomposition of heating or cooling curves. Converting the stages to RC ladders by the Foster – Cauer transformation we can directly synthesise a one-dimensional physical compact model of the thermal system.

The graphical representation of this model is the structure function, in which thermal resistance and capacitance values, dimensions and material parameters can be directly read.

All parameters of the light sources in solid state lighting systems, including luminous flux, colour temperature, etc., heavily depend on temperature and current. This makes necessary to develop automated arrangements measuring in the electric, thermal and optical domain. Combined measurements provide a model for LED sources reflecting the physical processes emitting light and generating heat.

The structural elements of light emitting systems can be identified with their real resistance and size in the optically corrected structure functions only.

ACKNOWLEDGEMENT

The LED testing/modelling work received funding in the context of the H2020 ECSEL project Delphi4LED (grant agreement 692465) [9] and co-financing for the Delphi4LED project by the Hungarian government through the National Research, Development and Innovation Fund.

REFERENCES

[1] V.Szekely:"Identification of RC networks by deconvolution:Chances and Limits", IEEE Trans. On Circuits and Systems – I: Fundamental Theory and Applications, Vol.45, No.3, pp.244-258, 1998.

[2] D. Schweitzer, H. Pape, L. Chen: "Transient Measurement of the Junction-To-Case Thermal Resistance Using Structure Functions: Chances and Limits", Proc. 24th SEMITHERM, San Jose, CA, 2008, DOI: 10.1109/STHERM.2008.4509389

[3] JEDEC JESD 51-14 Standard: Transient Dual Interface Test Method for the Measurement of the Thermal Resistance JTC … www.jedec.org/sites/default/files/docs/JESD51-14_1.pdf

[4] M. Rencz, V. Szekely: "Non-linearity issues in the dynamic compact model generation", Proc. 19th SEMITHERM, San Jose, CA, 2003, pp 263-270

[5] G. Farkas: "Thermal transient characterization of semiconductor devices with programmed powering", Proc. 29th SEMITHERM, San Jose, CA, 2013, pp. 248-255

[6] http://www.mentor.com/products/mechanical/products/t3ster

[7] http://www.mentor.com/products/mechanical/products/teraled

[8] A. Vass-Várnai, Z. Sarkany, M. Rencz: "Reliability testing of TIM materials with thermal transient measurements", 11th EPTC pp.823,827, 2009, DOI: 10.1109/EPTC.2009.5416437

[9] DELPHI4LED, http://delphi4led.org/consortium/, Accessed on March 21, 2017.

[10] C. Lasance, A. Poppe: "Thermal Management for LED Applications", Springer, 2014.

[11] G. Farkas, Q. van Voorst Vader, A. Poppe, Gy. Bognar, "Thermal Investigation of High Power Optical Devices by Transient Testing", IEEE Trans. on Components and Packaging Technologies, 28(1): 45-50 (2005), DOI: 10.1109/TCAPT.2004.843197

[12] P. Szabo; O. Steffens; M. Lenz; G. Farkas: "Transient junction-to-case thermal resistance measurement methodology of high accuracy and high repeatability", IEEE Trans. on Components and Packaging Technologies , 2005, Vol. 28, Issue: 4 pp: 630-636

[13] A. Poppe: "Multi-domain compact modeling of LEDs: an overview of models and experimental data", Microelectronics Journal 46(12A): pp. 1138-1151.