High-speed Cherry Hooper Flash Analog-to-Digital Converter

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Abstract

Purpose – The 60 GHz unlicensed band is being utilized for high speed wireless networks with data rates in the gigabit range. In order to successfully make use of these high speed signals in a digital system, a high speed analog-to-digital converter (ADC) is required. This paper presents the use of a common collector (CC) input tree and Cherry Hooper differential amplifier to enable analog-to-digital conversion at high frequencies.
Approach – The CC input tree is designed to separate the input Miller capacitance of each comparator stage. The CC stages are biased to obtain bandwidth speeds higher than the comparator stages while using less current than the comparator stages. The Cherry Hooper differential amplifier is modified to accommodate the low breakdown voltages of the technology node and used as a comparator. The comparator stages are biased to obtain a high output voltage swing and have a small signal bandwidth up to 29 GHz. Simulations were performed using foundry development kits to verify circuit operation. A two-bit ADC was prototyped in IBM's 130 nm silicon-germanium (SiGe) bipolar complementary metal–oxide–semiconductor (BiCMOS) 8HP technology node. Measurements were carried out on test printed circuit boards (PCBs) and compared with simulation results.
Findings – The use of the added CC input tree showed a simulated bandwidth improvement of approximately 3.23 times when compared to a basic flash architecture for a two-bit ADC. Measured results showed an effective number of bits (ENOB) of 1.18, from DC up to 2 GHz, whereas the simulated result was 1.5. The maximum measured integral non-linearity (INL) and differential non-linearity (DNL) was 0.33 least significant bits (LSBs). The prototype ADC had a figure of merit of 42 pJ/sample.
Originality/value – The prototype ADC results showed that the group delay for the Cherry Hooper comparator plays a critical role in ADC performance for high frequency input signals. For minimal component variation the group delay between channels deviate from each other, causing incorrect output codes. The prototype ADC had a low gain which reduced the comparator performance. The two-bit CC Cherry Hooper ADC is capable of achieving an ENOB close to 1.18 for frequencies up to 2 GHz, with 180 mW total power consumption.

Keywords Flash analog-to-digital converter (ADC), Cherry Hooper amplifier, Silicon Germanium (SiGe), heterojunction bipolar transistor (HBT), Software defined radio (SDR)

Paper type Research paper

1 Introduction

Analog-to-digital converters (ADCs) are key components for converting radio frequency (RF) signals into digital counterparts for signal processing. An example where high speed and large bandwidth are simultaneously required for direct signal processing is in software-defined radios (SDRs). In an SDR a large bandwidth is sampled in order to capture multiband services, reducing system size and cost (De Vito, 2013; Muñoz-Ferreras *et al*., 2011). The necessity for large bandwidth places stringent requirements on the ADC front-end and low speed ADCs are less suitable for such applications (De Vito, 2013; Arshad *et al*., 2013; Yuce *et al*., 2008). Flash ADCs provide the fastest sampling speeds and are therefore favored for applications such as SDR (Yuce *et al*., 2008). An important part of an ADC is the comparator, since it sets the achievable limit of the maximum bandwidth of the system. The comparator thus determines the effective resolution of the ADC and therefore the efficacy of the ADC. Therefore special care should be taken in comparator design to obtain a reliable high-speed ADC. A drawback of the flash ADC is that the large number of comparators at the input of the system creates a large input capacitance, which reduces the available bandwidth of the ADC. Care should thus be taken when designing the input network of a flash ADC.

The Cherry Hooper (C-H) amplifier is commonly used as a limiting amplifier for high-speed signals, exhibiting large gain and bandwidth (Razavi, 2003; Holdenried *et al*., 2004). The C-H configuration was consequently selected to operate as a comparator in a flash ADC. The common collector (CC) transistor configuration is a well-known unity gain amplifier configuration with large bandwidth, close to the transition frequency (f_t) of the transistor (Gray *et al*., 2001). Because of the unity gain, the CC amplifier does not suffer from the Miller effect and the effective input capacitance remains small. The use of CC input stages is therefore proposed to reduce the input capacitance of the C-H comparator stages. The 130 nm silicon-germanium (SiGe) bipolar complementary metal–oxide–semiconductor (BiCMOS) process from IBM was selected owing to the high f_t values of the heterojunction bipolar transistors (HBTs) and the use thereof in high-speed ADCs (Kobayashi *et al*., 2000). Section 2 describes the theory and conceptual design choices for the ADC design. Section 3 covers the detail on the circuit design while Section 4 depicts the simulated and measured results. The paper is concluded with Section 5 where the results are summarized.

2 Conceptual design

The ADC architecture consists of two main stages, the input tree and amplifier stages. A CC input tree was used to buffer the comparator stage and reduce the total input capacitance. The C-H amplifier is used for the ADC comparator due to its high bandwidth and degrees of freedom.

Figure 1 shows a block diagram depicting the input tree for an *n*-bit ADC. According to the well-known Miller theorem (Gray *et al.*, 2001), the effective input capacitance of an amplifier increases with the gain of the amplifier. Since the comparators are connected in parallel, the input capacitance of each input tree is added and creates a large total capacitance at the input of the ADC. This reduces the available bandwidth of the system. In order to overcome this problem, an input tree consisting of CC stages, is used. Only the parasitic capacitances of the first CC stage are therefore seen at the input of the ADC. This also separates each comparator's input capacitance from the rest of the ADC comparators, improving the bandwidth of the system.

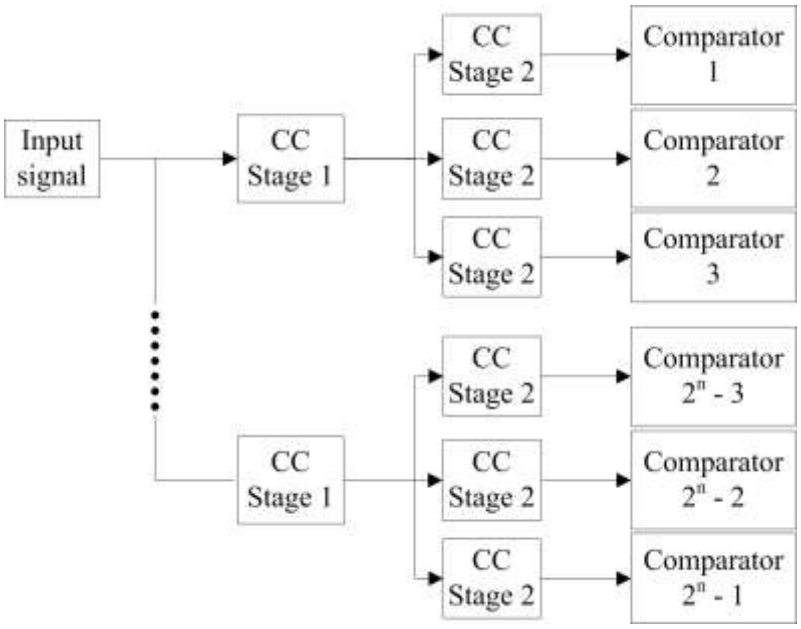

Figure 1. A block diagram depicting the input tree for an *n*-bit ADC

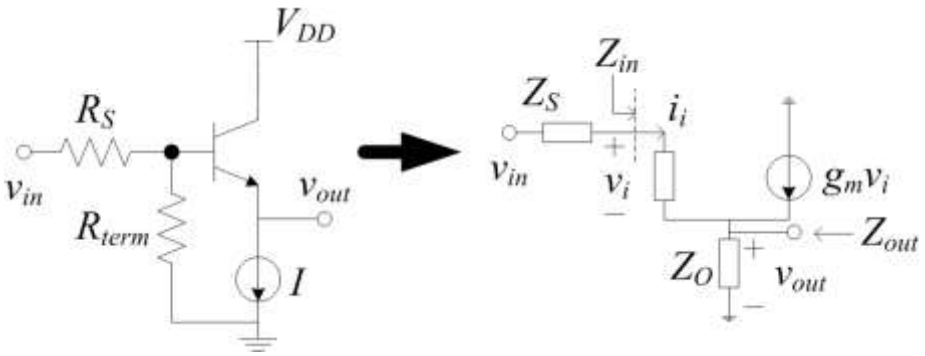

Figure 2. The circuit diagram for the first CC stage

3 Circuit design

3.1 Input buffer tree

Figure 2 shows the circuit diagram for the first CC stage. The output impedance, Z_O, includes the parasitic emitter resistance found at the emitter terminal of the HBT. Z_S similarly includes the parasitic base resistance found at the input terminal of the HBT. The impedance across v_i consists of the parallel combination of r_π and c_π, both dependent on HBT parameters. Using the HBT component values and $R_S = R_{term} = 50\ \Omega$, the voltage gain, dominant frequency pole and output resistance were calculated. The computed results for the complete CC tree are shown in Table 1.

Table 1 CC tree performance characteristics.

Parameter	Computed result
Low frequency gain	0.975 V/V
Dominant pole frequency	90.65 GHz
Output resistance	13 Ω

From Table 1 it is clear that the CC tree has a very high bandwidth and close to unity gain, as required. The output resistance is small, which reduces the time constant seen at each comparator input, thereby improving the system bandwidth.

3.2 Cherry Hooper comparator

The C-H amplifier configuration was used to serve as a comparator within the ADC. Assuming identical and matched transistors, half-circuit analysis can be used to determine the gain and bandwidth of the system. Referring to Figure 3, (1)-(4) is derived from the analysis of the half circuit using the pi-model for the transistors:

$$A = [g_{m1}g_{m3}h_{22}^{-1}z_1z_3Z_1]/[(z_1 + r_{e1}(\beta))(z_3 + R_S + \beta r_{e3})] \quad (1)$$

$$h_{22} = \frac{1}{R_1 + R_2} \quad (2)$$

$$h_{11} = R_F + \frac{z_\pi + R_1||R_2}{\beta + 1} \quad (3)$$

$$Z_1 = h_{11}||(z_2 + r_{e2}) \quad (4)$$

In (1)-(4), g_{m1} and g_{m3} are the transistor transconductance parameters, r_{e1} and r_{e3} are the parasitic emitter resistances, z_1 and z_3 are the parallel impedances from c_π and r_π of Q_1 and Q_3, R_S is the source resistance and h_{11}, h_{22} with Z_1 are feedback parameters. An advantage of the configuration shown in Figure 3 is that R_2 can be adjusted in order to increase the output voltage swing without considerably affecting the bandwidth, gain and overshoot of the comparator (Holdenried *et al.*, 2004). From (1), it is clear that the emitter resistance reduces the gain of the amplifier. Therefore a small emitter length is used to improve the gain of the circuit. Increasing the emitter length of the HBTs also increases the parasitic capacitance, which in turn reduces the available bandwidth of the ADC, reinforcing the choice for a small emitter length.

The HBTs within the 8HP process from IBM have high f_t values, which are favorable to allow a high bandwidth for the system. A drawback of the 130 nm technology node is that the breakdown voltages of the transistors are small and the C-H configuration requires relatively large supply rails due to the number of components stacked in the configuration.

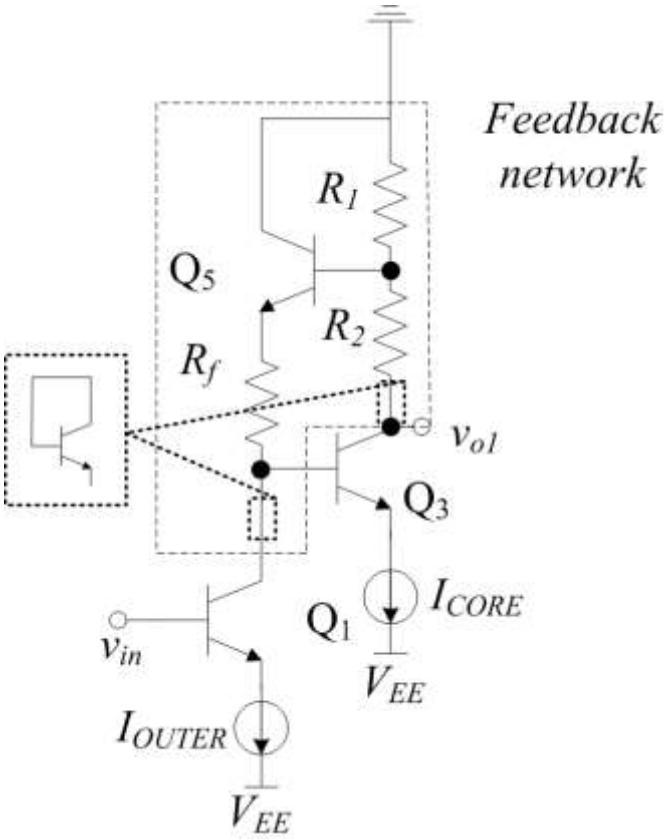

Figure 3. The analysis of the half circuit using the pi-model for the transistors

Care has to be taken in the design to prevent the transistors from entering breakdown. Diode-connected HBTs were placed at the collectors of the input transistors to prevent voltage breakdown over the collector-emitter terminals. The diode-connected HBTs add to the parasitic capacitances and resistances at the respective nodes. The parasitic capacitance is related to the technology node and is therefore relatively small for small device sizes. The resistance seen by the input stage due to the diode connected transistor is shown in (5).

$$R_{out} \approx \alpha/\mathrm{g}_m||r_O \tag{5}$$

In (5), $\alpha = \frac{\beta}{\beta+1} \approx 1$, r_O is the internal output resistance of the transistor and $r_O \gg \alpha/g_m$. Consequently the addition of the diode-connected transistors has a small effect on the gain and bandwidth since the resistance and parasitic capacitance is small. Figure 4 shows the CC tree and single comparator circuit diagram.

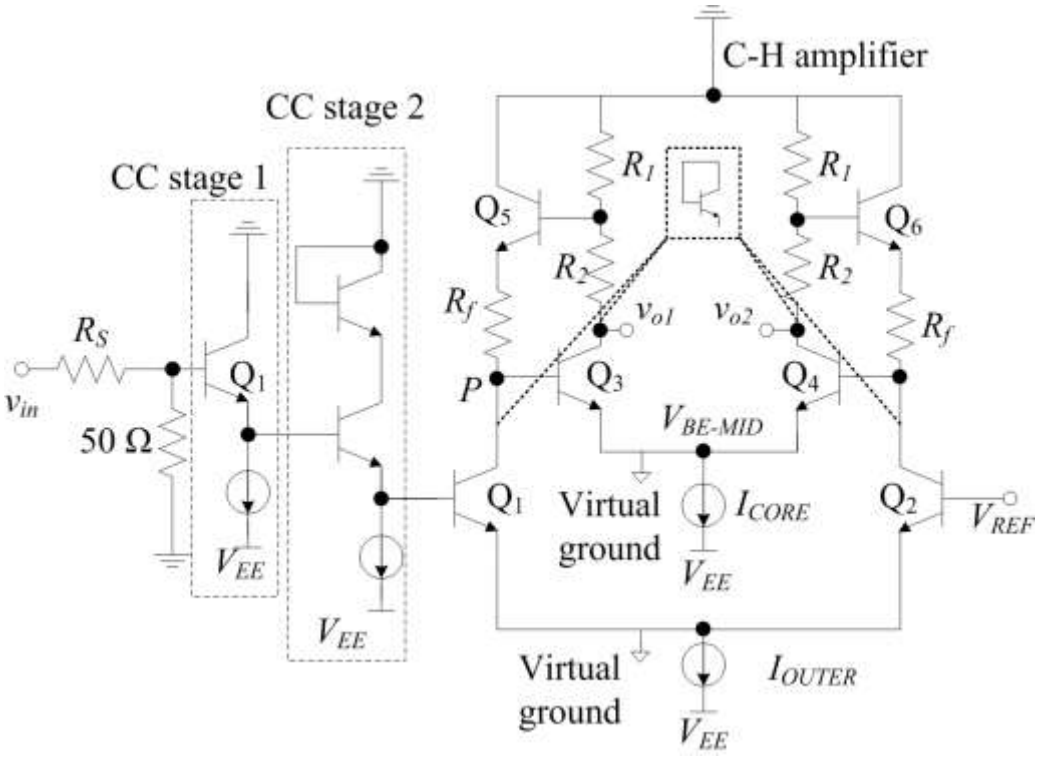

Figure 4. The CC tree and single comparator circuit diagram

4 Results and discussion

This section describes the simulation and measurement results. Matlab is used to theoretically simulate (1) described in Section 3. Spectre in Cadence Virtuoso was used to simulate the ADC and the design was prototyped on a multi-project wafer (MPW) IC run.

4.1 Simulation setup and results

In order to verify the mathematical model of the system, (1) was simulated in Matlab. Figure 5 shows the Matlab plot result for (1), as well as the AC response generated by Cadence Spectre. The -3dB cut-off point resides close to 29 GHz for both simulations.

Both plot results are similar for the cut-off frequency and low frequency gain. The Matlab theoretical response exhibits early and slower gain roll-off. This is due to the theoretical results using estimates for the gain factor, β, parasitics and ignoring the loading effects of each current source. Virtuoso uses the vertical bipolar intercompany (VBIC) model for HBTs and incorporates a technology file for the 130 nm process from IBM. The VBIC model is an improvement on the standard Gummel-Poon or pi-model and predicts HBT performance more accurately. This technology file also includes device and process parasitics within the specific technology node. Using both these parameters, Virtuoso is able to predict circuit performance more accurately than the textbook pi-model which was used to derive (1).

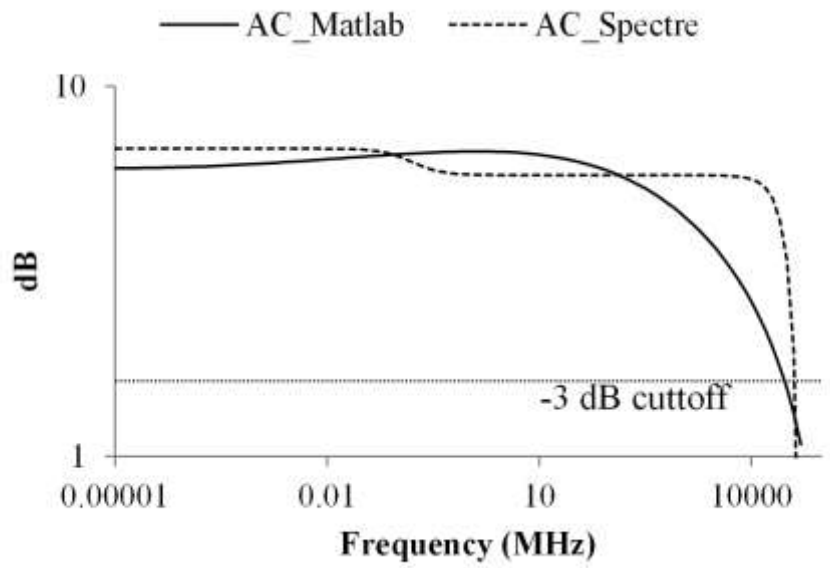

Figure 5. The Matlab plot result

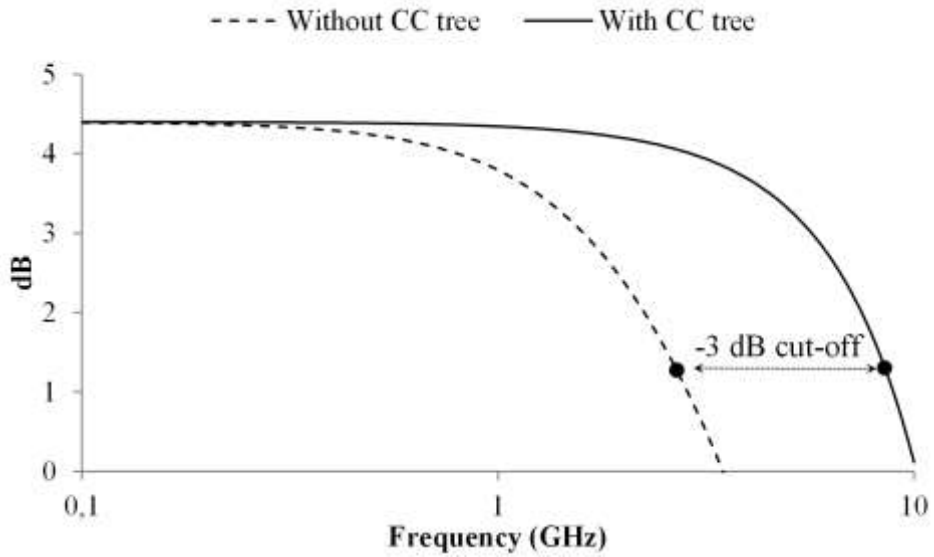

Figure 6. The simulation results performed on a basic flash ADC setup as well as the proposed circuit

In order to show the bandwidth improvement by using the CC input tree network, a simulation is performed for a standard two-bit flash ADC setup and plotted alongside the proposed architecture. Figure 6 shows the simulation results performed on a basic flash ADC setup as well as the proposed circuit.

A capacitance of 1 pF was added in front of each comparator, since the total effective capacitance of the three comparators is fairly small. A bandwidth improvement of approximately three times is visible from simulations.

The AC simulations only indicate the bandwidth at which the proposed circuit is able to amplify input signals. For an ADC, the time-domain simulation results provide a better measure of comparator switching performance, since the AC results do not provide out-of-band spurs and signal distortion. Spurious free signals are an important part of an ADC and need to be accounted for. Time-domain simulations were therefore performed at different frequencies for a complete two-bit ADC. Figure 7 shows the time-domain simulation output for a single comparator. The input signal was a 5 GHz sinusoidal signal with an offset of -300 mV with an amplitude of 300 mV. The reference voltage was tied to -300 mV. An output differential voltage swing of 400 mV was selected in the design and can be seen in Figure 7. Clear digital outputs can be seen in Figure 7, indicating key comparator performance at 5 GHz.

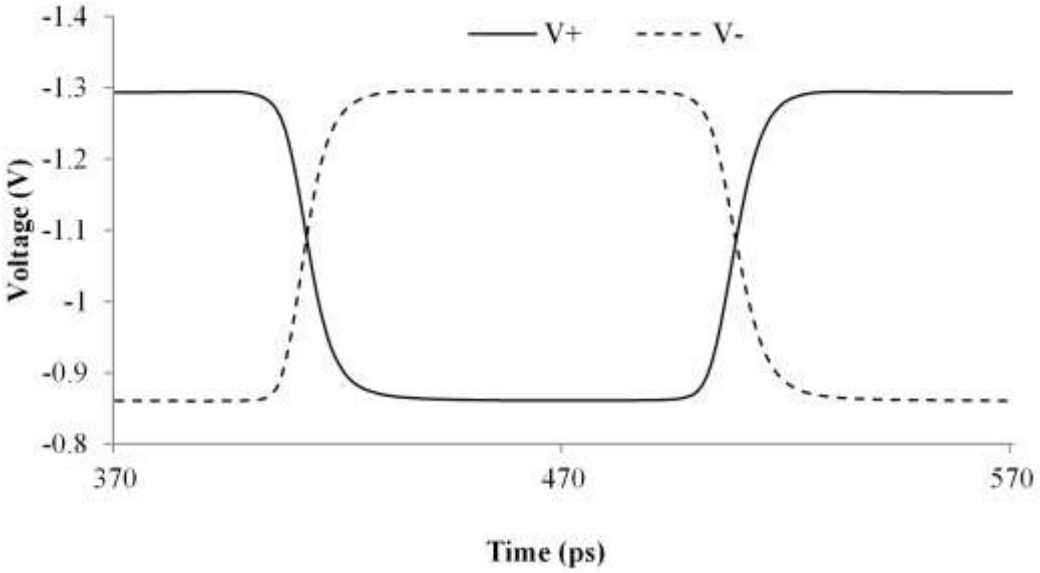

Figure 7. Clear digital outputs can be seen indicating key comparator performance at 5 GHz.

Table 2 provides a summary of various high performance comparators in relation to the current C-H design, with an added input tree. The CMOS comparator in Lu and Holleman (2013) trumps the comparator in this work with all the specifications and is aimed at improving the comparator sensitivity. The design was fabricated in a 500 nm technology node and only used CMOS transistors. Typically HBTs are able to operate at higher frequencies than CMOS transistors but with higher power consumption. This is clear from the results shown in Table 2 when compared to the current C-H design. The comparator presented in Ryman *et al*. (2013) shows better power consumption and gain, but occupies a larger chip area and has a reduced bandwidth. For this design there was a trade-off between the gain and bandwidth and therefore the design had a lower bandwidth when compared to the presented C-H design. The increased chip area is due to an 8-channel implementation and the topology of each comparator. The comparators in WenWei and Qiao (2014) and Kuo *et al*. (2005) have improved gain performance and a smaller active area than the current C-H design, but have a smaller bandwidth and output swing. The designs of both are similar utilizing cascaded gain stages, each with high bandwidth to improve the overall gain. This results in a reduction in the overall bandwidth of the system. WenWei and Qiao (2014) implemented active inductors in order to improve

sampling speeds and used a different technology node which resulted in improved performance. It must be noted that the comparators in Table 2 are latched comparators and the current C-H design does not include clocking circuitry. Including clocking circuitry will increase power consumption and the active area occupied by the C-H comparator.

Table 2 C-H comparator comparison to state-of-the-art comparators.

Parameter	(Lu and Holleman, 2013)	(Ryman *et al*., 2013)	(WenWei and Qiao, 2014)	(Kuo *et al*., 2005)	This work
Technology	500 nm CMOS	130 nm SiGe	180 nm SiGe	200 GHz SiGe	130 nm SiGe
Supply	5	-3.3 V	3.3 V	3.5 V	-3.3 V
Power consumption	5.65 µW	48 mW	28 mW	405 mW	87 mW
Gain	29.54 dB	42 dB	40 dB	11 dB	6 dB
Bandwidth	33 MHz	3.3 GHz	22 GHz	18 GHz	29 GHz
Input offset	50.57 µV	+/- 5 mV	N/A	< 8.4 mV	17 mV
Output swing	5 V	100 mV	~ 10 mV	~ 40 mV	400 mV
Active area (mm^2)	0.064	1.9	0.0053	0.0226	0.027

4.2 Experimental results

The ADC was prototyped in the 130 nm SiGe 8HP BiCMOS process from IBM. The project was part of a MPW run administered by MOSIS. A two-bit ADC was selected to validate the principles presented in this paper. Figure 8 shows the two-bit ADC on the shared chip die. Pads were made available for all inputs and outputs of the ADC.

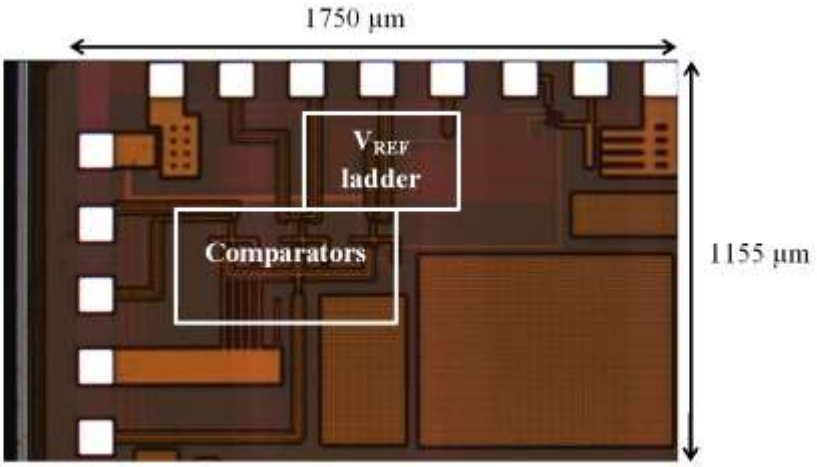

Figure 8. The two-bit ADC on the shared chip die

4.2.1 Measurement setup

Various test modules were designed and developed in order to test the two-bit ADC performance. An alumina substrate was used for three different test boards and these test boards were each enclosed in an aluminum (Al) box. The alumina substrate was selected since it has better performance characteristics at higher frequencies, when compared to standard FR4 material. An Al test box was used to reduce interference from unwanted RF signals. Additionally, a test board was developed on FR4 printed circuit board (PCB) with SMA connectors for the inputs and outputs. The alumina test boards were used to measure the integral non-linearity (INL), differential non-linearity (DNL) and time-domain measurements for the two-bit ADC. Figure 9 shows the alumina substrate test boards in the Al boxes.

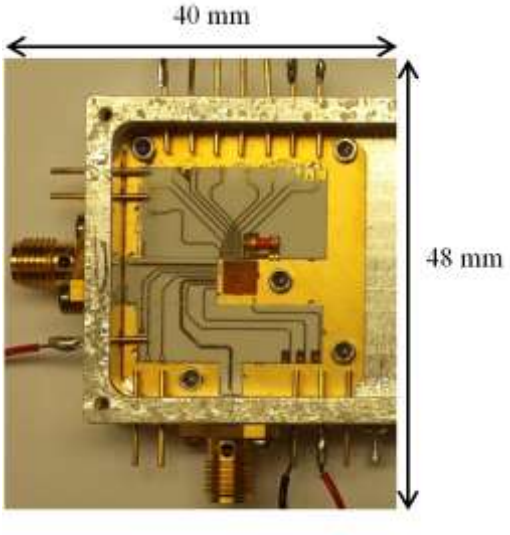

Figure 9. The alumina substrate test boards in the Al boxes

For the alumina test boards, SMA connectors were used to terminate the input signals. Short test probes were placed in the Al box to measure outputs and provide inputs to the other parts of the system. Three power supplies were used to provide input power to the system, as well as input offsets and the reference voltage. A high-speed oscilloscope with an analog bandwidth up to 4 GHz, from Tektronix, was used for time domain measurements. A logic analyzer was used to perform digital measurements on the test boards.

4.2.2 Two-bit ADC measurement results

Four different chip dies were measured and ADC characteristic data were subsequently computed. One test board was designed for DC tests to determine the static performance of the ADC. The other three were AC-coupled for high-frequency measurements. Table 3 shows the INL and DNL performance measured with the DC-connected ADC. The INL and DNL offsets are due to the low gain and large signal behavior of the C-H amplifier. The low gain of the amplifier causes the outputs to have a slow slew rate and thereby only achieve maximum output levels for a large difference between the differential inputs. This effect is further aggravated due to the large signal behavior of the C-H amplifier. As shown in Holdenried *et al*. (2004), for large signal performance the collector voltages of the input stage must be a lot larger than V_t for proper output switching performance. To improve the slew rate, the amplifier gain can be increased or an additional gain stage can be used at the cost of additional power consumption and bandwidth. Figure 10 shows the time-domain measurements for a sinusoidal input of 100 MHz on the FR4 test board. Bit 0 indicates the output of the least significant bit (LSB) comparator and Bit 2 the most significant bit (MSB) comparator.

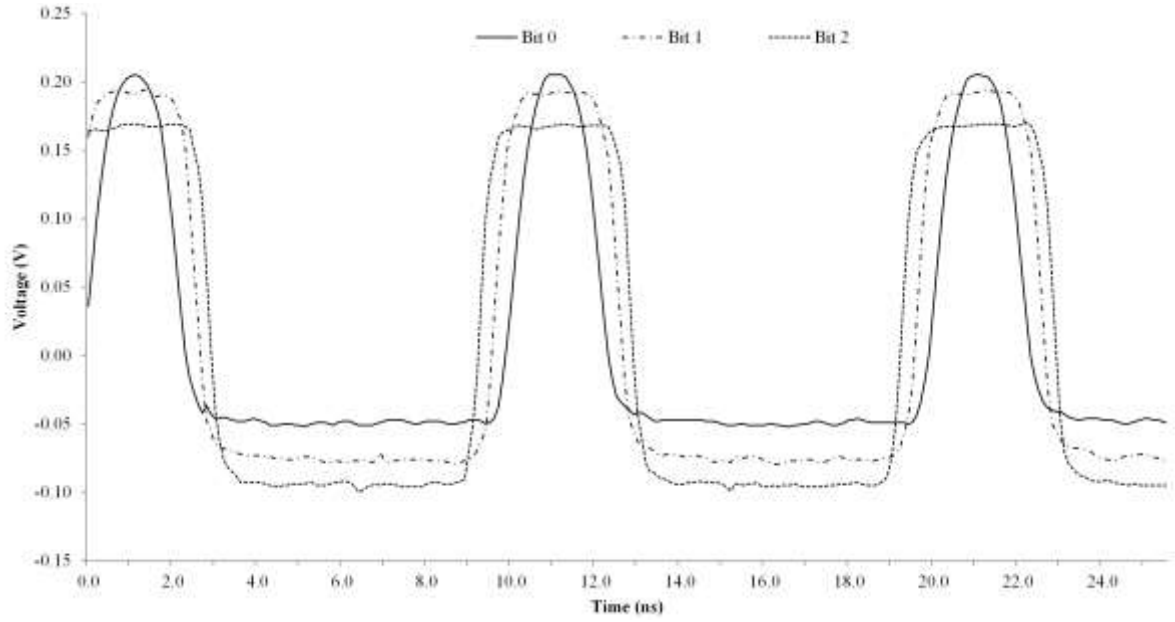

Figure 10. The time-domain measurements for a sinusoidal input of 100 MHz on the FR4 test board

From Figure 10 it is clear that the three outputs switch at the different voltage reference levels (ΔV_{ref} = 75 mV, V_{REF} = 0.3 V). The voltage levels are smaller than 400 mV because of the loss in the capacitive coupling to the oscilloscope and non-ideal matching network. Figure 11 shows the outputs measured on the alumina substrate for an input signal of 1.5 GHz. It is clear from Figure 11 that the

output waveforms start to distort and there is a delay between output waveforms. In order to determine delays between output signals, group delay simulations were performed on the two-bit ADC. Resistors R_1, R_2 and R_f were selected to deviate from ideal, for the LSB and MSB comparators.

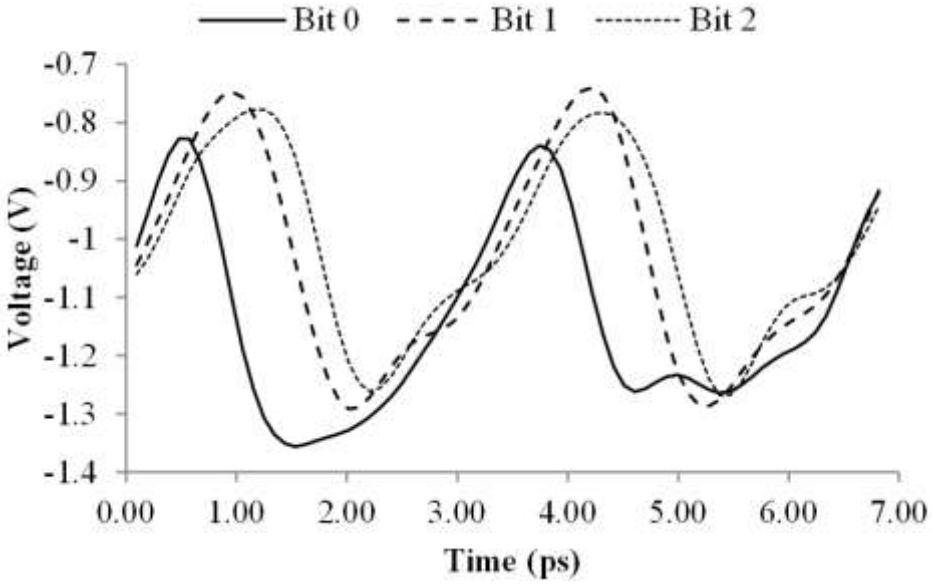

Figure 11. The outputs measured on the alumina substrate for an input signal of 1.5 GHz

The resistors for the MSB comparator had an increased value of 20% from ideal whereas the LSB comparator resistors had a decreased value of 20% from ideal. The group delay simulation results are shown in Figure 12.

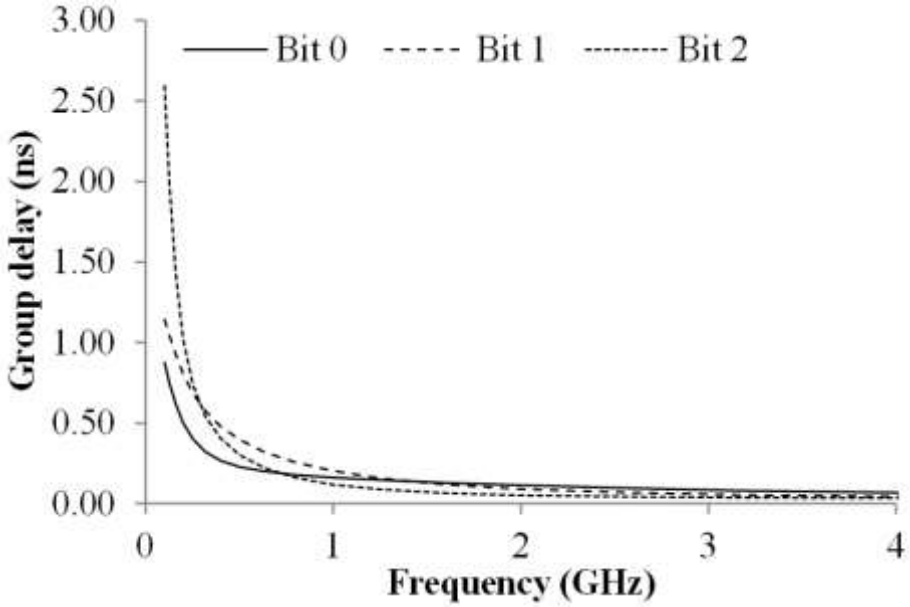

Figure 12. The group delay simulation results

From the results in Figure 12 large differences between comparator group delays are present at frequencies below 1 GHz. For frequencies above 1 GHz the difference between the group delays of each comparator reduces, but does not converge to the same value. For low-frequency signals the effect of the simulated group delay is minimal since it is much lower than the period of the operating frequency. The group delay for high-frequency signals will in turn have a large effect on performance, which is clearly visible in Figure 11. Figure 13 shows the outputs in Figure 11, but with the delay between each comparator removed. This indicates that each comparator switches at different reference voltages, but due to the delay between each channel, the measured output differs considerably from ideal.

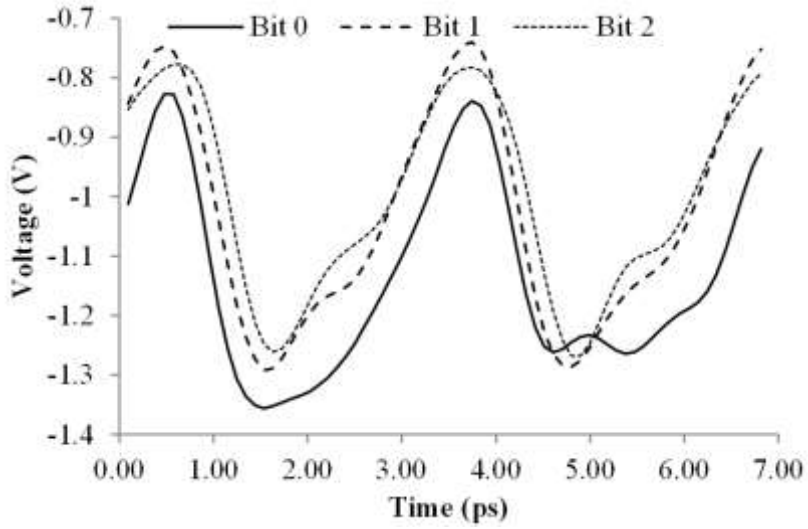

Figure 13. The outputs in Figure 11, but with the delay between each comparator removed

In order to measure the ENOB of the ADC a logic analyzer was used to capture the digital data for frequencies below 500 MHz. For higher frequencies a high-speed analog oscilloscope was used to measure time domain results. The sine-wave fit test method described in the IEEE standard for terminology and test methods for analog-to-digital converters were used to evaluate the ENOB of the ADC (Anon., 2011). The logic analyzer had a bandwidth of 500 MHz and digital acquisition of data was only performed up to this frequency. The reduction in ENOB close to 500 MHz was due to an increase in incorrect output codes obtained using the logic analyzer. This was attributed to the fact that the limits of the logic analyzers' bandwidth had been reached. The digital data was exported and processed within Matlab. A sample and hold circuit was used in conjunction with the two-bit ADC to facilitate sampling. Two synchronized signal generators (using 10 MHz reference clocks for synchronization) were used to generate the input and clock frequencies. For high-frequency signals, measurements were performed using the analog oscilloscope and the data was exported to be processed within Matlab with a selected threshold voltage. Figure 14 shows the simulated and measured ENOB of the ADC, up to 2 GHz. The reduction in ENOB is due to the gain difference in comparator stages, device mismatches and group delays through each channel. This causes invalid ADC outputs to occur thereby increasing the bit-error rate and reducing the ENOB.

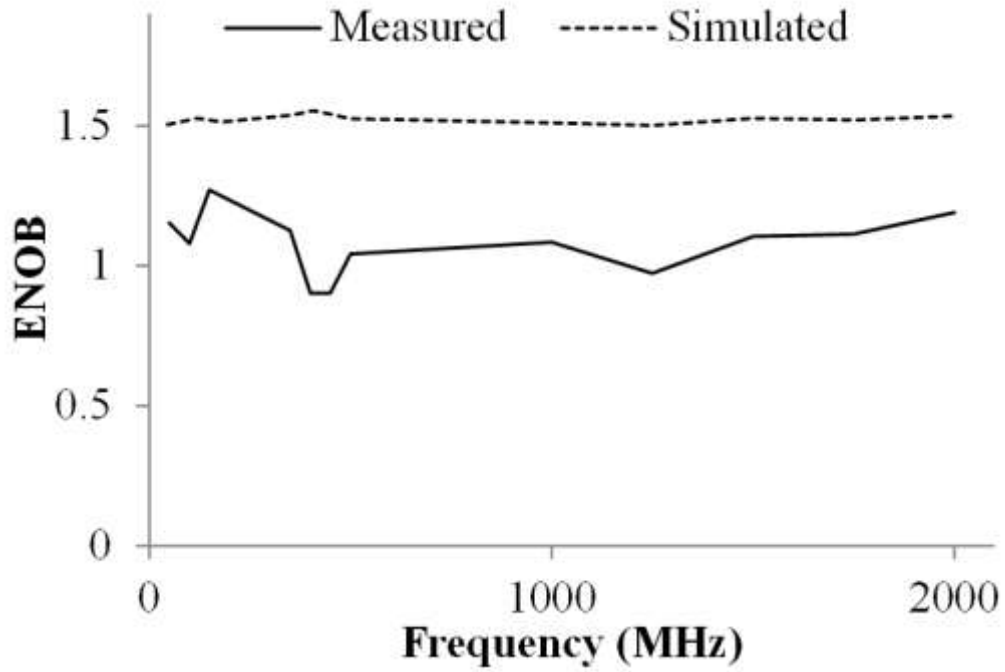

Figure 14. The simulated and measured ENOB of the ADC, up to 2 GHz

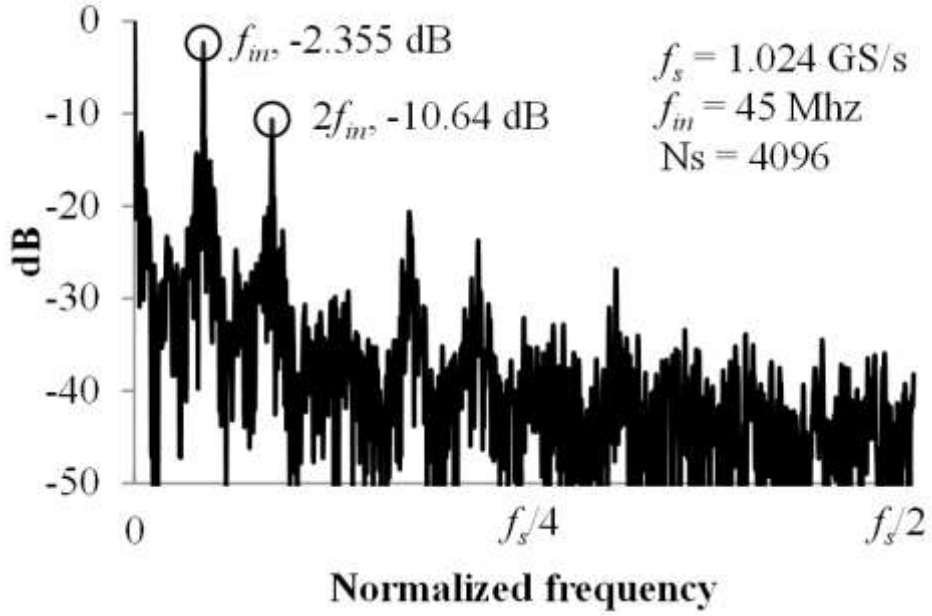

Figure 15. The fast Fourier transform (FFT) of the ADC output after the data has been processed within Matlab

Figure 15 shows the fast Fourier transform (FFT) of the ADC output after the data has been processed within Matlab. The relatively large harmonic is present due to the fact that the ADC only has a resolution of two bits. For higher resolution ADCs the unwanted harmonics reduce since the input sine wave is reproduced more accurately. Table 3 shows other important ADC characteristics compared to

other high-speed flash ADCs in literature. The figure of merit (FOM) was calculated using the measured bandwidth of the system.

Table 3 Comparison of ADC characteristics.

Parameter	This work	(Chu *et al.*, 2010)	(Kertis *et al.*, 2009)	(Shahramian *et al.*, 2009)	(Yi *et al.*, 2012)
Technology	130 nm SiGe	130 nm SiGe	130 nm SiGe	180 nm SiGe	130 nm CMOS
Bits	2	4	5	4	3
ENOB	1.19	3.5	4	3.7	N/A
Bandwidth	2 GHz	N/A	> 20 GHz	8 GHz	4.3 GHz
INL	0.33 LSB	< 1 LSB	< 0.05 LSB	< 0.5 LSB	0.11 LSB
DNL	0.33 LSB	N/A	< 0.05 LSB	< 0.5 LSB	0.18 LSB
Power consumption	180 mW	2.1 W	4.8 W	4.5 W	63 mW
FOM	42 pJ/sample[1]	10 pJ/sample	~11 pJ/sample[1]	~9 pJ/sample[1]	2.2 pJ/sample

1. Value estimated and/or rounded to closest integer.

4.3 Discussion

Simulation results gave an indication of analog-to-digital conversion up to 5 GHz with minimal overshoot and distortion. The AC simulation results showed a -3 dB bandwidth larger than 20 GHz, as well as an improvement when the CC input tree was used. Time-domain simulation results also showed minimal distortion up to 5 GHz with sinusoidal input test signals.

Measurement results did, however, differ greatly between the theoretical and simulation results. The -3 dB ADC bandwidth was estimated from DC - 2 GHz, but the measured signal showed increased distortion from 1.5 GHz. Time domain and frequency measurements show that the outputs are capable of high speed switching but incorrect output codes are observed due to the output codes not reaching maximum values and different group delays occurring through each ADC channel. The incorrect output codes reduce the ENOB dramatically. In order to improve the measured ENOB each ADC comparator channel must be identical in order to reduce the group delay between each channel. The gain must also be increased in order to improve the comparator sensitivity. The erroneous output codes are caused by the low gain causing the outputs not to achieve full swing and are also due to different group delays through the different comparators. The reduced measured bandwidth and signal distortion may be caused by improper input/output matching and measurement board parasitics. Due to the lower breakdown voltages an input CC tree of only 2 stages was used to ensure safe device operating voltages. This led to a maximum input voltage up to 1.2 V_{p-p} with a power dissipation of 180 mW.

5 Conclusion

A two-bit ADC with C-H comparators and a CC input tree is presented in this paper. The performance critical aspects of the ADC are presented and discussed. A CC input tree is proposed in order to improve the bandwidth of a flash ADC. The C-H amplifier was used as a comparator and its performance was theoretically characterized and provided, with and without, the CC input tree modification. From the measurement results it can be seen that high-speed analog-to-digital conversion up to 1.5 GHz can be performed. The ENOB was measured to be 1.19 up to 2 GHz. The two-bit ADC prototype's power consumption was 180 mW with a FOM of 42 pJ/sample. The prototype, with I/O pads, occupied an area of approximately 1.2 mm^2.

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