Electroluminescence From Two Junction Punch Through Structures in Silicon Nanowires

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***Abstract*— Hot carrier electroluminescence in two junction devices under punch through conditions manufactured in silicon on insulator nanowires are investigated. Of interest is the spectral content of the light emission, as well as the external power efficiency and the light extraction efficiency. An order of magnitude improvement in external power efficiency was achieved relative to a bulk silicon p-n junction in avalanche.**

***Index Terms*— SOI, silicon electroluminescence, nanowire, hot carriers.**

I. Introduction

Avalanche electroluminescence from silicon p-n junctions under reverse bias has been known for some time [1], but only during the last two decades some novel applications for this technology have been proposed [2]–[5]. Since silicon is an indirect band gap material, the internal quantum efficiency of electron to photon conversion is quite low. Other drawbacks of especially the avalanche mode of operation, are fairly large operating voltages and high internal electric fields. In this letter we introduce a technique to improve on the performance of avalanche electroluminescent devices. This technique involves the following; 1) dual junctions in back-to-back configuration, 2) operating the device in a punch through mode, and 3) placing the light emitting region in a silicon nanowire. Using these methods the operating voltage will be decreased (for improved power efficiency), long wavelength emission will be increased and the light extraction efficiency will be increased compared to bulk CMOS avalanche electroluminescence. In this letter we describe two terminal dual junction punch through devices (n^+pn^+) formed in silicon nanowires with diameters smaller than 60 nm. These devices were manufactured in a custom designed SOI (silicon on insulator) process.

II. Device Structure

A. Punch Through Devices

The typical two terminal punch through device diagram is depicted in Fig. 1 for different junction separation distances, with the electric field E distribution for each case also shown. In this configuration the first junction *J1* will be reverse biased and the second junction *J2* will be forward biased. In our study the junction separation distance d_{PT} was varied in the range from 250 to 600 nm. As the applied voltage is increased, the depletion region around *J1* will spread into the lightly doped p-region base towards junction *J2*. If the distance d_{PT} is too large, the junction *J1* can go into the avalanche breakdown mode before its depletion region reaches the narrow depletion region around forward biased junction *J2*. This will then be the normal avalanche region of operation. However, for shorter d_{PT}, the p-type region gets fully depleted as the depletion region around the junction *J1* spreads into the lightly doped p-type region and reaches the narrow depletion region formed around the forward biased junction *J2*. When this happens, the punch through condition has been reached. The result is that the energy barrier of the forward biased junction *J2* that prevents the diffusion current to flow is lowered by the approaching electric field distribution from the reverse biased junction *J1*. This will cause electrons to be injected across the forward biased junction into the electric field of junction *J1*. These carriers will then drift across the p-type base as a result of the electric field set up by the reverse bias across *J1*. The advantage of this situation is that large amounts of carriers will be injected into the high electric field without any carrier multiplication through avalanching. The electric field in the area where light is being generated in the device can thus be varied by varying the distance d_{PT} as shown in Fig. 1.

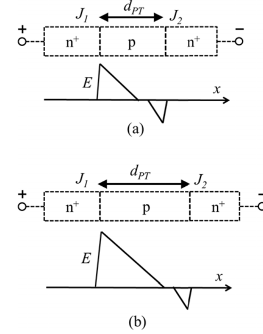

Fig. 1. The electric field distribution E in punch through n^+pn^+ devices with (a) short separation distance and low electric field, and (b) longer separation distance and higher electric field.

B. SOI Technology

The punch through p-n junctions were formed in a thin active silicon layer using a custom SOI process. The device structures are shown in Fig. 2. Two types of devices were

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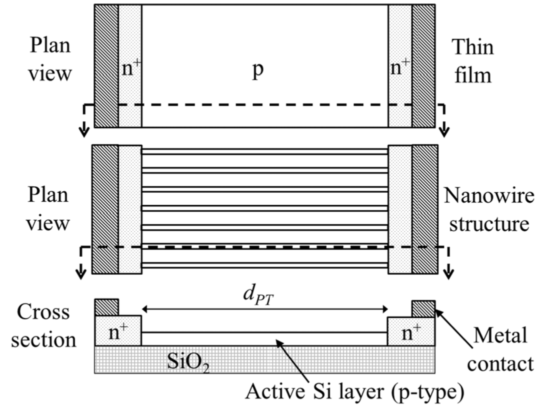

Fig. 2. The SOI thin film and nanowire structures.

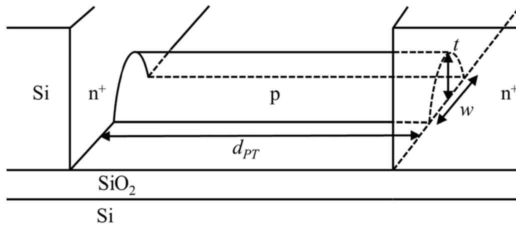

Fig. 3. The SOI (silicon on insulator) nanowire device structure.

realized, namely a device using a continuous thin film of active silicon, and a second device where the active layer is patterned into a large number of parallel nanowires. The cross sectional areas of the two types of devices were designed equal, so that at the same bias current they will have the same current densities and therefore the same carrier concentrations.

A typical nanowire device structure is shown in Fig. 3. The thicker n^+ silicon islands have an active silicon layer thickness of approximately 80 nm. These n^+ island regions are covered by a silicon nitride layer, and a selective oxidation technique is used to thin the p-type nanowires between the two n^+ islands to the required thickness. This technique of manufacturing nanowires on a SOI substrate is based on the oxidation method proposed earlier [6].

The nominal final active layer thickness is in the region of 40 nm. During the thermal oxidation the width of the nanowires are also reduced. This is illustrated in the scanning electron microscope (SEM) image of Fig. 4 where the nanowires are shown before and after the thermal thinning oxidation cycle. The nanowires have a nominal width w of 80 nm and a nominal thickness t of 40 nm. The final thermal silicon dioxide layer encapsulating the nanowires is approximately 30 nm thick. Although thin films or small diameter silicon nanowires on SOI can lead to a quasi-direct band-gap semiconductor due to the quantum mechanical confinement effect [7], for this process both the film thickness and nanowire diameter are too large for this effect to occur.

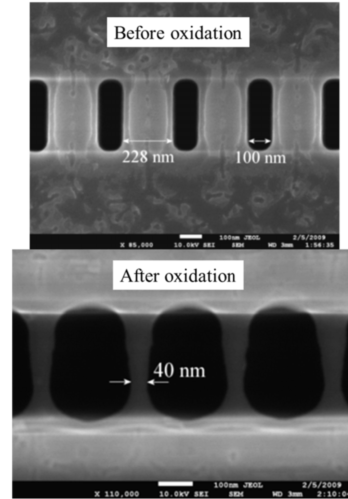

Fig. 4. SEM images showing the thinning of the silicon nanowires after thermal oxidation.

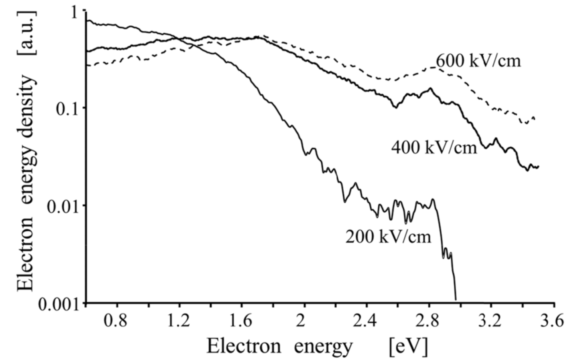

Fig. 5. The influence of electric field on the EED function.

III. Emission Spectra

A. Electron Energy Distribution (EED) Function

It has previously been postulated that the most dominant photon generation mechanisms in high electric field reverse biased silicon p-n junctions are direct and indirect intraband transitions of hot carriers [8], [9]. The direct intraband process will dominate at lower photon energies ($<$ 1.4 eV), and the indirect phonon assisted intraband process will dominate at higher energies ($>$ 1.4 eV). From Monte Carlo simulations of the EED (electron energy distribution) function in the conduction band [10], it can be seen that the electric field will determine the eventual emission spectrum. In Fig. 5 is shown the EED function at three electric fields, namely 200, 400 and 600 kV/cm. From this figure it can be seen that the high energy electron density increases with increasing electric field, while the low energy electron density decreases with increasing electric field.

The photons emitted from a forward biased junction in silicon will be the result of band-to-band indirect interband recombination. This is a rather narrowband emission centered near the 1.1 eV band gap energy of silicon.

B. Experimental Results

In Fig. 6 is shown the experimentally observed photon emission rate from two nanowire arrays as a function of

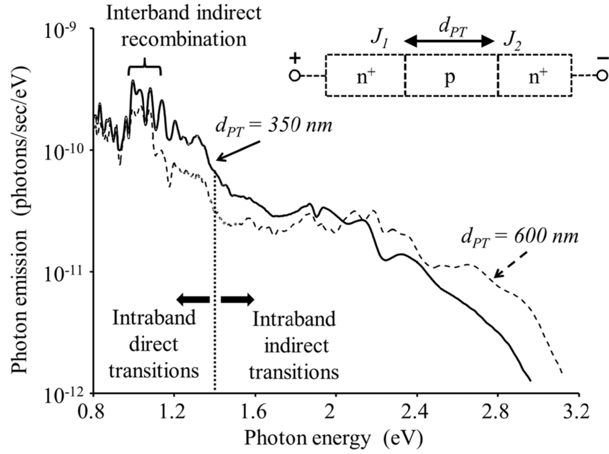

Fig. 6. Measured nanowire emission spectra at two different separation distances d_{PT}.

photon energy, and for two different punch through separation distances d_{PT}.

The first observation from Fig. 6 is that we can identify three photon generation modes, two broadband and one narrowband. Above a photon energy of 1.4 eV, the broadband intraband indirect phonon assisted hot carrier electroluminescence can be observed. This emission is mostly from the high electric field regions in the device and typically corresponds with the 400 to 600 kV/cm electric field plots in the EED function of Fig. 5. At photon energies less than 1.4 eV the broadband intraband direct transition emission is observed. This photon generation takes place in the low electric field region of the device and corresponds with the 200 kV/cm plot in Fig. 5. Fig. 6 exhibits an increase in low energy emission, very similar to the increase at low energies of the 200 kV/cm EED in Fig. 5.

Since junction *J2* is forward biased, some narrowband indirect band-to-band emission at photon energies close to the band gap energy should be observed. In Fig. 6 a narrowband emission can be seen at around a photon energy of 1.1 eV.

C. Discussion of Results

The spectra of Fig. 6 show differences between the two separation distances d_{PT}. Referring to Fig. 1, it can be seen that the longer separation distance d_{PT} should result in a higher average electric field in the device in comparison with the shorter distance. This occurs because the central lightly doped p-type region will be fully depleted at a lower applied voltage if the distance between the two junctions is shorter. One would therefore expect the $d_{PT} = 600$ nm device to have on average a higher electric field than the $d_{PT} = 350$ nm device. As can be observed in Fig. 6, the $d_{PT} = 600$ nm has more high energy photons than the $d_{PT} = 350$ nm device, and also less low energy photons than the $d_{PT} = 350$ nm device, which is a clear indication of a higher electric field as shown by the EED functions in Fig. 5. It is interesting to note that the crossover photon energy for the two nanowire devices in Fig. 6 is in the range 1.8 to 2 eV, which correlates well with the crossover energy of 1.8 eV for the 400 and 600 kV/cm electric fields in the EED function depicted in Fig. 5.

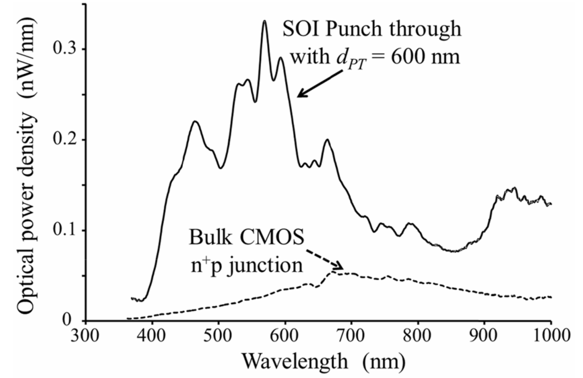

Fig. 7. Measured nanowire emission spectrum compared to emission spectrum from bulk CMOS pn junction.

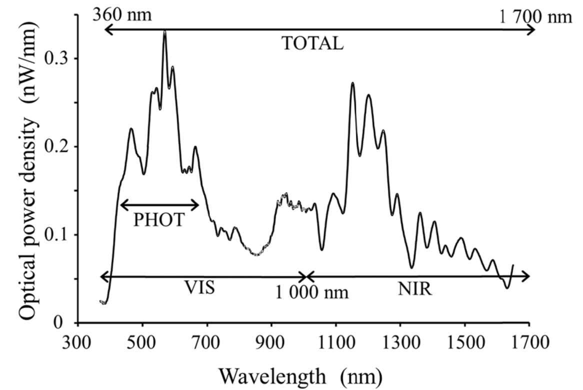

Fig. 8. Optical power classification and typical nanowire emission spectrum.

D. Comparison With Bulk Light Source

In Fig. 7 is shown the emission spectrum of the $d_{PT} = 600$ nm punch through device, as well as the emission spectrum from a standard avalanching n^+p single junction diode in a 350 nm bulk CMOS technology. The spectra are only shown up to 1 000 nm wavelength since we are mainly interested in radiation visible to the naked eye or radiation being detected by silicon based detectors. Fig. 7 indicates that the performance of the SOI punch through device is significantly better than the bulk CMOS diode.

In Fig. 7 it can be observed that the punch through nanowire emission spectrum is at least 10 times that of the bulk p-n junction at shorter wavelengths. At longer wavelengths the nanowire emission is only a factor 2 or 3 better than the bulk diode. This is especially important in the short wavelength photopic or visible region for micro display applications.

IV. Optical Power and Efficiency

The optical power emitted from the front surface of each device was determined. The optical power values were classified into four spectral ranges as defined in Fig. 8.

The total optical power (TOTAL) is the sum of the optical power ranging from 360 nm to 1 700 nm. The short wavelength optical power VIS covers the wavelength range

TABLE I

OPTICAL POWER AT 0.1 A BIAS CURRENT

Spectral range	Nanowire d_{PT} = 350 nm	Nanowire d_{PT} = 600 nm	Thin film d_{PT} = 463 nm
TOTAL	226 nW	176 nW	86 nW
VIS	105 nW	94 nW	29 nW
NIR	121 nW	85 nW	46 nW
PHOT	21 nW	28 nW	6 nW

TABLE II

SOI OPTICAL SOURCES VS. CMOS BULK SOURCES

Spectral range	SOI Nanowire n^+pn^+	CMOS Bulk n^+p	Ratio SOI/Bulk
VIS	1.05 nW/mA	0.125 nW/mA	8.6
PHOT	0.28 nW/mA	0.025 nW/mA	11.2

360 nm to 1 000 nm and the optical power NIR covers the range 1 000 nm to 1 700 nm. The photopic or visible power PHOT covers the visible spectral range and is weighted with the photopic eye function. Very noticeable in the linear scale plot of Fig. 8 is the narrowband indirect band-to-band recombination near 1 200 nm wavelength.

In Table I the optical power emitted from the front surface is given for two nanowire SOI structures and one thin film SOI structure, all at the same bias current of 100 mA.

From Table I it is evident that the nanowire SOI device efficiency is significantly better than the thin film SOI device by about a factor 3 to 4. It is also observed in Table I that the TOTAL optical power increases with decreasing distance d_{PT}. The separation distance $d_{PT} = 350$ nm has a better efficiency than the $d_{PT} = 600$ nm at the longer wavelengths (lower photon energies), a result in line with the spectra plotted in Fig. 6. Only in the short wavelength (high photon energy) photopic spectral range is the $d_{PT} = 600$ nm device superior. The nanowire diameter did not affect the efficiencies of the devices since quantum mechanical effects were not present [7]. The best SOI efficiency performance in Table I is 2.26 nW/mA over the TOTAL spectral range, 1.05 nW/mA in the VIS range, 1.21 nW/mA in the NIR range and 0.28 nW/mA in the photopic PHOT range.

It is worthwhile to compare the optical power emitted from the front surface of the SOI devices to that emitted from the front surface of a 350 nm process CMOS integrated circuit from a standard n^+p junction in avalanche. The two spectra were plotted in Fig. 7 indicating that the SOI devices are superior. The relative values are given in Table II.

In Table II the efficiency metric nW/mA emitted from the front surface of the SOI nanowire device is a factor 8.6 times better than the bulk CMOS device over the VIS spectrum shown. For the photopic spectral range PHOT the SOI nanowire device is a factor 11.2 times better than the bulk alternative. Taking into account that the operating voltage of the SOI nanowire was 7.5 V and that of the bulk CMOS diode was 10 V, it can be derived that the photopic external power efficiency (37.3 nW/W) of the SOI nanowire light source is a factor 14.9 better than the bulk CMOS diode.

V. Conclusions

It was shown that by using a two junction device in the punch through mode, the electric field can be adjusted via the separation distance between the two junctions. Furthermore, the operating voltage will be lowered compared to pure avalanche operation. It was also demonstrated that silicon nanowires in punch through, manufactured in a SOI technology, will have almost factor 15 better external power efficiency than a single CMOS junction in avalanche. Punch through devices in a continuous thin film rather than parallel nanowires also performed better than the CMOS bulk devices, but was still about a factor 3 less efficient than the nanowires. The light source efficiency ratios scale approximately 10:3:1 for SOI nanowires : SOI thin film : CMOS bulk. The better performance seen in the SOI devices is mostly due to an improvement in the efficiency of light extraction due to reflections from the substrate/oxide interface and reduced internal reflections in the hemispherical nanowires. Smaller dimensions will lead to quantum confinement, enhancing internal quantum efficiency as well.

The use of punch through devices as optical sources in SOI technology has been patented not only in the USA [11], but also Europe, China, Japan, South Korea, Taiwan and Canada.

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