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INVESTIGATING THE USE OF INDIRECT SENSING TECHNIQUES TO REDUCE THE EFFECT OF GEOMETRICAL CORRECTION FACTORS IN SEMICONDUCTOR HALL EFFECT PLATES

by

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SUMMARY

INVESTIGATING THE USE OF INDIRECT SENSING TECHNIQUES TO REDUCE THE EFFECT OF GEOMETRICAL CORRECTION FACTORS IN SEMICONDUCTOR HALL EFFECT PLATES

by

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Degree: PhD (Electronic Engineering)

This research thesis seeks to investigate a new method to sense the classical Hall effect in Hall devices under the influence of a magnetic field primarily manufactured in complementary metal oxide semiconductor (CMOS) technologies.

The thesis poses a research question enabling the investigation into whether or not the geometrical factor in a classical Hall device can be improved by proposing a new method to sense the Hall effect indirectly in standard CMOS technology. State of the art Hall effect devices rely on low ohmic contacts to sense the Hall voltage effect. These contacts along with the geometry can have an adverse effect on the Hall device sensitivity. Furthermore, the Hall voltage in Silicon can be very limited in comparison to high mobility semiconductor materials. It was found that by replacing the highly doped n-type sensing contacts of the Hall device with highly doped p-type contacts, a vertical bipolar junction transistor could be formed. This transistor, normally considered a parasitic element, ultimately leads to a very useful sensing technique in which the Hall current is sensed and amplified by the transistor forward gain, $\beta + 1$. The Hall effect appears as a current through the emitter of the transistor.

The major contribution of this research resides in a novel method to measure as well as amplify the Hall effect in a square n-well plate manufactured on a standard CMOS technology. The research also bridges the gap found in literature on the subject of direct versus indirect Hall sensing techniques. The outcome of the research also addresses practical implementations of such alternate methods as well as the effect the methods have

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on fundamental noise limits and differences in noise between the proposed method and traditional methods. The device although not improving the fundamental geometrical factor of the plate which was found to be dominated by the geometry itself, was proven to be functional as well as behaving according to Hall effect theory. Furthermore, the gain that even low forward gain bipolar transistors contribute to the signal, more than compensates for the loss of Hall effect contributed by the geometrical correction factor. The method also contributes less noise in comparison to typical traditional methods of Hall voltage amplification using operational amplifiers. The proposed method thus allows for a very simple measuring technique that is compatible with standard CMOS technology processes.

Keywords: Hall effect, Hall voltage, Hall current, CMOS, vertical BJT, sensitivity, forward gain, 0.35 µm process, noise, geometrical factor

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OPSOMMING

ONDERSOEK NA DIE GEBRUIK VAN INDIREKTE DETEKSIETEGNIEKE OM DIE EFFEK VAN GEOMETRIESE KORREKSIEFAKTORE IN HALFGELEIER HALL EFFEK SENSORS TE VERMINDER

deur

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Promotor:	Prof. M du Plessis
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Graad:	PhD (Elektroniese Ingenieurswese)

Hierdie navorsings tesis is gemik daarop om 'n nuwe meetmetode te ondersoek om die klassieke Hall effek te meet in Hall toestelle onder die invloed van 'n magneetveld wat primér in komplementêre metaaloksied-halfgeleiertegnologie (CMOS) vervaardig word.

Die tesis stel 'n navorsingsvraag wat lei tot die ondersoek van die vraag of die geometriese faktor in 'n klassieke Hall toestel verbeter kan word deur om 'n nuwe metode voor te stel om die Hall effek indirek te meet in standaard CMOS tegnologie. Nuutste navorsing oor meetmetodes in Hall effek toestelle, maak nog steeds staat op lae ohmiese kontakte om die Hall spanning effek te meet. Hierdie kontakte saam met die meetkunde van die toestel, het 'n nadelige uitwerking op die Hall toestel se sensitiwiteit. Verder is die Hall spanning in Silikon baie beperk met vergelyking tot hoë mobiliteit halfgeleier materiale. Daar is gevind dat deur die vervanging van die hoogs gedoteerde n-tipe meetkontakte van die Hall toestel met hoogs gedoteerde p-tipe kontakte, kan vertikale bipolêre transistors gevorm word. Hierdie transistor, gewoonlik beskou as 'n parasitiese element, lei tot 'n baie nuttige meet tegniek waarin die Hall stroom gemeet en versterk word deur die transistor se voorwaartse wins, $\beta + 1$. Die Hall effek verskyn as 'n stroom deur die emittor van die transistor.

Die grootste bydrae van hierdie navorsing lê in 'n nuwe metode om die Hall effek in 'n vierkantige n-dam plaat wat in standaard CMOS tegnologie vervaardig is te meet sowel as om die sein te versterk. Die navorsing oorbrug ook die gaping gevind in literatuur oor die onderwerp van direkte teenoor indirekte Hall meet tegnieke. Die uitkoms van die navorsing spreek ook die praktiese implementering van die meetmetode aan sowel as die

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effek wat die meetmetode op fundamentele ruisgrense en verskille in ruis tussen die voorgestelde meetmetode en tradisionele meetmetodes het. Die toestel, hoewel nie gelei het tot 'n verbetering van die fundamentele geometriese faktor van die plaat wat oorheers is deur die meetkunde van die plaat self, is wel funksioneel bewys, asook dat dit optree volgens Hall effek teorie. Verder is daar gevind dat die wins wat selfs lae voorwaartse wins bipolêre transistors bydra tot die sein, meer as die verlies wat die meetkundige faktor veroorsaak op die Hall effek kan herwin. Dié meetmetode dra ook minder ruis by met vergelyking tot tipiese tradisionele meetmetodes soos operasionele versterkers, wat vir Hall spanning versterking gebruik word. Die voorgestelde meetmetode skep dus 'n baie eenvoudige meettegniek wat versoenbaar is met standaard CMOS tegnologie prosesse.

Sleutelwoorde: Hall effek, Hall spanning, Hall stroom, CMOS, vertikale BJT, sensitiwiteit, voorwaartse wins, 0.35 μm proses, ruis, geometriese faktor

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Last but not least, I would like to extend my special gratitude for my wife Esté for her loyalty, understanding and support which has, without doubt, contributed to this milestone in my career. Also my children for the sacrifices they made while Daddy was “writing a book”.

Dedicated to my father and mother

George Sydney Mellet & Elizabeth Anne Mary Theck

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LIST OF ABREVIATIONS

ASIC	Application specific integrated circuit
Bi	Bismuth
CAD	Computer aided design
CCCS	Current controlled current source
CMOS	Complementary metal oxide semiconductor
DRC	Design rule checker
EEPROM	Electrically erasable programmable read only memory
EPROM	Electrically programmable read only memory
FIB	Focused ion beam
GaAs	Gallium Arsenide
Ge	Germanium
GMM	Giant magnetostrictive material
GMR	Giant magnetoresistance
HV	High voltage
IC	Integrated circuit
InAs	Indium Arsenide
InSb	Indium Antimonide
JFE	Junction field effect
LOCOS	Local oxidation of silicon
LVS	Layout versus schematic
MEMS	Microelectromechanical system
MKSA	Meter, Kilogram, Second, Ampere
MOSFET	Metal oxide semiconductor field effect transistor
RMS	Root mean square
SI	Système International d'Unités
Si	Silicon
SOI	Silicon on insulator
VHD	Vertical Hall device
µm	Micrometer
5C	Five contact

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CHAPTER 1 INTRODUCTION

1.1 INTRODUCTION

High velocity of charge carriers are required to generate a strong Hall effect [1]. To achieve this, it is required to have either a high electric field or a high mobility of quasi-electric carriers neither of which could be effectively achieved in the metal conductors used at the time of its discovery in 1879 [1]. The invention of semiconductor technology created a suitable candidate to simultaneously achieve these two qualities and consequently much improved signal levels. Semiconductors consist of low doped materials that possess quasi-electric carriers in low densities making it possible to apply a high electric field without causing thermal degeneration of the host material [1].

The need to sense the generated Hall voltage requires an appropriate contact point into the Hall device. Low ohmic contacts are typically used for this purpose but their intrinsic high doped properties contradict the fundamentals of achieving a strong Hall effect, specifically at its point of contact into a Hall device. The result is a diminution of the Hall voltage creating the need to introduce factors that explain the reduction of the theoretical maximum Hall effect achievable. Much research has been done over the decades to find methods of reducing this factor by manipulating parameters directly under the influence of a designer. These methods mainly include changing the geometrical shape to harness the various advantages that accompany them in specific technologies [2]. The problem is reintroduced however in vertical Hall sensing devices due to the limiting influence a designer has on the geometries in the vertical direction in CMOS technologies. With three dimensional Hall sensors [3], nanomagnetic logic devices [4] and nanobead sensing [5, 6] applications becoming ever more popular, there is continuous pressure to search for the fundamental sensing limits [7, 8] to increase the performance of such devices in various applications.

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1.2 OBJECTIVE

The objective of this thesis is to research the feasibility of using indirect sensing techniques as an alternate approach to sense the Hall voltage in a Hall effect device. The goal is to prove whether or not an indirect sensing approach can reduce or eliminate the effects associated with traditional direct sensing techniques ultimately forming the basis upon which the research hypothesis will be rejected or accepted.

1.3 JUSTIFICATION FOR THE RESEARCH

Up to now, it appears from literature that the only method of sensing the Hall effect in Hall devices is through the use of highly doped low ohmic contacts [1, 2, 3, 4, 5, 6, 7, 8]. Popovic [1] mathematically explores the Hall effect under the influence of the Lorentz force. His investigation illustrates a combination of effects appearing between the geometrical limits of infinitely long and short Hall plates. These effects lead to a diminution of the Hall voltage in a finite length Hall device due to non-perfect current confinement, contributed by the presence of the physical electrical contacts. The contacts cause a short circuiting effect at both the current supply, as well as the sensing terminals. The result is no Hall field at the current supply contacts and a reduction of the described Hall electric field in the direct vicinity of the sensing contacts as a result of a reduction in current density. These effects are modelled by a geometrical correction factor namely the ratio between the Hall voltage generated on an arbitrary shaped Hall plate and the Hall voltage generated on an infinitely long Hall plate, both influenced by the same magnetic field and under the same conditions [1, 7]. Vertical Hall effect devices are particularly adversely affected by this effect [7].

This research aims to challenge traditional thinking and methods with regards to the sensing of the Hall effect, itself the cause of a reduction in performance, in a semiconductor Hall device. From the literature pre-study it can be deduced that if it were possible to use a non-intrusive method to measure the Hall voltage generated by a Hall device under the influence of the Lorentz force, it may be possible to reduce the

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geometrical correction factor effect caused by the sensing contacts themselves. By succeeding in this, an increase of the geometrical factor seems possible leading to higher sensitivities between identical geometrical Hall devices using direct and indirect sensing techniques.

1.4 RESEARCH QUESTIONS AND HYPOTHESIS

1.4.1 Research questions

- Is it possible to reduce or eliminate short circuiting effects of the Hall voltage resulting from traditional direct sensing contacts using indirect sensing techniques?
- What are the main noise sources in conventional CMOS Hall effect devices?
- How will indirect sensing influence the noise performance of CMOS Hall sensors?

1.4.2 Hypothesis

If direct sensing contacts used to measure the Hall effect of a semiconductor Hall effect device results in a diminution of the Hall signal, then indirectly sensing the Hall signal may regain lost Hall effect by eliminating short circuiting effects resulting from direct contact.

1.5 METHODOLOGY

The research questions will guide an in depth study into semiconductor physics fundamentals that govern Hall effect design in CMOS as well as noise sources affecting sensing performance. Specific focus will be on understanding traditional Hall device implementation and Hall voltage sensing techniques. The theory will then be applied in the design and simulation of appropriate Hall devices as applicable to this study. Appropriate devices that illustrate the desired principles will be chosen to be manufactured. With targets set, the layout can be designed and submitted for fabrication. The fabricated device can be characterized and adjusted if required and results compared with theoretical and simulated data. The research hypothesis will then be tested against these findings and appropriate conclusions made whereby the findings will be the basis of either accepting or rejecting the hypothesis. The study will be concluded with proposals for future research in the field.

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1.6 CONTRIBUTION

This work contributes in the field of Hall effect devices in standard CMOS technologies. Most literature on the subject of sensing Hall effect voltages continue to be focused on direct contact into the Hall effect device. This results in a reduction of performance due to short circuiting effects arising from the low ohmic contacts in and around the region of contact. Although various geometries have been proposed over decades of research into horizontal devices that can reduce or even eliminate this effect [2], the problem continues to affect vertical structures [7]. The reason for this is due to the fact that a designer has little influence on the geometrical shape of such devices due to processing parameters and constraints. This work aims at bridging the gap found in literature on the subject of direct versus indirect Hall voltage sensing techniques. It also poses the question of whether an alternate method exists that can be successfully implemented to overcome the shortcomings of traditional methods. The work will also address practical implementations of such alternate methods as well as to study the fundamental noise limit differences between traditional and the proposed alternate method.

1.7 PUBLICATIONS LEADING FROM THIS RESEARCH

The following articles have been published in or submitted to accredited journals as part of the research activities of the author:

- Mellet, D.S. and du Plessis, M., 2014. A novel CMOS Hall effect sensor. *Sensors and Actuators A: Physical, Solid-State Electronics and Journal of Magnetism and Magnetic Materials*.
- Mellet, D.S. and du Plessis, M., 2014. Direct and indirect Hall effect sensing, a statistical analysis. *Sensors and Actuators A: Physical, Solid-State Electronics and Journal of Magnetism and Magnetic Materials*.
- Mellet, D.S. and du Plessis, M., 2014. The influence of indirect sensing techniques on noise performance in CMOS Hall effect devices. *Sensors and Actuators A:*

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Physical, Solid-State Electronics and Journal of Magnetism and Magnetic Materials.

1.8 OUTLINE

Chapter 1 introduces this thesis and explains the background and objective for the intended research. The objective is then supported by justifications thereof upon which the research questions and hypothesis are formulated. This is followed with a proposed methodology aimed at answering the research questions and providing evidence for the acceptance or rejection of the stated hypothesis. The chapter is concluded by the contributions of this research to the applicable body of knowledge.

Chapter 2 sets out the Hall effect theory related to this research. An extensive review of literature sets the foundation for this research, the intention of which is to summarize the background of the Hall effect in semiconductor technologies, applications, trends and recent technological developments. This is followed by an in depth study into semiconductor physics and its fundamental influence on the Hall effect. Various semiconductor Hall plate designs and techniques are presented, classified, analysed and summarized with specific focus on performance parameters, such that a comparison and conclusion can be drawn between them. The chapter is then concluded with the theoretical principles of the vertical parasitic BJT and its relevance as an indirect sensing technique.

Chapter 3 describes the methodology used in this research for its successful completion. A flow diagram outlines the basic structure used after which the detail of the tools used for the research and design is explained. These include computer aided design (CAD) packages, technologies, instruments and any relevant models and assumptions used during the process. This chapter serves as the basis upon which results and conclusions should be interpreted and scrutinized.

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Chapter 4 elaborates on the proposed design based on the methods described in the previous chapter. The design is then simulated and the projected targets are discussed and compared with the theory outlined in Chapter 2 . The layout design is then implemented in the target CMOS technology.

Chapter 5 focuses on characterizing the fabricated samples and the results are then compared to the theoretical and simulated projections.

Chapter 6 presents the conclusion of this thesis with suggestions for future research as well as some closing arguments.

1.9 CONCLUSION

Chapter 1 introduced the thesis with background of the Hall effect in semiconductor technology. The objective of the research was stated and the research justified by reference to relevant literature. The research questions were then stated followed by the formulation of the hypothesis upon which the outcome of the research will be tested. A brief summary of the intended methodology was given after which the contribution of this research was clarified.

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CHAPTER 2 HALL EFFECT THEORY

2.1 INTRODUCTION

In his last university year, E.W. Hall was intrigued by a passage he read on Maxwell's Electricity and Magnetism [9]. Maxwell stated that the force responsible for pressing a current carrying conductor across the lines of a magnetic force was mechanical and acted solely on the wire itself. What puzzled him was that in the absence of electric current, the wire was itself not affected by a magnet and when it was carrying a current, the effect was proportional to the strength of the current. With support and guidance from his Professor on the subject, Prof. Rowland, who was in agreement with Hall, he devised an experiment with the promise of revealing a better understanding of the matter. After two failed attempts, on the 28th of October 1879, he adapted his experimental setup by using a thin gold leaf on glass that would act as a disc and through which he would pass an electric current. In doing so he finally measured with the magnet in place, a potential perpendicular to the said current, a phenomenon that could only be explained by the effect of the electric current being pressed toward one side of the conductor. With this knowledge he improved his experiment aimed at demonstrating that, what he was measuring on the Thomson galvanometer, was indeed the proportional relationship between the electric current strength and the magnetic force applied. On the 28th of November 1879, Hall documented the results that proved that the relationship was the product of the two. Through his experiments, Hall deduced that the proportionality factor of the transverse field was

$$E' \propto Mv. \qquad (2.1)$$

In the notation used at the time, E' is the transverse electromotive force, M is the magnetic field intensity and v the drift velocity of charge carriers constituting the current through the conductor. The phenomenon was later attributed to his name [1] and would become one of the most mass produced and useful physical attributes in future magnetic sensors [10].

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This chapter deals with the theoretical aspects of the Hall effect. To fully appreciate this, the chapter begins with an illustration of where the Hall effect is positioned on the magnetic field strength scale based on state of the art technology at the time of this writing. After this, the Hall effect itself will be analysed followed by an in depth study of the ideal characteristics of a Hall device. The chapter is then concluded with a review of trends and state of the art Hall sensors and their applications.

2.2 THE HALL EFFECT: AN ANALYSIS

2.2.1 Terminology

Before we begin, it is necessary to define the terminology that will form part of this thesis [11]. The Hall effect itself refers to the galvanomagnetic effect discovered by Hall. Solid-state electron devices that have been designed with the primary purpose of application based on the Hall effect are classified under the term Hall effect devices the most conventional of these being the Hall plate. The Hall plate can take on many forms with the most common being the square Hall plate, the Hall cross, or Hall junction as it is sometimes referred to in physics literature, and the Hall bridge when two or more Hall crosses are combined. Both these and non-specific shaped devices are called Hall devices, Hall elements, Hall cells and in German literature Hall generators. When applied, a Hall device is normally referred to as a Hall magnetic sensor or just Hall sensor. Japanese literature refers to Hall sensors as Hall elements. Hall sensors are called Hall probes in the magnetic field measurement community whilst the microelectronic community call them integrated Hall effect magnetic sensors, Hall ASIC (application specific integrated circuit) or Hall IC (integrated circuit). This thesis focuses primarily on Hall devices implemented in CMOS and the terms CMOS Hall device and Hall device will be used interchangeably and both imply the same meaning. Furthermore, the focus shall lie in the analysis of the linear Hall effects but, because the Lorentz force origin gives rise to magnetoresistive effects as well, this will also be discussed as a possible indirect sensing method. Standard CMOS process will refer to commercially available standard n-well CMOS processes using high resistivity p-type substrates.

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2.2.2 Galvanomagnetic sensors

Many terms and units for magnetism have become known over the many years of its study and use. The most common units now use the meter, kilogram, second, ampere (MKSA) system which stems from the Système International d'Unités (SI) [12]. Magnetic field strength H was first related to ampere-windings or the number of turns forming a coil carrying a current I and thus measured in ampere per meter (A/m).

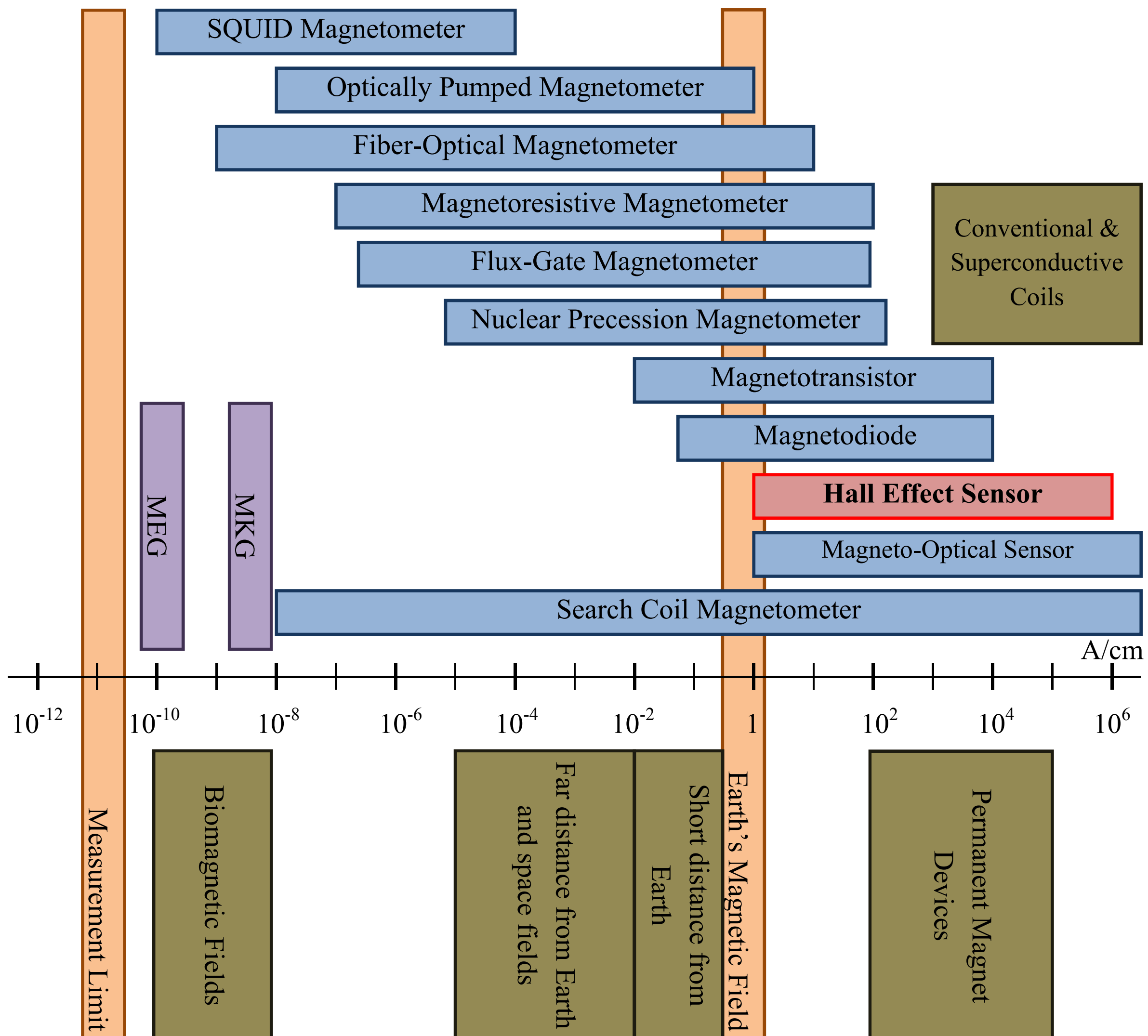

Figure 2.1 Magnetic field strength scale in A/cm showing sensor application range.

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The magnetic induction B is related to the magnetic field strength H in a vacuum by (2.2)

$$\boldsymbol{B} = \mu_0 \boldsymbol{H} \quad (2.2)$$

where μ_0 is the magnetic field constant $\mu_0 = 4\pi.10^{-7}$ Vs/Am [13]. In this study of the Hall effect, magnetic induction or flux density B will be used with its units in Tesla (T). Figure 2.1 graphically illustrates various magnetic sensor applications on a magnetic field strength scale H relative to the Earth's magnetic field strength of 0.5 A/cm [12, 14, 15, 16].

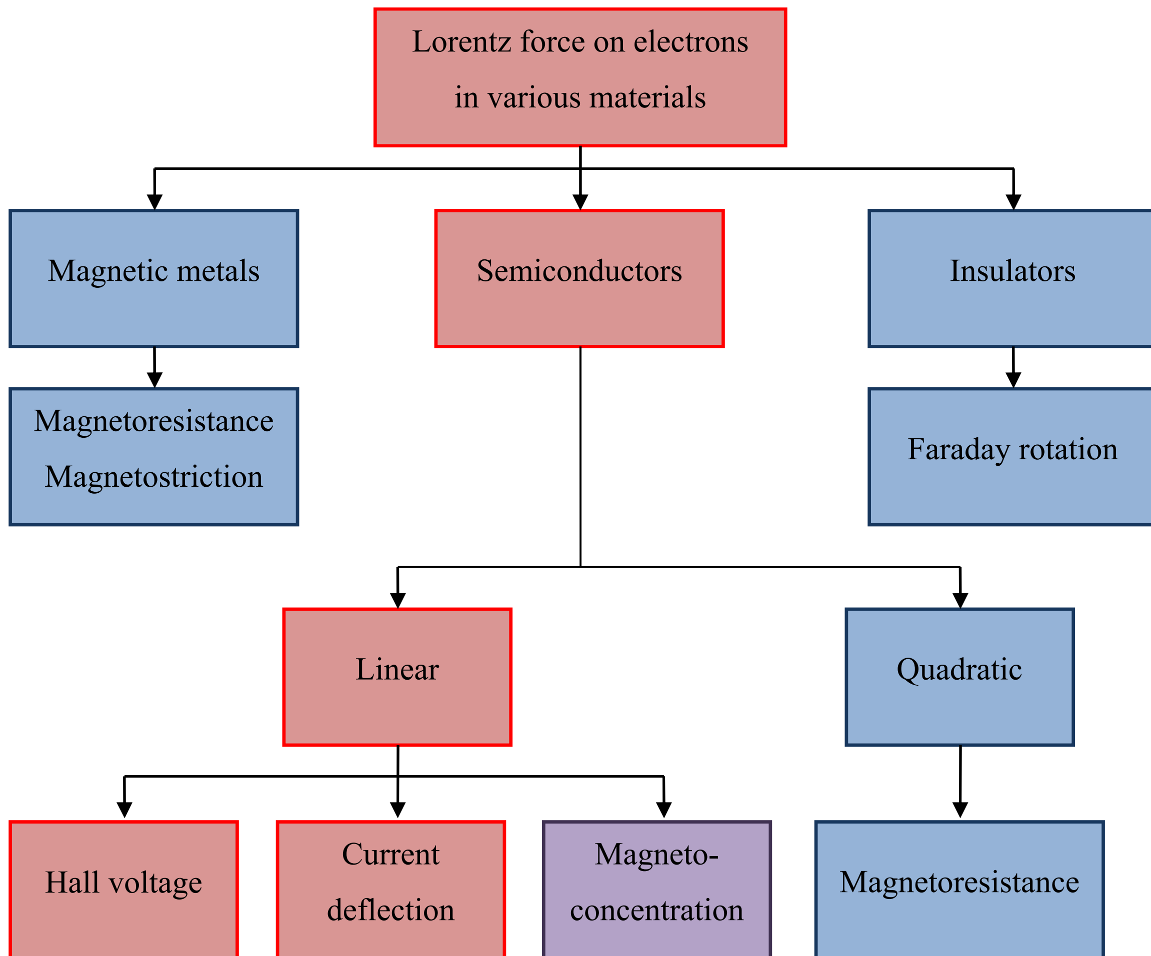

Figure 2.2 Classification of the Hall voltage resulting from the Lorentz force.

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As mentioned earlier, Hall devices fall under the general class of galvanomagnetic sensors which refers to a conductor carrying an electrical or *galvanic* current whilst under the influence of a *magnetic* field [12] and which forms a measurable response due to induced charge transport phenomena called galvanomagnetic effects. The best known galvanomagnetic effects are the Hall effect and the magnetoresistive effect. Figure 2.2 shows the classification of the Hall voltage and current deflection in the broader context of the effect of the Lorentz force on various materials [17, 18].

Popovic [11] defines the Hall effect as "a *transverse* isothermal galvanomagnetic effect" whilst the magnetoresistive effect is defined as "a *longitudinal* isothermal galvanomagnetic effect". The Hall effect itself is the result of an electromotive force transverse to the external electric field responsible for the current flow in a conductor, in response to the Lorentz force acting on the current due to a perpendicular magnetic field. The result is either the appearance of a voltage called the Hall voltage, collinear to the transverse electromotive force, or a deflection of the current flowing in the sample [11]. The current deflection also results in a third effect known as the magnetoresistive effect and is an increase in the sample's electrical resistance due to an increase in the flow path distance. The two effects thus always coexist. Although the magnetoresistive and Hall effects stem from the same origin, the former was discovered somewhat earlier in 1856 by William Thomson (Lord Kelvin) in his experiments on ferromagnetic thin sheet plates. Ironically their experimental setups were strikingly similar [19]. What Thomson observed was the combination of two effects namely; the magneto-concentration effect and a form of the galvanomagnetic effect in the non-magnetic layers whereas Hall only considered this effect in non-ferromagnetic materials [11]. It was Hall's discovery that led to a better understanding of the former [12]. The magnetoresistive effect is particularly useful in magnetoresistive sensors made from thin films of ferromagnetic transition metals. Here, there are at least three major contributors to the effect the first being the one just described, caused by the Lorentz force, proportional to $(\mu.\mathbf{B})^2$ with μ being the electron or hole mobility and $\mathbf{B}$ the magnetic flux density vector. A special band bending at the Fermi surface makes up the second contributor also proportional to $\mathbf{B}^2$ and also found in non-

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ferromagnetic and semimetals. The third contributor finds its origin in an altering of the density states at the Fermi level and is caused by a magnetic field's influence on an electron's positive and negative spin resulting in different shifts of energy levels [12, 20]. All three are referred to as magnetoresistive effects but should not be confused with each other. This thesis is mainly concerned with the first of these effects. Furthermore, to simplify the initial understanding of the Hall and magnetoresistive effects, two extreme conditions will be considered such that a study can be made of each effect in a theoretically purist form. The following assumptions will also be held: Firstly isothermal conditions will be assumed as required by the definition of the Hall and magnetoresistive effects. Secondly, equilibrium carrier concentrations are assumed thus neglecting diffusion currents and lastly a smooth-drift approximation will be held in that velocity of all carriers are the same and thus equal to the average drift velocity whilst neglecting thermal motion of carriers and approximating the energy dissipation effect of scattering by smooth friction. Under weak magnetic fields, electron motion is well approximated by the smooth-drift assumption and is defined by [11]

$$\mu B \ll 1. \tag{2.3}$$

2.2.3 The Lorentz force on quasi-free carriers in condensed matter

Popovic [11, 10] is one of the most active authors and an authority on the Hall effect. He presents an advanced physics approach on galvanomagnetic effects in semiconductors and upon which the following theoretical analysis is primarily based.

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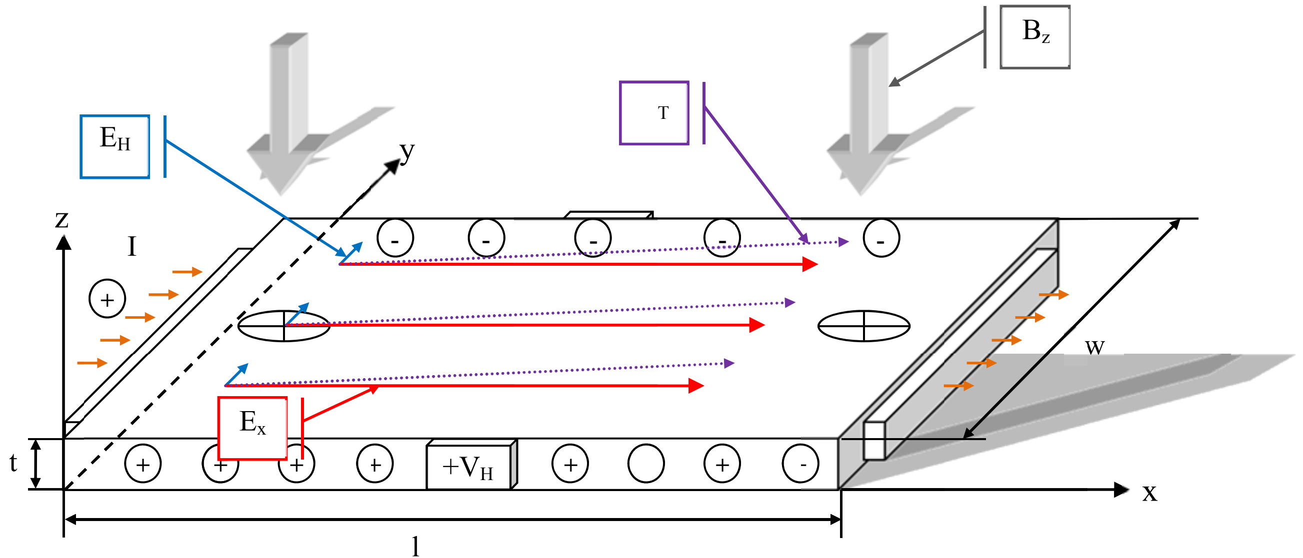

2.2.3.1 Hall voltage in long geometries

Figure 2.3 shows a typical long geometry Hall plate with dimensions length = l, width = w and thickness = t, with l >> w and four contacts at its boundaries. This geometry is very similar to the 2 x 9 cm sample used by Hall in his original experiment [9] the major difference being that in today's submicron semiconductor technologies, the dimensions have shrunk by at least four orders of magnitude.

The Hall plate can be biased in two fundamental ways namely constant voltage or constant current [11]. This example assumes a constant voltage is applied across the two current contacts, positive at x = 0 and negative at x = l, establishing an electric field $\mathbf{E}_x$ in the x direction forcing current to flow in the same direction along the length of the plate. Applying a magnetic field $\mathbf{B}_z$ perpendicular to the plate causes a transverse Lorentz force action on the charge carriers. The total force **F** acting on the carriers is given by

$$\boldsymbol{F} = q\boldsymbol{E}_x + \boldsymbol{q}[\boldsymbol{v}_d \times \boldsymbol{B}_z] \qquad (2.4)$$

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with q the charge of a single electron, $\mathbf{E}_x$ the externally applied electric field resulting from the voltage bias, $\boldsymbol{v}_d$ the free carrier velocity and $\mathbf{B}_z$, the perpendicular magnetic induction. The charge carriers are thus forced toward the transverse edges. The boundaries in the long sample confine the current density **J** such that no current can flow transverse to $\mathbf{E}_x$ thus causing a surface charge accumulation at the edge boundaries disturbing its charge neutrality. The result is a second electric field $\mathbf{E}_H$, called the Hall electric field, to appear. $\mathbf{E}_H$ increases until it balances out the force caused by the magnetic field such that

$$q[\boldsymbol{v_d} \times \boldsymbol{B_z}] + q\boldsymbol{E}_H = 0. \qquad (2.5)$$

The Hall electric field counter balances the magnetic "pressure" such that charge neutrality (2.6) can prevail.

$$n + N_A^- = p + N_D^+ \qquad (2.6)$$

Here, n is the concentration of electrons, N^-_A the ionized acceptor concentration, p is the concentration of holes and N_D^+ the ionized donor concentration. Due to the Hall electric field, a voltage V_H appears at the remaining two voltage contacts. This means that the charge carriers move parallel to the long sample as if only the external electric field $\mathbf{E}_x$ is acting upon them. Hall described this as a "pressing of the electricity" against the edge of the sample. Based on this explanation and in modern notation, (2.1) can be re-written as

$$\boldsymbol{E}_H = -[\boldsymbol{v_d} \times \boldsymbol{B_z}] \qquad (2.7)$$

where $\mathbf{E}_H$ denotes the Hall electric field, $\boldsymbol{v}_d$ the drift velocity of the charge carriers under the external electric field $\mathbf{E}_x$ and $\mathbf{B}_z$ again denoting the magnetic field vector to which the Hall plate is exposed. The drift velocity can furthermore be expressed as:

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$$\boldsymbol{v}_d = \mu \boldsymbol{E}_x. \qquad (2.8)$$

With μ the majority charge carrier mobility and thus (2.7) can be expressed as

$$\boldsymbol{E}_H = \mu[\boldsymbol{E}_x \times \boldsymbol{B}_z]. \qquad (2.9)$$

The force due to the magnetic field has the direction as specified by the cross product of the external electric field and the magnetic field and is irrespective of the charge carrier's direction and thus, the Hall electric field will always have opposite directions when observed in p-type and n-type semiconductors. The Hall voltage V_H resulting from the Hall electric field is specifically observed via the potential difference it creates between the two opposite edges of the plate in the same equipotential plane. From Figure 2.3, this voltage can be calculated as

$$V_H = \int_0^w \boldsymbol{E}_H \, dy. \qquad (2.10)$$

From (2.9), $E_H = \mu E_x B_z$ with $E_x=V/l$ and thus (2.10) results in

$$V_H = \mu \frac{w}{l} V B_{\perp}. \qquad (2.11)$$

Much more fundamental to the Hall effect is the Hall angle. The total electric field is given by (2.12).

$$\boldsymbol{E}_T = \boldsymbol{E}_x + \boldsymbol{E}_H \qquad (2.12)$$

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The total electric field is thus inclined at an angle to the current density given by (2.13) with θ_H the Hall angle.

$$\tan\theta_H = \frac{|\boldsymbol{E}_H|}{|\boldsymbol{E}_x|} \qquad (2.13)$$

Substituting for the electric fields $\mathbf{E}_H$ and $\mathbf{E}_x$, (2.13) becomes

$$\tan\theta_H = \mu B_\perp. \qquad (2.14)$$

It is also very useful to describe the Hall electric field as a function of the current density vector $\mathbf{J}_x$. From (2.8) the current density vector can be written as

$$\boldsymbol{J}_x = q\mu n\boldsymbol{E}_x \qquad (2.15)$$

with $\mathbf{J}_x$ the current density, q the charge of an electron, μ the mobility, n the number of free electrons and $\mathbf{E}_x$ the external electric field. Thus (2.9) becomes

$$\boldsymbol{E}_H = \frac{1}{qn}[\boldsymbol{J}_x \text{ x } \boldsymbol{B}_z]. \qquad (2.16)$$

It is useful to rewrite (2.16) as

$$\boldsymbol{E}_H = -R_H[\boldsymbol{J}_x \text{ x } \boldsymbol{B}_z]. \qquad (2.17)$$

The constant term R_H with units $VmA^{-1}T^{-1}$ is known as the Hall coefficient and is a material parameter that is normally used to characterize the intensity and sign of the Hall effect in a specific material. Its sign corresponds to that of the majority carriers in question.

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From (2.10) and (2.17) the Hall voltage for the long sample in Figure 2.3 can be calculated as

$$V_H = \frac{R_H}{t} I B_\perp \tag{2.18}$$

with V_H the Hall voltage, R_H the Hall coefficient, t the thickness of the plate, I the current through the plate and $B_\perp$ the perpendicular magnetic field. It can be seen from (2.18) that the Hall voltage is proportional to the Hall coefficient, the current through the plate as well as the intensity of the perpendicular magnetic field. Finally, it is also now clear that the thinner the Hall plate (or equivalently the higher the current density), the stronger the Hall voltage will be.

Another important factor for this study stems from the excess charge. This is the surface density of the charge that is separated by the magnetic force and resides at the device boundaries from which the Hall voltage stems. This surface charge density Q_s is given by

$$Q_s = C_s V_H \tag{2.19}$$

where C_s is the capacitance per unit area at the charged faces of the device.

2.2.3.2 Current deflection in short geometries

Figure 2.4 shows the geometry for a Hall device when configured as a short sample in that here, $l \ll w$. When an external electric field $\mathbf{E}_x$ is applied, current flows collinear to the field. Because of the large width, charge does not accumulate at the transverse edge boundaries as it did in the long sample and thus, a transverse electric field cannot appear as it did in (2.5) and (2.6). The result is that the total Lorentz force acting on the charge carriers causes them to divert from their original path as it did in the long sample without surface charge accumulation at the edges and for convenience, (2.4) is repeated (2.20).

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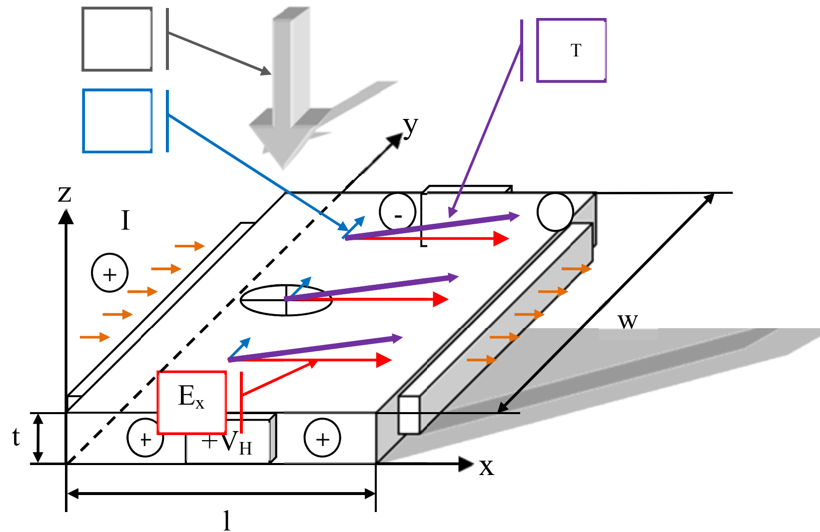

$$F = qE_x + q[v_d \times B_z] \qquad (2.20)$$

Substituting the resultant force **F** with its electric field equivalent, q**E** and multiplying by μn, (2.20) can be rewritten in terms of its current density vector

$$J_T(B) = J_x(0) + \mu[J_x(B) \times B_z] \qquad (2.21)$$

with $\mathbf{J}_T(\mathbf{B})$ the resultant current density vector in the presence of a magnetic field $\mathbf{B_z}$ and $\mathbf{J}_x(0)$ the current density due to the externally applied electric field in the absence of a magnetic field. It can now clearly be seen from (2.21) that the magnetic field's influence on the charge carriers in the x direction of a short sample results in their deviating from their original path at a slight angle. Again, this angle is the Hall angle and the Hall effect appears by a tilting of the current density $\mathbf{J}_x(\mathbf{B})$ with respect to the external electric field $\mathbf{E}_x$. The Hall angle is again defined as in (2.14).

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$$\tan\theta_H = \mu B_\perp \quad (2.22)$$

Similar to (2.11), (2.21) can be written in terms of the Hall current I_H biased by a current I and is given by:

$$I_H = \mu\frac{w}{l}IB_\perp. \quad (2.23)$$

The interesting aspect of the Hall device in current deflection mode is that it is independent of the plate thickness as it was in the long sample. It is however still desired to increase the resistance to reduce current consumption.

2.2.4 An accurate approach

Combining (2.4) and (2.9) as a function of the external electric fields gives

$$\boldsymbol{F} = q\boldsymbol{E}_x + q\mu[\boldsymbol{E}_x \times \boldsymbol{B}_z]. \quad (2.24)$$

The mobility μ in (2.24) used throughout 2.2.3 neglected the thermal agitation of the charge carriers [21]. Interestingly enough, (2.24) will still yield a fairly accurate approximation. Taking thermal agitation of the charge carriers into consideration yields a more accurate result and now (2.24) becomes

$$\boldsymbol{F} = q\boldsymbol{E}_x + q\mu_H[\boldsymbol{E}_x \times \boldsymbol{B}_z] \quad (2.25)$$

with μ_H the Hall mobility and given by

$$\mu_H = r_H\mu \quad (2.26)$$

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where r_H is called the Hall scattering factor. The Hall factor is a numerical value that describes the influence of thermal motion on carriers resulting in a scattering of the Hall effect. Generally the Hall scattering factor varies less than 20% from unity. This also applies to R_H in (2.17) which can now be rewritten as in (2.27).

$$R_H = \frac{r_H}{qn} \qquad \textbf{(2.27)}$$

A secondary effect that arises from the current deflection is called the magnetoresistive effect. It stems from (2.21) that due to the presence of the magnetically induced current density vector, the current density $\mathbf{J}_x(\mathbf{B})$ is slightly reduced in the direction of intended current flow collinear to the applied electric field. This is because the current is forced to take a longer path between the supply contacts, an effect that will be made more apparent in (2.32). The result at a macro level is that the resistance of the sample increases under the influence of a magnetic field. At a micro level, this can be translated as the relative increase in resistivity and

$$\frac{\rho_B - \rho_0}{\rho_0} = (\mu B)^2 \qquad \textbf{(2.28)}$$

with ρ_B the equivalent resistivity in the presence of a magnetic field, ρ_0 the resistivity in the absence of a magnetic field. Rewriting (2.28) in terms of conductivity yields

$$\sigma_B = \frac{\sigma_0}{(1 + \mu^2 B^2)} \qquad \textbf{(2.29)}$$

with σ_B the equivalent conductivity and σ_0 the conductivity in the absence of a magnetic field. Furthermore from Ohm's Law

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$$\boldsymbol{J} = \sigma \boldsymbol{E} \tag{2.30}$$

and substituting (2.29) and (2.30) into (2.25) we get

$$\boldsymbol{J} = \frac{\sigma_0 \mathbf{E}_x + \mu_H \sigma_0 [\boldsymbol{E}_x \text{ x } \boldsymbol{B}_z]}{(1 + \mu_H^2 B^2)} \tag{2.31}$$

For an arbitrary magnetic field direction, the formula in (2.31) gets a third term

$$\boldsymbol{J} = \frac{\sigma_0 \boldsymbol{E}_x + \mu_H \sigma_0 [\boldsymbol{E}_x \text{ x } \boldsymbol{B}_z] + \mu_H^2 \sigma_0 \boldsymbol{B}_z (\boldsymbol{E}_x . \boldsymbol{B}_z)}{(1 + \mu_H^2 B^2)} \tag{2.32}$$

such that (2.32) can be described as the sum of three current density vectors.

$$\boldsymbol{J} = \boldsymbol{J}_1 + \boldsymbol{J}_2 + \boldsymbol{J}_3 \tag{2.33}$$

In (2.33), $\mathbf{J}_1$ is proportional to $\mathbf{E}_x$, $\mathbf{J}_2$ to the cross product [$\mathbf{E}_x$ x $\mathbf{B}_z$] and is perpendicular to $\mathbf{E}_x$ and $\mathbf{B}_z$ and $\mathbf{J}_3$ is proportional to the vector $\mathbf{B}_z(\mathbf{E}_x.\mathbf{B}_z)$ and is collinear to the magnetic induction $\mathbf{B}_z$. This study focuses only on a magnetic induction perpendicular to the plate as in Figure 2.3 and Figure 2.4 making vectors $\mathbf{E}_x$ and $\mathbf{B}_z$ mutually orthogonal implying that $(\mathbf{E}_x.\mathbf{B}_z) = 0$. The third current density vector $\mathbf{J}_3$ will thus be ignored in further discussions.

2.3 GENERAL CHARACTERISTICS OF A HALL DEVICE

Making use of a specific phenomenon, material, property or any combination thereof to achieve a desired outcome requires, not only an understanding of how these factors each contribute individually to the measure, but also what influence or choices a designer may have to manipulate each individually. Generally, for magnetic sensors these factors can be

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divided into two broad classes [18, 22, 23]. The first class is environmental specific factors over which a designer has less influence and is broadly technology and application dependant. These typically include but are not necessarily confined to;

- application environment,
- availability, quality and cost of technology and materials, and
- magnetic field geometrical properties.

The Hall sensor is reported to be one of the best behaving magnetic sensors [16] making it extremely useful for a wide variety of applications [24, 25]. From (2.31) it is clear that high charge carrier mobility is required for a strong Hall effect signal. Even though there are many semiconductors that have higher electron mobility like Bismuth (Bi) for example, the material with the highest known mobility [26], CMOS in Silicon (Si), due to its abundance, quality, low cost and ease of manufacturability has become an extremely popular choice of technology for the implementation of Hall devices [27]. CMOS technology's physical constraints allow for very few Hall device implementations but many of its features are very well suited for its implementation and enhancement of performance as required for a useful Hall signal especially in the presence of conditioning electronics [28].

As described in 2.2.3, Hall devices make use of one of the two resulting phenomena of the Lorentz force namely the Hall voltage such as in a long device or current deflection such as in a short device [11]. For this reason, mainly buried plate-like structures, the vertical Hall device (VHD) and split drain magnetic field effect transistors (MAGFETs) have become the dominant structural choices for implementation. As CMOS processes develop however, many new features thereof are exploited to improve sensor performance [29, 30]. High voltage processes for example have become specifically ideal for the VHD whereby advantage is taken of the deep n-well to counter the short circuiting effects of the contacts in shallow n-wells [31]. To assess which material or structure to use to implement a Hall

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device, it is essential to fundamentally understand how various parameters influence the device performance. For example the current related sensitivity requires a thin material with low carrier concentration. Thin film technologies may be better suited than CMOS and have been studied for many years [32] due to their advantageous properties over normal Si technologies. The manufacturing processes and materials are however complex and expensive [33]. On the other hand, the voltage related sensitivity requires a high mobility material. These properties do not necessarily go hand in hand for example Indium Antimonide (InSb) with μ_n = 70000 $cm^2V^{-1}s^{-1}$ and Indium Arsenide (InAs) with μ_n = 30000 $cm^2V^{-1}s^{-1}$ may have very high mobility but due to their small band gaps they also have high carrier densities. This results in ohmic layers in the order of 10 Ω per square.

With the advent of large scale production and smart electronic integration, Germanium (Ge) and Si still remain the mainstream materials of choice and their lower mobility of μ_n = 3900 $cm^2V^{-1}s^{-1}$ and μ_n = 1500 $cm^2V^{-1}s^{-1}$ respectively, are compensated for by using signal conditioning circuits [34]. Generally low doped n-type semiconductors are used due to the electrons having higher mobility than holes. For Si, $\mu_n/\mu_p \approx 2.5$ whilst for Gallium Arsenide (GaAs) and InAs, it is 20 and 70 respectively [11]. Ongoing research however continues to push the boundaries of more exotic materials that have certain favourable properties over Si or are better suited to specific or demanding applications [35]. In the last ten years, post bulk processing techniques such as the addition of flux concentrators have also become very popular resulting in significant sensitivity gains [36, 25, 37].

The second class is sensor specific influential factors. It is closely related to performance and can be manipulated by the designer. These include:

- sensitivity,
- offset, noise and spatial resolution,
- temperature and cross-sensitivity,
- linearity,

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- frequency and time response,
- stability and drift,
- geometry, and
- testability.

2.3.1 Sensitivity

Sensitivity is a measure that describes how strongly a specific sensor output changes as a function of its input measurand. The absolute sensitivity factor S_A is its transduction ratio for large signals in a specific set of operating conditions and defined in (2.34) for both the Hall voltage and current modes with units VT^{-1} (volts per tesla) and AT^{-1} (ampere per tesla) respectively.

$$S_{VA} = \left|\frac{V_H}{B_\perp}\right| \text{ and } S_{IA} = \frac{S_{VA}}{R_{in}} \qquad (2.34)$$

The Hall device has two modes of operation, constant current bias and constant voltage bias. For constant current bias in a strongly extrinsic Hall plate, the current related sensitivity for both modes of operation is defined by (2.35) with units $VA^{-1}T^{-1}$ (volts per ampere per tesla) for Hall voltage mode and $AA^{-1}T^{-1}$ (ampere per ampere per tesla) = T^{-1} (per tesla).

$$S_{VI} = \frac{S_{VA}}{I} = \left|\frac{1}{I}\frac{V_H}{B_\perp}\right| \text{ and } S_{II} = \frac{S_{VI}}{R_{in}} \qquad (2.35)$$

From (2.18) and (2.27) the current related sensitivity S_{VI} for the Hall voltage mode can be written as in (2.36)

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$$S_{VI} = G_H \frac{r_H}{qnt}. \qquad (2.36)$$

Here S_{VI} denotes the current bias related sensitivity for the Hall voltage mode of operation, r_H the Hall factor, n the electron concentration, t the thickness of the plate and G_H the geometrical correction factor related specifically to the geometry of the device. The geometrical factor G_H is discussed in more detail in Paragraph 2.3.9. In a similar way, the voltage related sensitivity is defined as

$$S_{VV} = \frac{S_{VA}}{V} = \left|\frac{1}{V}\frac{V_H}{B_\perp}\right| = \frac{S_{VI}}{R_{in}} \text{ and } S_{IV} = \frac{S_{VV}}{R_{in}} \qquad (2.37)$$

with units $VV^{-1}T^{-1} = T^{-1}$ (per tesla). The input resistance is calculated as

$$R_{in} = \frac{l}{\mu qntw}. \qquad (2.38)$$

Substituting (2.38) into (2.37) and r_H by (2.26) yields the voltage related sensitivity as

$$S_{VV} = \mu_H \frac{w}{l} G_H. \qquad (2.39)$$

Here S_{VV} denotes the voltage biased related sensitivity for Hall voltage mode of operation, μ_H the Hall mobility of majority carriers, w/l the width-to-length ratio of the Hall device and G_H the geometrical correction factor. In the same way it can be shown that (2.39) holds for a current biased, current mode of operation. The sensitivities for the various materials defined in (2.36) and (2.39) is tabulated below. Note that current biased sensitivity is not material related whereas voltage biased sensitivity is.

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Table 2.1 Summary of sensitivities for various materials

Material	Sensitivity type	Reference	Minimum	Typical	Maximum
Not material related	S_{VI} ($VA^{-1}T^{-1}$)	[11]	50		500
Si	S_{VV} (T^{-1})	[11]		0.07	0.126
GaAs	S_{VV} (T^{-1})	[11]		0.2	0.67
Thin film InSb	S_{VV} (T^{-1})	[11]			3

From (2.39) it seems sensible to increase the sensitivity, materials with high Hall coefficients should be chosen. Care must be taken however as the higher the Hall coefficient of a material, the higher also its temperature dependant properties [24]. Extremely high sensitivities of 1243 $VA^{-1}T^{-1}$ for parallel field μ-Hall devices have been reported [38] but such high values become impractical due to the strong influence of surface charges and/or junction field effects (JFE) [11]. A typical μ-Hall device with an active area of 2.4 x 2.4 μm^2 would be more in the range of 175 $VA^{-1}T^{-1}$ [39]. For InGaAs/GaAs, sensitivities of up to 900 $VA^{-1}T^{-1}$ with excellent temperature performance of -0.016 %/K have been demonstrated [40].

Besides various materials, interesting variations on structures are also intensely researched such as to profit from specific technological characteristics such as the open bottom ended non-plate like Hall device. A sensitivity of 330 $VA^{-1}T^{-1}$ was achieved by varying its size, essentially affecting the penetration depth of the current flowing through the plate which translates to an “effective thickness” [41]. Various shapes and orientations of the familiar Hall plate have also been studied such as the three plate parallelogram implemented in Si and using a (100) oriented 7 μm bipolar 20V/40V high voltage (HV) process [42]. Various symmetrically patterned Hall plates were implemented achieving a maximum current related sensitivity of 180 $VA^{-1}T^{-1}$ for a parallelogram pattern and between 118 $VA^{-1}T^{-1}$ to 149 $VA^{-1}T^{-1}$ for other orthogonal structures. Various VHD geometries implemented using a standard high voltage CMOS process achieved current related sensitivities of between 18 $VA^{-1}T^{-1}$ to 127 $VA^{-1}T^{-1}$. High sensitivities of 400 $VA^{-1}T^{-1}$ are possible but require

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expensive processes [29]. Signal conditioning techniques are used to make various topologies possible normally not so for single standalone devices. The “ping pong” system is such an example in which one part of the circuit calibrates the first Hall device whilst the other part measures the second. The complete system uses four orthogonally connected plates, a flux concentrator, as well as auto-zeroing amplifiers resulting in a system with a magnetic gain of 420 $VA^{-1}T^{-1}$ [43]. Standalone Hall devices in Si using post deposited flux concentrators have been reported to achieve 125 $VA^{-1}T^{-1}$ [25]. Other post processing techniques also include an electroplated (as opposed to thin film technology) planar copper coil to generate a stable magnetic field of a few hundred μT. Furthermore a unique Ni/Fe core configuration surrounds the coils and Hall device and serves as a magnetic concentrator. A sensitivity of 105 $VA^{-1}T^{-1}$ and 77.5 $VA^{-1}T^{-1}$ were achieved with and without the magnetic core, an increase of 1.6 in sensitivity [44]. [45] Also demonstrates how the magnetoresistive effect plays a significant part in the sensitivity of short channel split drain MAGFETs when $l/w \leq 0.27$.

2.3.2 Offset

Probably one of the most studied Hall device characteristics is the offset usually described in terms of the offset voltage or current itself or expressed in terms of an equivalent magnetic field as in (2.40). The offset is one of the major deviations observed in a Hall device and is the DC signal measured in the absence of a magnetic field and thus cannot be distinguished from the quasi-static signal of interest [11]. Typically the offset as well as the offset drift of a conventional Hall plate is somewhat larger than the Earth’s magnetic field [16]. The main causes of the appearance of an offset is the process gradient across the chip, misalignment of masks and/or mechanical stresses resulting from fabrication as well as packaging [43, 46, 47, 48]. The offset can also vary as a result of supply voltage, current or temperature [25].

$$B_{off} = \frac{V_{off}}{S_A} \qquad (2.40)$$

Substituting the offset voltage (or current) by the equivalent offset voltage (or current) due

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to the asymmetry present in the plate resistance due to mask misalignment gives

$$V_{off} = \frac{\Delta R}{R} V_{in} \qquad (2.41)$$

and the absolute sensitivity for the Hall voltage and current mode of operation by

$$S_{AV} = S_V V_{in} = \mu_H \frac{w}{l} G_H V_{in} \qquad (2.42)$$

and

$$S_{AI} = S_V I_{in} = \mu_H \frac{w}{l} G_H I_{in}. \qquad (2.43)$$

The absolute sensitivity for the Hall current mode of operation results in an equivalent magnetic field of

$$B_{off} = \frac{\Delta R}{R} \frac{1}{\mu_H} \frac{l}{w G_H}. \qquad (2.44)$$

From (2.44), it can be seen that the higher the mobility, the lower the equivalent offset. For a typical Hall plate in Si with l/w ≈ 1, an offset in the range of $B_{off} \approx 10$ mT can be expected [24]. A geometrical tolerance of ±0.1 µm on a 500 µm x 500 µm plate can produce equivalent offsets of up to 6 mT.

A second source of offset is dependent on the orientation to the crystal structure and more commonly referred to as the piezoresistive effect due to the fact that it is highly affected by mechanical stresses. The magnetic equivalent offset is given by

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$$B_{off} = \frac{(\pi_l - \pi_t)X}{\mu_H^2 \left[3 - 2\left(\frac{w}{l}\right)\right] G_H\left(\frac{w}{l}\right)} \quad (2.45)$$

with π_l and π_t the longitudinal and transverse piezoresistance coefficients for the equivalent bridge resistors. For Si, the best orientation for a Hall device is parallel to the (110) crystal plane with the current flow in the <100> direction. Typically an encapsulation induced strain of 10^{-4} produces and equivalent offset of about 8.4 mT.

Techniques to reduce offsets include interconnecting of multiple orthogonal Hall devices [42], spinning current techniques, also known as chopper stabilizers [16, 49, 50], or a combination of both [43]. The disadvantages of these methods are that multiple plate configuration where up to four plates can be interconnected are fairly expensive in terms of area whilst spinning current methods are limited by their switching noise and bandwidths are limited by the output filter cut off frequencies [43]. By coupling the plates orthogonally and rotating them by 90° with respect to each other, it is possible to reduce the offset to between 0.5 mT [42] and 2 mT [43]. The spinning current method can typically achieve 0.2 mT to 0.5 mT in CMOS [50] but as low as 5 µT has also been reported [16]. The use of a flux concentrator can also reduce the offset due to magnetic gain to around 0.15 mT [25]. Novel geometries such as the double Hall device are also very capable of reducing the offset below 2 mT [51].

Examples of extremely low offset Hall plates include the eight contact spinning Hall plate [16] in which the bias is rotated from one contact to the next until the cycle is repeated and can achieve offsets down to a few µT. Combinations of offset reducing techniques were used in the "ping pong" system reported earlier. A magnetic concentrator made from high-permeability ferromagnetic material is deposited on the surface to amplify the magnetic field thus increasing the signal to offset ratio. A 5 to 5.6 magnetic gain is achieved with the concentrator saturating at a magnetic field of about 20 mT. This method multiplies the

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signal as well as the signal to offset ratio by the same amount. Orientating the sensor in the <110> crystallographic direction with current flowing in <100> direction to minimize the piezoresistive effect in an n-well Hall device was used. The offset was further reduced using the "ping pong" method consisting of two parts, one under calibration and the other measuring the signal finally achieving an offset of a few μV [43].

Another offset reduction method is the injection of current into an extra contact on the Hall device [52]. Very low offsets using this method along with orthogonally connected Hall plates have been reported with offsets ranging between ±5 μT but with similar sized standard deviation [42]. This result however is questionable given the reported achievements of others showing offsets more in the range of mT using this technique [43].

To reduce the offset due to the piezoresistive and piezo-Hall effects the following current direction should be used for the following substrate crystal orientations [53];

- In the (100) plane the piezoresistance is a minimum for current flowing in the <011> direction whilst the piezo-Hall effect is constant in all directions. This results in a highly sensitive strain gauge.
- In the (110) plane the piezoresistive as well as the piezo-Hall effects are minimum in <111> direction. This however does not coincide with the optimum stress dependent Hall offset voltage which is also in (110) plane but with current in the <100> direction.

Recently much research has been focused on VHDs due to their usefulness in fully integrated 3D magnetic sensors. VHDs are generally prone to lower sensitivities and higher offsets. The use of spinning current techniques is less effective than in Hall plate geometries. Offsets in the order of several hundred μT [3] to several mT [54] is expected and mainly due to unequal resistance modulation of inner and outer segments due to the JFE and device imperfections. The piezoresistive effect seems to only have a minor

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influence. It was demonstrated that the ideal VHD is symmetrical and well matched by ensuring a reduction of resistance asymmetries among the four segments, contacts and interconnection lines [31]. The offset in a VHD has been reported to comprise mainly of two components, a linear component due to contact shifts resulting from mask misalignments and a quadratic component mainly resulting from the JFE [55]. Methods for reducing the offset includes the cross connection of four sensors and more recently [56] proposed an alternative method whereby two, five contact (5C) VHDs are connected such that the offset was reduced by 80% in comparison to a single VHD whilst also increasing the sensitivity by 34 %.

2.3.3 Noise analysis

Typically, two types of noise are present in Hall devices namely generation noise and modulation noise. Generation noise is associated with internal electromotive force fluctuations. It is independent of device biasing conditions [11]. Modulation noise on the other hand is normally associated with fluctuations of device parameters and present only whilst current is flowing through the device. These include shot noise, recombination-generation noise and 1/f noise. Of these, thermal, recombination-generation noise and 1/f noise seem to be the most prominent. The root mean square (RMS) noise voltage v_n is given by its spectral density function $S_{NV}(f)$, where f is the frequency in Hz.

$$v_N = \sqrt{\left(\int_{f_1}^{f_2} S_{NV}(f)\, df\right)} \qquad (2.46)$$

with f_1 and f_2 the frequency boundary range in which the noise is to be defined [8].

2.3.3.1 Thermal noise

Thermal noise is a generation noise type also called Johnson-Nyquist noise and is a result of the thermal agitation of charge carriers. Its voltage spectral density is given by

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$$S_{VT}(f) = 4kTR \qquad (2.47)$$

with, k the Boltzmann's constant, T the absolute temperature and R the noise source resistance. Furthermore, thermal noise is independent of frequency up to very high frequencies and for this reason is called a white spectrum or white noise. A Si Hall device with a plate resistance of 500 Ω shows mainly thermal noise for frequencies larger than 5 kHz [34]. For VHDs thermal noise is in the range of 30 to 50 nT/√Hz [29] and for a µ-Hall device of size 2.4 x 2.4 μm^2 fabricated in 0.8 µm standard CMOS Si technology a thermal noise performance of 200 nT/√Hz for $f > 100$ Hz is achievable [39].

2.3.3.2 Shot noise

Shot noise results when charge carriers pass over a potential boundary, is independent of frequency and is given by

$$S_{VS} = 2qI \qquad (2.48)$$

with I the device current. For a current of a few mA, $S_{VS} \approx 10^{-21}$ T/√Hz and thus many orders smaller than the other noise sources and will consequently be ignored in further discussions.

2.3.3.3 1/f noise

1/f noise is a conductivity-modulating noise. Its current spectral density has been experimentally determined to behave according to (2.49).

$$S_{V\alpha} = \frac{\alpha}{n}\frac{1}{f^{\gamma}}V^2 \qquad (2.49)$$

Again V is the voltage over the device, n the total number of charge carriers in the device,

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α is called the Hooge parameter, a dimensionless value that may be associated with a specific device processing method, structure and temperature [57]. Lastly $\gamma \approx 1 \pm 0.1$ [11]. Interestingly the lowest Hooge parameters have been found in Si [10]. 1/f Noise particularly influence µ-Hall sensors due to the lower charge carrier concentration but generally 1/f noise can be virtually eliminated using spinning current techniques [27] with resulting ripple in the order of 100 µT which is equivalent to a magnetic noise density of 1 µT√Hz. A typical vertical Hall device in the 1/f frequency range can achieve around $S_{NB} \approx$ 550 nT√Hz at f = 100 Hz using this method. Making use of novel structures and arrays 50 nT/√Hz is achievable [58, 25]. Other noise reducing structures also exist such as the micro rod antenna manufactured from a Co-rich amorphous wire of 30 µm diameter and ranging between 1 and 10 mm in length. The antenna is placed perpendicular to the sensor and increases the mean magnetic flux density sensed by the Hall device. This increase is a factor that is dependent on the antenna dimensions and the antenna to sensor gap. The antenna serves to modulate the magnetic flux density to the sensor by shifting the spectrum of the useful signal to a frequency band where the sensor excess noise is negligible [57].

2.3.3.4 Generation-recombination noise

Generation-recombination noise is an independent random process causing fluctuations in the number of quasi-free carriers in a device around its equilibrium state at any given moment in time. The noise spectral current density is given by

$$S_{VGR} = \frac{AV^2}{1 + (2\pi f \tau_r)^2}. \qquad (2.50)$$

The parameter A depends on the details of the generation-recombination process [8] as well as device parameters with $A = 4\langle \Delta n^2 \rangle \tau / n^2$ with $\langle X \rangle$ the statistical average of X and Δn the charge carrier fluctuation. The carrier lifetime τ_r is the lifetime of the generation-recombination centre. The reverse junction leakage current also contributes to this type of noise [23].

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2.3.3.5 Combining the noise sources

Figure 2.5 show the combination of the three major noise source contributors and their dominance across the frequency spectrum. The output voltage noise spectral density is given by

$$S_{NV}(f) = S_{VT}(f) + S_{V\alpha}(f) + S_{VGR}(f) \qquad (2.51)$$

with $S_{VT}(f)$ the thermal, $S_{V\alpha}(f)$ the corner frequency or 1/f noise and $S_{VGR}(f)$ the generation-recombination noise spectral densities. Substituting each term with its mathematical equivalent from (2.47) to (2.50) gives

$$S_{NV}(f) = 4kTR + \frac{\alpha}{n}\frac{1}{f^{\gamma}}V^2 + \frac{A}{1 + (2\pi f \tau_r)^2}V^2. \qquad (2.52)$$

In a similar way to (2.44) and (2.45), it is possible to define the noise equivalent magnetic field spectral density by dividing voltage spectral density equation by the absolute sensitivity [11] and thus,

$$S_{NB}(f) = \frac{S_{NV}(f)}{S_A^2}. \qquad (2.53)$$

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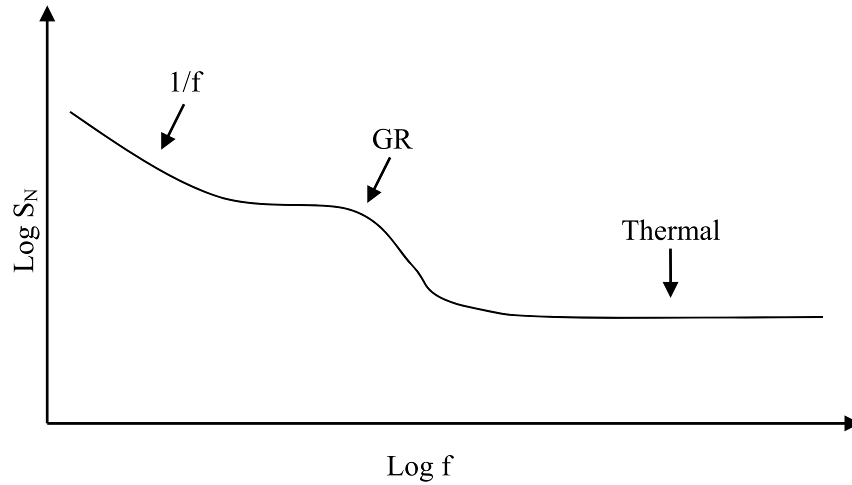

Figure 2.5 Current noise spectrum of a typical unipolar semiconductor device.

2.3.4 Spatial resolution

Spatial resolution is also a convenient method to describe noise and sometimes referred to as the detection limit. Defining the signal to noise ratio as one we can write

$$B_{DL} = \sqrt{S_{NB}(f)\Delta f}. \qquad (2.54)$$

A high resolution is obtainable when the Hall device is large and consists of high mobility material with a low Hooge 1/f noise parameter α and operating at a high level of power [11]. Theoretical resolutions of $B_N \approx 4 \times 10^{-11}$ T have been assessed based on a Hall device with a material mobility of $\mu_H = 6$ $m^2V^{-1}s^{-1}$ operating at P = 0.5 W. Achieving a high spatial resolution however requires a reduction in dimensions. To implement this, it is necessary to reduce the leads of the Hall device causing an increase in resistance as well as heating. This ultimately leads to an increase in noise. Spatial resolution is thus a trade-off between high spatial resolution and the signal to noise ratio. A method of using a focused ion beam (FIB) to pattern a μ-Hall device of a "clover leaf" structure in Bi polycrystalline thin film has been proposed [59]. The 0.25 x 0.25 μm^2 structure was able to increase

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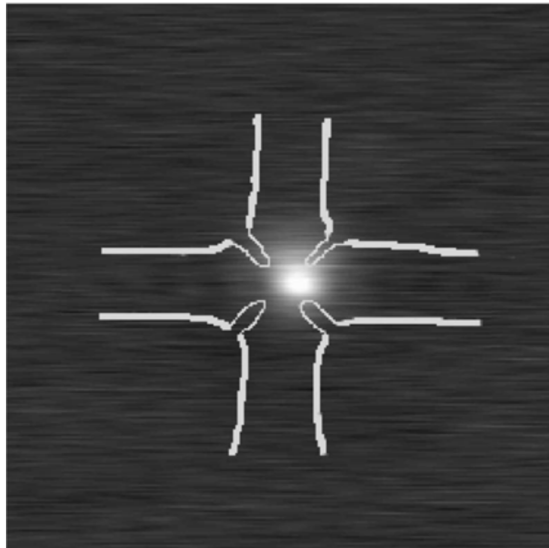
spatial resolution without the expense of increased resistance using this method and is shown in Figure 2.6.

The achievable magnetic field resolution capabilities of the µ-Hall cross, split-current and geometric magnetoresistive sensors have been compared [27]. A resolution of 100 nT/√Hz for a 2.4 µm Si Hall cross was reported. It is believed that Si µ-Hall sensors with a mobility of 0.15 $m^2V^{-1}s^{-1}$ can achieve spatial resolution of down to 30 nT/√Hz at 300K whilst for GaAs Hall devices with a mobility of 0.8 $m^2V^{-1}s^{-1}$ at the same temperature, 2 nT/√Hz is within reach. Other technologies with higher mobility have been demonstrated to achieve higher spatial resolutions for example InSb µ-Hall structures which have a mobility of 8 $m^2V^{-1}s^{-1}$ for bulk devices and 5 $m^2V^{-1}s^{-1}$ for thin film devices are able to detect down to 0.1 nT/√Hz at 300K. Hall cross, split-current and magnetoresistive sensors have a similar dependence on physical and geometrical parameters and for the same active areas, show similar spatial resolutions [27].



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A magnetic field resolution of 100 μT/√Hz at 300 K and 29 nT/√Hz at 77 K for a μ-Hall probe with dimensions 0.85 x 0.85 μm^2 manufactured in GaAs/$Al_{0.3}Ga_{0.7}$ has been achieved [60]. The probe was further expected to achieve 3.1 nT/√Hz at 4.2 K, good enough for imaging Abrikosov vortices in superconducting YBCO high Tc films. The combination of various technologies and methods such as the magnetic concentrator on a combination of geometrically orthogonal Hall plates with active auto-offset calibration analog circuitry is also capable of achieving a resolution of < 100 μT/√Hz at 300K [43].

The spatial resolution was found to be roughly equal to the active part of the Hall cross device [61] and that a flux-meter approximation is not an appropriate model for very close field sources.

2.3.5 Temperature and cross sensitivity

Cross sensitivity is defined as the sensor sensitivity to external environmental factors such as temperature, pressure or even magnetic field cross sensitivity in multidimensional Hall devices [29]. In general, cross sensitivity can be expressed as

$$PC = \frac{1}{S}\frac{\partial S}{\partial P} \qquad (2.55)$$

with P denoting the parameter of interest e.g. T replaces P for temperature and PC becomes TC. S represents the magnetic sensitivity of the Hall device namely; S_A, S_I, or S_V [11]. The higher the Hall coefficient of a material, the higher also its temperature dependant properties [24], a phenomenon Hall himself struggled to quantify correctly during his early studies on the four transverse effects in metals [62]. Early Hall sensors achieved performance within ±0.5% over the -50 to 80 ºC temperature range. VHDs are also sensitive to perpendicular magnetic fields. A magnetic field cross sensitivity for field strengths of between 0.2 and 2 T has been demonstrated [29]. A cross sensitivity of 0.01 $VA^{-1}T^{-1}$ at B = 2 T was shown which corresponds to 1/80000 of the Hall sensor sensitivity

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and is quadratic in nature. In the mT field strength range this is negligible. A temperature coefficient of 4 x 10^{-4} K^{-1} was measured and of the same order as conventional Si Hall plates [29]. Automatic calibration techniques using an on chip calibrating coil can virtually eliminate temperature cross sensitivity and achieve 200 kHz bandwidth using flux concentrator technology [25].

2.3.6 Linearity

Nonlinearity NL can be defined by the deviation of the true output of a Hall device (or any device) from the ideal output [63] and is expressed as

$$NL = \frac{V_H(I,B) - V_{H0}}{V_{H0}} = \frac{\Delta V_H}{V_{H0}} \qquad (2.56)$$

where V_H is the Hall voltage at a given bias current I and magnetic field B. V_{H0} denotes the best linear fit to the measured values. Nonlinearity results from the current-related sensitivity of a Hall device showing a dependence on the magnetic field to which it is being exposed (magnetoresistive effect) or a change in current bias due to other influential parameters such as R_H, G_H or t [11]. The result is a slight deviation from the ideal V_{H0}. Due to the low mobility in Ge and Si, the Hall plate is very linear up to fairly high magnetic fields with deviations occurring in the region where $\mu B \approx 1$ which corresponds to approximately 7 T for Si and 2.5 T for Ge [34]. This dependence must not be confused with magnetoresistive devices which are extremely nonlinear measuring devices [27]. Linearity in the region of 0.04% has been achieved for VHD in high voltage CMOS technology [29]. Apart from being a major contributor to offsets in VHD devices [31], the JFE is a source of nonlinearity in junction isolated devices. The JFE results from the depletion zone around the metallurgical junction of p- and n-doped regions. It is dependent on doping and the reverse voltage at the junction. Depletion extensions of between 0.3 μm and 1 μm were seen for various operating modes and for voltages of between 0 V and 3 V in VHD [55]. These depletion extensions can be calculated as in (2.57).

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$$W_n(V_{pn}) = k_{p/n}\sqrt{V_{pn} + V_{bi}} \tag{2.57}$$

The JFE also causes the effective thickness of the Hall device to vary as a function of the reverse junction bias voltages and is especially affected under constant current biased conditions. Furthermore, the Hall voltage itself causes variability in the reverse bias in the same equipotential line. It is assumed that the surrounding p-type jacket is strongly doped and that it is negatively biased with a constant voltage V_j. Nonlinearity due to the JFE is given by

$$NL_{JFE} \cong \frac{S_{I0}}{G_H r_H}\sqrt{\left(\frac{\varepsilon_s qn}{2(V_{bi} - V_j)}\right)} IB_{\perp} \tag{2.58}$$

where ε_s is the permittivity of the material, V_{bi} the built-in voltage, V_j the voltage potential at the first sense contact and $B_{\perp}$ the perpendicular magnetic field. From (2.58) it can be seen that in contrast to the geometrical and material nonlinearity which are proportional to the square of the magnetic field and independent of the bias current, the JFE nonlinearity is linearly dependent on both [11]. This nonlinearity plays a major role in high sensitivity devices.

2.3.7 Frequency and time response

The fundamental theoretical frequency limit of Hall devices are related to the relaxation time limit of a specific material [11]. Very high frequencies have been demonstrated [64] but generally most applications today make use of much lower limits where inductive and parasitic capacitive effects dominate at frequencies up to 10 MHz [11, 24]. Practical limits of only 1 MHz are achievable in systems as a result of interfacing electronics. The electroplated on-chip planar coil solution has reduced impedance at high frequencies in comparison to thin film technologies ultimately resulting in higher Hall voltages. This is

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however at the cost of increased area as electroplating has lower metal separation spacing as well as complexity [44].

2.3.8 Stability and Drift

Stability refers to the relative change in sensitivity over time and is directly proportional to the Hall coefficient which itself is not an absolute quantity. The piezo-Hall effect for example can be responsible for up to 2.5 % change in its value due to mechanical stress. Another factor influencing the stability is due to surface effects such as surface charge carrier density variations changing the nt product as well as localized electron traps due to surface imperfections.

Current spinning and chopper stabilized Hall elements can reduce the offset induced part of the piezoresistive and piezo-Hall effects but not its influence on sensitivity and temperature effects [25]. The problem with high sensitivity sensors is that high sensitivity and low thermal drift are in contradiction. Thermal drift is a direct function of temperature (voltage biased devices) and JFE variation with temperature affects plate thickness (current biased devices). 2D Heterostructure Hall devices are used to solve this with a sensitivity of 900 $VA^{-1}T^{-1}$ and -0.016%/℃ or -160 ppm/℃ achieved [40].

Hall devices making use of integrated magnetic flux concentrators may also suffer from magnetic shocks causing the ferromagnetic components to be slightly magnetized resulting in offset changes and is referred to as perming [11]. Problems with the planar coil solution cause a change in performance over time and are a direct result of excessively high currents through the coils resulting in self-heating [44]. It is possible to compensate and actively adjust the output for a thermal drift in resistance for example by using the same material as the Hall device (typically n-well) as a reference [65, 66]. The double Hall device from [51] showed an offset drift of < 11 μV/℃.

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2.3.9 Geometry

The geometries in 2.2.3.1 and 2.2.3.2 describe Hall devices of very long or very short rectangles. In reality these devices are not practical and will always have a shape somewhere in between the two extremes as shown in Figure 2.7 as well as a combination of the various galvanomagnetic effects.

For an arbitrary aspect ratio, current is forced along the isolating boundaries and thus a strong equipotential inclination generates a strong Hall electric field. The magnetoresistance effect will also be measurable in this region. Around the ohmic pickups used to sense the Hall voltage, the Hall field will experience a short circuiting and thus, in this region, results in current deflection and geometrical magnetoresistance effects.

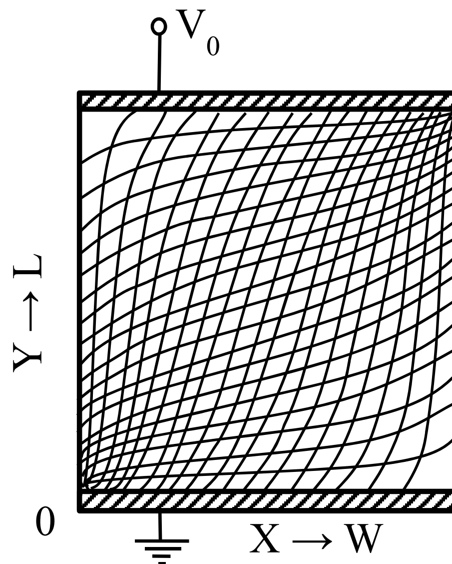

Figure 2.7 A square plate numerical model with w = l and no sense contacts under the influence of a perpendicular magnetic field. Taken from [127] with permission.

Lastly, the region in the middle of the device, the equipotential and current lines are

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moderately inclined. The net effect is a Hall voltage being generated slightly less than is the case for an infinitely long geometry and is described by the *geometrical correction factor* as expressed in (2.59)

$$V_H = G_H V_{H\infty} \qquad (2.59)$$

with V_H the Hall voltage and $V_{H\infty}$ the Hall voltage of a corresponding infinite length plate, all else being equal. The geometrical factor thus represents a reduction of the Hall voltage and is directly related to the non-perfect current confinement conditions in a finite length Hall device. Furthermore, it takes on a value between 0 and 1 with $G_H = 1$ for an infinitely long plate and $G_H = 0$ for an infinitely short plate. Equation (2.11) and can thus be rewritten as

$$V_H = G_H \mu \frac{w}{l} V B_{\perp}. \qquad (2.60)$$

and

$$I_H = G_H \mu \frac{w}{l} I B_{\perp}. \qquad (2.61)$$

The two most important structures are the Hall plate and the VHD as these geometries match the requirements of a good Hall device and the CMOS technology used for its implementation very well.

It was proved that the Hall plate's electrical efficiency is independent of geometry and that all shapes can be mapped between each other known as the conformal mapping theory [67]. The essence of conformal mapping theory can be summarized as follows [11] as is illustrated in Figure 2.8:

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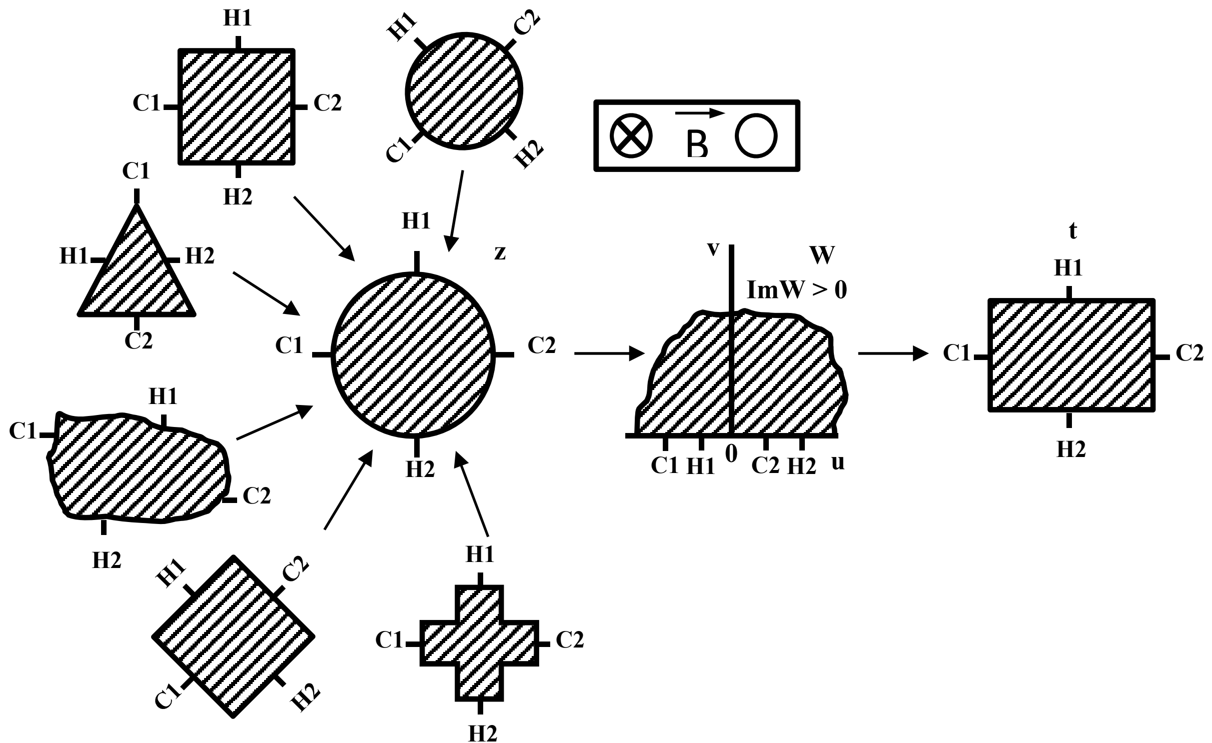

Figure 2.8 A visual representation of geometrical equivalence under the conformal mapping theory. Taken from [38] with permission.

- Regarding the geometrical factor, all Hall device shapes are equivalent (Figure 2.8),
- a long Hall plate is equivalent to a small contact device,
- the Hall voltage varies with the distance from the current bias contacts (Figure 2.9),
- finite sized voltage sensing contacts cause a reduction of the geometrical correction factor similar to the way finite sized current supply contacts do.

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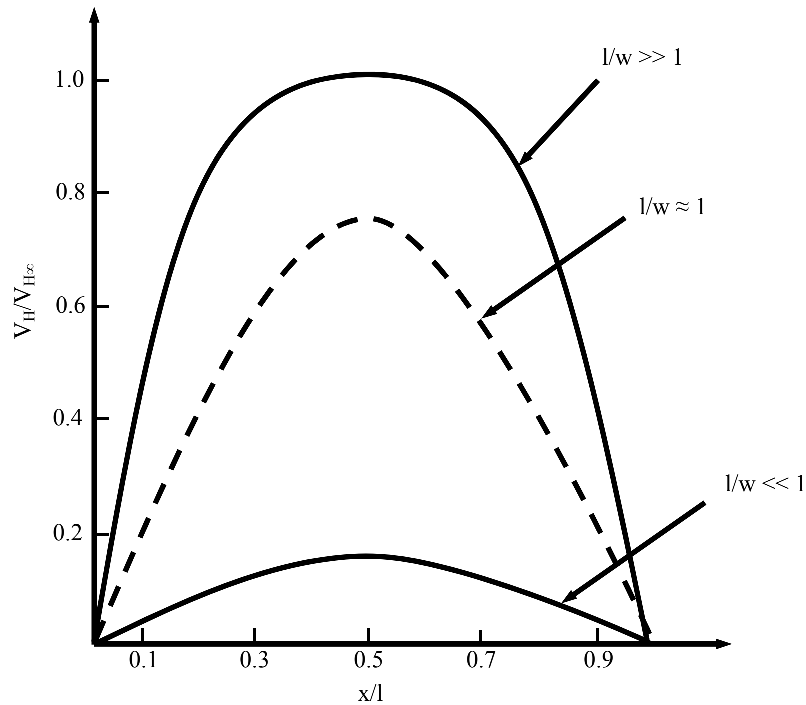

Figure 2.9 Graph illustrating the influence of the sensor contact at position x along the length l, for various lengths to width ratios l/w. Taken from [72] with permission.

2.3.9.1 Hall plates

Figure 2.10 shows some commonly used geometrical shapes [11]. Conformal mapping indicates the independence of performance on geometry but in practice this is not always true when considering additional properties. These include ease of manufacturing, Joule heating and available area to name but a few making a specific shape better suited to a specific application than another. In Figure 2.10(a), the rectangular plate makes a good approximation of a Hall strip. High geometrical factors can only be achieved for very small contacts. Conventional Hall devices (macro devices) have a typical active area of larger than 10 µm x 10 µm. Hall cross devices as small as 0.1 µm x 0.1 µm have been manufactured in Bi and smaller than 10 µm x 10 µm have been manufactured in Si, GaAs

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and heterostructures [27]. Some variations of the standard plate such as the open back plate have also yielded good results. The thickness of the plate is thus a function of the current path namely its depth and diffusion through the structure. The sensitivity of the device as a function of the plate thickness is thus rather a function of the effective current thickness which can be translated to an effective thickness of the plate and is dependent on the plate size whilst fixed plate thickness as a result of a fixed boundary is not [41]. An infinitely long strip can be approximated by the bridge device in Figure 2.10 (b) as it is less sensitive to larger contacts as is the case for the rectangular Hall plate. Large contacts can be used as no current flows (also the reason for very high geometrical factor) in this region making this shape well suited to technologies where the ohmic contacts have high resistances but can use a larger area for its implementation.

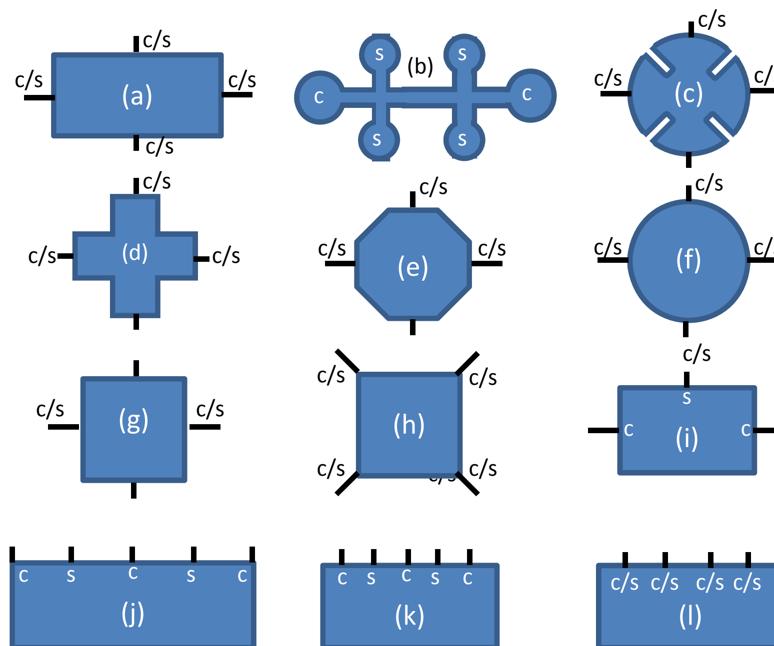

Figure 2.10 Illustration of various Hall geometries with signal contacts s and current contacts c.

The van der Pauw shape, or more commonly the clover-leaf in Figure 2.10 (c) is a macro version as used in Figure 2.6 and in principle a four contact equivalent of the bridge device

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as is the cross-shaped device in Figure 2.10(d). These two shapes possess all the advantages of the bridge device but are simpler to implement as well as less area intensive. The Hall cross is a very convenient implementation for the use of 1/f noise reduction techniques [27]. Devices Figure 2.10(g) and Figure 2.10(h) have the same active area but have their contact points rotated by 90° and are thus complementary or dual structures of each other. The rectangular plate in Figure 2.10(i) makes use of only one sensing contact which can be measured against a stable reference voltage but suffers from a reduction of the Hall voltage by two. The plate in Figure 2.10(j) consists of two adjacent single contact devices and thus the Hall voltage is the sum of two half Hall voltages. These two configurations are only useful if a single side of the Hall plate is accessible to make contact.

Conformal mapping theory was used as basis for the invention of the parallel or vertical Hall device (VHD) [38] as shown in Figure 2.10(k) and Figure 2.10(l). Thus, these two VHDs can be designed to be electrically equivalent to the plates from Figure 2.10(a) to Figure 2.10(h). The VHD is well adapted to angular position sensing. High voltage CMOS technology is very suitable for VHD implementation as it allows for deep n-wells of about 7 μm [29, 68, 69]. Typical thin n-wells of a standard CMOS process is around 2 μm and this causes current to flow through the sensing contacts instead of around them [58]. It is possible to overcome this limitation through the use of contacts outside the current path but this method does not reduce offsets, 1/f noise or short circuiting effects completely. The maximum sensitivity achievable however still seems to be independent of contact position and is limited to between 30% and 40% of the maximum sensitivity achievable in standard Hall plates [58]. The sensitivity of the structure thus becomes geometry size dependant reminiscent of the open back Hall plate by [41]. The one problem with the VHD is that they have lower sensitivities and higher offsets directly related to the processing technology used and new methods for modelling these offsets are continually being researched [31]. VHDs make the development of integrated 3D Hall probes possible but are also the cause of the overall performance limitation stemming directly from its intrinsic

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structure. 2D finite element analysis has been used to demonstrate this [7]. Performance can be enhanced using various non-standard techniques such as the gated VHD integrated with Si on Insulator (SOI) CMOS whereby a gain in performance of almost ten times was achieved over a conventional VHD [70].

2.3.9.2 Geometrical correction factor

Equation (2.59) described the generic expression of the geometrical correction factor. The geometrical factor is one of the most important parameters in this study and will be the measure against which the hypothesis will be tested. The factor itself is dependent on the Hall angle. Figure 2.11 illustrates in a simplified way how a stronger magnetic field results in a larger Hall angle thus forcing the portion of the current flowing parallel to the boundary to increase. As the Hall field only develops in a Hall device with isolating boundaries such that the current flowing is confined to run parallel to it, the Hall field in Figure 2.11(b) will be less affected by the short circuiting effects of contacts than in Figure 2.11(a). In a real device, Figure 2.11(b) appears longer than Figure 2.11(a) and thus will have a higher geometrical correction factor [11]. Furthermore, from Figure 2.11 it is evident that the larger the Hall angle, the larger the geometrical factor which tends to unity as the Hall angle θ_H tends to $\pi/2$ [11].

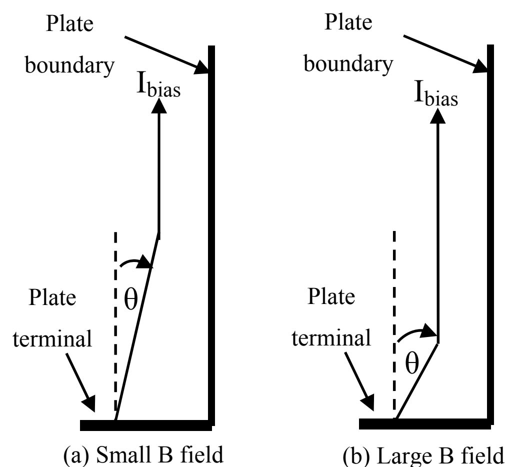

Figure 2.11 The effect of the Hall angle on the geometrical factor.

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The signal contacts s, in Figure 2.10 are effectively reduced to point contacts when shrinking its dimensions to zero, i.e. s = 0. Figure 2.12 shows the geometrical factor's dependence on the length-to-width ratio l/w and the Hall angle θ_H for a rectangular device with such point contacts positioned midway between the current contacts c [71, 72]. From Figure 2.12 it can be seen that for a l/w ratio > 3, the rectangular shape begins to act as if it were an infinitely long strip.

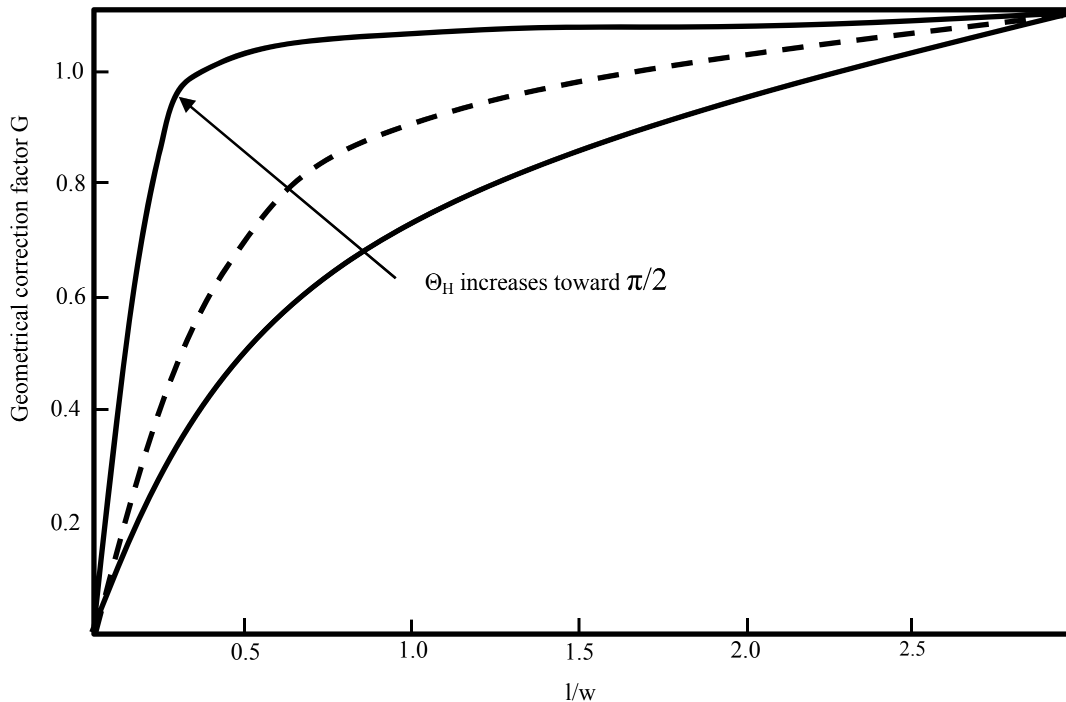

Figure 2.12 The geometrical correction factor and its dependence on the l/w ratio as well as the Hall angle. Taken from [72] with permission.

The geometrical factor for a point contact rectangular Hall device is approximated by

$$G_H \cong 1 - \frac{16}{\pi^2} e^{\left(-\frac{\pi l}{2w}\right)} \left[1 - \frac{8}{9} e^{\left(-\frac{\pi l}{2w}\right)}\right] \left(1 - \frac{\theta_H^2}{3}\right) \tag{2.62}$$

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and is true for $0.85 \leq l/w \leq \infty$ and $0 \leq \theta_H \leq 0.45$ with θ_H in radians.

The geometrical factor for a more practical device with a small Hall angle and small sense contacts such that $s/w < 0.18$ and $l/w > 1.5$ can be approximated by

$$G_H \cong \left[1 - \frac{16}{\pi^2} e^{\left(-\frac{\pi l}{2w}\right)} \frac{\theta_H}{\tan\theta_H}\right]\left(1 - \frac{2}{\pi}\frac{s}{w}\frac{\theta_H}{\tan\theta_H}\right). \qquad (2.63)$$

Equation (2.63) consists of two parts, the first inside the square brackets and the second inside the round brackets. These parts represent the contribution due to the current and sense contacts respectively.

Lastly, for a short rectangular Hall device with point sense contacts, the geometrical factor is approximated by

$$G_H \cong 0.742\frac{l}{w}\left[1 + \frac{\theta_H^2}{6}\left(3.625 - 3.257\frac{l}{w}\right)\right]. \qquad (2.64)$$

For a Hall cross device, the geometrical factor as illustrated in Figure 2.13 was calculated [73] with m the relative Hall angle calculated by (2.65) and λ in (2.66), the ratio of the sum of lengths of contacts and the total length of the plate boundary defined as in Figure 2.10 (d).

$$m = \frac{\theta_H}{\pi/2} \qquad (2.65)$$

$$\lambda = \frac{2s}{4k + 8h} \qquad (2.66)$$

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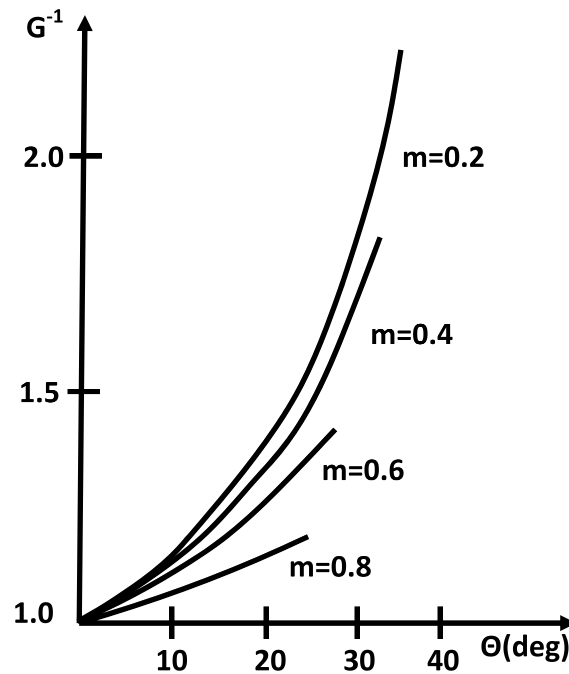

Figure 2.13 The reciprocal of the geometrical correction factor for a Hall cross device. Taken from [128] with permission.

2.3.10 Testing

Due to process variation and general imperfections it is necessary to ensure the testability of a Hall device such that it conforms to the desired target specifications. Hall devices need to be stimulated with application relevant signals (mostly external magnetic fields [74]) under various conditions such that effects such as offsets, temperature drift, nonlinearity or any such unwanted effects can be characterized and compensated for. The most common solution for this is by making use of electrically programmable read only memory (EPROM) whereby measured parameters are stored and can be recalled and used to compensate the devices under specific conditions requiring it. But such external magnetic field generators may themselves cause undesired variability and increase the cost of testing. A method using an on chip coil that is immune to self-heating has been proposed [74], reduces cost and is applicable over a wide temperature range of -40 ºC to 150 ºC. The

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solution makes it possible to do real time or self-calibration and is capable of producing a magnetic field in the range of 2-5 mT with only a few tens of mA. Challenges to achieve high accuracies however include, ringing, hot spots, temperature drift and cooling. Of these, temperature drift can be kept at a minimum as long as measurements are done faster than a few ms. Local hot spots can be significantly reduced using µs range spinning current methods. Along with a maximum current of 50 mA, a very specific coil current profile was devised to minimize all the mentioned effects. For every 1 mA of coil current, a three turn integrated coil can provide a calibrating magnetic induction of 0.15 mT [25].

2.4 THEORETICAL LIMITS

Designing a Hall device well suited to a specific application in standard CMOS technology, requires not only an understanding of applicable design theory as discussed in 2.2 and 2.3, but also an understanding of fundamental limitations. These include both theoretical limits based on solid state physics as well as general practical limitation drawn from the vast knowledge base available. For example early Hall device offsets were highly driven by the asymmetrically located contacts and imperfections of both materials and contacts and offset were reported in the range of between 20 µT and 1 mT [24].

Voltage sensitivity can be increased by keeping a constant bias voltage whilst decreasing the effective length of the Hall plate but once the plate becomes too short, the mode of operation changes from Hall voltage to current deflection. The maximum voltage sensitivity achievable under this condition becomes limited to the maximum geometrical factor achievable for a short device. From (2.64) with a very small Hall angle such that θ_H is approximately zero and l = w, G_H reduces to $G_H = 0.742$ and the maximum voltage sensitivity is given by

$$S_{Vmax} = 0.742\mu_{H.} \qquad (2.67)$$

This implies a maximum voltage sensitivity of $S_{Vmax} = 0.126\ T^{-1}$ and $S_{Vmax} = 0.67\ T^{-1}$ for

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low doped n-type Si and GaAs at 300 K respectively [11]. The maximum sensitivity for the Hall current mode is given by

$$S_{Imax} = S_{Vmax} I = 0.742 \mu_H I \qquad (2.68)$$

Of course the mobility is directly related to the material [34]. (2.67) is also based on the assumption that electron drift velocity saturation has not yet occurred. For large geometries this is normally no problem but for μ-Hall devices this becomes a limiting factor for Si at approximately 30 $kVcm^{-1}$. For a bias voltage of 5 V for example, this corresponds to a minimum length of 1.5 μm [11]. Scaling down of lateral dimensions also leads to an increase in noise on the Hall voltage [8] which tends to dominate in smaller dimensions [27].

Linearity is also a function of the strength of the magnetic field (see (2.3)). Hall devices have a linear response up to $\mu B \approx 1$ after which electrons start to deviate prior to their next collision [34]. This implies that the maximum allowable field is material dependant and about 7 T for Si and 2.5 T for Ge [34]. A *very weak* magnetic induction is based on a more stringent definition as in (2.69) where for all carrier energies

$$\mu^2 B^2 \ll 1. \qquad (2.69)$$

Assuming $\mu^2 B^2 < 0.1$, this implies a maximum magnetic field strength of B = 2.1 T for Si and B = 0.81 T for Ge [11, 31].

For measuring the spatial signature of a specific magnetic field it is necessary to reduce the active area of a Hall sensor. This is due to the fact that active area causes an averaging of the magnetic field. This is of specific interest in the field of superconducting nanostructures. As mentioned earlier, μ-Hall sensors are more prone to noise and this

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becomes the fundamental limiting factor for the minimum detection level also called the detection limit [8]. [8] Investigated the magnetic detection limit for GaAs/AlGaAs III-V heterostructures as well as for Si. From (2.36) and (2.46) the Hall device magnetic detection limit DL can be calculated as

$$DL = \sqrt{\left(\int_{f_1}^{f_2} \frac{S_{NV}(f)}{(IS_I)^2} df\right)} = \sqrt{\left(\int_{f_1}^{f_2} B_N^2(f)\, df\right)}. \qquad (2.70)$$

Now substituting (2.52) into (2.70) and studying the noise around a specific frequency of interest f, then a very small bandwidth $\Delta f = f_2 - f_1 << f$ yields

$$DL = \sqrt{\frac{4kTR}{(IS_I)^2} + \frac{\alpha R^2}{nfS_I^2} + \frac{R^2}{n^2 S_I^2}\frac{4\langle\Delta n^2\rangle\tau}{1 + (2\pi f\tau)^2}} \times \sqrt{\Delta f}. \qquad (2.71)$$

Again the three terms represent the thermal, 1/f and generation-recombination contributions to the noise equivalent magnetic field. From (2.71) it can be seen that any thermal noise contributions can be reduced by increasing the bias current I through the Hall device in a frequency range where thermal noise tends to dominate. Maximum current however must be limited such that charge carrier mobility degradation due to joule heating is avoided as well as the maximum electric field over the Hall device such as to avoid saturation of the carrier drift velocity. 1/f noise can be reduced by reducing α and increasing the number of available charge carriers n. This implies that larger Hall devices typically have better 1/f performance. Lastly for materials with dominant generation recombination noise, the noise is inversely proportional to n and thus at those frequencies the detection limit will show a dependence on the Hall device size [8].

For VHDs, the limits of the offsets were determined [7] to be about 400 μT with minimum resolutions of 100 μT over a 1.6 kHz bandwidth in comparison to standard Hall plate of <

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20 µT for both. The residual offset limits using spinning current technique was investigated [75] and it was found that a residual offset must be accepted for constant voltage bias even whilst using all four directions of a linear and symmetrical device. Under this condition, the technique can suppress the equivalent magnetic offset of a Hall device with a resistive nonlinearity of 10 %V^{-1} (due to JFE) to around 1 µT. A constant current supply can reduce this further down to 100 nT as long as the current is kept below the maximum allowable power dissipation level to avoid joule heating and thus carrier mobility degradation. Lastly, the average offset for four orthogonal current directions is half the average of two orthogonal current directions. It seems however that signal conditioning circuits' residual offsets and thermo-magnetic effects dominate Hall device performance [75].

Best bandwidths achievable commercially seem to be limited by the switching noise and output filter cut-off frequencies of the widely popular spinning current technique at 30 kHz with noise levels of 50 µT peak to peak (10 Hz to 10 kHz) and 1 mT offsets [43]. On-going research has already demonstrated bandwidths up to 500 kHz are achievable in VHDs and is also the highest reported thus far [69] rivalling high bandwidth microelectromechanical system (MEMS) sensors [76].

Geometries are also differently affected by noise as reported by [27]. For a µ-Hall cross sensor the Hall voltage is given by (2.18) and (2.36). The output resistance becomes

$$R = R_0 M \cong \frac{1}{\sigma_0 t}\frac{l}{w} M = \frac{1}{\mu q n t}\frac{l}{w} \qquad (2.72)$$

with R_0 the output resistance at zero magnetic field, M the magneto-geometrical factor which is dependent on µB and l/w. Substituting (2.72) into (2.70) gives the magnetic field resolution in the thermal noise frequency range as

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$$B_{min} = \frac{\sqrt{4kTR}}{S_I I} = \frac{\sqrt{4kTM}}{v\sqrt{\mu qn}G\left(\frac{w}{l}\right)\sqrt{wtl}}. \qquad (2.73)$$

For a constant bias voltage, scaling down μ-Hall devices causes an increase in the electric field E. Decreasing the dimensions further causes the drift velocity of the charge carriers to rise causing the device temperature to increase. This in turn increases the carrier density n thus reducing the mobility μ. Thus for μ-Hall devices, the saturation velocity of charge carriers is the main limitation in (2.73) and is dependent on the type of material used. Saturation electric fields vary between 0.1 and 100 $V\mu m^{-1}$. Saturation velocities for all semiconductors fall between 10^5 and 10^6 m/s. G(w/l) maximizes to approximately 0.4 for l/w ~ 2 and M minimizes to approximately 1 for weak magnetic fields, i.e. $\mu B << 1$. This reduces (2.73) to

$$B_{min} = \frac{\sqrt{4kTR_0}}{v_{sat}w}. \qquad (2.74)$$

It can be seen from (2.74) that scaling down the Hall cross active area for a constant thickness t results in a reduction in magnetic field resolution. Equation (2.74) also defines the minimum resolution for short Hall devices used in current deflection mode.

2.5 MODELLING FOR SIMULATION

An important part of the design phase is being able to accurately model the Hall device in question. The Hall plate is well modelled with the aid of a Wheatstone bridge [28]. Figure 2.14 for example shows its application to model the offset voltage due to mechanical shear stresses in a Hall cross device.

Under zero shear stress, or a stress applied along the main crystallographic axis, the Wheatstone bridge remains symmetrically balanced and no offset voltage can be measured

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between the measuring points S_2 and S_1. A shear stress however causes the loss of vertical and horizontal symmetries which results in an opposite absolute value change in adjacent resistors ultimately forcing an offset voltage to appear between the two sensing points [28].

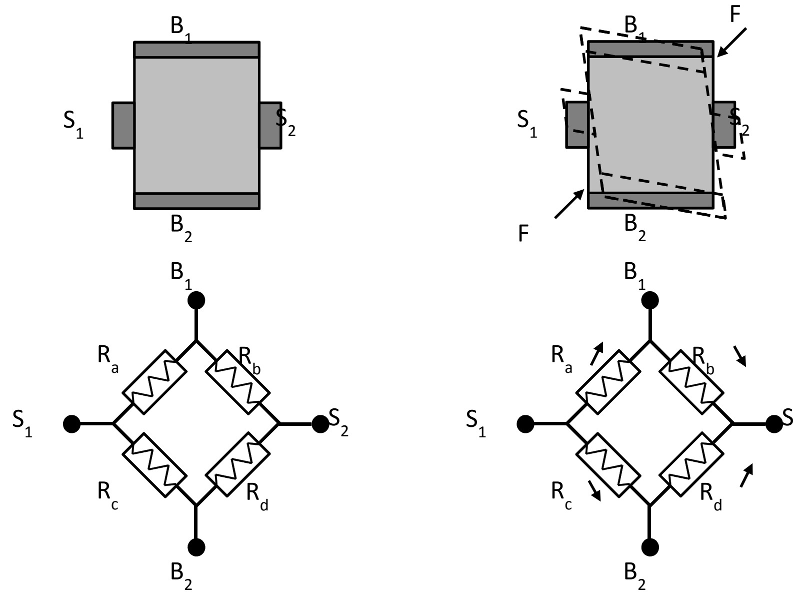

Figure 2.14 The modelling of the mechanical effects of a Hall device with the aid of a Wheatstone bridge [28] with permission.

More complex behaviour of the Hall cross sensor can be modelled with conventional components [77] as shown in Figure 2.15. NTY and NTX represent non-linear resistors with the following function;

$$R_{NT}(V_{NT}) = a_1 + a_2 V_{NT} + a_3 V_{NT}^2 \quad (2.75)$$

with fitting parameters a_1, a_2 and a_3. FYI and FXI are current controlled current sources (CCCS) used to simulate the magnetic field and controlled by current measured by VIY and VXY. The current gains are calculated as follows;

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$$K_{xy} = \mu_H B \frac{\Delta x}{\Delta y} \tag{2.76}$$

and

$$K_{yx} = \mu_H B \frac{\Delta y}{\Delta x} \tag{2.77}$$

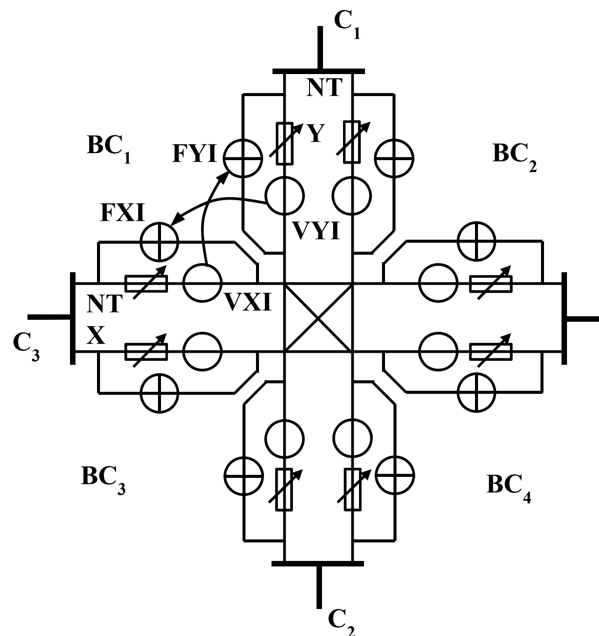

Figure 2.15 A macro model for simulating the Hall cross device. Taken from [77] with permission.

with μ_H the Hall mobility of the majority carriers, B the magnetic field and $\Delta x/\Delta y$ the length-to-width ratio of the resistors. The model was tested in SPICE for weak magnetic inductions to keep any magnetoresistive effects negligible against 3D simulations with fairly good agreement [77].

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The advancement in simulation tools with incorporation of powerful analog description languages have spawned improved modelling methods for simulating the Hall cross [78] depicted in Figure 2.16.

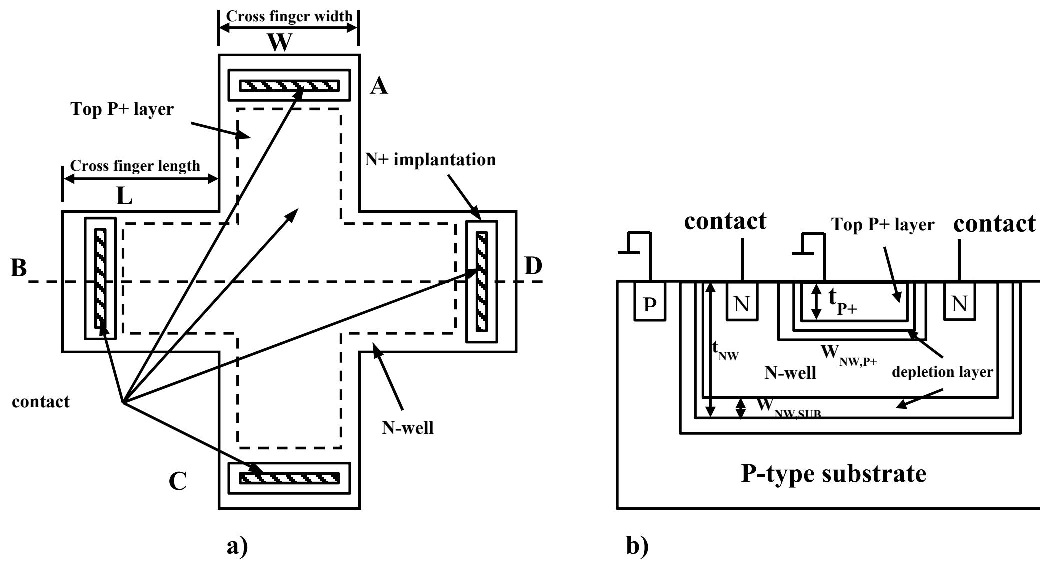

Figure 2.16 Top and cross sectional view of a Hall cross. Taken from [78] with permission.

The model covers voltage dependent non-linear, geometrical, temperature and packaging stress effects not taken into account using the standard Wheatstone bridge model as depicted in Figure 2.14. The model is based on 8-resistors with conventional JFETs normally used to model the JFE replaced by passive non-linear resistances and depletion capacitances. The model is valid for weak magnetic fields and illustrated in Figure 2.17.

The components are calculated with the help of Equations (2.78) to (2.82). R_H and R_D is a function of the length l, the width w and the sheet resistance R_s.

$$R_H = \frac{2R_s}{\pi}\left[\left(2\frac{l}{w}+\frac{2}{3}\right)\pi - 2ln(2)\right] \quad (2.78)$$

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$$\frac{R_H}{R_D} = 2 - \frac{8}{\pi}\frac{ln(2)}{2\frac{l}{w}+\frac{2}{3}} \qquad (2.79)$$

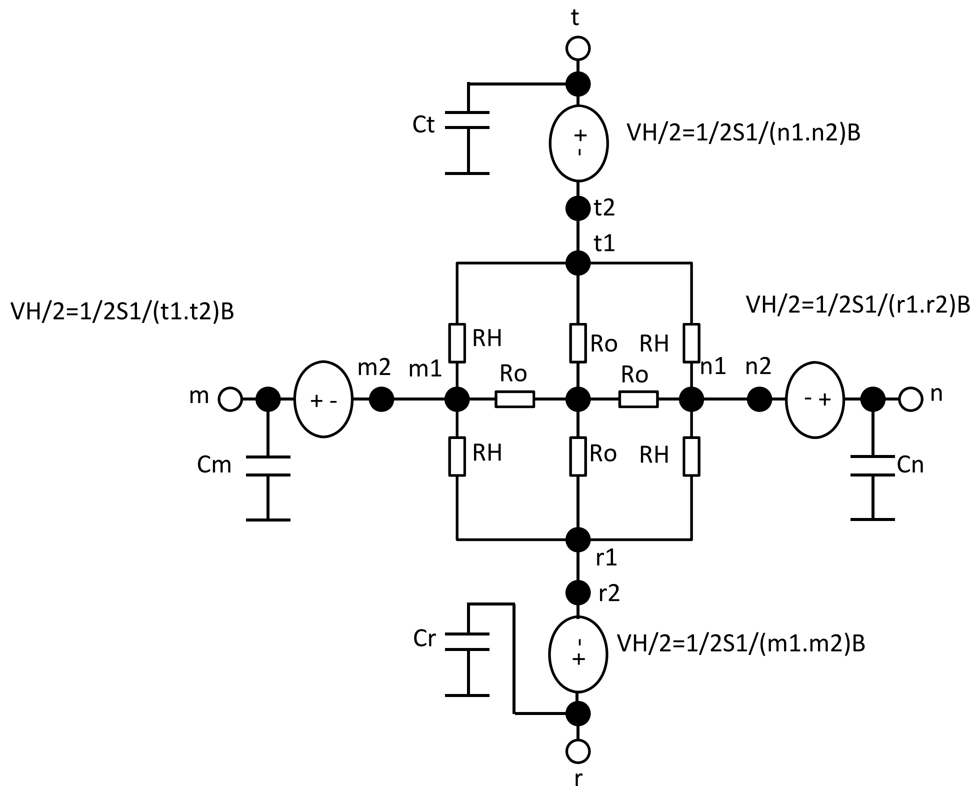

Figure 2.17 A macro model for simulating the Hall cross device including second order effects. Taken from [78] with permission.

$$R_s = \frac{1}{q\mu_n N_D t_{eff}} \qquad (2.80)$$

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$$C_{pn} = \sqrt{\frac{q\varepsilon_{si}N_D N_A}{2(N_D + N_A)}}\left[V_{bi} - V_{pn} - \frac{2kT}{q}\right]^{-\frac{1}{2}} \tag{2.81}$$

The junction capacitance C_{pn} is calculated with (2.81) where V_{bi} is the built in potential of the PN junction, ε_{si} the permittivity of Si, N_D and N_A the donor and acceptor doping concentrations respectively, k the Boltzmann's constant, T the absolute temperature, q the charge of an electron and V_{pn}, the reverse biased voltage (see Figure 2.16).

$$V_{H/2} = \frac{1}{2}S_{VI}I(n_1, n_2)B \tag{2.82}$$

Finally, each half Hall voltage $V_{H/2}$ is calculated using a current controlled voltage source as in (2.82) with S_{VI} the sensitivity based on constant current bias in Hall voltage mode of operation, B the magnetic field and $I(n_1,n_2)$ the current flowing between nodes n_1 and n_2. The sensitivity S_{VI} takes into account geometrical parameters due to the inclusion of the geometrical correction factor for a Hall cross device. The sheet resistance in (2.80) can be expanded further to include other higher order aspects such as effective dependence on the change of the thickness, voltage and temperature dependencies. Finally, the sensitivity can also be expanded to include its dependence on the piezoresistive and piezo-Hall effects [53, 46, 47, 48]. The model was tested against an implemented Hall device in 0.8 µm CMOS technology with good agreement between simulated and measured results [78].

Modern modelling of the 5C VHD have been improved by taking into account the multiple modes of operation not fully accounted for in older models [79].

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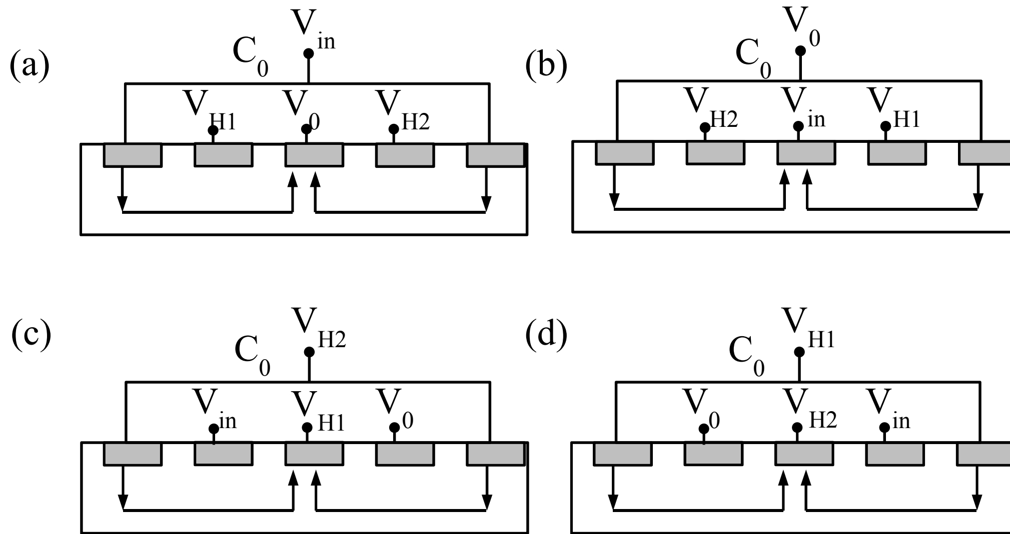

Figure 2.18 The four modes of operation of the 5C VHD. Taken from [31] with permission.

Figure 2.18 shows the four modes of operation of the 5C VHD with modes 1 to 4 illustrated by (a) to (d). The offset voltage can be modelled with the following second order polynomial [31, 55].

$$V_{off,i}(V_{in}) = A_i V_{in} + B_i V_{in}^2 \quad (2.83)$$

Here i represents the four modes, $V_{off,i}$ is the offset of each mode and A_i and B_i the linear and quadratic coefficients. The coefficient A_i is mainly dependent on the differences of the resistances of the two inner and two outer segments respectively whilst B_i is mainly dependant on the mismatch of the JFE between the inner and outer segments [55]. The physical model for (2.83) can be equated to a lumped resistor as is illustrated in Figure 2.19 (a) which can further be expanded into an equivalent Wheatstone bridge as in Figure 2.19 (b). The interested reader is referred to [31] for a detailed method of resistor calculations.

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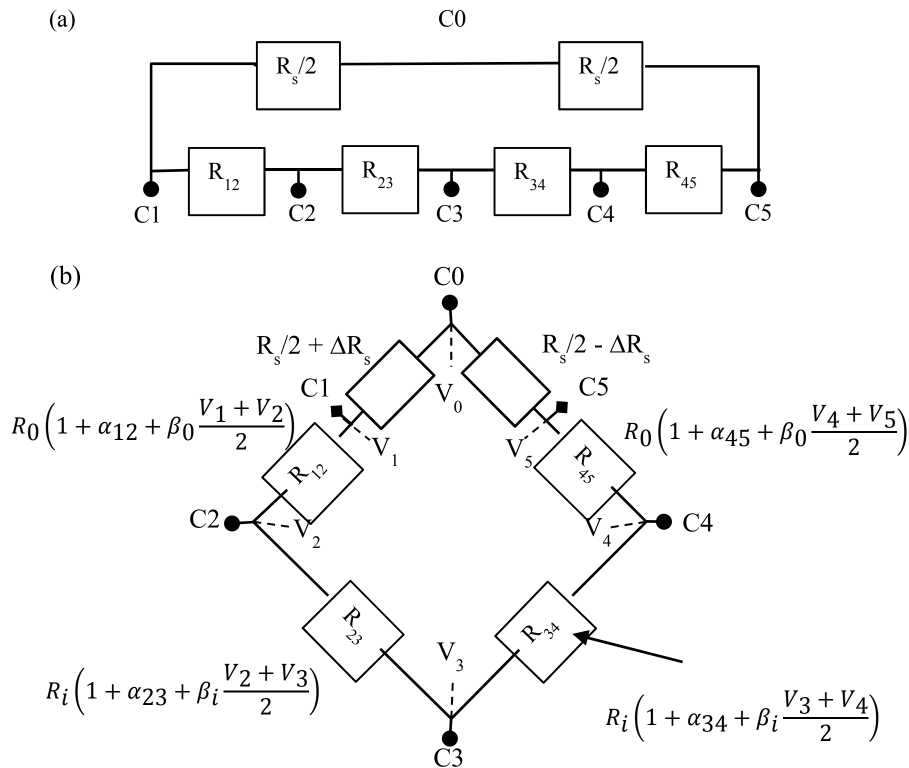

Figure 2.19 The equivalent lumped resistor model of the 5C VHD. Taken from [31] with permission.

Although a few of the models discussed take packaging effects into account, simple models can hardly begin to model these effects accurately [80]. Table 2.2 shows the influence various geometries and material parameters may have on the stress in moulded sensors after assembly and packaging.

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Table 2.2 The influence of different parameters on modelling package effects in Hall devices

Type	Parameter	Influence
Material parameter	Adhesive classic properties	+
	Adhesive shrinkage	0
	Adhesive time dependent properties	+
	Moulding compound elastic properties	++
	Moulding compound shrinkage	++
	Moulding compound time dependent properties	++
Geometry parameter	Thickness lead frame	+
	Thickness adhesive	0
	Thickness silicon	+++
	Thickness moulding compound	++

Packaging affects mainly the offset and sensitivity of Hall devices. This is due to the differences in thermal expansion coefficients between packaging materials as well as their time dependent viscous properties also called thermo-mechanical stresses. These properties manifest themselves in the Hall devices via the piezoresistive and piezo-Hall effects. Proper modelling requires the inclusion of these thermo-mechanical effects, shrinkage and the viscoelastic and viscoplastic behaviour of the packaging materials [80]. Reasonable accuracy has been achieved [80] to within 20 % also reveals how comprehensive knowledge about the material properties is fundamental to any reasonable simulation outcome.

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2.6 APPLICATION, TRENDS AND STATE OF THE ART

2.6.1 Sensor classification

Sensors are typically classified by the measurand [12]. This is the most fundamental quantity that a chosen sensor will measure and is also referred to as the primary quantity. Physical quantities can be subdivided into families for example electromagnetic, mechanical etc. This is shown in Table 2.3.

Table 2.3 List of sensor measurands

Measurand	Application	
Solid-mechanical	Displacement	Mass
	Position	Force
	Strain	Stress
	Speed and velocity	Torque
	Acceleration	
Fluid-mechanical	Density	Liquid level
	Flow rate	Pressure
	Humidity	Viscosity
Electromagnetic	Current	Magnetic induction
	Voltage	Electric flux
	Power	Magnetic flux
	Electric field strength	
Other	Temperature	Color
	Heat flux	Nuclear radiation
	Light intensity	Chemical

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2.6.2 General

Hall sensors have been the most widely used magnetic sensors for more than two decades [25, 69]. Applications are widely spread covering all four measurand domains in Table 2.3.

Interestingly enough, before the advent of μ-Hall devices they were relatively rarely used as linear magnetic sensors. Hall sensors are mostly applied as contactless sensors for linear position, angular position, velocity, rotation and electric current with a notable increase in new found applications in the last five years [81, 82, 83, 84, 8]. Hall sensors are extensively applied in automotive, ventilators and disc drives [25].

2.6.3 Linear position sensor

Early sensors called Gauss meters reported measurement capabilities from a few hundred μT to single digit T range and from these sensors it was possible to also produce linear magnetic control sensors using a known reference and field regulation of better than 0.5 ppm could be achieved [24]. Linear sensors can be divided into 1D, 2D and 3D applications.

2.6.3.1 1D

For most linear displacement sensors, offset and temperature drift remains the biggest challenges for applications requiring very accurate measurements. Novel ideas to combat this continue to be a main focus area of research such as the dual horizontal Hall device [85]. The device is capable of compensating for offset and temperature drift and is calibrated using external resistors. The output signal gets summed using operational amplifiers and the lowest detectable magnetic field was 12 μT in a frequency range of 1 Hz to 100 Hz. The sensor was specifically aimed at geotechnical applications such as testing the compression of soil or rock samples. It demonstrates a linear resolution of 1 mV per μm for a full range of 3000 μm ± 0.3% within a temperature range of 10℃ to 40℃. A VHD version was demonstrated by [86] which in principle is a conformal mapped version of [85]. A sensitivity of 40 $VA^{-1}T^{-1}$ was achieved with a nonlinearity < 0.8 % in a magnetic field range of ± 1.5 T. The lowest detectable magnetic field was 7 μT with an offset of

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approximately 0.9 mT. The temperature dependent performance was 0.1 % /℃.

2.6.3.2 2D

The compatibility of the VHD with HV CMOS deep n-well technologies makes it a very suitable candidate for 2D sensors when multiple devices are placed orthogonally as for example the six contact 360 ° angular sensor described by [68]. The device achieves a fair sensitivity of 0.035 $VV^{-1}T^{-1}$. Different orientations cause angular misalignment of ±0.4° mainly due to photolithography limitations as well as gain differences in the region of 0.3 %. The gain difference is kept to a minimum by making use of the same analog electronics via time division multiplexing. Nonlinearity is reduced from 0.14 % by electronic circuitry to 0.05 % over a magnetic range of ±100 mT. Major nonlinearity contributors are gain and phase mismatch. The total RMS noise over the frequency band 1 Hz to 1 kHz was measured at 70 µT and translates to a 0.05° error. The 1/f corner frequency is at 250 Hz with a measured 1/f noise over one decade of about 30 µT. With a die size of 2.4 mm^2 this device most certainly has economic viability.

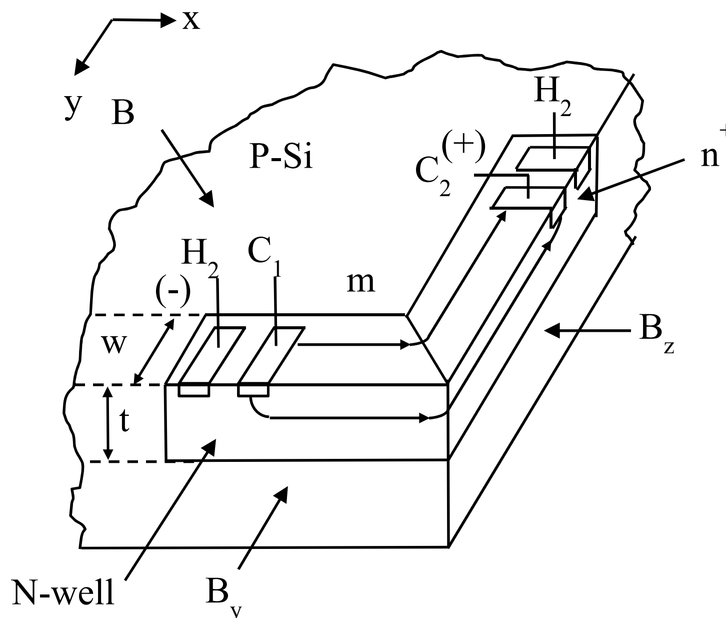

Figure 2.20 The one contact VHD with sense contact outside the active area. Taken from [87] with permission.

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The idea of the one contact VHD combined with its sense contact outside the active area to form a novel 2D structure is proposed [87]. Nonlinearity is slightly worse at < 0.3 % but over a larger magnetic range of 0 T to 300 mT in comparison to the previous example. The temperature performance measurement yielded a coefficient ≈ 0.1 %/℃ for 0 to 80℃. A sensitivity of S_{VI} = 19 $VA^{-1}T^{-1}$ was achieved with no observable cross sensitivity of the magnetic field up to 250 mT. Finally a bandwidth of 40 kHz could be obtained with 1/f noise measurement < 25 µT up to a frequency of 1 kHz. Figure 2.20 illustrates the layout of the novel single ended VHD and how the vector B_x and B_y interact with it to produce a two axis measurement capability. The biggest advantage of this structure is its compatibility with standard CMOS processes due to the non-interaction of the current with the sense contacts.

By creating an array of Hall devices it becomes possible to measure spatial magnetic fields. An example is the 32 x 32 CMOS Hall array implemented using a 31 µm pitch in 0.6 µm CMOS technology [88]. The minimum resolution achieved was 3.6 µm for lateral alignment and 16 µm for out of plane alignment. The system however has a major disadvantage in that it becomes large and complex and that each sensor's offset as well as any correction parameter if required must be individually stored. It is of the author's opinion that other methods can achieve similar results with less complexity. Another excellent 2D implementation example is the multi-contact VHD array implemented in n-well with contacts placed to form a circle and illustrated in Figure 2.21 [54]. Switches are used to sequentially activate an individual 5C VHD. Each device makes up a small portion of the well at a time and this reduces the offset and 1/f noise significantly from 40 mT to about 1.2 mT. Furthermore, by using their suggested "*subspinning*" method whereby each individual 5C VHD is also electrically rotated an offset of less than 40 µT may be achievable but at the cost of response time. The resolution of 14 µT corresponds to an error of 0.008° at a spinning rate of 100 Hz with the possibility for further reduction at the cost of increased signal processing and the sensitivity S_{VI} = 3 $VA^{-1}T^{-1}$. The geometrical factor achieved was quite low at 0.45 but is typical for VHD type elements. This sensor at 50 µm

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diameter can easily be expanded into a three dimensional sensor by using individual N^+ contacts as current and sense contacts in a Hall plate configuration. The sensor was implemented in 0.35 µm HV CMOS technology.

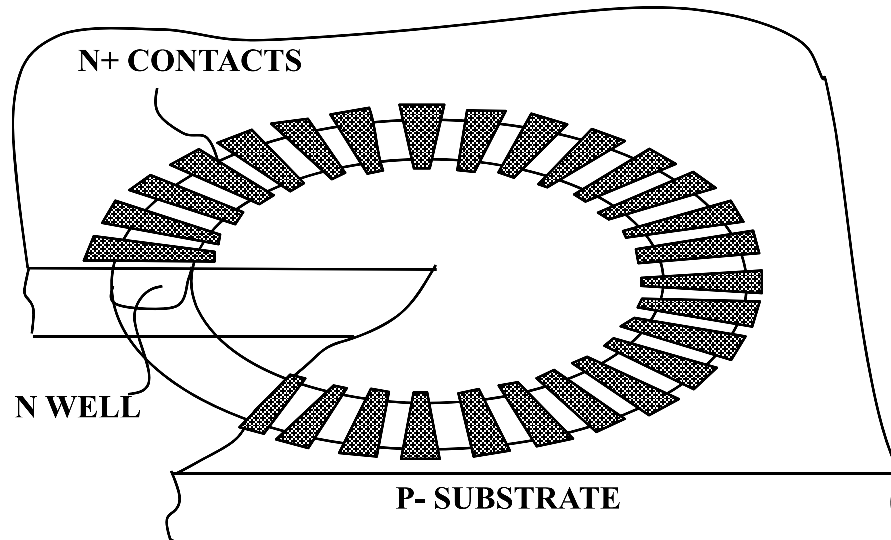

Figure 2.21 Multi contact VHD array for 2D sensing. Taken from [54] with permission.

2.6.3.3 3D

Generally what is implied by a three dimensional magnetic field sensor is one which is used either for positioning such as a compass [16], or to characterize a magnetic field for example in a reference plane [89]. The use of the third dimension in a typical angular position sensor makes for interesting application as reported by [90]. The sensor uses the third dimension to aid the positioning of the tilt of a permanent magnet above the sensor to a precision of ±1.2°. VHDs are used for x and y direction and achieves a precision of ±0.3° with four Hall plate devices used for the z-axis. The magnetic field strength is in the order of 40 mT. Early high accuracy 3D devices were however built using multiple chips placed orthogonally [89]. The already well known spinning current method was applied to an eight contact plate using low frequency switching of 8 Hz to reduce thermal settling effects

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that tend to modulate the Hall effect in the device. Fully integrated 3D devices have also been researched like the single active space 3D solution [3] that uses two supply contacts whilst sensing via four. A respectable sensitivity of S_{VI} = 827 $VA^{-1}T^{-1}$ is achieved for the VHD and S_{VI} = 909 $VA^{-1}T^{-1}$ for a Hall plate device measuring 50 µm x 50 µm. Nonlinearity is 3 % within a 1 T magnetic field range and increases to 9 % within a 2 T range. Cross sensitivity is also around 3 % up to 1 T increasing to 6 % for 2 T. Noise increases with a reduction in active size with the 50 µm x 50 µm device around two orders more noisy than the 500 µm x 500 µm device between 1 and 100 Hz.

2.6.4 Positioning

Earth magnetic field sensors must sense in the range of between 10 µT and 300 µT [15]. Early sensors based on eight contacts spinning Hall devices and configured using a multiple orthogonal chip solution, were also used for 3D earth magnetic field measurements from space and thus had to be hardened against radiation [16]. The eight contact device seemed a popular choice for such sensitive position sensors due to its low offset capabilities [91]. Such a device was implemented [91] in a 0.5 µm CMOS analog process. Testing the sensor was done using a ceramic enclosure to reduce package strain effects. Using these techniques, offsets of 2 µT could be achieved relating to an uncalibrated angle error of 4º. Calibration consists of rotating the sensor in the horizontal plane by 360º whilst measuring the output. For this application the maximum measurement frequency is important for example for a car, several hundred Hz scan rate would be required but for walking, a few Hz would suffice. Later, still using the 0.5 µm CMOS technology, an improved version was developed [92] that achieved 3.65 µT 3σ offset which was an order of magnitude better than commercially available sensors at the time. With an offset drift of less than 250 nT, the angle error translated to 0.5º. The noise of the sensor was dominated by the switching and measuring electronics at 0.3 uT/√Hz. Temperature drift was determined to be 8 nTK^{-1}. The full magnetic range of sensor is ±10.8 mT. Chip area was 2.9 mm^2 drawing 4.2 mA at 5 V.

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2.6.5 Energy measurement

Another popular application of the Hall device is in energy management systems. Hall devices are advantageous as they provide isolation by being contactless, transform very little energy into heat such as shunt resistors and can coincide with signal processing electronics and standard communication interfaces making for very intelligent sensor capability [93]. As the Hall voltage output is a direct product of the bias voltage and magnetic field, it is possible to use the Hall device as an analog multiplier to directly measure electric power [66]. A voltage divided copy of the mains supply is used to bias the Hall device. The sensor is then used to measure the magnetic field produced by the mains current passing through a conductor producing an output proportional to the electric power [94]. Such a solution was tested [94] in 0.5 µm CMOS technology and although linearity of the system was claimed to be 16 bits, only 14 bits was verified. The device is aimed at low power applications and the two systems presented draw only 100 µA and 380 µA respectively. No mention is made of the supply voltage but for 0.5 µm technology this would typically be between 3 V and 5 V yielding a power consumption of between 300 µW and 2 mW. This is an important figure compared to traditional technologies such as shunt resistors which would carry a few amperes at a resistance of approximately 1 mΩ and thus consume a few mW excluding any post processing electronics.

One of the challenges of these sensors is achieving a large dynamic range which has been solved [93] by implementing a dual range electrical current sensor using a VHD which typically has lower sensitivities for high fields and a standard Hall plate with a flux concentrator for measuring low fields. The sensor is very useful for measuring the energy of batteries in a hybrid vehicle which requires a wide dynamic range. The starter current for example can draw 1 kA whilst during idling no more than 30 mA is consumed. The flux concentrator saturates at around 40 mT and corresponds to a current of approximately 200 A flowing through a copper bus bar after which the VHD is then used to measure the upper range.

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For three phase power measurement, cores are used to sense the current through copper bars. Mounting Hall devices directly on copper bars make them susceptible to interference from the magnetic fields of other phases. A coreless Hall device for three phase power measurement was proposed [95] to overcome this. By symmetrically placing multiple Hall devices directly on the copper bars on each phase and using averaging formulas can practically eradicate cross sensitivities. Other technologies used include SOI [96] and magnetoresistive devices [97] but from literature it was found that these offer little if any advantage to a Hall device in standard CMOS.

2.6.6 Bimolecular microbeads

Microbeads are used in biological applications whereby thousands of nano-sized beads are chemically coated. The type of chemical causes the beads to attach to specific biological targets thus acting as a marker of biomolecules [98]. These targets can then in turn be isolated by identifying the microbeads in question. Traditional detection methods include complex and expensive technology such as superconducting quantum interference device sensors, giant magnetoresistance (GMR) arrays or by atomic force microscopy [39]. A µ-Hall device with an active area of 2.4 µm x 2.4 µm was demonstrated [39]. It is capable of detecting a single 2.8 µm microbead (Dynabeads M-280) at a distance of 7 µm above the sensor and is manufactured in 0.8 µm CMOS technology. The µ-Hall device has a fairly high resistance of 8.5 kΩ and a sensitivity of 175 $VA^{-1}T^{-1}$. Thermal noise dominates above 100 Hz but 0.2 µT/√Hz is achievable. An external AC magnetic field is applied to magnetize the microbead which creates a dipole around the bead thereby reducing the magnetic field over the Hall device and is shown in Figure 2.22. A lock in amplifier is then used to detect the signal from the Hall device to reduce noise. The signal is in the order of 5 µT down to 2 µT depending on whether the first or second harmonic is used for detection purposes. Although the detection level for the second harmonic method is lower, it suppresses the offsets and thus increases the allowable tolerances.

Using a Hall device for this application seems to be an exception as most literature reports the use of mainly spin valves [98, 99, 6, 100] , planar Hall devices [101, 102] and

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quantum-well μ-Hall device [103, 5]. Spin valves are of similar area roughly 12 μm^2, capable of detecting single beads of 2.8 μm down to 250 nm [99]. Biasing is done with a few mA achieving a signal in the hundreds of μV range but as low as 1 μV is also reported [6]. Typical excitation fields range between 1 mT and 2 mT. Sensors based on GMR and spin valves have high sensitivity but suffer from nonlinear responses and saturation at very low fields [103]. A typical spin valve sensor is shown in Figure 2.23.

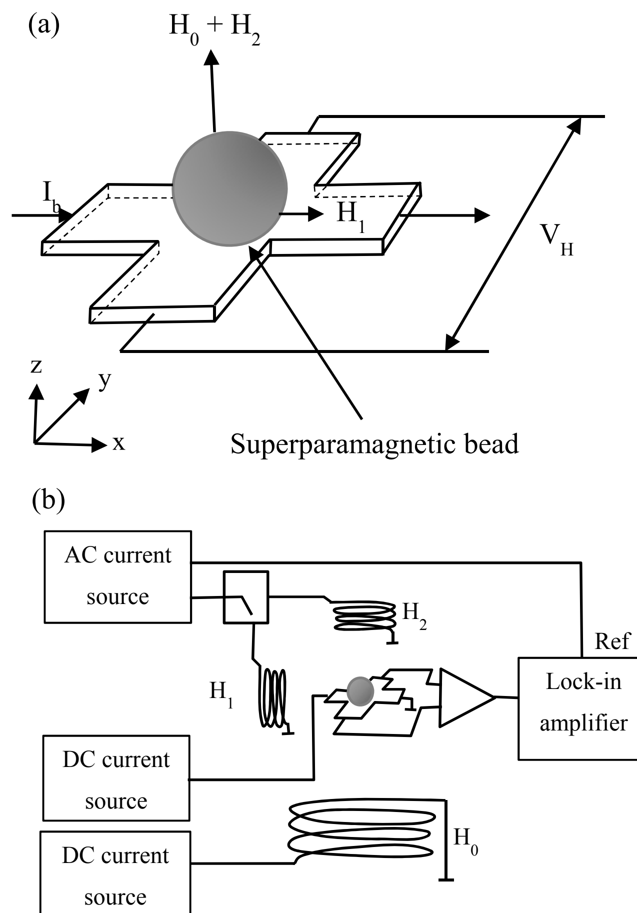

Figure 2.22 A method for detecting microbeads used in bimolecular applications. Taken from [39] with permission.

Permalloy planar Hall sensors show sensitivity in nT range [104] , have approximately four times higher SNR versus GMR and spin valve sensors and are capable in theory of

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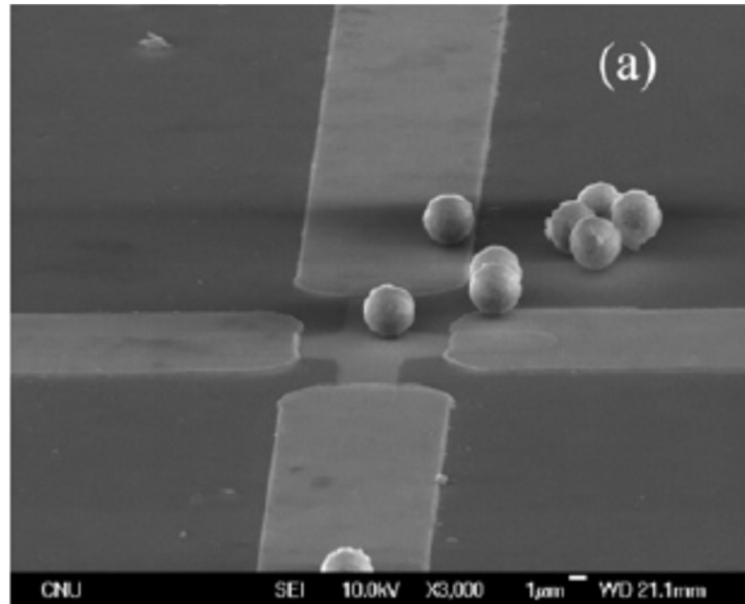
detecting single 40 nm beads with the aid of lock in amplifiers with active areas of 5 µm^2 [101, 104]. It has also been shown that the magnetic field generated from the sensing current alone yielded significant response from a single 2 µm bead without external magnetizing field [104].



with

Lastly the quantum-well µ-Hall device is theoretically capable of detecting a single 10 nm bead on a 0.3 µm x 0.3 µm device generating only 5 nV from a 10 µA bias with an excitation field in the region of 8 mT [103]. A signal of 200 nV per 2.6 µm bead was achieved [5] by implementing an array of six 1 µm x 1 µm quantum-well µ-Hall cross devices.

2.6.7 Force

A giant magnetorestrictive material (GMM) rod is used as a force sensing element based on the inverse magnetorestrictive effect. The GMM has a magnetorestrictive coefficient 100 to 1000 times larger than other commonly used magnetorestrictive materials. The

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sensor changes its magnetic properties proportional to the force exerted on it. An integrated Hall sensor is used to measure the magnetic flux density with respect to the external force applied to the rod. The Hall sensor is surrounded by a stainless steel ring to help keep the flux at an average level around the sensor [82].

2.6.8 Material characterization

In the field of material characterization, Hall sensors have been used to investigate noise sources in semiconductors [8], as a method to compliment the van der Pauw method for characterizing the resistivity of a semiconducting material [83] as well as researching nanomagnetic logic devices [4]. Parameters such as the Hall mobility itself are also a property of interest when studying various materials [105]. μ-Hall devices of $< 1\ \mu m^2$ are used to research nanostructure materials with strong magnetic properties [8]. When characterizing the resistivity and Hall coefficients of a semiconducting material it has been shown how a VHD with three contacts reduces the need for numerical coefficient calculations and relaxes the constraints on geometrical requirements. The result is accurate to within 5-6 % and comparable to alternative methods [83]. The use of extraordinary Hall devices to characterize Co/Pt multilayer film and single domain dot, nanomagnetic logic devices based on current deflection operation, i.e. split-current, also revealed details about the magnetic reversal process itself [4]. The intended application is for the implementation of non-volatile memory similar to [106].

2.6.9 Temperature

NiFe is strongly dependent on temperature with respect to its magnetic properties making a very useful temperature sensor in this regard. By magnetically exciting the material, the change in magnetic polarization and relative permeability is used to reveal information about the temperature and sensed via a typical Hall sensor [84].

2.6.10 Track Ball

It is possible to create a contactless track ball system by using a ball made from magnetic grade stainless steel alongside electromagnets used to magnetize the surface of the ball

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with a signature and then measured by a Hall sensor. The output of the sensor is then used to determine the speed and direction of movement. This method is advantageous over traditional opto-mechanical track balls as there is no contact, has less interference resulting from dirt accumulation and lower complexity in post signal processing [81].

2.6.11 Automotive

Automotive applications have by far been the driving factor behind the use of Hall sensor technology in the last decade [30]. Applications such as rotating target wheels e.g. crankshaft, camshaft, gearbox and wheel speed detection [107, 108, 109] with a sensing range requirement of between 1 mT and 200 mT capable of handling very extreme temperatures of -50 ºC to 210 ºC as required by the stringent conditions in automotive have become common place [110]. Linear positioning sensors are also widely used and have made features such as drive by wire possible [30]. Automotive applications have critical requirements for position sensors namely accuracy, reliability, safety, versatility and cost effectiveness. Extensive calibration is normally used to achieve these goals using digital signal processors (DSPs) with electrically erasable programmable read only memory (EEPROM) to store adjustment parameters sometimes compensating into the third order [110]. Special analog techniques have also become common place for example stress compensation done by using perpendicular diffusion resistors to bias a bandgap replica circuit that biases the n-well Hall device [110]. The p-diffusion and n-diffusion resistors have opposite stress coefficients. Placing them parallel and perpendicular to the flat of the (100) wafer makes the in-plane stress independent of the direction of the stress. This bandgap replica produces a voltage which is used to create the correct biasing conditions for the Hall device such that the stress related parameters are counteracted. Furthermore, redundancy is also required in safety critical applications which can be achieved with the use of multiple encapsulated devices working in parallel toward the same outcome [30]. Certain applications require very fast switch on time at extremely high temperatures over of 195 ˚C e.g. camshaft lift sensor [111, 112].

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2.7 HALL SENSOR PATENT REVIEW

Table 2.4 summarizes the results from multiple American patent searches. The first 50 hits for the following keyword searches have been intensely reviewed for any relevance to the intended study:

- "Capacitive pickup for Hall sensor",
- "Hall" & "current deflection",
- "Hall" & "current mode",
- "Hall plate" & "capacitive",
- "Hall sensor" & "capacitive" and
- "Capacitive magnetic field sensor".

The most relevant patent found was [113] but differs significantly in that the device used a split drain metal oxide semiconductor field effect transistor (MOSFET) in the current deflection mode whilst this study focuses on Hall plate devices in the Hall voltage mode of operation.

Figure 2.24 and Figure 2.25 show the results for "Hall sensor" patents and applications that were filed and published for the past twenty years. The last decade has seen an intensive patent rush mostly dominated by the automotive industry.

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Table 2.4 Hall sensor review

Reference	Patent no	Title	Relevance
[114]	4,190,799	"Noncontacting measurement of Hall effect in a wafer"	Use of a combined capacitive and inductive coupling technique for measuring the Hall angle in Si wafers.
[109]	4,982,155	"Hall-Sensor with High Pass Hall Voltage Filter"	High noise automotive application.
[115]	5,036,286	"Magnetic and Electric Force Sensing Method and Apparatus"	The use of capacitive sensing to monitor movement of a MEMS sensor.
[113]	5,083,174	"Floating Gate Magnetic Field Sensor"	Current deflection MAGFET sensed using floating gate capacitive coupling.
[106]	5,652,445	"Hybrid Hall Effect Device and Method of Operation"	The addition of a ferromagnetic layer combined with a Hall device for non-volatile memory.
[37]	5,818,227	"Rotatable Micromachined Device for Sensing Magnetic Fields"	The use of top level ferromagnetic deposition for magnetic field detection sensed using capacitive sensor.
[52]	6,008,643	"Offset Reduction and Separation of Hall and Piezoresistive Voltages through Current Injection"	The use of current injection to reduce offset caused by the piezo effects in semiconductors.
[76]	6,664,786	"Magnetic Field Sensor using Microelectromechanical System"	A MEMS device is used to physically measure Lorentz force deflection which achieves higher bandwidth in comparison to Hall devices.

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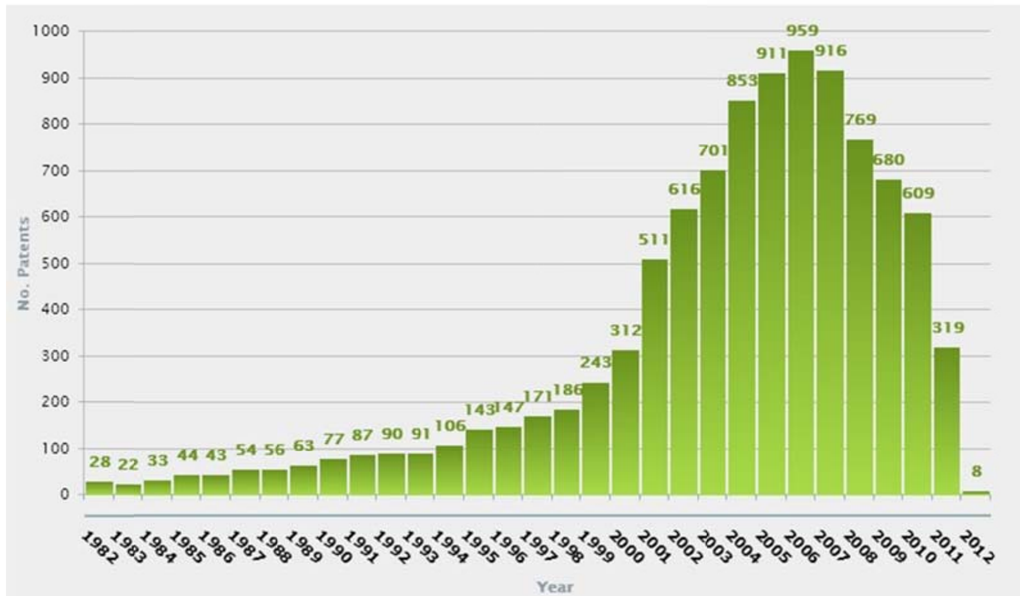

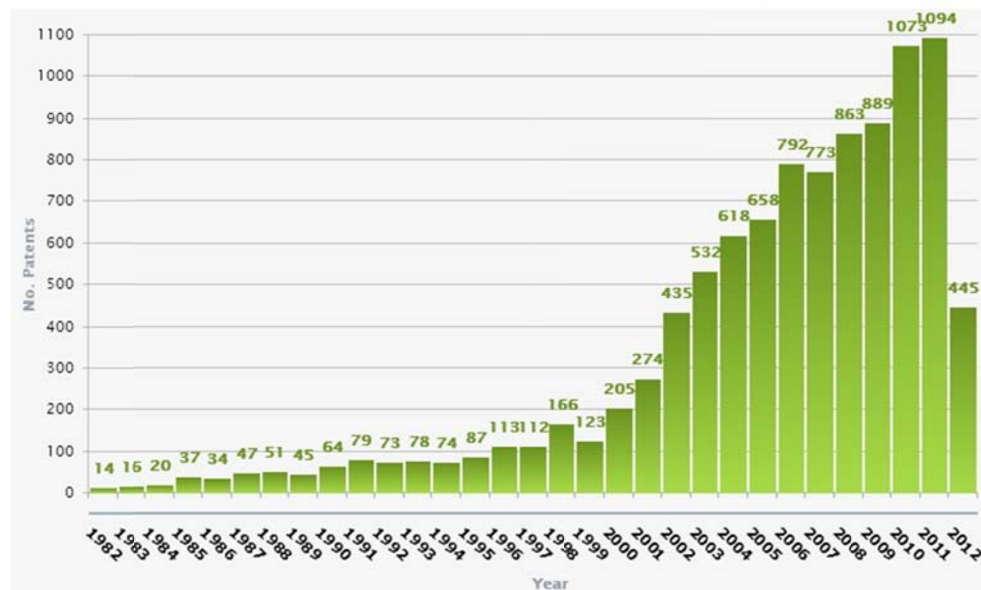

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2.8 CONCLUSION

Chapter 2 gave an in depth theoretical understanding of the Hall effect in Si. The Hall effect was described followed by a detailed analysis of the general characteristics of a Hall device. The theoretical limits were then presented to explore the boundaries of the Hall device in Si. Various modelling concepts for the design and simulation were then presented supported by various applications of the Hall effect device. The chapter was concluded with a patent review based on the concepts proposed in this thesis.

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CHAPTER 3 METHODOLOGY

3.1 RESEARCH APPROACH

Research can be defined [116] as:

"An inquiry into the nature of, the reasons for, and the consequences of any particular set of circumstances, whether these circumstances are experimentally controlled or recorded just as they occur. Further, research implies the researcher is interested in more than particular results; he is interested in the repeatability of the results and in their extension to more complicated and general situations."

Research has two main approaches namely quantitative and qualitative [116]. Quantitative research comprises of quantitative data generation which is then subject to analysis. It can be subdivided further into inferential, experimental and simulation approaches. The inferential approach is used when characteristics or relationships of a wider population is inferred from a collected data base describing a sample population. The experimental approach is used when a variable is to be observed by manipulating others under a controlled environment. Lastly, the simulation approach is used when the dynamic behavior of a system is to be observed using an artificial environment to generate relevant information and data. The former two approaches allow for new theory that can be used in simulation for the purposes of predicting future behavior. Qualitative research is mainly concerned with subjective assessment of attitudes, opinions and behavior and is then a product of the researcher's insights and impression. The research in this thesis is concerned with investigating an alternative sensing method to sense the Hall effect on a Hall device with the aim of deducing whether or not it is possible to reduce the geometrical factor. The nature of the research is thus scientific and a quantitative approach based on experiment and simulation as empirical studies is considered the most powerful support possible for a given hypothesis [116]. As far as possible, all facts will be sought at their source.

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Five sequential progressive stages of deductive (quantitative) research [117] are listed:

- Deducing a hypothesis,
- expressing the hypothesis in operational terms which propose a relationship between two specific concepts or variables,
- testing the operational hypothesis based on a research strategy,
- examining the specific outcome of the inquiry, thus either confirming the theory or indicating a need for modification of it, and
- modifying the theory if required in the light of the findings.

3.2 RESEARCH METHODOLOGY

It is important at this stage to clarify the difference between research methods and the research methodology. The research methods comprise of the techniques used to conduct or perform research operations whereas the methodology refers to the systematic approach used to solve the research problem. The methods used in this research will mainly comprise of:

- The collection of data through contemporary theory which will be used to
- design appropriate experiments to assist in establishing relationships capable of solving the research problem, and
- the use of well-established theory to evaluate the accuracy of the obtained results.

The research methodology will be scientific based mainly on experimentation, observation and logical arguments [116]. The scientific method outlined is based on certain basic postulates [116] that:

- Relies on empirical evidence,
- utilizes relevant concepts,

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- is committed to only objective considerations,
- presupposes ethical neutrality,
- results into probabilistic predictions,
- methodology is made known to all concerned for critical scrutiny and for use in testing the conclusions through replication, and
- formulates the most general axioms what can be termed as scientific theories.

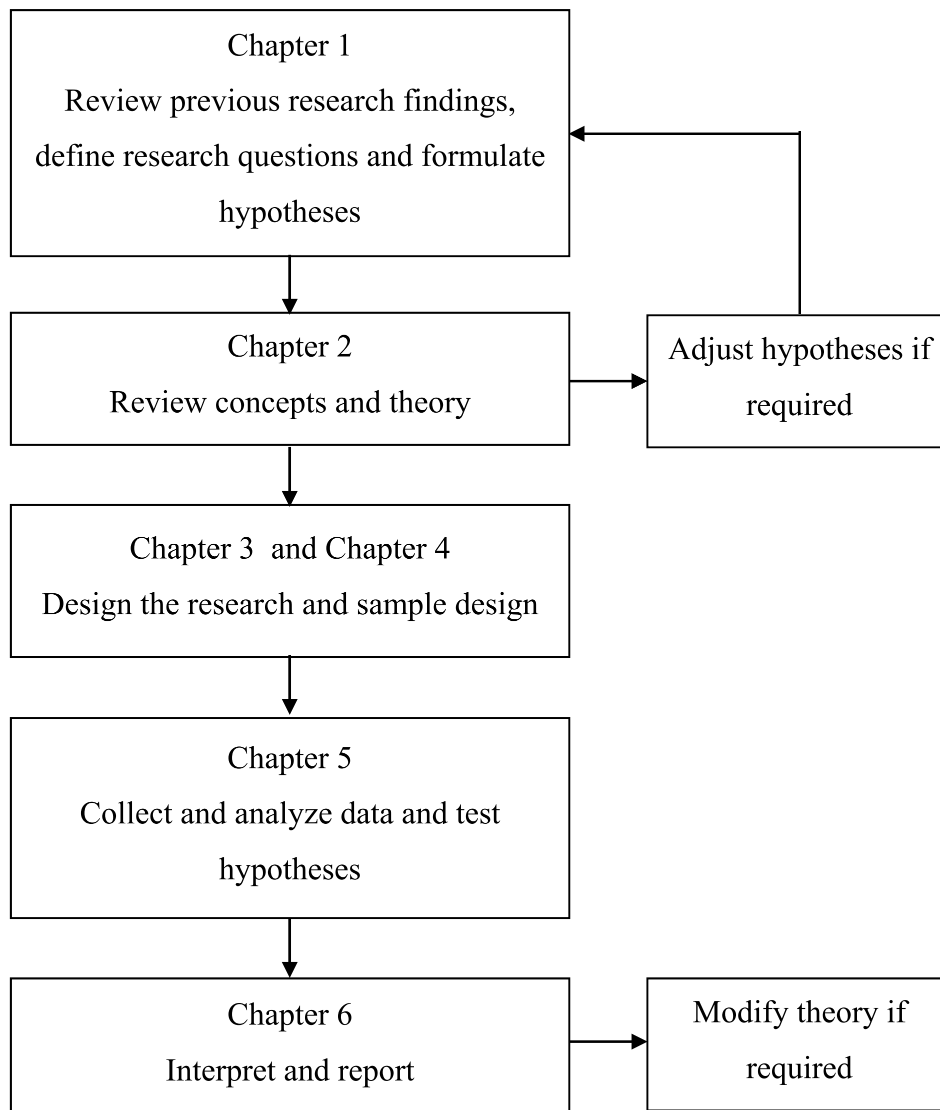

Figure 3.1 The proposed research methodology.

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In summary, scientific research is fundamentally systematic, logical, empirical and replicable [116]. Figure 3.1 illustrates the proposed research methodology or strategy that will be used in the thesis.

3.3 RESEARCH METHODS

3.3.1 The IC process

The process chosen for this research is 0.35 µm CMOS. The process features include:

- Standard 3.3 V field effect transistors with a minimum gate length of 0.35 µm,
- two poly-silicon layers making inter poly-silicon capacitors and high resistance resistors possible,
- four metal layers,
- single n-well, and
- minimum poly-silicon line width of 0.35 µm and minimum metal width of 0.5 µm.

IC fabrication was sponsored by Azoteq Pty(Ltd) as part of the company's semiconductor research.

3.3.2 Design, modelling, simulation and layout

The schematic design has been done using Cadence Virtuoso Schematic Editor, modeling and simulation was done using Spectre in the Cadence Analog Design Environment. The process will be used to understand and refine the design of a standard Hall plate with the aim of maximizing the processes capability to extract the maximum Hall effect performance from the device. As the interest is to understand the influence of the newly proposed sensing method on the geometrical factor, various geometries will be experimented with using both the traditional and proposed approach.

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After the design is completed, the various Hall plate designs can be transferred to the layout using Virtuoso Layout Editor. In some cases it may be necessary to break the design rules thus a thorough understanding of the process outline will be required. The Hall plate is not a standard device available as part of the technology and thus the standard design rules checker (DRC) and layout versus schematic (LVS) checker will be of little use as a tool for reviewing the integrity of the designed layout. An in depth manual peer review will thus be relied upon to ensure the integrity of the intended design.

3.3.3 Measurement setup and equipment

The Hall voltage of a standard Hall plate can easily be calculated, measured and verified using a high quality digital voltmeter. Measuring the emitter current through the vertical BJT will be done using a high quality digital ammeter. A rare earth magnet will be used to generate the require magnetic field <200 mT. Mounting the magnet on a vertically adjustable device capable of accurate sub-millimeter movement will be critical for repeatability. A calibrated linear Hall sensor with high sensitivity will be used as a reference against which the experimental design will be compared.

3.4 CONCLUSION

Chapter 3 has outlined the research approach, methodology and methods to be used in this thesis. The research approach was determined to be of a scientific nature and a quantitative approach based on experiment and simulation was proposed as the most powerful support possible for a given hypothesis given its empirical nature. The research methodology was then outlined and based on a systematic, logical, empirical and replicable approach and illustrated graphically. Finally the research methods comprising of the target technology, design approach and measurement setup and equipment were described.

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CHAPTER 4 HALL PLATE DESIGN AND ANALYSIS

4.1 INTRODUCTION

Prior to building a physical device, the proposed Hall Effect Plate will be theoretically analysed based on a commercially available standard 0.35 µm CMOS process. The design will be approached in two different ways such that a quantitative comparison can be made. From the data gathered in the process, conclusions can be made against which the proposed hypothesis can be tested. Firstly, a brief overview of the technology will be given according to which a classical Hall plate reference will be designed and implemented. This will be followed by a discussion on the parasitic vertical BJT which will be used as the sensing element in the newly proposed design and finally the Hall plate design itself.

4.2 TECHNOLOGY

Table 4.1 Summary of various technological parameters of the 0.35 µm CMOS process to be used

Parameter	Process Typical	Unit
P<100>	20	Ω-cm
N-well junction depth	2.0	µm
N+ junction depth	0.12	µm
P+ junction depth	0.15	µm
NMOS V_t	0.58	V
PMOS V_t	-0.67	V
N-well resistance	875	Ω/□
N-well doping concentration	$3.5x10^{16}$	cm^{-3}
P+ diffusion doping concentration	$5.5x10^{19}$	cm^{-3}
N-well electron mobility μ_n	0.102	m^2/Vs

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4.2.1 Overview

The process to be used for both the reference Hall plate as well as the proposed Hall plates is a commercially available standard 0.35 μm CMOS process. It is implemented on a p-type substrate of <100> orientation with a typical resistivity of 20 Ω-cm. The base process is a recess local oxidation of silicon (LOCOS) process which supports a single poly-silicon layer and two metal layers consisting of 12 masks. The Hall device however only requires a subset of 7 of these mask namely n-well, p-well, active, n+, p+, contact and metal 1. Figure 4.1 shows the cross section of the CMOS process that will be used to implement the Hall device. The specifications of interest to design the Hall plate are tabulated in Table 4.1.

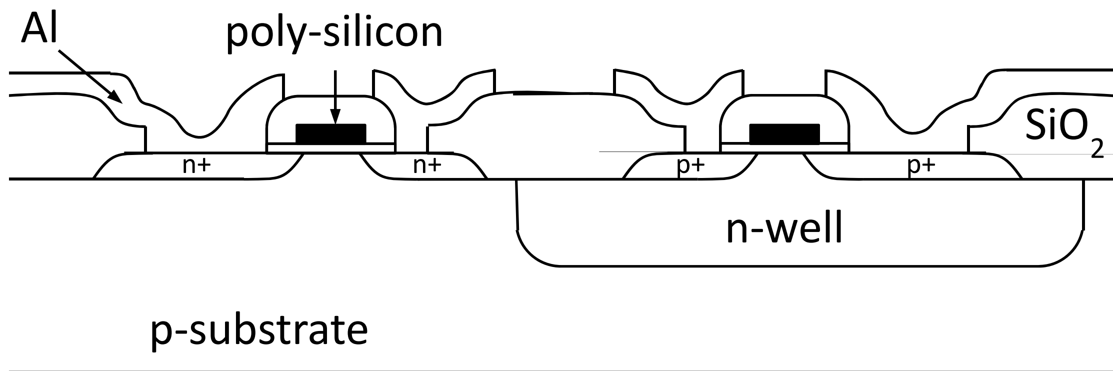

Figure 4.1 Cross section of the commercially available standard CMOS process used as basis for this research

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4.3 HALL PLATE DESIGN

4.3.1 Basic Hall effect characteristics

Table 4.2 Summary of calculated parameters for a Hall plate of 100 µm x 100 µm @ 1.7 V

Parameter	Calculated	Unit	Formula
B_{max}	185	mT	
V_{hmax} @ B_{max}	23.24	mV	(2.60)
I_H @ B_{max}	26.56	µA	(2.61)
I_{EH} @ B_{max}	106.26	µA	(4.8)
S_{VA} Hall voltage mode	0.1256	VT^{-1}	(2.34)
S_{IA} Hall current mode	1.436×10^{-4}	AT^{-1}	(2.34)
G_H	0.725	-	(2.62)
θ_{Hmax}	1.078	deg	(2.14)
Plate width w	100	µm	
Plate length l	100	µm	
Plate thickness t	2	µm	Table 4.1

A standard Hall plate with an area of 100 µm × 100 µm was planned as a test structure based on the technological parameters of the 0.35 µm CMOS technology. Substituting these technological parameters into their relevant equations (see Table 4.2), it was possible to determine the expected theoretical performance of the plate. These parameters will be used as a reference against which the device performance can be compared. A summary of the expected performance of the plate at the proposed bias voltage of V_{bias} = 1.7 V can be seen in Table 4.2. The device voltage was chosen to ensure appropriate biasing of the vertical sensing BJTs in their active forward region.

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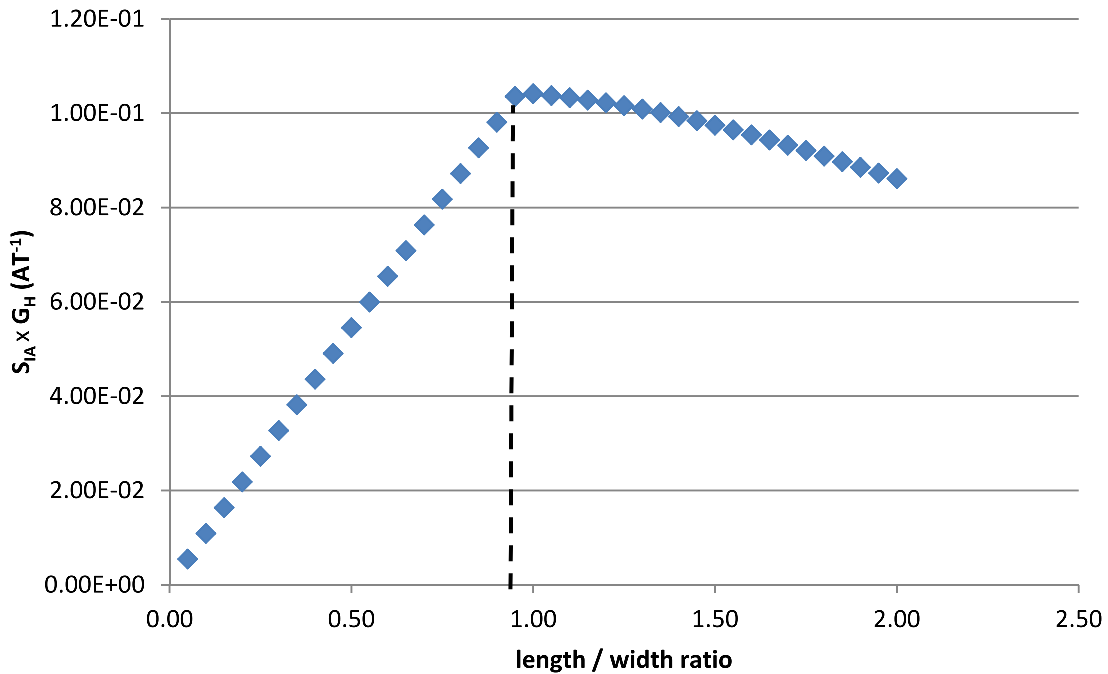

Figure 4.2 Graph illustrating the absolute sensitivity, geometrical factor product for the Hall current mode to maximizing performance.

A width-to-length ratio of unity was chosen as a practical device to use as it approximately coincides with the best trade-off between voltage (or current) sensitivity and the geometrical correction factor degradation as can be seen in Figure 4.2. According to [11], the maximum achievable voltage related sensitivity for a plate occurs for the shortest plate length. The mode of operation however changes from Hall voltage mode to Hall current mode once the plate becomes too short and thus for a very small Hall angle, the geometrical factor maximizes at 0.742. The maximum achievable voltage/current related sensitivity is thus $S_{VVmax} = S_{IImax} = 0.0756\ T^{-1}$. The square Hall device is also a good choice as a test structure given it is very well documented in literature and simple to fabricate and study.

Figure 4.3 shows how the geometrical factor relates to the length-to-width ratio for this Hall plate design according to the formulae given in (2.62), (2.63) and (2.64).

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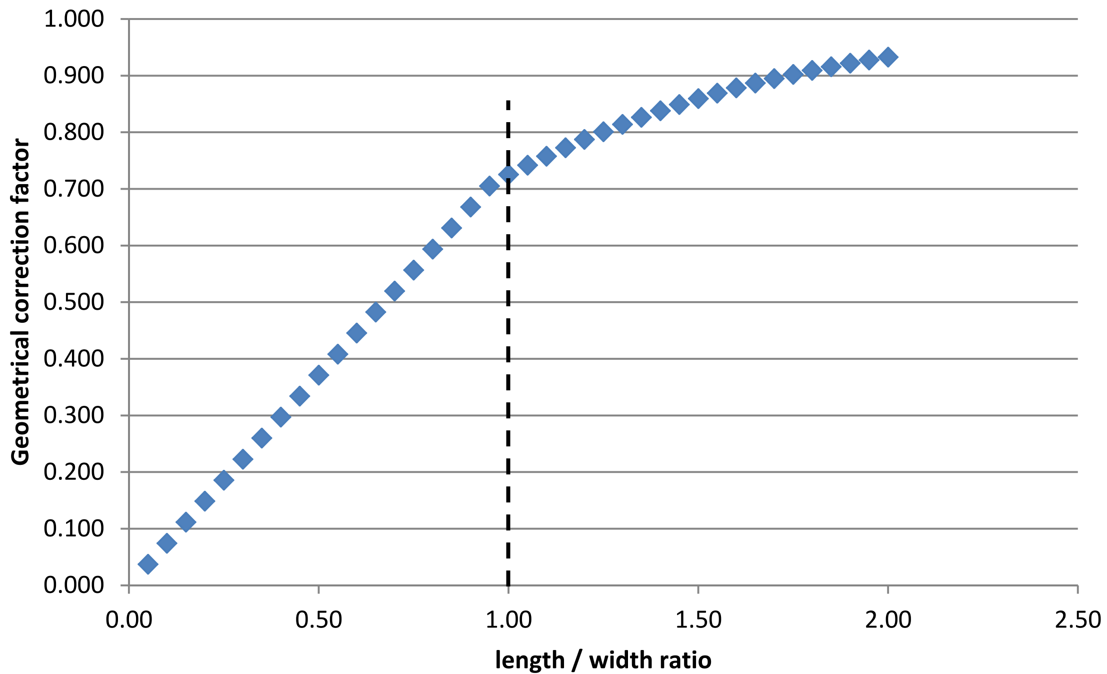

Figure 4.3 Geometrical correction factor as a fraction of length -to-width ratio according to (2.62), (2.63) and (2.64).

The theoretically calculated current related sensitivity at constant voltage bias according to (2.34) is 1.436 x 10^{-4} AT^{-1} which coincides with a value very close to the theoretical maximum as expected. It is also translates to a very typical voltage sensitivity for silicon and can be seen in Table 2.1. The chosen dimensions bode well with the intentional design of a plate with a low geometrical correction factor against which a proper comparison can be made. Figure 4.4 shows how the sensitivity varies with a change in length-to-width ratio for a Hall plate biased with a constant voltage.

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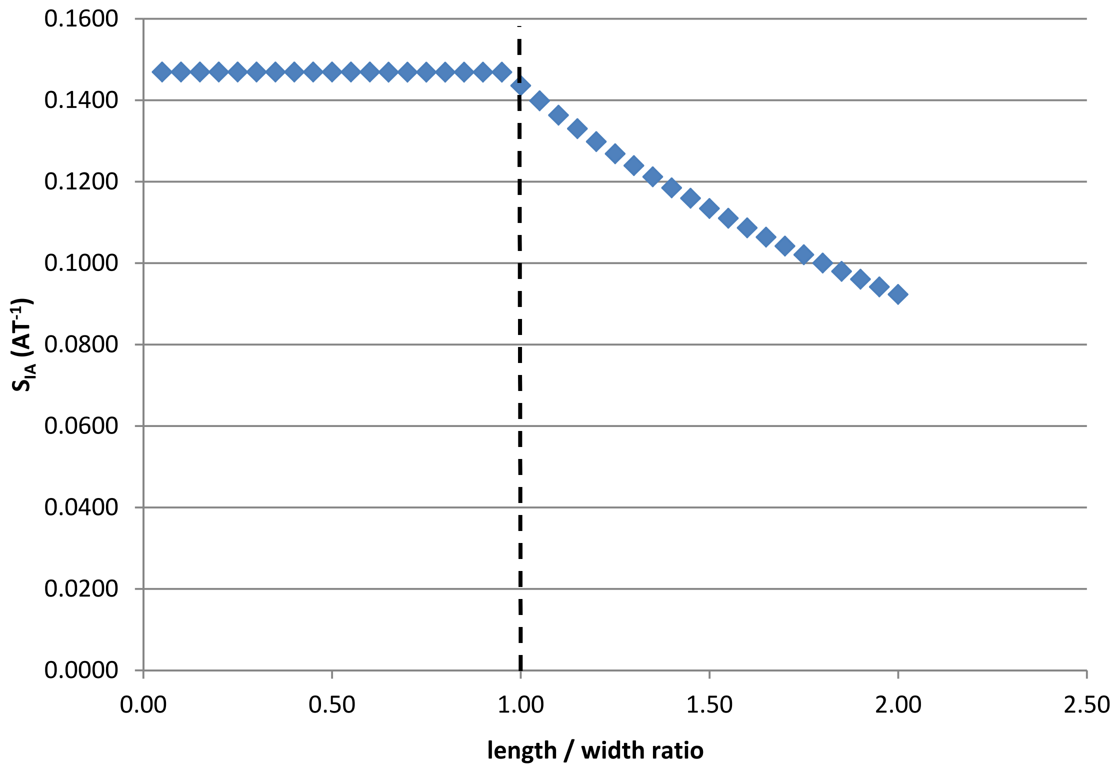

Figure 4.4 Current related sensitivity variation versus length-to-width ratio according to (2.39).

4.4 VERTICAL BJT

Figure 4.5 illustrates a cross and top section of the Hall plate at half-length through the sensing terminals. The vertical BJT forming between the P+ doped contacts through the N-well to the substrate can clearly be visualized. It is possible to bias the Hall device such that the BJT's become forward biased and in doing so, activates the inherent current gain of the transistor to amplify the Hall voltage/current into a useful signal via the emitters of the BJT's.

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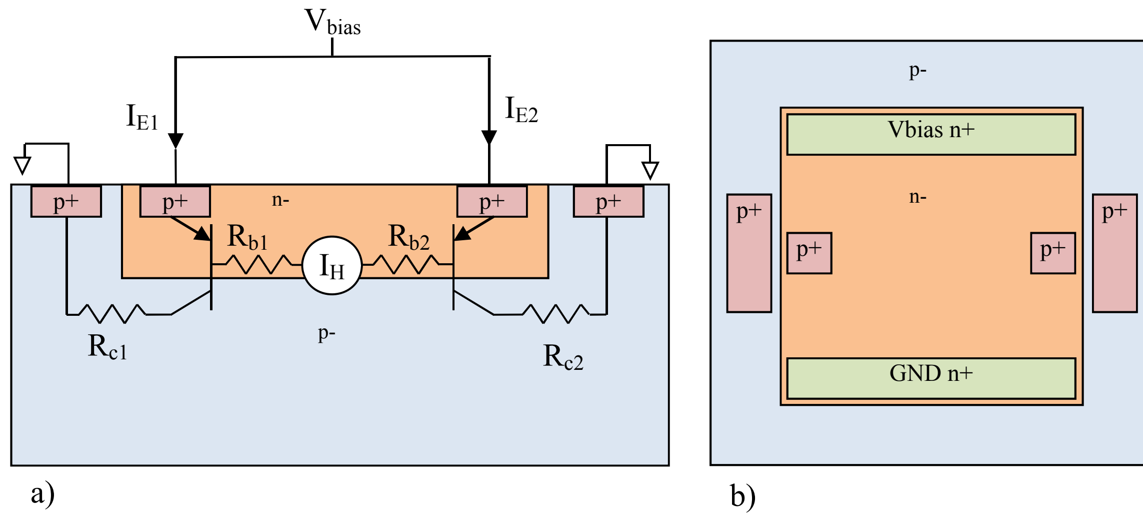

Figure 4.5 (a) Cross section and (b) top view of n-well Hall plate showing the presence of the parasitic vertical BJT between the p-type node p+ forming the emitter, the n-well n- forming the base and the substrate p- forming the collector. I_E denotes the emitter current, I_H the Hall current and R_{b1}, R_{b2}, R_{c1} and R_{c2} the relevant parasitic resistances.

The collector current for a BJT [118] is defined by

$$I_c = I_s e^{\frac{V_{BE}}{V_T}} \tag{4.1}$$

with I_c the collector current, I_s the reverse saturation current, V_{BE} the base emitter voltage and V_T the thermal voltage. Furthermore,

$$I_s = \frac{A_E q D_p n_i^2}{N_B W_B} \tag{4.2}$$

where A_E is the area of the emitter, q the charge of an electron, D_p a proportionality factor called the diffusion constant in m^2/s, n_i the intrinsic density in cm^{-3}, N_B the number of carriers in the base in cm^{-3} and W_B the base width in cm. The diffusion constant is

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calculated as

$$D_p = V_T \mu_p \tag{4.3}$$

with μ_p the hole mobility in m^2/Vs and typically a factor 3 times less than the electron mobility in the base μ_n. For a PNP BJT,

$$I_E = I_C + I_B \tag{4.4}$$

where I_E is the emitter current and I_B the base current calculated as

$$I_B = \frac{I_C}{\beta} \tag{4.5}$$

with β the forward current gain as defined in the technology electrical parameters.

Figure 4.6 shows a schematic representation of the Hall plate which can also be used as a first order simulation model. The Hall current I_H is modelled as a current source whilst the Hall plate offset is modelled by adjusting R_d which represents the mismatch that occurs in the plate resistance R_{s1} and R_{s2} and ultimately the zero magnetic field Hall current. Under ideal conditions, $R_{s1} = R_{s2} = R_S$. Typically in the technology used in this study, it was found that R_d was in the order of 0.2% of R_S which translates to approximately 2 Ω. V_{bias} is used to set up the bias current I_{bias} through the Hall plate causing a voltage drop of V_{EB} across both R_{s1} resistors. For relatively low bias currents and magnetic fields, the voltages V_{Rs1} and V_{Rs2} across R_{s1} and R_{s2} will be equal and the base resistance will have a very small impact on the emitter Hall current. If however V_{bias} increases to such extent that $V_{bias}/2$ exceeds the forward voltage of the base emitter junction V_{EB}, the voltage across R_{s2} will increase at a faster rate than the voltage across R_{s1} and will become a source of non-

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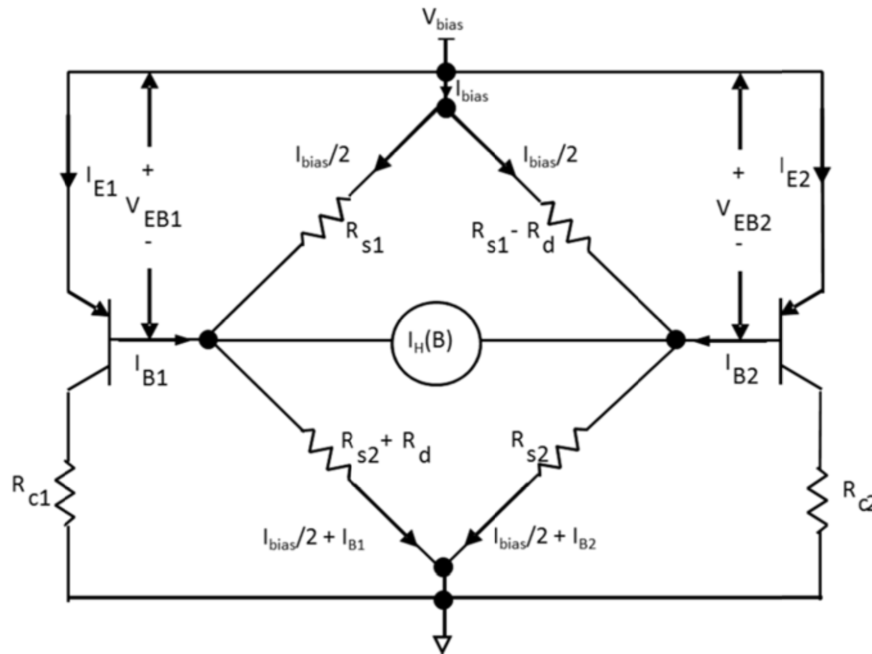
linearity. Ideally I_B should be kept very small, such that the current through R_{s1} and R_{s2} are approximately equal. R_{c1} and R_{c2} can be minimized through proper layout design of the BJT. Biasing the transistors requires that the base to emitter voltage $|V_{BE}|$ be greater than 0 V with a biasing voltage V_{bias} across the Hall plate as given in Equation (4.6) and thus:

$$V_{bias} \approx 2V_{BE} \approx 2V_{Rs1} \approx 2V_{Rs2}. \quad \textbf{(4.6)}$$



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Keeping V_{bias} as low as possible also reduces the consumed power and hence also the Joule heating in the Hall plate and is one of the major advantages of this technique. This does however come at the expense of sensitivity. Figure 4.7 shows both the pnp transistor's forward voltage $|V_{BE}|$ and gain β versus the collector current I_c characteristics as simulated from foundry data. It can be seen that a collector current as low as 1 nA is sufficient to bias

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the transistor enough to get stable current gain. As the main aim was to illustrate a proof of concept, biasing the emitter at the same V_{bias} greatly simplified the setup. For this experiment, the bias point is indicated in Figure 4.7 by the dotted black line at approximately 2 mA. From Figure 4.7 it can also be seen that the ideal biasing conditions for the Hall device would be for a collector current between 1 nA and 100 µA. This range yields a stable current gain factor beta over many decades of collector current and will also yield a decrease in inter-chip variation as well as lower temperature dependencies.

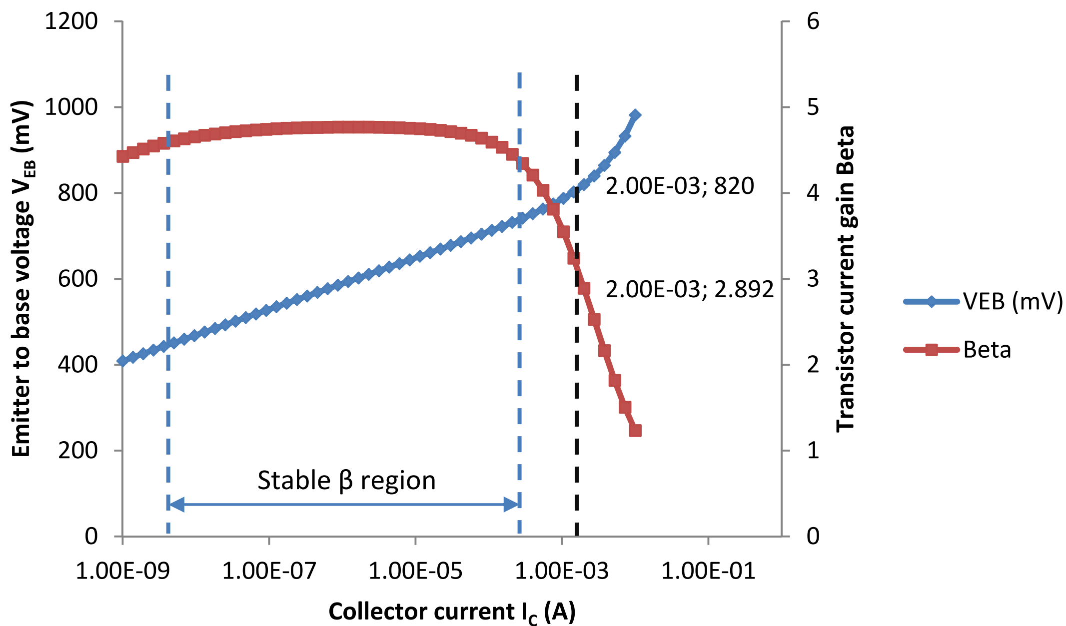

Figure 4.7 BJT forward current gain β and forward base emitter voltage V_{EB} as a function of the collector current I_C for a similar sized BJT as modelled by the foundry.

As we are most interested in how the emitter current translates into a measurable Hall effect parameter, it will be necessary to relate the emitter currents I_{E1} and I_{E2} to the effective Hall current ΔI_{EH} by measuring the difference between the emitter currents and is given by:

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$$\Delta I_{EH} = I_{E1} - I_{E2}. \quad (4.7)$$

Rewriting ΔI_{EH} as a function of the base currents I_{B1} and I_{B2}, from (4.4) and (4.5),

$$\Delta I_{EH} = (\beta + 1)(I_{B1} - I_{B2}) \quad (4.8)$$

with β the forward current gain as defined in the technological electrical parameters. The potential gain this method offers is quite significant especially in more sophisticated technologies such as BiCMOS processes where a much higher β should be achievable.

4.5 NOISE ANALYSIS

Two dominant noise sources are identified, namely i^2_{nR}, the noise contributed by the Hall resistive plate and i^2_{nT}, the input referred noise from the BJT.

The Hall plate noise i^2_{nR} is dominated by its thermal noise and 1/f flicker noise and can be approximated by

$$i_{nR}^2 = S_{nR} \cdot \Delta f = \left[\frac{4kT}{R_S} + \frac{\alpha}{n}\frac{1}{f}I^2\right]\Delta f \quad (4.9)$$

if recombination-generation noise is excluded. Current I is the bias current I_{bias} through the device, n the total number of charge carriers in the device, α is the Hooge parameter, a dimensionless value that may be associated with a specific device processing method and structure. Recently the Hooge parameter $\alpha \approx 10^{-5}$ has been determined for CMOS silicon Hall devices very similar to this research [119], and therefore this value was used in the calculations.

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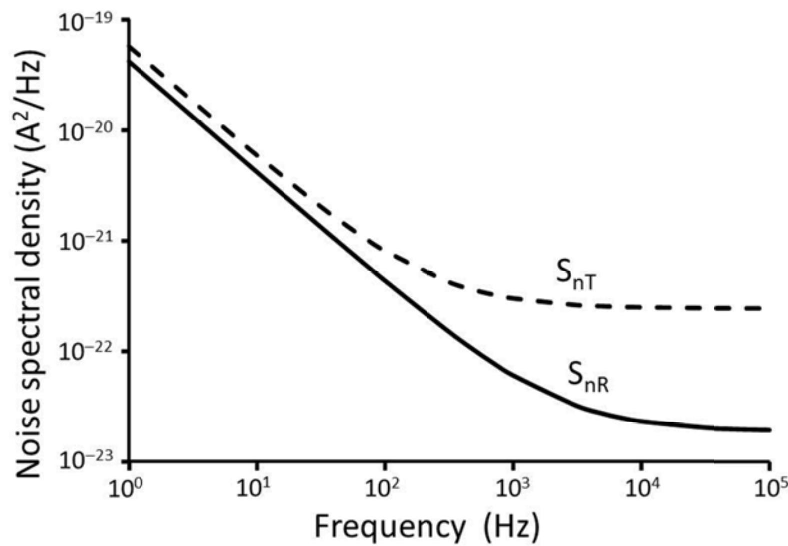
The input referred transistor noise i^2_{nT} has shot noise components as well as a flicker noise component, as shown in Equation (4.10). Since two transistors are connected to the Hall plate, the transistor noise contributions should be twice that of a single BJT.

$$i_{nT}^2 = S_{nT} \cdot \Delta f = 2\left[2qI_B + \frac{2qI_C}{\beta^2} + \frac{KI_B}{f}\right]\Delta f \qquad (4.10)$$

The flicker coefficient K will determine the corner frequency of the BJT noise spectral density where the flicker noise equals the “white” shot noise. Most of the BJT spectra measured in a detailed study had corner frequencies in the range of 10 Hz to 10 kHz [120]. In the calculations a corner frequency of 1 kHz was assumed, a typical value for BJT devices.

The Hall noise current is i^2_{nH} and will be given by:

$$i_{nH}^2 = S_{nH} \cdot \Delta f = i_{nR}^2 + i_{nT}^2 \qquad (4.11)$$



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The relevant noise spectral densities as calculated for the device are shown in Figure 4.8. From this figure it can be seen that at low frequencies the transistor 1/f noise is slightly larger than the Hall plate noise. The values calculated for a 100 Hz frequency noise are tabulated in Table 4.3.

Table 4.3 Summary of calculated noise contribution and minimum magnetic detection level at 100 Hz for a) a traditional plate without the integrated BJT's, b) the integrated BJT Hall device, and c) a traditional plate using a typical differential amplifier with similar gain as b)

Hall plate	Absolute sensitivity S_A	Total input noise density S_{nH}	Noise equivalent field
No BJT	140×10^{-6} **(A/T)**	4.32×10^{-22} **(A²/Hz)**	0.15×10^{-6} **(T/√Hz)**
with BJT	550×10^{-6} **(A/T)**	12.4×10^{-22} **(A²/Hz)**	0.25×10^{-6} **(T/√Hz)**
With diff amplifier	489.84×10^{-3} **(V/T)**	1×10^{-14} **(V²/Hz)**	0.80×10^{-6} **(T/√Hz)**

From Table 4.3 the spot noise figure NF = $(SNR_{out})/(SNR_{in})$ of the BJT amplifier circuit can be determined as the ratio of the two input referred noise densities, giving us the value of NF = 4.6 dB at 100 Hz frequency. The noise figure can be lowered by reducing the BJT base current, although too low a base current will limit the dynamic range.

Measurements of CMOS Hall sensors with a plate area of 20 μm x 20 μm = 400 μm^2, a layer thickness of 1 μm and a drive current of 0.2 mA resulted in a measured noise equivalent field of 5×10^{-7} T/√Hz at 100 Hz [8]. The estimation of the Hall plate noise equivalent field is 1.5×10^{-7} T/√Hz at 100 Hz, which is in the same range.

Smaller area Hall plate devices will generate significantly higher 1/f flicker noise than this quite large Hall plate. For μ-Hall devices electron drift velocity saturation may also become one of the main limiting factors and for silicon this occurs at an electric field of approximately 30 $kVcm^{-1}$ [11]. For a bias voltage of 5 V for example, this corresponds to a

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minimum length of 1.5 µm. Scaling down the lateral dimensions, especially in present day deep submicron technologies, leads to an increase in noise on the Hall signal [8] and tends to dominate in smaller dimensions [27]. This is mainly due to the limited number of carriers available as well as other effects such as Joule heating. This makes the integrated BJT very suitable to integrate with µ-Hall devices whereby much lower power consumption results in lower biasing currents and consequently I^2R heating effects.

Table 4.3 also illustrates how the noise equivalent field of a Hall plate integrated with a typical differential operational amplifier compares with the method proposed in this study. Assuming a typical noise of 100 nV/√Hz and similar gain as achieved by the new method, it can be seen that the proposed method potentially improves the noise equivalent field by almost a factor of 3 fold.

4.6 CONCLUSION

Chapter 4 has detailed the design of the Hall plate in the proposed 0.35 µm CMOS technology. The chapter begins with the given technological parameters of the process upon which the Hall plate design is based. A 100 µm x 100 µm Hall plate design was chosen given its low geometrical factor yet still practical sensitivity as well as being very well documented in literature. The design parameters were then used to explore the expected outcome based on two methods of indirect measuring of the Hall effect. The two methods conclude the chapter, clearly giving the upper and lower boundaries against which the final measurement results can be compared and tested against the hypothesis.

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CHAPTER 5 LAYOUT, FABRICATION AND MEASUREMENT RESULTS

5.1 INTRODUCTION

To enable a comparison to be made of the proposed indirect method it will be necessary to fabricate an example of the Hall plate. The fabricated device can then be used to make the required measurements. The proposed layout and fabricated device will be shown after which the test setup that was used for analysis will be discussed. Thereafter the measured data will be presented from which the conclusions can be drawn.

5.2 LAYOUT DESIGN

A layout was prepared according to the design proposed in Table 4.1 based on the technology described in 4.2. Figure 5.1 illustrates the resulting Hall plate layout measuring 100 µm x 100 µm. The Hall device has N+ ohmic contacts connected to $+V_{bias}$ and $-V_{bias}$ through which the plate will be electrically biased. The N+ contacts stretch across the entire width of the plate to ensure evenly distributed current flow through the device width. The P+ contacts are located at the half length point of the plate and are connected to I_{E1} and I_{E2} and measure 19.58 µm x 8.8 µm. Finally a substrate contact stretching around the entire plate is connected to the GND pad. Figure 5.1 shows a photograph of the fabricated device which was used for the measurements.

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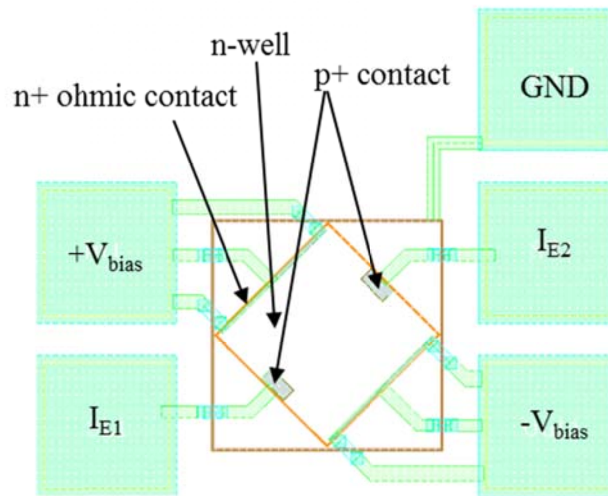

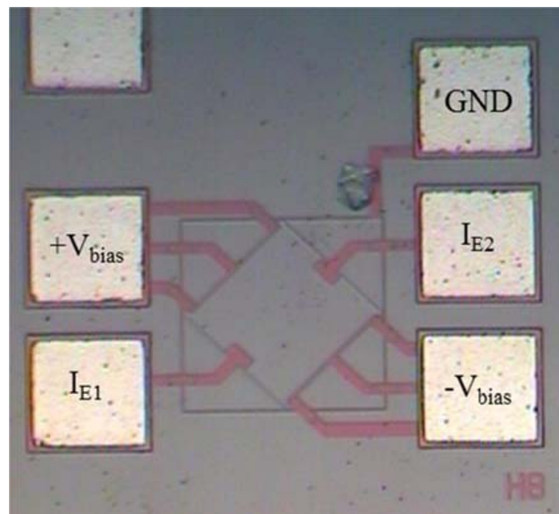

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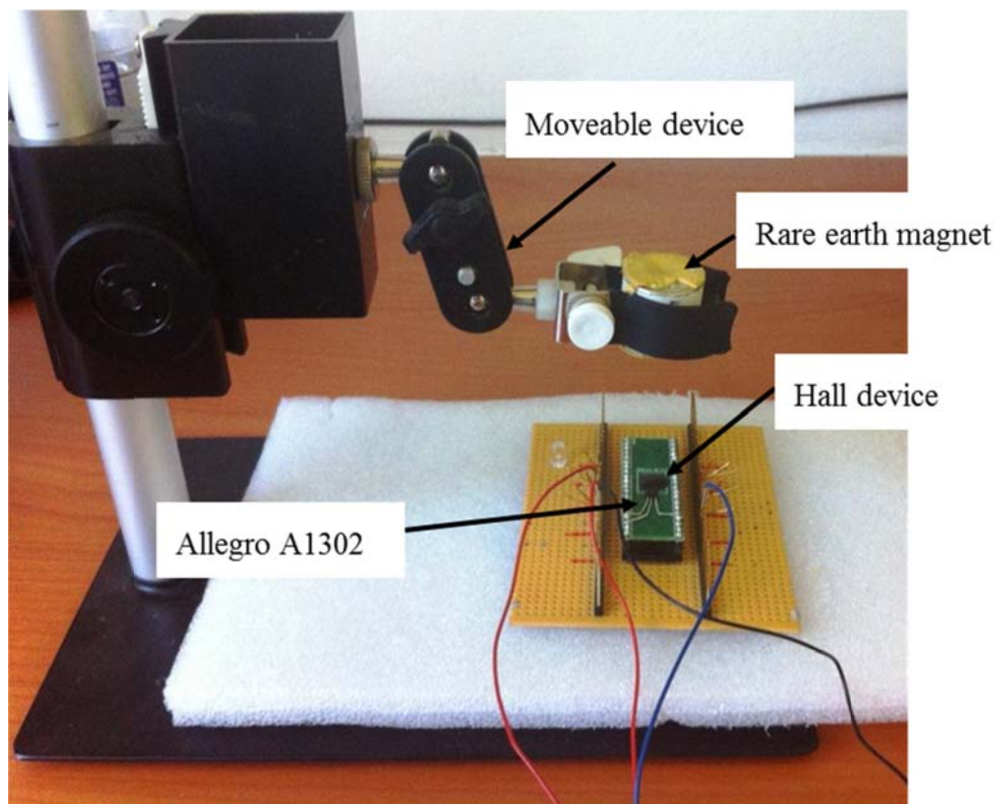
5.3 TEST SETUP

Figure 5.3 shows the test setup used for this experiment. An A1302 linear ratiometric Hall sensor manufactured by Allegro was used as a reference for the magnetic field in this experiment. The A1302 is a high precision linear Hall effect sensor which outputs a voltage that is directly proportional to the applied magnetic field. The A1302 was chosen as it has a very sensitive response of 1.3 mV/G [121]. At a supply of 5 V, it provides for a very large dynamic range with high enough resolution for the intended aims of this study.



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5.4 HALL CURRENT MEASUREMENT RESULTS

Ten samples were manufactured and prepared for measurements. It was first required to measure the emitter and collector currents so that the active forward gain β for each Hall plate's BJT could be calculated at the chosen bias condition. Using the design shown in Figure 4.6 with V_{bias} = 1.7 V, the beta for each BJT was calculated by measuring the emitter and collector current separately. The base current and hence the BJT's beta could be deduced. Table 5.1 below shows the calculated betas from the measured emitter and collector currents for ten samples used in this experiment which consist of the average of both BJT's per plate. It can be seen that the inter-chip variation is relatively good, matching within approximately ± 2.5%. This mismatch will however be larger between wafers and batches. The average current gain of the ten BJT's was calculated to be 2.98, which also compares well with the gain of 3 as specified in the technology.

Table 5.1 The measured vertical BJT emitter current I_E and collector current I_C used to calculate the forward gain β for a V_{CE} of 1.7 V

Device number	I_E	I_C	Calculated
	(mA)	(mA)	β
1	2.251	1.688	2.998
2	2.237	1.667	2.925
3	2.218	1.653	2.926
4	2.306	1.740	3.074
5	2.269	1.702	3.002
6	2.248	1.683	2.979
7	2.244	1.678	2.965
8	2.269	1.706	3.030
9	2.234	1.669	2.954
10	2.226	1.668	2.989
Average	2.250	1.685	2.984

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Next the Hall plate resistances were measured such that the electron mobility for each individual sensor could be calculated. The measured results of the ten samples were then used to calculate the theoretical Hall current I_H for each individual plate according to Equation (2.61). Using the physical setup illustrated in Figure 5.3 with the Hall plate integrated circuit mounted such that the magnetic field from a rare earth magnet directly above it would intercept the plate perpendicularly. The magnet was then moved up and down with linear magnetic field strength steps and the emitter currents measured using a MASTECH® MS8218 digital multimeter with a resolution of 1 µA, hence also reflecting the uncertainty in the measurement. The measured differential emitter current thus consists of the differential base currents of the transistors multiplied by $\beta+1$ as indicated by Equation (4.8). As with the Hall voltage, the Hall current appears positive through one of the BJT's and negative through the second, the sign reflecting the specific direction of the intercepting magnetic field.

Based on the results given in Table 4.2, the Hall current I_H could be calculated. The differential emitter currents $\Delta I_{EH} = I_{E2} - I_{E1}$ for each device was measured individually. A comparison of a typical measured ΔI_{EH} current and the calculated elemental Hall currents I_H is summarized in Table 5.2. The magnetic field itself was calculated by using the A1302 output voltage as reference. This is graphically illustrated in Figure 5.4. The Hall plate was subjected to a maximum magnetic field of approximately ±185 mT at a bias voltage of $V_{bias} = 1.7$ V.

In Table 5.2, it can be seen that the output of the Hall device is fairly consistent with the expected theoretically calculated geometrically corrected Hall currents (without amplification) for the ten Hall devices. It can thus be shown that the required sensitivity to measure 1 Gauss would be in the order of 150 nA, a feat easily achievable using very simple current mirroring techniques. Furthermore, by using high gain BJT's available in a BiCMOS process, significant gains can be made using this technique.

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Table 5.2 Theoretical Hall current without amplification and the average measured emitter Hall current calibrated against the A1302 output voltage

Calculated Magnetic Field B	A1302 output V_{out}	Measured emitter Hall current (average) I_{eh}	Theoretical Hall current I_H
(mT)	(V)	(μA)	(μA)
184.62	4.9	116.14	26.44
169.23	4.7	107.91	24.24
153.85	4.5	98.98	22.03
138.46	4.3	90.65	19.83
123.08	4.1	81.40	17.63
107.69	3.9	72.87	15.42
92.31	3.7	64.14	13.22
76.92	3.5	56.01	11.02
61.54	3.3	47.27	8.81
46.15	3.1	38.53	6.61
30.77	2.9	30.51	4.41
15.38	2.7	22.48	2.20
0.00	2.5	14.35	0.00
-15.38	2.3	6.31	-2.20
-30.77	2.1	-2.52	-4.41
-46.15	1.9	-10.75	-6.61
-61.54	1.7	-20.18	-8.81
-76.92	1.5	-28.22	-11.02
-92.31	1.3	-37.34	-13.22
-107.69	1.1	-45.87	-15.42
-123.08	0.9	-54.51	-17.63
-138.46	0.7	-63.14	-19.83
-153.85	0.5	-72.48	-22.03
-169.23	0.3	-81.11	-24.24
-184.62	0.1	-93.06	-26.44

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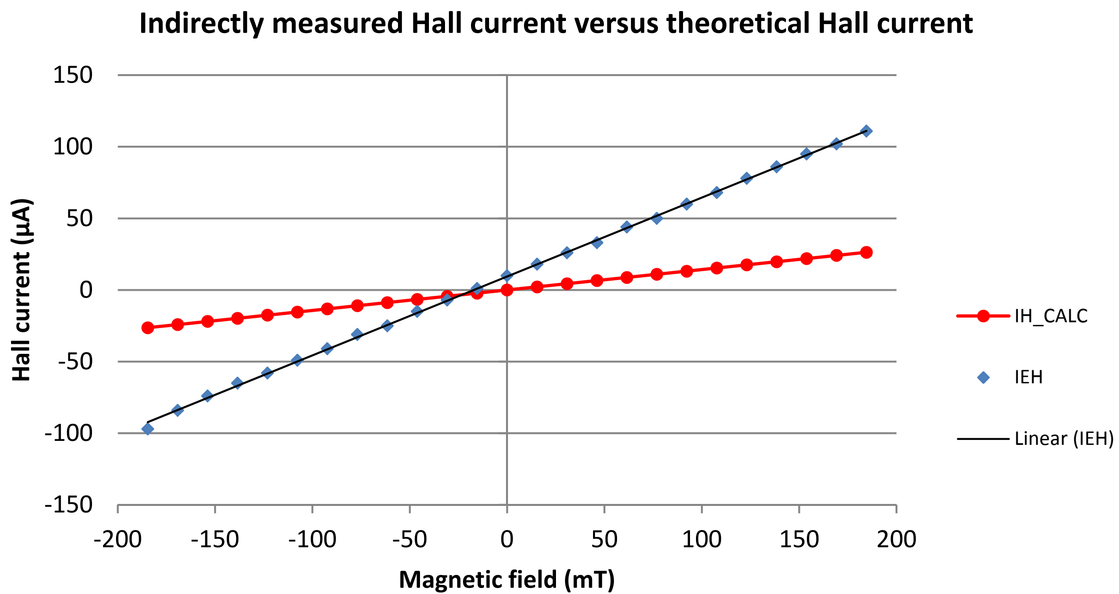

Figure 5.4 Measured differential emitter current ΔI_{EH} of one Hall device compared to the theoretical Hall current I_H in µA versus the magnetic field B in mT.

From Figure 5.4, it can be seen that a linear signal response is observed from the transistor circuit. The offset is in the order of 9 mT, which is not excessive, since no layout or circuit techniques were used to improve transistor matching. It can also be observed that the measured output current signal is significantly larger than the Hall current signal derived theoretically for the basic Hall element with no transistor readout. This is due to the current gain of the transistors.

5.5 STATISTICAL ANALYSIS

With the fabricated BJTs in fair agreement with the theoretical and simulated values according to the geometrically corrected formulae, it is now possible to assess whether or not the method shows any improvement in the measured Hall signal over traditional methods. The data is of interval type and unequal variance will be assumed due to the influence that the BJT characteristics may have on the measured results. The aim is to assess whether the measured data belongs to the geometrically affected results according to

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Equation (2.61) or not. The parameter to be tested thus requires testing the difference between two means with an unknown population variance using the two tailed t-test [122]. The critical value t will be calculated as shown in Equation (5.1) and is based upon the difference between the measured average x_1 and calculated average x_2 with variance s and number of samples n. This difference is then compared to the hypothesized population means μ_1 and μ_2 assumed to be equal.

$$t = \frac{(\overline{x_1} - \overline{x_2}) - (\mu_1 - \mu_2)}{\sqrt{\frac{s_1^2}{n_1} + \frac{s_2^2}{n_2}}} \qquad (5.1)$$

Equation (5.2) is used to calculate the required degrees of freedom v used to assess the tabulated t statistic based on a 95% confidence level or $\alpha = 0.05$.

$$v = \frac{\left(\frac{s_1^2}{n_1} + \frac{s_2^2}{n_2}\right)^2}{\frac{\left(\frac{s_1^2}{n_1}\right)^2}{n_1 - 1} + \frac{\left(\frac{s_2^2}{n_2}\right)^2}{n_2 - 1}} \qquad (5.2)$$

The confidence interval estimator can be calculated as in (5.3) with $t_{\alpha/2}$ the t-test based on the confidence level as stated in the previous paragraph.

$$(\overline{x_1} - \overline{x_2}) \pm t_{\alpha/2}\sqrt{\frac{s_1^2}{n_1} + \frac{s_2^2}{n_2}} \qquad (5.3)$$

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5.5.1 Geometrically affected Hall signal

As the aim is to assess whether or not the measured data belongs to the predicted value according to Equation (2.61), the null hypothesis can be stated as in Equation (5.4).

$$H_{0:}\,(\mu_1 - \mu_2) = 0 \tag{5.4}$$

The alternate hypothesis thus follows in Equation (5.5).

$$H_{1:}\,(\mu_1 - \mu_2) \neq 0 \tag{5.5}$$

5.5.2 Statistical results

Ten samples were characterized to assess their base parameters for example plate resistance etc. required to calculate the expected theoretical results for each device. Each sample's output was then measured at the maximum magnetic field of 185 mT in both magnetic directions, averaged and then statistically compared to the theoretical mean value. The Hall emitter current was measured for each device and the BJT base currents were calculated and tabulated and are summarized in Table 5.3 with the statistical calculations shown in Table 5.4. From Table 5.3 it can be seen that the Hall current output of the Hall device is fairly consistent with the expected geometrically corrected Hall current calculated per individual device according to Equation (2.61). The specific interest is whether or not there is a difference between the measured and expected results at a confidence level of 95%, more specifically the P-value of the two-tailed t-test result. With the aid of the statistical data analysis pack in Microsoft Excel, the various statistical parameters could be calculated.

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Table 5.3 Summary of measured Hall currents

Sample	Measured Hall current		Calculated Hall current	
	I_{EH} @ ±185 mT (μA)	I_H @ ±185 mT (μA)	I_H @ ±185 mT and G = 1	I_H @ ±185 mT and G ≠ 1
1	104.00	26.01	36.56	26.51
2	103.00	26.24	36.59	26.54
3	102.50	26.11	36.11	26.19
4	110.50	27.12	36.29	26.32
5	104.50	26.11	36.11	26.19
6	104.00	26.14	36.29	26.32
7	106.50	26.86	36.82	26.71
8	106.00	26.30	36.82	26.71
9	97.00	24.53	36.56	26.51
10	104.00	26.07	36.41	26.40

Table 5.4 Summary of the statistical analysis

Statistic	I_H	Equation
Mean	26.15	
Variance	1.929	
Observations	20	
Degrees of freedom	20.36	(5.2)
$t_{0.05,20.36}$ two-tail	2.09	
P(T<=t) two-tail	0.37	
t Statistic interval estimator UL (geometrical)	0.370	(5.3)
t-value (geometrical)	-0.917	(5.1)
t Statistic interval estimator LL (geometrical)	-0.950	(5.3)

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5.5.3 Interpretation

5.5.3.1 Geometrically affected Hall signal

From Table 5.4, the test statistic is -0.917 which is greater than the critical value of -2.09. The corresponding two-tailed p-value is equal to 0.37. At these values greater than or equal 0.05, there is not enough evidence given the chosen confidence level of 95% that the measured emitter current represents a Hall current that is not related to the geometrically affected Hall current results given by Equation (2.61). There is thus not enough statistical evidence to reject the null hypothesis in Equation (5.4) in favor of the alternate hypothesis in Equation (5.5). In principle this does not necessarily mean that the null hypothesis is true, only that there is not enough evidence currently to suggest that it is false and that the measured emitter current represents the behavior as predicted by Equation (2.61). It does however seem that there is statistical evidence indicating a correlation with these theoretically predicted values. Taking the ten sample averages over the full magnetic scale however reveals a striking consistency with the geometrically affected output as predicted by Equation (2.61) and it would be logical to interpret the result as that it is most likely behaving in this manner and is also affected by the geometrical correction factor in the same way that traditional Hall devices using ohmic contacts are affected. The results also suggest no significant improvement in the Hall current itself using this method.

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CHAPTER 6 CONCLUSION

6.1 INTRODUCTION

The previous chapter discussed the research results. This chapter revisits the purpose of this research with specific emphasis on answering the research questions and hypothesis. Final conclusions will be drawn on the implications this research may have on existing theory and the chapter will be concluded with recommendations for future research. The chapter and this research will be summarized with a few concluding remarks.

6.2 THE OUTCOMES OF INDIRECT SENSING TECHNIQUES IN CMOS HALL DEVICES

The initial aim and main focus of this research was to find a novel new method to sense the Hall effect fabricated as part of a standard CMOS process. Since 2000, there has been a large amount of patents filed on the Hall sensor which peaked in 2006 and has been on the decline ever since. This is a sure sign of saturation of technology and given the Hall sensor is such a useful and robust device, this research contributes to a fundamental mind shift in how these sensors can be used.

6.2.1 Research question 1

Is it possible to reduce or eliminate short circuiting effects of the Hall voltage resulting from traditional direct sensing contacts using indirect sensing techniques?

The **major finding** from the statistical evidence presented was that even though not enough evidence existed to suggest a significant improvement in the geometrical factor, there was also no significant degradation either. The **main conclusion** was that there existed enough statistical evidence at a confidence level of 95% to suggest that the device behaved strikingly similar to the practical approximation as given by Equation (2.63). The **implication** of this finding is that Equation (2.63) being valid for a sense contact to width ratio, $s/w < 0.18$, that the limits of the CMOS technology have not yet been explored. The minimum size of a low ohmic sense contact in the 0.35 µm process is 0.7 µm. At $s/w = 0.18$ in this technology, it implies that the limits of this finding will only be tested for a width << 3.8 µm. At these dimensions the Hall device falls under microbead sensing technology. Lastly, the technology specifies the minimum width for the n-well as 1.7 µm.

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6.2.2 Research question 2

What are the main noise sources in conventional CMOS Hall effect devices?

Current literature was consulted and the **major finding** was that conventional CMOS Hall devices are influenced by noise sources that can be divided into two groups namely generation noise and modulation noise. Generation noise is associated with internal electromotive force fluctuations and is independent of device biasing conditions. Modulation noise is associated with fluctuations of device parameters and present only whilst current is flowing through the device. The different types of noise sources, type and typical influence is tabulated in Table 6.1.

Table 6.1 Summary of noise sources in conventional CMOS Hall devices

Noise Source	Type	Typical influence
Thermal	Generation	50-200 nT/√Hz
Shot noise	Modulation	10^{-21} T/√Hz
1/f noise	Modulation	0.55-1 μT√Hz
Generation-recombination	Modulation	200-500 nT/√Hz

The **main conclusion** was that of the four main noise sources, 1/f noise was the most dominant of the four noise sources and increasing with reduction in device dimensions. This was followed by generation-recombination and thermal noise. Using correlation techniques it will be possible to significantly reduce the effects of these noise sources. The **implication** is that for high performance devices it will be necessary to incorporate mechanisms to filter, reduce or even eliminate various noise signals from information carrying signals. Furthermore, with increasing uses being found for the Hall device in nanoscale applications, better techniques may be required to be developed to deal with noise specifically associated with shrinking dimensions such as 1/f noise.

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6.2.3 Research question 3

How will indirect sensing influence the noise performance of CMOS Hall sensors?

The **major finding** was that this method does influence the noise performance. In fact, the use of any newly introduced elements such as the BJT's proposed in this research brings along with them their own noise sources. It was found that in BJT's for example that although shot noise and 1/f noise is the dominant noise source. It is not only affected by generation-recombination noise, thermal noise and shot noise as with the Hall device, but may also be affected by burst noise if the quality of the transistor is not up to the proper standard. Being a parasitic BJT, the desired properties thereof may not be optimized toward the highest performance for the purpose of a BJT application. In comparison to a typical differential operational amplifier used to amplify the signal using the voltage mode of working and by a similar factor as the BJT, the BJT method is an improvement over the voltage mode sensing method. The **main conclusion** is that it will be required to take into account any new sources that may be introduced but also to compare it to similar alternatives before drawing conclusions regarding performance. The **implication** is that it will be necessary to experiment and build a new noise model for the proposed Hall device consisting of the sum of the superimposed individual noise contributors.

6.2.4 The hypothesis

It was **hypothesized** that if direct sensing contacts used to measure the Hall effect of a semiconductor Hall effect device results in a diminution of the Hall signal, then indirectly sensing the Hall signal may regain lost Hall effect by eliminating short circuiting effects resulting from direct contact.

The first research question and the collective data presented in Chapter 5 resulted in the **rejection of the hypothesis** and that there did not exist enough evidence to support a significant increase in the geometrical factor between a point sense contact Hall device and the newly proposed indirect sensing method according to Equation (2.62).

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6.3 IMPLICATIONS ON EXISTING THEORY

This research has the following major implications for existing Hall effect device theory:

- Chapter 2 confirms that Hall effect device theory is very well developed and has been studied for decades. Current theory covers many various methods for detecting the Hall effect such as the Hall plate, VHD, MAGFET, thin films and the magnetoresistors all of which make use of either of the two Hall effect mechanisms namely the Hall voltage and current deflection effect. However, no theory explores the use of integrated current amplifying methods to sense the Hall effect.
- Current theory for more than a decade has been exploring the exploitation of known theory into variations of known devices, but it seems that in this time there has been very little development in terms of new structures to exploit the Hall effect in new novel ways.
- This research expands existing theory by the addition of a new novel Hall effect, indirect sensing device. Based upon known Hall effect and BJT theory, the combination has not only expanded Hall effect theory in terms of a new device, but also suggests a method that may be expanded to many other integrated CMOS sensors. With the addition of one or two elements, parasitic elements with normally negatively effects, can be exploited into extremely useful functions.

6.4 RECOMMENDATIONS FOR FUTURE RESEARCH

This research resulted in many topics that require both further study and analysis. The following recommendations are now stated.

- The use of parasitic devices may result in the non-compliance of specific technologies' DRC rules. It may be required to investigate with the aid of various test structures the effects of currents flowing where it is normally not desired, for example the substrate. Effects such as latchup may also be of concern as a result. Such structures may also result in a combination of structures not normally

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anticipated which may also require further study. Lastly, DRC and LVS rules may require adaptation to accommodate such novel structures.

- Modelling the device for simulation will be required for the proper design and simulation of the newly proposed Hall device into full systems. The addition of the BJT may have other higher order effects that are currently not being modelled by various known methods as discussed in Chapter 2.5.
- The device presented in this research was focused on the square plate geometry. The idea of integrating the BJT into other geometrical shapes should be researched for potential gains not covered in this text.
- The device presented in this research focused on dimensions well within the mathematical boundaries reported in this text as well as the technological limits of the chosen CMOS process. Shrinking the dimensions to the process limits will also yield results on or over the mathematical boundaries. These boundaries need exploring to determine the validity of the concepts reported in this research.
- The output of the BJT emitters may have many different methods of using and interpreting the signal. A system should be designed to use and convert the measured signal into a useful integrated system.
- The use of the integrated BJT concept as applied to other potential sensors and/or fields of study.
- Lastly, combined effects of the Hall device with the integrated BJT requires more depth in terms of parasitic effects, noise implications, V_{be} offset variations etc.

6.5 CONCLUSION

The major contribution of this research resides in a novel method to measure as well as amplify the Hall effect in a square CMOS plate. The device although not supporting the initial hypothesis, was proven to be functional as well as behaving according to Hall effect theory. This chapter concludes the research by answering the research questions posed in Chapter 1.4.1, discussing the outcome of the hypothesis in Chapter 1.4.2 as well as presenting the implications on existing theory and recommendations for future research.

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