QUASI-Z-SOURCE THREE-PHASE RECTIFIER MODELLING AND CONTROL

By

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SUMMARY

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Keywords: AC to DC converter, Z-source rectifier, quasi-Z-source rectifier, buck-boost rectifier, shoot-through, dynamic model, control.

AC to DC rectifiers are used as front-end interface in multiple applications with DC load or in inverter fed from line voltage. In applications with variable AC input voltage, rectifiers with buck-boost capability are critical for achieving the most efficient power conversion. The Z-source rectifier has been presented as the most suitable rectifier with buck-boost performance. This dissertation introduces and analyses the quasi-Z-source rectifier as an alternative efficient AC to DC converter with buck-boost capability. The model of the quasi-Z-source rectifier is derived. The model of the Z-source rectifier is also derived with an alternative approach. It is found from analytical results of the modelling that the quasi-Z-source is a more cost-effective rectifier than the Z-source rectifier due to lower rated capacitors. A two stages closed-loop controller for the quasi-Z-source rectifier is then designed. Software simulations and hardware experiments of the quasi-Z-source rectifier are performed and the results obtained confirm its efficient performances. This makes the quasi-Z-source rectifier appropriate in renewable energy systems with AC voltage variations such as wind power.

OPSOMMING

KWASI-Z-BRON DRIEFASE-GELYKRIGTER MODELLERING EN BEHEER

Deur

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Sleutelwoorde: WS na GS omsetter, Z-bron gelykrigter, Kwasi-Z-bron gelykrigter, bok-hupstoot gelykrigter, deurskiet, dinamiese model, beheer.

WS na GS gelykrigters word gebruik as 'n voorkant-koppelvlak in verskeie toepassings met GS vrag of met ’n omsetter gevoed vanaf lynspanning. Toepassings met veranderlike WS insetspanning gee dat gelykrigters met bok-hupstoot vermoë van kritieke belang is vir die bereiking van die mees doeltreffende drywing omskakeling. Die Z-bron gelykrigter word as die mees geskikte gelykrigter met bok-hupstoot vermoë voorgestel. Hierdie verhandeling stel en ontleed die kwasi-Z-bron gelykrigter as 'n alternatiewe doeltreffende WS na GS omsetter met bok-hupstoot vermoë. Die model is afgelei van die kwasi-Z-bron gelykrigter. Die model van die Z-bron gelykrigter is met ’n alternatiewe benadering afgelei. Vanuit die analitiese resultate van die modellering van die kwasi-Z-bron is bevind dat eersgenoemde 'n meer koste-effektiewe gelykrigter as die Z-bron gelykrigter tot gevolg het a.g.v. van verlaagde kapasitor spesifikasies. ’n Twee fase geslotelus-beheerder vir die kwasi-Z-bron gelykrigter word dan ontwerp. Sagteware simulasies en hardeware eksperimente van die kwasi-Z-bron gelykrigter word uitgevoer en die resultate wat verkry is bevestig sy doeltreffende verrigting. Dit maak die kwasi-Z-bron gelykrigter toepaslik in hernubare energie stelsels met WS spanning variasies o.a. windkrag opwekking.

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LIST OF ABBREVIATIONS

AC:	Alternating Current
A/D:	Analog to Digital
CSR:	Current Source Rectifier
DC:	Direct Current
DSP:	Digital Signal Processor
IC:	Integrated Circuit
FPGA:	Field Programmable Gate Array
MIMO:	Multiple-Input Multiple-Output
MPC:	Model Predictive Control
PI:	Proportional-Integral
PID:	Proportional-Integral-Derivative
PWM:	Pulse Width Modulation
QZSI:	Quasi-Z-Source Inverter
QZSR:	Quasi-Z-Source Rectifier
RHP :	Right Half Plane
V-DPC:	Voltage-direct Power Control
VF-DPC:	Virtual Flux-Direct Power Control
VFOC:	Virtual Flux Oriented Control
VOC:	Voltage Oriented Control
VSR :	Voltage Source Rectifier
ZOH:	Zero-Order Hold
ZSI:	Z-Source Inverter
ZSR:	Z-Source Rectifier
ZVS:	Zero Voltage Switching

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CHAPTER 1 INTRODUCTION

1.1. RESEARCH BACKGROUND AND MOTIVATION

The currently limited electrical energy resources available in the world and the rapidly increasing demand require energy efficient systems to decrease losses and to increase power availability. Power electronics systems are widely used as interfaces in power processing and have significant positive impact on the energy efficiency of many systems [1]. Power electronics converters make extensive use of inductors and capacitors as intermittent energy storage elements [1]. These passive elements are major factors in the energy efficiency, size and cost [1]. To achieve energy and cost-efficient systems, power electronics interfaces are required to be the most effective for the application and optimally designed.

A large number of applications such as motor drives, uninterruptible power supplies, battery charging and renewable energy sources like wind power require a rectifier as front-end processing unit to convert Alternating Current (AC) power to Direct Current (DC) power [2]. Traditionally AC to DC conversion was done with phase-controlled thyristor rectifier in Figure 1.1. Switch mode AC to DC conversion was done with the conventional Voltage Source three-phase Rectifier (VSR) in Figure 1.2 and with Current Source three-phase Rectifier (CSR) in Figure 1.3 [2]-[5]. Phase controlled rectifier drawbacks include, a decreasing power factor as the firing angle increases, and a high harmonic content input AC current, which result in a low energy efficiency conversion [2]-[4]. The advantages of the VSR over the phase controlled rectifier include, its capabilities of nearly instantaneous reversal of power flow, power factor correction, and reduction of input harmonic distortion [2]-[4]. The merits of CSR include circuit protection and rapid current response, but require bulky AC-line capacitors and DC-line inductors [3] [4].

However a VSR is essentially an AC-DC boost converter while a CSR is an AC-DC buck converter. This represents a major limitation in applications such as wind power requiring the DC output voltage to be constant irrespective of the variations of the peak value of the AC input voltage [3]-[6]. VSR or CSR will have to cascade a DC-DC converter as shown in Figure 1.4 to maintain a constant DC output voltage regulation in presence of the variations of the peak input AC voltage [7]. This leads to a less efficient system and additional complexity. Furthermore, VSR and CSR can sustain damage with short circuiting of any of the full-bridge switches leg caused by EMI noise and consequently decreases its reliability [3] [4].

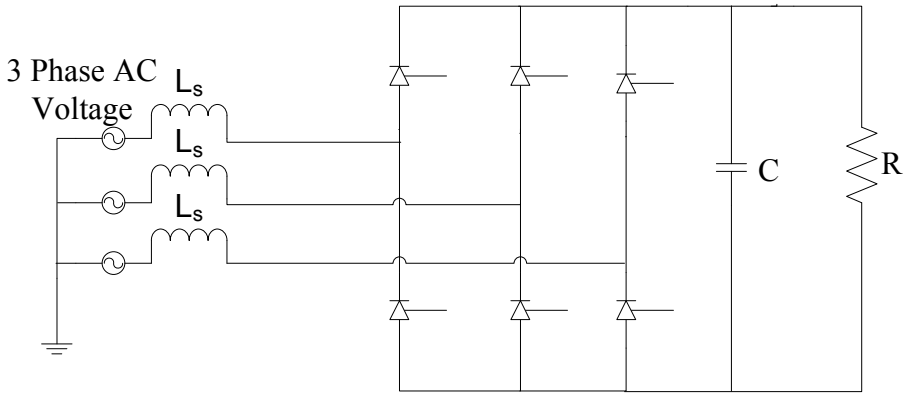

Figure 1.1. Phase-controlled thyristor three-phase rectifier

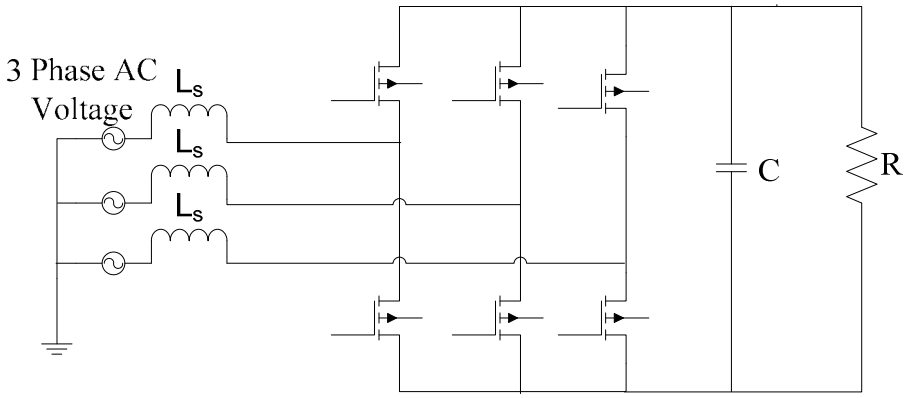

Figure 1.2. Voltage source three-phase rectifier

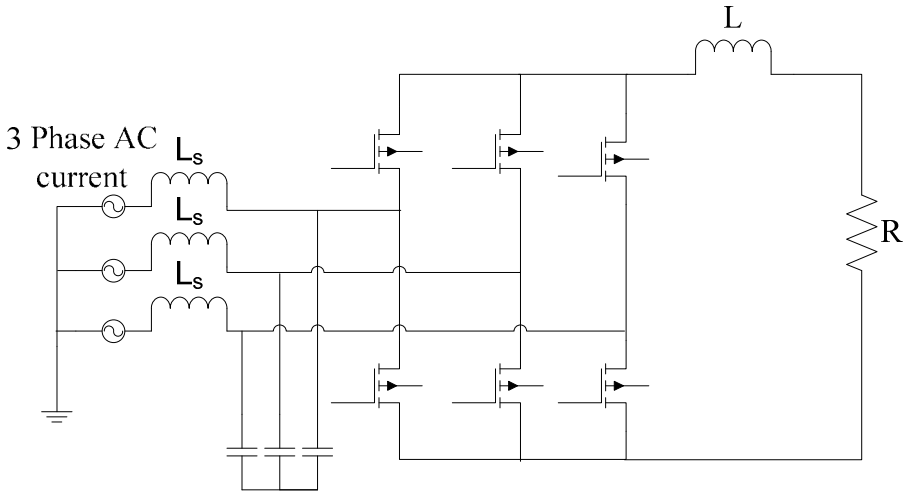

Figure 1.3. Current source three-phase rectifier

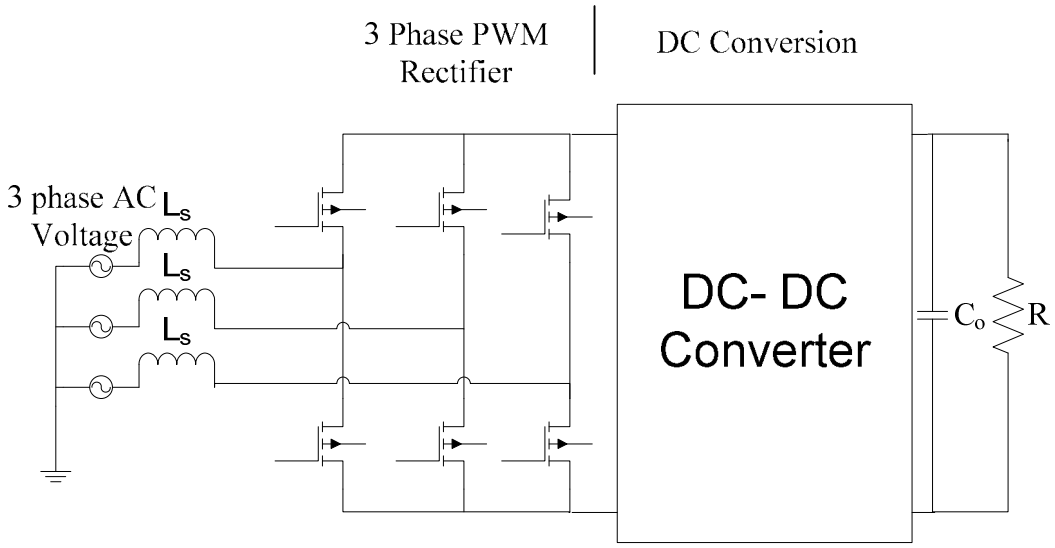

Figure 1.4. Two stage buck-boost PWM rectifier

To overcome the limitations of the conventional VSR and CSR, the Z-source three-phase rectifier (ZSR) was proposed in [8] and illustrated in [3] [4] with a voltage source such as in Figure 1.5. The ZSR features an unique impedance network and can produce a DC voltage larger or smaller than the peak value of the AC input voltage while operating at unity power factor with low harmonic distortion of the input AC current [3] [4] [5] [6] [7]. The current source ZSR in [9] also overcomes the limitations of the conventional CSR by providing buck-boost capability with bidirectional power flow. Unlike a conventional VSR or CSR

rectifier, the ZSR has one extra switching state, which is the shoot-through state. It has in total nine permissible switching states consisting six active vectors and three zero vectors including one with shoot-through [8]. The shoot-through state can be considered as short circuiting of both the upper and lower switches of any one phase leg, two phase legs or all three-phase legs [8]. During shoot-through state, the switch SW must be kept open [8].

This shoot-through zero state provides a unique feature of buck-boost operation [3] [8]. Unlike the VSR or CSR that can sustain damage during shoot-through state, the ZSR does therefore operate during shoot-through period, which increases its reliability compared to the VSR. The ZSR makes use of the shoot-through period to control the output voltage value. Any Pulse Width Modulation (PWM) technique can be used to control the ZSR [6]. The available shoot-through period is limited by the full-bridge modulation index and the Z-source circuit switch gating is synchronised with the full-bridge switches gating [6] [7] [8]. Rather than being seen as a two stages rectifier, the ZSR is indeed a one stage rectifier with insertion of the Z-source circuit control within the full-bridge PWM rectifier control. The buck-boost capability of the ZSR therefore makes it attractive to applications requiring a constant DC output with input AC voltage variations, such as in renewable energy sources and weak AC systems with poor voltage regulation.

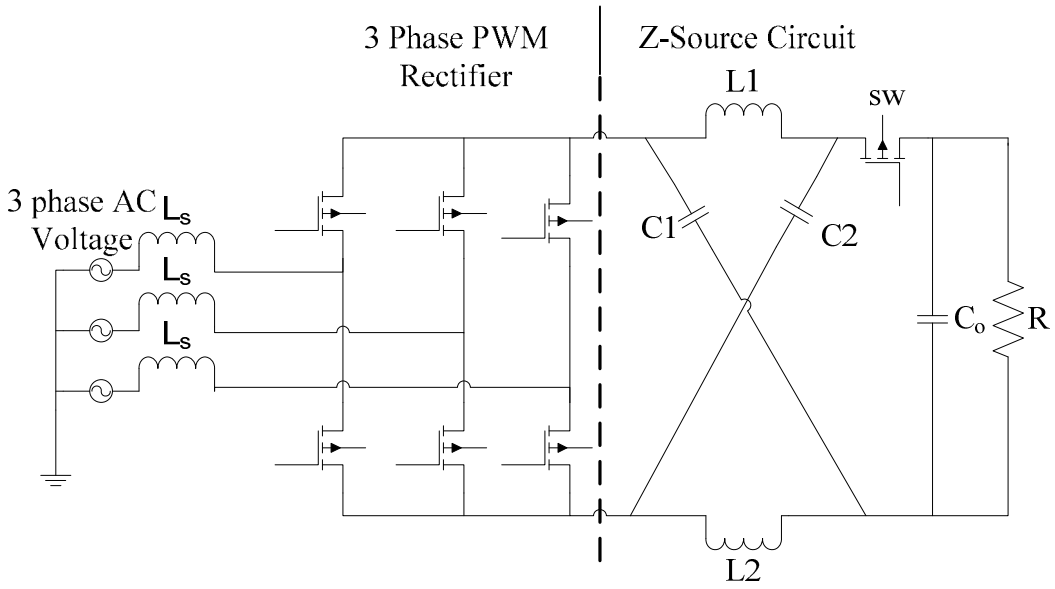

Figure 1.5. Voltage source Z-source three-phase rectifier

To improve on the traditional Z-source inverter, the quasi-Z-source inverter concept was developed in [10]. Similar to the Z-source circuit of [3] [4] [5], the quasi-Z-source circuit can also be used in AC to DC conversion. This research then introduces the quasi-Z-source three-phase rectifier (QZSR) shown in Figure 1.6 and analyses it to show its advantages over the ZSR.

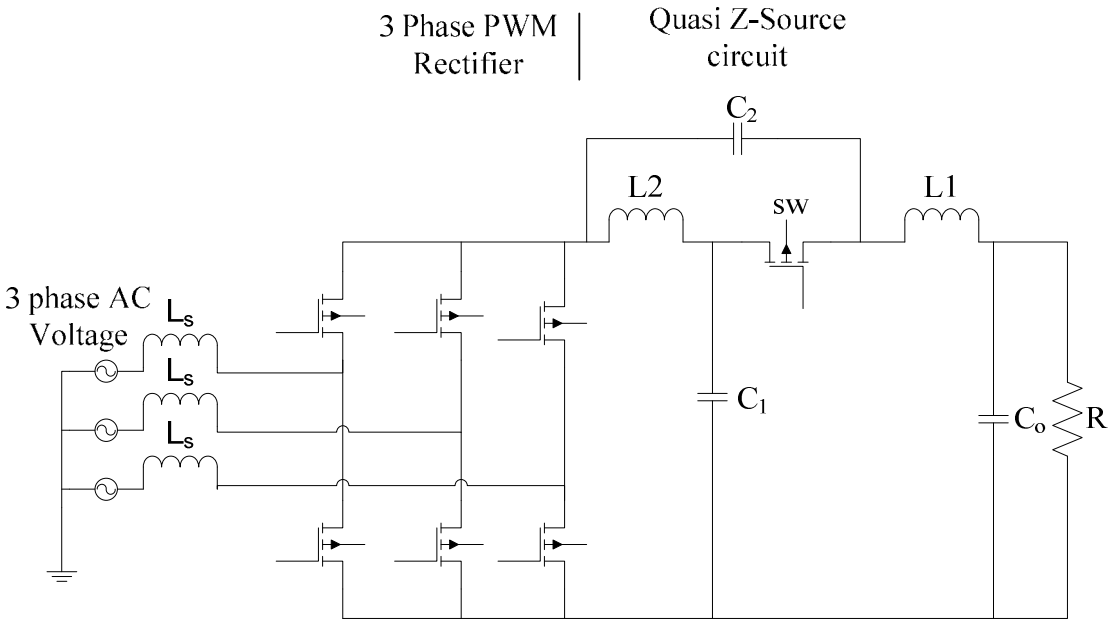

Figure 1.6. Quasi-Z-source three-phase rectifier

The quasi-Z-source three-phase rectifier in Figure 1.6 inherits all the advantages of the traditional Z-source three-phase rectifier and also features several improvements. These additional advantages of the QZSR include:

- The two capacitors C_1 and C_2 in the ZSR have to block the same DC voltage amplitude but the DC voltage of capacitor C_2 in the QZSR is much lower, which result in a lower capacitor C_2 voltage rating in the QZSR.
- The output capacitor C_o of the ZSR has to filter larger harmonic amplitude and has to sustain the full load current during shoot-through state, but the output capacitor C_o of the QZSR filters low harmonic amplitude because of the filtering provided by inductor L_1. Therefore, the current and voltage ratings of the output capacitor for the QZSR are much lower than the ZSR output capacitor.
- For the QZSR, there is a common DC Bus between the load and the rectifier, which makes it easy to build and results in less EMI problems.

Capacitors contribute a larger proportion of the total cost and space in a power electronic converter. Lower rated capacitors in the QZSR therefore make it a more cost effective rectifier compared to the ZSR. Similar to the ZSR, the QZSR has nine permissible switching states consisting of six active vectors and three zero vectors including one with shoot-through to obtain the buck-boost feature [10]. Any PWM modulation technique can be used to operate the QZSR [10].

The increasing electrical power demand and the reduced power availability require energy efficient systems. It is important to realise that the bulk of power generation is AC while a large portion of loads are DC. Thus the need of very efficient rectifiers as front end interface. The recently proposed Z-source three-phase rectifier and the quasi-Z-source three-phase rectifier that is introduced do potentially show attractive features. These could provide an alternative to the conventional active rectifier in applications with input AC voltage variations. Until now the ZSR and the QZSR had yet to be thoroughly analysed dynamically and optimally controlled to establish their full potential, limitations and possible improvements. Such analysis includes developing each rectifier model, comparing them analytically, and designing a closed-loop controller for the better rectifier to assess its performances. The motivation of this study is therefore to formally establish the performances of the ZSR and the QZSR as potential energy efficient interfaces.

1.2. LITERATURE REVIEW

Various methods of analysis for switching power converters have been developed up to now [1]. In most cases, they result in either significant reduction of the required amount of mathematical manipulations of the derivations for analysis, or models that represent all the essential properties with satisfactory accuracy [1]. Modelling of AC to DC rectifiers is done by combining the AC and DC side quantities in a single unit system, or reference frame, to simplify the analysis. The synchronous reference frame [11] is a popular tool in developing dynamic models of three-phase systems. It simplifies rectifier modelling by providing control parameters as DC quantities, and enables easy control of active and reactive power independently [11]. The single unit reference frame model of AC to DC converters can then be further used in one of the power converters modeling tool to obtain the detail dynamic

model. One of the most popular tools in analysis and design of power converters proposed by Middlebrook *et al*. [12] in 1976 is state-space averaging technique. It gives a convenient and compact way to model and study systems with multiple inputs and outputs [1] [13]. An alternative power converter modelling tool is circuit averaging in which solving time averaged system of equations is required [1] [13]. Since circuit averaging requires averaging and small-signal linearization, it is equivalent to state-space averaging [1] [13]. However, in many cases circuit averaging is easier to apply, and enables the small-signal AC model to be written almost by inspection [1] [13].

In the process of designing the controller circuits for the rectifiers, knowledge of transfer functions relating the dynamics of various variables is essential. Small-signal model of the rectifiers not only provides an overview but also a detailed view of system dynamics due to variation of passive components, guidelines on how to size them and understanding of the limit of systems. Research contributions on the dynamic modelling and the transient analysis of the ZSR are limited by the extent of the analysis and complexity involved [6] [7] [14] [15]. The dynamic model proposed in [6] [7] for the voltage source ZSR and in [15] for the current source ZSR combines the active rectification and the Z-source circuit model in a synchronous reference frame. This can provide all the transfer functions but the approach is complex to implement as it requires a 5x5 matrix inversion.

The ZSR concept is analytically introduced in [3] [4] [5] to show its buck-boost capability. The modified ZSR is also presented in [16] and [17] with the ability of zero voltage switching (ZVS). The analytical studies proposed do not show the significance (in terms of all components currents, voltages and dynamic response) of different operating points chosen and whether these are practically achievable. The controller proposed in [17] for the zero voltage switching Z-source three-phase rectifier is optimised for a specific operating point, and the performance of the system for input AC voltage variations is not presented.

An important and commonly used assumption in the analysis of the operating principle [3]-[5] of the Z-source circuit and in the dynamic modelling of the Z-source circuit [6] [7] [14] [17] is symmetry of passive components of the Z-source circuit. Symmetry of the Z-source

circuit refers to equal inductors and capacitors. While this simplifies the analysis of the Z-source circuit, there however is no mathematical basis given that justifies the need to use symmetrical components in the Z-source circuit.

The research contributions on the ZSR from [3] [4] [5] [6] [7] have analytically shown the steady state output voltage regulation capability of the ZSR and its buck-boost capability. However, test results of the output voltage regulation during peak AC input voltage and load current variations have not been presented due to the absence of a fast closed-loop control scheme. The steady state results given in the literature are based on open loop operations of the ZSR in [3] [4] [5] [6] [7] for instance. In [14] the limitations and difficulties of designing a fast closed-loop controller are pointed out using the dynamic model from [6]. These challenges mainly arise from the non-minimum phase zero encountered in the output voltage transfer function of buck-boost topology. Several closed-loop control schemes [18] [19] [20] [21] [22] [23] [24] have been developed for the Z-source inverter, which can be adapted to design a robust fast closed-loop controller for the conventional ZSR.

The quasi-Z-source concept is introduced in [10] with an inverter operating in open-loop. The quasi-Z-source circuit is also illustrated as quasi-Z-source inverter (QZSI) in several applications such as photo voltaic systems [25] [26], wind power generation system [27]-[29] and current-fed inverter systems [30] [31]. A dynamic average model of the QZSI is developed in [32]. A controller based on the extended boost is presented in [33], while two stages closed-loop controller for the QZSI is used in [34] for photo voltaic systems. The use of a QZSI inverter in wind power system could be substituted with a Quasi-Z-source three-phase rectifier. Using a QZSR as front end converter in wind power can be assessed against the QZSI in terms of components count, efficiency, and system complexity. However, the quasi-Z-source three-phase rectifier's operating principle, dynamic model, and closed-loop control are yet to be presented in the literature.

As stated in [8] and [10], all the PWM control methods can be used to control the ZSR and QZSR. The following PWM control methods applicable to the Z-source source inverter can

be used for the ZSR and QZSR: simple boost control [9], maximum boost control [35], maximum constant boost control [36], and the modified space vector PWM control [37]. The simple boost uses two straight lines equal to or greater than the peak value of the modulating signal of each phase to control the shoot-through duty ratio in a traditional sinusoidal PWM as shown in Figure 1.7 similar to what is in [8] [9]. The shoot-through state is activated when the triangular carrier waveform is greater than the upper line V_p or lower than the bottom line V_n. This method is straightforward, but results in high switch voltage stress because some traditional zero states are not utilized [38]. The maximum boost control shown in [35] extends the modulation index range by using all traditional zero states into shoot-through state, so that the switch voltage stress is minimised. But the maximum boost control brings in a low frequency current ripple that is associated with the output frequency in the inductor current and the capacitor voltage [35] [38]. This will cause a higher requirement of the passive components when the output frequency becomes very low, and makes this method suitable for applications that have a fixed or relatively high output frequency [38].

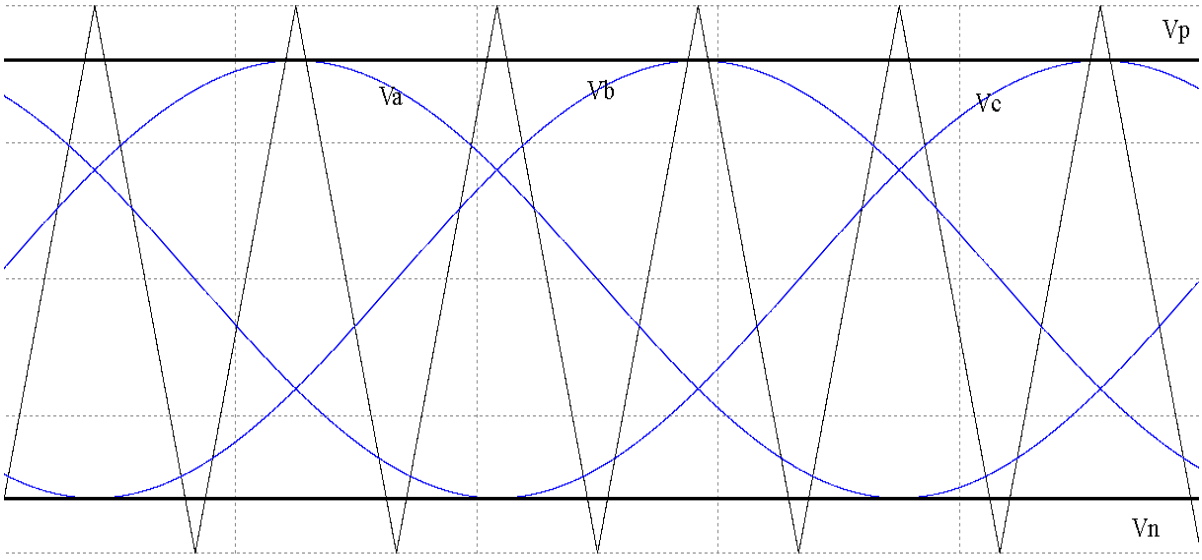

Figure 1.7. Simple PWM control method

The maximum constant boost control shown in [35] achieves the highest voltage gain of all methods at any given modulation index without producing low-frequency ripple that is related to the output frequency, and minimizes the voltage stress at the same time [36]. It therefore requires minimum inductance and capacitance, because the inductor current and

capacitor voltage contain no low-frequency ripples associated with the output voltage, thus reducing the cost, volume, and weight of the Z-source circuit [36]. The operation principle of the maximum constant boost control is identical to the maximum boost control; the only difference is that the modulation waveform is changed [35]. Third harmonic injection is used in the modulating signal to increase the modulation index range [35]. The modified space vector PWM control achieves a desired output AC voltage of the ZSI while minimising the voltage stress across the switch by a large factor [37]. For each of the PWM control method, an expression relating the modulation index and the shoot-through duty cycle is given in Table 1.1 [38].

Table 1.1: PWM control method expression for shoot-through and modulation index [35]

Control Method	**Simple boost**	**Maximum boost**	**Max constant boost**	**MSVPWM**
D	$1-M$	$\frac{2\pi-3\sqrt{3}M}{2\pi}$	$\frac{2-\sqrt{3}M}{2}$	$\frac{2\pi-3\sqrt{3}M}{2\pi}$

1.3. PROBLEM DEFINITION

The literature study suggests that the quasi-Z-source three-phase rectifier is not yet fully analysed, modelled, controlled and compared to the Z-source three-phase rectifier to prove its superior performance. Furthermore, foundation for components symmetry and a simpler modelling approach for ZSR have not been shown in the literature. The specific objectives and goals of this study are then to analyse thoroughly the QZSR in order to establish its competitive advantages and limitations by:

- Deriving a computationally simple and accurate dynamic model of the QZSR
- Modelling the ZSR with a simpler alternative method to obtain its block diagram representation
- Designing a closed-loop controller for the QZSR
- Analytically Comparing the QZSR to the ZSR

1.4. RESEARCH CONTRIBUTIONS

The main contributions of this study in respect to current knowledge will include:

- A computationally simpler and accurate alternative modelling approach of the ZSR leading to its block diagram representation
- An introduction of the QZSR
- A complete and accurate dynamic model of the QZSR
- A comprehensive analytical performances comparison between the ZSR and QZSR
- A practical system design taking into account size, cost and dynamics
- A closed-loop control design of the QZSR

1.5. DISSERTATION ORGANISATION

This dissertation is organised in 6 chapters. Chapter Two addresses the problem of the dynamic model of the conventional ZSR. A simpler modelling approach using circuit averaging is presented, and the mathematical basis for symmetrical Z-source components is shown. The ZSR transfer functions are given along with the inductor DC current and capacitor DC voltage expressions.

Chapter Three presents the quasi-Z-source three-phase rectifier dynamic model obtained using circuit averaging technique. The transfer functions of all variables are given, and the inductor DC current and capacitor DC voltages also obtained. The advantages of the QZSR over the ZSR are shown with a detailed analytical comparison of the two rectifier topology.

In chapter Four, a two-stage digital controller is designed for the quasi-Z-source. A current mode controller is designed for stage one of the input AC current and a voltage mode controller is designed for the quasi-Z-source circuit. Bode plots are given to confirm the effectiveness of the controller for the entire input AC voltage range.

In chapter Five, the performances of the quasi-Z-source three-phase rectifier with the designed controller is verified through software simulations and practical experiment. Performances for wide input voltage variations within the designed range and load changes

are shown. Chapter six concludes the dissertation and suggests potential further research investigations.

CHAPTER 2 THE Z-SOURCE THREE-PHASE RECTIFIER MODELLING

2.1. INTRODUCTION

A Z-source three-phase rectifier is essentially a voltage or current source three-phase PWM rectifier combined with a Z-source circuit. The Z-source circuit modifies the characteristics of the basic VSR or CSR to obtain the buck-boost capability and all the additional advantages. The overall model of the ZSR can be obtained by combining the traditional PWM rectifier model and the equivalent model of the Z-source circuit [6] [14]. Modelling of the ZSR presented in [6] [7] combines the average model of the Z-source circuit with the synchronous reference frame model of the full-bridge into a state space representation to obtain the overall model. However, the model, though accurate, does not give sufficient insight into the controller design and behaviour of the Z-source three-phase PWM rectifier system due to its complex multi-input multi-output (MIMO) nonlinear structure. It is complex to implement as it requires a 5x5 matrix inversion.

State space modelling of the entire system such as in [6] [7] then makes it challenging to design one closed-loop controller for both the three-phase PWM rectifier circuit and the Z-source circuit. This is reflected in the literature where no closed-loop control scheme based on the state space model has yet been proposed. These difficulties also arise due to the interacting nature of the two control variables: the d and q duty cycle and the shoot-through duty cycle. Despite its complexity, the state space approach also has the merit to reveal critical parameters of the system such as the resonance frequencies which are dependent on the influence of both circuits on each other [7].

In this research the dynamics and transfer functions of the ZSR in Figure 2.1 are similarly obtained by modelling the traditional PWM rectifier in synchronous reference frame and the Z-source circuit is modelled with circuit averaging. However the PWM rectifier and Z-source circuit models are not combined using state space in order to keep the analysis

simple and computationally easy to solve. Both averaged models are combined using the peak DC output voltage of the three-phase PWM rectifier full-bridge to obtain the overall block diagram representation which is not presented in [6] [7] due to the complexity of the approach. Modelling the two systems separately enable the design of multiple closed-loop controllers and the ability to adjust the influence of each control circuit on the overall performance of the rectifier. This is similar to the modelling approach adopted in [17] for the ZVS Z-source three-phase rectifier. The model that is derived is more detailed than in [17] by providing inductors transfer functions that can be used for current control of the Z-circuit. Furthermore the modelling approach does show mathematical basis for symmetry of the Z-source circuit passive components and how to size them. This constitutes an additional contribution.

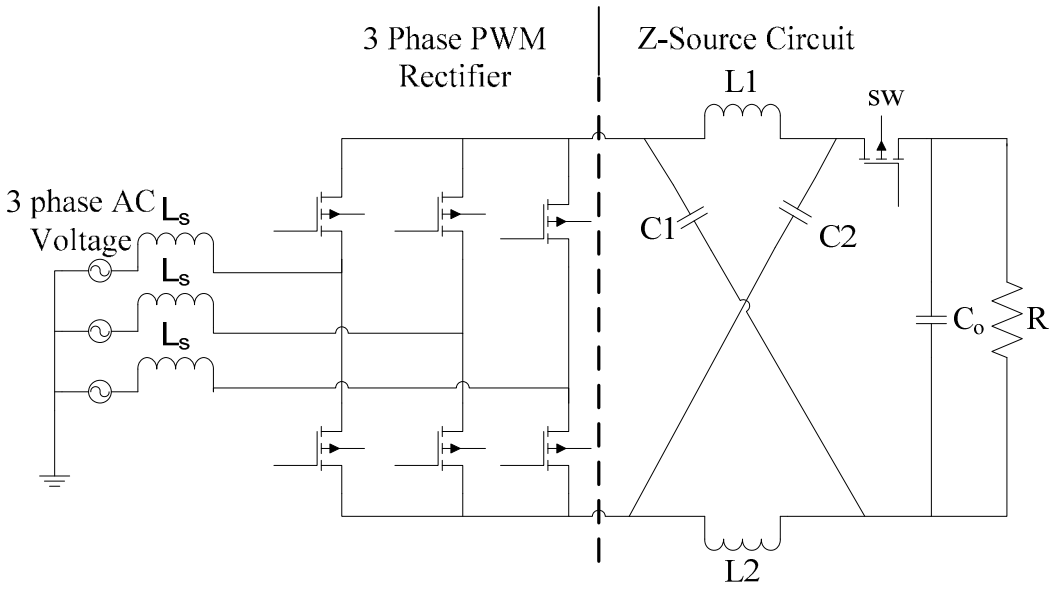

Figure 2.1. Voltage source Z-source three-phase rectifier

The Z-source circuit can be analysed during non-shoot-through and shoot-through period to obtain the steady state operating point [6] [17]. The following assumptions are used in the analysis of the Z-source circuit: the ZSR is operating with continuous inductor current, the passive components L and C are lossless and the switch on time losses are ignored, the shoot-through time is expressed by DT_{sw} and non-shoot-through time by (1-D) $T_{sw} = D'T_{sw}$ based on the simple boost modulation method. T_{sw} is the switching period.

Using Figure 2.2 during non-shoot-through interval, the dynamics of components are given by:

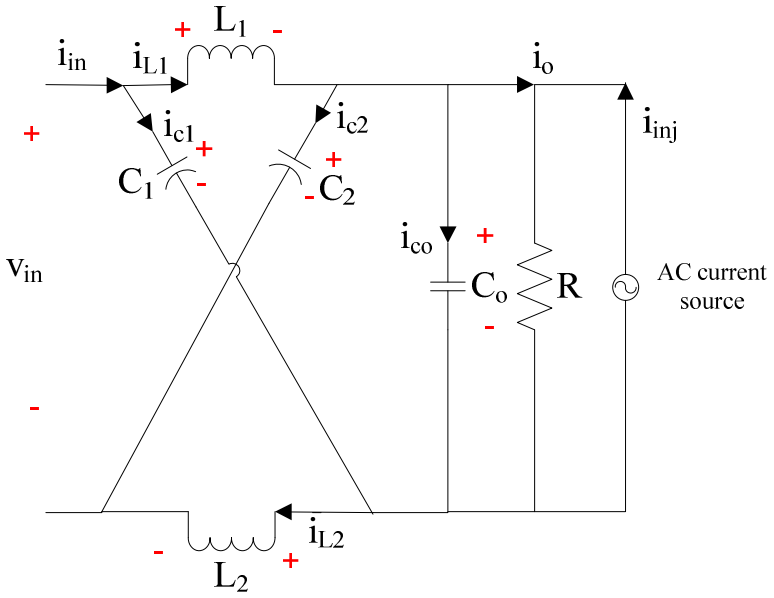

Figure 2.2. Z-source circuit in non-shoot-through mode

$$
\begin{aligned}
L_1 \frac{di_{L1}}{dt} &= v_{in} - v_{c2} \\
L_2 \frac{di_{L2}}{dt} &= v_{in} - v_{c1} \\
L_1 \frac{di_{L1}}{dt} &= v_{c1} - v_{co} \\
L_2 \frac{di_{L2}}{dt} &= v_{c2} - v_{co} \\
C_1 \frac{dv_{C1}}{dt} &= i_{in} - i_{L1} \\
C_2 \frac{dv_{C2}}{dt} &= i_{in} - i_{L2} \\
C_o \frac{dv_{Co}}{dt} &= i_{L1} + i_{L2} - i_{in} - i_o + i_{inj} \\
i_{sw} &= i_{L1} - i_{c2} = i_{L1} + i_{L2} - i_{in} \\
v_{sw} &= 0
\end{aligned}
\tag{2.1}
$$

Where v_{in} is the peak DC output voltage of the full-bridge PWM rectifier and the DC input voltage to the Z-source circuit. i_{sw} and v_{sw} are respectively the Z-source circuit switch DC

current and blocking voltage. i_{inj} is the current injected by a fictitious current source. It is needed to determine the output impedance

During the shoot-through interval shown in Figure 2.3, the dynamics of components are given by:

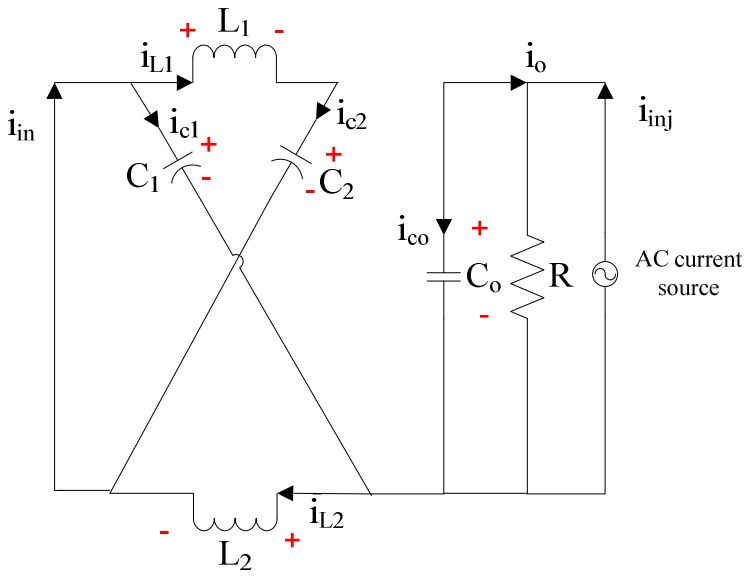

Figure 2.3. Z-source circuit in shoot-through mode

$$
\begin{aligned}
L_1 \frac{di_{L1}}{dt} &= -v_{c2} \\
L_2 \frac{di_{L1}}{dt} &= -v_{c1} \\
C_1 \frac{dv_{C1}}{dt} &= i_{L2} \\
C_2 \frac{dv_{C2}}{dt} &= i_{L1} \\
C_o \frac{dv_{Co}}{dt} &= -i_o + i_{inj} \\
v_{swblock} &= v_{c1} + v_{c2} - v_{co} \\
i_{sw} &= 0
\end{aligned}
\tag{2.2}
$$

The shoot-through duty ratio is used as a weight in the averaging process to obtain differential equations that describe the dynamics of the circuit over an entire switching period as follows:

$$\begin{aligned}
dL_1\frac{di_{L1}}{dt}+(1-d)L_1\frac{di_{L1}}{dt} &= v_{in}(1-d)-v_{c2}\\
dL_1\frac{di_{L1}}{dt}+(1-d)L_1\frac{di_{L1}}{dt} &= v_{c1}(1-d)-v_{c2}d-v_{co}(1-d)\\
dL_2\frac{di_{L2}}{dt}+(1-d)L_2\frac{di_{L2}}{dt} &= v_{in}(1-d)-v_{c1}\\
dL_2\frac{di_{L2}}{dt}+(1-d)L_2\frac{di_{L2}}{dt} &= v_{c2}(1-d)-v_{c1}d-v_{co}(1-d)\\
dC_1\frac{dv_{C1}}{dt}+(1-d)C_1\frac{dv_{C1}}{dt} &= i_{in}(1-d)-i_{L1}(1-d)+i_{L2}d\\
dC_2\frac{dv_{C2}}{dt}+(1-d)C_2\frac{dv_{C2}}{dt} &= i_{in}(1-d)-i_{L2}(1-d)+i_{L1}d\\
dC_o\frac{dv_{Co}}{dt}+(1-d)C_o\frac{dv_{Co}}{dt} &= (i_{L1}+i_{L2}-i_{in})(1-d)-i_o+i_{inj}
\end{aligned} \tag{2.3}$$

Separate the various parameters and variables into DC and AC components:

$$\begin{aligned}
v_{in} &= V_{in}+\tilde{v}_{in}\\
v_{c1} &= V_{c1}+\tilde{v}_{c1}\\
v_{c2} &= V_{c2}+\tilde{v}_{c2}\\
i_{L1} &= I_{L1}+\tilde{i}_{L1}\\
i_{L2} &= I_{L2}+\tilde{i}_{L2}\\
i_o &= I_o+\tilde{i}_o\\
d &= D+\tilde{d}
\end{aligned} \tag{2.4}$$

Substitute equation (2.4) into equation (2.3) yields to the perturbed expression of (2.5):

$$\begin{aligned}
L_1\frac{di_{L1}}{dt} &= (V_{in}+\tilde{v}_{in})(1-\tilde{d}-D)-V_{c2}-\tilde{v}_{c2}\\
L_1\frac{di_{L1}}{dt} &= (V_{c1}+\tilde{v}_{c1})(1-\tilde{d}-D)-(V_{c2}+\tilde{v}_{c2})(D+\tilde{d})-(V_{co}+\tilde{v}_{co})(1-\tilde{d}-D)\\
L_2\frac{di_{L2}}{dt} &= (V_{in}+\tilde{v}_{in})(1-\tilde{d}-D)-V_{c1}-\tilde{v}_{c1}\\
L_2\frac{di_{L2}}{dt} &= (V_{c2}+\tilde{v}_{c2})(1-\tilde{d}-D)-(V_{c1}+\tilde{v}_{c1})(D+\tilde{d})-(V_{co}+\tilde{v}_{co})(1-\tilde{d}-D)
\end{aligned} \tag{2.5}$$

$$
\begin{aligned}
C_1\frac{dv_{C1}}{dt} &= \left(I_{in}+\tilde{i}_{in}\right)\left(1-\tilde{d}-D\right)-\left(I_{L1}+\tilde{i}_{L1}\right)\left(1-\tilde{d}-D\right)+\left(I_{L2}+\tilde{i}_{L2}\right)\left(D+\tilde{d}\right)\\
C_2\frac{dv_{C2}}{dt} &= \left(I_{in}+\tilde{i}_{in}\right)\left(1-\tilde{d}-D\right)-\left(I_{L2}+\tilde{i}_{L2}\right)\left(1-\tilde{d}-D\right)+\left(I_{L1}+\tilde{i}_{L1}\right)\left(D+\tilde{d}\right)\\
C_o\frac{dv_{Co}}{dt} &= \left(I_{L1}+\tilde{i}_{L1}+I_{L2}+\tilde{i}_{L2}-I_{in}-\tilde{i}_{in}\right)\left(1-\tilde{d}-D\right)-I_o-\tilde{i}_o+\tilde{i}_{inj}
\end{aligned}
\tag{2.5}
$$

Separate the various parameters into DC components. The DC equations are given by equation (2.6):

$$
\begin{aligned}
0 &= V_{in}\left(1-D\right)-V_{c2}\\
0 &= V_{c1}\left(1-D\right)-V_{c2}D-V_{co}\left(1-D\right)\\
0 &= V_{in}\left(1-D\right)-V_{c1}\\
0 &= V_{c2}\left(1-D\right)-V_{c1}D-V_{co}\left(1-D\right)\\
0 &= I_{in}\left(1-D\right)-I_{L1}\left(1-D\right)+I_{L2}D\\
0 &= I_{in}\left(1-D\right)-I_{L2}\left(1-D\right)+I_{L1}D\\
0 &= \left(I_{L1}+I_{L2}-I_{in}\right)\left(1-D\right)-I_o
\end{aligned}
\tag{2.6}
$$

2.2. STEADY STATE ANALYSIS

By solving equation (2.6) expressions for the inductors DC current, the capacitors DC voltage, the peak DC voltage output of the three-phase full-bridge rectifier and the DC input current to the Z-source circuit are obtained in equation (2.7):

$$
\begin{aligned}
V_{c1} &= V_{c2} = \frac{\left(1-D\right)}{\left(1-2D\right)}V_{co}\\
V_{in} &= \frac{1}{\left(1-2D\right)}V_{co}\\
I_{L1,av} &= I_{L2,av} = I_{o,av}\\
I_{in,av} &= \frac{\left(1-2D\right)}{\left(1-D\right)}I_{o,av}
\end{aligned}
\tag{2.7}
$$

From the model in [6] [7] the inductors current are related to the load current by:

$$
I_{L1} = I_{L2} = \frac{I_o}{\left(1-2D\right)} \tag{2.8}
$$

However the model that was developed suggests that the inductor and load currents are equal in equation (2.7). In addition for the ZVS rectifier of [17] inductor and load current are related by equation (2.9) which is also different to equation (2.7):

$$I_{L1} = I_{L2} = (1-D)I_o \tag{2.9}$$

The Z-source circuit switch voltage during shoot-through is obtained from equation (2.2) and equation (2.7) as:

$$\begin{aligned} V_{sw} &= V_{c1} + V_{c2} - V_{co} = \frac{2(1-D)}{(1-2D)}V_{co} - V_{co} \\ &= \frac{1}{(1-2D)}V_{co} \end{aligned} \tag{2.10}$$

The overall DC gain of the rectifier is obtained by using the PWM full-bridge peak DC output voltage. The peak DC output voltage V_{in} of the full-bridge is given in [3] [4] [6] by:

$$V_{in} = \frac{2V_{sp}}{M\cos\theta} \tag{2.11}$$

With $\cos\theta = \arctan\frac{wL_S}{R_S}$ and V_{sp} the peak value of the line to neutral of the input AC source voltage, M is the modulation index, R_s the input resistance and L_s the input inductance [6].

From equation (2.7) $V_{co} = V_{in}(1-2D)$ and combining with equation (2.11), the output DC voltage is given by equation (2.12) [4] [4] [7] [14]:

$$\begin{aligned} V_{co} &= \frac{2V_{sp}(1-D)}{M\cos\theta} \\ &= \frac{2BV_{sp}}{\cos\theta} \end{aligned} \tag{2.12}$$

Where B is the DC gain of the rectifier or buck- boost factor given by equation (2.13) [3] [4] [7] [14]:

$$\begin{aligned} B &= \frac{1-2D}{M} \\ &= \frac{b}{M} \end{aligned} \tag{2.13}$$

Where $b = 1-2D$ (2.14)

For a given ripple value of the DC voltage and current, the component size can be found from equation (2.2) and are given by equation (2.15):

$$\begin{aligned} L_1 &= \frac{V_{c2} D}{F_{sw} \Delta i_{L1}} \\ L_2 &= \frac{V_{c1} D}{F_{sw} \Delta i_{L2}} \\ C_1 &= \frac{I_{L2} D}{F_{sw} \Delta v_{c1}} \\ C_2 &= \frac{I_{L1} D}{F_{sw} \Delta v_{c2}} \\ C_o &= \frac{I_o D}{F_{sw} \Delta v_{co}} \end{aligned} \tag{2.15}$$

With F_{sw} the Z-source circuit switching frequency. Because capacitors C_1 and C_2 DC voltages are equal and inductors L_1 and L_2 DC current are equal as shown by equation (2.7), capacitors C_1 and C_2, inductors L_1 and L_2 can be chosen to be equal. Hence this justifies using symmetrical components in the Z-source three-phase rectifier.

2.3. SMALL SIGNAL MODEL

The AC equations are obtained from equation (2.5) and given by equation (2.16):

$$\begin{aligned} L_1 \frac{di_{L1}}{dt} &= \tilde{v}_{in}(1-D) - V_{in}\tilde{d} - \tilde{v}_{c2} \\ L_1 \frac{di_{L1}}{dt} &= \tilde{v}_{c1}(1-D) - V_{c1}\tilde{d} - \tilde{v}_{c2}D - V_{c2}\tilde{d} + V_{co}\tilde{d} - \tilde{v}_{co}(1-D) \\ L_2 \frac{di_{L2}}{dt} &= \tilde{v}_{in}(1-D) - V_{in}\tilde{d} - \tilde{v}_{c1} \\ L_2 \frac{di_{L2}}{dt} &= \tilde{v}_{c2}(1-D) - V_{c2}\tilde{d} - \tilde{v}_{c1}D - V_{c1}\tilde{d} + V_{co}\tilde{d} - \tilde{v}_{co}(1-D) \\ C_1 \frac{dv_{C1}}{dt} &= \tilde{i}_{in}(1-D) - I_{in}\tilde{d} + I_{L1}\tilde{d} - \tilde{i}_{L1}(1-D) + I_{L2}\tilde{d} + \tilde{i}_{L2}D \\ C_2 \frac{dv_{C2}}{dt} &= \tilde{i}_{in}(1-D) - I_{in}\tilde{d} + I_{L2}\tilde{d} - \tilde{i}_{L2}(1-D) + I_{L1}\tilde{d} + \tilde{i}_{L1}D \\ C_o \frac{dv_{Co}}{dt} &= (\tilde{i}_{L1} + \tilde{i}_{L2} - \tilde{i}_{in})(1-D) - (I_{L1} + I_{L2} - I_{in})\tilde{d} - \tilde{i}_o + \tilde{i}_{inj} \end{aligned} \tag{2.16}$$

Making use of symmetrical components and transforming in Laplace form equation (2.16), the simplified AC expression is:

$$\begin{aligned}
sL\tilde{i}_L(s) &= \tilde{v}_{in}(s)(1-D) - V_{in}\tilde{d}(s) - \tilde{v}_c(s) \\
sL\tilde{i}_L(s) &= \tilde{v}_c(s)(1-2D) - 2V_C\tilde{d}(s) + V_{co}\tilde{d}(s) - \tilde{v}_{co}(s)(1-D) \\
sC\tilde{v}_c(s) &= \tilde{i}_{in}(s)(1-D) + (2I_L - I_{in})\tilde{d}(s) - \tilde{i}_L(s)(1-2D) \\
sC_o\tilde{v}_{co}(s) &= 2\tilde{i}_L(s)(1-D) - \tilde{i}_{in}(s)(1-D) - (2I_L - I_{in})\tilde{d}(s) - \frac{\tilde{v}_{co}(s)}{R} + \tilde{i}_{inj}(s)
\end{aligned} \tag{2.17}$$

From equation (2.17), the inductor current can be expressed by:

$$i_L(s) = \frac{v_{in}(s)(1-D) - V_{in}d(s) - v_c(s)}{sL} \tag{2.18a}$$

$$i_L(s) = \frac{v_c(s)(1-2D) - 2V_C d(s) + V_{co}d(s) - v_{co}(s)(1-D)}{sL} \tag{2.18b}$$

Eliminate the inductor current from the capacitors equations in (2.17) by substituting equation (2.18a) as follow:

$$\begin{aligned}
sC_o v_{co}(s) &= \frac{v_{in}(s)(1-D) - V_{in}d(s) - v_c(s)}{sL}2(1-D) - (1-D)i_{in}(s) \\
&\quad - (2I_L - I_{in})d(s) - \frac{v_{co}(s)}{R} + i_{inj}(s) \\
\left[s^2RLC_o + sL\right]v_{co}(s) &= v_{in}(s)2R(1-D)^2 - 2R(1-D)v_c(s) - sRL(1-D)i_{in}(s) \\
&\quad - \left[2(1-D)V_{in} + sL(2I_L - I_{in})\right]Rd(s) + sLRi_{inj}(s) \\
sCv_c(s) &= i_{in}(s)(1-D) + (2I_L - I_{in})d(s) - (1-2D)\frac{v_{in}(s)(1-D) - V_{in}d(s) - v_c(s)}{sL} \\
\left[s^2LC - (1-2D)\right]v_c(s) &= sL(1-D)i_{in}(s) - (1-2D)(1-D)v_{in}(s) \\
&\quad + \left[(2I_L - I_{in})sL + (1-2D)V_{in}\right]d(s)
\end{aligned} \tag{2.19a}$$

Eliminate the inductor current from the capacitors equations in (2.17) by substituting equation (2.18b) as follow:

$$\begin{aligned}
s^2LC_o v_{co}(s) &= 2(1-D)(1-2D)v_c(s) + 2(1-D)(V_{co} - 2V_C)d(s) - 2(1-D)^2 v_{co}(s) \\
&\quad - sL(1-D)i_{in}(s) - sL(2I_L - I_{in})d(s) - \frac{sLv_{co}(s)}{R} + sLi_{inj}(s) \\
\left[s^2RLC_o + sL + 2R(1-D)^2\right]v_{co}(s) &= 2R(1-D)(1-2D)v_c(s) - sRL(1-D)i_{in}(s) \\
&\quad + \left[2(1-D)(V_{co} - 2V_C) - sL(2I_L - I_{in})\right]Rd(s) + sLRi_{inj}(s)
\end{aligned} \tag{2.19b}$$

$$\begin{aligned} sCv_c(s) &= i_{in}(s)(1-D)+(2I_L-I_{in})d(s) \\ &\quad -(1-2D)\frac{[v_c(s)(1-2D)-2V_C d(s)+V_{co}d(s)-v_{co}(s)(1-D)]}{sL} \\ [s^2LC+(1-2D)^2]v_c(s) &= sL(1-D)i_{in}(s)+(1-2D)(1-D)v_{co}(s)+ \\ &\quad [(2I_L-I_{in})sL-(1-2D)(V_{co}-2V_c)]d(s) \end{aligned} \tag{2.19b}$$

From equation (2.19a) simplifying expressions are defined in equation (2.20a):

$$\begin{aligned} I_T &= 2I_L - I_{in} \\ D' &= 1-D \\ q_{ca} &= s^2LC-(1-2D) \\ q_{coa} &= s^2RLC_o+sL \end{aligned} \tag{2.20a}$$

From equation (2.19b) simplifying expressions are defined in equation (2.20b):

$$\begin{aligned} I_T &= 2I_L - I_{in} \\ V_T &= V_{co}-2V_c \\ D' &= 1-D \\ D'-D &= 1-2D \\ q_c &= s^2LC+(D'-D)^2 \\ q_{co} &= s^2RLC_o+sL+2R(1-D)^2 \end{aligned} \tag{2.20b}$$

A reduced equation (2.19a) is obtained after including the parameters from equation (2.20a):

$$\begin{aligned} q_{coa}v_{co}(s) &= 2RD'^2v_{in}(s)-2RD'v_c(s)-sRLD'i_{in}(s)-[2D'V_{in}+sLI_T]Rd(s)+sLRi_{inj}(s) \\ q_{ca}v_c(s) &= sLD'i_{in}(s)-(1-2D)D'v_{in}(s)+[I_TsL+(1-2D)V_{in}]d(s) \end{aligned} \tag{2.21a}$$

A reduced equation (2.19b) is obtained after including the parameters from equation (2.20b):

$$\begin{aligned} q_{co}v_{co}(s) &= 2RD'(D'-D)v_c(s)-sRLD'i_{in}(s)+[2D'V_T-sLI_T]Rd(s)+sLRi_{inj}(s) \\ q_cv_c(s) &= sLD'i_{in}(s)+D'(D'-D)v_{co}(s)+[sLI_T-(D'-D)V_T]d(s) \end{aligned} \tag{2.21b}$$

From equation (2.21a), substitute capacitor C voltage equation into capacitor C_o voltage equation to obtain the output capacitor voltage dynamic equations given by equation (2.22a):

$$\begin{aligned} q_{coa}q_{ca}v_{co}(s) &= 2RD'^2q_{ca}v_{in}(s)-2RLD'^2si_{in}(s)+2RD'^2(1-2D)v_{in}(s)-sq_{ca}RLD'i_{in}(s) \\ &\quad -2RD'[sLI_T+(1-2D)V_{in}]d(s)-q_{ca}[2D'V_{in}+sLI_T]Rd(s)+sq_{ca}LRi_{inj}(s) \\ [q_{coa}q_{ca}]v_{co}(s) &= [2RD'^2q_{ca}+2RD'^2(1-2D)]v_{in}(s)-[2RLD'^2s+sq_{ca}RLD']i_{in}(s) \\ &\quad -\{2RD'[sLI_T+(1-2D)V_{in}]+q_{ca}[2D'V_{in}+sLI_T]R\}d(s)+sq_{ca}LRi_{inj}(s) \end{aligned} \tag{2.22a}$$

From equation (2.21b), substitute capacitor C voltage equation into capacitor C_o voltage equation to obtain the output capacitor voltage dynamic equations given by equation (2.22b):

$$\begin{aligned}
&q_{co}q_c v_{co}(s) = 2RLD'^2(D'-D)si_{in}(s) + 2RD'^2(D'-D)^2 v_{co}(s) - sq_c RLD' i_{in}(s) \\
&\quad + 2RD'(D'-D)\left[sLI_T - (D'-D)V_T\right]d(s) + q_c R(2D'V_T - sLI_T)d(s) + sq_c LRi_{inj}(s) \\
&\left[q_{co}q_c - 2RD'^2(D'-D)^2\right]v_{co}(s) = \left[2RLD'^2(D'-D)s - sq_c RLD'\right]i_{in}(s) + \\
&\quad + \left\{2RD'(D'-D)\left[sLI_T - (D'-D)V_T\right] + q_c R(2D'V_T - sLI_T)\right\}d(s) + sq_c LRi_{inj}(s)
\end{aligned} \tag{2.22b}$$

Where

$$\begin{aligned}
Q_{co} &= q_{co}q_c - 2RD'^2(D'-D)^2 \\
&= L^2 C_o CRs^4 + L^2 Cs^3 + \left[RLC_o(D'-D)^2 + 2RLCD'^2\right]s^2 + L(D'-D)^2 s
\end{aligned}$$

From equation (2.21b), substitute capacitor C_o voltage equation in capacitor C voltage equation to obtain capacitor C voltage dynamic equations:

$$\begin{aligned}
&q_{co}q_c v_c(s) = sq_{co}LD' i_{in}(s) + 2RD'^2(D'-D)^2 v_c(s) - sRLD'^2(D'-D)i_{in}(s) \\
&\qquad + RD'(D'-D)(2D'V_T - sLI_T)d(s) + q_{co}\left[sLI_T - (D'-D)V_T\right]d(s) \\
&\left[q_{co}q_c - 2RD'^2(D'-D)^2\right]v_c(s) = \left[sq_{co}LD' - sRLD'^2(D'-D)\right]i_{in}(s) + \\
&\qquad + \left\{RD'(D'-D)(2D'V_T - sLI_T) + q_{co}\left[sLI_T - (D'-D)V_T\right]\right\}d(s)
\end{aligned} \tag{2.23}$$

Where

$$Q_c = q_{co}q_c - 2RD'^2(D'-D)^2 = Q_{co}$$

The transfer function relating the inductors current to the shoot-through duty ratio, and the transfer function relating the inductors current to the input current can also be obtained using the method of substitution. From equation (2.17), the capacitors' voltages equations are reduced using equation (2.20b) and can be written as:

$$\begin{aligned}
\tilde{v}_c(s) &= \frac{\tilde{i}_{in}(s)D' + I_T\tilde{d}(s) - \tilde{i}_L(s)(D'-D)}{sC} \\
\tilde{v}_{co}(s) &= \frac{2R\tilde{i}_L(s)D' - \tilde{i}_{in}(s)RD' - I_T R\tilde{d}(s)}{sRC_o + 1}
\end{aligned} \tag{2.24}$$

Substitute the capacitors' voltages from equation (2.24) into the inductors' current equations of (2.17):

$$\begin{aligned}
s^2 LC(sRC_o + 1)i_L(s) &= (sRC_o + 1)(D'-D)D' i_{in}(s) + (sRC_o + 1)(D'-D)I_T d(s) \\
&\quad - (sRC_o + 1)(D'-D)^2 i_L(s) - 2RCD'^2 si_L(s) \\
&\quad + RCD' I_T sd(s) + RCD'^2 si_{in}(s) + (sRC_o + 1)sCV_T d(s)
\end{aligned} \tag{2.25}$$

$$\begin{aligned}\left[s^2LC(sRC_o+1)+(sRC_o+1)(D'-D)^2+2RCD'^2\right]\tilde{i}_L(s)=&\\ \left[(sRC_o+1)(D'-D)D'+RCD'^2\right]\tilde{i}_{in}(s)&\\ +\left[(sRC_o+1)(D'-D)I_T+RCD'I_Ts+(sRC_o+1)sCV_T\right]\tilde{d}(s)&\end{aligned} \tag{2.25}$$

Where

$$\begin{aligned}Q_{iL}&=s^2LC(sRC_o+1)+(sRC_o+1)(D'-D)^2+2RCD'^2\\ &=RLC_oCs^4+LCs^2+\left[RC_o(D'-D)^2+2RCD'^2\right]s+(D'-D)^2\end{aligned}$$

The transfer functions derived are re-written from (2.22), (2.23) and (2.25) as follow:

From equation (2.22b) the transfer function relating the output voltage to control is obtained as:

$$\begin{aligned}G_{vd}&=\frac{\tilde{v}_{co}(s)}{\tilde{d}(s)}\Big|_{\tilde{in}(s)=0}\\ &=\frac{LRI_T(D'-D)+2LCRD'V_Ts-L^2CRI_Ts^2}{L(D'-D)^2+\left[2LCRD'^2+RLC_o(D'-D)^2\right]s+L^2Cs^2+L^2C_oCRs^3}\end{aligned} \tag{2.26a}$$

From equation (2.22b) the transfer function relating the output voltage ripple to the Z-source circuit input current ripple (current susceptibility) is given by:

$$\begin{aligned}G_{vg}&=\frac{\tilde{v}_{co}(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0}\\ &=\frac{\left[2RLD'^2(D'-D)-RLD'(D'-D)^2\right]-L^2CRD's^2}{L(D'-D)^2+\left[2LCRD'^2+RLC_o(D'-D)^2\right]s+L^2Cs^2+L^2C_oCRs^3}\end{aligned} \tag{2.26b}$$

From equation (2.22b) the transfer function relating the output voltage ripple to the injected current ripple (output impedance) is given by:

$$\begin{aligned}Z_{out}(s)&=-\frac{\tilde{v}_{co}(s)}{\tilde{i}_{inj}(s)}\Big|_{\tilde{d}(s)=0}\\ &=\frac{-RL^2Cs^2-RL(D'-D)^2}{L(D'-D)^2+\left[2LCRD'^2+RLC_o(D'-D)^2\right]s+L^2Cs^2+L^2C_oCRs^3}\end{aligned} \tag{2.26c}$$

From equation (2.22a) the transfer function relating the input current ripple to the input voltage ripple of the Z-source circuit (input admittance) with the output short circuited is given by:

$$\begin{aligned} Y_{in}(s) &= \frac{\tilde{i}_{in}(s)}{\tilde{v}_{in}(s)}\Big|_{\tilde{v}_{out}(s)=0} \\ &= \frac{\left[2RD'^2 q_{ca} + 2RD'^2(1-2D)\right]}{\left[2RLD'^2 s + sq_{ca}RLD'\right]} \end{aligned} \tag{2.26d}$$

From equation (2.23) the transfer function relating the Z-source circuit capacitor voltage to control is given by:

$$\begin{aligned} G_{vd} &= \frac{\tilde{v}_c(s)}{\tilde{d}(s)}\Big|_{\tilde{i}n(s)=0} \\ &= \frac{\left[2RLD'^2 I_T - RLI_T D'(D'-D) - LV_T(D'-D)\right] + \left[L^2 I_T - RLC_O V_T(D'-D)\right]s + RL^2 C_O I_T s^2}{L(D'-D)^2 + \left[2LCRD'^2 + RLC_O(D'-D)^2\right]s + L^2Cs^2 + L^2C_OCRs^3} \end{aligned} \tag{2.27a}$$

From equation (2.23) the transfer function relating the Z-source capacitor voltage to Z-source circuit input current is given by:

$$\begin{aligned} G_{vg} &= \frac{\tilde{v}_c(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0} \\ &= \frac{\left[2RLD'^3 - RLD'^2(D'-D)\right] + L^2D's + RL^2C_oD's^2}{L(D'-D)^2 + \left[2LCRD'^2 + RLC_o(D'-D)^2\right]s + L^2Cs^2 + L^2C_oCRs^3} \end{aligned} \tag{2.27b}$$

From equation (2.25) the transfer function relating the Z-source inductor current to control is given by:

$$\begin{aligned} G_{id} &= \frac{\tilde{i}_L(s)}{\tilde{d}(s)}\Big|_{i\tilde{n}(s)=0} \\ &= \frac{(D'-D)I_T + \left[I_T RC_o(D'-D) + RCI_T D' + CV_T\right]s + RC_oCV_T s^2}{(D'-D)^2 + \left[2CRD'^2 + RC_o(D'-D)^2\right]s + LCs^2 + LC_oCRs^3} \end{aligned} \tag{2.28a}$$

From equation (2.22b) the transfer function relating the Z-source inductor current to Z-source circuit input current is given by:

$$\begin{aligned} G_{ig} &= \frac{\tilde{i}_L(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0} \\ &= \frac{(D'-D)D' + \left[C_oR(D'-D)D' + CD'R\right]s}{(D'-D)^2 + \left[2CRD'^2 + RC_o(D'-D)^2\right]s + LCs^2 + LC_oCRs^3} \end{aligned} \tag{2.28b}$$

To complete the ZSR modelling, the Z-source circuit DC side dynamic equations are combined with the dynamic model of the three-phase full-bridge PWM rectifier AC side as follows:

The synchronous frame model of the three-phase full-bridge PWM rectifier is given by [6]:

$$\begin{aligned} L_s \frac{di_{Lsd}}{dt} &= v_{sd} - Ri_d - wL_s i_q - d_d v_{in} \\ L_s \frac{di_{Lsq}}{dt} &= v_{sq} - Ri_q + wL_s i_d - d_q v_{in} \end{aligned} \tag{2.29}$$

The input DC voltage to the Z-source circuit is given by equation (2.7) as:

$$V_{in} = \frac{V_{co}}{(1-2d)}$$

By substituting the input DC voltage to the Z-source circuit into equation (2.29), the synchronous frame equations become:

$$\begin{aligned} L_s \frac{di_{Lsd}}{dt} &= V_{sd} - Ri_d - wL_s i_q - d_d \frac{v_{co}}{(1-2d)} \\ L_s \frac{di_{Lsq}}{dt} &= V_{sq} - Ri_q + wL_s i_d - d_q \frac{v_{co}}{(1-2d)} \end{aligned} \tag{2.30}$$

The variations of the output voltage depend on the respective variations of the AC input current of the rectifier and the shoot-through duty ratio. The synchronous frame model of the three-phase full-bridge PWM rectifier and the dynamic equations of the Z-circuit are then combined to yield the block diagram of the model that was proposed. It is shown in Figure 2.4 and expressed by equation (2.31c).

$$\begin{aligned} &G_3(s)v_{co}(s) = G_2(s)d(s) + G_1(s)i_{in}(s) \\ &where \quad i_{in}(s) = (1-d)i_s \end{aligned} \tag{2.31a}$$

From the axes transformations the input AC current of the three-phase full bridge rectifier is given by:

$$i_s = \frac{3}{2}\left(d_q i_q + d_d i_d\right) \tag{2.31b}$$

By substituting equation (2.31b) into equation (2.32a), the mathematical equation of the block diagram is expressed as:

$$G_3(s)v_{co}(s) = G_2(s)d(s) + \frac{3}{2}G_1(s)(1-d)\left(d_q i_q + d_d i_d\right) \tag{2.31c}$$

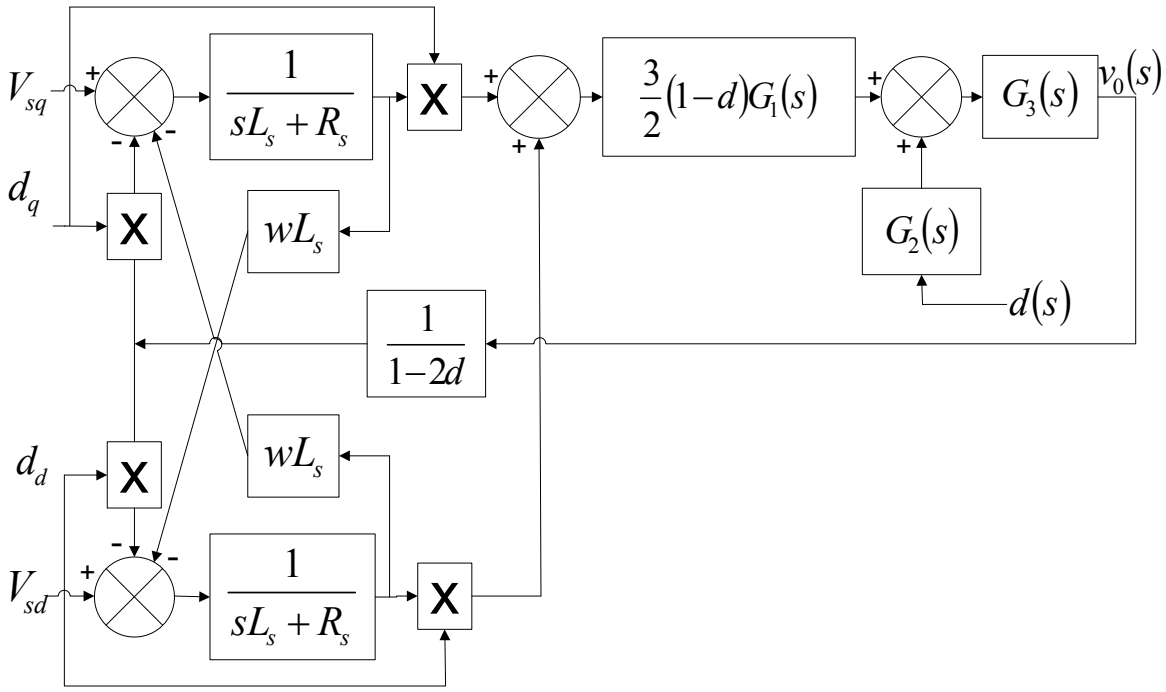

Figure 2.4. Block diagram of the model

With:

$$G_1(s)=\left[2RLD'^2(D'-D)-RLD'(D'-D)^2\right]-L^2CRD's^2 \tag{2.32}$$

$$G_2(s)=LRI_T(D-D')^2+2LCRDV_Ts-L^2CRI_Ts^2 \tag{2.33}$$

$$G_3(s)=L(D'-D)^2+\left[2LCRD'^2+RLC_o(D'-D)^2\right]s+L^2Cs^2+L^2C_oCRs^3 \tag{2.34}$$

Where V_T, I_T, D', $(D'-D)$ are expressed in equation (2.20)

The block diagram representation of the ZSR in Figure 2.4 can be used to design a closed-loop controller to regulate the output DC voltage and to obtain a low harmonic AC input current in phase with the AC voltage.

2.3.1 Dynamic model analysis

Bode plots of the transfer functions that were derived are obtained using Matlab software. The converter parameters used for the plots are given in Table 2.1. These parameters were chosen from many considerations such as satisfactory ripple performance and small physical size, proper quality factor and damping factor, resonant frequency far away from the Z-source circuit switching frequency for stability. The ripple performance is set to a maximum

of 0.2 % of the steady state capacitor voltage and a maximum of 8 % of the steady state inductor current.

Table 2.1. Converter Parameters

Parameters	**Value**
Input Voltage, Vs (line-to-line)	100 V
Input Resistance R_s	1.5 Ω
Input Inductance L_s	1400 μH
Output Voltage, Vo	150 V
Load Resistance, Ro	21.5 Ω
Z-circuit output capacitor C_o	26.6 μF
Z-circuit capacitor C_1 and C_2	17.2 μF
Z-circuit Inductor L	900 μH
Switching Frequency, f_s	40 kHz

Four significant transfer functions are required to analyse the dynamic performance of the Z-source circuit. The first significant transfer function is the one relating the output voltage to control. Regulation of the DC output voltage of the Z-source circuit depends on the response of the transfer function relating the output voltage to control [2] [13] [39]. In such transfer function, a flat and high gain is desirable in low frequencies to limit the controller gain to low values [2] [13] [40]. A high decade rate is desirable at high frequencies to prevent noises reaching the output [2] [13] [40]. The DC gain at low frequency is given by the steady state equation of the converter. Resonance on the response causing abrupt amplitude and phase change is undesirable, as this may stress the components beyond their voltage limits [2] [13]. Substituting the rectifier parameters from Table 2.1 into the transfer function relating the output voltage to control of equation (2.26a), the transfer function in equation (2.35) is obtained and used to draw the bode plot shown in Figure 2.5.

$$G_{vd} = \frac{\tilde{v}_{co}(s)}{\tilde{d}(s)}\Big|_{\tilde{m}(s)=0} = \frac{-2.337\times10^{-9}s^2 - 1.133\times10^{-4}s + 0.119}{7.958\times10^{-15}s^3 + 1.393\times10^{-11}s^2 + 8.517\times10^{-7}s + 5.59\times10^{-4}} \tag{2.35}$$

The pole-zero map of the transfer function in equation (2.35) is shown in Figure 2.6 where the presence of a Right Half Plane (RHP) zero is depicted at a frequency of 164 Hz and a dominant pole on the real axis at a frequency of 105 Hz. The slope of the magnitude plot remains flat below 1 kHz as the pole and zero magnitudes contribution cancel each other but the phase plot rolls down from 360 degree to 180 degree due this pole and zero. The contribution of the complex pair of poles at 1.64 kHz causes resonances on the magnitude plot and a phase rolls down of 180 degree [41]. The resulting magnitude slope introduced by the poles is -40 dB/decade. The presence of this complex pole so close to the imaginary results in oscillations observed in the transient response shown in Figure 2.7. The second zero located at 7.88 kHz introduces 20 dB/decade on the magnitude plot such that the high frequency magnitude slope is 20 dB/decade [41]. The zero also introduces 90 degree such that the high frequency phase is at 90 degree [41].

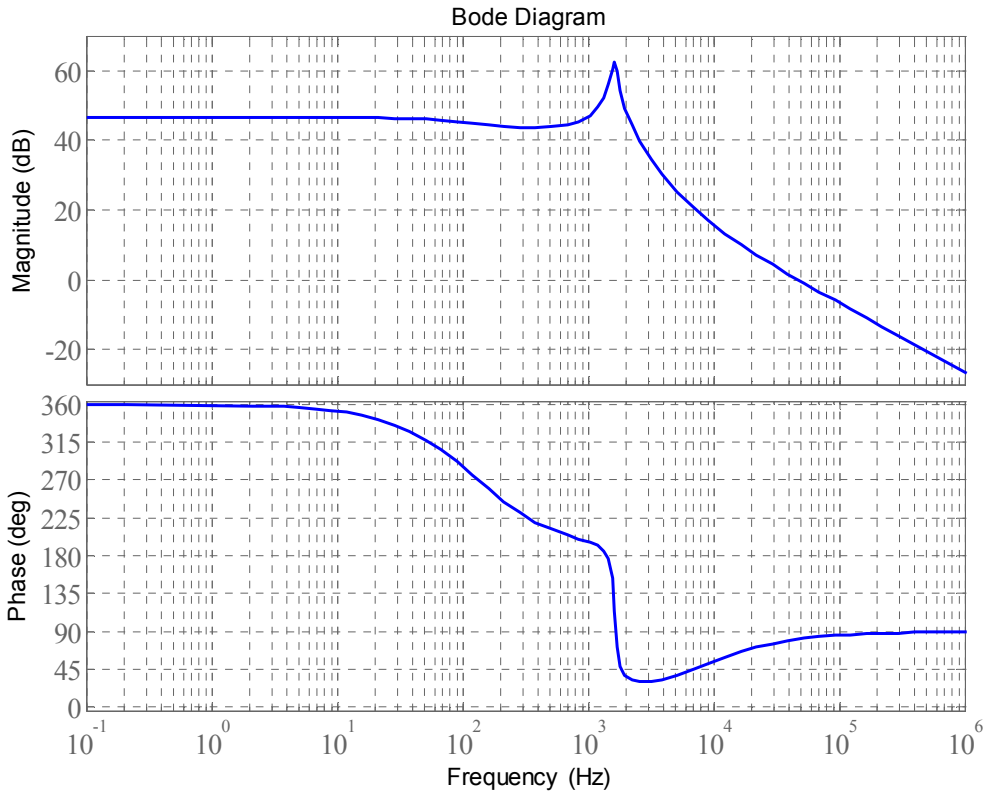

Figure 2.5. Bode plot of the transfer function relating the output voltage to control

From the bode plot response of Figure 2.5, a relatively flat response is observed in the low frequency region up to 100 Hz with a high gain of 46 dB and phase of 0 degree. The high

frequency decade rate is only at -20 dB/decade with a large negative phase caused by the zeros and poles of the transfer function. A higher decade rate and more positive phase would have been better in order to achieve better noise suppression and maintain higher stability. The presence of the RHP zero tends to destabilize the wide-bandwidth feedback loop, causes the inverse response observed in Figure 2.7, and imposes a maximum control bandwidth to the frequency of the RHP zero [41][42] [43] [44]. The presence of the RHP found in the model that was derived matches the findings of the model derived in [6], [14]. Multiple-loop inner-current-control-based scheme can be considered to design fast inner current loop not limited by the RHP zero location [44] and achieve an overall satisfactory faster response.

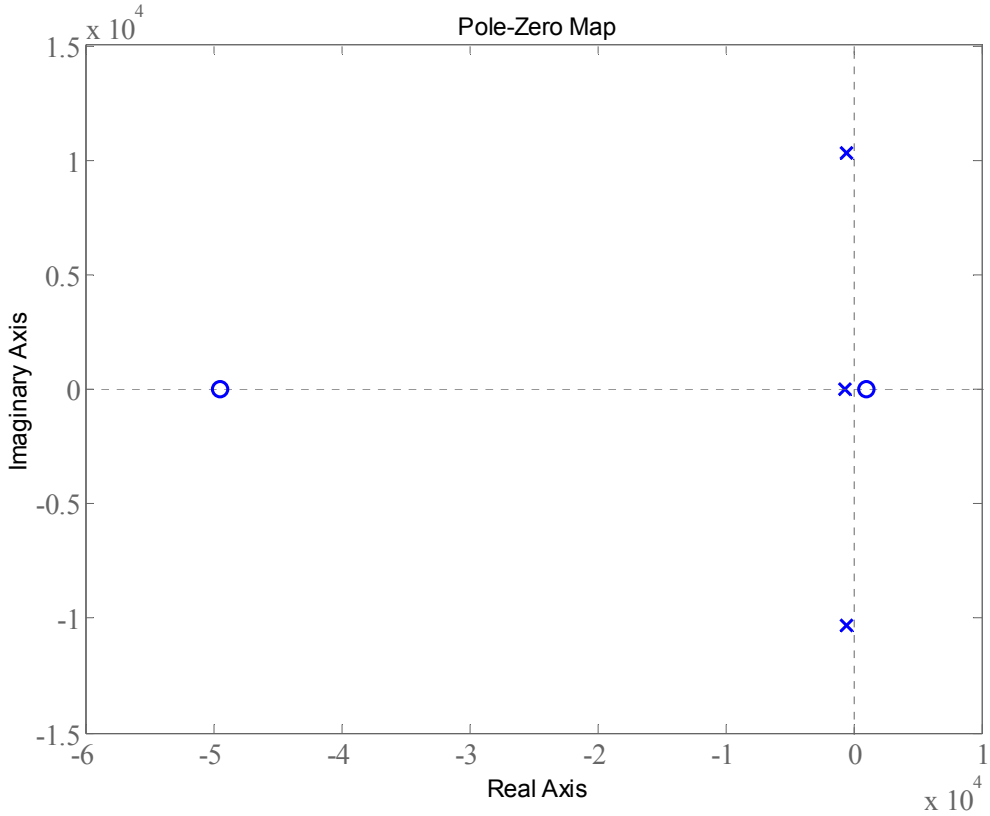

Figure 2.6. Pole-zero map of the transfer function relating the output voltage to control.

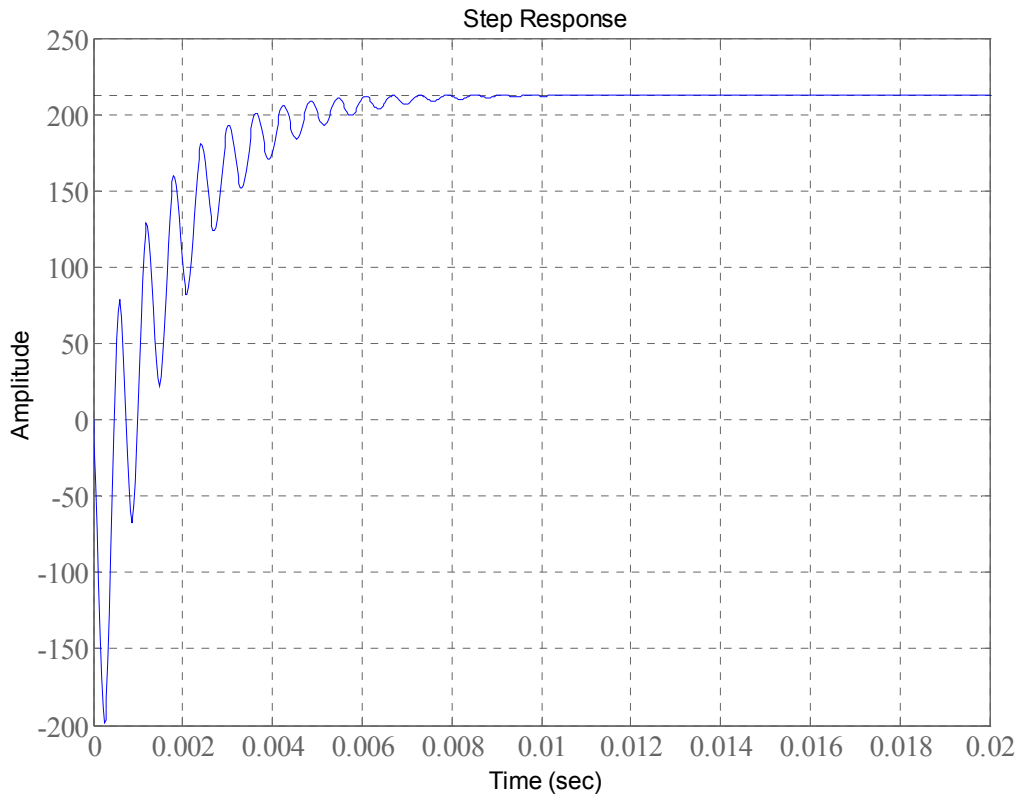

Figure 2.7. Step response of the transfer function relating the output voltage to control.

The next significant transfer function for the dynamic analysis of the Z-source circuit is the transfer function relating the output voltage ripple to the Z-source circuit input current ripple (current susceptibility). This transfer function describes how variations or disturbances in input current affect the output voltage [13]. Ideally, the bode plot response of this transfer function should have a very low magnitude and a high decade rate in the high frequency region where harmonics are expected [13] [40]. This is desired because the disturbances from input current harmonics should not lead to disturbances in the output voltage. The transfer function relating the output voltage ripple to the Z-source circuit input current ripple is given in equation (2.36) after substituting the converter parameters of Table 2.1 in equation (2.26b). The bode plot and the pole-zero map are shown in Figures 2.8 and 2.9 respectively.

$$G_{vg} = \frac{\tilde{v}_{co}(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0} = \frac{-2.678\times10^{-10}s^2 + 13.63\times10^{-3}}{7.958\times10^{-15}s^3 + 1.393\times10^{-11}s^2 + 8.517\times10^{-7}s + 5.59\times10^{-4}} \quad (2.36)$$

From the bode plot response of Figure 2.8, a relatively flat response is observed in the low frequency region up to 100 Hz with a high gain of 27 dB and phase of 0 degree. As the frequency is increased from 6 kHz, the magnitude is below 0 dB and a decade rate of -20 dB per decade is produced by the converter. Given the high switching frequency of 40 kHz of the Z-source circuit and the expected current ripple at higher frequency, the converter response from the bode plot is satisfactory in attenuating input current ripple and achieving low input current ripple transmission. It is also observed from the bode plot that the converter exhibits resonance at an input current with frequency of 1.64 kHz. However this resonant frequency is much lower than the expected current ripple frequency of the converter.

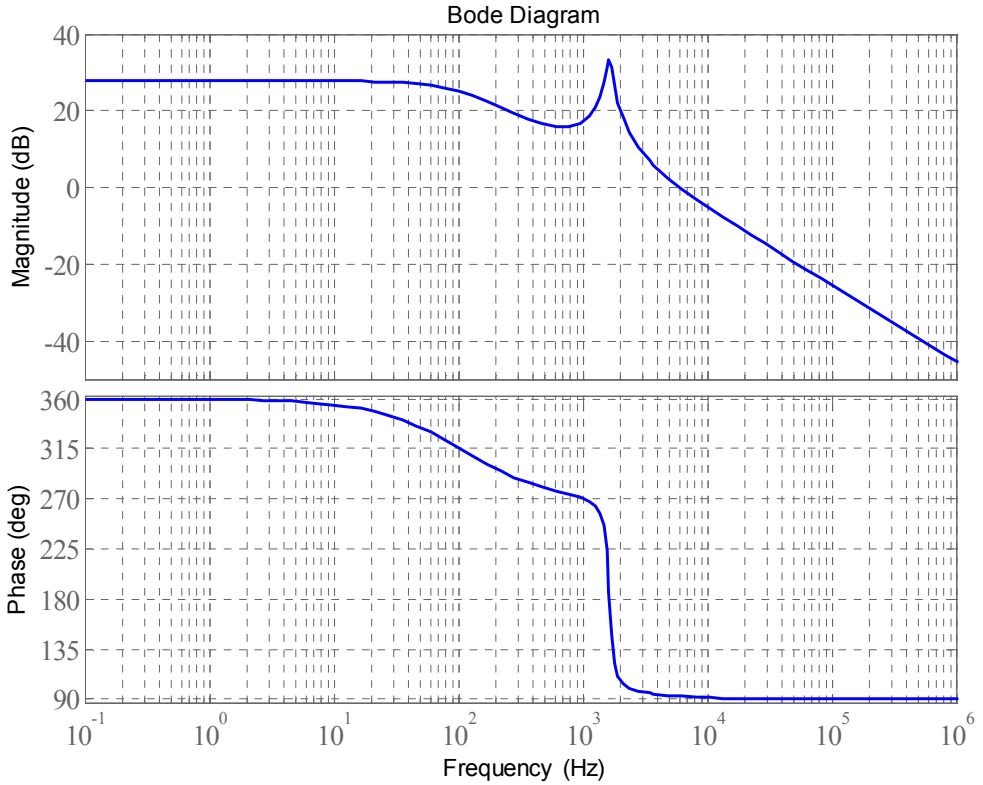

Figure 2.8. Bode plot of the transfer function relating the output voltage ripple to the Z-source circuit input current ripple

The pole-zero map of Figure 2.9 shows the presence of two real zeros at the same frequency of 1.14 kHz. However one zero is RHP and therefore the phase contribution of both zeros at that frequency is zero as they cancel each other. The phase plot is therefore dependant on the poles. For the three poles of the transfer function, the phase then rolls down by 270 degree with the abrupt phase drop at 1.64 kHz caused by the pair of poles close to the imaginary axis. The magnitude plot is flat until the first pole corner frequency of 105 Hz where the slope changes to -20 dB/decade. After resonance at 1.64 kHz the slope of the magnitude remain at -20 dB/decade as a result of the cancellation of the slope contributions of the poles at 1.64 kHz, and the zeros at 1.14 kHz. The non-minimum response featuring RHP zeros also affects to a very low scale the output voltage performance of the Z-source circuit during input current variations. However this inverse response effect is negligible because the RHP zero is located far away from the origin.

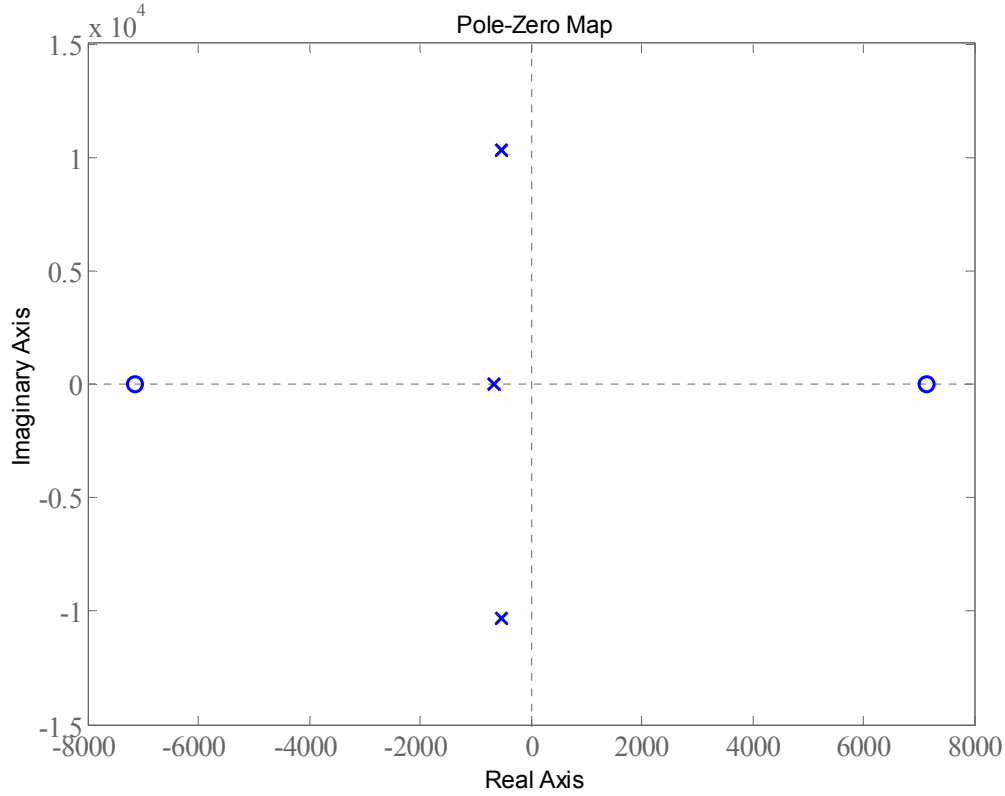

Figure 2.9. Pole-zero map of the transfer function relating the output voltage ripple to the Z-source circuit input current ripple

The additional significant dynamic analysis parameters are the output and input performance. The output performance of the Z-source circuit can be analysed using the output impedance transfer function of equation 2.26c. The output impedance describes how variations of the load current affect the output voltage [13]. Therefore low output impedance is ideally desired to limit variations in output voltage due to output current changes [13]. Using the converter parameters of Table 1 in equation (2.26c), the output impedance frequency is response is shown in Figure 2.10 from the expression given by:

$$Z_{out}(s) = -\frac{\tilde{v}_{co}(s)}{\tilde{i}_{inj}(s)}\Big|_{\tilde{d}(s)=0} = \frac{-2.995\times10^{-10}s^2 - 0.01202}{7.958\times10^{-15}s^3 + 1.393\times10^{-11}s^2 + 8.517\times10^{-7}s + 5.59\times10^{-4}} \tag{2.37}$$

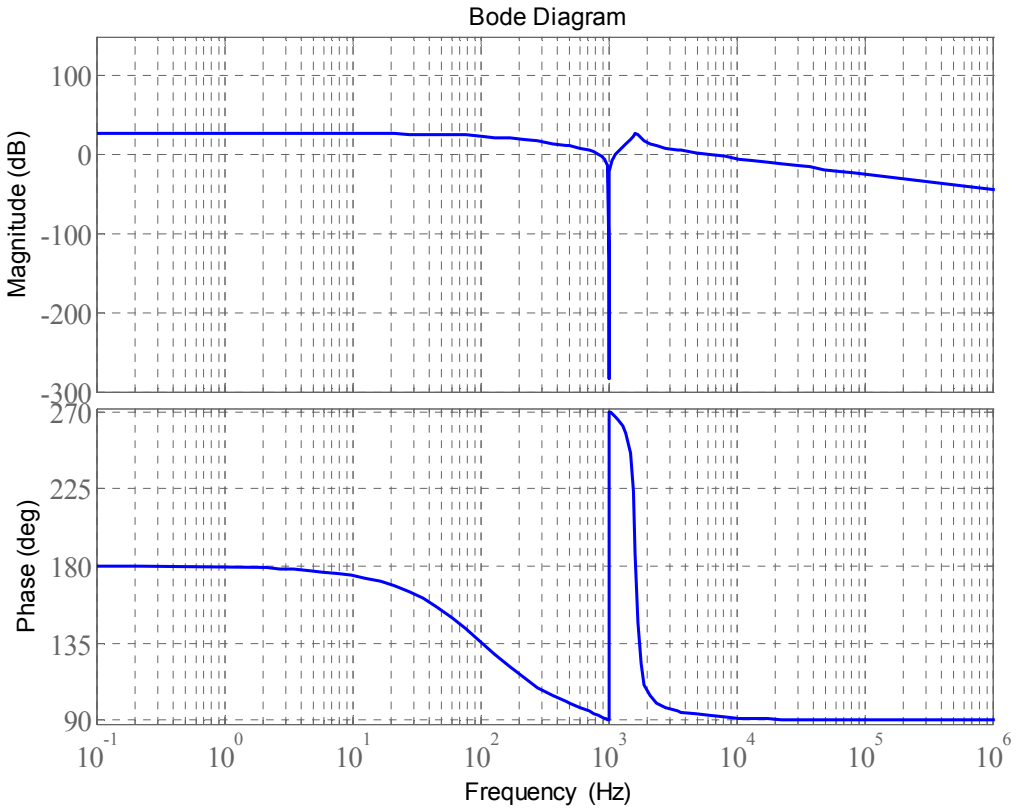

Figure 2.10. Bode plot of the transfer function of the output impedance of the Z-source circuit

Bode plot of the output impedance in Figure 2.10 shows a flat response in the low frequencies region below 100 Hz, and very low output impedance magnitude below 0 dB in the high frequency region of the plot from 6.2 kHz. The output impedance rolls down at -20 dB/decade in the high frequency region. The output performance of the converter is satisfactory given that it behaves as an effective first order filter to high frequency output current ripple. As a result of the low output impedance the output voltage is appreciably well regulated and constant in the presence of high frequency output current variations. An abrupt drop in impedance magnitude is observed at 1.02 kHz which translates to the converter shorting any current injected at that frequency.

The input performance of the Z-source circuit is analysed using the transfer function of the input admittance in equation (2.26d). The input admittance indicates the performance of the converter for connection to external systems such as EMI input filter [13] or a voltage source. For instance, the relative magnitude of the input admittance and the EMI filter output impedance influence if the EMI filter disrupts the transfer function G_{vd} [13]. Ideally a very low input admittance is desired to ensure that the converter has minimal influence and requirements on the performance of the source connected [40]. Such ideal input admittance translates to low harmonic current generated by the converter. Using the converter parameters of Table 1 in equation (2.26d), the input admittance is given by:

$$\begin{aligned} Y_{in}(s) &= \frac{\tilde{i}_{in}(s)}{\tilde{v}_{in}(s)}\Big|_{\tilde{v}_{out}(s)=0} \\ &= \frac{5.321\times10^{-7}s^2}{2.678\times10^{-10}s^3+0.0173s} \end{aligned} \tag{2.38}$$

The input performance of the Z-source circuit is satisfactory based on the bode plot in Figure 2.11. A low input admittance magnitude throughout the low frequencies and rolling at 20dB/decade is observed from the bode plot. This preserves the Z-source circuit from generating high frequency harmonic current at the supply. The source requirement in terms of current capability is reduced as a result of the low input admittance. Resonance is observed in the admittance bode plot at a frequency of 1.28 kHz and is similar to what is found in the admittance response of buck-boost and boost DC-DC converter [45]. This is the result of poles on the imaginary axis.

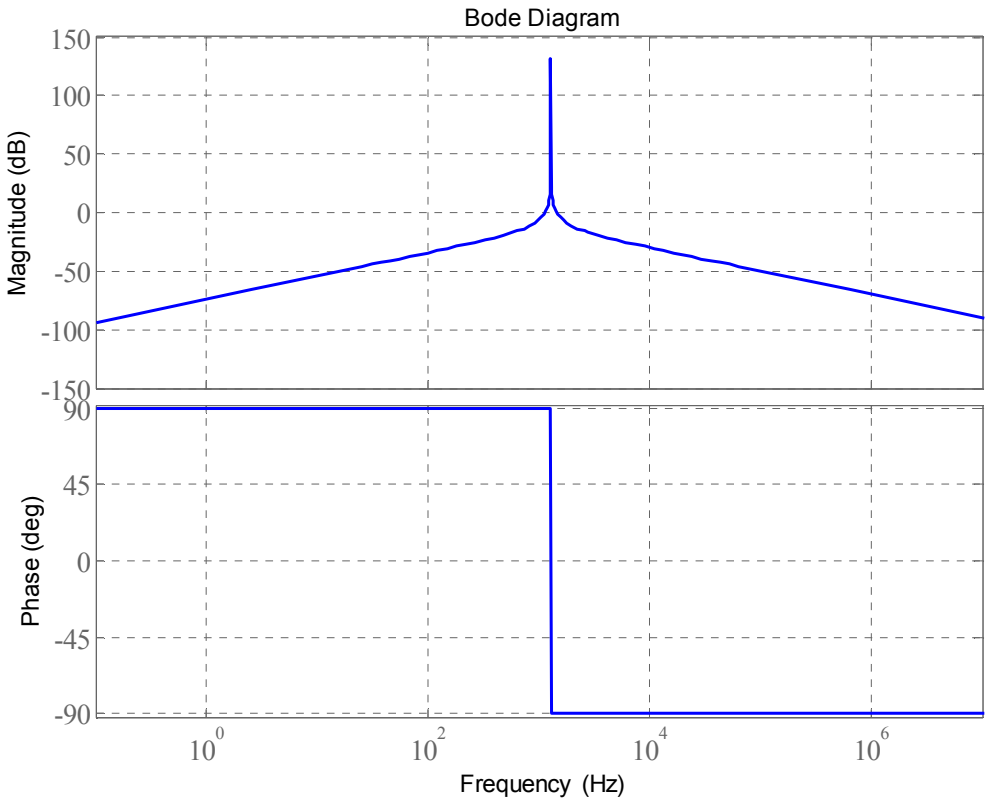

Figure 2.11. Bode plot of the transfer function of the input admittance of the Z-source circuit

Control of the Z-source circuit takes place using the duty cycle as the control variable and bode plot of the transfer function relating the control to the Z-source circuit capacitor and inductor are also shown. This is to reveal possible resonance and its frequency similarly to [7]. Such resonance of the capacitor voltage or the inductor current may occur. It is therefore important to assess whether the resonance magnitude and frequency may be detrimental to the components. The transfer function relating the Z-source circuit capacitor voltage to control is given by equation (2.39) after substituting the parameters of Table 2.1. The bode plot is shown in Figure 2.12.

$$G_{vd} = \frac{\tilde{v}_c(s)}{\tilde{d}(s)}\Big|_{\tilde{i}n(s)=0} = \frac{3.615\times10^{-9}s^2 + 8.353\times10^{-5}s + 0.27}{7.958\times10^{-15}s^3 + 1.393\times10^{-11}s^2 + 8.517\times10^{-7}s + 5.59\times10^{-4}} \tag{2.39}$$

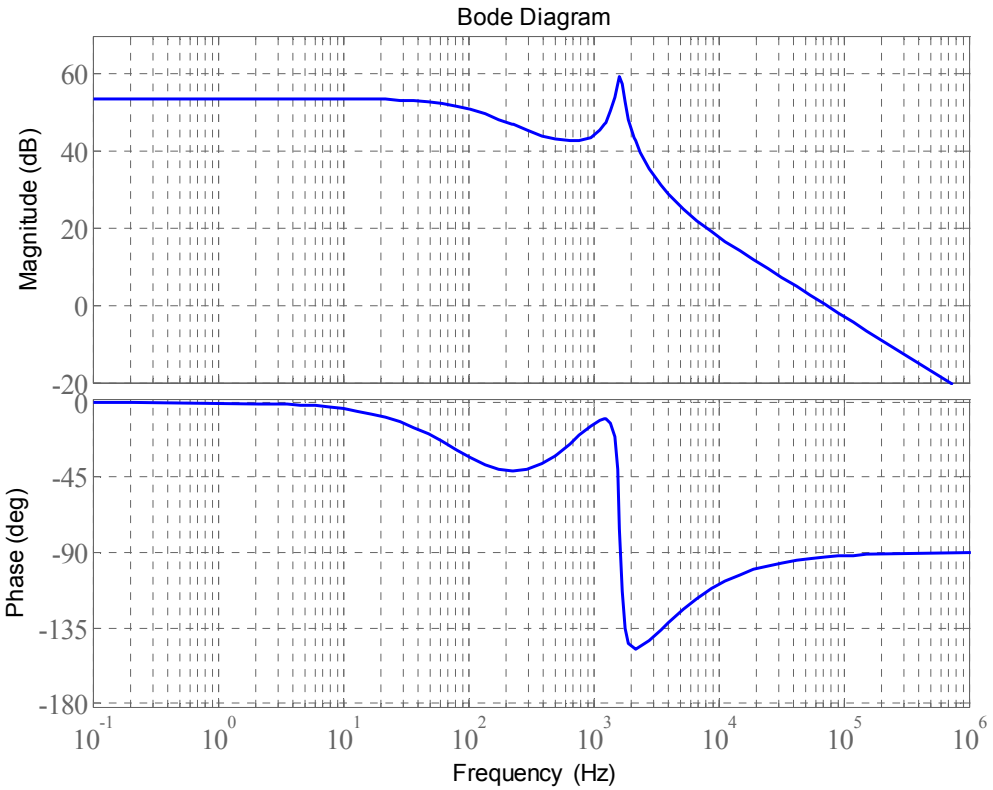

Figure 2.12. Bode plot of the transfer function relating the Z-source circuit capacitor voltage to control

The magnitude and phase plots in Figure 2.12 of the transfer function relating the Z-source circuit capacitor voltage to control shows that resonance of the capacitor voltage takes place at a frequency of 1.64 kHz. However the peak resonance magnitude is 5.8 dB higher than the DC magnitude of the capacitor voltage and is not too detrimental to the capacitor. Such resonance amplitude could well be within the capacitor tolerance. It is important to realise from the phase plot that the Z-source circuit capacitor voltage is expected to be stable for all frequencies because the phase rolls down within 180 degree. This transfer function can be used to implement direct or indirect control of the peak DC output voltage of the full-bridge rectifier similar to the inverter applications in [20] [46].

The transfer function relating the Z-source circuit inductor current to control is given by equation (2.40) after substituting the parameters of Table 2.1. The bode plot is shown in Figure 2.13. The significance of the transfer function relating the Z-source circuit inductor

current to control is on current control scheme of the Z-source circuit. Steady state analysis has shown in equation (2.7) that the average inductor current and the load current are equal. Control of the Z-source circuit inductor current can therefore be utilised to control the load current.

$$G_{id} = \frac{\tilde{i}_L(s)}{\tilde{d}(s)}\Big|_{\tilde{i}n(s)=0} = \frac{-1.872\times10^{-6}s^2 + 2.823\times10^{-3}s + 6.15}{7.958\times10^{-15}s^3 + 1.393\times10^{-11}s^2 + 8.517\times10^{-7}s + 5.59\times10^{-4}} \tag{2.40}$$

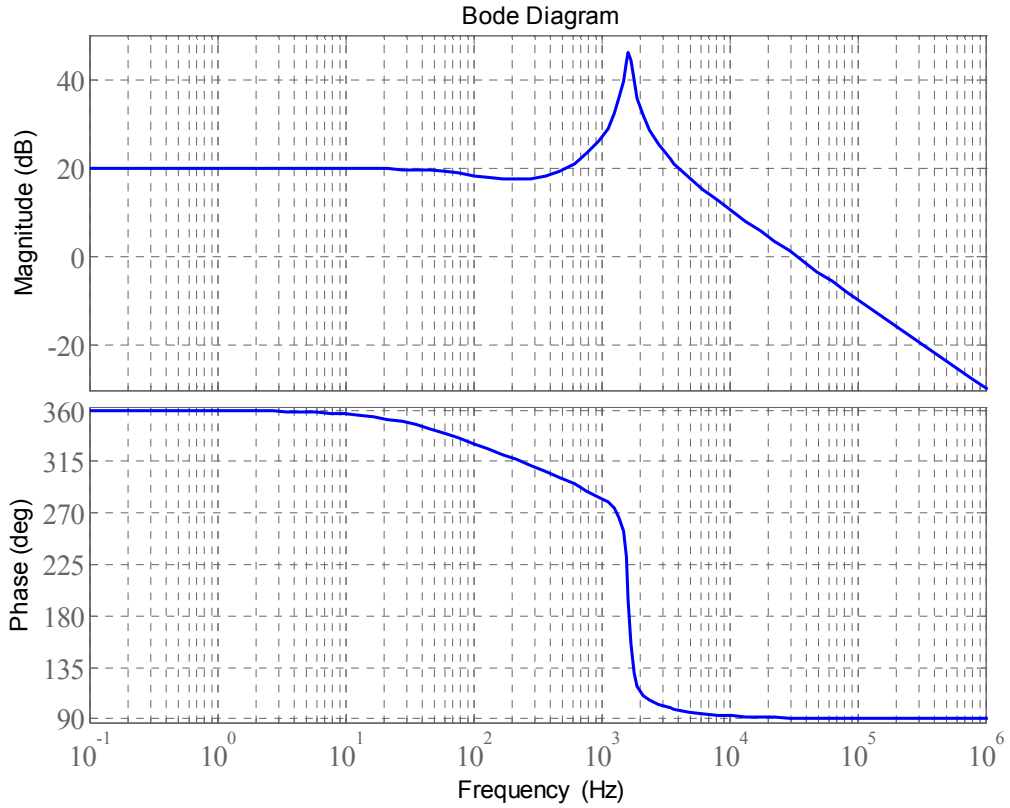

Figure 2.13. Bode plot of the transfer function relating the Z-circuit inductor current to control

The bode plot of the transfer function relating the Z-source circuit inductor current to control shown in Figure 2.13 is similar to the bode plot found in [14]. However the modelling approach that was developed leading to the transfer functions is much easier than the approach used in [14]. It is observed from the bode plot that resonance takes place at 1.64 kHz with a peak magnitude of 46.1 dB, and an abrupt phase drop to 180 degree. The

ideal performance with current control is to achieve the highest possible bandwidth for fast current response. However the bode plot of Figure 2.13 and the pole-zero map of Figure 2.14 show that the achievable bandwidth is limited well below the resonance frequency or the RHP zero frequency. For a switching frequency of 40 kHz of the Z-circuit this represents a low performance due to the characteristic of the transfer function relating the inductor current to control.

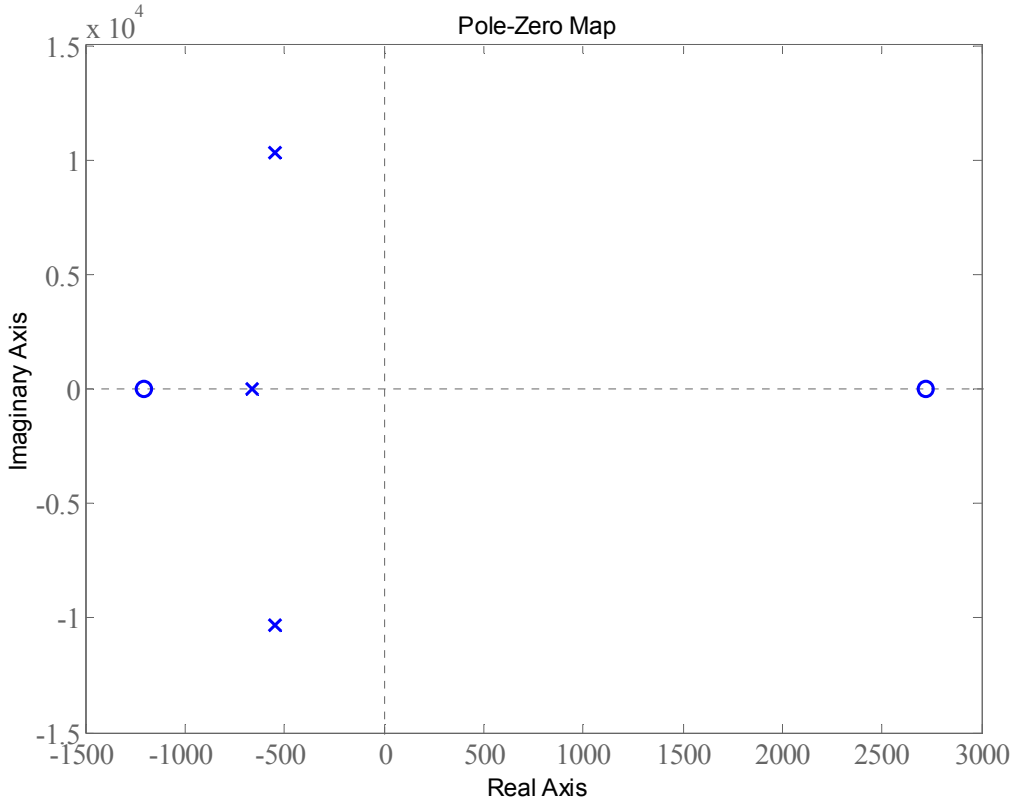

Figure 2.14. Pole-zero map of the transfer function relating the Z-circuit inductor current to control

2.4. CHAPTER CONCLUSION

Modelling of the ZSR was derived using circuit averaging and leads to similar output voltage and inductor current magnitude and phase bode plots as in [6] [7] [14]. Unlike the approach in [6] that uses state space modelling requiring a 5x5 complex matrix inversion to obtain the transfer functions, the simpler alternative approach based on circuit averaging produces all transfer functions and the block representation of the ZSR. Mathematical basis

for the use of symmetrical components in the ZSR is also demonstrated. The block diagram representation of the ZSR in Figure 2.4 can be used to design a closed-loop controller to regulate the output DC voltage and to draw a low harmonic AC input current in phase with the AC input voltage.

CHAPTER 3 MODELLING OF THE QUASI-Z-SOURCE THREE-PHASE RECTIFIER

3.1. INTRODUCTION

A quasi-Z-source three-phase rectifier is essentially a voltage or current source three-phase rectifier combined with a quasi-Z-source circuit. The quasi-Z-source circuit modifies the characteristics of the basic VSR or CSR to give it all the advantages described in the introduction. Similar to the modelling approach used for the Z-source three-phase rectifier, the overall model of the quasi-Z-source three-phase rectifier can be obtained by combining the traditional PWM full-bridge rectifier model and equivalent model of the quasi-Z-source circuit. Comparable arguments presented in chapter 2 motivating the use of this modelling approach for the Z-source three-phase are also applicable to the quasi-Z-source three-phase rectifier modelling.

State space modelling tool could be considered to analyse the quasi-Z-source circuit. However, modelling using state space will require a complex 5x5 matrix inversion due to the large number of variables in the quasi-Z-source circuit. The complex multi-input multi-output (MIMO) nonlinear structure from a state space model does not give clear insight on the behaviour of the converter and make it difficult to design a closed-loop controller for both the PWM full-bridge rectifier and the quasi-Z-source circuit. The alternative power converter modelling tool considered is circuit averaging in which small-signal linearization lead to the AC and DC model with ease. A major contribution is the use of circuit averaging to obtain a detailed and accurate model of the QZSR which enables the design of a closed-loop controller. The model that was developed using circuit averaging keeps the computation simple and relates the DC and AC quantities effectively.

The QZSR can be subdivided into two small sub-circuits: a rectification circuit through the full-bridge, and a DC-DC conversion operation through the quasi-Z-source circuit utilising the shoot-through duty ratio. The DC output from the rectification is used as input to the

quasi-Z-source circuit. The dynamic model of the quasi-Z-source three-phase rectifier is found by first developing the model for the quasi-Z-source circuit DC side and then combining it with the full-bridge rectifier model. The small-signal model and the steady state DC operating point of the quasi-Z-source circuit is obtained by analysing the circuit during shoot-through and non-shoot-through interval. The following assumptions are used in the analysis of the quasi-Z-source circuit:

- The QZSR is operating with continuous inductor current.
- The passive components L and C are lossless and the switch on time losses are ignored.

The shoot-through time is expressed by DT_{sw} and non-shoot-through time by (1-D) T_{sw} = $D'T_{sw}$ based on the simple boost modulation method that was used. T_{sw} is the switching period. The minimum DC output voltage from a full-bridge PWM rectification is twice the peak value of the AC input voltage [3]. The quasi-Z-source circuit model is most important in the rectifier operation for the interval where shoot-through is required to step down the full-bridge output voltage to the desired DC output voltage.

By considering the equivalent circuit of the quasi-Z-source circuit during non-shoot-through state shown in Figure 3.1 the circuit equations that were derived can be written as:

$$
\begin{aligned}
L_1 \frac{di_{L1}}{dt} &= v_{c1} - v_{c2} \\
L_2 \frac{di_{L1}}{dt} &= v_{c2} \\
L_1 \frac{di_{L1}}{dt} &= v_{in} - v_{c2} - v_{co} \\
L_2 \frac{di_{L1}}{dt} &= v_{in} - v_{c1} \\
C_1 \frac{dv_{C1}}{dt} &= i_{in} - i_{L1} \\
C_2 \frac{dv_{C2}}{dt} &= i_{in} - i_{L2} \\
C_o \frac{dv_{Co}}{dt} &= i_{L1} - \frac{v_{Co}}{R_o} + i_{inj} \\
i_{sw} &= i_{L2} - i_{c1} = i_{in} \\
v_{sw} &= 0
\end{aligned}
\qquad (3.1)
$$

Where v_{in} is the peak output DC voltage of the three-phase full-bridge PWM rectifier and the DC input voltage to the quasi-Z-source circuit. i_{sw} and V_{sw} are respectively the quasi-Z-source switch DC current and blocking voltage

By considering the equivalent circuit of the quasi-Z-source circuit during shoot-through state shown in Figure 3.2 the equations that were derived can be written as:

$$\begin{aligned}
L_1 \frac{di_{L1}}{dt} &= -v_{c2} - v_{co} \\
L_2 \frac{di_{L1}}{dt} &= -v_{c1} \\
C_1 \frac{dv_{C1}}{dt} &= i_{L2} \\
C_2 \frac{dv_{C2}}{dt} &= i_{L1} \\
C_o \frac{dv_{Co}}{dt} &= i_{L1} - \frac{v_{Co}}{R_o} + i_{inj} \\
v_{swblock} &= v_{c1} + v_{c2} \\
i_{sw} &= 0
\end{aligned} \tag{3.2}$$

The shoot-through duty ratio is used as a weight in the averaging process to obtain differential equations that describe the dynamics of the circuit over an entire switching period as follows:

$$\begin{aligned}
dL_1 \frac{di_{L1}}{dt} + (1-d)L_1 \frac{di_{L1}}{dt} &= v_{c1}(1-d) - v_{c2}d - v_{co} \\
dL_1 \frac{di_{L1}}{dt} + (1-d)L_1 \frac{di_{L1}}{dt} &= v_{in}(1-d) - v_{c2} - v_{co} \\
dL_2 \frac{di_{L2}}{dt} + (1-d)L_2 \frac{di_{L2}}{dt} &= v_{c2}(1-d) - v_{c1}d \\
dL_2 \frac{di_{L2}}{dt} + (1-d)L_2 \frac{di_{L2}}{dt} &= v_{in}(1-d) - v_{c1} \\
dC_1 \frac{dv_{C1}}{dt} + (1-d)C_1 \frac{dv_{C1}}{dt} &= i_{in}(1-d) - i_{L1}(1-d) + i_{L2}d \\
dC_2 \frac{dv_{C2}}{dt} + (1-d)C_2 \frac{dv_{C2}}{dt} &= i_{in}(1-d) - i_{L2}(1-d) + i_{L1}d \\
dC_o \frac{dv_{Co}}{dt} + (1-d)C_o \frac{dv_{Co}}{dt} &= i_{L1} - \frac{v_{co}}{R_o} + i_{inj}
\end{aligned} \tag{3.3}$$

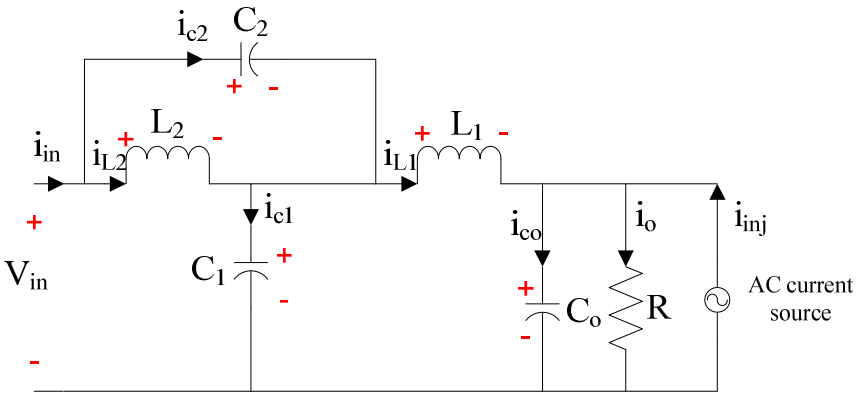

Figure 3.1. Quasi-Z-source circuit in non-shoot-through state

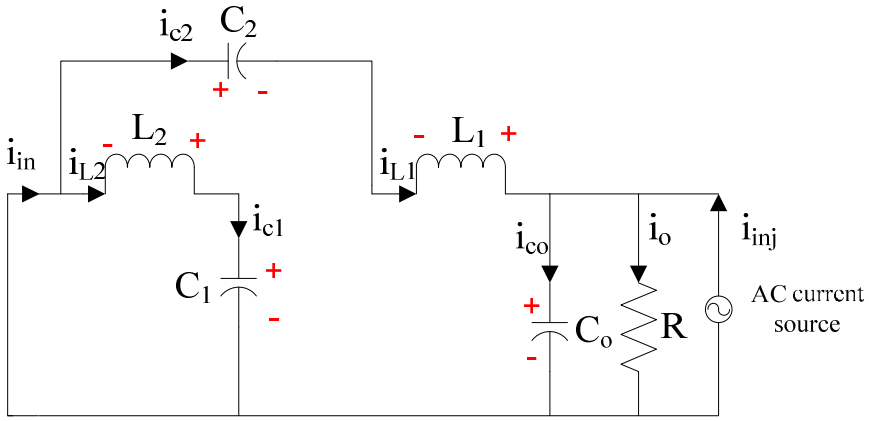

Figure 3.2. Quasi-Z-source circuit in shoot-through state

Separate the various parameters and variables into DC and AC components:

$$\begin{aligned} v_{in} &= V_{in} + \tilde{v}_{in} \\ v_{c1} &= V_{c1} + \tilde{v}_{c1} \\ v_{c2} &= V_{c2} + \tilde{v}_{c2} \\ i_{L1} &= I_{L1} + \tilde{i}_{L1} \\ i_{L2} &= I_{L2} + \tilde{i}_{L2} \\ v_{co} &= v_{co} + \tilde{v}_{co} \\ d &= D + \tilde{d} \end{aligned} \tag{3.4}$$

Substitute equation (3.4) into equation (3.3) to yield the perturbed equation (3.5) given by:

$$\begin{aligned} L_1 \frac{d\tilde{i}_{L1}}{dt} &= \left(V_{c1} + \tilde{v}_{c1}\right)\left(1 - \tilde{d} - D\right) - \left(V_{c2} + \tilde{v}_{c2}\right)\left(D + \tilde{d}\right) - \tilde{v}_{co} - V_{co} \\ L_1 \frac{d\tilde{i}_{L1}}{dt} &= \left(V_{in} + \tilde{v}_{in}\right)\left(1 - \tilde{d} - D\right) - V_{c2} - \tilde{v}_{c2} - \tilde{v}_{co} - V_{co} \end{aligned} \tag{3.5}$$

$$
\begin{aligned}
L_2\frac{d\tilde{i}_{L2}}{dt} &= (V_{c2}+\tilde{v}_{c2})(1-\tilde{d}-D)-(V_{c1}+\tilde{v}_{c1})(D+\tilde{d})\\
L_2\frac{d\tilde{i}_{L2}}{dt} &= (V_{in}+\tilde{v}_{in})(1-\tilde{d}-D)-\tilde{v}_{c1}-V_{c1}\\
C_1\frac{d\tilde{v}_{C1}}{dt} &= (I_{in}+\tilde{i}_{in})(1-\tilde{d}-D)-(I_{L1}+\tilde{i}_{L1})(1-\tilde{d}-D)+(I_{L2}+\tilde{i}_{L2})(D+\tilde{d})\\
C_2\frac{d\tilde{v}_{C2}}{dt} &= (I_{in}+\tilde{i}_{in})(1-\tilde{d}-D)-(I_{L2}+\tilde{i}_{L2})(1-\tilde{d}-D)+(I_{L1}+\tilde{i}_{L1})(D+\tilde{d})\\
C_o\frac{d\tilde{v}_{Co}}{dt} &= I_{L1}+\tilde{i}_{L1}-\frac{V_{co}}{R_o}-\frac{\tilde{v}_{co}}{R_o}+\tilde{i}_{inj}
\end{aligned}
\tag{3.5}
$$

Separate the various parameters and variables into DC components. The DC equations are obtained as follows:

$$
\begin{aligned}
&V_{c1}(1-D)-V_{c2}D-V_{co}=0\\
&V_{in}(1-D)-V_{c2}-V_{co}=0\\
&V_{c2}(1-D)-V_{c1}D=0\\
&V_{c1}=V_{in}(1-D)\\
&I_{L1}-I_o=0\\
&I_{in}(1-D)-I_{L1}(1-D)+I_{L2}D=0\\
&I_{in}(1-D)-I_{L2}(1-D)+I_{L1}D=0
\end{aligned}
\tag{3.6}
$$

3.2. STEADY STATE MODEL

By solving equation (3.6) the inductors' DC current and capacitors' DC voltage are given by:

$$
\begin{aligned}
V_{c1} &= V_{in}(1-D)=\frac{(1-D)}{(1-2D)}V_{co}\\
V_{c2} &= V_{in}D=\frac{D}{(1-2D)}V_{co}\\
V_{co} &= V_{in}(1-2D)\\
I_{L1,av} &= I_{L2,av}=I_{o,av}\\
I_{in,av} &= \frac{(1-2D)}{(1-D)}I_{o,av}
\end{aligned}
\tag{3.7}
$$

It is important to note that the quasi-Z-source circuit and the Z-source circuit inductor DC current and capacitor DC voltages of equation (3.7) and equation (2.7) are comparables except for capacitor C_2.

The quasi-Z-source circuit switch voltage during shoot-through interval is obtained from equation (3.2) and equation (3.7) as follows:

$$V_{sw} = V_{c1} + V_{c2} = \frac{(1-D)}{(1-2D)}V_{co} + \frac{D}{(1-2D)}V_{co} = \frac{1}{(1-2D)}V_{co} \tag{3.8}$$

The overall DC gain of the rectifier is obtained by making use of the PWM full-bridge peak DC output. The peak DC output voltage V_{in} of the full-bridge is given in [3] [4] [6] by:

$$V_{in} = \frac{2V_{sp}}{M\cos\theta} \tag{3.9}$$

With $\cos\theta = \arctan\frac{wL_S}{R_S}$ and V_{sp} the peak value of the line to neutral of the input AC source voltage, M is the modulation index, R_s the input resistance and L_s the input inductance [3] [6].

From equation (3.7) $V_{co} = V_{in}(1-2D)$ and combining with equation (3.9) the output DC voltage is given by equation (3.10) [1] [4] [6]:

$$V_{co} = \frac{2V_{sp}(1-2D)}{M\cos\theta} = \frac{2BV_{sp}}{\cos\theta} \tag{3.10}$$

Where B is the DC gain of the rectifier or buck- boost factor given by equation (3.11) [1] [4] [6]:

$$B = \frac{1-2D}{M} = \frac{b}{M} \tag{3.11}$$

Where

$$b = 1-2D \tag{3.12}$$

The buck-boost factor B is determined by the modulation index M and buck factor b. The buck factor is controlled by duty cycle of the shoot-through zero state over the non-shoot-through states of the rectifier PWM. To achieve the buck-boost performance of the QZSR, the buck-boost factor can vary from 0 to infinity by controlling the modulation index and the shoot-through duty ratio. It can be seen in Figure 3.3 that as the shoot-through duty cycle varies the rectifier changes from a boosting to a bucking action with a reversal of polarity of the output voltage with shoot-through above 0.5. However at shoot-through duty cycle above 0.3 the modulation index of the full-bridge converter is very low as per simple boost modulation method. It has been shown [2] [47] that low modulation PWM switching increases input AC current harmonic and the full-bridge switch stress. Furthermore high shoot-through duty cycle values increases the voltage across the switch of the quasi-Z-source circuit as given by equation (3.8). This voltage increase is due to the simple boost PWM control method chosen.

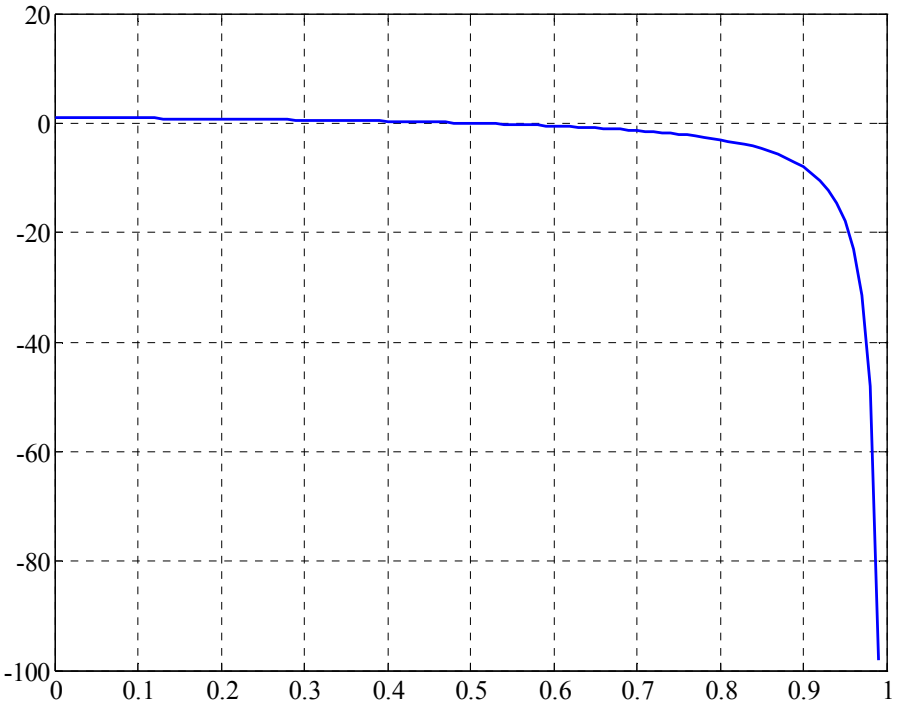

Figure 3.3. Relationship between the rectifier gain B and shoot-through duty cycle D

It is possible to make use of equation (3.2) in shoot-through state to size the component for a given ripple specification. The QZSR components can be sized from the expression given by:

$$\begin{aligned} L_1 &= \frac{(V_{c2}+V_{co})D}{\Delta i_{L1} F_{sw}} \\ L_2 &= \frac{V_{c1} D}{\Delta i_{L2} F_{sw}} \\ C_1 &= \frac{D I_{L2}}{\Delta v_{c1} F_{sw}} \\ C_2 &= \frac{D I_{L1}}{\Delta v_{c2} F_{sw}} \\ C_o &= \frac{\Delta i_{L1}}{8 \Delta v_{co} F_{sw}} \end{aligned} \tag{3.13}$$

Equation (3.13) demonstrates that it is not necessary to use symmetrical capacitors in a QZSR. The capacitors' DC voltages expressions that were derived in equation (3.7) show that capacitors C_1 and C_2 DC voltages are not equal. Considering that QZSR operations are limited to small shoot-through duty ratio, capacitor C_1 voltage is larger than C_2 voltage. For the same percentage ripple of their steady state voltage, the peak-to-peak ripple voltage of capacitor C_1 is larger than that of C_2, as a result capacitance of C_2 is larger than C_1. Therefore using symmetrical capacitors C_1 and C_2 will result in oversizing C_1 based on equation (3.7). The DC voltage rating of C_2 is however smaller than C_1 from equation (3.7). For the inductors symmetrical components may be used because the inductors DC currents are equal and equal DC voltage appear across each inductor as shown by equation (3.7).

3.3. SMALL SIGNAL MODEL

The response of a variable to multiple variations can be expressed from the superposition of its response to each individual input variation in its dynamic equation [13]. Accounting for all the variables appearing in the dynamic equation, the small-signal of each quasi-Z-source circuit capacitor and inductor can be expressed as:

$$\begin{aligned} v_c(s) &= G_{vg}(s).i_g(s) + G_{vd}(s).d(s) \\ i_L(s) &= G_{ig}(s).i_g(s) + G_{id}(s).d(s) \end{aligned} \tag{3.14}$$

Where G_{vg} is the transfer function relating the capacitor voltage to the input current, G_{ig} is

the transfer function relating the inductor current to the input current, G_{vd} is the transfer function relating the capacitor voltage to control, G_{id} is the transfer function relating the inductor current to control. These transfer functions are then derived for the QZSR from the AC equations linearised at the DC values given in equation (3.7).

The AC terms are extracted from equation (3.5) and transformed in Laplace form to obtain:

$$\begin{aligned}
sC_o\tilde{v}_{co}(s) &= \tilde{i}_{L1}(s) - \frac{\tilde{v}_{co}(s)}{R_o} + \tilde{i}_{inj}(s) \\
sC_1\tilde{v}_{c1}(s) &= \tilde{i}_{in}(s)D' - \tilde{i}_{L1}(s)D' + \tilde{i}_{L2}(s)D + \tilde{d}(s)I_{LT} \\
sC_2\tilde{v}_{c2}(s) &= \tilde{i}_{in}(s)D' + \tilde{i}_{L1}(s)D - \tilde{i}_{L2}(s)D' + \tilde{d}(s)I_{LT} \\
sL_1\tilde{i}_{L1}(s) &= \tilde{v}_{c1}(s)D' - \tilde{v}_{c2}(s)D - \tilde{v}_{co}(s) - \tilde{d}(s)V_{CT} \\
sL_1\tilde{i}_{L1}(s) &= \tilde{v}_{in}(s)D' - \tilde{v}_{c2}(s) - \tilde{v}_{co}(s) - \tilde{d}(s)V_{in} \\
sL_2\tilde{i}_{L2}(s) &= \tilde{v}_{c2}(s)D' - \tilde{v}_{c1}(s)D - \tilde{d}(s)V_{CT} \\
sL_2\tilde{i}_{L2}(s) &= \tilde{v}_{in}(s)D' - \tilde{v}_{c1}(s) - \tilde{d}(s)V_{in}
\end{aligned} \tag{3.15}$$

$$where \quad I_{LT} = I_{L1} + I_{L2} - I_{in} \; and \; V_{CT} = V_{C1} + V_{C2}$$

From equation (3.15), the inductors current can be expressed by:

$$\begin{aligned}
\tilde{i}_{L1}(s) &= \frac{\tilde{v}_{in}(s)D' - \tilde{v}_{c2}(s) - \tilde{v}_{co}(s) - \tilde{d}(s)V_{in}}{sL_1} \\
\tilde{i}_{L2}(s) &= \frac{\tilde{v}_{in}(s)D' - \tilde{v}_{c1}(s) - \tilde{d}(s)V_{in}}{sL_2}
\end{aligned} \tag{3.16a}$$

$$\begin{aligned}
\tilde{i}_{L1}(s) &= \frac{\tilde{v}_{c1}(s)D' - \tilde{v}_{c2}(s)D - \tilde{v}_{co}(s) - \tilde{d}(s)V_{CT}}{sL_1} \\
\tilde{i}_{L2}(s) &= \frac{\tilde{v}_{c2}(s)D' - \tilde{v}_{c1}(s)D - \tilde{d}(s)V_{CT}}{sL_2}
\end{aligned} \tag{3.16b}$$

Eliminate the inductors currents from the capacitors voltage equation (3.15) by substituting equation (3.16a) as follow:

$$\begin{aligned}
sC_o v_{co}(s) &= \frac{v_{in}(s)D' - v_{c2}(s) - v_{co}(s) - d(s)V_{in}}{sL_1} - \frac{v_{co}(s)}{R_o} + i_{inj}(s) \\
v_{co}(s) &= \frac{v_{in}(s)D' - v_{c2}(s) - d(s)V_{in} + sL_1 i_{inj}(s)}{s^2C_oL_1 + \frac{sL_1}{R_0} + 1}
\end{aligned} \tag{3.17a}$$

$$
\begin{aligned}
sC_1v_{c1}(s) &= i_{in}(s)D' - \left(\frac{v_{in}(s)D' - v_{c2}(s) - v_{co}(s) - d(s)V_{in}}{sL_1}\right)D' \\
&\quad + \left(\frac{v_{in}(s)D' - v_{c1}(s) - d(s)V_{in}}{sL_2}\right)D + d(s)I_{LT} \\
v_{c1}(s) &= \frac{L_2D'v_{c2}(s) + L_2D'v_{co}(s) + (L_1DD' - L_2D'^2)v_{in}(s)}{s^2C_1L_1L_2 + DL_1} \\
&\quad + \frac{[(L_2D' - L_1D)V_{in} + sL_1L_2I_{LT}]d(s) + sL_1L_2D'i_{in}(s)}{s^2C_1L_1L_2 + DL_1} \\
sC_2v_{c2}(s) &= i_{in}(s)D' + \left(\frac{v_{in}(s)D' - v_{c2}(s) - v_{co}(s) - d(s)V_{in}}{sL_1}\right)D \\
&\quad - \left(\frac{v_{in}(s)D' - v_{c1}(s) - d(s)V_{in}}{sL_2}\right)D' + d(s)I_{LT} \\
v_{c2}(s) &= \frac{D'L_1v_{c1}(s) - L_2Dv_{co}(s) + (L_2DD' - L_1D'^2)v_{in}(s)}{s^2C_2L_1L_2 + DL_2} \\
&\quad + \frac{[(L_1D' - L_2D)V_{in} + sL_1L_2I_{LT}]d(s) + sL_1L_2D'i_{in}(s)}{s^2C_2L_1L_2 + DL_2}
\end{aligned}
\tag{3.17a}
$$

Eliminate the inductor currents from the capacitors voltage equation (3.15) by substituting equation (3.16b) as follow:

$$
\begin{aligned}
sC_ov_{co}(s) &= \frac{v_{c1}(s)D' - v_{c2}(s)D - v_{co}(s) - d(s)V_{CT}}{sL_1} - \frac{v_{co}(s)}{R_o} + i_{inj}(s) \\
v_{co}(s) &= \frac{v_{c1}(s)D' - v_{c2}(s)D - d(s)V_{CT} + sL_1i_{inj}(s)}{s^2C_oL_1 + \frac{sL_1}{R_0} + 1} \\
sC_1v_{c1}(s) &= i_{in}(s)D' - \left(\frac{v_{c1}(s)D' - v_{c2}(s)D - v_{co}(s) - d(s)V_{CT}}{sL_1}\right)D' \\
&\quad + \left(\frac{v_{c2}(s)D' - v_{c1}(s)D - d(s)V_{CT}}{sL_2}\right)D + d(s)I_{LT} \\
v_{c1}(s) &= \frac{(L_2DD' + L_1DD')v_{c2}(s) + L_2D'v_{co}(s)}{s^2C_1L_1L_2 + D'^2L_2 + D^2L_1} \\
&\quad + \frac{(L_2D' - L_1D)V_{CT}d(s) + sL_1L_2I_{LT}d(s) + sL_1L_2D'i_{in}(s)}{s^2C_1L_1L_2 + D'^2L_2 + D^2L_1}
\end{aligned}
\tag{3.17b}
$$

$$
\begin{aligned}
sC_2v_{c2}(s) &= i_{in}(s)D' + \left(\frac{v_{c1}(s)D' - v_{c2}(s)D - v_{co}(s) - d(s)V_{CT}}{sL_1}\right)D \\
&\quad - \left(\frac{v_{c2}(s)D' - v_{c1}(s)D - d(s)V_{CT}}{sL_2}\right)D' + d(s)I_{LT} \\
v_{c2}(s) &= \frac{(L_2DD' + L_1DD')v_{c1}(s) - L_2Dv_{co}(s)}{s^2C_2L_1L_2 + D^2L_2 + D'^2L_1} \\
&\quad + \frac{(L_1D' - L_2D)V_{CT}d(s) + sL_1L_2I_{LT}d(s) + sL_1L_2D'i_{in}(s)}{s^2C_2L_1L_2 + D^2L_2 + D'^2L_1}
\end{aligned}
\tag{3.17b}
$$

From equation (3.17a) and equation (3.17b) the following characteristic equations and parameters are defined in equation (3.18):

$$
\begin{aligned}
q_{co} &= s^2C_oL_1 + \frac{sL_1}{R_o} + 1 \\
q_{c1a} &= s^2C_1L_1L_2 + DL_1 \\
q_{c2a} &= s^2C_2L_1L_2 + DL_2 \\
q_{c1} &= s^2C_1L_P + D'^2L_2 + D^2L_1 \\
q_{c2} &= s^2C_2L_P + L_2D^2 + L_1D'^2 \\
L_T &= L_1 + L_2 \\
L_P &= L_1L_2 \\
C_T &= C_1 + C_2 \\
C_P &= C_1C_2 \\
\alpha_1 &= L_2D' - L_1D \\
\alpha_2 &= L_1D' - L_2D
\end{aligned}
\tag{3.18}
$$

Equation (3.19a) and equation (3.19b) are obtained after including the expressions from equation (3.18):

$$
\begin{aligned}
q_{co}v_{co}(s) &= v_{in}(s)D' - v_{c2}(s) - d(s)V_{in} + sL_1i_{inj}(s) \\
q_{c1a}v_{c1}(s) &= L_2D'v_{c2}(s) + L_2D'v_{co}(s) + (L_1DD' - L_2D'^2)v_{in}(s) \\
&\quad + [\alpha_1V_{in} + sL_PI_{LT}]d(s) + sL_PD'i_{in}(s) \\
q_{c2a}v_{c2}(s) &= D'L_1v_{c1}(s) - L_2Dv_{co}(s) + (L_2DD' - L_1D'^2)v_{in}(s) \\
&\quad + [\alpha_2V_{in} + sL_PI_{LT}]d(s) + sL_PD'i_{in}(s)
\end{aligned}
\tag{3.19a}
$$

$$
\begin{aligned}
q_{co}v_{co}(s) &= v_{c1}(s)D' - v_{c2}(s)D - d(s)V_{CT} + sL_1i_{inj}(s) \\
q_{c1}v_{c1}(s) &= DD'L_Tv_{c2}(s) + L_2D'v_{co}(s) + \alpha_1V_{CT}d(s) + sL_PI_{LT}d(s) + sL_PD'i_{in}(s) \\
q_{c2}v_{c2}(s) &= DD'L_Tv_{c1}(s) - L_2Dv_{co}(s) + \alpha_2V_{CT}d(s) + sL_PI_{LT}d(s) + sL_PD'i_{in}(s)
\end{aligned}
\tag{3.19b}
$$

From equation (3.19a) and equation (3.19b) capacitor C_2 voltage is expressed by:

$$v_{c2}(s)=\frac{D'L_1v_{c1}(s)-L_2Dv_{co}(s)+\left(L_2DD'-L_1D'^2\right)v_{in}(s)}{q_{c2a}} \\ \frac{+\left[\alpha_2V_{in}+sL_PI_{LT}\right]d(s)+sL_PD'i_{in}(s)}{q_{c2a}} \tag{3.20a}$$

$$v_{c2}(s)=\frac{DD'L_Tv_{c1}(s)-L_2D'v_{co}(s)+\alpha_2V_{CT}d(s)+sL_PI_{LT}d(s)+sL_PD'i_{in}(s)}{q_{c2}} \tag{3.20b}$$

By substituting equation (3.20a) into equation (3.19a), capacitor C_2 voltage is eliminated from capacitor C_o and C_1 voltage to obtain equation (3.21a) given by:

$$\begin{aligned}
q_{c2a}q_{co}v_{co}(s)&=v_{in}(s)q_{c2a}D'-D'L_1v_{c1}(s)+L_2Dv_{co}(s)-\left(L_2DD'-L_1D'^2\right)v_{in}(s)\\
&\quad-\left[\alpha_2V_{in}+sL_PI_{LT}\right]d(s)-sL_PD'i_{in}(s)-d(s)q_{c2a}V_{in}+sq_{c2a}L_1i_{inj}(s)\\
\left[q_{c2a}q_{co}-L_2D\right]v_{co}(s)&=\left[q_{c2a}D'-\left(L_2DD'-L_1D'^2\right)\right]v_{in}(s)-sL_PD'i_{in}(s)\\
&\quad-\left[\left(\alpha_2V_{in}+sL_PI_{LT}\right)+q_{c2a}V_{in}\right]d(s)-D'L_1v_{c1}(s)+sq_{c2a}L_1i_{inj}(s)\\
q_{c2a}q_{c1a}v_{c1}(s)&=D'^2L_pv_{c1}(s)-L_2{}^2DD'v_{co}(s)+L_2D'\left(L_2DD'-L_1D'^2\right)v_{in}(s)\\
&\quad+L_2D'\left[\alpha_2V_{in}+sL_PI_{LT}\right]d(s)+sL_2L_PD'^2i_{in}(s)\\
&\quad+q_{c2a}L_2D'v_{co}(s)+q_{c2a}\left(L_1DD'-L_2D'^2\right)v_{in}(s)\\
&\quad+q_{c2a}\left[\alpha_1V_{in}+sL_PI_{LT}\right]d(s)+sq_{c2a}L_PD'i_{in}(s)\\
\left[q_{c2a}q_{c1a}-D'^2L_p\right]v_{c1}(s)&=\left[L_2D'\left(L_2DD'-L_1D'^2\right)+q_{c2a}\left(L_1DD'-L_2D'^2\right)\right]v_{in}(s)\\
&\quad+\left(sL_2L_PD'^2+sq_{c2a}L_PD'\right)i_{in}(s)+\left(q_{c2a}L_2D'-L_2{}^2DD'\right)v_{co}(s)\\
&\quad+\left[L_2D'\left(\alpha_2V_{in}+sL_PI_{LT}\right)+q_{c2a}\left(\alpha_1V_{in}+sL_PI_{LT}\right)\right]d(s)
\end{aligned} \tag{3.21a}$$

By substituting equation (3.20b) into equation (3.19b), capacitor C_2 voltage is eliminated from capacitor C_o and C_1 voltage to obtain equation (3.21a) given by:

$$\begin{aligned}
q_{co}q_{c2}v_{co}(s)&=q_{c2}v_{c1}(s)D'-q_{c2}d(s)V_{CT}-D^2D'L_Tv_{c1}(s)+L_2D^2v_{co}(s)\\
&\quad-D\alpha_2V_{CT}d(s)-sL_PI_{LT}Dd(s)-sL_PDD'i_{in}(s)+sq_{c2}L_1i_{inj}(s)\\
\left[q_{co}q_{c2}-L_2D^2\right]v_{co}(s)&=\left(D'q_{c2}-D^2D'L_T\right)v_{c1}(s)-\left(q_{c2}V_{CT}+D\alpha_2V_{CT}\right)d(s)\\
&\quad-sL_PI_{LT}Dd(s)-sL_PDD'i_{in}(s)+sq_{c2}L_1i_{inj}(s)\\
q_{c1}q_{c2}v_{c1}(s)&=\left(DD'L_T\right)^2v_{c1}(s)-L_2L_TD'D^2v_{co}(s)+DD'L_T\alpha_2V_{CT}d(s)\\
&\quad+sDD'L_TL_PI_{LT}d(s)+sDD'^2L_TL_Pi_{in}(s)+q_{c2}L_2D'v_{co}(s)\\
&\quad+q_{c2}\alpha_1V_{CT}d(s)+sq_{c2}L_PI_{LT}d(s)+sq_{c2}L_PD'i_{in}(s)\\
\left[q_{c1}q_{c2}-\left(DD'L_T\right)^2\right]v_{c1}(s)&=\left(q_{c2}-D^2L_T\right)L_2D'v_{co}(s)+\left(DD'L_T\alpha_2+q_{c2}\alpha_1\right)V_{CT}d(s)\\
&\quad+\left(DD'L_T+q_{c2}\right)L_PI_{LT}sd(s)+\left(DD'L_T+q_{c2}\right)L_PD'si_{in}(s)
\end{aligned} \tag{3.21b}$$

To simplify equation (3.21a) and equation (3.21b), define the following:

$$\begin{aligned} Q_{coa} &= q_{c2a}q_{co} - L_2 D \\ Q_{co} &= q_{co}q_{c2} - L_2 D^2 \\ Q_{c1a} &= q_{c2a}q_{c1a} - D'^2\, L_p \\ Q_{c1} &= q_{c1}q_{c2} - (DD'L_T)^2 \\ M_1 &= (q_{c2} - D^2 L_T)D' \\ M_2 &= M_1 L_2 \end{aligned} \tag{3.22}$$

A simpler equation (3.21a) and equation (3.21b) is obtained after including the parameters from equation (3.22):

$$\begin{aligned} Q_{coa}v_{co}(s) &= \left[q_{c2a}D' - \left(L_2 DD' - L_1 D'^2\right)\right]v_{in}(s) - sL_P D' i_{in}(s) \\ &\quad - \left[(\alpha_2 V_{in} + sL_P I_{LT}) + q_{c2a}V_{in}\right]d(s) - D'L_1 v_{c1}(s) + sq_{c2a}L_1 i_{inj}(s) \\ Q_{c1a}v_{c1}(s) &= \left[L_2 D'\left(L_2 DD' - L_1 D'^2\right) + q_{c2a}\left(L_1 DD' - L_2 D'^2\right)\right]v_{in}(s) \\ &\quad + \left(sL_2 L_P D'^2 + sq_{c2a}L_P D'\right)i_{in}(s) + \left(q_{c2a}L_2 D' - L_2{}^2 DD'\right)v_{co}(s) \\ &\quad + \left[L_2 D'(\alpha_2 V_{in} + sL_P I_{LT}) + q_{c2a}(\alpha_1 V_{in} + sL_P I_{LT})\right]d(s) \end{aligned} \tag{3.23a}$$

$$\begin{aligned} Q_{co}v_{co}(s) &= M_1 v_{c1}(s) - (q_{c2} + D\alpha_2)V_{CT}d(s) - sL_P I_{LT}Dd(s) \\ &\quad - sL_P DD' i_{in}(s) + sq_{c2}L_1 i_{inj}(s) \\ Q_{c1}v_{c1}(s) &= M_2 v_{co}(s) + (DD'L_T\alpha_2 + q_{c2}\alpha_1)V_{CT}d(s) + (DD'L_T + q_{c2})L_P I_{LT}sd(s) \\ &\quad + (DD'L_T + q_{c2})L_P D' s i_{in}(s) \end{aligned} \tag{3.23b}$$

From equation (3.23a) substitute capacitor C_1 voltage into capacitor C_o voltage of equation (3.23a) to obtain the output capacitor C_o dynamic equation given by:

$$\begin{aligned} Q_{c1a}Q_{coa}v_{co}(s) &= Q_{c1a}\left[q_{c2a}D' - \left(L_2 DD' - L_1 D'^2\right)\right]v_{in}(s) - sQ_{c1a}L_P D' i_{in}(s) \\ &\quad - Q_{c1a}\left[(\alpha_2 V_{in} + sL_P I_{LT}) + q_{c2a}V_{in}\right]d(s) + sQ_{c1a}q_{c2a}L_1 i_{inj}(s) \\ &\quad - D'L_1\left[L_2 D'\left(L_2 DD' - L_1 D'^2\right) + q_{c2a}\left(L_1 DD' - L_2 D'^2\right)\right]v_{in}(s) \\ &\quad - D'L_1\left(sL_2 L_P D'^2 + sq_{c2a}L_P D'\right)i_{in}(s) - D'L_1\left(q_{c2a}L_2 D' - L_2{}^2 DD'\right)v_{co}(s) \\ &\quad - D'L_1\left[L_2 D'(\alpha_2 V_{in} + sL_P I_{LT}) + q_{c2a}(\alpha_1 V_{in} + sL_P I_{LT})\right]d(s) \\ \left[Q_{c1a}Q_{coa} + D'L_1\left(q_{c2a}L_2 D' - L_2{}^2 DD'\right)\right]v_{co}(s) &= sQ_{c1a}q_{c2a}L_1 i_{inj}(s) \\ &\quad + Q_{c1a}\left[q_{c2a}D' - \left(L_2 DD' - L_1 D'^2\right)\right]v_{in}(s) \\ &\quad - D'L_1\left[L_2 D'\left(L_2 DD' - L_1 D'^2\right) + q_{c2a}\left(L_1 DD' - L_2 D'^2\right)\right]v_{in}(s) \\ &\quad - \left[sQ_{c1a}L_P D' + D'L_1\left(sL_2 L_P D'^2 + sq_{c2a}L_P D'\right)\right]i_{in}(s) \\ &\quad - Q_{c1a}\left[(\alpha_2 V_{in} + sL_P I_{LT}) + q_{c2a}V_{in}\right]d(s) \\ &\quad - D'L_1\left[L_2 D'(\alpha_2 V_{in} + sL_P I_{LT}) + q_{c2a}(\alpha_1 V_{in} + sL_P I_{LT})\right]d(s) \end{aligned} \tag{3.24a}$$

From equation (3.23b) substitute capacitor C_1 voltage into capacitor C_o voltage of equation (3.23b) to obtain the output capacitor C_o dynamic equation given by:

$$\begin{aligned}
Q_{co}Q_{c1}v_{co}(s) &= M_1M_2v_{co}(s)+(DD'L_T\alpha_2+q_{c2}\alpha_1)V_{CT}M_1d(s)+sQ_{c1}q_{c2}L_1i_{inj}(s)\\
&\quad+(DD'L_T+q_{c2})M_1L_PI_{LT}sd(s)+(DD'L_T+q_{c2})L_PD'M_1si_{in}(s)\\
&\quad-Q_{c1}(q_{c2}+D\alpha_2)V_{CT}d(s)-sQ_{c1}L_PI_{LT}Dd(s)-sQ_{c1}L_PDD'i_{in}(s)\\
(Q_{co}Q_{c1}-M_1M_2)v_{co}(s) &= [(DD'L_T\alpha_2+q_{c2}\alpha_1)M_1-Q_{c1}(q_{c2}+D\alpha_2)]V_{CT}d(s)\\
&\quad+[(DD'L_T+q_{c2})M_1-Q_{c1}D]L_PI_{LT}sd(s)\\
&\quad+[(DD'L_T+q_{c2})M_1-Q_{c1}D']L_PD'si_{in}(s)\\
&\quad+sQ_{c1}q_{c2}L_1i_{inj}(s)
\end{aligned} \tag{3.24b}$$

From equation (3.23b) substitute capacitor C_o voltage into capacitor C_1 voltage of equation (3.23b) to obtain capacitor C_1 dynamic equation given by:

$$\begin{aligned}
Q_{c1}Q_{co}v_{c1}(s) &= M_2M_1v_{c1}(s)-M_2(q_{c2}+D\alpha_2)V_{CT}d(s)-sM_2L_PI_{LT}Dd(s)\\
&\quad-sM_2L_PDD'i_{in}(s)+sM_2q_{c2}L_1i_{inj}(s)+Q_{co}(DD'L_T\alpha_2+q_{c2}\alpha_1)V_{CT}d(s)\\
&\quad+Q_{co}(DD'L_T+q_{c2})L_PI_{LT}sd(s)+Q_{co}(DD'L_T+q_{c2})L_PD'si_{in}(s)\\
(Q_{co}Q_{c1}-M_1M_2)v_{c1}(s) &= [Q_{co}(DD'L_T\alpha_2+q_{c2}\alpha_1)-M_2(q_{c2}+D\alpha_2)]V_{CT}d(s)\\
&\quad+[Q_{co}(DD'L_T+q_{c2})-M_2D]L_PI_{LT}sd(s)\\
&\quad+[Q_{co}(DD'L_T+q_{c2})-M_2D]L_PD'si_{in}(s)+sM_2q_{c2}L_1i_{inj}(s)
\end{aligned} \tag{3.25}$$

To obtain the dynamic equation of capacitor C_2, eliminate capacitor C_1 voltage. From equation (3.19b) capacitor C_1 voltage is given by:

$$\tilde{v}_{c1}(s)=\frac{DD'L_T\tilde{v}_{c2}(s)+L_2D'\tilde{v}_{co}(s)+\alpha_1V_{CT}\tilde{d}(s)+sL_PI_{LT}\tilde{d}(s)+sL_PD'\tilde{i}_{in}(s)}{q_{c1}} \tag{3.26}$$

Substitute equation (3.26) into capacitor C_o and C_2 voltage of equation (3.19b) to eliminate capacitor C_1 voltage as follows:

$$\begin{aligned}
q_{c1}q_{co}v_{co}(s) &= DD'^2L_Tv_{c2}(s)+L_2D'^2v_{co}(s)+D'\alpha_1V_{CT}d(s)+sD'L_PI_{LT}d(s)\\
&\quad+sL_PD'^2i_{in}(s)-q_{c1}v_{c2}(s)D-q_{c1}d(s)V_{CT}+sq_{c1}L_1i_{inj}(s)\\
[q_{co}q_{c1}-L_2D'^2]v_{co}(s) &= (DD'^2L_T-q_{c1}D)v_{c2}(s)+(D'\alpha_1-q_{c1})V_{CT}d(s)\\
&\quad+sD'L_PI_{LT}d(s)+sL_PD'^2i_{in}(s)+sq_{c1}L_1i_{inj}(s)\\
q_{c1}q_{c2}v_{c2}(s) &= (DD'L_T)^2v_{c2}(s)+L_2L_TD'^2Dv_{co}(s)+DD'L_T\alpha_1V_{CT}d(s)\\
&\quad+sDD'L_TL_PI_{LT}d(s)+sDD'^2L_TL_Pi_{in}(s)-q_{c1}L_2Dv_{co}(s)\\
&\quad+q_{c1}\alpha_2V_{CT}d(s)+sq_{c1}L_PI_{LT}d(s)+sq_{c1}L_PD'i_{in}(s)\\
[q_{c1}q_{c2}-(DD'L_T)^2]v_{c2}(s) &= (L_2L_TD'^2D-q_{c1}L_2D)v_{co}(s)+(DD'L_T\alpha_1+q_{c1}\alpha_2)V_{CT}d(s)\\
&\quad+(DD'L_T+q_{c1})L_PI_{LT}sd(s)+(DD'L_T+q_{c1})L_PD'si_{in}(s)
\end{aligned} \tag{3.27}$$

To simplify equation (3.27), the following expressions are defined:

$$\begin{aligned} Q_{co}^{'} &= q_{c1}q_{co} - L_2 D'^2 \\ Q_{c2} &= Q_{c1} = q_{c1}q_{c2} - (DD'L_T)^2 \\ M_3 &= D'^2\, DL_T - q_{c1}D \end{aligned} \tag{3.28}$$

A simpler equation (3.27) is obtained after including the parameters from equation (3.28)

$$\begin{aligned} Q_{co}^{'} v_{co}(s) &= M_3 v_{c2}(s) + (D'\alpha_1 - q_{c1})V_{CT} d(s) + sD'L_P I_{LT} d(s) + sL_P D'^2\, i_{in}(s) \\ &\quad + sq_{c1}L_1 i_{inj}(s) \\ Q_{c2} v_{c2}(s) &= M_3 L_2 v_{co}(s) + (DD'L_T\alpha_1 + q_{c1}\alpha_2)V_{CT} d(s) + (DD'L_T + q_{c1})L_P I_{LT} sd(s) \\ &\quad + (DD'L_T + q_{c1})L_P D' s i_{in}(s) \end{aligned} \tag{3.29}$$

Capacitor C_o voltage of equation (3.29) is substituted into capacitor C_2 voltage of equation (3.29) to obtain capacitor C_2 dynamic equation given by:

$$\begin{aligned} Q_{co}^{'} Q_{c2} v_{c2}(s) &= L_2 M_3^2 v_{c2}(s) + (D'\alpha_1 - q_{c1})M_3 L_2 V_{CT} d(s) + sM_3 L_2 D' L_P I_{LT} d(s) \\ &\quad + sM_3 L_2 L_P D'^2\, i_{in}(s) + (DD'L_T\alpha_1 + q_{c1}\alpha_2)Q_{co}^{'} V_{CT} d(s) + sM_3 L_2 q_{c1} L_1 i_{inj}(s) \\ &\quad + (DD'L_T + q_{c1})Q_{co}^{'} L_P I_{LT} sd(s) + (DD'L_T + q_{c1})Q_{co}^{'} L_P D' s i_{in}(s) \\ (Q_{co}^{'} Q_{c2} - L_2 M_3^2) v_{c2}(s) &= \left[(D'\alpha_1 - q_{c1})M_3 L_2 + (DD'L_T\alpha_1 + q_{c1}\alpha_2)Q_{co}^{'}\right] V_{CT} d(s) \\ &\quad + \left[M_3 L_2 D' + (DD'L_T + q_{c1})Q_{co}^{'}\right] L_P I_{LT} sd(s) \\ &\quad + \left[M_3 L_2 D' + (DD'L_T + q_{c1})Q_{co}^{'}\right] L_P D' s i_{in}(s) + sM_3 L_2 q_{c1} L_1 i_{inj}(s) \end{aligned} \tag{3.30}$$

The transfer functions relating the inductor current to control and to the input current can also be obtained using the method of substitution starting by eliminating from the inductor equations the capacitors voltages in equation (3.15). From equation (3.15), the capacitor voltage can be written as:

$$\begin{aligned} sC_o \tilde{v}_{co}(s) &= \frac{\tilde{i}_{L1}(s)}{sC_o + \dfrac{1}{R_o}} \\ \tilde{v}_{c1}(s) &= \frac{\tilde{i}_{in}(s)D' - \tilde{i}_{L1}(s)D' + \tilde{i}_{L2}(s)D + \tilde{d}(s)I_{LT}}{sC_1} \\ \tilde{v}_{c2}(s) &= \frac{\tilde{i}_{in}(s)D' + \tilde{i}_{L1}(s)D - \tilde{i}_{L2}(s)D' + \tilde{d}(s)I_{LT}}{sC_2} \end{aligned} \tag{3.31}$$

Substitute the capacitor voltage from equation (3.31) into the inductor current in equation (3.15) to obtain:

(3.32)

$$sL_2 i_{L2}(s) = \left(\frac{i_{in}(s)D' + i_{L1}(s)D - i_{L2}(s)D' + d(s)I_{LT}}{sC_2} \right) D'$$
$$+ \left(\frac{i_{in}(s)D' - i_{L1}(s)D' + i_{L2}(s)D + d(s)I_{LT}}{sC_1} \right) D - d(s)V_{CT}$$
$$\left(s^2 L_2 C_1 C_2 + D'^2 C_1 + D^2 C_2\right) i_{L2}(s) = DD' C_T i_{L1}(s) + \left(D'^2 C_1 - D' D C_2\right) i_{in}(s)$$
$$+ \left(D' C_1 - D C_2\right) I_{LT} d(s) - sC_1 C_2 V_{CT} d(s)$$
$$sL_1 i_{L1}(s) = \left(\frac{i_{in}(s)D' - i_{L1}(s)D' + i_{L2}(s)D + d(s)I_{LT}}{sC_1} \right) D'$$
$$+ \left(\frac{i_{in}(s)D' + i_{L1}(s)D - i_{L2}(s)D' + d(s)I_{LT}}{sC_2} \right) D$$
$$- \left(\frac{i_{L1}(s)}{sC_o + \frac{1}{R_o}} \right) - d(s)V_{CT}$$
$$\left[\left(s^2 L_1 C_o + \frac{sL_1}{R_o} + 1 \right) sC_1 C_2 + \left(D'^2 C_2 + D^2 C_1\right) \left(sC_o + \frac{1}{R_o} \right) \right] i_{L1}(s) =$$
$$+ DD' C_T \left(sC_o + \frac{1}{R_o} \right) i_{L2}(s) + \left(D'^2 C_2 - D' D C_1\right) \left(sC_o + \frac{1}{R_o} \right) i_{in}(s) \qquad (3.32)$$
$$+ \left(D' C_2 - D C_1\right) \left(sC_o + \frac{1}{R_o} \right) I_{LT} d(s) - \left(sC_o + \frac{1}{R_o} \right) sC_1 C_2 V_{CT} d(s)$$

Define the following characteristic equations from equation (3.32):

$$q_{il1} = \left(s^2 L_1 C_o + \frac{sL_1}{R_o} + 1 \right) sC_1 C_2 + \left(D'^2 C_2 + D^2 C_1\right) \left(sC_o + \frac{1}{R_o} \right) \qquad (3.33)$$
$$q_{il2} = s^2 L_2 C_1 C_2 + D'^2 C_1 + D^2 C_2$$

Substitute equation (3.33) into equation (3.32) to obtain a simpler equation given by:

$$q_{il1} i_{L1}(s) = DD' C_T \left(sC_o + \frac{1}{R_o} \right) i_{L2}(s) + \left(D'^2 C_2 - D' D C_1\right) \left(sC_o + \frac{1}{R_o} \right) i_{in}(s)$$
$$+ \left(D' C_2 - D C_1\right) \left(sC_o + \frac{1}{R_o} \right) I_{LT} d(s) - \left(sC_o + \frac{1}{R_o} \right) sC_P V_{CT} d(s) \qquad (3.34)$$
$$q_{il2} i_{L2}(s) = DD' C_T i_{L1}(s) + \left(D'^2 C_1 - D' D C_2\right) i_{in}(s)$$
$$+ \left(D' C_1 - D C_2\right) I_{LT} d(s) - sC_P V_{CT} d(s)$$

Inductor L_2 current of equation (3.34) is substituted into inductor L_1 current of equation (3.34) to obtain inductor L_1 dynamic equation given by:

$$
\begin{aligned}
&q_{il1}q_{il2}i_{L1}(s) = (DD'C_T)\left(sC_o + \frac{1}{R_o}\right)(D'^2C_1 - D'DC_2)i_{in}(s) \\
&+ (DD'C_T)^2\left(sC_o + \frac{1}{R_o}\right)i_{L1}(s) + (DD'C_T)\left(sC_o + \frac{1}{R_o}\right)(D'C_1 - DC_2)I_{LT}d(s) \\
&- (DD'C_T)\left(sC_o + \frac{1}{R_o}\right)sC_PV_{CT}d(s) + q_{il2}(D'^2C_2 - D'DC_1)\left(sC_o + \frac{1}{R_o}\right)i_{in}(s) \\
&+ q_{il2}(D'C_2 - DC_1)\left(sC_o + \frac{1}{R_o}\right)I_{LT}d(s) - q_{il2}\left(sC_o + \frac{1}{R_o}\right)sC_PV_{CT}d(s) \\
&\left[q_{il1}q_{il2} - (DD'C_T)^2\left(sC_o + \frac{1}{R_o}\right)\right]i_{L1}(s) = \\
&+ \left[(DD'C_T)\left(sC_o + \frac{1}{R_o}\right)(D'C_1 - DC_2) + q_{il2}(D'C_2 - DC_1)\left(sC_o + \frac{1}{R_o}\right)\right]I_{LT}d(s) \\
&- \left[(DD'C_T)\left(sC_o + \frac{1}{R_o}\right) + q_{il2}\left(sC_o + \frac{1}{R_o}\right)\right]sC_PV_{CT}d(s) \\
&+ \left[(DD'C_T)\left(sC_o + \frac{1}{R_o}\right)(D'^2C_1 - D'DC_2) + + q_{il2}(D'^2C_2 - D'DC_1)\left(sC_o + \frac{1}{R_o}\right)\right]i_{in}(s)
\end{aligned}
\tag{3.35}
$$

Inductor L_1 current of equation (3.34) is substituted into inductor L_2 current of equation (3.34) to obtain inductor L_2 dynamic equation given by:

$$
\begin{aligned}
&q_{il1}q_{il2}i_{L2}(s) = DD'C_T(D'^2C_2 - D'DC_1)\left(sC_o + \frac{1}{R_o}\right)i_{in}(s) \\
&+ (DD'C_T)^2\left(sC_o + \frac{1}{R_o}\right)i_{L2}(s) + DD'C_T(D'C_2 - DC_1)\left(sC_o + \frac{1}{R_o}\right)I_{LT}d(s) \\
&- DD'C_T\left(sC_o + \frac{1}{R_o}\right)sC_PV_{CT}d(s) + q_{il1}(D'^2C_1 - D'DC_2)i_{in}(s) \\
&+ q_{il1}(D'C_1 - DC_2)I_{LT}d(s) - sq_{il1}C_PV_{CT}d(s)
\end{aligned}
\tag{3.36}
$$

$$\begin{aligned}
&\left[q_{il1}q_{il2}-\left(DD'C_T\right)^2\left(sC_o+\frac{1}{R_o}\right)\right]i_{L1}(s)= \\
&+\left[DD'C_T\left(D'C_2-DC_1\right)\left(sC_o+\frac{1}{R_o}\right)+q_{il1}\left(D'C_1-DC_2\right)\right]I_{LT}d(s) \\
&-\left[DD'C_T\left(sC_o+\frac{1}{R_o}\right)+q_{il1}\right]sC_PV_{CT}d(s) \\
&+\left[DD'C_T\left(D'^2C_2-D'DC_1\right)\left(sC_o+\frac{1}{R_o}\right)++q_{il1}\left(D'^2C_1-D'DC_2\right)\right]i_{in}(s)
\end{aligned} \tag{3.36}$$

The transfer functions that were derived by solving the converter equation (3.15) are summarised as follow:

From equation (3.24b) the transfer function relating the output capacitor voltage to control is given by:

$$\begin{aligned}
G_{vd}&=\frac{\tilde{v}_{co}(s)}{\tilde{d}(s)}\Big|_{in(s)=0} \\
&=\frac{\left[M_1\left(DD'L_T\alpha_2+q_{c2}\alpha_1\right)-Q_{c1}\left(q_{c2}+D\alpha_2\right)\right]V_{CT}+\left[M_1\left(DD'L_T+q_{c2}\right)-Q_{c1}D\right]L_PI_{LT}s}{Q_{co}Q_{c1}-M_1M_2}
\end{aligned} \tag{3.37a}$$

From equation (3.24b) the transfer function relating the output voltage ripple to the quasi-Z-source circuit input current ripple (current susceptibility) is given by:

$$\begin{aligned}
G_{vg}&=\frac{\tilde{v}_{co}(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0} \\
&=\frac{\left[M_1\left(DD'L_T+q_{c2}\right)-Q_{c1}D\right]L_PD's}{Q_{co}Q_{c1}-M_1M_2}
\end{aligned} \tag{3.37b}$$

From equation (3.24b) the transfer function relating the output voltage ripple to the injected current ripple (output impedance) is given by:

$$\begin{aligned}
Z_{out}(s)&=-\frac{\tilde{v}_{co}(s)}{\tilde{i}_{inj}(s)}\Big|_{\tilde{d}(s)=0} \\
&=\frac{-sQ_{c1}q_{c2}L_1}{Q_{co}Q_{c1}-M_1M_2}
\end{aligned} \tag{3.37c}$$

From equation (3.24a) the transfer function relating the input current ripple to the input voltage ripple of the quasi-Z-circuit (input admittance) with the output short circuited is given by:

$$Y_{in}(s)=\frac{\tilde{i}_{in}(s)}{\tilde{v}_{in}(s)}\Big|_{\tilde{v}_{out}(s)=0}$$
$$=\frac{Q_{c1a}\left[q_{c2a}D'-\left(L_2DD'-L_1D'^2\right)\right]-D'L_1\left[L_2D'\left(L_2DD'-L_1D'^2\right)+q_{c2a}\left(L_1DD'-L_2D'^2\right)\right]}{\left[sQ_{c1a}L_PD'+D'L_1\left(sL_2L_PD'^2+sq_{c2a}L_PD'\right)\right]} \quad (3.37d)$$

From equation (3.25) the transfer function relating the quasi-Z-source circuit capacitor C_1 voltage to control is given by:

$$G_{vd}=\frac{\tilde{v}_{c1}(s)}{\tilde{d}(s)}\Big|_{\tilde{i}n(s)=0}$$
$$=\frac{\left[Q_{co}\left(DD'L_T\alpha_2+q_{c2}\alpha_1\right)-M_2\left(q_{c2}+D\alpha_2\right)\right]V_{CT}+\left[Q_{co}\left(DD'L_T+q_{c2}\right)-M_2D\right]L_PI_{LT}s}{Q_{co}Q_{c1}-M_1M_2} \quad (3.38a)$$

From equation (3.25) the transfer function relating the quasi-Z-source circuit capacitor C_1 voltage to the quasi-Z-source circuit input current is given by:

$$G_{vg}=\frac{\tilde{v}_{c1}(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0}$$
$$=\frac{\left[Q_{co}\left(DD'L_T+q_{c2}\right)-M_2D\right]L_PD's}{Q_{co}Q_{c1}-M_1M_2} \quad (3.38b)$$

From equation (3.30) the transfer function relating the quasi-Z-source circuit capacitor C_2 voltage to control is given by:

$$G_{vd}=\frac{\tilde{v}_{c2}(s)}{\tilde{d}(s)}\Big|_{\tilde{i}n(s)=0}$$
$$=\frac{\left[M_3L_2\left(D'\alpha_1-q_{c1}\right)+Q_{co}''\left(DD'L_T\alpha_1+q_{c1}\alpha_2\right)\right]V_{CT}}{Q_{co}''Q_{c1}-L_2M_3^2}$$
$$+\frac{\left[M_3L_2D'+Q_{co}\left(DD'L_T+q_{c1}\right)\right]L_PI_{LT}s}{Q_{co}''Q_{c1}-L_2M_3^2} \quad (3.39a)$$

From equation (3.30) the transfer function relating the quasi-Z-source capacitor C_2 voltage to the quasi-Z-source circuit input current is given by:

$$G_{vg}=\frac{\tilde{v}_{c2}(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0}$$
$$=\frac{\left[M_3L_2D'+Q_{co}\left(DD'L_T+q_{c1}\right)\right]L_PD's}{Q_{co}''Q_{c1}-L_2M_3^2} \quad (3.39b)$$

From equation (3.35) the transfer function relating the quasi-Z-source circuit inductor L_1 current to control is given by:

$$G_{id} = \frac{\tilde{i}_{L1}(s)}{\tilde{d}(s)}\Big|_{\tilde{i}n(s)=0}$$

$$= \frac{I_{LT}\left(sC_o + \frac{1}{R_o}\right)\left[DD'C_T\left(D'C_1 - DC_2\right) + q_{il2}\left(D'C_2 - DC_1\right)\right]}{\left[q_{il1}q_{il2} - \left(DD'C_T\right)^2\left(sC_o + \frac{1}{R_o}\right)\right]} \qquad (3.40a)$$

$$\frac{-sC_P V_{CT}\left(sC_o + \frac{1}{R_o}\right)\left[DD'C_T + q_{il2}\right]}{\left[q_{il1}q_{il2} - \left(DD'C_T\right)^2\left(sC_o + \frac{1}{R_o}\right)\right]}$$

From equation (3.35) the transfer function relating the quasi-Z-source circuit inductor L_1 current to the quasi-Z-source circuit input current is given by:

$$G_{ig} = \frac{\tilde{i}_{L1}(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0}$$

$$= \frac{\left(sC_o + \frac{1}{R_o}\right)\left[DD'C_T\left(D'^2\,C_1 - D'DC_2\right) + q_{il2}\left(D'^2\,C_2 - D'DC_1\right)\right]}{\left[q_{il1}q_{il2} - \left(DD'C_T\right)^2\left(sC_o + \frac{1}{R_o}\right)\right]} \qquad (3.40b)$$

From equation (3.36) the transfer function relating the quasi-Z-source circuit inductor L_2 current to control is given by:

$$G_{id} = \frac{\tilde{i}_{L2}(s)}{\tilde{d}(s)}\Big|_{\tilde{i}n(s)=0}$$

$$= \frac{\left[DD'C_T\left(D'C_2 - DC_1\right)\left(sC_o + \frac{1}{R_o}\right) + q_{il1}\left(D'C_1 - DC_2\right)\right]I_{LT}}{\left[q_{il1}q_{il2} - \left(DD'C_T\right)^2\left(sC_o + \frac{1}{R_o}\right)\right]} \qquad (3.41a)$$

$$\frac{-\left[DD'C_T\left(sC_o + \frac{1}{R_o}\right) + q_{il1}\right]sC_P V_{CT}}{\left[q_{il1}q_{il2} - \left(DD'C_T\right)^2\left(sC_o + \frac{1}{R_o}\right)\right]}$$

From equation (3.36) the transfer function relating the quasi-Z-source inductor L_2 current to the quasi-Z-source circuit input current is given by:

$$G_{ig} = \frac{\tilde{i}_{L2}(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0}$$
$$= \frac{\left[DD'C_T\left(D'^2 C_2 - DD'C_1\right)\left(sC_o + \frac{1}{R_o}\right) + q_{il1}\left(D'^2 C_1 - D'DC_2\right)\right]}{\left[q_{il1}q_{il2} - \left(DD'C_T\right)^2\left(sC_o + \frac{1}{R_o}\right)\right]} \quad (3.41b)$$

To complete the model of the quasi-Z-source three-phase rectifier, the quasi-Z-source circuit DC side dynamic equations that were derived are combined with the dynamic model of the full-bridge AC side as follows:

The synchronous frame model of the three-phase full-bridge PWM rectifier is given by [6]:

$$L_s\frac{di_{Lsd}}{dt} = v_{sd} - Ri_d - wL_s i_q - d_d v_{in}$$
$$L_s\frac{di_{Lsq}}{dt} = v_{sq} - Ri_q + wL_s i_d - d_q v_{in} \quad (3.42)$$

In the QZSR it was found from equation (3.7) that $V_{co} = V_{in}(1-2d)$.

Then the input voltage of the QZSR can be expressed as:

$$V_{in} = \frac{V_{co}}{(1-2d)} \quad (3.43)$$

Substituting equation (3.43) into (3.42), the synchronous frame equations become:

$$L_s\frac{di_{Lsd}}{dt} = v_{sd} - Ri_d - wL_s i_q - d_d\frac{v_{co}}{(1-2d)}$$
$$L_s\frac{di_{Lsq}}{dt} = v_{sq} - Ri_q + wL_s i_d - d_q\frac{v_{co}}{(1-2d)} \quad (3.44)$$

From equation (3.14) the variations of the output voltage depend on the respective variations of the input current of the rectifier and the shoot-through duty ratio. The synchronous frame model of the three-phase full-bridge PWM rectifier and the dynamic equations of the quasi-Z-source circuit are then combined to draw in Figure 3.4 the block diagram of the model that was developed and expressed by equation (3.45c).

$$G_3(s)v_{co}(s) = G_2(s)d(s) + G_1(s)i_{in}(s), \text{ where } i_{in}(s) = (1-d)i_s \quad (3.45a)$$

From the axes transformations the input AC current is given by:

$$i_s = \frac{3}{2}\left(d_q i_q + d_d i_d\right) \tag{3.45b}$$

The overall block diagram representation is then given by:

$$G_3(s)v_{co}(s) = G_2(s)d(s) + \frac{3}{2}(1-d)G_1(s)\left(d_q i_q + d_d i_d\right) \tag{3.45c}$$

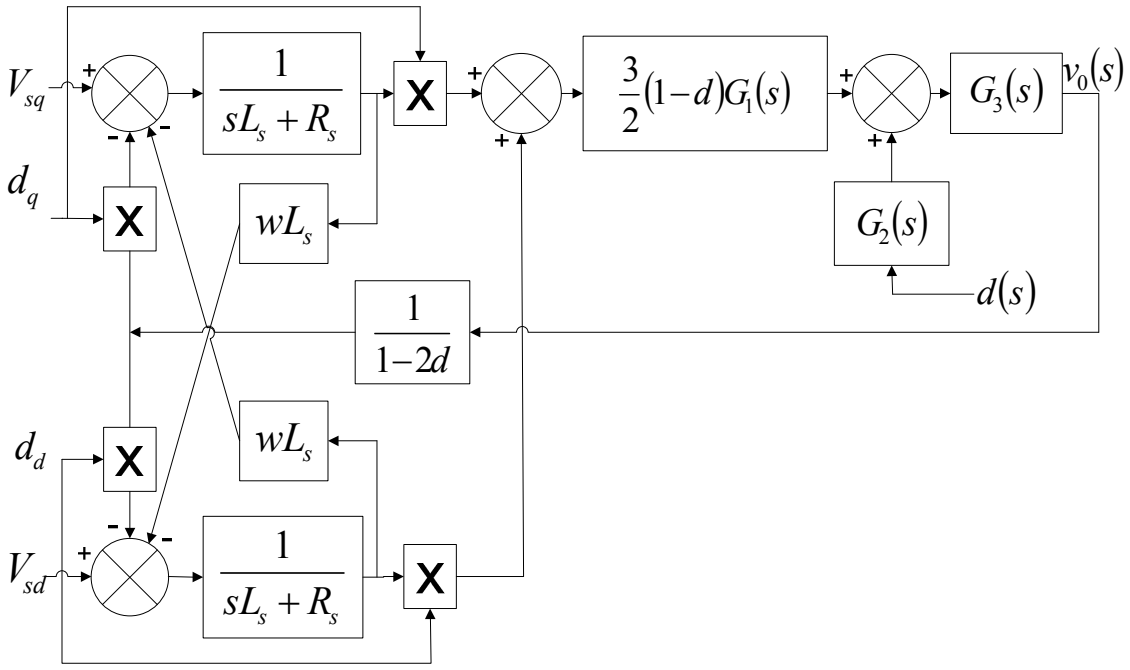

Figure 3.4. Diagram of the model Structure

With:

$$G_1(s) = \left[M_1\left(DD'L_T + q_{c2}\right) - Q_{c1}D\right]L_P D's \tag{3.46}$$

$$\begin{aligned} G_2(s) = {} & \left[M_1\left(DD'L_T\alpha_2 + q_{c2}\alpha_1\right) - Q_{c1}\left(q_{c2} + D\alpha_2\right)\right]V_{CT} \\ & + \left[M_1\left(DD'L_T + q_{c2}\right) - Q_{c1}D\right]L_P I_{LT}s \end{aligned} \tag{3.47}$$

$$G_3(s) = Q_{co}Q_{c1} - M_1M_2 \tag{3.48}$$

The block diagram representation of the QZSR in Figure 3.4 can be used to design a closed-loop controller to regulate the output DC voltage and to obtain a low harmonic AC input current in phase with the AC voltage.

During the interval where the peak input AC voltage is less than twice the desired DC output voltage, boosting action is required from the rectifier. During such intervals, the shoot-through duty cycle is set to zero and the quasi-Z-source circuit switch remains on for

the entire switching period. The QZSR then operates similarly to a conventional voltage source PWM rectifier. The equivalent quasi-Z-source circuit model during this interval is Figure 3.1 and equation (3.1). The capacitors DC voltage and inductors DC current are obtained by setting D = 0 in equation (3.7) and are given by:

$$\begin{aligned} V_{c1} &= V_{in} = V_{co} \\ V_{c2} &= 0 \\ I_{L1,av} &= I_{L2,av} = I_{in,av} = I_{o,av} \end{aligned} \tag{3.49}$$

3.3.1 Dynamic model analysis

Bode plots of the transfer functions that were derived from equation (3.37) to equation (3.41) are obtained using Matlab software. The converter parameters used for the plots are given in Table 3.1. These parameters were chosen from many considerations such as satisfactory ripple performance and small physical size, proper quality factor and damping factor, resonant frequency far away from the quasi-Z-source circuit switching frequency for stability. The ripple performance is set to a maximum of 0.2 % of the steady state capacitor voltage and a maximum of 8 % of the steady state inductor current. An input three-phase voltage of 70 V to 100 V is used to verify the performance of the rectifier. The output DC voltage is set to 150 V and the diagram in Figure 3.5 shows the region of operations of the rectifier based on equation (3.10) using the chosen AC input voltage and DC output voltage. For AC input voltage of the rectifier larger than 90 V, bucking action is needed in the quasi-Z-source circuit to maintain the DC voltage at 150 V. The bode plot responses are shown from Figures 3.6 to 3.24.

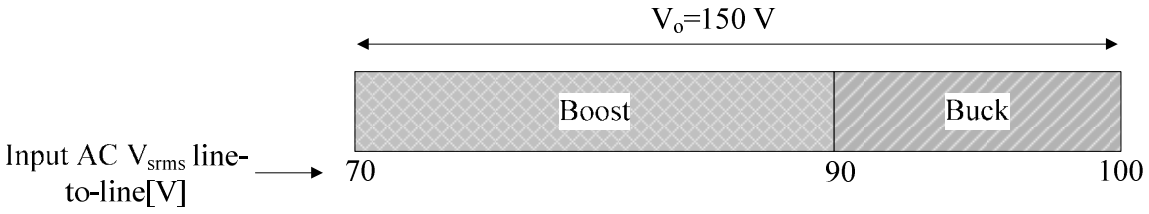

Figure 3.5. QZSR boost and buck interval

Table 3.1. Converter Parameters

Parameters	**Value**
Input Voltage, V_{srms} (line-to-line)	100 V
Input Resistance R_s	1.5 Ω
Input Inductance L_s	1400 μH
Output Voltage, V_o	150 V
Load Resistance, R_o	21.5 Ω
Output capacitor C_o	5.4 μF
Quasi-Z-source circuit capacitor C_1	17.2 μF
Quasi-Z-source circuit capacitor C_2	60.0 μF
Quasi-Z-source circuit Inductor L	900 μH
Switching Frequency, f_s	40 kHz

The bode plots shown in Figures 3.6 and 3.7 confirms that as the input AC voltage changes, the magnitude and phase variations are negligible. For frequencies above 1 kHz the magnitude and phase values are identical for each AC input voltage. The resonance frequencies vary between 600 Hz and 700 Hz for all AC input voltages but the resonance magnitude increases as the AC input voltage decreases. The bode plots are therefore comparable in terms of magnitude and phase irrespective of the AC input voltage. The conclusions of the dynamic analysis at one of the AC input voltages can be generalised to other AC input voltages without significant deviations. Four essential transfer functions are used to analyse the dynamic performance of the quasi-Z-circuit: the transfer function relating the output capacitor voltage to control, the transfer function relating the output voltage ripple to the quasi-Z-circuit input current ripple (Current susceptibility), the output impedance for output performance, and the input admittance for input performance.

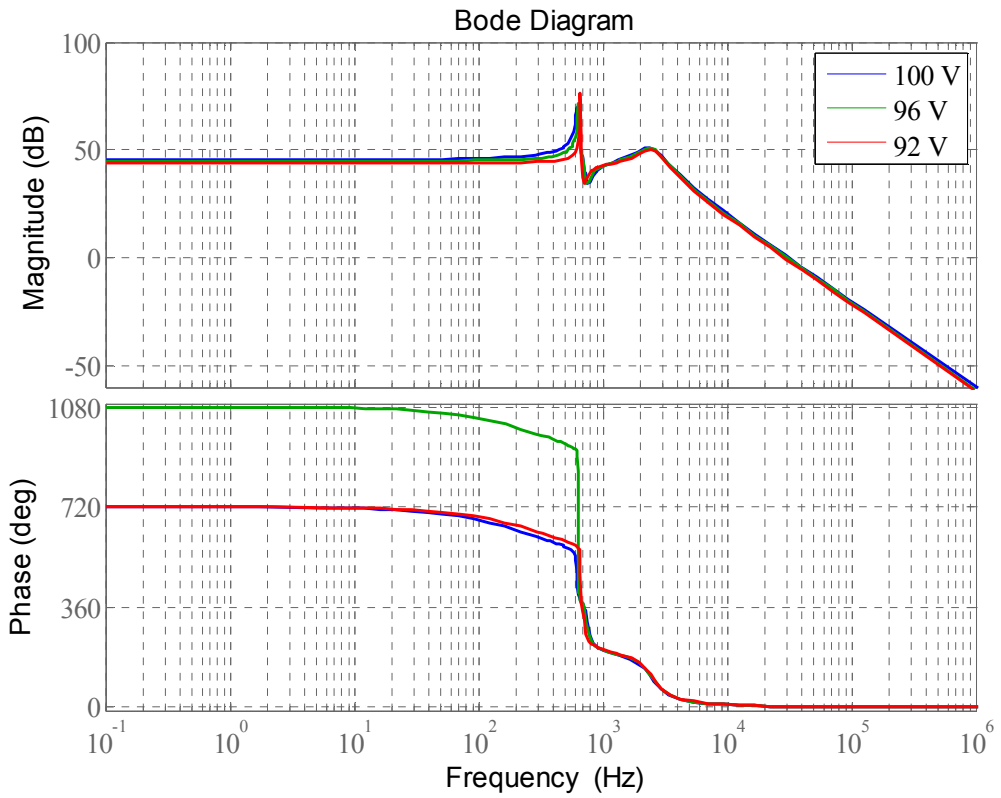

Figure 3.6. Bode plot of the transfer function relating the output voltage to control with variations of the AC input line-to-line voltage

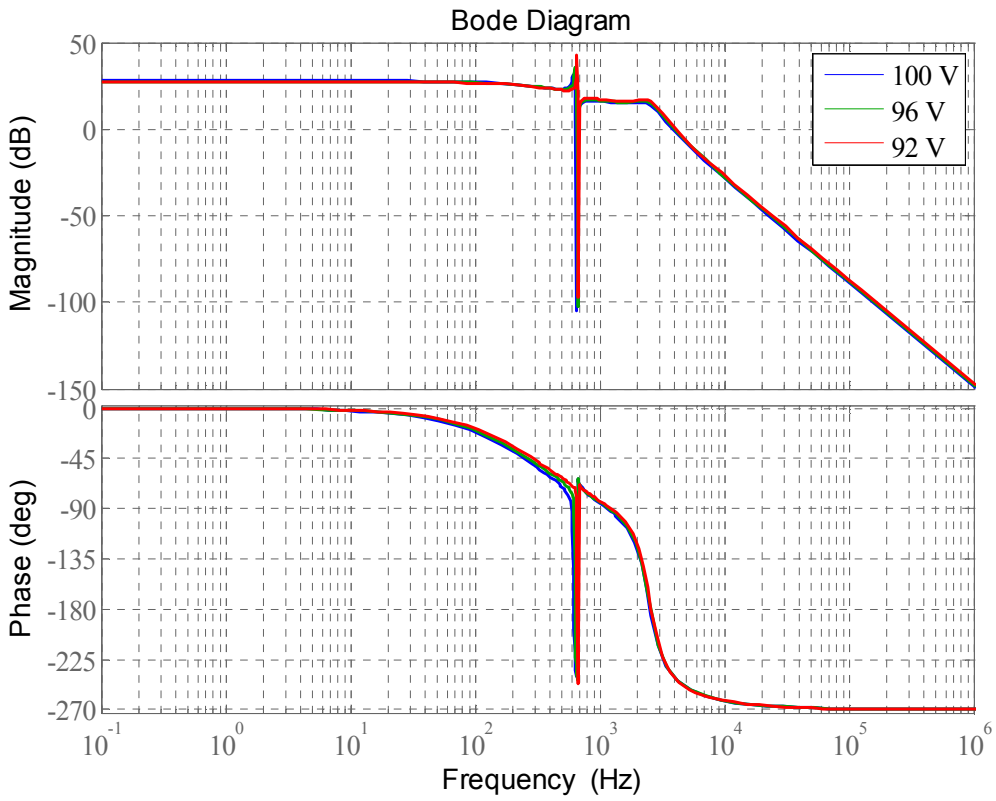

Figure 3.7. Bode plot of the transfer function relating the output voltage ripple to the quasi-Z-source circuit input current ripple with variations of AC input line-to-line voltage

The transfer function relating the output capacitor voltage to control is given in equation (3.50) after substituting the parameters of Table 3.1. This transfer function describes how control input variations influence the output voltage and is a key component of the loop gain in an output voltage regulator design [13]. Ideally a flat and high gain is desired in low frequencies to limit the controller gain to low values [2] [13] [40]. However at high frequencies the ideal desired response should have the lowest possible gain and a high decade rate to prevent noises reaching the output [2] [13] [40]. The DC gain at low frequency is given by the steady state equation of the converter. Resonance on the bode plot is undesirable because the abrupt amplitude and phase change may stress components beyond their voltage limits [13] [40]. Bode plot and pole-zero map are shown in Figures 3.8 and 3.9 respectively.

$$
\begin{aligned}
G_{vd} &= \frac{\tilde{v}_{co}(s)}{\tilde{d}(s)}\Big|_{\tilde{i}\tilde{n}(s)=0} \\
&= \frac{N_1 + N_2}{D_1 + D_2} \\
N_1 &= -6.283\times10^{-30}s^6 + 1.156\times10^{-26}s^5 - 2.41\times10^{-22}s^4 \\
N_2 &= 3.684\times10^{-19}s^3 - 2.201\times10^{-15}s^2 + 2.924\times10^{-12}s + 9.84\times10^{-24} \\
D_1 &= 1.604\times10^{-40}s^8 + 1.382\times10^{-36}s^7 + 4.622\times10^{-32}s^6 + 1.138\times10^{-28}s^5 \\
D_2 &= 1.287\times10^{-24}s^4 + 2.42\times10^{-21}s^3 + 9.454\times10^{-18}s^2 + 1.536\times10^{-14}s + 5.17\times10^{-26}
\end{aligned}
\tag{3.50}
$$

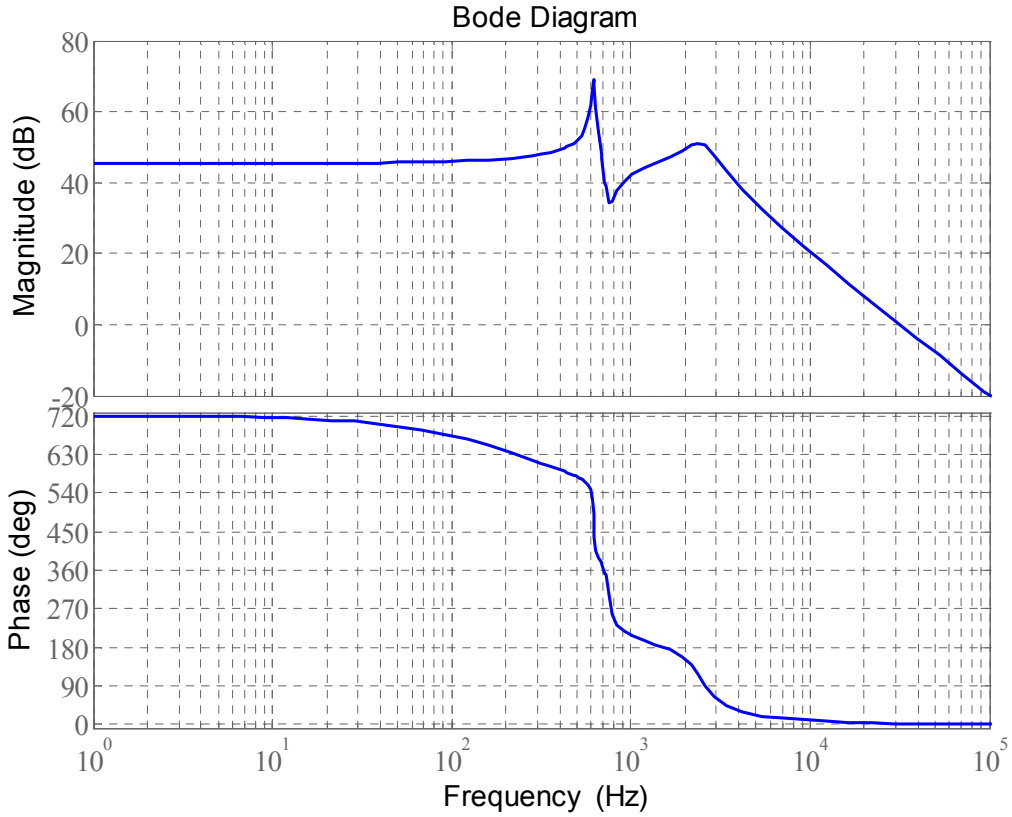

Figure 3.8. Bode plot of the transfer function relating the output voltage to control

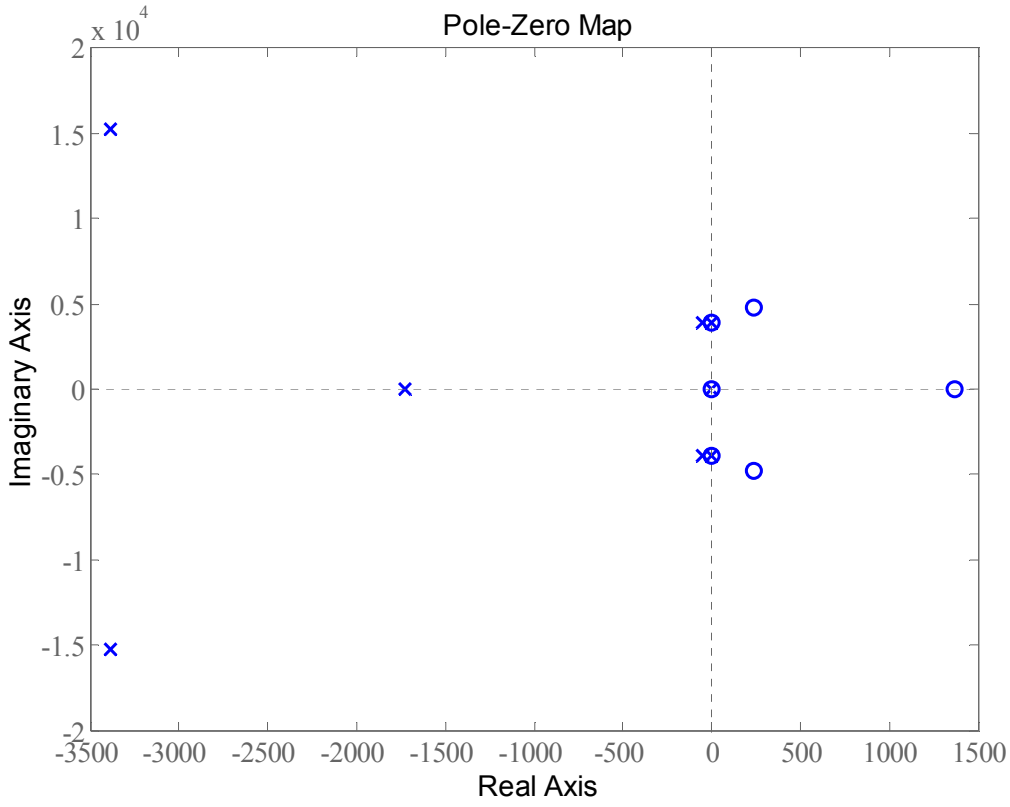

Figure 3.9. Pole-zero map of the transfer function relating the output voltage ripple to the quasi-Z-source circuit input current ripple

The real RHP zero at 217 Hz and the real LHP pole at 274 Hz cause the phase in Figure 3.8 to roll down from 720 to 540, while the magnitude (gain) remains flat as the magnitude contribution of the zero and the pole cancel each other. The complex pole on the imaginary axis at 616 Hz and the complex zero on the imaginary axis at 616 Hz cancel each other in their contribution to the magnitude, but add up in phase to cause the sharp 360 degree drop. Resonance occurs at 617 Hz due to the complex pole at 619 Hz which introduces -40 dB/decade slope and a phase roll down of -180 degree. The complex pair of RHP zeros at 759 Hz causes the notch in the magnitude plot due to the introduction of 40 dB/decade that tends to cancel the magnitude contribution of the pole at 619 Hz. The complex pair of RHP zeros at 759 Hz result in an additional phase roll down of -180 degree. The high frequency complex pair of LHP poles at 2.49 Khz introduces -40 dB/decade and an additional -180 degree phase roll down that results in a net high frequency gain slope of -40 dB/decade, and a phase of 0 degree.

Similar to fourth-order and higher order converters [40], the transfer function relating the output capacitor voltage to control contains RHP zeros comparable to the ZSR in [6]. The presence of these RHP zeros tends to destabilize the wide-bandwidth feedback loop and impose a maximum control bandwidth to the frequency of the RHP zero [40] [42] [43]. In a typical voltage mode control the output voltage response during control variations will exhibits a non-minimum phase effect as shown in the step response of Figure 3.10. This non-minimum phase effect caused by the RHP zero is undesirable because it slows down the converter response [13]. Furthermore the complex RHP zeros at 759 Hz produce the second inverse response in Figure 3.10 which could be detrimental to the physical system [48]. Multiple-loop inner-current-control-based scheme can be considered to design fast inner-loop current not limited by the RHP zero location [49], and achieve an overall satisfactory response.

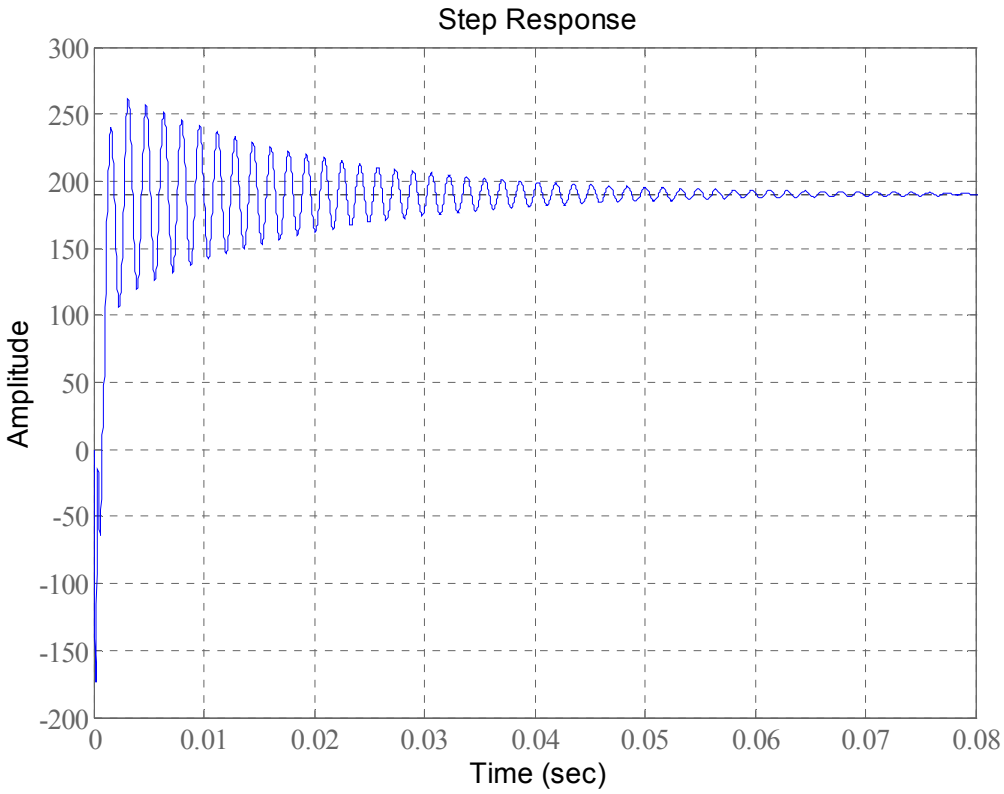

Figure 3.10. Step response of the transfer function relating the output voltage to control

Based on the bode plot response of Figure 3.8, a relatively flat response is observed in the low frequency region up to 100 Hz with a high gain of 46 dB and phase of 0 degree. The high frequency decade rate is at -40 dB/decade with a large negative phase caused by the zeros and poles of the transfer function. This is satisfactory for achieving noise suppression and to maintain higher stability at high frequencies. An ideal transient response in a converter should be overdamped without oscillation and with minimal settling time [2]. Oscillations observed in Figure 3.10 are related to the resonance frequency on the bode plot and are largely contributed by the dominant complex poles close to the imaginary axis. This underdamped nature of the transfer function relating the output voltage to control is a limiting factor on performance of the converter.

The transfer function relating the output voltage ripple to the quasi-Z-source circuit input current ripple (current susceptibility) is given in equation (3.51) after substituting the parameters of Table 3.1. This transfer function describes how variations or disturbances in input current affect the output voltage [13]. Ideally the bode plot response of this transfer function should have a very low magnitude and a high decade rate in the high frequency region where harmonics are expected [13] [40]. This is desired because the disturbances from input current harmonics should not lead to disturbances in the output voltage. Bode plot and the pole-zero map are shown in Figures 3.11 and 3.12 respectively

$$G_{vg} = \frac{\tilde{v}_{co}(s)}{\tilde{i}_{in}(s)}\Big|_{\tilde{d}(s)=0}$$
$$= \frac{1.482\times10^{-27}s^5 + 4.721\times10^{-20}s^3 + 3.747\times10^{-13}s}{D_1 + D_2} \quad (3.51)$$
$$D_1 = 1.604\times10^{-40}s^8 + 1.382\times10^{-36}s^7 + 4.622\times10^{-32}s^6 + 1.138\times10^{-28}s^5$$
$$D_2 = 1.287\times10^{-24}s^4 + 2.42\times10^{-21}s^3 + 9.454\times10^{-18}s^2 + 1.536\times10^{-14}s + 5.17\times10^{-26}$$

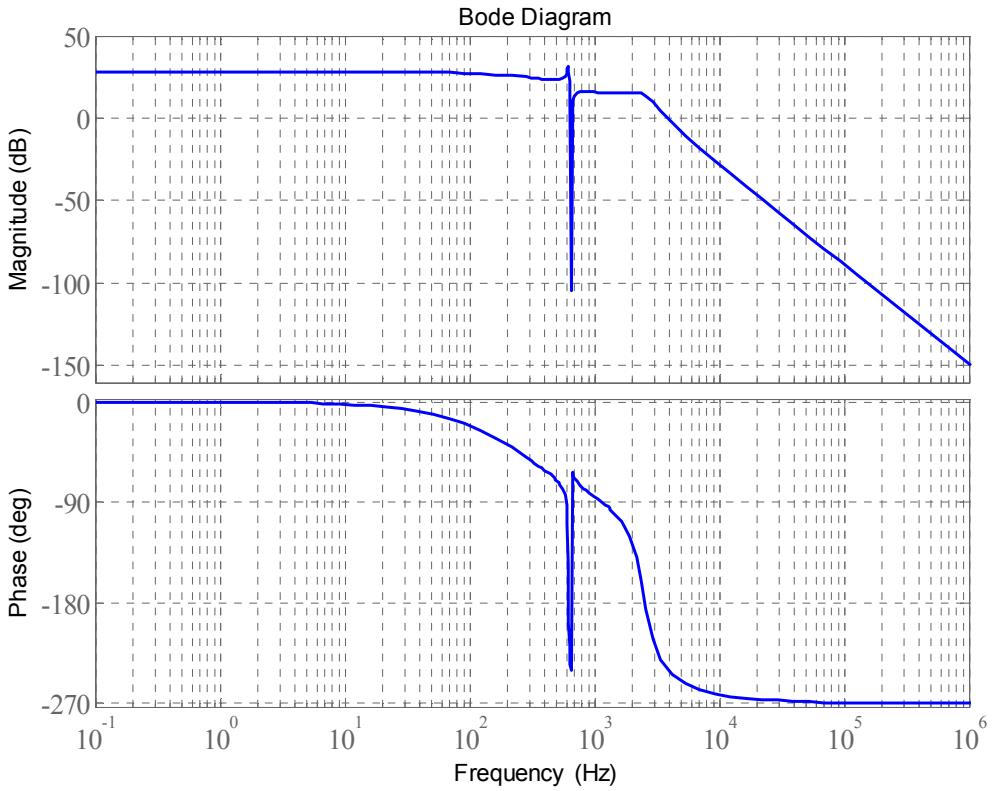

Figure 3.11. Bode plot of the transfer function relating the output voltage ripple to the quasi-Z-source circuit input current ripple

From Figure 3.12 the transfer function relating the output voltage ripple to the quasi-Z-source circuit input current ripple contains 2 pair of complex zeros on the imaginary axis at 616 Hz and 654 Hz, a zero at the origin and identical poles as the transfer function relating the output voltage to control. At the real pole frequency of 274 Hz the slope of the magnitude tends to change to -20 dB/decade and the phase drops by -45 degree. The contribution of the complex zeros at 616 Hz and the complex poles and 616 Hz merely cancel each other on the magnitude bode plot in Figure 3.11. The sharp notch on the magnitude plot and the sharp phase increase is caused by the zero on the imaginary axis at the frequency of 654 Hz. The slope and phase contribution of the zero at 654 Hz is cancelled by the complex pole at 619 Hz. At the last complex pole frequency of 2.49 kHz the magnitude slope changes to -60 dB/decade and the phase further rolls down by 180 degree. The presence of poles in the vicinity of the imaginary axis suggests that oscillations of the voltage can be expected if current ripple reaches the output. The zeros on the

imaginary axis translate to dips in the output voltage if input current ripple affect the output [48] [41] [50].

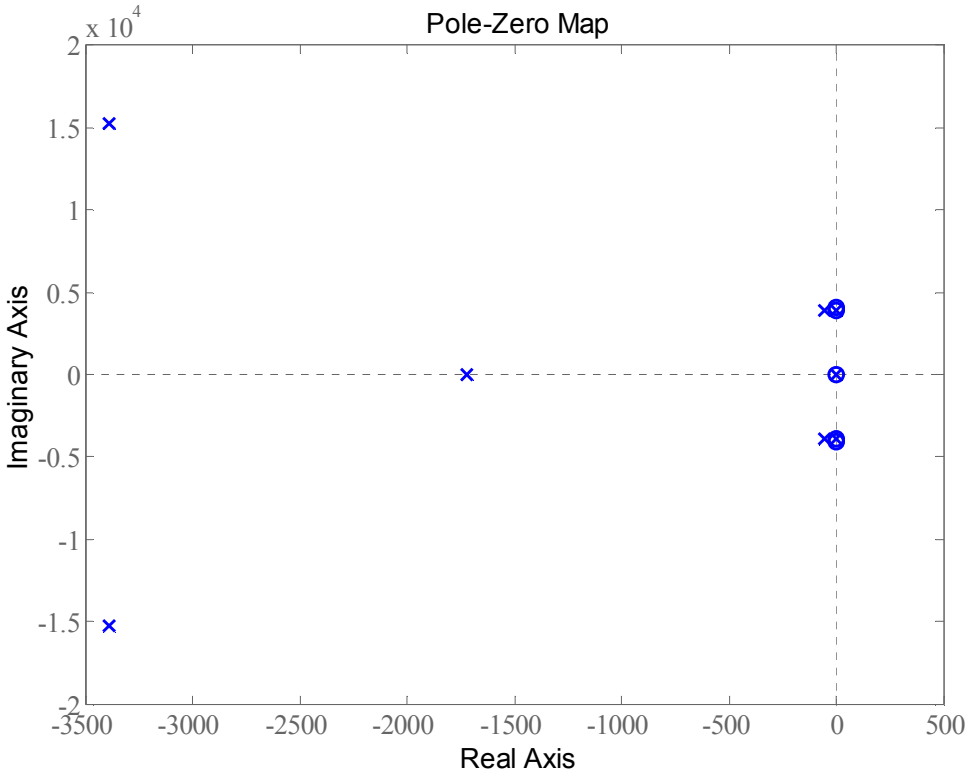

Figure 3.12. Pole-zero map of the transfer function relating the output voltage ripple to the quasi-Z-source circuit input current ripple

From the bode plot response of Figure 3.11, a relatively flat response is observed in the low frequency region up to 100 Hz with a high gain of 27 dB and phase of 0 degree. As the frequency is increased from 4 kHz, the magnitude is below 0 dB and a decade rate of -60 dB per decade is produced by the converter. Given the high switching frequency of 40 kHz of the quasi-Z-source circuit and the expected current ripple at higher frequency, the converter response from the bode plot is very satisfactory in attenuating input current ripple and achieving low input current ripple transmission. The high decade rate ensures that the output voltage is not sensitive to any input current ripple. It is also observed from the bode plot that the converter exhibit resonance at an input current with frequency of 587 Hz. However this resonant frequency is much lower than the expected current ripple frequency of the converter.

The output performance of the quasi-Z-source circuit can be assessed using the output impedance transfer function of equation (3.37c). The output impedance describes how variations in the load current affect the output voltage [13]. Therefore low output impedance is ideally desired to achieve constant output voltage regulation in presence of output current ripple [13]. Using the converter parameters of Table 3.1 in equation (3.37c), the output impedance bode plot in Figure 3.13 is obtained from the expression given by:

$$Z_{out}(s) = -\frac{\tilde{v}_{co}(s)}{\tilde{i}_{inj}(s)}\Big|_{\tilde{d}(s)=0}$$
$$= \frac{-2.971\times10^{-35}s^7 - 2.446\times10^{-27}s^5 - 5.202\times10^{-20}s^3 - 3.303\times10^{-13}s}{D_1 + D_2} \quad (3.52)$$
$$D_1 = 1.604\times10^{-40}s^8 + 1.382\times10^{-36}s^7 + 4.622\times10^{-32}s^6 + 1.138\times10^{-28}s^5$$
$$D_2 = 1.287\times10^{-24}s^4 + 2.42\times10^{-21}s^3 + 9.454\times10^{-18}s^2 + 1.536\times10^{-14}s + 5.17\times10^{-26}$$

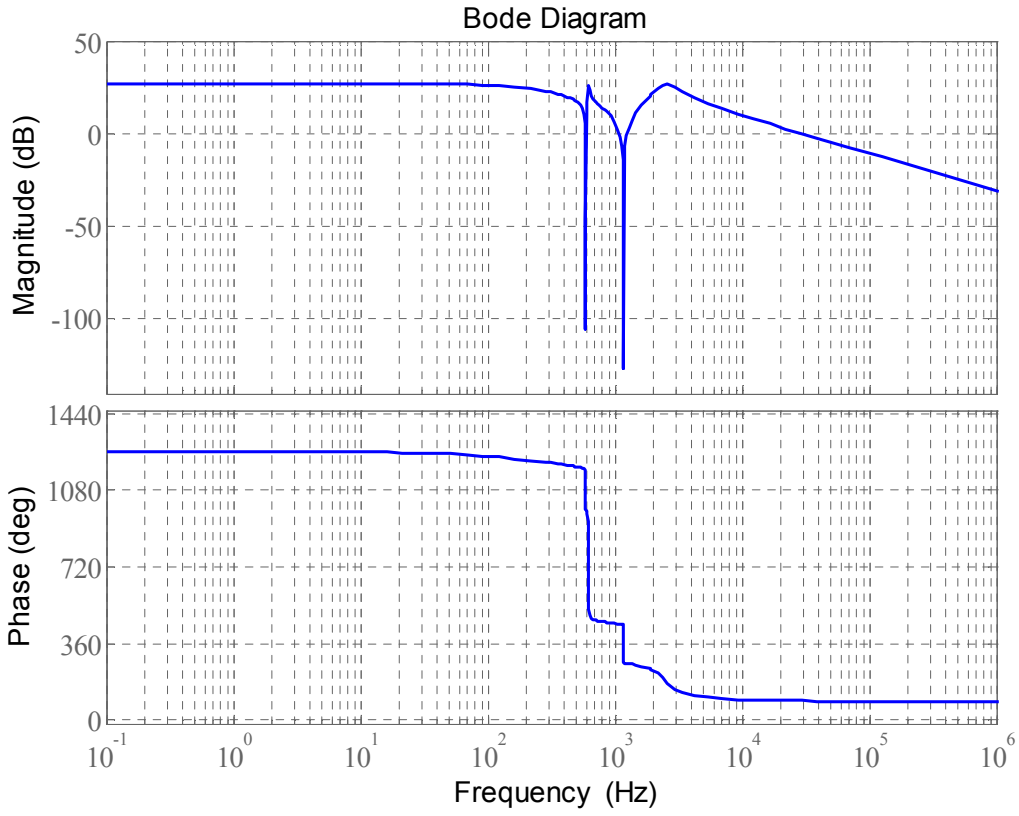

Figure 3.13. Bode plot of the transfer function of the output impedance of the Quasi-Z-circuit

Bode plot of the output impedance in Figure 3.13 shows a flat response in the low frequencies region below 100 Hz and very low output impedance magnitude below 0 dB in the high frequency region of the plot from 30 kHz. The output impedance rolls down at -20 dB/decade in the high frequency region. The output performance of the converter is satisfactory given that it behaves as an effective first order filter to high frequency output current ripple. As a result of the low output impedance the output voltage is appreciably well regulated and constant in the presence of output current variations. An abrupt drop in impedance magnitude is observed at 593 Hz and 1.16 kHz which translates to the converter shorting any current injected at that frequency.

The input performance of the quasi-Z-circuit is analysed using the transfer function of the input admittance in equation (3.37d). The input admittance specifies the performance of the converter interaction with external systems such as a voltage source or EMI input filter [13]. For instance, the relative magnitude of the input admittance and the EMI filter output impedance influence if the EMI filter disrupts the transfer function G_{vd} [13]. Ideally a very low input admittance is desired to ensure that the converter has minimal influence on the performance of the source connected [40]. Such ideal input admittance translates to low harmonic current generated by the converter. Using the converter parameters of Table 3.1 in equation (3.37d), the input admittance is given by:

$$\begin{aligned} Y_{in}(s) &= \frac{\tilde{i}_{in}(s)}{\tilde{v}_{in}(s)}\Big|_{\tilde{v}_{out}(s)=0} \\ &= \frac{2.951\times10^{-32}s^6 + 7.477\times10^{-25}s^4 + 1.352\times10^{-18}s^2}{4.911\times10^{-28}s^5 + 3.269\times10^{-20}s^3 + 6.215\times10^{-14}s} \end{aligned} \tag{3.53}$$

The input performance of the Quasi-Z-circuit is acceptable based on the bode plot in Figure 3.14. Low input admittance magnitude up to the frequency region below 7 kHz is observed from the plot. The low admittance in the low frequency region ensures that the QZSR does not negatively impact energy transfer from the supply. However at higher frequency the input admittance increases at 20dB/decade due to the admittance transfer function containing one more zero than poles. This results in a large input admittance at high frequency, and poor current harmonic rejection for a Quasi-Z-source circuit.

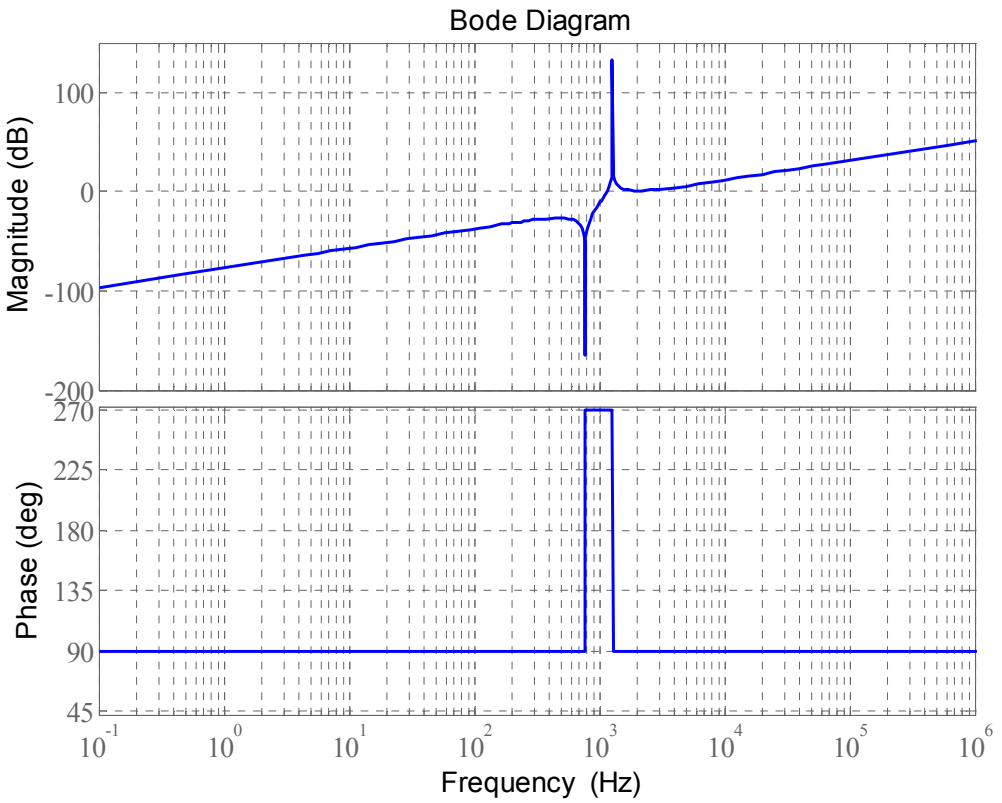

Figure 3.14. Bode plot of the transfer function of the input admittance of the Quasi-Z-source circuit

Control of the quasi-Z-source circuit makes use of the shoot-through duty cycle as the control variable and bode plot of the transfer function relating the control to the quasi-Z-circuit capacitors and inductors are also shown. This is to reveal possible resonance and its frequency similarly to the analysis shown in [7] for the ZSR. Resonance of the capacitor voltage or the inductor current may occur and it is therefore important to assess whether the resonance magnitude and frequency may be detrimental to the components. The transfer function relating capacitor C_1 voltage to control is given by (3.54) after substituting the parameters of Table 3.1. This transfer function is significant in direct and indirect control scheme of the peak output voltage of the full-bridge rectifier [20] [51]. The bode plot is shown in Figure 3.15.

$$
\begin{aligned}
G_{vd} &= \frac{\tilde{v}_{c1}(s)}{\tilde{d}(s)}\Big|_{\tilde{i}n(s)=0} \\
&= \frac{N_1 + N_2}{D_1 + D_2} \\
N_1 &= 6.507\times10^{-35}s^7 + 2.115\times10^{-30}s^6 + 2.896\times10^{-26}s^5 + 2.78\times10^{-23}s^4 \\
N_2 &= 8.883\times10^{-19}s^3 - 5.845\times10^{-17}s^2 + 7.027\times10^{-12}s + 2.952\times10^{-23} \\
D_1 &= 1.604\times10^{-40}s^8 + 1.382\times10^{-36}s^7 + 4.622\times10^{-32}s^6 + 1.138\times10^{-28}s^5 \\
D_2 &= 1.287\times10^{-24}s^4 + 2.42\times10^{-21}s^3 + 9.454\times10^{-18}s^2 + 1.536\times10^{-14}s + 5.17\times10^{-26}
\end{aligned}
\tag{3.54}
$$

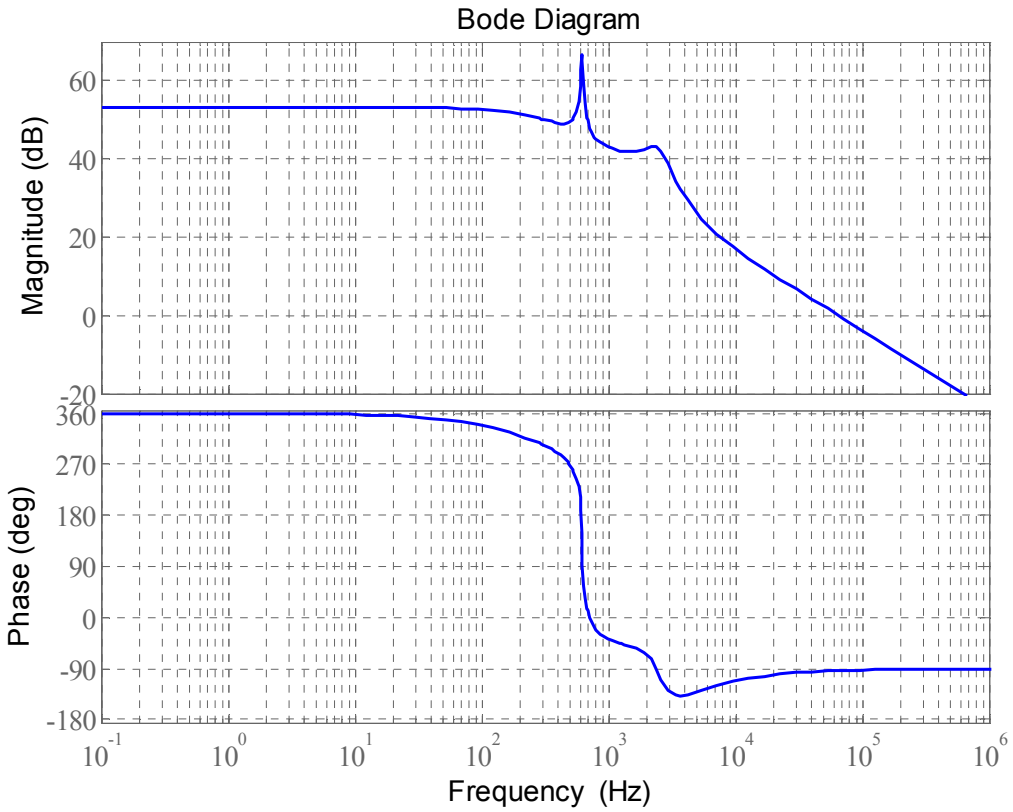

Figure 3.15. Bode plot of the transfer function relating the capacitor C_1 voltage to control

The magnitude and phase plot in Figure 3.15 of the transfer function relating capacitor C_1 voltage to control shows that resonance of the capacitor voltage takes place at the poles frequency of 616 Hz. Peak resonance magnitude is 13.4 dB higher than the DC magnitude of the capacitor voltage and could be detrimental to the capacitor. Such resonance amplitude should be accommodated within the capacitor tolerance. The transfer function relating capacitor C_1 voltage to control requires an adequate compensator in a perspective of using it to close a loop to control the full-bridge rectifier peak DC voltage. This is because some

overshoot and oscillations can be expected as in Figure 3.16 due to the dominant poles close to the imaginary axis. These poles are also related to the peak resonance observed on the bode plot.

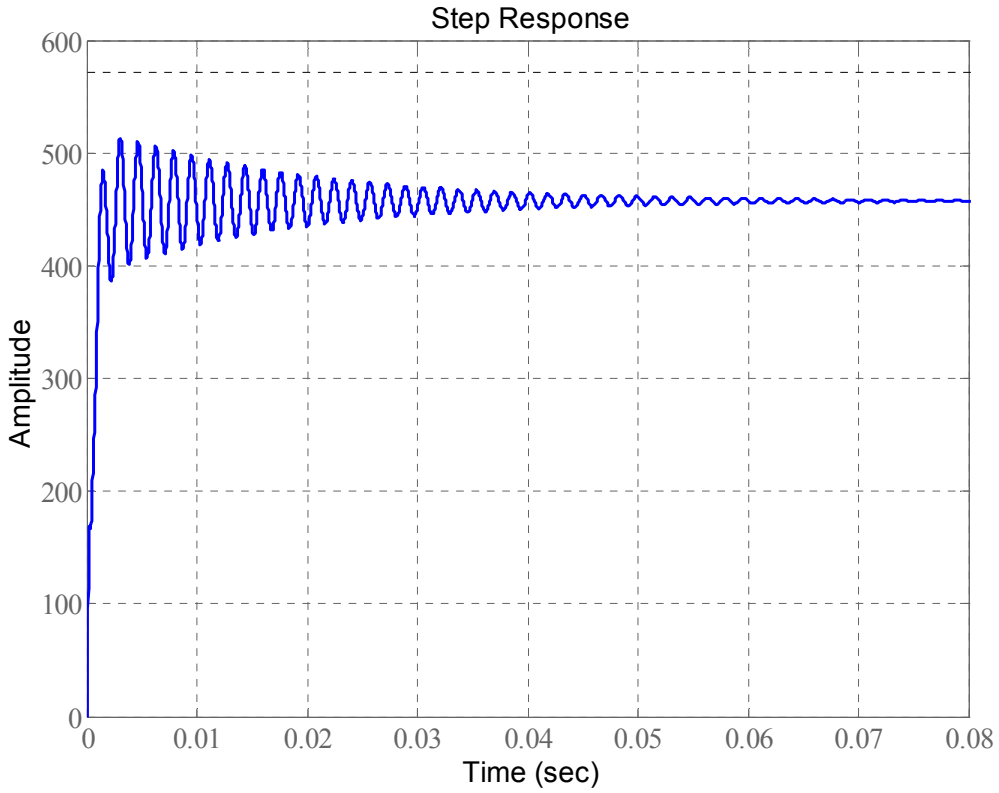

Figure 3.16. Step response of the transfer function relating the capacitor C_1 voltage to control

The transfer function relating inductor L_1 current to control is given by (3.55) after substituting the parameters of Table 3.1. Bode plot is shown in Figure 3.17. The significance of the transfer function relating inductor L_1 current to control is in current control scheme of the quasi-Z-source circuit. Steady state analysis has shown in equation (3.7) that the average inductor current and the load current are equal. This is further confirmed by the physical connection between the output and inductor L_1. Average current control of the load can be performed using the transfer function relating inductor L_1 current to control.

$$
\begin{aligned}
G_{id} &= \frac{\tilde{i}_{L1}(s)}{\tilde{d}(s)}\Big|_{\tilde{in}(s)=0} \\
&= \frac{N_1 + N_2}{D_1 + D_2} \\
N_1 &= -9.883\times10^{-25}s^4 - 6.693\times10^{-21}s^3 \\
N_2 &= -7.433\times10^{-18}s^2 - 1.683\times10^{-13}s + 2.643\times10^{-10} \\
D_1 &= 4.673\times10^{-30}s^5 + 4.025\times10^{-26}s^4 + 1.276\times10^{-21}s^3 \\
D_2 &= 2.711\times10^{-18}s^2 + 1.837\times10^{-14}s + 2.986\times10^{-11}
\end{aligned}
\tag{3.56}
$$

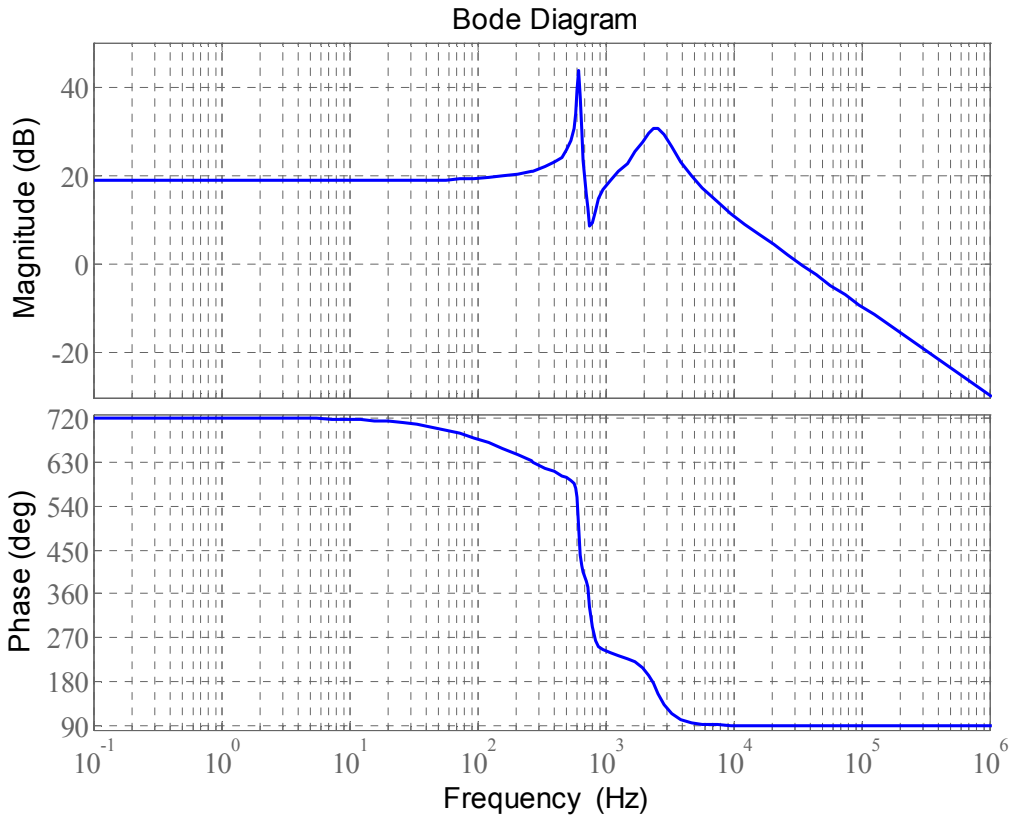

Figure 3.17. Bode plot of the transfer function relating inductor L_1 current to control

The pole zero map of Figure 3.18 shows that the transfer function relating inductor L_1 current to control has similar dominant poles and zeros as the transfer function relating the output capacitor to control. The control limitations caused by the RHP zeros and the poles close to the imaginary in the transfer function relating the output capacitor to control are also applicable to control strategy using the transfer function relating inductor L_1 current to control. These effects such as inverse response, oscillations and overshoot are shown on the

step response of Figure 3.19.

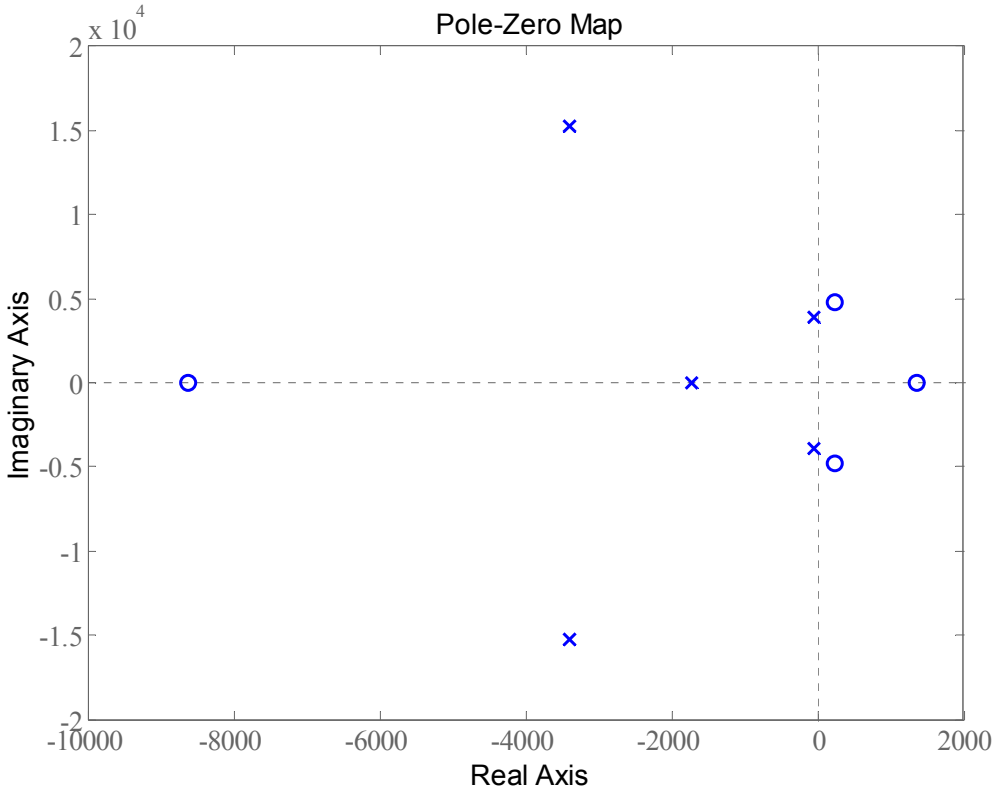

Figure 3.18. Pole-zero map of the transfer function relating inductor L_1 current to control

The ideal response should be such that the fastest current loop response can be achieved in the regulator design. However the bode plot of Figure 3.17 and the pole-zero map of Figure 3.19 show that the achievable bandwidth is limited well below the resonance frequency or the RHP zero frequency. For a quasi-Z-source circuit switching at a frequency of 40 kHz such low bandwidth represents a low performance caused by the characteristics of the transfer function relating the inductor L_1 current to control. The transfer function relating inductor L_1 current to control is such that it is challenging to design fast current control loop allowing to achieve the benefit of current control.

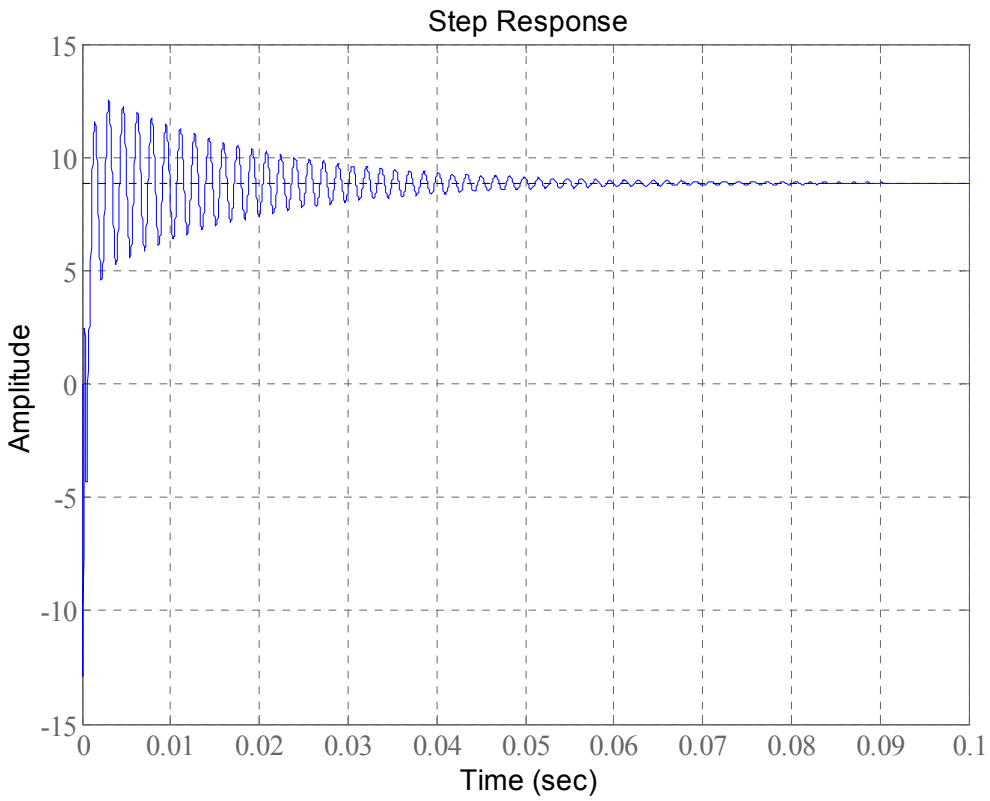

Figure 3.19. Step response of the transfer function relating inductor L_1 current to control

The findings relating to the quasi-Z-source circuit model can be summarised as follow: the frequency responses obtained are non-linear and the transfer functions relating each variable to control contain RHP zeros except for capacitor C_1. The RHP zeros reduce the achievable bandwidth for closed-loop control, limits how much gain can be used and makes the controller design difficult. A similar occurrence of RHP zeros is observed in boost and buck-boost like topology converter. Therefore control strategy for DC-DC boost and buck-boost converter can be considered for the QZSR. Similarly, the transfer functions relating each variable to the quasi-Z-source circuit input current have the same dominant pole location as the transfer functions relating each variable to control. The model that was derived is used together with the synchronous frame model of the full-bridge rectifier to design a control structure for the QZSR.

3.4. COMPARISON BETWEEN THE ZSR AND QZSR

Beside the advantage of a common DC rail between the input and the output in the QZSR topology, a detailed comparison between QZSR and ZSR is given in terms of:

3.4.1 Passive components ratings

It is shown in chapter two that symmetrical capacitors can be used for the ZSR. However the QZSR capacitors do not have to be equal to achieve the same performance. For the same input and output voltage specifications and the same output power rating for both rectifiers, capacitor C_1 of the QZSR is equal to the ZSR capacitor C_1 and C_2, because their DC voltages expression are identical as shown in equation (2.7) and equation (3.7) . Capacitor C_{2QZSR} has a larger capacitance but a much lower DC voltage rating than the identical capacitors C_{1QZSR}, C_{1ZSR}, C_{2ZSR}.

The output capacitor expression for each rectifier shown in equation (3.15) and equation (2.13) are repeated here:

$$C_{oZSR} = \frac{I_o D}{\Delta v_{co} F_{sw}} \quad \text{and} \quad C_{oQZSR} = \frac{\Delta i_{L1}}{8 \Delta v_{co} F_{sw}}.$$

Comparing the output capacitor expressions for the ZSR and QZSR, it can be seen analytically that the output capacitor for a QZSR is smaller compared to the traditional ZSR. Similar to the output capacitor current rating between a step-down and a step-up DC-DC converter [43], the output capacitor of the ZSR requires larger RMS current rating compared to C_o for the QZSR. Equations (3.15) and (2.13) show that the output capacitor of the ZSR has to supply the large load current during shoot-through like a step-up DC-DC converter when the switch is “on”. However, due to the inductor L_1 at the output, C_o for the QZSR only handles the inductor current ripple and results in a smaller capacitor like in a step-down DC-DC converter. The capacitors ratings were found to constitute one of the major differences between the ZSR and the QZSR.

The size of the inductors for both rectifiers is comparable in terms of inductance value and RMS current ratings, and can then be sized to be symmetrical in each rectifier. The quasi-Z-source circuit switch and the Z-source circuit switch are comparable in terms of blocking

voltage, RMS and peak current.

3.4.2 Steady state performance

The voltage gain B of the QZSR in equation (3.10) is similar to the gain of the ZSR in [2], confirming that both the QZSR and the ZSR have the same operational voltage range. Table 3.2 presents the steady state values of each rectifier component and it can be concluded that steady state performance is comparable between the ZSR and QZSR beside the capacitor voltage.

Table 3.2. Average Value of parameters for the ZSR and QZSR

DC Parameter	ZSR	QZSR
$\frac{V_{c1}}{V_o}$	$\frac{(1-D)}{(1-2D)}$	$\frac{(1-D)}{(1-2D)}$
$\frac{V_{c2}}{V_o}$	$\frac{(1-D)}{(1-2D)}$	$\frac{D}{(1-2D)}$
$\frac{V_{in}}{V_o}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$
I_{in}	$\frac{(1-2D)}{(1-D)}I_o$	$\frac{(1-2D)}{(1-D)}I_o$
I_{L1}	I_o	I_o
I_{L2}	I_o	I_o
I_{sw}	I_o	I_o
$\frac{V_{swblock}}{V_o}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$

3.4.3 Dynamic model and response

Based on mathematical computations, deriving the dynamic model of the QZSR is more complex than the ZSR mainly due to the absence of symmetry of the capacitors. This is confirmed by the transfer functions obtained where the highest order characteristic equation for the ZSR is 3 while the QZSR is up to 8. Comparing the response obtained, the following conclusions can be drawn from the four essential transfer functions of each converter:

Based on the transfer function relating the output capacitor voltage to control, the dynamic performance of the ZSR is slightly better than the QZSR. The dominant zero of the ZSR is located at 1030 (164 Hz) on the pole-zero map in Figure 2.6 while the dominant zeros for the QZSR are located at 1370 (217 Hz), at -237 ± 4760j (759 Hz) and at 616 Hz (on the imaginary axis) in Figure 3.9. The QZSR dominant zeros are therefore closer to the imaginary on RHP and will impose stricter limitation on the bandwidth and a larger inverse response compared to the ZSR. The dominant poles for the ZSR are located at -661 (105 Hz) and -544 ± 1030j (1.64 kHz) while the dominant poles for the QZSR are located at -1720 (274 Hz), -56 ± 3890j (619 Hz) and at 616 Hz (on the imaginary axis). The complex poles of the QZSR are closer to the imaginary axis which translates to more oscillations for voltage control loop in the QZSR than the ZSR. The poles and zeros locations therefore suggests that the QZSR output voltage response to control changes is slower and more underdamped than the ZSR. This is confirmed by the step response plot of Figure 3.20.

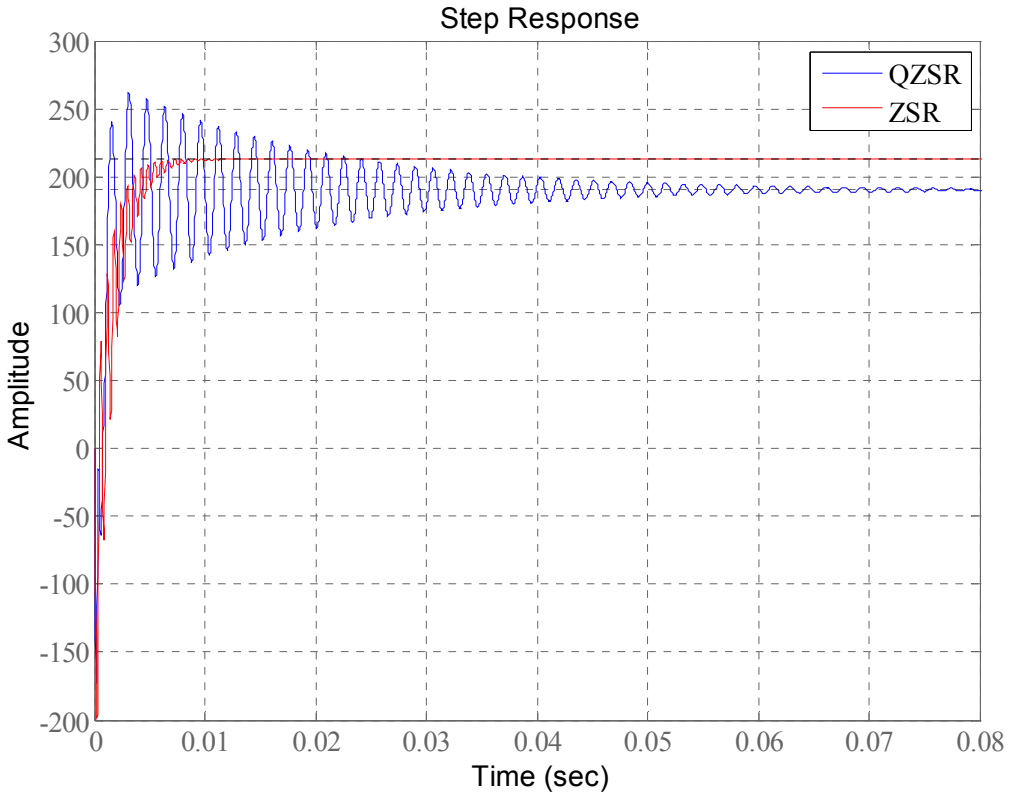

Figure 3.20. Step response of the transfer function relating the output capacitor voltage to control for the QZSR and the ZSR

Comparing bode plot of each converter in Figure 3.21 shows that the low frequency performance in terms of gain and phase are comparable. At high frequency the QZSR has a higher decade rate of -40 db/decade compared to the -20 db/decade of the ZSR. For a regulator design this translates to a better noise rejection from the QZSR compared to the ZSR. Resonance peak amplitudes of the two converters are comparable. The overall response of each transfer function is satisfactory for use in an output voltage regulator design with a slight advantage of the QZSR over the ZSR at high frequency.

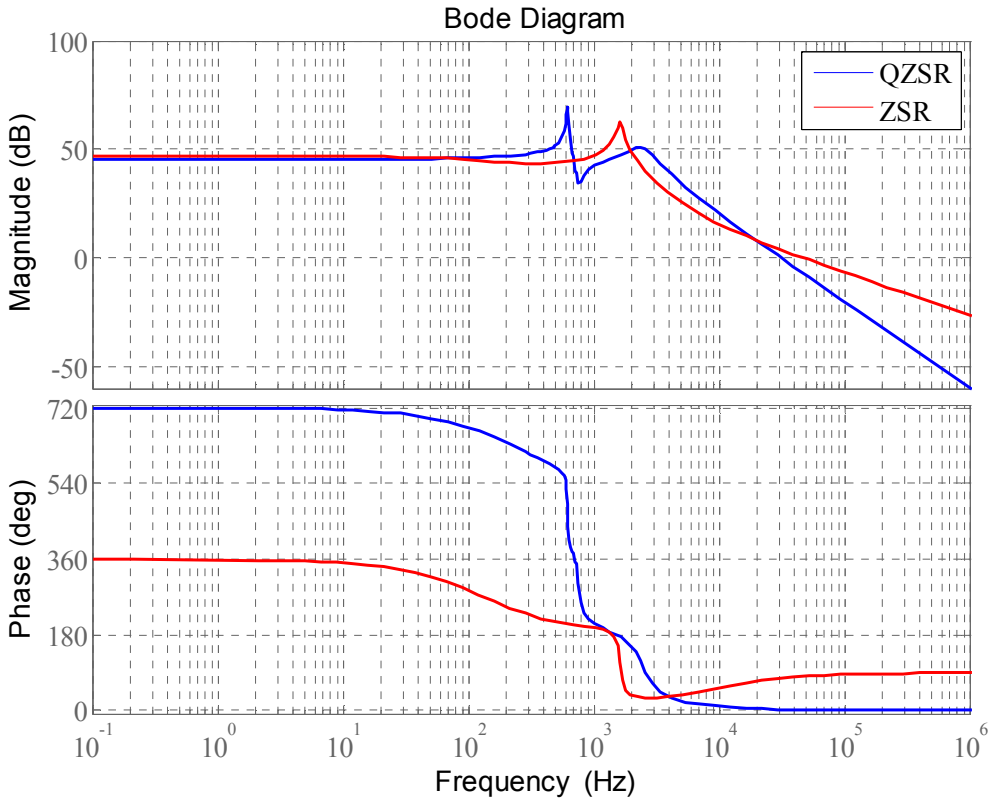

Figure 3.21. Bode plot of the transfer function relating the output capacitor voltage to control for the QZSR and the ZSR

The transfer functions relating the output voltage ripple to the input current ripple (current susceptibility) have the same poles locations as the transfer function relating the output capacitor voltage to control. Therefore the transient response advantages of the ZSR over the QZSR in terms of faster natural response and less oscillation are also applicable if input current ripple manage to affect the output voltage. Input current ripple effects on the output voltage will be observed with less oscillation in the ZSR compared to the QZSR.

The low frequency current susceptibility of the two circuits are comparable in the bode plot of Figure 3.22. However at high frequency the QZSR output voltage is less susceptible to input current ripple compared to the ZSR due to higher decade rate. The effects of input current variations on the output voltage are much smaller in the QZSR compared to the ZSR. But with the given switching frequency of the two converters the bode plot response suggests that input current ripple has negligible effect on the output voltage of each converter due to the high attenuation observed at high frequency.

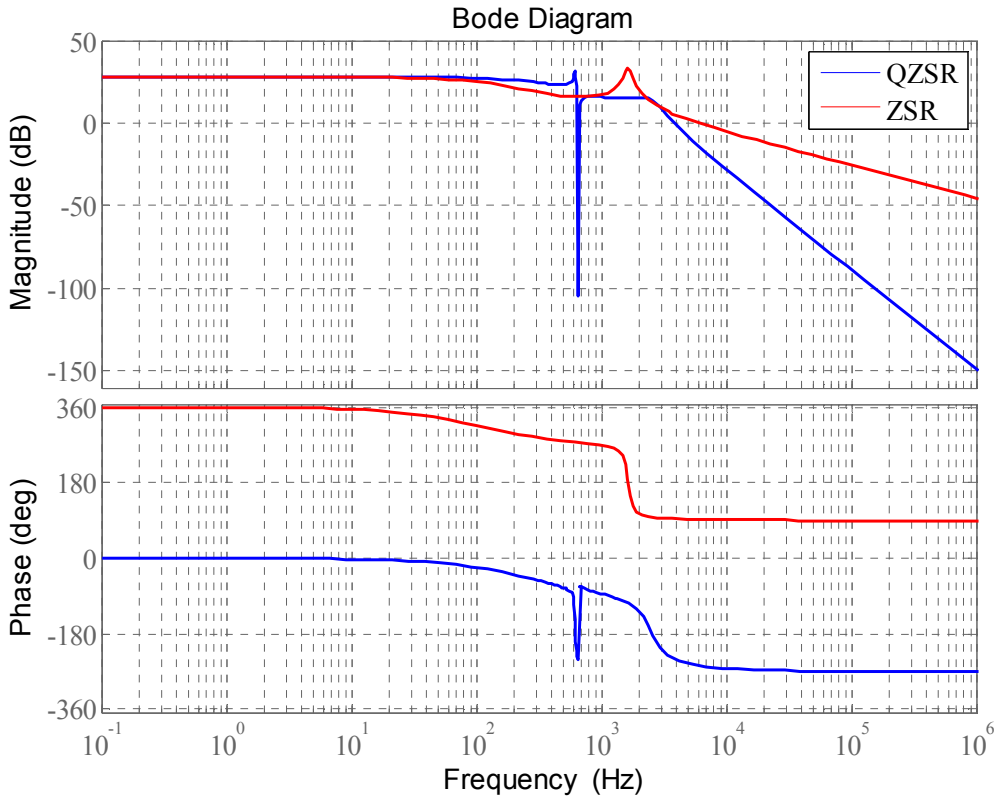

Figure 3.22. Bode plot of the transfer function relating the output voltage ripple to the input current ripple (current susceptibility) for the QZSR and the ZSR

Comparing the output performance of each converter using the output impedance bode plot in Figure 3.23 shows that the ZSR has slightly better output performance. At high frequency where current ripple can be expected, the ZSR output impedance is lower than the QZSR by 14 dB. This means that the output voltage of the ZSR is less affected by output current ripple compared to the QZSR. The output impedance performance of both converters is comparable at low frequency as shown in the bode plot.

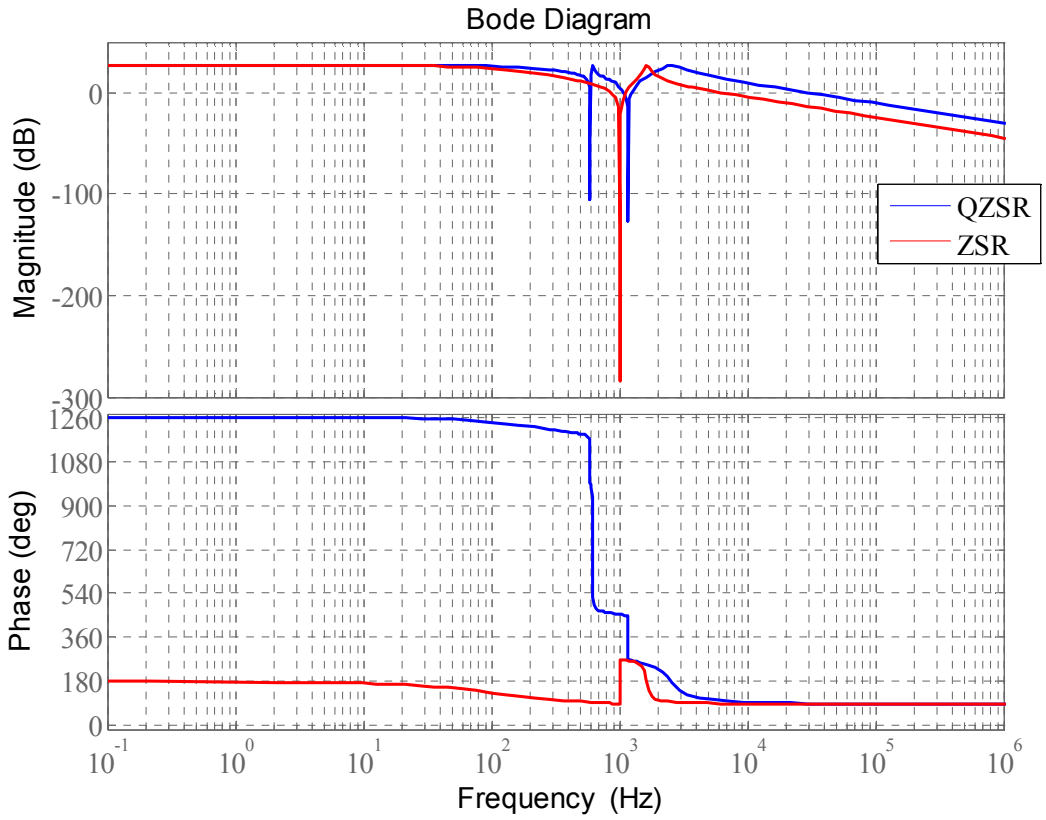

Figure 3.23. Bode plot of the transfer function of the output impedance of the QZSR and the ZSR

The input performance of each converter is analysed with the bode plot of the input admittance in Figure 3.24 from where it can be observed that the ZSR and QZSR have comparable input performance up to around 7 kHz. At higher frequency the ZSR input admittance rolls down at -20 dB/decade while the QZSR input admittance increases at 20 dB/decade. The low input admittance of the ZSR at high frequency ensures a low level of current disturbances is generated. This makes the dynamic admittance of ZSR better compared to that of the QZSR.

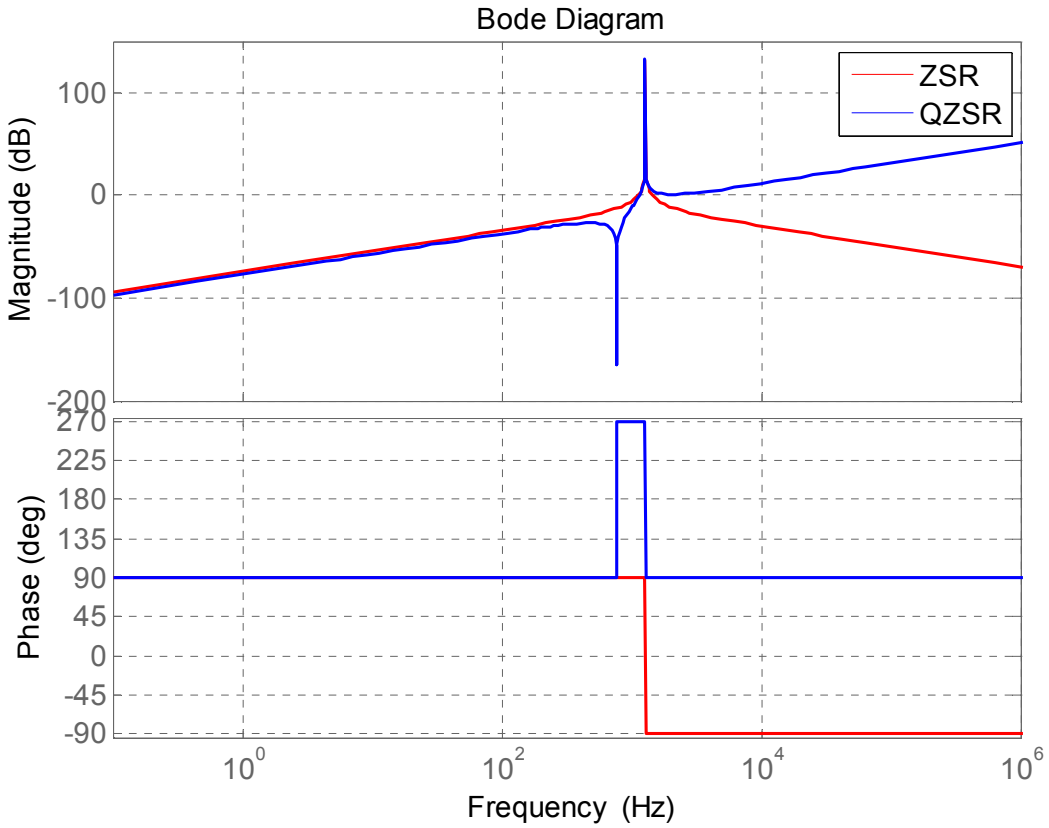

Figure 3.24. Bode plot of the transfer function of the input admittance of the QZSR and the ZSR

Based on the dynamics performances and the controller that will be required, it can be concluded that the ZSR perform better than the QZSR. However, from a system point of view the results have revealed that the QZSR is a more cost-effective system with lower rated capacitors.

3.5 CHAPTER CONCLUSION

Steady state model and small-signal model of the QZSR was derived using the synchronous reference frame and circuit averaging. The steady state model proves the lower capacitance and voltage rating of the QZSR compared to the ZSR. The small-signal model leads to all the transfer functions and the block diagram representation of the QSR essential to design a closed-loop controller. Detailed comparison between the ZSR and the QZSR shows that the ZSR exhibits better dynamic performance while the QZSR offer more cost efficient steady state performance with lower rated passive components.

CHAPTER 4 THREE-PHASE QUASI-Z-SOURCE RECTIFIER CONTROLLER DESIGN

4.1. INTRODUCTION

A quasi-Z-source three-phase rectifier is a PWM full-bridge rectifier modified at its output stage with a quasi-Z-source circuit. This is confirmed by the model that was obtained which is similar to the one of a three-phase PWM rectifier. The control techniques applicable to a three-phase PWM rectifier can then be analysed to control the QZSR with modifications where required. A controller is needed to achieve the objectives of the rectifier: maintaining the output DC voltage as close as possible to the desired value even under wide AC input voltage variations and ensuring that a low total harmonic distortion (THD) AC input current is drawn in phase with the AC input voltage. By making use of AC input current control scheme the advantage of reactive power control can also be fully utilised in the QZSR.

Traditionally the implementation of switch-mode controller has been accomplished using analog components such as Integrated Circuit (IC) or a controller built with passive components [52] [53]. Analog control can provide continuous processing of signal, thus allowing very high bandwidth [52] [53]. It also gives infinite resolution of the signal measured and is inexpensive [52] [53]. However analog control poses significant drawbacks related to analog components. Analog components are susceptible to variations due to tolerance, aging and working environment which lead to high maintenance cost and reduced reliability [52]. Furthermore, analog control is limited by the number of parts required in the system and the inflexibility of the design which cannot be optimised for large variations [52] [53]. In the view of these disadvantages, digital controllers in the form of digital-signal processors (DSP), microcontrollers, and field-programmable gate arrays (FPGAs) have been used in power electronics application in the past decades [52] [54].

With the advancement of microprocessors/DSP, digital control is increasingly used in various applications of switch-mode power converter [52] such as three-phase rectifier. Compared to analog control, DSP based digital control offers many distinctive advantages such as [52] [53] [55] [56]:

- Standard control hardware design for multiple platforms
- Less susceptibility to aging and environmental variations
- Better noise immunity
- Ease of implementations of sophisticated control algorithms
- Flexible design modifications to meet a specific application
- Single chip solution for both control and communication functions

However the disadvantages of digital control include: limited signal resolution due to finite word length of the processor and Analog to digital (A/D) converter; sampling time delay, and limited computation power and control loop bandwidth [53]. The benefits of using digital control with the computation required in vector control of a three-phase rectifier make it the design approach of choice.

Several digital design techniques have been proposed but there are in general two approaches to design a digital controller: digital redesign approach or design by emulation and direct digital approach [53] [56] [57] [58]. In the digital redesign approach the controller is designed in the continuous domain and then discretized into the discrete form [53] [56] [57] [58]. This approach has the advantages of reducing the controller design time by using continuous time design tool [53] [57]. In the direct digital approach the system plant in the continuous domain is first transformed into the z-domain and the controller design is carried out directly in the z-domain [53] [56] [57]. In the Z-domain the controller can be designed using methods such as discrete-time frequency response method, root-locus method, or deadbeat method [53] [56] [57] [58]. The direct digital approach has the advantage of producing a higher bandwidth and stability than any digital redesign [53] [57]. Irrespective of the digital controller approach used, discretization is required to transform into the Z-domain.

There are several discretization methods: the Backward Euler, the Bilinear Transformation, Step Invariant Transformation and the Pole/Zero Match Transformation [53] [58]. Each discretization method uses the transformation equation given in Table 4.1 to convert S-domain transfer function to Z-domain. The Backward Euler method is easy to apply but does not preserve the impulse and frequency response of the analog controller [53] [57]. The Bilinear Transformation method preserves both the gain and phase properties of the controller below 1/10 of the sampling frequency [53] [57]. The Step Invariant Transformation method preserves the step response, but does not preserve the impulse and frequency response [53] [57]. The Pole/Zero Match Transformation method preserves the pole-zero location, but is subject to aliasing if the frequencies of the zeros are greater than the Nyquist frequency [53] [57].

Table 4.1. Discretization Methods [57]

Transformation Method	**S-Domain**	**Z-Domain**
Backward Euler	s	$\frac{1-z^{-1}}{T_s}$
Bilinear	s	$\frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$
Step Invariant	$G_c(s)$	$Z\left(\frac{1-e^{-T_S S}}{s}G_c(s)\right)$
Pole/Zero Match	$s+a$	$1-z^{-1}e^{-aT_S}$
Pole/Zero Match	$s+a\pm jb$	$1-z^{-1}e^{-aT_S}\cos bT_s+z^{-2}e^{-2aT_S}$

It is shown in [53] [57] that in terms of control bandwidth, phase margin and output transient response during load change the Backward Euler method is the best digital redesign method. It produces the largest control bandwidth and the lowest THD with non linear load. However care needs to be taken in using the Backward Euler method at low sampling rate in applications with reduced margin for inaccuracy [41]. The transformation equation is based on finite difference approximation. Accurate transfer function transformations formulas based on Zero-order hold are suggested in [58] for control of systems depending on high modelling accuracy. The QZSR controller is designed using the

digital redesign approach with the Backward Euler method for discretization. The limitations of this approach are mitigated by including in the analysis all the expected delays from hardware components. Microcontrollers and DSP codes available for implementing the standard Proportional-Integral-Derivative (PID) digital controller are mostly derived using the Backward Euler method.

In most microprocessor based digital control of power converter computational and hardware delay must be included [53]. This is justified by the significant portion of the sampling period used to implement control algorithm and the dynamics of hardware used in analog filter for instance [53] [56]. The delay transfer function $H_{delay}(s)$ is made of the product of the transfer function modelling the Zero-Order Hold (ZOH) associated with the A/D sampling, and the transfer function modelling the computational delay associated with microcontroller operations during control implementation. $H_{delay}(s)$ is given by [53] [56]:

$$H_{delay}(s) = H_{ZOH}(s) \times H_c(s) = \frac{1 - e^{-T_S S}}{s} \times e^{-T_C S} \tag{4.1}$$

Furthermore the new controller output is usually implemented during the next sampling period. The computational and hardware delay is mostly modelled equal to the sampling period as Tc = Ts [53] [56]. Ts is the sampling period and Tc is the computation time.

There are several options in choosing the sampling frequency in a digital controller for a power converter. Sampling can be done either at switching frequency, higher than the switching frequency (oversampling), or at lower than the switching frequency (under sampling) [41]. The benefit of oversampling is on a more accurate controller action as multiple measurements are taken during a switching period [41]. However oversampling may not be possible with large complex control algorithm requiring long computation time. Oversampling results in excessive use of microcontroller resource for a limited increase in performance [41]. Under sampling may result in slow controller response but is well-suited for long and complex control algorithm. Sampling at switching frequency is mostly used as it gives good trade-off between under sampling and oversampling [41]. Sampling at switching frequency was chosen for the QZSR as it does not pose any difficulty in implementing the control algorithm and achieving a fast performance.

To achieve the control objectives and based on the model that was derived, an additional contribution is presented with the two stages control methodology applied to a quasi-Z-source three-phase rectifier. This control approach has been suggested in Z-source inverter [18] and quasi-Z-source [34] inverter where a dual control objective is required. It is utilised in the quasi-Z-source three-phase rectifier with separate control of the AC side input current in stage 1 and control of the DC output voltage of the QZSR in stage 2 as shown in Figure 4.1. The AC loop consists on a double loop with a fast inner current loop and a slower outer voltage loop to control the peak DC output voltage of the full-bridge.

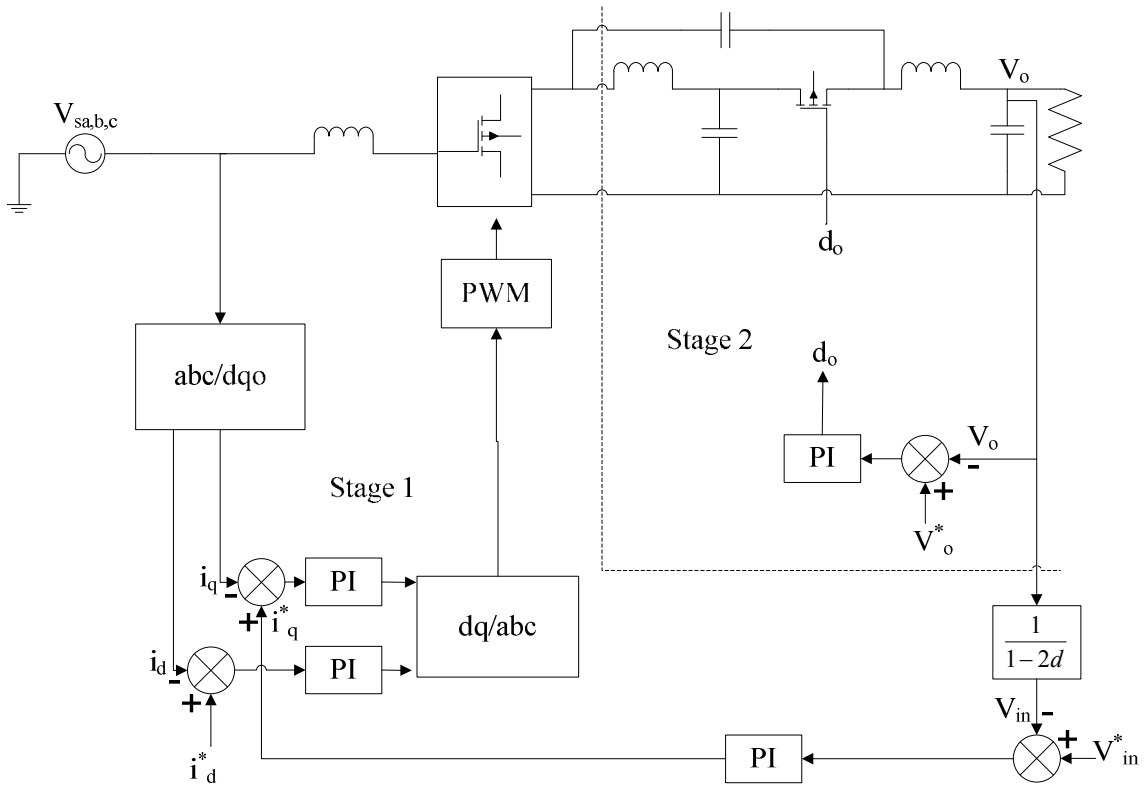

Figure 4.1. Two stage control diagram of QZSR

The set point of the peak DC output voltage of the full-bridge for the outer loop is calculated using the desired shoot-through duty cycle and the desired DC output voltage. The measured peak DC output voltage of the full-bridge is computed in real time using the measured output DC voltage and the actual shoot-through duty cycle. Therefore no peak detector is required and highlights one of the advantages of the unique approach that was developed for the QZSR control. The quasi-Z-source circuit DC output voltage is controlled using a single voltage loop. To ensure a fast overall response and avoid overlap between the

AC and DC loop, the input AC current loop is made faster than the DC voltage loop. The fast current loop response ensures that load current variations are compensated and do not affect capacitor voltages.

The additional challenge between the stages is the possible overlap of the shoot-through duty ratio D and the modulation index M. The interaction between D and M is resolved by inserting a null zone to account for fast changes, to prevent overlap and to limit these parameters to a maximum value as shown in Figure 4.2. The state diagram concept in Figure 4.2 is an additional contribution that modifies the state diagram concept of the Z-source inverter in [18] to apply it to the control of quasi-Z-source three-phase rectifier.

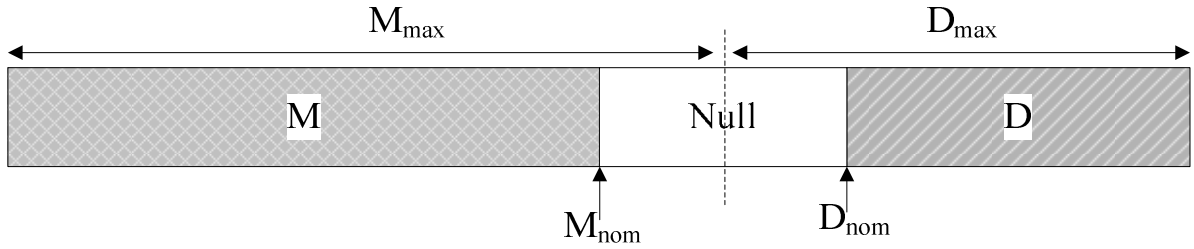

Figure 4.2. Shoot-through and Modulation Index diagram

The nominal value for modulation index (M_{nom}) and shoot-through duty cycle (D_{nom}), and their maximum value (M_{max} for modulation index and D_{max} for shoot-through duty cycle) to be used in the control loop can be calculated as follows:

For a given AC input voltage and fixed output DC voltage, the buck-boost factor is given by:

$$B = \frac{V_o \cos\theta}{2V_{speak}} \tag{4.2}$$

Using the buck-boost factor obtained from equation (4.2) into equation (3.7) given by $B = \frac{1-2D}{M}$, the nominal values for D_{nom} and M_{nom} can be obtained. However the insertion of the null zone in Figure 4.2 modifies equation (3.7) in computing D and M. Furthermore the modulation method used also modifies the equation between D and M. As suggested in [10] the modulation methods used for Z-source inverter and quasi-Z-source inverter can be used for quasi-Z-source three-phase rectifier. In [8] [35] [36] the modulation

methods along with the corresponding equations between the modulation index and shoot-through duty cycle are given as follow:

Simple boost: $$M \leq 1 - D \tag{4.3}$$

Maximum constant-boost: $$M \leq \frac{2}{\sqrt{3}}(1 - D) \tag{4.4}$$

Maximum boost: $$M \leq \frac{2\pi}{3\sqrt{3}}(1 - D) \tag{4.5}$$

Making use of the simple boost method and inserting a 1 % null zone, D and M are related by:

$$M + D + 0.01 = 1 \tag{4.6}$$

Solving for D: $$D_{nom} = 0.99 - M \tag{4.7}$$

Substituting D from equation (4.7) into equation (4.2) M_{nom} is given by:

$$M_{nom} = \frac{0.98}{2 - B} \tag{4.8}$$

The null zone value is split in 50 % for M and D such that the maximum value that is used as limiting value in the control loop is given by:

$$\begin{aligned} D_{\max} &= D_{nom} + 0.05 \\ M_{\max} &= M_{nom} + 0.05 \end{aligned} \tag{4.9}$$

For a varying three-phase voltage and a fixed output voltage, the buck-boost factor will be varying and as a result the ideal value of the nominal and maximum modulation index and shoot-through duty cycle need updating in real time. The influence of the insertion of the null zone is the decrease of the modulation index value and the small increase of the shoot-through duty cycle. This results in higher quasi-Z-source capacitor voltages. A 1% null zone increases the capacitors voltages by 2 V which can be considered negligible.

4.2. FULL-BRIDGE CONTROLLER DESIGN

Control techniques for PWM rectifier can generally be classified as voltage based and virtual flux based. Four types of these techniques can be identified: voltage oriented control (VOC), Voltage based direct power control (V-DPC), virtual flux-oriented control (VFOC), and virtual flux-based direct power control (VF-DPC) [59]. The VOC and VFOC have comparable performances in term of achievable power factor, fixed frequency used and

micro-processor resources needed. The VF-DPC provides the best control performances with the highest power factor and the lowest THD but requires variable frequency (difficult input filter design) and more microprocessor resources [59].

Any of the PWM rectifier control techniques can be used in the QZSR AC current control loop. To keep the control simple and effective Voltage oriented control was used for the QZSR. In the voltage-oriented control scheme, the unity-power-factor condition is enforced by aligning the quadrature component of the reference voltage vector with the current vector, and by setting to zero the reference value of the direct component i^*_d of the current vector [59]. Control of the QZSR starts by designing a stable and fast inner current loop for the full-bridge input AC current using the synchronous frame model. From the system diagram in Figure 4.1, the block diagram of the inner q-axis current loop is shown in Figure 4.3 including the additional delay block accounting for the digital implementation of the controller:

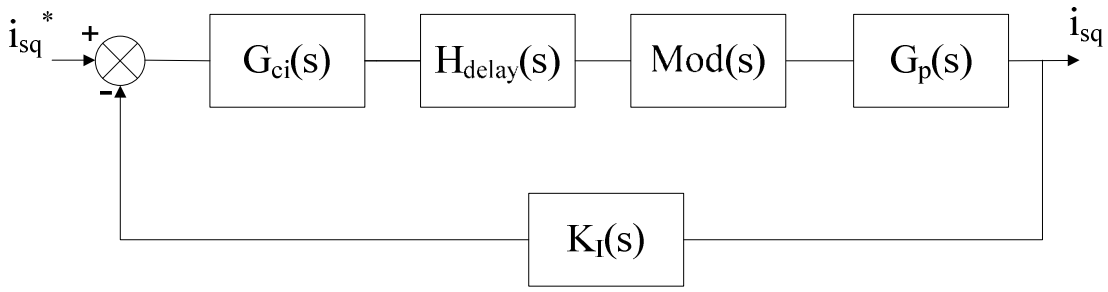

Figure 4.3. q-axis current control loop block diagram in s-domain

The transfer functions of Figure 4.3 are defined as follow:

The digital current controller transfer function $G_{ci}(s)$

The PWM modulator transfer function: $Mod(s) = G_{PWM}$ (4.10)

The converter transfer function: $G_P(s) = \dfrac{1/R_S}{1+sT_{sp}}$ (4.11)

The block K_I represents the transfer function of the LEM sensor and the active low pass filter used. The current sensor and the filter transfer function are given by:

$$K_I(s) = k_i \frac{1}{1 + C_{2f}(R_{1f} + R_{2f})s + C_{1f}C_{2f}R_{1f}R_{2f}s^2} \quad (4.12)$$

The parameters used in equations (4.10) to (4.12) are defined by:

$T_{SP} = \frac{L_S}{R_S}$: Time constant of the input inductor and resistor

G_{PMW}: PWM modulator gain

$T_{SW} = \frac{1}{F_{SW}}$: Switching period

k_i: Current sensor gain

The uncompensated open loop transfer function is given in (4.13) by:

$$L_{iq} = \frac{G_{PWM} k_i \left(1 - e^{-T_S S}\right) e^{-T_S S}}{R_S (1 + sT_{SP}) \left[1 + C_{2f}\left(R_{1f} + R_{2f}\right)s + C_{1f} C_{2f} R_{1f} R_{2f} s^2\right] s} \tag{4.13}$$

The delay transfer function needs to be transformed to an equation suitable for use in a linear bode plot. The transfer function of the delay associated with the computation time is approximated by a 1st order Pade approximation and given by equation (4.14) [41]:

$$e^{-T_S S} = \frac{2 - sT_S}{2 + sT_S} \tag{4.14}$$

The transfer function of the delay associated with the zero-order hold is also approximated by a 1st order Pade approximation and given by equation (4.15) [60]:

$$\frac{1 - e^{-T_S S}}{s} = \frac{1}{1 + \frac{f_s s}{2}} \tag{4.15}$$

The delay approximations are substituted into equation (4.13) and the new uncompensated open loop transfer function is given by:

$$L_{iq} = \frac{G_{PWM} k_i \left(2 - sT_S\right)}{R_S (1 + sT_{SP}) \left[1 + C_{2f}\left(R_{1f} + R_{2f}\right)s + C_{1f} C_{2f} R_{1f} R_{2f} s^2\right] \left(2 + sT_S\right)\left(1 + \frac{f_s s}{2}\right) s} \tag{4.16}$$

For a bipolar switching scheme, the modulator gain is given by equation (2.19) [61]:

$$G = \frac{V_{DC}}{4V_{tri}} \tag{4.17}$$

Where V_{DC} is the full-bridge rectifier output voltage, k_v is the output voltage sensor gain and V_{tri} the triangular carrier peak amplitude in sine PWM. The AC current controller is

designed using the model parameters when the AC input voltage is 100 V in the PWM rectifier mode. However verification of the controller performance is done for other input voltage such that throughout voltage variation adequate loop crossover frequency is achieved. Bode plot of the transfer function of the uncompensated current loop is shown in Figure 4.4 using the converter parameter in Table 4.2 into equation (4.16) and equation (4.17).

Table 4.2. Converter parameter.

Parameters	Value	Parameters	Value
L_S	1400 μH	R_{1f}	1 $k\Omega$
R_S	1.5 Ω	R_{2f}	1 $k\Omega$
F_{SW}	20 kHz	C_{1f}	0.1 μF
T_S	50 μs	C_{2f}	25 μF
k_i	0.027171	G_{PWM}	37.5

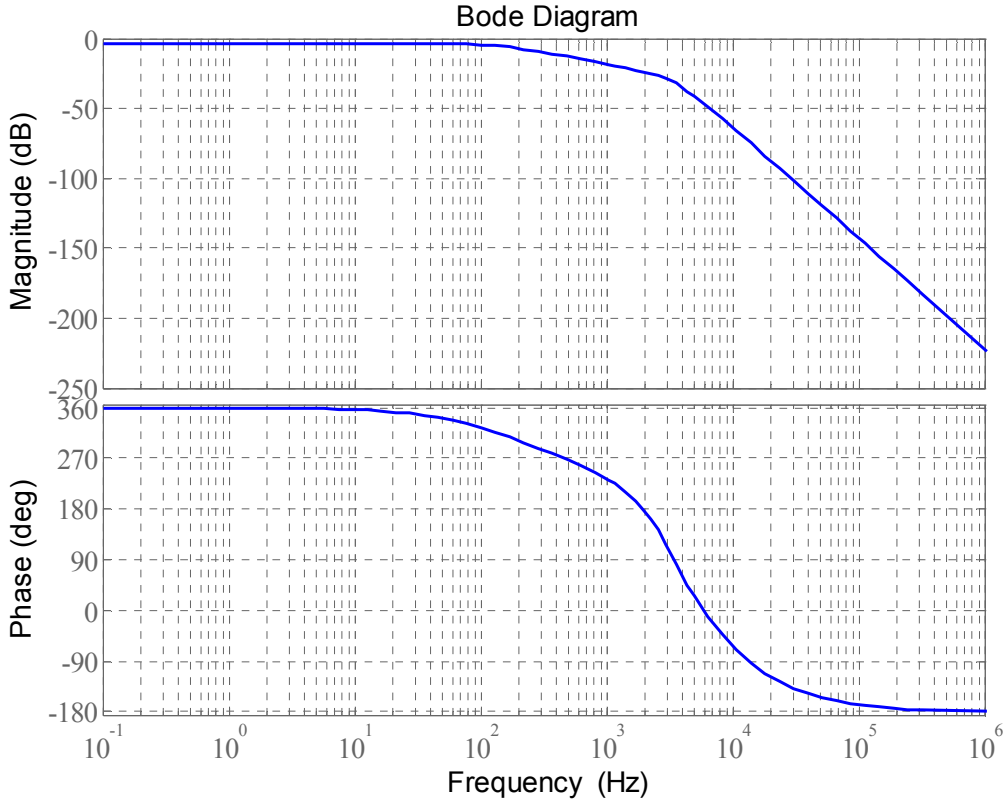

Figure 4.4. Bode plot of the transfer function of the uncompensated q-axis current

A suitable inner current loop crossover frequency of 0.2 F_{sw} in power converter results in a fast current loop without any switching frequency noise [13]. However the bode plot of transfer function of the uncompensated open loop of Figure 4.4 suggests that this desired crossover frequency is very difficult to attain mostly due to the digital control implementation. The delays included reduce the phase at high frequency to an unstable region. The achievable crossover frequency will therefore have to be reduced significantly. To achieve good steady state tracking, a Proportional-Integral (PI) compensator is designed using the transfer function of the uncompensated q-axis current open loop of Figure 4.4.

The s-domain expression for a PI controller is given by [41]:

$$G_c(s) = K_C\left(1 + \frac{2\pi f_s}{s}\right) \tag{4.18}$$

The z-domain PI controller is obtained from the s-domain gain and time constant using finite difference transformation and given by [41]:

$$G_c(z) = \frac{K_C\left(1 + \frac{T_s}{t_I}\right) - K_C z^{-1}}{1 - z^{-1}} \tag{4.19}$$

The crossover frequency is chosen such that a minimum phase margin of 60 degree is achieved at the highest possible frequency. A phase margin of 60 degree translates to minimal current overshoot and a high crossover frequency ensures a fast current response. A phase angle of 70 degree is attained at 700 Hz on the bode plot of the transfer function of the uncompensated q-axis current in Figure 4.4. A PI controller coefficient is then selected so that a crossover frequency of 700 Hz and a phase margin of 60 degree minimum are obtained. Taking into account the -45 degree phase reduction introduced by a PI controller at the corner frequency, it is selected sufficiently low to maintain adequate phase margin of 60 degree in the current loop gain [13]. This corresponds to a corner frequency low by a factor of 10 relative to the desired crossover frequency [13]. The PI controller gain is adjusted such that the magnitude is zero at the desired crossover frequency [13]. For a 700 Hz desired crossover frequency, the PI controller corner frequency is 70 Hz. The s-domain PI controller for the q-axis current loop is given by equation (4.20) and its bode plot shown in Figure 4.5.

$$G_{ci}(s) = 6.0954\left(1 + \frac{6.28 \times 70}{s}\right) \tag{4.20}$$

The z-domain controller of equation (4.20) is expressed by:

$$G_{ci}(z) = \frac{6.2294 - 6.0954z^{-1}}{1 - z^{-1}} \tag{4.21}$$

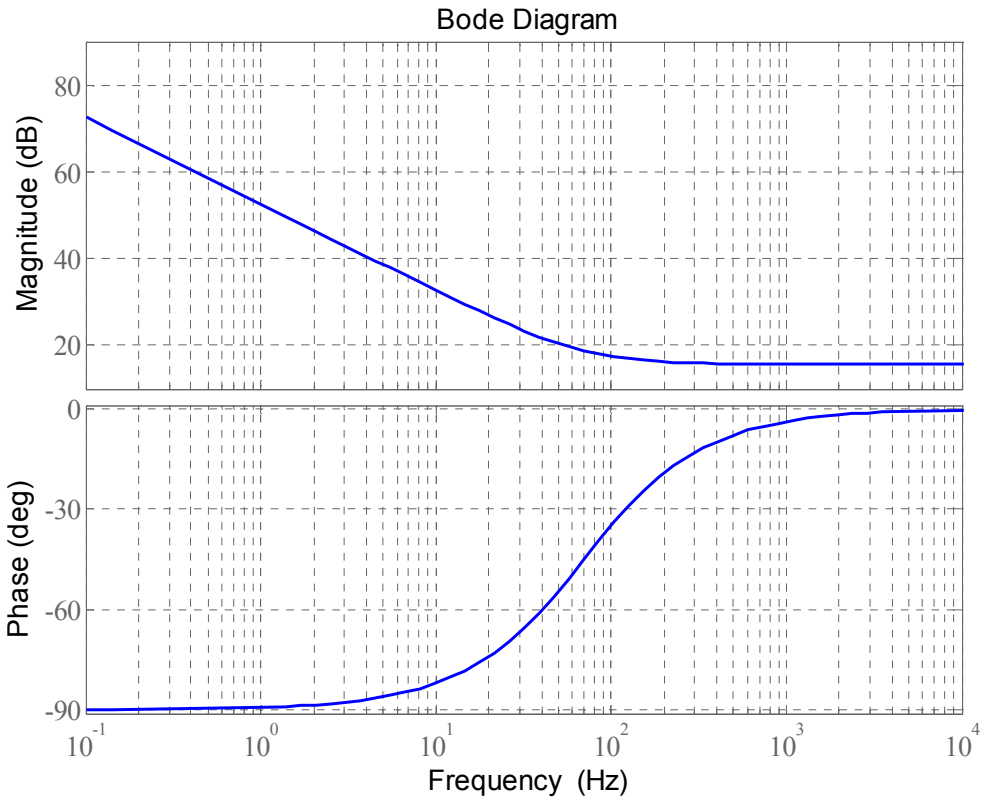

Figure 4.5. Bode plot of the transfer function of the q-axis current PI controller

Bode plot of the transfer function of the compensated q-axis current loop in Figure 4.6 shows a crossover frequency of 700 Hz and a phase margin is 66 degree. For a rectifier switching frequency of 20 kHz, the crossover frequency obtained is by 5.7 lower than the benchmark power converter bandwidth value of $0.2F_{sw}$. Higher crossover frequency can be designed by increasing gain. However the digital control implementation and the analog filter used require the use of lower gain to avoid any oscillation and loss of control. Large current oscillations occurs at any bandwidth above 800 Hz. Despite the limitations, the phase margin and bandwidth of the compensated loop result in a satisfactory current response, as shown by the closed-loop step response of Figure 4.7. The 95% settling time is

2.5 ms and the current overshoot negligible. The settling time achieved compares well to PWM rectifier current response time of less than a quarter of cycle [62] [63] [64]. The d-axis controller uses the same controller as the q-axis controller. Because the transfer function of current loop is independent of the input AC voltage, the fixed gain controller is satisfactory throughout the operating voltage range.

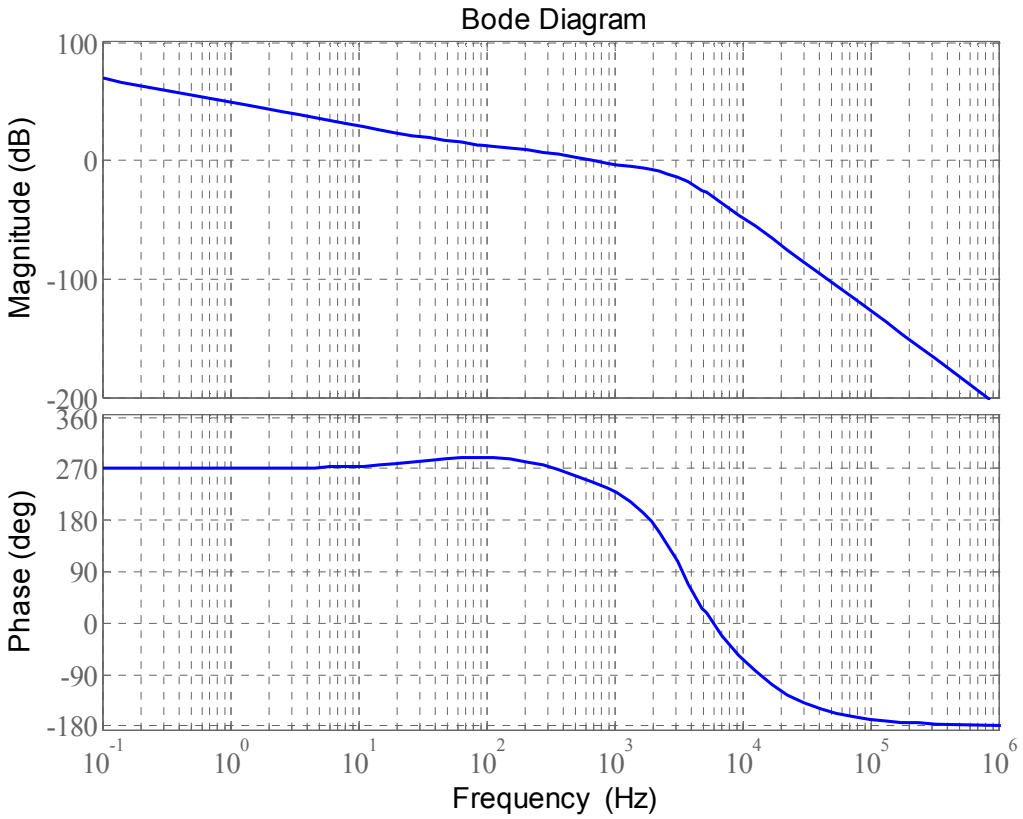

Figure 4.6. Bode plot of the transfer function of the compensated q-axis current loop

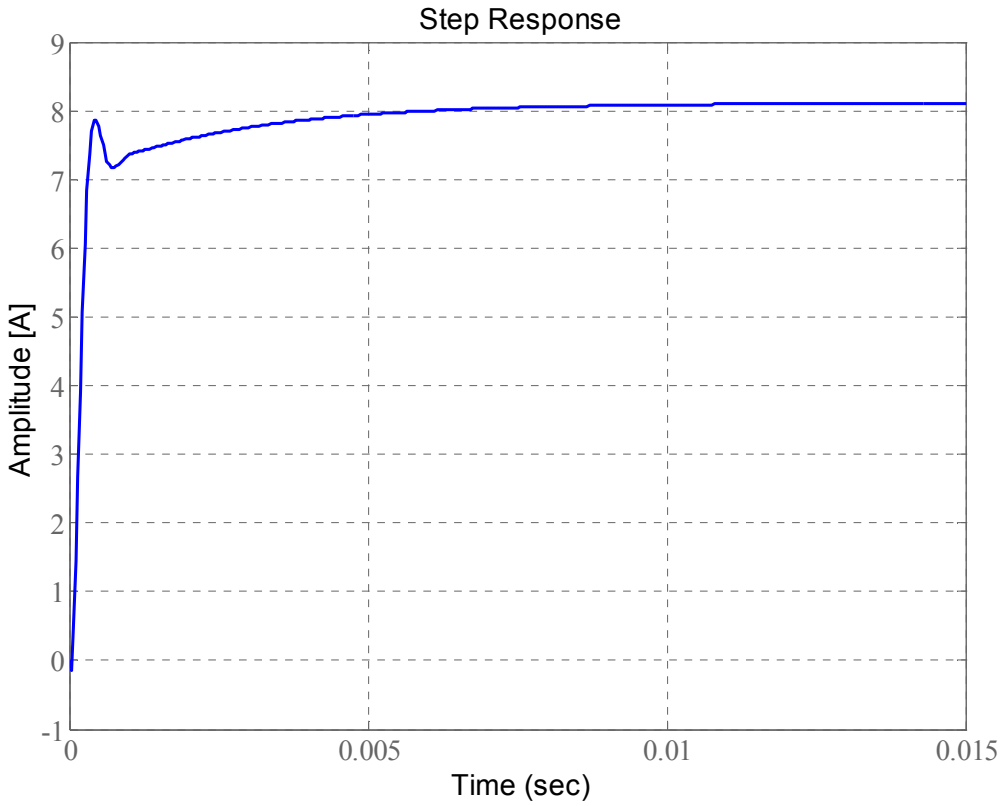

Figure 4.7. Step change response of the compensated closed current loop

To complete the current loop design compensation is needed to decouple the currents. The cross coupling terms appearing in equation (3.42) tend to slow and disturb the loop responses. Several decoupling techniques have been developed such as cross coupling decoupling [65], series decoupling [66] and state feedback decoupling [67]. To ensure decoupled control of quadrature and direct axis current, cross coupling decoupling using d-q axis is implemented. Feedforward terms (4.22) are added to the output of the q-axis and d-axis controller respectively as shown in Figure 4.8 [68].

$$v_{df} = \frac{wL_S i_q}{G}$$
$$v_{qf} = \frac{V_{sq}}{G} - \frac{wL_S i_d}{G} \tag{4.22}$$

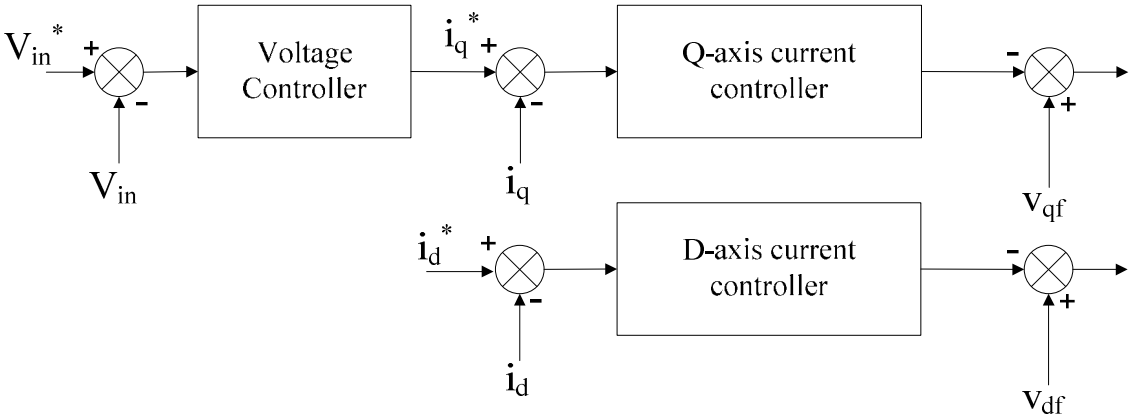

Figure 4.8. Current axis decoupling through feedforward terms [68]

With the current loop crossover frequency and phase margin obtained, the outer voltage loop for the q-axis current is designed from the block diagram that was derived and shown in Figure 4.9. To achieve satisfactory response, the outer voltage loop should be at least 10 times slower than the inner current loop [69]. This is equivalent to a voltage loop bandwidth specification of 70 Hz based on the current loop bandwidth. However 70 Hz voltage bandwidth specification is slow because of the 700 Hz current loop bandwidth. The voltage loop bandwidth specification is then increased to 140 Hz, which is equivalent to 5 times slower than the current loop bandwidth. 140 Hz voltage loop bandwidth corresponds to a settling time specification of less than 5 line frequency cycles acceptable for three-phase PWM rectifier. The Phase margin specification is a minimum of 60 degree so that voltage overshoot and ringing is avoided as it could be detrimental to components.

The set point of the outer voltage loop is the peak DC output voltage of the full-bridge rectifier. The outer voltage loop effectively controls the peak DC voltage to a value such that the quasi-Z-circuit controller can set the correct step down ratio. The peak DC output voltage of the full-bridge rectifier changes as a result of the variations of input AC voltage. This implies constantly calculating the set point V_{in}^{*} using equation (4.2), equation (4.7) and equation (4.8) into equation (4.23). The voltage set point expression is given by:

$$V_{in}^{*} = \frac{V_o}{1-2D_{nom}} \tag{4.23}$$

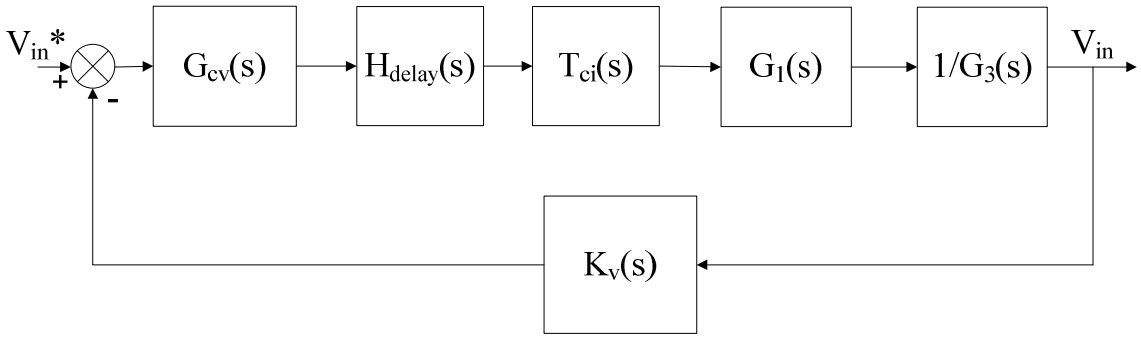

Figure 4.9. Outer voltage loop control block diagram

In the control loop of Figure 4.9 V_{in} is indirectly measured by using in equation (4.23) the measured output DC voltage and the shoot-through duty ratio from the controller output. The transfer function G_1 and G_3 are given in equations (3.46) and (3.48) respectively. The q-axis current closed-loop transfer function T_{ci} is given by

$$T_{ci}(s) = \frac{\frac{G_{ci}H_{delay}ModG_P}{K_I}}{1+\frac{G_{ci}H_{delay}ModG_P}{K_I}} \tag{4.24}$$

The transfer function K_V models the voltage sensor and the 1st order low pass filter and is given by:

$$K_V(s) = k_v \frac{1}{1+sR_{1f}C_{1f}} \tag{4.25}$$

The transfer function of the uncompensated voltage loop is then given by:

$$L_v(s) = T_{ci}H_{delay}G_1G_3K_V \tag{4.26}$$

The voltage sensor gain k_v is set to 0.0033523 and the filter parameter R_{1f} to $1\,k\Omega$, C_{1f} to $0.1\,\mu F$. Bode plot of the transfer function of the uncompensated voltage loop is shown in Figure 4.10.

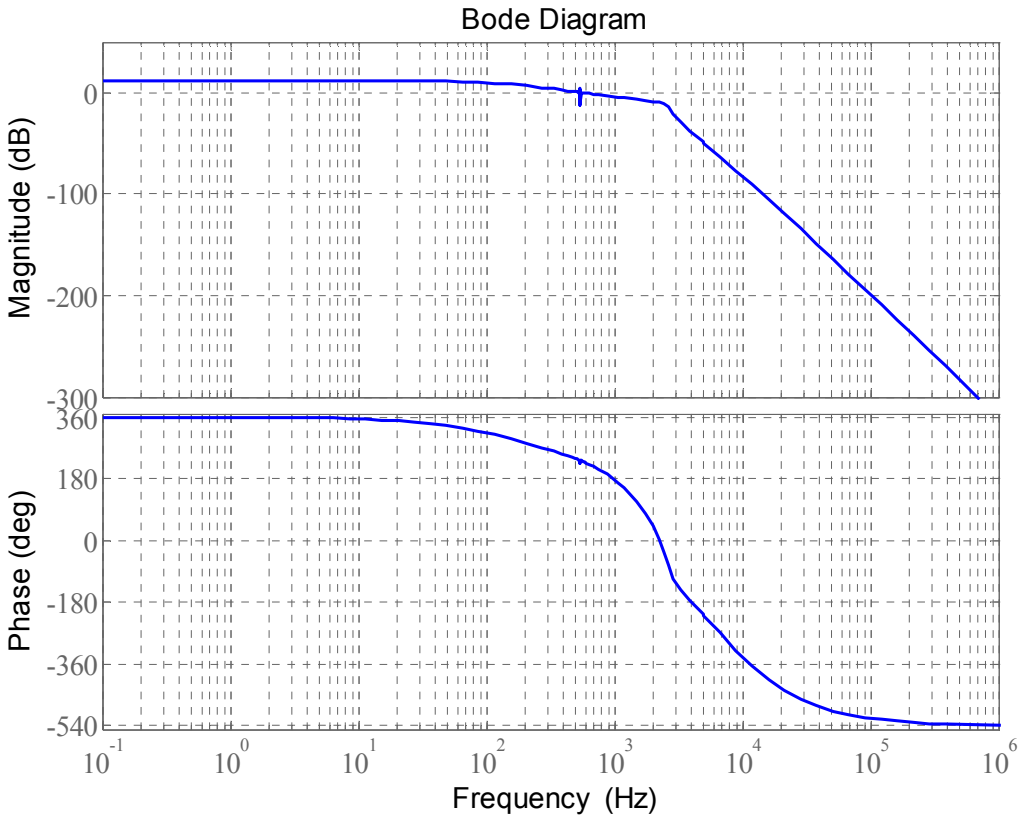

Figure 4.10. Bode plot of the transfer function of the uncompensated voltage loop

Bode plot of the transfer function of the uncompensated voltage loop in Figure 4.10 shows a crossover frequency of 550 Hz and a margin of 52 degree. This is satisfactory compared to the voltage loop specification because the uncompensated voltage loop bandwidth is close to the inner current bandwidth of 700 Hz. A PI controller is then designed so that the voltage loop meets the specifications and achieves low steady state error [69]. To preserve the phase at the desired crossover frequency of 140 Hz, the PI controller corner frequency is set to 14 Hz. The controller gain is obtained by calculating the attenuation required at 140 Hz to obtained 0 dB. The PI controller is given by equation (4.27) and its bode plot response is shown in Figure 4.11

$$G_{CV} = 0.3737\left(1+\frac{6.28\times 14}{s}\right) \tag{4.27}$$

In z-domain, the controller of equation (4.27) is given by:

$$G_{cv}(z) = \frac{0.3753 - 0.3737z^{-1}}{1 - z^{-1}} \tag{4.28}$$

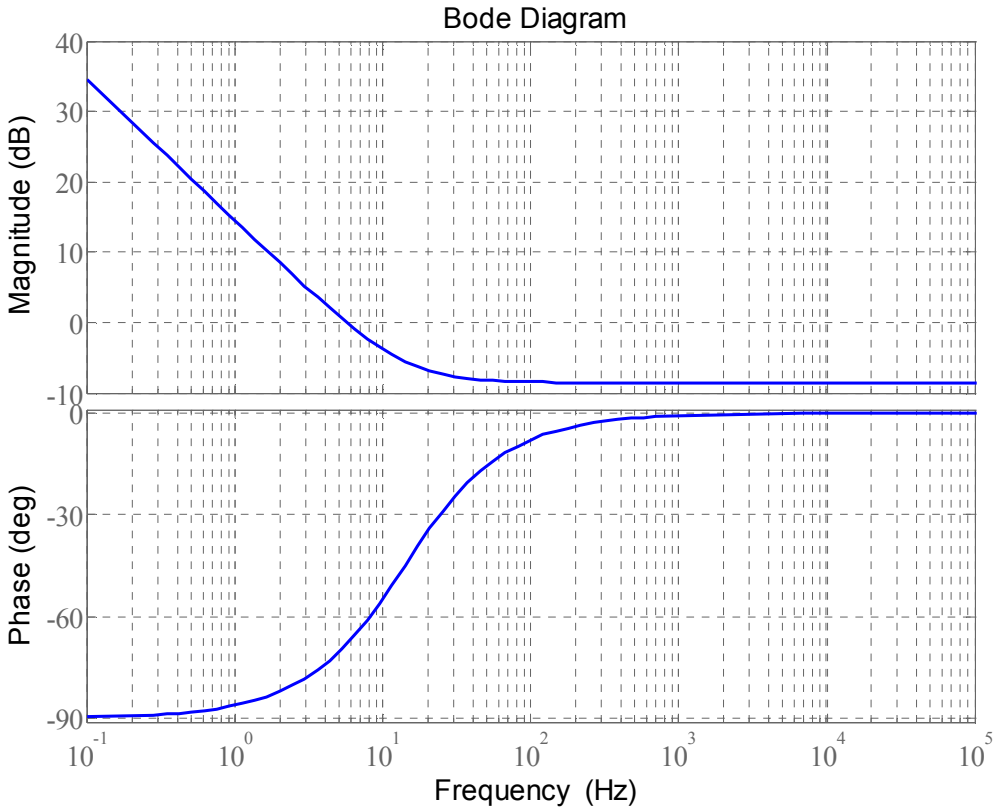

Figure 4.11. Bode plot of the transfer function of the Voltage loop PI controller

The compensated voltage loop response is shown in Figure 4.12 in which the phase margin is 115 degree and the crossover frequency is 140 Hz. The phase margin and crossover frequency obtained are therefore satisfactory for fast and smooth voltage loop response. This is confirmed by the step change response in Figure 4.13 in which no voltage overshoot is observed and the 95% settling time is 37 ms, which is less than 2 line frequency cycle.

In Figure 4.14 bode plot of the compensated outer voltage loop is shown in the case when the QZSR operates with shoot-through duty cycle higher than 0 and the three-phase AC input voltage to its maximum value of 100 V. This is to ensure that with the controller of equation (4.27) the voltage loop remains stable and can deliver satisfactory performance throughout the input AC voltage variation range.

The crossover frequency obtained for QZSR mode in Figure 4.14 is 85 Hz with a 140 degree phase margin, and confirms that the controller is satisfactory throughout the input voltage range. The outer voltage loop crossover frequency obtained in QZSR mode is then by almost half slower to the voltage loop crossover frequency in PWM rectifier mode. However the reduced bandwidth in QZSR mode does not bring any significant limitation as the voltage bandwidth is around the power converter outer voltage loop specification of 10 times slower than the inner-loop.

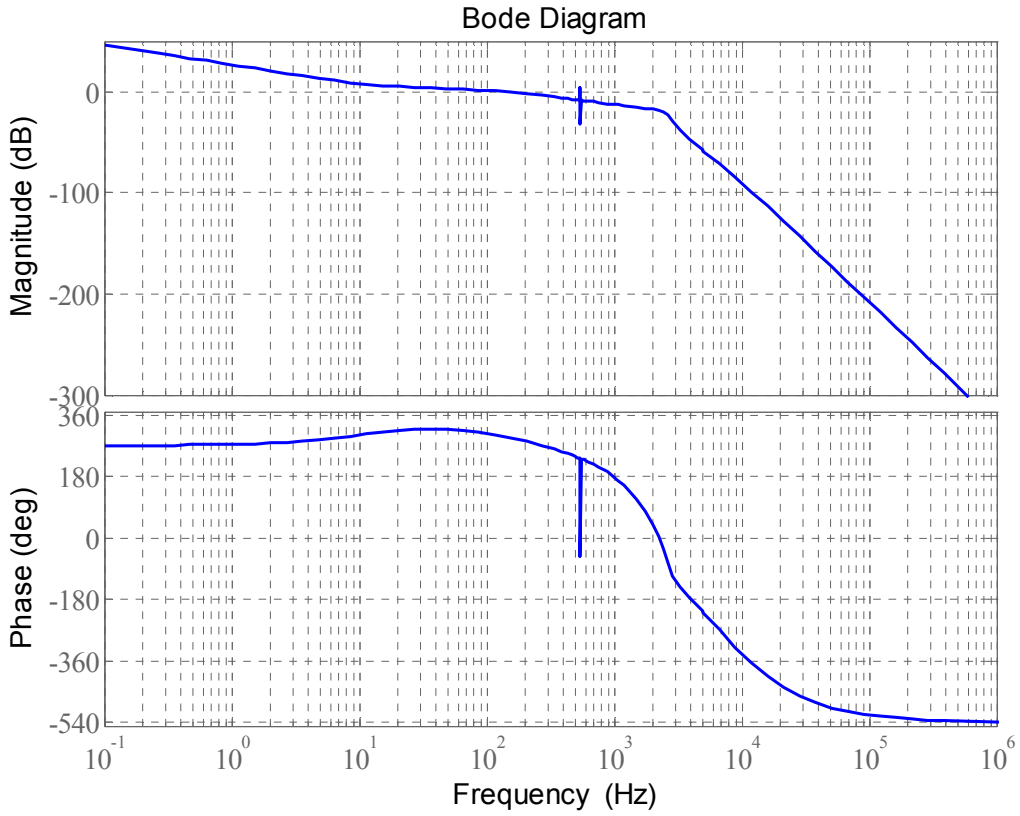

Figure 4.12. Bode plot of the transfer function of the Compensated outer voltage loop

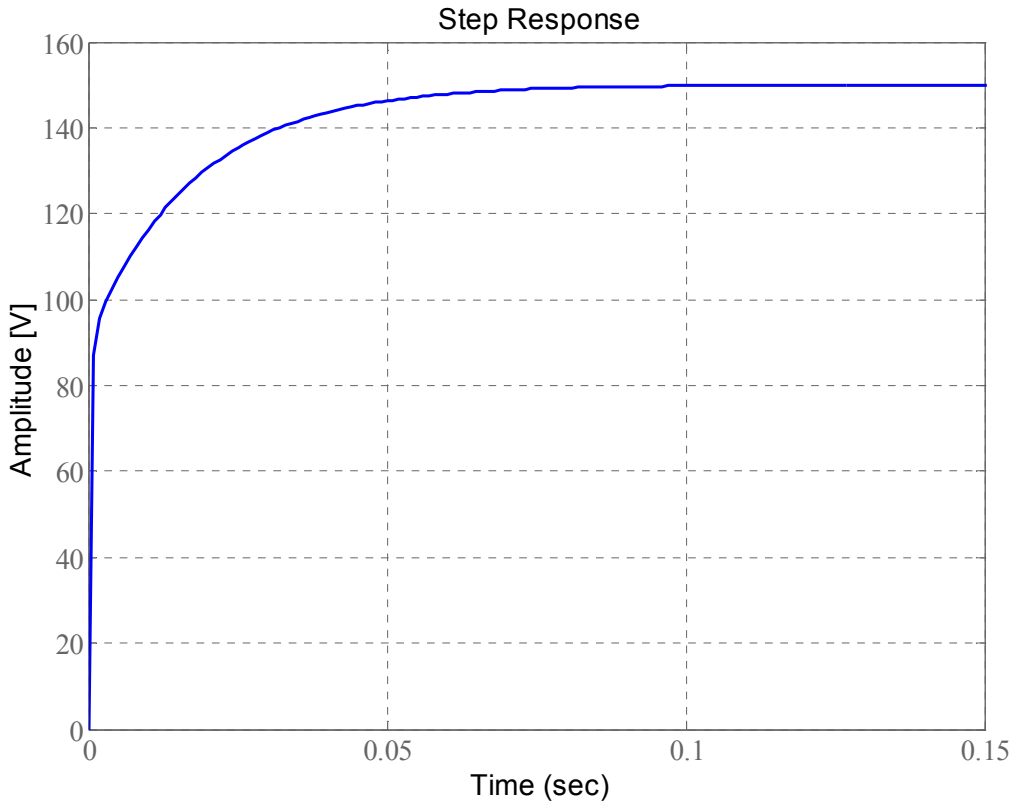

Figure 4.13. Step change response of the compensated closed voltage loop

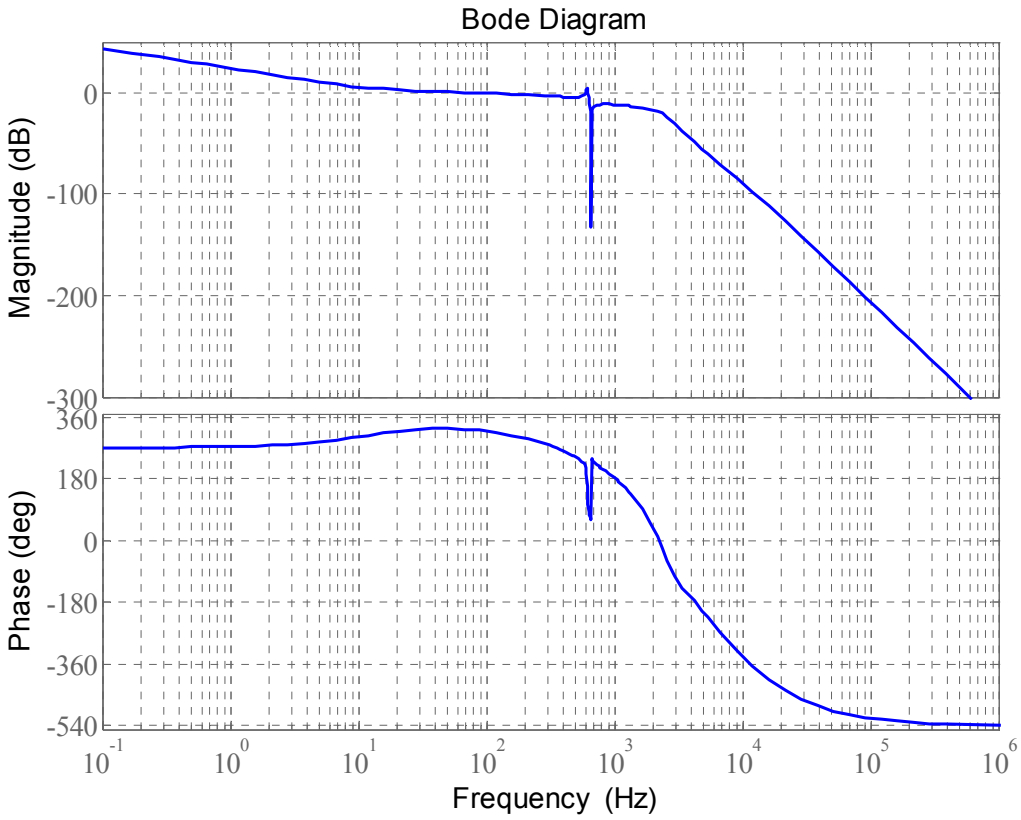

Figure 4.14. Bode plot of the transfer function of the compensated voltage loop when Vs = 100 V

4.3. QUASI-Z-CIRCUIT CONTROLLER DESIGN

A controller is required in the quasi-Z-source circuit to regulate the final DC output voltage of the system. The quasi-Z-source circuit takes its input from the output of the full-bridge rectifier. The controller action is needed in the range where the three-phase input voltage is above 92 V. To avoid an overlap between the DC and AC side dynamic, the quasi-Z-source circuit voltage loop crossover frequency is limited to below the crossover frequency of the inner q-axis current loop. However the quasi-Z-source circuit voltage loop bandwidth is chosen comparable (within 20%) to the bandwidth of the outer voltage loop of the full-bridge circuit during QZSR mode for efficient voltage loops response coordination.

The quasi-Z-circuit voltage loop bandwidth specification is therefore set to a minimum of 70 Hz and the phase margin to a minimum of 60 degree to limit voltage overshoot. As a

result of the lower loop response speed required for the quasi-Z-circuit a voltage mode control is adopted despite the non-minimum phase response present in the transfer function relating the output capacitor to control. The low bandwidth effect of the RHP is utilised with the adopted control strategy. The quasi-Z-source circuit control block diagram that was derived is shown in Figure 4.15.

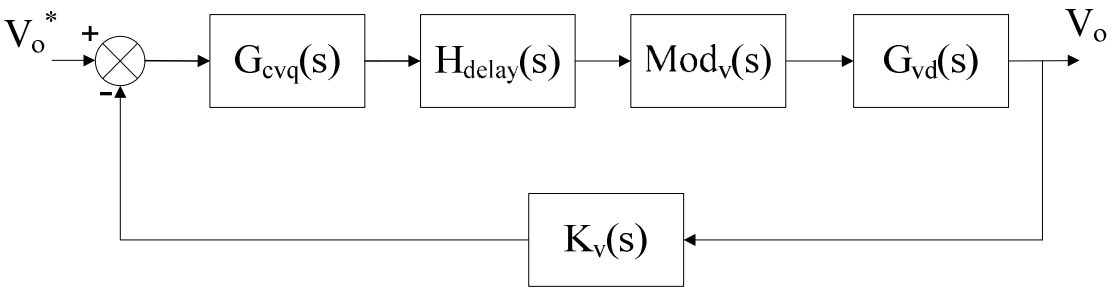

Figure 4.15. Quasi-Z-circuit voltage control loop

In the block diagram of Figure 4.15 G_{vd} is the transfer function relating the output capacitor to control given in equation (3.37a), K_V the sensor gain and filter transfer function of equation (4.25), Mod(s) the PWM modulator transfer function and G_{cvq} the digital voltage controller transfer function. The sensor gain of $k_v = 0.0033583$ is effectively an equivalent digital gain taking into account the transformation of the physical analog sensor, the ADC voltage and number of bits. In order to design the controller, the modulator transfer function is derived from the modified modulation method suggested in [20]. The modulator output for the traditional modulation method for simple boost shown in Figure 4.16 similar to the Figure 3 in [20] and is given by equation (4.29) [20]:

$$D_o = 1 - \frac{V_m}{V_{tri}} \tag{4.29}$$

Deriving a transfer function for the traditional modulation method from equation (4.29) is difficult. Therefore the modified modulation method in Figure 4.16 is used. The transfer function for the modified modulation of Figure 4.16 is expressed by [20]:

$$Mod(s) = \frac{D_o}{V_m} = \frac{2}{V_{tri}} \tag{4.30}$$

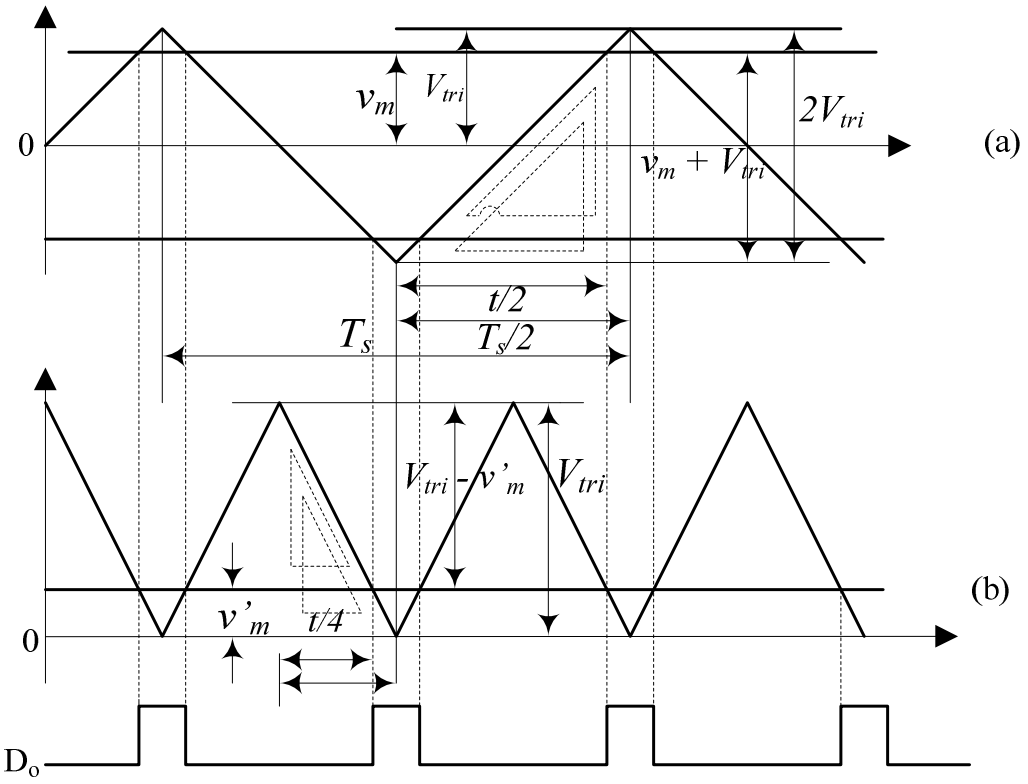

Figure 4.16. Quasi-Z-circuit modulation method; (a) Traditional modulation method for simple boost; (b) Modified modulation for simple boost

In equation (4.29) and equation (4.30) V_m is the modulating signal, V_{tri} the peak value of triangle carrier wave and D_o the shoot-through duty cycle. The modified modulation thus requires doubling the carrier frequency and only one positive modulating signal compared to the traditional modulation method. Using the modulator transfer function of equation (4.30), the transfer function of the uncompensated voltage loop of the quasi-Z-circuit is given by:

$$L_v(s) = H_{delay} ModG_{vd} K_V \tag{4.31}$$

Bode plot of the transfer function of the uncompensated voltage loop of the quasi-Z-circuit is shown in Figure 4.17 and it is unsatisfactory in term of the bandwidth and phase margin specifications of the voltage loop. A controller is therefore needed to increase the phase margin and reduce the crossover frequency to the desired specification.

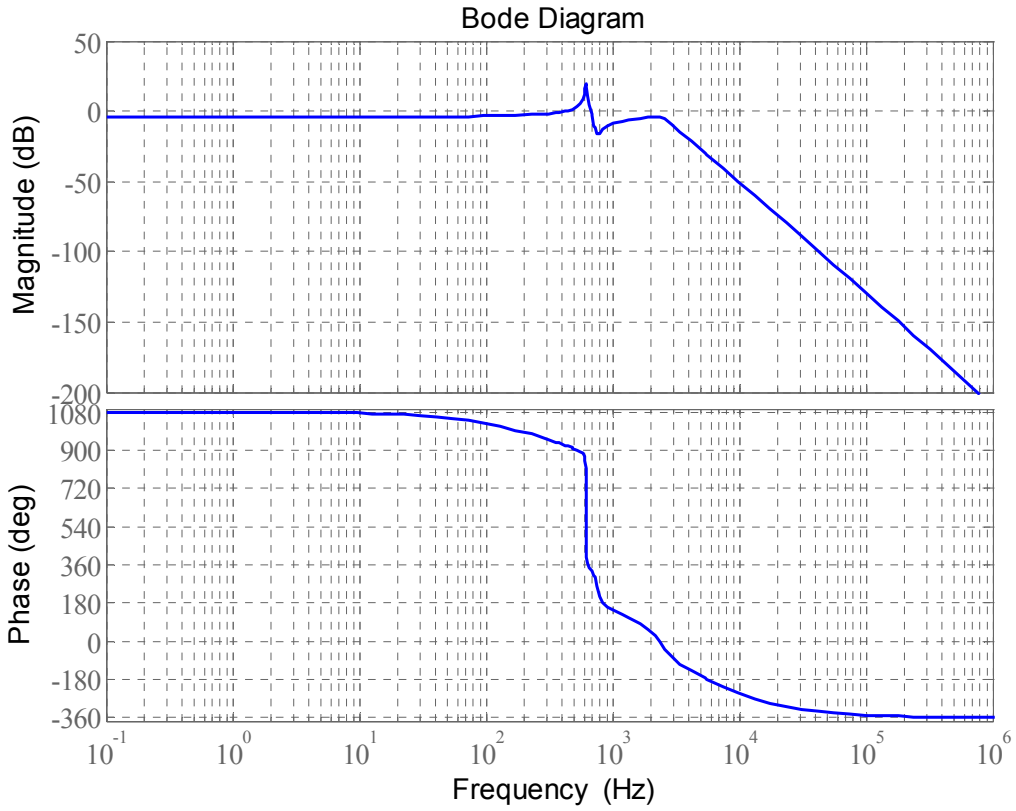

Figure 4.17. Bode plot of the transfer function of the quasi-Z-source circuit uncompensated voltage loop

To achieve the control objective the PI controller in equation (4.32) is designed to additionally reduce the steady state error to very low value [69]. Bode plot of the voltage loop PI controller is shown in Figure 4.18.

$$G_{CV} = -0.0153\left(1+\frac{6.28\times 7000}{s}\right) \tag{4.32}$$

In z-domain, the controller of equation (4.32) is given by:

$$G_{cv}(z) = \frac{0.0489 - 0.0153z^{-1}}{1 - z^{-1}} \tag{4.33}$$

The negative controller gain is justified by the nature of the circuit requiring a direct acting controller [41]. This can be explained as follow [41]: when the error is positive, if the output decreases, the controller output has to decrease. When the error is negative, if the output increases, the controller output has to increase. Bode plot of the transfer function of the compensated voltage loop transfer function is shown in Figure 4.19 where the crossover

frequency is 70 Hz and the phase margin is 52 degree. The crossover frequency specification is satisfied at the cost of an 8 degree reduced phase margin relative to the specification. Satisfying the phase margin specification will result in a bandwidth reduction compromising the response time. However, the bandwidth and phase margin achieved are acceptable, as the reduced phase margin translate to an increased overshoot as shown in the step response of Figure 4.20. The 95% settling time is 7 ms, and the voltage overshoot is 15%, which is well within passive components safety factor and therefore tolerable. The DC voltage settling time is less than half the line frequency and is therefore satisfactory with PWM rectifier voltage response time.

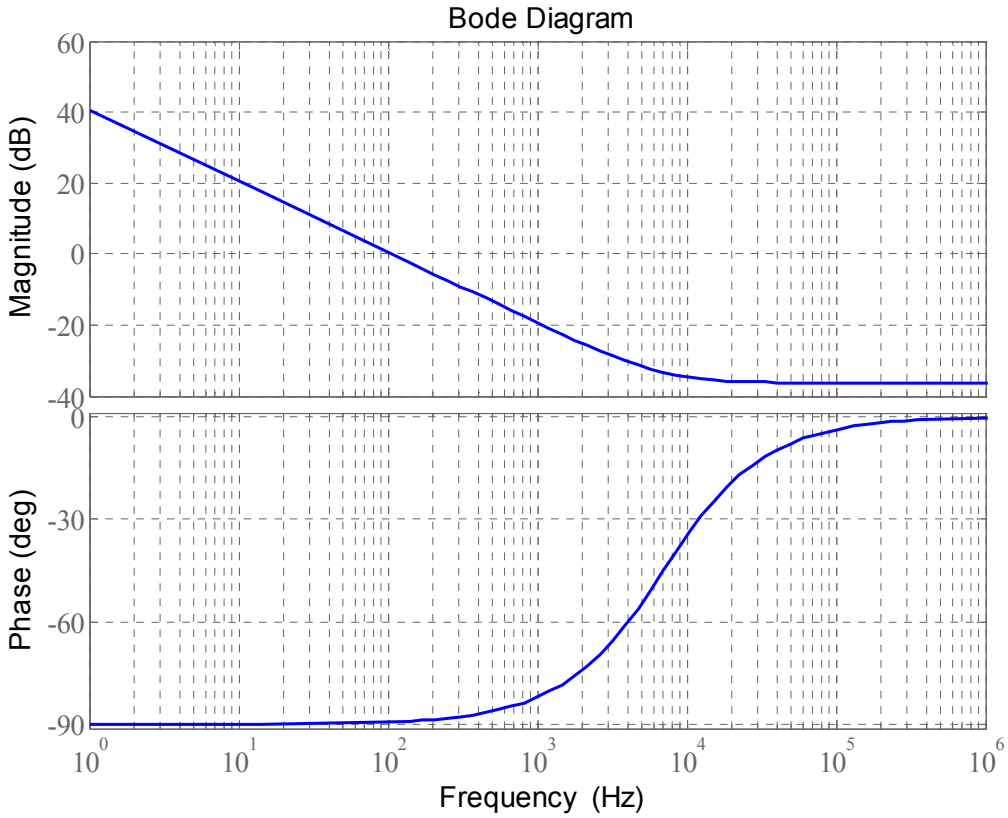

Figure 4.18. Bode plot of the transfer function of the Voltage loop PI controller

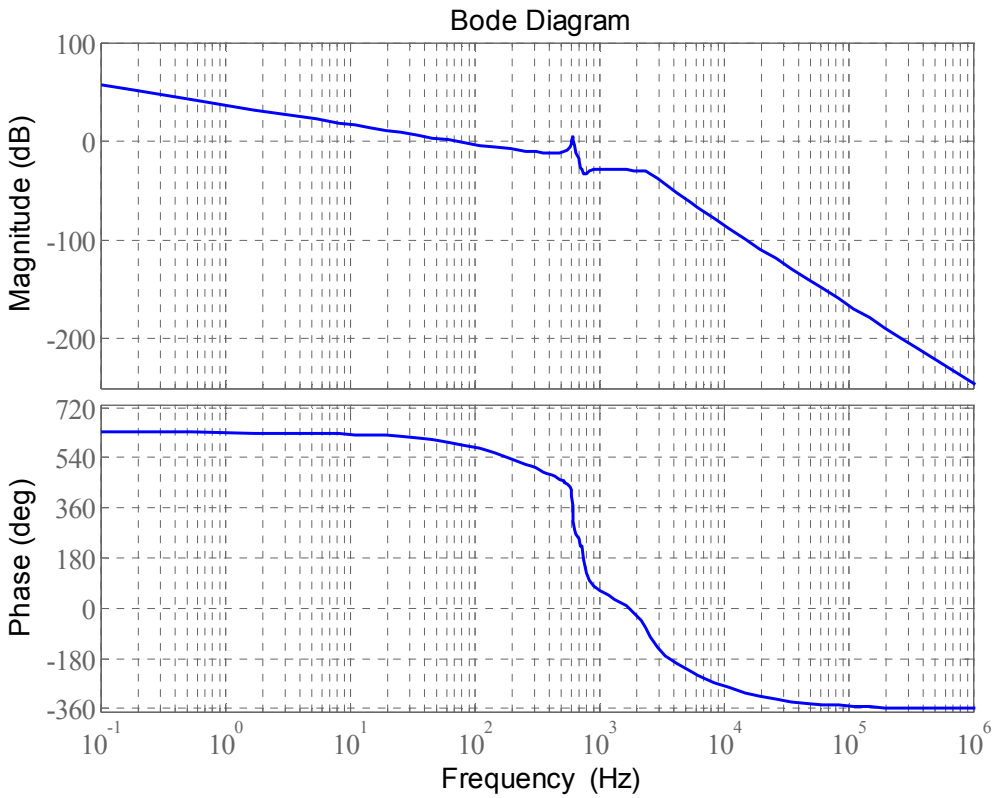

Figure 4.19. Bode plot of the transfer function of the Compensated voltage loop

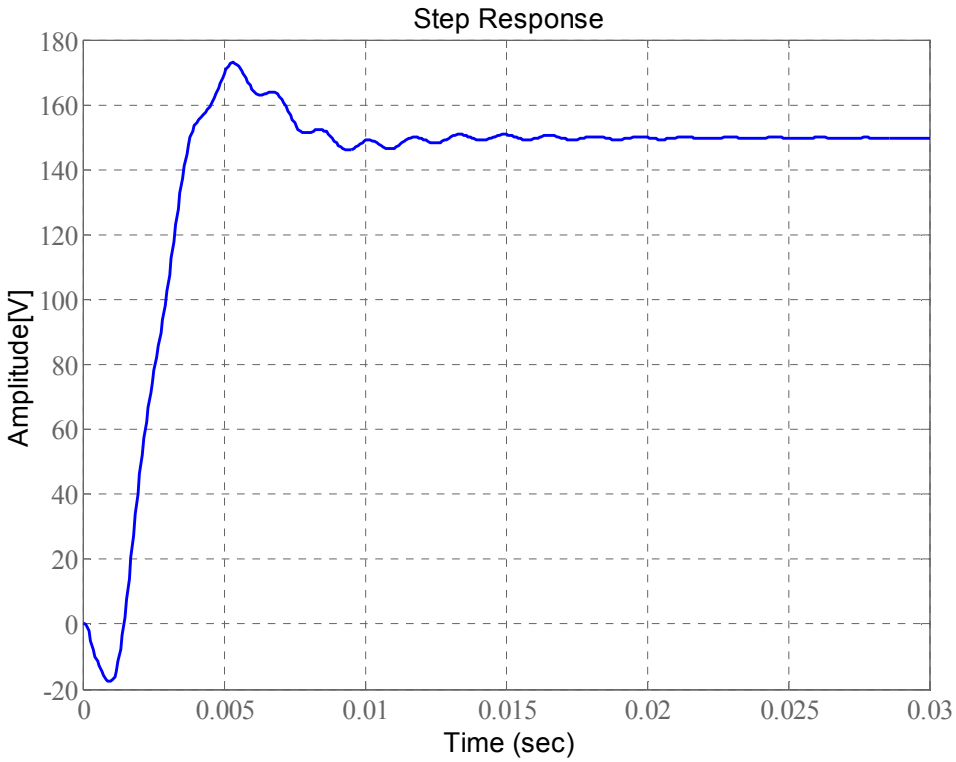

Figure 4.20. Step change response of the compensated closed voltage loop of the quasi-Z-source circuit

4.4. CHAPTER CONCLUSION

It has been shown in this chapter that the digital controllers designed are able to achieve the objective of the quasi-Z-source rectifier of maintaining the desired DC voltage, and drawing sinusoidal current with unity power factor from the supply. This has been attested by the step responses where satisfactory dynamics are exhibited by the converter. These closed-loop dynamics performances of the quasi-Z-source rectifier compare well with the conventional three-phase rectifier. These controllers are then implemented in simulation and in the practical circuit to validate the performance of the rectifier.

CHAPTER 5 SIMULATION AND EXPERIMENTAL RESULTS

5.1. INTRODUCTION

To validate the model that was developed and the controller that was designed, software and hardware simulations of the rectifier were performed. The software simulations were performed using the Power simulator (Psim) software. In the simulation the rectifier is supplying a nominal power of 1000 W during QZSR mode and 700 W during PWM rectifier mode to a load modelled with a resistance. Logic OR gates are used to implement shoot-through state in software. Implementation of the modified modulation technique for the quasi-Z-source circuit requires that the switching frequency of the triangular carrier wave of the quasi-Z-circuit modulator is double of the carrier wave of the modulator of the full-bridge rectifier. In the practical experimental system shown in Figure 5.1 the digital controller is implemented using Freescale DSP 56F807. This DSP is well-suited for digital control of the QZSR given the low switching frequency used, the available optimised code for vector control computation, and the large number of dedicated peripherals in a single development board.

The converter parameters used in the simulation are exactly the same as in Table 3.1 for the quasi-Z-circuit components and as in Table 4.2 for the rest of the converter. Due to the variable three-phase input voltage, the equivalent value for the nominal modulation index, nominal shoot-through duty cycle, and set point value V_{insp} of the full-bridge DC output voltage are shown in Table 5.1. V_{insp} and its measured value are updated as the three-phase input AC voltage varies. During the PWM rectifier mode without shoot-through, the quasi-Z-source circuit switch remains on for the entire switching period and the output DC voltage of the quasi-Z-source three-phase rectifier is equal to the average voltage of the full-bridge rectifier output.

Table 5.1. Nominal Shoot-through duty cycle, Modulation index and Full-bridge peak DC output voltage set point value as function of AC input voltage

3 phase Input Voltage [V] / Parameters	70	78	94	100
D_{nom}	0	0	0.0586	0.1060
M_{nom}	0.7941	0.8849	0.9414	0.8940
V_{insp}	0.5028	0.5028	0.9377	0.6392

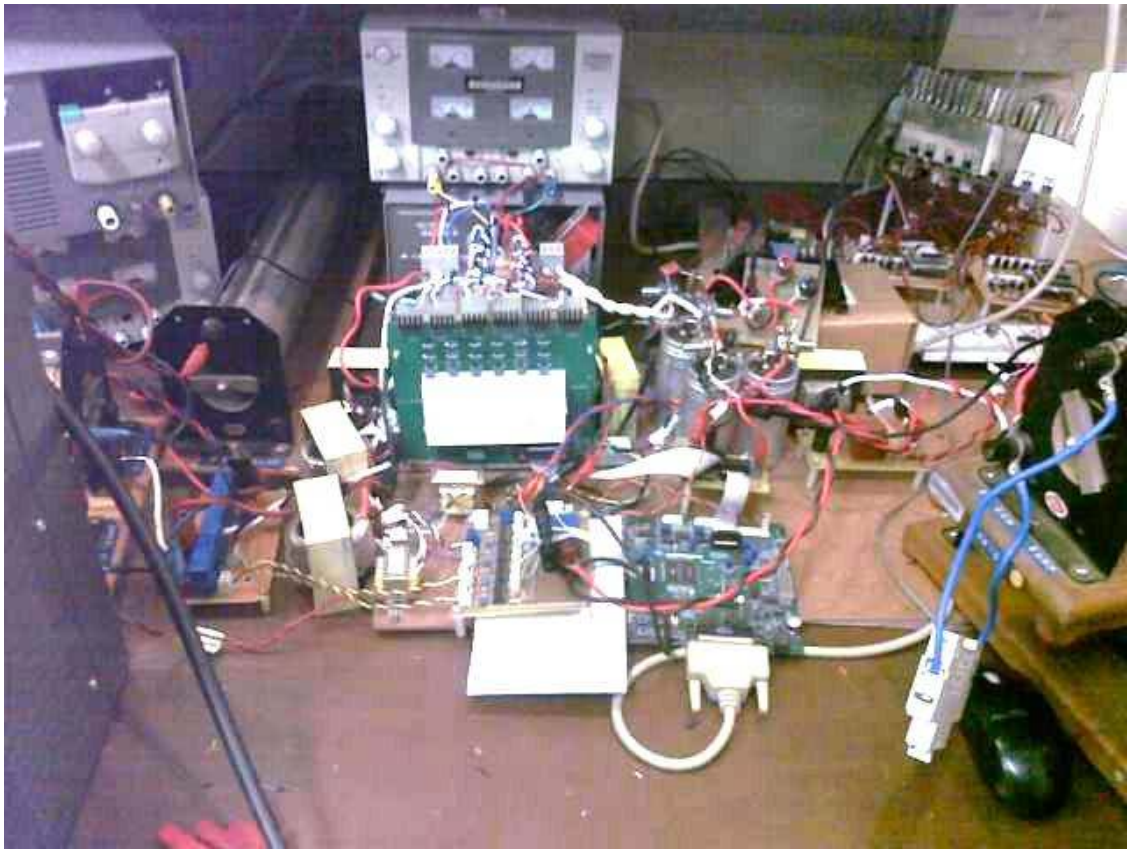

Figure 5.1. Quasi-Z-source three-phase rectifier practical circuit.

5.2. SIMULATION AND EXPERIMENTAL RESULTS DURING PWM RECTIFIER MODE

The simulations results of the quasi-Z-source three-phase rectifier when the three-phase input voltage is at 70 V are shown from Figures 5.2 to 5.11. At this AC input voltage, the QZSR operates similarly to a conventional voltage source PWM full-bridge rectifier.

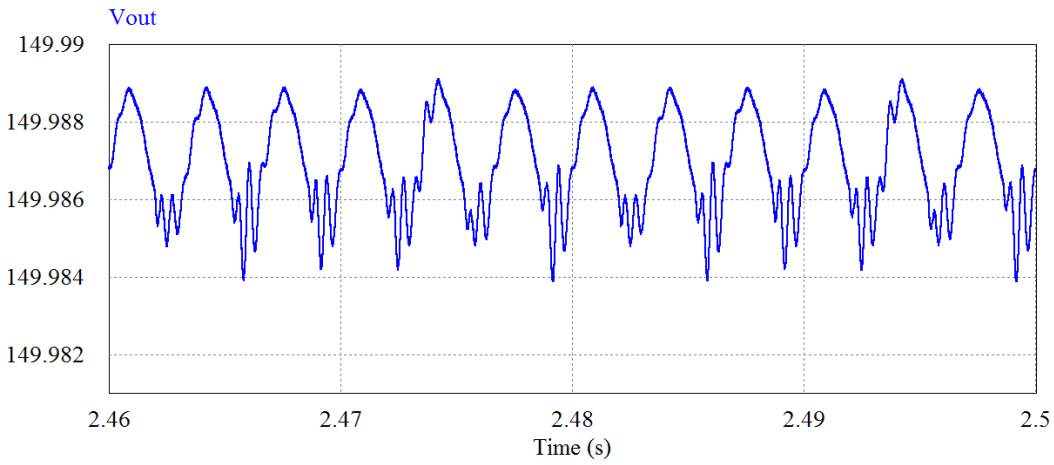

Figure 5.2. QZSR output DC voltage when V_s = 70 V

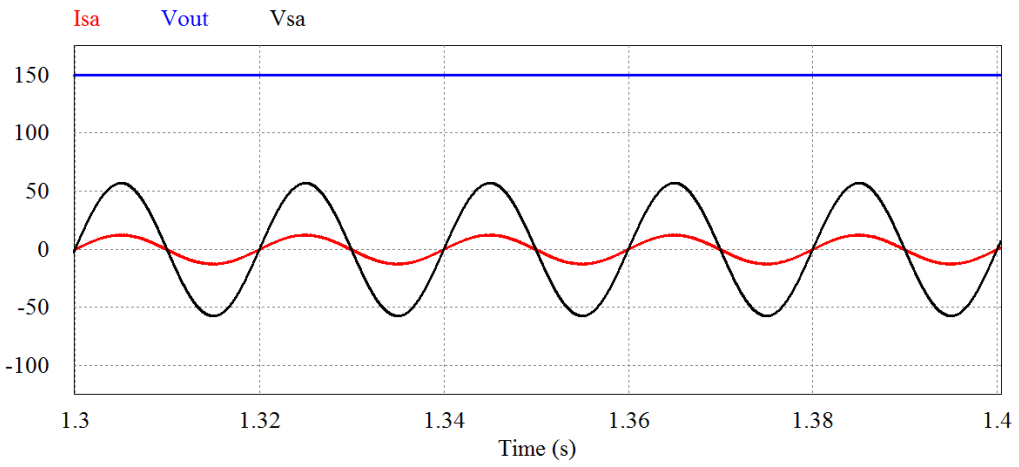

Figure 5.3. QZSR phase A AC input Voltage and Current; output DC voltage at V_s = 70 V

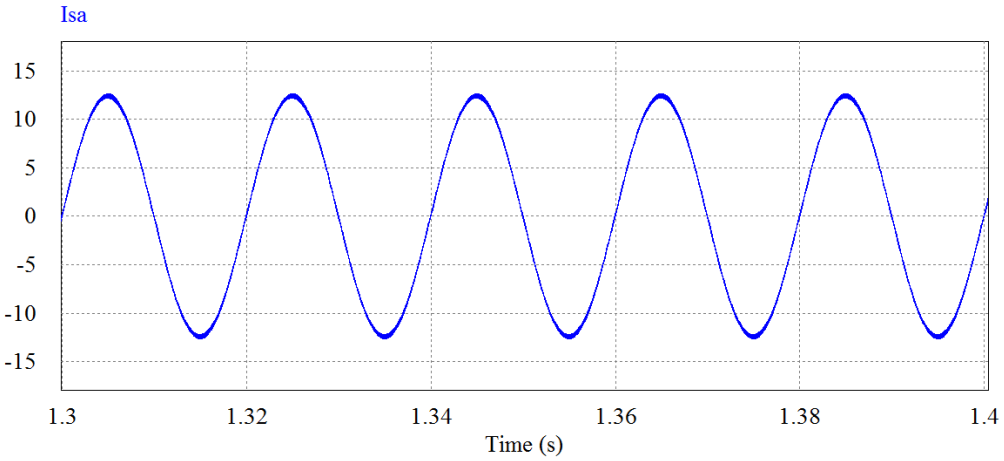

Figure 5.4. QZSR phase A AC input Current when V_s = 70 V

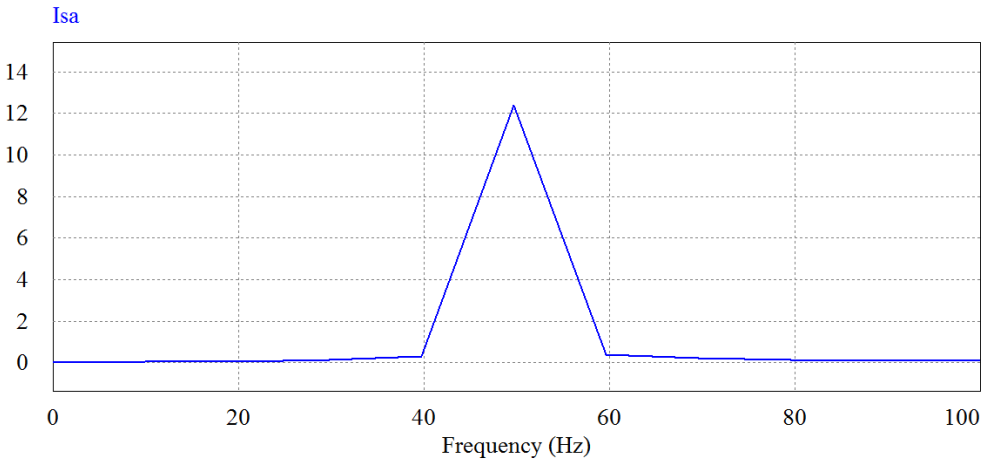

Figure 5.5. QZSR phase A AC input Current spectrum when V_s = 70 V

The AC input current spectrum is shown in Figure 5.5 and the rms value of the AC current at each harmonic frequency in Table 5.2. The current spectrum in Figure 5.5 only presents the amplitude at 50 Hz because the switching frequency ripples are not significant relative to the line frequency. This is the result of the high AC side 1.4 mH inductor filters. The distortion power factor is obtained as follows:

$$p.f_{distorsion} = \frac{I_{s1}}{I_s} = \frac{8.755}{8.767} = 0.9986$$

From Figure 5.3 the phase current and phase voltage are exactly in phase, which implies a displacement (disp) power factor of 1. The total power factor of the rectifier is therefore:

$$p.f_{tot} = p.f_{distorsion} \; x \; p.f_{displacement} \cong 1$$

Table 5.2. Input AC current harmonic amplitudes

Frequency	Total rms	50 Hz	20 KHz	40 KHz	60 KHz	80 KHz	100 KHz
Is [A]	8.767	8.755	0.0283	0.0547	0.0181	0.0070	0.0060

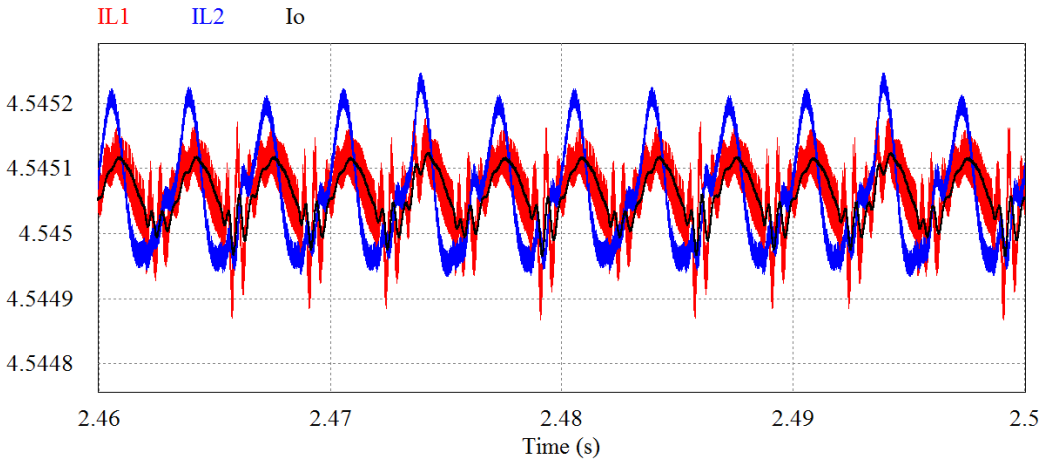

Figure 5.6. QZSR Inductors L_1, L_2 and load I_o current when V_s = 70 V

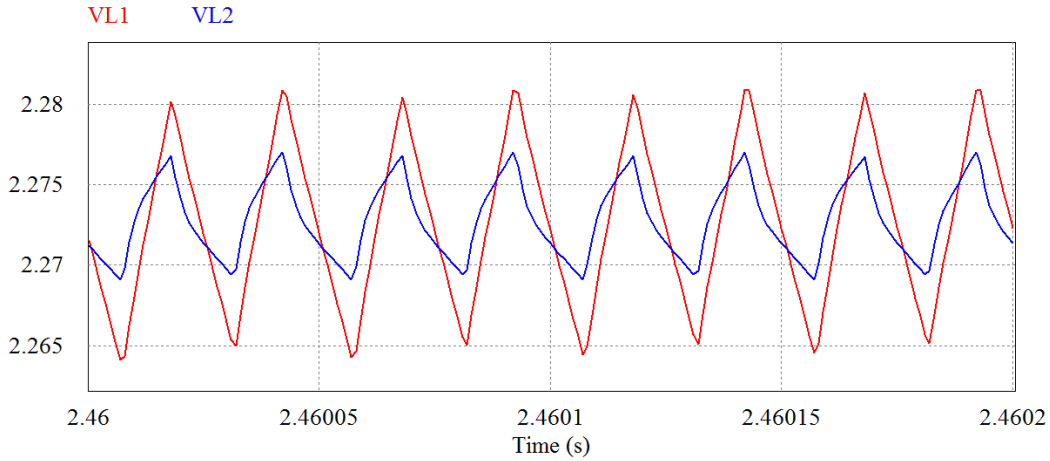

Figure 5.7. QZSR Inductors L_1 and L_2 voltage when V_s = 70 V

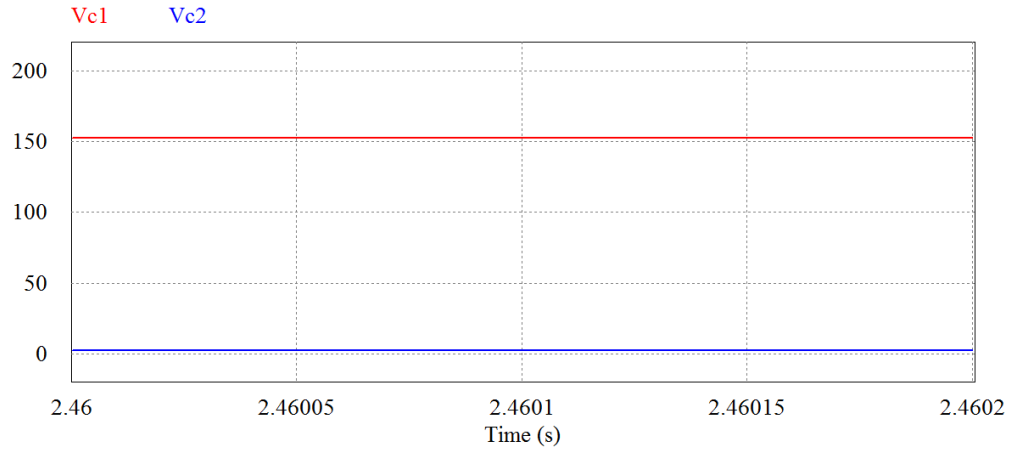

Figure 5.8. QZSR Capacitors C_1 and C_2 voltage when V_s = 70 V

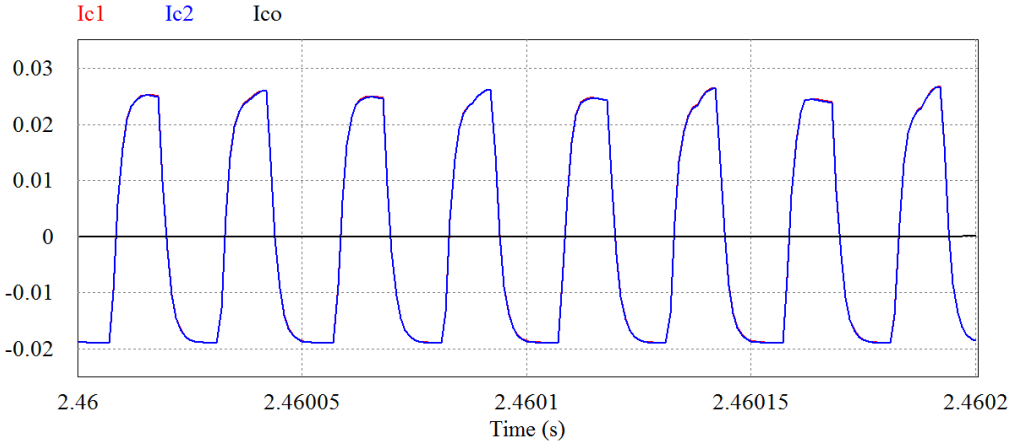

Figure 5.9. QZSR Capacitors C_1, C_2 and Co current when V_s = 70 V

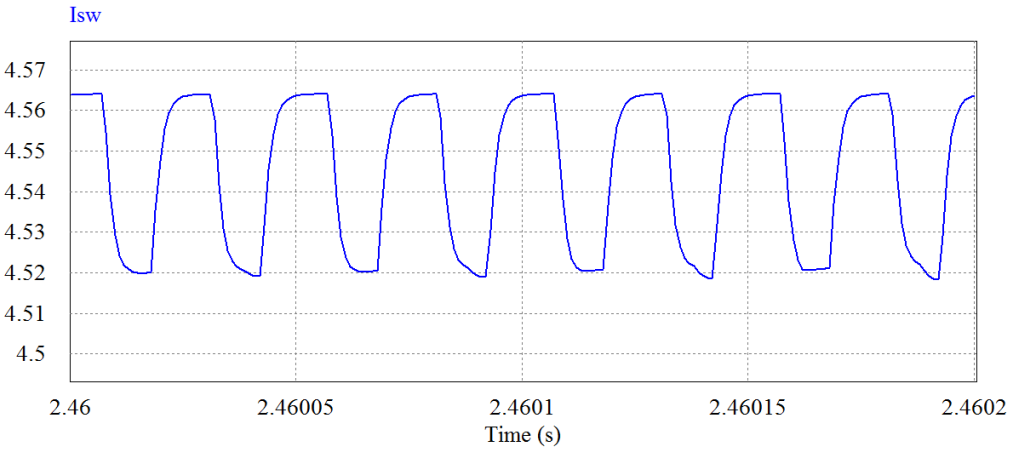

Figure 5.10. QZSR Switch Current when = 70 V

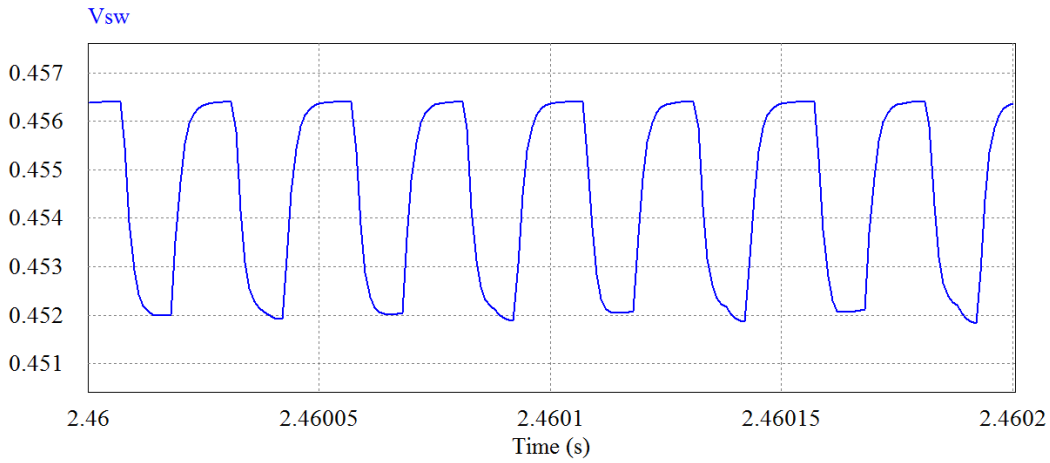

Figure 5.11. QZSR Switch Voltage when V_s = 70 V

Practical results of the QZSR in the PWM rectifier mode are shown in Figures 5.12 to 5.18. The voltage probe scaling is 1/1000 and its oscilloscope scaling is 1x500, such that the effective voltage is half of what is displayed. The current probe setting is 100 mV/A and the oscilloscope scaling is 1x10, such that the effective current scaling on the oscilloscope display is 1 V = 1 A. The oscilloscope channels are identified as follows: Yellow for Channel 1, Blue for channel 2, Pink for channel 3 and Green for channel 4. Furthermore the three-phase AC voltage supply used in the practical experimental was not an ideal voltage source. Only a high impedance three-phase variac with slow dynamic was available for the practical experiment. The voltage source quality and its effects on other measurements can be seen on the practical waveforms, and this negatively impacted on the performance of the rectifier by injecting noise. Despite an improved layout of the practical circuit, noise was the cause of DC voltage collapses resulting in large AC current drawn from the supply making it difficult to capture waveforms. Capacitors had to be inserted at each input AC voltage phase to improve the supply voltage and reduce noise in the system.

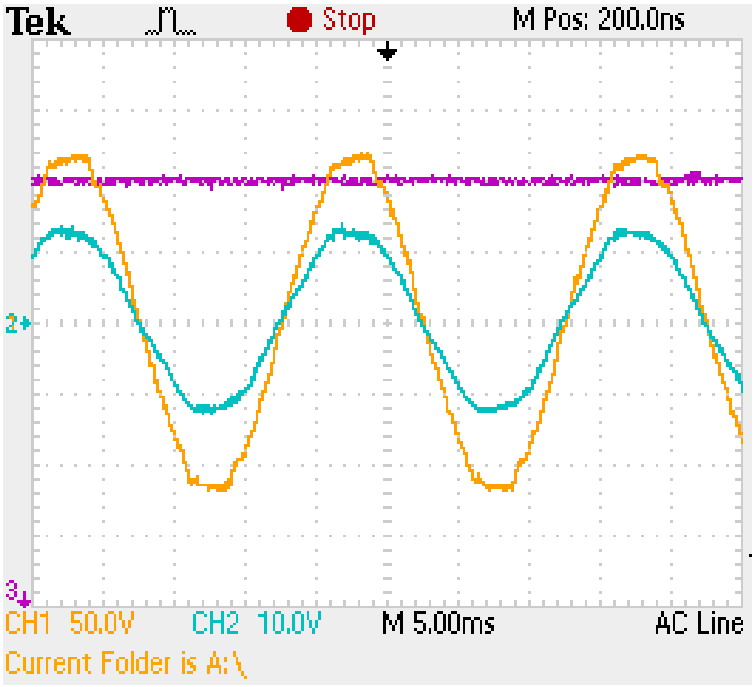

Figure 5.12. QZSR input AC voltage (line-neutral, CH1 at 50V/div), input AC current (CH2 at 5V/div) and output DC voltage (CH3 at 50V/div) with 5 ms/div

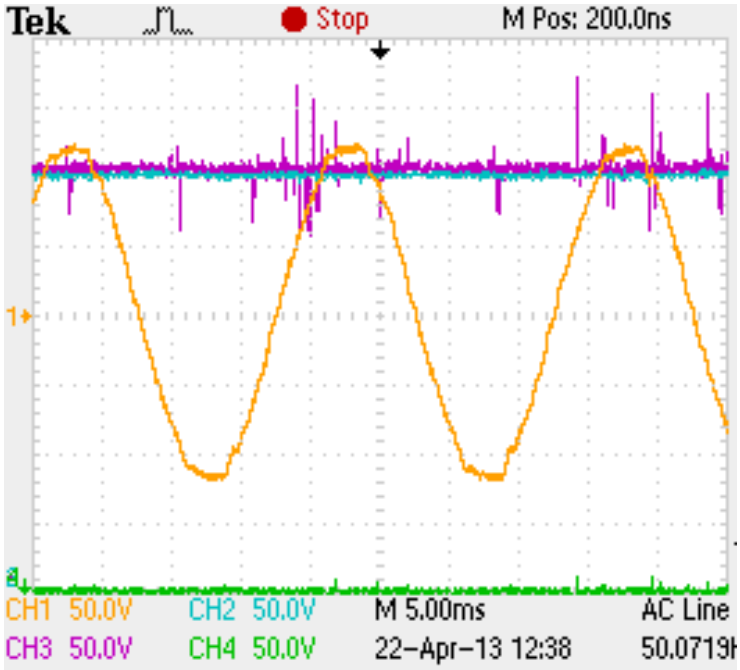

Figure 5.13. QZSR input AC voltage (line-neutral, CH1 at 50V/div), output DC voltage (CH2 at 50V/div) and Capacitor C_1 Voltage (CH3 at 50V/div) and Capacitor C_2 Voltage (CH4 at 50V/div) with 5 ms/div

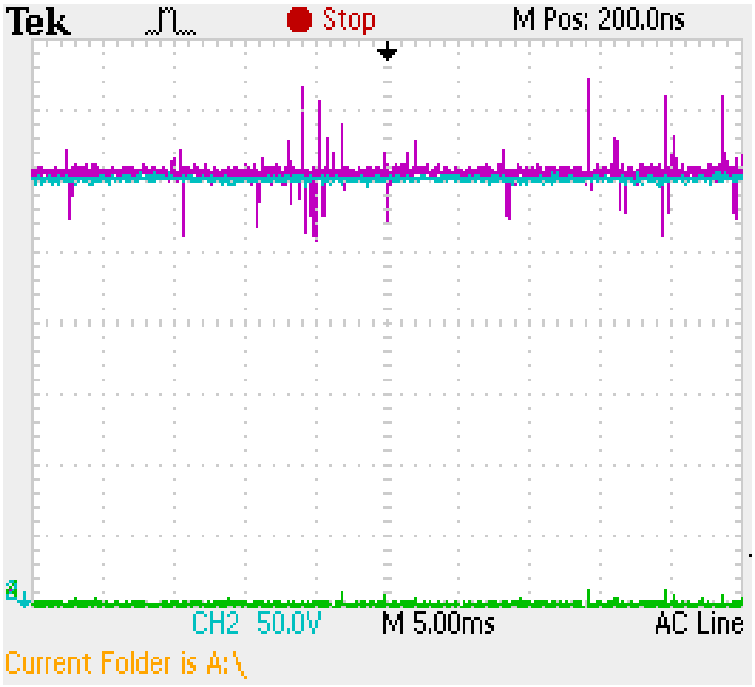

Figure 5.14. Output DC voltage (CH2 at 50V/div), Capacitor C_1 Voltage (CH3 at 50V/div) and Capacitor C_2 Voltage (CH4 at 50V/div) with 5 ms/div

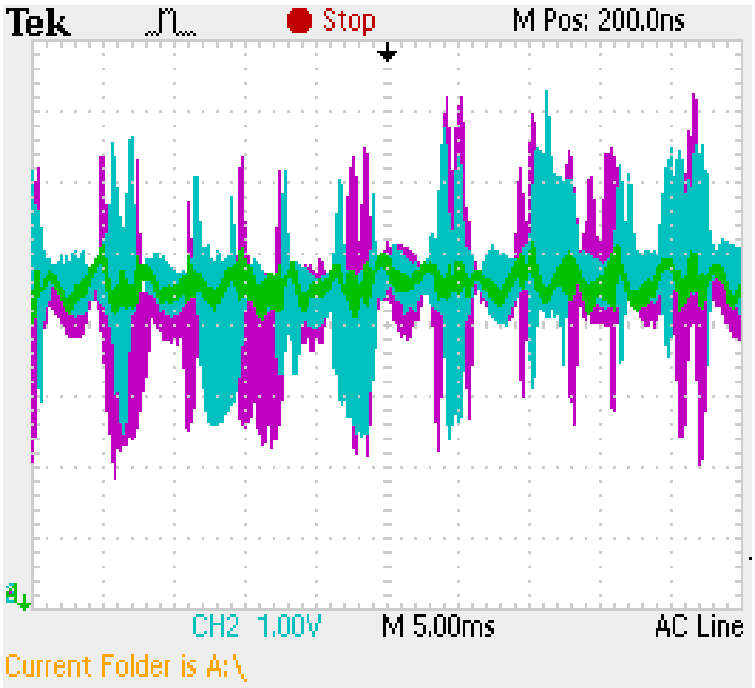

Figure 5.15. QZSR output current (CH2 at 1V/div), Inductor L_1 current (CH3 at 1V/div) and Inductor L_2 current (CH4 at 1V/div) with 5 ms/div

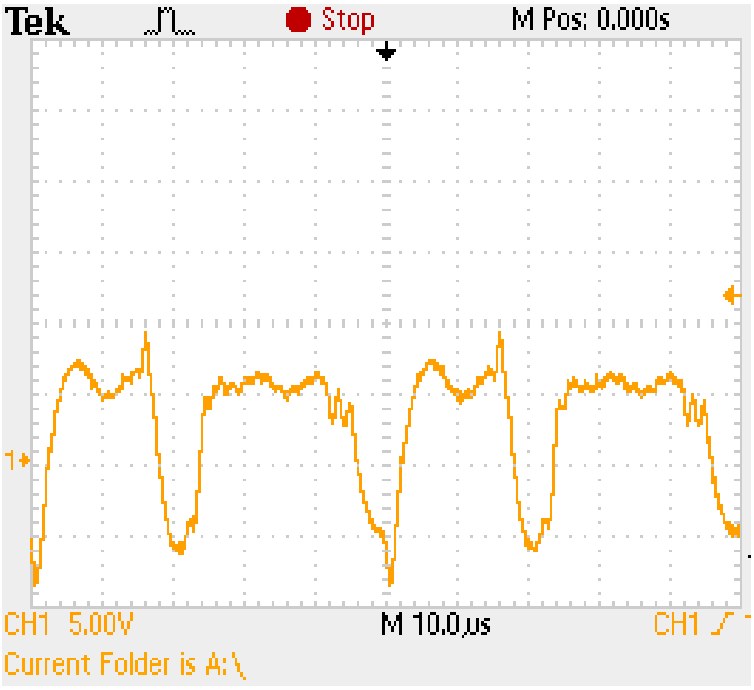

Figure 5.16. QZSR switch current (CH1 at 5V/div) with 10 us/div

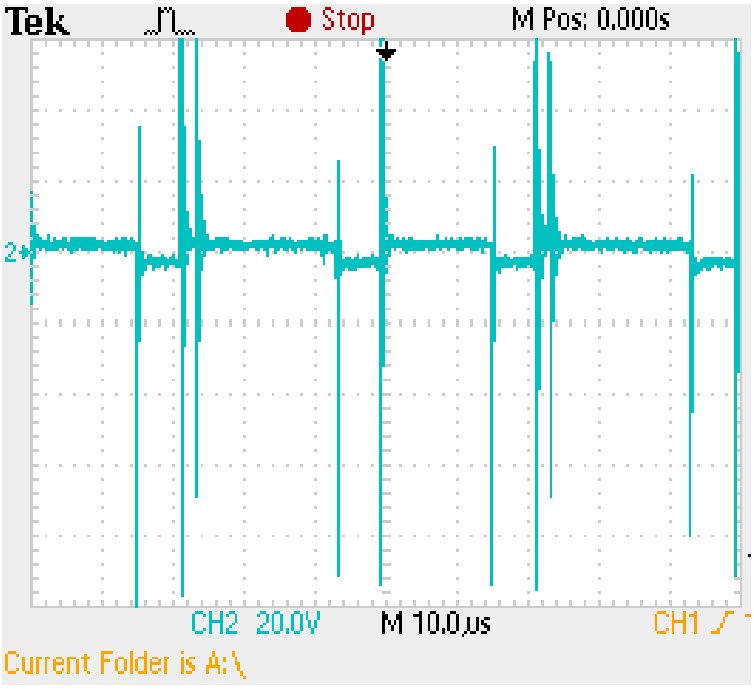

Figure 5.17. QZSR switch voltage (CH2 at 20V/div) with 10 us/div

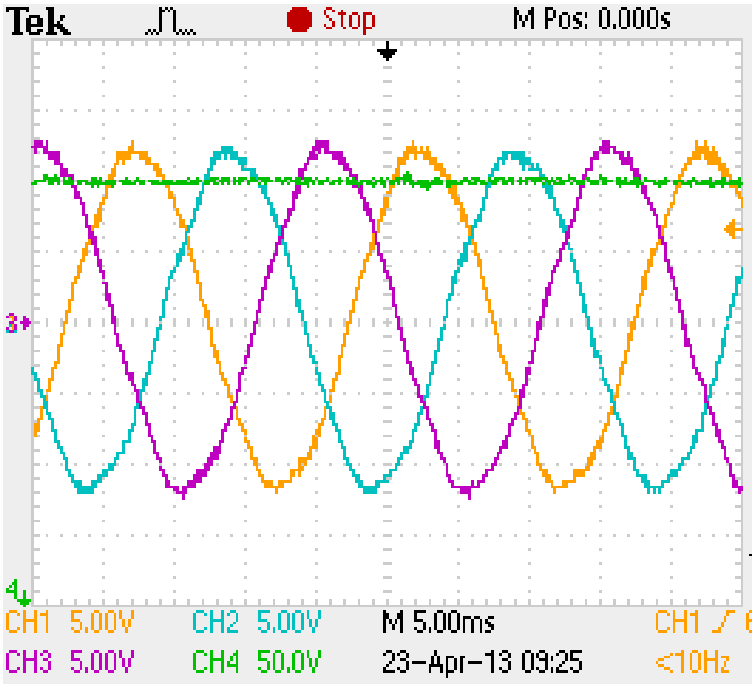

Figure 5.18. QZSR output voltage (CH4 at 50V/div), Phase A (CH1 at 5V/div), Phase B (CH2 at 5V/div) and Phase C (CH3 at 5V/div) with 5 ms/div

The average value of the output DC voltage of the system in Figure 5.2 is equal to 149.98 V with a peak-to-peak voltage ripple of 0.006 V, which is less than 0.01 % of the steady state value. Phase A of the input AC current is in phase with phase A of the input AC voltage as shown in Figure 5.3. The THD of the AC input current is equal to 0.14 % and the harmonic current magnitudes are well below the limit set by the IEC 61000-3-2 standard. Figure 5.6 confirms that the average current for the inductors and the load are equal, as it was found in the model. It is also confirmed by Figure 5.9 that capacitors C_1 and C_2 current are equal. From the simulation results shown in Figures 5.3 to 5.11, the quasi-Z-source three-phase rectifier operations in the full-bridge PWM mode are satisfactory and comply with the design objectives.

In the practical experimental system the average value of the output DC voltage in Figure 5.12 is equal to 150 V with a peak to peak voltage ripple of 1 V which is less than 1 % of the steady state value. The input AC voltage and current are in phase as shown in the practical waveform of Figure 5.12. This confirms that the QZSR using the controllers designed is capable of unity displacement power factor operation. The input AC current is

fairly sinusoidal, which implies that current harmonic magnitudes are well below the limit set by the IEC 61000-3-2 standard. Despite noise on the inductor and load current waveforms, the DC components of the waveforms in Figure 5.15 also confirm the theoretical finding that the average current of the inductors and the load are equal. Overall practical results waveforms are comparable to the simulation waveforms and therefore validate that the QZSR is a cost-effective rectifier capable of stepping up the input voltage. From the practical results shown in Figures 5.12 to 5.18 the Quasi-Z-source three-phase rectifier operations in the full-bridge PWM mode are satisfactory and comply with the design objectives.

It was found in the model that capacitor C_2 average voltage is equal to zero, and that capacitor C_1 average voltage is equal to the output voltage. The simulation result in Figure 5.8 and the practical result in Figure 5.14 agree with the theoretical capacitor voltage value within 2%. The discrepancy is the result of the capacitor ESR not included in the theoretical computation. Noise in the circuit can be seen on capacitor C_1 voltage waveform. The switch in the quasi-Z-source circuit is to remain on during the entire switching period and result in a constant switch current. Unlike the switch current waveform of the simulation in Figure 5.10 the drop of the switch current in Figure 5.16 of the practical circuit is the result of the physical switching transition that takes place despite the 100% on time duty cycle. Because of the mosfet on resistance, the voltage drop on the switch is not zero during conduction as seen in Figure 5.17.

Table 5.3 compares where applicable the simulation results of Figures 5.2 to 5.11, the practical results of Figures 5.12 to 5.18 and the theoretical value based on the model that was derived. It can be seen that the simulation and practical results are within 2 % of the calculated value and hence confirm the effectiveness of the model that was derived and the controller that was designed.

Table 5.3. QZSR theoretical, simulation and practical results when Vs = 70 V

Parameter	Theory Results	Simulation Results	Practical Results	Parameter	Theory Results	Simulation Results	Practical Results
V_{codc}	150 V	149.98 V	150 V	ΔV_{co}	0 V	0.0045 V	1 V
I_{corms}	0 A	0.00004 A	NA				
V_{c1dc}	150 V	152.71 V	152 V	V_{c2dc}	0 V	2.726 V	1.55 V
ΔV_{c1}	0 V	0.0175 V	2 V	ΔV_{c2}	0 V	0.0049 V	0 V
I_{c1rms}	0.019 A	0.0197 A	NA	I_{c2rms}	0.019 A	0.0197 A	NA
I_{L1dc}	4.54 A	4.54 A	4.5 A	I_{L2dc}	4.54 A	4.54 A	4.5 A
ΔI_{l1}	0 A	0.00024 A	NA	ΔI_{l2}	0 A	0.00024 A	NA
V_{swdc}	0 V	0.4553 V	0.1 V	I_{swrms}	4.54	4.54 A	4.5 A

5.3. SIMULATION AND EXPERIMENTAL RESULTS DURING QUASI-PWM RECTIFIER MODE

The simulations results of the quasi-Z-source three-phase rectifier when the three-phase input voltage is at 100V are shown in Figures 5.19 to 5.28

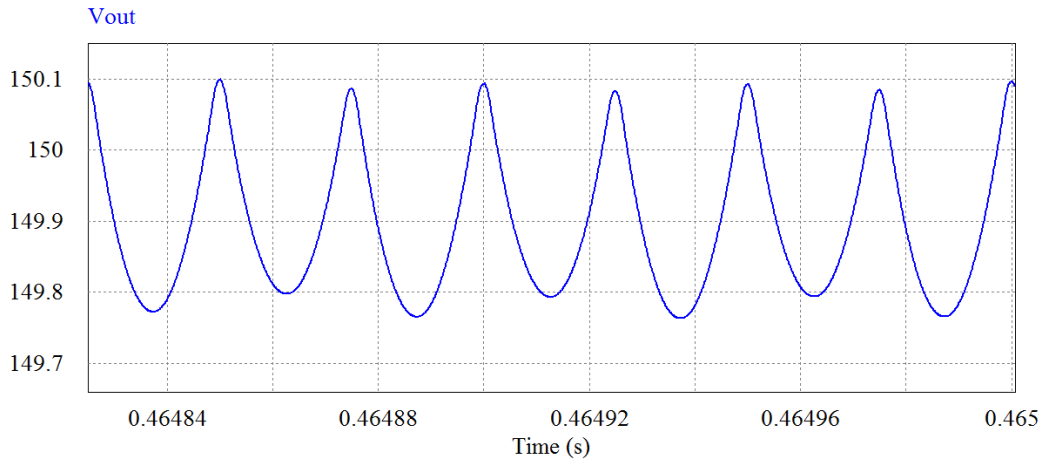

Figure **5.19.** QZSR output DC voltage when V_s = 100 V

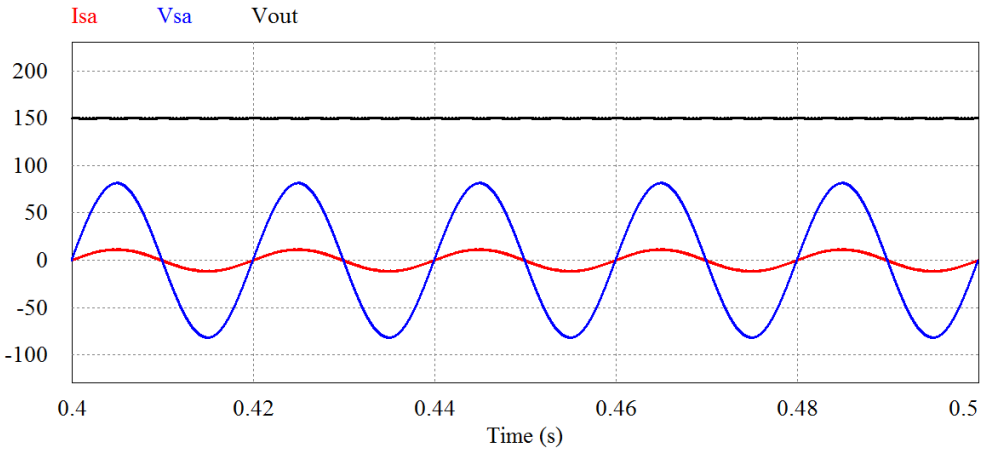

Figure 5.20. QZSR phase A AC input Voltage and Current when V_s = 100 V

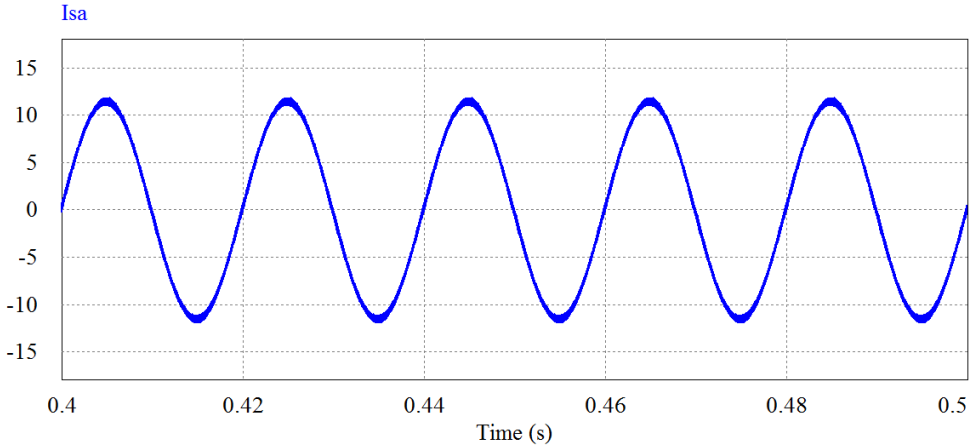

Figure 5.21. QZSR phase A AC input Current when V_s = 100 V

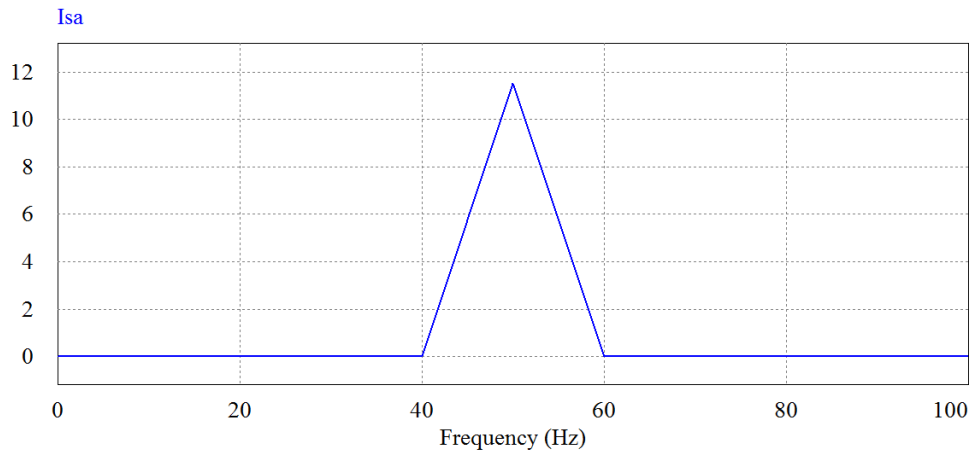

Figure 5.22. QZSR phase A AC input Current spectrum when V_s = 100 V

The AC input current spectrum is shown in Figure 5.22 and the rms value of the AC current at each harmonic frequency in Table 5.4. The current spectrum in Figure 5.22 only presents the amplitude at 50 Hz because the switching frequency ripples are not significant relative to the line frequency. The distortion power factor is obtained as follows:

$$p.f_{distorsion} = \frac{I_{s1}}{I_s} = \frac{8.14}{8.141} = 0.9998$$

From Figure 5.20 the phase current and phase voltage are exactly in phase, which implies a displacement power factor of 1. The total power factor of the rectifier is therefore:

$$p.f_{tot} = p.f_{distorsion} \; x \; p.f_{displacement} \cong 1$$

Table 5.4. Input AC current harmonic Amplitudes

Frequency	Total rms	50 Hz	20 KHz	40 KHz	60 KHz	80 KHz	100 KHz
Is [A]	8.141	8.14	0.0591	0.0738	0.02764	0.0042	0.00796

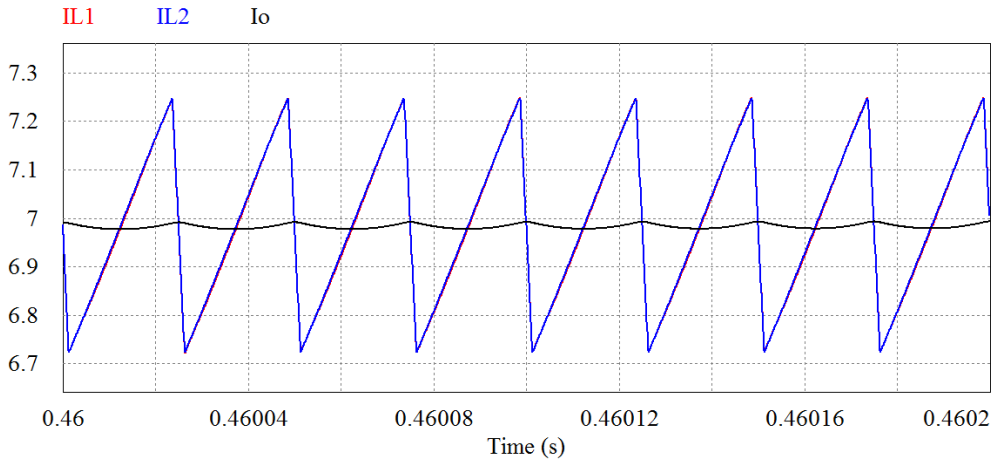

Figure 5.23. QZSR load current I_o and Inductors L_1 and L_2 current when V_s = 100 V

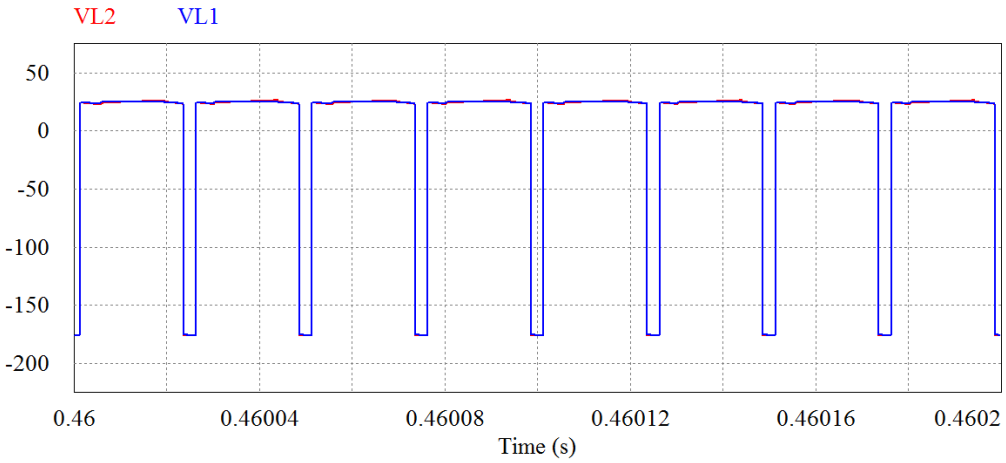

Figure 5.24. QZSR Inductors L_1 and L_2 voltage when V_s = 100 V

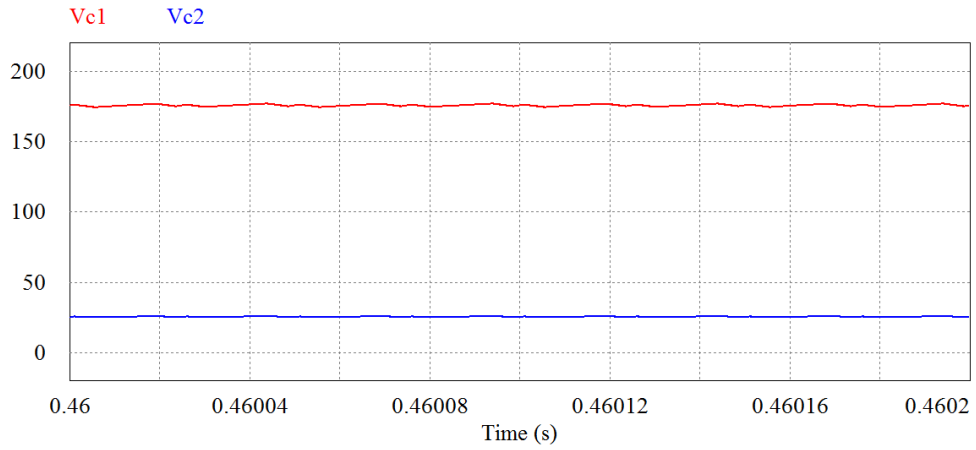

Figure 5.25. QZSR Capacitors C_1, C_2 and Co voltage when V_s = 100 V

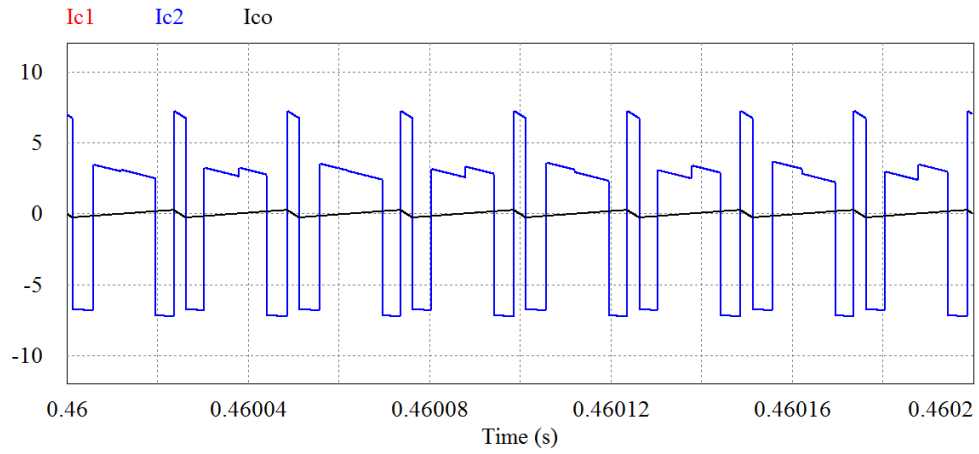

Figure 5.26. QZSR Capacitors C_1, C_2 and C_o current when V_s = 100 V

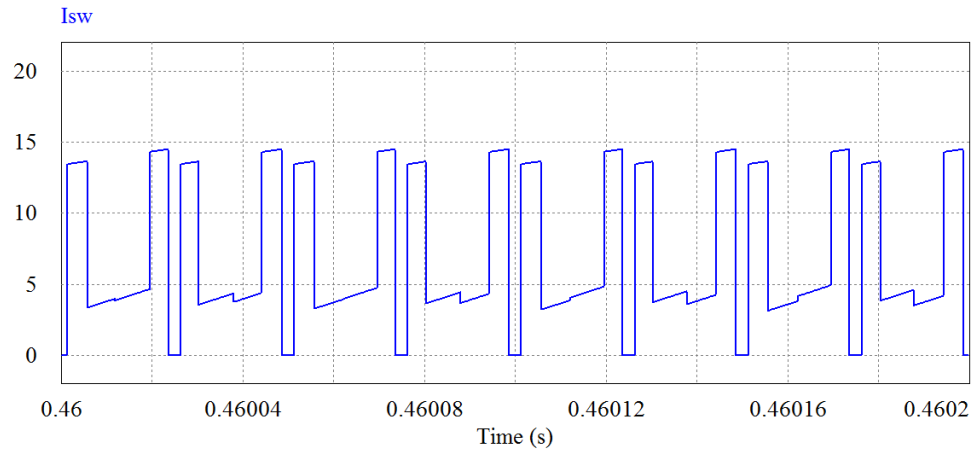

Figure 5.27. QZSR Switch Current when V_s = 100 V

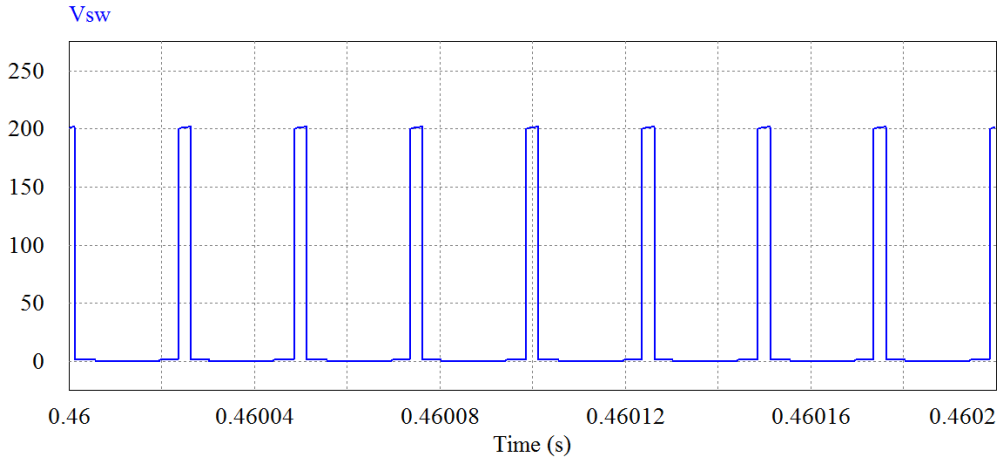

Figure 5.28. QZSR Switch Voltage when V_s = 100 V

Practical results of the QZSR in the shoot-through mode are shown in Figures 5.29 to 5.35. The voltage probe scaling is 1/1000, and oscilloscope scaling is 1x500, such that the effective voltage is half of what is displayed. The current probe setting is 100 mV/A, and the oscilloscope scaling is 1x10, such that the effective current scaling on the oscilloscope display is 1 V = 1 A. The oscilloscope channels are identified as follows: Yellow for Channel 1, Blue for channel 2, Pink for channel 3 and Green for channel 4.Furthermore the three-phase AC voltage supply used in the practical experimentation was not an ideal voltage source. Only a high impedance three-phase variac with slow dynamic was available for the practical experiment. The voltage source quality can be seen on the practical waveforms and this negatively impacted on the performance of the rectifier by injecting

noise despite the improved layout of the circuit. Capacitors had to be inserted at each input AC voltage phase to improve the supply voltage and reduce noise in the system.

Because of the shoot through operation more noise was injected by the supply which caused collapse of the DC voltage, resulting in large current drawn from the AC supply. The noise problem was more prominent when low AC current amplitude was drawn from the supply. As a consequence of these problems the output power during through mode was increased from 700 W supplied in the PWM mode to 1000 W with shoot through on, such that a sufficient higher AC current is drawn from the supply.

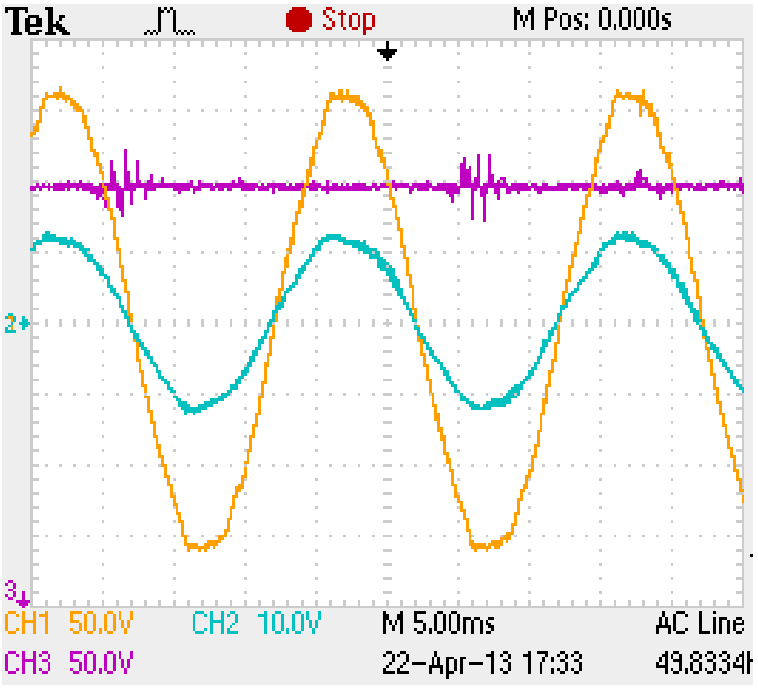

Figure 5.29. QZSR input AC voltage (line-neutral, CH1 at 50V/div), input AC Phase A current (CH2 at 10V/div) and output DC voltage (CH3 at 50V/div) with 5 ms/div

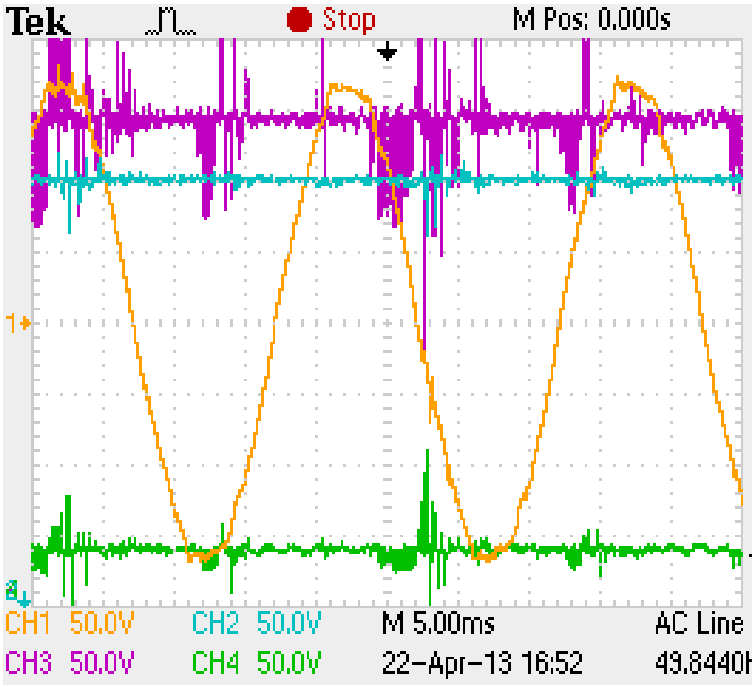

Figure 5.30. QZSR input AC voltage (line-neutral, CH1 at 50V/div), output DC voltage (CH2 at 50V/div) and Capacitor C_1 Voltage (CH3 at 50V/div) and Capacitor C_2 Voltage (CH4 at 50V/div) with 5 ms/div

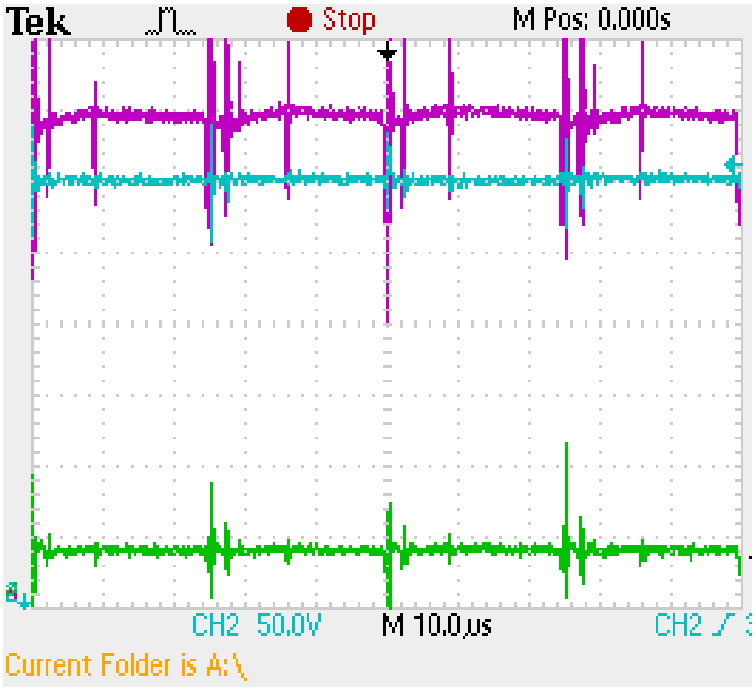

Figure 5.31. Output DC voltage (CH2 at 50V/div), Capacitor C_1 Voltage (CH3 at 50V/div) and Capacitor C_2 Voltage (CH4 at 50V/div) with 10 us/div

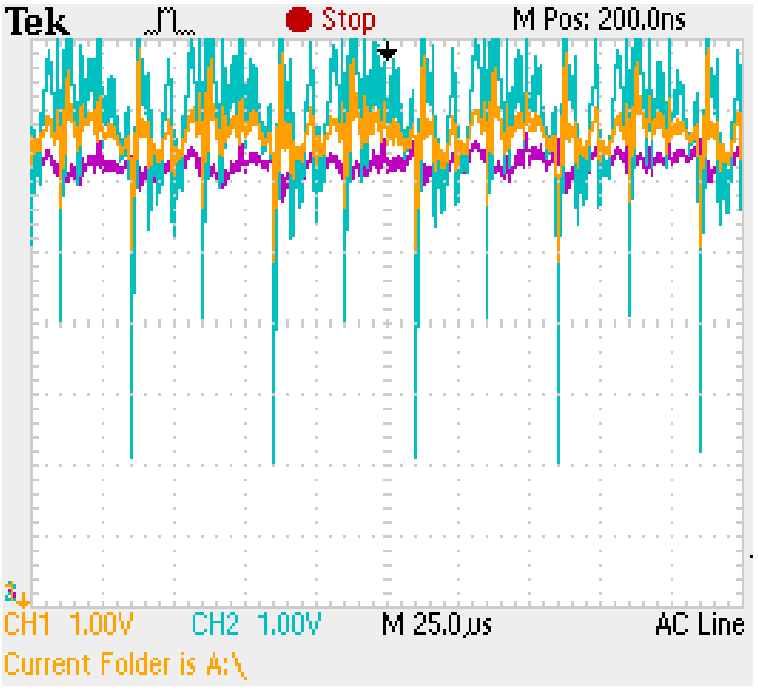

Figure 5.32. QZSR output current (CH1 at 5V/div), Inductor L_1 current (CH2 at 5V/div) and Inductor L_2 current (CH3 at 5V/div) with 25 us/div

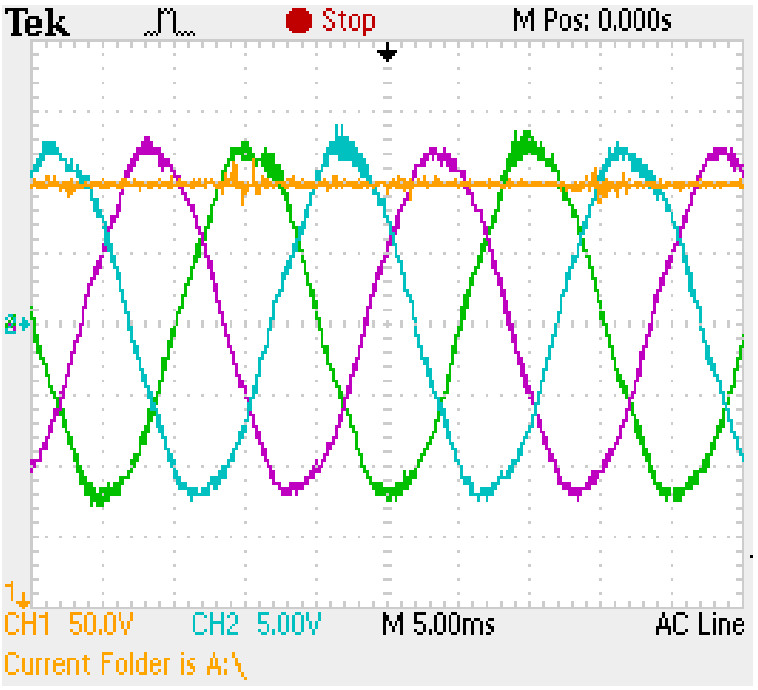

Figure 5.33. QZSR output DC voltage (CH1 at 50V/div), Phase A (CH2 at 5V/div), Phase B (CH3 at 5V/div) and Phase C (CH4 at 5V/div) input AC current with 5 ms/div

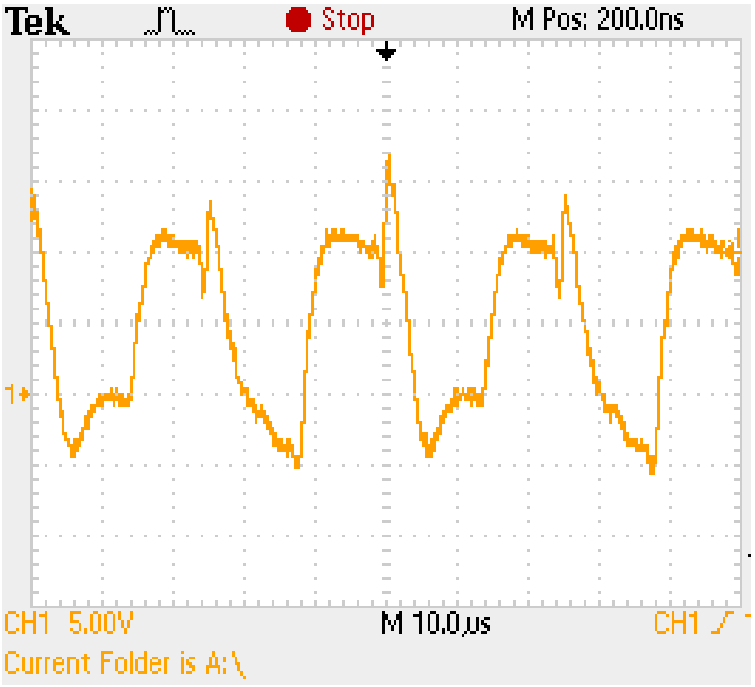

Figure 5.34. QZSR switch current (CH1 at 5V/div) with 10 us/div

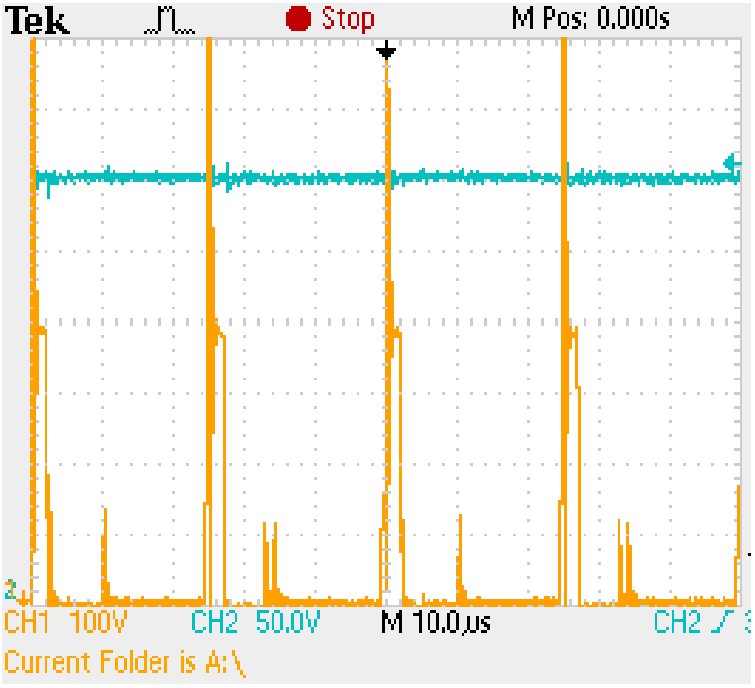

Figure 5.35. QZSR switch voltage (CH1 at 100V/div) and Output DC voltage (CH2 at 50V/div) with 10 us/div

The average value of the output DC voltage of the system in Figure 5.19 is equal to 150 V with a peak-to-peak voltage ripple of 0.33 V, which is equal to 0.2 % of the steady state value. Phase A of the input AC current is in phase with phase A of the input AC voltage as shown in Figure 5.17. The THD of the AC input current is equal to 0.02 % and the harmonic current magnitudes are well below the limit set by the IEC 61000-3-2 standard. Figure 5.23 confirms the findings of the model that the inductors' currents are equal and that the average current of the inductors and the load are also equal. It is also confirmed by Figure 5.26 that capacitors C_1 and C_2 current are equal. From the simulation results shown in Figures 5.19 to 5.28 the quasi-Z-source three-phase rectifier operations in shoot-through mode are satisfactory and comply with the design objectives.

In the practical experimental system the average value of the output DC voltage in Figure 5.29 is equal to 150 V, with a peak-to-peak voltage ripple of 0.9 V, which is less than 1 % of the steady state value. The input AC voltage and current are in phase as shown in the practical waveform of Figure 5.29. This confirms that the QZSR using the controllers designed is capable of unity displacement power factor operation. The input AC current is fairly sinusoidal which implies that current harmonic magnitudes are well below the limit set by the IEC 61000-3-2 standard. The practical waveform of Figure 5.32 also confirms the theoretical finding that the average current of the inductors and the load are equal. As a consequence of the noise in the practical circuit despite the improved layout, no better inductor current could be captured. However the steady state inductor and load current can be compared on the waveform of Figure 5.32 and these are within 4% of the simulation and theoretical results.

The simulation result in Figure 5.25 and the practical result in Figures 5.30 and 5.31 of the quasi-Z-circuit capacitors' voltage agree with the theoretical result within 3%. The discrepancy is the result of the capacitors ESR not included in the theoretical computation. The capacitor practical waveform is affected by noise present in the circuit and causing the voltage spike. The quasi-Z-circuit switch current waveform of Figure 3.34 and voltage waveform of Figure 3.35 are comparable to the simulation waveform. Switch Current reversal is observed in Figure 3.34 during switching transition of the quasi-Z-switch. The

large switch voltage spike in Figure 3.35 and not encountered in the simulation is the result of non ideal characteristics such as leakage inductance present in the practical system. Despite noise affecting some practical waveforms, overall they are comparable to the simulation waveforms within an acceptable error and therefore validates that the QZSR is a cost effective rectifier capable of stepping down the input voltage.

Table 5.5 compares where applicable the simulation results of Figures 5.19 to 5.28, the practical results of Figures 5.29 to 5.35, and the theoretical value based on the model that was derived. It can be seen that both the simulation and practical results are within 4 % of the calculated value. Deviation over 4 % is only seen in capacitor C_1 and C_2 voltage ripple. The percentage deviations are the result of noise in the circuit and component non ideal characteristics not accounted for in the model that was developed for theoretical calculations. Despite the errors that do not significantly degrade overall performance and that can be reduced with better components, the results obtained confirm the effectiveness of the model that was derived and the controller that was designed.

Table 5.5. QZSR theoretical, simulation and practical results when Vs = 100 V

Parameter	Theory Results	Simulation Results	Practical Results	Parameter	Theory Results	Simulation Results	Practical Results
V_{codc}	150 V	150.0 V	150.0 V	ΔV_{co}	0.3 V	0.33 V	0.9 V
I_{corms}	0.154 A	0.155 A	NA				
V_{c1dc}	170.2 V	175.4 V	174.5 V	V_{c2dc}	20.16 V	25.39 V	22.5 V
ΔV_{c1}	1.0 V	5.1 V	5.8 V	ΔV_{c2}	0.30 V	2.898 V	2.6 V
I_{c1rms}	5.45	5.47 A	NA	I_{c2rms}	5.45	5.469 A	NA
I_{L1dc}	6.976 A	6.978 A	6.92 A	I_{L2dc}	6.976 A	6.978 A	6.62 A
ΔI_{l1}	0.5	0.52 A	NA	ΔI_{l2}	0.5	0.52 A	NA
V_{swdc}	190.3 V	201 V	195 V	I_{swrms}	8.66 A	8.674 A	8.22 A

5.4. SIMULATIONS AND PRACTICAL RESULT AT THREE-PHASE AC SUPPLY VARIRATION

To confirm the effectiveness of the rectifier for large variable three-phase AC input voltage, simulation and practical results of the output DC voltage, phase A input AC voltage and current are shown in Figures 5.36 to 5.39 at the input AC voltages within the designed range.

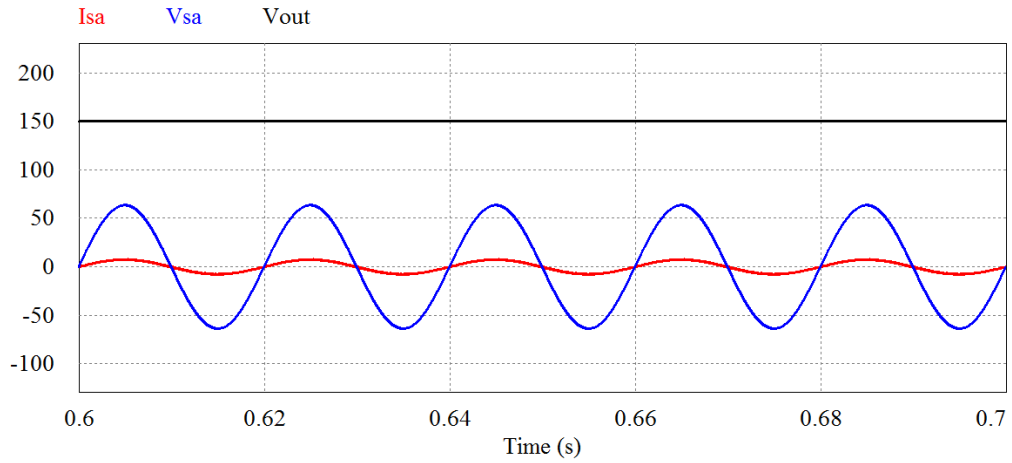

Figure 5.36. Simulation waveforms of Output DC voltage and phase A AC input Voltage and Current at V_s = 78 V

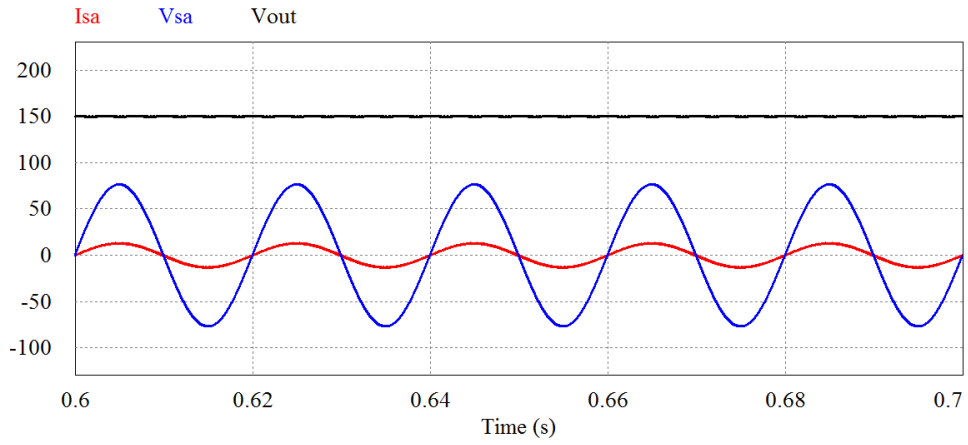

Figure 5.37. Simulation waveforms of Output DC voltage and phase A AC input Voltage and Current at V_s = 94 V

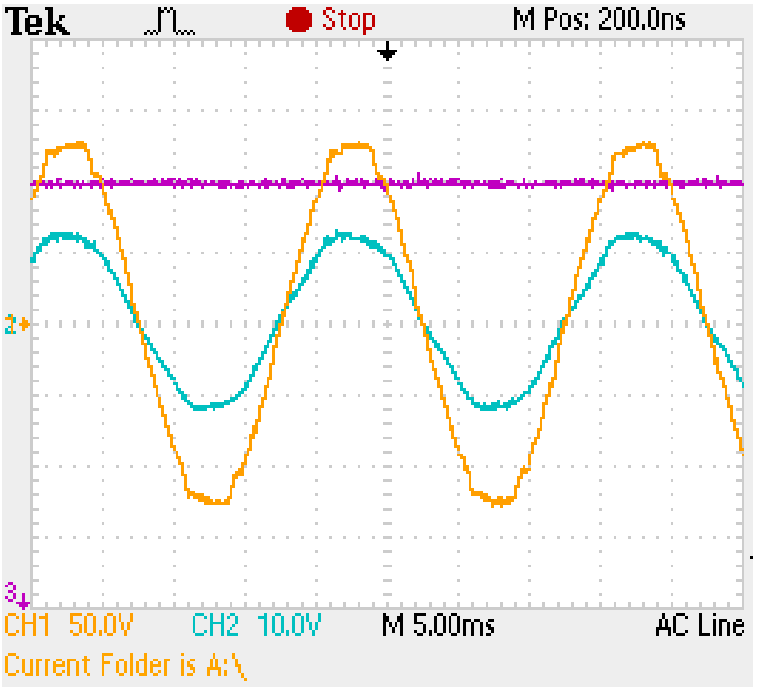

Figure 5.38. QZSR input AC voltage (line-neutral, CH1 at 50V/div), input AC current (CH2 at 10V/div) and output DC voltage (CH3 at 50V/div) with 5 ms/div at V_s = 78 V

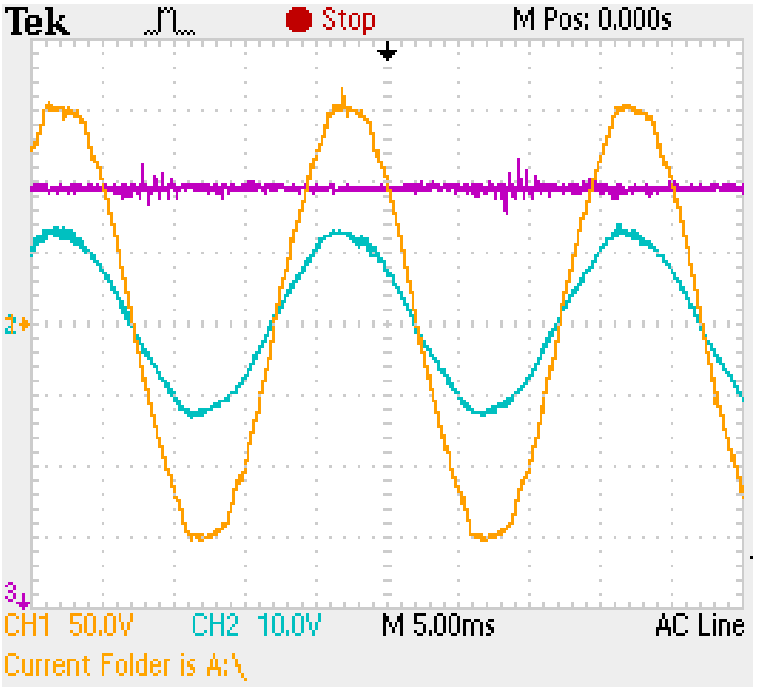

Figure 5.39. QZSR input AC voltage (line-neutral, CH1 at 50V/div), input AC current (CH2 at 10V/div) and output DC voltage (CH3 at 50V/div) with 5 ms/div at V_s = 94 V

The simulations and practical results shown in Figures 5.36 to 5.39 show that the quasi-Z-source three-phase rectifier will regulate the output at the desired value of 150 V while supplied with a variable three-phase input voltage of 70 V to 100 V. While regulating the DC output during the input AC voltage variation, the quasi-Z-source three-phase rectifier draws from the supply an AC current with THD lower than 1 % and in phase with the phase input Voltage.

Table 5.6 summarises the variation of phase A rms input current, the total input power and the efficiency as the three-phase input voltage varies from 70 V to 100 V while the output power is fixed to 700 W. It can be concluded from Table 5.5 that as the AC input voltage increases, the efficiency of the rectifier increases. The trend is justified by the higher copper losses occurring at lower AC input voltage resulting in large AC input current. The efficiency can be significantly improved by using a low impedance voltage source to reduce the losses at the input resistors.

Table 5.6. Variations of AC supply current, input Power and efficiency

3 Phase Input voltage [V]	Isrms [A]	Pin[KW]	Efficiency[%]
70	8.767	1062	65.91
78	6.83	922.7	75.86
88	5.57	848.9	82.46
94	5.09	828.7	84.47
100	4.68	810.6	86.35

5.5. DYNAMIC PERFORMANCE RESULTS

The dynamic performance of QZSR is tested with a 30 % step change increase in load using a resistor**.** Figures 5.40 and 5.41 show the response of the system to load changes when the three-phase input voltage is 100 V and 70 V respectively. The advantage of the fast current loop designed can be seen from the current waveform where an almost instantaneous and smooth current change occurs as the load varies in both mode of operation. During shoot-through mode in Figure 5.40, the current settling time is close to 0 ms and the 95% voltage settling time is 0.7 ms; the voltage undershoot is 11 %. The settling times achieved during shoot-through mode are by a factor of 10 shorter relative to the designed value shown in the

closed-loop step changes responses of Figures 4.7 and 4.20. The voltage overshoot achieved is by 4% smaller compared to the design result shown by the step change response of Figure 4.20.

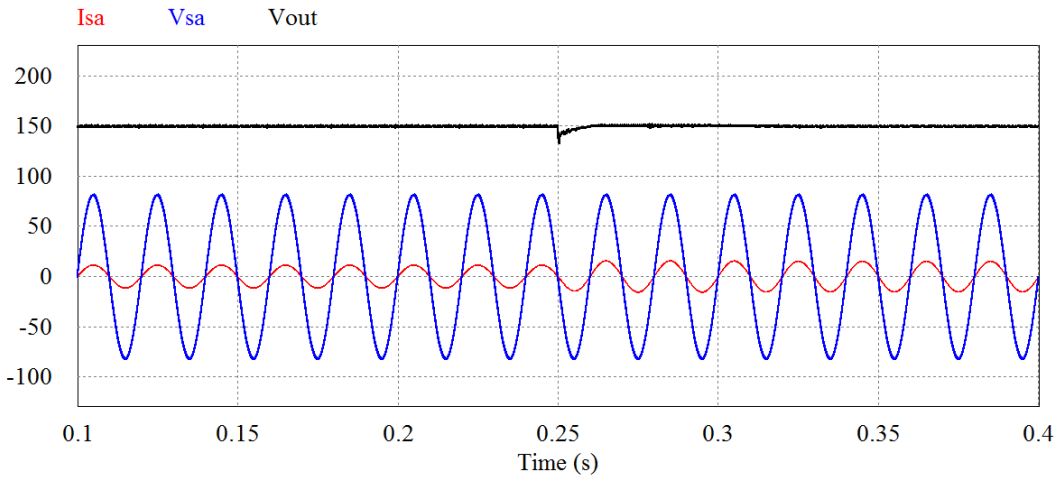

Figure 5.40. QZSR output DC voltage and phase A AC input Voltage and Current during 30 % step change in load when Vs = 100 V

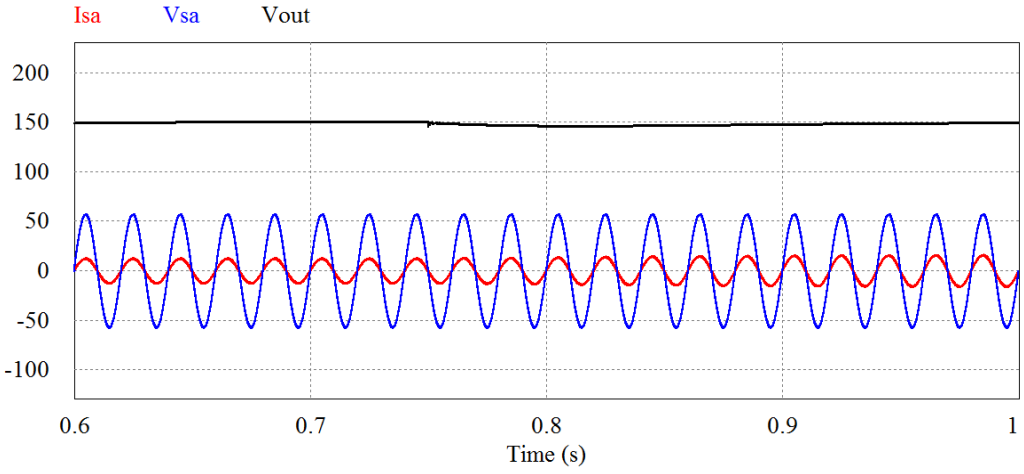

Figure 5.41. QZSR output DC voltage and phase A AC input Voltage and Current during 25 % step change in load when Vs = 70 V

During PWM mode in Figure 5.41 the current settling time is about 3 line frequency cycle and 95% voltage of the steady state voltage is not reached during the voltage drop. However the 98% voltage settling time is 100 ms and no overshoot is observed on the output voltage.

The dynamic performances during PWM mode are comparable to the design result in terms of voltage overshoot and settling time. But it is clear from the simulation results that the dynamic performances of the QZSR are better during shoot-through mode. This is mainly the result of one of the major concepts that was contributed by this research with the double stage control loop producing a faster response as the additional quasi-Z-source circuit also tracks the voltage. At 70 V input voltage, when the shoot-through is not used, the slower response is due to the fact that the quasi-Z-source circuit does not operate in switch mode, and depends on the natural response of the passive element in the quasi-Z-source circuit. Furthermore, the overdamped voltage response during PWM mode is the result of the large phase margin designed, while the voltage overshoot in shoot-through mode is justified by the lower phase margin. Overall, the dynamic performances during both mode of operation are satisfactory and comparable to conventional three-phase PWM rectifier [62] [63] [64].

5.6. CHAPTER CONCLUSION

This chapter has validated through simulations and practical experimentations that the QZSR is capable of stepping up or stepping down the voltage while drawing a unity total power factor current from the supply. The results obtained are within an acceptable error comparable to the theoretical expectations. As such it is validated that the inductors and load current are equal in the QZSR. It is also validated that the QZSR capacitors voltages are not equal and therefore the capacitors do not have to be symmetrical. Control concept such as double stage for QZSR that was introduced in this research has been satisfactorily implemented and has resulted in fast dynamic responses.

CHAPTER 6 CONCLUSIONS

Active rectifiers are increasingly used as interface for AC to DC conversion for their high efficiency and power factor. In wind generator applications they lower the reactive power demand and thus most of the output from the generator is available as active power. Conventional voltage and current source three-phase rectifiers have largely been used as topology for active rectifiers. However, the limitations of VSR and CSR in applications requiring buck-boost capability of the rectifier have led to the development of a more efficient rectifier topology the Z-source. Until recently, the Z-source three-phase rectifier has been the more efficient AC to DC conversion to use due to its buck-boost capability. But the quasi-Z-source circuit has been introduced as a better topology than the ZSR in rectifier applications. In this dissertation, the quasi-Z-source three-phase rectifier has been illustrated in detail showing its superior performance than the Z-source three-phase rectifier. Among some of this research's unique contributions, the dynamic models of the ZSR and QZSR are obtained using a simpler method, the control block diagram of both rectifier is given, a detailed comparison of the both rectifiers proving the higher efficiency of the QZSR is provided, a closed-loop controller of the QZSR is designed, and simulations as well as practical experiments results are given to validate the performance of the QZSR.

In chapter one, the introduction analytically states the background of this research, the theoretical advantage of the QZSR over the ZSR by looking at the topology and conducting a review of the current literature on the analysis, modelling and control of the QZSR and the ZSR. In chapter two, the ZSR modelling is revisited using circuit averaging in this research to obtain the model with ease. Furthermore, it is shown in chapter two of this dissertation the mathematical basis for using symmetrical components in the ZSR. In chapter three, the major contribution of this dissertation is presented with the analysis of the QZSR through the dynamic model that was developed. The model is validated by bode plots of the transfer function of all passive elements of the quasi-Z-source circuit and the DC voltage and current expressions are also given. Chapter three is concluded with a detailed comparison of the QZSR and ZSR in terms of DC values of component and dynamic responses. The

comparison confirms that the QZSR is a more efficient rectifier than the ZSR because of lower rated capacitors. In chapter four, a closed-loop controller is designed to control the QZSR using the block diagram that was derived in this research. The controller designed in this research uses a unique two stages control diagram to separate the AC side and DC side control. Stage one for the input AC current control uses a double loop control with a fast inner current loop and a slower outer voltage loop linked with the DC output voltage of the QZSR. Stage two regulates the DC output voltage of the quasi-Z-source network. In chapter five, software simulations and hardware experimentation of the QZSR with the designed controller is performed. The simulation and experiment show that the QZSR operates as expected from the analytical conclusions. The simulations and practical experiment confirm that the QZSR maintain a good line and load regulation and therefore make it a very efficient AC to DC conversion interface for applications with wide voltage and load variations.

The QZSR modelling contributions of this research in chapter 3 have presented at the 2012 IEEE APEC conference with the paper title: Three-phase Quasi-Z-source Rectifier modelling. The paper presents the steady state performance of the QZSR where it is shown that the QZSR has lower rated non symmetrical capacitor compared to the ZSR. The small-signal modelling in the paper presents the transfer functions and the block-diagram necessary for closed-loop control of the QZSR. The analysis of the quasi-Z-source circuit transfer function in the paper points out the non-minimum zero limitations and possible mitigations method to improve the dynamic performance of the rectifier in closed-loop control.

The research on the quasi-Z-source three-phase rectifier can be further investigated by considering the following alternatives:

1. The model derived uses ideal passive components and switches. A more accurate model can be obtained by including components non ideal characteristics and comparing the obtained model with the one obtained in this dissertation. This will

help to appreciate if components non ideal characteristics have significant impact on the analysis using ideal components.

2. The model and the modulation method of this research is simple boost. The limitations of simple boost method have been presented in the literature review. The QZSR can be modelled and controlled using other modulations method such as maximum constant boost to leverage its advantages.

3. For control of the QZSR, a model predictive control (MPC) of a grid connected QZSR can be considered where the grid current is perfectly controlled during transient and steady state operation by including inductor current, capacitor voltage as well as switching frequency as additional control constraints. Both steady state and transient results will be of great interest as it can show high performance response of the new control technique.

This research has shown the attractive features of the QZSR for variable input voltage systems. Such variable input voltage systems are encountered in renewable energy systems such as wind power. A further investigation will be to connect a wind generator at the input of the QZSR and verify its performance. This might require modelling the QZSR, taking into account the wind generator dynamic and designing appropriate controller with maximum wind power tracking.

REFERENCES

[1] A. Sangswang, "Uncertainty modeling of power electronic converter dynamics," Drexel University, Philadelphia, PhD Thesis, June 2003.

[2] N. Mohan, T. M. Undeland and W. P. Robins, Power Electronics: converter, applications and design, New York: Wiley, 2003.

[3] X. Ding and Z.Quian, "Three phase Z-source rectifier," in *Proc. IEEE Power Electronic Specialists Conf.*, 2005, pp. 494-500.

[4] S. H. Hosseini, F. Sedaghati and M. Sarhangzadeh, "Improved power quality three phase AC-DC converter," in *Proc. IEEE Int. Conf. on Electrical Machines and Systems.*, Oct. 2010, pp. 148-153.

[5] Y. Xie, Z.Quian, X. Ding and F. Z. Peng, "A novel Buck-Boost Z-source Rectifier," in *Proc. IEEE Power Electronic Specialists Conf.*, June 2006, pp. 1-5.

[6] D. M. Vilathgamuwa, P. C. Loh and K. Karunakar, "Modelling of three phase Z-source boost-buck rectifiers," in *Proc. Int. Conf. on Power Electronics and Drive Systems*, 2007, pp.1471-1476.

[7] G. Lo Calzo, A. Lidozzi, L. Solero and F. Crescimbini, "Three-Phase Z-Source Power Supply Design and Dynamic Modeling," in *Proc. IEEE Energy Conversion Congress and Exposition* , Sept. 2011, pp.1339-1345.

[8] F. Z. Peng, "Z-Source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, No.2, pp. 504-510, March/April 2003.

[9] Q. Lei, S. Yang, F. Z. Peng and R. Inoshita, "Three-phase current-fed Z-source PWM Rectifier," in *Proc. IEEE Energy Conversion Congress and Exposition*, Sept. 2009, pp. 1569-1574.

[10] J. Anderson and F.Z. Peng, "Four quasi-Z-source Inverters," in *Proc. IEEE Power Electronic Specialists Conf.*, 2008, pp. 2743-2749.

[11] M.N. Gitau, "Modelling and control of Active rectifier," EED 780 class notes, Department of Electrical, Electronic and Computer Engineering, University of Pretoria, 2009.

[12] R.D. Middlebrook and S. Cuk, "A General Unified Approach to Modeling Switching-Converter Power Stages," in *Proc. IEEE Power Electronic Specialists Conf.*, 1976, pp. 18-34.

[13] R. W. Ericsson and D. Maksimović, *Fundamentals of Power electronics*, 2nd Ed, Kluwer academic Publishers, 2001.

[14] K. Karunakar and D. M.Vilathgamuwa, "Dynamic analysis of three-phase Z- source boost-buck rectifier," in *Proc. IEEE Int. Power and Energy Conf.* , 2008, pp.198-202.

[15] Q. Lei, S. Yang, F. Z. Peng and R. Inoshita, "Steady state and transient analysis of a three-phase current fed Z-source PWM Rectifier ," in *Proc. IEEE Vehicle Power and Propulsion Conf.*, Sept. 2009, pp. 426-432.

[16] X. Ding, Z. Qian, Y. Xie and F. Z. Peng, "A novel ZVS Z-source rectifier," in *Proc. IEEE Applied Power Electronics Conf. and Exp.*, 2006, pp. 951-955.

[17] X. Ding, Z. Qian, Y. Xie and F. Z. Peng, "Transient modeling and control of the novel ZVS Z-source rectifier," in *Proc. IEEE Power Electronic Specialists Conf.*, 2006, pp. 1-5.

[18] C.J. Gajanayake, D.M Vilathgamuwa and P.C. Loh, "Development of a Comprehensive Model and a Multiloop Controller for Z-Source Inverter DG Systems," in *Proc. IEEE Power Electronic Specialists Conf.*, 1976, pp. 18-34.

[19] G. Sen, "Voltage and current programmed modes in control of the Z-source converter," M.S thesis, Graduate Faculty, Akron Univ., Akron, Ohio, 2008.

[20] X. Ding, Z. Qian, S. Yang, B. Cui, F. Z. Peng, "A PID Control Strategy for DC-link Boost Voltage in Z-source Inverter," in *Proc. IEEE Applied Power Electronics Conf.*, 2007, pp. 1145-1148.

[21] X. Ding , Z. Qian, S. Yang, Bin Cui, F. Z. Peng, "A Direct Peak DC-link Boost Control Strategy for Z-Source Inverter", in *Proc. IEEE Applied Power Electronics Conf.*, 2007, pp. 648-653.

[22] X. Ding, Z. Qian, S. Yang, B. Cui and F.Z Peng, "A direct DC-link boost voltage PID-like fuzzy control strategy in Z-source inverter," in *Proc. IEEE Power Electronic Specialists Conf.*, 2008, pp. 405-411.

[23] M. J. Rastegar Fatemi, S. Mirzakuchaki and S. M. J. Rastegar Fatemi, "Wide-Range Control of Output Voltage in Z-source Inverter by Neural Network," in *Proc. IEEE Int. Conf. on Electrical Machines and Systems.*, 2008, pp. 1653-1658.

[24] S.Yang, X. Ding, F. Zhang, F. Z. Peng and Z. Qian, "Unified Control Technique for Z-Source Inverter," in *Proc. IEEE Power Electronic Specialists Conf.*, 2008, pp. 3236-3242.

[25] Li. Yuan, J. Anderson, F. Z. Peng and D. Liu, "Quasi-Z-Source Inverter for Photovoltaic Power Generation Systems," in *Proc. IEEE Applied Power Electronics Conf.*, 2009, pp. 918-924.

[26] J. H Park, H. G Kim, E.C Nho, T. W Chun and J. Choi, "Grid-connected PV System Using a Quasi-Z-source Inverter," 'in *Proc. IEEE Applied Power Electronics Conf.*, 2009, pp. 925-929

[27] L. Yushan, G. Baoming, F. Z. Peng, A. R. Haitham, A. T. de Almeida and F. J. T. E. Ferreira, "Quasi-Z-Source Inverter based PMSG Wind Power Generation System," in *Proc. IEEE Energy Conversion Congress and Exposition*, Sept. 2011, pp. 291-297.

[28] L. Bisenieks, D. Vinnikov and I. Galkin, "New Isolated Interface Converter for Grid-Connected PMSG based Wind Turbines," 'in *Proc. IEEE Int. Conf. on Environement and Electrical Engineering*, 2011, pp. 1-4

[29] L. Bisenieks, D. Vinnikov and J. Zakis, "Analysis of Operating Modes of the Novel Isolated Interface Converter for PMSG Based Wind Turbines," 'in *Proc. IEEE Int. Conf. on Power Engineering, Energy and Electrical Drives*, May 2011, pp. 1-8.

[30] S. Yang, F. Z. Peng, Q. Lei, R. Inoshita and Z. Qian, "Current-fed Quasi-Z-Source Inverter with Voltage Buck-Boost and Regeneration Capability," 'in Proc *Proc. IEEE Energy Conversion Congress and Exposition*, 2009, pp. 3675-3682.

[31] Q. Lei, S. Yang, F. Z. Peng and R. Inoshita, "Application of Current-fed Quasi-Z-Source Inverter for Traction Drive of Hybrid Electric Vehicles," 'in *Proc. IEEE Vehicule Power and Propulsion Conf.*, 2009, pp. 754-760

[32] A. Liske, G Clos and M. Braun, "Analysis and modeling of the Quasi-Z-Source-Inverter," in *Proc. IEEE Annual Industrial Electronics Conf.*, 2011, pp. 1197-1202

[33] C. J. Gajanayake, H. B. Gooi, F. L. Luo, P. L. So, L. K. Siow and Q. N. Vo, "Simple modulation and control method for new extended boost quasi Z-source," in *Proc. IEEE Region 10 Conf.*, 2009, pp. 1-9

[34] Y. Li, F.Z. Peng, J.G. Cintron-Rivera and S. Jiang, "Controller Design for Quasi-Z-Source Inverter in Photovoltaic Systems," in *Proc. IEEE Power Electronic Specialists Conf.*, 2010, pp. 494-500.

[35] F. Z. Peng, M. Shen and Z. Qian, "Maximum boost control of the Z-source inverter," *IEEE Trans. Power Electron*., vol. 20, no. 4, pp. 833-838, Jul. 2005

[36] M. S. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert and D. J. Adams, "Constant Boost control of the Z-source inverter to minimise current ripple and voltage stress," *IEEE trans. Ind. Appl*., vol 42, no 3, pp. 770-778, May/June 2006.

[37] T. W. Chun, Q. V. Tran, J. R. Ahn, and J. S. Lai, " AC Output Voltage Control with Minimization of Voltage Stress Across Devices in the Z-Source Inverter Using Modified SVPWM," in *Proc. IEEE Power Electronic Specialists Conf*., 2006, pp. 3030-3034

[38] O. Ellabban, J. Van Mierlo and P. Lataire, "Comparison between Different PWM Control Methods for Different Z-Source Inverter Topologies," in *Proc. IEEE European Conf. on Power Electronics and Applications*, 2009, pp. 1–11.

[39] G. Sen and M. E. Elbuluk, "Voltage and Current Programmed Control Modes in control of the Z-source converter," *IEEE trans. Ind. Appl*., vol 46, no 2, pp. 680-686, May/April 2010.

[40] T. Suntio, *Dynamic Profile of Switched-Mode Converter: Modeling, Analysis and Control*, 1st Ed, Weinheim: Wiley-VCH, 2009.

[41] D. E. Seborg, T.F. Edgar and D. A. Mellichamp, *Process dynamics and control,* 2nd Ed, New York: John Wiley & Sons, 2004.

[42] S. Skogestad and I. Postlethwaite*, Multivariable Feedback Control*. New York: Wiley, 1996.

[43] J. Liu, J. Hu and L. Xu, "Dynamic modeling and analysis of Z-source converter derivation of AC small-signal model and design-oriented analysis," *IEEE Trans. Power Electron.*, vol. 22, no.5, pp. 1786-796, Sept. 2007.

[44] B. Yin, R. Oruganti, S. K. Panda and A. K. S. Bhat, "A Simple Single-Input–Single-Output (SISO) Model for a Three-Phase PWM Rectifier," *IEEE Trans. Power Electron.* vol. 4, no.3, pp. 620-631. March. 2009.

[45] M. K. Kazimierczuk and R. Cravens II, "Open-loop dc and small-signal characteristics of PWM buck-boost converter for CCM", in *Proc. IEEE National Aerospace and Electronics Conf.*, 1994, pp. 226-233.

[46] D. Xinping, Q. Liu, Q. Zhaoming, Y. Shuitao, C. Bin and F. Z. Peng, "A Direct Peak DC-link Boost Voltage Control Strategy in Z-Source Inverter," in *Proc. IEEE Applied*

Power Electronics Conf., 2007, pp. 648-653.

[47] J. Li, J. Liu and Z. Liu, "Comparison of Z-source inverter and traditional two-stage boost-buck inverter in grid-tied renewable energy generation," in *Proc. IEEE Int. Power Electronics and Motion Control Conf.*, 2009, pp. 1493-1497.

[48] D. R. Yang (2006). Dynamic Behaviours of Representative processes. Department of Chemical and Biological Engineering, Korea University. Seoul. [Online]. Available: http://ocw.korea.edu/ocw/college-of-engineering/process-control/lecture-notes-1/l6-dynresp.pdf.

[49] B. Yin, R. Oruganti, S. K. Panda and A. K. S. Bhat, "A Simple Single-Input–Single-Output (SISO) Model for a Three-Phase PWM Rectifier," *IEEE Trans. Power Electron.* vol. 4, no.3, pp. 620-631. March. 2009.

[50] Massachusetts Institute of Technology, "Understanding Poles and Zeros," Analysis and Design of Feedback Control Systems, Department of Mechanical Engineering.

[51] D. Xinping, Q. Liu, Q. Zhaoming, Y. Shuitao, C. Bin and F. Z. Peng, "A Direct Peak DC-link Boost Voltage Control Strategy in Z-Source Inverter," in *Proc. IEEE Applied Power Electronics Conf.*, 2007, pp. 648-653.

[52] S. Kim and P. Enjeti. Digital control of switching power supply-power factor correction stage. Deptartment of Electrical Engineering, Texas A&M University. College Station, Texas. [Online]. Available: http://enjeti.tamu.edu/Dsp-smps.PDF

[53] Y. Duan, "Digital Control Loop design for Power Converter Systems," The Shanghai Jiao Tong University, Shanghai, Master Dissertation, 1993.

[54] M. Hagen and V. Yousefzadeh, "Applying Digital Technology to PWM Control-Loop Designs", Texas Instruments, Dallas, Texas, 2008-2009 Power Supply Design Seminar, pp. 7.1 – 7.28.

[55] S. Choudhury, "Average Current Mode Controlled Power Factor Correction Converter using TMS320LF2407A," Texas Instruments, Dallas, Texas, Application Report SPRA902A, July 2005.

[56] S. Choudhury, "Designing a TMS320F280x Based Digitally Controlled DC-DC Switching Power Supply," Texas Instruments, Dallas, Texas, Application Report SPRAAB3, July 2005.

[57] Y. Duan and H. Jin, "Digital Controller design for Switch-mode Power Converters," in *Proc. IEEE Applied Power Electronic Conf.*, 1999, pp. 967-973.

[58] K. Ogata, *Discrete-Time Control Systems*, 2nd Ed., Prentice Hall, Englewood Cliffs, NJ. 1994.

[59] M. Malinowski, M.P. Kazmierkowski and A. Trzynadlowski, "Review and comparative study of control techniques for three-phase PWM rectifiers," *Math. Comput. Simul.*, vol. 63, pp.349 2003.

[60] Department of Electrical, Computer and Energy Engineering. Introduction to Converter Sampled-Data Modeling. University of Colorado. Boulder, Colorado. [Online]. Available: http://ecee.colorado.edu/~ecen5807/lectures/L20_5807_notes.pdf

[61] M. N Gitau, I.R Smith and J.G Kettleborough, "Mathematical modelling of analogue controlled voltage source converter for Improved Dynamic Response," Journal of Circuits, Systems, and Computers, Vol. 8, No. 4 (1998) pp. 483-496.

[62] V. Blasko and V. Kaura, "A New Mathematical Model and Control of a Three-Phase AC–DC Voltage Source Converter," *IEEE trans. On Power Electronics*, Vol. 12, No. 1, January 1997, pp. 116-123.

[63] C. C. Houand and P. T. Cheng, "Experimental verification of the active front-end converters dynamic model and control designs," in *Proc. IEEE Applied Power Electronics Conf.*, 2009, pp. 370-375.

[64] W. Ke-xin and W. Shui-ming, "Modeling and Simulation of Three-Phase Voltage Source PWM Rectifier," in *Proc. IEEE Advanced Computer Theory and Engineering Conf.*, 2008, pp. 982-986.

[65] N. R Zargari and G. Joos, " Perfomance investigation of a current controlled voltage regulated PWM rectifier in rotating and stationary frames," in *Proc. IEEE Power Electronic Specialists Conf.*, 1993, pp. 1193-1198.

[66] J. Jung, S. Lim and K. Nam, "A Dynamic decoupling control scheme for high-speed operation of induction motors," *IEEE trans. On Ind. Electronics*, Vol. 46, No. 1, Feb. 1999, pp. 100-110.

[67] R. D. Lorentz and D.B. Lawson, "Performance of feedforward Current regulators for field oriented induction machine controllers," *IEEE trans. on Industry Applications*, Vol. IA-23, No. 4, July/August 1997, pp. 597-602.

[68] J. S. Siva Prasad, T. Bhavsar, R. Ghosh and G. Narayanan, "Vector control of three-phase AC/DC front-end converter," in SADHANA Academy proceedings in

Engineering Sciences, Special issue on Power Electronics, Springer, Vol.33, No.5, Oct 2008.

[69] R.C. Dorf and R.H. Bishop , *Modern Control Systems,* 11th Ed., Prentice Hall, 2008.

APPENDIX A THREE-PHASE QUASI-Z-SOURCE RECTIFIER CONTROL DSP CODE

```
/** ###################################################################
**     Filename  : QZSR_Control.C
**     Project   : QZSR_Control
**     Processor : 56F807
**     Version   : Driver 01.12
**     Compiler  : Metrowerks DSP C Compiler
**     Date/Time : 2011/11/21, 04:26 PM
**     Abstract  :
**         Main module.
**         Here is to be placed user's code.
**     Settings  :
**     Contents  :
**         No public methods
**     (c) Copyright UNIS, spol. s r.o. 1997-2006
**     UNIS, spol. s r.o.
**     Jundrovska 33
**     624 00 Brno
**     Czech Republic
**     http      : www.processorexpert.com
**     mail      : info@processorexpert.com
** ###################################################################*/
/* MODULE QZSR_Control */
/* Including used modules for compiling procedure */
#include "Cpu.h"
#include "Events.h"
#include "AD1.h"
#include "PWMC1.h"
```

```
#include "TMR1.h"
#include "MC1.h"
#include "TFR1.h"
#include "MFR1.h"
#include "MEM1.h"
#include "PWMC2.h"
#include "MC2.h"
/* Include shared modules, which are used for whole project */
#include "PE_Types.h"
#include "PE_Error.h"
#include "PE_Const.h"
#include "IO_Map.h"
extern unsigned int values[7]=
{
        0,0,0,0,0,0,0
};
extern int init = 1;
extern int sync = 0;
extern int block = 1;
extern int count = 0;
extern Frac16 check_1 = 0;
extern Frac16 check_2 = 0;
extern Frac16 check_3 = 0;
tfr16_tSinPIxLUT pSWG;
mcgen_s3PhWaveData pHandle;
extern Frac16 PhaseIncrement=164;
extern Frac16 Amplitude=32767;
void main(void)
{
 /* Write your local variable definition here */
 /*** Processor Expert internal initialization. DON'T REMOVE THIS CODE!!! ***/
 PE_low_level_init();
```

```
  /*** End of Processor Expert internal initialization.                    ***/
  /* Write your code here */
  MC1_mcgen3PhWaveInit(&pSWG,&mcgenSineTable[0], 256, &pHandle);
  AD1_EnableIntTrigger();
  for(;;) {}
}
/* END QZSR_Control */

#pragma interrupt called /* Comment this line if the appropriate 'Interrupt preserve registers'
        property */
/*
**     Event       :  AD1_OnEnd (module Events)
**     From bean   :  AD1 [ADC]
**     Description :
**         This event is called after the measurement (which
**         consists of <1 or more conversions>) is/are finished.
**         The event is available only when the <Interrupt
**         service/event> property is enabled.
**     Parameters  : None
**     Returns     : Nothing
*/
#pragma interrupt called /* Comment this line if the appropriate 'Interrupt preserve registers'
        property */
                    /* is set to 'yes' (#pragma interrupt saveall is generated before the ISR)      */
void AD1_OnEnd(void)
{
  mc_s3PhaseSystem V_abc;
  mc_s3PhaseSystem I_abc;
  mc_s3PhaseSystem I_abc_out=
        {
          1,1,1
        };
```

```
Frac16 Vout;
mc_sPhase V_AlphaBeta;
mc_sPhase I_AlphaBeta;
mc_sPhase I_AlphaBeta_out;
mc_sDQsystem Idq;
mc_sDQsystem Idq_out;
static Frac16 Vref = 16477;
static Frac16 Vref_pn = 20945;
static Frac16 Iqref=0;
static Frac16 Idref=0;
static Frac16 shoot = 0;
static Frac16 Vpn = 0;
mc_sAngle pSinCos;
mc_sDQsystem Vdq;
mc_sPIparams control;
mc_sPIparams control_v;
mc_sPIparams control_vshoot;

        values[0]=*((unsigned int *) ADC_RESULT_REG0);
        values[3]=*((unsigned int *) ADC_RESULT_REG3);
        values[4]=*((unsigned int *) ADC_RESULT_REG4);
        values[5]=*((unsigned int *) ADC_RESULT_REG5);
        values[6]=*((unsigned int *) ADC_RESULT_REG6);

          V_abc.PhaseA= values[0];
          Vout = values[3];
          I_abc.PhaseA= values[4];
          I_abc.PhaseB= values[5];
          I_abc.PhaseC= values[6];

          MC2_cptrfmClarke(&I_AlphaBeta, &I_abc);
          pSinCos.sine = sintable[sinecount];
```

```
pSinCos.cosine = costable[sinecount];
MC2_cptrfmPark(&Idq, &I_AlphaBeta, &pSinCos);

Idq.d_axis = negate(Idq.d_axis);
Idq.q_axis = negate(Idq.q_axis);

control.ProportionalGain = 199727;
control.IntegralGain = 4390;
control.PositivePILimit = 32766;
control.NegativePILimit = 0;
control.IntegralPortionK_1 = 0;

control_v.ProportionalGain = 12245;
control_v.IntegralGain = 8;
control_v.PositivePILimit = 10000;
control_v.NegativePILimit = 0;
control_v.IntegralPortionK_1 = 0;

control_vshoot.ProportionalGain = 501 ;
control_vshoot.IntegralGain = 1102;
control_vshoot.PositivePILimit = 3604;
control_vshoot.NegativePILimit = 0;
control_vshoot.IntegralPortionK_1 = 0;
if(Vout > 26252)
        {
                Vpn = 32766;
        }
        else
        {
                Vpn = div_s(Vout,26252);
        }
```

```
  shoot = PI_control_vshoot(Vout ,Vref,&control_vshoot);
  Iqref = PI_control_v(Vref,Vpn,&control_v);
  Idq_out.d_axis = PI_control_d(Idq.d_axis,Idref,&control);
  Idq_out.q_axis = PI_control_q(Idq.q_axis,Iqref,&control);

  Idq_out.q_axis = Mod_adjust(Idq_out.q_axis);
  Idq_out.d_axis = Mod_adjust(Idq_out.d_axis);
  // Negate because to revert back to DSP transform equation
  Idq_out.d_axis = negate(Idq_out.d_axis);
  Idq_out.q_axis = negate(Idq_out.q_axis);

  MC2_cptrfmParkInv(&I_AlphaBeta_out, &Idq_out, &pSinCos);
  MC2_cptrfmClarkeInv(&I_abc_out,&I_AlphaBeta_out);

  pHandle.DutyCycle.PhaseC = add(I_abc_out.PhaseC,16384);
  pHandle.DutyCycle.PhaseB = add(I_abc_out.PhaseB,16384);;
  pHandle.DutyCycle.PhaseA = add(I_abc_out.PhaseA,16384);
 test.pwmChannel_1_Value = shoot;
 test.pwmChannel_2_Value = shoot;

PESL(PWMB,
PWM_UPDATE_VALUE_REGS_COMPL,(pwm_sComplementaryValues*)(&pHan
dle.DutyCycle));
PESL(PWMA, PWM_UPDATE_VALUE_REGS_INDEP,&test);
  sinecount = sinecount + 1;
if(sinecount == 400)
{
  sinecount = 0;
}
asm(nop);
}
```

```
/*
** ===================================================================
**     Event       :  AD1_OnZeroCrossing (module Events)
**
**     From bean   :  AD1 [ADC]
**     Description :
**         This event is called when the Zero crossing on any
**         channel has occurred. The Zero crossing means that the
**         sign of the result has been changed in the selected
**         direction by <Zero crossing> property. If the <Number of
**         conversions> property is greater than 1, then during one
**         measurement this event may be invoked more than once per
**         each of the measured channels. This event is available
**         only when <MeasureChan> and <EnableIntChanTrigger>
**         methods are disabled - "don't generate code".
**     Parameters  : None
**     Returns     : Nothing
**
*/
#pragma interrupt called /* Comment this line if the appropriate 'Interrupt preserve registers'
       property */
                    /* is set to 'yes' (#pragma interrupt saveall is generated before the ISR)      */
void AD1_OnZeroCrossing(void)
{
       static int zerocount=0;
       zerocount =  zerocount + 1;
         if(zerocount == 300)
       {
         if(init == 1)
         {
         init = 0;
         sinecount = 0;
```

```
        }
        }
      else
      {
        sinecount = 0;
        return;
      }
 }
Word16   PI_control_q(Word16   DesiredValue,Word16   MeasuredValue,mc_sPIparams
      *pParams)
{
 static Word16 ProportionalPortion, IntegralPortion, PIoutput,PIoutput_delta;
 static Word16 InputError,InputError_delta;
 static Word16 InputError_1 = 0;
 static Word16 PIoutput_1 = 0;
 Word16 NegILimit = -32766;
 Word16 PosILimit = 32766;
 /*-----------------------------------------------------------------------------------------*/
 /* Saturation mode must be set */
 /*   InputError = sub(DesiredValue, MeasuredValue); */  /* input error */
 /*-----------------------------------------------------------------------------------------*/
 /* input error calculation - 16bit range, with and without saturation mode  */

 InputError = sub(DesiredValue,MeasuredValue);
 InputError_delta = sub(InputError,  InputError_1);
 InputError_1 = InputError;
  /*-----------------------------------------------------------------------------------------*/
 /* proportional portion calculation */
 ProportionalPortion = mult_r(pParams -> ProportionalGain, InputError_delta) ;
 /*-----------------------------------------------------------------------------------------*/
 /* integral portion calculation */
 IntegralPortion = mult_r(pParams -> IntegralGain, InputError);
```

```
  /* integral portion limitation */
 if(IntegralPortion > PosILimit)
  pParams -> IntegralPortionK_1 = PosILimit;
 else
  if(IntegralPortion < NegILimit)
   pParams -> IntegralPortionK_1 =  NegILimit;
  else
   pParams -> IntegralPortionK_1 =  IntegralPortion;
 /*-----------------------------------------------------------------------------------------*/
 /* controller output calculation */
 /* proportional portion + integral portion */
 PIoutput = add(ProportionalPortion, pParams -> IntegralPortionK_1); /* controller output
       */
 PIoutput = add(PIoutput, PIoutput_1);
  /* controller output limitation */
 if(PIoutput > pParams -> PositivePILimit)
  PIoutput = pParams -> PositivePILimit;
 else
  if(PIoutput < pParams -> NegativePILimit)
   PIoutput =  pParams -> NegativePILimit;
PIoutput_1 = PIoutput;
 return (PIoutput);       /* controller output with limitation */
}
Word16    PI_control_d(Word16    DesiredValue,Word16    MeasuredValue,mc_sPIparams
       *pParams)
{
 static Word16 ProportionalPortion, IntegralPortion, PIoutput,PIoutput_delta;
 static Word16 InputError,InputError_delta;
 static Word16 InputError_1 = 0;
 static Word16 PIoutput_1 = 0;
 Word16 NegILimit = -32766;
 Word16 PosILimit = 32766;
```

```
/*-----------------------------------------------------------------------------------------*/
/* Saturation mode must be set */
/*   InputError = sub(DesiredValue, MeasuredValue); */  /* input error */
/*-----------------------------------------------------------------------------------------*/
/* input error calculation - 16bit range, with and without saturation mode  */
  InputError = sub(DesiredValue,MeasuredValue);
InputError_delta = sub(InputError,  InputError_1);
InputError_1= InputError;
  /*-----------------------------------------------------------------------------------------*/
/* proportional portion calculation */
ProportionalPortion = mult_r(pParams -> ProportionalGain, InputError_delta) ;
/*-----------------------------------------------------------------------------------------*/
/* integral portion calculation */
IntegralPortion = mult_r(pParams -> IntegralGain, InputError);
  /* integral portion limitation */
if(IntegralPortion > PosILimit)
  pParams -> IntegralPortionK_1 = PosILimit;
else
  if(IntegralPortion < NegILimit)
    pParams -> IntegralPortionK_1 =  NegILimit;
  else
    pParams -> IntegralPortionK_1 =  IntegralPortion;
  /*-----------------------------------------------------------------------------------------*/
/* controller output calculation */
/* proportional portion + integral portion */
PIoutput = add(ProportionalPortion, pParams -> IntegralPortionK_1); /* controller output
      */
PIoutput = add(PIoutput, PIoutput_1);
  /* controller output limitation */
if(PIoutput > pParams -> PositivePILimit)
  PIoutput = pParams -> PositivePILimit;
else
```

```
if(PIoutput < pParams -> NegativePILimit)
    PIoutput =  pParams -> NegativePILimit;
    PIoutput_1 = PIoutput;
    return (PIoutput);       /* controller output with limitation */
}
Word16    PI_control_v(Word16    DesiredValue,Word16    MeasuredValue,mc_sPIparams
      *pParams)
{
 static Word16 ProportionalPortion, IntegralPortion, PIoutput,PIoutput_delta;
 static Word16 InputError,InputError_delta;
 static Word16 InputError_1 = 0;
 static Word16 PIoutput_1 = 0;
 Word16 NegILimit = -32766;
 Word16 PosILimit = 32766;
 /*-----------------------------------------------------------------------------------------*/
 /* Saturation mode must be set */
 /*   InputError = sub(DesiredValue, MeasuredValue); */  /* input error */
 /*-----------------------------------------------------------------------------------------*/
 /* input error calculation - 16bit range, with and without saturation mode  */
   InputError = sub(DesiredValue,MeasuredValue);
    InputError_delta = sub(InputError,  InputError_1);
 InputError_1= InputError;
   /*-----------------------------------------------------------------------------------------*/
 /* proportional portion calculation */
 ProportionalPortion = mult_r(pParams -> ProportionalGain, InputError_delta) ;
 /*-----------------------------------------------------------------------------------------*/
 /* integral portion calculation */
 IntegralPortion = mult_r(pParams -> IntegralGain, InputError);
   /* integral portion limitation */
 if(IntegralPortion > PosILimit)
   pParams -> IntegralPortionK_1 = PosILimit;
 else
```

```
if(IntegralPortion < NegILimit)
     pParams -> IntegralPortionK_1 =  NegILimit;
   else
     pParams -> IntegralPortionK_1 =  IntegralPortion;
     /*-----------------------------------------------------------------------------------------*/
 /* controller output calculation */
 /* proportional portion + integral portion */
 PIoutput = add(ProportionalPortion, pParams -> IntegralPortionK_1); /* controller output
       */
 PIoutput = add(PIoutput, PIoutput_1);
  /* controller output limitation */
 if(PIoutput > pParams -> PositivePILimit)
   PIoutput = pParams -> PositivePILimit;
 else
   if(PIoutput < pParams -> NegativePILimit)
     PIoutput =  pParams -> NegativePILimit;
     PIoutput_1 = PIoutput;
   return (PIoutput);        /* controller output with limitation */
}
Word16  PI_control_vshoot(Word16  DesiredValue,Word16  MeasuredValue,mc_sPIparams
       *pParams)
{
 static Word16 ProportionalPortion, IntegralPortion, PIoutput,PIoutput_delta;
 static Word16 InputError,InputError_delta;
 static Word16 InputError_1 = 0;
 static Word16 PIoutput_1 = 0;
 Word16 NegILimit = -32766;
 Word16 PosILimit = 32766;
 /*-----------------------------------------------------------------------------------------*/
 /* Saturation mode must be set */
 /*   InputError = sub(DesiredValue, MeasuredValue); */  /* input error */
 /*-----------------------------------------------------------------------------------------*/
```

```
/* input error calculation - 16bit range, with and without saturation mode  */
  InputError = sub(DesiredValue,MeasuredValue);
     InputError_delta = sub(InputError,  InputError_1);
InputError_1= InputError;
  /*-----------------------------------------------------------------------------------------*/
/* proportional portion calculation */
ProportionalPortion = mult_r(pParams -> ProportionalGain, InputError_delta) ;
/*-----------------------------------------------------------------------------------------*/
/* integral portion calculation */
IntegralPortion = mult_r(pParams -> IntegralGain, InputError);
  /* integral portion limitation */
if(IntegralPortion > PosILimit)
  pParams -> IntegralPortionK_1 = PosILimit;
else
  if(IntegralPortion < NegILimit)
    pParams -> IntegralPortionK_1 =  NegILimit;
  else
    pParams -> IntegralPortionK_1 =  IntegralPortion;
   /*-----------------------------------------------------------------------------------------*/
/* controller output calculation */
/* proportional portion + integral portion */
PIoutput = add(ProportionalPortion, pParams -> IntegralPortionK_1); /* controller output
      */
PIoutput = add(PIoutput, PIoutput_1);
 /* controller output limitation */
if(PIoutput > pParams -> PositivePILimit)
  PIoutput = pParams -> PositivePILimit;
else
  if(PIoutput < pParams -> NegativePILimit)
    PIoutput =  pParams -> NegativePILimit;
    PIoutput_1 = PIoutput;
  return (PIoutput);       /* controller output with limitation */
```

```
}
Word16 Mod_adjust(Word16 initial)
{       Word32 result;
        static Word16 cst = 16384;
        result = L_mult_ls(L_deposit_l(initial), cst);
        return (extract_l(result));
}
```