Chapter 4

Algorithm Testing

A large number of tests were conducted on this algorithm. These tests were conducted to ensure that the fitness calculation is correct, determine good values for the parameters, compare various options, and to compare this algorithm with published results.

Ten test problems were used to evaluate the algorithm and are presented in Section 4.1. The tests performed include accuracy verification in Section 4.2, parameter value tests in Section 4.3, and run time evaluation in Section 4.4. The results obtained are summarised in Section 4.5 and comparisons to published results are given in Section 4.5.1. The implications of the results obtained here will be considered in Chapter 5.

4.1 Test Problems

The problems used to test this algorithm are presented in this section. Ten problems from a number of different sources and circumstances were used to test the algorithm as thoroughly as possible. A number of active devices, manufacturers, and types of problem were considered to provide as wide a variety of test cases as possible.

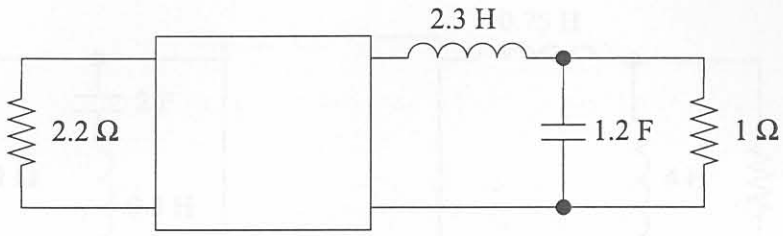

Figure 4.1: Test Problem 2.

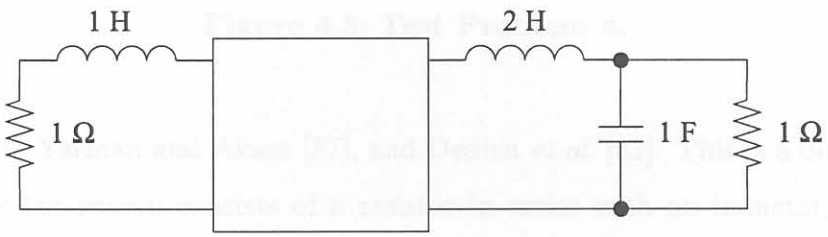

Figure 4.2: Test Problem 3.

Problem 1 is taken from Abrie [2] and involves matching a source of resistance of 25 Ω to a load resistance of 100 Ω from 2 to 6 GHz. A frequency spacing of 0.25 GHz was used for this problem.

Problem 2 has been used extensively in the literature to test impedance matching algorithms. Papers that use this problem include Fano [57, 58], Carlin [4], Carlin and Amstutz [5], and Dedieu *et al.* [82]. This is a single matching problem where a resistive source is matched to a network consisting of the parallel combination of a capacitor and a resistor in series with an inductor as shown in Figure 4.1. The value of the source resistor is not specified, but Carlin [4] found that a value of 2.2 Ω gives the best results, and experiments with this algorithm indicate that this is true in this case as well. The matching network must have a low-pass form with a maximum frequency of 1 rad/s. The circuit was scaled in frequency so that the maximum frequency is 1 GHz, and a frequency spacing of 0.1 GHz was used. The impedances were scaled by 50 Ω for the distributed, mixed, and microstrip tests to ensure sensible results are obtained.

Problem 3 is also taken from the literature and is used by Carlin and Yarman [8], Yarman

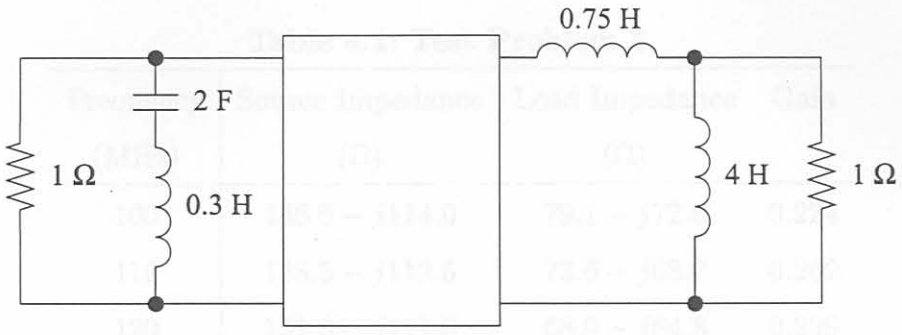

Figure 4.3: Test Problem 4.

and Fettweis [9], Yarman and Aksen [87], and Dedieu *et al.* [82]. This is a double matching problem where the source consists of a resistor in series with an inductor, and the load consists of the parallel combination of a capacitor and a resistor in series with an inductor as shown in Figure 4.2. The network must match the load to the source from 0 to 1 rad/s, so this is a low-pass problem. The problem was again scaled in frequency so that the frequency range is from 0 to 1 GHz, and a frequency spacing of 0.1 GHz was used. The impedances were scaled by 50 Ω for the distributed, mixed, and microstrip tests to ensure sensible results are obtained.

Problem 4 appears in the papers by Carlin and Yarman [8], Yarman and Fettweis [9], and Dedieu *et al.* [82]. The problem involves matching a source consisting of a resistor in parallel with the series combination of a capacitor and an inductor to a load consisting of the parallel combination of an inductor and a resistor is series with an inductor as shown in Figure 4.3. The frequency range for this problem extends from 0.3 to 1 rad/s, but this range was scaled to be from 0.3 to 1 GHz with frequency steps of 0.1 GHz being used. The impedances were scaled by 50 Ω for the distributed, mixed, and microstrip tests to ensure sensible results are obtained.

The number of points used for Problems 1 to 4 was chosen to allow fast simulations while still producing good results. Doubling the frequency spacing for Problem 1 produces slightly better results, while halving the frequency spacing produces better results for Problems 2 and 3, and essentially the same results for Problem 4. This means that the frequency

Table 4.1: Test Problem 5.

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	Gain
100	$146.0 - j114.0$	$79.1 - j72.6$	0.224
110	$138.5 - j112.5$	$73.6 - j68.7$	0.262
120	$131.0 - j111.0$	$68.0 - j64.8$	0.299
140	$137.0 - j103.0$	$63.2 - j56.8$	0.400
160	$144.0 - j88.0$	$59.6 - j47.9$	0.559
180	$140.0 - j88.0$	$57.5 - j47.3$	0.709
190	$136.5 - j92.0$	$55.0 - j41.9$	0.764
200	$133.9 - j96.0$	$53.5 - j40.4$	0.818

Table 4.2: Test Problem 6.

Frequency (GHz)	Source Impedance (Ω)	Load Impedance (Ω)	Gain
2	$75.08 + j0.84$	$83.16 - j135.9$	0.7462
3	$81.22 + j2.98$	$53.02 - j102.9$	0.8874
4	$81.94 - j1.52$	$35.56 - j77.55$	0.8802
5	$85.15 - j1.40$	$39.93 - j68.64$	1.0000
6	$81.44 - j1.19$	$22.69 - j46.11$	0.8605

spacings used above are conservative in the sense that different frequency spacings typically lead to better results.

Problem 5 is a double matching problem taken from Abrie [2]. Impedances and transducer gains are specified at a number of frequency points from 100 to 200 MHz as shown in Table 4.1.

Problem 6 considers an interstage match between two transistors and is also taken from Abrie [2]. The problem is part of the design of a two-stage amplifier. Impedances and

Table 4.3: Test Problem 7.

Frequency (GHz)	Impedance (Ω)	Gain
9.5	$1.932 - j10.43$	0.07468
10.0	$5.860 - j7.550$	0.2468
10.5	$7.200 - j4.424$	0.3334
11.0	$8.199 - j1.178$	0.4288
11.5	$9.976 + j1.985$	0.6111
12.0	$11.03 + j4.857$	0.8252
12.5	$10.02 + j7.515$	0.7809
13.0	$9.265 + j9.974$	0.7816
13.5	$8.671 + j12.47$	0.7978
14.0	$8.215 + j15.27$	0.8397
14.5	$6.952 + j18.36$	0.7546
15.0	$6.906 + j21.62$	0.8803
15.5	$6.281 + j25.21$	0.9430

transducer gains are specified at a number of frequency points from 2 to 6 GHz as shown in Table 4.2.

Problem 7 involves mismatching the output of a transistor to level the gain. The transistor chosen was the CFY35 GaAs FET from Infineon biased at 2.5 V and 10 mA. The gain was levelled at 9 dB from 9.5 to 15.5 GHz in steps of 0.5 GHz. The problem was converted to a passive matching problem using the equations derived by Abrie [2]. The impedances and transducer gains required by the transistor are given in Table 4.3. The transistor impedances in Table 4.3 were used as the load impedance, and the source impedance is 50 Ω at all frequencies.

Problem 8 requires the input of a transistor to be matched so as to obtain a specified noise figure. The device used is an Agilent ATF-36163 PHEMT biased at 2 V and 10 mA. The

Table 4.4: Test Problem 8.

Frequecy (GHz)	Impedance (Ω)	Gain
5	$32.9 + j60.0$	0.321
6	$27.6 + j43.5$	0.335
7	$26.0 + j32.7$	0.355
8	$27.9 + j22.7$	0.371
9	$28.3 + j14.8$	0.335
10	$31.6 + j4.0$	0.319
11	$37.1 - j7.5$	0.304
12	$46.0 - j17.1$	0.321
13	$64.5 - j24.0$	0.402
14	$97.5 - j20.3$	0.515
15	$136.9 + j14.4$	0.609
16	$138.5 + j78.8$	0.704
17	$87.6 + j91.9$	0.829
18	$48.1 + j86.1$	0.962

noise figure was levelled at 2 dB from 5 to 8 GHz in steps of 1 GHz. This would not necessarily be a good approach to designing a real amplifier because the problem should rather be set up to ensure that the noise figure is less than a specified value. However, the objective here is to set up a difficult test problem and designing a matching network for a specified gain is more complex than designing for a minimum gain. The problem was converted to a passive matching problem using the equations derived by Abrie [2]. The impedances and transducer gains required by the transistor are given in Table 4.4. The transistor impedances in Table 4.4 were used as the load impedance, and the source impedance is 50 Ω at all frequencies.

Problem 9 considers matching the output of a transistor for maximum output power. The active device is an Ericsson PTF10112 LDMOS biased at 28 V and 580 mA. The optimum

Table 4.5: Test Problem 9.

Frequency (GHz)	Impedance (Ω)
1.75	$1.48 - j0.25$
1.80	$1.56 + j0.20$
1.85	$1.66 + j0.50$
1.90	$1.32 + j0.80$
1.95	$1.16 + j0.60$
2.00	$1.10 + j0.45$
2.05	$1.18 + j0.30$

Table 4.6: Test Problem 10.

Frequency (GHz)	Impedance (Ω)
1.775	$34.27 + j36.07$
1.780	$41.33 + j33.14$
1.785	$48.17 + j27.34$
1.790	$53.12 + j18.53$
1.795	$54.45 + j7.97$
1.800	$51.68 - j2.07$
1.805	$46.01 - j9.68$
1.810	$39.24 - j14.31$
1.815	$32.73 - j16.47$
1.820	$27.09 - j16.96$
1.825	$22.47 - j16.47$

power match is required by the transistor given in the datasheet and is repeated in Table 4.5. The transistor impedances in Table 4.5 were used as the load impedance, with a source impedance of 50 Ω being used at all frequencies.

Problem 10 requires an antenna to be matched to 50 Ω. The antenna is a probe-fed patch antenna on a GIL MC3D substrate, and the data were supplied by Mr David de Haaij. Mr de Haaij is working towards a masters degree at the University of Pretoria and is considering patch antenna impedance matching. The antenna is designed for a 50 Ω system and a centre frequency of 1.8 GHz. Its dimensions are a length of 43.3 mm, a width of 47 mm, and a feed inset of 11.6 mm. The original data supplied was from 1.6 to 2 GHz in steps of 1 MHz. Using this full range would be impractical because the wide bandwidth would lead to poor results, and the algorithm would be slow because of the large number of frequency points. The data was thus reduced to be from 1.775 GHz to 1.825 GHz (a 2.78% bandwidth with a centre frequency of 1.8 GHz) in steps of 5 MHz as shown in Table 4.6. The antenna impedances in Table 4.6 were used as the load impedance, and the source impedance is 50 Ω at all frequencies. This is an extremely useful problem because an antenna is a resonant structure unlike the devices in the problems considered above.

This selection of test problems provides a large number of different cases which can be used to evaluate the performance of this algorithm. The problems include low-pass and band-pass networks, gain and noise matches, a GaAs FET and a PHEMT, single and double matching problems, resonant structures, purely real loads and sources, and established and new problems.

4.2 Accuracy Verification

The first important stage of testing involves confirming that the error function calculations are correct. This was done using Hewlett-Packard's Touchstone microwave circuit simulation software. Only single elements are considered here because complete circuits will be accurate if all the element models are accurate.

Version 2.000.104.019 of EEsof was used to verify the accuracy of the error calculations. This version of EEsof was released in 1994 and is thus a little old. This is not a great

problem because the major changes that have been made are to the user interface and this is obviously not relevant here. While the EESof models are not perfect they do provide a basis for evaluating the accuracy of the models implemented here. Using comparisons to measurements or full-wave electromagnetic simulations would be desirable, but were considered to be beyond the scope of this work. The agreement between EESof and the models implemented here should be good because the EESof models are, in most cases, based on the published models used here.

4.2.1 Single Elements

The first round of tests was conducted by considering only one type of element to determine the accuracy of each element. The input impedance of a 50 Ω system was calculated and then compared to the results obtained using EEsof.

The error was calculated from the magnitude of a type of reflection coefficient defined by

$$E = \left| \frac{Z - Z_{EEsof}}{Z + Z_{EEsof}} \right| \tag{4.1}$$

where E is the error, Z is the input impedance calculated, and Z_{EEsof} is the input impedance calculated by EEsof. The difference between the definition of reflection coefficient given in (3.21) and (4.1) is that conjugates are not used here. This change is necessary because the objective is to find the error between two impedances rather than a conjugate match.

Rounding errors caused some difficulties. The highest error for a parallel inductor was 0.227 and occurred with impedances of $2.2 \times 10^{-14} + j10^{-6}$ for EEsof and $7.9 \times 10^{-15} + j6.3 \times 10^{-7}$ for the current algorithm. This is obviously not a true error because the impedances are very small so all points where the real and imaginary parts of both impedances were less than 10^{-6} were ignored.

The first tests were run for purely lumped components. The EEsof models for an ideal inductor (IND) and capacitor (CAP) were used. The component values were logarithmically

swept from 10^{-15} to 10^{-3}. The highest error was less than 10^{-8}, so the lumped component models used in this algorithm are exact to within rounding errors.

Perfect transmission lines were tested next. The EEsof models for a series transmission line (TLIN), a parallel shorted stub (TLSC), and a parallel open stub (TLOC) were used here. These models require the length in degrees at a specified frequency and the characteristic impedance of the line. The minimum and maximum values of the characteristic impedance were 1 Ω and 400 Ω respectively. These values are the rounded minimum and maximum impedances obtained when the effective dielectric constant of a microstrip line can vary from 1 to 10, and the width of the microstrip line can vary from $0.01h$ to $100h$, where h is the substrate height. The length was varied from 0.1λ to 1λ, where λ is the wavelength of the transmission line. The highest error obtained was less than or equal to 10^{-4} in all cases, so the transmission line models used in this algorithm are exact to within rounding errors.

The next step was to test the system using microstrip lines using the full model which includes dispersion effects. The EEsof models for a series microstrip line (MLIN), a parallel shorted stub (MLSC), and a parallel open stub (MLOC) all use the full microstrip model including dispersion. These models require the substrate to be specified, and the length and width of the lines to be given. Only the relative dielectric constant and height of the substrate were specified with all other values being set to zero. The substrate used has a height of 1 mm and a relative dielectric constant of 1, 2, 5, and 10. This substrate was used for all the microstrip and discontinuity tests in this section. The minimum and maximum line widths were $0.01h$ and $100h$ respectively, and the line length was varied from 1 mm to 10 cm. The worst results for a series microstrip line are shown in Table 4.7, and are typical of all three cases. The results are very good and show that the model used here is accurate when the substrate relative dielectric constant is low and the frequency is low.

The open-end model was tested next using the EEsof microstrip line model that includes the end effect (MLEF) with the length of the lines set to zero to isolate the end effect. The average and worst results are shown in Table 4.8 and the agreement is good even at high

Table 4.7: Microstrip Line Worst Results.

Frequency (GHz)	$\varepsilon_r = 1$	$\varepsilon_r = 2$	$\varepsilon_r = 5$	$\varepsilon_r = 10$
0.1	0	1.33×10^{-4}	3.41×10^{-4}	5.23×10^{-4}
0.2	0	2.90×10^{-4}	7.67×10^{-4}	1.52×10^{-3}
0.3	0	5.03×10^{-4}	1.32×10^{-3}	2.40×10^{-3}
0.4	0	1.04×10^{-3}	2.10×10^{-3}	4.08×10^{-3}
0.5	1.15×10^{-6}	1.22×10^{-3}	3.85×10^{-3}	4.99×10^{-3}
0.6	2.01×10^{-6}	1.35×10^{-3}	3.31×10^{-3}	6.11×10^{-3}
0.7	4.05×10^{-7}	1.52×10^{-3}	4.06×10^{-3}	7.43×10^{-3}
0.8	4.18×10^{-7}	2.06×10^{-3}	5.22×10^{-3}	8.68×10^{-3}
0.9	1.67×10^{-6}	2.18×10^{-3}	5.20×10^{-3}	9.37×10^{-3}
1.0	1.15×10^{-6}	2.63×10^{-3}	6.27×10^{-3}	1.10×10^{-2}
2.0	1.02×10^{-5}	5.41×10^{-3}	1.11×10^{-2}	1.62×10^{-2}
3.0	1.00×10^{-5}	7.82×10^{-3}	1.41×10^{-2}	3.03×10^{-2}
4.0	1.50×10^{-5}	9.47×10^{-3}	2.17×10^{-2}	2.05×10^{-2}
5.0	2.11×10^{-5}	1.34×10^{-2}	2.44×10^{-2}	3.78×10^{-2}
6.0	1.01×10^{-5}	1.40×10^{-2}	3.41×10^{-2}	3.91×10^{-2}
7.0	4.40×10^{-6}	1.53×10^{-2}	4.35×10^{-2}	4.32×10^{-2}
8.0	1.22×10^{-5}	2.16×10^{-2}	5.24×10^{-2}	4.91×10^{-2}
9.0	1.02×10^{-5}	1.58×10^{-2}	5.70×10^{-2}	7.31×10^{-2}
10.0	1.33×10^{-5}	2.41×10^{-2}	5.75×10^{-2}	9.13×10^{-2}

frequencies.

The model used for the inductance of a via hole was compared to the VIA2 model used by EEsof. The results were identical indicating that the model implemented here is the same as the model implemented by EEsof.

Microstrip width steps were compared to the EEsof microstrip step model (MSTEP). The width of each of the lines was varied from $0.1h$ to $10h$, and the width ratio between the

Table 4.8: Microstrip Open End Results.

Frequency	$\varepsilon_r = 1$		$\varepsilon_r = 2$		$\varepsilon_r = 5$		$\varepsilon_r = 10$	
(GHz)	Mean	Worst	Mean	Worst	Mean	Worst	Mean	Worst
0.1	$< 10^{-3}$	0.002	$< 10^{-3}$	0.001	$< 10^{-3}$	0.001	$< 10^{-3}$	0.001
0.2	0.001	0.004	$< 10^{-3}$	0.003	$< 10^{-3}$	0.002	$< 10^{-3}$	0.002
0.3	0.001	0.006	0.001	0.004	$< 10^{-3}$	0.003	$< 10^{-3}$	0.002
0.4	0.001	0.008	0.001	0.006	0.001	0.004	$< 10^{-3}$	0.002
0.5	0.001	0.010	0.001	0.007	0.001	0.004	$< 10^{-3}$	0.002
0.6	0.002	0.012	0.001	0.008	0.001	0.005	$< 10^{-3}$	0.001
0.7	0.002	0.014	0.001	0.009	0.001	0.005	$< 10^{-3}$	0.001
0.8	0.002	0.016	0.001	0.010	0.001	0.005	$< 10^{-3}$	0.001
0.9	0.002	0.018	0.002	0.011	0.001	0.005	$< 10^{-3}$	0.001
1.0	0.003	0.020	0.002	0.012	0.001	0.005	$< 10^{-3}$	0.002
2.0	0.005	0.035	0.003	0.018	0.001	0.003	0.002	0.009
3.0	0.007	0.046	0.004	0.020	0.001	0.002	0.003	0.014
4.0	0.009	0.052	0.004	0.021	0.001	0.004	0.004	0.019
5.0	0.010	0.056	0.005	0.021	0.001	0.007	0.005	0.023
6.0	0.012	0.059	0.005	0.020	0.002	0.010	0.007	0.026
7.0	0.013	0.061	0.005	0.020	0.003	0.012	0.008	0.029
8.0	0.014	0.063	0.005	0.020	0.003	0.014	0.010	0.033
9.0	0.015	0.064	0.005	0.019	0.004	0.016	0.011	0.036
10.0	0.015	0.065	0.005	0.019	0.005	0.019	0.013	0.038

lines was varied from a factor of 2 to a factor of 10. A number of options for the step discontinuity model were considered with the model presented in Section 2.4.5 giving the best results. The results are given in Table 4.9 where the data are presented as the ratio between the substrate height and the wavelength in the substrate when the error is 1% and 5%. The model is seen to perform best when the relative dielectric constant is low and the ratio of the two line thicknesses is small.

Table 4.9: Microstrip Width Step Results.

w_1/w_2	$\varepsilon_r = 1$		$\varepsilon_r = 2$		$\varepsilon_r = 5$		$\varepsilon_r = 10$	
	1%	5%	1%	5%	1%	5%	1%	5%
2	0.006	0.033	0.006	0.027	0.005	0.022	0.004	0.017
3	0.009	0.037	0.009	0.038	0.006	0.024	0.005	0.018
5	0.004	0.019	0.008	0.036	0.007	0.024	0.005	0.017
10	0.002	0.010	0.005	0.020	0.010	0.030	0.007	0.020

Table 4.10: Microstrip T-Junction Results.

w_1/w_2	$\varepsilon_r = 1$		$\varepsilon_r = 2$		$\varepsilon_r = 5$		$\varepsilon_r = 10$	
	1%	5%	1%	5%	1%	5%	1%	5%
1	0.011	0.017	0.011	0.017	0.010	0.016	0.010	0.016
2	0.006	0.025	0.006	0.024	0.005	0.021	0.004	0.018
3	0.002	0.008	0.002	0.009	0.002	0.008	0.001	0.006
5	0.002	0.009	0.001	0.008	0.001	0.007	0.001	0.006
10	0.001	0.005	0.001	0.005	0.002	0.005	0.001	0.004

The microstrip T-junction model was compared to the EEsof T-junction model (MTEE). The width of each of the lines was varied from $0.1h$ to $10h$, and the width ratio between the lines was varied from a factor of 1 to a factor of 10. The results are given in Table 4.10 where the data is presented as the ratio between the substrate height and the wavelength in the substrate when the error is 1% and 5%. The model is seen to perform best when the relative dielectric constant is low, and the ratio of the line thicknesses is small.

The microstrip cross model was compared to the EEsof cross model (MCROS). The width of each of the lines was varied from $0.4h$ to $2h$, and the width ratio between the lines was varied from a factor of 1 to a factor of 5. This is the maximum range of values over which the EEsof cross model is accurate. The results are given in Table 4.11 where the data is presented as the ratio between the substrate height and the wavelength in the substrate

Table 4.11: Microstrip Cross Results.

w_1/w_2	$\varepsilon_r = 1$		$\varepsilon_r = 2$		$\varepsilon_r = 5$		$\varepsilon_r = 10$	
	1%	5%	1%	5%	1%	5%	1%	5%
1	0.002	0.011	0.004	0.017	0.007	0.036	0.013	0.054
2	0.001	0.005	0.001	0.007	0.002	0.012	0.003	0.016
3	0.001	0.004	0.003	0.013	0.002	0.008	0.002	0.011
5	0.001	0.002	0.001	0.003	0.001	0.005	0.001	0.007

when the error is 1% and 5%. The model is seen to be poor, but this is expected because this is a modified T-junction model rather than a true cross model.

4.2.2 Circuits

The accuracy of complete circuits is considered here. The microstrip results obtained in the tests conducted for Section 4.5 include comparisons to the results obtained using EEsof.

The results in Tables A.4, A.8, A.12, A.16, A.20, A.24, A.28, A.32, A.36, and A.40 on pages 160 to 173 include both the results obtained with the current algorithm and the results obtained using EEsof. The first results are those obtained using the current algorithm and the second results are those obtained using EEsof. Crosses were not allowed because of the comparatively poor performance of the cross model.

The agreement is seen to be very good in most cases with the only exceptions being Problems 2 to 4. These problems all use an air substrate with a height of 3 mm. Problem 5 uses the same substrate, but does not have large errors, probably because it has a much lower maximum frequency than Problems 2 to 4.