

CHAPTER 6: LAYOUT AND FABRICATION

6.1 INTRODUCTION

In order to verify the simulated results given in Chapter 5 the LNA was submitted for fabrication in the IBM 7WL 0.18 μm SiGe BiCMOS process on a MPW run. Thirty prototypes were received.

The layout of the LNA was done using the Virtuoso Layout Editor. The HIT-kit provided by IBM offers parameterized cells which greatly simplifies the layout process. Assura was used to do the DRC based on the rule file included in the HIT-kit and also for layout-versus-schematic checking to verify the correctness of the layout. The above process is discussed in this chapter along with the packaging considerations.

A test PCB was designed for the measurement of the LNA performance. The schematic of the bias circuits on this PCB and other related considerations are also discussed.

6.2 CIRCUIT LAYOUTS

Two versions of the LNA was submitted for fabrication as well as a separate first and second amplifier stage to allow verification of those sections of the LNA separately should unforeseen errors prevent correct characterisation of the complete LNA circuits. The first LNA that was implemented is the version without linearity improvement discussed in Section 5.5. The second is the LNA optimized for linearity by adding emitter degeneration in the second and third stages as discussed in Section 5.5.5. The layouts of the individual circuits are shown in Figure 6.1 to Figure 6.4. Additional layout views showing more detail of each amplifier stage are provided in Appendix B.

Spiral inductors were laid out within an 80 μm perimeter free of substrate contacts and other components as suggested in the process documentation and discussed in Section 3.7. A ring of substrate contacts was placed around this perimeter, and sufficient substrate contacts were placed close to the other circuit components as well. An interconnect current density of 1 $\text{mA}/\mu\text{m}$ has been used throughout.

The final chip area occupied by the LNA without bonding pads is 740 μm x 750 μm which is 0.555 mm^2 . There is however a significant chip area that is not used for the LNA and

could contain other circuits in an integrated system or the three inductors could be placed length wise to minimize the occupied area. The total area covered by the LNA circuit itself is 0.4272 mm^2 .

As discussed in Section 2.8 active inductors can be substituted for passive inductors in circuits where noise is not very important and also at the cost of increased power consumption. The advantages of active inductors are increased Q-factors and greatly reduced chip area. If the load inductor of stage 2 (L_3) is implemented as an active inductor since the noise at the second stage output is greatly reduced when referred to the input, the total chip area can be reduced by $78,400 \mu\text{m}^2$ if the active inductor circuit is placed in the open area left of C_F in Figure 6.1. That is 18.4 % reduction in chip area.

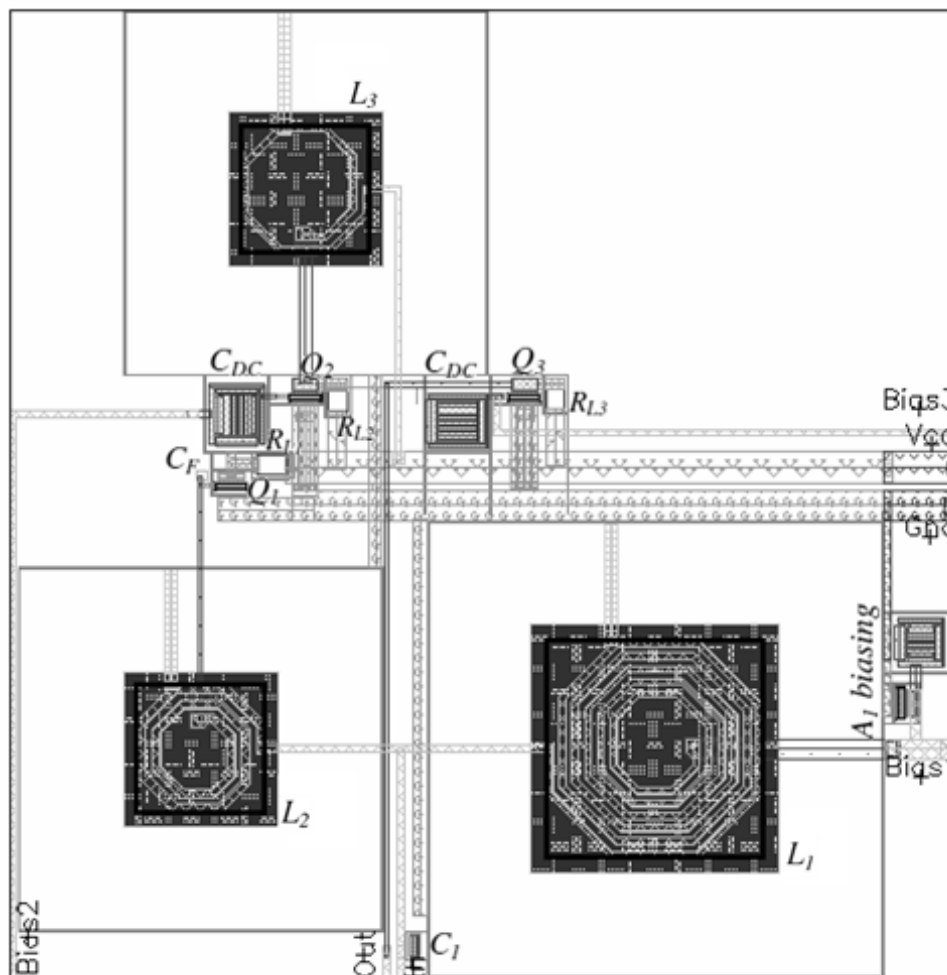


Figure 6.1. Layout of the standard LC-ladder and capacitive shunt-shunt feedback LNA.

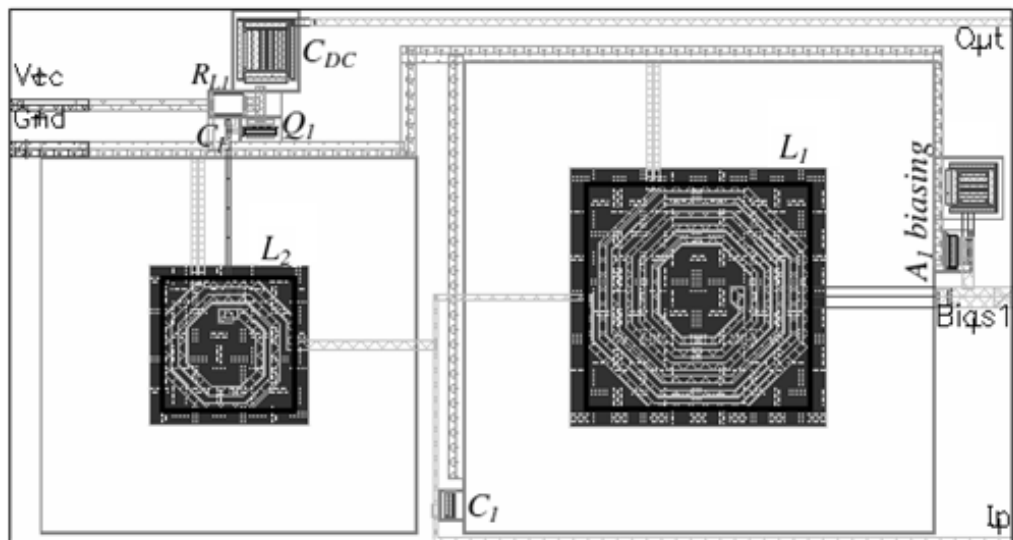


Figure 6.2. Layout of the first amplifier stage and input matching network.

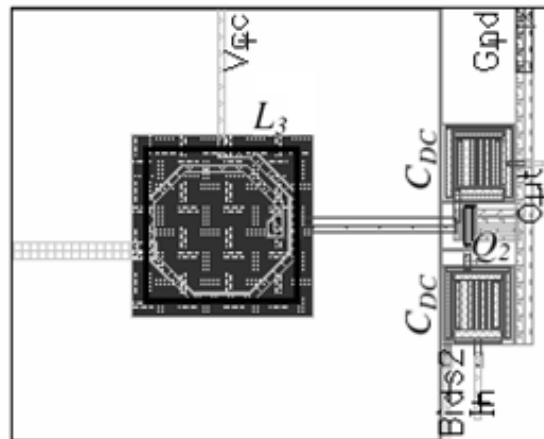


Figure 6.3. Layout of the second amplifier stage.

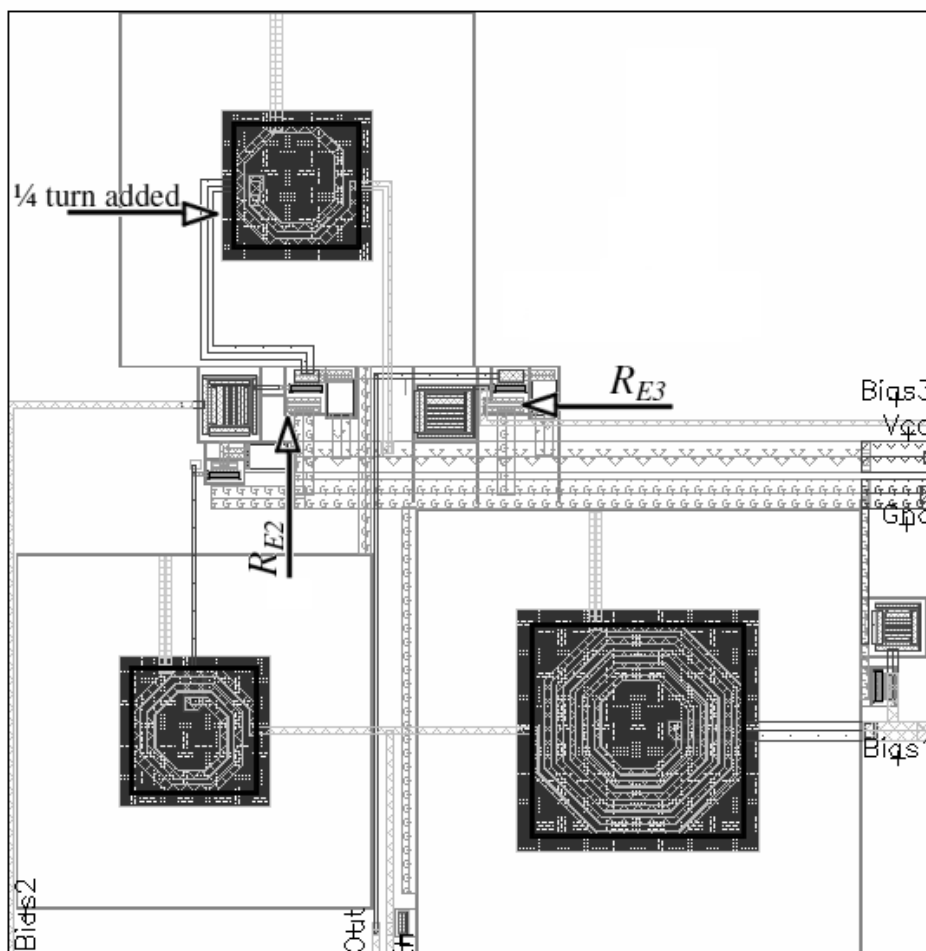


Figure 6.4. Layout of the LC-ladder and capacitive feedback LNA optimized for linearity indicating the additional resistors and modified inductor.

6.3 PHOTOS OF THE FABRICATED CHIP

The fabricated chip was photographed under a microscope. These photos are shown in Figure 6.5 to Figure 6.9. The top metal layers are clearly visible, showing the inductors, capacitors and most of the interconnects. In Figure 6.5 the LNAs are in the top left corner as indicated. The circuits for two other projects are also included on this chip.

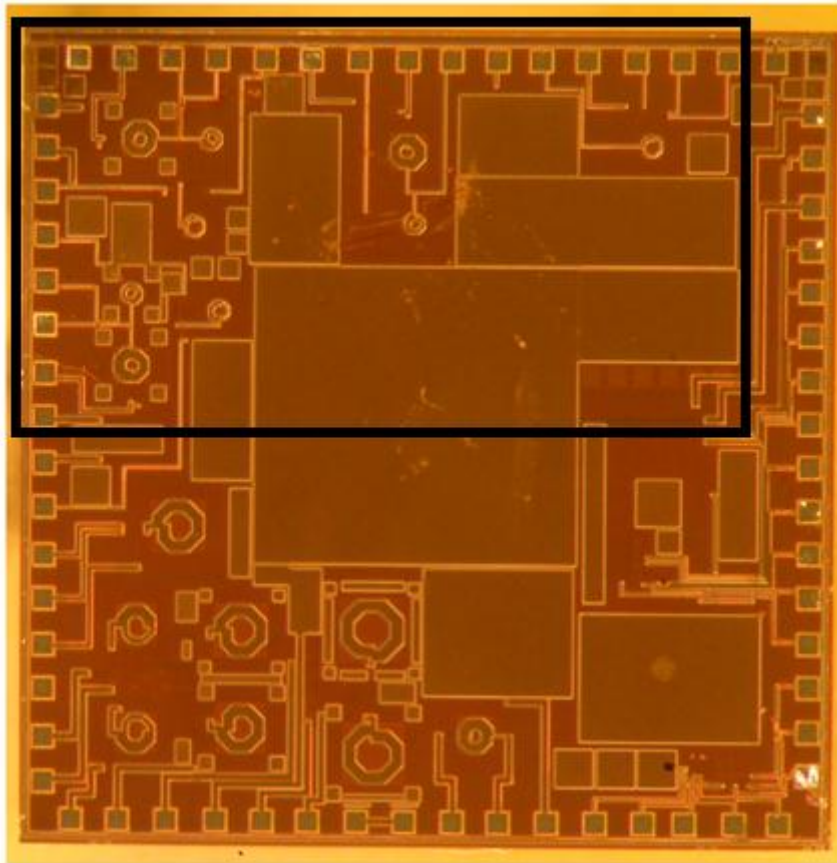


Figure 6.5. Overall view of the fabricated chip showing the LNAs
(compare to the bonding diagram in Figure B.7).

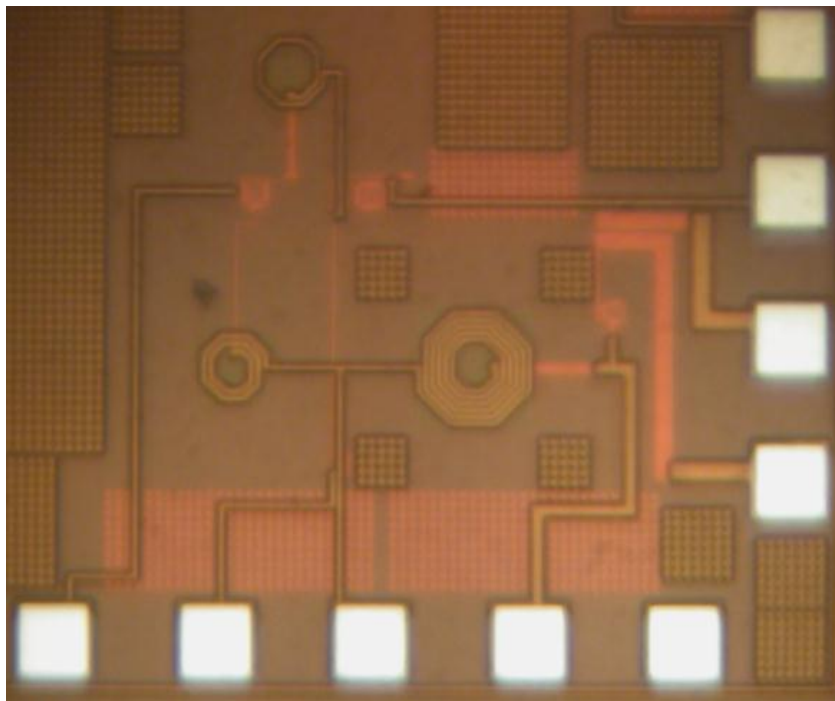


Figure 6.6. Fabricated standard LC-ladder and capacitive shunt-shunt feedback LNA
(compare to Figure 6.1).

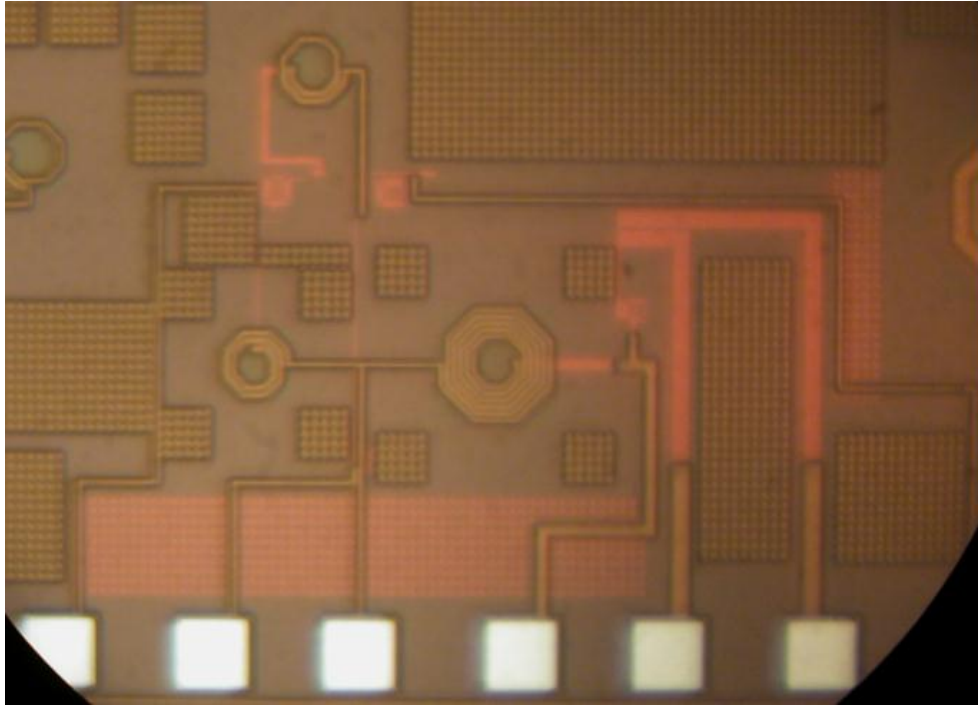


Figure 6.7. Fabricated LC-ladder and capacitive feedback LNA optimized for linearity (compare to Figure 6.4).

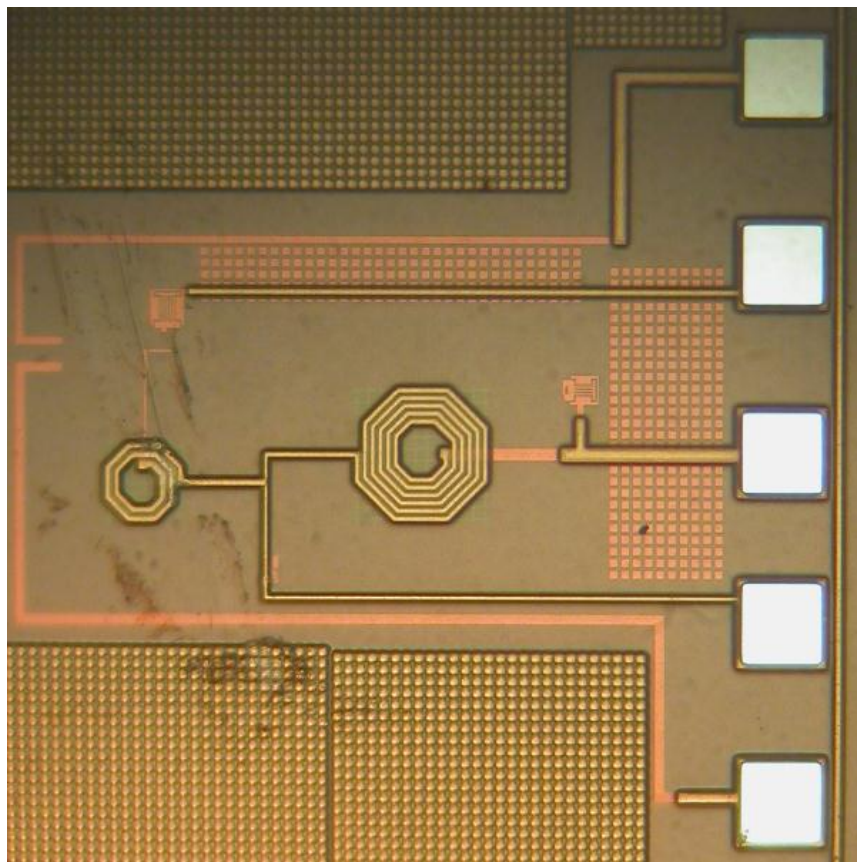


Figure 6.8. Fabricated first amplifier stage and input matching network (compare to Figure 6.2).

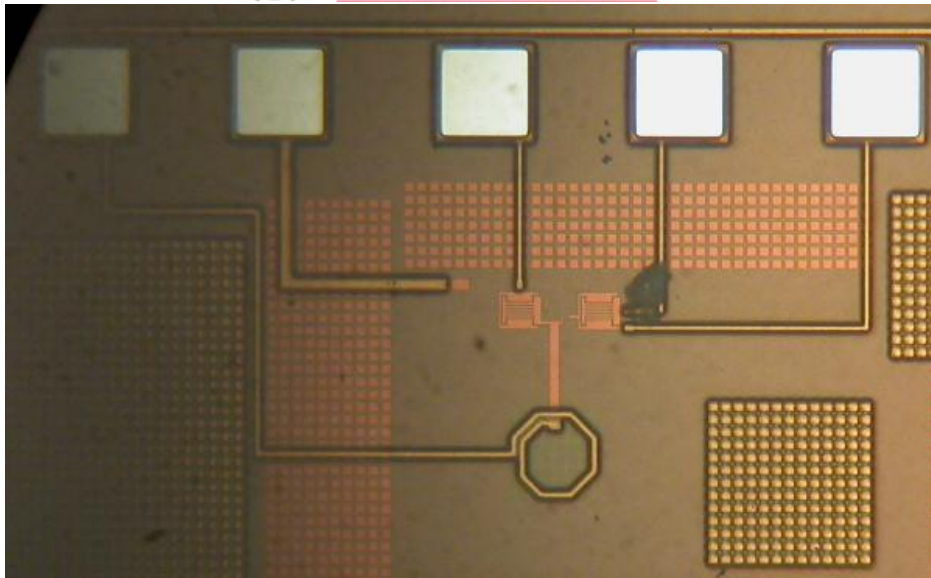


Figure 6.9. Fabricated second amplifier stage (compare to Figure 6.3).

6.4 PACKAGING

Since on-wafer measurement equipment was not available the dies were packaged and mounted on a PCB. Two packaging options were considered namely QFN and BGA packages. Since the solder joints of BGAs are error prone due to uneven heat distribution and cracking due to stresses QFN packages were chosen.

The LNA was fabricated in a MPW run with two other projects on the same chip and as such a 64 pin QFN package was used of which a drawing is shown in Figure 6.10 and the final IC mounted on the test PCB is shown in Figure 6.11. The outer dimensions of the package are 9 mm x 9 mm x 1.4 mm.

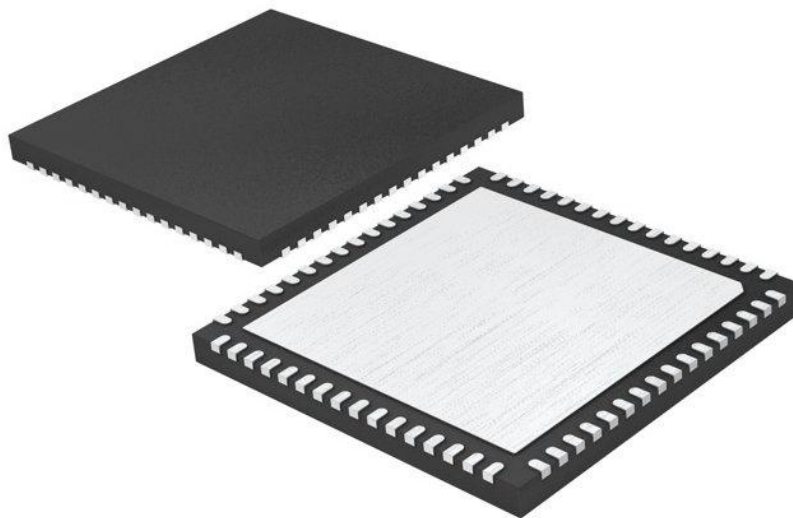


Figure 6.10. Drawing of a 64 pin QFN package.



Figure 6.11. Photo of the 64 pin QFN packaged IC mounted on the test PCB.

6.5 PACKAGE PARASITICS AND ITS EFFECT ON PERFORMANCE

Unfortunately the bond wire inductance in QFN packages is approximately 1 nH per millimetre which greatly attenuates the signal above 10 GHz. To evaluate the effect of the bond wire inductance the circuit in Figure 6.12 was simulated with the most important package parasitics included. Since the package model was not available 1 nH inductance was assumed for each bond wire. The bond pad at the input is not shown since it has already been absorbed into C_I of the IMN.

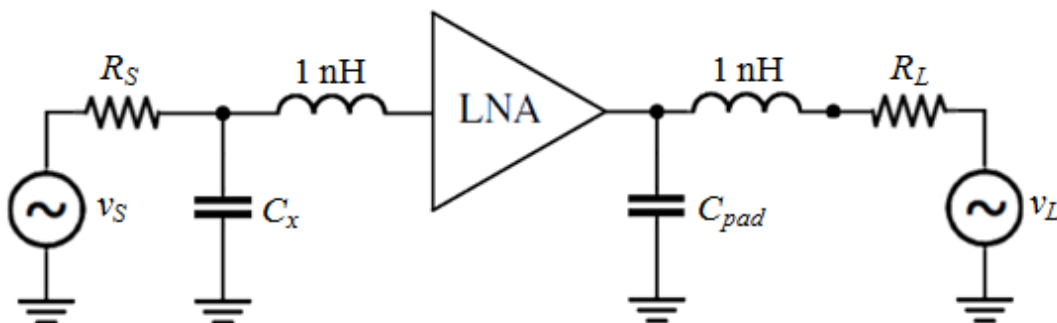


Figure 6.12. Schematic of the test bench circuit including package parasitics – the input pad capacitance has been absorbed in the IMN.

It was found that performance is severely degraded above 10 GHz by the bond wire inductance as shown in Figure 6.13 to Figure 6.15. The output pad capacitance has only a negligible influence on the high frequency gain. Through subsequent simulations it was found that increasing the shunt capacitance on either side of the bond wire inductance improves the performance somewhat and this is also shown. The final implemented value

of C_I is 230 fF and an off-chip shunt capacitance (C_x) of 150 fF will be added close to the IC pin.

In an attempt to characterize the losses due to the package and test PCB a calibration path was included on the chip for which two bond pads were directly connected. The loss through this path could be subtracted from the measured LNA S_{2I} and served to de-embed the LNA performance to an extent.

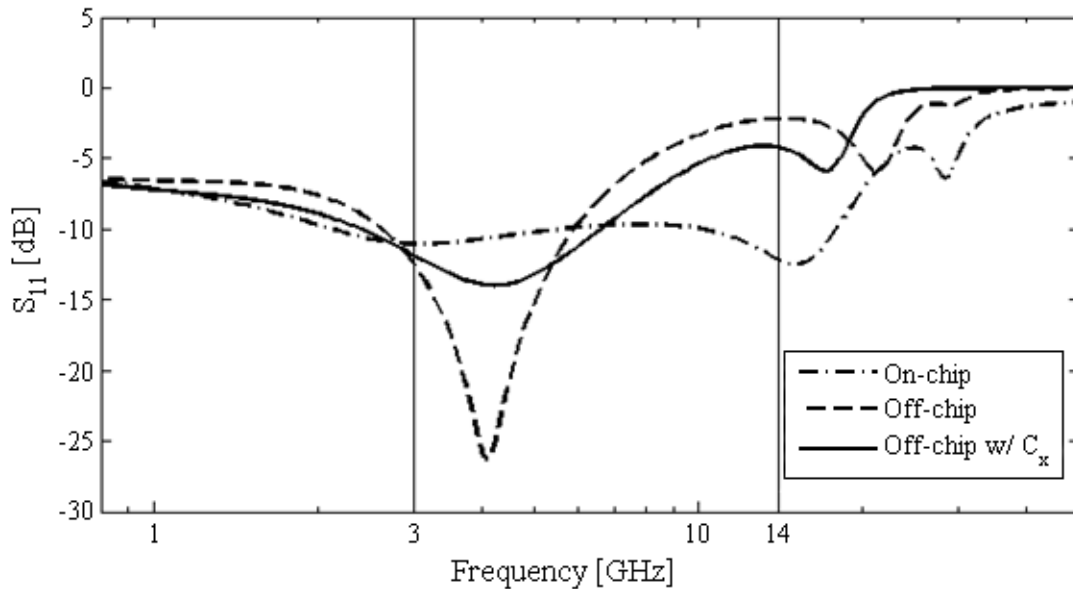


Figure 6.13. S_{1I} of the LNA with package parasitics with and without the off-chip shunt capacitor.

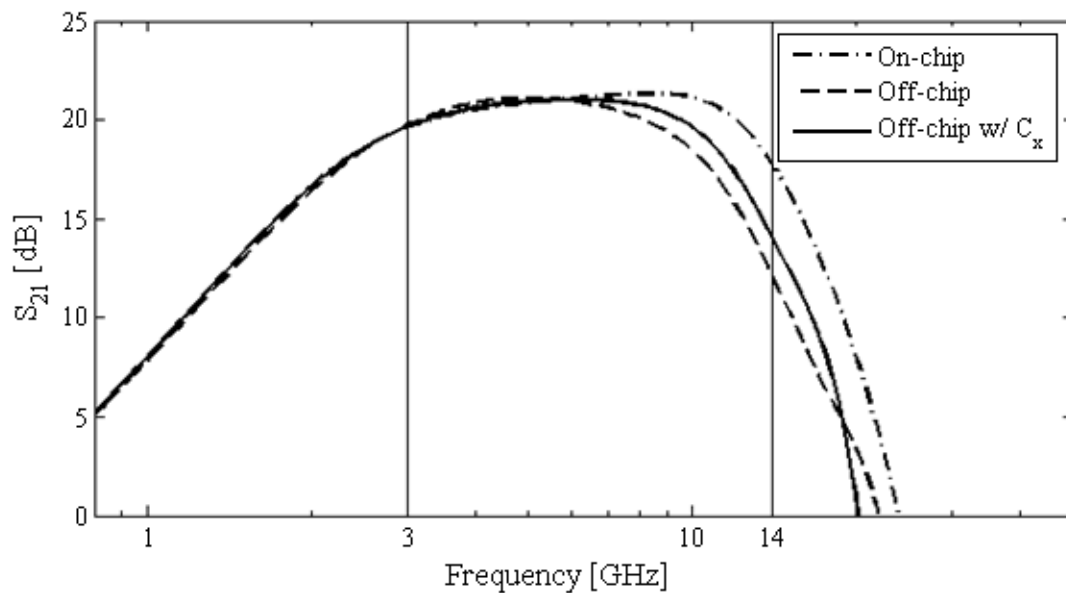


Figure 6.14. S_{2I} of the LNA with package parasitics with and without the off-chip shunt capacitor.

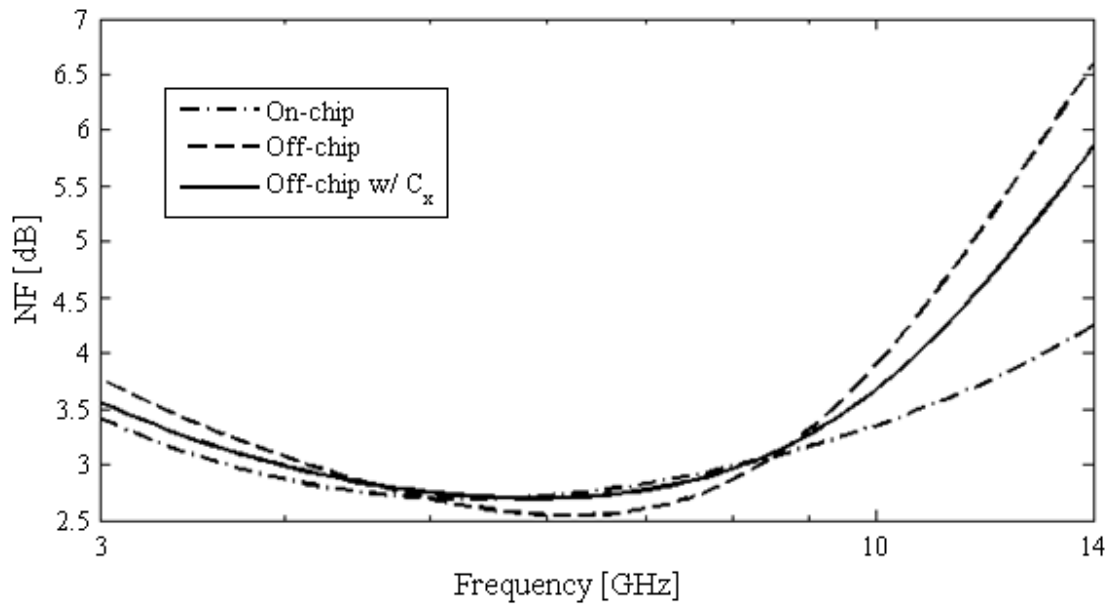


Figure 6.15. NF of the LNA with package parasitics with and without the off-chip shunt capacitor.

6.6 TEST PCB

As discussed in Section 6.4 on-wafer measurement equipment was not available and therefore the dies were packaged using QFN packages and soldered onto a PCB for testing purposes. This PCB consisted of biasing circuitry and also transmission lines from the IC to SMA connectors. Microstrip co-planar waveguides were used as signal interconnects.

The first amplifier stage requires current biasing and thus a resistor to the positive supply was used to set the collector current. The second and third stages use voltage biasing and were biased using the active voltage bias configuration seen in Figure 6.16. The potentiometers can be used to vary the collector current and set it to the desired value.

To facilitate setting the collector currents of the stages individually while using only two 1.8 V power supplies, one for the bias circuits and one for V_{CC} , jumpers were placed in series with the bias circuits. By removing two of the jumpers the biasing of any one of the three stage can be turned on individually and the total collector current flowing into V_{CC} measured with a multi-meter is the collector current of that particular stage.

The bias circuit in Figure 6.16 was duplicated and used for both LNAs, and subsections of it was used for the individual LNA stages as well. A photo of the final populated PCB is

presented in Figure 6.17, including the test circuitry for the two other projects on this chip. Rogers RO4003 material was used for the RF layers of the PCB.

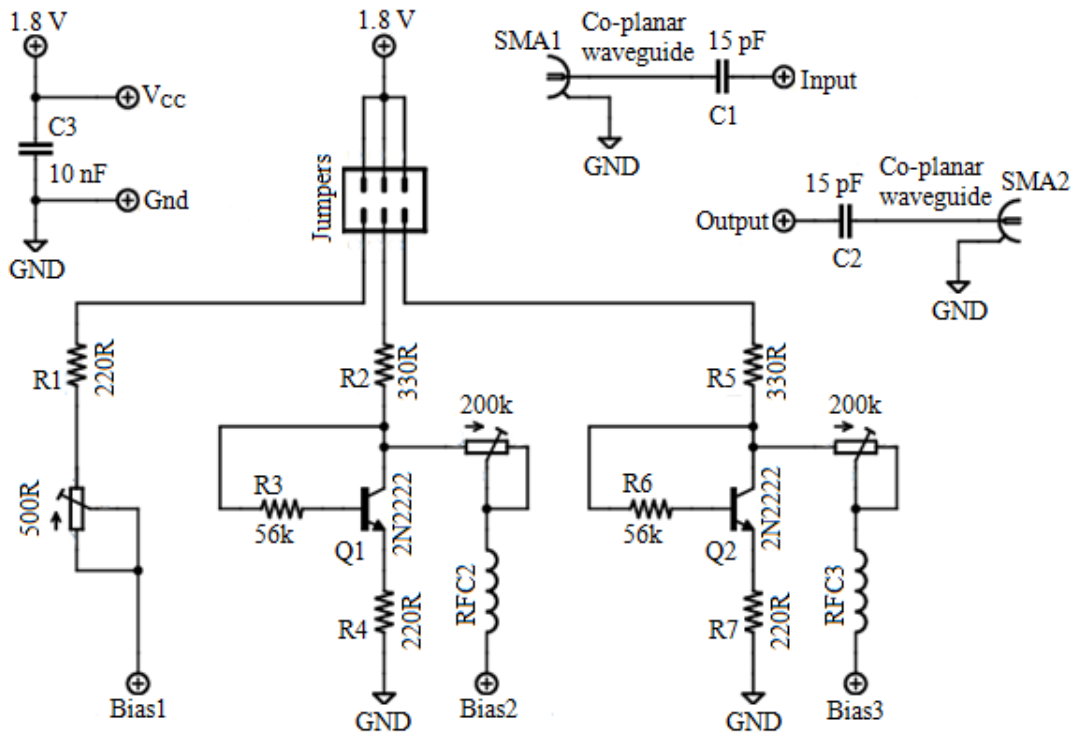


Figure 6.16. Schematic of the test PCB.

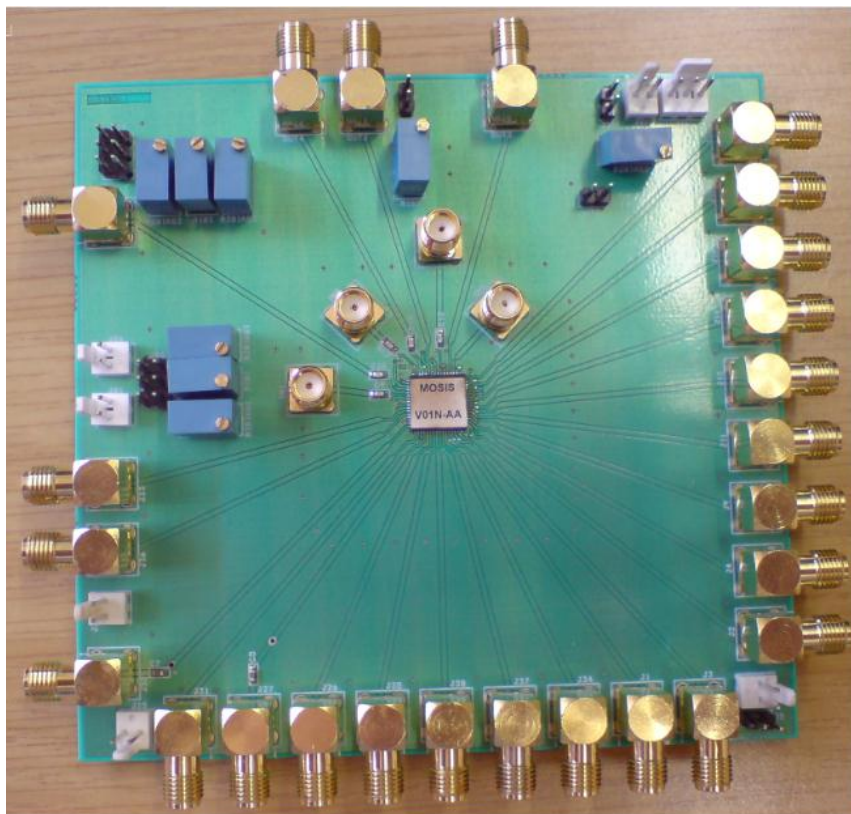


Figure 6.17. Photo of the test PCB.

6.7 SHORTCOMINGS OF THE TEST PCB

6.7.1 SMA connectors

Although many SMA connector datasheets specify a maximum frequency of at least 12 GHz for SMA connectors in general the right-angle connectors that were used on the PCB had a cut-off frequency of about 2 GHz. This is due to the through-hole pins of the connectors shown in Figure 6.18.

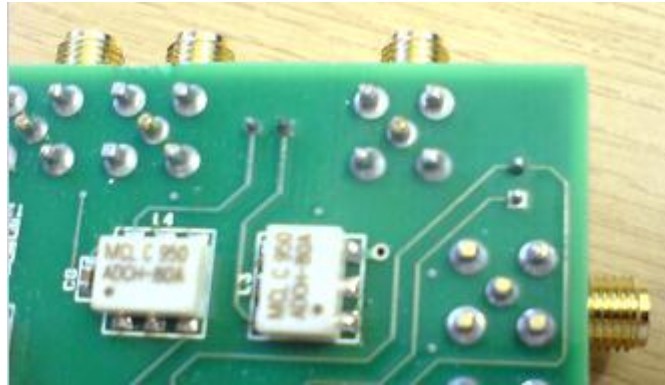


Figure 6.18. Through-hole pins of the PCB mounted SMA connectors

Since measurements up to at least 14 GHz were necessary the board had to be modified using coaxial cable and cable mounted SMA connectors with a cut-off frequency of about 18 GHz. The modifications are shown in Figure 6.19. Although this still resulted in significant signal loss measurement up to 6 GHz was feasible and allowed characterization of the LNAs up to this frequency.

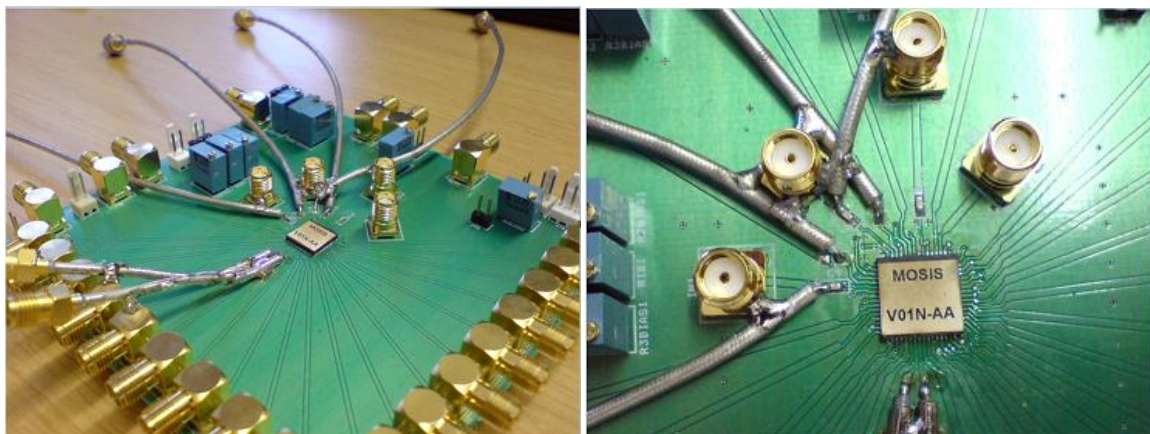


Figure 6.19. Modifications to the PCB to allow measurement above 2 GHz.

For high speed circuits with operating frequencies above 2 GHz the SMA connector of choice should be the Emerson SMA connector with part number 142-0761-841 which mounts onto the side of the PCB in line with the waveguide offering a true 18 GHz cut-off frequency. This type of connector is shown in Figure 6.20.



Figure 6.20. Emerson 142-0761-841 side mounting SMA connector.

6.7.2 On chip DC blocking capacitors

When the LNA circuit design was done the input DC blocking capacitor was kept off-chip to avoid affecting the input matching network where the bond pad capacitance was absorbed into C_1 . An on-chip DC blocking capacitor would need to be inserted in between this pad capacitance and the rest of the IMN.

In retrospect however the use of off-chip capacitors is far more detrimental to the circuit performance due to the package parasitics of these capacitors. Even with the use of C06CF150J range porcelain RF capacitors from Dielectric Laboratories, Inc. the performance was still degraded. Although these capacitors have an equivalent series resistance (ESR) of less than 1Ω they still have a self resonant frequency of only 3.2 GHz [70].

6.7.3 Layout recommendations for future testing

Although co-planar waveguides were correctly used as transmission lines a technique called RF-stitching should be incorporated as well on future test boards. This technique dictates that vias be placed at short regular intervals next to the waveguide to the ground plane below. This shortens the path along the ground plane from one side of the waveguide to the other.



Another problem with the layout is the extremely thin tracks connecting the ends of the transmission lines to the IC pins which can be seen clearly in Figure 6.11. These thin tracks act as inductors at high frequencies and attenuate the signal from about 5 GHz upwards with severe attenuation above 10 GHz. Based on cost considerations a single board for testing the circuits of all three projects on the chip was used. Had a dedicated PCB rather been designed for testing only the LNAs the space might have been less constrained allowing the transmission lines to end closer to the chip, and thicker and shorter tracks with lower inductance to be used for connecting them to the chip.

6.8 CONCLUSION

This chapter presented the layouts of the LNA circuits submitted for fabrication as well as the photographs of the fabricated circuits. The packaging options were also discussed and the limitations of the QFN package and its effect on performance above 10 GHz have been indicated.

The small-signal simulation results of the circuit including the package parasitics are the expected results of the experimental measurements and will be used for comparison. In order to compare the performance of the fabricated devices to the simulations a method of de-embedding the on-chip LNA performance has to be used. A calibration path has been included on the chip to this end which was used to characterize the loss due to the PCB and IC package.

The design and schematic of the test PCB with bias circuitry was discussed. The shortcomings of this PCB in terms of the signal interconnects were pointed out along with the lessons learnt.