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A SiGe BiCMOS LNA FOR mm-WAVE APPLICATIONS

by

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SUMMARY

A SiGe BiCMOS LNA FOR mm-WAVE APPLICATIONS

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Keywords: Low-noise amplifier (LNA), millimeter-wave (mm-wave), bipolar CMOS (BiCMOS), heterojunction bipolar transistor (HBT), silicon germanium (SiGe), cascode amplifier, impedance matching network (IMN), integrated circuit (IC), transmission line, coplanar waveguide (CPW), slow-wave CPW (S-CPW), electromagnetic (EM) analysis

A 5 GHz continuous unlicensed bandwidth is available at millimeter-wave (mm-wave) frequencies around 60 GHz and offers the prospect for multi gigabit wireless applications. The inherent atmospheric attenuation at 60 GHz due to oxygen absorption makes the frequency range ideal for short distance communication networks. For these mm-wave wireless networks, the low noise amplifier (LNA) is a critical subsystem determining the receiver performance i.e., the noise figure (NF) and receiver sensitivity. It however proves challenging to realise high performance mm-wave LNAs in a silicon (Si) complementary metal-oxide semiconductor (CMOS) technology. The mm-wave passive devices, specifically on-chip inductors, experience high propagation loss due to the conductivity of the Si substrate at mm-wave frequencies, degrading the performance of the LNA and subsequently the performance of the receiver architecture.

The research is aimed at realising a high performance mm-wave LNA in a Si BiCMOS technology. The focal points are firstly, the fundamental understanding of the various forms of losses passive inductors experience and the techniques to address these issues, and secondly, whether the performance of mm-wave passive inductors can be improved by means of geometry optimising. An associated hypothesis is formulated, where the research

outcome results in a preferred passive inductor and formulates an optimised passive inductor for mm-wave applications. The performance of the mm-wave inductor is evaluated using the quality factor (*Q*-factor) as a figure of merit. An increased inductor *Q*-factor translates to improved LNA input and output matching performance and contributes to the lowering of the LNA NF.

The passive inductors are designed and simulated in a 2.5D electromagnetic (EM) simulator. The electrical characteristics of the passive structures are exported to a SPICE netlist which is included in a circuit simulator to evaluate and investigate the LNA performance. Two LNAs are designed and prototyped using the 0.13 µm SiGe BiCMOS process from IBM as part of the experimental process to validate the hypothesis. One LNA implements the preferred inductor structures as a benchmark, while the second LNA, identical to the first, replaces one inductor with the optimised inductor. Experimental verification allows complete characterization of the passive inductors and the performance of the LNAs to prove the hypothesis.

According to the author's knowledge, the slow-wave coplanar waveguide (S-CPW) achieves a higher *Q*-factor than microstrip and coplanar waveguide (CPW) transmission lines at mm-wave frequencies implemented for the 130 nm SiGe BiCMOS technology node. In literature, specific S-CPW transmission line geometry parameters have previously been investigated, but this work optimises the signal-to-ground spacing of the S-CPW transmission lines without changing the characteristic impedance of the lines. Optimising the S-CPW transmission line for 60 GHz increases the *Q*-factor from 38 to 50 in simulation, a 32 % improvement, and from 8 to 10 in measurements. Furthermore, replacing only one inductor in the output matching network of the LNA with the higher *Q*-factor inductor, improves the input and output matching performance of the LNA, resulting in a 5 dB input and output reflection coefficient improvement. Although a 5 dB improvement in matching performance is obtained, the resultant noise and gain performance show no significant improvement. The single stage LNAs achieve a simulated gain and NF of 13 dB and 5.3 dB respectively, and dissipate 6 mW from the 1.5 V supply. The LNA focused to attain high gain and a low NF, trading off linearity and as a result obtained poor 1 dB compression of -21.7 dBm. The LNA results are not state of the art but are comparable to SiGe BiCMOS LNAs presented in literature, achieving similar gain, NF and power dissipation figures.

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OPSOMMING

'n SiGe BiCMOS LRV VIR mm-GOLF TOEPASSINGS

deur

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Sleutelwoorde: Laeruis-versterker (LRV), millimeter-golf (mm-golf), bipolêre CMOS (BiCMOS), Heterovoegvlak-bipolêre transistor (HBT), silikon germanium (SiGe), kaskade versterker, impedansie aanpasnetwerk, geïntegreerde stroombaan (IC), transmissie lyne, koplanar golfgeleier (CPW), stadige-golf CPW (S-CPW), elektromagnetiese (EM) analise

'n 5 GHz deurlopende ongelisensieerde bandwydte is beskikbaar by millimeter-golf (mm-golf) frekwensies rondom 60 GHz en bied die vooruitsig vir multi-gigabis draadlose toepassings. Die inherente atmosferiese attenuasie by 60 GHz te danke aan suurstof absorpsie maak die frekwensie reeks ideaal vir nabygeleë kort afstand kommunikasie netwerke. Wat deel vorm van hierdie mm-golf draadlose netwerke, is die laeruis-versterker (LRV) 'n kritiese substelsel wat die ontvanger se werksverrigting bepaal, dit wil sê, die ruis figuur (RF) en ontvanger sensitiwiteit. Dit is egter moeilik om hoë werksverrigting LRVs te realiseer in silikon (Si) aanvullende metaal-oksied halfgeleier (CMOS) tegnologie. Die mm-golf passiewe toestelle, spesifiek die induktore, ervaar hoë voortplantingsverliese as gevolg van die geleidingsvermoë van die Si substraat by mm-golf frekwensies, wat tot gevolg het dat die werksverrigting van die LRV en die ontvanger argitektuur versleg.

Die navorsing is daarop gemik om 'n hoë werksverrigting mm-golf LRV in 'n Si CMOS-tegnologie te realiseer. Die fokuspunte is eerstens om die basiese begrip van die verskillende vorme van verlies wat passiewe induktore ervaar, en die verskillende soorte tegnieke om hierdie kwessies aan te spreek, en tweedens, of die werksverrigting van mm-golf passiewe induktore verbeter kan word deur middle van geometriese optimisering. In

die lig van die vermelde hipotese, lewer die navorsing 'n voorkeur passiewe induktor en formuleer 'n optimal passiewe induktor vir mm-golf toepassings. Die werksverrigting van die mm-golf induktor word geëvalueer deur die kwaliteit faktor (Q-faktor) as 'n figuur van meriete. 'n Hoër induktor *Q*-faktor dra by tot verbeterde LRV inset en uitset aanpas werksverrigting en dra by tot die LRV RF.

Die passiewe induktore is ontwerp en gesimuleer in 'n 2.5D elektromagnetiese (EM) simulator. Die elektriese eienskappe van die passiewe strukture word in 'n SPICE netlys vertaal wat in 'n stroombaan simulator ingesluit word, om die werksverrigting van die LRV te evalueer en te ondersoek. Twee LRV's is ontwerp en prototypes is ontwikkel in die 0.13 µm SiGe BiCMOS proses van IBM as deel van die eksperimentele proses of die hipotese te bevestig. Een LRV implementeer die voorkeur induktore as 'n maatstaf, terwyl die tweede LRV, identies soos die eerste, 'n induktor vervang met die optimale induktor. Eksperimentele verifikasie voltooi die karakterisering van die passiewe induktore en die werksverrigting van die LRV's om die hipotese te bewys.

Volgens die skrywer se kennis, bereik die stadige-golf koplanar golfgeleier (S-CPW) 'n hoër *Q*-faktor as mikrogeleier en koplanar golfgeleier transmissielyne by mm-golf frekwensies in die 130 nm SiGe BiCMOS tegnologie node. Spesifieke S-CPW transmissielyn geometriese parameters is voorheen in die letterkunde ondersoek, maar hierdie werk optimaliseer die sein-tot-grond spasiëring van die S-CPW transmissielyne sonder om die karakteristieke impedansie van die lyne te verander. Optimaliseering van die S-CPW transmissielyne vir 60 GHz, verhoog die *Q*-faktor van 38 tot 50 in simulasie, wat 'n 32 % verbetering meebring, en 'n verhoging van 8 tot 10 in meet resultate. Verder, die vervanging van slegs een induktor in die uitset aanpasnetwerk van die LRV met die hoër *Q*-faktor induktor, verbeter die inset en uitset refleksie koëffisiënte van die LRV met 5 dB. Hoewel die 5 dB verbetering in die werksverrigting van die ooreenstemmende aanpasnetwerk behaal is, is daar geen betekenisvolle verbetering in die wins en ruis behaal nie. Die enkel stadium LRV bereik onderskeidelik 'n gesimuleerde wins en ruis figuur van 13 dB en 5.3 dB en benodig 6 mW van die 1.5 V toevoer. Die LRV fokus op hoë wins en lae ruis ten koste van lineariteit en bereik gevolglik 'n 1 dB kompressiepunt van -21.7 dBm. Die LRV resultate is nie besonders nie, maar is vergelykbaar met BiCMOS LNAs in die letterkunde, wat ook soortgelyke wins, ruis en drywingsaanvraag syfers bereik.

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LIST OF ABBREVIATIONS

AC	Alternating current
ADE	Analogue design environment
BEOL	Back-end-of-line
BiCMOS	Bipolar metal-oxide semiconductor
BJT	Bipolar junction transistor
CB	Common base
CBE	Collector-base-emitter
CBEBC	Collector-base-emitter-base-collector
CE	Common emitter
CMOS	Complementary metal-oxide semiconductor
CMP	Chemical mechanical polishing
CPW	Coplanar waveguide
DC	Direct current
DRC	Design rule check
DUT	Device under test
EDA	Electronic design automation
EM	Electromagnetic
GSG	Ground-signal-ground
HBT	Heterojunction bipolar transistor
IC	Integrated circuit
IMN	Impedance matching network
IP3	Third-order intercept point
ITRS	International technology roadmap for semiconductors
LNA	Low noise amplifier
LVS	Layout versus schematic
MDS	Minimum detectable signal
MEMS	Microelectromechanical system
MEP	MOSIS educational program
MIM	Metal-insulator-metal
MIS	Metal-insulator-semiconductor
mm-wave	Millimeter-wave
MMIC	Monolithic microwave integrated circuit
MOM	Method of moments

MOS	Metal-oxide semiconductor
MOSFET	MOS field-effect transistor
MOSIS	MOS implementation system
MPW	Multi-project wafer
MSG	Maximum stable gain
NDA	Non-disclosure agreement
NF	Noise figure
PA	Power amplifier
PDMA	Plastic deformation magnetic assembly
PSS	Periodic steady state
Q-factor	Quality factor
RF	Radio frequency
S-CPW	Slow-wave coplanar waveguide
SL	Strip length
SOC	System-on-a-chip
SOLT	Short-open-load-through
SS	Strip spacing
SNR	Signal-to-noise ratio
SPICE	Simulation program with integrated circuit emphasis
TEM	Transverse electromagnetic
VNA	Vector network analyzer
VCO	Voltage controlled oscillator
WLAN	Wireless local area networks
WPAN	Wireless personal area networks

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CHAPTER 1: INTRODUCTION

1.1 BACKGROUND TO THE RESEARCH

A typical wireless transceiver system consist of several building blocks, ranging from a power amplifier (PA), low noise amplifier (LNA), mixers, oscillators, passive components for matching networks, filters, data converters and digital complementary metal-oxide semiconductor (CMOS) for baseband processing [**1**]. Typically, these building blocks use distinct integrated circuit (IC) technologies to achieve acceptable system performance and must be combined to form the complete transceiver system. It is however advantageous to utilize a technology that potentially enables system-on-a-chip (SOC) integration to achieve a smaller form factor, reduced packaging complexity and ultimately lower total system cost [**2**].

Silicon-germanium (SiGe) technology is an enabler of this possibility as it integrates with standard silicon (Si) CMOS to produce a monolithic SiGe BiCMOS technology. The addition of strained SiGe alloys to the Si material is referred to as bandgap engineering and culminates in the SiGe heterojunction bipolar transistor (HBT) [**3**]. Not only do strained SiGe alloys improve the performance of Si transistors to be at least competitive with III-V devices, it maintains the high yield, cost and manufacturing advantages of conventional Si fabrication. Currently SiGe HBT devices achieve transition frequencies (f_T) in excess of 200 GHz and competitive noise performance due to their high current gain (β) and low base resistance (r_B). The higher performance obtained with the addition of strained SiGe epitaxy resulted in the SiGe HBT becoming a viable option for millimeter-wave (mm-wave) circuits which was once dominated by III-V technologies [**4**].

As a consequence several LNAs have been realised at mm-wave frequencies using SiGe technologies [**5**], [**6**], [**7**], [**8**], [**9**]. The realisation of SiGe LNAs at mm-wave frequencies are an essential step to accomplish full SOC integration, but are not without difficulties. Although the active devices do provide high performance, the transistors are operating much closer to their cutoff frequencies resulting in reduced gain and higher noise figure (NF). As a result of the lower gain, multistage topologies are required to reduce the NF contribution of the subsequent stages. Multistage LNAs require more power and consume a larger area, are less linear than single stage topologies and require extensive stability checks due to the high number of internal nodes. The lower transistor gain also translates to fewer margins for process and temperature variations and is more susceptible to voltage

fluctuations [**10**]. Furthermore, other performance metrics for mm-wave amplifier design include the f_T, maximum stable gain (MSG), maximum unilateral gain (U), output power (P_{out}) and minimum noise figure (NF_{min}). The NF_{min} is the most critical characteristic in the design of mm-wave LNAs and it therefore becomes imperative to design for this performance metric. With the eminent gain per transistor drop as the frequency of operation increases and technology determining the severity of this trend [**11**], it becomes more difficult to attain receiver NF specifications.

High performance transistors are not the only components required in mm-wave analogue design. Passive components are typically used in impedance matching networks, resonators, filters and bias circuits. Passive components have proved critical to determine the performance of LNAs, voltage controlled oscillators (VCOs), mixers and PAs. Since the resistivity of typical silicon substrates are in the range of 1 to 20 Ω-cm [**12**], passives placed directly on the substrate experience high loss diminishing overall circuit performance [**4**], [**13**], [**14**]. Consequently, on-chip inductors have deliberately moved from spiral inductor structures to transmission lines due to the proper defining of reference planes and improved confinement of electric fields [**15**]. Additionally, other difficulties include the small wavelength associated with mm-wave frequencies. Interconnects which are an appreciable size of the wavelength must be treated as transmission lines to accurately model its distributed effects. Transmission lines therefore, become important elements in the mm-wave regime as they are used as interconnects and to realise passive components [**10**]. Capacitors for the mm-wave range should however be realised as lumped elements to act as high frequency coupling or bypass capacitors. Shorted or shunted transmission line stubs can only be used in matching networks or resonating circuits. High frequency coupling and bypass capacitors are therefore characteristically implemented as metal-oxide-metal or metal-insulator-metal (MIM) capacitors. Substrate coupling and the large size of frequency coupling and bypass capacitors severely impacts the *Q*-factor and self-resonating frequency of these passive devices. Metal layer stacking together with finger width and length optimisation, multiple via connections for introducing via-to-via capacitance, and shielding structures are layout techniques typically implemented in mm-wave capacitors to achieve the required high frequency performance [**16**], [**17**].

1.2 RESEARCH PROBLEM AND HYPOTHESIS

Typically the back-end-of-line (BEOL) determines the setting for passive components. The BEOL consists of several metal layers characteristically denoted as global, intermediate and local metal layers. The intermediate and local metal layers typically consist of copper and the global metal layers of aluminium. In order to achieve a specific integration density a number of metal layers is typically available in the technology. Contrary to active device tendency where technology scaling improves performance, the influence of substrate and metal losses on the propagation constant becomes more severe. With technology scaling, the vertical shrink of the BEOL together with the decrease in metal and dielectric thickness and metal pitch are deteriorating the performance of passive devices; the root cause is the skin effect, proximity effect and induced substrate loss [**14**].

Together with the various metal types and thicknesses included in the BEOL for a given technology, the layout design rules are imposing restrictions on the design of passive components. Chemical mechanical polishing (CMP) is typically used to provide planar surfaces throughout BEOL processing. To meet CMP process requirements, a metal pattern density are required to provide surface planarity [**18**]. With lower metal density the insulator is typically curved inwards and the same occurs for wide metal lines. The lack of planarity can lead to problems at higher metal levels. The pattern density constraints have to be taken into account at the beginning of the passive component design. The maximum signal line width is controlled by design rule check (DRC) rules and limits the theoretical choices for metal widths. Additionally, the minimum signal line width must adhere to electromigration rules determined by the maximum current density requirement [**18**].

With the process limitations and design rule restrictions discussed it becomes difficult to realise high performance passive components on Si substrates. A great deal of emphasis has been placed on passive inductors and how to improve its performance. Various techniques exists ranging from different inductor geometries, dimensioning, placement, alterations to the substrate profile and shielding mechanisms. All of these techniques are discussed in this dissertation and the effect of each on the quality factor (*Q*-factor) is investigated.

The hypothesis is stated as follows:

> *If the Q-factor of mm-wave inductors realised in a Si technology can be enhanced by optimising the geometry of the inductor layout within the process environment and physical limitations, then the performance of a 60 GHz LNA can be improved.*

The following research questions are constructed from the hypothesis:

- How can high *Q*-factor mm-wave inductors in Si technology be realised?
- Is *Q*-factor characterisation over the chosen geometry parameter possible to allow optimisation of the mm-wave inductor?
- How is the LNA performance characteristics influenced when improving the *Q*-factor of inductors in the LNA design?

In order to validate the hypothesis, the preferred inductor structure is simulated in electromagnetic (EM) software to determine any performance improvement through optimisation. The optimised inductor structure is implemented in a LNA circuit design and simulated at schematic level. An integrated circuit (IC) is prototyped based on the LNA circuit schematic. The prototype is measured and the results are used to confirm the feasibility of the proposed design and hypothesis.

1.3 JUSTIFICATION FOR THE RESEARCH

A wide continuous unlicensed bandwidth is available at mm-wave frequencies around 60 GHz. Although the unlicensed bandwidth differs slightly at different locations, i.e. in the US (57 – 64 GHz) and in Europe and Japan (59 – 66 GHz), there is a 5 GHz overlapping bandwidth offering prospects for multi gigabit point-to-point links, wireless local area networks (WLAN), and wireless personal area networks (WPAN), vehicular radar, intercity communication networks, and mm-wave mobile networks. The interesting propagation characteristics near 60 GHz are a unique feature of this frequency spectrum. The inherent atmospheric attenuation, due to oxygen absorption makes this region ideal for short distance communication networks. As a result, these networks are more secure with lower inter-system interference [**19**], [**20**].

The mm-wave wireless networks must be realised using cost effective technologies specifically for the consumer market. The SiGe HBT and BiCMOS technologies are the most promising candidates to meet these requirements. However, the 60 GHz prospect exhibits several challenges [**11**] where in particular, some of the difficulties surrounding mm-wave LNAs has been discussed.

Passive devices are essential in mm-wave LNAs; it therefore becomes important to determine the characteristics of the waves that propagate on these devices [**21**]. The characteristics need to be quantified to enable effective modelling and consequently be included in the circuit design. Other aspects such as parasitic effects must additionally be incorporated to determine the coupling of adjacent components to obtain accurate practical performance. With transmission lines such a critical circuit component realised as interconnects and passive components, it provides the opportunity for much research and improvement.

1.4 METHODOLOGY

The methodology followed to validate the hypothesis consists of a thorough literature study on the various topics of passive inductors namely, the various loss mechanisms associated with passive inductors at mm-wave frequencies and the assorted techniques used to address these issues. In order to realise high performance LNAs, research is also conducted on the various noise contributions within SiGe HBTs. An understanding of the noise generation in SiGe HBTs allows the correct methodology and approach to be followed to design for this critical performance characteristic. In order to strengthen the hypothesis, a LNA is prototyped following the results from the literature study. Passive inductors are modelled using an EM software package to characterise its performance. Equivalent circuits for the passive inductors are modelled and incorporated in a circuit simulator. After schematic entry, the layout design of the LNA is sent for fabrication and prototyped and finally measured for its practical performance. On-chip measurements are used to validate the results. A complete description of the design methodology is provided in chapter 3.

1.5 OUTLINE OF THE DISSERTATION

The dissertation is outlined as follows:

- Chapter 1: Introduction

  This chapter serves as an introduction to the research problem where several difficulties regarding mm-wave circuit design is examined. The hypothesis and motivation for the research has been discussed with a brief introduction to the research methodology.

- Chapter 2: Literature review

  The chapter is divided into two distinct sections namely, noise analysis and mm-wave passive inductors. The chapter emphasises the individual importance of the two sections. The noise analysis show where the contributor of noise sources is in LNAs and how to reduce its effect. The passive inductor section discusses the loss mechanisms at mm-wave frequencies. An assessment of various mm-wave inductors is given with a comprehensive study of each. Various contributions are also placed in context to emphasise the theories relating to this research.

- Chapter 3: Methodology

  The chapter describes the research methodology used to develop a functional circuit as well as the experimental setup to validate the hypothesis. The chapter gives an overview of the software packages used in the modelling of the passive inductors and the schematic and layout design of the LNA. The measurement process and equipment used to evaluate the prototype is also discussed.

- Chapter 4: Inductor design

  The chapter discusses the modelling, simulation and optimisation of mm-wave inductors. The chapter is divided into three sections namely, parameter extraction for modelling, simulation and optimisation of the inductor geometry. The chapter concludes with the preferred and optimised mm-wave inductor geometry that will be implemented in the design of the LNA to validate the hypothesis.

- Chapter 5: Amplifier design and simulation

The mathematical design of the LNA is discussed in this chapter. The essential techniques to achieve optimal noise and power matching are employed together with appropriate transistor sizing and bias requirements. The optimised inductor geometry is implemented and realised in the LNA design. Simulation results are conducted as a theoretical assessment of the LNA performance.

- Chapter 6: Layout and fabrication

  The layout and fabrication of the inductors, LNA and printed-circuit board (PCB) is discussed in this chapter. Several layout concerns are also discussed including layout parasitic which may result in LNA instability. The chapter concludes with the layout of the PCB and discusses the wirebond connections providing on-chip biasing for the LNA. The wirebonds proved problematic due to the long wirebond lengths and the possibility of intruding during on-chip measurements.

- Chapter 7: Experimental results

  This chapter discusses the measurement results for the inductors and LNA. The experimental results for the inductors are de-embedded to remove the measurement parasitics and then compared to the simulation results presented in chapter 4. The inductor parameters are extracted to characterise the performance of the inductors to enable evaluation against the simulation results. The LNA is characterised at DC to determine the biasing operating conditions followed by the high frequency measurements. Several setbacks and problems attained during measurements are also discussed followed by a conclusion and interpretation of the experimental results.

- Chapter 8: Conclusion

  This chapter summarises the dissertation and provides critical evaluation of the hypothesis and findings from the mathematical, simulation and measurement results. The chapter also discusses the limitations and assumptions made during this dissertation and further elaborates on future areas of research that resulted from this work.

1.6 DELIMITATIONS OF THE SCOPE OF THE RESEARCH

The scope of the research is limited to passive inductor components specifically for 60 GHz LNAs. A significant number of geometry parameters exist in order to optimise the preferred mm-wave inductor. Much of these geometry parameters are chosen with sound engineering deduction while others are defined by process parameters. The chosen parameters and optimised variable are justified in chapter 4. The end result is an inductor providing the lowest ohmic and substrate losses for the chosen geometry parameters within the specified process parameters, effectively obtaining the highest *Q*-factors.

The LNA is specifically designed to validate the hypothesis. Even though LNA design is compounded by a multi-dimensional optimisation intricacy, the LNAs realised in this work is designed to achieve maximum gain and minimum NF. The linearity trade-off is particularly severe in order to achieve high gain and low NF. Additionally, only a single stage LNA is designed in order to critically evaluate the influence of the inductor on the amplifier performance.

1.7 CONCLUSION

This chapter provided a preface to the dissertation. An introduction to the research problem and hypothesis was provided and justified. A brief methodology is given to show the process involved to prove the hypothesis. The dissertation is outlined and the limitations of the research are provided.

CHAPTER 2: LITERATURE REVIEW

2.1 INTRODUCTION

Passive inductors are critical circuit components and often limit the performance of mm-wave LNAs. Inductors utilised in mm-wave LNAs serve multiple purposes such as achieving noise and power matching in input matching networks, increase the amplifier linearity by means of transistor degeneration, and increase the frequency response by resonating with the parasitic capacitance at a particular node. Another important property is that inductors can be used to bias active devices since they simultaneously provide a low impedance path to DC but a finite AC impedance. However, passive inductors have various forms of losses increasing the total noise contribution in LNAs [**22**]. It is therefore important to find techniques to increase and realise higher performance passive inductors.

The first part of this chapter focuses on the noise analysis of LNAs. This critical parameter is crucial in reaching high performance receiver architectures as it determines the minimum detectable signal (MDS) of the receiver architecture [**23**]. The second part of this chapter discusses the various loss mechanisms accompanying mm-wave passive inductors. Several inductor configurations will be discussed which was also previously used in radio frequency (RF) designs, together with inductors specifically modified for the mm-wave regime. Subsequently several shielding techniques will also be discussed as well as their trade-offs to inductor performance characteristics.

2.2 NOISE ANALYSIS

The LNA has various critical aspects to take into account for instance power gain, noise analysis, frequency response, stability, linearity, distortion, dynamic range, variation to temperature, process and voltage fluctuations, and power dissipation. While all these aspects are important to realise high performance LNAs, this literature study will only focus on the noise characteristic and specifically at mm-wave frequencies. Other aspects such as LNA configurations and matching networks are also discussed since they determine the noise performance boundaries.

2.2.1 Noise in integrated circuits

Analogue signal ICs are corrupted by two different types of noise: electronic noise and “environmental” noise. The former refers to types of noise generated by the passive and

active components in the circuit. The latter refers to random disturbances the circuit experiences through supply or ground lines or through the substrate.

There are five types of noise defined as electronic noise; these are: Thermal or Johnson noise, Flicker or *1/f* noise, shot noise, burst noise and avalanche noise [**24**]. These five types of noise are discussed in the following section.

Thermal noise is due to random motion of electrons in a conductor and introduces fluctuations in the voltage measured across the conductor. Thermal noise of a resistor can be modelled as a series voltage source with a thermal noise voltage given by

$$\overline{v_n^2} = 4kTR\Delta f, \tag{2.1}$$

where k is Boltzmann's constant (1.38×10^{-03} J/K), T is absolute temperature in K and Δf is the bandwidth determined by the circuit. It is evident that the spectrum of thermal noise is white. In reality the spectrum drops at higher frequencies of approximately 100 THz, but for all practical purposes and the frequency band of interest, the white spectrum is accurate [**24**].

Flicker noise exists due to the trap-and-release phenomenon introduced by the "dangling" bonds that appear at the interface between the gate-oxide and silicon substrate in a MOSFET. Some charge carriers are randomly trapped and later released, introducing "flicker" noise in the drain current. Flicker noise can be modelled by a voltage source in series with the gate of the transistor and is roughly given by

$$\overline{v_n^2} = \frac{K_f}{C_{ox}WL}\frac{1}{f}, \tag{2.2}$$

where K_f is a process dependent constant. This constant can only be determined through measurements. The value of the constant can vary widely for different transistors or integrated circuits and is due to the dependency of flicker noise on crystal imperfections and contaminations that can vary randomly even on the same silicon wafer [**24**]. The noise contribution of flicker noise decays with increasing frequency, and while it can be neglected in most frequency operations, it may be eminent in voltage controlled oscillators, contributing to phase noise.

Burst noise is another type of low frequency noise. It has been shown to be related to the presence of heavy-metal ion contamination, i.e. found in gold-doped devices. The spectral density of burst noise is of the form

$$\overline{i^2} = K_2 \frac{I^c}{1+\left(\frac{f}{f_c}\right)^2} \Delta f, \tag{2.3}$$

where K_2 and c are constants for the particular device, where c ranges between 0.5 and 2. As with flicker noise, the constant K_2 varies considerably and must be determined through measurements. Equation (2.3) shows that the noise spectrum falls rapidly at high frequencies at a rate of $1/f^2$.

Shot noise is generated by a direct current flowing through a p-n junction and is always present in diodes, MOS transistors, and bipolar transistors. The current which appears to be a steady current is in fact composed of a large number of random independent current pulses. These fluctuations are given as

$$\overline{i^2} = 2qI\Delta f, \tag{2.4}$$

where q is the electronic charge. As in the case of thermal noise, shot noise exhibit a flat current spectral density. The shot noise spectral density is shown Figure 2.1 and is often called white noise.

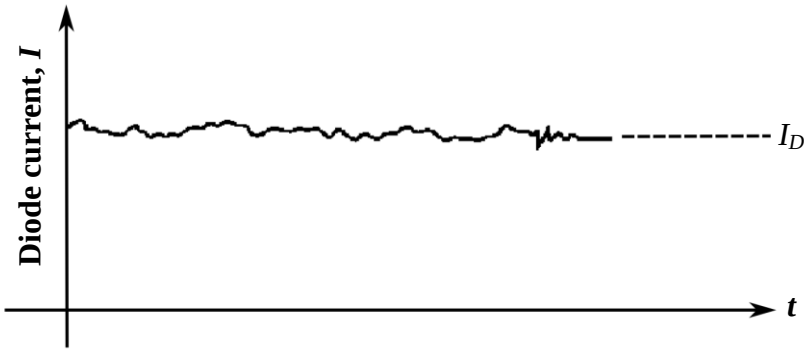

Figure 2.1. Shot noise spectral density [**24**] (© [2001] IEEE).

Avalanche noise occurs in a reverse biased p-n junction where holes and electrons in the depletion region, acquire sufficient energy to create electron-hole pairs by colliding with silicon atoms. This form of noise spikes is typically larger than all other noise sources when present and is due to a single carrier which can start an avalanche process producing a current burst containing many carriers moving together.

The various types of noise sources within ICs can be simplified by only considering thermal and shot noise. This is due to their high frequency noise spectrums and the low voltage application of the LNA.

2.2.2 Noise figure and noise parameters

In a transistor amplifier the signal and the noise at the input is amplified by the gain of the amplifier. Furthermore, noise generated inside the transistor propagates to the output, producing additional noise which degrades the signal-to-noise ratio (SNR) at the output. The NF of an amplifier is defined as the SNR at the input divided by the SNR at the output. Additionally, the noise generated by the transistor is a function of the source termination. With the source termination admittance, Y_s given by $Y_s = G_s + jB_s$, the NF is given by

$$NF = NF_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{s,opt}\right|^2, \tag{2.5}$$

where NF_{min} is the minimum noise figure, R_n is the noise resistance (Ω) and G_s is the real part of Y_s (Ω^{-1}). Together these are referred to as the noise parameters of a two-port network. A noise match is defined when Y_s is equal to the optimum source admittance, $Y_{s,opt}$. Any difference between Y_s and $Y_{s,opt}$ is then multiplied by R_n and then contributes to NF_{min}. R_n therefore determines the sensitivity of the NF to a source impedance mismatch [**25**], [**26**].

2.2.3 Noise in HBT amplifiers

The primary high frequency noise sources in HBTs are the base current shot noise $2qI_B$, the collector shot noise $2qI_C$ and the thermal noise generated by the base resistance $4KTr_B$ [**27**]. This is illustrated in Figure 2.2.

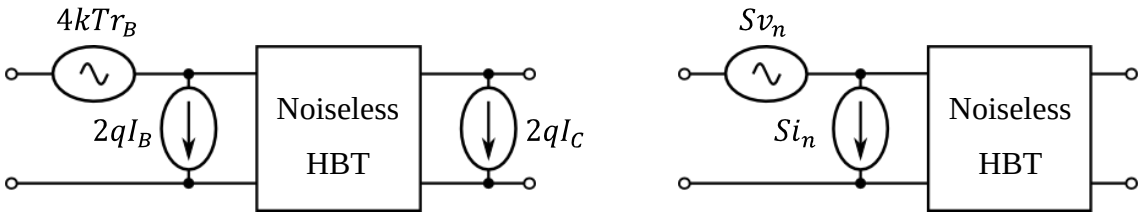

Figure 2.2. Two-port model of an HBT transistor amplifier. Figure (a) shows the primary noise sources while (b) shows the conversion to their spectral density equivalent.

Figure 2.2 shows the two-port model conversion of the primary noise sources of the HBT from the input and output to their spectral density equivalent. In high frequency HBT models, the base resistance consists of two components: the intrinsic base resistance r_{bi} which is a fictitious equivalent resistance used to model the two-dimensional current flow within the base, and the physical extrinsic base resistance r_{bx}. Typically these two

components can be lumped together as a single term r_B without introducing significant errors. Other noise sources within the transistor such as the collector series resistor r_C and the emitter series resistor r_E can usually be neglected from the noise model due to their negligible effects on the transistor noise performance.

The base current in a transistor produces shot noise due to majority carrier injection from the base to the emitter. The collector current shot noise component is generated due to the majority carriers in the emitter crossing the emitter-base junction, which drifts across the base region and is then accelerated by the electric field across the collector-base depletion region to form the collector current [**24**]. Due to the emitter-base junction being the origin of the collector and base shot noise components, a correlation between the components exists. This correlation plays a significant role in the noise performance of HBTs at high frequencies [**27**]. The spectral densities of the input noise current, input noise voltage and their cross-correlation, which is denoted as S_{i_n}, S_{v_n} and $S_{i_n v_n^*}$, respectively can be expressed in terms of device parameters as

$$S_{i_n} = 2qI_C\left[\frac{1}{\beta} + \left(\frac{\omega(C_{be}+C_{bc})}{g_m}\right)^2\right], \tag{2.6}$$

$$S_{v_n} = 4KT\left(r_B + \frac{1}{2g_m}\right), \tag{2.7}$$

$$S_{i_n v_n^*} = 2KT\left(\frac{1}{\beta} + \frac{j\omega(C_{be}+C_{bc})}{g_m}\right), \tag{2.8}$$

where β, g_m, C_{be} and C_{bc} are the current gain, transconductance, base-emitter and base-collector capacitance of the transistor, respectively. The noise spectral densities of (2.6) to (2.8) can then be used to find the noise parameters R_n, $Y_{s,opt}$ and NF_{min} where

$$Y_{s,opt} = G_{s,opt} + jB_{s,opt}, \tag{2.9}$$

$$R_n = r_B + \frac{1}{2g_m}, \tag{2.10}$$

$$G_{s,opt} = \sqrt{\frac{g_m}{2R_n}\frac{1}{\beta} + \frac{(\omega C_i)^2}{2g_m R_n}\left(1 - \frac{1}{2g_m R_n}\right)}, \tag{2.11}$$

$$B_{s,opt} = -\frac{\omega C_i}{2g_m R_n}. \tag{2.12}$$

The NF_{min} can then be equated

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{\frac{2g_m r_B + 1}{\beta} + \frac{2\left(r_B + \frac{1}{2g_m}\right)(\omega C_i)^2}{g_m}} \times \sqrt{\left(1 - \frac{1}{2g_m r_B + 1}\right)}. \tag{2.13}$$

It is clear from (2.13) that a higher β, higher f_T and lower r_B is desired to reduce NF_{min}. Also, as the imaginary part of the optimum source admittance $B_{s,opt}$ in (2.12) is negative, a series inductor is required for noise matching of the imaginary part of the source. In typical applications where $g_m r_B \gg 1/2$, (2.13) can be further simplified to

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m r_B}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2}. \quad (2.14)$$

According to (2.14), NF_{min} is divided into two distinct regions. At frequencies less than $f_T/\sqrt{\beta}$, the NF_{min} is independent of frequency and has a white noise spectrum. In this region a large β and a small r_B are key to achieving good noise performance. With frequencies above $f_T/\sqrt{\beta}$, the NF_{min} rises linearly with frequency with slope proportional to $\sqrt{r_B}/f_T$. At the same time, the impact of β on the NF_{min} becomes less significant, therefore requiring f_T and r_B scaling to reduce NF_{min}. An illustration of the two NF_{min} regions as a function of frequency is shown Figure 2.3.

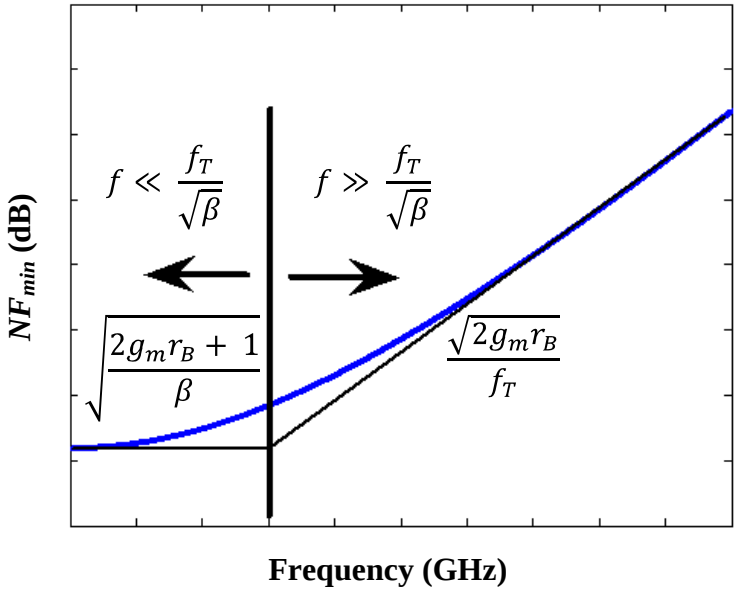

Figure 2.3. The two distinct regions of NF_{min} as a function of frequency.

From the following derivation it is evident that SiGe HBTs have superior noise compared to the Si BJT due to its ability to simultaneously achieve high cut-off frequency f_T, a low base resistance r_B, and a high current gain β [**28**].

2.2.4 Input noise matching

Noise matching becomes an essential performance requirement for LNAs. Unfortunately noise matching for optimum source admittance in general differs from the optimum source admittance for gain matching [**29**]. Equation (2.5) shows that in the ideal case where R_n is equal to zero, a minimum NF is achieved irrespective of the source admittance. Therefore a simultaneous noise and gain match can be achieved. In practical cases however, R_n can never be zero but should be minimized to desensitise any variations in the source admittance. A minimum NF can therefore only be achieved when $Y_s = Y_{s,opt}$. Under these

optimal noise matching conditions, the maximum available gain can be calculated in terms of the transistor parameter as

$$G_a = \frac{1}{(2\pi f)^2 C_{bc} C_i r_B} \sqrt{\frac{g_m r_B + 1/2}{2} \frac{g_m^2}{\beta} + \frac{g_m r_B (\omega C_i)^2}{2}}, \quad (2.15)$$

where $C_i = C_{be} + C_{bc}$, C_{bc} is the base-collector and C_{be} is the emitter-base capacitance of the transistor [**25**]. The maximum available gain is illustrated in Figure 2.4 and a number of important observations can be made from (2.15).

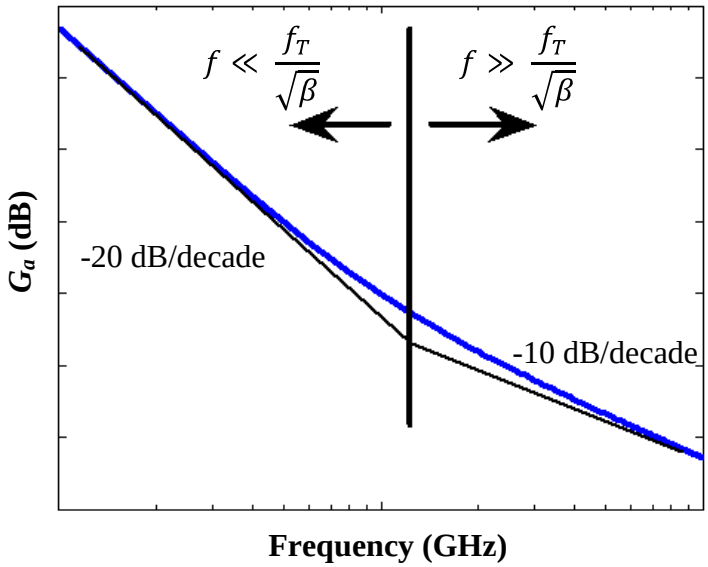

Figure 2.4. The two distinct regions of G_a as a function of frequency.

At low frequencies where the first term in the square root dominates, a higher β decreases G_a. This emphasizes the trade-off between low noise design and a large power gain at frequencies less $f_T/\sqrt{\beta}$. The two terms inside the square root is equal at $f = f_T/\sqrt{\beta}$. At frequencies less than $f_T/\sqrt{\beta}$, G_a decreases with a frequency dependency of $1/\omega^2$ (-20 dB/decade) while G_a decreases with a frequency dependency of $1/\omega$ (-10 dB/decade) at frequencies higher than $f_T/\sqrt{\beta}$. As was the case for NF_{min}, the effect of β becomes less significant at higher frequencies due to the dominant second term inside the square root. Although C_{bc} does not influence NF_{min} directly as shown in (2.14), it should be minimized to maximize G_a.

2.3 AMPLIFIER CONFIGURATIONS

The most frequent LNA configurations employed at mm-wave frequencies is shown in Figure 2.5. The familiar cascode shown in Figure 2.5(a) consists of a common-emitter (CE) stage (Q_1), connected to a common-base (CB) stage (Q_2). Advantages include an

increase in voltage gain by a factor of approximately $g_m r_o$ compared to a CE amplifier, and the suppression of the Miller-effect which leads to an increase in bandwidth. The cascode configuration operating at frequencies well below the f_T of the transistors provide good reverse isolation, input matching, and a low NF. Ideally the NF of the cascode configuration is determined by the CE stage since the CB provides unity current gain, but practically the CB stage will increase the NF as opposed to a single CE amplifier [**30**]. Additionally, the pole situated between Q_1 and Q_2 shunts a considerable portion of the AC to ground, thereby reducing the gain and increases the noise generated by the CB transistor [**31**]. These observations suggest that the preferred solution is a CB-stage shown in Figure 2.5(b), before voltage amplification occurs.

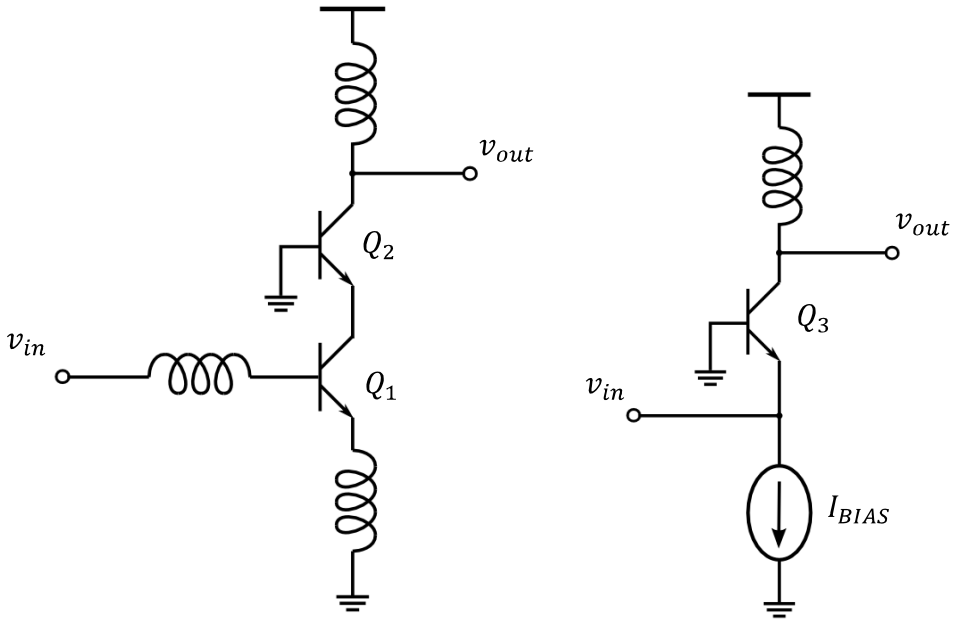

Figure 2.5. Two popular LNA configuration used in mm-wave frequencies. Figure 2.5(a) shows the cascode and Figure 2.5(b) shows the CB configuration.

A similar approach was followed by [**32**] with the same observation that a CB configuration provides improved receiver performance. It has also been suggested that a resonating circuit be placed between the two transistors, Q_1 and Q_2 of the cascode configuration to resonate with the total parasitic capacitance at that node [**10**], [**33**]. A series inductor accomplishes this and therefore improves the NF of the cascode configuration without this modification.

2.4 MATCHING NETWORKS

As the LNA is the first block of the receiver, it plays a crucial role in amplifying the received signal while adding as little noise to the signal as possible. Matching networks situated between the LNA and the antenna is just as important as it plays a major role in the receiver performance. In addition, a power match is also required to prevent the incoming signal from reflecting between the antenna and the LNA.

The most popular matching technique is known as inductor degeneration [**13**], [**34**]. The matching topology is shown in Figure 2.6. The degeneration inductance L_E results in an equivalent input resistance given by

$$R_i = \omega_T L_E, \tag{2.16}$$

where ω_T is the unity gain frequency of the transistor [**35**], [**36**].

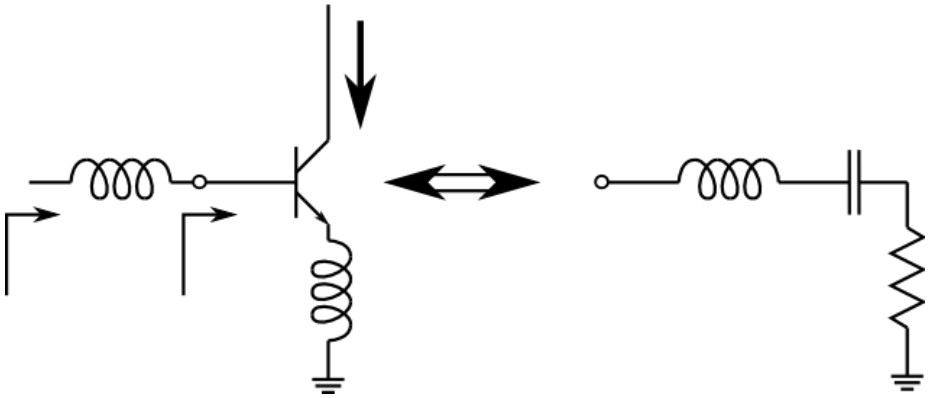

Figure 2.6. Equivalent circuit for an inductive degenerated transistor [**35**] (© [2004] IEEE).

A second inductor is placed in series with the transistor to cancel the imaginary part of the transistor's input impedance. The equivalent high frequency circuit is also shown in Figure 2.6. This technique only provides matching within a narrow bandwidth, due to the passive components which only provide a real resistance in a narrow range of frequencies. The 5 GHz overlapping bandwidth discussed in section 1.3 allocated around 60 GHz ensures an upper corner to lower corner frequency ratio of approximately equal to one. The bandwidth allocation for 60 GHz is therefore considered narrowband and this matching network is sufficient for the frequency range of interest.

2.5 INDUCTOR LOSS MECHANISMS

The *Q*-factor of integrated passive devices is strongly dependent on the material properties with which it is manufactured. The semiconductor substrate and metal layers used to build the device plays an important role.

2.5.1 Metal losses

The resistive component in metal interconnects exists because of the imperfect conductor characteristics. These resistive losses can typically be broken down in two components: DC and high frequency losses. The DC losses primarily depend on the resistivity and the cross-sectional area of the conductor given by ρ/A where ρ and A denotes the resistivity and the cross-sectional area of the conductor, respectively. The general DC resistance equation is measured in Ω/m and the current flow is uniformly distributed across the conductor cross sectional area. The more profound form of loss is the frequency dependent resistive loss. In this case, the high frequency current in a conductor is not uniformly distributed throughout the cross-sectional area of the conductor. Magnetic fields within the conductor changes the current distribution to flow in the outer rim underneath the surface of the conductor. This increases the resistance and is known as the skin effect. The thickness of the conduction band is called the skin depth. The skin effect is an inductive mechanism related to the rate of change of magnetic fields and therefore becomes more prominent at higher frequencies.

The presence of a changing magnetic field on a conducting material induces circulating eddy currents within the material. The eddy currents circulate around the incoming magnetic field lines. The circulating eddy currents merge continuously together, forming a counter-clockwise circulation of current around the perimeter of the conductor. This effect is illustrated in Figure 2.7. The figure shows how the eddy currents flow in the same general direction of current flow at the perimeter of the conductor, but opposes the current flow at the centre of the conductor, which gives rise to the skin effect.

The frequency dependent resistance can be approximated by extending the general DC resistance equation. With the current flow restricted to a smaller area around the conductor, the effective resistance is given by

$$R_{ac\ signal} \approx \frac{\rho}{p\delta}, \tag{2.17}$$

where ρ is the resistivity of the material, p is the perimeter of the conductor and δ is the skin depth. The effective resistance can be rewritten in the form

$$R_{ac\ signal} \approx \frac{\sqrt{\omega\mu}}{p\sqrt{2\sigma}} = \frac{\sqrt{\rho\pi\mu f}}{p}, \tag{2.18}$$

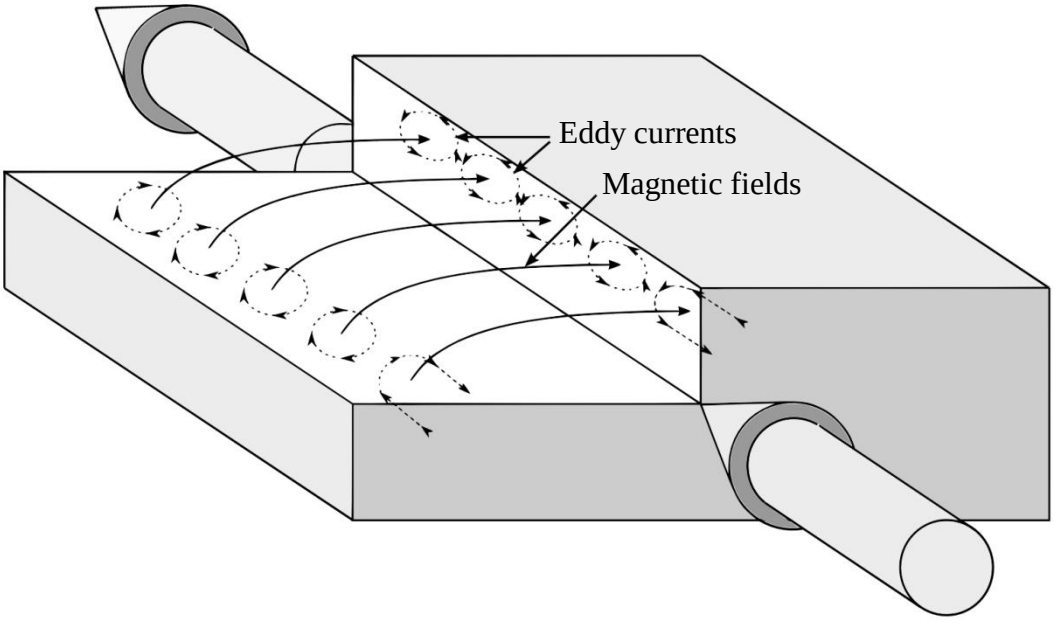

Figure 2.7. Cutaway of a conductor illustrating the internal magnetic fields and generated eddy currents.

where μ is the magnetic permeability of the conductor. With

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}. \tag{2.19}$$

where σ is the reciprocal of ρ, it is therefore apparent that the resistance increases proportional to the square root of frequency and is inversely proportional to the depth of current flow. The skin effect resistance is only one part of the frequency dependent resistance. The portion of the resistance not included is the resistance of the return current on the ground plane (reference plane). Unlike low frequency designs where the return current follows the path of least resistance, the return current in high frequency designs follow the path of least inductance. Therefore, the return current will flow underneath the signal line with the highest amount of current concentration directly beneath the conductor. The current density distribution for the current in the ground plane can be approximated by

$$I(D) = \frac{I_O}{\pi H}\frac{1}{1+(D/H)^2}, \tag{2.20}$$

where I_O is the total signal current, D is the distance from the trace and H is the height above the ground plane. The current density distribution is illustrated in Figure 2.8.

W

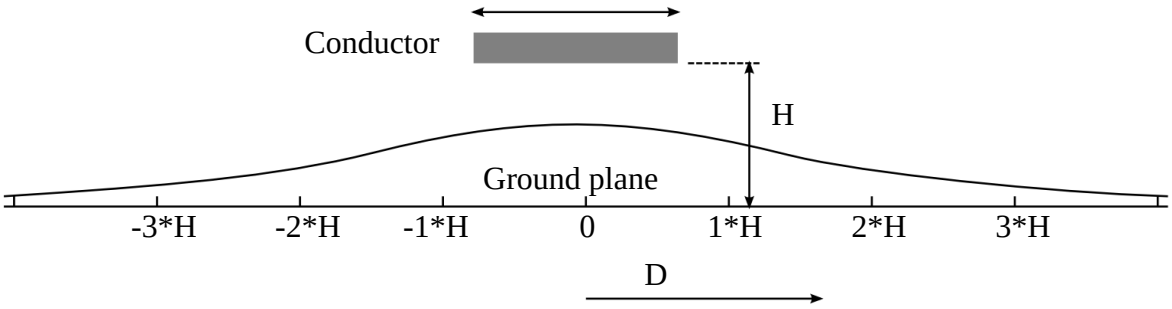

Figure 2.8. The distribution of the high frequency return current on a ground plane [**37**] (© [2000] IEEE).

In [**37**] it is shown that approximately 80 % of the return current is confined to flow in an area approximated by $\delta + 6H$ below the signal trace. The ac ground resistance is then given by

$$R_{ac\ ground} \approx \frac{\sqrt{\rho\pi\mu f}}{6H}. \tag{2.21}$$

The total frequency dependent resistance of a conductor and ground plane can be approximated by $R_{ac\ signal} + R_{ac\ ground}$ given by

$$R_{ac\ conductor} = \frac{\sqrt{\rho\pi\mu f}}{W} + \frac{\sqrt{\rho\pi\mu f}}{6H}. \tag{2.22}$$

Equation (2.22) is a first order approximation of the ac resistance of a conductor and does not account for the surface roughness that also contributes to the effective resistance of the line.

The proximity effect redistributes the current around the perimeter of the conductor in a slight non-uniform way. This also increases the apparent resistance of the conductors above what is expected from the skin effect alone. The proximity effect stands apart from Ampére's force law where adjacent wires carrying opposite DC will repel each other. Ampére's law pushes the structures apart while the proximity effect redistributes the small signal current density around the perimeters of the two wires. The proximity effect exerts no net mechanical force on the two wires.

The proximity effect is an inductive mechanism caused by changing magnetic fields and ignores steady currents generating static magnetic fields. The magnetic fields of the first wire induce eddy currents on the second wire, redistributing the current on the surface of the second wire. The current flowing in the second conductor is still bound to the shallow band underneath the surface by the internal skin effect, but the proximity effect redistributes the current around the perimeter of the second wire. The magnetic fields

penetrating the second conductor induces circulating eddy currents which concentrates more current to the inside-facing surface of the conductor and less at the outside. The proximity effect is illustrated in Figure 2.9.

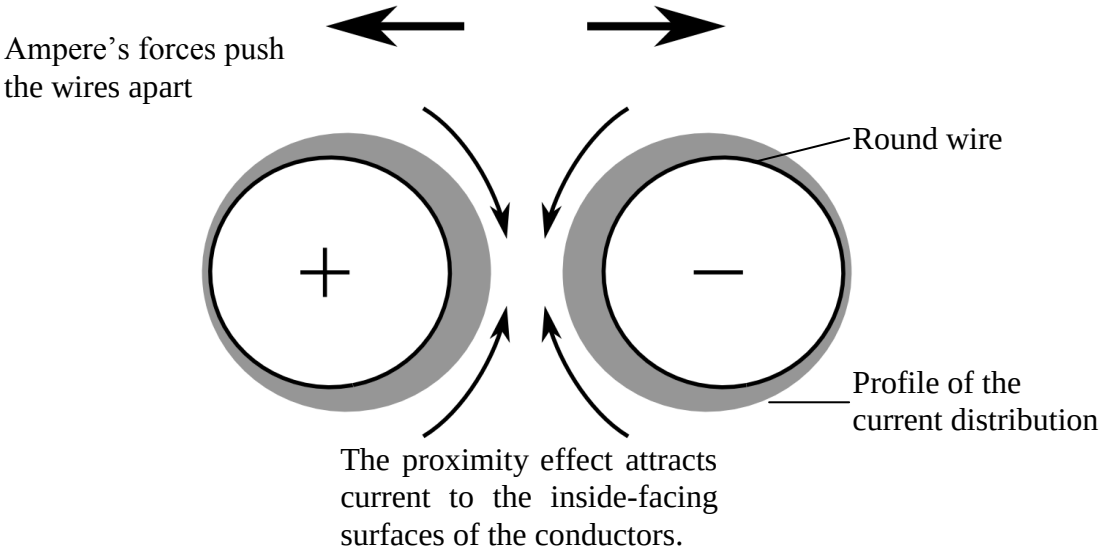

Figure 2.9. An illustration of the current redistribution due to the proximity effect [**38**] (© [2003] IEEE).

The skin effect and the proximity effect are two manifestations of the same principle. The skin effect is due to magnetic fields generated by a current flowing within the conductor while the proximity effect is due to magnetic fields generated by a current flowing in a neighboring conductor.

2.5.2 Substrate losses

The substrate is a major source of loss and is a direct consequence of the conducting nature of Si (as opposed to the insulating nature of GaAs). The resistivity of Si substrates typically varies from 10 kΩ-cm for lightly doped Si to 1 mΩ-cm for heavily doped Si. This is in comparison to GaAs substrates with resistivities in the order of 10^7 Ω-cm.

The conductive nature of the Si substrate leads to various forms of loss, converting electromagnetic energy to heat in the volume of the substrate. The various forms of substrate loss can be delineated to three separate mechanisms [**14**]. If a voltage difference exists between the conductors and the substrate, electric fields will consequently couple to the substrate and generate displacements currents that flow to nearby grounds either at the surface of the substrate or at the backplane. This form of loss is commonly referred to as

capacitive substrate loss. The second form of loss is time varying magnetic fields penetrating the substrate which induces currents to flow in the substrate. The direction of currents flowing in the substrate is opposite to the current flowing in the conductors. Since this form of loss is associated with magnetic fields, it is commonly referred to as inductive substrate loss. The third form of loss is radiation, which are electromagnetically induced losses which occur when the physical dimensions of the device approaches the wavelength at the frequency of propagation in the medium.

2.6 *Q*-ENHANCEMENT TECHNIQUES

With the various forms of loss mechanisms associated with on-chip inductors, several *Q*-enhancement techniques have been used to improve the inductor *Q*-factor. The first of these enhancement techniques optimizes the trace layout of the inductor. In [**39**], it is proposed that the inner turns of a spiral inductor be narrower than the outer turns. This reduces magnetically induced losses which are more concentrated at the inner turns. Unfortunately, inductors with variable line lengths on a conducting Si substrate, shows no substantial improvement in *Q*-factor due to the excessive capacitive losses of the substrate, [**40**].

A possible solution to reduce capacitive substrate loss is by using microelectromechanical systems (MEMS) technology. The first technique lends itself in removing the Si substrate beneath the inductor using micromachining techniques [**41**], [**42**]. This is typically achieved with a chemical etching process which results in the inductor suspended over a cavity. In a second approach, the inductor is elevated above the substrate without removing the substrate below the inductor. The suspended inductors are typically fabricated on pillars providing substrate isolation and structural stability [**43**], [**44**], [**45**]. A crucial design aspect of micromachined and suspended inductors is temperature stability which results in structural deformation of the inductor via thermal expansion of the material. Various simulations are conducted to observe the variation in inductor performance and reliability. Both these techniques have shown considerable *Q*-factor improvements but only in the RF range. At mm-wave frequencies the substrate isolation techniques presented by MEMS quickly diminishes and substrate losses continue to reduce the *Q*-factors.

Another approach to improve the *Q*-factor of inductors is by fabricating the inductors vertically. In this approach the magnetic fields flow perpendicular to the substrate reducing

magnetic loss and due to the lower effective area of the inductor with respect to the substrate, capacitive loss is reduced. In [**46**], the vertical spiral inductors are fabricated using a plastic deformation magnetic assembly (PDMA) process. The spiral inductor is first fabricated horizontally and then permanently deformed in a vertical position using a magnetic field on the magnetic material. The *Q*-factor of the inductor is 3.5 while in the horizontal position and improves to 12 after the deformation process, showing a considerable performance improvement.

Shielding structures are also proposed where a solid ground shield is placed between the conductor trace and the substrate. The electric fields of the inductor are terminated before reaching the silicon substrate, ultimately reducing capacitive substrate loss. A serious drawback to this approach is that the magnetic fields induce an image current flowing on the ground plane which generates an opposing magnetic field reducing the inductance of the inductor. In order to eliminate the image current, the ground shield is patterned to cut-off the path of the induced current loop, [**47**]. Theoretically the patterned ground shield does reduce the electric field leakage to the substrate to zero, but in practise it becomes difficult to implement a ground reference that does not suffer some voltage fluctuation due to interconnect parasitics, [**17**]. This voltage fluctuation on the grounded shield is responsible for electric fields leaking to the substrate, reducing its shielding effectiveness. A floating shield which is not connected to any voltage lines is proposed in order to reduce substrate loss. This shielding technique is only possible when the shield is subjected to a net electric flux from the inductor, equal to zero. The voltage on the floating shield will remain 0 V with respect to the inductor and can therefore act as an effective electric shield between the inductor and substrate.

2.7 INDUCTOR CONFIGURATIONS

Inductors are generally divided into spiral inductors and transmission lines. Spiral inductors generally have a total length that is less than a 10th of the wavelength at the frequency of operation and is typically implemented in the RF and microwave frequency range. Transmission lines are used when the frequency of operation allows practical line length implementations on-chip and is therefore ideally suited for the mm-wave frequency range. Transmission lines are typically implemented as quarter or half wave stubs. The following section will discuss some of the preferred inductor configurations and their respective advantages.

2.7.1 Spiral inductors

Spiral inductors are defined by its trace width (*W*), trace spacing (*S*), the diameter (*d*) of the spiral and the number of turns (*N*). The trace height (*t*) is typically defined by the fabrication process, depending on the metal layer used. Various configurations are possible ranging from rectangular, circular, octagonal spirals or simple meander lines. Rectangular and octagonal spirals are more frequently used than circular structures due to their simpler layout, but do suffer decreased performance compared to circular structures [**40**]. Other more complex structures use stacked inductors [**48**]. Using the metal layers available in a fabrication process, inductors are connected in such a way that the high frequency current flows in the same direction through the stacked inductors. The magnetic flux lines add which results in higher mutual inductance. The total inductance of a two-level stacked inductor is given by

$$L_T = L_1 + L_2 + 2M, \tag{2.23}$$

where L_1 and L_2 are the self inductances of the spirals and M is the mutual inductance between them. For stacked spirals, the inductors are identical ($L_1 = L_2 = L$) and the mutual inductance ($M \approx \sqrt{L_1 L_2}$) is equal to L when tightly coupled. Thus the maximum inductance of the two-level stacked configuration approaches $4L$. Similarly, an n-layer inductor will achieve an inductance of n^2 times that of one spiral. With the availability of a number of metal layers in a fabrication process, high inductance values can be achieved in a smaller area.

2.7.2 Transmission lines

The microstrip structure is defined by a signal width (*W*), a signal thickness (*t*) on top of a dielectric substrate with a thickness (*h*). The bottom of the substrate is a ground plane. The electromagnetic fields of the microstrip extend within two media: the air above and the substrate below. The structure is therefore inhomogeneous and does not support pure transverse electromagnetic (TEM) wave. Pure TEM wave only has transverse components and the propagation velocity only depends on the material properties (permittivity, ε and permeability, μ) of the structure. The presence of the two media will ensure that no longitudinal components of electric and magnetic fields exists and their propagation velocities will depend not only on the material properties, but also on the physical dimensions of the microstrip. One may assume that the longitudinal components of the fields for the dominant mode are much smaller than the transverse components and may

therefore be neglected. The dominant mode then behaves like a TEM mode and the TEM transmission line theory is applicable for the microstrip. This is called the quasi-TEM approximation. With this approximation, a homogeneous dielectric material with an effective dielectric permittivity replaces the inhomogeneous dielectric-air media of the microstrip. The transmission characteristics of the microstrip are then described by two parameters: the effective dielectric constant ε_{eff} and the characteristic impedance Z_C.

A coupled microstrip line will support two quasi-TEM modes, i.e. an even mode and an odd mode as shown in Figure 2.10 [**49**]. In an even mode excitation, the lines have the same voltage potential (the same sign charges) resulting in a magnetic wall at the symmetry plane. In the case of an odd-mode excitation, both lines have opposite potentials (opposite sign charges) so the symmetry plane is an electric wall. If the two modes are excited at the same time, they will propagate with different phase velocities because they are not pure TEM modes, which mean they experience different permittivities. A coupled microstrip line is characterized by the characteristic impedance and the effective dielectric constants of the two modes. The coplanar waveguide (CPW) structure resembles a coupled microstrip line without the ground plane. The structure is defined by three conductors separated by a distance (*S*). The center conductor is the signal line with a signal width (*W*) and two adjacent conductors acting as the ground plane. The CPW structure is also assumed to support the quasi-TEM mode of propagation and offers several advantages over conventional microstrip lines. The most prominent advantage is that the electric fields are confined between the signal and ground conductors, reducing coupling to the substrate.

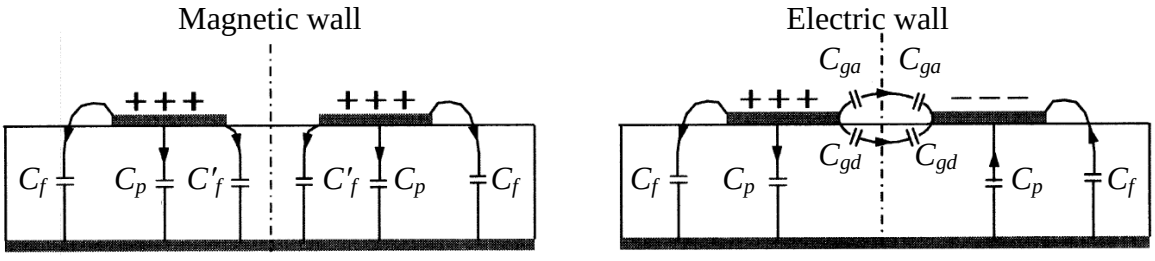

Figure 2.10. Quasi-TEM modes of a pair of coupled microstrip lines: (a) even mode; (b) odd mode [**49**] (© [2001] IEEE).

The relatively small signal-to-ground spacing defined by the fabrication process for microstrip monolithic microwave integrated circuits (MMICs) constrains the reactive

energy storage of the structure. Very little design freedom is available for the microstrip structure. The signal width is specified for a given characteristic impedance and effective dielectric [**49**]. CPW in contrast allows a much wider signal line because the signal-to-ground spacing is not defined by the dielectric thickness [**50**]. CPW can therefore provide more variability in design to achieve the same characteristic impedance and effective permittivity than microstrip lines.

2.7.3 Slow-wave transmission lines

Transmission line theory states that the phase velocity of a propagating wave is controlled by the surrounding dielectric media given by

$$v_p = f.\lambda = \frac{c_o}{\sqrt{\mu_r \varepsilon_r}}, \tag{2.24}$$

where c_o is the velocity of light, μ_r is the effective relative permeability and ε_r is the effective relative permittivity. Generally, a reduction in phase velocity will result in a reduction in wavelength and a corresponding increase in ε_r at the operating frequency. Thus for conventional transmission lines such as microstrip and CPW, the wavelength is fixed and therefore the structures remain fairly large even at very high frequencies.

The relationship between wave propagation and the resistivity of the silicon substrate on a Si-SiO_2 system has been summarized in [**51**]. It was concluded that three modes of propagation exist, i.e., dielectric quasi-TEM mode, skin-effect mode and slow-wave mode, which is shown in Figure 2.11, with the frequency–resistivity condition for each.

The three modes of propagation are shown to exist due to different behaviours of the substrate when frequency and resistivity is varied. The quasi-TEM mode of propagation would exist when the substrate acts like a good dielectric (low conductivity Si substrate) at high frequencies. The skin-effect mode propagates when the substrate conductivity is large enough to yield a small depth of penetration and behaves like a lossy conductor. Between these two modes at intermediate frequencies, the slow-wave mode of propagation exists. The slow surface wave propagates along the line with the substrate acting like neither a dielectric nor metallic. Measurements of the metal-insulator-semiconductor (MIS) transmission lines revealed that the slow-wave mode has desirable characteristics such as lower dispersion and losses. The measured velocity of the slow-wave mode was 15 to 30 times slower than the velocity of light in a vacuum.

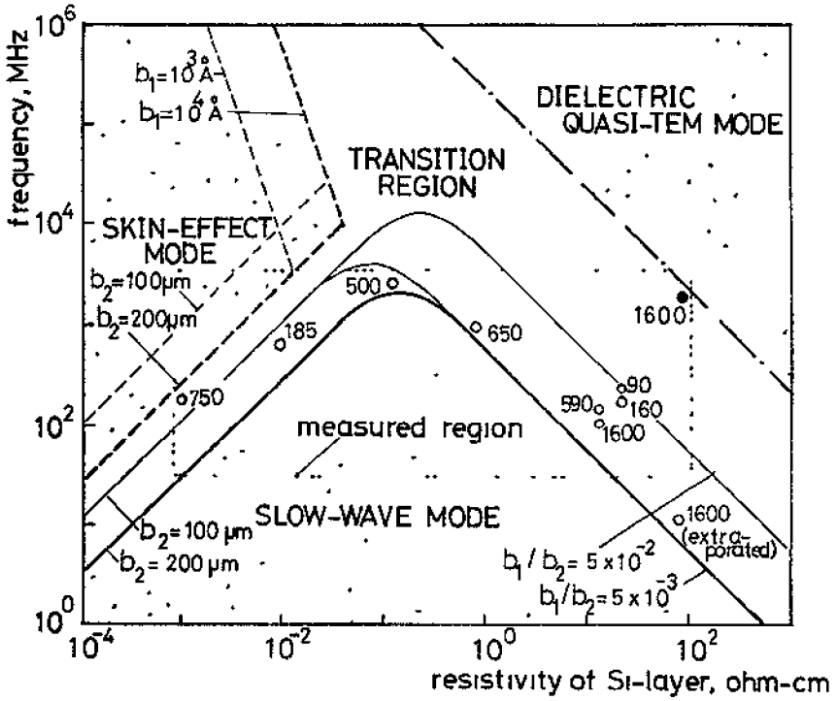

Figure 2.11. The three propagation modes given by the frequency-resistivity domain chart [**51**] (© [1971] IEEE).

To improve the performance of slow-wave microstrip lines and generate a significant slow-wave effect, a periodic structure in the ground plane was proposed [**52**]. The unique ground plane produced a distributed LC network that resulted in a slow-wave factor of 1.2 to 2.4 times larger than conventional microstrip lines over a much wider frequency range. As long as the current density of the return current is small, no considerable loss will be introduced by the discontinuities in the ground plane.

With the little design freedom available in microstrip lines, [**53**] showed that CPW structures are also able to achieve the slow-wave mode of propagation. In this case, an epitaxial layer is grown below the CPW conductors which allow magnetic field lines to pass through but prohibits electric field lines to penetrate the substrate. Consequently, electric energy is stored between the CPW and epitaxial layer while the magnetic energy is stored around the CPW conductors. Due to this partitioning of energy storage, the propagation velocity is much smaller than the permittivity of the surrounding media suggests. Another approach to create a slow-wave substrate is to fabricate a cross-tie periodic pattern below the CPW lines, which consists of periodically doped regions within the substrate [**54**], [**55**]. Analysis shows that the basic structure consists of two different transmission line segments with different characteristic impedances and phase constants.

Together, the total characteristic impedance of the cross-tie transmission line is given by $Z_o = \sqrt{Z_A Z_B}$ where Z_A and Z_B represent the characteristic impedance of the two sections. It was also found that the attenuation constant of the cross-tie transmission line can be further reduced by using metal strips instead of highly doped regions within the substrate.

In [**17**], [**21**], [**56**], metal strips are placed on a lower metal layer in the fabrication technology. Similar to the cross-tie periodic pattern described in [**54**] and [**55**], the metal strips are placed below the CPW traces to produce the slow-wave substrate. This is illustrated in Figure 2.12. As the shield is placed in close proximity to the CPW structure, the capacitance is primarily determined by the distance between the shield and CPW lines. The inductance is given by the area between the signal conductor and the return ground lines.

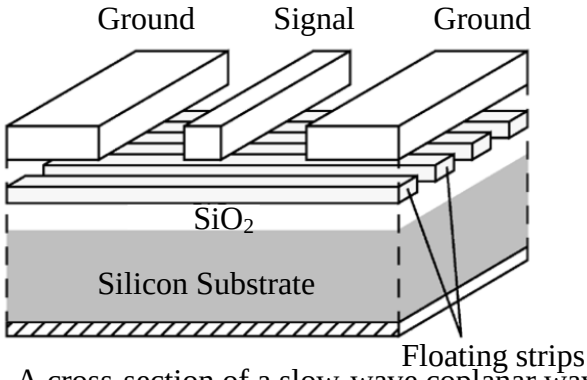

Figure 2.12. A cross-section of a slow-wave coplanar waveguide transmission line [**17**] (© [2006] IEEE).

Eddy-current loss plays a significant role in the effectiveness of the shielding structures, owing to the high conductivity of the metal strips. In [**57**], it was reported that patterned ground shields lose their shielding effectiveness at 20 GHz or above and that *Q*-factors of devices with patterned ground shields can be degraded further to be even lower than that of unshielded structures. Floating shields prove to be more advantageous at higher frequencies and should be the preferred choice above 20 GHz. The properties of the shielding structures such as the strip length (SL), strip spacing (SS) and the dielectric height (h) have also been investigated with respect to the critical transmission line properties such as attenuation constant (α), effective relative permittivity (ε) and *Q*-factor [**57**]. Experimental results revealed that an increase in shielding density together with an increase in h reduces α of the slow-wave structure. This is an opposing interest to the effective relative permittivity which increases when h decreases. The *Q*-factor of

transmission lines are defined by $\beta/2\alpha$ where β is the phase constant of the transmission line and will therefore judge the overall trade-off between the attenuation loss and effective relative permittivity. It has been shown that at lower frequencies, the shielding structure should be placed closer to the CPW lines as the phase constant dominates to produce the highest *Q*-factors. At higher frequencies, the shielding structure should be placed further away from the CPW lines, therefore increasing the density of the shields to reduce eddy-current loss. This will ultimately reduce the effective relative permittivity of the slow-wave structure but will decrease the overall attenuation constant which proves to be the dominant factor at higher frequencies.

2.8 CONCLUSION

This chapter has identified some of the important concepts relating to the design and manufacturing of mm-wave LNAs; the most important of which is the proper design and selection of on-chip passive inductors. The major sources of inductor loss have also been identified which is responsible for the *Q*-factor degradation at high frequencies. MEMS technology has been unable to effectively isolate the inductor from substrate loss since it proves more advantageous to fabricate the inductor in the highest metal layer available in a fabrication process, further away from the substrate and because the higher metal layers provide the lowest conductor loss. Transmission lines have therefore been the preferred passive component to produce an effective inductance.

The slow-wave mode of propagation has also been realised due to the addition of metallic shielding structures which also proves to be the most effective substrate isolation technique. The slow-wave phenomenon reduces the wavelength of the propagation wave which reduces the required length of the transmission line. With the reduction of substrate loss due to the patterned shields, higher *Q*-factor figure of merits are obtained. Some of the *Q*-factor improvements of the slow-wave CPW lines compared with normal CPW lines are summarised in Table 2.1 with a description of the accompanying geometry layout given in Table 2.2.

Table 2.1. *Q*-factor improvements due to the metal strips introduced to conventional CPW transmission lines

References	Characteristic impedance (Ω)	Frequency range	Measured *Q*-factor	*Q*-factor improvement
[**17**]	50	15-40 GHz	25-35	> 2
[**21**]	30-50	20-100 GHz	10-15	> 3
[**57**]	20-60	30-40 GHz	15-20	> 5
[**58**]	35-45	30-60 GHz	12-14	> 2

Table 2.2. *Q*-factor improvements due to the metal strips introduced to conventional CPW transmission lines

References	Fabrication process	CPW metal layer	Shield metal layer	Shield type
[**17**]	0.18 µm SiGe BiCMOS	M4	M3	Floating
[**21**]	90 nm CMOS	-	-	Ground
[**57**]	45 nm CMOS	M10	M9	Floating
[**58**]	65 nm CMOS	M6	M1, M2	Ground

It is shown that *Q*-factor improvements of more than two are realizable over a very wide frequency range as listed in Table 2.1. *Q*-factors of more than 10 are feasible with the appropriate CPW geometry and accompanying shielding structure. Table 2.2 describes the geometry layout of the CPW conductors and the metal shield. The placement and type of shielding structure employed establishes a specified attenuation constant and effective relative permittivity. It is apparent that the geometry and layout of the CPW lines and shielding structure contribute to the *Q*-factor and that optimisation is required to reduce the various forms of losses.

CHAPTER 3: METHODOLOGY

3.1 INTRODUCTION

Chapter 2 provided a literature review concerning the noise analysis of LNAs and the various noise sources in SiGe HBTs, as well as the different loss mechanisms associated with on-chip mm-wave passive inductors and techniques to address them. Chapter 3 describes the methodology followed to undertake the research of the proposed topic to test the hypothesis in question. This chapter will further elaborate on the introduction to the methodology given in section 1.4 in chapter 1 and provide the appropriate research procedures followed.

3.2 JUSTIFICATION FOR THE METHODOLOGY

Several Si-based LNAs operating at mm-wave frequencies have been implemented and all emphasizes that, active and passive devices at mm-wave frequencies require thorough investigation before implementing in a design [**31**], [**32**], [**50**]. Specifically passive components used in input and output matching networks directly determine the power transfer and noise performance of LNAs. Consequently, passive component modelling becomes essential to determine the high frequency losses and coupling effects associated with mm-wave frequencies which alter the characteristic impedance and performance of the structures [**21**]. Close correlation with process parameters are also required for DRC and accurate modelling.

Experimental verification by means of a fabricated prototype allows complete characterization of the passive inductors and consequently the performance of the LNA. The prototype allows for gathering of the data required to test the hypothesis.

3.3 OUTLINE OF THE METHODOLOGY

The research methodology followed in this dissertation is summarised in Figure 3.1. The outline consists of four main sections, i.e. research foundation, experimental setup, experimental results and conclusion. Figure 3.1 also shows the associated subsections which exemplifies the research methodology in more detail.

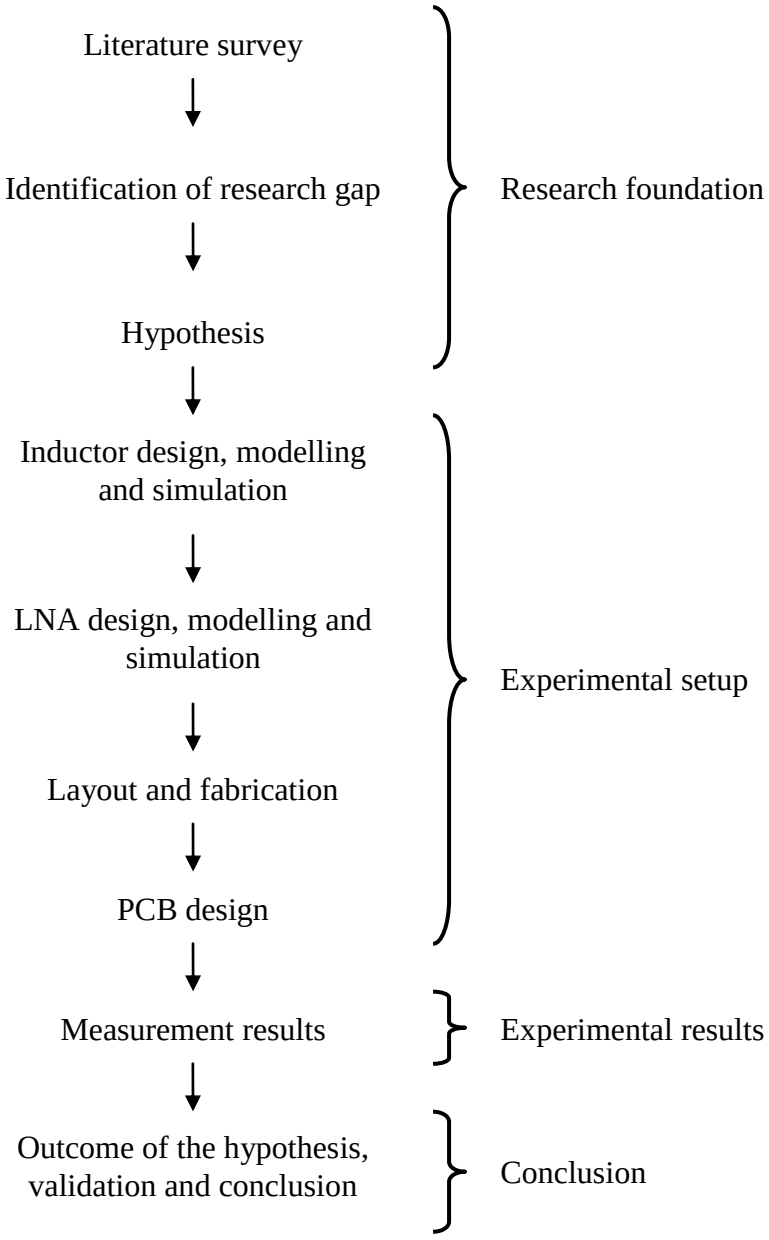

Figure 3.1. Outline of the research methodology.

The following list describes the research procedures undertaken to prototype the LNA:

- *Theoretical background* – A literature study is conducted on a number of important aspects concerning LNAs in general. Critical aspects are discussed such as NF and gain, the matching networks and circuit topologies. Furthermore, the literature study also focussed on several high frequency effects associated with on-chip inductors. Various techniques and improvements are discussed to address these problems.

- *Mathematical and software design* – Further investigation in optimising passive inductors for the 60 GHz LNA is achieved through mathematical modelling and software design. The modelling and software design is very closely integrated and subsequently done concurrently. The passive inductors are designed and simulated in EM software to achieve the optimised response and an equivalent circuit is extracted to be included in Cadence design systems. The LNA is designed and simulated in Cadence Virtuoso. The LNA design methodology and the software packages used in the design are discussed in sections 3.4 and 3.5, respectively.

- *Low level design* – The LNA is prototyped using the 0.13 µm SiGe BiCMOS process from IBM. The low level design includes the final chip layout together with DRC and layout versus schematic (LVS) verification. Cadence Virtuoso from Cadence design systems is the software package used to construct the low level design.

To gather data required to test the hypothesis, the experimental setup can be further broken down as follows:

- *Passive inductors* – With complete characterisation of the passive inductors required for data collection, several passive inductors are fabricated and prototyped. These inductors are prototyped completely independent from the LNA. The passive inductors fabricated and included in the IC design are discussed in chapter 4.

- *LNA* – Two LNAs are fabricated which includes the characterised passive inductors. The two LNAs provide a comparative measure to allow any performance difference to be observed. The two LNAs are identical in most aspects to eliminate any external control to influence the results. The LNAs and the passive inductors implemented in the design are discussed in chapter 5.

Following the experimental setup as illustrated in, measurements are conducted on the fabricated prototype. The prototype is fabricated by IBM, wirebound and soldered to a PCB. The PCB provides the DC biasing required for the LNA circuits while simultaneously allow on-chip measurements to be conducted. The equipment used for

measurements and the complete measurement setup is discussed in sections 3.6 and section 3.7, respectively.

3.4 LNA DESIGN METHODOLOGY

The key performance requirements for mm-wave LNAs are power gain, NF, linearity, stability, impedance matching, power dissipation, bandwidth and design robustness with respect to process, voltage and temperature variation [**10**]. Typically these requirements are universal making LNA design a multi-dimensional optimisation problem. The requirements are graphically illustrated in Figure 3.2. LNA design methodology at mm-wave is to some extent similar to the methodology followed at lower frequencies, but requires a different emphasis at the fundamental design stage [**59**]. The circuit topologies are different and the design at mm-wave is required to account for difficulties namely, designing the transistor closer to its f_T which limits the maximum available power gain and the smaller wavelengths necessitates distributed effects be taken into account. The implications of this are careful design and consideration to high frequency effects and stray parasitics.

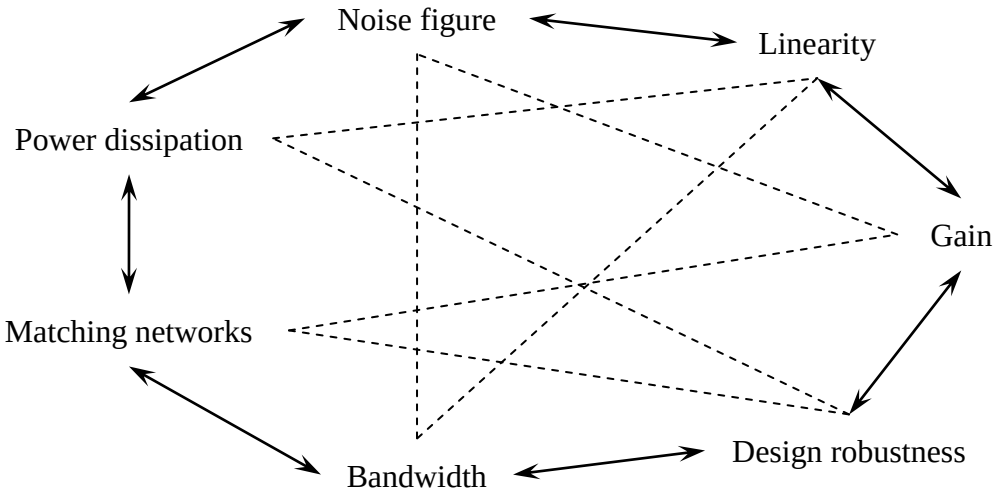

Figure 3.2. A graphical illustration of the multi-dimensional optimisation problem faced in the LNA design.

For mm-wave LNAs, the fundamental objective is to provide a high power gain while contributing a minimal amount of noise [**34**], [**30**]. The purpose of the LNA is to deemphasise the noise of subsequent receiver stages and can only be achieved with sufficient gain. The mm-wave LNA methodology firstly selects the optimum bias point,

layout and transistor technology with a suitable f_T, to achieve a NF_{min}. The input and output impedance matching networks are optimised to achieve NF_{min} and maximum power transfer [**10**]. Failing to achieve a noise and power match will result in a suboptimal return loss and high NF.

The methodology for the input matching network is described in [**13**] where a relationship is established between the optimum noise impedance and input impedance of the device; the optimum noise conductance, $G_{s,opt}$ differs from the input conductance and the optimum noise susceptance, $B_{s,opt}$ is equal to the complex conjugate of the input susceptance of the device. This characteristic allows the real part of the input impedance to be matched separately from the real part of the noise impedance and consequently allows simultaneous input impedance and noise matching. In this methodology, the size of the transistor is considered a design variable and the optimum noise current density is found to realise the 50 Ω system impedance. Noise matching is therefore realised with optimal biasing and transistor sizing. Input impedance matching is realised by including an emitter inductor to match the real part of the input impedance to 50 Ω. Lastly a base inductor is placed to cancel the input reactance to simultaneously achieve a noise and input impedance match.

The output impedance is matched to the characteristic impedance of the system typically with a three element matching network as described in [**7**], [**8**].

3.5 MODELLING, SIMULATION AND LAYOUT DESIGN

Modelling and simulation of the LNA is done in two sections. The first comprises the design of passive components and in particular, the inductors. These structures are very large and lossy and therefore require a great deal of optimisation. To find the detail necessary to investigate the losses associated with inductors, a high quality EM simulator is used. The chosen simulator is IE3D from Mentor Graphics which is a 3D method of moment (MOM) simulator. The justification for using a surface simulator and not a volume simulator is based on the geometry of the inductors which is very planar. Surface simulators also tend to be much faster than volume simulators with the added advantage of providing smooth current and electric field distributions. The only concern is the coupling between the metal lines due to their finite thickness which is crucial in inductor design but is addressed in IE3D. A typical MOM simulator models the metal layers of any structure as an infinitely thin strip which is particularly problematic with shielded inductors due to the

strong coupling between conductors and the shielding strips. The simulation results would inadvertently overestimate the characteristic impedance and *Q*-factor for these structures. IE3D resolves this by modelling the true metal thickness. With sufficient meshing together with the true metal thickness, more accurate simulation results are achieved.

After the design and optimisation phase, the inductors are modelled as an equivalent circuit which can then be incorporated in a circuit simulator. The Cadence Virtuoso package from Cadence Design Systems is the electronic design automation (EDA) tool chosen for this purpose. Cadence is the world's leading EDA company with vast experience in electronic design and EDA tools. The LNA together with the modified inductor models are designed in the Cadence Virtuoso graphical schematic level circuit design environment and simulated in Virtuoso analog design environment (ADE). Virtuoso layout editor is used to generate the layout design and Assura LVS and DRC is used to verify the accuracy and appropriateness of the design for fabrication.

3.6 MEASUREMENTS AND MEASUREMENT EQUIPMENT

Typically an IC is packaged as it readily integrates with a larger system and simplifies the measurements process, but mm-wave device packaging can become a source of performance degradation as wirebonds and flip-chip bumps are not of a waveguide structure and therefore create signal mismatches [**60**]. These performance degradation concerns are one of the primary reason why on-chip measurements are typically performed using precision measurement equipment together with an on-wafer probe station. The probe station lowers contact probes onto the chip and makes contact with the input and output connections of the device under test (DUT). Careful considerations have to be made during mm-wave layout and must be completed prior to the circuit design phase. One of the key concerns is the IC connection to the wafer-prober. Square bondpads are placed around the chip to accommodate DC needle-type bias injection probes or wirebonds to supply the circuit with the necessary biasing. The RF input and output connections are made using the ground-signal-ground (GSG) format. Three pads are placed alongside each other with ground connections on either side of the signal pad, providing a reliable RF ground for the circuit. The probes used for measurements will determine the spacing between the adjacent bondpads and bondpad size. The probe pitch is crucial as the size of the bondpads determine parasitic effects which must be included in the circuit schematic. The probe used in this work is shown in Figure 3.3.

Figure 3.3. GSG probe used during measurements.

The probes shown in Figure 3.3 are known as Picoprobes manufactured by GGB industries[1]. The Picoprobe 67a DP-type mounting style is used in this work. The probe has a frequency range from DC-to-67 GHz and has a probe pitch of 150 µm.

Measurements are conducted using the Anritsu 37397D vector network analyser (VNA). The analyser has a frequency range of 40 MHz to 65 GHz and is shown in Figure 3.4. On-wafer measurements are performed with the PM5/Suss MicroTek probe station. The MicroTek probe station allows wafer or substrate measurements of up to 150 mm (6”).

Figure 3.4. The Anritsu 37397D VNA.

The DC measurements and characterisation is realised using the 4200-SCS Keithley Semiconductor Characterisation System. The 4200-SCS Keithley enables voltage and current biasing and is compatible with DC needle-type probes. Additionally, voltage and

[1] www.ggb.com

current sweeps enable the 4200-SCS Keithley real-time characterisation and analysis of the DC performance of the DUT.

3.7 MEASUREMENT SETUP

Calibration of the VNA with the probe station up to the probe tips is achieved with the alumina calibration standard substrates from GGB industries. The CS-5 and short-open-load-through (SOLT) calibration substrate and calibration support type is used, respectively. The GSG footprint and 150 µm probe pitch is supported in this calibration setup. The measurement setup is calibrated from 40 MHz to 65 GHz with accurate calibration obtained by means of a calibration power sensitivity of -15 dBm. Following the VNA calibration, direct on-wafer measurements of the inductors is obtained characterising the inductor performance with the 2-port *s*-parameter results.

The LNA setup is illustrated in Figure 3.5.

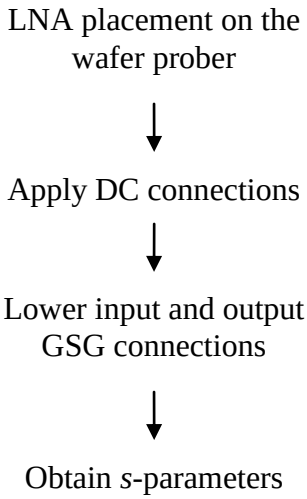

Figure 3.5. The measurement setup of the LNA.

Figure 3.5 illustrates the measurement setup for the LNA. The LNA setup firstly connects the 4200-SCS Keithley to apply the appropriate bias condition. The one probe connection of the 4200-SCS Keithley is connected to the base connection of the LNA to supply the required current and voltage bias. The second and third probes are connected to the supply voltage and ground connection of the LNA, respectively. After the correct bias connection is applied, the GSG probes from the probe station are lowered onto the LNA input and

output pad connections. With proper connection the s-parameter measurements for the LNA are obtained.

3.8 CONCLUSION

This chapter provided a complete overview of the research methodology used in this dissertation. The steps involved to design, simulate and prototype the LNA and the software packages used is also described. The measurement equipment used during the experimental testing as well as the measurement setup is discussed.

CHAPTER 4: INDUCTOR DESIGN

4.1 INTRODUCTION

This chapter focuses on the design of on-chip passive inductors. Following the literature study in chapter 2 it is essential to design high performance inductors specifically for the 5 GHz unlicensed bandwidth around 60 GHz. The performance metric used is the *Q*-factor and this chapter will focus on improving and optimising the geometry of the inductor which will be implemented in the design of the LNA in chapter 5. The performance of the LNA has a direct relation to the inductor *Q*-factor as the matching networks contribute to the LNA gain, NF and bandwidth.

Due to the short wavelength at mm-wave frequencies, transmission lines will be used as the preferred inductor configuration. The limited design freedom present in microstrip marks the CPW as the favoured transmission lines structure. As reported in chapter 2, transmission lines experience high insertion loss due to the losses associated with the substrate. It is therefore required to isolate the transmission line from the substrate by means of a patterned metal shield. Additionally, the patterned metal shield will slow the propagation velocity because electric fields will mostly be confined between the metal strips and the CPW traces, while the magnetic fields will pass the metal shield. The resulting structure will be the slow-wave coplanar waveguide (S-CPW) transmission line. Chapter 2 furthermore reported that the SL, SS and the separation distance of the signal conductor and the shielding structure has previously been investigated with respect to the attenuation and phase constant. This chapter will utilize the signal-to-ground spacing of the S-CPW transmission line as the geometrical parameter to optimise. Optimisation of the signal-to-ground spacing will facilitate an improvement of the S-CPW *Q*-factor which has not previously been investigated in literature.

The first part of this chapter starts with the extraction of parameters used to define the performance of passive inductors. These parameters are used to generate an equivalent simulation program with IC emphasis (SPICE) model that can be imported into a circuit simulator to form part of the LNA design. The chapter uses technology information defined by the fabrication foundry which determines the minimum and maximum distances of metal lines, the resistivity of the conductors, and the permittivity of the dielectrics used in fabrication. The technology information is used to determine the simulation environment in which the EM modelling is conducted.

Two types of simulation are conducted on the inductor structures. These two types of simulation will be used to define and characterise the performance of the inductor structures and to obtain the preferred geometry. The first simulation is done by varying the signal-to-ground spacing of the CPW conductors. This geometry parameter plays a significant role in the overall performance of the structures. The inductor characteristics are simulated over the signal-to-ground spacing to investigate the structure's behaviour over this critical parameter. The second simulation investigates the structure's behaviour over frequency. All the characteristics are simulated in order to determine the preferred geometry which will be used in the LNA design of chapter 5.

The chapter concludes with a visual illustration of the electric field distribution of the inductor structure. This illustration is a graphical representation of electric field distribution of the inductor geometry at 60 GHz. The electric field distribution demonstrates the strong coupling between signal conductors and the metal shield, but also the reduced coupling of the electric field to the substrate.

4.2 PARAMETER EXTRACTION AND EQUIVALENT MODELS

Conventional small-signal parameters, *z*-, *y*-, *ABCD*-parameters are unable to accurately model high frequency transmission lines given that ideal open and short circuit terminations becomes impossible to realise [**61**]. Alternatively, *s*-parameters are represented by voltage ratios entering and leaving ports and is therefore ideally suited to characterise any high frequency multi-port network. It is however required to model a transmission line in terms of distributed or lumped equivalent elements or circuits. It is therefore necessary to extract the transmission line parameters from the *s*-parameters which are described hereunder.

The *s*-parameter matrix is typically generated from simulation and/or measurements. It is then converted to *ABCD*-parameters which contain the complex propagation constant, γ, and characteristic impedance, Z_c through the following relationship.

$$[ABCD] = \begin{bmatrix} Cosh(\gamma l) & Z_c Sinh(\gamma l) \\ \frac{1}{Z_c} Sinh(\gamma l) & Cosh(\gamma l) \end{bmatrix}. \tag{4.1}$$

Once γ and Z_c is determined, the distributed element transmission line parameters can be calculated from Telegrapher's equation [**61**]

$$\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} = \alpha + j\beta, \tag{4.2}$$

$$Z_c = \sqrt{\frac{(R\prime + j\omega L\prime)}{(G\prime + j\omega C\prime)}}, \tag{4.3}$$

where *R'*, *L'*, *G'* and *C'* represent the frequency dependent resistance, inductance, conductance, and capacitance of the transmission line, respectively. The distributed parameters are given in "per unit length" values. The parameters must be multiplied by the length of the transmission line segment they represent to obtain the actual resistance, inductance, conductance, and capacitance of the line. The distributed transmission line parameters can be calculated from

$$R' = Re\{\gamma Z_c\}, \tag{4.4}$$

$$L' = \frac{Im\{\gamma Z_c\}}{\omega}, \tag{4.5}$$

$$G' = Re\left\{\frac{\gamma}{Z_c}\right\}, \tag{4.6}$$

$$C' = \frac{Im\left\{\frac{\gamma}{Z_c}\right\}}{\omega}. \tag{4.7}$$

Additionally, lumped equivalent circuits can also be used to model inductors only when the electrical length of the structure is much less than the operational wavelength [**62**]. A lumped element model for a two-port transmission line can be obtained by converting the *s*-parameters of the line and fitting a resistance, capacitance and inductance value to the *y*-parameters to create a two-port π-equivalent lumped element model which is illustrated in Figure 4.1.

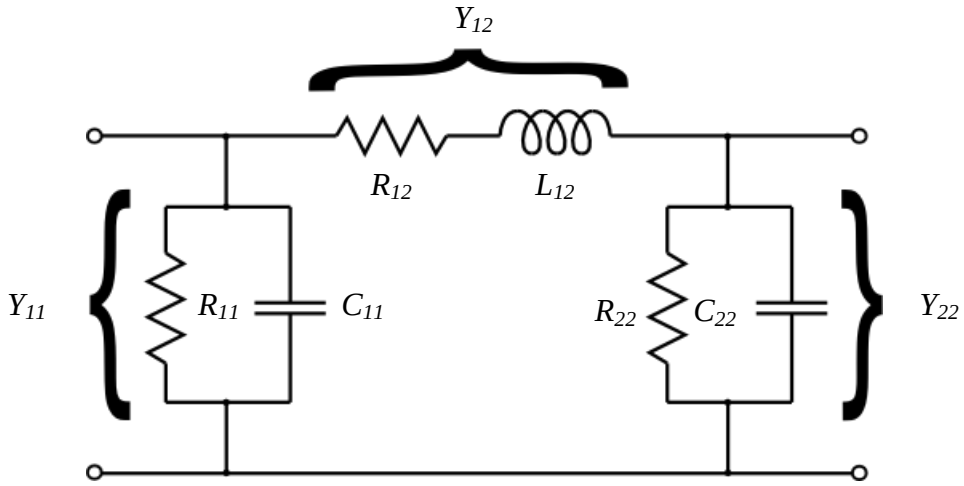

Figure 4.1. Lumped equivalent model generated from *y*-parameters.

A lumped equivalent model representing an entire length of transmission line is limited to a small frequency range, given that the elements within the model are frequency dependent. This model becomes problematic in wideband applications but is preferred due to its simplicity.

IE3D has two outstanding features when creating an equivalent model for a transmission line. The first is that a variety of (whether one-port, two-port, series *RL* and parallel *RC*, ect.) narrowband equivalent models can be generated from the *s*-parameters simulated from a transmission line structure. Secondly, IE3D addresses the small bandwidth limitation by being able to create a lumped equivalent model which represents the *s*-parameters of a transmission line over a wide frequency range. This lumped equivalent model can become quite complicated depending on the frequency range and structure simulated but can then be extracted in SPICE format to easily integrate in a larger design.

4.3 PROCESS PARAMETERS

The inductors must be designed with process specific parameters and layout rules as it determines the simulation environment with which the inductors will be simulated and designed with. The parameters will also determine the minimum and maximum distances between metal conductors.

A free IBM 8HP run was provided by MOSIS through the MOSIS educations program[2] (MEP). The free 8HP run formed part of a multi-project wafer (MPW) run which was a grant obtained through the acceptance of a research proposal relating to this author's work. The technology information and exact process parameters for the IBM 8HP process cannot be provided due to a non-disclosure agreement (NDA) with the foundry.

4.4 SLOW-WAVE TRANSMISSION LINE GEOMETRY

The slow-wave transmission line geometry is shown in Figure 4.2. It consists of a CPW over a patterned metal shield. The CPW is defined by the signal width (*W*), the spacing between the ground and the signal conductor (*S*), and the length of the transmission line (*L*). The patterned shield is placed a distance below the CPW (*H*) on a lower metal layer and is patterned with a SL and a SS.

[2] http://www.mosis.com/products/mep/mep-about.html

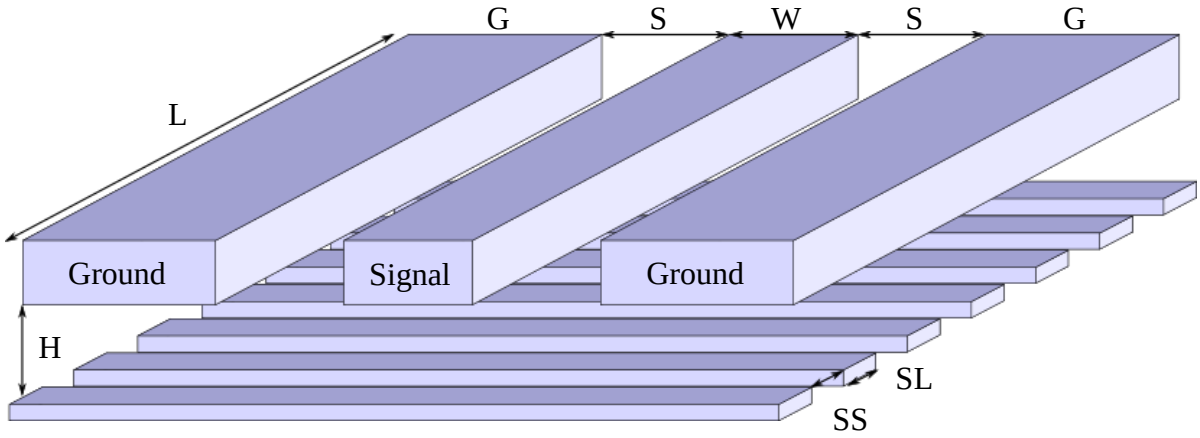

Figure 4.2. The slow-wave transmission line geometry.

From [**63**] the top most metal layer (AM) achieves the lowest ohmic loss per square which validates the reason for designing inductors on the top most metal layer in the fabrication technology.

To characterise the S-CPW through EM simulation, three slow-wave transmission line geometries were simulated. The three geometries have signal conductor widths of 28 µm, 32 µm and 36 µm which will enable the signal conductors to adhere to electron migration rules when carrying a DC, and simultaneously produce a characteristic impedance of approximately 50 Ω with proper selection of the ground conductor and shield spacing. The length of the geometries is chosen as 340 µm. This is to adhere to the requirement from IE3D Mentor Graphics which states that the electrical length of the line should be shorter than half of the waveguide wavelength. The ground conductor width is 50 µm which was chosen much larger than the width of the signal conductor so it appears as a ground plane. Finally, the patterned shield is chosen directly below AM, on LY, which is 4 µm away from the signal conductors and even though the LY metal minimum spacing is 1.52 µm, the SL and SS was chosen 5 µm. The chosen AM to LY separation distance together with the SL and SS spacing is sufficient to produce a high density metal shield below the CPW and simultaneously achieve a satisfactory trade-off between phase constant and effective relative permittivity. The geometry parameters are summarised in Table 4.1.

Table 4.1. The geometry parameters used to simulate the slow-wave transmission line structures

Geometry parameters	Dimension [µm]		
Transmission line length (L)	340		
Signal width (W)	28	32	36
Ground width (G)	50		
Signal-to-shield spacing (H)	4		
SL	5		
SS	5		

4.5 SIMULATION RESULTS OVER SIGNAL-TO-GROUND SPACING

With most of the geometry parameters of Table 4.1 defined by process definitions and simulation software requirements, it becomes necessary to investigate the behaviour of the S-CPW over various signal-to-ground spacings and its influence on the various transmission line parameters. This is graphically shown in Figure 4.3 where the structure exhibits the geometry parameters of Table 4.1 but at different signal-to-ground spacings.

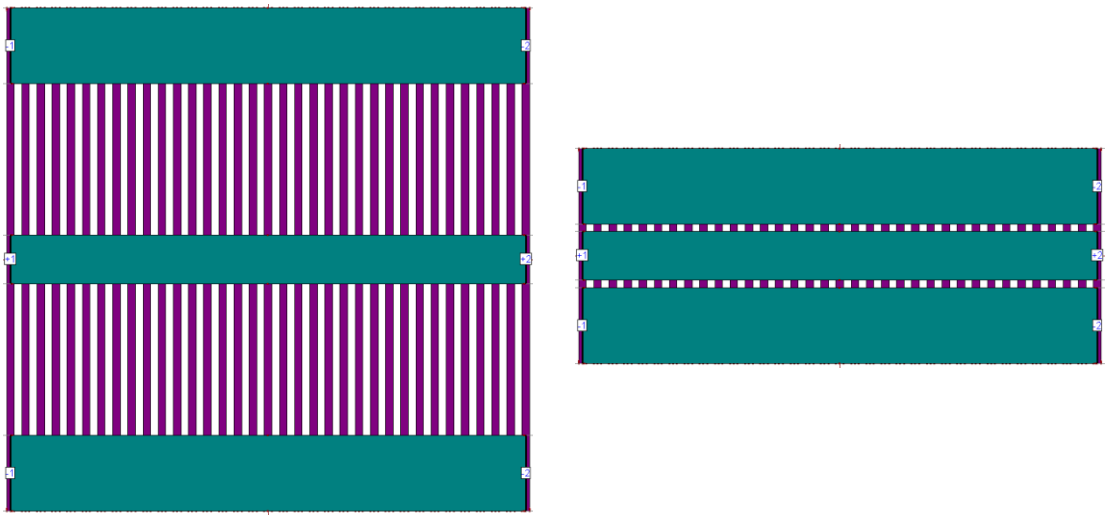

Figure 4.3. S-CPW with a signal width of 32 µm and a signal-to-ground spacing from 100 µm to 5 µm.

The three S-CPW structures with signal widths, 28 µm, 32 µm, and 36 µm, are simulated with a signal-to-ground spacing varying from 5 µm to 100 µm. This variation is investigated to find the optimum S-CPW geometry for each signal width. For this simulation the frequency is constant at 60 GHz.

Figure 4.4 shows that the characteristic impedance of the three S-CPW structures changes in a limited way when the signal-to-ground spacing is increased above 25 µm but decreases rapidly when the spacing is less than 25 µm. This shows that the total capacitance of the S-CPW is dominated by the signal-to-shield spacing when the signal-to-ground spacing is more than 25 µm but that the capacitance between signal-and-ground conductors must be taken into account when the spacing is less that 25 µm. The small discontinuity jumps in the characteristic curves is due to the meshing of the structure. A more finely meshed structure will result in a smoother response.

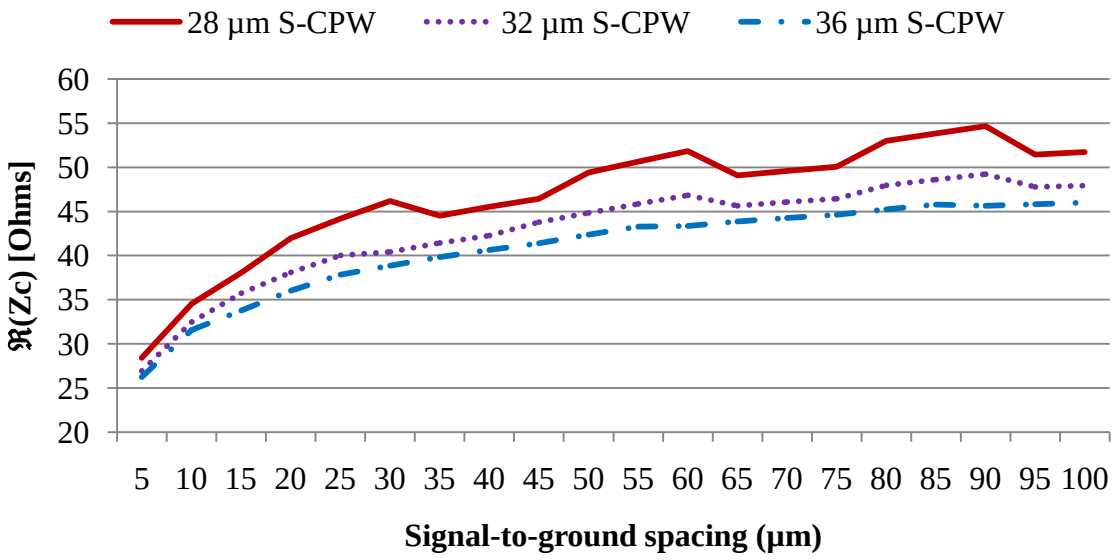

Figure 4.4. The real part of the characteristic impedance over the signal-to-ground spacing for the three S-CPW structures.

To find the *Q*-factor over the signal-to-ground spacing for all three the S-CPW structures, the attenuation and phase constant is simulated as shown in Figure 4.5 and Figure 4.6. The phase constant remains fairly linear over the entire spacing range but the attenuation constant increases rapidly when the spacing is less than 25 µm.

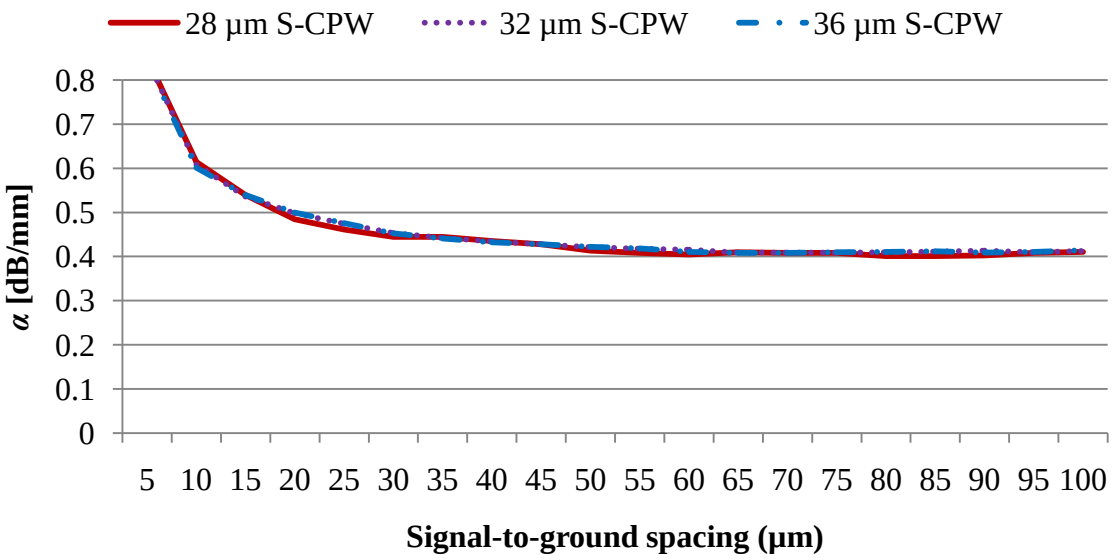

Figure 4.5. The attenuation constant over signal-to-ground spacing for the three S-CPW structures.

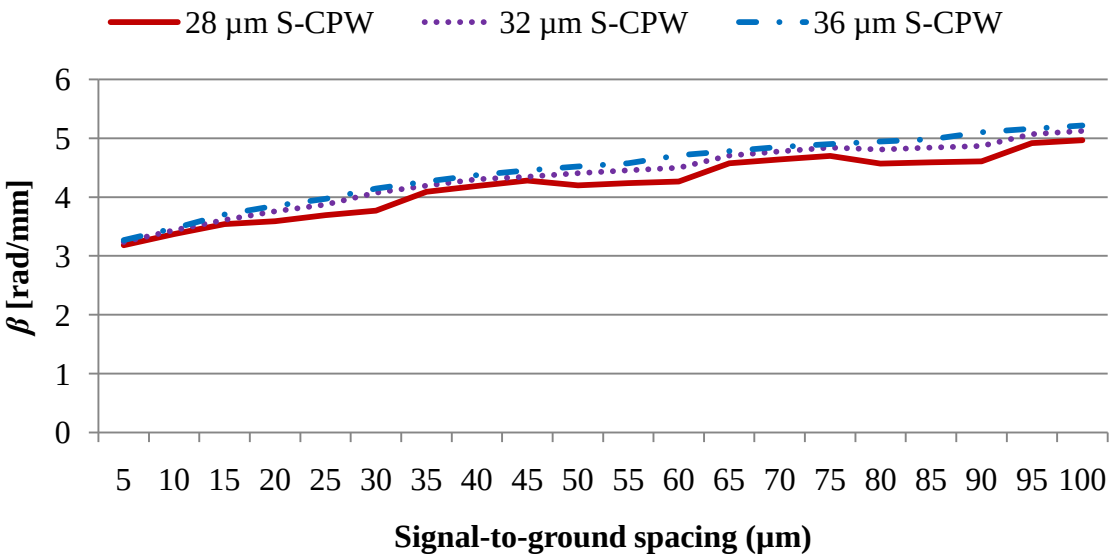

Figure 4.6. The phase constant over signal-to-ground spacing for the three S-CPW structures.

Figure 4.5 shows that the attenuation constant for all three structures is approximately the same but the phase constant differs slightly for each. The *Q*-factor is calculated using the relationship given in (4.8)

$$Q = \frac{\beta}{2\alpha}, \tag{4.8}$$

where α is converted to Nepers/mm and β in rad/mm. Figure 4.7 shows the Q-factor and how it increases as the signal-to-ground spacing is increased.

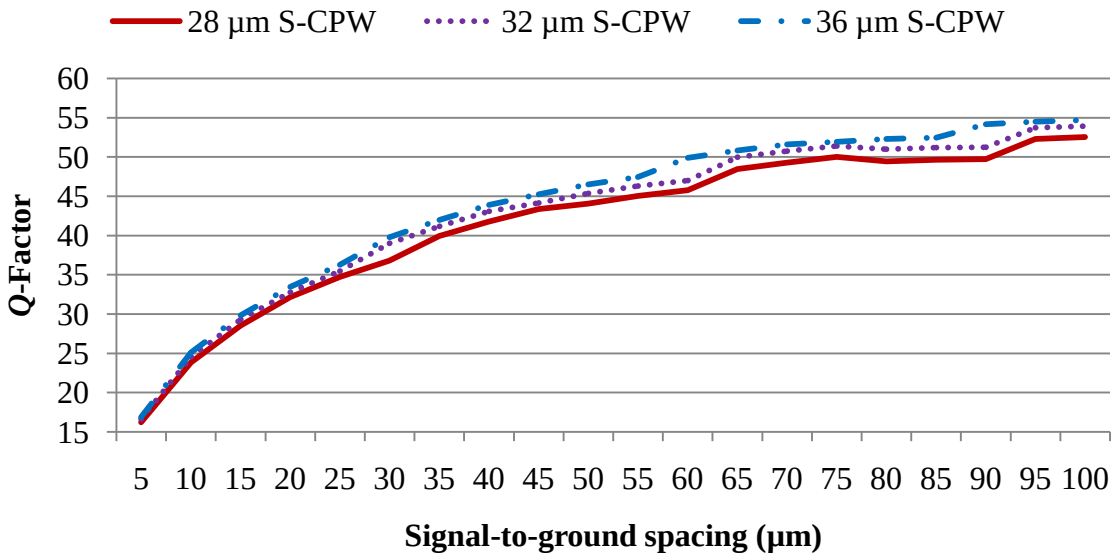

Figure 4.7. The Q-factor over signal-to-ground spacing for the three S-CPW structures.

From the transmission line parameters extracted from simulations conducted on the three S-CPW structures over signal-to-ground spacing, it is apparent that the range consists of two separate regions. Below 25 µm the S-CPW structures exhibit very high capacitive losses which are demonstrated by the attenuation constant response of Figure 4.5. For the three signal conductor widths of 28 µm, 32 µm, and 36 µm it is therefore more advantageous to choose a signal-to-ground spacing larger than 25 µm. There is however no dramatic Q-factor difference between the three signal conductor widths.

4.6 SIMULATION RESULTS CONDUCTED OVER FREQUENCY

To further investigate the three S-CPWs in terms of frequency, two signal-to-ground spacings for each signal width are chosen. Table 4.2 shows the chosen signal-to-ground spacing for each signal width. The selected parameters in Table 4.2 are justified using Figure 4.4 to facilitate characteristic impedance approximately equal to 50 Ω. All the signal-to-ground spacings are chosen to be larger than 25 µm.

Table 4.2. Two sets of signal-to-ground spacing is chosen for each S-CPW with a given signal width

S-CPW	Narrow signal-to-ground spacing	Wide signal-to-ground spacing
28 µm S-CPW	29 µm	62 µm
32 µm S-CPW	29 µm	69 µm
36 µm S-CPW	33 µm	90 µm

With two signal-to-ground spacings chosen for each signal width, six S-CPW structures will be simulated over frequency. In addition to the S-CPW structures, three CPW structures are also simulated to verify the performance improvement of the shield and to provide a performance metric comparison. The three CPW structures have a signal width of 15 µm, 25 µm, and 35 µm and a signal-to-ground spacing of 7 µm, 10 µm, and 13 µm, respectively. They are chosen to achieve a characteristic impedance of approximately 50 Ω similar to the S-CPW structures. The CPW lines are also designed in the top AM metal layer, the same process parameters and layout rules as the S-CPW structures. To uniquely identify each structure, a naming convention is applied as summarised in Table 4.3.

Table 4.3. A summary of the three CPW and six S-CPW structure geometries and the naming of each

Inductor summary	Signal width [µm]	Signal-to-ground spacing [µm]
15 µm CPW	15	7
25 µm CPW	25	10
35 µm CPW	35	13
28 µm S-CPW Narrow	28	29
28 µm S-CPW Wide	28	62
32 µm S-CPW Narrow	32	29
32 µm S-CPW Wide	32	69
36 µm S-CPW Narrow	36	33
36 µm S-CPW Wide	36	90

The first simulation shows that all the structures exhibit a characteristic impedance close to 50 Ω. The simulations are conducted with the specified transmission line geometries of Table 4.3 from 1 GHz to 100 GHz. Figure 4.8 to Figure 4.10 shows the real and imaginary components of the characteristic impedance of the wide S-CPWs, the narrow S-CPWs, and the three CPW structures, respectively.

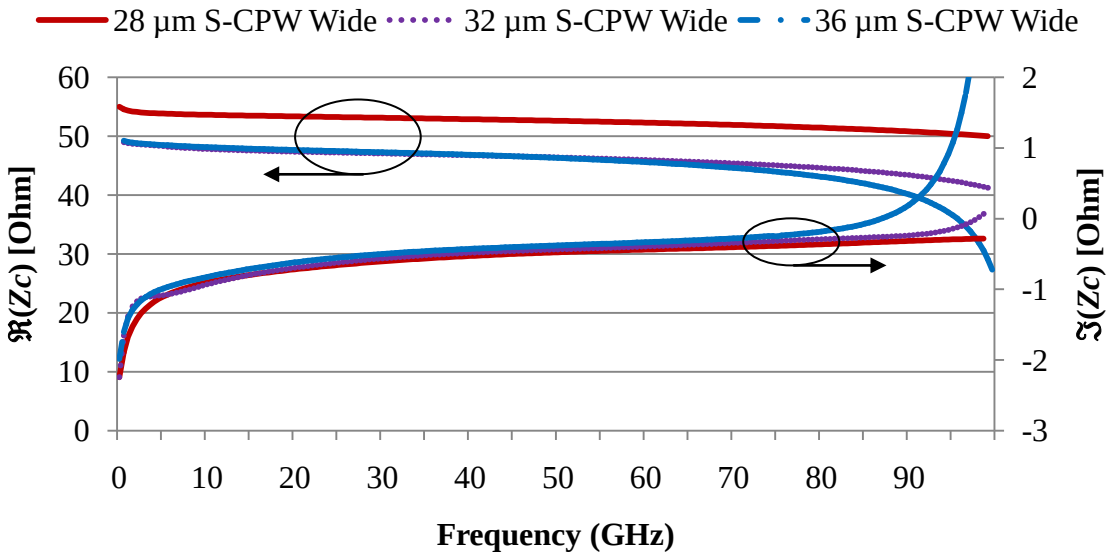

Figure 4.8. The real and imaginary characteristic impedance of the wide S-CPW structures from 1 GHz to 100 GHz.

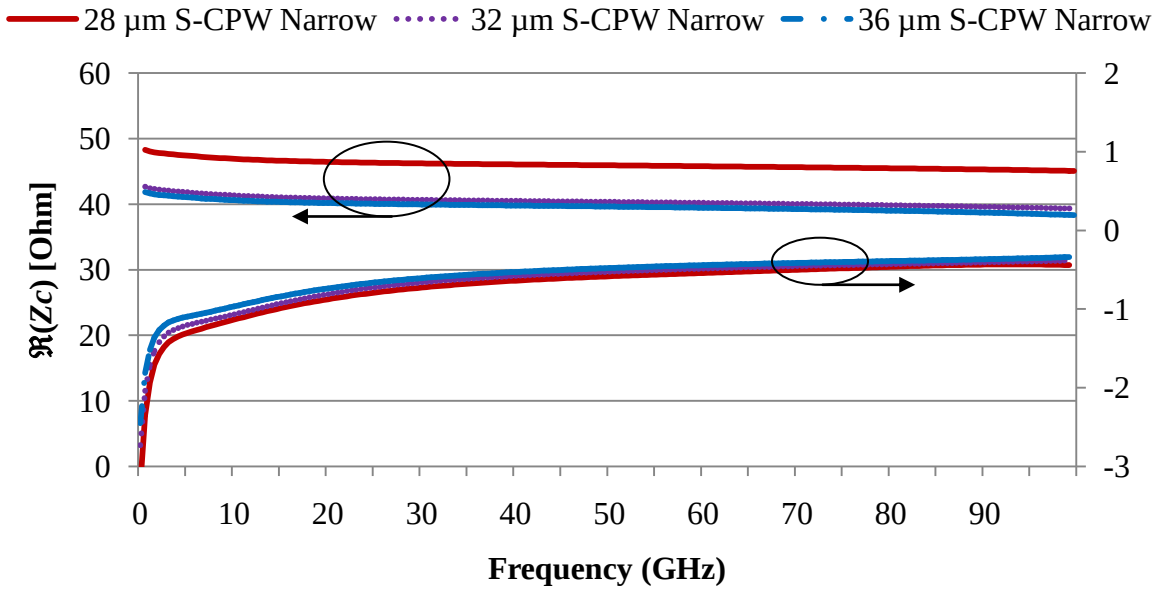

Figure 4.9. The real and imaginary characteristic impedance of the narrow S-CPW structures from 1 GHz to 100 GHz.

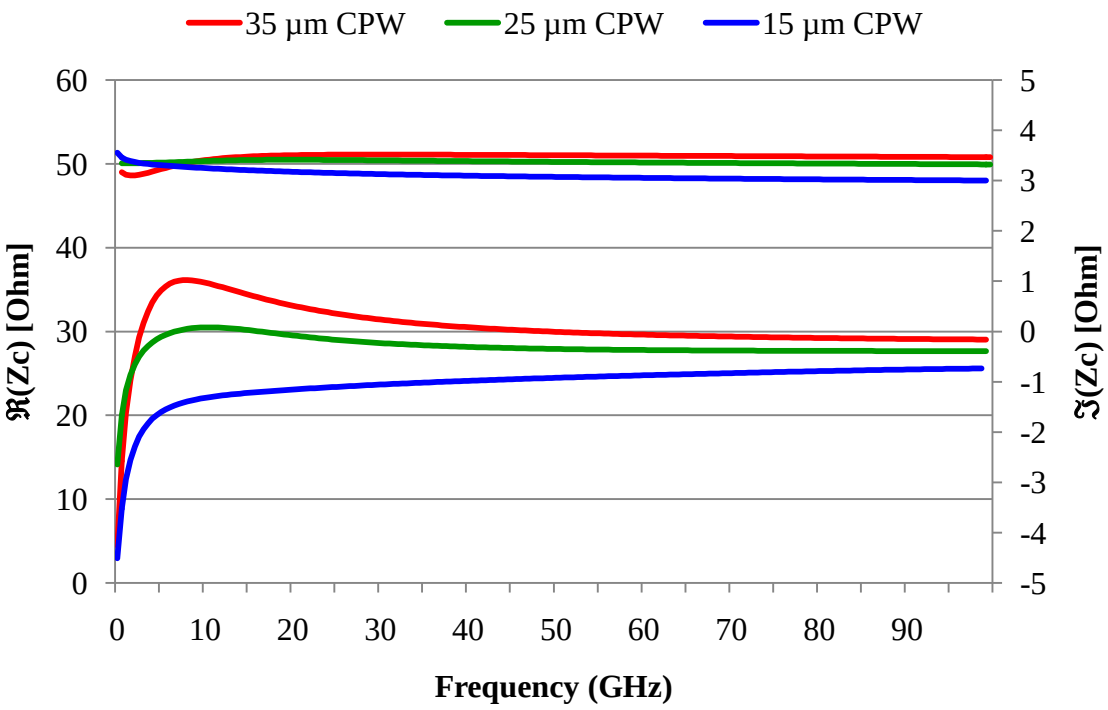

Figure 4.10. The real and imaginary characteristic impedance of the three CPW structures from 1 GHz to 100 GHz.

Two observations can be made when investigating the impedance variation with frequency. From Telegrapher's equation

$$Z_c^2 = \frac{(R'+j\omega L')}{(G'+j\omega C')} \tag{4.9}$$

$$= \left(\frac{R'G'+\omega^2 L'C'}{G'^2+(\omega C')^2}\right) + j\left(\frac{\omega L'G'-\omega R'C'}{G'^2+(\omega C')^2}\right) \tag{4.10}$$

the characteristic impedance is composed of a resistive and reactive component. When the reactive component is negative the structure is capacitive, and when the reactive component is positive the structure is inductive. Figure 4.10 shows that the two smaller CPW structures (the 15 µm and 25 µm CPW) remain capacitive over the entire frequency range but the largest CPW structure (the 35 µm CPW) becomes inductive at 3 GHz and turns capacitive again at 65 GHz.

With the addition of the metallic shield, a significant capacitance is added to the S-CPW structures which are also reflected in the reactive part of the characteristic impedances of Figure 4.8 and Figure 4.9. The other observation is the wide S-CPW structures of Figure 4.8 approach their resonant frequency. Extraction of the RLGC parameters of these wide S-CPWs reveals that the series resistance and the shunt conductance is respectively

decreasing and increasing rapidly as the resonant frequency is approached. For the largest S-CPW structure (the 36 µm S-CPW Wide) the series resistance becomes negative beyond 90 GHz. This is graphically illustrated in Figure 4.11.

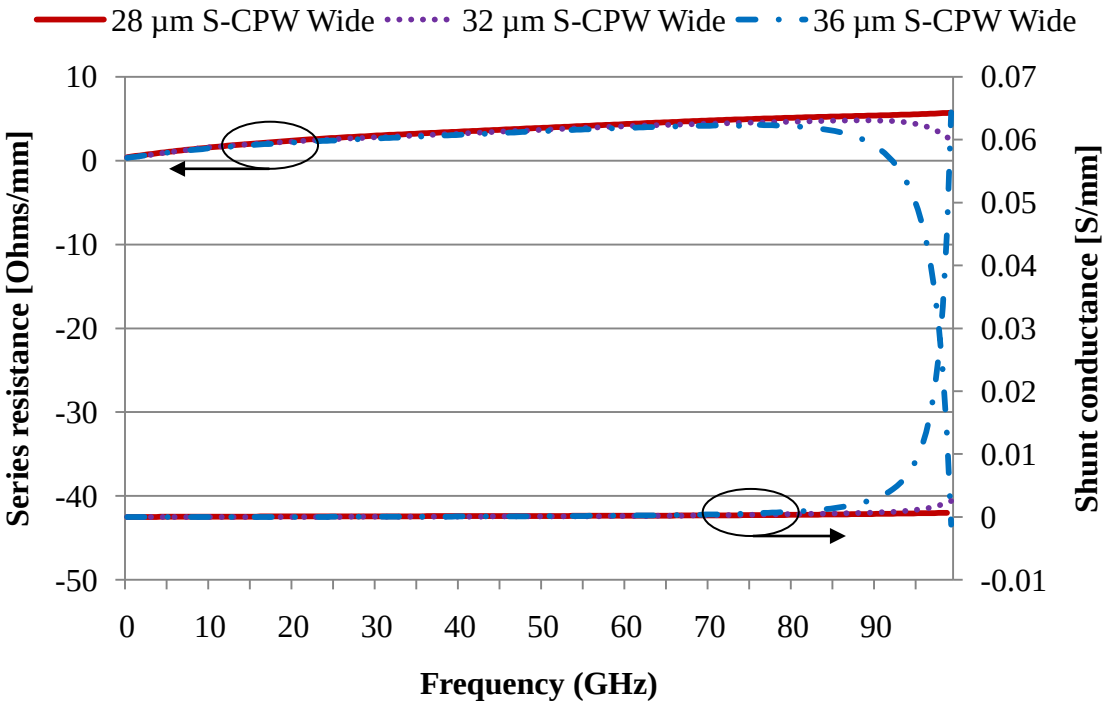

Figure 4.11. The series resistance and shunt conductance of the wide S-CPW structures over frequency.

The attenuation constant for all the structures is shown in Figure 4.12. The CPW structures experience at least 0.2 dB/mm more attenuation than the S-CPW structures. As the characteristic impedance of Figure 4.8 shows and the extracted RLCG parameters of Figure 4.11 suggest, the wide S-CPW structures experience larger attenuation constants as the frequency increases.

In Figure 4.13, the phase constant for all the structures is simulated. The figure shows a highly linear behaviour for all the structures. It is evident that the CPW structures achieves the lowest phase constant and that no matter the geometry, they all achieve roughly the same phase constant. With the metallic shield applied to a CPW structure a significant increase in phase constant is noticeable. The wide S-CPW structures achieve the highest phase constant with almost a factor 2 higher than the CPW structures.

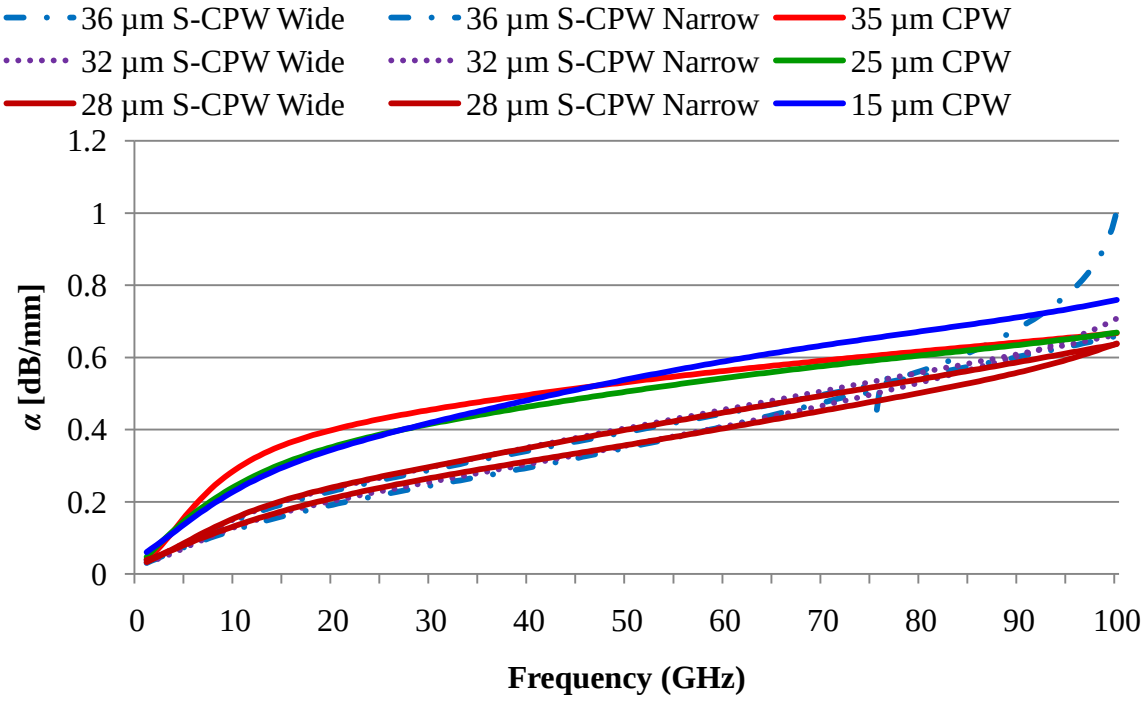

Figure 4.12. The simulated attenuation constant for all the transmission line structures is shown over frequency.

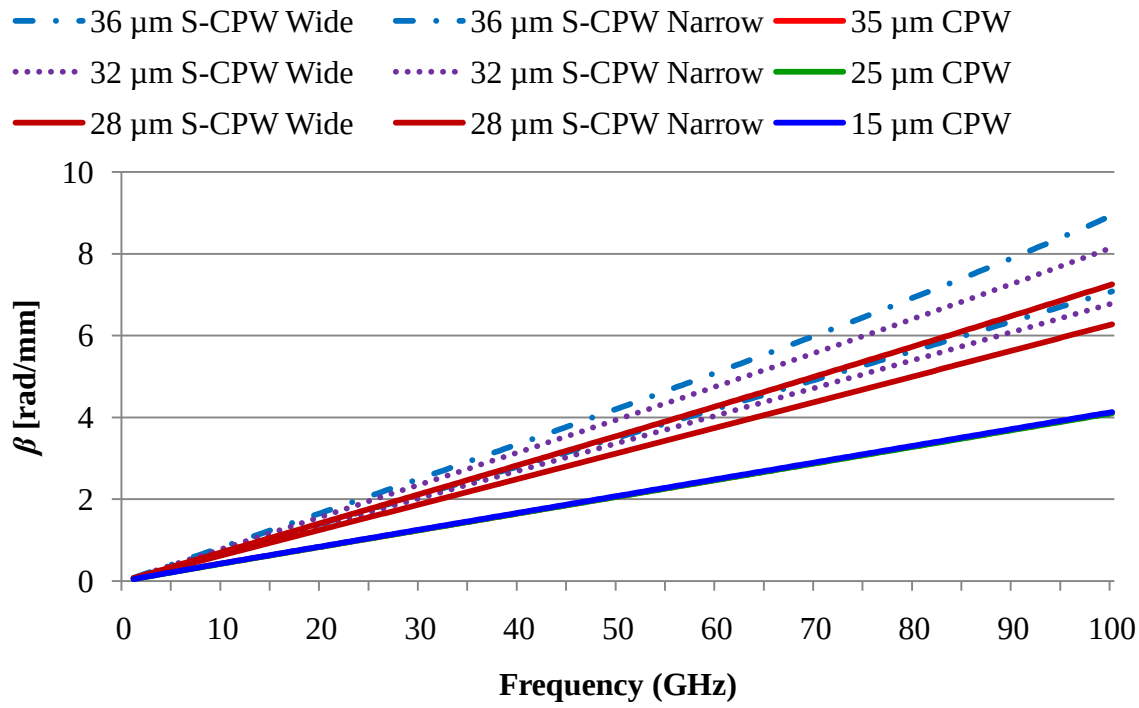

Figure 4.13. The simulated phase constant for all the structures over frequency.

Using the same definition previously used, the *Q*-factor for these structures can be calculated. The *Q*-factor for all the structures is shown in Figure 4.14. It is evident that the

wider S-CPWs achieve the highest *Q*-factors mostly due to their higher phase constants. There is a limitation as demonstrated by the 36 µm S-CPW Wide. Although it experiences a very high phase constant, the attenuation increases rapidly with frequency thereby decreasing the *Q*-factor.

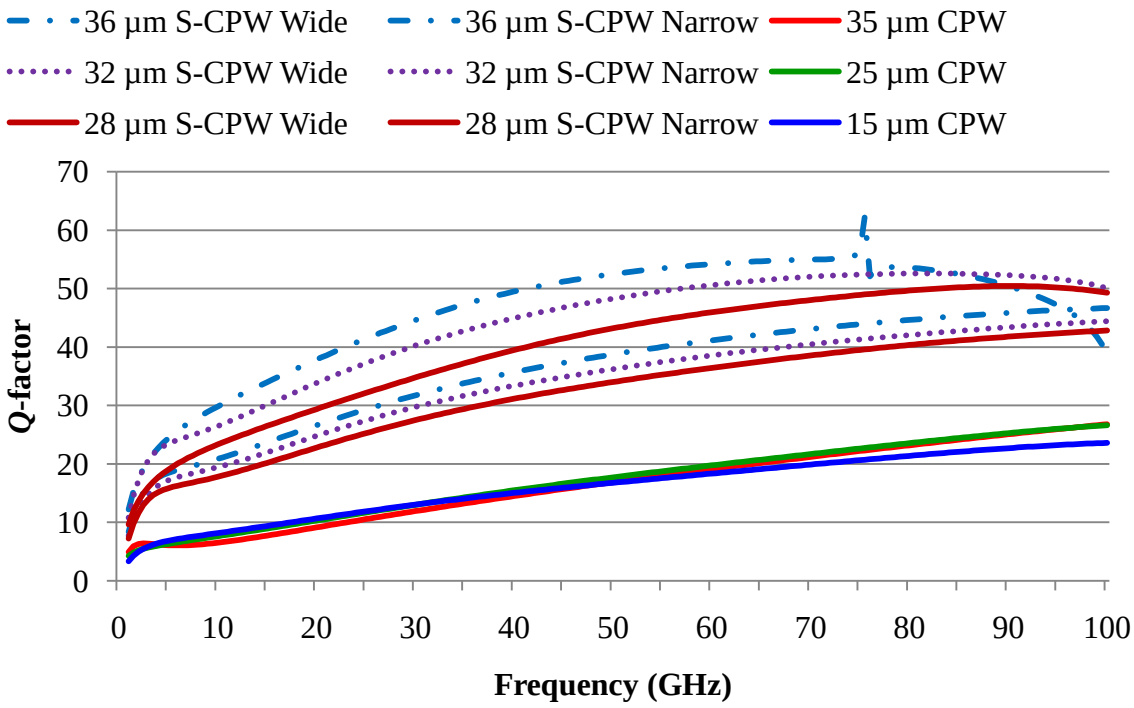

Figure 4.14. The *Q*-factor of all the structures over frequency.

The CPWs are grouped at the bottom of Figure 4.14. For the geometry parameters chosen in Table 4.1 and Table 4.3, the presence of the metallic shield improves the *Q*-factors by a factor of 2 over conventional CPWs.

4.7 ELECTRIC FIELD DISTRIBUTION

To visualise the coupling of the electric fields to the substrate and surrounding dielectric material and the difference the metallic shield induces, the total electric field distribution is analysed for the CPW and S-CPW structures at two geometric points. With the S-CPW geometry layout as shown in Figure 4.15, the total electric field is simulated at 60 GHz where a segment is made at X = 0 µm and X = 5 µm. The significance of these two sections is that at X = 0 µm, a metallic strip is directly below the three signal conductors and at X = 5 µm, no shielding strip is below the conductors. For the CPW structures, the electric fields are only analysed at X = 0 µm since no shield is present. Figure 4.16 shows the total electric field for the 25 µm CPW. The figure illustrates just how much of the electric field

penetrates the substrate. Regions of red show a very high electric field concentration while blue areas indicate a very low electric field concentration. Because of the small signal-to-ground spacing of the CPW structures, most of the electric field is confined between the signal conductors, but a large portion couples to the substrate which is the reason for their poor performance at very high frequencies.

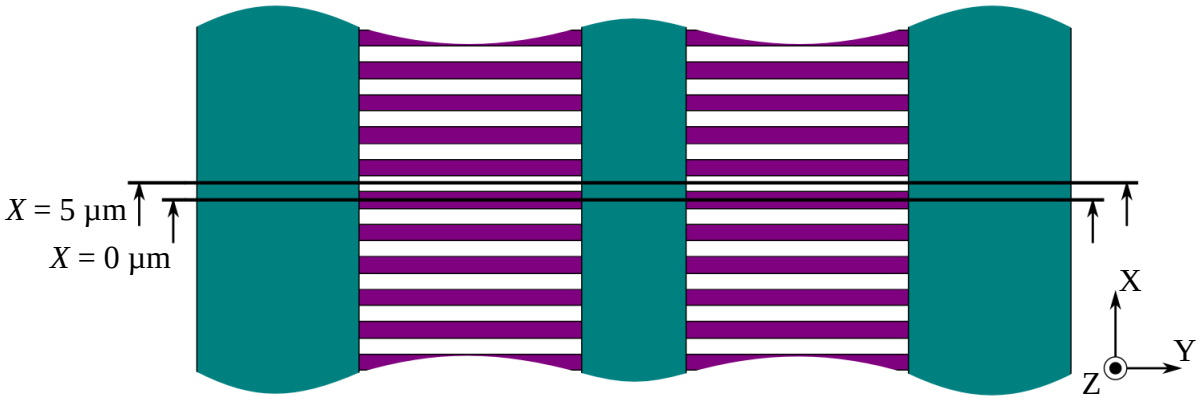

Figure 4.15. A section of S-CPW illustrating where the total electric field is simulated. The coordinate axial system is also shown.

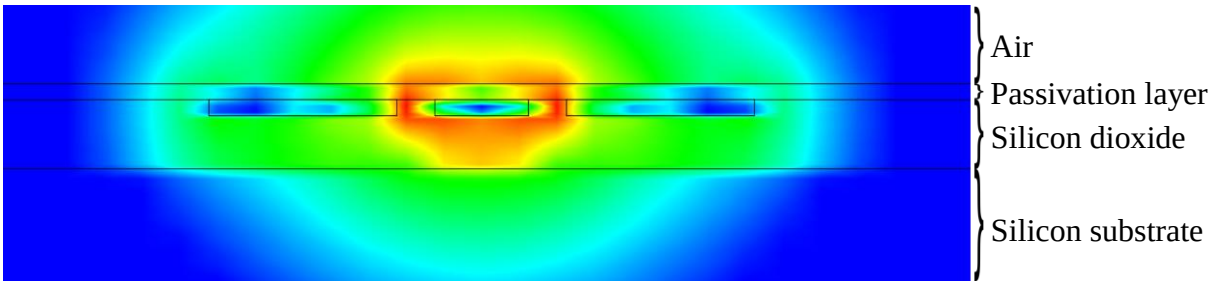

Figure 4.16. The total electric field distribution of the 25 µm CPW at X = 0 µm is shown including the surrounding dielectric material at 60 GHz.

Figure 4.17 shows the total electric field distribution of the 32 µm S-CPW Narrow at X = 0 µm. With the presence of the metallic shield, a significant difference in electric field distribution is observed compared to Figure 4.16. The first is that the electric field does not couple so strongly between the signal and ground conductors. Instead, the electric field from the signal conductor couples to the metallic shield which in turn couples to the ground conductors. Secondly, a significant decrease in electric field coupling to the substrate is found. From simulation and visually this proves that the metallic shield do prohibit the electric field from penetrating the substrate.

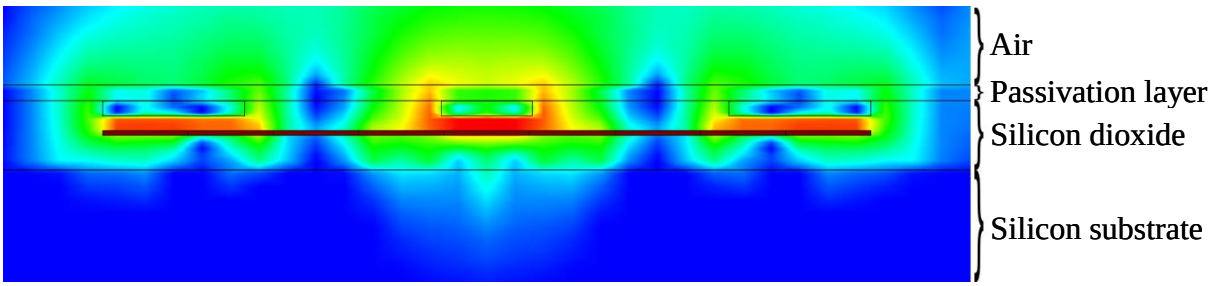

Figure 4.17. The total electric field distribution of the 32 µm S-CPW Narrow at X = 0 µm is shown including the surrounding dielectric material at 60 GHz.

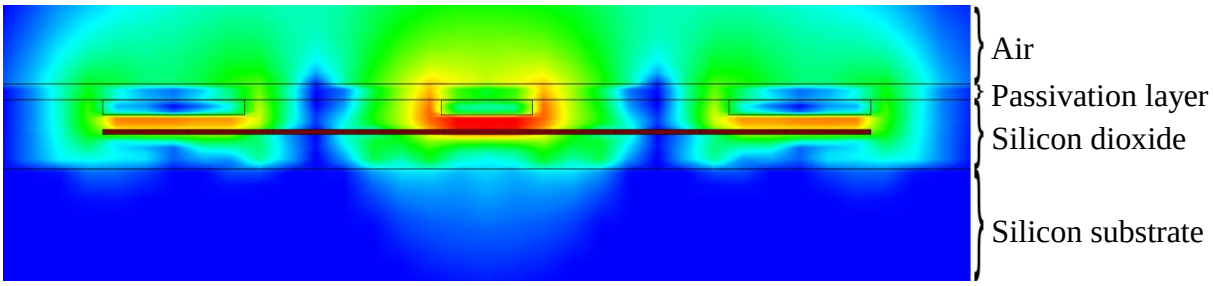

Figure 4.18. The total electric field distribution of the 32 µm S-CPW Narrow at X = 5 µm is shown including the surrounding dielectric material at 60 GHz.

Figure 4.17 is a section through X = 0 µm which has a shield strip directly beneath the CPW conductors. Figure 4.18 shows that even when a section is made through X = 5 µm, right between the shield strips, significant less electric field penetration occurs. There is no significant difference found between Figure 4.17 and Figure 4.18. This result justifies the shield strip width and spacing chosen in section 4.4.

4.8 CONCLUSION

With the two types of simulations conducted on the geometry parameters of Table 4.1, and following the simulation results the 32 µm S-CPW was chosen as the preferred S-CPW geometry. As will be discussed in chapter 5, both the narrow and the wide geometries will be used to design the LNA in order to compare the performance difference of the LNAs.

The 32 µm S-CPW was chosen because the wide geometry reaches its peak Q-factor at 60 GHz and does not exhibit the characteristics of the 36 µm S-CPW approaching its resonant frequency. The 28 µm S-CPW is more suitable at higher frequencies as it reaches its peak Q-factor above 80 GHz. The 32 µm S-CPW is therefore the preferred choice concerning geometry, size and frequency and has been optimised with respect to the signal-to-ground spacing.

CHAPTER 5: AMPLIFIER DESIGN AND SIMULATION

5.1 INTRODUCTION

The LNA is a critical component in receiver architectures and presents a considerable challenge for its simultaneous requirement to achieve high gain, low noise, and excellent input and output matching, unconditional stability and low power consumption. The problem becomes more severe with the limited active device performance and parasitic substrate loss associated at these high frequencies.

In the mm-wave regime the parasitic capacitance and resistance of devices worsen due to the high frequencies and as such, even the active device layout must be considered to find any performance enhancement. The IBM SiGe BiCMOS 8HP technology has two transistor layout variants i.e., the collector-base-emitter (CBE) and collector-base-emitter-base-collector (CBEBC). The CBE configuration is not the preferred transistor layout for LNA design due to its higher base resistance compared to the CBEBC layout. Furthermore, the CBEBC layout has a higher f_T and f_{max} than the CBE layout which is attributed to the reduction in the collector resistance and the symmetric spread of injected electrons into the collector. The CBEBC layout delays the onset of the Kirk effect which is responsible for a rapid increase in the forward charging time and a resultant decrease in f_T [**64**]. The CBEBC layout will therefore be preferred in the design of the LNA compared to the CBE configuration.

The circuit topology is also a crucial consideration as it determines the minimum and maximum performance boundaries and the consequential tradeoffs in order to realise the LNA at mm-wave frequencies. The cascode configuration is chosen based on its ability to address the two most important concepts in LNA design: suppression of the Miller effect and a high current gain to reduce the output noise referred to the input [**65**]. As a consequence, the cascode is the preferred LNA topology when compared to single transistor configurations with additional advantages which includes increased gain and improved stability due to its high reverse isolation characteristic. Two disadvantages are the higher voltage headroom that is required due to the stacked transistors and the reduction in linearity due to the reduced output swing.

5.2 AMPLIFIER DESIGN

The 1.2 V supply voltage specified by the IBM SiGe BiCMOS 8HP process is not sufficient voltage headroom for the cascode topology. The supply voltage must be adjusted to ensure the correct operating region of the stacked transistors. As will be shown in section 5.2.1 the transistor operating point is calculated to realize a minimum NF. Consequently the supply voltage is chosen so the transistor has sufficient headroom before entering saturation or breakdown. A supply voltage of 1.5 V is therefore chosen. Several other important considerations are made in the biasing of the cascode stage. Firstly a base current I_B is used to bias transistor Q_1 at the required current density. The bias current is supplied through a choke (L_1). Transistor Q_2 is biased with resistor R_1 while C_1, C_2, C_3 and C_4 act as high frequency shorts. Inductor L_2 is another high frequency choke which supplies the cascode with a collector current. The cascode topology with the bias circuitry is shown in Figure 5.1.

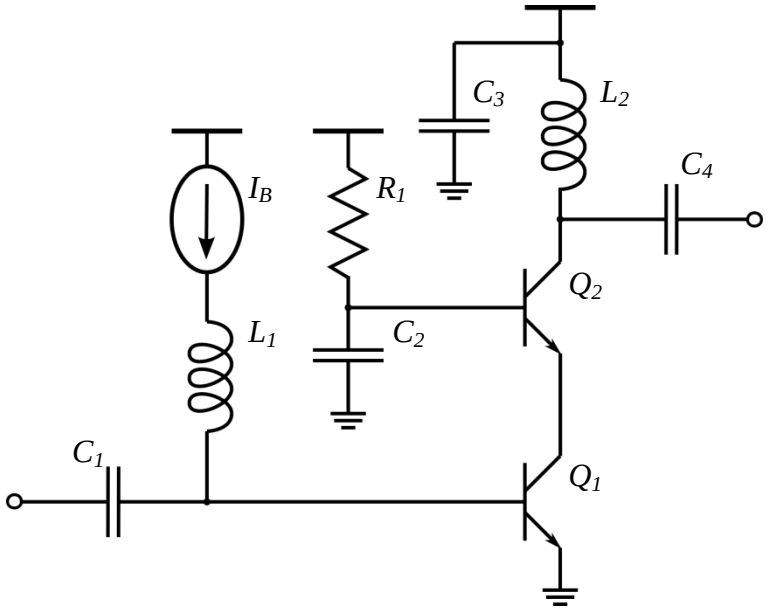

Figure 5.1. Biasing of the cascode LNA circuit.

Subsequently the transistor size and biasing current must be optimised to meet the gain, noise, and linearity requirements. The two important aspects in the design are the matching networks for minimum return loss, and noise matching to achieve the minimum NF. A simultaneous noise and power match is possible and is discussed in the following sections [**13**], [**34**].

5.2.1 Transistor sizing and biasing

For small signal operation, the NF of a transistor with a source driving impedance of $Z_s = R_s + jX_s$ is given by

$$NF = NF_{min} + \frac{1}{R_n R_s}\left|Z_s - Z_{s,opt}\right|^2. \quad (5.1)$$

where $Z_{s,opt} = R_{s,opt} + jX_{s,opt}$ is the optimum noise matching impedance. NF_{min}, $Z_{s,opt}$ and R_n are general functions of the biasing current, transistor size and frequency [**34**]. The definition of the source impedance in (5.1) is particularly important due to the parasitic effects associated with the on-chip components. Typically, a 50 Ω source impedance is used for measurements, with a measurement probe making contact with a bondpad connecting the LNA. At 60 GHz, the parallel plate and fringing capacitance of the bondpad is approximately 45 fF with respect to ground [**66**]. This capacitance is shunting the 50 Ω source resistance producing a source impedance equal to Z_s = 29 – j24.7 Ω. Therefore, to achieve NF = NF_{min}, $Z_{s,opt}$ must be transformed to Z_s as illustrated in (5.1). To achieve maximum power transfer, Z_{in} must be transformed to the complex conjugate of Z_s.

The input matching network can be simplified by adjusting the SiGe HBT emitter length so that $R_{s,opt}$ is equal to 50 Ω. Consequently, the matching network only needs to cancel the parasitic capacitance of the bondpad and transform the input impedance of the transistor to the complex conjugate of Z_s.

To obtain a NF_{min} where $R_{s,opt}$ is equal to 50 Ω at a specific biasing condition, several transistor parameters are required for the calculation. These transistor parameters are given in the IBM SiGe BiCMOS 8HP documentation provided in [**67**] for different transistor sizes and biasing currents. These parameters can be used to obtain $R_{s,opt}$ and NF_{min} which is approximated by [**13**]

$$R_{s,opt} = \frac{R_n f_T}{f}\frac{\sqrt{\frac{I_C}{2V_T}(r_E + r_B)\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\left(\frac{f_T^2}{4\beta_0 f^2}\right)}}{\frac{I_C}{2V_T}(r_E + r_B)\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{1}{4}\left(1+\frac{f_T^2}{\beta_0 f^2}\right)}, \quad (5.2)$$

$$NF_{min} = 1 + \frac{1}{\beta_0} + \frac{f}{f_T}\sqrt{\frac{2I_C}{V_T}(r_E + r_B)\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{f_T^2}{\beta_0 f^2}}, \quad (5.3)$$

where f_T is the transition frequency, f is the frequency of operation, V_T is the threshold voltage, β_0 is the current gain, and r_E and r_B is the emitter and base resistances, respectively. The parameters provided in [**67**] and used in (5.2) and (5.3) cannot be provided due to the NDA.

The other parameters required is the frequency of operation, *f*, which is equal to 60 GHz and β_0 which is assumed to be 300 and constant over the emitter length and collector current range. The assumption that β_0 remains constant is validated in Section 2.2.3 where it was proven that NF_{min} is largely independent of β_0 if the frequency of operation is larger than $f_T/\sqrt{\beta}$ [**25**], [**27**]. $R_{s,opt}$ and NF_{min} is calculated using (5.2) and (5.3) and equates to the values in Table 5.1 and Table 5.2.

Table 5.1. $R_{s,opt}$ (Ω) calculated at various emitter lengths and collector currents

Collector current (mA)	**Emitter Length**			
	3 µm	**6 µm**	**12 µm**	**18 µm**
1 mA	92.5	29.58	6.44	2.23
4 mA	177.1	80.72	28.65	12.50
8 mA	123.3	95.97	42.20	20.98
12 mA	4.76	19.52	38.57	29.68

Table 5.2. NF_{min} (dB) calculated at various emitter lengths and collector currents

Collector current (mA)	**Emitter Length**			
	3 µm	**6 µm**	**12 µm**	**18 µm**
1 mA	1.93	2.8	3.97	4.89
4 mA	1.65	2.01	2.33	2.58
8 mA	1.8	1.91	2.05	2.18
12 mA	5.23	3.24	2.11	1.95

Correlation of Table 5.1 and Table 5.2 results in a rough estimate of the attainable NF_{min} and its accompanying $R_{s,opt}$, at a specific biasing current and transistor emitter length. Inspection shows that the desired performance is achieved by choosing an emitter length of 12 µm, with an 8 mA collector current. The chosen emitter length results in the lowest possible NF_{min} with $R_{s,opt}$ very close to 50 Ω.

5.2.2 Input matching network

With $R_{s,opt}$ close to 50 Ω and the transistors biased to achieve a low NF_{min}, the input matching network only needs to cancel the parasitic bondpad capacitance and transform the input impedance to Z_s^* where Z_s^* denotes the complex conjugate of Z_s. Looking into the base of transistor Q_1 in Figure 5.1, the input impedance is given by

$$Z_{in} = r_B + \frac{1}{j\omega C_{be}} = 13.7 - j10.7\ \Omega. \tag{5.4}$$

The input impedance is mainly capacitive with a small real component determined by the base resistance. A technique to increase the real part of the input impedance is to add an emitter inductor, L_E as shown in Figure 5.2.

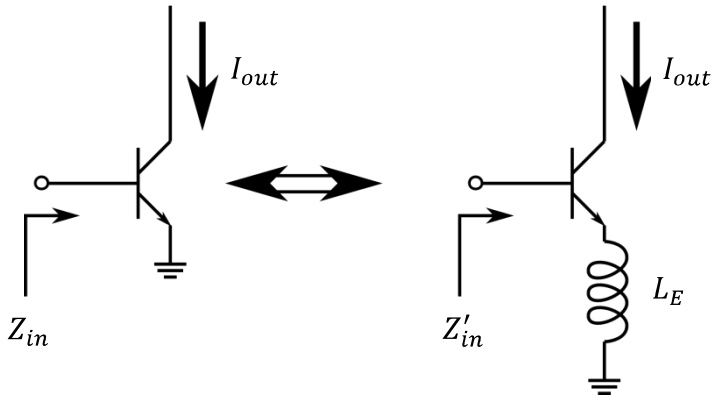

Figure 5.2. Inclusion of the emitter inductor to modify Z_{in}'.

The impedance looking into the base of the transistor with the emitter inductor, changes to

$$Z'_{in} = r_B + \frac{1}{j\omega C_{be}} + (1 + \beta)j\omega L_E \tag{5.5}$$

The prime sign indicates the new input impedance. The AC current gain, β is a function of frequency as described in [**68**]. β will roll off by 10 dB/decade at the corner frequency

$$\omega_\beta = \frac{2\pi f_T}{\beta_0} \cong 4\ \text{GHz}, \tag{5.6}$$

where β_0 is the low frequency AC current gain approximately. With the frequency of operation higher than ω_β, the value of β can be determined by

$$\beta = -j\frac{\omega_T}{\omega}. \tag{5.7}$$

By substituting (5.7) into (5.5), the input impedance can be rewritten as

$$Z'_{in} = r_B + \frac{1}{j\omega C_{be}} + j\omega L_E + \omega_T L_E. \tag{5.8}$$

Equation (5.8) shows that a resistive component, $\omega_T L_E$ and imaginary component, $j\omega L_E$ is produced where L_E can be altered to adjust the input impedance. L_E can be approximated by letting $\Re\{Z_{in}'\} = \Re\{Z_s\} = 29\ \Omega$

$$L_E = \frac{29\,\Omega - r_B}{2\pi f_T} = 14\ \text{pH}. \tag{5.9}$$

The change in input impedance is graphically illustrated using a Smith Chart shown in Figure 5.3. Using a normalisation impedance of 50 Ω, z_{in} is equal to (0.27 – j0.21) and changes with the inclusion of L_E to z_{in}' = (0.58 – j0.4). Subsequently, the imaginary part of Z_{in}' is matched with the inclusion of a base inductor, L_B such that $\Im\{Z_{in}'\} = -\omega L_B - \Im\{Z_s^*\}$

$$L_B = \frac{1}{\omega^2 C_{be}} + L_E + \frac{24.5}{\omega} = 118 \text{ pH}. \tag{5.10}$$

In Figure 5.3, z_{in}' moves to z_s^* equal to (0.58 + j0.49). Both the input resistance and reactance are now conjugate matched to the source driving impedance. The last movement on the Smith Chart indicated by a thick patterned line, is the shunt parasitic capacitance of the bondpad which will result in the 50 Ω system impedance. It is interesting to note that the inclusion of L_E does not affect $R_{s,opt}$ nor NF_{min} but does change $X_{s,opt}$ [**34**]. The new $X_{s,opt}$ is given by

$$X_{s,opt}' = \frac{1}{\omega C_{be}} + \omega L_E + 24.5\ \Omega = \text{j}18.15\ \Omega. \tag{5.11}$$

This movement is shown on the Smith Chart in Figure 5.4, with $z_{s,opt}$ moving to $z'_{s,opt}$. The L_B required to noise match $X'_{s,opt}$ is given by

$$L_B = \frac{X_{s,opt}'}{\omega} = \frac{1}{\omega^2 C_{be}} + L_E + \frac{24.5}{\omega}, \tag{5.12}$$

which is identical to the L_B required for impedance matching in (5.10). With the inclusion of L_B, $z'_{s,opt}$ moves to z_s. A simultaneous input impedance and noise match is achieved. The resulting circuit is shown in Figure 5.5.

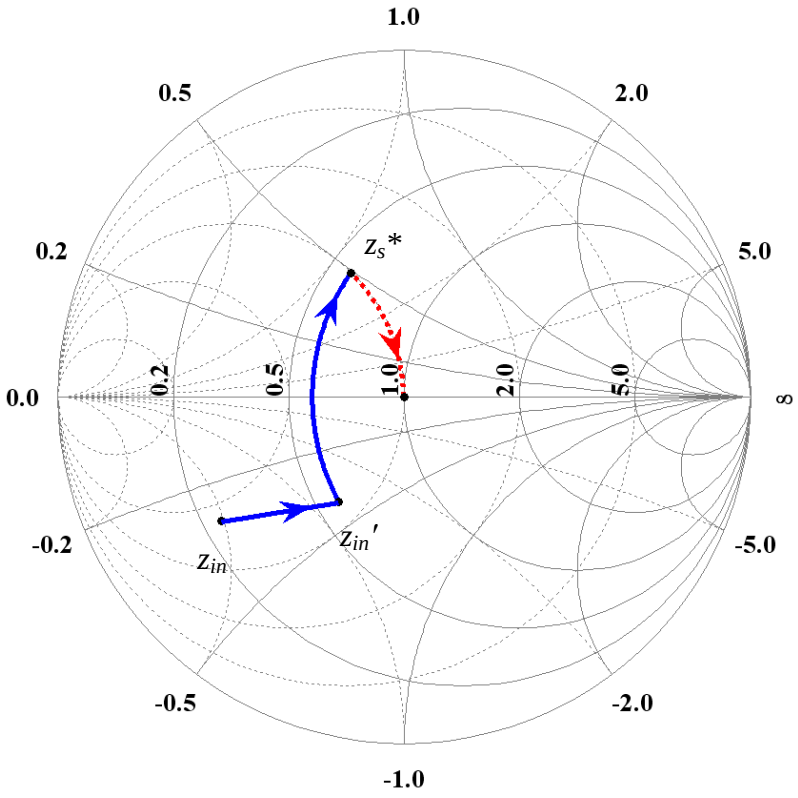

Figure 5.3. Smith Chart showing the input impedance transformation.

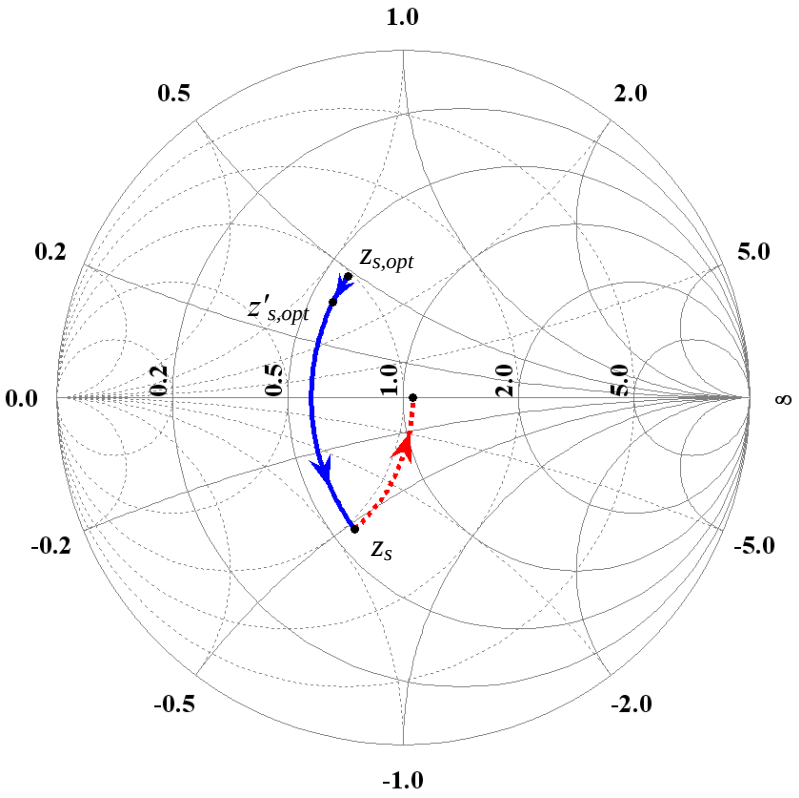

Figure 5.4. Smith Chart showing the optimum source impedance transformation.

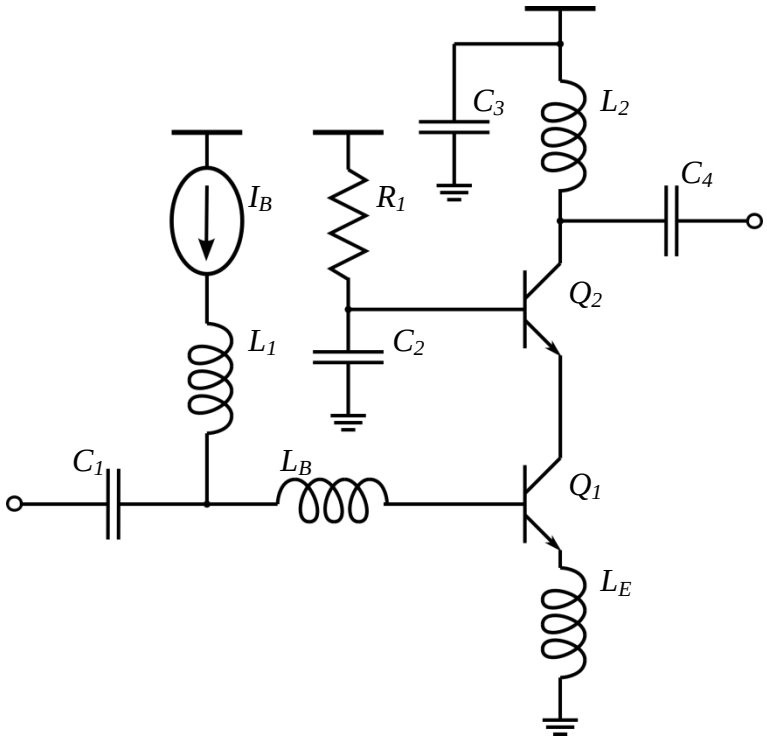

Figure 5.5. Cascode LNA with the biasing and input matching network.

5.2.3 Output matching network

The output matching network follows classical matching network theory where the output impedance of the transistor is transformed to the complex conjugate of the load impedance,

Z_L^*. The output matching network is designed by first estimating the output impedance of the LNA cascode of Figure 5.1 when looking into the collector of Q_2, which is approximated by [**69**]

$$Z_{out} \cong \frac{r_B}{1+g_m r_B} + \frac{1}{j\omega C_{bc}(1+g_m r_B)} = 2.5 - j51.4\ \Omega. \tag{5.13}$$

The output impedance is mainly capacitive with an extremely low output resistance. Z_{out} can be matched to Z_L^* using a three element matching network consisting of two inductors and a capacitor. Z_{out} is normalised and placed on the Smith Chart shown in Figure 5.6.

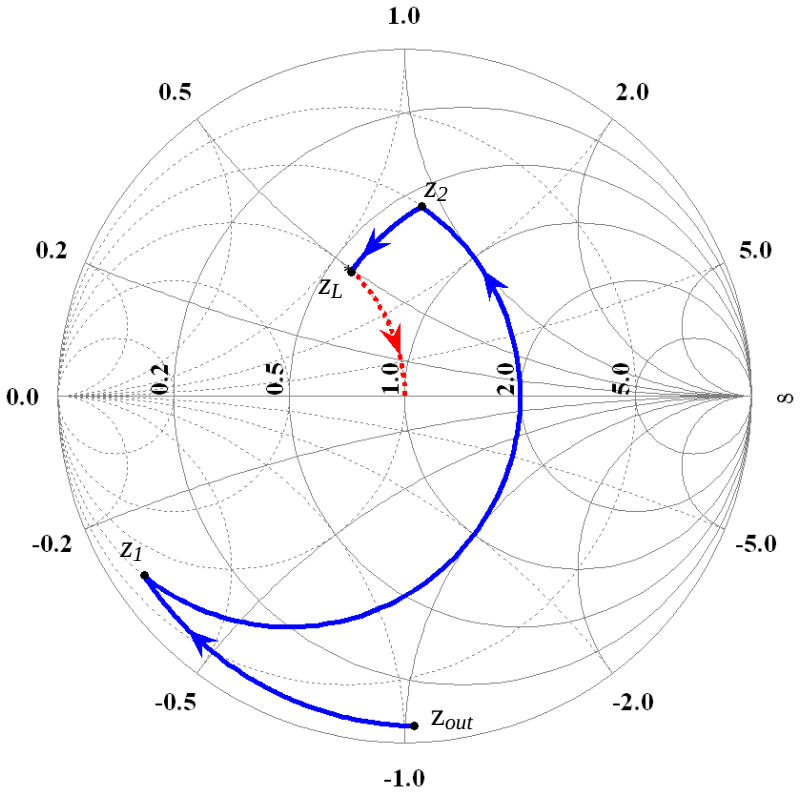

Figure 5.6. Smith Chart showing the output impedance transformation.

Other matching network topologies such as a multi component matching networks extending to more than three elements, or quarter-wave transmission line stubs can be used in contrast to the proposed three element matching network. The alternatives to the three element matching network would theoretically produce higher matching network *Q*-factors [**70**], however these matching networks tend to be large, consuming significant Si area. The three element matching network is sufficient to produce a higher performance LNA and to determine the outcome of the hypothesis.

The movement from Z_{out} to Z_1 is the impedance added by the series inductor L_S at the collector output. The inductor is calculated by

$$L_s = \frac{0.69(50)}{2\pi(60\times10^9)} = 91 \text{ pF} \tag{5.14}$$

The shunt inductor L_P moves from Z_1 to Z_2 on the constant conductance circle and is equated by

$$L_P = \frac{0.27(50)}{2\pi(60\times10^9)} = 35 \text{ pH.} \tag{5.15}$$

A series capacitor is responsible for the impedance movement from Z_2 to Z_L^*. The capacitance is equal to

$$C_O = \frac{1}{2\pi(60\times10^9)(0.42)(50)} = 126 \text{ fF} \tag{5.16}$$

The last movement on Figure 5.6 indicated by the thick patterned line, is the shunt parasitic capacitance of the bondpad which will result in the 50 Ω output impedance. The cascode LNA with the biasing network and input and output matching network is shown in Figure 5.7.

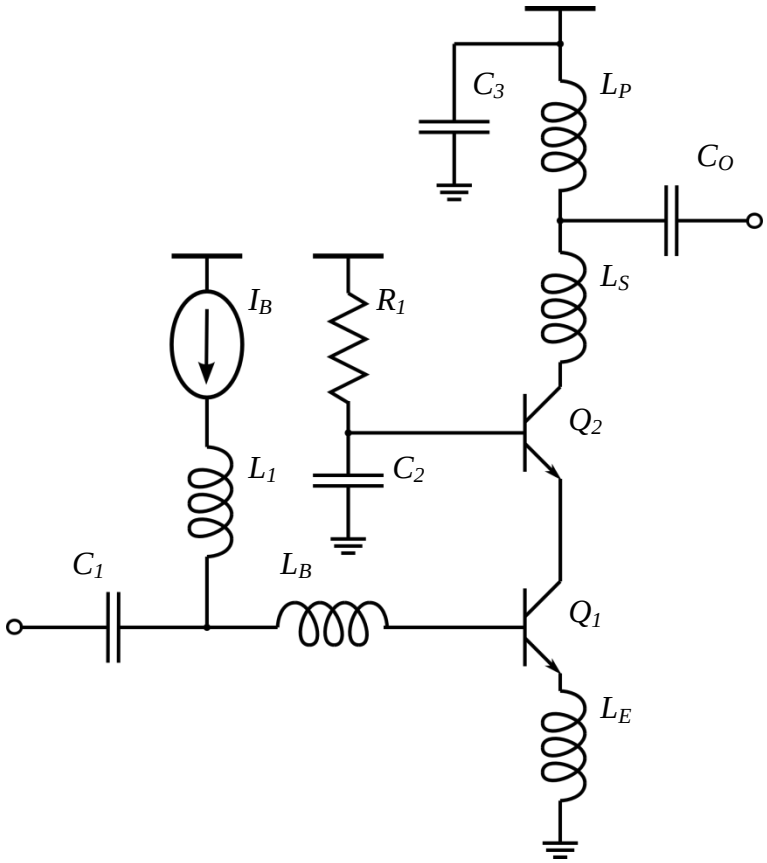

Figure 5.7. Cascode LNA with the biasing and input and output matching network.

5.2.4 Optimised LNA with S-CPW lines

The LNA design is finalised by verifying the calculated results using Cadence Virtuoso. At first, the transistor size and biasing current of section 5.2.1 is adjusted until the optimum

result is achieved. Table 5.3 shows the calculated transistor emitter length and collector current and the final value chosen through optimisation. The difference in the calculated $R_{s,opt}$ and NF_{min} and the end result is also shown.

Table 5.3. Calculated and simulated transistor parameters and biasing current

Summary	Calculated	Simulated
Emitter length	12 µm	15 µm
Collector current (I_C)	8 mA	4 mA
$R_{s,opt}$	42.2 Ω	48.1 Ω
NF_{min}	2.05 dB	3.8 dB
Z_{in}	$13.7 - j10.7$ Ω	$5.9 - j12.9$ Ω
Z_{out}	$2.5 - j51.4$ Ω	$1.1 - j36.3$ Ω

Table 5.4. Calculated and simulated passive component values

Summary	Calculated	Recalculated
L_S	91 pH	55 pH
L_B	118 pH	122 pH
L_E	14 pH	23 pH
L_P	35 pH	35 pH
C_O	126 fF	126 fF

Table 5.3 shows that after optimisation the lowest NF_{min} with $R_{s,opt}$ close to 50 Ω is achieved with a lower collector current and longer emitter length than the calculated values. The simulated NF_{min} of 3.8 dB is also roughly 2 dB higher than the calculated value, even though the optimised collector current and base resistance has decreased, demonstrating that (5.3) largely underestimates the NF_{min} at mm-wave frequencies. Table 5.4 shows the new calculated passive component values after optimisation. A small discrepancy is found between the new and previously calculated values due to the small difference in the calculated and simulated input and output impedances of Table 5.3.

Next the ideal inductors of the input and output matching networks of Figure 5.7 must be replaced with the S-CPW transmission lines discussed in section 4.4 in chapter 4. Chapter 4 concluded that the 32 µm S-CPW is the preferred structure concerning overall performance for the chosen transmission line parameters. Two differently sized 32 µm S-CPW transmission lines were demonstrated, each with a different signal-to-ground spacing. To investigate whether optimisation of the S-CPW geometry improves the performance of LNAs, two LNAs will be designed. The first LNA will only consist of 32 µm S-CPW Narrow transmission lines and will be denoted as LNA 1. The second LNA will be identical to the first LNA but replaces only one inductor (L_S) with the 32 µm S-CPW Wide to observe any performance improvements and will be denoted as LNA 2. Justification for substituting only the one inductor, L_S, is due to the complex relationship of the input matching network simultaneously realising a noise and input power match. Additionally, inductor L_P in the output matching network is much smaller than inductor L_S, so the effect of a Q-factor improvement in L_S would be more profound. To incorporate the S-CPW in the schematic of Figure 5.7, it must be characterised as an equivalent circuit to include the parasitic losses. In section 4.2 the equivalent model of the S-CPW transmission line was discussed.

Figure 5.7 shows that inductors L_E and L_P have one terminal connected to AC ground and do therefore not require a full two-port representative model. Inductors L_E and L_P will instead be characterised by a one-port model. The 32 µm S-CPW transmission lines must be sized accordingly to attain the required inductance value. The transmission line length must be selected to achieve the required effective inductance. With the inclusion of the parasitic effects in the equivalent circuits of the S-CPW transmission lines, the input and output matching networks are further optimised in Cadence Virtuoso. Table 5.5 shows the calculated inductance values of Figure 5.7, the optimised S-CPW transmission line length and its geometry type, followed by the equivalent circuit parameters for each inductor given in Table 5.6.

Table 5.5. Calculated inductor geometry values.

Inductor	LNA	Calculated (pH)	S-CPW length (µm)	S-CPW type
L_S	1	55	220	Narrow
L_S	2	55	180	Wide
L_B	1, 2	122	180	Narrow
L_E	1, 2	23	120	Narrow
L_P	1, 2	35	80	Narrow

Table 5.6. Optimised S-CPW transmission line equivalent circuit parameters.

Inductor	L_{eff} (pH)	R_S (Ω)	R_{P1} (kΩ)	C_{P1} (fF)	R_{P2} (kΩ)	C_{P2} (fF)
L_S	84.7	0.67	38.5	31.3	38.5	31.3
L_S	94.7	0.55	56.9	25.6	56.9	25.6
L_B	72.3	0.59	66.6	24.7	66.6	24.7
L_E	56.1	0.53	-	-	-	-
L_P	36.0	0.32	-	-	-	-

Table 5.6 shows that inductor L_E and L_P are only represented by an equivalent one-port model and only includes an effective inductance and series resistance. The equivalent circuit parameters listed for all the inductors are extracted using IE3D and a strong correlation is found between the calculated values of section 5.2.2 and section 5.2.3 given in Table 5.4 and the extracted effective inductance values, L_{eff} in Table 5.6. A very small series resistance, R_S is also modelled and is directly proportional to the S-CPW line length and signal conductor width.

There are two different inductors L_S which is used in the respective LNA designs. Both inductors must represent the calculated inductance of 91 pH. Since L_S of LNA 1 is represented by the 32 µm S-CPW Narrow transmission line, the line length must be longer than the L_S used in LNA 2 which is represented by the 32 µm S-CPW Wide transmission line. This is reflected in Table 5.5 and is due to the difference in signal-to-ground spacing.

5.2.5 Simulation results

The two LNAs are simulated in Cadence Virtuoso ADE. The Virtuoso Spectre Circuit Simulator defines the LNAs as a generic two-port circuit. Spectre calculates the *s*-parameters using the circuit from which all other two-port parameters can be extracted. The simulation results presented in the following sections include the bondpad parasitic losses, the lumped equivalent circuit models of the inductors and the device models provided by the IBM foundry for the BiCMOS SiGe 8HP process [**67**].

5.2.5.1 *s*-parameter simulations

The *s*-parameters of both LNAs are shown in Figure 5.8 and Figure 5.9. The simulation is limited to a small frequency range around 60 GHz. Each S-CPW transmission line lumped equivalent model restricts the simulation to a 5 GHz bandwidth. Extending the simulation to a wider bandwidth will produce inaccurate and invalid results.

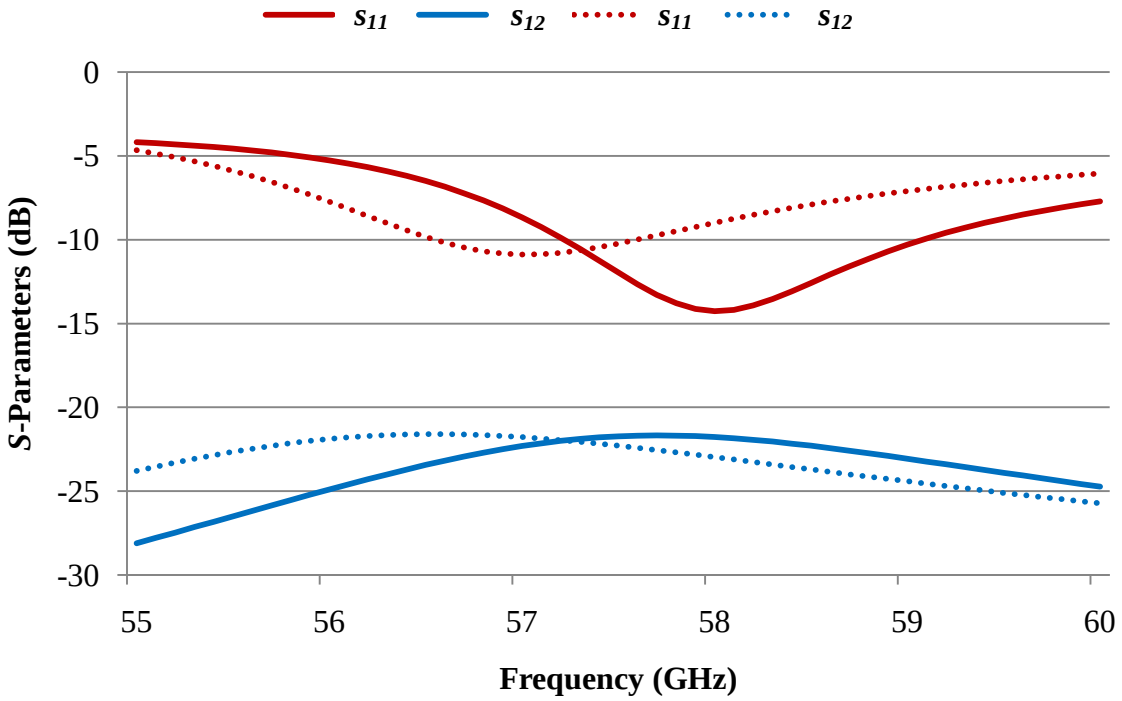

Figure 5.8. s_{11} and s_{12} parameters of LNA 1 and LNA 2 where the dotted and solid lines represent LNA 1 and LNA 2, respectively.

Figure 5.8 and Figure 5.9 show that both single stage LNAs achieve a gain of approximately 13 dB, with a reverse isolation better than -20 dB. The input reflection coefficient, s_{11} is less than -10 dB in both designs and s_{22} less than -20 dB. Unfortunately

the design frequency has shifted approximately 3 GHz to 57 GHz from the calculated results which are due to the parasitic effects of the inductors.

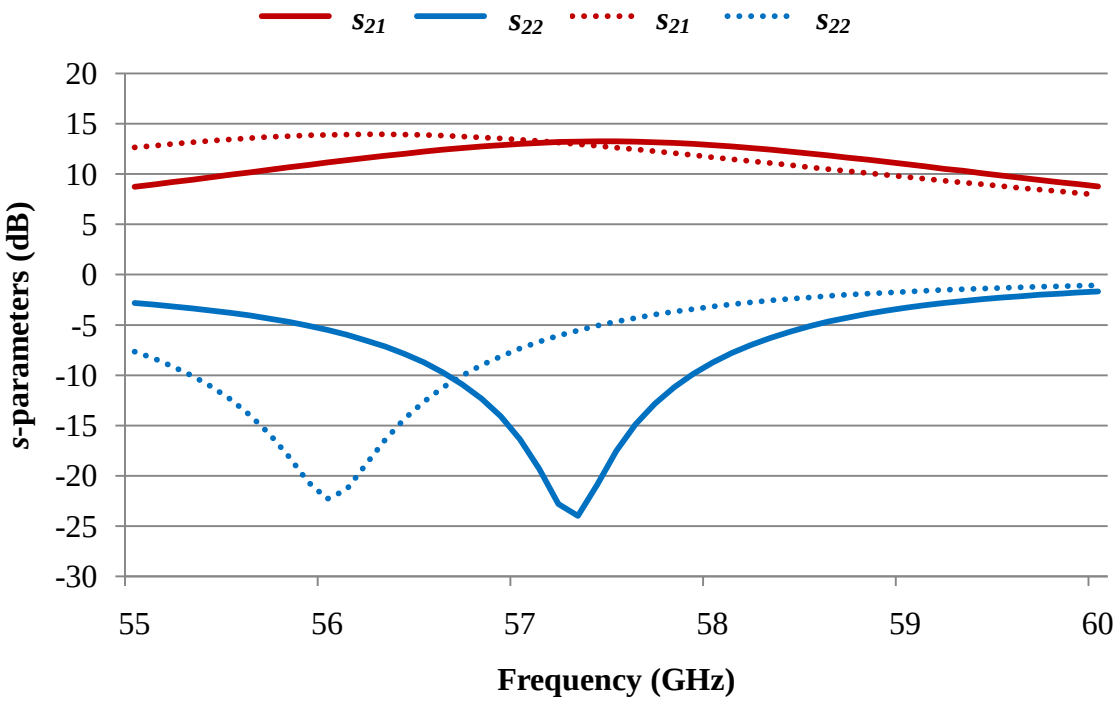

Figure 5.9. s_{21} and s_{22} parameters of LNA 1 and LNA 2 where the dotted and solid lines represent LNA 1 and LNA 2, respectively.

The most significant difference between the results of Figure 5.8 and Figure 5.9 is the s_{22} parameter. The s_{22} operation frequency of LNA 2 is shifted 600 MHz higher than the s_{22} parameter of LNA 1 and is due to the lower series resistance of the output matching network inductor, L_S. It is also apparent that a sharper response is noticeable which can only be attributed to the *Q*-factor difference of inductors L_S. There is also a slight difference in the s_{11} parameters. LNA 2 achieves a better input match although no change is made at the input of the LNAs. LNA 2 achieves a 5 dB input and output matching improvement over LNA 1. The bandwidth of the LNAs is calculated from the -3 dB cut-off points determined by the s_{21} parameter. The bandwidth of LNA 1 is 4.4 GHz and the addition of the higher *Q*-factor inductor in LNA 2 reduces the bandwidth to 3.6 GHz. As a consequence, the loaded *Q*-factor given by

$$Q_L = \frac{f_0}{BW}, \tag{5.17}$$

of LNA 2 improves from 13.6 to 16.7 over LNA 1.

5.2.5.2 Noise figure simulations

The noise performance of the LNAs are simulated and presented in Figure 5.10. The NF and NF_{min} are almost identical for both LNAs. The two LNAs have very similar noise performance. No significant difference exists between the two designs but a small discrepancy is found in the NF_{min} of approximately 0.1 dB. Apart from this difference, both LNAs achieve NF and NF_{min} of 5.3 dB and 4.1 dB at 57 GHz, respectively. The difference in the NF_{min} value presented in Figure 5.10 and that of Table 5.3 is due to the input and output matching networks improving the minimum attainable NF which is attributed to lower series inductor losses.

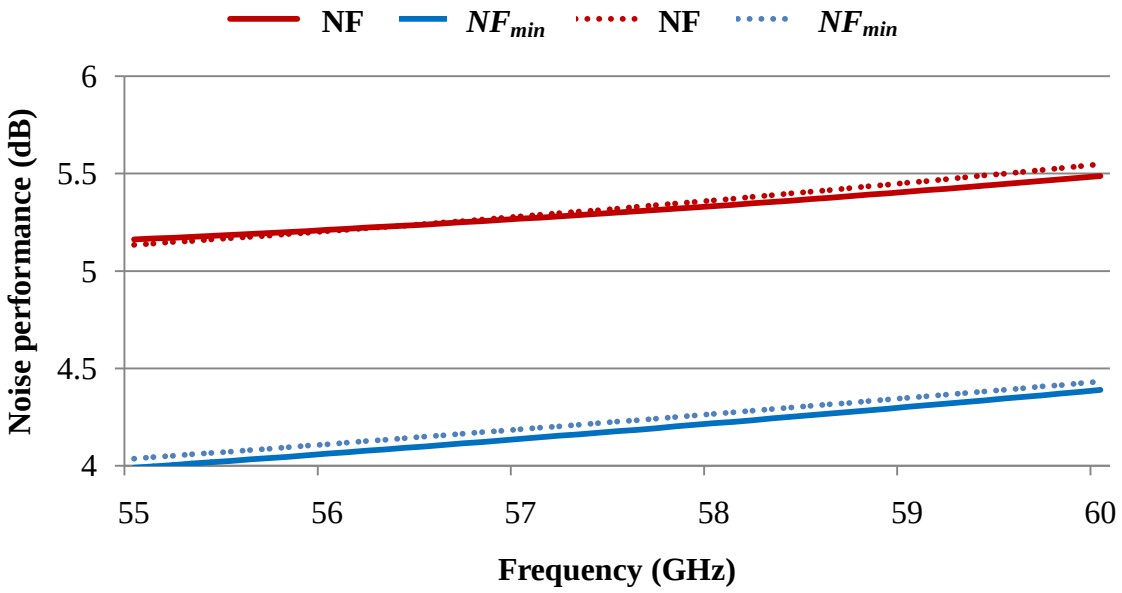

Figure 5.10. NF and NF_{min} of both LNAs where the dotted and solid lines represent LNA 1 and LNA 2, respectively.

SpectreRF allows investigation of the individual noise contributions within the LNA. Careful inspection shows the dominant noise contributor responsible for the LNA NF. A periodic steady state (PSS) analysis on both LNAs shows that the dominant noise contributors are the base resistances of both transistors. Table 5.7 shows the noise contributions of the individual transistors of each LNA. r_{bx}, r_{bi} and r_e denotes the extrinsic and intrinsic base resistance and emitter resistance of each transistor, respectively.

Table 5.7. Noise contribution within each transistor of the LNAs

Transistor parameters	LNA 1		LNA 2	
	Q1	***Q2***	***Q1***	***Q2***
r_{bx}	16.3 %	3.7 %	16.1 %	4.3 %
r_{bi}	4.1 %	1 %	4.6 %	1.3 %
r_e	1.6 %	0.7 %	1.6 %	0.8 %

The base resistance of transistor Q_1 in both LNAs is the largest contributor to the NF with a contribution of roughly 20 %. It is evident that the dominant noise contributor of the cascode LNA is transistor Q_1 since the noise contribution of the same noise sources in Q_2 is much smaller.

5.2.5.3 Stability factor

The stability of the LNA can be calculated by plotting the load and source stability circles on a Smith Chart. The boundary condition can be shown and the regions for unconditional stability can be expressed on the normalised impedance Smith Chart [**29**]. The load and source stability circles can be plotted by equating the coordinates of the circle center and the associated radius given by

$$r_L = \frac{|S_{12}S_{21}|}{||S_{22}|^2-2|\Delta|^2|}, \tag{5.18}$$

$$C_L = \frac{(S_{22}-2S_{11}^*\Delta 1^*}{|S_{22}|^2-2|\Delta|^2}, \tag{5.19}$$

and

$$r_S = \frac{|S_{12}S_{21}|}{||S_{11}|^2-1|\Delta|^2|}, \tag{5.20}$$

$$C_S = \frac{(S_{11}-1S_{22}^*\Delta 2^*}{|S_{11}|^2-1|\Delta|^2}, \tag{5.21}$$

where r_L and C_L denotes the circle radius and circle center of the load, respectively and r_S and C_S the circle radius and circle center of the source, respectively. The load and source stability circles for both LNAs at 57 GHz reside far outside the Smith Chart region and cannot be shown graphically. Instead, the Rollet stability factor, K_f and its intermediate term, B_{1f} is calculated which is another popular approach to demonstrate amplifier stability. The two parameters are related to the *s*-parameters which are calculated by SpectreRF and are given by

$$K_f = \frac{1-|S_{11}|^2-1|S_{22}|^2+|\Delta|^2}{2|S_{21}||S_{12}|}, \tag{5.22}$$

and

$$B_{1f} = 1 + |S_{11}|^2 - 1|S_{22}|^2 - 2|\Delta|^2, \tag{5.23}$$

where

$$\Delta = S_{11}S_{22} - S_{21}S_{12}. \tag{5.24}$$

Figure 5.11 shows the stability parameters for both LNAs.

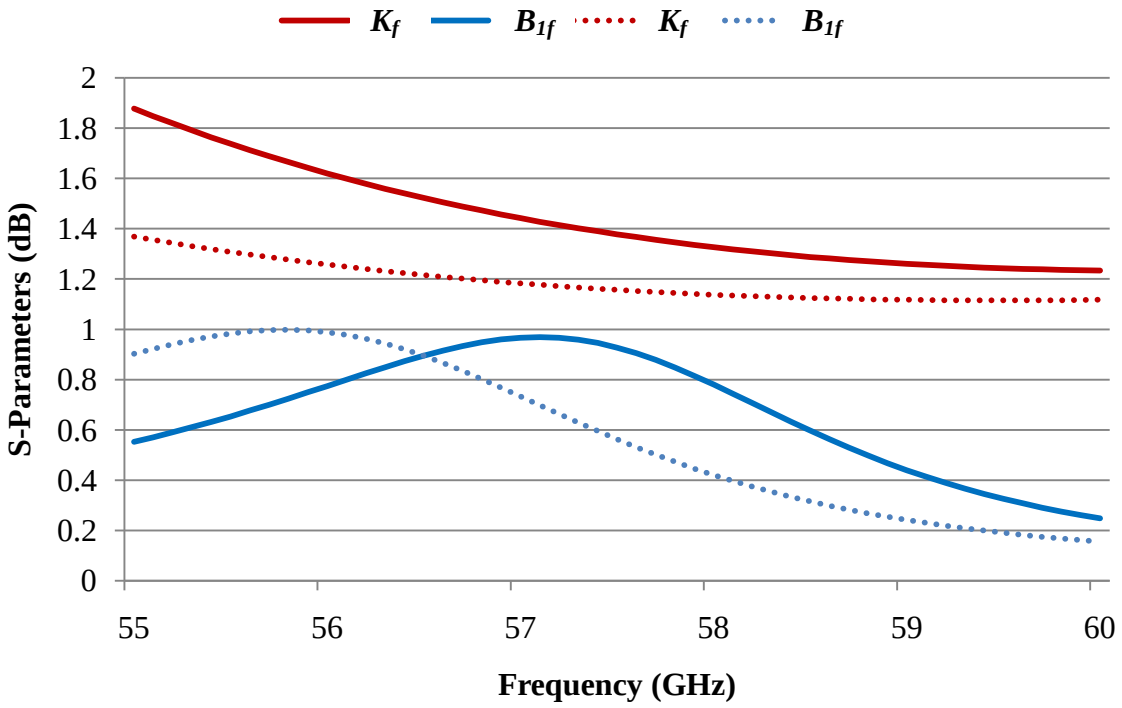

Figure 5.11. The stability parameters of both LNAs where the dotted and solid lines represent LNA 1 and LNA 2, respectively.

For unconditional stability K_f must be larger than 1 ($K_f > 1$) with B_{1f} larger than 0 ($B_{1f} > 0$). This is the case for both LNAs over the 5 GHz bandwidth simulated. Unfortunately, testing unconditional stability over a wider frequency range was not conducted due to the validity of the lumped equivalent circuit bandwidth.

5.2.5.4 Linearity simulations

The 1 dB compression point is a common method to simulate linearity. It only requires one tone for simulation and is simply the power specified at the input where the output power is 1 dB less than it would have been in an ideal linear circuit [**23**]. The 1 dB compression point is given by

$$10Log_{10}\left(\frac{v_0}{v_{oi}}\right) = -1 \text{ dB}, \tag{5.25}$$

where v_o is the output voltage and v_{oi} is the ideal output voltage. The simulation results for LNA 1 and LNA 2 are shown in Figure 5.12, respectively. The 1 dB compression point is the intersection of the output amplitude and the ideal output amplitude shifted by 1 dB.

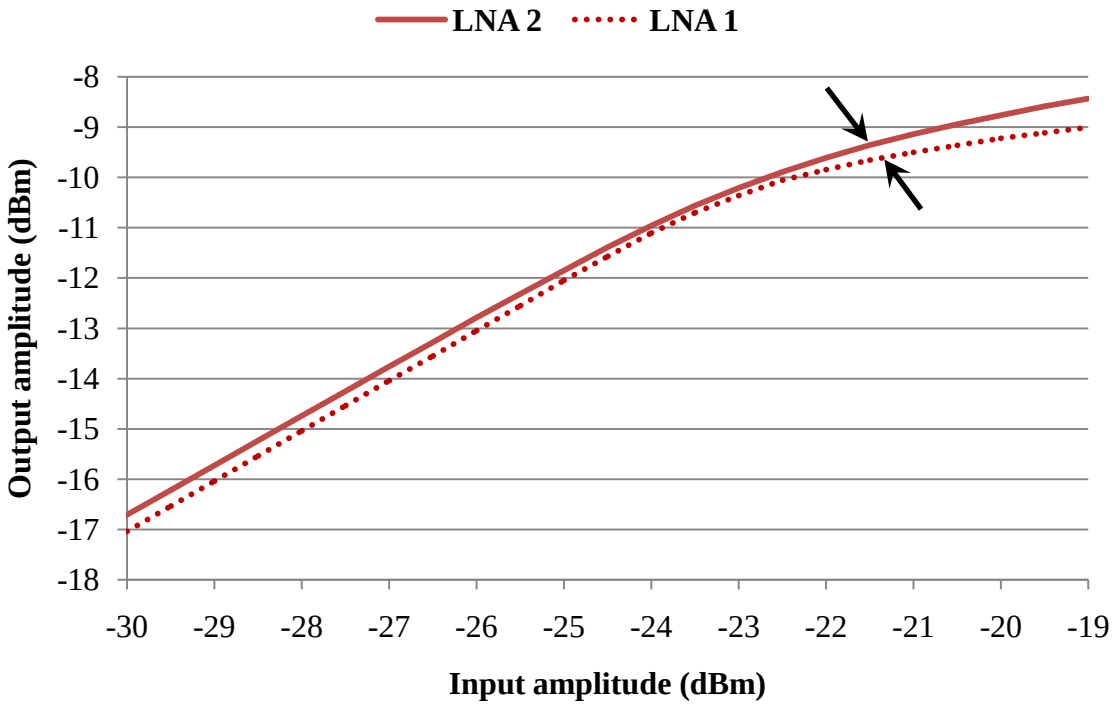

Figure 5.12. The 1 dB compression point of both LNAs where the dotted and solid line represents LNA 1 and LNA 2, respectively -21.7 dBm.

The simulated 1 dB compression point for LNA 1 is -21.7 dBm, while the simulated 1 dB compression point for LNA 2 is -21.0 dBm. From the simulation results, it is shown that the largest input signal that can be applied to the input of the LNA is approximately 80 µV.

5.3 CONCLUSION

Two LNAs are implemented using the S-CPW transmission lines of chapter 4. The four inductors used in the matching networks of LNA 1 are implemented using the four 32 µm S-CPW Narrow transmission lines. LNA 2 implements three 32 µm S-CPW Narrow transmission lines and replacing one inductor (L_S) with a 32 µm S-CPW Wide transmission line. Furthermore, the LNAs have identical transistor sizing and biasing conditions for comparative purposes.

The simulation results reveal very little difference between the LNAs and are mostly attributed to the difference in the equivalent circuits used for the 32 µm S-CPW

transmission lines. The design focussed on realising the best input and output matching performance and the lowest NF and very little compromise was made concerning linearity. The lowest possible supply voltage for the correct transistor operating point was chosen for lowest power dissipation at the expense of linearity. This is shown in the simulation results of Figure 5.12. Finally, both LNAs are unconditionally stable over the simulated 5 GHz bandwidth around 60 GHz. With a NF of 5.3 dB, a power gain of 13 dB and a visible difference between LNA 1 and LNA 2 to prove the hypothesis, the two designs were accepted.

CHAPTER 6: LAYOUT, FABRICATION AND MEASUREMENT SETUP

6.1 INTRODUCTION

This chapter discusses the layout and fabrication of the S-CPW transmission lines, LNAs and PCB. Several layout considerations are discussed to ensure the correct operation of the LNAs. The fabricated chip is placed on PCB and the design and manufacturing thereof is discussed as well as the placement of the wirebonds which proved to be problematic in the LNA measurements.

6.2 CHIP LAYOUT

The layout and fabrication of the chip formed part of a MPW run sponsored by MOSIS. Three sub-projects formed part of the chip which is illustrated in Figure 6.1.

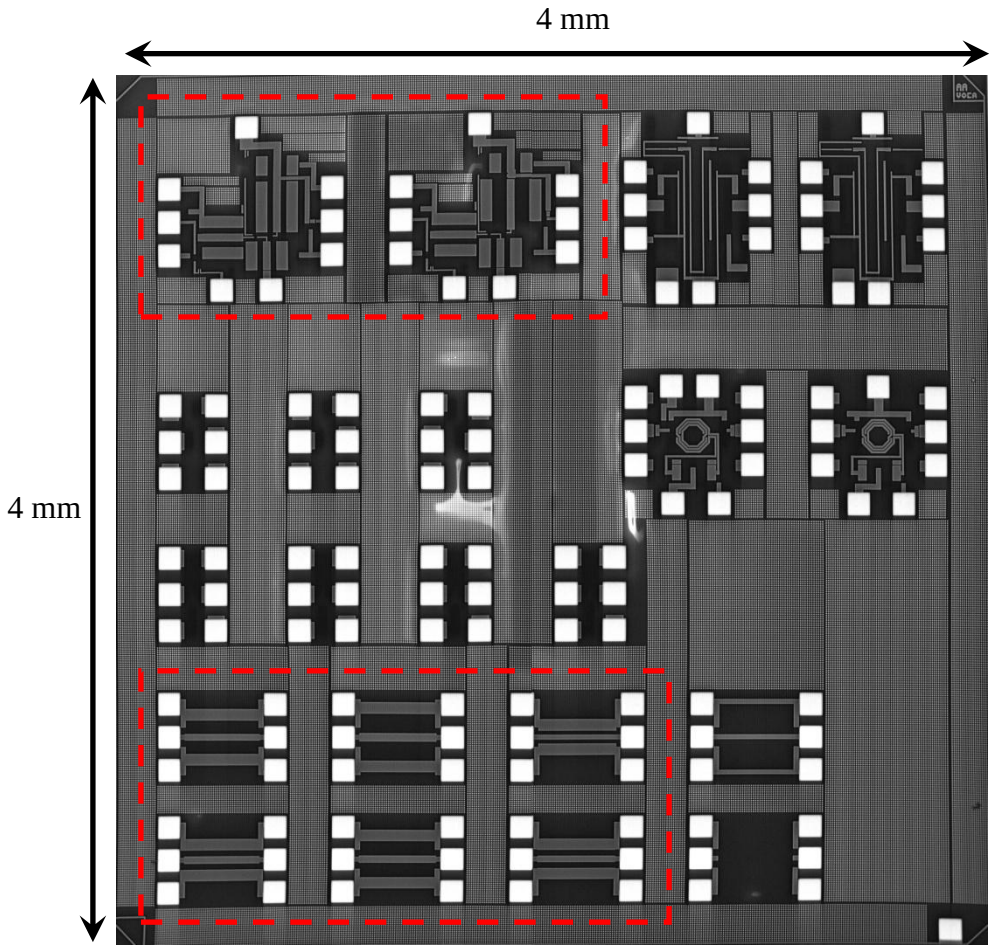

Figure 6.1. Complete chip layout illustrating the sections (patterned frames) of the chip produced by this work. The MPW run was sponsored by MOSIS through the MEP.

The detail surrounding the highlighted two sections of the fabricated chip which forms part of this work is shown in Figure 6.1 and is discussed in the following two sections, i.e. the inductor layout and then the LNA layout are discussed.

6.2.1 Inductor layout

Chapter 4 characterised six S-CPW transmission lines through simulation where the signal-to-ground spacings are varied with the incentive to obtain higher *Q*-factors. In order to verify the simulation results and confirm that the wide S-CPW geometries obtain higher *Q*-factors than the narrow S-CPW geometries, several transmission lines are included on-chip. The 32 µm S-CPW is the most critical as it is implemented in the LNA design, as a result both narrow and wide structures are included on-chip. The 28 µm narrow and wide S-CPW transmission lines are also included to determine their application at frequencies higher than 60 GHz. Additionally, a 20 µm S-CPW Narrow and 36 µm Wide transmission line is included to further characterise the performance of the S-CPWs as two extreme geometries. The transmission lines are fabricated using the 0.13 µm SiGe BiCMOS process from IBM and is shown in Figure 6.2.

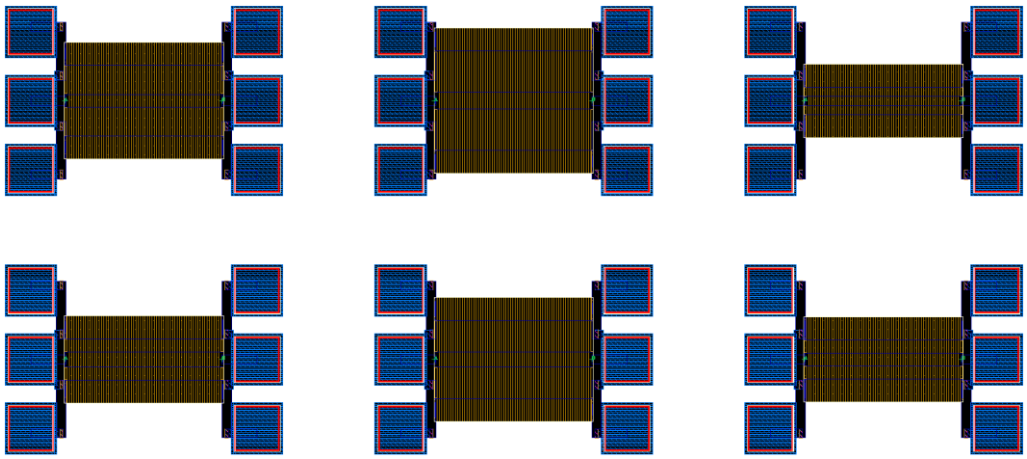

Figure 6.2. Layout of the six S-CPW transmission lines.

Due to the small chip dimensions from the MPW run together with the large size of the S-CPW transmission lines, the three CPW structures discussed in section 4.6 could not be manufactured and included on-chip. Even though, the six S-CPW structures are characterised and experimentally measured. Each of the S-CPWs has an electrical length of 340 µm which is the same length as simulated in chapter 4. With the diverse physical

geometries of the S-CPW transmission lines, measurement pads where placed at the ends to enable on-chip probing.

6.2.2 LNA layout

The layout of LNA 1 and LNA 2 is shown in Figure 6.3 (a) and Figure 6.3 (b), respectively. The input and output GSG pads are placed on the left and right of the amplifier, respectively with the bias pads on the top and bottom.

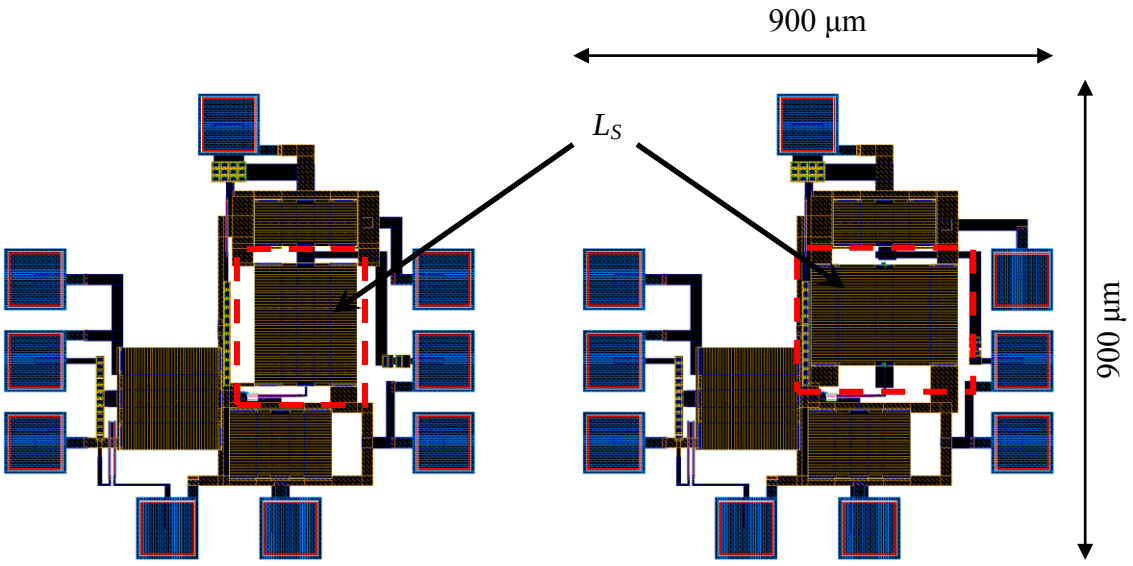

Figure 6.3. Layout of (a) LNA 1 and (b) LNA 2. The substitution of inductor L_S is also illustrated.

The 32 µm S-CPW Narrow transmission line is used as inductors in the design of the LNAs. The two LNAs are identical apart from the one inductor (inductor L_S) substituted in LNA 2 with the 32 µm S-CPW Wide transmission line. This is clearly visible by comparing Figure 6.3 (a) and Figure 6.3 (b). DC blocking capacitors are placed at the input and output signal probe pads as well as decoupling capacitors located at the supply terminal providing a high frequency ground.

6.3 LAYOUT CONSIDERATIONS

Amplifier instability due to high frequency parasitic effects is a critical concern. Long interconnect lengths can introduce a parasitic inductance and together with the capacitance at a particular node cause resonance and subsequently instability. The base node of the CB transistor in the cascode amplifier needs careful consideration due to the high frequency

degeneration of the CB transistor (Q_1) experiences [**10**] [**10**]. Figure 6.4 illustrates the possible instability.

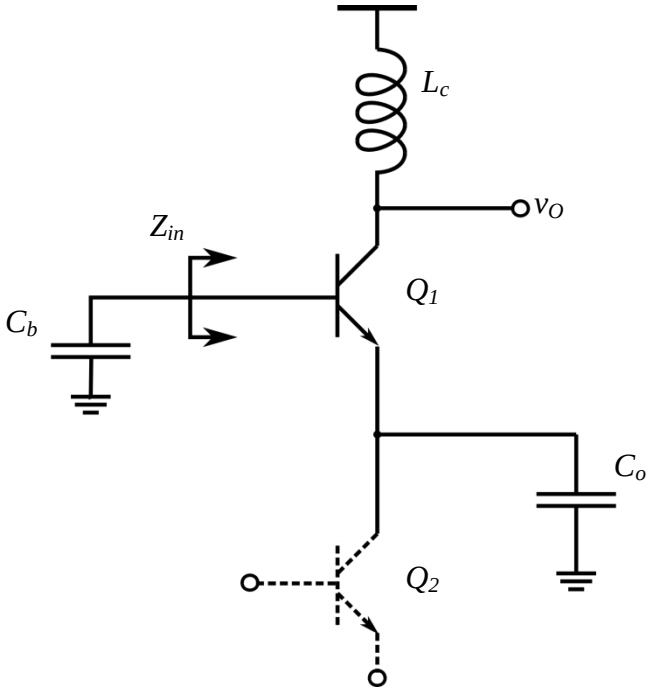

Figure 6.4. High frequency degeneration of the Q_1 producing possible instability.

The impedance seen into the base of Q_1 is approximately given by

$$Z_{in} = \frac{-g_m}{\omega^2 C_o C_{be}} + \frac{1}{j\omega C_o} + \frac{1}{j\omega C_{be}} \tag{6.1}$$

where C_o and C_{be} denotes the degeneration capacitance and the base-emitter capacitance of Q_1, respectively. Equation (6.1) shows a negative real part impedance. A parasitic or physical resistance at the base node of Q_1 must be larger than the negative real part of the input impedance to ensure amplifier stability. This can be realised with the inclusion of a series resistor, but will worsen the noise performance and degrade the amplifier gain. Instead, the losses of the bypass capacitor fulfil this function, providing unconditional stability as simulation showed in section 5.2.5.3. Additionally, the bypass capacitor, C_b, is placed as close as possible to the base of Q_1, firstly to prevent long interconnect lengths producing a parasitic inductance, which may also result in possible instability, and secondly to provide a good quality high frequency ground connection.

Another layout subject concerns the grounding of the LNA. No distinction is made between high frequency and DC grounding and all ground connections are interconnected. Since the high frequency return current follows the path of least inductance and the DC

return follows the path of least resistance, sufficient grounding metal is routed around the circuit allowing the shortest possible return current paths.

6.4 PCB DESIGN AND FABRICATION

The PCB layout is illustrated in Figure 6.5. The PCB dimensions are 12 cm x 12 cm with a physical height of 4 cm to enable the PCB to be placed on the probing station of the VNA.

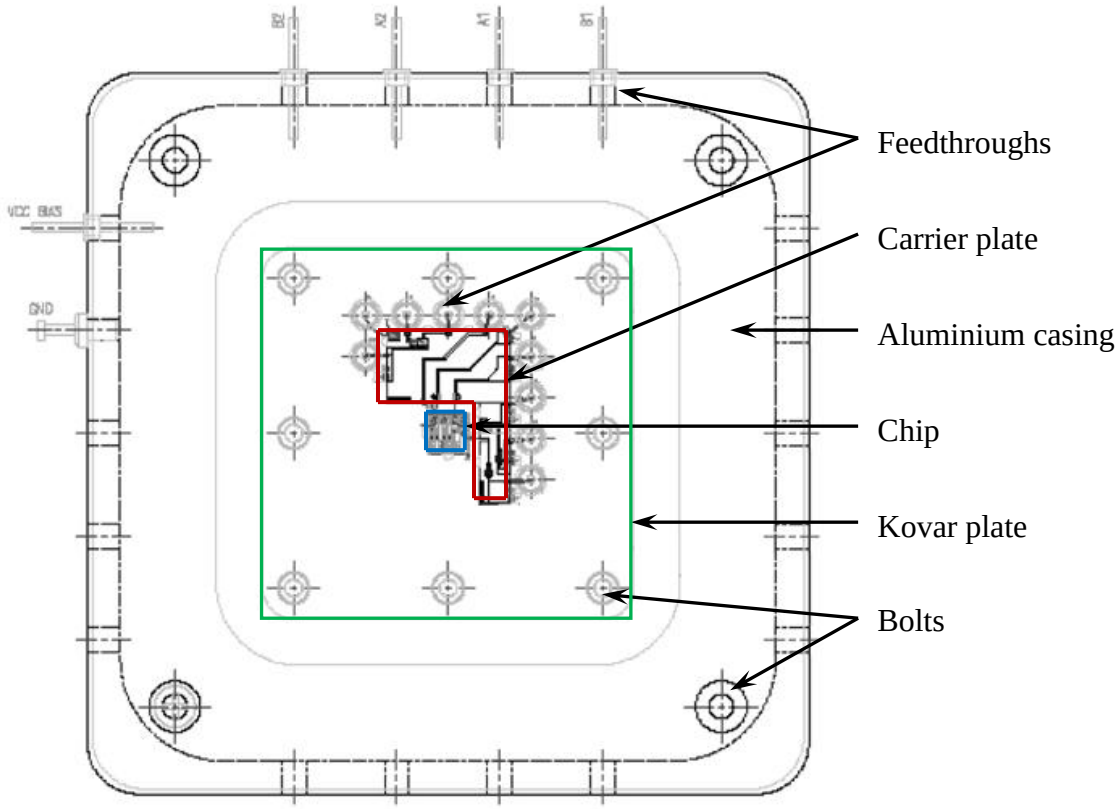

Figure 6.5. PCB layout and chip placement.

Figure 6.5 shows that the 4 mm x 4 mm chip fabricated by IBM is centered onto a gold plated kovar plate using a conductive epoxy. The kovar plate is grounded to serve as the ground plane underneath the chip. Several carrier plates are soldered onto the kovar plate which includes external circuitry used for biasing the on-chip circuits as well as providing wirebond pad connections. The external circuitry includes filter capacitors and RF chokes to provide pure biasing conditions. The carrier plate is an alumina substrate plate soldered onto the kovar plate. The on-chip wirebonds are attached to the wirebond pad connections on the carrier plate.

The kovar plate is bolted to a nickel plated aluminium casing. The aluminium casing houses several feedthrough connections used to connect to external measurement

equipment. The feedthroughs are soldered to the aluminium casing and wirebound to the carrier plate.

6.5 WIREBOND CONSIDERATIONS

Performing high frequency measurements using the probe station while the biasing pads are wirebound presented a potential problem seeing that the wirebonds may intrude during the placement of the GSG probes. Careful planning of the wirebonds is necessary to ensure the optimal placement of the wirebonds to prevent possible shorted connections. A microphotograph of the wirebound LNA together with the probe connection is shown in Figure 6.6.

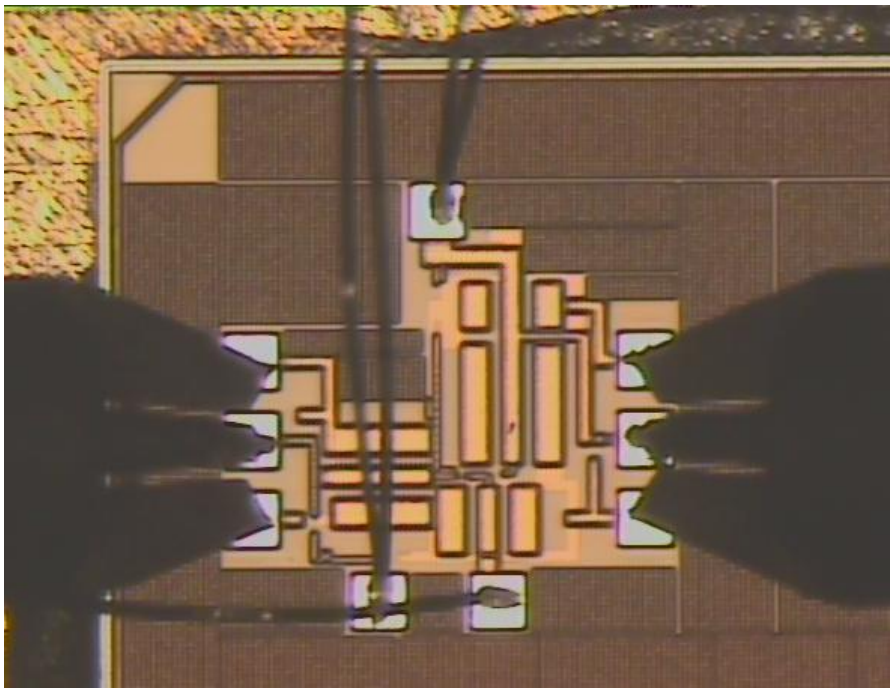

Figure 6.6. An on-chip photograph of the wirebound LNA with the placement of the probe connections.

The layout of the LNA is not optimal as the wirebond lengths are long due to the placement of the biasing pads. The wirebonds can therefore easily damage or break when contacting with the probe tips. The long wirebond lengths will not influence the high frequency performance of the LNA as decoupling capacitors are placed at the biasing pads. A future improvement on the LNA layout would be to place the biasing pads on the same side of the LNA, near the chip edge to ensure short wirebond lengths, decreasing the

possibility of shorting connections during probe placements and damaging the wirebonds during measurements.

6.6 CONCLUSION

This chapter discussed the layout and fabrication of the S-CPW transmission lines, LNAs, the PCB and several difficulties to prevent and address problematic measurement setups. The non-optimal layout of the LNAs presented the most problematic concern during the placement of the wirebonds for when the on-wafer measurements are conducted.

CHAPTER 7: MEASUREMENT RESULTS

7.1 INTRODUCTION

This chapter discusses the measurement results obtained for the S-CPW transmission lines and LNAs. The measurements are conducted with the fabricated PCB which is discussed in section 6.5. The PCB is placed on the VNA probe station which allows for on-chip biasing and probing. The first part of this chapter presents the *s*-parameter results for the S-CPW transmission lines, the *s*-parameter results after de-embedding the pad parasitics, and the extracted transmission line parameters. A conclusion about the performance of the S-CPW transmission lines are discussed thereafter. The second part of this chapter presents the measurements of the LNA which is characterised at DC to determine the bias operating regions, followed by the high frequency measurements. The chapter concludes with the interpretation of the findings after measurements.

7.2 SCPW PAD PARASITICS AND DE-EMBEDDING

Six S-CPW transmission lines are measured to characterise the intrinsic device performance of the transmission lines for the purpose of modelling its behaviour at 60 GHz to be included in the LNA circuit. Due to the incoherent width and signal-to-ground spacings of the transmission lines to the measurement probe width, probe pads are placed to ensure measurement contact. The probe pad parasitics must be de-embedded to obtain the actual transmission line performance since the measurements contain the intrinsic device characteristics together with the pad parasitics. One approach to de-embedding is to include calibration patterns which include the open, short, load and through connections on the same die with pads to mimic the transmission line pads. The probe pads are calibrated with the measurement equipment to directly allow the measurements to quantify the de-embedded transmission line response. Unfortunately, due to the limited chip real estate available it was not possible to include the complete de-embedding calibrations patterns. Instead off-wafer de-embedding is performed by only including one de-embedding structure on-chip. The shunt parasitic capacitance which include the fringing capacitance of the probe pads are the dominant form of loss [**61**], [**71**] and therefore the open probe pad structure is placed on-chip. After measurements are performed, the *s*-parameter results from the open pad structure are subtracted from the transmission line measurements to obtain the intrinsic S-CPW transmission line performance. Figure 7.1 and Figure 7.2 shows an illustration of the shunt parasitic capacitance and the s_{11} parameter of the probe pads, respectively.

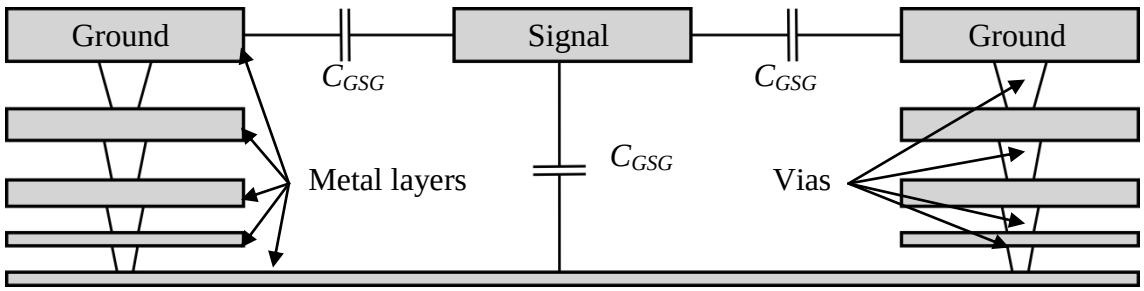

Figure 7.1. Shunt parasitic capacitance due to the ground metal below and adjacent to the signal conductor.

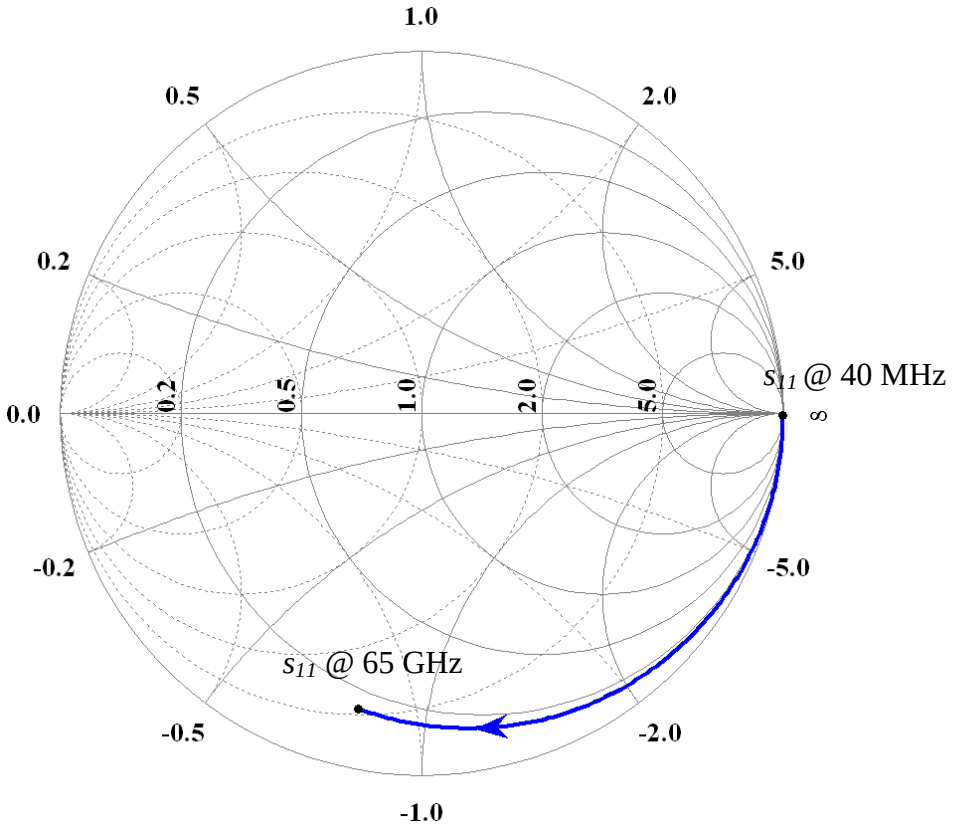

Figure 7.2. Smith chart showing the s_{11} parameter of the open pad structure.

Figure 7.1 shows that a ground shield is implemented on the bottom metal layer of the BEOL underneath the probe pads to prevent coupling to the substrate. The s_{11} parameter result of Figure 7.2 shows that the pad parasitics are predominantly capacitive with a high *Q*-factor, but not an ideal open connection at 65 GHz.

The de-embedding is done by measuring the *s*-parameters of the transmission line and the de-embedding open pad structure. The left probe pads and the right probe pads are

measured separately to characterise the probe pads individually. Each individual probe pad is subtracted from the transmission line *s*-parameters to obtain the S-CPW response. An illustration of this procedure is shown in Figure 7.3.

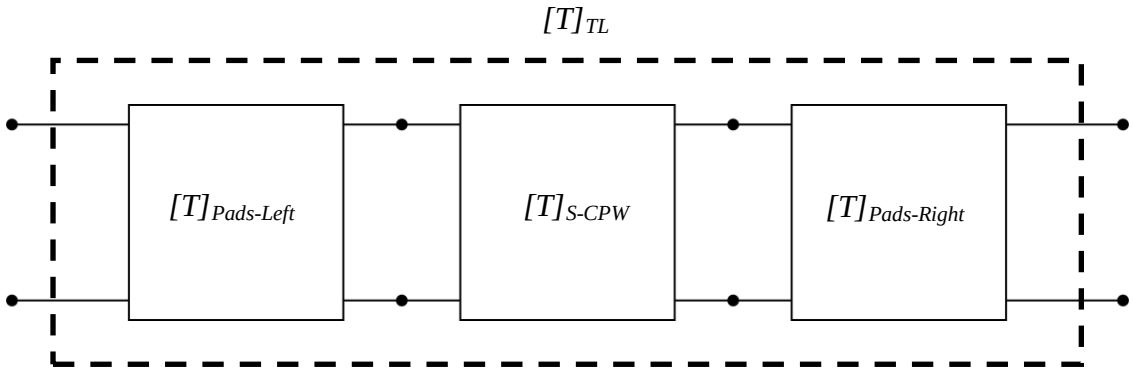

Figure 7.3. Obtaining the S-CPW response by de-embedding the pad parasitics.

Figure 7.3 shows a cascade of two-port models for each individual structure. The pads on the left, the S-CPW structure and the pads on the right together form the complete transmission line structure. A mathematical equation for the transmission line response is given in *t*-parameters by

$$[T_{TL}] = [T_{Pads-Left}][T_{S-CPW}][T_{Pads-Right}], \tag{7.1}$$

where $T_{Pads\text{-}Left}$ is the *t*-parameters of the left pads, $T_{Pads\text{-}Left}$ is the *t*-parameters of the right pads, T_{TL} is the *t*-parameters of the measured transmission line including the pad structures and $T_{S\text{-}CPW}$ is the *t*-parameters of the S-CPW excluding the pads. The response of the S-CPW transmission line can be obtained using

$$[T_{S-CPW}] = [T_{Pads-Left}]^{-1}[T_{TL}][T_{Pads-Right}]^{-1}. \tag{7.2}$$

The de-embedding procedure in (7.2) is not analytically performed but instead carried out using the in-built de-embedding function provided by AWR[3].

7.2.1 *s*-parameter measurements and de-embedding results

The experimental *s*-parameter results for the 32 µm Wide and the 32 µm Narrow S-CPW transmission line are shown in Figure 7.4 to Figure 7.7. Only the 32 µm SCPW transmission lines are employed in the LNAs and will therefore be the focus of this section. The s_{11} and s_{12} measurements together with the de-embedded measurement results are shown and compared with the IE3D simulations results.

[3] http://web.awrcorp.com

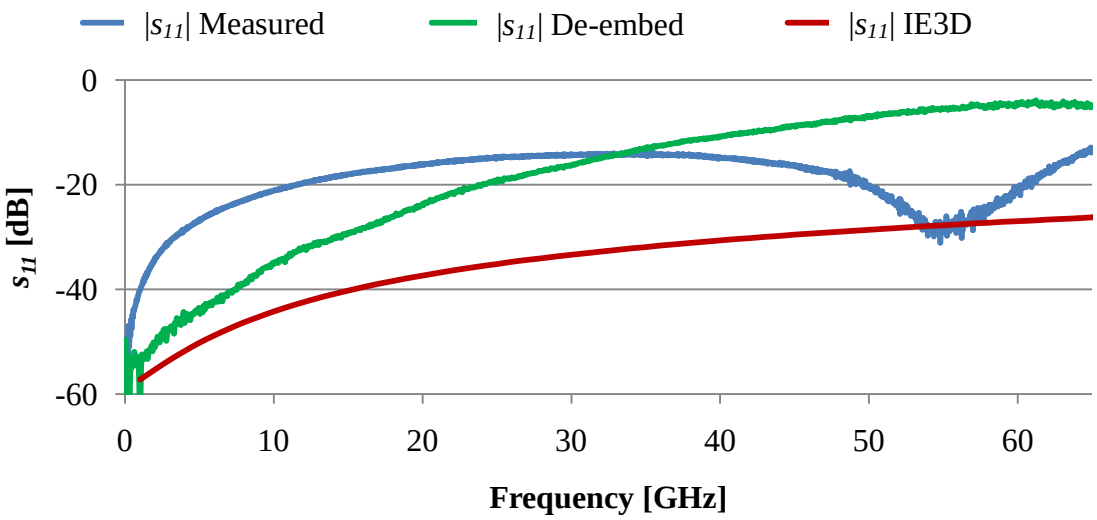

Figure 7.4. The s_{11} measured, de-embedded and simulation results of the 32 µm S-CPW Wide.

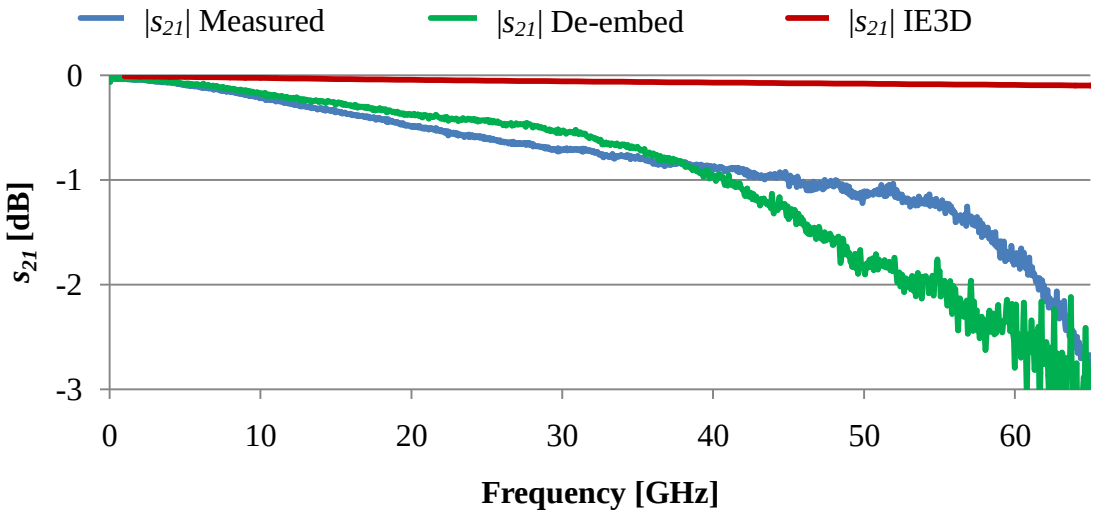

Figure 7.5. The s_{12} measured, de-embedded and simulation results of the 32 µm S-CPW Wide.

Figure 7.4 and Figure 7.5 shows the discrepancy between the measured and the de-embedded results for the 32 µm S-CPW Wide. Figure 7.4 indicates a resonant frequency at 55 GHz which is due to the parasitic capacitance of the probe pads and the coupling of the pads to the transmission line structure. The de-embedded result removes the parasitic capacitance and shows no resonant peak in the measured de-embedded frequency results. IE3D simulation results differ significantly from the de-embedded results and become worse at higher frequencies for all structures. This discrepancy shows that the coupling and the complex high frequency effects between the signal and ground conductors of the

S-CPW transmission lines are underestimated by IE3D. The IE3D simulation results are however approximating the de-embedded results up to 20 GHz but then underrate the transmission and permittivity losses due to the 2.5D nature of the simulator.

Figure 7.6 and Figure 7.7 show the s_{11} and s_{21} measurement, de-embedded and IE3D simulation results for the 32 µm Narrow S-CPW transmission line.

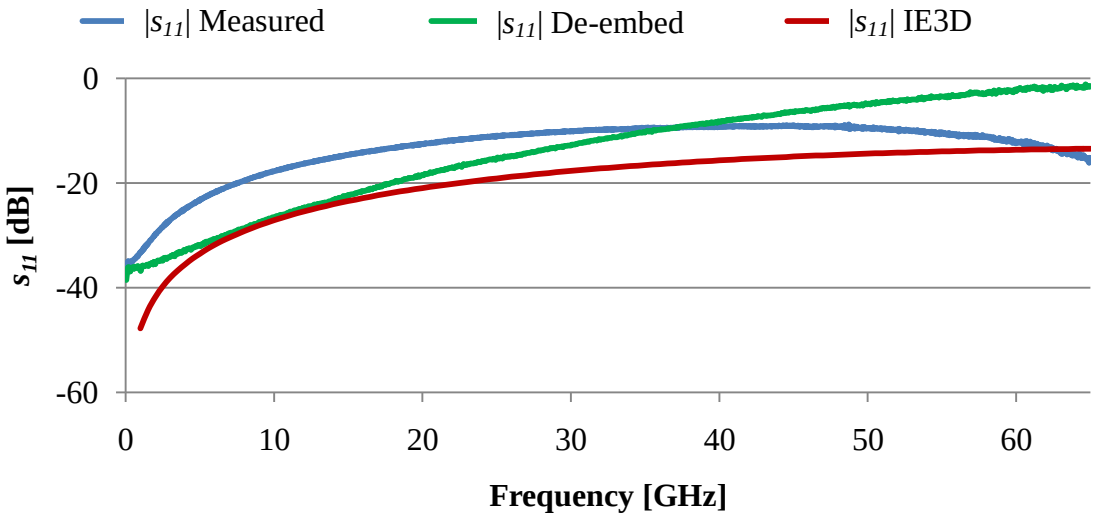

Figure 7.6. s_{11} measured, de-embedded and simulation results of the 32 µm S-CPW Narrow.

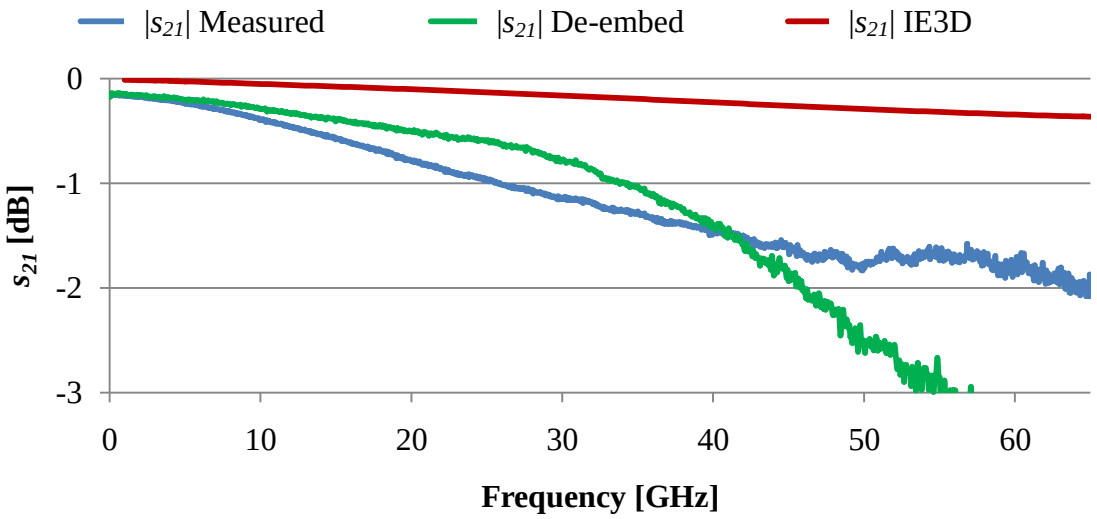

Figure 7.7. s_{21} measured, de-embedded and simulation results of the 32 µm S-CPW Narrow.

The simulation results for the 32 µm S-CPW Narrow also show that IE3D approximates the *s*-parameter measurement response only up to 20 GHz. The measurement results show

no resonant frequency for the narrow transmission line. A comparison of the de-embedded results between the 32 µm Narrow and the 32 µm Wide S-CPWs shows that the wide transmission line achieves less reflection and transmission attenuation than the narrow line, predicting that the wide transmission line will realise higher *Q*-factors than the corresponding narrow transmission line.

7.2.2 Transmission line parameter extraction results

Figure 7.8 and Figure 7.9 shows the extracted characteristic impedance of all the measured transmission line structures and are compared with the simulated results presented in section 4.6. The S-CPW measured results presented are from the 20 µm Narrow, 28 µm Narrow and Wide, 32 µm Narrow and Wide and the 36 µm Wide S-CPW transmission lines.

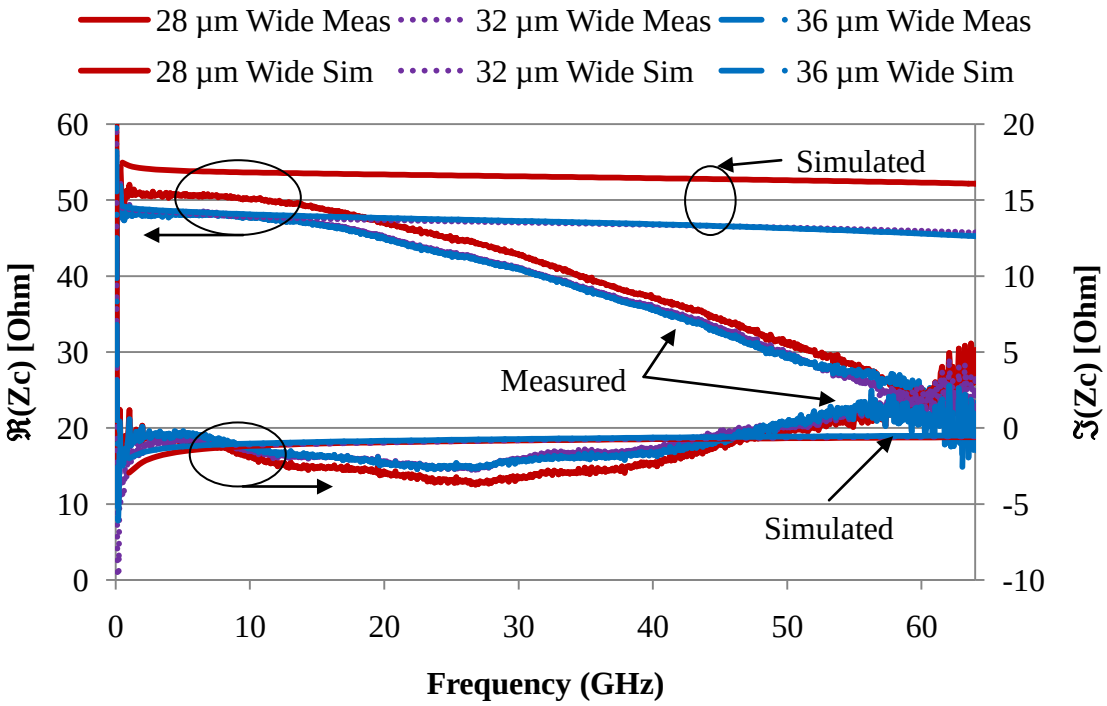

Figure 7.8. The extracted real and imaginary characteristic impedance of the de-embedded and simulated Wide S-CPW structures from 1 GHz to 65 GHz.

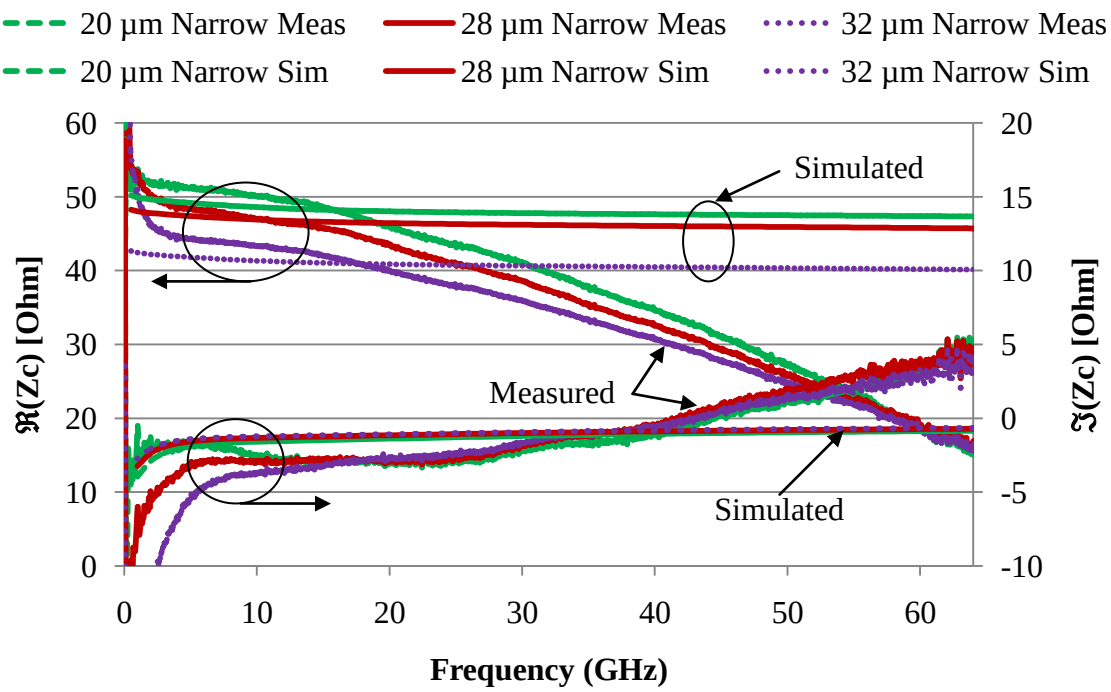

Figure 7.9. The extracted real and imaginary characteristic impedance of the de-embedded and simulated Narrow S-CPW structures from 1 GHz to 65 GHz.

Figure 7.8 and Figure 7.9 shows that the real part of the characteristic impedance of the measured S-CPW transmission lines is approximating the real part of the characteristic impedance for the simulated lines, but only up to 20 GHz. At frequencies higher than 20 GHz, the real part of the characteristic impedance drops rapidly due to an increase in the conductance and capacitance of the transmission line without a simultaneous increase in transmission line inductance. The increase in conductance and capacitance of the transmission line without the simultaneous increase in inductance is reflected in the increase in the imaginary component of the characteristic impedance at frequencies higher than 20 GHz.

The attenuation constant for the de-embedded measured Wide S-CPW and Narrow S-CPW structures is shown in Figure 7.10 and Figure 7.11, respectively. The measured results vary considerably from the simulation results for both the Wide and Narrow S-CPWs. At 40 GHz the attenuation constant simulated for the 32 µm Wide S-CPW transmission line is 0.3 dB/mm while the measurement result is 1.75 dB/mm. The simulation prediction underestimated the attenuation constant by a factor 5.8 which will inadvertently reflect in the *Q*-factor performance.

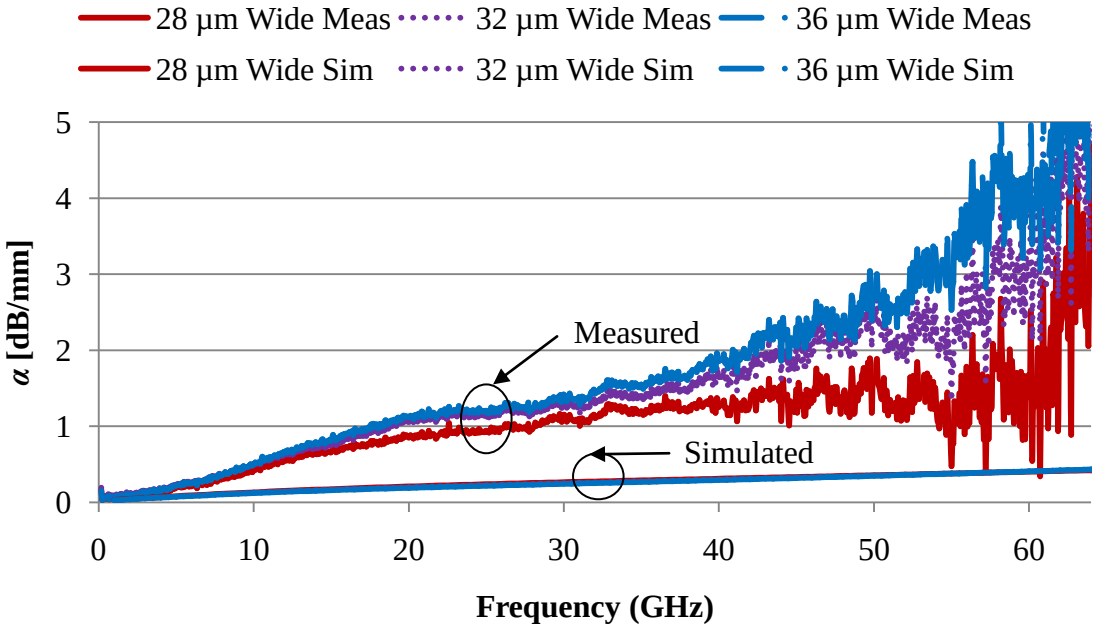

Figure 7.10. The extracted de-embedded and simulated attenuation constant for the Wide S-CPW structures from 1 GHz to 65 GHz.

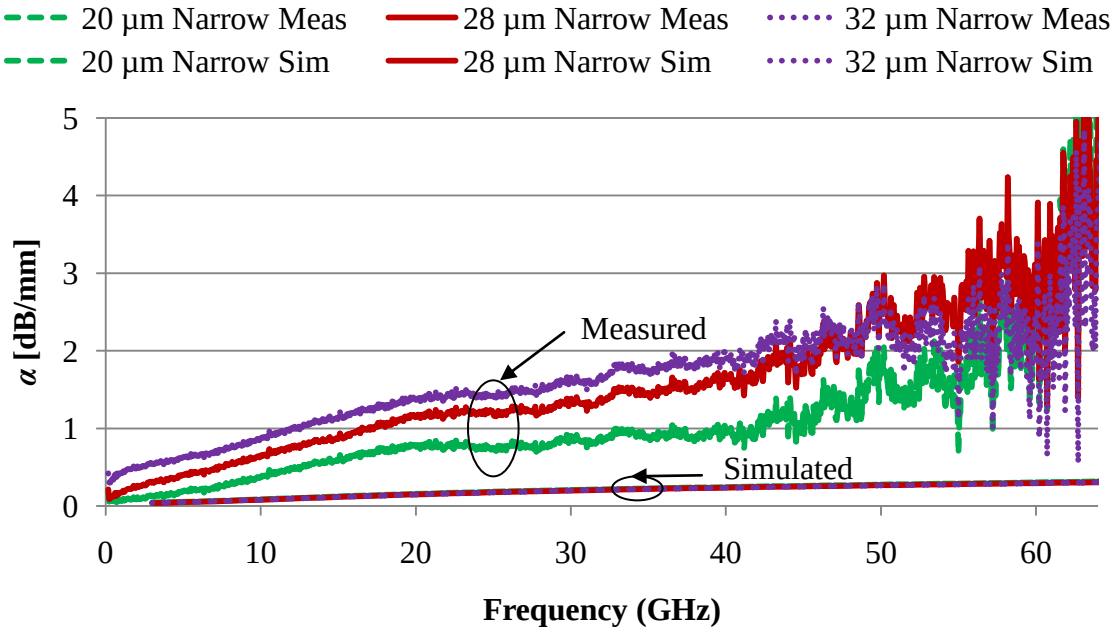

Figure 7.11. The extracted de-embedded and simulated attenuation constant for the Narrow S-CPW structures from 1 GHz to 65 GHz.

A comparison between the measured Narrow and Wide transmission lines in Figure 7.10 and Figure 7.11 show that the Wide structure achieves 0.2 dB/mm lower attenuation than the respective Narrow structure over the measurement frequency range. The attenuation constant consists of two parts: conductive and dielectric/substrate attenuation. The

attenuation discrepancy is attributed to dielectric and substrate attenuation since the geometry parameters of the Narrow and Wide S-CPW transmission lines are the same apart from for the signal-to-ground spacing, and will therefore achieve the same conductor attenuation. The results also reveal that the 28 µm S-CPW transmission line achieves a smaller attenuation constant than the 32 µm S-CPW transmission line. This result shows that substrate losses remain considerable and that the shield does not completely prevent electric field to substrate coupling. Furthermore, the 32 µm S-CPW Wide transmission line is not the optimised S-CPW geometry at 60 GHz for the chosen geometry and process parameters. Apart from the signal-to-ground spacing, the signal conductor widths are therefore another geometry parameter that needs optimisation to achieve the lowest possible attenuation constant.

The phase constant for the Wide and Narrow transmission lines is extracted from the simulated and de-embedded measurement results and is shown in Figure 7.12 and Figure 7.13, respectively.

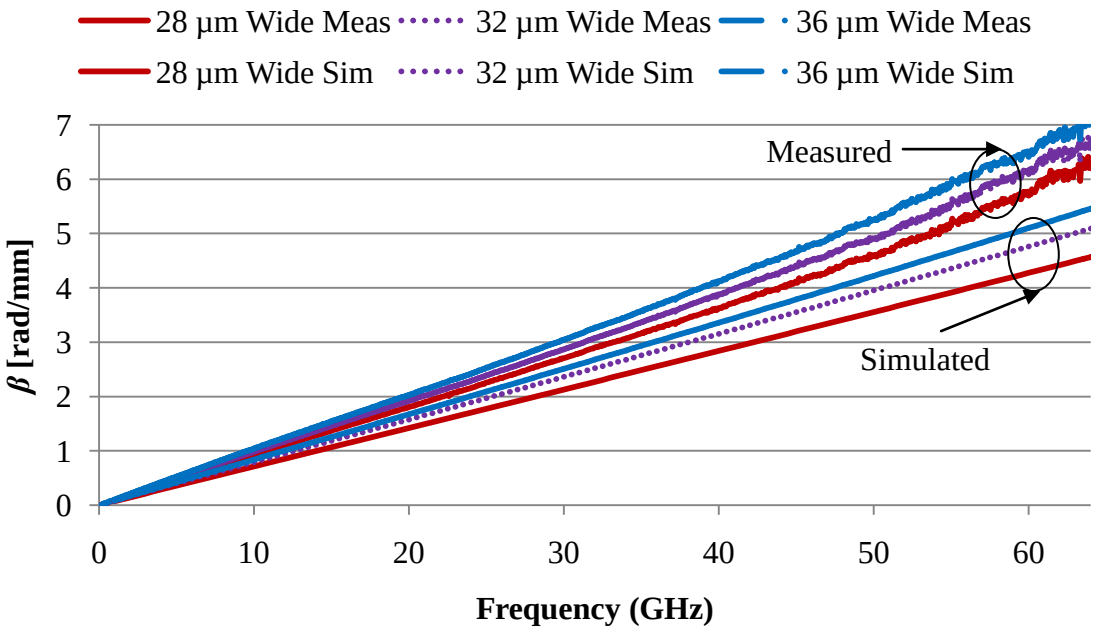

Figure 7.12. The extracted de-embedded and simulated phase constant for the Wide S-CPW structures from 1 GHz to 65 GHz.

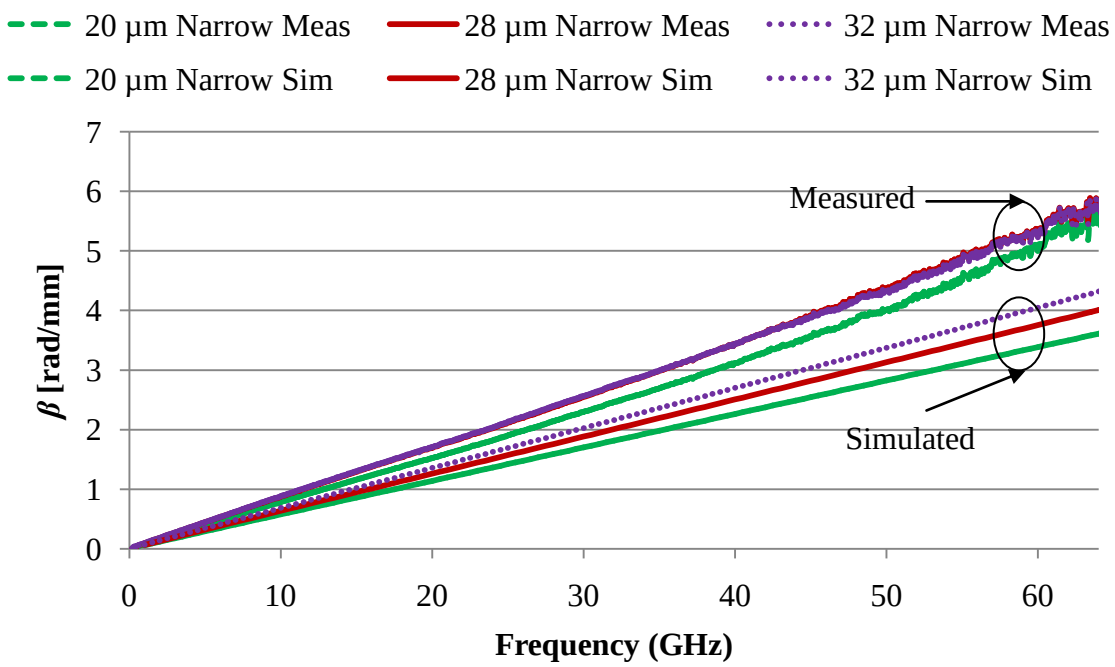

Figure 7.13. The extracted de-embedded and simulated phase constant for the Narrow S-CPW structures from 1 GHz to 65 GHz.

The phase constant for both the Wide and Narrow lines shown in Figure 7.12 and Figure 7.13, respectively remain linear over the frequency range. The simulation results reasonably predict the phase constant performance for the Wide and Narrow transmission line structures. A comparison between the measured results in Figure 7.12 and Figure 7.13 show that the phase constant for the Narrow S-CPWs are only slightly lower than the phase constant achieved by the Wide S-CPWs.

The *Q*-factor from the simulated and de-embedded measured results for the Wide and Narrow transmission lines is calculated and shown in Figure 7.14 and Figure 7.15, respectively.

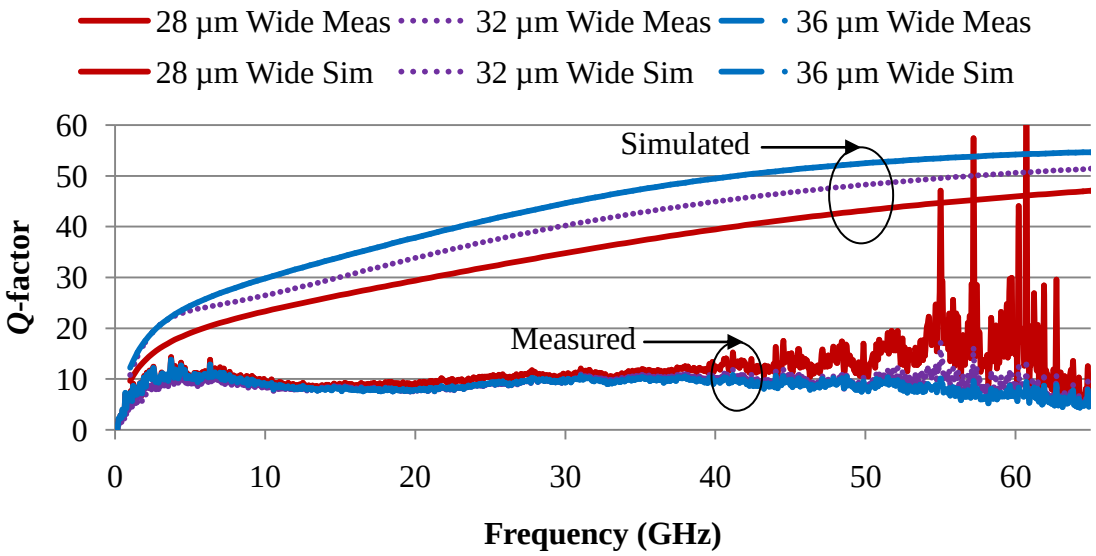

Figure 7.14. The extracted de-embedded and simulated *Q*-factor for the Wide S-CPW structures from 1 GHz to 65 GHz.

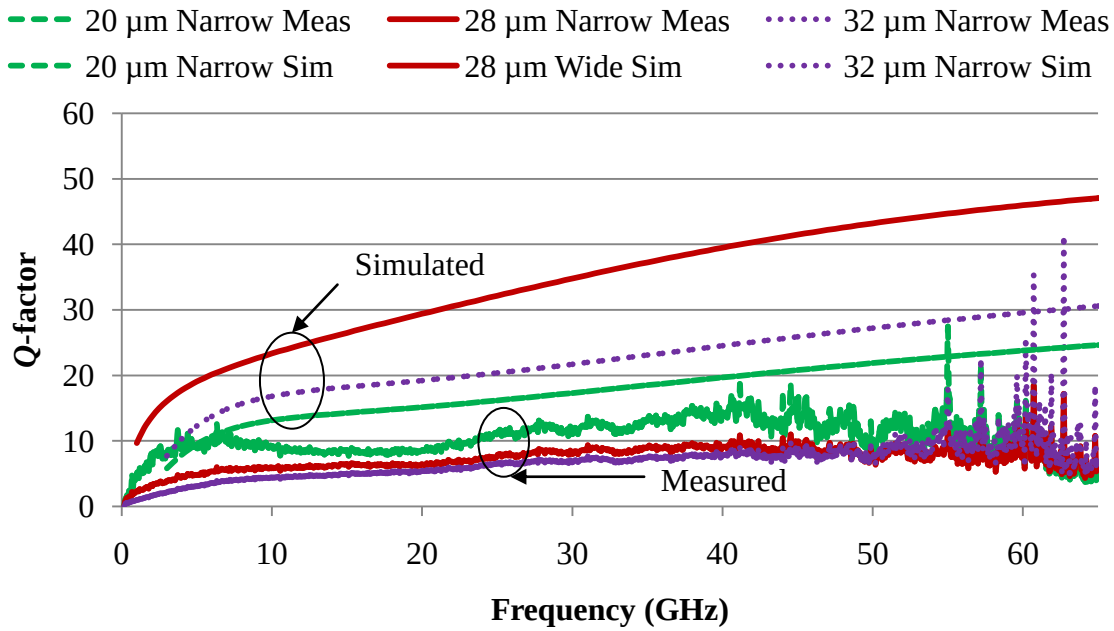

Figure 7.15. The extracted de-embedded and simulated *Q*-factor for the Narrow S-CPW structures from 1 GHz to 65 GHz.

The simulated *Q*-factor results between the Wide and Narrow S-CPW structures show large differences when compared to the *Q*-factor results for the measurements. The calculated *Q*-factors from the measurements are much lower than the simulated values which are primarily due to the higher measured attenuation constant. The calculated *Q*-factors from measurements are lower than expected, although the prediction that the Wide

S-CPW structures achieve higher *Q*-factors than the Narrow S-CPWs remains valid. The 32 µm Wide S-CPW transmission line achieves a *Q*-factor of 10 compared to the 32 µm Narrow S-CPW transmission line which obtains a *Q*-factor of 8 over most of the measured frequency range.

The attenuation and phase constant measurement results presented in Figure 7.10 to Figure 7.13 show significant deviation from what simulation predicted. A possible explanation may be due to the complex coupling between the signal conductor and the adjacent ground conductors. The coupling of the electric field for the 32 µm Narrow and the 32 µm Wide S-CPW is shown in Figure 7.16 and Figure 7.17, respectively.

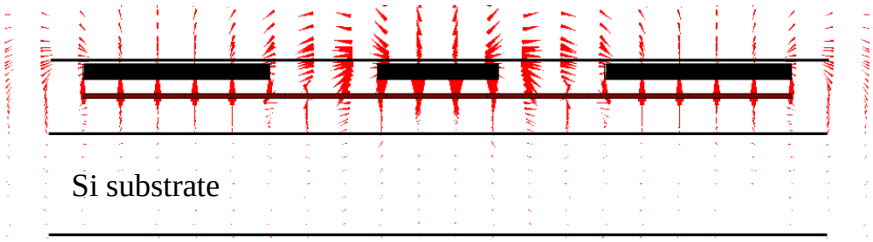

Figure 7.16. Electric field vectors for the 32 µm Narrow S-CPW transmission line.

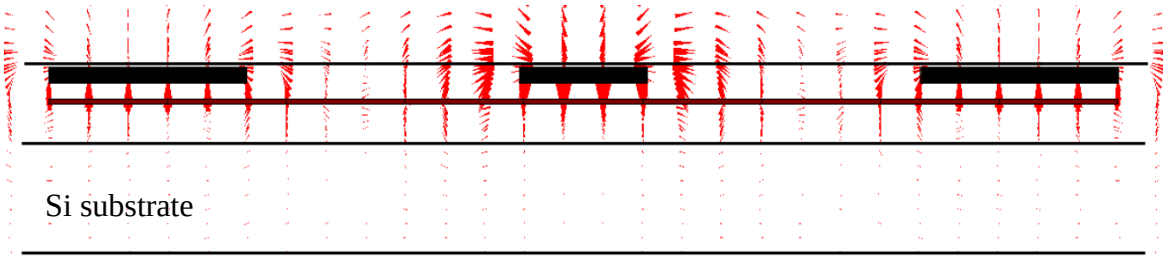

Figure 7.17. Electric field vectors for the 32 µm Wide S-CPW transmission line.

Figure 7.16 and Figure 7.17 show the vector electric field components from the signal conductor to the adjacent ground conductors. For the 32 µm Narrow S-CPW a large portion of the electric field directly couples to the adjacent ground conductors while another portion couples to the floating shield and then couples to the ground conductors. For the 32 µm Wide S-CPW, the coupling is different. Most of the electric field couples to the floating shield which then couples to the ground conductor. This is mathematically envisaged by the displacement current that exists between the signal and ground conductors. The displacement current defined as the rate of change of electric flux density between the signal and ground conductors prefer to flow in the metal shield as opposed to

through the lossy SiO_2 dielectric. Consequently, the wider the signal-to-ground spacing with the addition of the shield improves the dielectric attenuation constant for the structures as it allows electric field coupling at a shorter effective distance through the metal shield as opposed to coupling directly to the ground conductors through the dielectric. As IE3D is a surface simulator and not a volume simulator together with the S-CPWs operating at 60 GHz, results in the prediction of the complex coupling between the signal and ground conductors being inaccurate. A 3D simulator would more thoroughly account for the dielectric loss and predict more accurate *Q*-factor results.

An important observation can be drawn from the measurement results. The addition of the floating metal shield introduces a capacitance to the CPW transmission line, but more so, dominates the capacitance of the line. Therefore, as the signal-to-ground spacing of the S-CPW transmission line is increased, the resultant *Q*-factor would increase due to an increase in the effective magnetic energy storage. The measurement results also show that the signal conductor width can be optimised by decreasing the signal width which decreases the effective footprint area of the inductor. The measurement results show that the 28 µm Wide S-CPW achieved a higher *Q*-factor than the 32 µm Wide S-CPW, which reveals that the 32 µm Wide S-CPW is not the optimised geometry at 60 GHz for the chosen geometry and process parameters. The dielectric/substrate attenuation is more severe than the conductor attenuation which demonstrates much room for further improvement.

7.3 LNA MEASUREMENTS

The LNA measurements consist of two parts. The first part characterises the LNA at DC to determine the bias conditions for the correct operating regions of the transistors. The DC behaviour of the LNA is determined using the Keithley 4200-SCS Semiconductor Characterization System. The system also enables LNA biasing during high frequency measurements as well as parameter calculation for post measurement analysis. Two bias conditions are chosen which is used in the high frequency measurements. The second part characterises the LNA at high frequencies using the Anritsu 37397D VNA to obtain the *s*-parameter measurements from 40 GHz to 65 GHz. Only LNA 1 is measured and characterised due to a layout complication found during measurements. The layout complication is discussed in section 7.3.1.

7.3.1 LNA layout setback

A layout complication with LNA 2 is found during measurements. The problem is shown in Figure 7.18 indicating a connection break between the output matching network inductors. This break in the signal line in the output matching network resulted in a completely dysfunctional LNA. No biasing or characterisation could be performed due to the location of the connection break. The connection break is highlighted by a dashed rectangle encapsulating the issue.

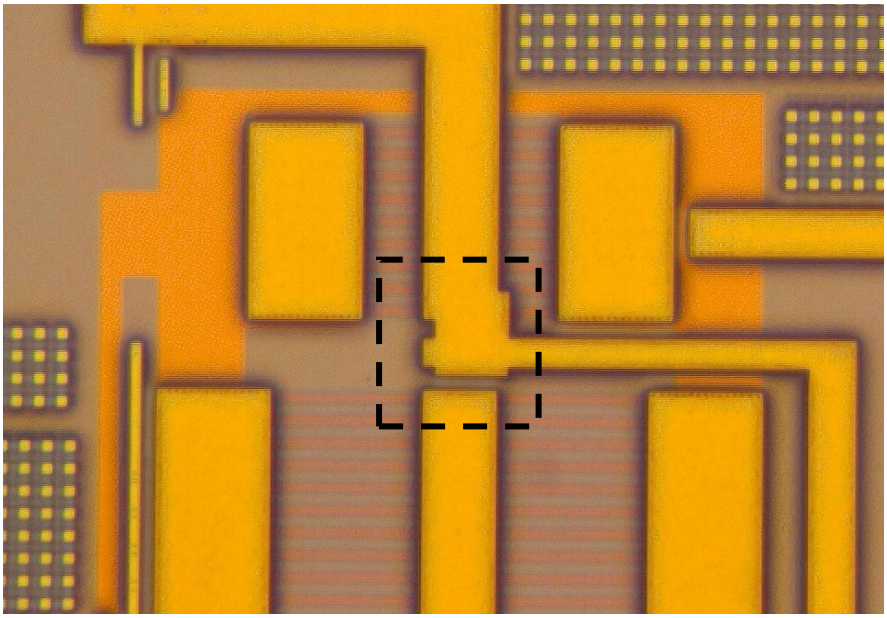

Figure 7.18. The layout complication of LNA 2 prohibiting any measurements or characterisation.

The LVS for each individual LNA performed successfully. The layout complication occurred between placement of each individual subsystem on the chip, and the layer flattening process before fabrication submission. The separation distance of the signal line break is 6 µm. An attempt to correct the issue is complicated due to the nitrite layer forming part of the passivation layer deposited over the die providing scratch protection. The break in signal connection could not be corrected due to the cost implications trying to remove the nitride layer. No LNA 2 measurements could therefore be conducted.

7.3.2 DC characteristics

The current-voltage (I-V) characteristic of LNA 1 is shown in Figure 7.19. The supply voltage is swept from 0 V to 3.5 V with a specific base current applied to the LNA, and the

corresponding supply current is measured. It is also apparent that the transistor breakdown voltage is approached at 3.5 V when a base current of 1 µA is applied.

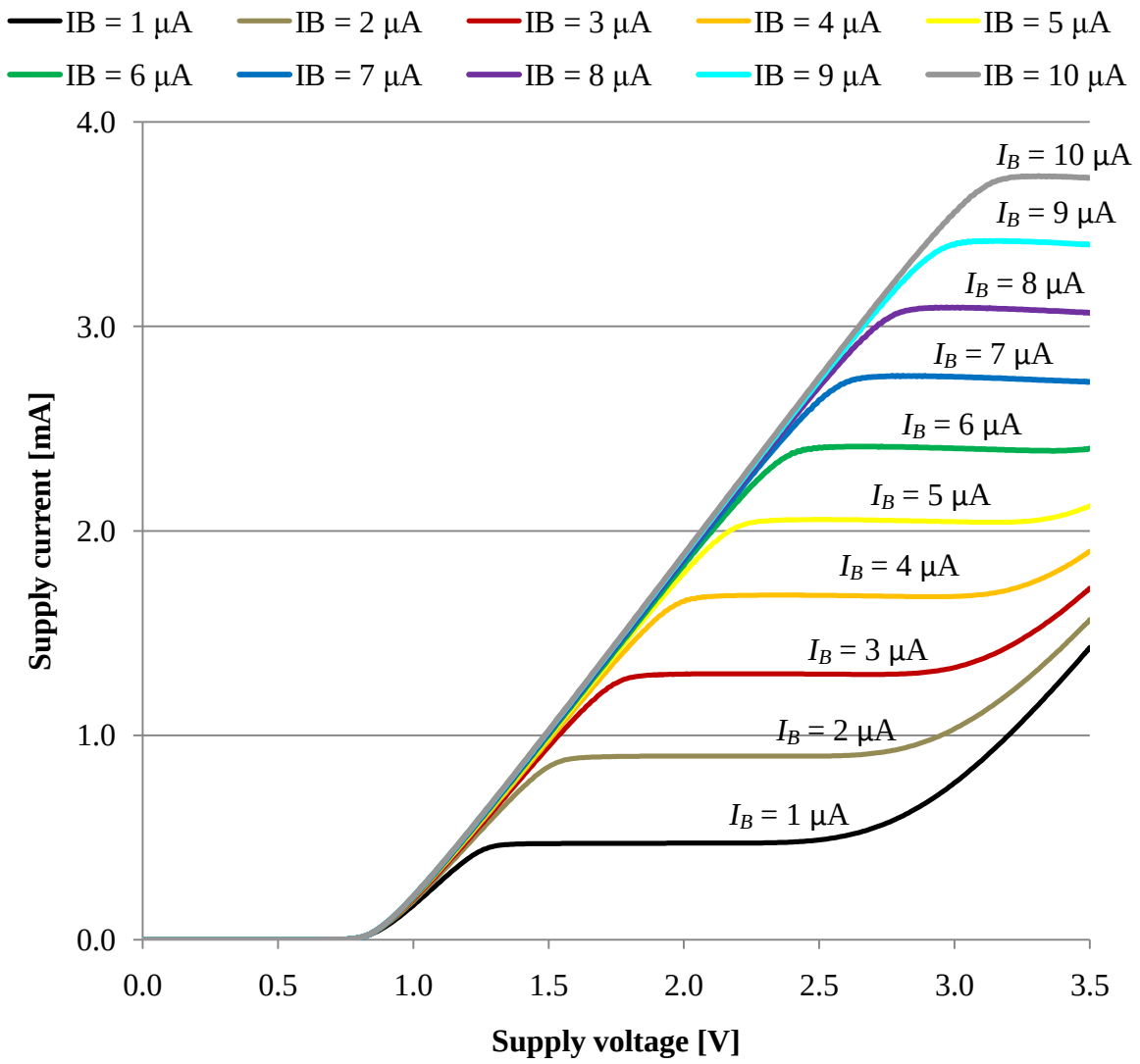

Figure 7.19. I-V characteristic of LNA 1 with different supplied base currents varying from 1 µA to 10 µA

The theoretical design of the LNAs required a supply voltage of 1.5 V and a collector current of approximately 4 mA which is equivalent to a base current of 10 µA. From Figure 7.19 this is undoubtedly not possible as the two transistors of the LNA are operating in saturation under the preferred theoretical bias conditions. A comparison of the theoretical simulation results and the measured results are presented in Figure 7.20 for base currents equal to 1 µA and 10 µA.

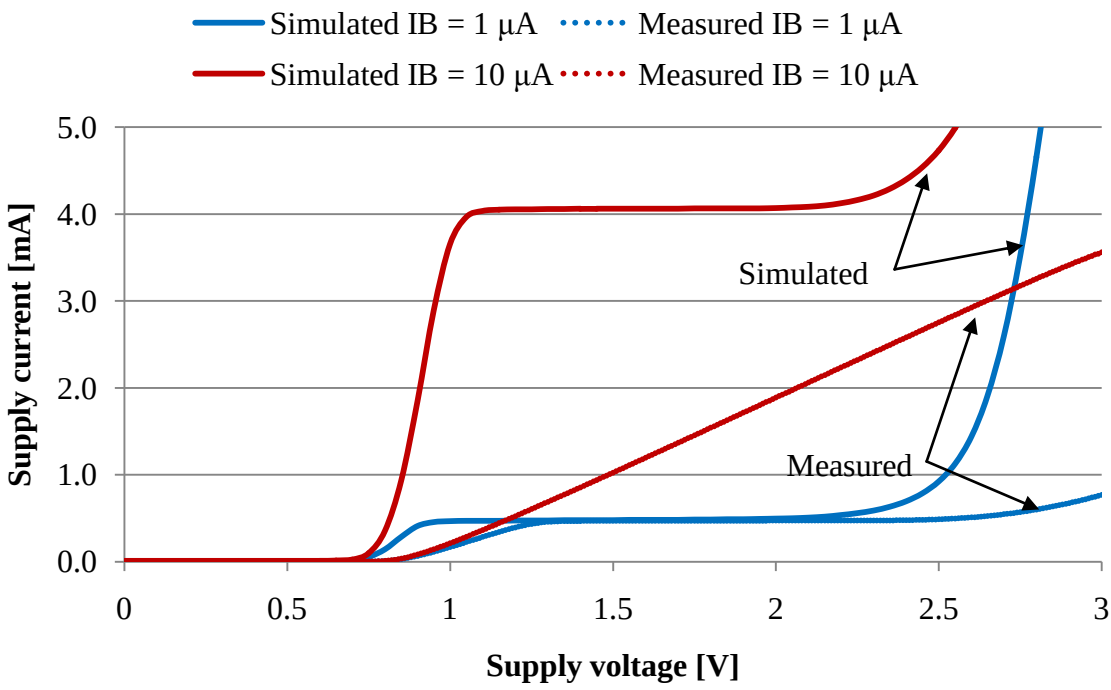

Figure 7.20. Comparison of the simulated and measured I-V characteristic of LNA 1 for two applied base currents. The simulated and measured results are shown with a solid and dotted line, respectively.

The simulated result for a base current of 10 µA shows that the transistors enter saturation at a supply voltage of 0.7 V and enters the active region of operation at 1 V. The conductance slope in the saturation region is extremely high and illustrates the small resistive losses of the transistors. For the same bias condition where a base current of 10 µA is applied, the measured result shows a significant deviation from the simulated result. The two transistors only enter the active region of operation at a 3 V supply voltage. For the bias condition where the LNA is biased at 1.5 V, a maximum base current of 1 µA may be applied.

A possible conclusion for the measured results to exhibit a response with a much lower slope than the simulated results, is that the CB transistor of the cascode configuration is experiencing a significant emitter degeneration resistive loss. Calculating the slope of the measured results by

$$R_{E,CB} = \frac{\partial V_{CC}}{\partial I_C}, \tag{7.3}$$

equates to a 500 Ω degeneration resistor. The dilemma is that the degeneration resistance is in the signal path of the LNA and will inevitably affect the high frequency performance.

7.3.3 High frequency characteristics

The high frequency measurements are conducted at two bias conditions. The first bias condition is with LNA 1 biased at 1.5 V with a base current of 1 µA and is shown in Figure 7.21 and Figure 7.22. The second bias condition is when the LNA is operating at 3.5 V with a 10 µA base current and is shown in Figure 7.23 and Figure 7.24.

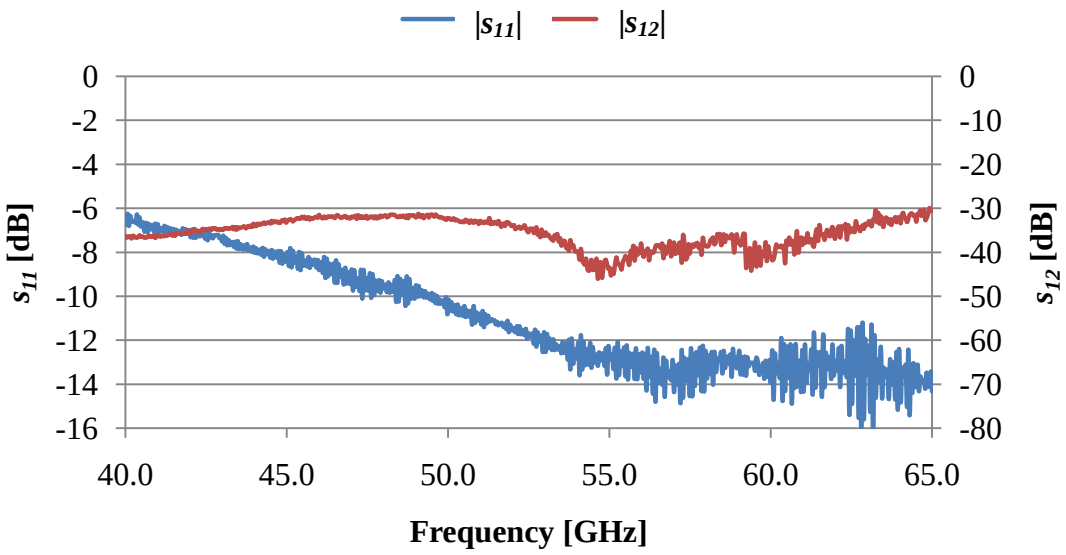

Figure 7.21. s_{11} and s_{12} measurements for LNA 1 operating with 1.5 V supply and a 1 µA base current.

Figure 7.21 shows the s_{11} and s_{12} measured results for the 1.5 V, 1 µA bias condition. The reverse isolation is below -30 dB for the frequency range shown. The input reflection coefficient is below -10 dB from 50 GHz up to 65 GHz. The lowest s_{11} is obtained at 57 GHz equal to -14 dB.

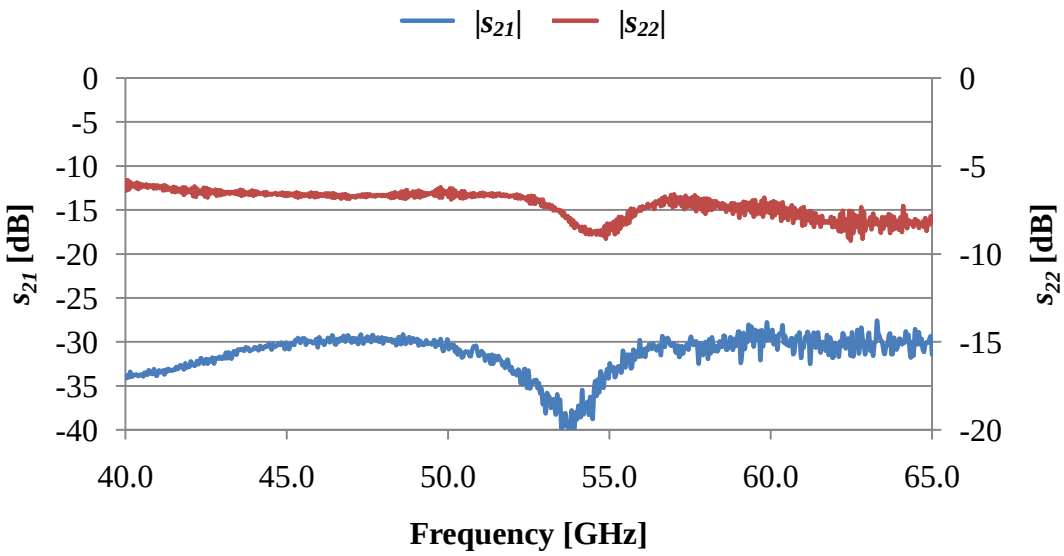

Figure 7.22. s_{21} and s_{22} measurements for LNA 1 operating with 1.5 V supply and a 1 µA base current.

Figure 7.22 shows s_{21} and s_{22} for the 1.5 V, 1 µA bias condition. The LNA achieves no gain as s_{21} is equal to -30 dB at 57 GHz. The output matching network is not optimal as s_{22} achieves -9 dB at 55 GHz.

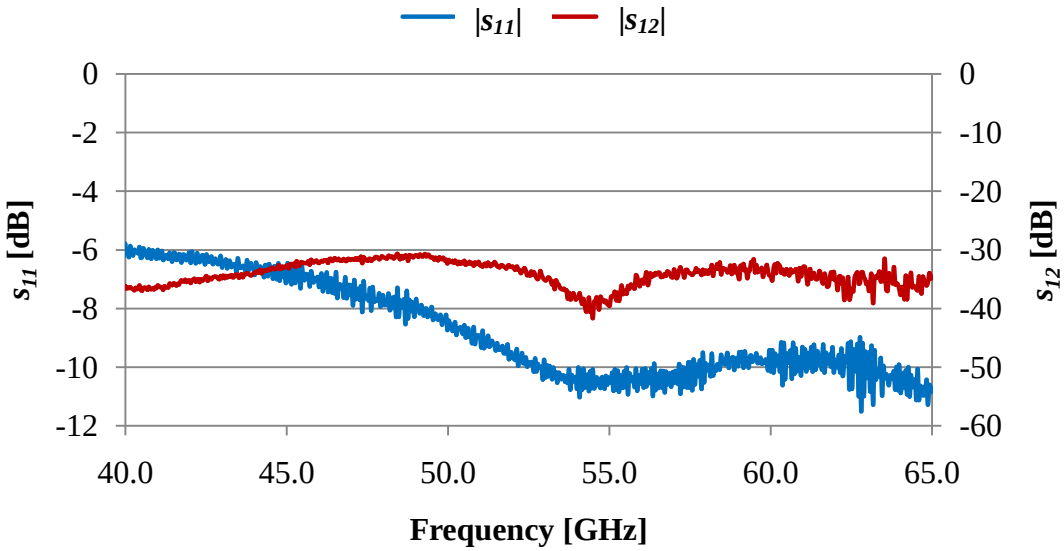

Figure 7.23. s_{11} and s_{12} measurements for LNA 1 operating with 3.5 V supply and a 10 µA base current.

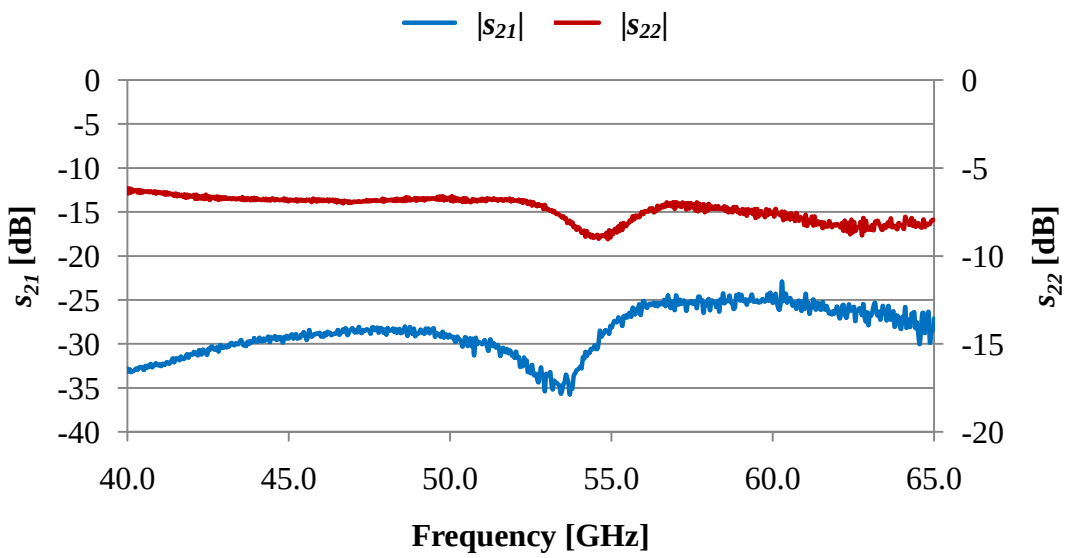

Figure 7.24. s_{21} and s_{22} measurements for LNA 1 operating with 3.5 V supply and a 10 µA base current.

Figure 7.23 and Figure 7.24 shows the *s*-parameter measurement results for the 3.5 V, 10 µA bias condition. The input reflection coefficient reaches -11 dB at 55 GHz and remains roughly at -10 dB from 54 GHz to 65 GHz. The result is slightly worse than the s_{11} measured for the 1.5 V bias condition, showing a very small dependency on the bias condition change. The gain in Figure 7.24 is unchanged when compared to s_{21} measured in Figure 7.22. This is due to the large resistive loss discussed in section 7.3.2 which completely corrupts the forward voltage gain. The s_{22} measured response in Figure 7.24 is identical to the measured s_{22} in Figure 7.22 which is due to the output matching network being bias independent. The s_{22} parameter achieves -9 dB at 55 GHz.

7.4 CONCLUSION

This chapter presented the measurement data obtained for the S-CPW transmission lines and the LNA. The raw S-CPW transmission line measurements are de-embedded and compared with the simulation results. The simulation results approximated the de-embedded results only up to 20 GHz. At frequencies higher than 20 GHz, the simulation results underestimate the coupling losses between the signal and the ground conductors, and predictably overvalue the *Q*-factors. The 2.5D IE3D simulator was not able to predict the associated losses up to 65 GHz. The transmission line parameters are extracted and show that the attenuation constant for the measured S-CPW lines are much higher than the simulated attenuation results. The calculated *Q*-factor for all the measured S-CPW lines is

also much lower than the predicted simulation results. *Q*-factors in the range of 10 were obtained which is a reduction by a factor of 5 when compared to the *Q*-factor simulation results. Even though the measured *Q*-factors were lower and the performance between the Narrow and Wide S-CPW transmission lines is diminutively discernable, the Wide S-CPW lines provide higher *Q*-factors than the Narrow S-CPW lines. This result stems from the inclusion of the floating metal shield which enables the signal-to-ground spacing to widen without increasing the inductor losses. The widening of the signal-to-ground spacing increases the magnetic energy storage of the S-CPW lines which invariably increases the *Q*-factor.

The LNA measurements are performed by characterising LNA 1 at DC to determine the biasing conditions. A significant resistive loss is obtained between the transistors of LNA 1 which resulted in LNA 1 not attaining the biasing design requirement. High frequency measurements are performed at two alternative biasing conditions: at the design supply voltage of 1.5 V, resulting in a base current of 1 µA, and at a supply voltage of 3.5 V, resulting in the required base current of 10 µA. The input matching network performed optimally at both biasing conditions and provided an input return loss lower than -10 dB from 54 GHz to 65 GHz. The output matching network achieved -9 dB output reflection at 55 GHz and remained unchanged at both biasing conditions. The resistive loss between the transistors unfortunately prohibited any gain from the amplifier. The reason for the resistive loss is attributed to process variation since DRC, LVS, electron migration and wire resistance rules were adhered to.

The connection problem in LNA 2 disallowed any characterisation and measurements to be performed. A comparison between LNA 1 and LNA 2 is therefore not realisable. The cost implication trying to etch the nitride layer and repair the connection break prohibited the mending effort. Physically removing the nitride layer also proved unsuccessful as the nitride layer is deposited onto the chip for the dedicated purpose to provide scratch resistance.

CHAPTER 8: CONCLUSION

8.1 INTRODUCTION

This chapter summarises the research and the data gathered throughout the dissertation to provide critical evaluation of the hypothesis. Chapter 1 and chapter 2 presented a literature review on the hypothesis which stated that the performance of a mm-wave LNA implemented in a Si technology can be improved by improving on-chip inductor performance. The research focussed on the fundamental understanding of the associated forms of losses an on-chip mm-wave inductor experiences and the various techniques to address performance degradations. Chapter 3 discussed the research methodology followed to prove the hypothesis. Chapter 4, chapter 5 and chapter 6 documented the inductor and LNA design, modelling and simulation including the layout and PCB design, respectively which is an element of the experimental setup required to validate the hypothesis. Chapter 7 discussed the results of the experimental setup and provided an assessment of the inductor and LNA performance.

8.2 CRITICAL EVALUATION OF HYPOTHESIS

The following section lists some of the important aspects of the research work including the process, implementation and outcome.

- Of the various forms of losses a mm-wave inductor experiences, substrate losses proved particularly severe and required several techniques and process related considerations to address this performance degradation in order to improve the *Q*-factor.

- A patterned floating metal shield together with the CPW transmission line proved to be the preferred inductor structure at mm-wave frequencies. The CPW transmission line confines most of the electric field density between the signal and ground conductors while the patterned floating metal shield is placed below the CPW to prevent the electric field from penetrating the substrate. The floating metal shield is only effective when the shield is subjected to a net electric flux from the inductor, equals to zero.

- The patterned floating metal shield provides a two-fold benefit, firstly by adding a capacitance to the inductor, which allows the signal-to-ground spacing of the inductor to be altered to maintain a constant characteristic impedance, and secondly slowing down the propagation velocity of the travelling wave, decreasing the effective transmission line length to achieve a specific inductance.

- The addition of the patterned floating metal shield permits the signal-to-ground spacing of the CPW to be altered as the chosen geometric parameter to improve the *Q*-factor. Various other geometric parameters are analysed and discussed in literature, but according to the author's knowledge, the signal-to-ground spacing has not been previously examined for the 130 nm SiGe BiCMOS technology node specifically at 60 GHz. The *Q*-factor of the inductor has been characterised over the chosen signal-to-ground spacing allowing optimisation over this parameter [**72**].

- Two identical transmission line geometries except for different signal-to-ground spacings are compared to investigate the *Q*-factor improvement. Simulation and measurement results up to 65 GHz reveal that higher *Q*-factors are obtained by increasing the signal-to-ground spacing.

- The EM simulations are conducted in IE3D. The simulation and measurement inductor comparison proved that the simulation results are only valid up to 20 GHz. The dielectric losses in particular due to the coupling between the signal and ground conductors are underestimated at frequencies higher than 20 GHz.

- Two single stage cascode LNAs are realised to investigate the performance improvement of a higher *Q*-factor inductor in the output matching network of the LNA. The simulation results revealed that the higher *Q*-factor inductor in the output matching network provided a 5 dB improvement in the input and output matching performance together with a narrower and sharper bandwidth response. No significant improvement in noise and gain performance was obtained but the small discrepancy obtained in the NF_{min} response is attributed to the lower series resistive losses of the higher *Q*-factor S-CPW transmission line.

- The noise performance of the LNA is dictated by the intrinsic noise parameters of the transistors and optimal noise matching of the LNA. The simulation results show that the NF improvement due to higher *Q*-factor inductors is attributed to the lower resistive inductor losses.

- Cadence Virtuoso software package is used as the circuit simulator for the LNA. The inductor models consist of ideal component equivalent circuits and are incorporated into the Cadence Virtuoso circuit schematic.

8.3 LIMITATIONS AND ASSUMPTIONS

Only a single stage cascode amplifier is utilised as the LNA configuration as opposed to multi-stage or cascade amplifiers typically implemented in literature, and secondly that only one inductor instead of several or all of the inductors in the LNA matching networks is replaced with a higher *Q*-factor inductor. These limitations enable critical deductions to be made to validate the hypothesis.

Although the NF and linear performance of the LNAs are simulated and theoretically investigated to show the impact of the higher *Q*-factor inductor in the output matching network, no NF or linearity measurements were conducted due to the negligible gain of the amplifier.

8.4 FUTURE WORK AND IMPROVEMENTS

Higher accuracy simulation results are attainable when utilising a full 3D simulator instead of the 2.5D simulator used in this work. Higher accuracy modelling and characterisation will lead to an optimised signal-to-ground spacing of the transmission lines for the chosen geometry parameters for the 0.13 µm SiGe BiCMOS technology node which will correlate more closely with measurement results. The modelling and characterisation of the transmission lines could additionally be extended to frequencies higher than 65 GHz. Furthermore, the signal width of the transmission lines is identified as an additional geometry parameter that can potentially increase the *Q*-factor of the inductors.

An off-chip de-embedding procedure is used in this work where only the shunt and fringing capacitance of the probe pads is de-embedded. Full de-embedding algorithms

could be included on-chip to enable effective de-embedding of the probe pad parasitic components to obtain more accurate tangible inductor performance.

The *Q*-factor performance of the measured inductors became difficult to interpret at frequencies above 40 GHz. This is attributed to the electrical length of the transmission lines approaching a quarter of the effective wavelength. Improved off-chip de-embedding procedures together with shorter electrical length transmission lines will result in less noisy extracted performance parameters.

The lumped equivalent circuits created to model the electrical characteristics of the inductors which forms part of the matching networks of the LNA, is only valid for a 5 GHz bandwidth. More accurate wideband inductor models would enable improved LNA behaviour and performance prediction over a wider frequency range. The models could potentially include corner parameters, fabrication and process tolerances to enable the inductor models to function within the corner and Monte Carlo simulation environment.

The LNA is realised with the primary focus of achieving high gain and low NF and was achieved by trading off linearity. An optimised trade-off between the multi-dimensional LNA characteristics can be achieved.

The scope of the research is limited to passive inductors and the contribution higher *Q*-factor inductors have on the performance of LNAs. The application for higher *Q*-factor inductors at mm-wave frequencies is not limited to LNA configurations and may be realised in other transceiver system building blocks i.e. improve the performance of PAs or the phase noise performance of VCOs.

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