

**An integrated CMOS optical receiver with clock and  
data recovery circuit**

by

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## SUMMARY

### **An integrated CMOS optical receiver with clock and data recovery**

#### **Circuit**

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**Keywords:** Optical receiver, photodetector, front-end, inductive peaking, clock and data recovery circuit, oscillator, phase-locked loop, frequency-locked loop.

Traditional implementations of optical receivers are designed to operate with external photodetectors or require integration in a hybrid technology. By integrating a CMOS photodetector monolithically with an optical receiver, it can lead to the advantage of speed performance and cost.

This dissertation describes the implementation of a photodetector in CMOS technology and the design of an optical receiver front-end and a clock and data recovery system. The CMOS detector converts the light input into an electrical signal, which is then amplified by the receiver front-end. The recovery system subsequently processes the amplified signal to extract the clock signal and retime the data.

An inductive peaking methodology has been used extensively in the front-end. It allows the accomplishment of a necessary gain to compensate for an underperformed responsivity from the photodetector.

The recovery circuits based on a nonlinear circuit technique were designed to detect the timing information contained in the data input. The clock and data recovery system consists of two units viz. a frequency-locked loop and a phase-locked loop. The frequency-locked loop adjusts the oscillator's frequency to the vicinity of data rate before phase locking takes place. The phase-locked loop detects the relative locations between the data transition and the clock edge. It then synchronises the input data to the clock signal generated by the oscillator.

A system level simulation was performed and it was found to function correctly and to comply with the gigabit fibre channel specification.

## OPSOMMING

### 'n Geïntegreerde CMOS optiese ontvanger met klok en data herwinnings stroombaan

deur

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**Sleutelwoorde:** Optiese ontvanger, fotodetektor, voorkant, induktiewe piek metode, klok en data herwinning stroombaan, ossillator, fase sluit lus, frekwensie sluit lus.

Tradisionele implementasies van optiese ontvangers is of ontwerp om met eksterne fotodektors te werk of hibriede integrasie tegnologie motet gebruik word. Deur 'n CMOS foto detektor monolities te integreer met die optiese ontvanger kan voordele in terme van spoed, werksverrigting en koste verwag word.

Hierdie dissertasie beskryf die implementasie van 'n foto detektor in CMOS tegnologie asook die ontwerp van 'n optiese ontvanger voorkant en 'n klok en data herwinning stelsel. Die CMOS detektor verander die optiese inset na 'n elektriese sein wat daarna versterk word by die ontvanger voorkant. Die herwinning stroombaan prosesseer dan die versterkte sein om die klok data te verkry en die data te hersinkroniseer.

Induktiewe piek metodes was ekstensief in dit voorkant gebruik. Addisionele versterking word hierdeur verkry om te kompenseer vir die swak respons van die foto detektor.

Die herwinning stroombane is gebaseer op 'n nie-lineêre stelsel tegniek wat ontwerp is om die sinkronisasie informasie uit die data te herwin. Die klok en data herwinning stelsel bestaan uit twee eenhede naamlik 'n frekwensie-sluit-lus en 'n fase-sluit-lus. Die frekwensie-sluit-lus verstel die ossillator se frekwensie in die bereik van die data tempo voordat fase sluiting plaasvind. Die fase-sluit-lus bepaal die relatiewe posisies van die data-en klok transisies.

'n Stelsel vlak simulatie is gedoen, en daar was gevind dat dit korrek funksioneer en voldoen aan die gigabit vesel optiese spesifikasie.

## LIST OF ABBREVIATIONS

AMS	Austria Micro System International
BER	bit-error rate
CDR	clock and data recovery
CM	common-mode
CMFB	common-mode feedback
DETFs	double-edge-triggered flip-flops
FD	frequency detector
FLL	frequency-locked loop
IC	integrated circuit
ISI	intersymbol interference
LA	limiting amplifier
LAN	local area networks
LPF	low pass filter
NRZ	nonreturn-to-zero
OTA	operational transconductance amplifier
PFD	phase/frequency detector
PLL	phase-locked loop
PRBS	pseudorandom bit sequence
RGC	regulated cascode
SML	spatially modulated light
SNR	signal to noise ratio
TIA	transimpedance amplifier
VCO	voltage-controlled oscillator
TM	typical-mean
TSPC	true-single-phase-clock
WO	worst-one
WP	worst-power
WS	worst-speed
WZ	worst-zero

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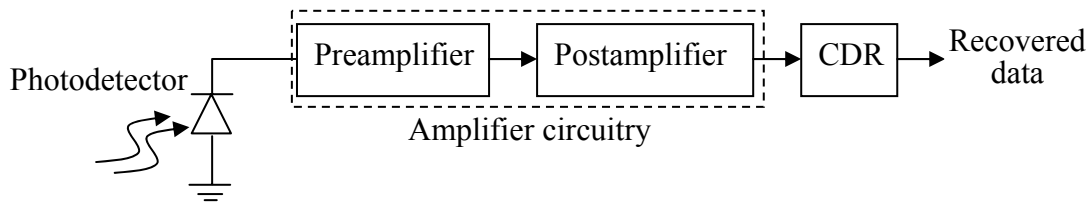
## CHAPTER 1

### INTRODUCTION

The rapid global growth of information technology has resulted in the need to transport large volumes of data across broadband networks such as optical communication infrastructures. Low loss and high bandwidth can easily be achieved with optical fibres and data can be transported over vast distances without significant loss of signal integrity. However, there is an increasing challenge for users to directly and seamlessly access high capacity information from networks. The multimedia used by users is not efficient for high speed operations and the throughput of networks is thus limited. The need for high speed communication is therefore becoming more prominent.

Data transportation can easily be accomplished by implementing short distance applications such as optical-based local area networks (LAN). The success of these systems has encouraged the trend of and opportunities for optical communication technology. Traditionally, performance rather than cost has been the design goal of optical receivers. As a result, high-speed semiconductor technologies rather than the CMOS process have been widely implemented and have resulted in prohibitively expensive receivers. With the expansion of optical communications it has become necessary to design the system for both performance and cost. The integration in CMOS technology, together with its improved functionality and performance, has accelerated the implementation of CMOS integrated circuits.

A typical optical system consists of a transmitter, an optical fibre and a receiver. On the transmitting side of the optical network, modulated information is processed by an optical source to generate an optical signal. This optical signal is transmitted through an optical fibre and finally impinges on the photodetector at the receiving end. The receiver consists of an optical detector, amplifier circuitry and a clock and data recovery (CDR) circuit, as depicted in Figure 1.1.



**Figure 1.1 Optical receiver.**

The photodetector converts the optical signal into an electric current which is then converted into a voltage signal and processed by the amplifier circuitry to boost the voltage swings. The final module of the receiver, the synchronous stage, retimes and recovers the original data.

In order to achieve high bandwidth operation, high volume production and low cost fabrication, a silicon-based photodetector has to be realised monolithically with CMOS receiver circuits. However, the ability to realise high-performance CMOS detectors presents a problem for the integration of optical communication systems and places a tight design constraint on sensitivity and responsivity. The objective of this dissertation is to design a fully integrated optical receiver with a standard CMOS process while achieving acceptable bit-error rate (BER) performance at gigabit data rate.

## 1.1 SUMMARY OF RELATED WORK

### 1.1.1 Photodetectors

In optical communications photodetectors are required to convert incident photons to an electric current. When light pulses hit the detector, a fraction of photons penetrates the detector, generating a photocurrent through the creation of electron-hole pairs. The amount of the current generation, hence the responsivity ( $\mathfrak{R}$ ) of the detector, is affected by the characteristics of the semiconductor material of the detector, as described in Equation 1.1 [1],

$$\mathfrak{R} = \frac{\eta q}{h\nu}, \quad (1.1)$$

where  $\eta$  is the quantum efficiency (which is strongly related to the absorption coefficient for light at the wavelength of operation and the geometry of the detector),  $q$  is the unit electron charge,  $h$  is Planck's constant and  $\nu$  is the frequency of the photon. The absorption coefficient of the material is a function of the wavelength. Thus, in order to maximise the

responsivity, the incident light wavelength should be spectrally matched to the operating region of the wavelengths of the detectors. The sensitivity of the detector is also influenced by the amount of photons received. By widening the photon reception window, the sensitivity can be increased. However, this also increases the parasitic capacitance and trades the system speed for sensitivity.

Overall, detector capacitance and/or the carrier transient time are the major factors that determine the speed of photodetectors. For high speed operation, such as gigabit applications, it is necessary to have a detector that provides low capacitance and fast carrier transient time, while maintaining reasonable sensitivity.

The following discussion explains some detector implementations.

High responsivity can be obtained by implementing the n-well and p-substrate in a standard CMOS process at a wavelength of 850 nm [2]. Nevertheless, the random motion of carriers of the diffusion process of this photodetector results in long current tails in impulse response, hence impeding the detector speed.

Woodward *et al.* realized a detector based on the concept of using the n-well as a screening terminal [2]. The slowly responding carriers diffuse to the substrate, after which they are screened by the n-well from a set of lateral interdigitated p-n junctions that forms the active contact of the detector. However, this methodology results in a very limited responsivity and high junction capacitance.

The detector based on the twin-tub CMOS process [3] that uses the low doped epitaxial layer to form the intrinsic region of the p-i-n photodiode can achieve reasonable speed and quantum efficiency. However, this approach has the danger of latch-up unless appropriate design measures are taken. Furthermore, a protection mask is required to block out the threshold-adjusting implantation from the n<sup>-</sup> epitaxial layer across which the detector is to be realised.

Spatially modulated light (SML) detectors presented in [4] implement the masked and unmasked regions of the p<sup>-</sup>n junctions to amplify the spatial gradient in carrier concentrations. The differential approach eliminates the long current-tail effect and leads to dramatic speed improvement. Unfortunately, this approach trades responsivity for speed.

### 1.1.2 Front-End

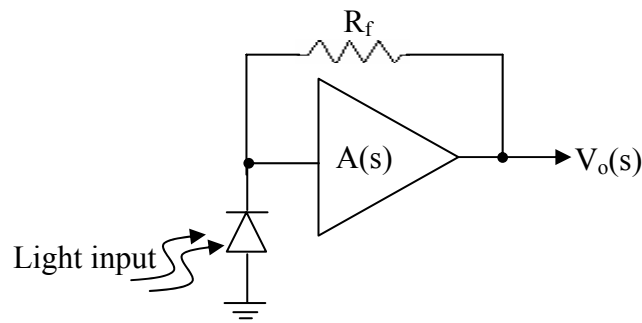
After the conversion of the incident light to an electric current by the photodetector, a low-noise, high-bandwidth preamplifier must be implemented so that this current can be converted to a sufficiently large voltage. A string of postamplifiers is then cascaded to the preamplifier for further amplification to a voltage level sufficient for the reliable operation of the succeeding circuits.

#### 1.1.2.1 Preamplifier

Preamplifiers are critical in optical receivers because speed, sensitivity and the noise performance of optical communication systems are mainly determined by the front-ends. Low-impedance amplifiers, high-impedance amplifiers and transimpedance amplifiers (TIA) are commonly used preamplifiers in optical communication receivers [1].

In a low-impedance amplifier, a sufficiently small value for the bias resistor has to be chosen to achieve a preamplifier bandwidth that is greater than or equal to the signal bandwidth. The voltage developed across the input impedance and the bias resistor is, thus, relatively small and results in a low receiver sensitivity. The thermal noise of the bias resistor can be reduced to a minimum by selecting a very large resistor. This results in an alternative design: the high-impedance amplifier. Although all sources of noise in the high-impedance amplifier are reduced to an absolute minimum and it has been proved to have a very high sensitivity, the large input RC time constant results in a front-end bandwidth that is less than the signal bandwidth. Integration and equalisation techniques have to be employed for the compensation. This causes the circuits to suffer from a limited dynamic range.

Designs based on transimpedance amplifiers overcome the drawbacks of the high-impedance amplifiers. Compromises are achieved between the wide bandwidth of the low-impedance configuration and the high sensitivity of the high-impedance design. In the transimpedance amplifier, the negative feedback is implemented (as shown in Figure 1.2) through a feedback resistor to provide a wide dynamic range, a high bandwidth and a good sensitivity. Due to the above-mentioned factors, transimpedance amplifiers are the most popular approach for the front-end implementations in optical receiver systems.



**Figure 1.2 Transimpedance amplifier.**

Depending on the application, the multiple amplifying stages may be necessary. The maximum achievable value of the transimpedance amplifier open-loop gain is ultimately restricted by the propagation delay and phase shift of the amplifying stage within the feedback loop. Because a constant gain-bandwidth product is maintained at all times, at higher speed operations, the open loop gain is necessarily reduced and the number of amplifying stages is decreased to minimise the excessive phase shift. As a result, a significant amount of noise is produced by the feedback resistor. Thus, tradeoffs between speed, transimpedance gain and sensitivity exhibit as the design challenges for a high speed TIA.

Over the past decades, several TIA configurations have been developed. Toumazou and Park [5] have reported high speed and low noise common-gate and common-source transimpedance amplifiers. However, these configurations require dual supplies and only the simulation results were provided. The CMOS multi-stage TIAs [6] may become unstable.

Regulated cascode (RGC) techniques have been implemented recently to efficiently isolate the input capacitance from the performance determination [7, 8, 9]. The RGC circuit behaves like a common-gate transistor with a large transconductance as a result of the local feedback stage. Schrodinger et al. [10] have implemented a folded cascode technique for the transimpedance amplifier. The design can work at low supply voltage and the Miller capacitances can be reduced effectively. Both the RGC and folded cascode-based TIAs provide high bandwidths and reasonable equivalent input noise currents. However, with a low responsivity photodetector, these input noise currents are not low enough to achieve the required bit-error rate performance.

In Razavi [11], the feedback resistor is replaced by two capacitors (the gain definition network). One capacitor is used to sense the voltage across the second capacitor and return a proportional current to the input. If the gain of the amplifying stage within the feedback loop is much greater than unity, then the circuit can operate as a current amplifier. The equivalent input noise of this configuration is effectively reduced because the gain definition network does not contribute noise. Although the design contributes only 4.5 pA/ $\sqrt{\text{Hz}}$  at a data rate of 622 Mb/s, at higher data rates a slightly higher input noise spectrum is produced and the TIA fails to meet the performance requirement.

A different approach for the transimpedance amplifier is implemented using a common-drain-common-source configuration [12]. In the design, an input source follower is placed before the gain stage to prevent the Miller capacitance effect and hence increase the closed loop bandwidth. It has been reported that an input noise current density of only 4.6 pA/ $\sqrt{\text{Hz}}$  was measured at a data rate of 1 Gb/s. Unfortunately large transistors with transistor widths in the range of 100  $\mu\text{m}$  are required to achieve high gain and reduce the noise current. As a result, the bandwidth becomes limited. In Nakahara *et al.* [13], the transimpedance amplifier is implemented by using a single stage CMOS inverter that takes the advantage of the NMOS and PMOS transistors at the input to achieve high gain [14]. The amplifier was reported to achieve a high sensitivity of -27 dBm at 1Gb/s and a bandwidth of over 1 GHz with the feedback resistor set as high as 5 k $\Omega$ .

### **1.1.2.2 Postamplifier**

The postamplifier must have a voltage gain large enough to provide sufficient voltage swing for the subsequent CDR circuit and a large enough bandwidth to amplify the signal with negligible intersymbol interference (ISI). It also provides isolation for the transimpedance amplifier from the subsequent synchronous circuits, preventing the corruption of the data signal from the clock feed-through of the synchronous circuits.

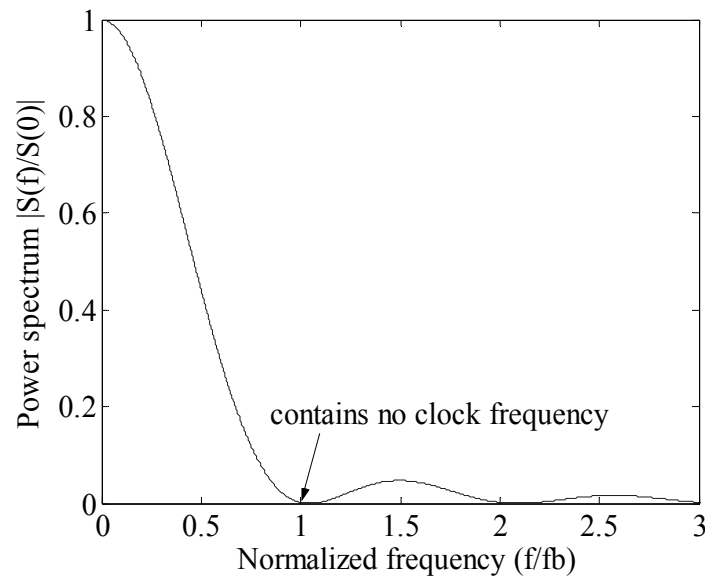
Gilbert gain cells [15] have been widely used in many communication systems but they consume a great voltage headroom and require level-shift circuits between the stages. Thus, at a low supply voltage, the utility of the Gilbert gain cell becomes limited.

Sackinger and Fischer [16] have modified a conventional CMOS limiting amplifier (LA), consisting of NMOS differential pairs, to achieve high bandwidth. The inverse scaling technique is applied to all gain stages to effectively reduce the total load capacitance and

improve the frequency response. The stage bandwidth is further enhanced with the implementation of inductive shunt-peaking techniques [16, 17].

In Ingels and Steyaert [18], the configuration of the postamplifier is based on a string of modified, biased high-speed inverters that achieve both the linear and limiting amplification. The biasing of the postamplifier is performed through an offset tolerant replica circuit.

### 1.1.3 Clock and Data Recovery Circuit



**Figure 1.3 NRZ power spectrum.**

The information transmitted over the optical network is generally encoded as nonreturn-to-zero (NRZ) data stream. These NRZ signals do not contain any information about the clock signal or the spectral component at the data rate, as shown in Figure 1.3. Only by determining the minimum spacing between consecutive zero crossings of the data stream can the clock signal be derived from the data. This information can be extracted through the implementation of non-linear circuits, such as high Q-filters or phase-locked loops (PLL) [19]. PLLs are often the solution, due to the difficulty in integrating monolithically high Q-filters with other circuits.

Transmitting data through an optical network, consisting of a series of regenerators, results in a jittered data signal. Thus, jitter generation of regenerators is stringently specified. This specification is closely related to the closed-loop bandwidth of the system and has to be traded off between jitter suppression, capture range and acquisition range [20]. With the

unaided CDR circuit, the acquisition range is limited by the loop bandwidth that tightens the constraints of designing PLLs. When the difference between the data frequency and the voltage-controlled oscillator (VCO) frequency is larger than roughly the loop bandwidth, the PLL will fail to lock. By increasing the acquisition range of the phase-locked loop, the locking problem can be solved. However, this results in an unacceptable high output jitter. In modern designs, this problem is overcome by incorporating PLLs with a frequency acquisition scheme [15]. Two different schemes are generally adapted: one that incorporates a phase/frequency detector (PFD) as part of a single phase- and frequency-locked loop and the other that implements a dual loop frequency acquisition.

A single loop CDR consists of a PFD that derives phase and frequency errors between the input data and VCO signals. These error signals are fed back to the VCO to cancel the static phase error and increase the frequency capture range. The PFD circuit is generally implemented in digital mode. It is required to convert the two output states to an average voltage through a charge pump and a low pass filter [21, 22]. The action of current pumping creates significant ripple and produces great jitter at the VCO output.

In a dual loop frequency acquisition, two control inputs are fed to the VCO input. One control provides a low sensitivity tuning driven by the main analogue loop; and the second control, driven by a digital frequency-locked loop (FLL), provides a wide range tuning [20, 21]. When the VCO frequency is tuned to the vicinity of the signal frequency, the FLL remains relatively quiet and does not produce high jitter.

## 1.2 CONTRIBUTION OF THIS STUDY

The emphasis on cost and modest sensitivity targets for optical interconnect and short-distance optical communication systems such as local area networks operating at short wavelengths ( $\sim 850$  nm or shorter), has encouraged the integrated silicon solution. CMOS detectors allow short wavelength detection of light due to the fact that the silicon-based detector has a cutoff wavelength of approximately  $1.06 \mu\text{m}$  and a peak sensitivity near the infra-red region [1].

Conventional CMOS optical receivers are incapable of realising high-performance, silicon-based photodetectors. Such detectors are often implemented externally or integrated into receiver circuits with hybrid technology. With external implementation, the input



capacitance from the interconnections and bonding wire inductance tends to be large and limits the bandwidth of the receiver-amplifier circuit. Hybridised photodetectors have been used widely to solve the problem. This is expensive to manufacture, however. The aim of this dissertation is to develop an optical receiver system with a monolithically integrated photodetector in commercial CMOS technology. The system is designed to perform at 1 Gb/s application.

## 1.3 PRESENTATION OF THE DISSERTATION

### 1.3.1 Objective

The objective of this dissertation was to design an integrated CMOS optical receiver for gigabit optical communication systems. The following describes the overall system specifications that had to be achieved [23, 24]:

- The photodetector, front-end receiver and CDR circuit had to be integrated to provide a single chip CMOS integrated circuit (IC) solution using a standard 0.35  $\mu\text{m}$  CMOS process technology.
- The circuit had to operate from a single 3.3 V supply voltage.
- The system had to comply with the 1 Gb/s fibre channel specification.
- The photodetector optical reception window had to be optimised for the 50  $\mu\text{m}$  or 62.5  $\mu\text{m}$  optical fibre, and the operating region of the wavelengths of the detectors had to be within the range from 770 nm to 860 nm.
- The receiver sensitivity had to be greater than or equal to -17 dBm.
- The receiver had to operate within the BER objective of  $10^{-12}$ .
- The total output jitter of the IC had to be less than 600 ps peak-to-peak to comply with the jitter budget specification.

### 1.3.2 Dissertation Outline

**Chapter 1** A brief introduction is presented.

**Chapter 2** The choice of photodetector is discussed and the chosen detector is analysed.

**Chapter 3** The analysis and design of the preamplifier is discussed and the circuit is evaluated by means of simulation.

**Chapter 4** The design, layout and simulation of the CDR circuit are discussed.

**Chapter 5** The overall system is evaluated.

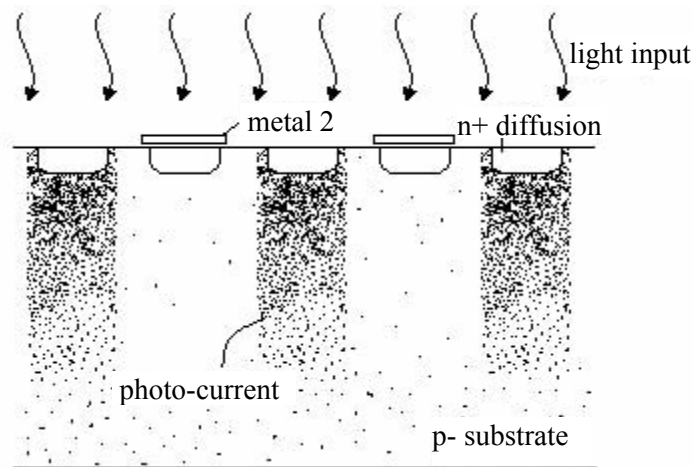
**Chapter 6** Conclusions to this dissertation are provided.

## CHAPTER 2

### PHOTODETECTOR

#### 2.1 INTRODUCTION

In order to achieve high-speed performance, such as that required for gigabit applications, the SML-detector is preferable. The design is based on the differential structure (as shown in Figure 2.1). When the light strikes the detector, carriers are generated only below the unmasked zones and contribute to the major amount of the immediate current output. The random motion diffusive carriers in the substrate will finally reach  $pn$  junctions as time progresses and will yield the deferred current output and contribute partially to the immediate current. While taking the difference between the response of the immediate carriers and that of the deferred carriers, the long diffusive current response is eliminated, and improves dramatically the speed performance that trades off with the responsivity.



**Figure 2.1 Cross-section of the SML detector (adapted from [4]).**

The low responsivity can be partially compensated for by the detector capacitance. It has been shown that the sensitivity of preamplifiers is proportional to  $\sqrt{C_D/\mathfrak{R}}$ , where  $C_D$  and  $\mathfrak{R}$  are the capacitance and the responsivity of the detector respectively [25]. The detector capacitance is mainly determined by the junction capacitance because the photodiodes generally operate under the reverse-bias condition [26]. Thus, by increasing the reverse-bias voltage, which in turn increases the depletion width, the junction capacitance can be decreased.

## 2.2 IMPLEMENTATION

The junction capacitance of the detector can be calculated as follows [26]:

The junction potential that exists across the  $pn$  junction is

$$\phi_j = V_T \ln \left( \frac{N_A N_D}{n_i^2} \right), \quad (2.1)$$

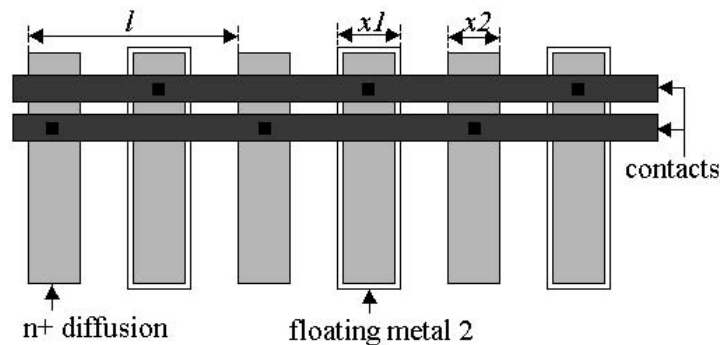
where  $N_A$  (atoms/cm<sup>3</sup>) is the acceptor impurity concentration,  $N_D$  (atoms/cm<sup>3</sup>) is the donor impurity concentration,  $n_i = 10^{10}$ /cm<sup>3</sup> is the intrinsic carrier density in silicon at room temperature and  $V_T \approx 0.025$  V is the thermal voltage. For  $n^+p^-$  junction between the  $n^+$  active implantation and the  $p^-$  substrate of the 0.35  $\mu\text{m}$  CMOS technology,  $N_D \approx 3.3 \times 10^{19}$ /cm<sup>3</sup> and  $N_A \approx 1.3 \times 10^{15}$ /cm<sup>3</sup> [27],  $\phi_j \approx 0.842$  V. With the junction potential known, the total width of the depletion region for an applied reverse-bias voltage  $v_R$  is

$$w_d = x_n + x_p = \sqrt{\frac{2\varepsilon_S}{q} \left( \frac{1}{N_A} + \frac{1}{N_D} \right) (\phi_j + v_R)} = w_{d0} \sqrt{1 + \frac{v_R}{\phi_j}}, \quad (2.2)$$

where  $x_n$  and  $x_p$  are the junction depths from the metallurgical junction on the  $n$ -type material and  $p$ -type material respectively,  $\varepsilon_S$  is the permittivity of silicon and  $q$  is the electronic charge.

The capacitance of the reverse-biased  $pn$  junction is then given by

$$C_j = \frac{\varepsilon_S A}{w_d} = \frac{\varepsilon_S A}{w_{d0} \sqrt{1 + \frac{v_R}{\phi_j}}}. \quad (2.3)$$



$l$  (grid periodicity): 5.6  $\mu\text{m}$ .

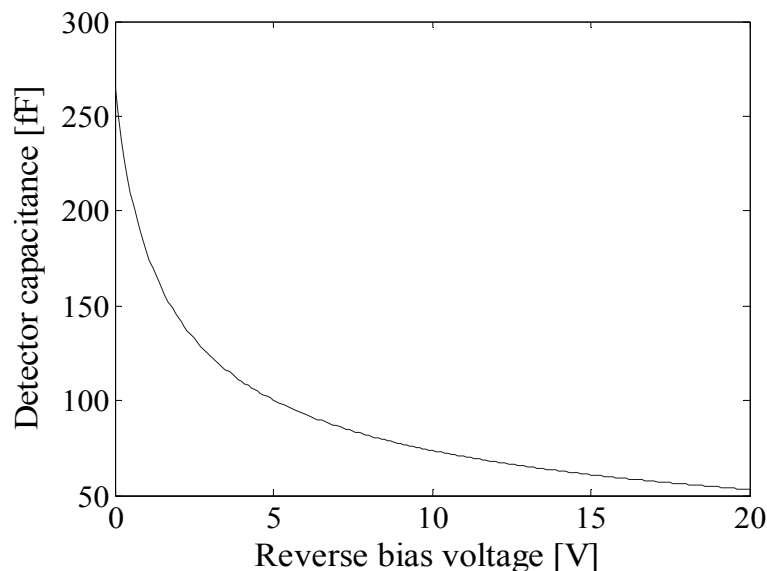
$x1$ : 1.8  $\mu\text{m}$ .

$x2$ : 1.3  $\mu\text{m}$ .

**Figure 2.2 Six-finger SML detector top view.**

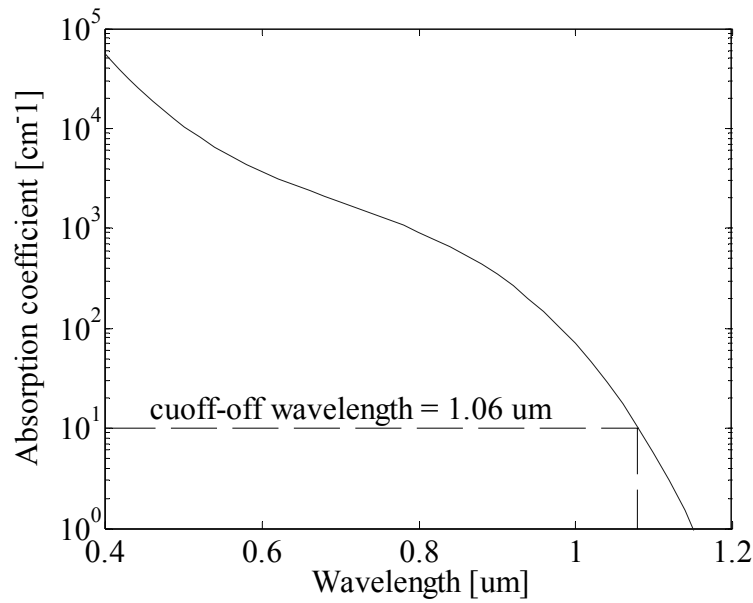
The standard fibre core diameter is 50  $\mu\text{m}$  or 62.5  $\mu\text{m}$  [23]. In order to receive the maximum optical power, the area of the photodetector shall be  $A_{\text{PD}_T} \approx 3906 \mu\text{m}^2$ . Thus, for a grid periodicity of 5.6  $\mu\text{m}$  (as depicted in Figure 2.2), a maximum of 22 fingers can be realised within the defined width of 62.5  $\mu\text{m}$ . The effective detector area is  $A_{\text{PD}} = (1.8 \times 62.5 \times 22) \mu\text{m}^2 = 2475 \mu\text{m}^2$ .

Figure 2.3 indicates that the junction capacitance is greatly dependent on the reverse bias voltage. As shown, it is desirable to work at a higher reverse bias voltage. However, the maximum reverse bias voltage is limited by the supply voltage and the input voltage of the transimpedance amplifier. For a reverse bias voltage of 1.6 V (from Equations 2.1 to 2.3) the width of the depletion region is computed to be 1.54  $\mu\text{m}$  and the junction capacitance is 156 fF.



**Figure 2.3 Detector capacitance vs. reverse-bias voltage for the chosen CMOS technology (the effective area of the detector is 2475  $\mu\text{m}^2$ ).**

When light (which has an energy greater than or equal to the bandgap energy of the semiconductor) strikes the surface of the detector, photons are absorbed to create electron-hole pairs. The number of electron-hole pairs created depends on the absorption coefficient of material at the wavelength of the optical source. The silicon detector has a significant absorption coefficient at wavelengths below its cutoff wavelength (1.06  $\mu\text{m}$ ). Figure 2.4 illustrates the absorption coefficient of silicon as a function of wavelength.



**Figure 2.4 Absorption coefficients versus wavelengths of silicon (adapted from [1]).**

Photon flux travels through the semiconductor exponentially [28], hence, the optical power,  $P(x)$ , at a depth of  $x$  below the surface can be defined as

$$P(x) = (1 - R_f) P_0 e^{-\alpha(\lambda)x}. \quad (2.4)$$

Here,  $R_f$  is the reflectivity at the entrance face of the photodetector,  $P_0$  is the incident optical power level and  $\alpha(\lambda)$  ( $\text{cm}^{-1}$ ) is the absorption coefficient at a wavelength of  $\lambda$ . Assume that carriers generated at the depletion layer lost by recombination are negligible and that those generated within a diffusion length of the depletion-layer edges contribute to an appreciable fraction of the recombination process. Then, at worst case, the optical power being effectively absorbed is across the depletion region. Using Equation 2.4 and assuming that the reflectivity tends to be infinitesimal, the absorbed power is derived as

$$P = P_0 (e^{-\alpha(\lambda)x_1} - e^{-\alpha(\lambda)x_2}), \quad (2.5)$$

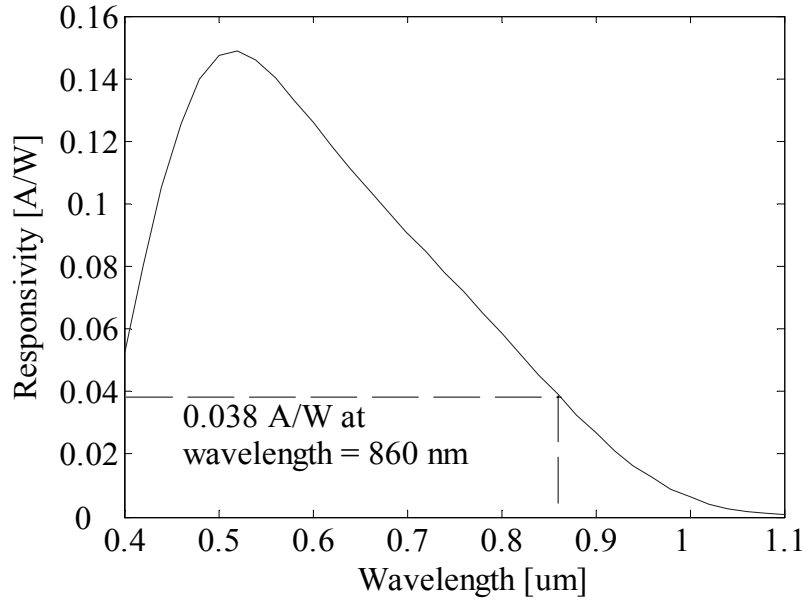
where  $x_1$  and  $x_2$  are the distance from the detector surface to the top and bottom of the depletion region respectively. The important characteristic quantum efficiency  $\eta$  of a photodetector is the ratio between the number of the electron-hole carrier pairs generated and incident photon of photon energy  $h\nu$  [1]. Relating the quantum efficiency to power absorption in Equation 2.5,  $\eta$  is

$$\eta = \frac{P/h\nu}{P_0/h\nu} = e^{-\alpha(\lambda)x_1} - e^{-\alpha(\lambda)x_2}. \quad (2.6)$$

From Equation 2.2,  $x_n$  and  $x_p$  can be derived and calculated.

$$x_n = \frac{w_{d0}}{(1 + N_D/N_A)} \sqrt{1 + \frac{v_R}{\phi_j}} = 0.061 \text{ nm}, \text{ and} \quad (2.7)$$

$$x_p = \frac{w_{d0}}{(1 + N_A/N_D)} \sqrt{1 + \frac{v_R}{\phi_j}} = 1.54 \text{ } \mu\text{m}. \quad (2.8)$$



**Figure 2.5 Responsivity of the n-diffusion p-substrate SML detector vs. wavelength.**

At the wavelength of 860 nm and  $\alpha(\lambda)$  of  $700 \text{ cm}^{-1}$ , the computed quantum efficiency is  $\eta \approx 0.11$ . Because half of the area of the photodetector is masked with floating metals, when the detector is illuminated with light, only half of the photon flux is absorbed by the semiconductor, while the rest is reflected. Thus, the effective responsivity only has a value of that computed with Equation 1.1. The responsivity of the detector at the wavelength of 860 nm is  $\mathcal{R} = 0.038 \text{ A/W}$ . The responsivity at different wavelengths is shown in Figure 2.5.

The current response of perpendicular  $pn$  junction detectors is mainly determined by the transportation of the minority carriers (which can be represented by the continuity equation as described in Equation 2.9) in the region below the depletion region [4].

$$\frac{\partial n_p}{\partial t} = D_n \frac{\partial^2 n_p}{\partial x^2} + D_n \frac{\partial^2 n_p}{\partial y^2} - \frac{n_p}{\tau_n} + g(t, y)e^{-\alpha x}, \quad (2.9)$$

here  $n_p$  is the minority carrier concentration in the p-type doped layer,  $D_n$  is the diffusion coefficient of the minority carrier in the p-type doped layer,  $\tau_n$  is the minority carrier

lifetime and  $g(t,y)$  is the electron generation rate at the lower border of the space charge region.

With appropriate boundary conditions, the photogenerated minority-carrier profile is derived as (Appendix A)

$$n_p(x, y, t) = n_{p,st}(x, y) + \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} A_{mn} e^{-((l/D_n\tau_n)+(m\pi/a)^2+(2n-1)\pi/b)^2 D_n t} \sin \frac{m\pi}{a} x \cos \frac{(2n-1)\pi}{b} y, \quad (2.10)$$

where  $n_{p,st}(x,y)$  is the steady-state solution,  $a$  and  $2b$  are the depth and the length of a single finger respectively, and the coefficients  $\{A_{mn}\}$  is

$$A_{mn} = \frac{2}{ab} \int_{-b}^b \int_0^a (n_0 - n_{p,st}(x, y)) \sin\left(\frac{m\pi}{a} x\right) \cos\left(\frac{(2n-1)\pi}{b} y\right) dx dy. \quad (2.11)$$

The current density profile as a function of frequency has been solved analytically, from which the 3-dB frequency response of the detector was derived [4]. When  $1/l$  is assumed to be much larger than  $\alpha$ , the -3-dB frequency is given by

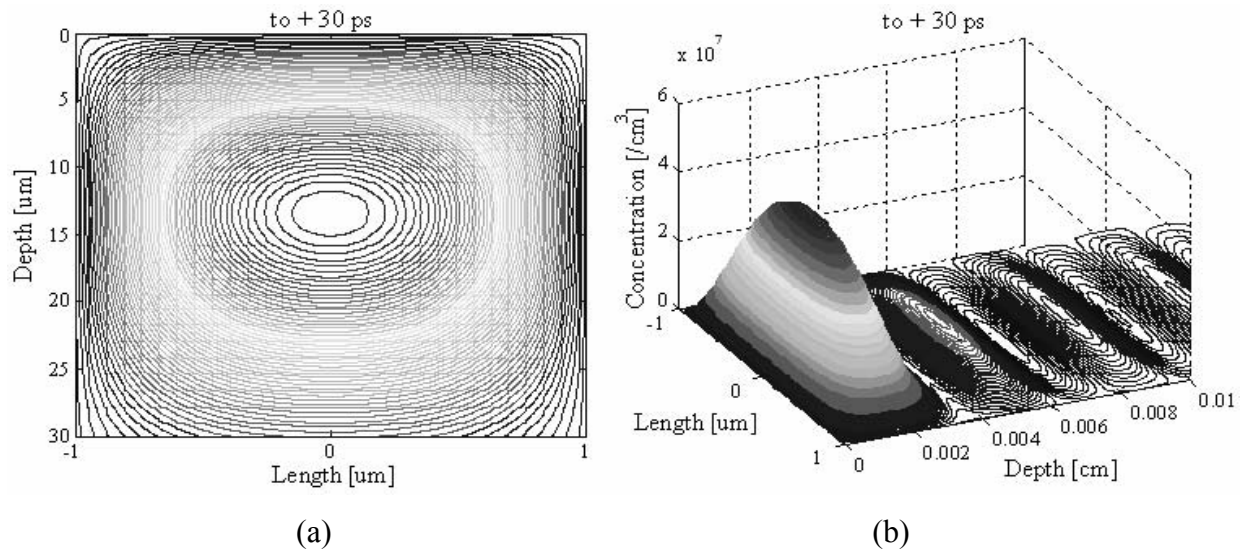
$$f_{-3dB} \approx 2\pi D_n \sqrt{3} \left( \left( \frac{1}{l} \right)^2 + \left( \frac{1}{L_n} \right)^2 \right), \quad (2.12)$$

where  $l$  is the grid periodicity of metal fingers of identical structures and  $L_n$  is the electron diffusion length. With the analogy to the argument for the transportation of the minority carriers below the space charge region, the carrier profile above the space charge region has also been postulated [4]. If the detector speed is limited by the hole diffusion, then the -3-dB frequency of the detector is

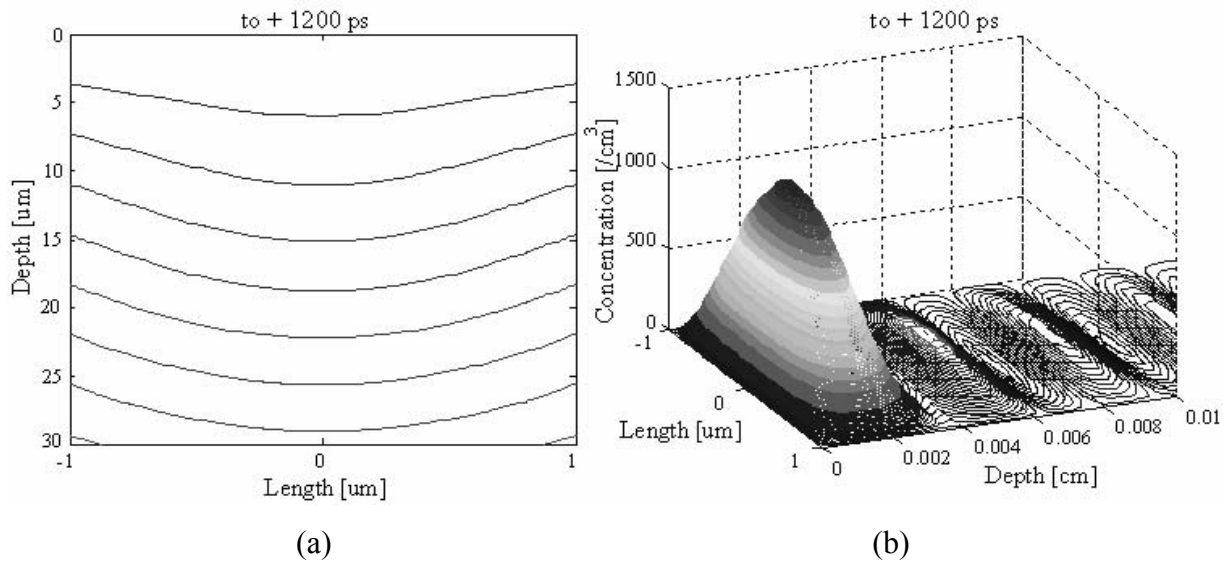
$$f_{-3dB} \approx \frac{\pi D_p}{2} \sqrt{3} \left( \left( \frac{1}{2l_x} \right)^2 + \left( \frac{1}{l_y} \right)^2 + \left( \frac{1}{L_p} \right)^2 \right) \quad (2.13)$$

with  $D_p$  being the diffusion constant of the holes in the n-doped layer,  $l_x$  the distance between the surface and the lower point of the space charge region,  $l_y$  the grid periodicity and  $L_p$  the diffusion length of the holes.

Applying the model described in Equation 2.10, Figures 2.6 and 2.7 illustrate the minority carrier profiles in the p- substrate after the diode was being illuminated for 1 ps. The profiles below demonstrate only the responses of a basic vertical  $pn$  photodiode. As shown, when time progresses, the diffusion process due to the transient response almost diminishes only after 1200 ps.



**Figure 2.6 (a) Total and (b) transient minority carrier concentrations below the  $pn$  junction 30 ps after illumination.**



**Figure 2.7 (a) Total and (b) transient minority carrier concentrations below the  $pn$  junction 1200 ps after illumination.**

The slow transportation mechanism is a result of the random motion of carriers of which the frequency response of a basic  $pn$  junction detector with an infinite dimension can be described as [4]

$$f_{standard} \approx 1.3542 \frac{(\alpha L_n + 1)^2}{2\pi\tau_n}. \quad (2.14)$$

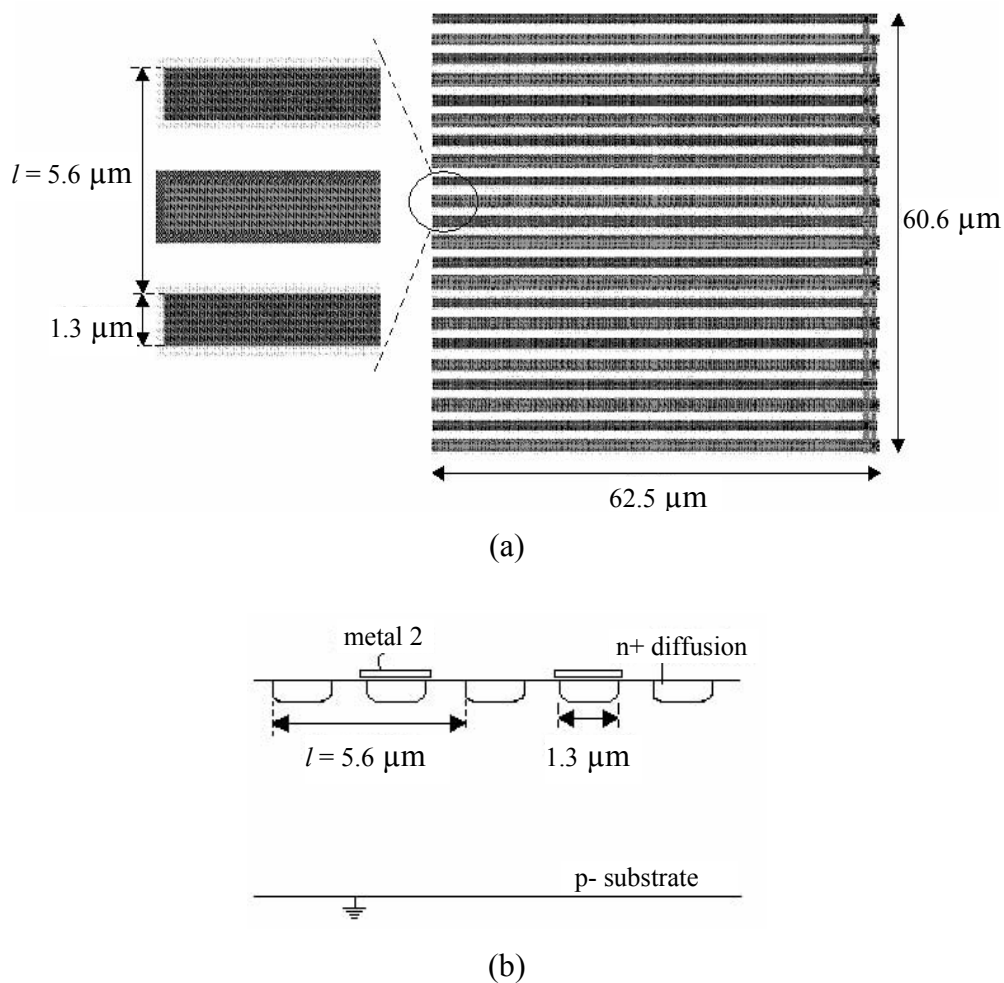
Comparing Equations 2.12 and 2.14, the speed performance of the detector is expected to improve greatly when the differential structure is implemented.



With current CMOS technology, the n+ diffusion layers are made shallow. Thus, when the detector is illuminated, the minority carriers generated in the n+ diffusion layer are immediately swept across the  $pn$  junction. This results in no diffusion in the n-doped top layer. Consequently, it reduces the maximum hole diffusion length and has a fast hole response current. Thus, the detector speed of the n+ diffusion and p- substrate junction is dominated by electron diffusion. For a SML detector with a grid periodicity of  $5.6 \mu\text{m}$ , the detector speed is approximately equal to  $f_{3dB} \approx 8.5 \text{ GHz}$ .

### 2.3 LAYOUT

The layout of the photodetector, as shown in Figure 2.8(a), was completed in the  $0.35 \mu\text{m}$  Austria Micro System International (AMS) CMOS process [24]. Figure 2.8(b) depicts the finger pitch in a cross-sectional view. The area of the detector is  $3787.5 \mu\text{m}^2$ .



**Figure 2.8 (a) Layout of the photodetector; (b) Dimensions in an illustrative cross-section.**

## CHAPTER 3

### FRONT-END

#### 3.1 INTRODUCTION

The preamplifier is necessary to convert the photocurrent into a voltage. Further amplification is often achieved by a cascade of postamplifiers because the voltage produced by the preamplifier is normally inadequate for the clock and data recovery circuit. In this chapter, the operation and design of the transimpedance amplifier and post-amplifiers are discussed. The performance of the front-end circuit was evaluated by means of simulation.

#### 3.2 TRANSIMPEDANCE AMPLIFIER

The performance requirement of the preamplifier is influenced by the characteristics of the photodetector. For the SML detectors, the bit-error rate is determined by [4]

$$BER = \frac{1}{2} \operatorname{erfc} \frac{S}{\sqrt{ISI_v^2 + N^2}} = \frac{1}{2} \operatorname{erfc} \left( \left( \left( \frac{S}{ISI_v} \right)^{-2} + \left( \frac{S}{N} \right)^{-2} \right)^{\frac{1}{2}} \right), \quad (3.1)$$

where  $ISI_v$  is the statistical variation of the intersymbol interference,  $S$  is the signal power and  $N$  is the noise power. Assume that the TIA bandwidth is larger than 0.7 times the bit rate and that the ISI and the total integrated noise are well compromised. Then the ISI can be assumed to be negligible.

At the BER of  $10^{-12}$ , the computed required signal to noise ratio (SNR) is 6.97 dB. For a photodetector with a 0.038 A/W responsivity and a -17 dBm optical input power, the maximum allowable equivalent input noise current at the data rate is approximately 340 nA.

From Figure 1.1, the closed loop transimpedance gain can be approximated as

$$\frac{V_{out}(s)}{I_{PD}} = \frac{A_{OL}(s)}{1 + \frac{A_{OL}(s)}{R_F}}, \quad (3.2)$$

$$\approx \frac{A(s)R_F}{s^2 C_{in} R_F C_{out} R_{out} + s(C_{in} R_F + C_{out} R_{out}) + \frac{1 - A(s)^2 R_F}{A(s)R_F}}$$

where  $A_{OL}(s)$  is the open loop gain,  $A(s)$  is the amplifier gain (as shown in Figure 1.2),  $R_F$  is the feedback resistor,  $C_{in}$  is the total input capacitance, and  $C_{out}$  and  $R_{out}$  are the output capacitance and output resistance respectively. The total input capacitance is normally large compared to the output capacitance and with a large  $A(s)$  the dominant pole is assumed to be located at the input. From Equation 3.2, the upper 3-dB frequency,  $\omega_{-3dB}$ , of the transimpedance amplifier can be described as

$$\omega_{-3dB} = \frac{1 + A(s)}{C_{in} R_F}. \quad (3.3)$$

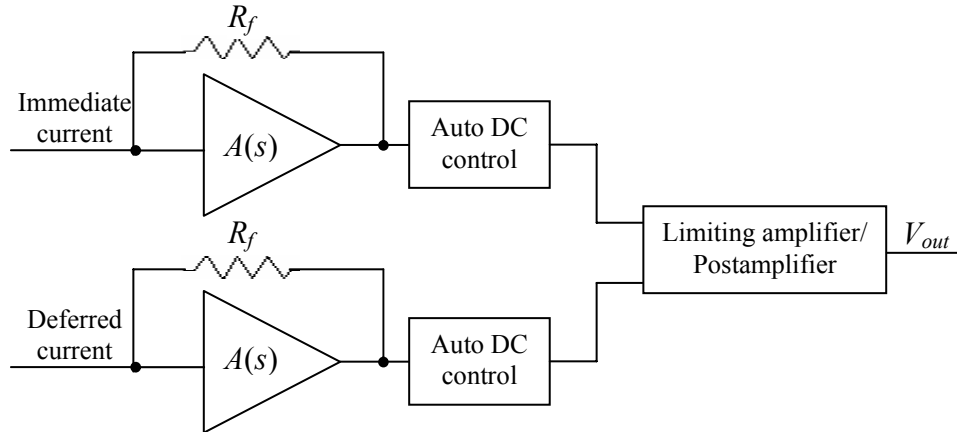
For the basic circuit of a transimpedance amplifier, as illustrated in Figure 1.1, the equivalent input-referred noise is approximated as [18]

$$\overline{i_{eq,in}^2} \approx \frac{16}{9} \frac{kT\omega^2 C_{in}^2 L^2}{\mu C_{gs} (V_{gs} - V_{TH})} + 4 \frac{kT}{R_F}, \quad (3.4)$$

where  $g_m$  represents the transconductance,  $C_{gs}$  is the gate-source capacitance,  $V_{gs}$  is the gate-source voltage and  $V_{TH}$  is the threshold voltage of the preamplifier's input transistor, and  $\mu$  is the mobility of the minority carriers. It is clear that at low frequencies, the thermal noise of the feedback resistor becomes dominant. Thus, it is desirable to minimise the noise by implementing a large feedback resistance, while compromising the closed loop bandwidth by increasing the open loop amplifier gain. Unfortunately, the amplifier gain  $A(s)$  is frequency dependent and the chosen circuit technology may constrain the bandwidth requirement of the system. Furthermore, the higher order poles are lowered when the open loop gain increases, thus decreasing the phase margin and limiting the stability requirement.

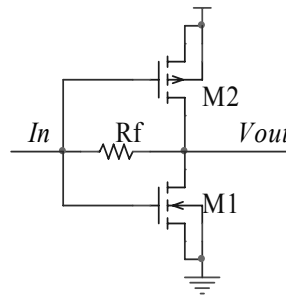
In order to obtain the effective information from the SML photodetector, the signal is extracted differentially to eliminate the diffusive carriers. It would be possible to implement a fully differential preamplifier. However, as discussed previously, none of the preamplifiers other than the CMOS inverter transimpedance amplifier [13] can achieve an acceptable noise performance. In the implementation, as illustrated in Figure 3.1, two identical transimpedance amplifiers were connected to the immediate and the deferred

outputs of the detectors. The subsequent differential postamplifiers were implemented to extract the difference response.



**Figure 3.1 Overview of the receiver front-end.**

Figure 3.2 shows the implementation of the topology of the transimpedance amplifier in transistor level. The configuration is based on the design in [13].



**Figure 3.2 Schematic diagram of the transimpedance amplifier.**

The open loop gain of the transimpedance amplifier is given by

$$A_{OL}(s) \approx R_F \frac{(g_{m1} + g_{m2})(g_{ds1} + g_{ds2})^{-1}}{(1 + sC_{in}R_f)(1 + sC_{out}R_{out})}, \quad (3.5)$$

where  $g_{ds1}$  and  $g_{ds2}$  are the conductance of  $M1$  and  $M2$ , and  $C_{in}$  and  $C_{out}$  are the input and output capacitances respectively.

Using Equation 3.2, the quality factor can be derived as

$$Q = \frac{\sqrt{A(s)C_{in}R_fC_{out}R_{out}}}{C_{in}R_f + C_{out}R_{out}}. \quad (3.6)$$

For high speed applications it is desirable to employ  $Q$  values larger than 0.5 to increase the bandwidth. However, when  $Q$  becomes too large the peaking effect becomes serious and leads to signal distortion. For practical applications,  $Q \leq 0.85$  is required to allow an

overshoot of less than 10%. In order to provide an adequate input voltage to bias the photodetector, the threshold voltage of the amplifier is set to

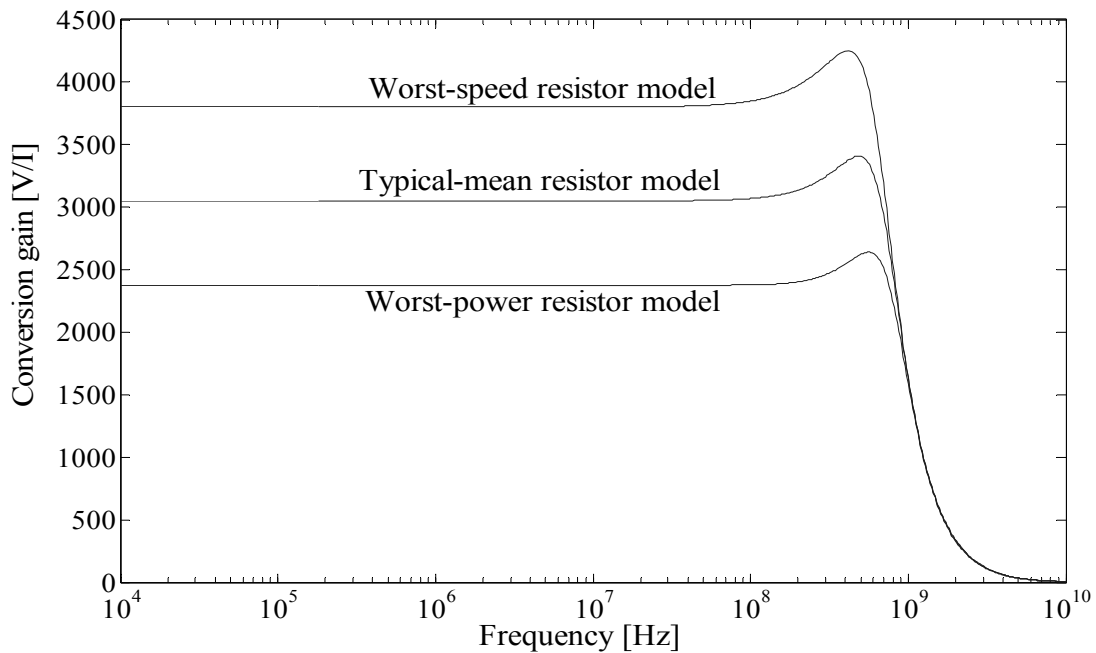
$$V_{ih} = V_{THn} + \sqrt{\frac{K_p (W/L)_2}{K_n (W/L)_1}} (V_{DD} + V_{THp}) \left( 1 + \sqrt{\frac{K_p (W/L)_2}{K_n (W/L)_1}} \right)^{-1} = 1.6, \quad (3.7)$$

where  $V_{THn}$  and  $V_{THp}$  are the threshold voltages of the NMOS and PMOS transistors respectively. With the threshold voltage defined, this leads to  $(W/L)_2/(W/L)_1 \approx 3$ . As described in Equation 3.4, the minimum transistor channel length is necessary to minimise the input-referred noise current. Large transistor widths were chosen to reduce the output resistances of  $M1$  and  $M2$ , thus, placing the frequency of the output pole a few degrees higher than that of the input pole. By letting  $Q = 0.8$  and assuming the output capacitance of approximately 100 fF, the calculated feedback resistance is 3 k $\Omega$ . A large value resistor can be realised with a small transistor, hence reducing the phase shift that would be introduced by a long integrated resistor. However, when the open loop gain of the amplifier is sufficiently large, the transimpedance gain is approximately equal to the feedback resistance, as can be shown from Equation 3.2. This implies that the frequency response is highly dependent on the quality of the feedback resistor. The threshold voltages of MOS resistors are greatly influenced by the model processes. For the chosen topology, depending on the type of MOS resistor, it is especially sensitive to the worst-zero (WZ) or the worst-one (WO) case and easily fails to meet the minimum bandwidth requirement with either of the two process corners. Different topologies could be implemented to solve the problem. However, none of the other literature studied can provide a satisfactory noise performance. Due to the influence of process variations, the feedback resistor has to be realised with available resistor implementations. The high resistive-poly was implemented as it has the lowest temperature coefficient and the highest sheet resistance of 1.2 k $\Omega/\square$  [27] contributing to a relative low parasitic capacitance. Unfortunately, a minimum of five squares is required for the layout of a high resistive-poly module, which translates to a minimum resistance of 6 k $\Omega$ , Therefore, the feedback resistor was realised by connecting two 6 k $\Omega$  high resistive-polys in parallel.

### Simulation

The small-signal equivalent circuit of the photodetector is modelled by a parallel combination of a current source and a capacitor. For an input photocurrent of 100 nA and

200 fF detector capacitance, the characteristic of the preamplifier in the frequency domain is illustrated in Figure 3.3.



**Figure 3.3 Frequency response of the transimpedance amplifier across different resistor models with worst-speed (WS) transistor model.**

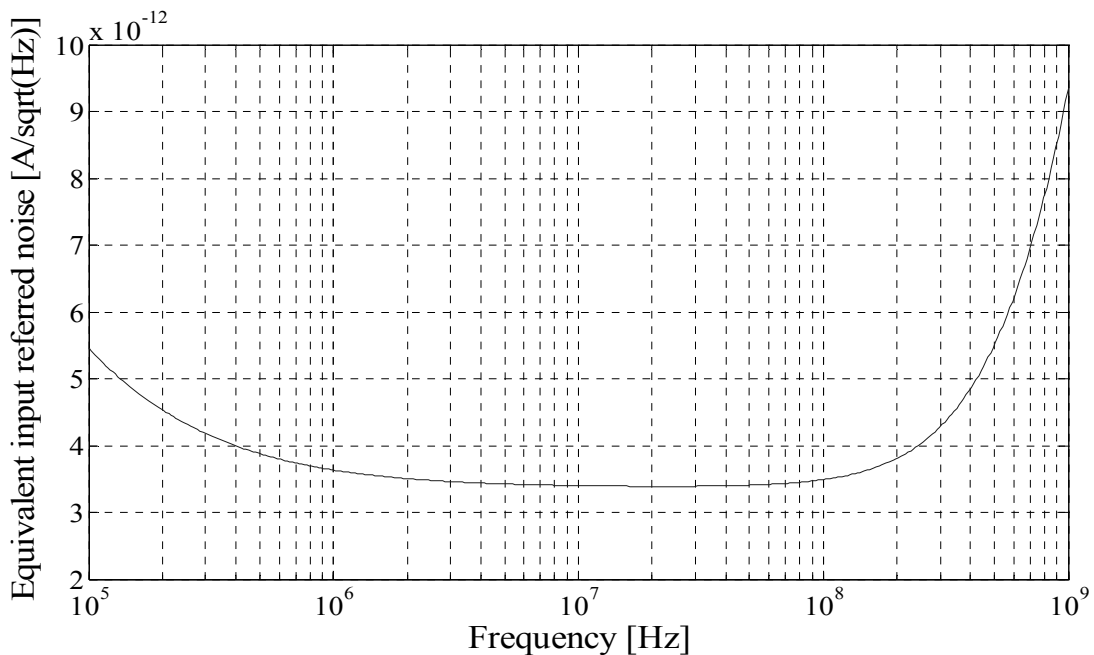
Table 3.1 shows the frequency response of the transimpedance amplifier for different process conditions. The typical-mean (TM), typical-mean MOS transistors and typical-mean high resistive-poly, bandwidth of the TIA is 910.5 MHz and the transimpedance gain is approximately 69.7 dBΩ. As can be seen, the TIA bandwidth is larger than 70% of the bit rate for all process conditions. In the process corner with the worst-speed MOS transistors and worst-speed high resistive-poly, the frequency response of the TIA is capable of achieving a bandwidth of 724.2 MHz.

**Table 3.1 TIA frequency response across different process conditions.**

Resistor model \ Transistor model	Typical-mean		Worst-speed		Worst-power	
	Bandwidth [MHz]	Conversion gain [dBΩ]	Bandwidth [MHz]	Conversion gain [dBΩ]	Bandwidth [MHz]	Conversion gain [dBΩ]
Typical-mean	910.5	69.7	811.3	69.7	907	69.5
Worst-speed	795.2	71.5	724.2	71.6	779.1	71.4
Worst-power	1048	67.5	913.4	67.5	1074	67.4

The analysis of the input referred noise of the preamplifier is performed and plotted in Figure 3.4. Assuming this noise is bandwidth limited and has a bandwidth from 100 kHz to

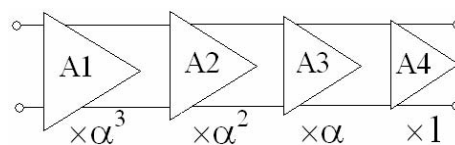
1 GHz, then the equivalent input referred noise current is approximately 182 nA. For the BER of  $10^{-12}$ , it requires a minimum optical input power of -19.7 dBm.



**Figure 3.4** Equivalent input referred noise current density of the preamplifier.

### 3.3 LIMITING AMPLIFIER [16]

Limiting amplifiers are implemented as part of the postamplifiers to boost the binary voltage swings produced by the TIA and to isolate the synchronous stages from the transimpedance amplifier. In order to achieve sufficient overall gain and meet the minimum bandwidth requirement for the gigabit applications, a multi-stage, low-gain pre-stage is necessary for the optimal design. Traditionally, a cascade of common-source differential pair gain stages is used to achieve the high-gain bandwidth product. Selecting large widths for all the transistors and large current tails, a reasonable bandwidth and noise figure can be achieved but at the cost of power consumption.



$\alpha$ : scaling factor.

**Figure 3.5** CMOS limiting amplifier block diagram.

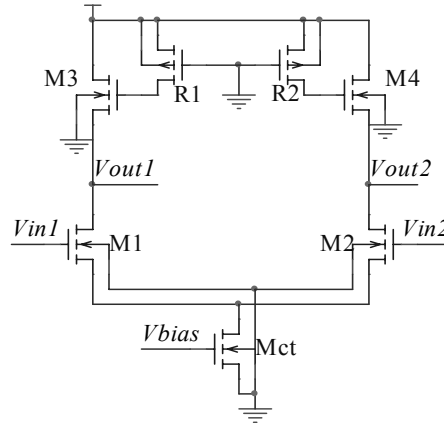
The modified LA employs the inverse scaling technique, as shown in Figure 3.5. A scaling factor  $\alpha$  is applied to the widths of all MOS transistors and current sources of the driven

gain stage such that the transistor sizes in the driving stage are  $\alpha$  times larger than those in the driven stage. Assuming that each gain stage has one dominant pole and it is strongly dependent on the total load capacitance of the stage  $C_{tot}$  (which consists of the stage output capacitance  $C_o$ , the wiring capacitance  $C_w$  and the input capacitance  $C_i$  of the next stage), applying a scaling factor to the driven stages, the bandwidth extension factor of the  $n^{\text{th}}$  gain stage can be defined as

$$\kappa = \frac{C_{o1} + C_{i1} + C_w}{\left(\frac{1}{\alpha}\right)^{n-1} (C_{o1} + C_{i1}) + C_w}. \quad (3.8)$$

As shown, a significant bandwidth extension is achieved for all stages. Hence, an obvious improvement in the overall bandwidth can be obtained.

The circuit topology of individual gain stages is illustrated in Figure 3.6. Each stage is a basic common-source differential. In order to alleviate the bandwidth degradation caused by the parasitic capacitances, active inductors were implemented for bandwidth enhancement. The active inductor consists of an NMOS transistor  $M3$  and a PMOS resistor  $R1$ . By changing the PMOS resistance, various inductance values can be obtained.



**Figure 3.6 Circuit topology of an individual gain stage.**

Assuming the products  $C_L \cdot C_{gs3}$  and  $C_{gs3} \cdot C_{\mu3}$  are negligible, then the impedance  $Z_L$  of the active inductor can be approximated by

$$Z_L \approx \frac{1 + sR(C_{gs3} + C_{\mu3})}{g_{m3} + s[g_{m3}RC_{\mu3} + (C_{gs3} + C_L)]}, \quad (3.9)$$

where  $C_{gs3}$ ,  $C_{\mu3}$  and  $C_L$  are the gate-source, gate-drain and load capacitances;  $g_{m3}$  is the transconductance of the transistor  $M3$ ; and  $R1$  is the PMOS resistance. If the condition

$$g_{m3} \gg g_{m3}RC_{\mu3} + (C_{gs3} + C_L) \quad (3.10)$$

is satisfied, then the inductive peaking is achieved.



The voltage gain of each cell can be expressed as

$$A = \frac{g_{m1}}{g_{m3}} \frac{1 + sR_1(C_{gs3} + C_{\mu3})}{1 + s[g_{m3}R_1C_{\mu3} + (C_{gs3} + C_L)]/g_{m3} + s^2R_1[C_L(C_{gs3} + C_{\mu3}) + C_{gs3}C_{\mu3}]/g_{m3}} \quad (3.11)$$

with poles and zero

$$\begin{aligned} p_1 &\approx \frac{g_{m3}}{g_{m3}R_1C_{\mu3} + (C_{gs3} + C_L)} \\ p_2 &\approx \frac{g_{m3}R_1C_{\mu3} + (C_{gs3} + C_L)}{R_1[C_L(C_{gs3} + C_{\mu3}) + C_{gs3}C_{\mu3}]} \\ z_p &= \frac{1}{R_1(C_{gs3} + C_{\mu3})} \end{aligned} \quad (3.12)$$

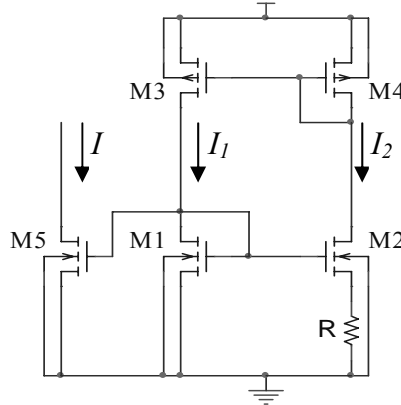
From Equation 3.12, the dominant pole can be approximated by  $p_1$ . Setting the zero equal to  $p_1$ ,  $p_2$  becomes the dominant pole and improves the bandwidth. The serious overshoot is prevented by selecting the  $Q$ -factor

$$Q = \frac{\sqrt{g_{m3}R_1[C_L(C_{gs3} + C_{\mu3}) + C_{gs3}C_{\mu3}]}}{C_L + C_{gs3} + g_{m3}R_1C_{\mu3}} = 0.707. \quad (3.13)$$

Due to the relatively low responsivity of the photodetector, the input photocurrent is in the range of only hundreds of nano-amperes. A moderate conversion gain is provided by the preamplifier to compensate between system sensitivity and bandwidth. In order to amplify the voltage swing to an amplitude of 400 mV peak-to-peak, a voltage gain of at least 56 dB (784) is required, while maintaining a sufficient bandwidth. The high-gain high-speed requirement forces the implementation of a long chain postamplifier. A ten-stage amplification is necessary and the effect of DC coupling resulting from cascading is remedied by DC-control circuits. The differential amplifier is designed with a voltage gain of 2. A scaling factor of 1.2 is applied to the limiting amplifier to prevent a serious capacitive loading of the first common-source differential stage to its preceding stage. DC-control circuits are also implemented immediately after the two single-ended TIAs to provide adequate DC input voltages to the limiting amplifier and to cancel the DC offset voltages from the TIAs. A moderately large width ( $W_{1,2} = 16.2 \mu\text{m}$ ) for the input transistors was chosen for the first-stage limiting amplifier in order to reduce a systematic offset voltage and to provide a moderate input capacitance. To achieve a voltage gain of 2, it leads to a width with a value of  $W_{3,4} = 4.3 \mu\text{m}$  for the load transistors  $M3$  and  $M4$ . The minimum channel length is used for transistors  $M1$ - $M4$  to achieve a high frequency response. A large tail current is required to ensure that the circuit meets the bandwidth

requirement. However, it also has to be kept moderate for transistors to operate in saturation. A tail current of  $I_{tail} \approx 1.4$  mA was chosen to meet the conditions. Using Equation 3.13, a PMOS resistance of  $R_I \approx 3$  k $\Omega$  is required to set  $Q = 0.707$ . This sets the ratio  $(W/L)_{R_I} \approx 2$ . The sizes of transistors for the following stages are scaled subsequently. The complete circuit diagrams can be found in Appendix C.

### 3.3.1 Current Reference Circuit



**Figure 3.7** Current reference circuit.

The bias currents of the LA circuit and the rest of the circuits discussed in the following chapters were implemented via current mirrors from current reference generators. Consider the reference circuit shown in Figure 3.7 [15]. PMOS transistors  $M3$  and  $M4$  form a negative feedback loop and force the currents

$$I_1 = I_2 = I, \quad (3.14)$$

when the PMOS transistors with identical dimensions are assumed. The gate voltages of the transistors  $M1$  and  $M2$  are equal. If all four transistors operate in the saturation region, applying Kirchoff's voltage law around the gate-source loop consisting of  $M1$ ,  $M2$  and  $R$  gives

$$\sqrt{\frac{2I}{k'_N (W/L)_1}} + V_{T1} = \sqrt{\frac{2I}{k'_N (W/L)_2}} + V_{T2} + IR. \quad (3.15)$$

Ignoring the body effect and all other secondary effects and letting  $(W/L)_2 = K(W/L)_1$ , Equation 3.15 gives

$$\sqrt{2k'_N (W/L)_1} I = g_{m1} = \frac{\sqrt{K}}{2(\sqrt{K} - 1)} \frac{1}{R}. \quad (3.16)$$

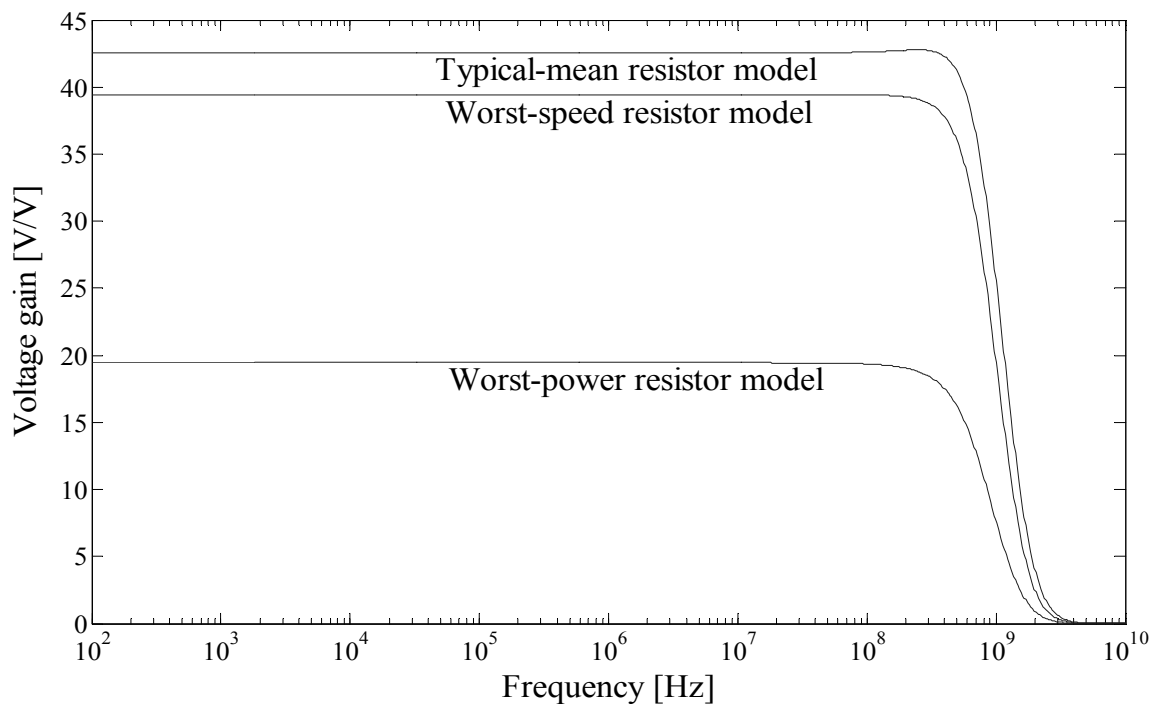
Hence, the reference current  $I$  can be represented as

$$I = \frac{2}{k'_N \left(\frac{W}{L}\right)} \frac{1}{R^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2. \quad (3.17)$$

As shown, the current is independent of the supply voltage. If minimum length transistors were implemented, the channel-length modulation effect becomes prominent and the circuit behaviour is undesirable. In order to minimise the mismatch of the current in all branches and the influence of the short-channel effect, relatively large transistors of  $W/L = 6.85 \mu\text{m}/1.5 \mu\text{m}$  were chosen for a reference current of  $100 \mu\text{A}$ . The  $W/L$  ratio between  $M1$  and  $M2$  was chosen to be 2 so as to reduce the size of  $M2$  and to limit the size of the resistor. From Equation 3.17 the resistance was calculated to be in the region of  $1.46 \text{ k}\Omega$ . The resistor was realised with a poly resistor. As with all the other resistor types it is least process dependent and does not vary with voltages.

### Simulation

The frequency response of the six-stage limiting amplifier is shown in Figure 3.8 and Table 3.2. The analysis was performed with an input voltage of  $1 \text{ mV}$ . The voltage gain of the limiting amplifier is basically determined by the operation of NMOS transistors and the bandwidth enhancement depends on the quality of the PMOS resistors in conjunction with the transconductance of the input transistors of the differential amplifiers.



**Figure 3.8 Frequency response of the limiting amplifier across different resistor models with worst-speed transistor model.**

**Table 3.2 LA frequency response across different process conditions.**

Resistor model Transistor model	Typical-mean		Worst-speed		Worst-power	
	Bandwidth [MHz]	Voltage gain [dB]	Bandwidth [MHz]	Voltage gain [dB]	Bandwidth [MHz]	Voltage gain [dB]
Typical-mean	1133	34.6	961.4	33.4	1258	35.7
Worst-speed	875.9	32.6	766.2	31.9	645.9	27
Worst-power	1506.8	35.7	1280.9	34.3	1702.4	37.8
Worst-zero	770.1	33	656.1	32.1	679.2	30
Worst-one	1450	35.9	1297.8	34.5	1584.4	38

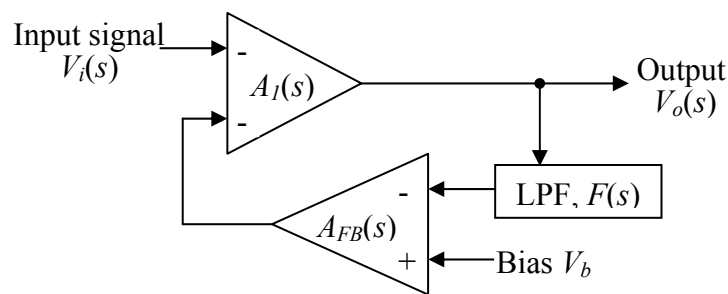
In the worst-zero condition, NMOS transistors are relatively weak and the absolute threshold voltage of PMOS resistors becomes as small as 0.487 V. As a result, the NMOS-determined transconductance becomes smaller than that in the typical-mean environment, and a larger PMOS resistance is produced. In the worst-zero condition, the system, however, barely meets the condition for inductive peaking, as described in Equation 3.10, and results in a moderate bandwidth of between 770 and 656 MHz for all resistor models. When the NMOS transistors are weak, the deviation of resistor models from the typical-mean resistor condition causes degradation in both the bandwidth and voltage gain. The worst scenario occurs in the worst-speed transistor models and worst-power resistor model. The resultant bandwidth and voltage gain are 645.9 MHz and 27 dB respectively. However, this is considered to be acceptable. The voltage gain and bandwidth in the typical-mean simulation are approximately equal to 34.6 dB and 1.13 GHz, respectively.

### 3.4 AUTO-DC-CONTROL CIRCUITS AND POSTAMPLIFIER [18]

The DC-control circuits and postamplifier are based on the design in [18]. They serve the functions as to set the common-mode input voltages for their succeeding circuits and to provide a further amplification. The design consists of a string of modified inverters biased at their threshold voltage. Through the implementation of offset tolerant replica biasing circuits, the bias voltage of the inverters is accomplished and forced to the threshold voltage of its replica. Upon receiving a small input signal, the inverters behave as linear amplifiers and clipping occurs at the end of the chain. With a larger input signal, the first clipping at the rail-to-rail voltage is simply shifted forward and results in a large dynamic range.

### 3.4.1 Replica biasing control

The correct threshold voltage setting of the inverter string is critical. The non-optimal biasing of inverters will result in a degradation of the duty cycle of the signal and can be remedied by implementing a replica biasing scheme. The replica uses the negative feedback to force the DC output voltage of the inverter chain  $V_o(s)$  equal to the bias voltage  $V_b$  by level-shifting the signal. Passing the output voltage signal to a low-pass filter, the average signal can be measured. Once the mean signal is obtained, it is presented to the input of the comparator and is compared with the replica's threshold voltage. The output of the comparator is then sent to a level shifter that adjusts the threshold of the inverter and forces the DC output to  $V_b$ .



**Figure 3.9 Mathematical model of the replica biasing control.**

Figure 3.9 illustrates the principle of replica biasing. The mechanism of the principle can be derived as

$$V_o(s) = \frac{V_b A_{FB}(s) A_I(s) F(s)}{A_{FB}(s) A_I(s) F(s) - 1} + \frac{V_i(s) A_I(s)}{A_{FB}(s) A_I(s) F(s) - 1}, \quad (3.18)$$

where  $F(s)$  is the transfer function of the low-pass filter (LPF). At the frequency below the -3-dB bandwidth of the low-pass filter,  $F(s) \rightarrow 1$ , assume  $A_{FB}(s) A_I(s) \gg 1$  and  $A_{FB}(s) \gg 1$ , then the DC bias of  $V_o(s)$  is

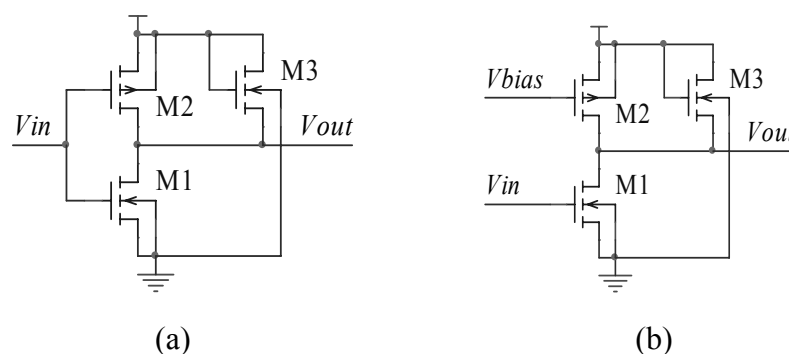
$$V_o(s) \approx V_b. \quad (3.19)$$

Due to parameter variations in the circuit, there is a slight deviation from the desired bias voltage. This standard deviation is inversely proportionate to the square of the voltage gain  $A_I$ . Thus, by enlarging  $A_I$ , the effect of mismatch can be reduced.

### 3.4.2 Realisation of the Postamplifier

Applying an input photocurrent of 100 nA to the preamplifier and having a single-ended differential amplifier cascaded to the ten-stage limiting amplifier, an output voltage of 566 mV is achieved. A gain of at least 2.9 is required to amplify this voltage to a 3.3 V rail-to-

rail voltage. As a small amplification is required, one replica-biased inverter string was implemented in the front-end. The feedback loop of the replica biasing consists of three modified inverters for the postamplifier or one modified inverter for the DC control circuit, a comparator and a level shifter that also performs an extra inversion. For the postamplifier implementation, due to the high speed requirement in the signal path, multiple inverter stages are necessary as the gain of each stage is limited. The voltage gain of the DC control circuit, typically a gain of unity, does not have to be high as it only has to set the biasing point for its succeeding circuits. The biasing circuit would try to compensate for any DC shifts present in the signal output. In order to avoid a degraded biasing resulting from the DC deviation due to frequency components larger than the -3-dB frequency of the inverters, bandwidths of the inverters in the signal path must be sufficiently larger than the signal's bandwidth. However, the bandwidth of the standard Class B amplifier is limited by its high gain characteristic. Modification of the inverter is done by connecting a diode-coupled transistor to the output, as shown in Figure 3.10(a), to limit the gain and achieve high bandwidth. By replacing the diode-coupled transistors with active inductors, a further bandwidth extension is achieved. In the configuration, the NMOS transistor is preferred over a PMOS as it is smaller for a given  $g_m$  and the non-zero bulk-source voltage further enhances the transconductance. As a result, this topology has a minimal increased capacitive loading. The shifter has the same topology (refer to Figure 3.10 (b)) as it is also in the signal path and has to provide a comparable bandwidth. Thus, it serves as a level shifter and as an inverting amplifier with a limited gain. The NMOS in the shifter acts as the input for the signal and the PMOS performs the level shifting.



**Figure 3.10 Circuit topology of (a) the high-speed inverter; and (b) the level shifter (adapted from [18]).**

Based on the topology, similar equations are derived to describe both the inverter and the shifter. For simplicity, assume that the MOS resistor value of the active inductor is small. Then the output voltage of the inverter is

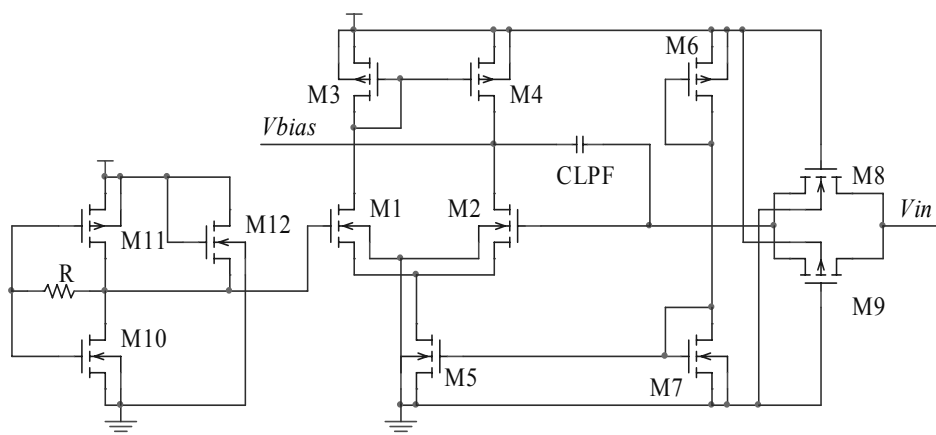
$$V_o = -V_{in} \left( \frac{g_{m1}}{g_{m3}} + \frac{g_{m2}}{g_{m3}} \right), \quad (3.20)$$

and the output voltage of the level shifter is

$$V_o = -V_{in} \frac{g_{m1}}{g_{m3}} - V_{bias} \frac{g_{m2}}{g_{m3}}. \quad (3.21)$$

As will be shown later, the voltage gain determined by transistors  $M2$  and  $M3$  becomes overly effective in the worst-zero transistor models. In order to reduce the effect, a small ratio  $(W/L)_2/(W/L)_3$  has to be implemented. However, the ratio  $(I_{D1}(W/L)_1)/(I_{D3}(W/L)_3)$  has to be large enough to achieve an adequate voltage gain while providing an adequate inverter threshold voltage. Compromising all the factors, the transistor sizes are set with a ratio  $(W/L)_2/(W/L)_1 = 2$  and relatively large widths ( $W_1 = 4 \mu\text{m}$ ,  $W_2 = 8 \mu\text{m}$ ) are used to provide fast rise and fall time. Setting the drain current of transistor  $M3$  to  $I_{D3} \approx 0.4 I_{D1}$ , the width of  $M3$  is calculated to be  $4.45 \mu\text{m}$ . This results in a voltage gain of approximately 2 with a 1.85 GHz bandwidth.

The major components of the replica feedback loop are the  $RC$  low-pass filter and the comparator (Figure 3.11). The output DC voltage of the replica biased circuit is measured by the loop filter. It is compared to the replica's threshold and adjusted through the loop. The -3-dB frequency of the loop filter has to be sufficiently low to ensure stability as the gain of the cascaded inverters is high at the mid-band frequency. Unfortunately, the lower the corner frequency the longer the settling time is.



**Figure 3.11 Replica feedback loop.**

For a low-corner frequency, the resistor and capacitor values are rather large. In order to minimise the implementation area and prevent excess phase shift resulting from the implementation of large resistors and capacitors, the resistor was replaced by a PMOS

transistor in its triode region and a large capacitor was realised by utilising the Miller effect with the comparator as gain element. Nonetheless, the postamplifier was implemented at the last stage of the front-end where the input was large. As the input voltage becomes large, the PMOS transistor enters the saturation region and results in an increased resistance value. With the large input signal, the behaviour of the MOS transistors becomes undesirable. In order to solve the problem of the final postamplifier stage, an additional NMOS transistor was placed in parallel with the PMOS transistor. However, the cost of an additional transistor is the increased parasitic capacitance and the degraded amplifier frequency response.

The Miller capacitance can be expressed as

$$C_{Miller} = C_{LPF}(1 + A_V), \quad (3.22)$$

where  $A_V$  is the comparator gain. The comparator is realised with a simple operational transconductance amplifier (OTA). The specifications of the OTA are not too stringent. The gain

$$A_V = g_{m2}(r_{o2} // r_{o4}), \quad (3.23)$$

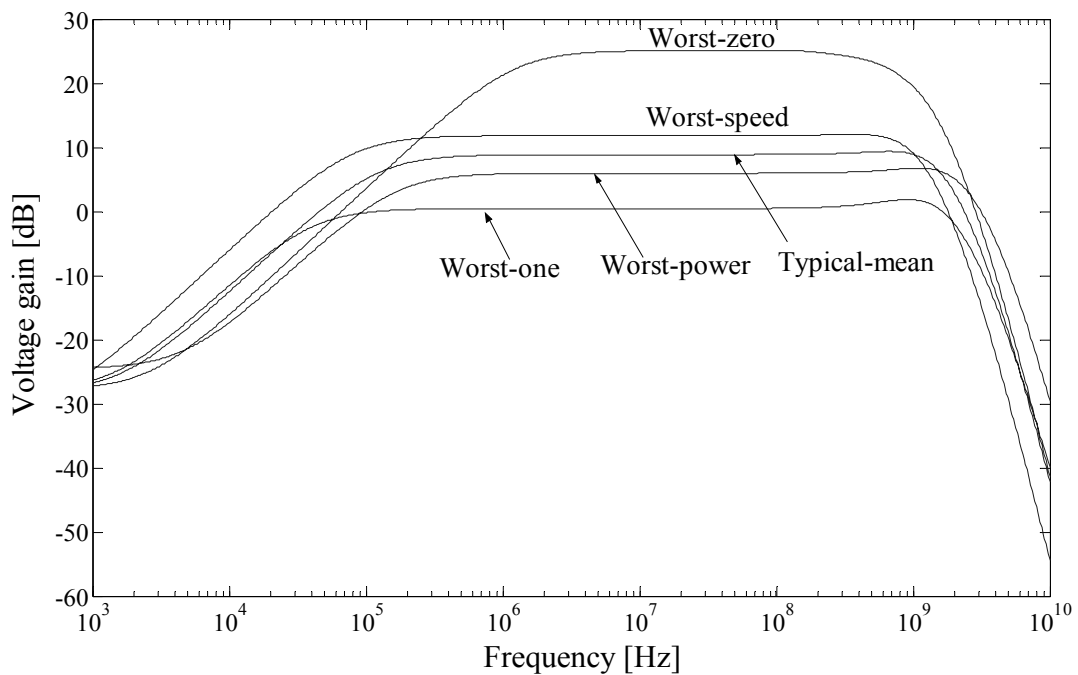
however, should not be too low, about 36.9 dB. The channel lengths and widths of the input transistors are made large ( $W_{1,2} = 100 \mu\text{m}$ ,  $L_{1,2} = 1.5 \mu\text{m}$ ) to avoid systematic offset and to reduce the effect of process variations. A constant transconductance is biased with a tail current of 4 mA. With  $M2_{level-shifter}$  of the level shifter (Figure 3.10(b)) connected to the output of the OTA, it defines the gate-source voltage of  $M2_{level-shifter}$ ,  $V_{SG2,level-shifter} = V_{DS4,OTA}$ . With perfect matching and zero input voltages, it requires

$$\frac{I_{D3,OTA}}{(W/L)_{3,OTA}} = \frac{I_{D4,OTA}}{(W/L)_{4,OTA}} = \frac{I_{D2,level-shifter}}{(W/L)_{2,level-shifter}}. \quad (3.24)$$

This sets the size of  $M3_{OTA}$  and  $M4_{OTA}$  to  $(W_{3,4})_{OTA} = 34 \mu\text{m}$  and  $(L_{3,4})_{OTA} = 0.6 \mu\text{m}$ .

As the parasitic capacitances of the transmission gate,  $M8-M9$ , further increase the output capacitive loading to the postamplifier, it is necessary to keep the sizes of the transistors of the transmission gate small, which leads to the implementation of minimum width transistors,  $M8-M9$ . For a low-pass resistance of approximately 50 k $\Omega$ , it sets the channel lengths for transistors  $M8-M9$  to  $L_8 = 7.4 \mu\text{m}$  and  $L_9 = 2.5 \mu\text{m}$ . To obtain a low-corner frequency of about 15 kHz, it requires a 20 pF low-pass capacitor  $C_{LPF}$  to be placed in the Miller configuration. The output voltage of the OTA sets the biasing point of the shifter.



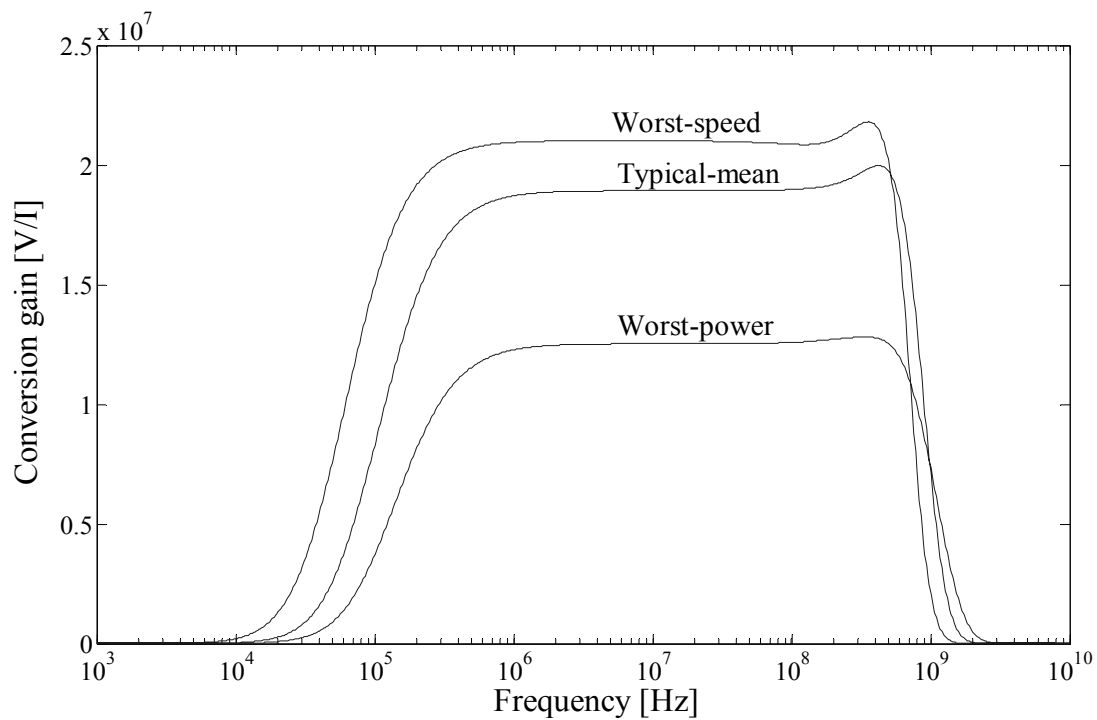


**Figure 3.12 Postamplifier frequency response across different transistor process conditions with typical-mean resistor model.**

The characteristics of the postamplifier are illustrated in Figure 3.12 and the frequency response across all process conditions is given in Table 3.3. Figure 3.12 depicts the frequency responses of the circuit to a 1 mV input voltage across all the transistor models. It can be seen that the circuit is relatively sensitive to the process conditions. The hole mobility of PMOS transistors is intrinsically smaller than the electron mobility of NMOS transistors, and thus large PMOS transistors are required to provide a reasonable gain of  $g_{mp}/g_{mn}$ . In the worst-zero simulation, PMOSs become very strong and NMOSs are relatively weak, consequently producing an extremely large gain. In order to prevent severe bandwidth degradation, the number of replica biased stages is limited. The worst case speed bandwidth of the postamplifier is approximately equal to 1 GHz. For the nominal transistor models, the voltage gain is about 8.9 dB and the bandwidth is 1.5 GHz.

**Table 3.3 Postamplifier frequency response across different process conditions.**

Resistor model Transistor model	Typical-mean		Worst-speed		Worst-power	
	Bandwidth [MHz]	Voltage gain [dB]	Bandwidth [MHz]	Voltage gain [dB]	Bandwidth [MHz]	Voltage gain [dB]
Typical-mean	1529	8.9	1529.1	8.9	1529.1	8.9
Worst-speed	1007.5	11.8	1007.5	11.8	1007.5	11.8
Worst-power	2347.7	6	2347.2	6	2347.2	6
Worst-zero	688.1	25.1	688.2	25	688	25.1
Worst-one	1859.3	0.45	1859.3	0.45	1859.3	0.45



**Figure 3.13 Front-end frequency responses for different transistor models with typical-mean resistor model.**

The characteristics of the front-end system can be seen in Figure 3.13 and Table 3.4. Under the worst-speed, worst-power and the typical-mean transistor and resistor model simulations, the characteristics of the front-end system are within the specifications.

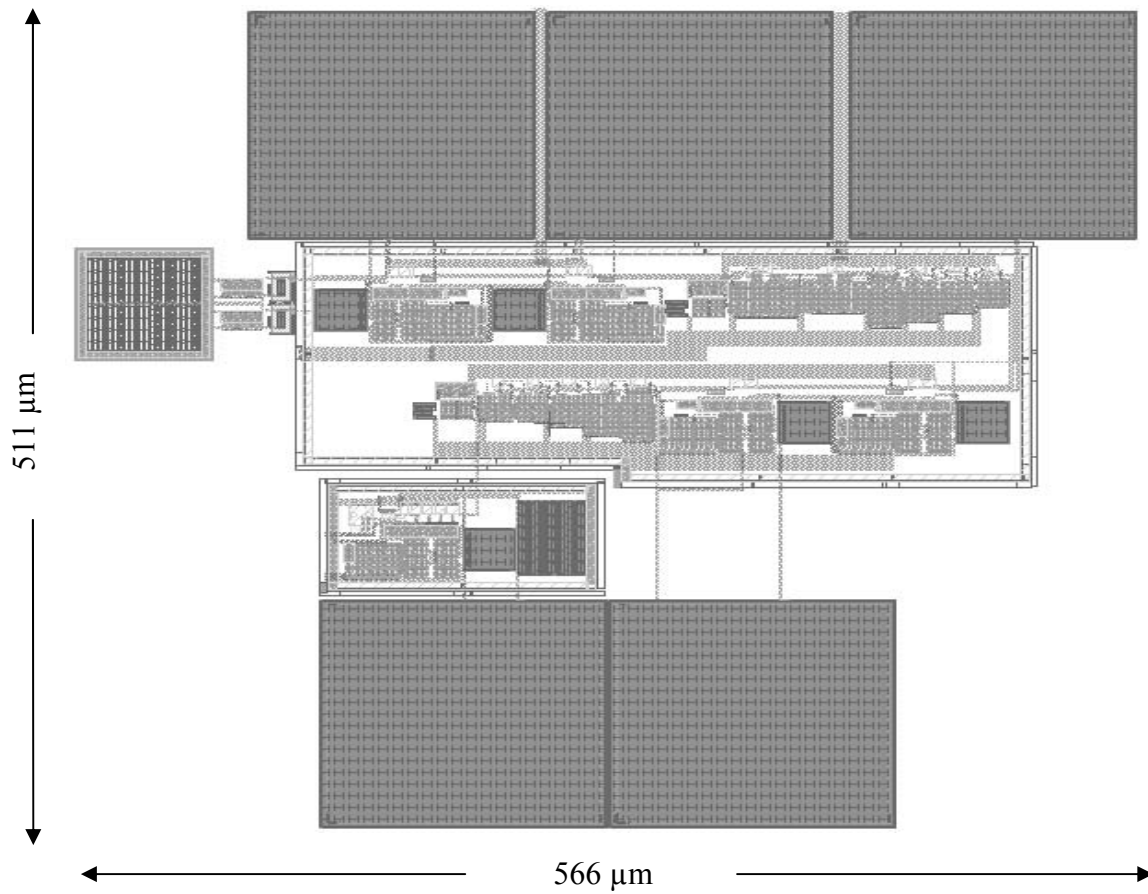
**Table 3.4 Front-end frequency response across different process conditions.**

Transistor model Resistor model	Typical-mean		Worst-speed		Worst-power	
	Bandwidth [MHz]	Conversion gain [dBΩ]	Bandwidth [MHz]	Conversion gain [dBΩ]	Bandwidth [MHz]	Conversion gain [dBΩ]
Typical-mean	769.2	145.5	621.7	146.5	866.6	141.9
Worst-speed	660.3	145.9	569.2	147.9	706.2	140.9
Worst-power	876.5	145	558.6	135.5	1039	143.8

### 3.5 LAYOUT

The layout of the front-end circuit was completed and is shown in Figure 3.14. The common-centroid method was used wherever matching between transistors was required to cancel the effect of first-order process-related gradients across the die along both vertical and horizontal axes. It was implemented by decomposing the input devices into two halves which were cross-connected [15]. Wide devices were decomposed into multifinger transistors to reduce the gate resistance. For current mirrors, unit transistors were used

wherever possible to obtain better current matching and non-minimum lengths were implemented to further suppress mismatches.



**Figure 3.14** Layout of the front-end.

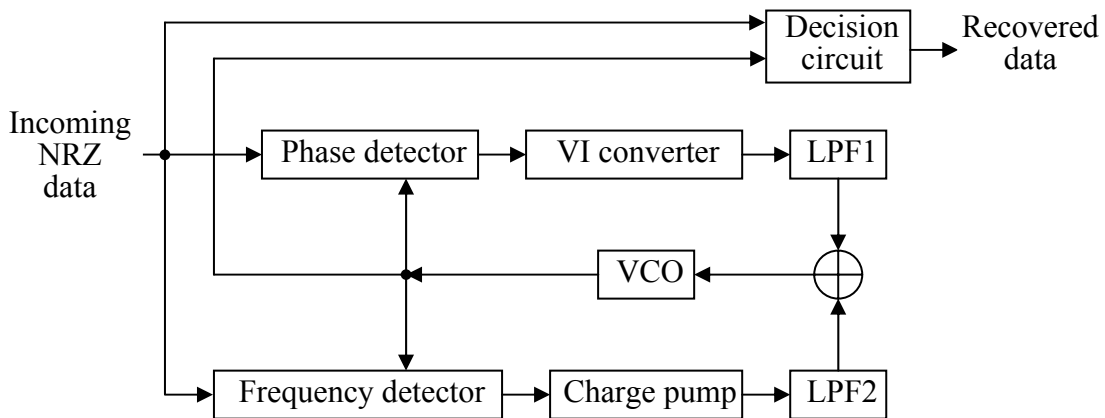
## CHAPTER 4

### CLOCK AND DATA RECOVERY CIRCUIT

#### 4.1 INTRODUCTION

The clock and data recovery circuit forms the core of the receiver. It consists of a phase-locked loop and a frequency-locked loop. In order to recover the original data sequence and reduce the intersymbol interference, it is necessary to retiming and synchronise the input signal with an extracted clock signal. In the CDR circuit, a clock signal is generated so that sampling of the input data occurs at the optimum point. The frequency-locked loop performs the coarse adjustment of the clock frequency and provides a large range for frequency acquisition. The phase-locked loop provides a fine control for the clock signal. In this chapter, the implementations and results of the CDR system are given.

#### 4.2 CLOCK AND DATA RECOVERY PRINCIPLE



**Figure 4.1 Dual-loop clock and data recovery circuit.**

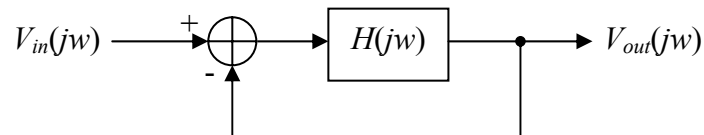
The phase-locking clock and data recovery circuit with a frequency acquisition scheme is shown in Figure 4.1. During the CDR operation, the location of the data transition is compared to the clock edge. If the data signal leads the clock, the clock speeds up. The clock frequency is decreased if the data signal lags the clock. When the data zero crossings coincide with the clock edge, the clock is kept constant, ensuring phase lock. Phase drift can cause a false data extraction. Stable operation must therefore be maintained for random input signal including consecutive input data bits.

In the recovery circuit, a clock signal is generated by the voltage-controlled oscillator. The VCO's frequency information is compared to that of the incoming data. The difference in frequencies is utilised by the FLL to coarsely adjust the voltage-controlled oscillator frequency until the difference is sufficiently small and the FLL becomes inactive. The phase and the frequency of the VCO clock signal are then compared to that of the data in the phase detector. An error signal is generated and used to set the voltage required by the VCO to oscillate at the frequency of interest. When the data phase and the clock phase differ by a small constant offset, the phase-locked loop remains locked. Once the clock signal is recovered, it is used to retime the data in the decision circuit.

#### 4.2.1 Phase-Locked Loop

##### 4.2.1.1 Voltage Controlled Oscillator [20]

The VCO design [21] impacts directly on the jitter performance and reproducibility of the CDR. LC oscillators have potentially lower jitter. However, it is difficult to obtain a target frequency due to their limited tuning range and the fact that they are not practical in the 100 MHz to 1 GHz frequency range [29, 30]. Thus, a ring oscillator, due to its speed and ease of integration, was implemented to compensate for process and temperature variations.



**Figure 4.2 Negative feedback system.**

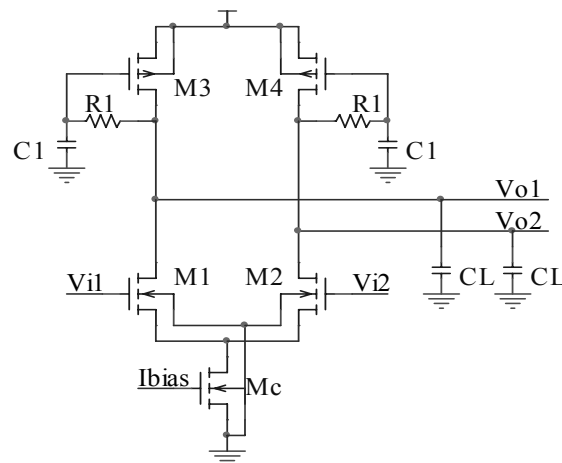
The oscillator can be modelled linearly as illustrated in Figure 4.2 [31]. This can be expressed as

$$\frac{V_{out}(jw)}{V_{in}(jw)} = \frac{H(jw)}{1 + H(jw)}, \quad (4.1)$$

where  $H(jw)$  is the transfer function of the gain stages of the oscillator. At the frequency  $\omega_0$  of interest, the amplifier experiences sufficient phase shift to cause the feedback to become positive and for an oscillation to occur. Thus, for the oscillation to occur, the negative feedback system must satisfy the two Barkhausen criteria simultaneously [15], which can be defined as

$$\begin{aligned} H(jw) &\geq 1 \\ \angle H(jw) &= 180^\circ \end{aligned} \quad (4.2)$$

The CDR circuit was incorporated with a frequency-locked loop. The oscillator was designed to generate quadrature outputs as a provision for the frequency detector. A ring oscillator is formed by  $N$  delay stages. Each gain stage must contribute a phase shift of  $180^\circ/N$ . For a differential ring oscillator, an even number of stages must be implemented to produce outputs with the quadrature phase. The phase inversion is achieved by inverting two feedback connections. The differential implementation results in an area overhead and power penalty. It is, however, necessary to be traded off to achieve high-speed operation with low sensitivity and low jitter generation. In the oscillator, as the number of delay stages increases, it becomes difficult to achieve the required speed with a given CMOS technology and it has a high power consumption. However, a single stage ring does not produce sufficient phases and oscillation cannot occur. Thus, at least a two-stage topology is necessary for quadrature outputs. In a two-stage ring oscillator, each stage must establish a phase shift of  $90^\circ$  within its unity-gain bandwidth. With conventional differential delay stages, the overall phase shift around the loop can achieve  $180^\circ$  only at infinite frequency [20]. The loop gain drops to zero at very high frequencies. The oscillator, thus, fails to oscillate. By introducing an additional phase in each stage, a greater phase shift can be achieved around the loop.



**Figure 4.3 Differential delay cell.**

The single stage differential delay cell is shown in Figure 4.3 is the. Each load consists of a resistor, a PMOS transistor and a capacitor. The parasitic capacitance determined by the drain junction capacitance of the MOS devices, the input capacitance of the next stage and the input capacitances of the isolation buffers, results in the load capacitance of the differential stage. Choosing proper parameters and transistor sizes, the composite load becomes inductive and produces excess phase shift to allow oscillation.

The transfer function of each delay stage is derived as [20]

$$\frac{V_o(s)}{V_{in}(s)} = - \frac{g_{m1}(1 + sR_1C_1)}{g_{m3} + s(C_1 + C_L + R_1C_1/r_{o3}) + s^2R_1C_1C_L}. \quad (4.3)$$

The transfer function exhibits a zero at

$$\omega_z = - \frac{1}{R_1C_1}, \quad (4.4)$$

and has two poles with a sum of

$$\omega_{p1} + \omega_{p2} = \frac{C_1 + C_L}{R_1C_1C_L}. \quad (4.5)$$

At every pole frequency there is a  $-45^\circ$  phase shift and at every zero frequency a  $+45^\circ$  phase shift occurs. Thus, in order to provide a sufficient phase shift of  $-90^\circ$  within the unity-gain bandwidth, the sum of the two pole frequencies must be less than the frequency of zero. Then, from Equations 4.4 and 4.5, it is required that [20]

$$C_1 < C_L \approx 265 \text{ fF}. \quad (4.6)$$

For an  $N$ -stage ring oscillator, the frequency of oscillation is inversely proportional to the number of stages  $N$  and the delay per stage  $T_d$ . The frequency of oscillation can be defined as [22]

$$f_{osc} = \frac{1}{2NT_d}. \quad (4.7)$$

Consider an oscillator to be a system that converts the current and voltage to a phase that can be directly related to the delay. Applying a step current to an oscillator, time delay can be defined as the time it takes to respond from when the oscillator output voltage is at its mid point to when it is at its maximum amplitude [36]. Thus,  $T_d$  can be expressed as [26]

$$T_d \approx \frac{2V_{out}}{SR}, \quad (4.8)$$

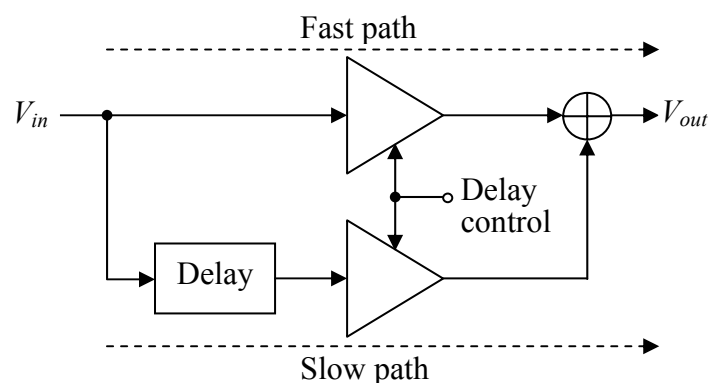
where  $V_{out}$  is the single-ended oscillator output peak voltage and  $SR = I/C_L$  is the slew-rate of the differential pair with  $I$  being the maximum current that charges the load capacitor  $C_L$ . Using Equations 4.7 and 4.8, an oscillation frequency of approximately 1.5 GHz can be achieved with an 800 uA tail current and a 500 mV peak-to-peak voltage.

As shown in Equation 4.7, the frequency of oscillation can be varied either by altering the effective number of stages or the delay of each stage. However, altering the effective number of stages may require a difficult logic, while the delay can be easily adjusted through the tail current.

In order to avoid the unnecessary logic, while compensating for the process and temperature variations, the VCO incorporates delay interpolation, providing a wide tuning range. To ensure oscillation and high speed operation, a gain of approximately 2.5 was implemented in the design. A relatively large bias current was implemented to keep the output voltage swing constant and to minimise the output jitter of the oscillator.

### Delay Interpolation

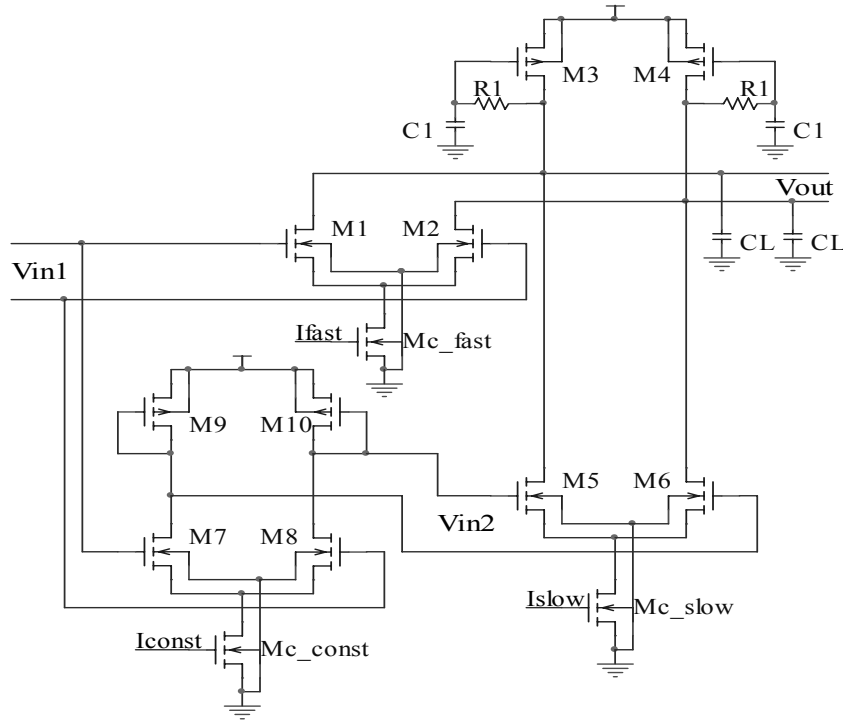
The conceptual illustration of delay interpolation is depicted in Figure 4.4. Each oscillator stage consists of a fast path and a slow path with shared output nodes. The voltage gains of the two paths are adjusted through the differential delay control voltage. By differentially varying the delay control voltage, the current steered between the fast and slow paths can be adjusted and hence the voltage gains of the two paths adjusted. Since the large-signal slew rate that is related to the current drive and capacitance results in the delay of each stage, therefore, adjusting the gains leads to delay variations and thus influences the oscillation frequency.



**Figure 4.4 Delay interpolation.**

The transistor implementation of each delay stage is shown in Figure 4.5. Each stage is realised with differential amplifiers, as described in Figure 4.3, where outputs are summed in the current domain. As shown in the circuit, the slow path consists of the differential pairs  $M5-M6$  and  $M7-M8$ . The differential pair  $M1-M2$  describes the fast path. The outputs of the two paths are summed in the current domain.





**Figure 4.5 Transistor implementation of the delay interpolation.**

For the small signal equivalent circuit, the summed current is [15]

$$I_{out} = g_{m1,2}V_{in1} + g_{m5,6}V_{in2}. \quad (4.9)$$

By varying the tail currents  $I_D$  of  $M1-M2$  and  $M5-M6$  in opposite directions, the transconductance of the respective stage

$$g_m = \sqrt{2K_n' \left( \frac{W}{L} \right) I_D}, \quad (4.10)$$

and thus the weighted sum of the delays of the slow path and the fast path is altered.

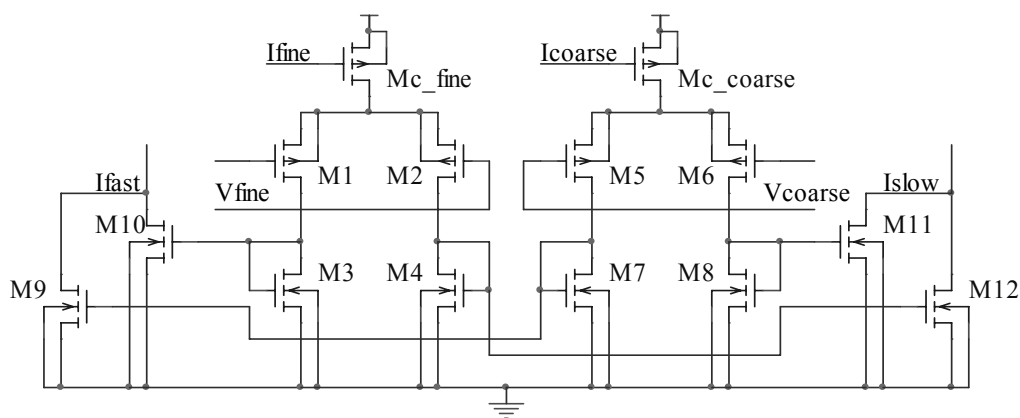
Assume that an impulse current consisting of  $\Delta q$  coulombs is applied to one of the outputs of the two-stage ring oscillator. It causes an instantaneous change in the voltage and results in a shift in the transition time [34]. This instantaneous change in the voltage can be expressed as

$$\Delta V = \frac{\Delta q}{C_o}, \quad (4.11)$$

where  $C_o$  is the effective capacitance at that output. Timing jitter can therefore be improved by introducing a larger capacitance at the outputs of each VCO stage. This can be done by implementing wide transistors to suppress timing jitter and to provide the adequate driving capability that is required to drive a large number of latches in the CDR circuit. Consequently, large currents and minimum gate length (0.35  $\mu\text{m}$ ) implementation

are necessary to achieve high speed performance. Assume that the delay control voltage of Figure 4.4 lies midway between the two extremes so that both the slow and fast paths are on. A tail current  $I_{D,Mc\_const} = 250 \mu\text{A}$  was chosen for the constant current  $M7$ - $M8$  differential stage. For the  $M1$ - $M2$  and  $M5$ - $M6$  differential stages, the tail currents are set at  $I_{D,Mc\_fast} \approx 2I_{D,Mc\_slow} = 560 \mu\text{A}$ , providing a two-to-one tuning range. The overdrive voltages ( $V_{GS} - V_{TH}$ ) for the input transistors ( $M1$ - $M2$ ,  $M5$ - $M6$  and  $M7$ - $M8$ ) are set low (at approximately 0.25 V) to ensure the operation of transistors in saturation. This translates to transistor widths of  $W_{1,2} = 12 \mu\text{m}$ ,  $W_{5,6} = 6 \mu\text{m}$  and  $W_{7,8} = 8 \mu\text{m}$ . A voltage gain of approximately 1.25 is set for the fast path. This requires a voltage gain of 2 from the differential stage  $M7$ - $M8$  to achieve a total gain of 2.5 per delay stage. As a result the load transistor widths are set to  $W_{3,4} = 12 \mu\text{m}$ , and  $W_{9,10} = 6 \mu\text{m}$ .

Stacking differential pairs under the delay stages makes it difficult in a low supply environment. In order to avoid voltage headroom consumption, current folding topology (as shown in Figure 4.6) was implemented to steer the currents of  $M1$ - $M2$  and  $M5$ - $M6$ . Two PMOS differential pairs were used to drive the current mirrors. Inputs to the differential pairs are controlled by a fine control and a coarse control. The two controls set the current flows into their relative current mirrors, which are fed into the delay cells, thus adjusting the oscillation frequency. The fine tuning sensitivity of the oscillator is minimised by minimising the transconductances of the fine control input transistors of the current folding circuit. This is achieved by setting a small tail current,  $I_{D,Mc\_fine}$ , with a small  $(W/L)_{1,2}$  ratio. Large transconductances for transistors  $M5$  and  $M6$  were implemented to obtain a high sensitivity and thus a wide coarse tuning range. The dimensions of current mirror transistors are chosen large with  $L = 2 \mu\text{m}$  to provide a good current matching.



**Figure 4.6 Coarse and fine controls with the current folding topology.**

The fast path of the oscillator only consists of one delay cell per stage, as shown in Figure 4.4. Consequently, the maximum oscillation frequency of the implemented VCO is determined by the delay cell in the fast path. Incorporating the first criterion in Equation 4.2 and the transfer function in Equation 4.3, the maximum oscillation frequency can be derived as

$$f_{max} = \frac{\sqrt{2}}{4\pi r_{o3} R_1 C_1 C_L} \left\{ g_{m1}^2 r_{o3}^2 (R_1 C_1)^2 + 2r_{o3}^2 g_{m3} R_1 C_1 C_L - (C_1 + C_L)^2 r_{o3}^2 - 2(C_1 + C_L) r_{o3} R_1 C_1 - (R_1 C_1)^2 + \dots \right. \\ \left. \left[ g_{m1}^4 r_{o3}^4 (R_1 C_1)^4 - 2g_{m1}^2 r_{o3}^2 (R_1 C_1)^4 + 4(C_1 + C_L) r_{o3} (R_1 C_1) \left( (C_1 + C_L)^2 r_{o3}^2 + \frac{3}{2}(C_1 + C_L) r_{o3} (R_1 C_1) + \dots \right) \right. \right. \\ \left. \left. (R_1 C_1)^2 \right) + (C_1 + C_L)^4 r_{o3}^4 - 2g_{m1}^2 r_{o3}^2 (R_1 C_1)^2 (C_1 + C_L) \left( r_{o3}^2 (C_1 + C_L) + 2r_{o3} R_1 C_1 \right) + (R_1 C_1)^4 - 4r_{o3}^2 R_1 \dots \right. \\ \left. C_1 g_{m3} C_L \left( (R_1 C_1)^2 - g_{m1}^2 r_{o3}^2 (R_1 C_1)^2 + r_{o3}^2 (C_1 + C_L)^2 + 2r_{o3} R_1 C_1 (C_1 + C_L) + r_{o3}^2 R_1 C_1 C_L g_{m1}^2 / g_{m3} \right) \right]^{1/2} \left. \right\}^{1/2} \quad (4.12)$$

When the control voltage is at one extreme so that all the tail current is steered to the fast path, the slow path is disabled. From Equation 4.12, a maximum oscillation frequency of approximately 2.1 GHz (with  $R_I = 5 \text{ k}\Omega$ ,  $C_I = 0.194 \text{ fF}$ ,  $g_{m1} = 3.706 \text{ mS}$  and  $g_{m3} = 1.535 \text{ mS}$ ) is yielded.

Conversely, disabling the fast path and enabling only the slow path due to an extra delay cell in the slow path, the minimum oscillation frequency results. The weighted sum of the delays of the two delay cells in the slow path constitutes the total delay of each stage. Thus, the delay of the slow path per stage can be expressed as [32]

$$T_d = (1/g_{m9,10}) C_{L,c} + (R_I / (1 + R_I g_{m3,4})) C_L, \quad (4.13)$$

where  $C_{L,c} \approx 0.13 \text{ pF}$  is the output capacitance of the differential pair with the constant tail current. Using Equation 4.13 and 4.7, the minimum oscillation frequency is approximately equal to 834.2 MHz with  $g_{m9,10} = 0.878 \text{ mS}$  and  $g_{m3,4} = 1.16 \text{ mS}$ ,

### Phase Noise and Jitter in the Ring Oscillator [31]

In optical communication systems, the clock signal is generated to drive the sampling circuits in which phase noise performance is critical. The noise requirements are more stringent as system speed increases. In a single chip integrated circuit substantial noise is produced by different functional circuits [33]. Nevertheless, the reduction of jitter due to VCO fluctuations has been shown [33] to be the key design factor for low-jitter CDR circuits. The VCO is assumed to be the dominant jitter source in the closed loop conditions. With the implementation of differential circuit techniques, the power supply noise can be minimised.

Consider that the voltage amplitude change caused by the current impulse is small and the phase shift is linearly proportional to the injected charge [34]. Furthermore, assume that the phase noise is much smaller than the period of the oscillation. The loop can be considered to be linear and noise contributions can be expressed by the transfer function [35]. The linearised model of ring oscillators in Figure 4.2 was employed to estimate the phase noise at the output of the oscillator [31]. In the analysis, white, unrelated noise sources are assumed and the amplitude of the noise signal is assumed to be much smaller than the clock signal. Assume that various noise components are injected into the signal path. From Equation 4.1, the noise power spectral density at a frequency  $\Delta\omega$  offset from the oscillation frequency  $\omega_0$  can be expressed as

$$\frac{|V_{out}[j(\omega_0 + \Delta\omega)]|^2}{|V_{in}[j(\omega_0 + \Delta\omega)]|^2} \approx \frac{1}{(\Delta\omega)^2 \left| \frac{dH}{d\omega} \right|^2}. \quad (4.14)$$

The transfer function of one delay stage is described in Equation 4.3. As mentioned earlier, two delay stages are required for oscillation with quadrature outputs. Then the oscillator transfer function can be written as

$$H(j\omega) = \left( -\frac{g_{m1}(1 + sR_1C_1)}{g_{m3} + s(C_1 + C_L + R_1C_1/r_{o3}) + s^2R_1C_1C_L} \right)^2, \quad (4.15)$$

and its derivative is

$$\frac{dH}{d\omega} = \frac{j2g_{m1}R_1C_1(-j\omega g_{m1}R_1C_1 - g_{m1})}{\left( -\omega^2R_1C_1C_L + j\omega\left( C_1 + C_L + \frac{R_1C_1}{r_{o3}} \right) + g_{m3} \right)^2} - 2 \frac{(-j\omega g_{m1}R_1C_1 - g_{m1})^2 \left( -2\omega R_1C_1C_L + j\left( C_1 + C_L + \frac{R_1C_1}{r_{o3}} \right) \right)}{\left( -\omega^2R_1C_1C_L + j\omega\left( C_1 + C_L + \frac{R_1C_1}{r_{o3}} \right) + g_{m3} \right)^3}. \quad (4.16)$$

The three types of phase noise that have been identified [31] are subsequently discussed.

### Additive Noise

The noise of each differential pair and the load transistors is represented by the additive noise and is modelled as current sources,  $I_{n1}$  and  $I_{n2}$ , at the outputs of the delay stages. Relating noise currents to the VCO stages, since capacitors do not contribute noise [36], the effective output resistance of each stage can be described by  $(R_1/(1 + g_{m3}R_1))$ . Therefore, at a frequency in the vicinity of the oscillation frequency,  $\omega = \omega_0 + \Delta\omega$ , the total additive output phase noise power density is expressed as

$$|V_n[j(\omega_0 + \Delta\omega)]|^2 \approx 2 \left( \frac{R_1}{(1 + g_{m3}R_1)} \right)^2 \left| \frac{V_{out}[j(\omega_0 + \Delta\omega)]}{V_{in}[j(\omega_0 + \Delta\omega)]} \right|^2 I_{n1,2}^2. \quad (4.17)$$

The oscillation frequency is usually also modulated by the flicker  $1/f$  noise of the transistors. However, when the VCO is placed within a PLL, the  $1/f$  noise is rejected by the PLL loop filter [35]. Hence, the thermal noise per unit bandwidth of MOS transistors is expressed as [36]

$$I_n^2 = 4kT \left( \frac{2}{3} g_m \right), \quad (4.18)$$

where  $k$  is Boltzmann's constant, and at room temperature  $4kT = 1.66 \times 10^{-20}$  V-C .

Thus,

$$|V_{n1}[j(\omega_0 + \Delta\omega)]|^2 \approx \frac{16kT}{3} (g_{m1} + g_{m3}) \left( \frac{R_1}{(1 + g_{m3}R_1)} \right)^2 \left| \frac{V_{out}[j(\omega_0 + \Delta\omega)]}{V_{in}[j(\omega_0 + \Delta\omega)]} \right|^2. \quad (4.19)$$

### ***High-Frequency Multiplicative Noise***

This noise is caused by the nonlinearity that exists in differential stages. When a white noise with an amplitude of  $A_n$  at a frequency of  $\omega_n$  is injected at the VCO input in a differential configuration,  $V_{in}(t) = A_0 \cos(\omega_0 t) + A_n \cos(\omega_n t)$ , the output signal

$$V_{out}(t) \propto \alpha_3 A_0^2 A_n \cos(2\omega_0 - \omega_n)t \quad (4.20)$$

becomes a significant cross-product. Due to the nonlinear behaviour of the circuit, the low-frequency noise is up-converted to the region above  $\omega_0$  and high-frequency noise is down-converted to the region below  $\omega_0$ . As a result, as indicated from simulation results [31], the noise power spectrum estimated in Equation 4.19 is effectively doubled.

### ***Low-Frequency Multiplicative Noise***

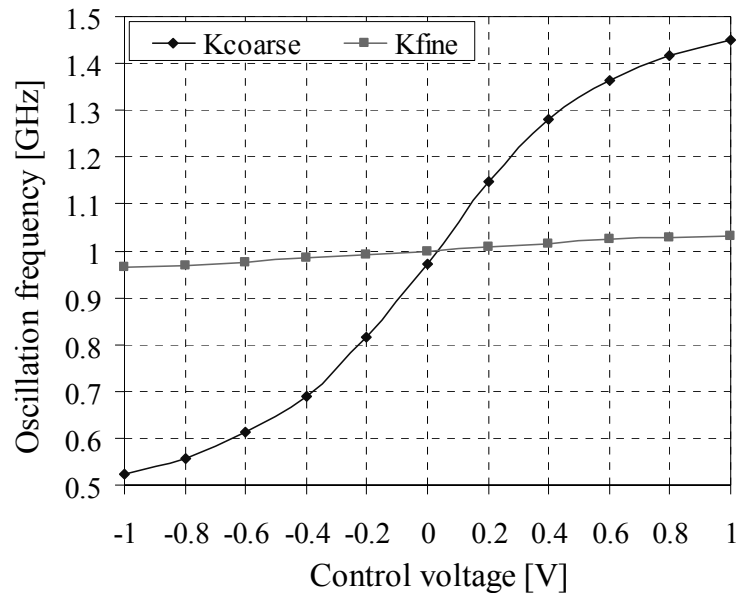
In the implemented VCO, the oscillation frequency is adjusted by varying the tail current. Thus, noise in the tail current can cause frequency modulations and contribute to the output jitter. The current components  $I_{ns} = \left( \frac{\sqrt{3}}{4} \right) I_{n0} \cos(\omega_0 \pm \omega_n)t$  exist in the signal path when the frequency is corrupted by the tail current noise,  $I_n = I_{n0} \cos(\omega_n t)$ , produced by the tail current source transistors. Then the output phase noise power density is expressed as

$$|V_{n2}[j(\omega_0 + \Delta\omega)]|^2 \approx 2 \left( \frac{\sqrt{3}}{4} \right)^2 \left( \frac{R_1}{(1 + g_{m3}R_1)} \right)^2 \left| \frac{V_{out}[j(\omega_0 + \Delta\omega)]}{V_{in}[j(\omega_0 + \Delta\omega)]} \right|^2 |I_n|^2. \quad (4.21)$$

### Estimation and Simulation

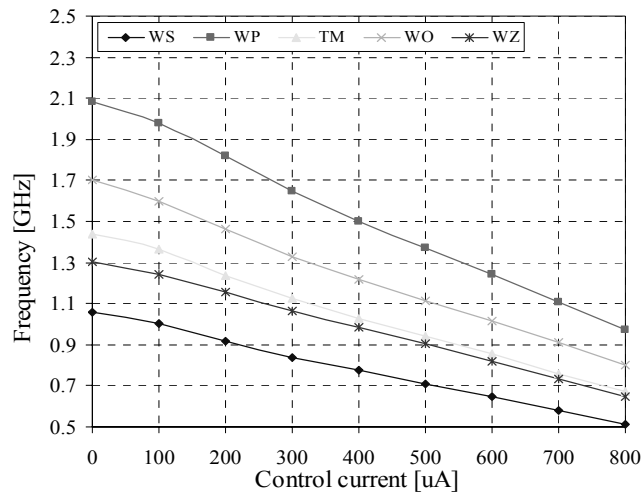
Using Equations 4.19 and 4.21,  $|V_{tot}[j(\omega_0 + \Delta\omega)]|^2 = 2|V_{n1}[j(\omega_0 + \Delta\omega)]|^2 + |V_{n2}[j(\omega_0 + \Delta\omega)]|^2$ , the total output phase noise power of  $1.4276 \times 10^{-17} \text{ V}^2/\text{Hz}$  was estimated at the output of the oscillator.

Simulations were done on the VCO circuit. Figure 4.7 depicts the frequency characteristic of the voltage-controlled oscillator versus both coarse and fine control voltage. It can be seen that the fine and coarse control sensitivities of the VCO for the typical-mean transistor models are  $K_{Fine} = 37.5 \text{ MHz/V}$  and  $K_{Coarse} = 537.875 \text{ MHz/V}$  respectively. As shown, the lock range is approximately equal to 32 MHz.

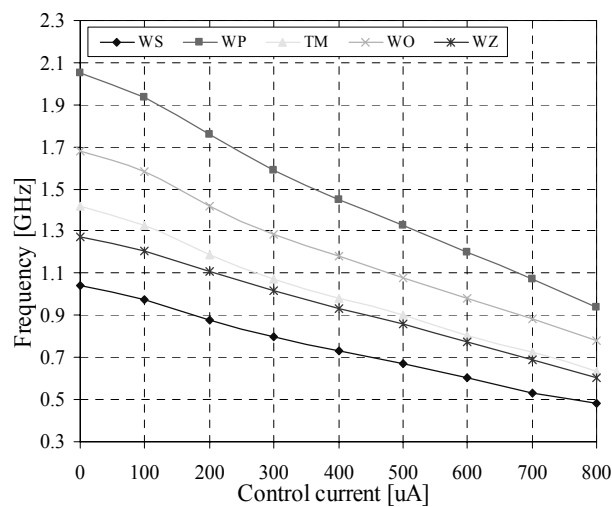


**Figure 4.7 VCO characteristic.**

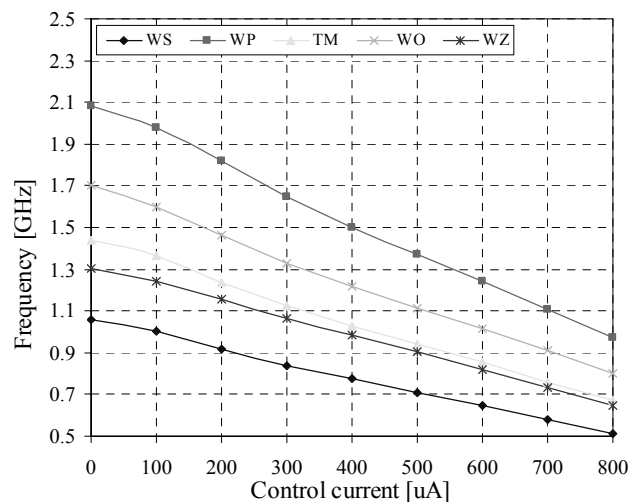
Figure 4.8 depicts the VCO coarse control sensitivity across the four corners and the typical-mean simulation models. It indicates that the VCO is typically sensitive to the worst-speed and worst-power transistor models. However, the qualities of resistors and capacitors do not have any obvious effect on the VCO sensitivity. In the simulation, the tail current was varied differentially, where the sum of the two tail current remains as  $800 \mu\text{A}$ . As shown in the figures, in the worst-power transistor simulation, the tuning range is about 15 MHz in the negative direction around the center frequency, and about 40 MHz in the positive direction in the worst-speed transistor simulation. If less current is partitioned to the slow path, a greater range can be obtained in the worst-power transistor simulation. Unfortunately, in a non-ideal environment, the frequency range around the center frequency is undesirably decreased, although it is still operational at 1 Gb/s.



(a)



(b)

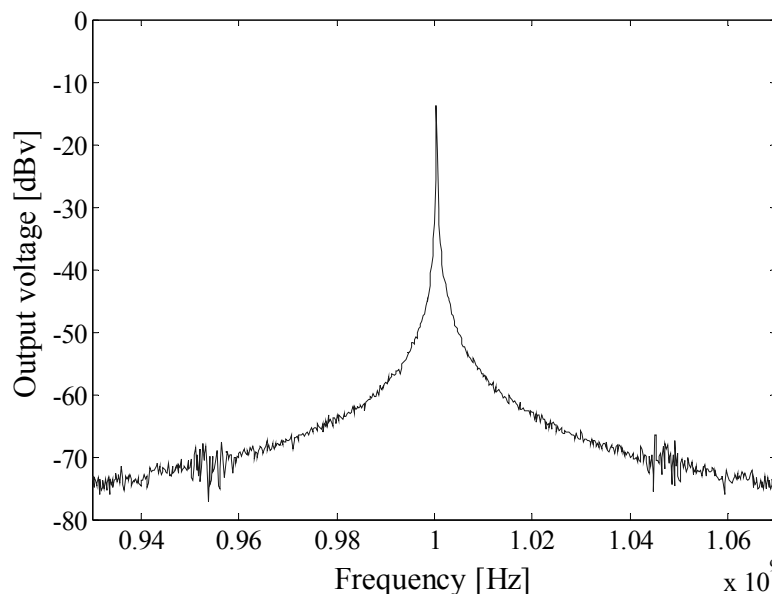


(c)

**Figure 4.8 Free running characteristics of VCO at different transistor process conditions with (a) typical-mean resistor and typical-mean capacitor models; (b) worst-speed resistor and worst-speed capacitor models; and (c) worst-power resistor and worst-power capacitor models.**

The frequency range can be increased by increasing the sensitivity of coarse controlling transistors in the current folding circuit. However, in a certain tuning range there is an inevitable increase in the VCO gain. The oscillator becomes more susceptible to the current increase and undesirably and tremendously decreases the frequency of oscillation.

The free running output spectrum of the oscillator is illustrated in Figure 4.9. It was obtained by processing the simulated time domain output waveform in Matlab. The additive noise, high-frequency multiplicative noise and tail noise current were modelled by sinusoidal voltage and current sources superimposed at the output branches and to the tail current sources of the oscillator. As can be seen, the phase noise in the VCO is approximately equal to  $-91.8$  dBc/Hz at a 1 MHz offset relative to the carrier frequency.



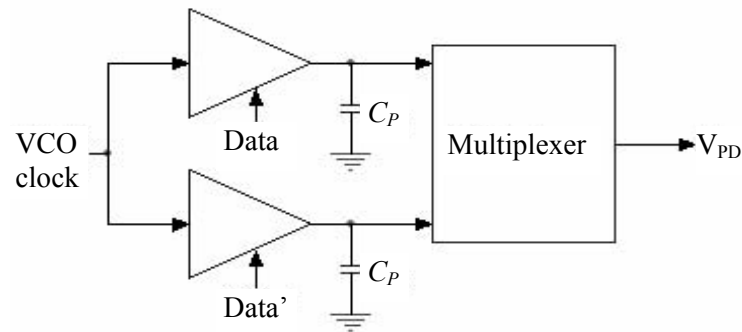
**Figure 4.9 Free-running spectrum of the oscillator.**

#### **4.2.1.2 Linear Phase Detector**

The phase detector is the key component for generating the phase error between the VCO clock signal and the data sequence. When the difference between the clock frequency and the data rate is small enough for the VCO clock signal to fall within the capture range of the phase detector, the frequency detector is disabled and the phase detector takes over. Once the phase lock is achieved, the control voltage to the VCO should stay constant and should not be corrupted by the phase detector output. Thus, a low jitter phase detector is required.

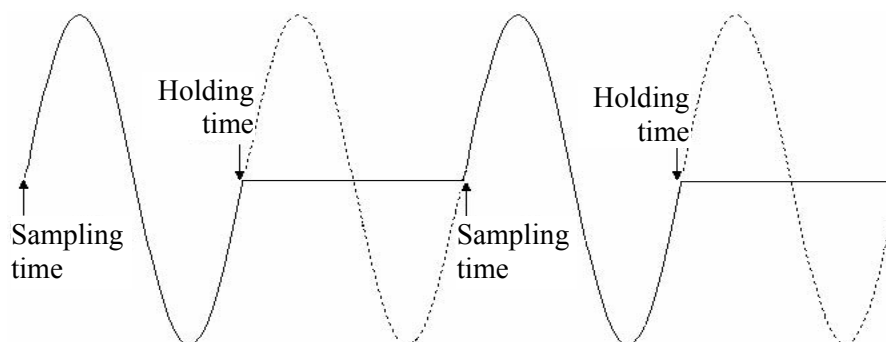


In digital mode operations, the binary nature of the phase detector creates significant jitter on the control line in the locked loop and at the CDR output [37]. In order to minimise jitter generation, the analogue phase detector was implemented to provide a linear behaviour. The phase detector consists of two sample-and-hold circuits as described in [20] and a multiplexer.



**Figure 4.10 Linear phase detector.**

Figure 4.10 illustrates the general topology of the sample-and-hold phase detector. The general operation of the phase detector is described in Figure 4.11. At each rising data transition, one sample-and-hold circuit tracks the data and the other holds the instantaneous sampled voltage level. At every falling data transition, the unit that was in the tracking mode switches to the hold mode and stores the voltage level, while in the other it switches to the tracking mode. At every data transition, the multiplexer only selects the sample-and-hold unit that is in the hold mode, thus avoiding a transparent path from the input to the output and generating an output that is linearly proportional to the phase difference within the locking range.



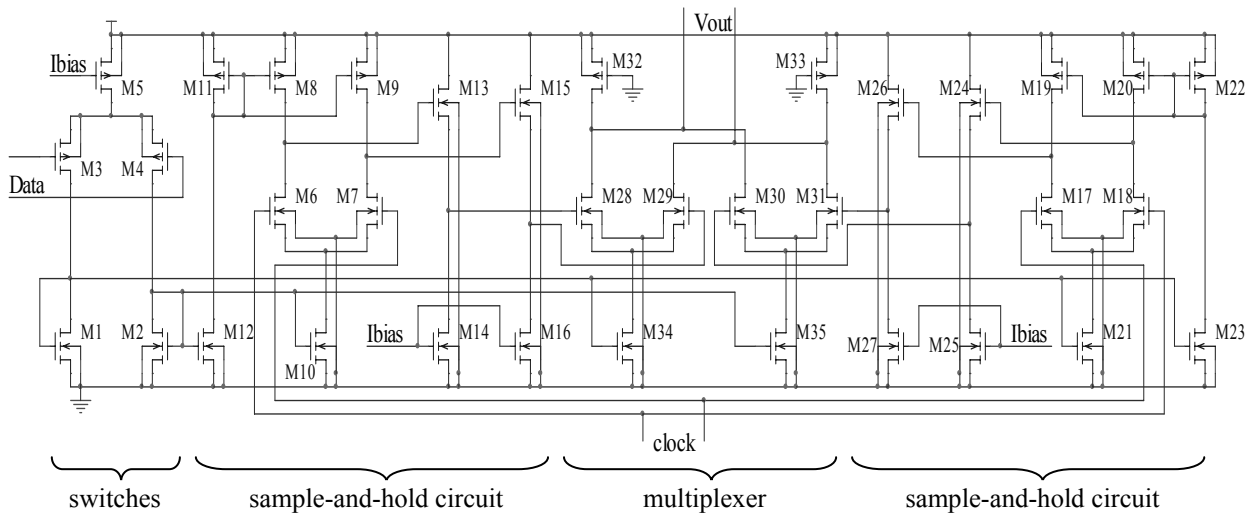
**Figure 4.11 Sampling example.**

Figure 4.12 depicts the circuit implementation of the phase detector. The tail currents of the sample-and-hold circuits and of the multiplexer are controlled by a current folding circuit allowing a low-supply voltage operation. In the current folding circuit, transistors

$M1-M4$  act as switches. They are designed with large widths and short channels to provide high speed and high driving capability. The sample-and-hold circuits were implemented with differential pairs and source followers. In the hold mode, the tail current and the load devices turn off simultaneously and the instantaneous voltage of the VCO is stored in the parasitic transistor capacitors of source followers that are connected at the outputs of the differential pairs. When transistor  $M11$  is on, transistors  $M8$  and  $M9$  operate in the triode region. The same applies to transistors  $M22$  and  $M19-M20$ . Taking the rise and fall time and the driving capability into account, a gate-source voltage of approximately 2 V was chosen for transistors  $M11$  and  $M22$ . At the drain current  $I_{D,11} = I_{D,22} = 1$  mA, this sets the dimensions of  $M11$  and  $M22$  to  $(W/L)_{11} = (W/L)_{22} \approx 8 \mu\text{m}/0.35 \mu\text{m}$ . In order to process the VCO signal at high speed, a small voltage gain of approximately 1.5 was chosen for the differential pairs of the sample-and-hold circuit. Setting the transconductances at  $(g_m)_{6,7} = (g_m)_{17,18} \approx 1.25$  mS, it requires a load resistance of 1.2 k $\Omega$  that is given by

$$R_{on} = \left[ K'_P \left( \frac{W}{L} \right) (V_{SG} - |V_{TH,P}|) \right]^{-1}, \quad (4.22)$$

where  $K'_P$  and  $V_{TH,P}$  are the gain factor and threshold voltage of the PMOS transistor respectively. The dimensions of the load transistors are thus set at  $(W/L)_{8,9} = (W/L)_{19,20} \approx 3 \mu\text{m}/0.35 \mu\text{m}$ .

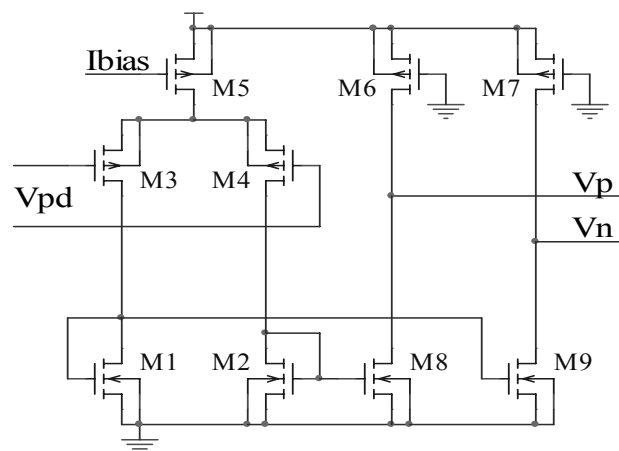


**Figure 4.12 Sample-and-hold phase detector.**

#### 4.2.1.3 Voltage-to-Current (V-I) Converter and Loop Filter

The V-I converter (as shown in Figure 4.13) is necessary for linearly converting the PD output voltage to a current that charges the loop filter that attenuates high frequency components of the loop and provides a fine control voltage to the oscillator. As depicted in

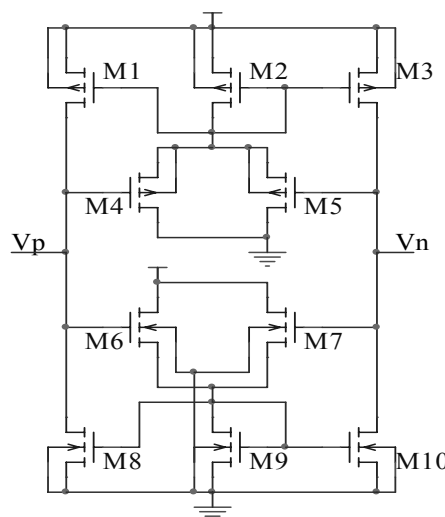
the figure, the phase detector output voltage is fed into the inputs of the PMOS differential pair and thus defines the current flows into the NMOS current mirrors that charge the loop filters. The output of the V-I converter is folded up to produce an output common-mode (CM) level that is compatible with the VCO control voltage. The matching and channel-length modulation of the transistors in the V-I converter stage impact on the static phase error between the data and the VCO output in locked condition. To minimise static error, a V-I converter with high output impedance and transistors with relatively large lengths and widths are required. The phase detector gain has a direct impact on the loop bandwidth [33]. Setting a large  $K_{PD}$  will result in a large loop bandwidth that can provide a good jitter reduction but is unable to provide a good suppression of the external input noise. However, setting a small loop bandwidth by implementing a small  $K_{PD}$ , the external input jitter can be significantly reduced but much of the VCO noise remains unreduced [35]. Compromising the two factors and the requirement of high output impedance, the V-I converter gain was chosen to be 2: the differential pair  $M3$ - $M4$  had a gain of 0.25 and the common-source amplifiers ( $M8$  and  $M9$  stages) had a gain of approximately 8.5. For transistor matching, the transistor lengths of current mirrors ( $M1$ ,  $M2$ ,  $M8$  and  $M9$ ) were chosen as  $1\ \mu\text{m}$  to reduce the effect of channel length modulation. The speed of the V-I converter is not stringent. The circuit only has to run at a frequency equal to the difference between the data rate and the VCO frequency. A small bias current of  $50\ \mu\text{A}$  was chosen for the differential pair. Set  $g_{m3,4}$  to  $70\ \mu\text{S}$ , the dimensions of transistors  $M1$ - $M4$  with  $(W/L)_{3,4} = 1.25\ \mu\text{m}/1.5\ \mu\text{m}$  and  $(W/L)_{1,2} = 4\ \mu\text{m}/1\ \mu\text{m}$  are required. To achieve high output impedances, the bias currents of the common-source stages are halved. This sets the  $R_{on,6-7}$  of  $M6$ - $M7$  PMOS transistors to  $63\ \text{k}\Omega$ , which translates to a  $(W/L)_{6,7}$  ratio of 0.1.



**Figure 4.13 V-I converter.**

A common-mode feedback circuit was included to provide correction to the output CM level. The CM level is adjusted by counteracting the common-mode variations on the differential lines ( $V_p$  and  $V_n$ ) of the loop filter, at which the DC output level is set at a value of approximately of  $V_{DD}/2$ , preventing transients from creating steady-state components on parasitic line capacitors. Figure 4.14 illustrates the common-mode feedback (CMFB) circuit topology.

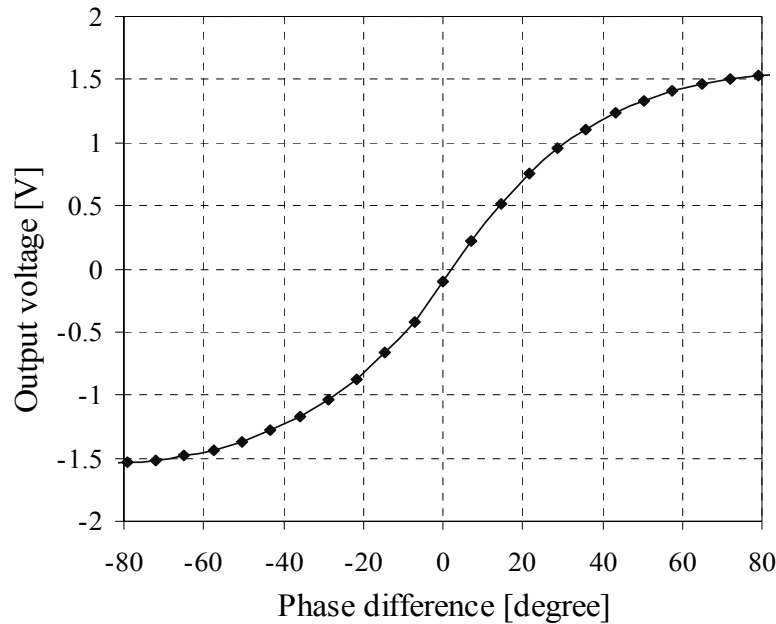
Transistors  $M4$ - $M7$  sense the common-mode voltage of  $V_p$  and  $V_n$ . When the CM voltage is higher than  $V_{DD}/2$ , the gate-source voltages  $V_{GS,6}$  and  $V_{GS,7}$  increase and cause NMOS transistors  $M8$  and  $M10$  to sink more current, thus discharging the two lines similarly and decreasing the common mode DC level. If the CM voltage is lower than  $V_{DD}/2$ ,  $V_{GS,4}$  and  $V_{GS,5}$  decrease, transistor  $M2$  responds accordingly and the current is mirrored to  $M1$  and  $M3$ . It causes  $M1$  and  $M3$  to source more current, therefore pulling up the common-mode voltage level of the loop filter outputs. At  $V_p = V_n = V_{DD}/2$ , the sunken and sourced currents of the NMOS ( $M8$ - $M10$ ) and PMOS ( $M1$ - $M3$ ) networks, respectively, are set at a small value of  $20 \mu\text{A}$  to limit the static power dissipation. The dimensions of unit transistors were implemented with  $(W/L)_{1-5} = 7.4 \mu\text{m} / 1 \mu\text{m}$  and  $(W/L)_{6-10} = 2.5 \mu\text{m} / 1 \mu\text{m}$ , for PMOS and NMOS transistors respectively, ensuring small overdrive voltages, thus the operation of transistors in saturation. Non-minimum lengths were implemented to reduce the effect of process variations.



**Figure 4.14 Common-mode feedback circuit.**

The input/output characteristic of the phase detector is shown in Figure 4.15. The phase detector gain is equal to  $K_{PD} = 1.534 \text{ V/rad}$  in its linear range. Due to the systematic error

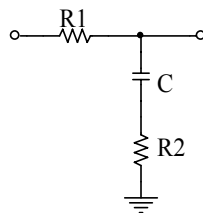
and different propagation delays between the data and the clock signal, as shown in the figure, a small phase error persists.



**Figure 4.15 Input/output characteristic of the phase detector with the V/I converter.**

### Loop Filter [33]

Jitter characteristics of the phase-locked loop are strongly dependent on the damping factor  $\zeta$  and the natural angular frequency  $\omega_n$  [31]. Thus, the loop parameters of the PLL must be optimised to achieve good jitter characteristics. The implementation of the PLL low-pass filter, as shown in Figure 4.16, was based on the design method of optimising the PLL parameters described in [33]. A small loop bandwidth and high damping factor are commonly implemented to reduce the input noise.



**Figure 4.16 Lead-lag loop filter.**

Based on the phase-transfer function, the jitter transfer function of the CDR with a simple lead-lag filter can be expressed as

$$H(j\omega) = \frac{\omega_n^2 + j\left(2\zeta\omega_n - \frac{\omega_n^2}{K}\right)\omega}{\omega_n^2 - \omega^2 + j2\zeta\omega_n\omega}, \quad (4.23)$$

where  $K$  is the open loop gain of the PLL.

By setting  $\zeta\omega_n = Z_w$ ,  $|H(j\omega)|$  is approximated by

$$|H(j\omega)| = \sqrt{\frac{(Z_w/\zeta)^4 + 4Z_w^2\omega^2}{((Z_w/\zeta)^2 - \omega^2)^2 + 4Z_w^2\omega^2}}. \quad (4.24)$$

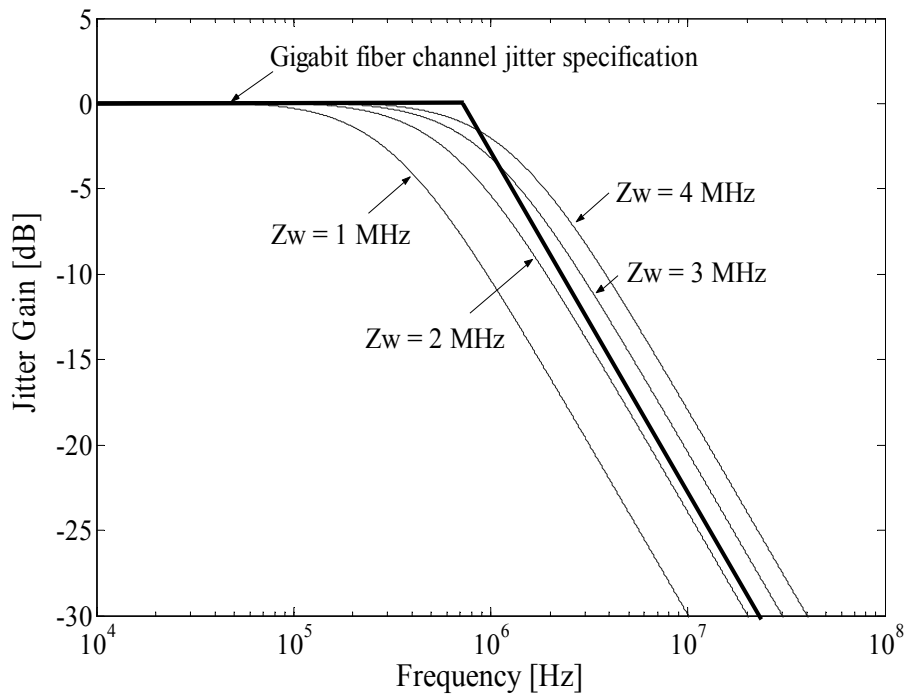
To alleviate jitter accumulation on the fibre link, it is recommended that the jitter peaking should be below 0.1 dB. Thus, at  $\omega = \omega_n$ , the jitter transfer curve can be expressed as

$$|H(j\omega)| \rightarrow \sqrt{1 + \frac{1}{4\zeta^2}} \leq 0.1 \text{ dB}. \quad (4.25)$$

Then the damping factor is set by Equation 4.23 as

$$\zeta \geq 4. \quad (4.26)$$

By examining Equation 4.24, it can be proved that the jitter transfer curve becomes independent of the damping factor when  $\zeta$  is larger than or equal to 4. As will be shown later, the value of  $\zeta$  directly impacts on the choices of the size of the loop filter's components. With the minimum value of  $\zeta = 4$ , the jitter transfer function for different values of  $Z_w$  is shown in Figure 4.17. As illustrated, in order to meet the jitter specification,  $Z_w \leq 2 \text{ MHz}$  has to be implemented.



**Figure 4.17 Jitter transfer function.**

It has been shown [33] that the output jitter of the CDR circuit is mainly caused by the additive noise at the input and the noise generated in the circuit. Assuming the additive white Gaussian noise, jitter generation (in phase deviation) is approximated by

$$\sigma_{out} \approx \sqrt{\frac{N_O}{A_m^2} Z_W + \frac{\eta\pi^2}{2} \frac{1}{Z_W} + 10\xi\pi^2 \frac{1}{Z_W^2}} \text{ [rad]}, \quad (4.27)$$

where  $N_O$  is the white noise power spectral density at the input,  $A_m$  is the input signal amplitude,  $\eta$  is the power spectral density of Gaussian white noise frequency modulation and  $\xi$  is the power spectral density of Gaussian flicker noise frequency modulation.

As shown in Equation 4.27, by maximising  $Z_W$ , a low output jitter CDR circuit can be obtained. Choosing the upper limit of  $Z_W = 2$  MHz and with  $\zeta = 4$  set, the loop filter time constant  $\tau_2$  is given as

$$\tau_2 = CR_2 = \frac{2\zeta^2}{Z_W} = 16 \text{ } \mu\text{s}. \quad (4.28)$$

The pull-in range (capture range) is related to the time constants,  $\tau_1$  and  $\tau_2$ , of the loop filter and is defined as

$$\Omega_p = 2Z_W \sqrt{2 \left( \frac{\tau_1}{\tau_2} + 1 \right)}. \quad (4.29)$$

For a given system, it is desirable to have a large pull-in range that can be obtained by maximising the ratio  $\tau_1/\tau_2$ . However, it is limited by the open loop gain and the limited phase comparison range

$$K_{cr} = 2Z_W \left( \frac{\tau_1}{\tau_2} + 1 \right). \quad (4.30)$$

The open loop gain of the PLL is defined as

$$K = K_{PD}K_{Fine}, \quad (4.31)$$

where the phase detector gain is  $K_{PD} = 1.534$  V/rad and the VCO fine control gain is  $K_{Fine} = 37.5$  MHz/V. As shown in Figure 4.15, the transfer characteristic of the phase comparator has a limited range. In order to obtain phase lock, the phase difference between the VCO frequency and the data signal must be less than  $\pm 40$  degree. Thus, the gain related to the capture range is defined as

$$K_{cr} = K(2\pi/9). \quad (4.32)$$

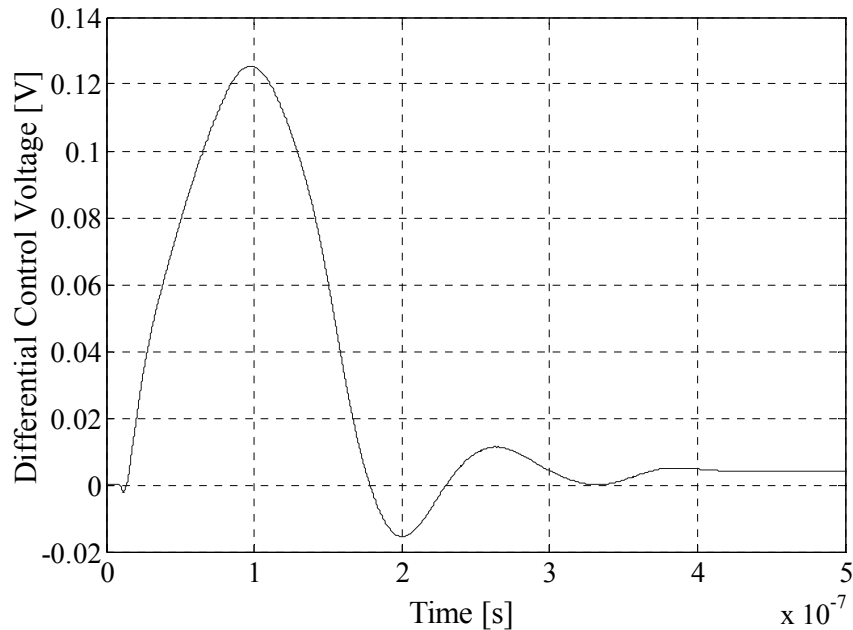
Equating formulae 4.30 and 4.32, the ratio of the two time constants is

$$\tau_1/\tau_2 \approx 9. \quad (4.33)$$

Then,

$$\tau_1 = C(R_1 + R_2) \approx 144 \mu\text{s}. \quad (4.34)$$

Choosing  $C = 150 \text{ pF}$ , then  $R_2 = 106 \text{ k}\Omega$  and  $R_1 = 854 \text{ k}\Omega$ .



**Figure 4.18 PLL differential control voltage output during phase acquisition.**

A  $2^{10}-1$  pseudorandom bit sequence (PRBS) was generated by a gold-sequence generator in Simulink in Matlab. Figure 4.18 depicts the behaviour of the overall phase-locked loop circuit at the transistor level in response to the 1 Gb/s  $2^{10}-1$  PRBS data. During the acquisition period, the phase between the VCO signal and the input data is compared and adjusted through the feedback loop. A transition of approximately 420 ns is required before phase lock.

### Jitter [38]

Ideally, the spacing between clock transitions should be constant. However, the noise sources involved cause the transition spacing to be variable and uncertain. This uncertainty results in a difficulty for the estimation of the statistics of jitter. Nonetheless, jitter can be indirectly determined from its relationship with the associated phase noise, as its corresponding free-running phase noise can be more easily approximated. Assume that the phase noise is a result of only white noise sources. Then the closed-loop jitter of a phase-locked oscillator can be approximated by

$$\Delta T_{PLL} = \frac{1}{\sqrt{2\pi}f_u} \sqrt{S_\phi(\Delta\omega)} \frac{\Delta\omega}{\omega_0} \text{ [s]}, \quad (4.35)$$

where  $S_\phi(\Delta\omega)$  is the relative phase noise power at an offset frequency of  $\Delta\omega$  and  $f_u$  is the -3 dB frequency of the PLL.



The -3-dB frequency of a second-order PLL with a zero can be described as [36]

$$f_u = K_{PD} K_{Fine} \left( \frac{\omega_1}{\omega_2} \right), \quad (4.36)$$

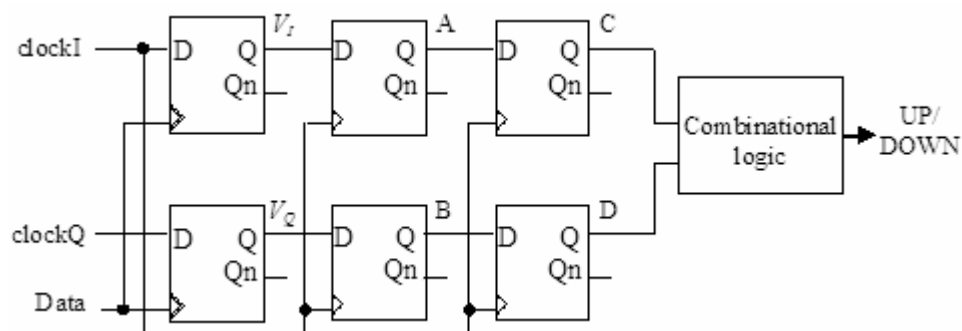
where  $\omega_1$  and  $\omega_2$  denote the pole and the zero of the loop filter respectively.

With the design parameters, the closed-loop unity-gain bandwidth was computed to be approximately equal to 20 MHz and the closed-loop jitter performance at 1 GHz is equal to 2.32 ps rms.

#### 4.2.2 Frequency-Locked Loop

Systems in the fibre optical communication network have to ensure an exact data rate operation required. However, process and temperature variations result in a large deviation between the VCO frequency and the input data rate, which may cause a false clock signal extraction. In order to guarantee the VCO oscillation at the data rate with a tolerable discrepancy, the oscillator was designed with a wide frequency tuning range. Due to the small capture range of the phase detector, the PLL CDR circuit cannot acquire lock when the data rate and the VCO's starting oscillation frequency differ greatly. This problem was relaxed by the implementation of a frequency-locked loop. The frequency detector compares the VCO oscillation frequency and the data rate, and adjusts the VCO frequency to a value where the difference between the two frequencies is small enough for acquiring phase lock. The frequency detector then becomes inactive and the phase detector takes over to align the phase.

##### 4.2.2.1 Frequency Detector [40]



**Figure 4.19 Schematic of the frequency detector.**

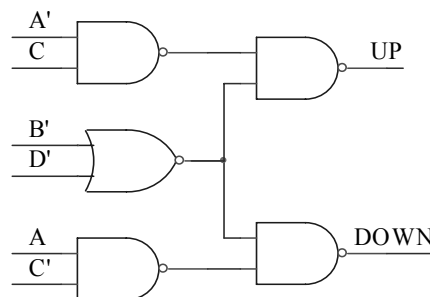
In the project, the frequency detector was realised with a digital quadricorrelator [17, 40], the operation of which is based on the bang-bang concept. The in-phase and the quadrature clock signals are sampled at the rising and falling edges of the NRZ data signal, generating

the corresponding in-phase and quadrature baseband components,  $V_I$  and  $V_Q$  (as shown in Figure 4.19). During the operation, when there is a frequency difference, a beat frequency proportional to this difference is generated at the output of the detector. The direction of the difference is determined by the relative zero crossings of the  $V_I$  and  $V_Q$  signals.

The operation of the circuit can be interpreted as follows. If  $V_Q$  leads  $V_I$ , the VCO frequency is too slow, and the VCO frequency is too fast when  $V_Q$  lags  $V_I$ . The comparison of the two signals is done through a synchronous transition detector which guarantees that the gain of the frequency detector is not affected by the input data rate. After the transition detector, combinational cells were implemented to realise the logic operation. At the output of the detector, an UP pulse is generated when the VCO frequency is slow and a DOWN pulse is generated when the VCO frequency is fast. If there is no frequency discrepancy, no output pulses are generated by the frequency detector. Thus, it does not affect the operation of the phase detector. Table 4.1 describes the operation scheme of the detector and was realised by the logic cells as shown in Figure 4.20.

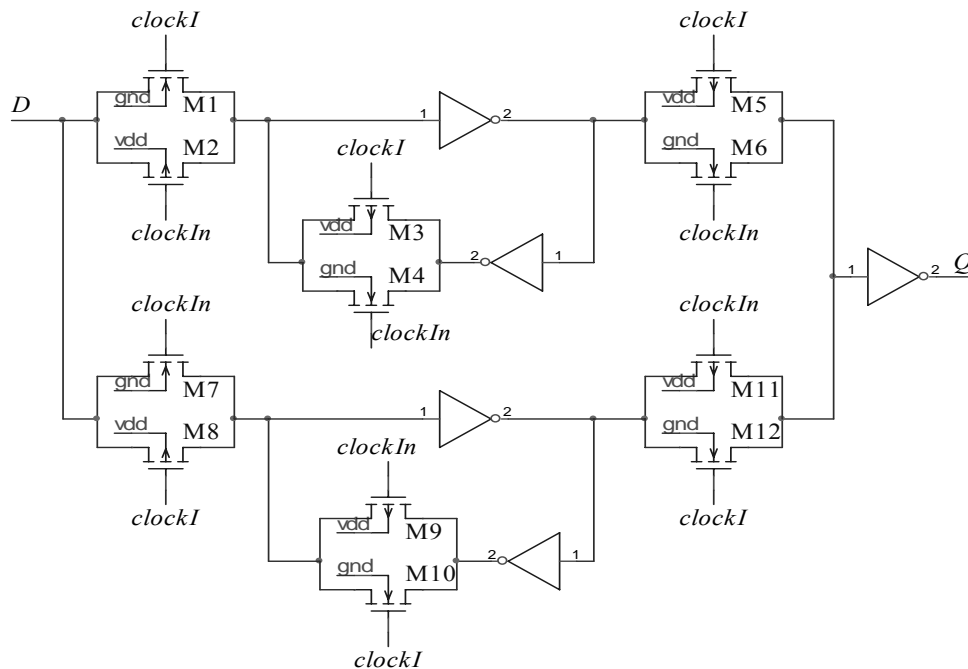
**Table 4.1 Truth table of the frequency detector (adapted from [40]).**

A	C	B	D	VCO frequency
0	0	×	×	RESET
0	1	0	0	UP
0	1	0	1	UP
0	1	1	0	UP
0	1	1	1	RESET
1	0	0	0	DOWN
1	0	0	1	DOWN
1	0	1	0	DOWN
1	0	1	1	RESET
1	1	×	×	RESET

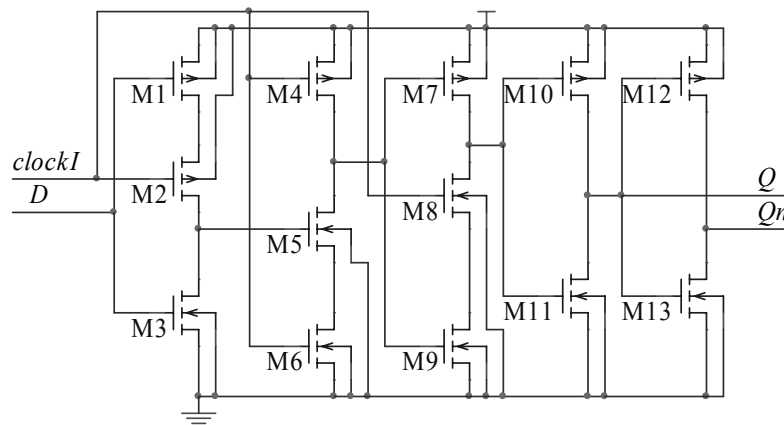


**Figure 4.20 Circuit implementation of the combinational logic.**

As shown in Figure 4.19, the data signal is used to clock the VCO signal, which oscillates at full-rate, at the two inputs of the frequency detector. For a faster locking, the two input detectors were implemented using double-edge-triggered flip-flops (DETFFs) to increase the correction rate of the CDR circuit and reduce the output jitter. The subsequent detectors were implemented with single-edge-triggered logic, since the full-rate VCO signal is applied to the triggers. Double-edge-triggered flip-flops, described in [41], were implemented for the two flip-flops at the input of the frequency detector. The design is shown in Figure 4.21. Due to the large number of subcircuits involved, it is expected to have a relatively high noise environment within the integrated circuit. Thus, as shown in the figure, transmission gates are used as pass transistors to alleviate the effect of charge injection.



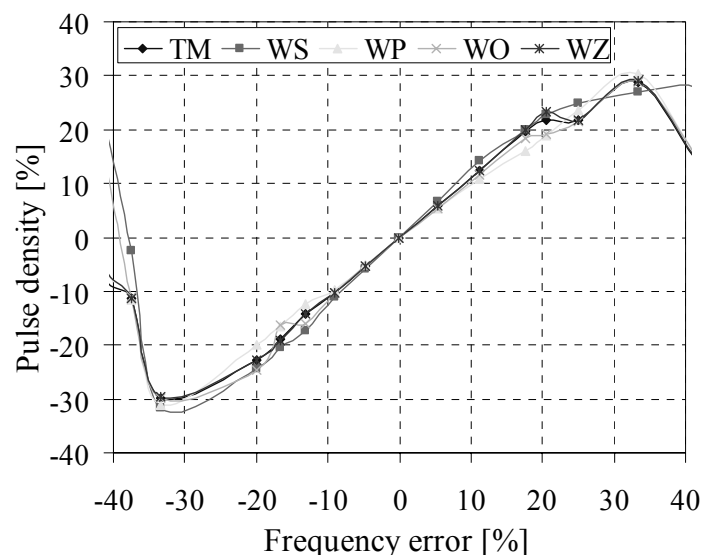
**Figure 4.21 Double-edge-triggered flip-flop.**



**Figure 4.22 Positive edge-triggered TSPC flip flop.**

In order to achieve a high clock frequency, true-single-phase-clock (TSPC) flip-flops [42], as shown in Figure 4.22, were implemented in place of the single-edge-triggered logic. The flip-flop shown in Figure 4.21 could have been modified to perform a single-edge-triggered operation. However, with this implementation, one of the outputs at the frequency detector is initialised to high and results in almost rail-to-rail voltages at the charge pump's outputs. These high differential signals cause nonlinearities in the FLL and large transients are necessary before frequency locking. To avoid the problem of initial voltages at the FD outputs, the TSPC flip-flops were utilised. By making the TSPC logic transistors strong, the flip-flop operating frequency was maximised. Unfortunately, the TSPC logic requires several clocked transistors and results in a relatively high power consumption.

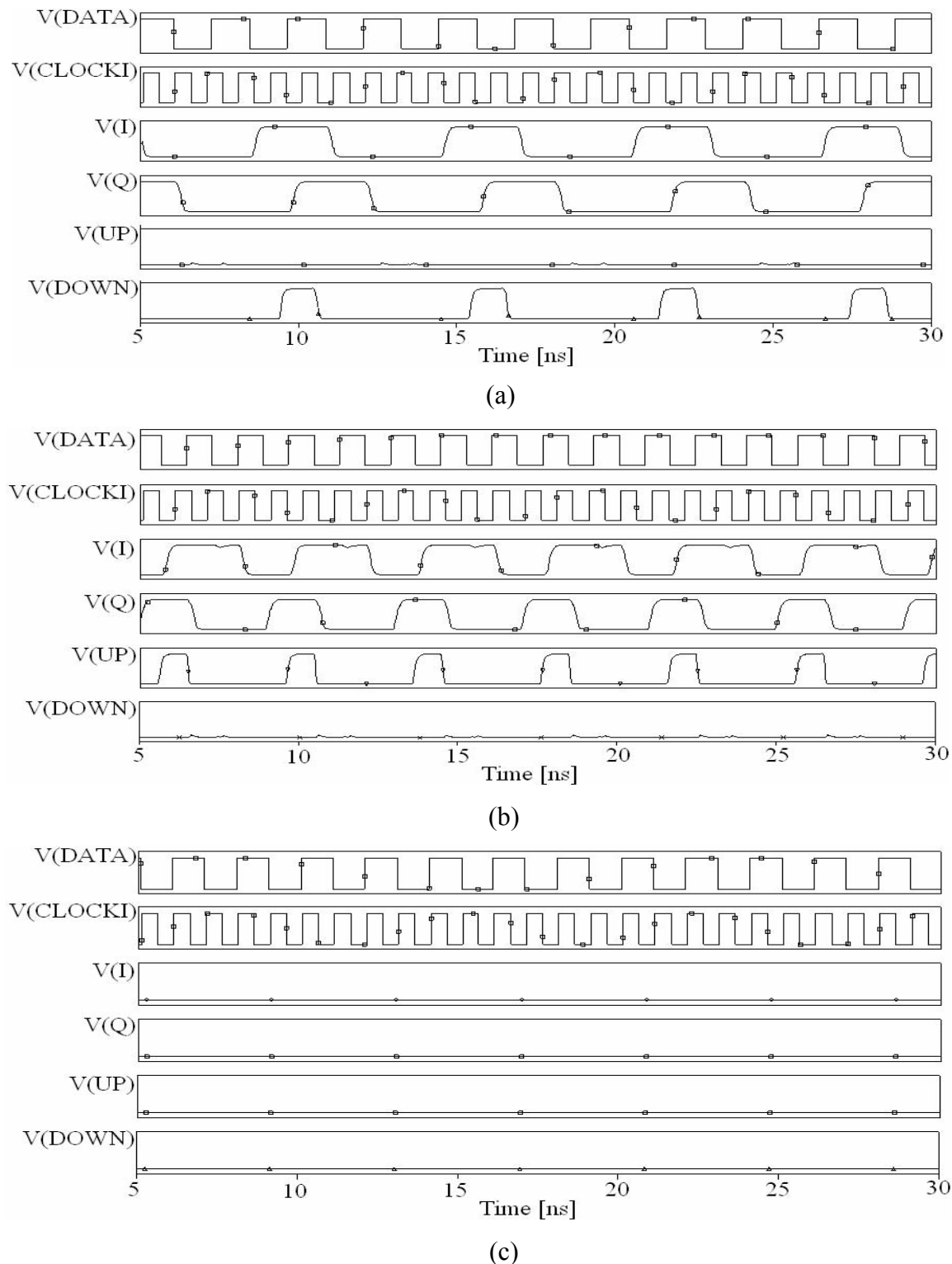
Figure 4.23 depicts the characteristics of the digital frequency detector. Simulations indicate that the detector is relatively insensitive to different process conditions. The percentage duty cycle at the output of the detector was represented by the pulse density. In the figure, the positive pulse density corresponds to an UP signal and the negative pulse density corresponds to a DOWN signal. As shown, the frequency detector can correct the oscillation frequency error to approximately  $\pm 32\%$  of the data rate.



**Figure 4.23** Frequency detector transfer function across different process corners.

Figure 4.24 illustrates the frequency detector's responses to a fast clock and to a slow clock. In response to a faster clock signal, the signal  $V_I$  leads  $V_Q$  and the DOWN pulses are produced at the output of the FD, as shown in Figure 4.24(a), to adjust the faster VCO frequency. In Figure 4.24(b), signal  $V_Q$  leads  $V_I$  and the FD outputs UP pulses to correct

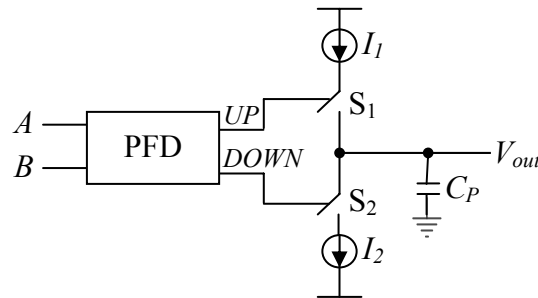
the slower VCO frequency. In response to a bit rate VCO clock signal, both the UP and DOWN outputs are quiet, as shown in Figure 4.24(c), providing no correction to the VCO frequency.



**Figure 4.24** Frequency detector timing diagrams with (a) a slow clock signal; (b) a fast clock signal; and (c) a bit rate clock signal.

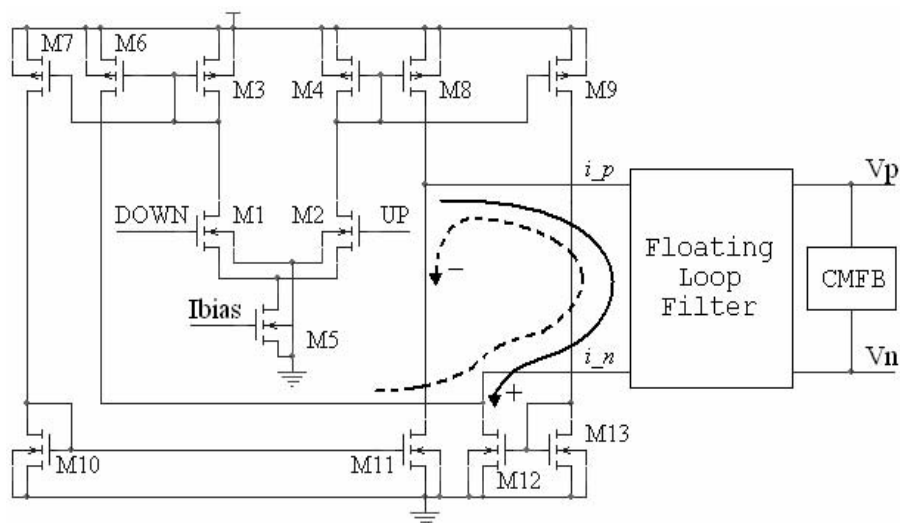
#### 4.2.2.2 Charge Pump and Loop Filter

Traditional charge pump circuits (Figure 4.25) have been realised by directly replacing the ideal switches with MOS transistors. Due to the nonideality of the PMOS and NMOS switches, charge injection occurs and a mismatch between the currents from the PMOS and NMOS transistors is generated [22].



**Figure 4.25 Traditional charge pump (adapted from [15]).**

The charge pump implemented in this project was based on the circuit proposed in [22]. It employs a switched current source with a positive and a negative current pump (as shown in Figure 4.26) to drive a floating loop filter. In the circuit, switching is done by means of a 3-state frequency detector where the UP and DOWN logic signals are converted by the charge pump into a VCO low frequency control signal.



**Figure 4.26 Differential charge pump (adapted from [22]).**

As illustrated in the figure, the circuit uses differential, current steering techniques to allow fast switching and alleviates charge-sharing problems. The differential topology also provides a high common-mode noise rejection and thus further reduces phase noise and spurs in the VCO. Two identical output paths are provided to charge and discharge loop filters in order to solve the problem of the current discrepancy generated in traditional

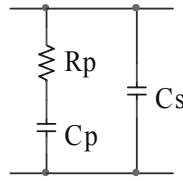
charge pump circuits. The operation of the charge pump can be explained as follows. Input transistors  $M1$  and  $M2$  act as current switches. During frequency locking, when the UP input signal is asserted and the DOWN signal is low, transistor  $M2$  is on and all the tail current is steered to  $M2$  providing a constant bias current to  $M4$ , which is then mirrored to transistors  $M8$ - $M9$ , with a mirroring ratio of 5. The NMOS current mirrors then force  $I_{D,11} \approx 0$  A and  $I_{D,12} \approx 125$   $\mu$ A and thus direct the flow of the output current in the positive direction through the floating loop filter. When DOWN is high and UP is unasserted, the tail current is steered to  $M1$  and mirrored to  $M6$ - $M7$  forcing  $I_{D,11} \approx 125$   $\mu$ A and  $I_{D,12} \approx 0$   $\mu$ A. Therefore, the current is pumped onto the loop filter in the negative direction. If both UP and DOWN inputs are asserted, the NMOS current mirror pairs ensure that the sourced and sunken currents are identical, creating zero static phase offset. For full tail current steering, it requires the input transistors in saturation. This can be done by setting the overdrive ( $V_{ov,1-2} = V_{GS,1-2} - V_{TH,n}$ ) voltage small. However, with a rail-to-rail switching signal, this design constraint is relaxed. The overdrive voltages for  $M1$ - $M2$  were chosen to be approximately 0.5 V, with a bias current of 50  $\mu$ A. This sets the  $(W/L)_{1,2}$  ratio to 2.5. To ensure operation in saturation, the gate-source voltage of the current mirror load ( $M3$ - $M4$ ) must satisfy the condition:

$$V_{SG,3-4} \leq V_{DD} - V_{DS\_sat,1-2} - V_{DS\_sat,5}, \quad (4.37)$$

where  $V_{DS\_sat}$  represents the drain-source voltage for which the transistor operates in the saturation region. With  $V_{DS\_sat,1-2} \geq (V_{GS,1-2} - V_{TH,n}) \approx 0.5$  V and  $V_{DS\_sat,5} \geq (V_{GS,5} - V_{TH,n}) \approx 0.3$  V, it requires  $V_{SG,3-4} \leq 2.5$  V. For  $V_{SG,3-4} = 1.2$ V, the  $(W/L)_{3,4}$  ratio is 2.5. With mirroring and perfect matching,  $V_{ov,3} = V_{ov,4} = V_{ov,6} = V_{ov,7} = V_{ov,8} = V_{ov,9} = 0.55$ V. This sets the margin for the gate-source voltage of transistors  $M10$  and  $M13$  to  $(V_{GS,10}, V_{GS,13}) \leq 2.75$ V. Since the currents are mirrored to  $M11$  and  $M12$  and the output common-mode voltage is set midway between the supplies,  $V_{ov,11}$  and  $V_{ov,12}$  have to be less than  $V_{DD}/2$  to ensure the transistors to operate in the saturation region. The overdrive voltage was therefore chosen as  $V_{ov,10} = V_{ov,11} = V_{ov,12} = V_{ov,13} \approx 1$  V to meet the above-mentioned conditions. This results in a small  $(W/L)_{11-13}$  ratio of 1.25, which can conserve layout area. In the design, long channel length transistors were used to minimise the mismatch between output currents.

The loop filter was implemented to eliminate the undesired high-frequency noise signals and to provide a stable control voltage to the VCO. The filter consists of a series  $RC$

network in parallel with a second capacitor (as shown in Figure 4.26), resulting in a type II third-order frequency-locked loop.



**Figure 4.26 Floating loop filter used in the FLL.**

A shunt capacitor is included to suppress the discrete voltage step at the VCO control voltage due to the instantaneous changes in the output current of the charge pump [15]. When  $C_P \gg C_S$ , second-order approximations can be made [22]. As capacitors are the most area-consuming element, the floating loop filter was implemented to minimise the layout area.

From Figure 4.26, the impedance of the passive filter can be derived as

$$Z(s) = \frac{s(C_P R_P) + 1}{s \left( s \frac{C_S C_P R_P}{C_S + C_P} + 1 \right) (C_S + C_P)} \quad (4.38)$$

Define the time constants which determine the pole and zero of the transfer function as

$$\begin{aligned} \tau_P &= R_P \frac{C_S C_P}{C_S + C_P}, \\ \tau_Z &= R_P C_P \end{aligned} \quad (4.39)$$

then the resulting open loop gain of the FLL can be expressed by

$$G(s)H(s) = \frac{I_P K_{Coarse}}{2\pi} \frac{s\tau_Z + 1}{s^2 (C_S + C_P) (s\tau_P + 1)}, \quad (4.40)$$

where  $I_P$  is the charge pump current in phase control mode and  $K_{coarse} \approx 537.9$  MHz/V is the VCO coarse control sensitivity.

From Equation 4.40, the cross-over frequency can be approximated by

$$\omega_C \approx \frac{I_P K_{coarse} R_P}{2\pi} \quad (4.41)$$

In [43], it is stated that the maximum capture range can be approximated by the open-loop bandwidth which is a function of loop filters. Using Equation 4.29, a capture range of 17.89 MHz is estimated. For a charge pump current of 125  $\mu$ A and  $K_{coarse} = 537.9$  MHz/V, a resistor value of 1.67 k $\Omega$  can be derived using Equation 4.40.



Let the zero frequency be approximately a factor of 5 below the cross-over frequency, then

$$C_p = \left( \frac{1}{\tau_z} R_p \right)^{-1} \approx 26.6 \text{ pF}. \quad (4.42)$$

From the open loop gain transfer function, the phase margin can be defined as

$$\phi(\omega) = 180^\circ + \tan^{-1} \left( \frac{\omega}{\omega_z} \right) - \tan^{-1} \left( \frac{\omega}{\omega_p} \right). \quad (4.43)$$

To ensure loop stability, a maximum phase margin is desirable. The frequency at which the maximum phase margin occurs can be found by setting the derivative of Equation 4.43 equal to zero,

$$\frac{d\phi}{d\omega} = \frac{\tau_z}{1 + (\omega\tau_z)^2} - \frac{\tau_p}{1 + (\omega\tau_p)^2} = 0. \quad (4.44)$$

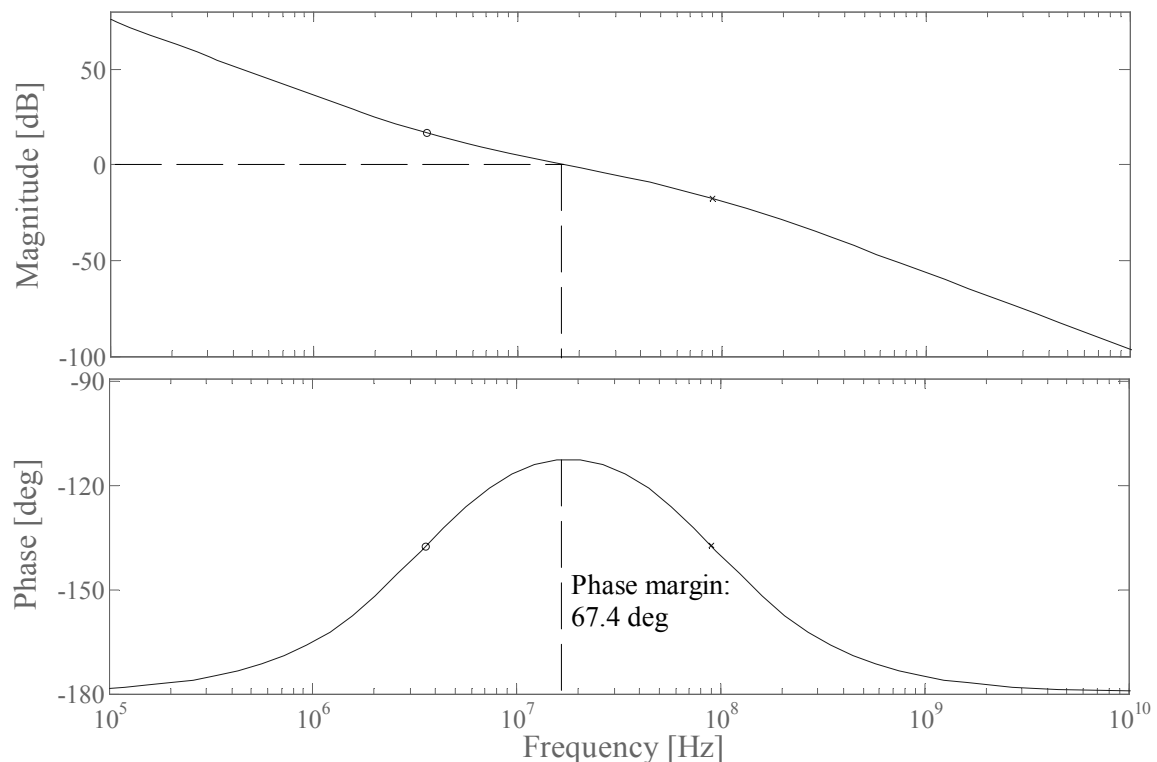
Solving the equation, the maximum phase margin is at

$$\omega_c = \sqrt{\omega_z \omega_p}. \quad (4.45)$$

Therefore the pole frequency is at  $\omega_p = 5\omega_c$  and the value of the shunt capacitor is

$$C_s = \left( \omega_p R_p - \frac{1}{C_p} \right)^{-1} \approx 1.1 \text{ pF}. \quad (4.46)$$

From the above design parameters, as shown in Figure 4.27, a phase margin and a cutoff frequency of approximately 67.4 degree and 17.2 MHz can be achieved respectively.



**Figure 4.27 FLL open loop gain bode plot.**

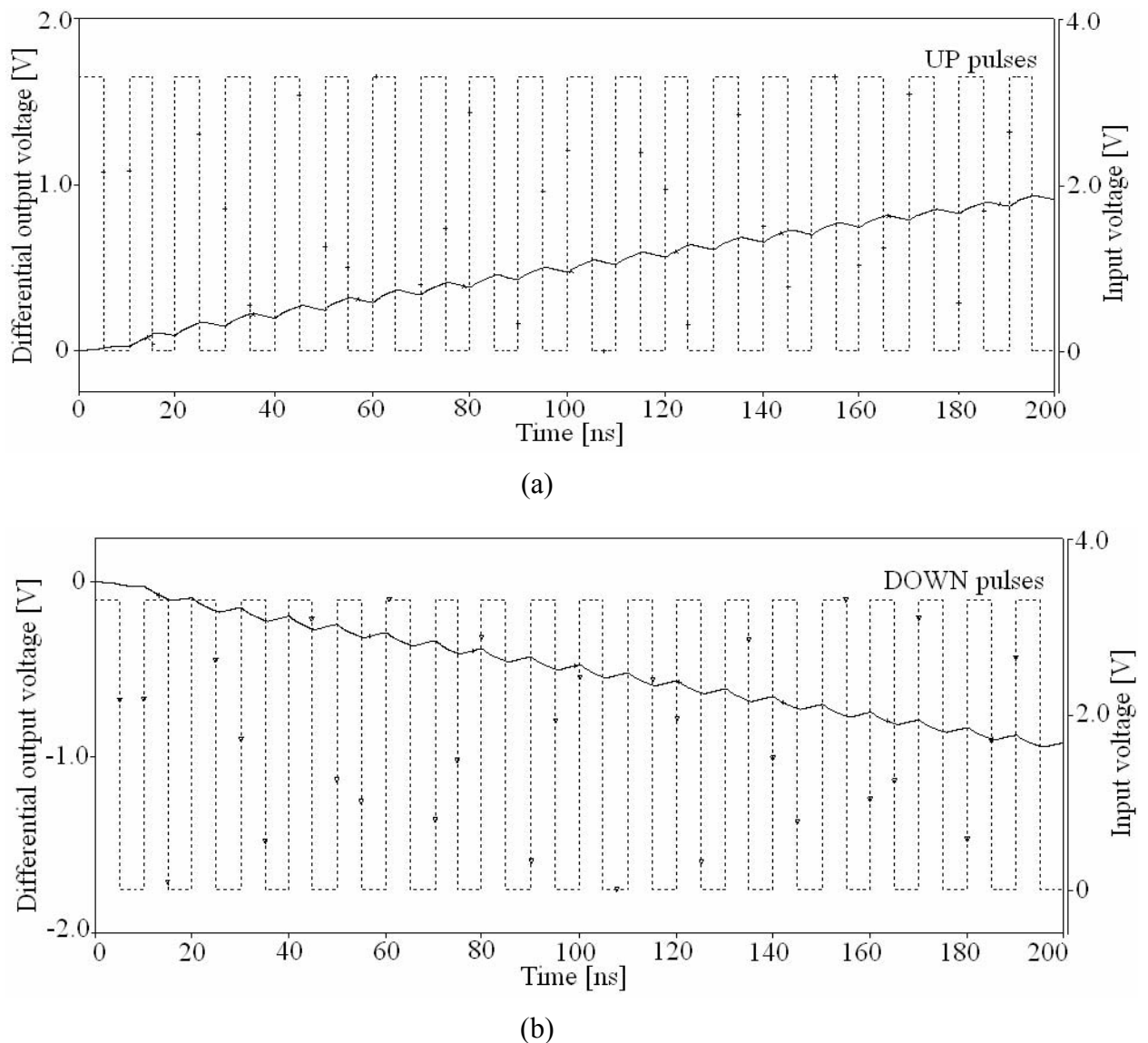
As can be seen, the resulting  $C_S$  is much smaller than  $C_P$ . Second-order approximation can be made and the delay time constant can then be approximated by [15]

$$\frac{1}{\zeta\omega_c} = \frac{4\pi}{R_p I_p K_{coarse}} \approx 111.9 \text{ ns}. \quad (4.47)$$

The common-mode feedback was implemented to define a loop-filter output CM level that is compatible with the VCO control voltage for stable frequency acquisition. The implementation of the CMFB circuit is shown in Figure 4.14.

### Simulation

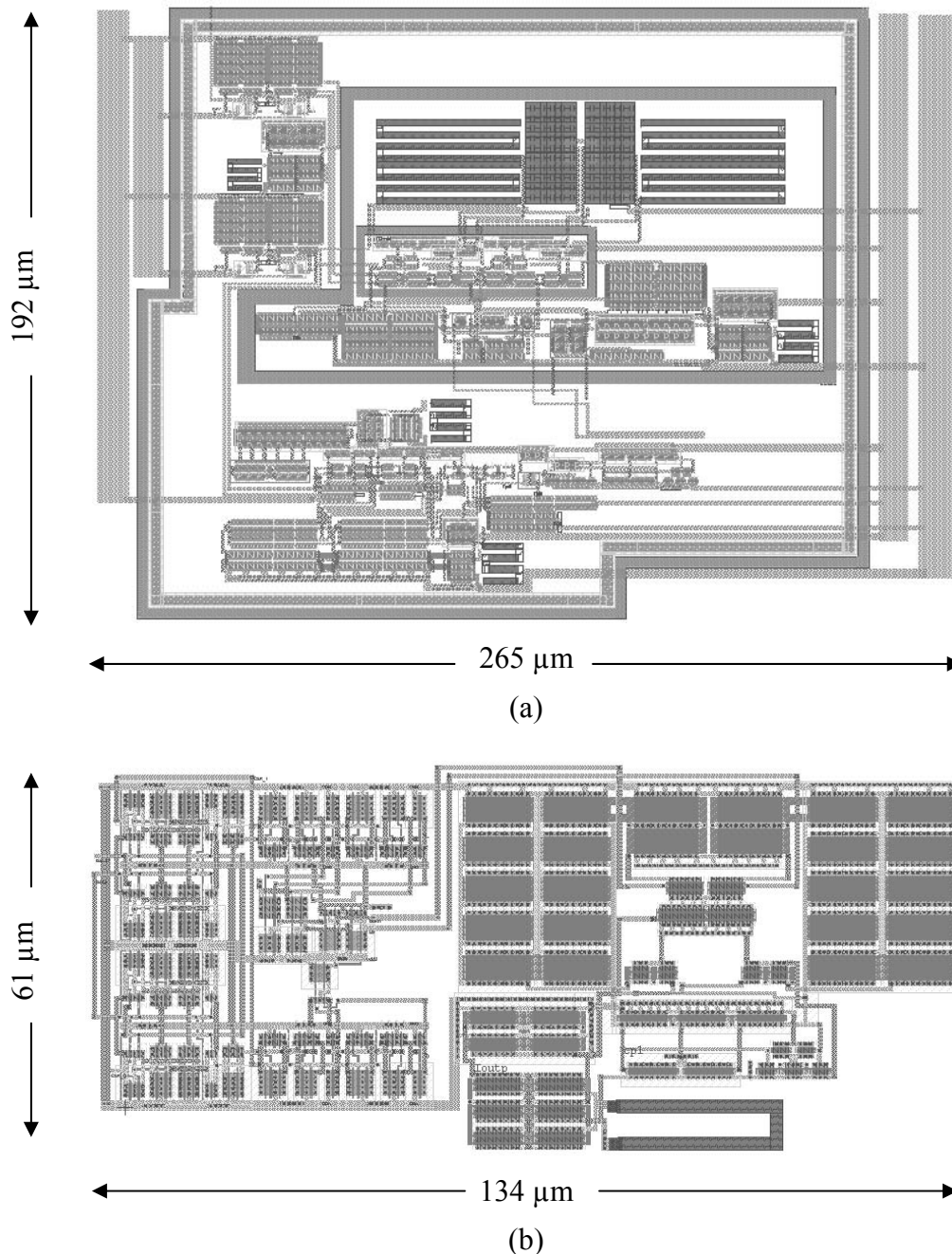
In simulation, load capacitance of 100 fF was used in place of the input capacitances of the coarse control input transistors of the VCO circuit.



**Figure 4.28 (a) Charging and (b) discharging action of the charge pump circuit.**

Figure 4.28 illustrates the functioning of the charge pump. When the UP signal is high and the DOWN signal is low, as shown in Figure 4.28(a), the charge is deposited onto the loop filter raising the differential output voltage. When the DOWN signal is activated and the UP signal is low, as shown in Figure 4.28(b), the NMOS current mirrors sink the current discharging the loop filter and decreasing the output voltage. It can be seen from both figures that when both of the input signals are low, the output voltage remains almost constant until the next input pulse is activated.

### 4.3 LAYOUTS



**Figure 4.29 Layout: (a) PLL circuit without the loop filters; (b) Frequency detector and charge pump.**

Figures 4.29(a) and 4.29(b) depict the layouts of the PLL and frequency detector circuits respectively. The common centroid method was applied to all differential circuits and the same orientation was used for all transistors in order to alleviate the effect of any diffusion gradients that might be present and to minimise the offset voltage of differential pairs. In addition, a substrate contact was placed between the sensitive small signal circuits and the large signal circuits to seal the noise generated in the circuits [33] and to create low resistance in the substrate. Unit transistors were used whenever current matching is necessary. The Metal 4 layer was used as far as possible for the routing as it has the least capacitance and resistances of all routing metals.

## CHAPTER 5

### OPTICAL RECEIVER

#### 5.1 INTRODUCTION

All circuits required for an optical receiver have been discussed separately thus far. The detector senses the photon input and transforms it into an electric current. The transimpedance amplifier, preamplifier and postamplifier that followed convert the current into a voltage and amplify it to a large enough swing for the clock and data recovery circuit. The CDR circuit, the core of the receiver, recovers the clock signal and uses this clock signal to retime the incoming data, thus improving the signal-to-noise ratio of the receiver. In this chapter, the performance of the complete system is discussed.

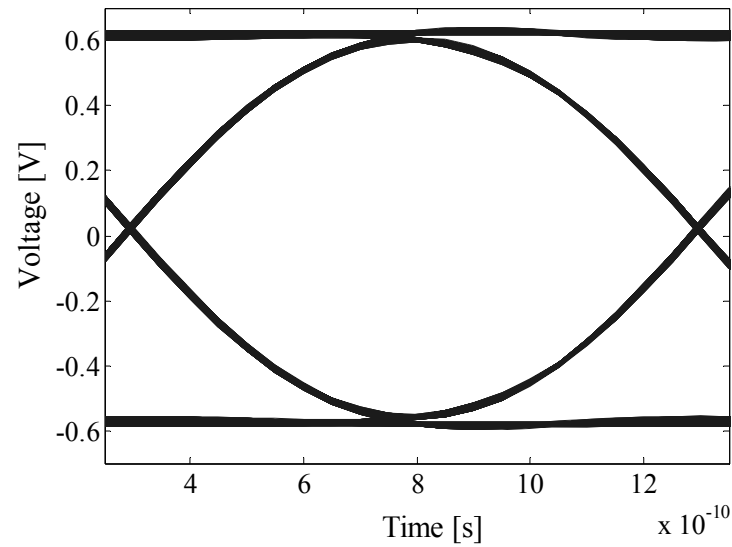
#### 5.2 OPTICAL RECEIVER SYSTEM

Table 5.1 summarises the performance of the system.

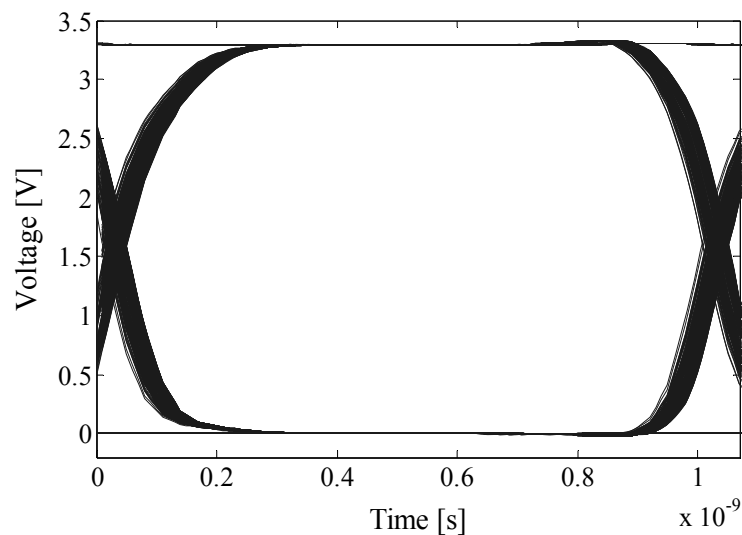
**Table 5.1 Performance summary of the optical receiver.**

<b>Bit rate</b>	1 Gb/s
<b>Front-end</b>	
Wavelength	770 nm ~ 860 nm
Photodetector responsivity at a wavelength = 860 nm	0.038 A/W
Detector capacitance	156 fF
Detector speed	8.5 GHz
Transimpedance gain	69.7 dB $\Omega$
Equivalent input referred noise current	182 nA
Sensitivity at a BER of $10^{-12}$	-19.7 dBm
Overall front-end gain	145.5 dB $\Omega$
Overall front-end bandwidth	769.2 MHz
<b>Clock and data recovery circuit</b>	
Capture range	17.89 MHz
Lock range	32 MHz
Tuning range	160 MHz
Phase noise at 1 MHz offset	-91.8 dBc/Hz
RMS jitter for $2^{10}$ -1 PRBS data	2.32 ps
<b>Total power dissipation</b>	155 mW
<b>Chip core area</b>	$0.853 \times 1.315 \text{ mm}^2$
<b>Technology</b>	AMS 0.35 $\mu\text{m}$ CMOS

The capture range is dependent on the type of the PLL loop filter used and is difficult to predict analytically [36]. For the lead-lag loop filter, however, the capture range can be estimated using Equation 4.29. Substituting design parameters into the equation, a capture range of approximately 17.89 MHz was estimated. The lock range is independent of the properties of the loop filter [36] and is determined by the VCO fine tuning range. The fine tuning range of the VCO in Figure 4.7 indicates that the PLL system has a lock range of approximately 32 MHz.



(a)



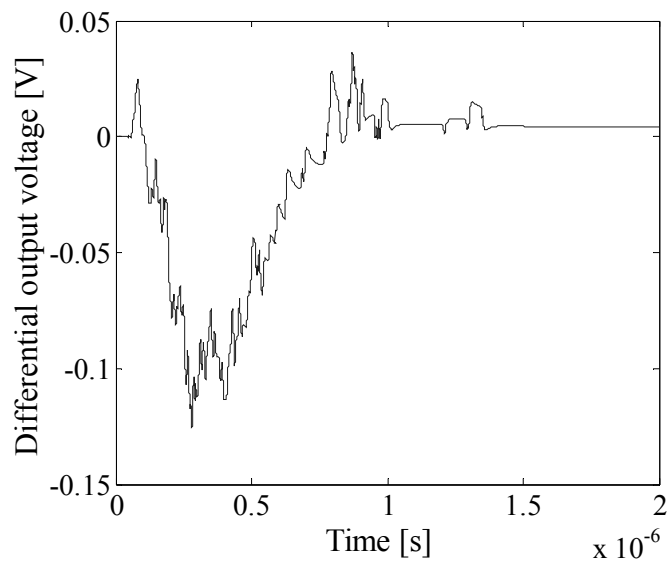
(b)

**Figure 5.1 Eye diagram of (a) the front-end differential output; and (b) the retimed data output in response to 1 Gb/s  $2^{10}-1$  PRBS data.**

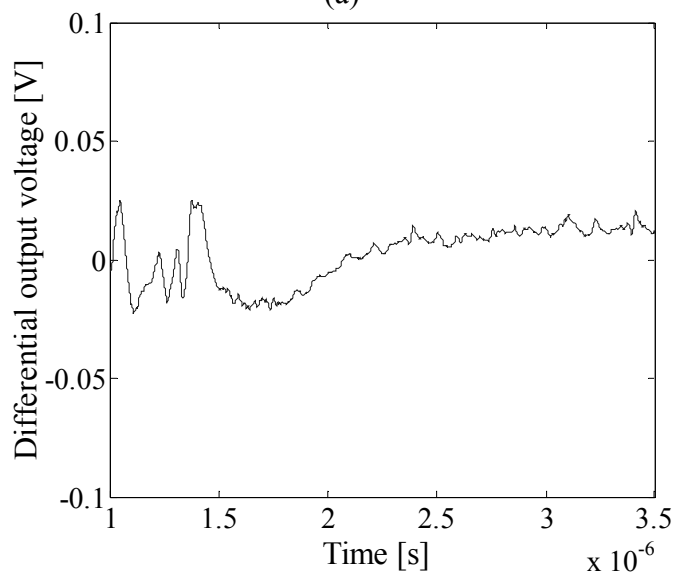
Assuming a noiseless environment, Figure 5.1(a) shows the simulated eye diagram at the front-end output in response to a  $2^{10}-1$  PRBS NRZ data sequence represented by an input

current of 100 nA peak-to-peak. As shown, the inverse scaling and inductive peaking produce a complete open eye, however, at the cost of high power consumption. The retimed data eye diagram is illustrated in Figure 5.1(b). Using the output shown in Figure 5.1(b), the BER of the system was calculated. With a  $2^{10}-1$  1 Gb/s pseudorandom bit pattern, the BER is better than  $10^{-12}$ .

The implementation of the auto-biasing circuit in the front-end mandates a sufficient low corner frequency to ensure stability which unavoidably prolongs the settling time of the whole system. Equation 4.47 denotes that the FLL is capable of locking at the data rate of within approximately 115 ns. Unfortunately, the correct frequency capture can only occur after the input data signal has been properly biased.



(a)

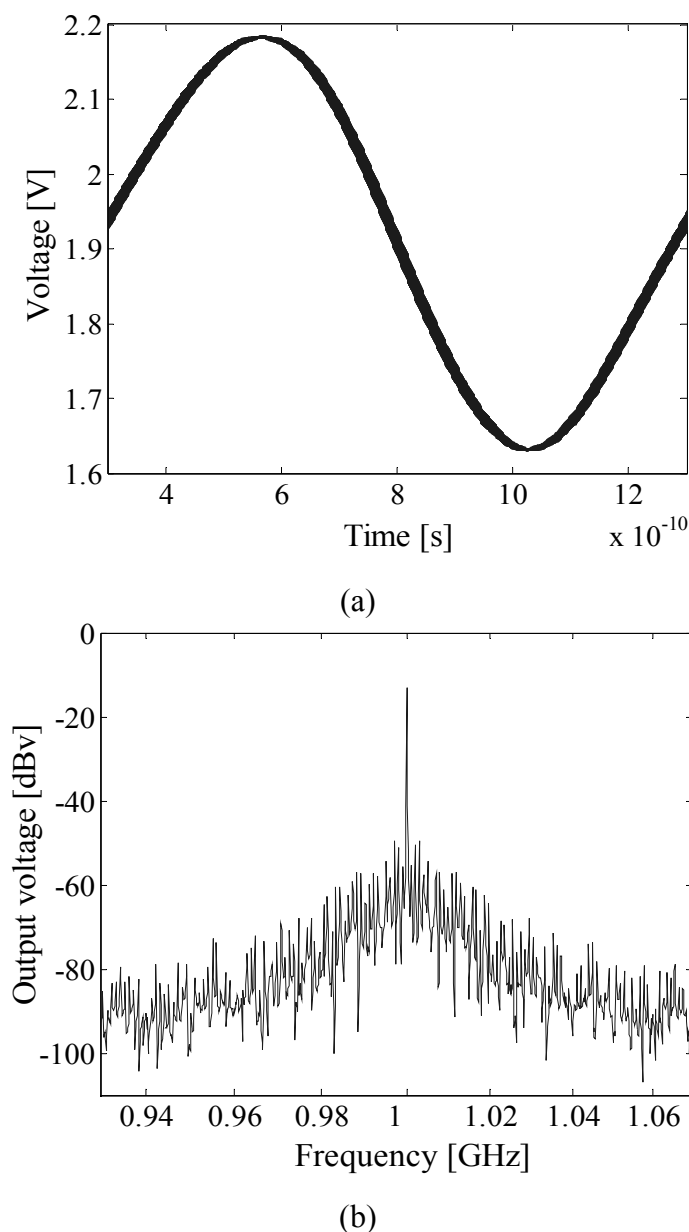


(b)

**Figure 5.2** Lock transients of the (a) frequency-locked loop; and (b) phase-locked loop.

As shown in Figure 5.2(a), upon receiving a 1 Gb/s PRBS sequence of length  $2^{10}-1$  the adequate front-end signal biasing together with frequency capture is only achieved after about 1.4  $\mu\text{s}$ . Once the frequency is captured, the PLL loop requires a transition of approximately 1  $\mu\text{s}$  before it locks. The voltage ripple of the PLL control line is approximately 10 mV.

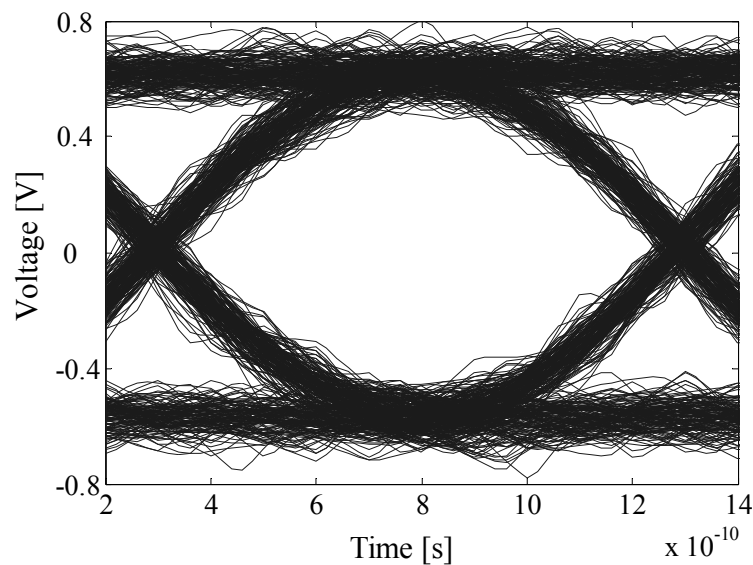
Figures 5.3(a) and 5.3(b) depict the recovered clock signal in both the time and frequency domains in response to a 1 Gb/s random data sequence of length  $2^{10}-1$ . The phase noise at a 1 MHz offset is approximately equal to -98.8 dBc/Hz as shown in Figure 5.3(b). With a random sequence of length  $2^{10}-1$ , the rms jitter is 1.02 ps.



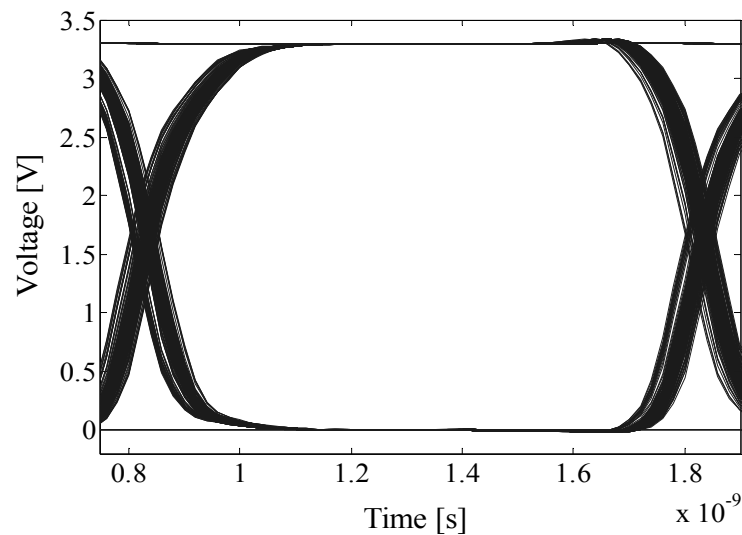
**Figure 5.3 (a) Recovered clock signal in time domain; and (b) recovered clock spectrum.**



The following figures demonstrate an example of the expected output when a certain amount of noise is injected into the system. White Gaussian noise with a signal-to-noise ratio of 18 dB was generated with a “wgn” command in MATLAB. The sample noise was then superimposed onto the inputs of the front-end. As shown in the figures, the 1 Gb/s eye opening at the output of the front-end is still well defined in the presence of a noise source with a SNR of 18 dB.



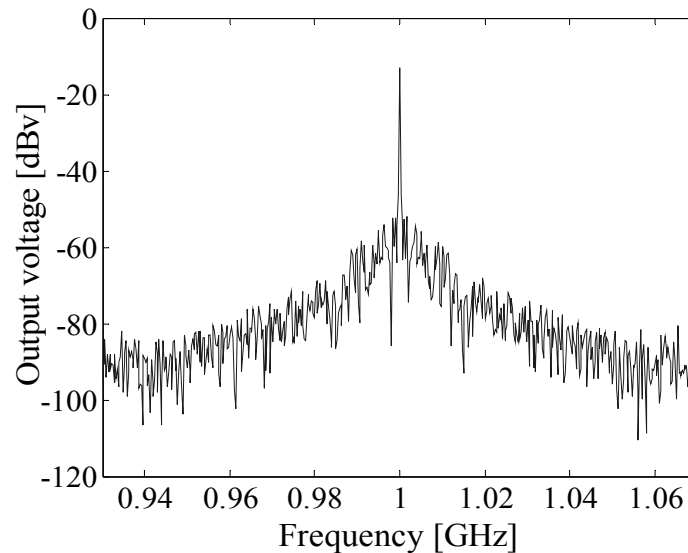
(a)



(b)

**Figure 5.4 Eye diagram of (a) the front-end differential output; and (b) the retimed data output in the presence of noise sources in the system.**

Figure 5.5 depicts the phase noise for a random data sequence of length  $2^{10}-1$ . The phase noise is approximately equal to -94.8 dBc/Hz at a 1 MHz offset, and the resulting closed-loop jitter is 1.62 ps rms.

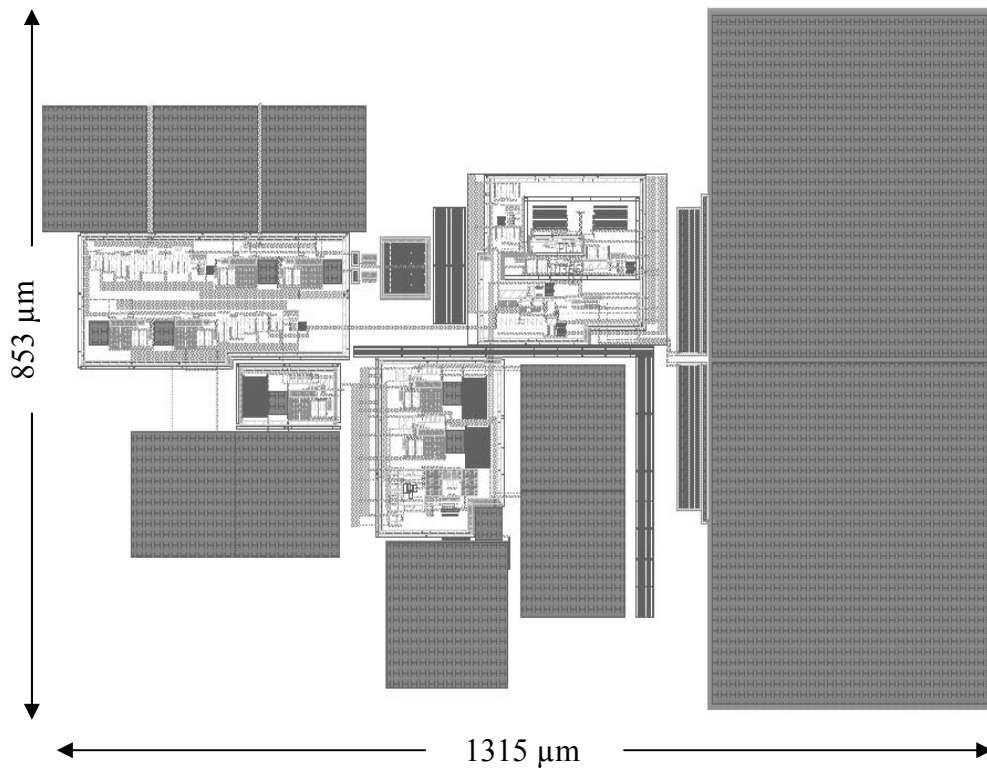


**Figure 5.5 Recovered clock spectrum in the presence of noise sources in the system.**

As shown, noise significantly degrades the eye opening of the front-end output and the jitter performance of the system. As can be expected, the system BER performance and operating frequency will be limited by the amount of noise present. The total power consumed by the circuit is 155 mW from a 3.3 V supply. The front-end, the VCO, the PLL and the frequency detector circuits consume 106 mW, 7.43 mW, 25.6 mW and 5.13 mW respectively. Unfortunately, due to the low photo-generated input current, long-chain voltage amplifiers with large tail currents are necessary to amplify the input signals to adequate amplitudes and results in high power consumption in the front-end circuit.

### 5.3 LAYOUT

The complete system was realised in a four-metal double-poly 0.35  $\mu\text{m}$  CMOS process with a supply voltage of 3.3 V. In order to suppress noise and interference, loop filters are integrated monolithically. Loop filter capacitors for both the PLL and FLL are integrated on chip using linear double-poly capacitors. Resistors are implemented using poly-silicon resistors. As discussed in the previous chapters, poly-silicon is least process conditions dependent and is not voltage dependent. The front-end circuit and the CDR system are separated by a substrate contacts to prevent interference. Figure 5.6 shows the layout of the complete system. The core area is 1.12  $\text{mm}^2$ .



**Figure 5.6** Layout of the optical receiver.

## CHAPTER 6

### CONCLUSION

#### 6.1 PHOTODETECTOR

A low cost, monolithic photodetector is feasible. With spatially modulated light methodology, the photodetector with the *pn*-junction formed by the  $n^+$  active implantation and the  $p$ - substrate realised in a standard  $0.35\ \mu\text{m}$  CMOS process can be used in optical communication operating up to a data rate of 4.25 Gb/s in the nonreturn-to-zero mode. Despite the high speed response obtainable, the detector responsivity is traded off. At the wavelength of 860 nm, the detector responsivity is relatively low (0.038A/W) for a 59% active area detector. Nonetheless, this non-optimal responsivity is partially compensated by the inherent low detector capacitance that greatly profits high speed fibre optical systems.

#### 6.2 FRONT-END

Research has been done on devising high speed, high gain transimpedance amplifiers. However, not much has been done to minimise the equivalent input noise current. At the front-end of a high speed operating system, a design challenge arises in achieving high speed, moderate transimpedance gain, low equivalent input noise current simultaneously. In order to achieve the sensitivity specification stipulated for gigabit fibre channel systems, the bandwidth of the transimpedance amplifier is compromised. The preamplifier exhibits a sensitivity better than -17 dBm at a bit-error-rate of  $10^{-12}$ .

The high bandwidth and further amplification is achieved by the limiting amplifier based on the inverse scaling topology. The amplifier operates from a single voltage supply and exhibits a bandwidth greater than the minimum requirement. To obtain high operating frequency, the system results in relatively high power dissipation. Nevertheless, in many LAN systems power supply is substantial.

The postamplifier was implemented as part of the DC control to ensure a reasonable performance of the front-end circuit at different process conditions. The low-filter corner frequency required for the stability issue results in a long settling time. Unfortunately, it consequently prolongs the transient time for the CDR circuit. The voltage gain stages, high

speed inverters, are modified from the push-pull amplifier. To achieve reasonable gain and output bias, the inequality  $\sqrt{K'_p(W/L)_p} / \sqrt{K'_n(W/L)_n} \geq 1$  must be satisfied. Typically, the mobility of PMOS transistors is much slower than that of the NMOS transistors. To satisfy the above-mentioned condition, strong PMOS transistors and weak NMOS devices are required. As a result, the effect of strong PMOS transistors becomes prominent and degrades the frequency response significantly in the worst-zero case simulation.

### 6.3 CLOCK AND DATA RECOVERY CIRCUIT

To achieve high speed and low power consumption, a two-stage differential ring oscillator was implemented. The phase shift requirement is established by introducing additional delays in each stage. Under process, voltage and temperature variations, the oscillation is sustained by the wide tuning range of the oscillator.

The ability of maintaining the output hold level at the sample-and-hold phase detector makes the system tolerant to the consecutive data bits and allows the control voltage for the VCO to be kept relatively constant. Nevertheless, phase comparison is an amplitude sensitive process. Any fluctuation in the input signals may cause a slight shift of the paradigm of phase comparison. As it is difficult to maintain constant VCO voltage swings, VCO frequency fluctuation due to noise in the loop or phase locking instantaneously leads to VCO amplitude fluctuation. As a result, a small ripple persists on the control line in phase lock.

The frequency detector exhibits reliable frequency acquisition if the frequency difference is within  $\pm 32\%$  of the data rate. During frequency acquisition, false locking onto harmonics or subharmonics is suppressed by the low-gain charge pump and low pulse density at the output of the detector. If the initial VCO frequency is close to a harmonic or subharmonic frequency, false locking may still occur. However, with the initial control voltages set at  $V_{DD}/2$ , as estimated in Figure 4.8, the occurrence is unlikely under process variations. Once the clock frequency is brought to the vicinity of the data rate, the outputs of the frequency detector stays unasserted. Consequently, a steady control voltage can be maintained to suppress the jitter being added to the VCO output.

The complete system is integrated in a standard 0.35  $\mu\text{m}$  CMOS process without any process modifications. Frequency synchronisation, phase locking and data regeneration is performed within the CDR circuit. As shown in Chapter 5, the eye opening of the retimed data in response to a 1 Gb/s random data sequence of length  $2^{10}-1$  is sufficiently wide and a reasonable jitter performance at 1 GHz may be achieved.

## 6.4 FUTURE WORK

Integrating silicon photodetectors in a standard CMOS process is a feasible solution for a high-speed optical communication network. In order to operate in a high-speed environment, however, the responsivity of the detector is inevitably traded off. As a result, the front-end, viz. the transimpedance amplifier and the limiting amplifier, requires a comparatively high conversion gain to amplify the small input current to a reasonable voltage swing. An overall gain of approximately 95 dB $\Omega$  has often been implemented in a standard 0.35  $\mu\text{m}$  CMOS process for systems operating between 1 Gb/s and 2.5 Gb/s. Realising a system with a gain of approximately 132 dB $\Omega$ , while achieving a high bandwidth, demands a long chain implementation which undesirably increases the group delay and degrades the phase response. With a 0.35  $\mu\text{m}$  CMOS process, the realisation of high-speed operating systems with an extremely high gain becomes impeded. Given this difficulty, a lower CMOS process technology could be implemented to ease the bandwidth while achieving a large conversion gain. Another solution is the implementation of active feedback together with inductive peaking and negative Miller capacitance techniques [44]. However, each stage requires four inductors in the range of 10 nH for gigabit bandwidth in a 0.35  $\mu\text{m}$  CMOS process that will result in enormous area overhead. Furthermore, the magnetic crosstalk among coils may severely influence and degrade the CDR performance [45].

The noise performance of the ring oscillator is relatively poor. However, it is still capable of meeting the gigabit fibre channel specification. In a system where lower noise is mandatory, the LC oscillator has to be used at the cost of a large area and narrow tuning range. The ability of LC oscillators to more accurately predict the resonance frequency could suppress frequency fluctuations and ease the phase comparison. Furthermore, differential current steering logic [46] could also be implemented instead of voltage switching flip-flops to suppress the common-mode noise.

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## APPENDIX A: DERIVATION FOR THE MINORITY CARRIER CONCENTRATION

The continuity equation for electrons in a  $p$ -type region of an illuminated detector has the form [4]

$$\frac{\partial n_p}{\partial t} = D_n \frac{\partial^2 n_p}{\partial x^2} + D_n \frac{\partial^2 n_p}{\partial y^2} - \frac{n_p - n_0}{\tau_n} + g(t, y) e^{-\alpha x} \quad (\text{A.1})$$

with:

$x$  – depth of the material

$y$  – width of the material

$t$  – time

$n_p$  – concentration of electrons

$n_0$  – initial concentration of electrons

$D_n$  – Diffusion constant of electrons

$\tau_n$  – minority carrier lifetime

$\alpha$  – absorption coefficient

$g(t, y)$  – electron generation rate

The boundary conditions are

$$n_p(0, y, t) = n_0, \text{ for } -b < y < b \text{ and } t > 0$$

$$n_p(a, y, t) = 0, \text{ for } -b < y < b \text{ and } t > 0$$

$$n_p(x, -b, t) = 0, \text{ for } 0 < x < a \text{ and } t > 0$$

$$n_p(x, b, t) = 0, \text{ for } 0 < x < a \text{ and } t > 0$$

$$n_p(x, y, 0) = n_0, \text{ for } 0 < x < a \text{ and } -b < y < b$$

where  $a$  and  $2b$  denote the depth and the length of a single detector finger.

In order to solve the nonhomogeneous formula of equation A.1, Modification is applied by letting [47]

$$n_p(x, y, t) = v(x, y, t) + \psi(x, y)$$

to change the dependent variable.

Then,

$$\frac{\partial^2 n_p}{\partial x^2} = \frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 \psi}{\partial x^2}, \frac{\partial^2 n_p}{\partial y^2} = \frac{\partial^2 v}{\partial y^2} + \frac{\partial^2 \psi}{\partial y^2} \text{ and } \frac{\partial n_p}{\partial t} = \frac{\partial v}{\partial t} \quad (\text{A.2})$$

Substituting these conditions into equation A.1 results in

$$\frac{\partial v}{\partial t} = D_n \left( \frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 \psi}{\partial x^2} \right) + D_n \left( \frac{\partial^2 v}{\partial y^2} + \frac{\partial^2 \psi}{\partial y^2} \right) - \frac{1}{\tau_n} (v(x, y, t) + \psi(x, y)) + \frac{n_0}{\tau_n} + g(t, y) e^{-\alpha x} \quad (\text{A.3})$$

A homogeneous equation can be obtained if the following condition is applied

$$D_n \left( \frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} \right) - \frac{1}{\tau_n} \psi(x, y) + \frac{n_0}{\tau_n} + g(t, y) e^{-\alpha x} = 0 \quad (\text{A.4})$$

Again applying a change of dependent variable by letting

$$\psi(x, y) = s(x, y) + \zeta(x) \quad (\text{A.5})$$

By substitution, equation A.4 becomes

$$\frac{\partial^2 s}{\partial x^2} + \frac{\partial^2 s}{\partial y^2} + \zeta'' - \frac{1}{D_n \tau_n} (s(x, y) + \zeta) + \frac{n_0}{D_n \tau_n} + \frac{1}{D_n} g(t, y) e^{-\alpha x} = 0 \quad (\text{A.6})$$

Equation A.6 becomes homogeneous when

$$\zeta'' - \frac{1}{D_n \tau_n} \zeta + \frac{n_0}{D_n \tau_n} + \frac{1}{D_n} g(t, y) e^{-\alpha x} = 0 \quad (\text{A.7})$$

The complementary function of equation A.7 is

$$\zeta_c(x) = A \exp\left(\frac{1}{\sqrt{D_n \tau_n}} x\right) + B \exp\left(-\frac{1}{\sqrt{D_n \tau_n}} x\right)$$

Set the particular solution to

$$\zeta_p(x) = C \exp(-\alpha x) + D$$

with

$$\zeta_p' = -\alpha C \exp(-\alpha x) \text{ and } \zeta_p'' = \alpha^2 C \exp(-\alpha x)$$

Substitution yields

$$\alpha^2 C \exp(-\alpha x) - \frac{1}{D_n \tau_n} (C \exp(-\alpha x) + D) = \frac{-n_0}{D_n \tau_n} - \frac{1}{D_n} g(t, y) e^{-\alpha x}$$

Equating the coefficients of like terms, it yields the particular solution

$$\zeta_p(x) = n_0 - g(t, y) \exp(-\alpha x) / (\alpha^2 D_n - (1/\tau_n))$$

and the general solution

$$\zeta(x) = A \exp\left(\frac{1}{\sqrt{D_n \tau_n}} x\right) + B \exp\left(-\frac{1}{\sqrt{D_n \tau_n}} x\right) + n_0 - \frac{g(t, y) e^{-\alpha x}}{\alpha^2 D_n - 1/\tau_n} \quad (\text{A.8})$$

The initial conditions are

$$n_p(0, y, t) = v(0, y, t) + \psi(0, y) = n_0$$

$$n_p(a, y, t) = v(a, y, t) + \psi(a, y) = 0$$

$$n_p(x, -b, t) = v(x, -b, t) + \psi(x, -b) = 0$$

$$n_p(x, b, t) = v(x, b, t) + \psi(x, b) = 0$$

Provided

$$\psi(0, y) = n_0 \text{ and } \psi(a, y) = \psi(x, -b) = \psi(x, b) = 0$$

Then,

$$v(0,y,t) = v(a,y,t) = v(x,-b,t) = v(x,b,t) = 0$$

Furthermore, letting  $s(0,y) = s(a,y) = 0$ , then

$$\zeta(0) = n_0 \text{ and } \zeta(a) = v$$

Applying the initial conditions of  $\zeta$  to equation A.8, it yields

$$\zeta(x) = n_0 \left( 1 - \frac{\sinh\left(\frac{x}{\sqrt{D_n \tau_n}}\right)}{\sinh\left(\frac{a}{\sqrt{D_n \tau_n}}\right)} \right) + \frac{g(t,y)}{\alpha^2 D_n - 1/\tau_n} \left\{ \frac{\sinh\left(\frac{x}{\sqrt{D_n \tau_n}}\right)}{\sinh\left(\frac{a}{\sqrt{D_n \tau_n}}\right)} \cdot \left( \exp(-\alpha a) - \exp\left(\frac{a}{\sqrt{D_n \tau_n}}\right) \right) + \left( \exp\left(\frac{x}{\sqrt{D_n \tau_n}}\right) - \exp(-\alpha x) \right) \right\}$$

The initial conditions  $\psi(x,-b) = s(x,-b) + \zeta(x)$  and  $\psi(x,b) = s(x,b) + \zeta(x)$  imply  $s(x,-b) = s(x,b) = -\zeta(x)$ . It is then required to solve  $s(x,y)$  with the adopted boundary conditions, the boundary-value problem is described by

$$\begin{aligned} \frac{\partial^2 s}{\partial x^2} + \frac{\partial^2 s}{\partial y^2} - \frac{1}{D_n \tau_n} s(x,y) &= 0, \quad 0 < x < a, \quad -b < y < b \\ s(0,y) = s(a,y) &= 0, \quad -b < y < b \\ s(x,-b) = s(x,b) &= -\zeta(x) \quad 0 < x < a \end{aligned} \quad (\text{A.9})$$

This Dirichlet problem consists of two nonhomogeneous initial conditions and is not directly susceptible to the method of separation of variables. The boundary-value problem in (A.9) is split into two problems each with a nonhomogeneous boundary condition. The sum of the solutions  $s_1$  and  $s_2$  is the solution of the original problem.

Substitution of  $s(x,y) = XY$ , then the separation of variables leads to

$$\frac{X''}{X} = -\frac{Y''}{Y} + \frac{1}{D_n \tau_n} = -\lambda \quad (\text{A.10})$$

where  $\lambda$  is a constant.

The boundary conditions of both the single nonhomogeneous boundary-value problems have  $X(0) = X(a) = 0$ . Then the eigenvalue and the associated eigenfunction for  $X'' + \lambda X = 0$  for both solutions are

$$\lambda_n = n^2 \pi^2 / a^2, \quad X_n = \sin(n\pi/a) \quad \text{for } n = 1, 2, 3, \dots$$

Equation A.10 gives a second eigenvalue problem

$$Y'' - \left( \frac{1}{D_n \tau_n} + \lambda \right) Y = 0$$

The general solution to the above differential equation is

$$Y_n(y) = A_n \cosh\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}} y\right) + B_n \sinh\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}} y\right) \quad (\text{A.11})$$

Let the first single nonhomogeneous boundary-value problem have a nonhomogeneous boundary condition at  $s(x, -b) = -\zeta(x)$ , then  $s(x, b) = 0$ . Applying the initial condition  $s(x, b) = 0$  to equation A.11, then

$$Y_n(y) = c_n \sinh\left(\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}}\right)(b - y)\right)$$

where  $c_n = A_n / \sinh\left(\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}}\right)b\right)$ .

The power series solution is therefore of the form

$$s_1(x, y) = \sum_{n=1}^{\infty} c_n \sin \frac{n\pi}{a} x \sinh\left(\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}}\right)(b - y)\right)$$

The coefficients  $\{c_n\}$  is calculated by setting  $y = -b$ ,

$$s_1(x, -b) = \sum_{n=1}^{\infty} c_n \sin \frac{n\pi}{a} x \sinh\left(\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}}\right)(b - (-b))\right) = -\zeta(x)$$

Thus,

$$c_n = \frac{2}{a \cdot \sinh\left(\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}}\right)(2b)\right)} \int_0^a -\zeta(x) \sin \frac{n\pi}{a} x \cdot dx$$

Similarly, the solution to the second single nonhomogeneous boundary-value problem with the boundary conditions  $s(x, b) = -\zeta(x)$  and  $s(x, -b) = 0$  is

$$s_2(x, y) = \sum_{n=1}^{\infty} c_n \sin \frac{n\pi}{a} x \sinh\left(\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}}\right)(-b - y)\right)$$

with

$$c_n = \frac{2}{a \cdot \sinh\left(\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}}\right)(-2b)\right)} \int_0^a -\zeta(x) \sin \frac{n\pi}{a} x \cdot dx$$

Therefore the final solution to the function  $s$  is  $s(x, y) = s_1(x, y) + s_2(x, y)$ , which is simplified to



$$s(x, y) = \sum_{n=1}^{\infty} \frac{2}{a} \frac{\cosh\left(\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}}\right) y\right) \sin\left(\frac{n\pi}{a} x\right)}{\cosh\left(\left(\sqrt{\frac{1}{D_n \tau_n} + \frac{n^2 \pi^2}{a^2}}\right) b\right)} \cdot \int_0^a -\zeta(x) \sin \frac{n\pi}{a} x \cdot dx.$$

The solution for  $\psi(x,y)$  is obtained by adding  $s(x,y)$  to  $\zeta(x)$ , i.e.  $\psi(x,y) = s(x,y) + \zeta(x)$ .

The final step is to solve the new boundary-value problem described by

$$\frac{\partial v}{\partial t} = D_n \frac{\partial^2 v}{\partial x^2} + D_n \frac{\partial^2 v}{\partial y^2} - \frac{v}{\tau_n} \quad (\text{A.12})$$

$$v(0, y, t) = 0, \text{ for } -b < y < b \text{ and } t > 0$$

$$v(a, y, t) = 0, \text{ for } -b < y < b \text{ and } t > 0$$

$$v(x, -b, t) = 0, \text{ for } 0 < x < a \text{ and } t > 0$$

$$v(x, b, t) = 0, \text{ for } 0 < x < a \text{ and } t > 0$$

$$v(x, y, 0) = n_0 - \psi(x, y), \text{ for } 0 < x < a \text{ and } -b < y < b$$

Substituting  $v(x,y,t) = XYT$  in equation A.12, the following is obtained

$$\frac{X''}{X} = -\frac{Y''}{Y} + \frac{T'}{D_n T} + \frac{1}{D_n \tau_n}$$

If each term of the above equation is described by a constant, then,

$$X'' + \lambda^2 X = 0$$

$$Y'' + \mu^2 Y = 0, \text{ and}$$

$$T' + ((1/D_n \tau_n) + \lambda^2 + \mu^2) D_n T = 0$$

where  $\lambda$  and  $\mu$  are constants.

With the boundary conditions, the eigenvalues and the associated eigenfunctions for  $X$  and  $Y$  are

$$\lambda = m\pi/a, X = c_1 \sin(m\pi x/a), \quad m = 1.2.3 \dots$$

$$\mu = (2n-1)\pi/b, Y = c_2 \cos((2n-1)\pi y/b), \quad n = 1.2.3 \dots$$

and the general solution for  $T$  has the form  $T = c_3 \exp(-((1/D_n \tau_n) + \lambda^2 + \mu^2) D_n t)$

Applying the superposition principle, the power series solution is

$$v(x, y, t) = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} A_{mn} e^{-((1/D_n \tau_n) + (m\pi/a)^2 + ((2n-1)\pi/b)^2) D_n t} \sin \frac{m\pi}{a} x \cos \frac{(2n-1)\pi}{b} y \quad (\text{A.13})$$

Equating equation A.13 to  $n_0 - \psi(x,y)$  at  $t = 0$ , the coefficients  $\{A_{mn}\}$  is

$$A_{mn} = \frac{2}{ab} \int_{-b}^b \int_0^a (n_0 - \psi(x, y)) \sin\left(\frac{m\pi}{a} x\right) \cos\left(\frac{(2n-1)\pi}{b} y\right) dx dy$$

Finally, the solution of the original problem is

$$n_p(x, y, t) = n_{p,ILLU}(x, y, t) = \psi(x, y) + v(x, y, t)$$

$$= s(x,y) + \zeta(x,y) + v(x,y,t) \quad (\text{A.14})$$

where  $\psi(x,y) = s(x,y) + \zeta(x)$  is the steady-state solution and  $v(x,y,t)$  is the transient solution.

In order to determine the minority carrier distribution after the illumination was cut off, the continuity equation for the minority carriers in a p-type region is rewritten in the form

$$\frac{\partial n_p}{\partial t} = D_n \frac{\partial^2 n_p}{\partial x^2} + D_n \frac{\partial^2 n_p}{\partial y^2} - \frac{n_p - n_0}{\tau_n}$$

with the carrier generation rate  $g(t,y)e^{-\alpha x}$  equals to zero.

At the time the illumination was cut off, the initial concentration of the minority carriers at time zero is described by  $n_{p,ILLU}(x,y,t_1)$ , equation A.14, with  $t_1$  denoting the duration of illumination. Thus, the boundary conditions for the boundary value problem are

$$n_p(0,y,t) = n_0, \text{ for } -b < y < b \text{ and } t > 0$$

$$n_p(a,y,t) = 0, \text{ for } -b < y < b \text{ and } t > 0$$

$$n_p(x,-b,t) = 0, \text{ for } 0 < x < a \text{ and } t > 0$$

$$n_p(x,b,t) = 0, \text{ for } 0 < x < a \text{ and } t > 0$$

$$n_p(x,y,0) = n_{p,ILLU}(x,y,t_1), \text{ for } 0 < x < a \text{ and } -b < y < b$$

Applying the same argument as previously described in the first boundary value problem, the new  $\zeta_v(x)$  and  $v(x,y,t)$  are

$$\zeta_v(x) = n_0 - \frac{n_0}{\sinh\left(\frac{1}{\sqrt{D_n \tau_n}} a\right)} \sinh\left(\frac{1}{\sqrt{D_n \tau_n}} x\right), \text{ and}$$

$$v_v(x,y,t) = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} A_{mn} e^{-\left(\frac{1}{D_n \tau_n} + (m\pi/a)^2 + ((2n-1)\pi/b)^2\right) D_n t} \sin \frac{m\pi}{a} x \cos \frac{(2n-1)\pi}{b} y$$

with

$$A_{mn} = \frac{2}{ab} \int_{-b}^b \int_0^a (n_{p,ILLU}(x,y,t_1) - s_v(x,y) - \zeta_v(x)) \sin\left(\frac{m\pi}{a} x\right) \cos\left(\frac{(2n-1)\pi}{b} y\right) dx dy$$

Then, the minority carrier concentration profile after the illumination was cut off is

$$\begin{aligned} n_p(x,y,t) &= \psi_v(x,y) + v_v(x,y,t) \\ &= s_v(x,y) + \zeta_v(x) + v_v(x,y,t) \end{aligned}$$

## APPENDIX B: FREQUENCY DETECTOR LOGIC

The logic cell design of the frequency detector is described in this section. Only the inverting logics were implemented, since it require less digital cells and occupy less circuit area.

From table 4.1, the minimum sum of products for the UP and DOWN signals were derived as follows

$$\begin{aligned}
 \text{UP} &= A'C(B'D' + B'D + BD') \\
 &= A'CB'D' \\
 &= (A + C')(BD)' \\
 &= [(A + C') + (BD)']' \\
 &= [(A'C)' + (B'+D')]'
 \end{aligned}$$

And,

$$\begin{aligned}
 \text{DOWN} &= AC'(B'D' + B'D + BD') \\
 &= AC'B'D' \\
 &= [(AC')' + (B'+D')]'
 \end{aligned}$$

## APPENDIX C: CIRCUIT DIAGRAMS

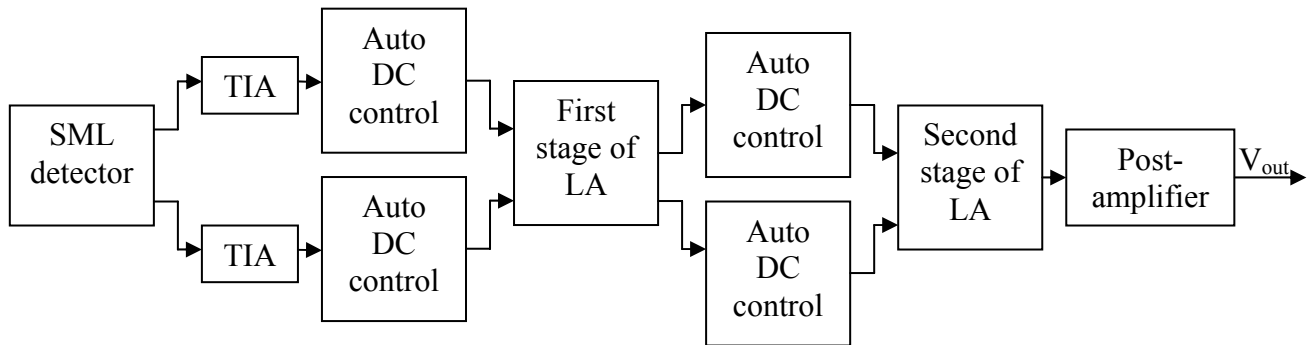


Figure C.1 Front-end overview.

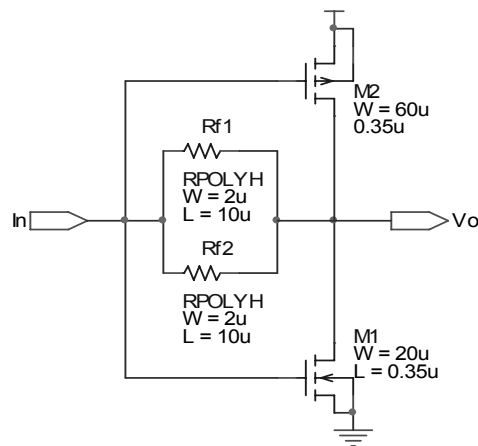


Figure C.2 Transimpedance amplifier.

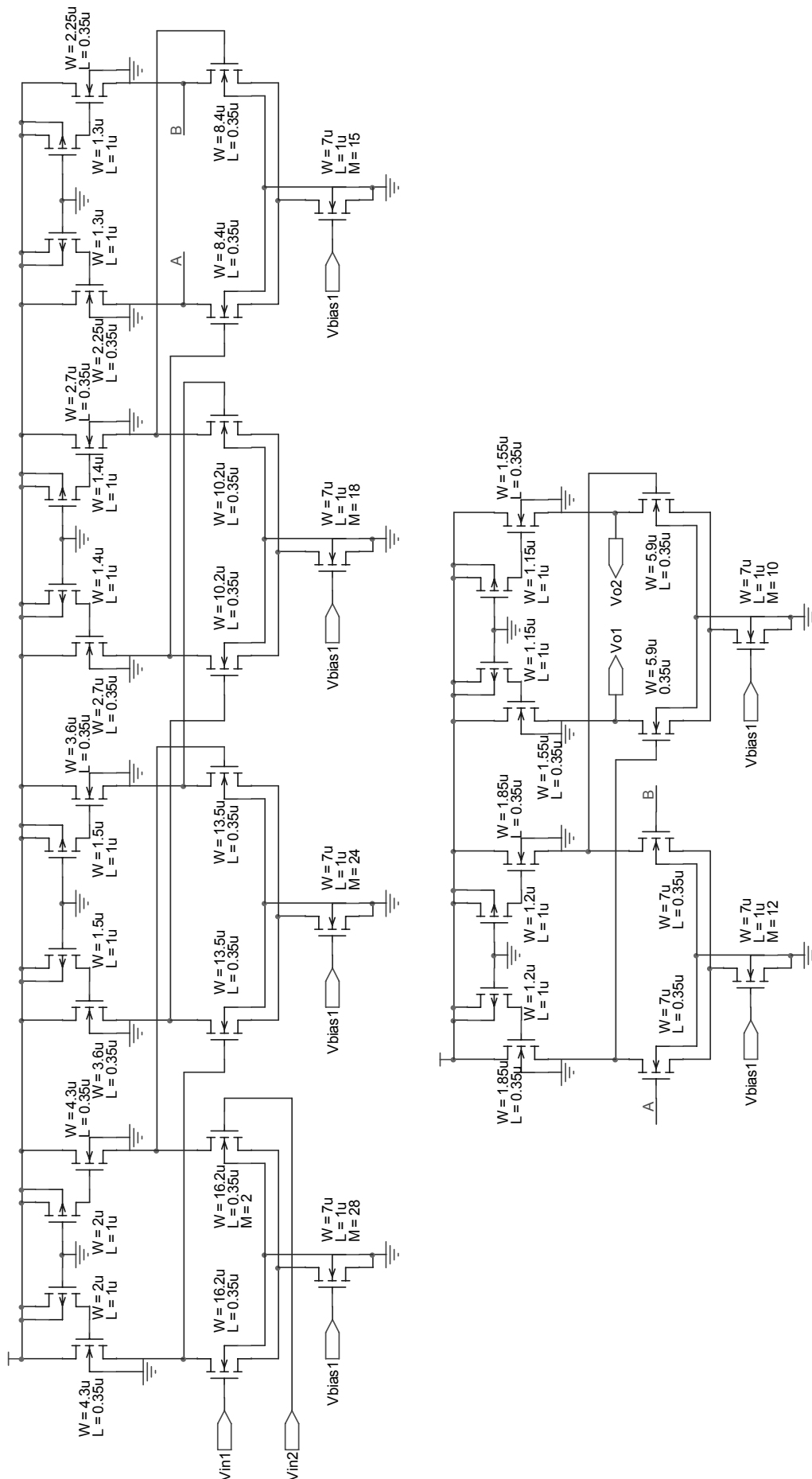


Figure C.3 First stage of the limiting amplifier.

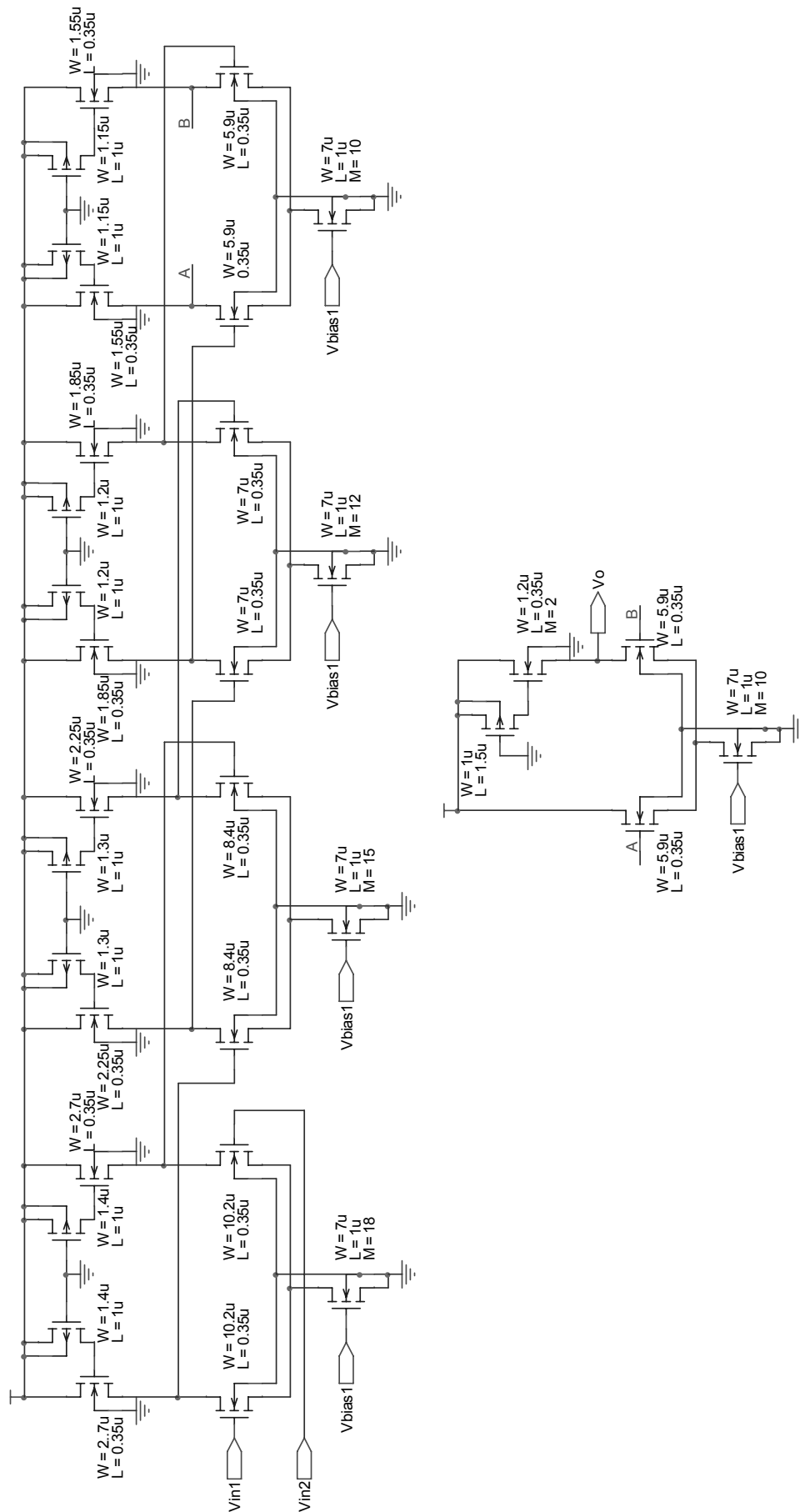


Figure C.4 Second stage of the limiting amplifier.

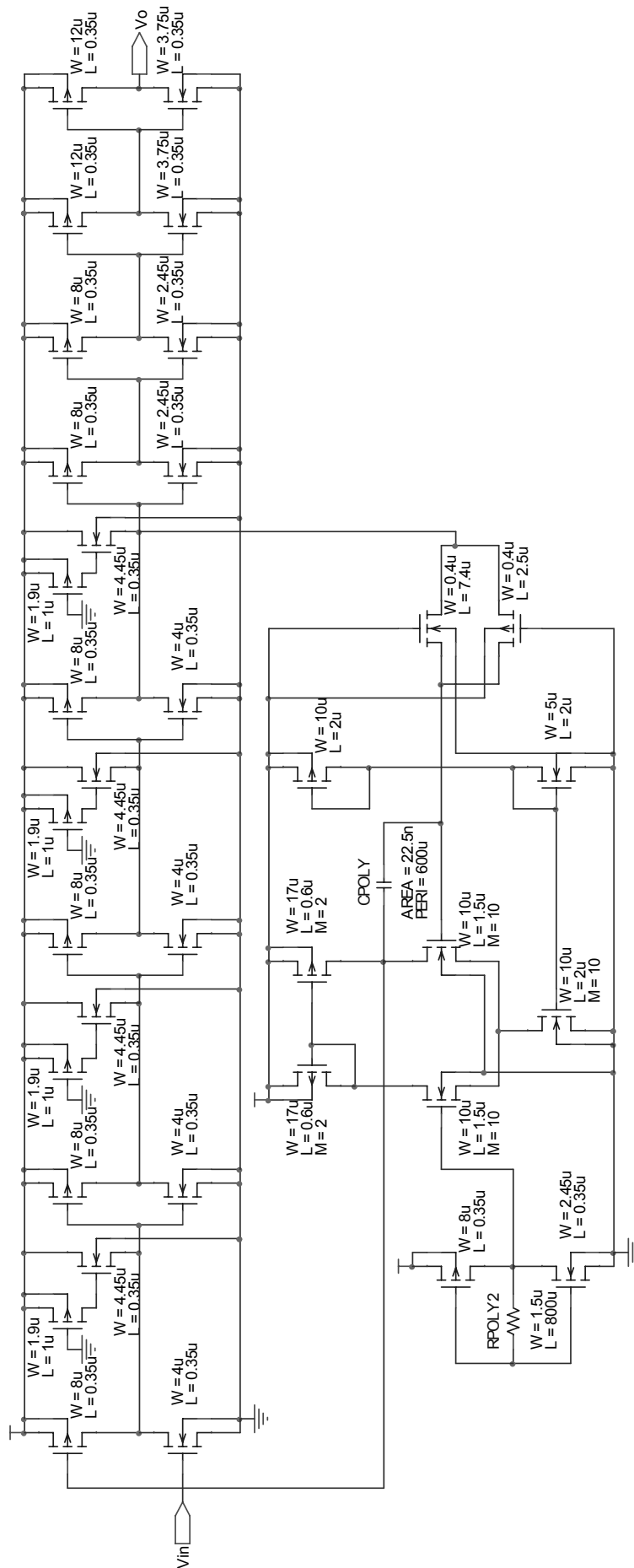


Figure C.5 Postamplifier

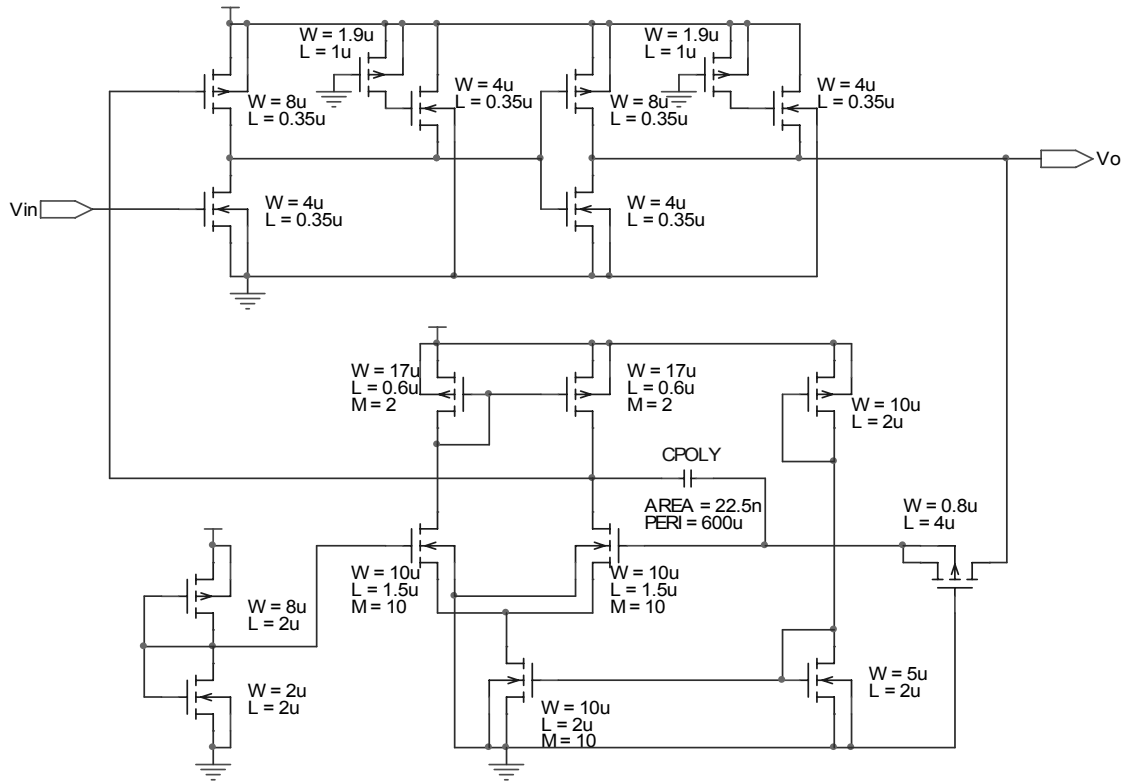


Figure C.6 Auto DC-control.

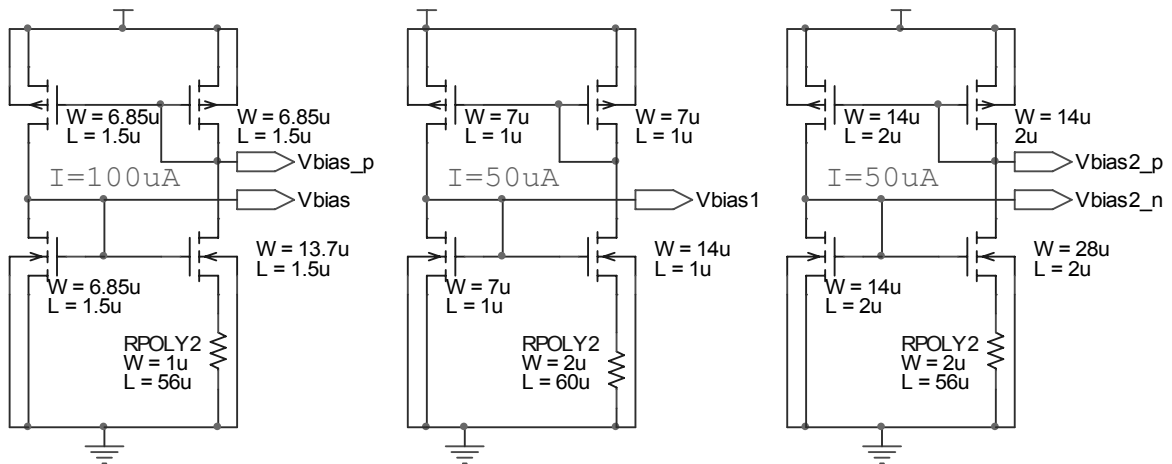


Figure C.7 Current reference circuits.



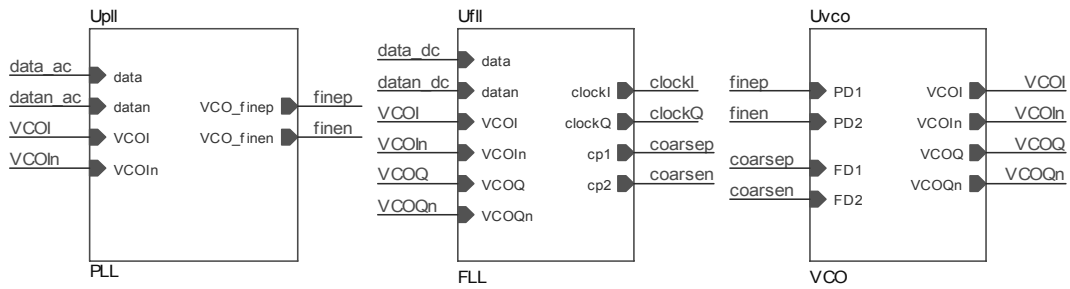


Figure C.8 CDR system.

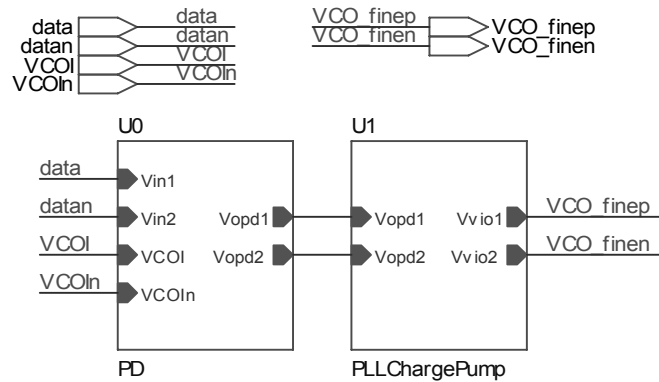


Figure C.9 Phase locked loop.

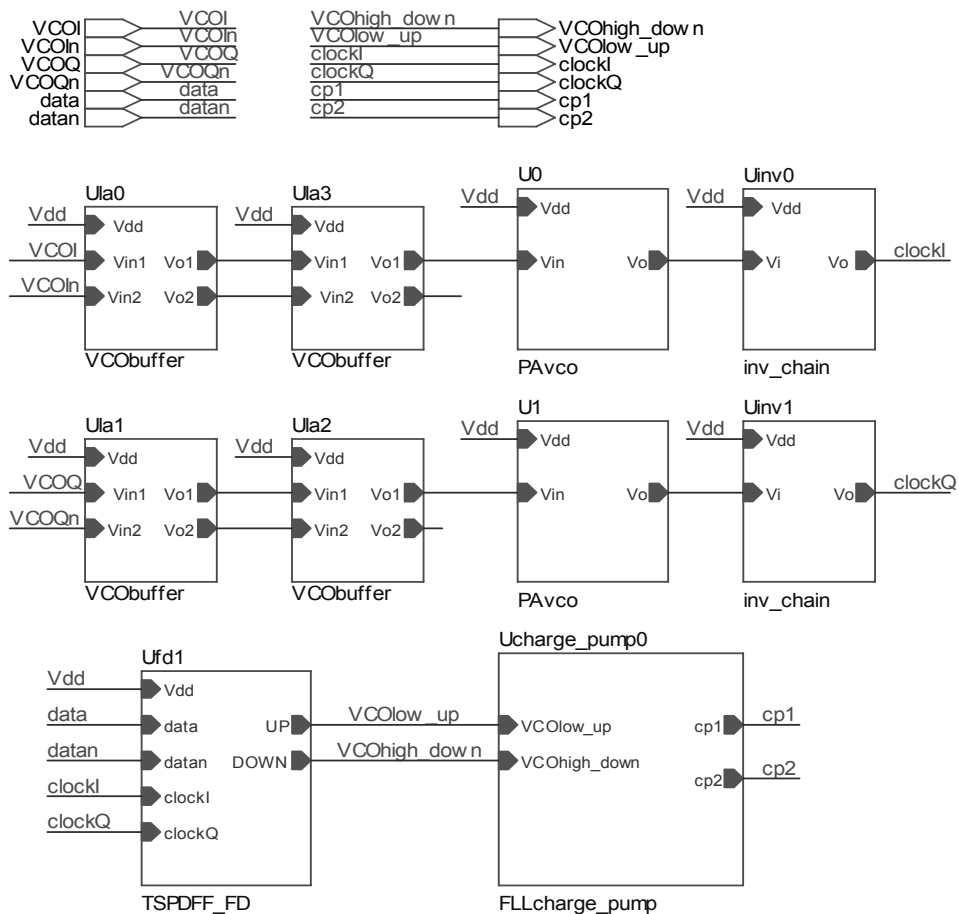


Figure C.10 Frequency locked loop.

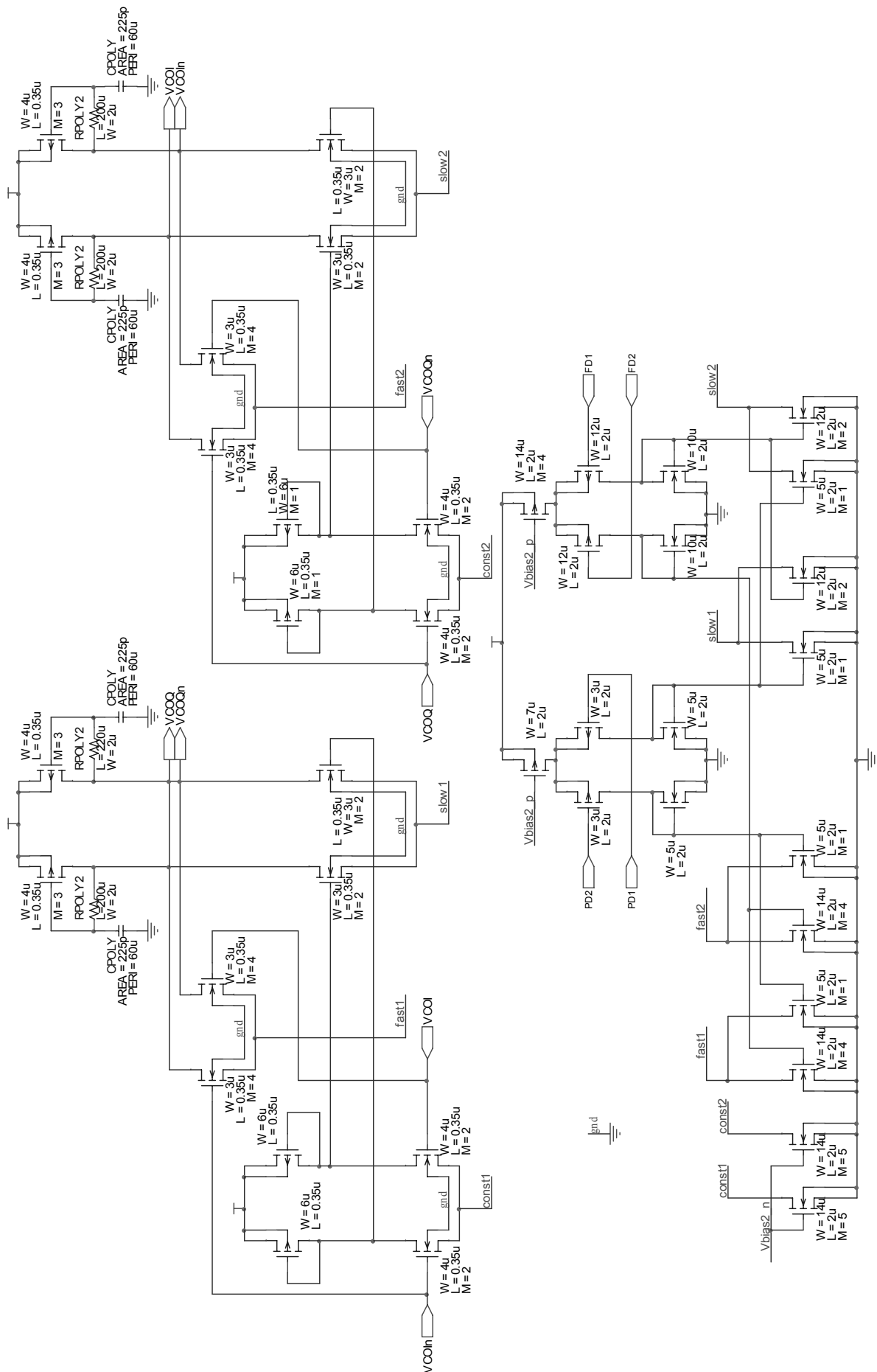


Figure C.11 Voltage controlled oscillator.

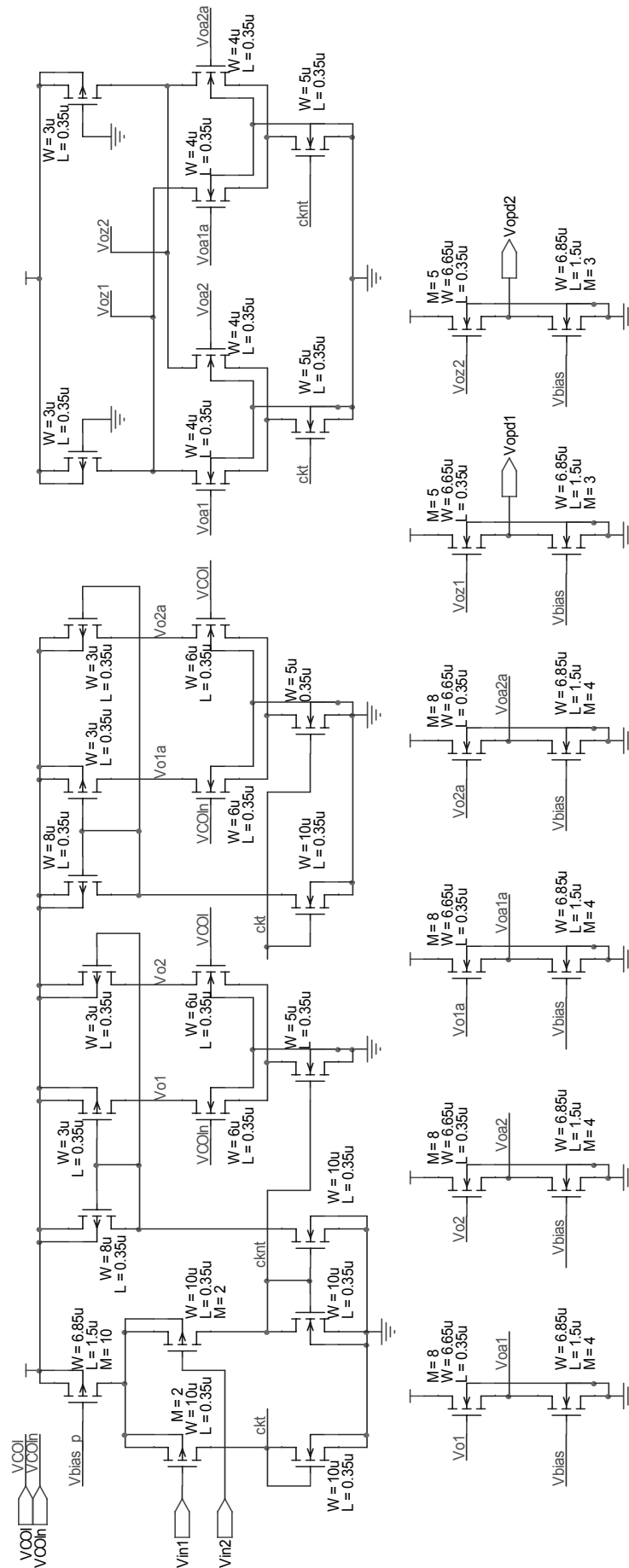


Figure C.12 PLL unit: Phase detector.

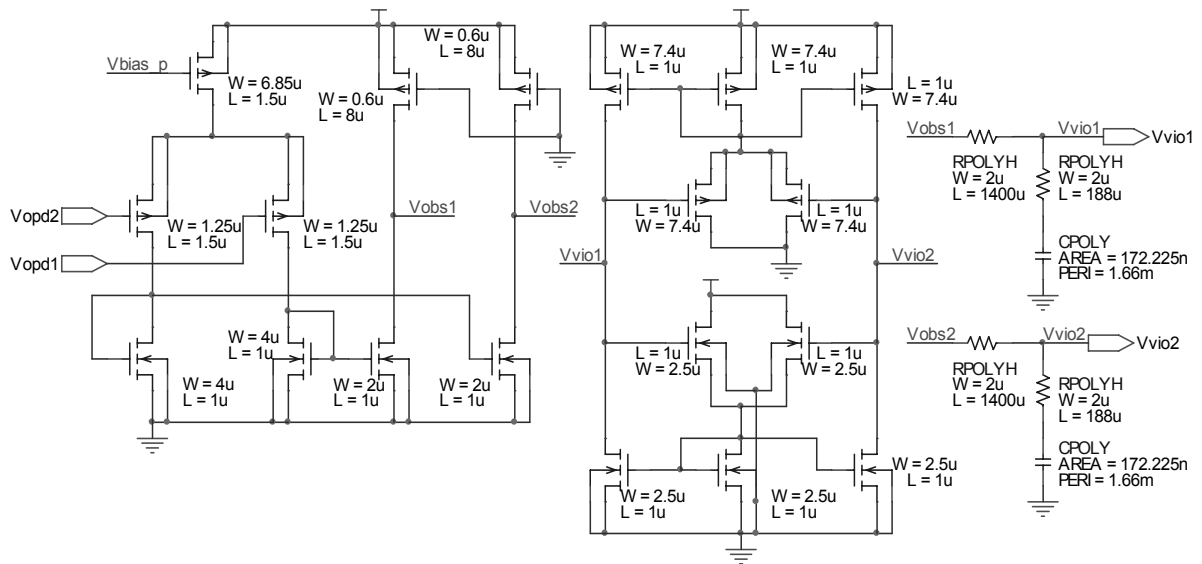


Figure C.13 PLL unit: Charge pump and loop filter.

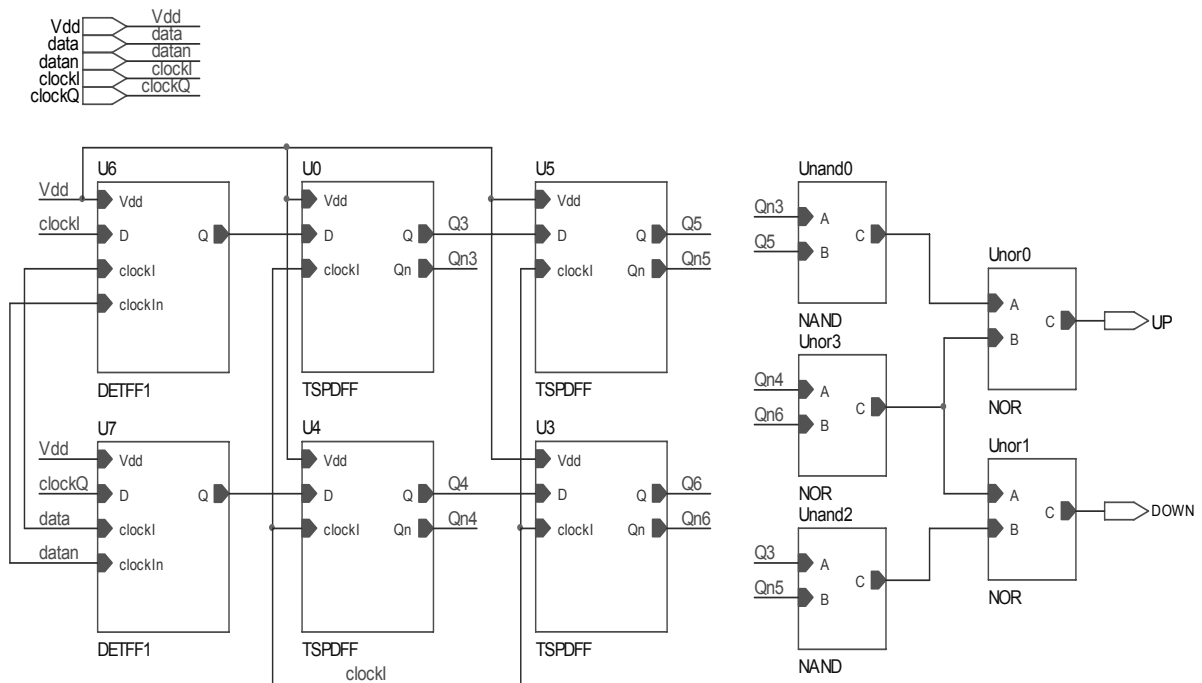


Figure C.14 FLL unit: Frequency detector.

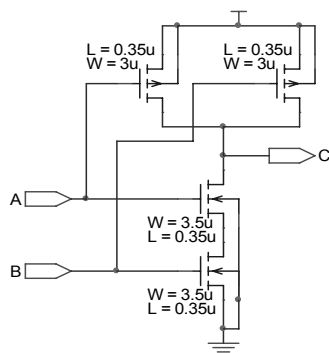


Figure C.15 FLL unit: NAND gate.

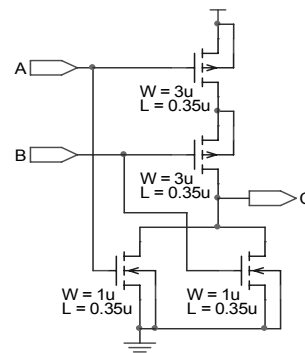


Figure C.16 FLL unit: NOR gate.

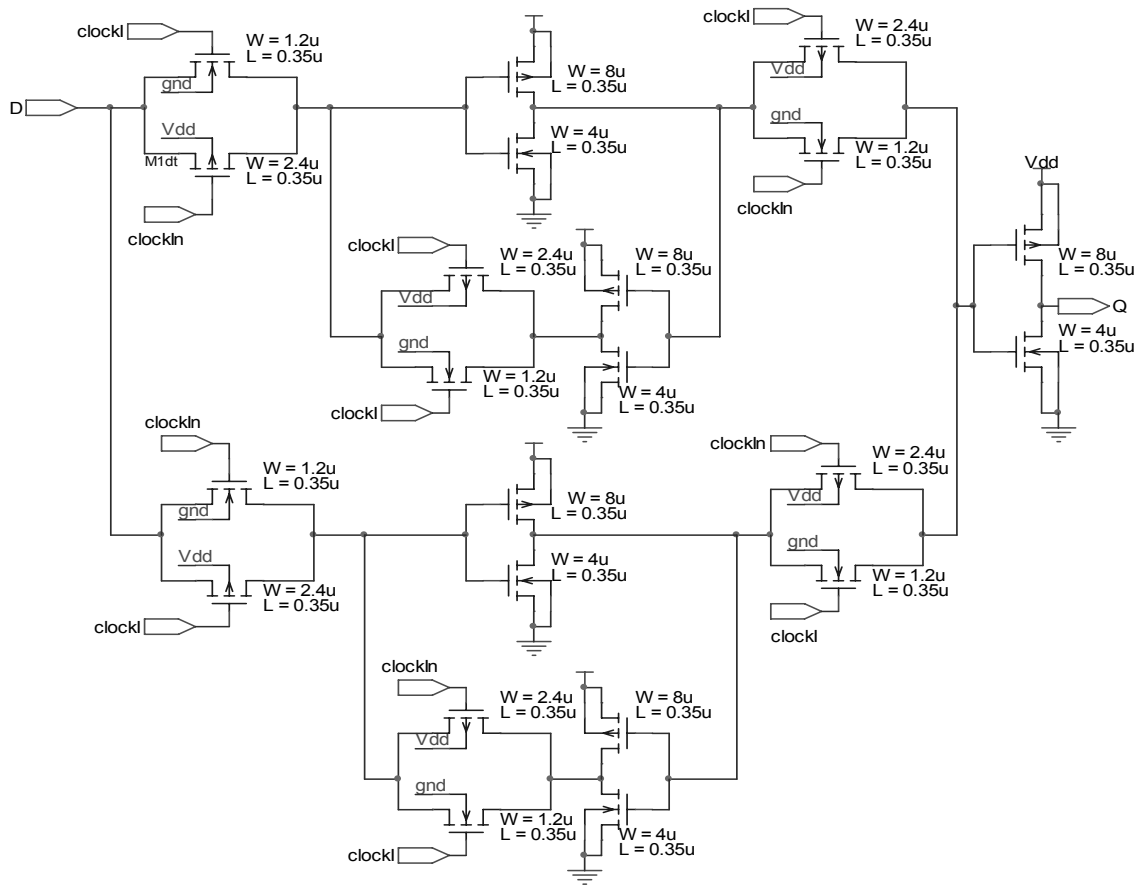


Figure C.17 FLL unit: Double-edge triggered Flip-flop.

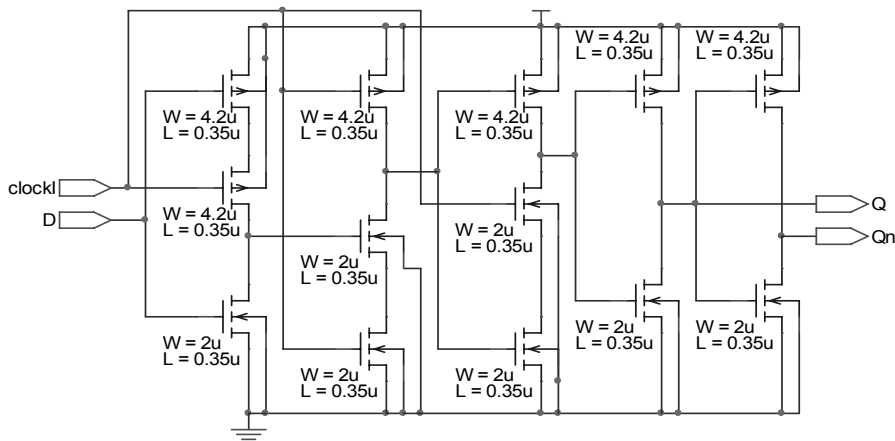


Figure C.18 FLL unit: Positive-edge triggered true single phase clocked flip-flop.

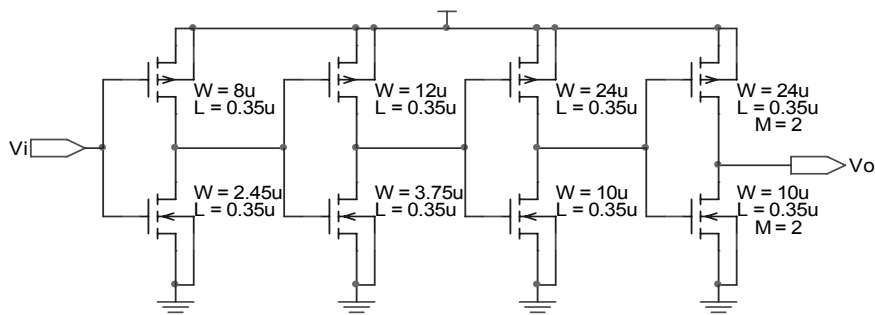


Figure C.19 FLL unit: inverter chain.

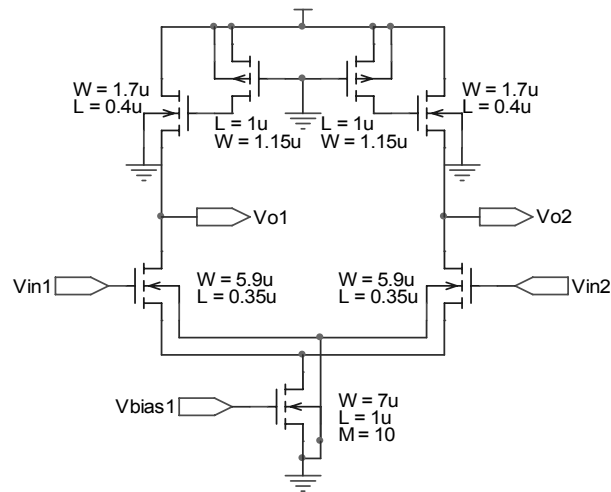


Figure C.20 FLL unit: VCO buffer.

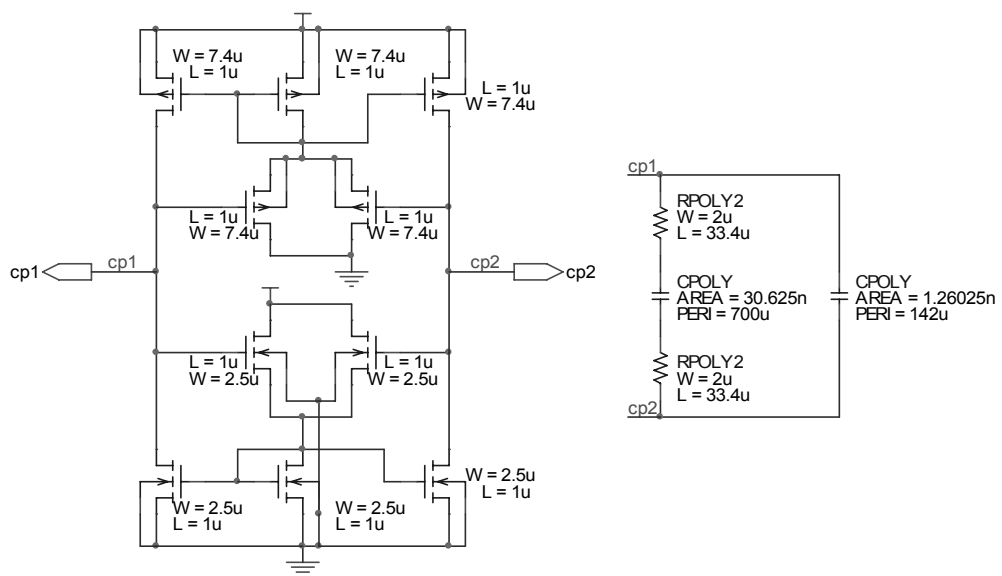
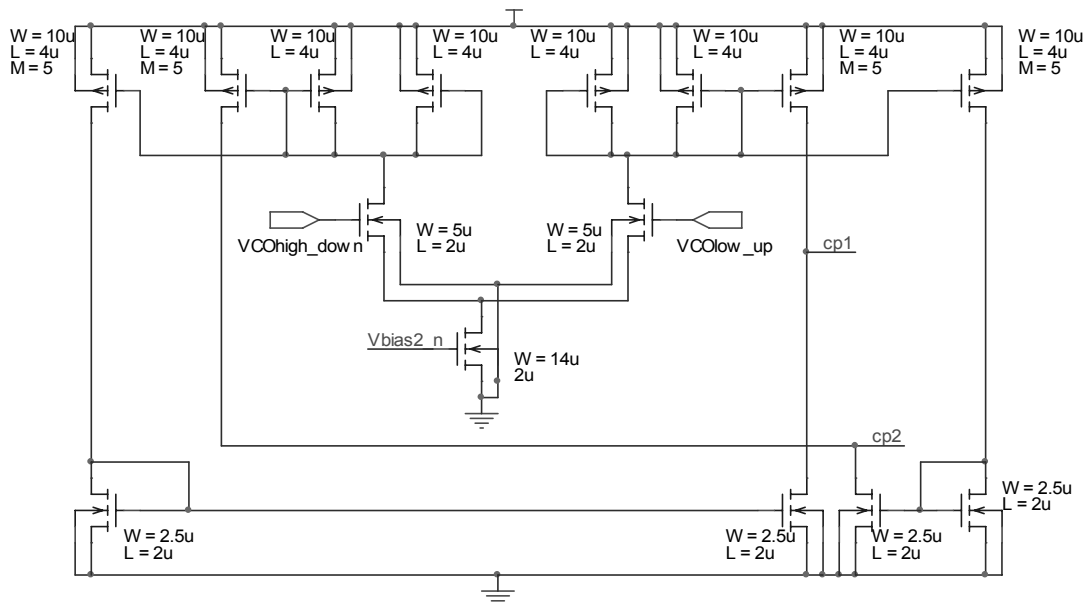


Figure C.21 FLL unit: charge pump and loop filter.