

## A FULLY CMOS OPTICAL TRANSMISSION SYSTEM BASED ON LIGHT EMITTING AVALANCHE DIODES

P. Ellinghaus<sup>1</sup>, P.J. Venter<sup>2</sup>, M. du Plessis<sup>3</sup>, P. Rademeyer<sup>4</sup> and A.W. Bogalecki<sup>5</sup>

<sup>1,4</sup> and <sup>5</sup> INSiAVA (Pty) Ltd, UP Graduate Centre, Hatfield, Pretoria, 0083

<sup>2</sup> and <sup>3</sup> Carl and Emily Fuchs Institute for Microelectronics, Dept. of Electrical, Electronic & Computer Engineering, Corner of University Road and Lynnwood Road, University of Pretoria, Pretoria 0002, South Africa

E-mail: <sup>1</sup>[pellinghaus@ieee.org](mailto:pellinghaus@ieee.org), <sup>2</sup>[jannes.venter@up.ac.za](mailto:jannes.venter@up.ac.za)

**Abstract:** The successful realization of optical interconnects for inter- and intra-chip communication strongly depends on the use of a light source that is compatible with existing, well established manufacturing processes – primarily CMOS/VLSI. The problematic integration of III-V light sources with CMOS technology has not been surmounted thus far. While silicon is ill-suited as an optical material, silicon based light sources present a huge advantage: complete monolithic integration using existing CMOS processes. This advantage can only be exploited if these devices show sufficient switching speed and optical power emission to make high speed clock and data transmission feasible. This paper illustrates the switching speed of silicon based light emitting devices in excess of 100 MHz and the viability of using such a device for an all-silicon optical link for clock and data distribution.

**Key words:** Optical interconnect, silicon light emission, silicon photonics.

### 1. INTRODUCTION

As CMOS component feature sizes are constantly being scaled down, delay degradation and power dissipation in metal interconnects will remain problematic. In the International Technology Roadmap For Semiconductors (ITRS)-2007 [1] it is predicted that optical interconnects could become one of the most viable alternative solutions to improve device and systems-on-a-chip solution performances, as the down-scaling continues.

The industry has used III-V light emitters for optical communication, over long distances, because of their high quantum efficiencies. However, the relatively short distances involved in inter- and intra-chip optical interconnects require much less optical power. This makes less efficient on-chip silicon light sources a viable alternative in the above mentioned application fields [2]. It is also well documented that silicon light emitting diodes normally have low light emitting efficiencies, but if the latter can be optimized [3], it can be utilized effectively in all-silicon optical interconnect solutions [4].

This paper will highlight the fact that even with relatively low effective power efficiencies (EPE), of the order of  $10^{-6}$ , the p-n silicon light sources designed and developed to operate in the reversed bias avalanche mode [5], could be modulated at clock frequencies of up to 120 MHz. The only restriction lies in the fact that the detector circuit was band limited to 100 MHz.

Furthermore data transfer rates of up to 700 kbps were obtained between chips, with relatively low optical power output of the silicon light source, the main limitation.

### 2. SILICON LIGHT SOURCE

#### 2.1 Point source description

The light sources consist of a reverse biased *pn*-junction formed in bulk silicon in a standard CMOS process. *n*+ structures are defined such as to enhance current density for illuminating a single concentrated point with submicron dimensions. A number of these point sources are stacked into an array and then modulated off chip by switching the devices at the boundary of avalanche breakdown. The devices break down at around 9 V, where the voltage across the devices is biased just below this value. Pulsed currents are then used to cause avalanche emission in the devices, resulting in a usable optical signal for transmission.

#### 2.2 Reflectors

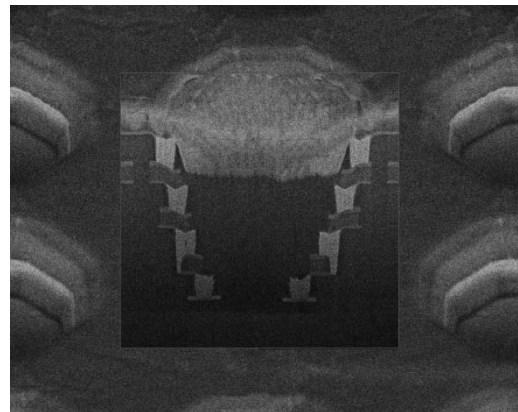


Figure 1: Cross section of reflector structure as seen under scanning electron microscope (SEM).

Figure 1 shows the light directing reflector structures used to further enhance the amount of light available perpendicularly to the light sources. Since the fibre is mounted orthogonally to the substrate plane, the reflectors assist in coupling stray light into the fibre, which improves the overall external power efficiency of the source.

### 3. SWITCHING SPEED

#### 3.1 Si diode light modulation

Silicon light emitting diodes operating in avalanche breakdown have been shown to allow light modulation up to 20 GHz using streak camera tests [6] with emission resulting from hot carrier luminescence [7]. These results prove that the modulation speed of light emitting silicon diodes in avalanche breakdown is not limited by the underlying physical processes but rather the electrical bandwidth of supporting circuitry and devices.

In this paper the high speed switching capability of Si light emitting devices is measured electrically – requiring an optical-electrical conversion – which also shows that the recovery of a useful electrical signal is possible.

#### 3.2 Experimental setup

The experimental setup is shown (conceptually) in Figure 2. A function generator (Agilent 33250A) was used to generate a sinusoidal signal to serve as an input to a driver circuit that modulated the current through the light emitting diode. The driver circuit – an emitter coupled transistor pair – was built using discrete components. The on-chip silicon light source was aligned to an optical fibre in a makeshift manner. The specifications of the optical fibre are given in Table 1.

At the receiver end, the fibre was directly connected to a commercial silicon avalanche photo diode (APD) module (detailed in Table 2). The voltage output of the APD module was connected to a spectrum analyzer (Rohde & Schwarz FSP).

A spatial separation of ~13 m between the transmitter and the receiver was used to limit the influence of electromagnetic coupling. To verify that the signal measured by the spectrum analyzer was indeed optical, measurements were taken both with and without the optical fibre connected to the APD module. This is illustrated in Figure 3 for a transmitted 120 MHz clock signal. The optical signal is clearly distinguishable over the noise floor.

The detection of clock signals at higher frequencies is primarily limited by the bandwidth of the APD module currently used which has a -3 dB bandwidth of 100 MHz.

The successful transmission and detection of a clock signal in the GHz range will require a faster APD

module, improved driver circuitry (likely to be integrated on-chip) and a mechanism to limit bandwidth integrated noise.

Table 1: Specifications for Thorlabs BFL-600 low OH optical fibre.

Length	15 m
Core diameter	600 $\mu\text{m}$
Numerical aperture	0.37 N.A.
Type	Multimode
Spectral range	400 nm – 2200 nm
Attenuation	0.01 – 0.1 dB/m

Table 2: Specifications for Hamamatsu silicon APD module C5331-11.

Bandwidth	4 kHz – 100 MHz
Photoelectric sensitivity	$\sim 2.5 \times 10^4$ V/W
Active diameter	1.0 mm
Peak sensitivity (Si APD)	0.42 A/W @ 620nm

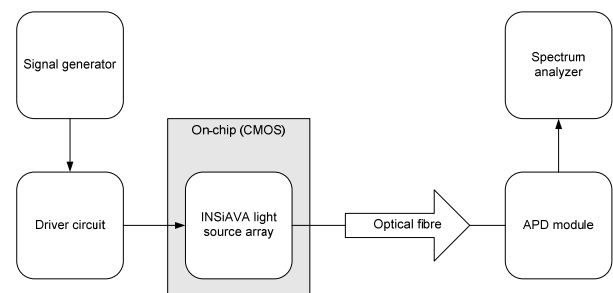


Figure 2: Conceptual experimental setup for optical clock transmission and measurement at the receiver.

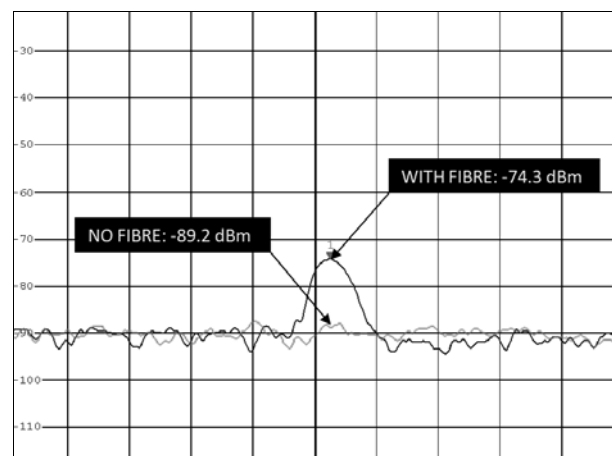


Figure 3: Measured spectrum of a 120 MHz clock signal with and without the optical fibre connected to the APD module.

#### 4. DATA LINK

To illustrate the viability of using silicon light sources for data transmission, a simple baseband modem was designed to operate at a data rate of 176 kbps. A conceptual overview of the optical data link is shown in Figure 4.

##### 4.1 Experimental setup

With reference to Figure 4: A pseudo random binary signal generator (T.1) was used as a data source. The voltage of the corresponding non-return-to-zero (NRZ) encoded data was appropriately adjusted (T.2) and fed to the driver circuit (T.3) to modulate the current of the light emitting device (T.4).

A 15 m optical fibre was once again coupled to the light source. At the receiving end the APD module (R.1) converts the optical signal to a voltage. The magnitude of this voltage signal is not large enough to be displayed on an oscilloscope; it must first be amplified (R.2) before further signal processing steps may be performed on it. After amplification the signal is passed through a Nyquist filter (R.3). The filtered signal is fed to a comparator (R.4) which hard-limits the signal to digital voltage levels (0-5 V). The embedded clock is recovered (R.5) from the NRZ encoded data, which is then used to re-time (R.6) the digital data signal.

The clock recovery, as illustrated in Figure 4, was performed in a conventional manner by performing a non-linear operation (R.5.1) on the signal to generate a spectral component at the clock frequency unto which the phase-locked loop (R.5.3) can lock. A monostable multivibrator (R.5.2), configured to be non-retriggerable, is triggered by the pulses from the zero-crossing detector (R.5.1) to ensure consistently shaped pulses. A delay element is added to adjust the clock phase to ensure the data signal is sampled at the optimal time instant i.e. in the middle of the 'eye'.

Figure 5 shows an eye diagram with a 176,000 baud rate and 35 mV<sub>p-p</sub> amplitude. The evident spikes are caused by the switching noise of the oscilloscope's trigger signal. With the use of high speed current feedback operational amplifiers (AD8011), this symbol rate was quadrupled to 704,000 baud (as shown in Figure 6). However, further signal processing steps (i.e. R.4 to R.6) were not implemented at this symbol rate.

##### 4.2 CMOS integration

The discussed system was built using only commonly available integrated circuits (mainly from the 4000 CMOS logic family). The employed APD module also uses a silicon APD. Thus, the entire system could be implemented, using a CMOS process, in a single integrated circuit.

Optical receiver front-end designs, using standard CMOS processes, have been reported [8]-[10] most recently operating up to 10 Gbps [11]. The design of high speed CMOS driver circuits for vertical cavity lasers, operating at 10Gbps, have also been shown [12]. Similar designs could be used to drive Si diodes [2] instead of III-V light sources. This all implies that a 10 Gbps optical interconnect, using only CMOS technology, is definitely feasible if the present power efficiency of silicon light sources can be further improved.

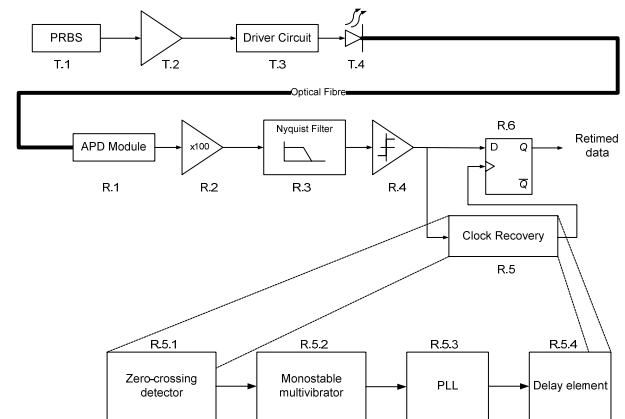


Figure 4: Conceptual overview of baseband modem for all-silicon optical data link.

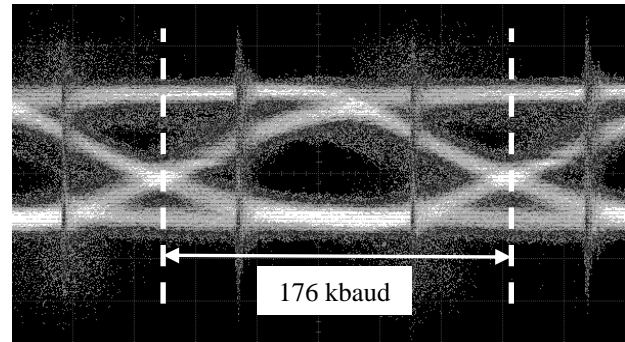


Figure 5: Eye diagram showing a symbol rate of 176 kbaud with an amplitude of 35 mV<sub>p-p</sub>.

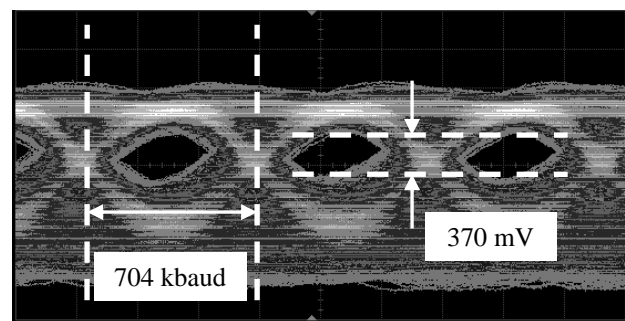


Figure 6: Eye diagram showing a symbol rate of 704 kbaud with a vertical eye opening of 370 mV.

## 5. CONCLUSION

The modulation of a VLSI-compatible silicon light emitting device has been successfully shown up to 120 MHz, primarily limited by the bandwidth of the APD module used. Furthermore, a fully functional, CMOS based, inter-chip optical interconnect operating at 176 kbps proves the feasibility of using an all-silicon solution for data and clock distribution. With increased EPE of silicon light emitters, the realization of a 10 Gbps optical interconnect should be feasible.

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