FEASIBILITY OF OPTICAL CLOCK DISTRIBUTION FOR FUTURE CMOS TECHNOLOGY NODES

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Abstract: CMOS is arguably the most successful semiconductor technology in electronics history. This is clear by the constant efforts involved in scaling as the key driver of improving the performance of ICs to keep up with consumer expectations. However, this trend has lately been haltered by another on-chip component: the interconnect. As scaling decreases active device dimensions for a corresponding performance increase, interconnect dimensions suffer under reduction due to increasing capacitance and resistance. One possible solution might be to move the long, power consuming global signal nets into the optical domain. This paper compares predicted electrical versus optical global signal distribution for future nanometre CMOS nodes, based on clock distribution and the associated power consumption.

Keywords: Optical interconnect, CMOS, optical clock distribution, hybrid.

1. INTRODUCTION

CMOS still has an immense impact as the dominant semiconductor technology for mass integration. Given the monetary and development investment up to date, the industry is throwing its full weight behind the continuation of scaling, both in terms of function density and in performance. With various breakthroughs on device level, the limitations on future scaling lie in the development of adequate interconnects to support the increase in logic density. There are numerous factors influencing the interconnect architecture used. None more so than the global clock distribution scheme. In modern microprocessor units (MPUs), the clock distribution network can be the single most power consuming entity.

This work aims to take the International Technology Roadmap for Semiconductors (ITRS) [1] requirements for future technology nodes, along with predictive SPICE modelling, in order to extrapolate on what can be expected from future electrical clock networks. As a comparative platform, an electrical H-tree is characterised in terms of its electrical power consumption components. The results are then used to indicate the feasibility of optical clock networks as device dimensions decrease.

2. PREDICTIVE TECHNOLOGY MODEL

In order to produce sensible circuit performance results, predictive SPICE modelling is used. Based on models developed by [2] and updated with the latest ITRS [1] predicted requirements for devices, SPICE based models are employed for the simulation of the optical front end receiver and clock buffer circuits. This method ensures that aspects such as short circuit currents on switching events and device drain capacitances, which may influence the results substantially, are incorporated into the prediction.

3. COMPARATIVE ARCHITECTURE

3.1 An overview of future technology parameters

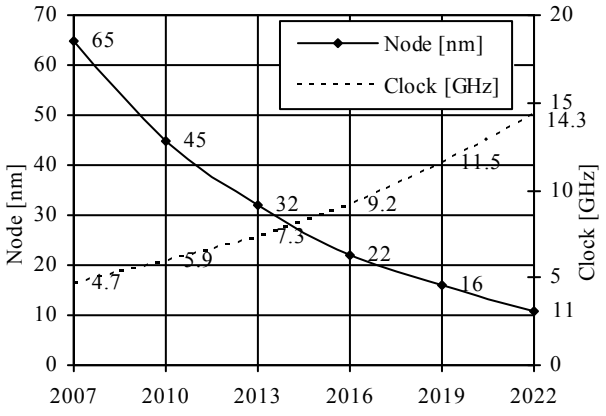

Figure 1: CMOS scaling and local clock frequency timeline.

The ITRS publishes data on an annual basis wherein technology requirements are stipulated, based on past technology trends and future market interests. Combining this information with physical modelling of, for instance, the interconnects and CMOS active devices, key technology parameters affecting the performance of clock networks can be derived. Figure 1 shows the predicted trend for CMOS scaling within the next decade, along with the expected local clock frequencies. Table II summarises the most important characteristics that can be derived from process predictions, to be expected in the near future. Logic area is predicted to maintain a relatively constant portion of chip area, as opposed to the great reduction of logic portion in [3], since both logic and SRAM functions are expected to increase at the same rate [1]. Intel's 45nm Penryn [3] reinforces this trend

Table I: Overall technology characteristics.

Parameters	Units	65nm	45nm	32nm	22nm	16nm	11nm
System characteristics							
V_{DD}	[V]	1.1	1.1	1	0.9	0.9	0.8
f_{clk}	[GHz]	4.7	5.9	7.3	9.2	11.5	14.3
Logic area	[cm^2]	2.86	2.87	2.87	2.88	2.88	2.88
D_{xtor}	[M/cm^2]	357	714	1427	2854	5708	11416
Device characteristics							
I_{on}	[μA/μm]	1006	1370	1948	1943	2344	2533
$L_{physical}$	[nm]	32	24	18	14	10.7	8.1
T_{oxp}	[nm]	1.2	0.95	0.7	0.7	0.6	0.55
T_{oxe}	[nm]	1.85	1.27	1.1	1.1	1	0.95
V_{th}	[mV]	225	175	103	105	109	109
Global interconnect characteristics							
r_{int}	[Ω/μm]	0.39	0.91	1.74	3.53	6.20	12.67
c_{int}	[F/μm]	2E-16	1.8E-16	1.7E-16	1.5E-16	1.5E-16	1.3E-16
Local interconnect characteristics							
r_{int}	[Ω/μm]	1.20	2.74	5.14	10.33	19.53	39.35
c_{int}	[F/μm]	1.8E-16	1.6E-16	1.5E-16	1.3E-16	1.3E-16	1.1E-16

where the logic area portion remained roughly the same as the previous generation MPU, although the core size is smaller than predicted for high performance MPUs [1]. The current trend is roughly double the functions per area from one technology generation to the next. On a device level, where channel depths become small enough, it is important to include the quantisation effects as an electrical equivalent oxide thickness. The physical thickness represents the effective thickness for SiO_2, while newer high-κ solutions might utilise thicker gates to minimise gate tunnelling [4]. I_{on} shows the strong inversion saturation current for NMOS devices at logic levels. The interconnect resistance and capacitance terms were calculated assuming full shielding, with minimum dimensions used for maximum density. Resistivity calculations consider effective resistance increases as dimensions decrease, including the grain boundary component, as well as the inclusion of the skin effect at high frequencies.

3.2 Clock tree topology

The three most often used topologies include grids, trees and length matched serpentines [5]. Given the capacitive and skew advantages of tree structures, the symmetrical H-tree is used as a comparative topology for comparing electrical and optical power consumption performance. This topology applies to the distribution of the global clock signal, where handover occurs at the end points into local clock regions constructed with a local grid. This local region is fed by a local clock buffer and will be common to both electrical and optical networks. Each end point sees exactly the same path as any other from the source, making skew depend only on process and environmental variations. For the purpose of this work, a square die is assumed, sized according to the predicted logic portion of a typical modern MPU. Figure 2 shows a die partitioning using an H-tree, with *n* representing the tree depth. Note that *n* for this work is not necessarily defined the same as compared to other works [3], [6]. For each increment of *n*, four new terminations, or end points will be instanced per (*n - 1*) level end point. A summary of characteristics in a typical H-tree network is shown in Table II. The depth of the tree, *n*, is determined by the

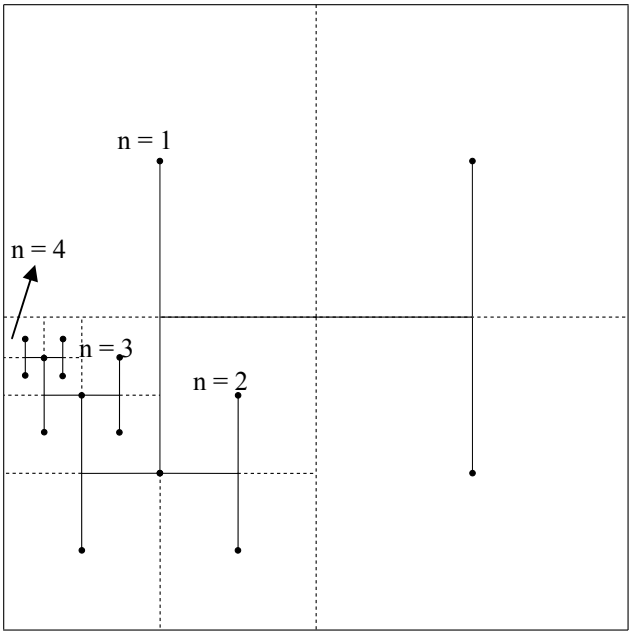

Figure 2: Partitioning of an H-tree.

maximum allowable skew for a local region, defined in [3]. As technology scales and the skew reaches a certain critical limit, the depth is incremented. The introduction of repeaters between tree splits along the segment becomes important to maintain signal flanks of an acceptable level. The 20 % - 80 % transition time metric is used, where this should be maintained below 10% of the relevant technology node's clock period, T_{clk}. The expressions developed in [7] can be modified to determine an expression for the interconnect length at which the transition time does not meet the stated criteria (see Section 4.1).

3.3 Tree depth and local region design

The depth of the tree is determined by the maximum allowable skew within a local region; that is, after a global end point feeds the local clock grid. Given the known transistor density, it is assumed for the purpose of calculations that a there are 64 gates in a register and 25 transistors per gate. If the local region dimensions are known, it is possible to calculate the number of registers in a local region and consequently determine the longest Manhattan-type interconnect length from the local region

Table II: H-tree length equations.

$\frac{3}{4}L\sum_{k=1}^{n}2^k$	Total H-tree length
$3\times L\times 2^{n-2}$	Length contributed at level *n*
$L\times 2^{-(n+1)}$	Segment length at level *n*
$3\times 2^{2n-1}$	Number of segments at level *n*
$L^2/2^n$	Area of local region at level *n*
$l_{die}/2^n$	Local area sidewall dimension
2^{2n}	Number terminating end points

buffer to the farthest register. This then represents the path of worst skew within a local region. If a maximum skew of 10 % of the clock period is used, it is possible to determine how deep the tree needs to be to adhere to the local skew requirements.

Table III: Tree and repeater design for future nodes.

Parameters		65nm	45nm	32nm	22nm	16nm	11nm
Tree design							
Max local l_{seg}		464.2	296.4	201.9	138.0	90.3	62.2
Tree depth n		6	6	7	7	8	9
# of end points		4096	4096	16384	16384	65536	262144
Max global l_{seg}		412.73	260.93	193.62	126.23	84.17	56.03
# of repeaters		4850	7070	19532	28484	80642	311798
# of split buffers		6142	6142	24574	24574	98302	393214
Repeater design parameters							
A	[Ω·µm]	695.8	575.65	395.4	366.15	315.65	273.25
B	[F/µm]	5.7E-15	4.8E-15	2.9E-15	3.0E-15	3.0E-15	2.9E-15
R		0.35	0.37	0.47	0.44	0.43	0.42
W	[µm]	13.36	7.98	5.35	3.46	2.45	1.51

4. CIRCUIT DESIGN

4.1 Electrical repeater circuits

$$\begin{aligned} a &= 0.5545 r_{int} c_{int} \\ b &= 1.386\left(r_{int} C_B + c_{int} R_B\right) \\ c &= 1.386 R_B C_B - T_{10\%} \\ l_{seg} &\le \frac{-b+\sqrt{b^2-4ac}}{2a} \end{aligned} \quad (1)$$

Equation 1 shows the maximum allowable interconnect length before the 20 % - 80 % time degrades beyond $T_{CLK}/10$. The repeaters are sized to minimise l_{seg}. A limit of two inverter pairs per repeater is set to maintain practicality. The input inverter pair is sized smaller compared to the output pair by a ratio R. This has the advantage of reducing the input capacitance, while maintaining a stronger driving capability. A lower limit exists on the value of R to maintain the requirement of a 20% - 80% transition time between inverter pairs. Equation 2 quantifies the lower limit based on the timing constraints.

$$R = \frac{1.386AB}{T_{10\%}} \times 1.1 \quad (2)$$

$T_{10\%}$ is one tenth of a clock period and the factor of 1.1 is inserted as a safety margin to ensure that the inter-stage transition time is not limiting. Although Equation 2 states a limit, an optimal value for R can be found if the total capacitance, that is the sum of the interconnect and repeater components, are normalised to a per unit length metric.

$$\frac{\partial C_{total/length}}{\partial R} = \frac{\partial}{\partial R}\left(c_{int} + \frac{B \times W \times (1+R)}{l_{seg}}\right) = 0 \quad (3)$$

Solving Equation 3, with l_{seg} as the maximum allowable segment length and c_{int} as the interconnect capacitance per unit length, yields a solution for an optimal R value. The optimal width W represents a scaling factor for transistor width, where A and B represent width dependent input capacitance and output resistance parameters of the buffer determined through maximising the segment length in Equation 1, shown in Equation 4.

$$W = \sqrt{\frac{c_{int} A}{r_{int} RB}} \quad (4)$$

4.2 Photodiode design

One limiting factor in the design of an optical system is that the photodiode does not scale along with technology. This is partly due to the lower limit on the physical dimension of the *pn*-junction region to accommodate the wavelength of incident light. Another important factor is the light intensity per unit area, which becomes unrealistic if the photodiode active region is too small. Based on [8] it is possible to obtain multi-gigahertz operation with an *n*-well based photodiode with a responsivity of 0.3 A/W, with a device capacitance of 5 fF.

4.3 Optical receiver

The chosen topology for the optical receiver front end is a high impedance design, similar to the approach in [3]. Figure 3 shows the configuration, where the photodiode discharges the input node in order to generate a logic transition by the first inverter. The following cascade of inverters serves both to delay the transition and to buffer the signal for subsequent stages. The signal v_{CH} then recharges the input node after the cascade dependent delay.

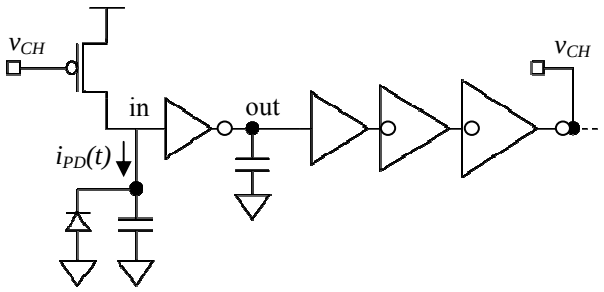

Figure 3: High impedance switched optical front end.

Although this requires a relatively strong optical pulse, the duration thereof may be very short. This topology is also well suited to standard cell compatibility, has a far superior noise performance when compared to transimpedance amplifier (TIA) approaches, and only consumes power on transitions. Most of the power consumed is due to the inverters required for driving a local region clock buffer.

5. POWER CONSUMPTION

5.1 SPICE simulations

It is possible to, from a completely theoretical perspective, utilise the following equation to determine the dynamic power dissipation of the clock networks (Equation 5).

$$P_{dyn} = C \times f_{clk} \times V_{DD}^2 \quad (5)$$

The true power consumption will increase due to short circuit currents on a switching event, and buffer output capacitances, which are difficult to model by hand. Therefore, predictive models (see Section 2) are used to estimate a more accurate quantity for expected power consumption of circuits and interconnects, which is used in the subsequent comparisons. This will obviously be more comprehensive than simply using Equation 5.

5.2 Electrical components

Figure 4 shows the resulting power consumption based on the above methodology. Because the interconnect dimensions is kept at minimum, the power consumption of the supporting circuitry for maintaining signal fidelity, namely the repeaters, are responsible for a substantial contribution to the overall power consumption. Of course, increasing the interconnect dimensions results in the component power being replaced by an increased interconnect component. It is also clear that the deep tree in the 16 nm and 11 nm nodes are contributory to the sharp increase in global power consumed.

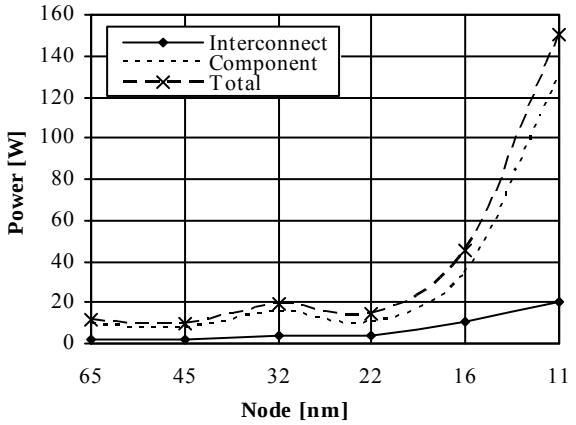

Figure 4: Electrical network power consumption.

5.3 Optical components

Figure 5 shows the situation when a fully optical tree replaces the electrical tree in Section 5.2. It becomes clear that the optical power required to maintain reasonable operation also suffers at the smaller nodes. One big reason for the sudden increase is the constant charging capacitance present on the input node in Figure 3, while the operating frequency increases. This is due to the large photodiode capacitance, which is assumed to remain constant throughout. The electrical component represents the power required to amplify the signal enough to drive a local region buffer, as well as recharging the input node capacitance back to a high logic state.

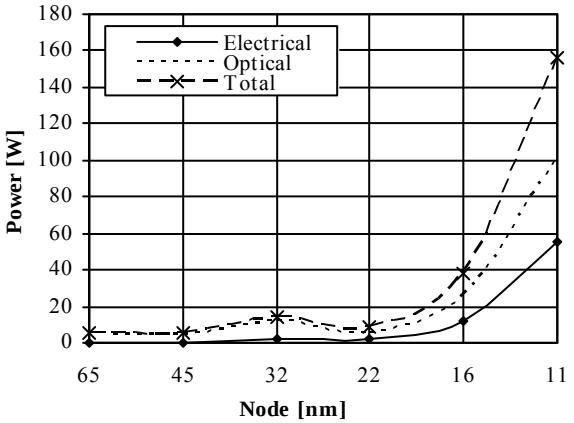

Figure 5: Optical network power consumption.

5.4 Hybrid network performance

From Figure 4 and Figure 5 it is clear that the 16 nm and 11 nm nodes presents a limit to where optical networks will outperform electrical networks. Figure 6 shows the total global clock network power consumed when the tree is made up of an optical tree up to level *n*, and then continues as an electrical tree for the rest of the tree levels. It is interesting to note that an optical tree stopping at level 7 is just as power hungry as a fully optical tree (stopping at level 8), while the required external power efficiency (EPE) to beat a completely electrical network is less stringent. Note that this EPE value does not include propagation, bending and coupling losses.

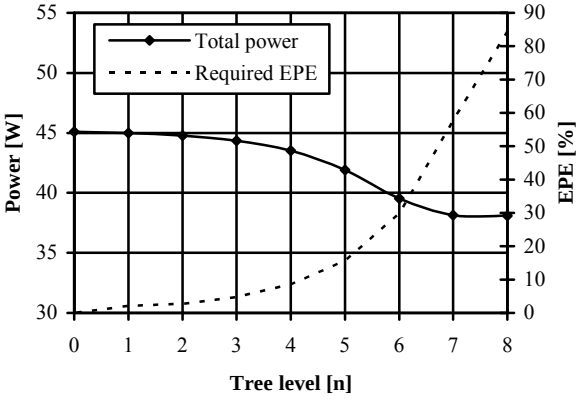

Figure 6: Total power with optical tree up to different depths, 16 nm node.

An even more interesting result is shown in Figure 7, where it can be seen that the total power consumption of the clock network decreases as the optical tree is introduced at deeper levels, but only up to a point. After a tree depth of 7 the overall power consumption increases drastically, where the required EPE to beat an electrical

system exceeds 100 %, showing that the optical network fails to surpass the performance of an electrical one.

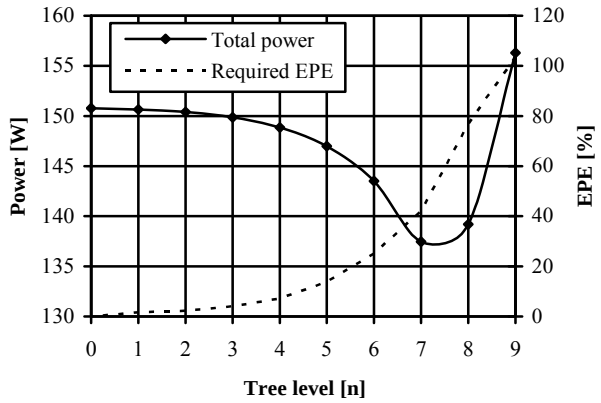

Figure 7: Total power with optical tree up to different depths, 11 nm node.

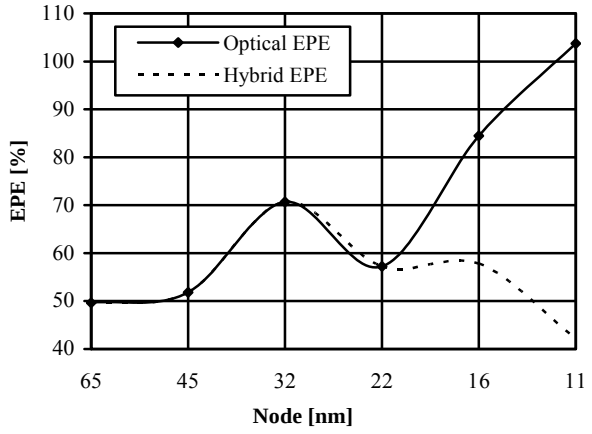

Figure 8: Optical vs. hybrid network EPE.

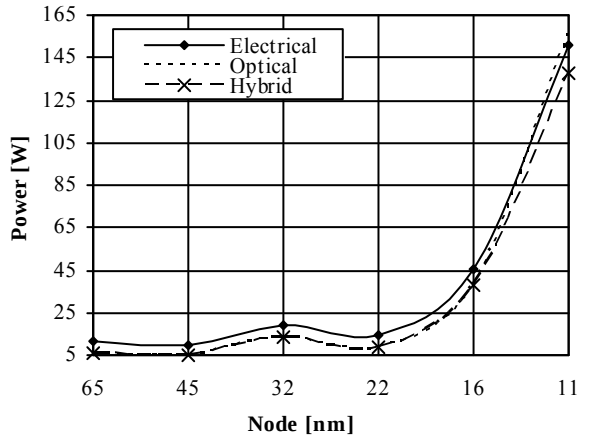

Figure 9: Electrical, optical and hybrid network total power consumed.

This shows that the optimal power consumption might be obtainable if a hybrid network is considered. Figure 8 shows that a hybrid network also relaxes the requirement for the source EPE, allowing more headroom for losses. Figure 9 shows the resulting power consumption comparisons for fully electrical, fully optical and hybrid networks for the 65 nm to 11 nm nodes.

6. CONCLUSION

The future of interconnect technology, especially for global signals, might not necessarily find solutions in a completely pure move from electrical to optical, but rather in exploiting the advantages of both in the form of hybrid networks. It is also seen that there are some fundamental limits to scaling down the optics before it would really contend as a replacement for electrical networks. For now, if light sources and on chip interconnects can handle the requirements, it would seem that optical networks are already viable for replacing electrical networks at a global signal level.

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