

High boost-ratio bidirectional converter for interfacing low-voltage battery energy storage system to a DC-bus

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Abstract

Supply and demand mismatches in renewable energy systems are addressed by integrating battery banks. Selecting battery bank terminal voltage to match DC-bus voltage (350–450 V for single-phase AC loads), necessitates employing battery banks with long-string connections along with their attendant shortcomings. To employ short-string battery banks, high-boost-ratio bidirectional interfaces are required between the DC-bus and battery bank. Current literature lacks a single source where high-boost-ratio converters' are categorised and their strengths and weaknesses identified. Comprehensive literature review is hence carried out to determine attributes of various high-boost-ratio DC–DC converters and also categorise them. The key attributes of a topology to interface battery storage to a DC-bus are determined. Based on these a bidirectional tapped-inductor boost converter emerges as the best candidate. Moreover, in order to regulate output voltage, voltage-gain versus duty-ratio characteristics should not be very steep. Since battery terminal voltage varies with state-of-charge, closed-loop control is necessary. Converter's small-signal transfer-functions are derived and a two-loop controller to regulate output voltage and inductor current while allowing bidirectional power flow designed. A novel bidirectional passive lossless snubber circuit is employed to clamp the voltage spikes across the active switches, without altering the normal operation of the converter.

Keywords – high-boost-ratio DC-DC converters' characteristics, bidirectional interleaved tapped-inductor converter, two-loop controller, small-signal modelling, disturbance rejection, lossless bidirectional snubber circuit, low-voltage battery storage interface.

1. Introduction

The current advances in harnessing of renewable energy sources (RES) such as wind and solar and also energy storage systems (ESS) have resulted in the increased application of DC systems in power distribution. DC distribution systems offer numerous advantages such as high power transmission capability, improved reliability, simple structure, and reduced losses as compared to the conventional AC systems [1]-[3].

Most practical DC microgrids utilise 350-400V [4-13] and 700-800V [4-5, 13-14] DC-busses to supply single-phase and three-phase inverters respectively. The terminal voltages of the RES feeding the DC microgrids are, however, much lower than these DC-bus voltages, necessitating the use of high boost-ratio DC-DC converters (HBRCs) to interface these sources to the DC-bus [4-8, 10-12, 15]. The HBRCs employed in these applications can be categorised into those with galvanic isolation [8, 14-17] and those without [4-15, 18-26]. Galvanic isolation can be provided using either transformers or coupled inductors [14-17]. Converters with transformer isolation can be further grouped into voltage-fed and current-fed [8, 15]. Voltage-fed topologies suffer from the following shortcomings: high-pulsed input currents that lead to

high conduction losses, high semiconductor devices' voltage stress due to leakage inductance, high transformer turns-ratio and high components count [6-8, 15, 24, 27]. Converters based on current-fed topology have lower input current ripple and lower turns-ratio [8, 15]. However, they do suffer from high input current, high switch voltage stress, high components count and self-starting problems [15].

Nonisolated HBRCs include: cascaded boost converters which suffer from high switch voltage stress, low efficiency and bidirectional capability has not been demonstrated [6-7, 15], switched-capacitor boost converters which require complex drive circuitries, have high input current ripple, capacitor voltage sharing challenges and low efficiency [6-8, 12-13, 15], and three-state switching cell boost converters which suffer from duty-ratio limitations and bidirectional power flow is not always possible [7, 15]. Moreover, all three topologies suffer from high component count and are not easy to interleave thus limiting their suitability in high power applications.

The coupled-inductor boost converters (CIBCs) have been identified as a viable solution for high boost-ratio applications [4-11, 15, 20]. The topology can be divided into two basic subgroups: cascaded CIBCs [6-7, 15] and stacked CIBCs [6-7, 15]. Variants of these two basic topologies have been developed to address their various shortcomings. Voltage-lift circuits [6-8, 15, 19], voltage multiplier circuits

(VMCs) [6-8, 15], combinations of voltage-lift and VMCs [6-7], as well as multiple windings coupled-inductors [6-7, 9], are introduced to increase voltage boost-ratio. Voltage spikes and oscillations due to leakage inductance, parasitic capacitors and effects of diode reverse recovery are alleviated using clamping circuits and soft-switching techniques [6-8, 15]. Multiwinding CIBCs also have higher flexibility and distribute voltage stress of the rectifier diodes [6, 9]. To reduce input current ripple, integrated [6, 9-12, 17] and interleaved CIBCs have been developed [6-7, 11, 16]. Integrated or hybrid topologies incorporate a conventional boost or Sepic converter input stage to lower the input current ripple and a second stage to increase voltage gain [6]. However, they suffer from high switch and diode voltage stress [6]. Interleaved CIBCs have input-side always parallel connected to share input current, thus reducing conduction and switching losses and also increasing power handling capability [4-6, 15]. In cascade CIBCs, the output-side part of the circuit is also parallel connected [6, 13, 15] lowering output current and voltage ripple. However, for stacked CIBCs, the output-side is series connected [15, 21] and output current stress is thus not lowered. They are thus not modular and increasing the number of phases in order to handle more power, reduce current stress or current ripple would cause the output voltage to increase. Moreover, those based on VMC require a high number of output capacitors [6, 21] and some topologies suffer from capacitor voltage unbalance and common mode noise problems [6, 15].

The intermittent nature of RES and their slow dynamics demands the integration of an efficient ESS to maintain system reliability and power quality [8, 18-19]. Low terminal voltage battery energy storage systems (LVBESS) are preferable to avoid the shortcomings associated with long-string connections [4-5, 8, 19]. Thus, a HBRC interface is required to cater for charge and discharge cycles. A non-isolated bidirectional interface is considered in this study due to its many advantages over isolated topologies as previously discussed. Stacked CIBCs are not considered in this study due to the shortcomings that were identified. The cascaded CIBCs with bidirectional capability [4, 5, 8, 13, 14, 18, 19, 22] are therefore those to choose from. In selecting the topology to be employed, key attributes that it must possess were defined as: modularity, size and number of output (electrolytic) capacitors, gradient of voltage-gain versus duty-ratio characteristic, switch and diode voltage stress, duty-ratio limitations, efficiency and total components count. The converters in [8, 13, 14, 18, 19, 22] have more controlled devices per phase than those in [4, 5]. Topologies in [8, 18, 22] have voltage-gain characteristics with a quadratic dependency on $1/(1-D)$ and hence have low voltage gain at low duty-ratios and very steep gradients at

moderate and high duty ratios. This makes the output voltage very sensitive to duty-ratio variations and thus difficult to regulate. Converters in [13, 14] have many switched capacitors, output-side does not benefit from interleaving and continues to experience switching frequency ripple thus requiring large output capacitors. Further, input ripple frequency is only twice switching frequency for a 4-phase converter due to the manner in which switches are gated. The topology in [19] is in addition not easy to interleave. Consequently, the bidirectional tapped-inductor converter (BTIBC) topology [4, 5] was adopted as it does not suffer from the problems identified above and is thus an efficient, simple and low cost bidirectional converter [4-5, 23-24].

As already mentioned, TIBC devices suffer from voltage spikes due to leakage inductance. A snubber circuit which can effectively clamp the voltage spikes without altering the normal operation of the converter is thus required. Although an effective clamp circuit consisting of an active switch, capacitor and a pair of inductors has previously been proposed [25], it makes the converter interface complex, expensive to implement and difficult to control. A novel bidirectional passive lossless snubber circuit to clamp the voltage spikes without affecting normal operation is thus proposed. For operation with low input and output ripple allowing significant filter capacitor reduction, input current sharing for higher power ratings and efficiency, low input voltage and hence switch voltage stress the structure for the interface is modular [4-7]. Through careful selection of the tapped-inductor windings turns-ratio and duty-cycle, the necessary boost- and buck-ratio and further reductions in size of components can be achieved while keeping the device blocking voltages within acceptable limits. Additionally, no study has previously implemented average current-mode control (ACMC) to regulate current and voltage in BTIBC.

2. Operation of the proposed two-phase bidirectional tapped-inductor converter

The proposed interface comprising of a two-phase BTIBC topology is presented in Fig. 1(a). Only the continuous current mode (CCM) operation is investigated. Converter components include MOSFETs, two sets of coupled inductor, output-side filter capacitor, and a load resistor. r_{LIN} and r_{L2N} are input- and output-side inductor resistances respectively while $r_{ds,on}$ is the MOSFETs channel resistance. Pulse Width Modulation (PWM) drives the active switches by varying the gate pulse to obtain the desired duty ratio. The gate signal driving S_{11} and S_{21} leads the gate signal for S_{12} and S_{22} by 180° respectively.

Dynamic analysis and component sizing is carried out by considering only one phase of the

converter as all the phases are identical. The windings for L_{1N} and L_{2N} are on the same core and hence, are coupled magnetically. The relationship between L_{1N} and L_{2N} is determined by the turns-ratio, n , of the magnetic element, that is,

$$\frac{L_{2N}}{L_{1N}} = \left(\frac{N_{2N}}{N_{1N}}\right)^2 = n^2 \quad (1)$$

where; N_{1N} is the primary inductor, L_{1N} , number of turns and N_{2N} is the secondary inductor, L_{2N} number of turns. This converter can operate in either buck- or boost-mode. During boost-mode operation current flows from the battery to the DC-bus and vice-versa in buck-mode operation.

2.1 Buck-mode converter operation

In buck-mode, the converter operates in two states: time-intervals $0 < t < \delta_2 T_{sw}$ when S_{2N} conducts, and $\delta_2 T_{sw} < t < T_{sw}$ when S_{1N} conducts and δ_2 is duty-ratio during buck-mode. Fig. 1(b) presents the equivalent circuits of the converter.

2.2 Boost-mode converter operation

In boost-mode, the converter operates in two states: time-intervals $0 < t < \delta_1 T_{sw}$ when S_{1N} conducts, and $\delta_1 T_{sw} < t < T_{sw}$ when S_{2N} conducts with δ_1 being the duty-ratio during boost-mode. Fig. 1(c) presents the equivalent circuit of the converter.

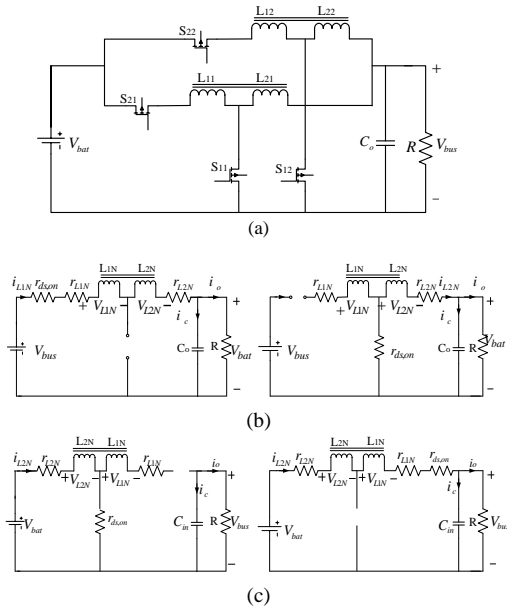


Fig. 1: (a) Two-phase BTIBC; equivalent circuit (b) when S_{2N} and S_{1N} are conducting in buck-mode operation, and (c) when S_{1N} and S_{2N} are conducting in boost-mode operation.

2.3 Small-signal transfer-functions

To facilitate control system design, the small-signal transfer-functions of the converter are derived. In Fig. 1, R is load resistor, V_{bat} , is battery voltage, V_{bus}

is DC-bus voltage, C_o , C_{in} are output and input capacitors, i_{L1N} , i_{L2N} are phase inductors L_{1N} and L_{2N} currents respectively. Further, D_1 and D_2 are switches S_{2N} and S_{1N} duty-ratios respectively and k is coupling coefficient.

2.3.1 Buck-mode transfer-functions:

In buck-mode operation, the small-signal transfer-functions are obtained from Figs. 1(b) by considering inductors L_{1N} and L_{2N} current dynamics and capacitor, C_o , voltage dynamics. During the time-interval when switches S_{1N} and S_{2N} are conducting, the relevant equations are:

$$v_{L1N} = \frac{(nk-1)\{V_{bus} - V_{bat} - i_{L1N}r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\}}{nk} \quad (2)$$

$$v_{L2N} = \frac{\{V_{bus} - V_{bat} - i_{L1N}r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\}}{nk} \quad (3)$$

$$C_o \frac{dv_{c_o}}{dt} = i_{L2N} - \frac{v_{bat}}{R} \quad (4)$$

During the interval when switches S_{1N} and S_{2N} are off, the relevant equations are obtained as:

$$v_{L1N} = (1 - nk)\{V_{bat} + i_{L2N}(r_{ds,on} + r_{L2N})\} \quad (5)$$

$$v_{L2N} = \{-V_{bat} - i_{L2N}(r_{ds,on} + r_{L2N})\} \quad (6)$$

$$C_o \frac{dv_{c_o}}{dt} = i_{L2N} - \frac{v_{bat}}{R} \quad (7)$$

After averaging the two sets of equations ((2)-(4) and (5)-(7)), perturbing and letting $D_1 = D_2 = D$, the small-signal expressions are obtained as:

$$L_{2N} \frac{d\hat{i}_{L2N}}{dt} = \hat{\delta} \left\{ \frac{1}{nk} [V_{bus} - V_{bat} - \frac{I_{L2N}R_A}{nk-1}] + V_{bat} + I_{L2N}R_B \right\} + \hat{v}_{bus} \frac{D}{nk} + \hat{v}_{bat} \frac{D+nk(1-D)}{nk} + \hat{i}_{L2N} \frac{DRA}{nk(nk-1)} - \hat{i}_{L2N}(1-D)R_B \quad (8)$$

$$C_o \frac{d\hat{v}_{bat}}{dt} = \hat{\delta} \frac{2-nk}{nk-1} I_{L2N} + \hat{i}_{L2N} \left(D \frac{2-nk}{nk-1} + 1 \right) - \frac{\hat{v}_{bat}}{R} \quad (9)$$

where $R_A = r_{ds,on} + r_{L1N} + r_{L2N}$, $R_B = r_{ds,on} + r_{L2N}$. After transforming (8) and (9) to the s -domain and rearranging, the transfer-function relating input to the output voltage is obtained as,

$$G_{1-bu} = \frac{\hat{v}_{bat}(s)}{\hat{v}_{bus}(s)} \Big|_{\hat{\delta}_1(s)=0} = \frac{D_1 R \{D_1 + nk(1-D_1)\}}{\Delta} \quad (10)$$

$$\Delta = nk(nk-1)s^2 L_{2N} C_o R - s \{C_o R r_{eq1} - nk(nk-1)L_{2N}\} + R \{D_1 + nk(1-D_1)\}^2 - r_{eq1}$$

where Δ denotes ac-terms. Similarly, the control-to-output transfer-function of the converter is obtained as,

$$G_{2-bu} = \frac{\hat{v}_{bat}(s)}{\hat{\delta}_1(s)} \Big|_{\hat{v}_{bus}(s)=0} = \frac{nk(nk-1)(2-nk)I_{L2N}R \{sL_{2N} + r_{eq1}\}}{\Delta} + \frac{(D_1 + nk(1-D_1))R \{V_{bus} - V_{bat} - I_{L1N}R_A\} + nk[V_{bat} + I_{L2N}]R_B}{\Delta} \quad (11)$$

The transfer-function that relates the inductor current to input voltage is obtained as

$$G_{3-bu} = \frac{\hat{i}_{L2N}(s)}{\hat{v}_{bus}(s)} \Big|_{\hat{\delta}_1(s)=0} = \frac{(sC_o R + 1)D_1}{\Delta} \quad (12)$$

The control-to-inductor current transfer-function is obtained as,

$$G_{4-bu} = \frac{\hat{i}_{L2N}(s)}{\hat{\delta}_1(s)} \Big|_{\hat{v}_{bus}(s)=0} = \frac{(sC_o R + 1)\{V_{bus} - V_{bat} - I_{L1N}R_A\} + nk\{V_{bat} + I_{L2N}R_B\}}{\Delta} + \frac{-RI_{L2N}\{D_1 + nk(1-D_1)\}}{\Delta} \quad (13)$$

where: $r_{eq1} = D_1(r_{ds,on} + r_{L1N} + r_{L2N}) + nk(nk - 1)\{D_1(r_{ds,on} + r_{L2N}) - (r_{ds,on} + r_{L2N})\}$.

2.3.2 Boost-mode transfer-functions:

The small-signal transfer-functions for buck-mode operation are obtained from Fig. 1(c) by considering inductors' L_{1N} and L_{2N} current dynamics and capacitor, C_{in} , voltage dynamics. During the time-interval when switches S_{1N} and S_{2N} are conducting, the relevant equations are:

$$v_{L1N} = nk\{V_{bat} - i_{L2N}r_{ds,on} - i_{L2N}r_{L2N}\} \quad (14)$$

$$v_{L2N} = \{V_{bat} - i_{L2N}r_{ds,on} - i_{L2N}r_{L2N}\} \quad (15)$$

$$C_{in} \frac{dv_{c_{in}}}{dt} = i_{L1N} - \frac{v_{bus}}{R} \quad (16)$$

During the interval when switches S_{1N} and S_{2N} are off, the relevant equations are obtained as:

$$v_{L1N} = \frac{nk\{V_{bat} - V_{bus} - i_{L2N}(r_{ds,on} + r_{L1N} + r_{L2N})\}}{1 + nk} \quad (17)$$

$$v_{L2N} = \frac{\{V_{bat} - V_{bus} - i_{L2N}(r_{ds,on} + r_{L1N} + r_{L2N})\}}{1 + nk} \quad (18)$$

$$C_{in} \frac{dv_{c_{in}}}{dt} = i_{L1N} - \frac{v_{bus}}{R} \quad (19)$$

After averaging the two sets of equations ((14)-(16) and (17)-(19)), perturbing and letting $D_1 = D_2 = D$, the small-signal expressions are obtained as:

$$L_{2N} \frac{d\hat{i}_{L2N}}{dt} = \hat{\delta} \left\{ V_{bat} - I_{L2N}R_B + \frac{(V_{bus} - V_{bat} + I_{L2N}R_A)}{1 + nk} \right\} + \frac{-\hat{v}_{bus}(1-D) + \hat{v}_{bat}(1 + nkD) - \hat{i}_{L2N}DR_A}{1 + nk} - \hat{i}_{L2N}DR_B \quad (20)$$

$$C_{in} \frac{d\hat{v}_{bus}}{dt} = -\hat{\delta}I_{L2N} + \hat{i}_{L2N}(1-D) - \frac{\hat{v}_{bus}}{R} \quad (21)$$

After transforming (20) and (21) into the s-domain and rearranging, the converter small-signal transfer-function relating input voltage to output voltage during boost-mode of operation is obtained as,

$$G_{1-bo} = \frac{\hat{v}_{bat}(s)}{\hat{v}_{bus}(s)} \Big|_{\hat{\delta}_2(s)=0} = \frac{R(1-D_2)\{1 + nkD_2\}}{(nk+1)s^2L_{2N}C_{in}R + s\{C_{in}Rr_{eq2} + (nk+1)L_{2N}\} + R\{1-D_2\}^2 + r_{eq2}} \quad (22)$$

Similarly, the control-to-output transfer-function of the converter is obtained as,

$$G_{2-bo} = \frac{\hat{v}_{bat}(s)}{\hat{\delta}_2(s)} \Big|_{\hat{v}_{bus}(s)=0} = \frac{-I_{L2N}R\{(1+nk)sL_{2N} + r_{eq2}\}}{(nk+1)s^2L_{2N}C_{in}R + s\{C_{in}Rr_{eq2} + (nk+1)L_{2N}\} + R\{1-D_2\}^2 + r_{eq2}} + \frac{R(1-D_2)\{1+nk\}[V_{bat} - I_{L2N}R_Y] + V_{bus} - V_{bat} + I_{L2N}R_Z}{(nk+1)s^2L_{2N}C_{in}R + s\{C_{in}Rr_{eq2} + (nk+1)L_{2N}\} + R\{1-D_2\}^2 + r_{eq2}} \quad (23)$$

The expression relating inductor current to input voltage is obtained as

$$G_{3-bo} = \frac{\hat{i}_{L2N}(s)}{\hat{v}_{bus}(s)} \Big|_{\hat{\delta}_2(s)=0} = \frac{(sC_{in}R + 1)(1 + nkD_2)}{(nk+1)s^2L_{2N}C_{in}R + s\{C_{in}Rr_{eq2} + (nk+1)L_{2N}\} + R\{1-D_2\}^2 + r_{eq2}} \quad (24)$$

The control to inductor current transfer-function is obtained as,

$$G_{4-bo} = \frac{\hat{i}_{L2N}(s)}{\hat{\delta}_2(s)} \Big|_{\hat{v}_{bus}(s)=0} = \frac{(sC_{in}R + 1)\{(1+nk)[V_{bat} - I_{L2N}R_Y] + V_{bus} - V_{bat} + I_{L2N}R_Z\} - RI_{L2N}(1-D_2)}{(nk+1)s^2L_{2N}C_{in}R + s\{C_{in}Rr_{eq2} + (nk+1)L_{2N}\} + R\{1-D_2\}^2 + r_{eq2}} \quad (25)$$

where: $r_{eq2} = D_2\{r_{ds,on} + r_{L1N} + r_{L2N}\} + (nk + 1)[r_{ds,on} + r_{L2N}]$ and $R_Y = (r_{ds,on} + r_{L2N})$

and $R_Z = (r_{ds,on} + r_{L1N} + r_{L2N})$

3 Performance Analysis

Ignoring the parasitic components, The DC voltage-gain during buck-mode operation, can be obtained from Figs. 1(b) and (c) as,

$$\frac{V_{bat}}{V_{bus}} = \frac{D_1}{D_1 + nk(1-D_1)} \quad (26)$$

Similarly, the DC voltage-gain during boost-mode operation and ignoring the non-ideal terms, can be obtained from Figs. 1(d) and (e) as,

$$\frac{V_{bus}}{V_{bat}} = \frac{1 + nkD_2}{1 - D_2} \quad (27)$$

Equations (26) and (27), show that voltage-gain of the BTIBC depends on turns-ratio, coupling coefficient and duty-cycle. The choice of turn-ratio also influences the active switches S_{1N} and S_{2N} blocking voltages V_{S1N} and V_{S2N} , respectively and which are given by,

$$V_{S1N} = \frac{\{[V_{bus} - I_{L1N}(r_{ds,on} + r_{L1N})] + n[V_{bat} + I_{L1N}r_{ds,on} + I_{L2N}r_{L2N}]\}}{n} \quad (28)$$

$$V_{S2N} = V_{bus} - I_{L1N}r_{ds,on} - (1-n)\{V_{bat} + I_{L2N}(r_{ds,on} + r_{L2N})\} \quad (29)$$

Consequently, converter's optimal operation requires a careful selection of turns-ratio and duty-cycle to provide the necessary boost- and buck-ratios while keeping the device blocking voltages within acceptable limits. High blocking voltages increase both the cost of

the active switching devices, and the power losses leading to reduced efficiency of the converter and larger heatsinks.

The choice of phase power rating also, has an influence on the converter performance. From [4-5], when phase power is 1kW, efficiency should be greater than 92%. Further, from [5], for a 2-phase converter, minimum ripple occurs at $D=0.5$. For a given phase power, 2-phase converter operates with lower current ripple and total RMS current than 1-phase converter. Interleaving will thus reduce the input current ripple and hence conduction and switching losses. For a total output power of up to 2kW, 2-phase converter should ensure a satisfactory efficiency over the entire power range. From (26)-(29) for a given voltage-gain, increase in turns-ratio lowers both the required duty-ratio and switch S_{2N} blocking voltage but causes a higher switch S_{1N} blocking voltage. For example, for a voltage-gain of 8, $n=6$ coincides with $D=0.5$, a switch stress of $0.25V_{bus}$ and diode stress of $1.75V_{bus}$; $n=4$ coincides with $D=0.5833$, switch stress of $0.3V_{bus}$ and diode stress of $1.5V_{bus}$. Lower turns-ratio (i.e. high input voltage) means higher switch stress and vice-versa. From [4-5], a high duty-ratio equates to high ripple operation.

BTIBC performance is evaluated based on the above design considerations, by designing and simulating a 2-phase converter with the following specifications: $V_{bat}=60V$ (during charging) and $48V$ (during discharging); $V_{bus}=380V$, $P_o=1kW$, $f_{sw}=100kHz$, output voltage ripple is 2% of the capacitor voltage, coupling coefficient, $k=0.99$, turns-ratio, $n=6$, duty-cycle, $D_1=0.53$ (in buck-mode operation) and $D_2=0.5$ (in boost-mode operation), $L_{1N}=2.97mH$, $L_{2N}=84.8\mu H$, $C_o=2.5\mu F$, $r_{L1N}=0.75\Omega$, $r_{L2N}=0.028\Omega$, and $r_{ds,on}=0.032\Omega$.

3.1 Passive lossless snubber circuit operation

Figs. 2(a) and (b) present switches S_{1N} and S_{2N} voltage waveforms in the absence of snubber circuits. It is seen that switch voltage stress is unacceptably high and there is a definite need to employ snubber circuits. Two sets of passive lossless snubber circuits are proposed to clamp the voltage spikes and recycle the leakage energy. These snubber circuits have previously been employed individually in a boost and buck converter topology based on tapped-inductor [25-26]. However, no study has proposed employing them in a BTIBC. The first set (boost-mode snubber) consists of three diodes, D_{S1N} , D_{S2N} and D_{S3N} , and two capacitors, C_{S1N} and C_{S2N} , while the second set (buck-mode snubber) consists of a capacitor, C_{CN} and two diodes, D_{C1N} and D_{C2N} . These snubber circuits allow bidirectional flow of current and do not alter the normal operation of the converter. Fig. 2(c) presents the proposed snubber circuits.

3.1.1 Buck-snubber circuit:

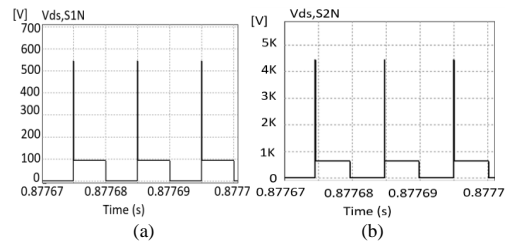
Buck snubber circuit clamps the voltage spike across S_{2N} during buck-mode operation. In the first switching interval, S_{2N} is turned on allowing current to flow from the input to the output-side. Meanwhile, the tapped-inductors get charged. In the second switching interval, S_{2N} is turned off while S_{1N} is turned on. The leakage energy is stored in the snubber capacitor, C_{CN} , and is only released to the output, via the forward biased diode, D_{C1N} , when S_{2N} turns on in the next cycle

3.1.2 Boost-mode snubber:

Boost snubber circuit clamps the voltage spike across S_{1N} during boost-mode operation. In the first switching interval, S_{1N} conducts while S_{2N} is off and the tapped-inductor gets charged. In the second switching interval, S_{1N} is switched off. The energy stored in the leakage inductance is discharged into the clamp capacitor, C_{S2N} , via the forward biased diode, D_{S1N} . This energy is further transferred to the output through the resonant capacitor, C_{S1N} , providing additional boost capability and higher efficiency.

4 Controller design

Two sets of PWM algorithms are used to drive the pair of bidirectional switches, one set in boost-mode and the other in buck-mode operation. Average current mode control (ACMC) is employed in this study to control the input current and output DC voltage. This controller offers superior performance such as excellent noise immunity and high degree of accuracy compared with other control schemes like the voltage mode control (VMC) [28]. ACMC consists of two loops; an inner current-loop designed with a higher bandwidth and hence faster dynamics compared to the outer voltage-loop. The output voltage of the proposed battery interface is regulated by sensing the output voltage and comparing it with a stable reference voltage, V_{ref} . The resultant error is compensated using an appropriate compensator network before it is fed to the inner current-loop as the reference current, I_{ref} . Fig. 2(d) shows a block diagram of a two-loop controller incorporating an ACMC. H_c and H_v represent the current and voltage sensor gains respectively.



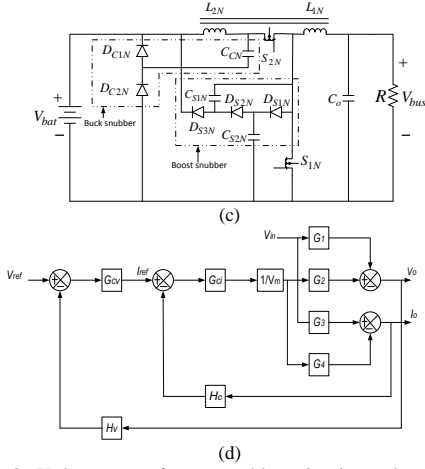


Fig. 2: Voltage waveforms, snubber circuits and controller block diagram: (a), (b) switches S_{1N} and S_{2N} voltage waveforms respectively in the absence of a snubber; (c) proposed passive lossless snubber circuit and (d) two-loop controller block diagram

The gain-bandwidth characteristic of the current-loop is tailored for optimum performance by the compensation network, G_{ci} , while the outer voltage-loop is enhanced by the inclusion of the compensator network; G_{cv} . V_m represents the amplitude of the PWM saw-tooth signal while G_1 - G_4 represents the open-loop transfer-functions of the converter.

4.1 Buck-mode controller design

The buck-mode of operation corresponds to the charging of the specified lead-acid battery. Charging should be done in a way that limits the maximum charging voltage to avoid damaging the battery cells. For a 48V rated battery, the charging voltage is determined as 55.2V to 60V as cell charging voltages range from 2.3V to 2.45V. Additionally, most manufacturers recommend a maximum charging current equivalent to 25% of the battery capacity (Ampere-hours) [29]. Therefore, for the 100Ah lead-acid battery considered in this study, the maximum charging current of 25A would suffice. However, to increase the battery lifespan, a smaller charging current of 17A is preferred which is equal to the converter output current during the converter buck-mode operation.

4.1.1 Current-loop design:

Current-loop is designed with a 20kHz bandwidth (BW), a current overshoot of 25% corresponding to a phase-margin (PM) of 45° and a settling-time (T_{settle}) less than 0.5ms. From Fig. 2(d), the open current-loop transfer-function, T_c , can be expressed as,

$$T_c = \frac{H_c \times G_{ci} \times G_4}{V_m} \quad (30)$$

Substituting converter specification into (30) while assuming the compensator transfer-function, $G_{ci}=1$, T_c is obtained as,

$$T_c = \frac{0.0087s + 496.8}{5.3 \times 10^{-8}s^2 + 2.5 \times 10^{-3}s + 40.17} \quad (31)$$

The open current-loop Bode plots are shown in Fig. 3(a). The uncompensated system has $PM=87.1^\circ$ at the desired 20kHz crossover frequency (f_{cross}). From the step-responses shown in Fig. 3(b), the current-loop has an overshoot of 12.5% and takes 0.28ms to settle within 2% of its final steady-state value. To decrease the system bandwidth to the desired f_{cross} , a lag-compensator is proposed. It improves the steady-state error by increasing only the low frequency gain while leaving the system with sufficient phase-margin. The transfer-function of the lag-compensator is obtained as,

$$G_{ci} = \frac{3.01 \times 10^{-6}s + 0.913}{1.92 \times 10^{-5}s + 1} \quad (32)$$

Fig. 3(a) presents the Bode plots of the compensated current-loop transfer-function, T_{ci} . The $PM=44.8^\circ$ at a $f_{cross}=20.4$ kHz. From the step-response, shown in Fig. 3(b), the compensated system has a steady-state error (SSE) of 2%, current-overshoot of 23.9% and settles to within 2% of its final value in 0.4ms. Hence the system meets the design specifications.

4.1.2 Voltage-loop design:

The voltage-loop is designed for $BW=5$ kHz to provide a good separation between voltage and current loops operational dynamics. In addition, the voltage-loop is designed for an overshoot of 5%, corresponding to $PM=65^\circ$ and $T_{settle}=2$ ms. The open voltage-loop transfer-function T_v is obtained from Fig. 2(d) as,

$$T_v = G_{cv} G_2 H_v \times \frac{1}{H_c G_4} \times \frac{T_{ci}}{1 + T_{ci}} \quad (33)$$

Let compensator transfer-function, $G_{cv}=1$. Substituting the converter specifications into (33) yields the open-loop voltage-gain. Fig. 3(c) presents the open voltage-loop transfer-function, T_v , Bode plots. The corresponding $PM=170.4^\circ$ at the desired $f_{cross}=5$ kHz. From the step-response, shown in Fig. 3(d), the voltage-loop has an overshoot of 2.1% and takes 0.89ms to settle to within 2% of its final value. A phase-lag compensator is proposed to decrease the PM to 66° . The lag-compensator's transfer-function is obtained as,

$$G_{cv} = \frac{2.55 \times 10^{-5}s + 1.5}{1.11 \times 10^{-5}s + 1} \quad (34)$$

The Bode plot of the compensated voltage-loop transfer-function, T_{cv} , is presented in Fig. 3(c). The $PM=65^\circ$ at $f_{cross}=5.01$ kHz. From the step-response shown in Fig. 3(d), the closed-loop has 3.95% voltage-overshoot and takes 1.5ms to settle to within 2% of its final steady-state value.

4.2 Boost-mode controller design

The boost-mode operation corresponds to the discharging of battery energy source to supply the DC-bus. The controller is designed to regulate the output bus voltage in the presence of varying input voltage as the battery charge diminishes and voltage drops below its rated value.

4.2.1 Current-loop design:

The current-loop of the converter operating in boost-mode is designed with the same specifications as those given for buck-mode operation. That is: $BW=20\text{kHz}$, current overshoot of 25%, $PM=45^\circ$ and $T_{\text{settle}} < 0.5\text{ms}$. The open current-loop transfer-function, T_c , is obtained from (30) as,

$$T_c = \frac{0.037s + 208.8}{3.39 \times 10^{-7}s^2 + 8.42 \times 10^{-4}s + 36.54} \quad (35)$$

The open current-loop Bode plots are presented in Fig. 4(a). The $PM=88.6^\circ$ at the desired f_{cross} of 20kHz. From the step-response shown in Fig. 4(b), the current-loop has an overshoot of 14.5% and requires 0.35ms to settle to within 2% of its final value. A lead-lag compensator is proposed to reduce phase-margin at 20kHz to the desired 45° . The lead-lag compensator network, G_{ci} , is derived as,

$$G_{ci} = \frac{1.16 \times 10^{-8}s^2 + 9.18 \times 10^{-6}s + 2.67}{1.39 \times 10^{-8}s^2 + 1.85 \times 10^{-5}s + 1} \quad (36)$$

The Bode plots of the compensated current-loop transfer-function, T_{ci} , are presented in Fig. 4(a). $PM=45.2^\circ$ at $f_{\text{cross}}=20.1\text{kHz}$. Fig. 4(b) shows that the compensated system has a SSE of 2%, current overshoot of 21.2% and takes 0.32ms to settle within 2% of its final value.

4.2.2 Voltage-loop design:

Just like in the case of buck-mode converter operation, the voltage-loop is designed for $BW=5\text{kHz}$, voltage overshoot of 5%, $PM=65^\circ$, and $T_{\text{settle}} < 2\text{ms}$. The open-loop transfer-function is evaluated by substituting the converter specifications into (33), with the compensator transfer-function, $G_{cv}=1$. Fig. 4(c) presents the open voltage-loop transfer-function, T_v , Bode plots. The $PM=144.5^\circ$ at the desired f_{cross} of 5kHz. Further, from the step-response, shown in Fig. 4(d), the uncompensated voltage-loop has an overshoot of 24% and settling-time of 2.5ms. A lead-lag compensator is proposed to achieve the specified f_{cross} . Compensator transfer-function is obtained as,

$$G_{cv} = \frac{1.16 \times 10^{-8}s^2 + 2.83 \times 10^{-3}s + 8.71}{1.39 \times 10^{-8}s^2 + 2.99 \times 10^{-4}s + 1} \quad (37)$$

The Bode plots of the compensated voltage-loop transfer-function, T_{cv} , are presented in Fig. 4(c). The compensated system has $PM=65.1^\circ$ at $f_{\text{cross}}=5.01\text{kHz}$. In addition, Fig. 4(d) shows that the system has a steady-state error of 1.14%, voltage overshoot of 4.96% and requires 1.5ms to settle to within 2% of its final value.

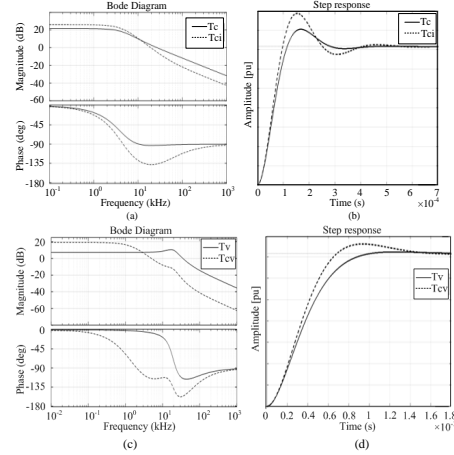


Fig. 3: Bode plots and step responses of buck-mode (a), (b) current-loop and (c), (d) voltage-loop

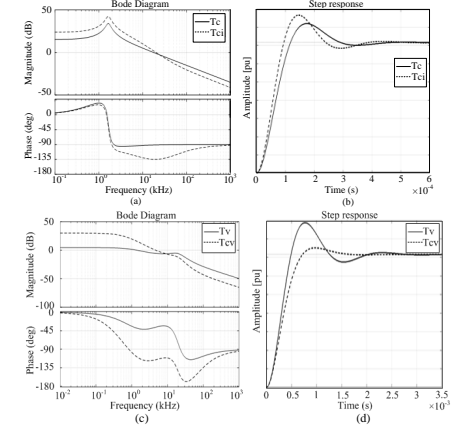


Fig. 4: Bode plots and step responses of boost-mode (a), (b) current-loop and (c), (d) voltage-loop

5 Simulation Results

Simulation of LVBESS interface, with the aforementioned specifications, is carried out using PSIM software. The key parameters of the converter interface such as output voltage, V_o , and current, I_o , input RMS current ripple, $I_{in,rms,ripple}$, input peak-to-peak current, $I_{in,pk-pk}$, switch voltages and efficiency, η , are plotted and their values compared with those derived from theoretical analysis. Both buck- and boost-mode operation are simulated to demonstrate bidirectional power flow capability. Effects of load disturbances are also investigated.

5.1 Buck-mode converter operation

Figs. 5 (a) and (b) present converter interface output voltage and current simulated waveforms for full-load operation and with a 25% step change in load. The converter achieves a large voltage step-

down of approximately 6 times at a moderate duty-cycle of 0.53. Additionally, simulation results show that the controller regulates the output voltage to within 2.5% of desired value following load disturbances.

Comparison of the parameter results obtained from simulation and those derived from theoretical analysis of the converter are presented in Table 1. It is seen that the results are in good agreement.

Table 1: Performance parameters for the converter interface operating in buck-mode.

Parameter	Analytical results	Simulated results
Duty-cycle, (D_1)	0.53	0.53
Buck-ratio	6.33	6.3
Input RMS current, ($I_{in,rms}$)	2.85A	2.77A
$I_{in,pk-pk}$	2.25A	2.26A
$I_{in,rms-ripple}$	0.75A	0.76A
Capacitor RMS current ($I_{c,rms}$)	4.78A	5.01A
V_o	60V	59.95V

5.2 Boost-mode converter operation

Figs. 5 (c) and (d) present the simulated output voltage and current waveforms for full-load operation and with a 25% step change in load. The converter achieves a voltage-gain of approximately 8 times at a moderate duty-cycle of 0.5. Additionally, simulation results indicate that the controller tracks the output voltage ensuring a voltage regulation of approximately 1.1% following load disturbances.

Comparison of the parameter results obtained from simulation and those derived from theoretical analysis of the converter topology are presented in

Table 2. It is seen that the results are in good agreement. Table 3 and

Table 4 present losses for the converter interface operating in buck- and boost-mode respectively. These losses and the corresponding efficiencies are calculated at different power levels.

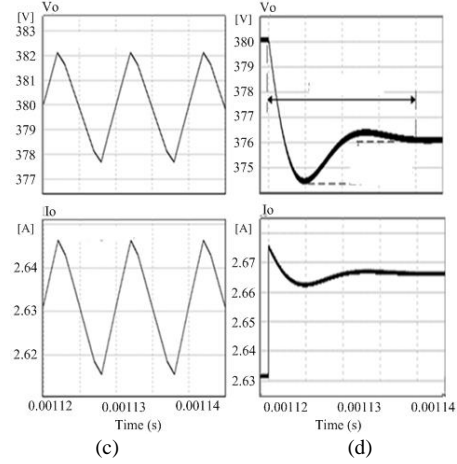
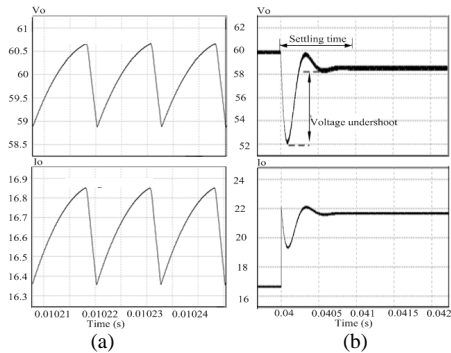


Fig. 5: Simulated output voltage and current waveforms at full-load and with a step change in load: buck-mode (a), (b) and boost-mode (c), (d)

Table 2: Performance parameters for the converter interface operating in boost-mode

Parameter	Analytical results	Simulated results
Duty-cycle, (D_2)	0.5	0.5
Boost-ratio	7.92	7.9
$I_{in,rms}$	21.8A	22.1A
$I_{in,pk-pk}$	17.1A	17.4A
$I_{in,rms-ripple}$	2.96A	2.97A
$I_{c,rms}$	0.84A	0.88A
V_o	380V	379.9V

Table 3: Converter losses for buck-mode operation at different power levels

P_o (W)	P_{cu} (W)	P_{sw} (W)	P_{cond} (W)	P_t (W)	η (%)
500	3.24	6.97	9.23	20.08	96.14
750	7.1	11.12	14.44	32.66	95.83
1000	15.5	14.93	22.8	53.23	94.95
1250	24.5	19.91	28	72.41	94.52
1500	37.4	23.64	39.7	100.74	93.71

Where P_o =output power; P_{cu} =inductor copper loss; P_{sw} =device switching loss; $P_t=P_{cu}+P_{sw}+P_{cond}$.

Table 4: Converter losses for boost-mode operation at different power levels

P_o (W)	P_{cu} (W)	P_{sw} (W)	P_{cond} (W)	P_t (W)	η (%)
500	4.28	7.43	8.02	19.73	96.2
750	4.69	12.48	14.77	31.94	95.92
1000	16.3	17.3	22.8	56.3	94.7
1250	25.1	23.1	32.32	80.5	94
1500	36.7	29.5	43.4	108.6	93.3

From Tables 3 and 4, it is observed that the bidirectional interface operates with high efficiencies during both buck- and boost-mode operation. The

slight differences could be attributed to differences in duty-cycles and RMS current during the two modes of operation.

6 Experimental Verification

A prototype of the proposed bidirectional converter interface was built to verify theoretical analysis and simulation results. The prototype was designed for rated power of 1000W but was tested at 500W.

6.1 Buck-mode operation

Fig. 6(a) shows the simulated and experimental waveforms of input and output DC voltage. An output voltage of 60V is obtained from an input voltage of 380V. These waveforms verify the large voltage step-down capability of the chosen converter interface. Figs. 6(b)-(c) present the total output and input phase inductor current waveforms while Table 5 presents the experimental, simulated and theoretical results. There is a good agreement among the results.

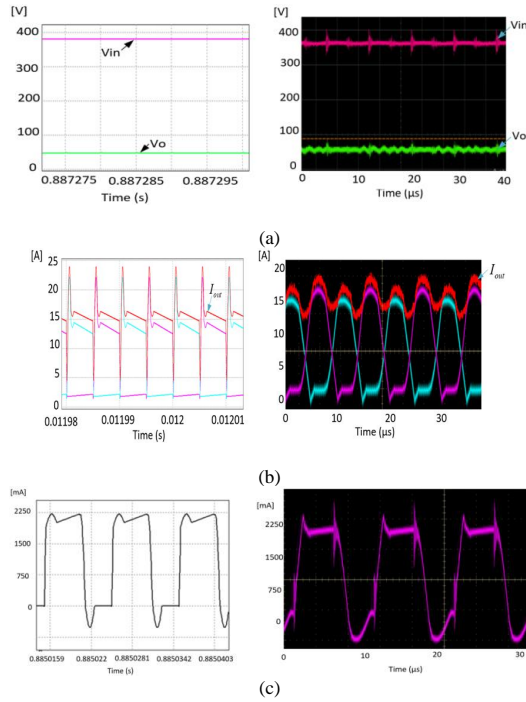


Fig. 6: Various simulated and experimental waveforms: (a), input and output voltage, (b) output currents and (c) input phase current

Table 5: Comparison of experimental, simulation and analytical results

	$I_{in,rms}$	$I_{in,pk-pk}$	$I_{L1N,pk-pk}$
Experimental	1.35A	1.3A	2.66A
Simulation	1.39A	1.12A	2.78A
Theoretical analysis	1.18A	1.1A	2.25A

6.2 Boost mode operation

Fig. 7(a) shows the simulated and experimental waveforms of input and output DC voltage. An output voltage of 380V is obtained from an input voltage of 48V. These waveforms verify the large voltage step-up capability of the chosen converter interface. Figs. 7(b)-(c) present the input and primary inductor current waveforms. Table 6 presents experimental, simulated and theoretical results.

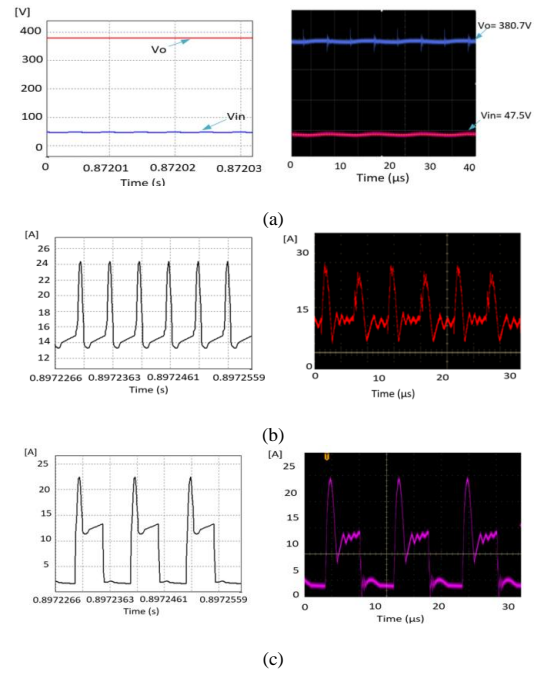


Fig. 7: Various simulated and experimental waveforms for boost-mode operation (a) input and output voltage, and (b) input and (c) primary inductor current

Fig. 8(a) shows switch S_{1N} simulated and experimental voltage waveforms while Figs. 8(b) shows switch S_{2N} simulated and experimental voltage waveforms. There is a good agreement between the simulated and experimental waveforms. The switch voltage spikes are clamped to acceptable levels verifying the suitability of the proposed passive lossless snubber circuit for both buck- and boost-modes operation.

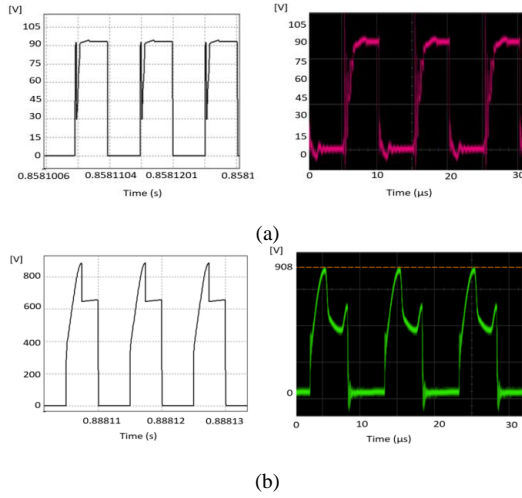


Fig. 8: Simulated and experimental switch voltage waveforms for boost-mode operation (a), (b) and buck-mode operation (c), (d)

Table 6: Comparison of experimental, simulation and analytical results

	$I_{in,rms}$	$I_{in,pk-pk}$	$I_{L21,pk-pk}$
Experimental	13.3A	22A	26.4A
Simulation	13.82A	11.2A	20.7A
Theoretical analysis	12.9A	8.55A	10A

Table 7 presents efficiency results of the converter in both buck- and boost-mode operation. There is a good agreement between the simulation and

experimental results.

Table 7: Efficiency-power characteristics of the converter interface prototype

Power	Buck-mode efficiency	Boost-mode efficiency
250W	95%	94%
500W	94.1%	93.1%

7 Conclusion

Comprehensive literature review is carried out to categorise available HBRCs and identify strengths and weaknesses of each category. The attributes of a converter topology for interfacing a LVBESS to a DC-bus are determined and used to select the best candidate from amongst those identified from the literature. The BTIBC topology emerged as the best topology. Given that battery terminal voltage varies with state-of-charge, closed-loop control is required to regulate output voltage. The BTIBC voltage-gain versus duty-ratio characteristics make it suitable for closed-loop operation compared with other topologies whose characteristics are too steep making it difficult

to regulate output voltage. Small-signal transfer-functions for both buck- and boost-mode operation are derived, and used to design a two-loop average current-mode controller. Simulation and experimental results demonstrate that the proposed BTIBC achieves a voltage boost- and buck-ratio of approximately 8 and 6 times respectively at moderate duty-cycles of 0.5 and 0.53. This is due to careful selection of the converter's tapped-inductor turns-ratio and duty-cycle, which also ensures that the active switch blocking voltage remains within acceptable limits. Interleaving allowed handling of higher power while reducing the RMS input and output ripple current, making it possible to use smaller passive components and achieve higher efficiencies.

The study also presents the design and operation of a novel passive lossless snubber circuits which does not alter the operation of the converter interface. These snubber circuits effectively clamped voltage spikes and recycled the leakage energy for additional voltage-gain and higher efficiency. Simulation results demonstrate the controller ability to reject both line and load disturbances. It was shown that the two-loop controller regulates the output voltage within 2.5% of the desired value. In both modes of operation, the bidirectional converter achieves efficiencies of 93% or higher.

8 References

- [1]. Sri R.B., Prabhakar, M.: "Transformer high-gain DC-DC converter for microgrids," IET PE 2016, 9(6), pp. 1170-1179
- [2]. Dragicevic, T., Lu, X., Vasquez, J.C., and Guerrero, J. M.: "DC microgrids-Part I: A review of control strategies and stabilisation techniques," IEEE Trans. PE, 31(7), 2016, pp. 4876-4891
- [3]. Che, L., Shahidehpour, M., Alabdulwahab, A.: "Hierarchical coordination of a community microgrid with AC and DC microgrids," IEEE Trans. Smart Grid, 6(6), 2015, pp. 3042-3051
- [4]. Gitau, M. N., Hofsajer, I. W.: "Analysis of a 4-phase tapped-inductor DC-DC converter for high boost ratio wide input voltage range applications," Proc. Industrial Electronics Society Conf., IECON, Dallas, Texas, USA, Oct. 2014, pp. 5468-5474
- [5]. Gitau, M. N.: "Analysis of N-phase tapped-inductor boost DC-DC converter," Proc. IEEE IECON., Florence, Italy, Oct. 2016, pp. 1294-1300
- [6]. Liu, H., Hu, H., Wu, H., Xing, Y.: "Overview of high-step-up coupled-inductor boost converters," IEEE JESTPE, 2016, 4(2), pp. 689-704
- [7]. Tofoli, F.L., Pereira, D.C., Paula, W.J., Junior, D.S.O.: "Survey on non-isolated high-voltage step-up DC-DC topologies based on the boost converter," IET PE, 2015, 8(10), pp. 2044-2057
- [8]. Hsieh, Y.P., Chen, J.F., Yang, L.S., Wu, C.Y., Liu, W.S.: "High conversion ratio bidirectional DC-DC converter with coupled inductor," IEEE Trans. I.E., 2014, 61(1), pp. 210-222

- [9]. Tseng, K.C., Lin, J.T., Huang, C.C.: "High step-up converter with three-winding coupled inductor for fuel-cell energy source applications," *IEEE Trans. P.E.*, 2015, 30(2), pp. 574-581
- [10]. Tseng, K.C., Cheng, C.A., Chen, C.T.: "High step-up interleaved boost converter for distributed generation using renewable and alternative power sources," *IEEE JESTPE*, 2017, 5(2), pp. 713-722
- [11]. Li, W., Xiang, X., Li, C., Li, W., He, X.: "Interleaved high step-up ZVT converter with built-in transformer voltage doubler cell for distributed PV generation system," *IEEE P.E.*, 2013, 28(1), pp. 300-313
- [12]. Ajami, A., Ardi, H., Farakhor, A.: "A novel high step-up DC-DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications," *IEEE Trans. P.E.*, 2015, 30(8), pp. 4255-4263
- [13]. Wang, Y.F., Xue, L.K., Wang, C.S., Wang, P., Li, W.: "Interleaved high-conversion-ratio bidirectional DC-DC converter for distributed energy-storage systems: circuit generation, analysis and design," *IEEE Trans. P.E.*, 2016, 31(8), pp. 5547-5561
- [14]. Xue, L.K., Wang, P., Wang, Y.F., Bei, T.Z., Yan, H.Y.: "A four-phase high voltage conversion ratio bidirectional DC-DC converter for battery applications," *Energies*, 2015, 8, pp. 6399-6426
- [15]. Padhee, S., Pati, U.C., Mahapatra, K.: "Overview of high-step-up DC-DC converters for renewable energy sources," *IETE Technical Review*, Taylor and Francis, 2016, 35(1), pp. 99-115
- [16]. Hu, Y., Wu, J., Cao, W., Xiao, W., Li, P., Finney, S.J., Li, Y.: "Ultrahigh step-up DC-DC converter with distributed generation by three degrees of freedom approach," *IEEE Trans. P.E.*, 2016, 31(7), pp. 4930-4941
- [17]. Lee, J.H., Liang, T.J., Chen, J.F.: "Isolated coupled-inductor-integrated DC-DC converter with nondissipative snubber for solar energy applications," *IEEE Trans. I.E.*, 2014, 61(7), pp. 3337-3348
- [18]. Ardi, H., Ajami, A., Kardan, F., Avilagh, S.N.: "Analysis and implementation of a nonisolated bidirectional DC-DC converter with high voltage gain," *IEEE Trans. I.E.*, 2016, 63(8), pp. 4878-4888,
- [19]. Wai, R.J, Duan, R.Y., Jheng, K.H.: "High efficiency bidirectional DC-DC converter with high voltage-gain," *IET Power Electronics*, 2012, 5(2), pp. 173-184
- [20]. Kim, J.K, Moon, G.W.: "Derivation, analysis and comparison of non-isolated single-switch high step-up converters with low voltage stress," *IEEE Trans. P.E.*, 2015, 30(3), pp. 1336-1344
- [21]. Nouri, T., Vosoughi, N., Hosseini, S.H., Sabahi, M.: "A novel interleaved nonisolated ultrahigh step-up DC-DC converter with ZVS performance," *IEEE Trans. IE*, 2017, 64(5), pp. 3650-3661
- [22]. Babaei, E., Saadatizadeh, Z.: "High voltage gain DC-DC converters based on coupled inductors," *IET PE*, 2018, 11(3), pp. 434-452
- [23]. Yuanmao, Y., Cheng, K. W., Liu, J., Xu, C.: "Bidirectional tapped-inductor-based buck-boost convertor and its circuit application," 5th International Conference on Power Electronics Systems and Applications (PESA), 2013, pp. 1-7
- [24]. Sathyan, S., Suryawanshi, H.M., Ballal, M.S., Shitole, A.B.: "Soft-switching DC-DC converter for distributed energy sources with high step-up voltage capability," *IEEE Trans. IE*, 2015, 62(11), pp. 7039-7050
- [25]. Kang, J. I., Han, J., Han, S. K.: "Lossless snubber for tapped-inductor boost converter for high step-up application," *IEEE International Conference on Industrial Technology (ICIT)*, 2014, pp. 253-260
- [26]. Yao, K., Lee, K., Meng, F.C., Wei, J.: "Tapped-inductor buck converters with a lossless clamp circuit," *IEEE APEC*, 2002, (2), pp. 693-698
- [27]. Chen, Z., Liu, S., Shi, L.: "A soft-switching full-bridge converter with reduced parasitic oscillations in a wide load range," *IEEE Trans. P.E.*, 2014, 29(2), pp. 801-812
- [28]. Shahab, H. A., Ahmad, A., Abdolreza, R.: "Modelling and current programmed control of a bidirectional full-bridge DC-DC converter," *Energy and Power Engineering*, 2012, 4(3), pp. 446-456
- [29]. Yoshihiko, H.: "Apparatus for controlling the currents supplied for battery charging and an electric load during charging of an electric vehicle battery," U.S. Patent No. 5,656,916, 1997