SVPWM-Based Power Control Strategy for a Three-Port Four-Leg DC/AC Converter With Enhanced Power Transfer Mode

Jingyuan Wu, Shiming Hu, Abhishek Kumar, *Senior Member, IEEE*, Raj M. Naidoo, *Senior Member, IEEE*, and Yan Deng, *Senior Member, IEEE*

***Abstract*—The single-stage T-type three-port converter enables efficient and accurate power distribution between two dc ports and one ac port without embedding an auxiliary dc/dc converter. Considering the diversity of loads, this article adds a T-type fourth leg to efficiently handle asymmetric and nonlinear loads. Accordingly, a new simplified space vector modulation strategy suitable for the asymmetric vector space is proposed. Only eight special switching states are used to compose the reference vector. Then, a unified algorithm is presented to obtain the maximum power distribution range of the dc port for both the T-type three-leg and four-leg three-port converters. Besides, to reduce the limitation on the dc port power transfer from the light loads, a novel technique based on the zero-sequence current is proposed to significantly expand the power distribution range. This method leverages the zero-sequence loop provided by the basic filtering components to generate additional converter currents that are crucial for the power distribution. The effectiveness of the newly proposed strategies is convincingly demonstrated through tests conducted on a 3-kW prototype.**

***Index Terms*—Maximum port power distribution, port power range expansion, three-port four-leg converter, vector control.**

I. Introduction

RENEWABLE sources, such as wind and solar energy, play an increasingly important role in the world energy landscape [1], [2]. Due to the inherent unpredictability and intermittent characteristics of these sources, there is a significant demand for energy storage systems (ESS) to guarantee stability and consistency in power supply system [3], [4]. The multistage energy transfer in traditional solutions increases the complexity of the system, and as a result, the overall efficiency is also reduced [5]. To overcome these drawbacks, single-stage multiport converters have garnered significant attention in research [6], [7], [8]. A T-type three-phase three-leg three-port converter (TPTLTPC) with two dc ports and one ac port is presented in Fig. 1. The T-type leg provides an attractive three-level output and acts as a highly integrated power transfer path for the three ports [9]. The independent low voltage U_{L} connected to the bidirectional switch only needs to be less than the high voltage U_{H}. This feature brings an ultra-wide input range of U_{L} without embedding any dc/dc converters and extra bulky passive components, which effectively improves the system integration and the power density [10], [11]. TPTLTPC has been applied to different fields for its high integration and power density, such as hybrid powertrains [12], [13], ESS [14], voltage sag compensation [15], and photovoltaic [16].

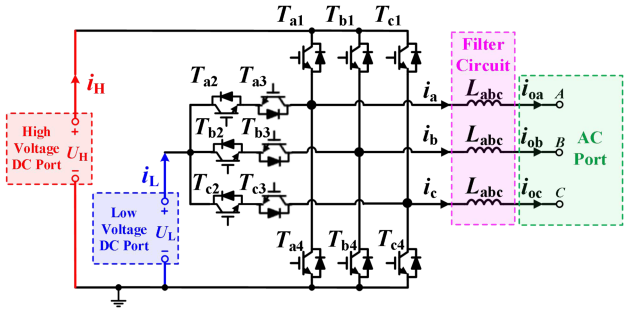

Fig. 1. T-type three-leg three-port converter (TPTLTPC).

The compact topology comes with the need for new modulation strategies. As U_{H} is not always twice U_{L}, the vector space of TPTLTPC is shifted, which makes the traditional SVPWM strategies designed under the symmetric output voltages perform not well. Another new challenge is that power decoupling is required while ensuring the ac output. In [17], the output vectors are selected by analyzing the impact on the port power. Wang et al. [18] uses specific vectors to compose the virtual vectors for sector division, and the port power is controlled by adjusting the length of the virtual vectors. The above two strategies

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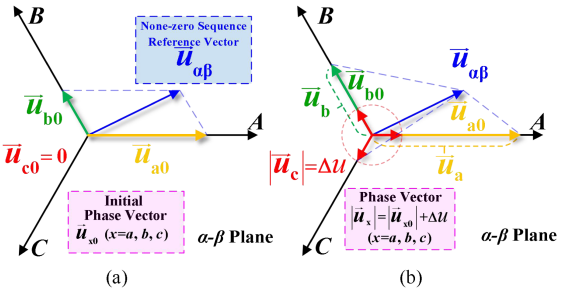

Fig. 2. Nonzero sequence reference vector decomposition in TPTLTPC. (a) Initial phase vector calculation. (b) Phase vector increment Δu.

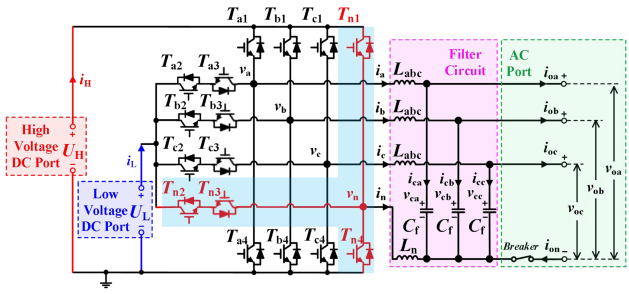

Fig. 3. Proposed TPFLTPC.

TABLE I
BASIC SWITCHING STATES

Output	U_L		U_H	
Leg x	Switching State S_i	$\lvert\vec{u}_{Lx}\rvert$ ($\lvert\vec{u}_{Lx\_\gamma}\rvert$)	Switching State S_i	$\lvert\vec{u}_{Hx}\rvert$ ($\lvert\vec{u}_{Hx\_\gamma}\rvert$)
A	S_1:(U_L, 0, 0, 0)	$2U_L/3$ ($U_L/3$)	S_2:(U_H, 0, 0, 0)	$2U_H/3$ ($U_H/3$)
B	S_3:(0, U_L, 0, 0)	$2U_L/3$ ($U_L/3$)	S_4:(0, U_H, 0, 0)	$2U_H/3$ ($U_H/3$)
C	S_5:(0, 0, U_L, 0)	$2U_L/3$ ($U_L/3$)	S_6:(0, 0, U_H, 0)	$2U_H/3$ ($U_H/3$)
N	S_7:(0, 0, 0, U_L)	U_L	S_8:(0, 0, 0, U_H)	U_H

realize a certain range of power distribution but do not clarify the maximum power distribution range (MPDR) in the fundamental period T_b, which can precalibrate the power transfer limit of the convert and make accurate power predictions. A unique SVPWM strategy is proposed in [19] and [20] by decomposing the nonzero sequence reference vector $\vec{u}_{\alpha\beta}$ into three virtual phase vectors $\vec{u}_x$ without section division. All phase vectors $\vec{u}_x$ are adjusted by the phase vector increment Δu, as shown in Fig. 2. Liu et al. [20] further divide the dc port power expression into two cases based on the number of the leg currents consistent with the given port power polarity. They also discussed how to obtain MPDR by Δu in each case is discussed separately.

Although many studies about TPTLTPC have been validated, there are more and more occasions that require the converter to circulate the zero-sequence current from asymmetric and nonlinear loads [21]. Four-leg structure has been proven to have flexible output capabilities in different scenarios, such as power quality improvement [22], [23] and stand-alone inverter [24], [25]. However, there is no research combining a T-type three-port converter with a four-leg converter to improve the system integration and provide more precise port power control. The two-level fourth leg has been researched in many papers, but since the fourth leg should be in parallel with U_H to ensure a sufficient zero-sequence adjustment range, U_L cannot participate in energy transfer through the fourth leg. So, for a three-port converter, a T-type fourth leg is a more reasonable structure and the proposed T-type three-phase four-leg TPC (TPFLTPC) is shown in Fig. 3.

There have been some research works on modulation strategies for four-leg structures. The expected performance can be realized by predictive control [24], hysteresis loop control [25], carrier modulation [26], vector control [27], etc. Among them, 3-D vector modulation (3D-SVM) stands out due to its high-quality waveforms, high dc voltage utilization, etc. 3D-SVM is usually realized in 3D-ABC or $\alpha\beta\gamma$ coordinates. The SVM in the 3D-ABC coordinate has no coordinate transformations. But, the independent control for each phase cannot be directly realized if the fourth inductor L_n is included. A well-designed L_n can reduce the current ripple while reducing the total inductor (L_n+3L_{abc}) of the filter [28]. In contrast, the control in the $\alpha\beta\gamma$ coordinate is decoupled and simple. The coupling introduced by L_n is limited to the separated zero-sequence circuit, when $\vec{u}_{ref}$ contains a zero-sequence reference $\vec{u}_\gamma$ in addition to $\vec{u}_{\alpha\beta}$. However, vector space division and reference vector localization have been the main challenges for 3D-SVM both in the above two coordinates. Many papers on simplifying 3D-SVM have been proposed and validated [29], [30], [31], [29], and determined the tetrahedron where $\vec{u}_{ref} = (U_A, U_B, U_C)$ is located and the nearest three vectors by comparing U_A, U_B, U_C, and zero. Bouzidi et al. [31] first decomposed $\vec{u}_{mathbfref}$ into a new $\rho\tau\theta$ coordinate and then summarized a criterion for identifying tetrahedrons. So far, there have been no vector strategies capable of power decoupling for the shifted 3D vector space. The vector strategy proposed in this article can exactly satisfy the above two requirements at the same time. These are two of the distinctive contributions of this article.

The rest of this article is organized as follows.

1) In Section II, the vector space is divided into two parts to simplify the reference vector composition. The reference vector $\vec{u}_{ref}$ is decomposed into a nonzero sequence reference $\vec{u}_{\alpha\beta}$ and a zero-sequence reference $\vec{u}_\gamma$. New virtual vectors are rationally defined to illustrate how to compose $\vec{u}_{\alpha\beta}$ and $\vec{u}_\gamma$, respectively. Based on these definitions, the acquisition of the MPDR is mathematically proved subsequently, and the proposed power control algorithm can be applied to both the T-type three-leg and four-leg three-port converters.
2) The analysis of the dc port power expression in Section III shows that the MPDR of a T-type three-port converter is limited by the low leg currents in light-load conditions, which means that dc port power transfer will be directly influenced by ac load uncertainty. A new working mode for expanding the MPDR by the fourth leg's current i_n is proposed. By disconnecting the zero-sequence circuit of the ac port, additional zero-sequence leg currents will be generated in the filter under the output of $\vec{u}_\gamma$. In this

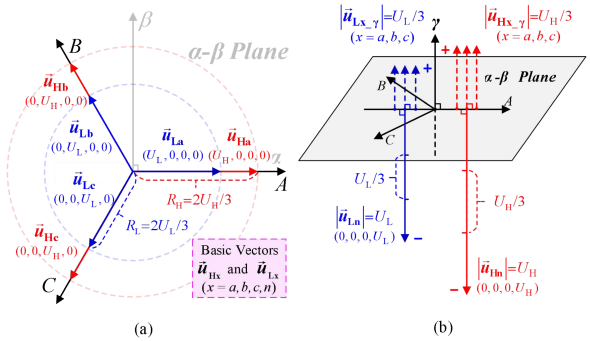

Fig. 4. Shifted vector space. (a) Nonzero sequence basic vectors. (b) Zero-sequence vectors.

mode, the fourth leg acts as an auxiliary leg and no extra devices are added.

3) In Section IV, the experimental results from a 3-kW prototype are presented.
4) Finally, Section V concludes this article.

Compared with [32], the derivation of the proposed strategies in Section II, as well as the related presentations are fully optimized and improved, and all the remaining sections are completely new.

II. Topology and Vector Space

A. Proposed Topology

In Fig. 3, $v_{\rm x}$ and $i_{\rm x}$ are the leg voltages and currents. $v_{\rm ox}$ and $i_{\rm ox}$ are the ac output voltages and currents. $v_{\rm cx}$ and $i_{\rm cx}$ are the capacitor voltages and currents. The unchanged T-type legs make $U_{\rm L}$ still, which only need to be less than $U_{\rm H}$, and TPFLTPC requires only a basic ac filter for proper operation. The type of the filter is the same as the traditional filter. According to the application scenario, it can be an *L*-type, *LC*-type, or *LCL*-type filter. In this article, a common *LC* filter with a fourth-leg inductor, $L_{\rm n}$, is used. Since this article chooses to control and analyze in the $\alpha\beta\gamma$ coordinate, $\vec{\boldsymbol{u}}_{\boldsymbol{ref}}$ is decomposed into a nonzero sequence reference $\vec{\boldsymbol{u}}_{\boldsymbol{\alpha\beta}}$ and a zero-sequence reference $\vec{\boldsymbol{u}}_{\boldsymbol{\gamma}}$.

B. Reference Vector Decomposition

TPFLTPC has a total of 81 switching states, and the reference voltage vector $\vec{\boldsymbol{u}}_{mathbfref}$ is usually composed of the selected switching states in sequence. However, the output of TPFLTPC can also be considered as the sum of the respective output from each leg. According to the Clarke transform, $\vec{\boldsymbol{u}}_{\boldsymbol{ref}}$ can also be composed of the eight special basic switching states in Table I. The commonality of these eight basic switching states is that only one leg outputs $U_{\rm L}$ or $U_{\rm H}$ while all remaining legs output zero. Liu et al. [20] only defined six virtual nonzero sequence basic vectors for the three-leg structure and the zero-sequence components are ignored. So, in the proposed four-leg topology, we should define new virtual vectors to correct the expression of $\vec{\boldsymbol{u}}_{mathbfref}$.

First, the vector space is divided into a nonzero sequence ABC coordinate in the $\alpha-\beta$ plane and a zero-sequence axis γ, which is perpendicular to the ABC coordinate, as shown in Fig. 4. The zero-sequence and nonzero sequence components of each basic switching state will be assigned a virtual vector. We define the nonzero sequence components of S_{1-6} as the ABC legs' basic vectors. Since leg N only generates negative zero-sequence voltage, the zero-sequence components of S_{7-8} are defined as the basic vectors of leg N. The two basic vectors of each leg are labeled with $\vec{\boldsymbol{u}}_{\rm Hx}$ and $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx}}$ as shown in Fig. 4. Besides, S_{1-6} also generate the additional positive zero-sequence components, $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Hx\_\gamma}}$ and $\vec{\boldsymbol{u}}_{\rm Lx\_\boldsymbol{\gamma}}$, as shown in Fig. 4(b). The magnitudes of all virtual vectors are also given in Table I according to the Clarke transform.

Second, define $\vec{\boldsymbol{u}}_{\boldsymbol{x}}$as the phase vector of each leg and the relationship between $\vec{\boldsymbol{u}}_{\boldsymbol{x}}$ and the corresponding two basic vectors, $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Hx}}$ and $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx}}$, in *ABC* legs is shown as follows:

$$\begin{cases} \vec{\boldsymbol{u}}_{\boldsymbol{x}} = d_{\rm Lx}\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx}} + d_{\rm Hx}\vec{\boldsymbol{u}}_{\boldsymbol{\rm Hx}} & (x=a,b,c) \\ |\vec{\boldsymbol{u}}_{\boldsymbol{x}}| = |\vec{\boldsymbol{u}}_{\boldsymbol{x0}}| + \Delta u = 2d_{\rm Lx}U_{\rm L}/3 + 2d_{\rm Hx}U_{\rm H}/3 & (x=a,b,c) \end{cases} \tag{1}$$

where $d_{0\rm x}$, $d_{\rm Lx}$, and $d_{\rm Hx}$ here are the duty cycles of zero, $U_{\rm L}$, and $U_{\rm H}$ in leg *x*, respectively. $|\vec{\boldsymbol{u}}_{\boldsymbol{x0}}|$ is the initial value of $|\vec{\boldsymbol{u}}_{\boldsymbol{x}}|$ and Δu is the phase vector increment for each $|\vec{\boldsymbol{u}}_{\boldsymbol{x0}}|$. Since the fourth leg's basic vectors are 1.5 times those of the *ABC* legs, $\vec{\boldsymbol{u}}_{\boldsymbol{n}}$ needs to be defined separately to unify all phase vector magnitude expressions. $\vec{\boldsymbol{u}}_{\boldsymbol{n}}$ is defined by [32]

$$\begin{cases} \vec{\boldsymbol{u}}_{\boldsymbol{n}} = 2d_{\rm Ln}\vec{\boldsymbol{u}}_{\boldsymbol{\rm Ln}}/3 + 2d_{\rm Hn}\vec{\boldsymbol{u}}_{\boldsymbol{\rm Hn}}/3 \\ |\vec{\boldsymbol{u}}_{\boldsymbol{n}}| = |\vec{\boldsymbol{u}}_{\boldsymbol{n0}}| + \Delta u = 2d_{\rm Ln}U_{\rm L}/3 + 2d_{\rm Hn}U_{\rm H}/3. \end{cases} \tag{2}$$

Therefore, the magnitude of all phase vectors can be expressed uniformly as follows:

$$|\vec{\boldsymbol{u}}_{\boldsymbol{x}}| = |\vec{\boldsymbol{u}}_{\boldsymbol{x0}}| + \Delta u = 2d_{\rm Lx}U_{\rm L}/3 + 2d_{\rm Hx}U_{\rm H}/3. \tag{3}$$

A unified expression of $|\vec{\boldsymbol{u}}_{\boldsymbol{x}}|$will play a key role in the subsequent power control. Now, we can use the above virtual vectors to express $\vec{\boldsymbol{u}}_{\boldsymbol{\rm ref}}$. According to Fig. 4, only S_{1-6} output the nonzero sequence basic vectors. So, $\vec{\boldsymbol{u}}_{\boldsymbol{x}}$ (x = *a*,*b*,*c*) consisting of the nonzero sequence basic vectors in Fig. 4(a) will compose $\vec{\boldsymbol{u}}_{\boldsymbol{\alpha\beta}}$. The remaining zero-sequence virtual vectors $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Hx\_\gamma}}$, $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx\_\gamma}}$, and $\vec{\boldsymbol{u}}_{\boldsymbol{n}}$ in Fig. 4(b) will compose $\vec{\boldsymbol{u}}_{\boldsymbol{\gamma}}$ together as shown in (4). Since all the zero-sequence vectors are colinear, the zero-sequence output in the following is directly given as a scalar u_{γ}:

$$\begin{cases} \vec{\boldsymbol{u}}_{\boldsymbol{\alpha\beta}} = \vec{\boldsymbol{u}}_{\boldsymbol{a}} + \vec{\boldsymbol{u}}_{\boldsymbol{b}} + \vec{\boldsymbol{u}}_{\boldsymbol{c}} \\ |\vec{\boldsymbol{u}}_{\boldsymbol{x}}| = 2(d_{\rm Lx}\,|\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx\_\gamma}}| + d_{\rm Hx}\,|\vec{\boldsymbol{u}}_{\boldsymbol{\rm Hx\_\gamma}}|)(x=a,b,c) \\ u_{\boldsymbol{\gamma}} = -3\,|\vec{\boldsymbol{u}}_{\boldsymbol{n}}|/2 + \sum_{x=a,b,c}(d_{\rm Lx}\,|\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx\_\gamma}}| + d_{\rm Hx}\,|\vec{\boldsymbol{u}}_{\boldsymbol{\rm Hx\_\gamma}}|) \\ \qquad = -3\,|\vec{\boldsymbol{u}}_{\boldsymbol{n}}|/2 + \sum_{x=a,b,c}(|\vec{\boldsymbol{u}}_{\boldsymbol{x}}|/2)\,. \end{cases} \tag{4}$$

We notice that $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx}}$ and $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx\_\gamma}}$ or $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx\_\gamma}}$ and $\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx\_\gamma}}$ are always output at the same time. So, we can replace $|\vec{\boldsymbol{u}}_{\boldsymbol{\rm Hx\_\gamma}}|$ and $|\vec{\boldsymbol{u}}_{\boldsymbol{\rm Lx\_\gamma}}|$ with $|\vec{\boldsymbol{u}}_{\boldsymbol{x}}|$ to simplify $\vec{\boldsymbol{u}}_{\boldsymbol{\gamma}}$, according to Table I and (3). Now, $\vec{\boldsymbol{u}}_{\boldsymbol{\rm ref}}$ can be expressed only by $|\vec{\boldsymbol{u}}_{\boldsymbol{x}}|$, and Fig. 5 further illustrates the above multilevel decomposition process.

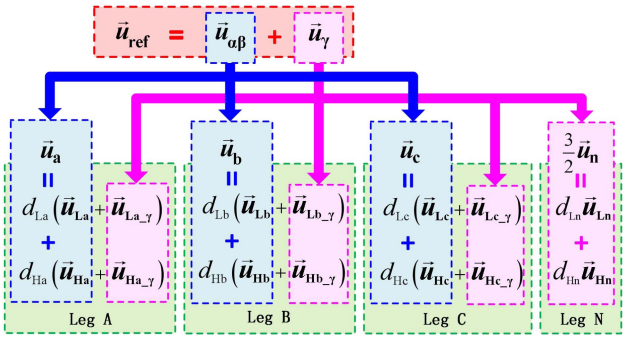

Fig. 5. Reference vector multilevel decomposition.

C. Initial Phase Vector Calculation

To get the duty cycles from (3), we still need $|\vec{u}_{\mathbf{x}}|$. We notice that if a phase vector increment Δu is increased for each $|\vec{u}_{\mathbf{x0}}|$, $\vec{u}_{\alpha\beta}$ and $\vec{u}_{\gamma}$ both stay unchanged. As all ABC basic vectors as well as their phase vectors lie on the symmetric ABC axes, the same Δu for ABC legs will not generate a nonzero sequence component and $\vec{u}_{\alpha\beta}$ remains constant. So, $\vec{u}_{\alpha\beta}$ is determined by the three initial phase vectors $|\vec{u}_{\mathbf{x0}}|$ $(x=a,b,c)$ from the ABC legs. For $\vec{u}_{\gamma}$, we can directly bring $|\vec{u}_{\mathbf{x}}|=|\vec{u}_{\mathbf{x0}}|+\Delta u$ into u_{γ}

$$\begin{aligned} u_{\gamma} &= -3\left(|\vec{u}_{\mathbf{n0}}|+\Delta u\right)/2+\sum_{x=a,b,c}\left[\left(|\vec{u}_{\mathbf{x0}}|+\Delta u\right)/2\right] \\ &= -3\,|\vec{u}_{\mathbf{n0}}|/2+\sum_{x=a,b,c}\left(|\vec{u}_{\mathbf{x0}}|/2\right). \end{aligned} \tag{5}$$

Equation (5) shows that u_{γ} is also determined only by the constant initial phase vectors, which will be introduced next. Therefore, we only need to calculate all the $|\vec{u}_{\mathbf{x0}}|$ and the maximum range of Δu to obtain all combinations of $|\vec{u}_{\mathbf{x0}}|$ that satisfy $\vec{u}_{\mathbf{ref}}$. The calculation of $|\vec{u}_{\mathbf{x0}}|$ in the four-wire system is different from [20]. $\vec{u}_{\alpha\beta}$ is also decomposed into two adjoining axes first as shown in Fig. 6(a). Although the resulting intermediate vectors $\vec{u}^{*}_{\mathbf{x0}}(x=a,b,c)$ satisfy $\vec{u}_{\alpha\beta}$, they cannot be directly used as the ABC initial vectors because the zero-sequence component produced from them is $(|\vec{u}^{*}_{\mathbf{a0}}|+|\vec{u}^{*}_{\mathbf{b0}}|+|\vec{u}^{*}_{\mathbf{c0}}|)/2$, which may not satisfy u_{γ}. In addition, each $|\vec{u}_{\mathbf{x}}|$ is less than $2U_{\mathrm{H}}/3$ according to (3), and $\Delta u_{\max}$ can be expressed as

$$\Delta u_{\max}=2U_{\mathrm{H}}/3-\mathrm{Max}\left\{|\vec{u}_{\mathbf{a0}}|,|\vec{u}_{\mathbf{b0}}|,|\vec{u}_{\mathbf{c0}}|,|\vec{u}_{\mathbf{n0}}|\right\}. \tag{6}$$

Each $|\vec{u}_{\mathbf{x0}}|$ should be as small as possible to obtain the maximum range of Δu, ensuring that all phase vector combinations satisfying $\vec{u}_{\mathbf{ref}}$ can be taken into account. $|\vec{u}_{\mathbf{x0}}|$ can be determined by the following discussion.

1) When $(|\vec{u}^{*}_{\mathbf{a0}}|+|\vec{u}^{*}_{\mathbf{b0}}|+|\vec{u}^{*}_{\mathbf{c0}}|)/2<u_{\gamma}$, we should increase the positive voltage from ABC legs. $|\vec{u}_{\mathbf{x0}}|$ is determined in the following and the calculation process is also shown in Fig. 6(b):

$$\begin{cases} \Delta u^{*}=\left(2u_{\gamma}-\sum_{y=a,b,c}\left|\vec{u}^{*}_{\mathbf{y0}}\right|\right)/3 \\ |\vec{u}_{\mathbf{x0}}|=|\vec{u}^{*}_{\mathbf{x0}}|+\Delta u^{*}(x=a,b,c) \\ |\vec{u}_{\mathbf{n0}}|=0. \end{cases} \tag{7}$$

TABLE II
EXPRESSIONS OF DUTY CYCLES

Power direction	$P_{\mathrm{L}}>0$ $(P_{\mathrm{L}}<0)$		
Current polarity	$i_{\mathrm{x}}>0$ $(i_{\mathrm{x}}<0)$		$i_{\mathrm{x}}\le 0$ $(i_{\mathrm{x}}\ge 0)$
$\lvert\vec{u}_{\mathbf{x}}\rvert$	$0<\lvert\vec{u}_{\mathbf{x}}\rvert<2U_{\mathrm{L}}/3$	$2U_{\mathrm{L}}/3<\lvert\vec{u}_{\mathbf{x}}\rvert<2U_{\mathrm{H}}/3$	
$d_{\mathrm{Lx\text{-}max}}$	$(1.5\lvert\vec{u}_{\mathbf{x}}\rvert)/U_{\mathrm{L}}$	$(U_{\mathrm{H}}\text{-}1.5\lvert\vec{u}_{\mathbf{x}}\rvert)/(U_{\mathrm{H}}\text{-}U_{\mathrm{L}})$	0
d_{Hx}	0	$1\text{-}d_{\mathrm{Lx\text{-}max}}$	$(1.5\lvert\vec{u}_{\mathbf{x}}\rvert)/U_{\mathrm{H}}$
$d_{0\mathrm{x}}$	$1\text{-}d_{\mathrm{Lx\text{-}max}}$	0	$1\text{-}d_{\mathrm{Hx}}$

2) When $(|\vec{u}^{*}_{\mathbf{a0}}|+|\vec{u}_{\mathbf{b0}^{*}}|+|\vec{u}_{\mathbf{c0}^{*}}|)/2\ge u_{\gamma}$, we should use the negative voltage from the fourth leg to reduce the zero-sequence voltage output, and $|\vec{u}_{\mathbf{x0}}|$ is determined as follows:

$$\begin{cases} \Delta u^{*}=\left(-2u_{\gamma}+\sum_{y=a,b,c}\left|\vec{u}^{*}_{\mathbf{y0}}\right|\right)/3 \\ \left|\vec{u}_{\mathbf{x0}}\right|=\left|\vec{u}^{*}_{\mathbf{x0}}\right|(x=a,b,c) \\ \left|\vec{u}_{\mathbf{n0}}\right|=0+\Delta u^{*}. \end{cases} \tag{8}$$

The aforementioned calculation minimizes all $|\vec{u}_{\mathbf{x0}}|$ while ensuring the accurate output. The following part will demonstrate the process for deriving the MPDR building upon this foundation.

D. Maximum DC Port Power Control

This part presents the sorting derivative algorithm (SDA), a new algorithm to calculate the MPDR for both TPTLTPC and TPFLTPC. We can calculate the maximum range of the average port power P_{L} in each switching period $T_{\mathrm{s}}=1/f_{\mathrm{s}}$ and then sum it cycle by cycle to obtain the MPDR, as shown in the following:

$$\mathrm{MPDR}=\frac{1}{N}\sum_{k=1}^{N}P_{\mathrm{L}}(k)(N=T_{\mathrm{b}}/T_{\mathrm{s}}). \tag{9}$$

The SDA determines whether to increase Δu or not based on the sign of $\mathrm{d}P_{\mathrm{L}}/\mathrm{d}\Delta u$, which is the derivative of the zero-sequence phase vector increment Δu with respect to the low-voltage port power P_{L}. The nonitalic symbol "d" is the differential operator and the maximum power output of U_{L} is chosen to illustrate the SDA. P_{L} can be expressed as follows:

$$P_{\mathrm{L}}=U_{\mathrm{L}}\sum_{i_{\mathrm{x}}>0}d_{\mathrm{Lx}}i_{\mathrm{x}}+U_{\mathrm{L}}\sum_{i_{\mathrm{x}}\le 0}d_{\mathrm{Lx}}i_{\mathrm{x}}. \tag{10}$$

So, (9) always holds

$$P_{\mathrm{L}}/U_{\mathrm{L}}=\sum_{i_{\mathrm{x}}>0}d_{\mathrm{Lx}}i_{\mathrm{x}}+\sum_{i_{\mathrm{x}}\le 0}d_{\mathrm{Lx}}i_{\mathrm{x}}\le\sum_{i_{\mathrm{x}}>0}d_{\mathrm{Lx}}i_{\mathrm{x}}\le\sum_{i_{\mathrm{x}}>0}d_{\mathrm{Lx-max}}i_{\mathrm{x}} \tag{11}$$

where U_{L} is a constant. To scale up P_{L}, each d_{Lx} with $i_{\mathrm{x}}\le 0$ should be zero and each d_{Lx} with $i_{\mathrm{x}}>0$ should be the maximum value that can be taken. According to (3), the expressions of $d_{\mathrm{Lx\text{-}max}}$ are summarized in Table II.

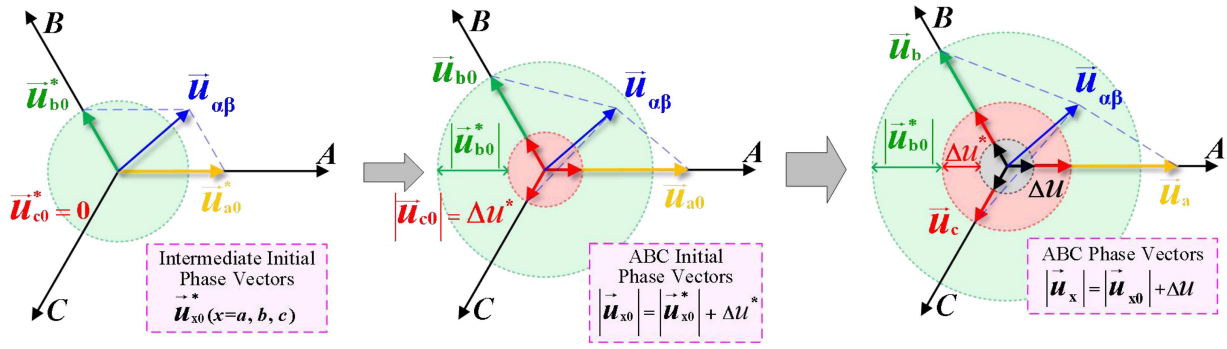

Fig. 6. Initial phase vector calculation when $(|\vec{u}_{a0}|+|\vec{u}_{b0}|+|\vec{u}_{c0}|)/2 < u_{\gamma}$.

To prevent the differential operator "d" and the duty cycle symbol "*d*" from being mixed up, we use $f_x(|\vec{u}_{x0}|+\Delta u)$ to represent $d_{Lx\text{-}max}$. Since $|\vec{u}_{x0}|$ has been determined in the previous section, $d_{Lx\text{-}max}$ is simply a function of Δu. As $d|\vec{u}_x| = d(|\vec{u}_{x0}|+\Delta u) = d\Delta u$, P_L and $dP_L/d\Delta u$ can be expressed as

$$\begin{cases} P_L = U_L \cdot \sum_{i_x>0} [d_{Lx-max} i_x] = U_L \cdot \sum_{i_x>0} [f_x(|\vec{u}_x|) i_x] \\ \frac{dP_L}{d\Delta u} = U_L \cdot \sum_{i_x>0} \left[\frac{df_x(|\vec{u}_x|)}{d\Delta u} i_x \right]. \end{cases} \tag{12}$$

By Table II, $df_x/d\Delta u$ is a piecewise constant function [32]

$$\frac{df_x(|\vec{u}_x|)}{d\Delta u} = \begin{cases} \frac{3}{2U_L} & 0 < \Delta u+|\vec{u}_{x0}| < \frac{2U_L}{3} \\ -\frac{3}{2(U_H-U_L)} & \frac{2U_L}{3} < \Delta u+|\vec{u}_{x0}| < \frac{2U_H}{3}. \end{cases} \tag{13}$$

When Δu is equal to the breakpoint ($2U_L/3$-$|\vec{u}_{x0}|$) of $df_x/d\Delta u$, $df_x/d\Delta u$ changes from positive to negative, and $|\vec{u}_x| = 2U_L/3$. The order of all $|\vec{u}_x|$ exceeding $2U_L/3$ is only determined by $|\vec{u}_{x0}|$ because all initial phase vectors increase by Δu simultaneously. $df_x/d\Delta u$ with a larger $|\vec{u}_{x0}|$ will change its sign earlier. As a linear combination of $df_x/d\Delta u$, $dP_L/d\Delta u$ will also decrease and share the same breakpoints with all $df_x/d\Delta u$ ($i_x > 0$). So, $dP_L/d\Delta u$ is also a piecewise constant function that decreases segment by segment with the increase of Δu. Such mathematical properties make it possible to obtain the MPDR with some simple calculations. The actual calculations contain the following cases [32].

1) When $dP_L/d\Delta u|_{\Delta u = 0} \le 0$, the value of $dP_L/d\Delta u$ decreases segment by segment. So, $dP_L/d\Delta u \le 0$ always holds and Δu should be zero.
2) When $dP_L/d\Delta u|_{\Delta u = \Delta u_{max}} \ge 0$, $dP_L/d\Delta u \ge 0$ always holds and Δu should be Δu_{max}.
3) When $dP_L/d\Delta u|_{\Delta u = 0} > 0$ and $dP_L/d\Delta u|_{\Delta u = \Delta u_{max}} < 0$, only $|\vec{u}_{x0}|$ that matches both $i_x > 0$ and $|\vec{u}_{x0}| \le 2U_L/3$ may change the sign of $dP_L/d\Delta u$. From (12) and (13), if their $df_x/d\Delta u$ decreases, $dP_L/d\Delta u$ will also decrease. So, pick all $|\vec{u}_{x0}|$ satisfying the above two requirements and check whether $dP_L/d\Delta u$ will change its sign at the breakpoint $\Delta u_{temp} = 2U_L/3$-$|\vec{u}_{x0}|$. The calibration can be repeated in the order of Δu_{temp} from smallest to largest. Δu_{temp} that changes the sign of $dP_L/d\Delta u$ can easily be found but it still has to be compared with Δu_{max}. The optimal Δu that maximizes P_L should be the smaller of Δu_{temp} and Δu_{max} to ensure that no $|\vec{u}_{x0}|$ exceeds $2U_H/3$.

For the case of maximum power input, only reserve d_{Lx} satisfies $i_x < 0$ in (10). Correspondingly, the Δu that minimizes P_L should change $dP_L/d\Delta u$ from negative to positive while the rest of the calculation remains the same. The key to SDA is the unified phase vector expression and the unchanged ac output with the synchronization change of all the phase vectors. It is obvious that both the expression of $|\vec{u}_x|$ and the port power expression P_L in TPTLTPC are completely consistent with the topology proposed. So, the SDA can be applied to the existing TPTLTPC.

According to SDA, the role of i_n in transferring energy is as important as the ABC leg currents. It indicates that the fourth leg also has the potential to actively expand the MPDR. Section III will discuss the necessity of this power expansion mode and the steps to realize it.

III. Power Range Expansion

While the SDA can determine the optimal duty cycle combination for achieving the MPDR, it is important to note that the MPDR is inherently limited by the leg currents i_x according to (11). The most challenging scenario arises under no-load conditions, where all leg currents are minimal, leading to a significant reduction in MPDR. This problem occurs in both TPTLTPC and TPFLTPC. Consequently, a novel power expansion mode becomes essential to mitigate the impact of light-load conditions on the power transfer capabilities. In scenarios where acquiring additional currents from the ac port is challenging, an alternative approach is to source currents within the converter. This is difficult for TPTLTPC because its three leg currents are determined only by the ac loads. But it can be achieved using a common *LC* or *LCL* filter in TPFLTPC, where the filter capacitors are connected parallel to the ac port's zero-sequence circuit. By disconnecting this zero-sequence circuit, the filter can independently generate the required additional zero-sequence current i_n under $\vec{u}_{\gamma}$, as shown in Fig. 7(a). Under these conditions, TPFLTPC operates in a three-wire configuration, as depicted in Fig. 7(b), with outputs through the nonzero sequence circuit akin to a traditional three-leg converter.

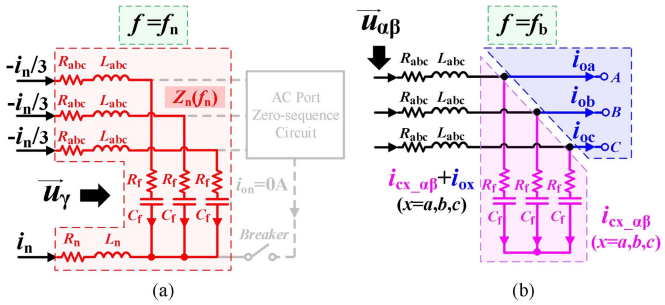

Fig. 7. Equivalent output circuit with the breaker off. (a) Independent zero-sequence filter circuit. (b) Nonzero sequence ac output circuit.

TABLE III
THEORETICAL ANALYSIS PARAMETERS

Parameters	Quantity
Input voltage U_H, U_L	600 V, 0–580 V
Output voltage U_o	311 V
Output frequency f_b	50 Hz
Output power factor φ_o	-π–π
Zero-sequence frequency f_n	50–2000 Hz
Zero-sequence current I_n	0–30 A
Filter Capacitor C_f	11 μf
Filter Inductor L_{abc}, L_n	700 μH, 1.1 mH
Three-phase light load	600 VA
Three-phase heavy load	3 kW (φ_o = 0)

This proposed mode is particularly effective for three-phase three-wire loads, which typically do not involve the zero-sequence load current i_{on}. Despite certain load limitations, the mode benefits from the use of standard components found in complete power systems, such as an *LC* or *LCL*-type filter and a circuit breaker, ensuring system compactness. In this setup, the fourth leg functions as an auxiliary element, broadening the power transfer range. We consider this power expansion mode as a supplementary approach to the standard four-wire operation. The parameters for the subsequent discussions are detailed in Table III. For the light-load conditions, the apparent power S_o is set at 600 VA, and an additional 3 kW load is used to evaluate whether the proposed power expansion mode can effectively enhance the MPDR under heavy load conditions.

A. Zero-Sequence Circuit

The zero-sequence loop of the filter is separated in Fig. 7(a), and the capacitor current i_{cx} consists of $i_{cx\cdot\alpha\beta}$ and $i_{cx\cdot\gamma} = -i_n/3$. The circuit in Fig. 7(a) is equivalent to an *LCR* series load, where $L_{eq} = L_{abc}/3+L_n$, $C_{eq} = 3C_f$, and $R_{eq} = (R_{abc}+R_f)/3+R_n$. The resonant frequency f_r is $1/(2\pi\sqrt{L_{eq}C_{eq}})$. Since i_n cannot flow in the nonzero sequence circuit of the ac port, i_n can be any controllable waveform. To simplify the control, a sine waveform is chosen in this article, which means that the zero-sequence output u_γ in a steady state is also a sine waveform. i_n can be controlled by a simple PR controller or even an open loop.

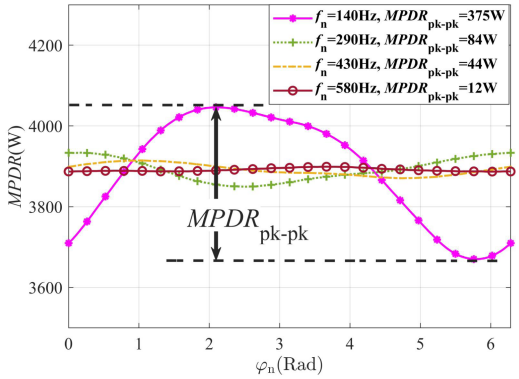

Fig. 8. Power fluctuation in P_L caused by φ_n.

B. Parameters of i_n

Under the above premise, i_n and u_γ can be expressed as follows:

$$\begin{cases} i_n = I_n\cos(w_n t+\varphi_n) = U_\gamma/|Z_n|\cdot\cos(w_n t+\varphi_n) \\ u_\gamma = -U_\gamma\cos(w_n t+\varphi_n+\varphi_{Z_n}) \\ Z_n(w_n) = R_{eq}+j\,[w_n L_{eq}-1/(w_n C_{eq})]. \end{cases} \tag{14}$$

The closer the f_n is to f_r, the smaller the zero-sequence output to generate I_n. The change in u_γ will affect the calculation results of the SDA. If $I_n = 3$ A and $f_n = 50$ Hz, the U_γ required is $I_n*|Z_n(50\text{ Hz})| = 285$ V. As U_H is usually about 600 V, it is a great challenge to the converter's zero-sequence output capability. In addition, the extra zero-sequence voltage on the capacitor is 286 V. Therefore, whether to decrease U_γ or to reduce the capacitor voltage stress, f_n should not be set too small. It is better for f_n to be close to f_r, thus reducing $|Z_n(f_n)|$.

For the zero-sequence initial phase φ_n, since f_n does not always satisfy $f_n = k*f_b$ (k is a positive integer), it is meaningless to set φ_n. Because, for ABC legs, $i_x = [i_{cx\cdot\alpha\beta}(f_b)+i_{ox}(f_b)]$-$i_n(f_n)/3$ and the converters currents are no longer periodic waveforms. So, the MPDR will change in adjacent fundamental cycles. This power fluctuation can be considered to be caused by the change of φ_n in adjacent fundamental cycles as shown in the following:

$$\begin{cases} t = t^* + 1/f_b \\ \varphi_n = \mathrm{Mod}(\varphi_n^* + 2\pi f_n/f_b, 2\pi). \end{cases} \tag{15}$$

Since higher leg currents may cause higher power fluctuation, Fig. 8 shows the influence of φ_n on the MPDR with different f_n under the heavy-load condition ($P_o = 3$ kW). When f_n is low, $\mathrm{MPDR}_{pk\text{-}pk}$ is larger, but when f_n is near f_r, MPDR will only fluctuate within a small range, e.g., only $\mathrm{MPDR}_{pk\text{-}pk} = 12$ W at $f_n = 580$ Hz. Therefore, the increase of f_n can also significantly weaken the power fluctuation caused by φ_n. At the same time, to exclude the interference of φ_n, the theoretical calculations will be weighted and summed as shown in the following:

$$\mathrm{MPDR}(f_n, I_n) = \frac{\Delta\varphi_n}{2\pi}\cdot\sum_{k=1}^{2\pi/\Delta\varphi_n}\mathrm{MPDR}(f_n, I_n, k\Delta\varphi_n). \tag{16}$$

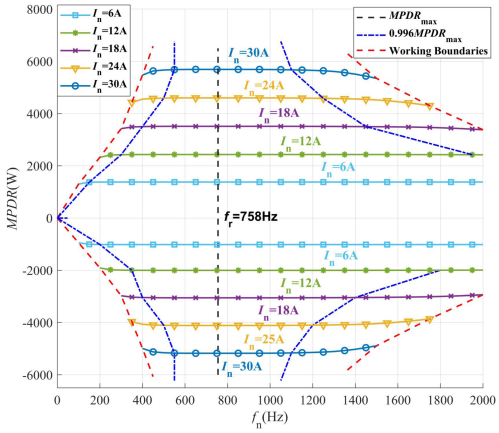

Fig. 9. Relationship between MPDR and f_n while $\varphi_o = 0$, $P_o = 600$ W, and $U_L = 500$ V.

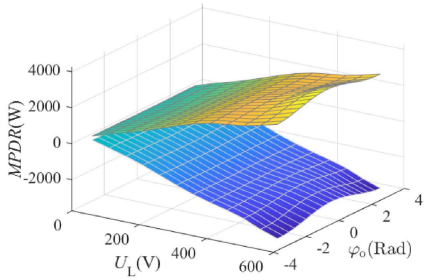

Fig. 10. Relationship among MPDR, U_L and φ_o while $S_o = 600$ VA, $U_L \in$[20 V,580 V], $f_n = 500$ Hz, and $I_n = 15$ A.

C. Theoretical MPDR Calculation

Fig. 9 shows the relationship between MPDR, f_n, and I_n. The available frequency band decreases with the increase of I_n. When f_n is too small or too large, U_γ exceeds the output capability of the converter. So, the points outside the working boundaries are dropped. Regardless of f_r, MPDR always takes its maximum value at $f_n = f_r$. When f_n is near f_r, MPDR basically does not change with f_n. This means that for a given I_n, f_n can be appropriately lowered for higher f_s/f_n. Too low f_s/f_n will reduce the quality of i_n and affects the accuracy of the theoretical prediction.

Fig. 10 illustrates the relationship among MPDR, φ_o, and U_L. To more clearly demonstrate the increase of MPDR, Fig. 11 displays the calculation results for both light and heavy loads under the unit output power factor $\varphi_o = 0$. MPDR is, indeed, significantly affected when the load is reduced. When $I_n = 0$ A and $U_L = 580$ V, MPDR reduced from (3435 W, −628 W) to (805 W, −247 W). But after adding i_n, the MPDR increases significantly at all working points. When $I_n = 4$ A, the MPDR under the light-load condition increases by 62.3%–209.8% and 12.5%–73.9% for the heavy-load condition both in two power directions. Sometimes, the MPDR under the light-load condition even exceeds the MPDR without i_n under the heavy-load condition when $U_L < 400$ V and $P_L > 0$. Therefore, using i_n to ensure the power transfer is remarkably effective, and i_n can also be used to further expand the MPDR.

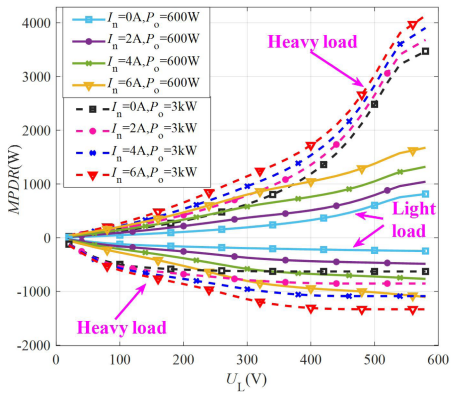

Fig. 11. Comparison of the MPDR under two different loads while $\varphi_o = 0$ and $f_n = 500$ Hz.

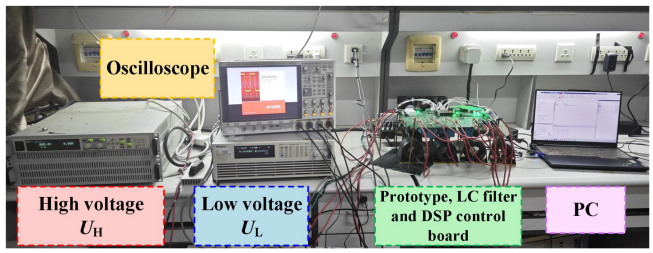

Fig. 12. Experimental platform.

TABLE IV
EXPERIMENTAL PARAMETERS

Symbol	Quantity
Input voltage U_H, U_L	600 V, 0–580 V
Output voltage U_o	311 V
Output frequency f_b	50 Hz
Switching frequency f_s	20 kHz
Zero-sequence frequency f_n	[500, 700] and [820, 900] Hz
Zero-sequence current I_n	0–6 A
Filter Capacitor C_f	11 μF
Filter Inductor L_{abc}, L_n	700 μH, 1.1 mH
Unbalanced rectifier load	400 W
Balanced rectifier load	1.1 kW
Three-phase resistive loads	600 W, 3 kW

IV. EXPERIMENTAL VERIFICATION

To verify the effectiveness of the proposed topology and associated strategies, Fig. 12 shows the prototype and the experimental platform. For simulating two independent dc sources, two programmable power supplies have been utilized. Each leg of the prototype comprises of four discrete insulated-gate bipolar transistors (IGBTs), and the implementation of closed-loop control is using a digital signal processor (DSP). The detailed parameters pertaining to the experimental platform are provided in Table IV. The control block diagram is shown in Fig. 13. When the load

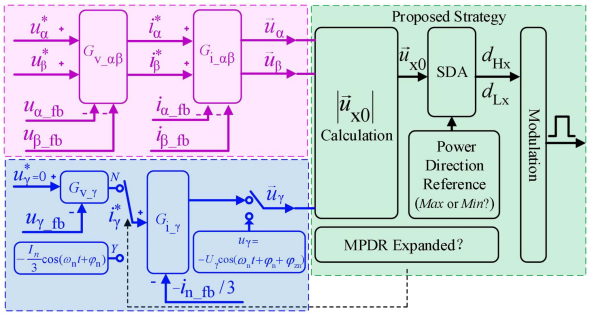

Fig. 13. Control diagram for different scenarios.

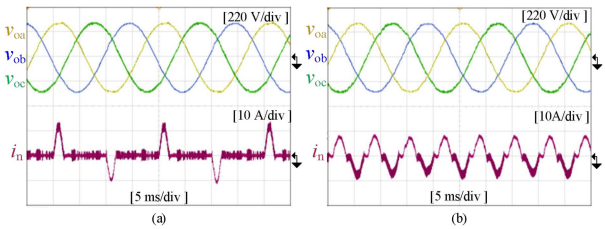

Fig. 14. Load waveforms for the rectifier loads. (a) Unbalanced rectifier load. (b) Balanced rectifier load.

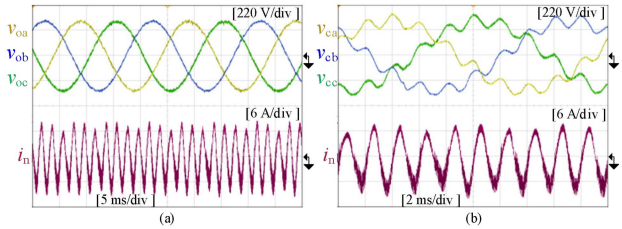

Fig. 15. Steady-state waveforms in the power expansion mode while $I_N = 6$ A, $f_n = 500$ Hz, and $P_o = 600$ W. (a) Load voltages v_{ox} ($x = a,b,c$) and i_n. (b) Capacitor voltages v_{cx} ($x = a,b,c$) and i_n.

is nonlinear, the external voltage loops generate the reference vector of the internal current loops. The voltage controllers used are repetitive controllers. It is well known that the repetition controller has good tracking performance for periodic signals and the current controllers are proportional controllers. When operating in the power range expanded mode, the zero-sequence control loop is changed to a current loop to control i_n. Since i_n in this article is a sinusoidal waveform, a PR controller is a good choice. If more simplification of the control loop is required, the zero-sequence controller even can be replaced by an open loop. After it is determined, all duty cycles will be calculated based on the reference of the port power direction and the SDA. Finally, all driving signals are generated by modulation.

A. Experimental Waveforms

Figs. 14–16 show the steady-state output waveforms under four different loads. Table V tabulates the corresponding total harmonic distortion (THD) and the voltage unbalanced factor (VUF). The fast fourier transform (FFT) analysis shows that

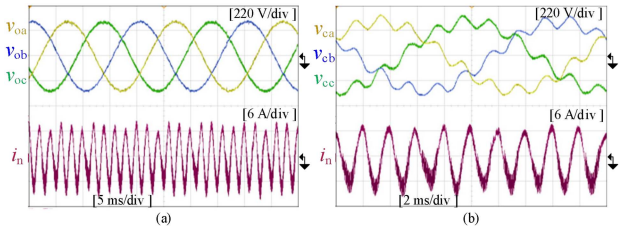

Fig. 16. Steady-state waveforms in the power expansion mode while $I_N = 6$ A, $f_n = 500$ Hz, and $P_o = 3$ kW. (a) Load voltages v_{ox} ($x = a,b,c$) and i_n. (b) Capacitor voltages v_{cx} ($x = a,b,c$) and i_n.

TABLE V
MEASURED THD AND VUF FOR LOAD VOLTAGES

Load type	THD (%)			VUF (%)	
	A	B	C	VUF_{neg}	VUF_{γ}
Unbalanced Rec. load	1.61	1.74	1.71	0.12	0.19
Balanced Rec. load	2.20	2.15	2.30	0.30	0.16
Balanced heavy Res. load	1.54	1.64	1.35	0.13	0.17
Balanced light Res. load	1.63	1.61	1.68	0.12	0.13

the load voltages of the unbalanced rectifier load contain 3rd, 5th, 7th, and 9th-order harmonics, while the balanced rectifier load mainly includes 5th and 7th-order harmonics. Waveforms are overall satisfactory for two nonlinear loads. THD and VUF under the balanced rectifier load are slightly higher because the controllers have not been further optimized. THD is less than 2.3% and VUF is less than 0.3%. For the linear loads in the power expansion mode, the load voltages are of good quality. Considering that i_n does not flow on the load side, there is no need for a too-high waveform quality of i_n. Therefore, to verify the feasibility of the proposed working mode, the simplest zero-sequence open loop is chosen. As shown in Figs. 15(a) and 16(a), I_N and f_n are still basically stabilized at 6 A and 500 Hz. Figs. 15(b) and 16(b) also show the additional capacitor voltages due to i_n. The capacitor voltages only increase by about 54 V. If f_n is larger, the additional zero-sequence voltages will be reduced. Therefore, when using the power expansion mode, I_N should be determined first based on the most important power demand and subsequently decide the appropriate f_n based on the rated voltage of the capacitors, so that the MPDR can be expanded without too high voltage stress and overly affecting the lifetime of the capacitors.

B. Experimental MPDR

Figs. 17–20 show the experimental results of the MPDR for the above four loads, respectively. The theoretical results of the nonlinear loads are derived from the simulation model with parasitic parameters. Given that it is difficult to accurately simulate the actual converter and the nonlinear loads, the errors in Fig. 17 are slightly larger. The maximum absolute errors are 25.5 W (7.1%, $U_L < 300$ V) and 53 W (4.4%, $U_L > 300$ V), respectively. In addition to the model, current sampling accuracy

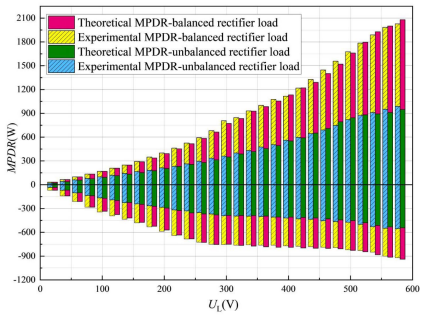

Fig. 17. Theoretical and experimental results of MPDR under the rectifier loads.

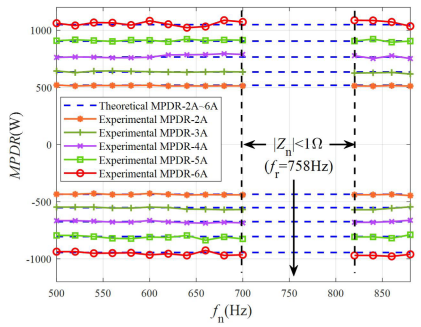

Fig. 18. Relationship between MPDR and f_n with different I_n when P_o = 600 W and U_L = 400 V.

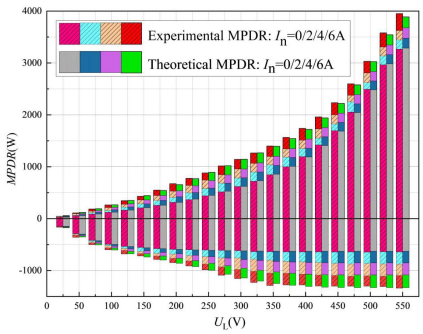

Fig. 19. Theoretical and experimental results of MPDR under the linear heavy load (P_o = 3 kW) while f_n = 500 Hz.

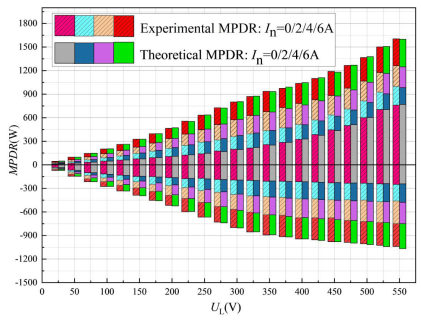

Fig. 20. Theoretical and experimental results of MPDR under the linear light load (P_o = 600 W) while f_n = 500 Hz.

and component parameter deviations are two other major sources of the errors.

Fig. 18 shows the experimental MPDR for the power expansion mode under the light-load condition. Since the MPDR in this case can be easily obtained by numerical calculation, the errors are significantly reduced. The maximum absolute error in Fig. 18 is 38.34 W(3.6%). When f_n is too close to f_r, the zero-sequence output is less than 6 V and it is difficult to guarantee the accuracy of the output. i_n contains a small resonant current, which enlarges the leg currents. So, the experimental results are slightly larger when f_n approaches f_r. The unexpected resonant current is good for increasing the MPDR but for more accurate power control, working points from 700 to 820 Hz are dropped. Sometimes, a slight reduction in f_n for increasing $|Z_n|$ is also necessary. So, f_n is set to 500 Hz in Figs. 19 and 20 while U_L changes from 25 to 550 V. The maximum absolute errors in Figs. 19 and 20 are only 27.4 W(2.5%) and 60.9 W(1.5%), respectively. When I_n increases from zero to 6 A, the experimental MPDR under the light-load condition increases from 10–760 W to 45–1603 W and from −33∼−249 W to −72∼−1040 W in two power directions, respectively. The MPDR is significantly increased for all U_L working points. For the heavy-load condition with I_n = 6 A, the experimental MPDR increases from 27∼3267 W to 45∼3950 W and from −149∼−641 W to −167∼−1340 W. Although the effect is not as significant as in the light-load condition, the expansion of the MPDR is still considerable.

V. Conclusion

The incorporation of a T-type fourth leg had greatly improved the converter's compliance with nonlinear loads. The shifted 3-D vector space had been split between components with zero-sequence and those with nonzero sequence. Through the analysis of the eight basic switching states, we defined new virtual vectors that comprehensively represented the reference vector. After that, a novel phase vector for the fourth leg was defined separately and the zero-sequence output expression had also been thoroughly examined. Under the unified phase vector magnitude expression, the phase vector increment Δu retained its usefulness for the MPDR's derivation with a precise specification. The optimal Δu for achieving the MPDR was ascertained through an expanded scaling and derivation of the power expression. This scaling process skillfully correlated port power with Δu, while the derivation process clarified Δu's influence on port power and established the principles for selecting Δu. The straightforward and logical mathematical foundation of the SDA rendered it suitable for other topologies with three-level legs, provided that there was a consistent phase vector magnitude expression and a synchronized increment Δu that maintained the integrity of the reference vector. Given the obvious limitation on MPDR from the light-load conditions, a novel power expansion mode had been proposed, which significantly increased the MPDR by supplementing leg currents without additional components. Notably, the zero-sequence current i_n had many possible waveforms other than the most common sinusoidal

form, indicating an untapped reservoir of MPDR potential within this mode. A 3-kW prototype had been used to validate the proposed methodology, and empirical findings have confirmed the viability and accuracy of the proposed strategies.

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