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# LOW-COST CMOS CAPACITIVE E. COLI BIOSENSOR FOR POINT-OF-NEED WATER QUALITY MONITORING

by

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Submitted in partial fulfillment of the requirements for the degree

Master of Engineering (Microelectronic Engineering)

in the

Department of Electrical, Electronic and Computer Engineering

Faculty of Engineering, Built Environment and Information Technology

UNIVERSITY OF PRETORIA

May 2023

# SUMMARY

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| Keywords: | Capacitive Biosensing, CMOS, E. coli, Lab-on-Chip, Water Quality Monitoring, |

Exposure to pathogenic Escherichia coli (*E. coli*) bacteria through contaminated water can cause potentially life threatening diarrhea and vomiting, and it is a useful water quality indicator. Testing for *E. coli* in point-of-need situations such as rural areas of Southern Africa can be expensive and time consuming. This is an ideal application area for low-cost point-of-care water quality monitoring devices, with a specific focus on capacitive biosensing. In this study, simulations and experiments are conducted to give guidelines on low-cost capacitive biosensing devices, and a custom integrated circuit that can be used in a low-cost capacitive biosensing device is delivered. Finite element modelling was conducted to compare the electric fields (E-fields) and capacitance from castellated and interdigitated electrodes on different feature size and footprint electrodes using different materials. This analysis included cell substitutes with electric properties similar to that of *E. coli*. The material used for the electrode features have a negligible effect on electrode performance, whereas the material used for the substrate has a small effect. The size of electrode features was found to have the biggest impact on both electric field strength and relative capacitance change in the presence of cell-like structures. A metric called size ratio was introduced to have a useful metric for comparing electrode performance across different combinations of footprint and feature size. The simulation results are used to provide clarifying

assumptions on the manner in which simulations for the design of capacitive sensing electrodes need to be conducted. Capacitance measurement of a range of low-cost and commercial electrodes was conducted using a benchtop LCR meter and 3 µm microbeads as substitutes for *E. coli* cells. It was found that the measured capacitance increases as the concentration of microbeads increases, and the low-cost electrodes seem to show a higher than expected sensitivity when compared to commercial electrodes with smaller feature sizes. Electric impedance spectroscopy experiments conducted on *E. coli* cells showed a similar performance as characterisation experiments using microbeads. These insights inform the development of guidelines that may be used to design low-cost electrodes for similar applications.

A custom integrated circuit (IC) featuring a capacitive sensing array with sub-surface electrodes was designed and delivered. This IC also includes the custom operational amplifier used in the sensing array, which was used in a low-cost capacitive biosensor prototype for point-of-need use. The low-cost device was characterised with 3 µm microbeads using a subset of the electrodes used in the LCR experiments, with comparable results achieved using the low-cost device. Lessons learned in the design of the low-cost system guide the development of a design flow for the design of point-of-need water quality monitoring devices and gives guidance on the required hardware to build such devices.

# LIST OF ABBREVIATIONS

| | |
|---|---|
| CBCM | Charge-based capacitance measurement |
| CMRR | Common Mode Rejection Ratio |
| CFC | Capacitance to Frequency Conversion |
| CFU | Colony forming unit |
| CVC | Capacitance to Voltage Conversion |
| DEP | Dielectrophoresis |
| DRC | Design Rule Check |
| E-fields | Electric fields |
| EIS | Electrical impedance spectroscopy |
| ELISA | Enzyme-linked immunosorbent assay |
| FEM | Finite element method |
| GBP | Gain-Bandwidth Product |
| IC | Integrated circuit |
| IDE | Interdigitated Electrode |
| KCL | Kirchhoff's current law |
| LB broth | Luria-Bertani broth |
| LoC | Lab-on-Chip |
| LoCMOS | Lab-on-CMOS |
| LOD | Limit of Detection |
| LVS | Layout versus schematic |
| SMU | Source Measure Unit |
| VBA | Visual Basic for Applications |
| VFC | Voltage to Frequency Conversion |
| WHO | World Health Organisation |

# TABLE OF CONTENTS

# CHAPTER 1 INTRODUCTION

## 1.1 PROBLEM STATEMENT

### 1.1.1 Context of the problem

In 2003, the World Health Organisation (WHO) established the ASSURED (Affordable, Specific, User-friendly, Rapid and robust, Equipment-free, Deliverable) criteria to guide the development of healthcare diagnostic tools in the developing world. Recent technological advances have led to the suggestion to include *Real-time connectivity* and *Ease of specimen collection* to these criteria, leading to the adjusted acronym REASSURED [1]. The rise of increasingly sensitive transducing circuitry, coupled with ubiquitous electronic devices and electronic engineering design has enabled the extraction of the electrical properties of biological materials. This has enabled more complex analyses on the properties of various types of biological matter, such as cancer antigens [2], DNA [3], or bacterial cells [4], [5]. These devices are especially important in clinical and point-of-need diagnostic applications in Southern Africa [6], with more emerging technologies and methods enabling low-cost diagnostic solutions. Escherichia coli (*E. coli*) is often used as a bacterial indicator of faecal matter [7] and is important for use in water quality monitoring. A number of strains of *E. coli* have been identified as pathogenic [8], with these strains leading to potentially fatal contamination of drinking water [9] or animal products [10]. In the context of low-cost methods to monitor water quality, therefore, it is useful to develop devices that can accurately measure *E. coli* concentrations.

### 1.1.2 Research gap

Although there exists a body of work using Lab-on-Chip (LoC) and similar devices to measure the presence of bacterial cells such as *E. coli*, there does not yet exist a device or guidelines on designing devices that achieve this goal in resource-limited settings.

The gap that will be addressed in this study is the lack of direction that designers and researchers have

when aiming to design biosensors or Lab-on-Chip (LoC) devices that comply with the REASSURED criteria set out in [1]. The potential of additive manufacturing techniques for such devices will also be discussed.

## 1.2 RESEARCH OBJECTIVE AND QUESTIONS

Array-based capacitive biosensing is uniquely suited to the study of *E. coli* [11] because it can be used to study the growth of colonies [12]. It is notable that the minimum feature size in the available CMOS process could be an important factor in the limit of detection of such a sensor [4]. With the aim of addressing the REASSURED criteria [1], a number of questions were identified for the development of a low-cost *E. coli* biosensor. These have broadly been categorised into three investigation areas: the simulation problem, the hardware problem, and the system-level problem. The first research question will be addressed on a simulation level, from which insights may be drawn to develop and evaluate a physical solution with suitable hardware to answer the second research question. The hardware-based solution and its evaluation lead naturally to the development of a system, which requires system-level definitions. These will be based on the interaction requirements between the sensing solution developed for the hardware-based problem and the required subsystems required to enable an integrated diagnostic system. Since the research questions may be generalised to multiple cell types, the questions are set up to be as general as possible, but these questions will be applied specifically to *E. coli*:

1. What assumptions may be made regarding how cells interact with one another and the electrodes and how does this affect design choices surrounding electrode geometry?
2. How do the materials and geometry of an off-chip electrode affect the accuracy of a device and its associated cost?
3. What external hardware is required besides the LoC to deliver a complete sensing system, and what trade-offs are acceptable to ensure a low-cost point-of-need biosensing device?

## 1.3 APPROACH

The procedure required to answer the questions from Section 1.2 is a linear process, with each subsequent problem relying on insights gained from investigating the preceding problem. Feedback between sections can also confirm hypotheses. All three problems identified in Section 1.2 need not necessarily be addressed simultaneously - these problem areas are structured such that they still provide research outputs which are at least theoretical in nature, but also such that they can scale and include empirical research outputs. The steps to investigate each of the three problems and their accompanying questions are set out below.

### 1.3.1 Simulation-based problem

1. Conduct finite element analyses:

   Explore the effect of different cellular and solution dielectric properties, cell sizes, electrode geometries and sizes, and cell position relative to the electrodes and other cells. Finite element analysis software packages like ANSYS are available to the University.

2. Investigate and validate the results:

   Compare and critically evaluate the simulation results obtained to published results of similar cells to verify the simulation results.

3. Identify the optimal combination of conditions for measuring a specific cell to transfer testing to a hardware platform.

### 1.3.2 Hardware-based problem

The hardware problem may be investigated with polystyrene beads as a substitute for cells. Intra-university partnerships at the University of Pretoria could potentially grant access to *E. coli* samples that can be used for measurement. If required, an application for ethical clearance will be submitted to the University of Pretoria before the commencement of any experiments. The steps for investigating the hardware problem are:

1. Design the discrete electrodes and the required interfacing to external circuitry.
2. Measure the impedance of bacterial cells or bacterial cell substitutes (polystyrene microbeads) using an appropriate impedance measurement tool, such as the LCR meter in CEFIM.
3. Design and build the front end and processing platform for the hardware system.

### 1.3.3 System-level problem

Addressing the system-level problem will require a new set of simulations and include the development of new hardware subsystems. This is due to the unique challenges posed by on-chip circuits and system design. The steps to investigating the system-level problem are:

1. Determine the appropriate cell manipulation strategy, if applicable.
2. Design and test the CMOS-based cell manipulation and measurement system.
3. Integrate the cell manipulation- and counting systems and test the functionality and performance. Critically evaluate the performance of the integrated system.

## 1.4 RESEARCH GOALS

This study aims to deliver a methodology that can be used to design capacitive biosensors for a variety of applications by verifying simulation techniques against different experimental setups. The methodology is demonstrated through the design of a low-cost capacitive biosensor prototype aimed at *E. coli* detection using a custom-designed CMOS integrated circuit. This integrated circuit also includes an array-based Lab-on-CMOS (LoCMOS) system aimed at low-concentration detection of *E. coli* from small sample volumes. The difference between LoC and LoCMOS systems is that the LoC is a system using a specialised CMOS-based device with complementary circuitry and analyte control built around it, whereas everything required for the experiment is integrated on the CMOS die in the LoCMOS case. Although integration into a device is not complete, a roadmap towards integrating the LoCMOS into a low-cost device for point-of-care applications is also developed.

## 1.5 RESEARCH CONTRIBUTION

The study aims to provide a low-cost LoC capacitive biosensor for *E. coli* measurement in a point-of-need water quality monitoring device. Material choices and design guidelines will be generated to guide the future development of similar low-cost devices for use in resource-limited settings.

## 1.6 RESEARCH OUTPUTS

A peer-reviewed international conference paper was published in the proceedings of the IEEE Africon 2021:

G. Andrews, U. Hilleringmann, and T.-H. Joubert, "The viability of a non-flow capacitive biosensing microsystem for whole cell counting", in *2021 IEEE AFRICON*, IEEE, 2021, pp. 1-6 [13].

A journal article based on this work will be submitted for publication in the IEEE Sensors journal.

Parallel work conducted using the same cell measuring methodology to monitor the growth of lead-precipitating bacterial cells led to a paper published in MDPI Sensors:

G. Andrews, O. Neveling, D.J. de Beer, E.M.N. Chirwa, H.G. Brink, T.-H. Joubert, "Non-destructive Impedance Monitoring of Bacterial Metabolic Activity Towards Inline Lead Biorecovery", *Sensors*, vol. 22, no. 18, p. 7045, 2022. [14].

## 1.7 OVERVIEW OF STUDY

This dissertation is organised as follows: Chapter 2 gives a review on *E. coli* and capacitive biosensing, outlining the current state of research for some of the most important topics relevant to this study. Chapter 3 provides a description of the experimental methodology for the simulations and experiments to be conducted. The design, layout, and simulations for the proposed LoCMOS system is presented

in Chapter 3. In Chapter 5, results from simulations and experiments proposed in Chapter 3 are presented and briefly discussed. The results from the two preceding chapters are summarised and discussed in Chapter 6. Chapter 7 draws conclusions from the results and discussions presented, and provides recommendations on the shortcomings of this work, as well as the possible future work that is available.

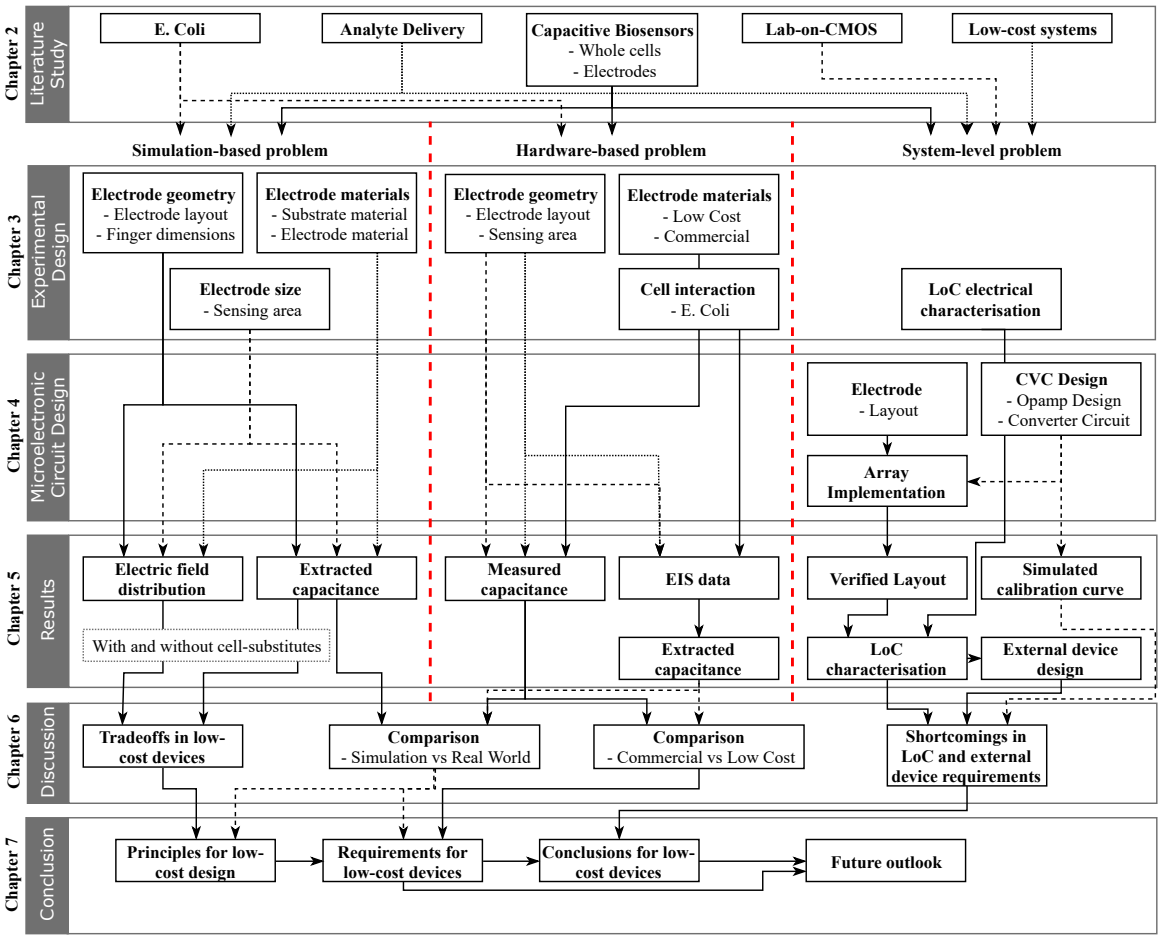



**Figure 1.1.** Overview of dissertation.

Fig. 1.1 shows a visual overview of the dissertation broken down according to chapters, sections and subsections. The blocks corresponding to each of the subsections are grouped according to the three problem areas outlined above.

# CHAPTER 2 LITERATURE STUDY

## 2.1 CHAPTER OVERVIEW

This chapter presents the literature study for this dissertation. Section 2.2 gives an overview of Escherichia coli (*E. coli*), including the motivation for studying this particular bacterium, methods currently in use to measure and quantify *E. coli*, and its electrical and physical properties. Different methods of delivering cells to the electrode for measurement are discussed in Section 2.3, with a focus on flow-based and droplet-based delivery techniques. In Section 2.4, a brief overview is given of capacitive biosensing, with a focus on bacterial-based applications. Lab-on-CMOS applications and design considerations from recent literature are outlined in Section 2.5. Section 2.6 briefly gives perspectives specifically on the use of additive manufacturing and its implications on low-cost sensing solutions.

## 2.2 ESCHERICHIA COLI

### 2.2.1 Motivation for measuring *E. coli*

One of the biggest dangers to humans and the environment, according to the WHO, is the emergence of antibiotic-resistant pathogens [15], as these pose a significant risk to humans exposed to them. Antibiotics are one of the most effective tools humanity has against bacterial pathogens and without antibiotics, exposure to some of these pathogens could prove fatal. Some strains of *E. coli* have been found to be resistant to a wide array of antibiotics [16], with food-borne strains such as O157:H7 considered some of the most dangerous strains in the developing world [10]. Infection may also occur due to dangerous strains in water sources [7], with infection from these sources potentially leading to conditions such as typhoid fever, cholera, or lethal diarrhea [8]. Concentrations of as few as 10-100 cells in food products could be enough to cause *E. coli* infection [8], [17].

According to the newest WHO reporting [18], sub-Saharan Africa leads the world in deaths due to unsafe water, sanitation, and hygiene (WASH). South Africa has a mortality rate of 13.67 per 100 000, the lowest of all our Southern African neighbours except Botswana (11.77 deaths per 100 000). *E. coli* is one of the most reliable indicator organisms for the presence of fecal matter in water because it is present in all mammalian feces but does not multiply considerably in the environment [19]. Established biochemical methods of bacterial concentration estimation such as culture counting, polymerase chain reaction (PCR), and enzyme-linked immunosorbent assays (ELISA) are slow, expensive, and unfit for analysis of samples on-site in food production facilities [17]. This has led to the development of biosensor devices capable of detecting bacterial cells quickly and accurately [12], [17], [20], with specific requirements, including sensitivity, specificity, robustness, and reproducibility [8]. Over and above the requirements for general biosensor devices, the WHO, among others [1], has identified further requirements that ensure quality sensor devices are available in point-of-care situations. The so-called REASSURED criteria aim to deliver biosensors that offer real-time connectivity, ease of use to those that do the testing, and immediate results at the point of care.

#### 2.2.1.1 Established methods of measuring *E. coli*

Quantitative PCR (qPCR) has long been the primary method used to quantify suspected *E. coli* in a prepared sample due to its high specificity and flexibility in target identification [21]. PCR works by using the fluorescence of an indicator molecule in a reaction to identify reactants by the DNA present in the sample [22].

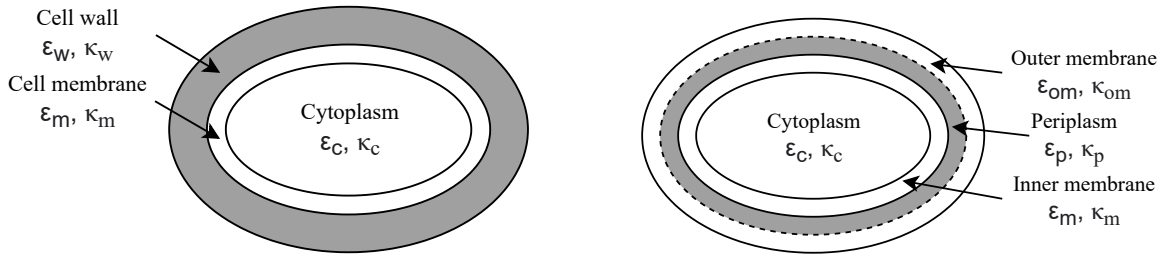
One drawback to using qPCR is its high limit of quantification of $10^3$ CFU/g, as well as requiring standardised laboratory equipment and the necessary expertise to carry out experiments. For samples with low bacterial counts, it is possible to use digital-droplet PCR (ddPCR) because a sample is split into many nanoliter droplets, with analysis done on the fraction of positive result droplets, allowing better quantification of samples with suspected low cell counts [23]. PCR-based tests can be very sensitive, which could be considered a drawback if they detect bacterial concentrations well below the infection threshold [22].

Many other established methods of quantifying *E. coli* presence rely on optical methods. For example, optical density measured at a fixed wavelength ($OD_{600}$ uses 600 nm) may be used to quantify the growth of *E. coli* colonies. The method used in [24] requires 3.5 hours to complete but could be

completed in 45 minutes at the cost of an order of magnitude of sensitivity, which makes it useful for testing samples in which high cell concentrations are suspected. $OD_{600}$ measurements, combined with measurements of the dried biomass of grown samples of *E. coli*, can also provide insights into the metabolic processes and growth rate of cells [25]. The dispersion of light caused by *E. coli* cells can be used to derive the cell morphology [26], which can be confirmed through inspection under a microscope. These kinds of quantification experiments, along with dielectric experiments performed in [27] and [28], allow for more accurate simulation models that can be used to capture the behaviour of cells. Established methods of measuring, such as biochemical testing and PCR testing, are giving way to detection methods that can deliver more specific and sensitive results in a shorter timeframe, especially if done more cost-effectively [17]. Widespread adoption and use of point-of-care diagnostic devices are likely to have the most profound effect on the use of antibiotics to combat the spread of bacterial infections in the developing world [22]. Depending on the electrical quantity being sensed, detection methods for biosensors can be divided into different classes [8]. These include voltammetric [17], [20], amperometric [29], or impedimetric [12], and within each of these classes, there are various different methods. This review focuses on impedimetric methods, which include capacitive and magnetic methods, and methods based on the impedance spectrum. Although capacitive and inductive sensing are frequency-dependent and could be considered part of spectrum-based measurements, for the purposes of this review capacitive sensing occurs at a single frequency unless otherwise specified. Methods based on impedance spectrum are also clearly specified as such. Any impedimetric method, however, requires an understanding of the electrical properties of the cells in question.

### 2.2.2 Electrical properties of *E. coli*

Before considering the electrical properties of *E. coli*, it is worth looking at the morphology of a cell, because this often informs its electrical characteristics. In studying individual *E. coli* cells, [26] found them to be approximately rod-shaped, with domed caps of the same diameter at the end of the rod. The cells studied had a mean length of approximately 2.5 µm and a mean diameter of approximately 0.7 µm, which agrees with values seen in much earlier research [27]. The interior of the cell consists of the cytoplasm, a resistive protein-filled solution containing the organelles required for cell functioning. The cytoplasm is enclosed by a cell membrane and cell wall, electrically modeled as a set of two confocal ellipsoids as seen in Fig. 2.1(a) [27]. More recent measurements use the same confocal ellipsoid model as [27] but split the cell wall into two ellipsoids corresponding to the outer membrane and the periplasmic space, as seen in Fig. 2.1(b) [28]. The periplasmic space, a 10 nm thick layer between the inner cell membrane and the outer membrane, is part of what was previously considered




**(a)** Cross section of *E. coli* cell model as proposed by [27].

**(b)** Cross section of *E. coli* cell model as proposed by [28].

**Figure 2.1.** Two different *E. coli* electrical cell models shown in cross section.

the cell wall. However, it is important to note that increasing the complexity of the cell model in this manner increases the difficulty in solving for the electrical parameters of interest. The cytoplasm has a relative permittivity of 100, slightly higher than water, and a conductivity between 0.2 and 0.4 S/m depending on the model used for curve fitting and the measurement method. Next, the cell membrane covering the cytoplasm has a specific capacitance of 0.7 μF/cm$^2$ [28].

Due to the complexity of the model used in [28], the conductivity ($\kappa$) of the outer membrane is fixed, which in turn affects the specific permittivity ($\varepsilon$): when $\kappa \approx 10^{-4}$, the outer membrane capacitance is 1.3-1.5 μF/cm$^2$, and when $\kappa \approx 10^{-3}$, the specific capacitance is 4.3 μF/cm$^2$. These values are similar to those seen in [9] for COMSOL simulations and in finite element method (FEM) analysis [11]. The permittivity of cellular media has been found to display frequency-dependent dispersions [27], which correspond to decay in permittivity as the excitation frequency increases, though this effect is not as prominent at frequencies below 1 MHz. The measured impedance of bacterial cells decreases during the logarithmic growth phase of the cells, reaching a minimum when the cells reach the stationary point in their growth curve [30]. Due to the size of the whole cell and the difficulty in ensuring bacterial specificity for *E. coli*, no product has yet been developed that can be used for real-world applications [8].

## 2.3 ANALYTE DELIVERY IN BIOSENSING

An important consideration for biosensor design is delivering the solution with the cells to the electrode to be measured. The most common methods include liquid flow-based microfluidics and droplet-based approaches with stationary fluid in contact with the electrodes. The most appropriate choice of delivery method is informed by the measurement method required, the cells being measured, and the required

throughput of the biosensor device [31]. Droplet-based approaches on CMOS devices are considered rapid prototyping techniques, and their inaccurate nature often makes them unsuitable for systems where many high-precision microchannels and wells are required [32]. For this reason, not much research is conducted on the use of non-flow methods of cell delivery.

### 2.3.1 Flow-based delivery

The most effective analyte delivery method is a microchannel with flowing liquid and electrodes embedded in or around the channel to detect a voltage pulse when a cell passes by the electrodes [31]. This voltage pulse can be used to extract the resistance change in the solution due to the presence of a cell, with higher frequency stimuli or fluorescence methods [31] delivering more detailed insights into the morphology of the cell [30]. Recent advancements in the field of flow-based microfluidic analyte delivery systems include miniaturisation [9], [33], cell immobilisation [34], and simplified sensing systems [35].

The application of COMSOL and other similar FEM simulation tools extends beyond simulating electrical properties of cells as in [11] but can also be used to determine the most effective channel geometry for *E. coli* detection [9]. It is no surprise that the most accurate channel is found to be the smallest size that allows cells to pass. Simulation and measurement results show that the channel height relative to the electrodes has a significant impact on the accuracy of the sensing system. This shortcoming may be overcome through clever electrode design that allows the analyte to be trapped on the surface of the electrode through methods like dielectrophoresis (DEP) [33].

DEP uses positive or negative electric fields to attract or repel cells using a set of electrodes [36], after which a smaller electric field can be used to measure the impedance response on the same electrodes. Implementing DEP concentrators upstream of the measurement electrodes in a microchannel [36] has also been shown to double the sensitivity of DEP-based impedance measurement [37]. The DEP technique has also been used to separate living and dead yeast cells to measure their impedimetric response [34]. Using microchannels allows a reference-based measurement technique [38] by introducing a clean solution and one spiked with *E. coli* cells to two sets of identical electrodes on an LoC simultaneously. A disperse phase method combines continuous-flow sample measurement with droplet-based measurement by splitting the sample into nanoliter aqueous droplets separated by an oil-based solution, allowing pseudo-bulk measurement of cells in small amounts at a time [35].

### 2.3.2 Droplet-based delivery

Droplet-based biosensing measures a droplet of solution with suspended cells on the surface of a set of electrodes [39]. Specifically in LoCMOS applications, droplet-based sensing relies on insulating the surface of the chip and its external connections while leaving the sensitive sensing area exposed to the solution [32]. This is especially important in cases where the topmost insulating layer of the manufactured IC is foregone to expose the final metal layer. Polydimethylsiloxane (PDMS) is often used as this insulating material, and is used as the passivation layer over the electrodes in the case of an 8x8 array of microelectrodes with an electrode pitch of 50 µm used to monitor the growth of human carcinoma cells [40].

Concentrating droplets in the correct position on the chip is important for ensuring the most accurate readings possible. In this regard, some have used a plastic ring to direct cells to the surface of the electrode array [40] or added silicon tubes to the surface of the insulating layer to create wells that achieve the same goal [12]. This latter method allowed the observation of cell migration of human ovarian cancer cells [8], [12], as well as obtaining single-cell measurement resolution [40].

Array-based sensing is nearly ubiquitous in droplet-based measurement methods, with the sensing array used in [5] accurately used to determine *E. coli* concentrations correlated to established optical density measurements. Epoxy is often used to protect wire bonds of packaged ICs [4], [12], since the liquid of the droplet may spread and affect the electrical performance of the rest of the chip. This is also used in conjunction with measuring setups that do not necessarily require additional insulating layers on the IC surface [4], [5]. Besides LoC applications, in situ droplet-based relative impedance change was measured with 1 mL samples to monitor the growth of *E. coli* bacteria in milk [10].

## 2.4 CAPACITIVE BIOSENSORS

Within the subset of impedimetric biosensing methods, the focus for this review is limited mostly to capacitive biosensing and electrical impedance spectroscopy (EIS), with sporadic mention of novel or important findings involving other methods where relevant. One of the first and biggest challenges facing capacitive biosensors is the interface between the electrode and the solution the analyte is suspended in [41]. When conducting any impedance-based measurements, some charge has to be applied to the electrode, which attracts charged ions in the solution to the surface of the electrode. This displaces oppositely charged ions, creating a double layer of ions called the electrical double layer. The charge built up on either side of this layer causes the double layer capacitance, which is independent of

ionic concentration in the solution [41]. It is important to note that the capacitance of the double layer decreases when the excitation frequency increases, motivating the use of non-DC excitation signals to bypass this effect [9] or even using EIS to quantify the size of the double layer capacitance [41]. In some instances, it is possible to use the effect of the double layer capacitance as measurement: the presence of *E. coli* in milk samples increase the double layer capacitance after many hours, which can be measured as a relative change in EIS observable at 10 Hz [10]. Although the complex impedance is useful to measure, the capacitance alone is often easier to measure since only the reactive part of the impedance is measured [39].

The capacitance measured by a biosensor is rarely interpreted directly as capacitance - it is usually converted to a voltage in capacitance-to-voltage conversion (CVC) or a frequency in capacitance-to-frequency conversion (CFC) [32]. Capacitive biosensing, regardless of the analyte being sensed, can be completed in differential-mode using a reference capacitance [42], [43] or reference less mode [4]. One of the main advantages of using differential sensing methods is the greater sensitivity these provide since these sensors measure the difference in capacitance between a measured capacitance and a reference capacitance.

One area where differential sensing is often not preferred is array-based LoC applications [4], [5], where chip space could be at a premium. In differential CVC, the sensing and reference electrodes are charged and discharged [43], redistributing charge between them and using an appropriate amplifier to amplify the difference in capacitance which can only be caused by the presence of the analyte [38], [32]. This principle is used in charge-based capacitance measurement (CBCM) [39] by connecting the sensing and reference electrodes in parallel with a pair of switches that control the current through a set of current sources [44]. Using current mirrors allows the sensed current and the reference current to be subtracted from one another, which is then amplified as the measured capacitance. The same principle may allow the difference in currents to flow into a capacitor, effectively integrating this current and transforming it into a voltage [38]. For differential measurement, it is possible to introduce averaging before or after subtracting the reference and sensed signals, depending on the requirement of the biosensor [32], [45].

In reference-less CVC, charge redistribution between capacitors still has to occur, which often results in simply using a capacitor with a fixed, known value in an integrator- or charge-sharing circuit. If the biosensor is an array-based implementation, a clever design of the driving clocks that control a pixel

can be used to deposit the charge from the electrode onto the fixed-value capacitor in the cell, which then holds the voltage at the output of the cell at a fixed level by controlling the gate voltage of an NMOS current source [4]. The current output for all the cells in a column can then be amplified with a dedicated, specially designed column amplifier. Converting the measured capacitance to frequency is advantageous because this is more immune to noise than voltage-output sensors, but these sensors are dependent on parasitic capacitances [32], making them difficult to design. The first type of CFC circuit consists of any appropriate CVC circuit, with a comparator connected to its output.

Once the measured voltage reaches the threshold voltage of the comparator, a pulse is created, triggering the charge from the CVC circuit to reset [42]. The second, more direct method of CFC is simply using a ring oscillator consisting of an uneven number of inverter logic gates to create an oscillator. Connecting the sensing electrode between two of the stages of the oscillator [12] allows the frequency of the oscillator to change in proportion to the change of the sensed capacitance. Using the sensor capacitance as part of the reactive circuit elements in the LC tank of a free running oscillator allows the change in capacitance to affect the free-running frequency of the oscillator [5]. It is then possible to relate the relative shift in the frequency to a change in the sensed capacitance [32].

### 2.4.1 Whole Cell Detection

In whole-cell detection, EIS methods are preferred over voltammetric or amperometric methods due to the spectral information that can be gathered [31], which allows for much greater sensitivity and specificity [4]. Using single-frequency impedimetric methods vastly simplifies the circuitry required for a measurement at the cost of detailed cellular information obtained through spectrum-based methods, though careful consideration of the parameters of interest may make such a simplification worthwhile. These methods are also often preferred because they are label-free and can be non-invasive [39], and impedance-based sensing allows the extraction of a number of cell characteristics such as cell size [9], electric characteristics [28], cell viability [10], cell proliferation [12], [40], and more [46]. Although it is useful to use EIS methods for characterising the electrical response of cells, many applications only require the response at a single frequency to determine cell distribution or concentration.

FEM may be used to investigate the electrical fields and expected values to understand where and how to optimise the design of capacitive biosensors for whole-cell detection [11]. The simulation in [11] assumes liquid flow conditions and a channel geometry that limits cells that are smaller than 2.5

µm. The *E. coli* cell is modelled as a single ellipsoid with $\varepsilon_r = 60$ and $\kappa = 0.5$ S/m, significantly simplifying the electrical model as used in [27] and [28]. It is worth noting that the simulation is not aimed at detecting single cells, but bulk detection of many cells, so simplifying the electrical properties for simulation is not unreasonable. Using a single set of electrodes shows a decrease in capacitance as the number of cells increases.

Similar simulation-based research has also been done on whole-cell detection of cancer cells [13]. Although research into the physical and electrical properties of bacterial cells is important for understanding the cells themselves [28], one of the research areas that gets more attention is studying the growth of bacteria [38]. A CBCM circuit used on-chip allows differential measurement of two electrodes: one electrode measuring only the medium cells are suspended in, and the other measuring the presence of *E. coli* cells. Using two separate microchannels connected to each of these electrodes allows proper separation of the two analytes while ensuring concurrent exposure to both the reference and measurement electrodes.

Whole-cell detection is also used outside the study of bacterial cells, such as the study of cell proliferation of human cancerous cells using an array of sensors [12]. A ring-oscillator-based CFC method implemented in an LoC array can give high-resolution measurements of cell proliferation without the need for components that require much on-chip space [12]. CBCM used in an 8x8 array has also demonstrated usefulness in monitoring the cell growth of human lung cancer cells [40] over 30 hours. The strength of such an array implementation is its ability to map growth over the observed time period, displaying the change in cell concentration on the array surface, with these array-based sensing methods also decreasing the required sample volume and detection time [31]. With electrode areas of 50x50 µm, this array can detect a single cancer cell per electrode. Although not used to map out cellular concentration over the electrode area, implementing transmission line crossings on-chip allows capacitive detection of *E. coli* cells between 1-3 GHz [47]. Using the presence of bacteria to change the frequency of oscillators, this method can detect concentrations as low as $10^3$ CFU/mL. By using the appropriate bio-functionalisation, this method also shows selectivity for *E. coli* cells. Array-based implementations are most important for studying cell growth and proliferation [38], [40], [47], but careful design of the electrodes is paramount to ensure adequate spatial resolution for the measurement of low concentrations of cells [12].

### 2.4.2 Electrodes

Bacteria at the surface of interdigitated electrodes (IDEs) degenerate the effective area of the electrode, affecting the interaction between the electrode surface and the suspending medium [30], which can be measured as an impedance change at frequencies as low as 10 Hz [10]. When studying the effect of electrodes in capacitive biosensing, the most natural place to start is the assumption that the electrodes act like a parallel-plate capacitor [11].

For applications where microchannels are used, the parallel plate assumption is often valid if the electrodes are embedded in the microchannel on opposite sides [48]. When using the parallel plate assumption, [11] gives the capacitance as

$$C_{\parallel} = \frac{\varepsilon_r \varepsilon_0 A}{d}, \tag{2.1}$$

with $\varepsilon_0$ the vacuum permittivity, $\varepsilon_r$ the permittivity of the dielectric between the plates (this is the solution the cells are suspended in, typically water or a saline solution), $A$ the area of the electrodes, and $d$ the distance between them, typically the width or height of the channel. Depending on the application and measurement method, complex capacitance may also be extracted from a measurement [41]. Capacitive biosensors can use parallel-plate or coplanar electrodes, with the latter being easier to manufacture at the cost of non-uniform electrical fields [49].

Coplanar electrode setups also allow for more intricate shapes, such as interdigitated [2], castellated [50], and serpentine [51], which have allowed the use of cell-manipulation techniques like DEP [31], [50]. Using more advanced electrode geometries affects the capacitance between plates and the nature of the electrical fields between them [30]. Interdigitated electrodes are constructed by using alternating digits corresponding to each plate of a conventional capacitor [2], with the formula to calculate the capacitance given by [52] as

$$C_{IDE} = \varepsilon_r \varepsilon_0 \frac{\eta l t}{d}, \tag{2.2}$$

with $\eta$ the number of IDE fingers, $l$, $t$, and $d$ the length, thickness, and distance respectively between consecutive fingers. If the assumption is made that the electrodes are identical, the total impedance between the two sets of interdigitated fingers is simply the sum of the impedance between consecutive digits [52].

One of the main advantages of using IDEs and their derivatives is the fact that these electrode topologies provide greater surface area than a conventional solid electrode [2], which in-

creases sensitivity [53]. Increasing the number of fingers on the set of IDEs increases the electric field magnitude between them, as does decreasing the width of fingers or the gap between them [53], as extrapolated from (2.2). The electric field over an IDE is mostly uniform, with the strongest fields seen at the corners of the electrodes closest to another another IDE corner, and decreasing further away from the surface of the electrode [13]. The two IDE derivations studied both use the IDE as the foundation and then implement a method to increase the interaction between consecutive fingers, further increasing the effective area between the electrodes. With castellated electrodes, sub-fingers are added to the fingers seen in the IDE case to increase the electrical field gradient seen between sets of fingers [50]. Similarly, the improvement seen in [51] uses a combination of conventional IDE and a meandering structure to create a serpentine electrode. This results in higher capacitance between the electrodes than seen in a conventional IDE with identical geometrical proportions.

Both of these cases occur at an increase in the complexity required to manufacture their electrodes, which affects their manufacturing cost [51]. With a set of interdigitated electrodes featuring a finger width and spacing of 8 µm, [10] demonstrated a detection limit of 7 cells/mL. By adding a layer of gold nanoparticles to the surface of a gold electrode on a silicon substrate, the sensitivity of a set of interdigitated electrodes can be increased significantly to measure cancerous cells [2].

These electrode geometries translate well to LoCMOS applications, where the electrodes are simply manufactured from the topmost metal layer of the IC [4], [31], with array-based versions enjoying particular attention due to the ease with which such an array can be scaled. An array of 1488 individual sensors with dimensions of 50x100 µm each are sufficient to distinguish between living and dead *E. coli* cells by using an LC resonator architecture [5], and growth of human carcinoma cells was monitored using 50x50 µm electrodes in an 8x8 array [40].

## 2.5 LAB-ON-CHIP

Conventional benchtop impedance sensors are limited in their available inputs, limiting the number of electrodes that can be used. This problem allows the development of dedicated on-chip systems for a nearly arbitrary number or arrangement of electrodes [39]. In most cases, the electrodes themselves may be manufactured using the topmost metal layer of the CMOS manufacturing process [4], [5], [40]. CMOS technology has long been considered the technology of choice for most LoC devices due to the small footprint CMOS circuits require [44], as well as the low cost, power con-

sumption, and noise. CMOS technology for use in life sciences also allows the designer high resolution and adaptive sensitivity, making it suitable for a wide range of sensing applications [43].

The sensing applications of LoCs are not restricted to the capacitive biosensors already discussed [4], [5], [38], but also in fluorescence [54], and magnetic [45] measurements. Since only the reactive part of the impedance is measured in capacitive biosensors and the resistance can be ignored, this circuitry generally requires less space than would be necessary if the complex impedance is to be measured [39].

One of the most useful features of most capacitive conversion techniques implemented in CMOS technology is that they are particularly simple to digitize [55], further reducing the requirement for large and expensive chip real estate.

The importance and prevalence of array-based sensing techniques in LoC systems have been demonstrated [12], [40], but these techniques introduce their own trade-offs and design challenges that need to be taken into account for a biosensor system. Their low complexity and high precision make them ideal for applications that require high measurement throughput [32]. One method to shrink the size of the pixels in the array is to use minimal circuitry in the pixel itself, using only the required circuitry to store charge. Sensing of this charge can then be implemented outside the array [4], which also allows the same set of amplifiers to be used for all the sensing pixels in a column.

For the high-frequency application seen in [5], using an inductive coil for the resonator circuit requires more real estate than active circuitry. The irregularly shaped footprint of the resulting sensing pixel requires a unique approach to the layout of the sensing array - in this case, a houndstooth pattern is used. Controlling the location of the droplet is a demanding problem, but controlling the location of the cells in the droplet is one of the biggest challenges that face any array-based implementation. To that end, cell manipulation techniques are often used in conjunction with array-based systems to increase their sensitivity and accuracy [34].

With the opaque substrate that LoC systems require, visual validation of cell counts relies on reflective microscopy [12], which limits the clarity and quality of images that can be taken to count cells. This limits the reliability of calibration curves drawn from these validations. The calibration of CMOS-based circuits is paramount to ensure continued resilience to environmental changes, parasitics, and remnants

of previous experiments on the electrode, and is one of the most difficult problems to address in LoC devices [44]. Sensing circuitry may be designed such that calibration would not be necessary [44], or a referenced sensing architecture may be considered [38], [45] to remove common-mode offsets or effects that would influence the measurement of the reference and measurement electrodes. A number of methods are available to achieve this calibration, including the use of a calibration curve obtained from measured data of cell position relative to the electrodes [12], or implementing a large on-chip capacitance as a baseline to measure against [4]. The major drawback to the latter approach is that such a chip would be specific to an expected application, and could not be used for general capacitive LoC measurements.

Although electrochemical biosensors implemented on-chip are well developed specifically for *E. coli* detection, many still require the use of specific bioreceptors to prevent non-target molecules from interfering with the sensed signals [8]. With lower power consumption and significantly lower costs than conventional benchtop systems [39], LoC systems are a natural choice for the future of biosensor systems, especially if these are to be deployed in point-of-need settings.

Work in LoC systems is overcoming several biological, chemical, and technical shortcomings of established measuring methods, and holds a promising future for clinical applications and bacterial identification [22].

## 2.6 ADDITIVE MANUFACTURING AND LOW COST SYSTEMS IN BIOSENSING

There is potential to address all of the REASSURED criteria by leveraging low-cost manufacturing and design methods such as printed electronics and additive manufacturing [6], lowering the barrier to entry and enabling the rapid prototyping and deployment of biosensor devices at point-of-need locations [56]. Printing electrodes for electrochemical applications using conductive materials allows rapid prototyping of different designs and reduces the lead time and cost of manufacturing [57]. Additive manufacturing also allows electrodes to be printed on non-conventional flexible substrates [58].

Recent research in the field of additive manufacturing for biosensors is often aimed at manufacturing the housing for interfacing commercial electrodes with a sensor platform [59]. This concept can be expanded by using additive manufacturing techniques for microfluidic analyte manipulation, typically in the form of microchannels that can mix, separate, or otherwise deliver the analyte to the electrodes [60].

Additive manufacturing methods also allow the printing of lower-cost components, such as a peristaltic micropump [61] for a microfluidic-based system, or the electrodes for a capacitive sensor [48]. Recent research into approaches that aim to lower the cost of any kind of biosensor device is sparse, often involving prototype suggestions that use simpler electrode geometries and cheaper materials as interface with the analyte while still requiring commercial capacitive sensing methods [62].

Impedance-based biosensor devices are more suited to low-cost applications than optical methods due to the inherent need for high performance, expensive equipment in the latter case [30]. Combining clever use of lithography techniques with lower-cost materials, [36] demonstrates a system that uses DEP in a microchannel to focus *E. coli* cells such that a cheap camera could be viable as an electro-optical sensor. This system is combined with specialist image processing software to extract cell concentrations, so it is not necessarily viable for point-of-need applications.

## 2.7 FINAL REMARKS

Designing accurate biosensors for bacteria detection is invaluable in monitoring the quality of water, especially in resource-limited areas like Sub-Saharan Africa.

The dangers of E. coli exposure make it an ideal bacterium to investigate the requirements for point-of-need biosensor devices. Although plentiful quality research exists on the electrical properties of single cells, not much work has been done on population average data for higher cell counts. This phenomenon informs the direction taken in designing application-specific sensors and systems for flow-based microfluidic systems, which include their own design difficulties and trade-offs. Impedance-based sensing, and especially capacitive sensing, is suited to bacterial biosensing applications due to its non-reliance on expensive and highly specialised measuring equipment. The electrodes in a capacitive biosensor system require careful design, with significant work available regarding different topologies and their effect on cellular manipulation and measurement results.

When looking at biosensor systems, LoC applications cannot be ignored, and the potential for highly accurate LoC systems cannot be overstated. There is no shortage of capacitive LoCMOS circuit design literature, but there is limited consideration given to requirements that can make such a system robust enough for use outside a typical laboratory setting.

The potential of additive manufacturing and low-cost materials was also briefly discussed, but since

these are emergent technologies the research has to date been focused on manufacturing methods rather than applications. This study aims to address some of these shortcomings by looking at available resources and providing a framework for biosensor designers to design sensing systems for low-cost, point-of-need applications.

# CHAPTER 3 EXPERIMENTAL DESIGN

## 3.1 CHAPTER OVERVIEW

This chapter provides an overview of the experiments and tests designed to understand the potential of a low-cost capacitive biosensor device, focusing particularly on using components on the packaged integrated circuit designed in Chapter 4 for such a device. First, the procedure and parameters of interest for the simulation-based problem is outlined in Section 3.2, including geometry and sizes of electrodes and materials of electrodes.

Next, Section 3.3 details the experimental procedure followed for *E. coli* experiments using a commercial potentiostat, as well as the experiments conducted using a low-cost device. The design of this low-cost device is presented in Chapter 4, as well as the design of a custom CMOS operational amplifier for use in the CVC sensing array. Finally, the procedure for characterising the electrical performance of the operational amplifier is outlined in Section 3.4.

## 3.2 SIMULATION

Using FEM-based simulations for investigating the performance of electrodes for various parameter changes has a number of benefits. By validating simulation data against measured data, the use of such simulations may be expanded for designing electrodes for capacitive biosensors. Further, by providing a methodology for studying the performance of different electrodes, further avenues are opened into this field to improve understanding of the electrical performance of electrodes for capacitive sensors and biosensors.

Simulations planned for this investigation are conducted in CST-MWS. To investigate the effect of changes in various parameters on capacitance, an electrode is modelled in CST Microwave Studio. First, a block is placed with its corner at the origin, and its length, width, and height are parameterised

with variables. The material assigned to this block is FR4, a popular substrate for printed circuit boards (PCBs) with electric permittivity $\varepsilon = 4.3$. Using the origin of the modeller as the corner of the model allows for a fixed reference point for the addition of all subsequent modelled blocks, but this means that any computational optimisations which may rely on symmetry cannot be used because the 3D model is not symmetric about any axis through the origin. The substrate is 100 µm bigger in the $x$ and $y$ direction than the electrode area, which is parameterised.

For all simulations of low-cost electrodes, the thickness of the FR4 substrate is kept to 1.5 mm, and the thickness of electrodes are kept to 5 µm to approximate what can be achieved with appropriate manufacturing methods.

### 3.2.1 Electrode geometry

Microsoft Visual Basic for Applications (VBA) scripts can be used to set up tests and generate shapes in CST. A VBA script was set up to automatically generate the fingers and subfingers of square interdigitated and castellated electrodes as seen in Fig. 3.1. This script uses the dimensions of the electrode and the width of the fingers on either side to generate the required shape. The pitch for the fingers in an IDE is defined by

$$w_{IDE} = w_{finger} + w_{spacing} \,, \tag{3.1}$$

with $w_{finger}$ the width of one finger and $w_{spacing}$ the width of the spaces between fingers. For the purposes of this investigation, both dimensions are kept the same for all widths investigated. Castellated electrodes differ from IDEs by the addition of smaller sub-fingers perpendicular to the fingers in an IDE. This structure may be nested multiple times, but for this investigation, only one set of subfingers is added to each finger for the castellated electrode. Using subfingers allows for local maximum electric fields at the corners of the sub-fingers. For this investigation, subfingers protrude only one finger width from the side of the main finger.

The pitch for the castellated electrode, therefore, is calculated as

$$w_{castellated} = 2w_{finger} + w_{spacing}, \tag{3.2}$$

which allows for alternating sets of subfingers on subsequent electrode fingers. The number of fingers in both the IDE and the castellated electrode is calculated as

$$\eta_{fingers} = \frac{w_{footprint}}{w_{(electrode)}}, \tag{3.3}$$

where $w_{(electrode)}$ refers to the pitch calculated in (3.1) or (3.2). Once the number of fingers for either electrode topology has been calculated, the cubic shapes used for fingers can be placed using the pitch in (3.1) or (3.2) in the $y$ direction to form the electrode.

The main connecting bar is placed on either side just inside the electrode area to connect alternating fingers to the opposite side. The length of fingers, therefore, is simply calculated as

$$l_{fingers} = w_{electrode} - w_{finger} - w_{spacing}, \tag{3.4}$$

with each alternating finger placed with an offset in the $x$ direction of either 0 or $w_{electrode} + w_{spacing}$.

Odd-numbered fingers are connected at the left (closest to the origin of the modeller), while even-numbered fingers are connected at the right-hand side. For the castellated electrode, sub-fingers need to be added perpendicularly to each finger, with an offset such that consecutive fingers have sub-fingers that are only adjacent to sub-fingers associated with a consecutive finger. This is achieved by implementing an alternating offset for the sub-fingers of consecutive fingers.

The pitch for these alternating sets of sub-fingers is also given by (3.2), with the number of sub-fingers used per finger calculated as

$$\eta_{sub} = \frac{l_{fingers}}{w_{castellated}}. \tag{3.5}$$

Main fingers are added in the $y$ direction and sub-fingers are added in the $x$ direction. For sub-fingers associated with odd-numbered fingers, the offset in the x-direction is simply half the width of a finger ($w_{finger}/2$), while the offset for sub-fingers associated with even-numbered fingers is $-1.5w_{finger}$. The width of sub-fingers in the $y$ direction, as measured from the centre of each finger is $-1.5w_{finger}$. Fig. 3.1 shows a comparison of the two types of electrodes with the same geometric dimensions.

In VBA, a simple command is used to generate shapes. Once the origin and size of fingers and sub-fingers have been determined, these are used as arguments in the *create shape* command to create the electrodes. Fig. 3.2 shows a flow diagram of the VBA script used to generate electrodes for both the interdigitated and castellated geometries, with the additional blocks in blue only required for the castellated case. Once blocks have been generated and grouped by the script, all the fingers for one side are selected, and a boolean union operation is performed so the solver considers them as a single

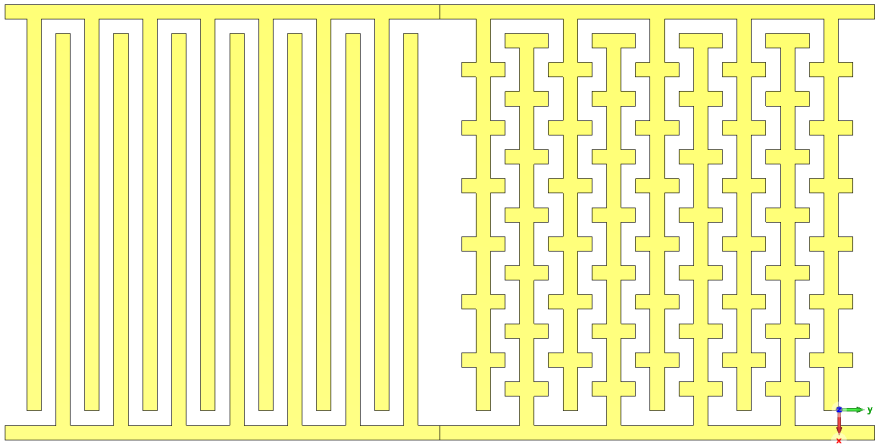



**Figure 3.1.** Comparison of 3x3 mm IDE (left) and castellated electrode (right) with 100 µm finger width and spacing, as generated in CST. Note that *x* is to the bottom of the page and *y* is to the right.

shape. This is done to lower the simulation time, as the solver does not have to check the properties of these overlapping features when generating the mesh.

Within the domain of IDEs and castellated electrodes, three geometric features will be the main focus of study: the total area of the electrode, the size of the electrode features (finger widths and spacing), and the materials the electrodes are made of.

Commercial interdigitated electrodes [63] are available in a variety of configurations from Dropsens, with IDEs manufactured on plastic substrates featuring finger widths down to 100 or 50 µm. The same manufacturer sells electrodes on a glass substrate with finger widths down to 10 or 5 µm at a significant increase in price. For investigating the effect of changing the width of fingers and sub-fingers on low-cost electrodes, three widths are therefore considered: 100, 50, and 25 µm.

Further, it is clear from [52] that increasing the number of fingers in an IDE will increase the overall capacitance. An increase in the capacitance does not translate to an increase in the sensitivity or performance of the sensor [64], so the finger widths considered for the electrodes are repeated with different total electrode areas: 1x1 $mm^2$, 3x3 $mm^2$, and 6x6 $mm^2$. A summary of the electrode sizes investigated can be seen in Table 5.1. The frequency-domain solver then solves Maxwell's equations to give the E-field distribution and capacitance matrix for the different combinations of variables considered. Simulating electrodes used in an LoC application is another important step in verifying

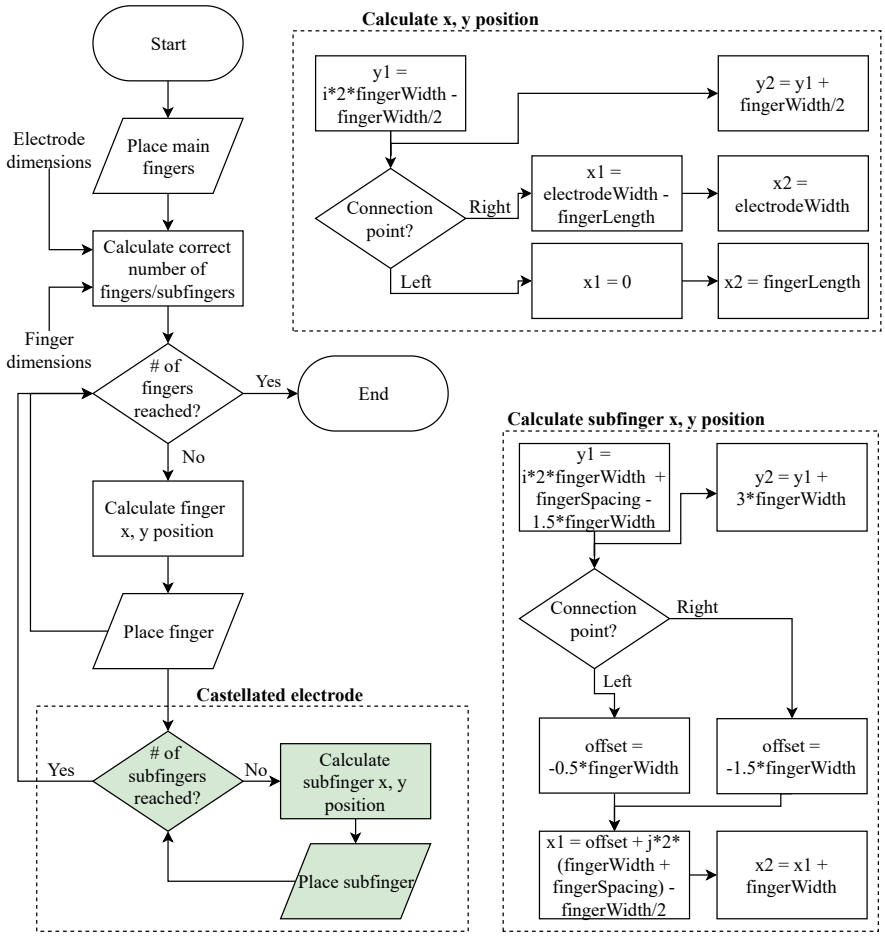



**Figure 3.2.** Software flow diagram of the VBA script used to generate interdigitated and castellated electrodes.

their usefulness in low-cost devices. As such, the comparisons conducted for low-cost electrodes are repeated for a smaller area and feature-size electrodes appropriate to LoC implementation.

The comparison between IDE and castellated electrodes for LoCMOS implementation is repeated on two electrode setups:

1. a single electrode with an area 0.25 $mm^2$ and finger widths of 25 µm,
2. an electrode aimed at array-based electrode implementations with an area of 25 $\mu m^2$ and finger widths of 0.6 µm.

The 0.6 µm in the latter case is chosen as it is the minimum width of the topmost metal layer used in the LoCMOS design (see Chapter 4).

Further, the construction of this set of electrodes differs from the low-cost version by using the layer thicknesses defined for a 0.35 µm CMOS process. Inter-metal dielectric layers are 1 µm, which will act as both a substrate below and an insulating layer on top of the electrode, while the relevant metal layer is 640 nm thick [65]. To apply the electric fields to the electrodes, a set of 25 µm wide perfect electrical conductor (PEC) fingers are added at either side of the main fingers. The PEC fingers are also 5 µm thick and as long as the main fingers, abutting the latter along its full length. Contact between the PEC fingers and the main connecting fingers allows current to flow to the blocks used for the electrode. The contact between the PEC fingers and the main connecting fingers is required, as a potential in CST can only be applied to PEC surfaces. Contact between PEC and other electrically conductive materials then allows electric fields to be generated between fingers. The PEC fingers on either side of the electrode correspond to the main connecting finger at the top and bottom of the electrodes shown in Fig. 3.1.

### 3.2.2 Electrode materials

When creating the electrodes, the specified material is gold. However, to investigate the performance of potentially lower-cost materials for electrodes, pure copper and silver are also considered. The electrical properties for the three materials in the CST library are listed as permittivity $\varepsilon = 1$ for all three, and conductivity, $\sigma$, of $4.56 \times 10^7$ , $5.96 \times 10^7$ , and $6.3 \times 10^7$ S/m, respectively. With conductivities as close to one another as these, differences between runs are likely to be small.

Once electrodes have been generated and the union operation has been done, the material of the combined electrode shape may be changed. This fact is used to eliminate variation in capacitance due to cell positioning by running comparative electrode geometries with identical cell counts and merely changing electrode material between consecutive simulation runs.

Although a number of substrates exist for manufacturing low-cost electrodes through methods such as screen printing and additive manufacturing, the focus of this investigation is mainly on the effect of changing geometry. As such, the main substrate considered for simulation is FR4. One comparison is made between a substrate made from FR4 and a paper substrate with a smaller thickness of 500 µm and a different dielectric constant ($\varepsilon = 2.31$). A fixed geometry is used for both, and LoCMOS electrodes are investigated separately.

The LoCMOS simulations use $SiO_2$ as the substrate and inter-metal dielectric used as an isolating

material over the surface of the electrodes. The metal used for the electrodes is aluminium. The droplet of water is added on top of the isolating layer in the same manner as with the low-cost electrode simulations. A summary of the materials used for simulations can be seen in Table 5.1.

### 3.2.3 Cell interactions

On the surface of the electrode, a 2 mm thick block of water ($\varepsilon = 78$, and $\sigma = 0.5$ S/m) with the same area as the substrate is used as the bulk solution which cells are suspended in. It is known that the electric fields generated by the electrodes decay significantly in the first 40 µm from the electrode [13]. Placing cells a considerable distance away from the surface of the electrode, therefore, results in inaccurate estimations of the performance of electrodes. In this case, the solution is to limit the spread of the cells to the first 100 µm from the surface of the electrode, since this captures the detection range of the electrode. The performance of the low-cost electrodes in the presence of increased cell counts is assessed by considering the same cell concentration per electrode rather than the cell count.

From the limit imposed in the $z$ direction, the area of the electrode is used to calculate the number of cells per cubic mm. Cell concentration for the low-cost electrodes is assessed at 0-50 cells per mm$^3$, in intervals of 10 cells per mm$^3$ and with the three electrode areas considered, Table 3.1 shows the actual number of cells that have to be generated.

**Table 3.1.** Actual cell counts to study changing cell concentrations for different sizes of low-cost electrodes.

| Cell concentration (cells/mm$^3$) | Number of cells for different electrode areas | | |
|---|---|---|---|
| | 1x1 mm$^2$ | 3x3 mm$^2$ | 6x6 mm$^2$ |
| 10 | 1 | 9 | 36 |
| 20 | 2 | 18 | 72 |
| 30 | 3 | 27 | 108 |
| 40 | 4 | 36 | 144 |
| 50 | 5 | 45 | 180 |

Although the electrical model of an *E. coli* cell contains multiple layers, this investigation adopts the single solid body method used in [11], with a cell approximated by a cylinder with one set of electrical properties. Regular positioning of cell-substitute models shown promising results in the

study of increased cell counts [11], [13]. For this study, cells are placed randomly in the $x$, $y$, and $z$ directions within the footprint of the electrode and 100 µm of its surface.

The random direction and position are achieved by a VBA script that generates uniformly random numbers for various parameters: one for the spread in the $x$, $y$, and $z$ directions respectively, and one for the orientation of the cylindrical rods. These random numbers are generated as a value between 0 and 1. For the cell position, this number is scaled to the area of the electrode and the height limit imposed. The value of the fourth random number is checked against three thresholds. First, if the value of the random number is less than 0.33, the cylinder is oriented in the $x$ direction. Second, if the value of the random number is between 0.33 and 0.66, the cylinder is oriented in the $y$ direction. And third, if the value of the random number is greater than 0.66, the cylinder is oriented in the $z$-direction. This ensures the orientation and position of cells are uniformly distributed.

A cylindrical rod, 0.7 µm in diameter and 2.6 µm in length, and with permittivity $\varepsilon = 60$ and conductivity $\sigma = 0.5$ S/m, is placed at the determined location and orientation. Two simplifications are made to reduce computational complexity. First, only a cylinder is placed with no spherical caps at either end, and second, the cylinder in question comprises 50 segments rather than a perfect cylinder. The former resolves the majority of material intersections between two spheres and a cylinder for each cell placed, and the reduced sections of the cylinder make it easier for mesh generation around a less curved surface. This results in reduced computational complexity for the FEM simulations. Since the focus of this investigation is aimed at the interaction of a large number of cells in a large volume of suspended liquid, this is an acceptable trade-off.

### 3.2.4 Solver setup

The solver used for this investigation is a low-frequency solver that solves Maxwell's equations in the frequency domain [66]. This allows the visualisation of the electric fields at low MHz frequencies and below, while at the same time extracting an admittance matrix that is used to derive a capacitance matrix.

The low-frequency solver can solve electroquasistatic or magnetoquasistatic equations - relating to electric and magnetic fields, respectively. Both are approximations of Maxwell's general equations that can be used when

$$\frac{L}{c} \ll \tau \,, \tag{3.6}$$

where $L$ is the length of the feature under consideration, $c$ is the speed of the electromagnetic wave propagating through the medium at the speed of light, and $\tau$ is the characteristic time for the sinusoid to reach steady state [67]. The characteristic time $\tau$ of the sinusoid is the inverse of its angular frequency $\omega$, such that:

$$\tau = \frac{1}{\omega} = \frac{1}{2\pi f}. \tag{3.7}$$

Running the simulations up to a frequency of 1 MHz, it was determined that the electroquasistatic setting is adequate for the purposes of this investigation. This electric field solver requires an electric source that can only be applied to PEC, so a 5 V sinusoidal source is applied to a PEC finger on one side of the electrode, and a fixed 0 V is applied to the other side of the electrode.

For FEM simulations, a mesh needs to be generated that is used to solve Maxwell's equation on sections of the 3D model. Global mesh settings are set to 10 per maximum box's edge in the model, and 3 per edge in the background. The background starts at 100 µm in every direction from the outside surface of the substrate and droplet. The solver then automatically refines the mesh further to increase the accuracy around regions that contain discontinuities.

With the mesh established, the electroquasistatic solver solves Maxwell's equations in the frequency domain at one point per decade from 1 kHz to 1 MHz. Table 3.2 summarises the parameters used for the setup of the CST simulations. Once a simulation run is complete, the maximum electric field strength over the model and the capacitance matrix is extracted.

**Table 3.2.** CST electroquasistatic solver setup.

| Parameter | Value | Unit |
|---|---|---|
| Minimum frequency | 1 | kHz |
| Maximum frequency | 1 | MHz |
| Excitation amplitude | 5 | V |
| Minimum cell size | 10 | cells/max model box edge |

## 3.3 MEASUREMENT

Fig. 3.3 shows all the electrodes used for the capacitance experiments, with the leftmost three electrodes used in experiments with *E. coli*, and the others included in experiments using the low-cost biosensing device. The electrode interface connector lines have the same pitch, simplifying the design of a custom holder that can be used for all the electrodes.

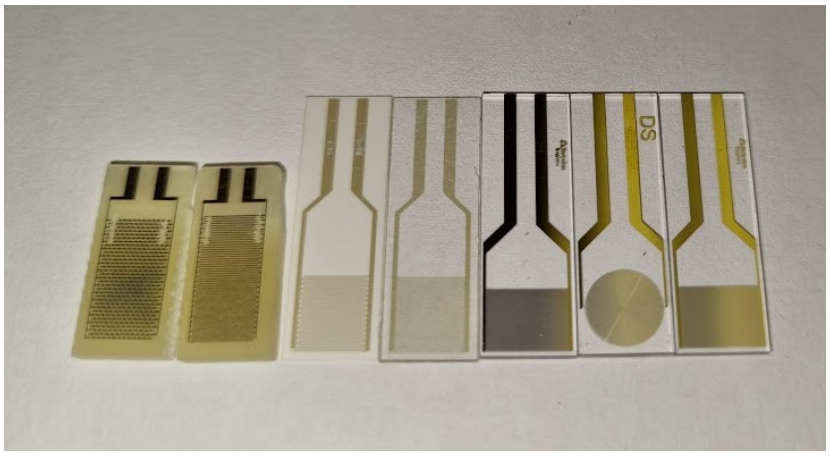



**Figure 3.3.** Electrodes used for capacitance experiments: low-cost castellated, low-cost IDE, commercial 100 µm, 50 µm, 10 µm, concentric 10 µm, 5 µm IDEs. The first three of these are used for *E. coli* experiments and the rightmost four are included in the low-cost biosensing device experiments.

Although it can be seen that the low-cost electrodes in Fig. 3.3 have a larger area, the effective size of these electrodes is reduced by breaking the connections between the fingers that span the width of the electrode surface and the main fingers that connect them to a measurement device.

Fig. 3.4 shows a measurement jig that was designed and 3D printed to hold a microcuvette and the electrode in a fixed position relative to one another, with the microcuvette containing a sample of a cloudy bacteria-based bioreactor. The jig consists of a base that holds the microcuvette, as well as a saddle that can hold the electrode at a fixed location. This is achieved through the addition of holes through the pillars of the base spaced 1 mm apart, into which a height limiter can be inserted at the appropriate location. The bulk liquid at the top of the microcuvette is used for measurement to ensure that the electrode is fully immersed and measures only the solution containing the cells.

Verification experiments are conducted using a Metrohm Dropsens µStat-i400s [68] potentiostat capable of EIS. The reactance can be extracted from the complex impedance data, and the capacitance can be calculated from the reactance. The experimental setup for EIS measurements is outlined in Section 3.3.2.

### 3.3.1 Electrode materials and geometry

Benchmarking low-cost electrodes against one another and a commercial electrode allows for a complete characterisation of the differences that arise due to differences in geometry and materials.

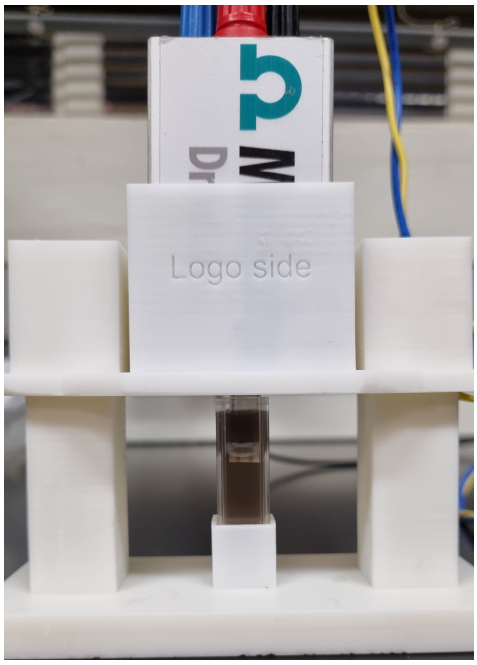



**Figure 3.4.** Measurement jig to ensure consistent electrode placement and constant volume across consecutive samples.

Three different electrodes are used to compare their response to *E. coli*. The first is a commercial IDE patterned in gold on a plastic flexible plastic substrate [63]. Two low-cost alternatives are proposed: an IDE and a castellated electrode, as seen in Section 3.2. Both the low-cost electrodes use FR4 as a substrate with copper traces plated with a thin layer of gold. From the electrical properties seen in Section 3.2, the two substrate materials affect the response, whereas no significant difference between the gold and gold-plated copper electrode materials is expected.

One reason for coating the traces in gold is to ensure that they are inert to interactions with air and the suspending solution. For proper benchmarking across the electrodes, the finger width and spacings are kept constant at 100 µm, and the area of the electrodes is kept constant at 6x6 $mm^2$. Although it can be seen that the low-cost electrodes in Fig. 3.3 have a larger area, the effective size of these electrodes is reduced by breaking the connections between the fingers that span the width of the electrode surface and the main fingers that connect them to an excitation source.

### 3.3.2 Cellular interaction

Cell manipulation is a very useful technique when analysing single cells or small known quantities of cells. These manipulation techniques allow the cells to be attracted to the electrode surface for the

most effective analysis of the electrical properties of the cells. For measuring the concentration of an unknown quantity of cells, however, any manipulation technique that manipulates cells to or away from the electrode surface may affect the extracted concentration. Therefore, no cell manipulation techniques are applied for EIS or other measurements, but samples are limited in volume by using a microcuvette to hold a fixed volume of liquid for each sample.

Living *E. coli* cells for experiments are obtained through a partnership with the Department of Chemical Engineering at the University of Pretoria. Since the experiments are not conducted on live bacteria, no ethical clearance is necessary for experiments conducted with *E. coli*. Three reactors are prepared simultaneously and identically to ensure the repeatability of the results obtained.

*E. coli* cells are grown in a standard Luria-Bertani (LB) broth consisting of

- 5 g/L yeast extract,
- 10 g/L Tryptone,
- 10 g/L NaCl.

Each reactor uses 500 mL of the broth from the recipe above and is placed in serum bottles before being placed in an autoclave at 121° for 15 minutes to ensure the environment is sterile. The serum bottles are removed from the autoclave and left to cool to ensure that proteins in the *E. coli* do not immediately denature and that the bacteria are viable to grow. To prevent the growth of unwanted gram-positive bacteria, the *E. coli* strain is initially plated in a gram-negative selective agar, Eosin Methylene Blue. From the bacteria grown on this plated sample, 0.2 mL of culture is used to inoculate each reactor. All three reactors are then sealed and purged with $N_2$ to ensure growth occurs in anaerobic conditions. Aerobic growth requires oxygen, whereas anaerobic growth happens in the absence of oxygen and requires different circumstances to ensure optimal growth. All three reactors are placed in an incubator set to 35° and set to spin at 120 RPM. Reactors are spun to ensure growth happens in the solution rather than on the inside of the serum bottles. Every hour, each of the three serum bottles is shaken, and a 2 mL sample is withdrawn using a hypodermic needle and sterile syringes to ensure a sterile environment is maintained. The optical density at a wavelength of 600 nm ($OD_{600}$) is then measured to determine cell growth.

Once the *E. coli* stops growing, after at least 20 hours, serial dilutions are prepared from the three stationary growth reactors. Seven sets of consecutive 1:10 dilutions are prepared with autoclaved distilled water. A 1 mL sample is taken from the reactor and added to the first container with 9 mL of distilled water for the $10^{-1}$ dilution. This container is then agitated, after which a 1 mL sample is taken from it and added to a new container with 9 mL distilled water.

This process is repeated until seven tenfold dilutions have been prepared for each of the three reactors. These dilutions are used for measuring *E. coli* concentration by taking 2 mL from each dilution and placing this in the microcuvette setup seen in Fig. 3.4. As a benchmark for the EIS measurements, 0.1 mL of the $10^{-4}$, $10^{-5}$, $10^{-6}$, and $10^{-7}$ dilutions are spread across the surface of agar plates prepared from the same LB broth and incubated at 35 °C for 72 hours, after which the colony forming units (CFU) can be counted.

With the Metrohm Dropsens a 100 mV sinusoid is applied across the electrodes. The frequency of this sinusoid is swept from 10 Hz to 1 MHz in half-decade steps, which results in a sample at the start and in the middle of each decade. Table 3.3 summarises the device setup used for EIS measurements.

For each dilution, the setup is kept constant while running the experiment for the three electrode types. Dilutions are measured in increasing concentrations (from $10^{-7}$ to $10^{-1}$) for one reactor at a time to prevent cross-contamination between reactors. Each set of three electrodes is reused for all dilutions of one reactor, and a new set of electrodes is used for each set of reactor dilution measurements.

**Table 3.3.** Metrohm Dropsens setup for EIS measurement.

| Parameter | Value | Unit |
|---|---|---|
| Minimum frequency | 10 | Hz |
| Maximum frequency | 1 | MHz |
| Excitation amplitude | 100 | mV |
| Sample points | 11 | |

The proprietary Dropview software's data is exported in.csv file format and then read into Python as magnitude and phase data for further processing. Although an equivalent circuit can be fit to this data as seen in [14], this investigation is aimed at extracting the capacitance of the mixture. Since this

investigation focuses purely on capacitance, the magnitude and phase data are converted to real and imaginary impedance (resistive and reactive impedance), and the resistive part is ignored.

Using the formula for the reactance of a capacitor,

$$X_C = \frac{1}{2\pi f C}, \tag{3.8}$$

the capacitance, $C$, may be calculated using the frequency at which the reactance is measured.

### 3.3.3 Low-cost biosensor device

The opamp designed in Section 4.2 for use in the array-based CVC is included as a component on its own on the manufactured chip. This allows a low-cost biosensor device to be developed using the opamp placed on the chip. The low-cost biosensor device is designed to be used in the same jig as seen in Fig. 3.4, replacing the saddle that houses the proprietary Dropsens electrode holder with a saddle that houses the low-cost validation device.

This validation experiment is conducted with polystyrene microbeads available at CEFIM and provides a valuable comparison to the extracted capacitance from the EIS measurements of *E. coli*. Although a biosensor array with integrated electrodes was designed and the layout for it is complete, the work required to integrate the delivery of the liquid sample and electrical connections off-chip is beyond the scope of this investigation.

Using this approach also allows the investigation of the potential of low-cost electrodes in bulk capacitive cell sensing in comparison to commercially available electrodes, seen in Table 3.4. An Arduino Uno R3 powered using USB from a computer is used as the 3.3 V power supply required for the custom IC and as the digitisation front end.

The topology for the biosensor device that uses low-cost and commercial electrodes is nearly identical to the CVC design in Section 4.3. However, the low-cost electrodes seen in Fig. 3.3 exhibit a higher baseline capacitance than the proposed on-chip electrode proposed in Section 4.3.1, which requires discrete components that cannot be implemented on-chip. The CVC operates on the principle of charge sharing between a sensing electrode, $C_S$, and an integrator capacitor used in the feedback path, $C_{int}$, as seen in Fig. 3.5. Ideal opamp analysis of the CVC shown in Fig.3.5 yields a transfer function of the form

$$\frac{V_o}{V_i} = \frac{C_{int}}{C_s}. \tag{3.9}$$

**Table 3.4.** Electrode comparison conducted using low-cost biosensor device and LCR meter.

| Finger width (µm) | Note |
|---|---|
| 100 | Low-cost IDE<br>Low-cost castellated<br>IDE on plastic substrate |
| 50 | IDE on plastic substrate |
| 10 | IDE on glass substrate<br>Concentric ring IDE on glass substrate |
| 5 | IDE on glass substrate |

A reset switch, $S_1$ (CD4066BE), in the feedback path is required to clear the charge stored on $C_{int}$ to prevent the opamp from saturating. $R_1$ is an optional resistor included at the input of the opamp to attenuate the input signal to the opamp, which slightly extends the dynamic range of the CVC. Omitting this resistor moves the effective detection range to smaller capacitance values.

A 5 V clock pulse from the Arduino is passed through a voltage divider to attenuate its amplitude as required, after which it is used as an excitation input voltage for the CVC and for controlling the switch used for resetting the output of the CVC. The output of the CVC is read into the Arduino at the maximum ADC sampling rate of 77 kHz with the full range of the ADC, after which ADC values are averaged over 1024 samples at a time. These averaged values are sent to a PC interface over UART at a baud rate of 9600 bit/s.

The components of the low-cost CVC device are soldered onto Veroboard, and in combination with the Arduino microprocessor, this system is installed on a custom saddle similar to that seen in Fig. 3.4 to be used in conjunction with the same base. To hold the electrode in the correct orientation and in the same position for consecutive measurements, a custom electrode holder based on a clothes peg is designed and built. Fig. 3.6 shows the low-cost biosensor installed on the custom saddle, with the custom IC in a zero-insertion force holder at the front, the electrode holder in the middle, and the Arduino at the back. Appropriately spaced header pins installed in a wooden clothing peg act as an electrode holder, with wires connecting these header pins to the correct position in the soldered circuit.

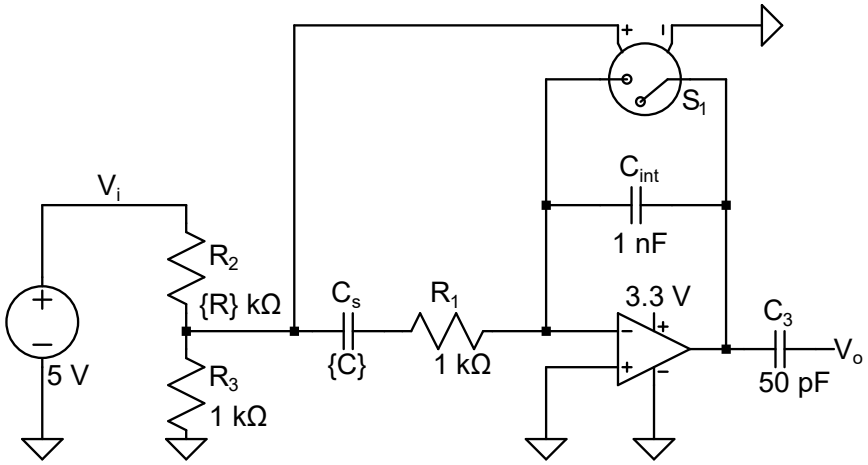



**Figure 3.5.** Circuit used for the low-cost biosensor device.

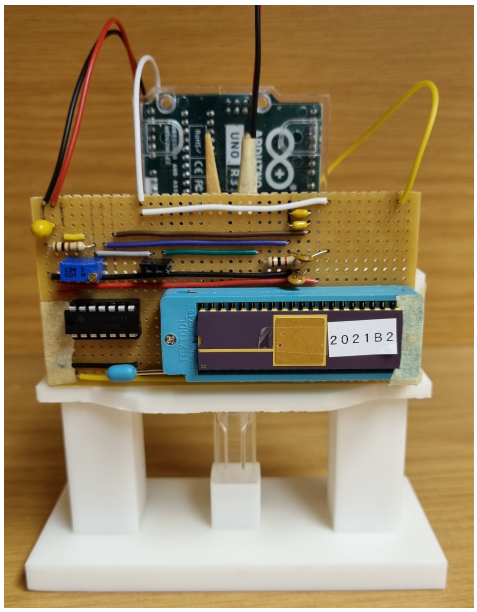


**Figure 3.6.** Measurement jig containing the low-cost biosensing device saddle.

Before conducting experiments with this device, a calibration curve of its output for various capacitance inputs is drawn, and from this calibration curve, the capacitance of an arbitrary solution may be determined. The calibration curve uses capacitance measured from discrete capacitors validated against the GW Instek LCR meter, after which the value read into the Arduino is noted, and this relation is tabulated and graphed.

To ensure the low-cost biosensor is a fitting device for measuring bacterial cells, 3 µm diameter

polystyrene beads (Sigma-Adrich, St Louis, MN, USA) are used. The number of particles per $mm^3$ is calculated as [69]:

$$N = \frac{(6 \times 10^{10}) \times S \times P_L}{\pi \times P_s \times d^3}, \tag{3.10}$$

where S is the % suspended solids (2.5%), $P_L$ is the density of the bulk polymer the microbeads are suspended in (1.005 g/mL for latex), $P_s$ is the density of the bulk polymer (1.05 g/mL for polystyrene).

Substituting these values yields a microbead concentration of $1.523 \times 10^{16}$/mL. A 5 µL sample is taken and added to 5 mL deionised (DI) water, resulting in a 1:1000 dilution of the original sample, which gives a starting concentration of $1.523 \times 10^{13}$/mL. Serial 1:10 dilutions are prepared using this known starting concentration by adding 1 part of this sample to 9 parts DI water. This process is repeated several times to observe the change in capacitance for a tenfold change in microbead concentration.

From these prepared 10 mL dilutions, a 2 mL sample is taken and placed into a microcuvette in the bottom holder seen in Fig. 3.4. The low-cost biosensor device on the custom saddle is lowered into position to expose the electrode to the bulk sample liquid at the top of the cuvette, after which a measurement is taken.

## 3.4 LOC ELECTRICAL CHARACTERISATION

Characterisation of the custom IC designed in Chapter 4 is required to confirm the proper functioning of the array switching method implemented for the LoC array and to characterise the performance of the operational amplifier designed in Section 4.2 when used as a discrete opamp.

### 3.4.1 Opamp characterisation

Opamp characterisation occurs using two tools: an HP 4155B semiconductor parameter analyser and an oscilloscope. Using these tools will confirm whether the chip performs as simulated. The following tests are conducted using the parameter analyser:

- DC gain,
- Input offset voltage,
- Output range.

These parameters can be extracted by keeping one of the input terminals at a constant potential and sweeping the other to create a differential input voltage.

Constant positive (+1.65 V) and negative (-1.65 V) rail voltages are supplied to the $V_{DD}$ and $V_{SS}$ pins of the IC, respectively, using two of the available Source Measure Units (SMUs) of the parameter analyser. A third SMU channel is set up with a variable voltage swept from -1.65 V to +1.65 V and applied to the non-inverting terminal, with the fourth available SMU set up in common-mode and connected to the inverting input of the opamp.

One of the available Voltage Measure Units (VMU) is connected to the output terminal of the opamp. A transfer curve is drawn of the output voltage, $V_o$, versus the input voltage, $V_i$, from which the required parameters can be extracted. Fig. 3.7 shows the test setup for all tests conducted using the parameter analyser.

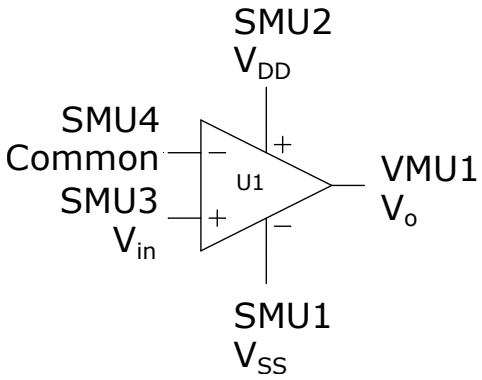



**Figure 3.7.** Test setup for DC transfer characterisation conducted with the parameter analyser.

After characterising the DC performance of the opamp using the parameter analyser, the transient and AC responses of the opamp may be characterised using a power supply, function generator, and oscilloscope. The parameters of interest in this characterisation include:

- Slew rate (SR)
- Bandwidth
- Gain-bandwidth product (GBP)

The first of these parameters may be measured using the opamp in a voltage buffer configuration, with the output connected to the inverting terminal and the excitation signal applied to the non-inverting terminal. Slew rate gives a measure of how quickly an opamp can respond to large signal changes in its input [70]. A large-signal square wave of an appropriate frequency is required at the input during the slew rate measurement. Although an arbitrary frequency of the input signal may be used, the transient response of the opamp has to be studied to ensure the output value settles to a fixed value. For this investigation, a signal of 1 kHz at 1 $V_{pp}$ is used.

The output is then monitored on the oscilloscope. To calculate the slew rate, the time taken for the output wave to rise from 10% to 90% of the maximum voltage is measured. The change in voltage is then divided by the change in time to give the slew rate:

$$SR = \frac{V_{90\%} - V_{10\%}}{t_{90\%} - t_{10\%}}. \tag{3.11}$$

Bandwidth is defined as the frequency at which the low-frequency open loop gain of the opamp drops by 3 dB, as this represents a halving of the power output. Since it is expected that the opamp has large gain at low frequencies and could saturate, the input from the signal generator is set to 1 $mV_{pp}$ and further attenuated using a 1000:1 voltage divider to provide a µV-range input voltage.

The frequency of this sinusoid is swept until a 3 dB drop in gain is observed. The gain-bandwidth product of the opamp for single-pole compensated opamps is defined as the product between the open-loop gain at a specific frequency and the frequency itself [70],

$$GBP = A_o(f) \times f. \tag{3.12}$$

This value is the transition frequency at which the gain of the opamp reaches unity (or 0 dB). To measure these parameters, a common DC voltage is applied to both input terminals of the opamp, with a small signal differential sinusoidal signal of 1 kHz applied to the non-inverting input.

### 3.4.2 CVC array functional testing

As part of the array control logic, output pulses are used for synchronising the row and column clocks.

The first step toward possible future full integration of the LoCMOS into a full capacitive sensing array is to ensure that the timing works as intended. Two timing clocks are required: one for the rows and one for the columns. For each rising edge of the row clock, the column clock needs to have eight rising

edges to accommodate each of the 8 columns per row. These clocks are generated on an FPGA using an appropriate clock divider to ensure output pulses are visible on an oscilloscope since the update frequency of the sensing array can be as high as the technology allows or as high as the application requires.

These two clocks are then fed into pins used to control the array on the LoCMOS. At the rising edge of the first column, a pulse is echoed back on an output pin as confirmation that a specific row has begun. Similarly, for the first row, an output pulse is echoed, which signifies the first row. This means that detecting both echoed output pulses signifies the start of a reading cycle for the entire array. The clocks and corresponding output pulses are read on an oscilloscope to verify their correct timing.

## 3.5 CHAPTER SUMMARY

In this chapter, the approach as proposed in Section 1.3 is expanded to explain the experiment setups required to answer the research questions from Section 1.2. First, Section 3.2 discusses the automatic parameterised electrode generation used in the finite-element analysis of the various electrodes. The simulation setup, including the materials and geometry of electrodes, is explained, as is the procedure used to generate *E. coli* cell substitutes. Section 3.3 expands on the setup used to measure the performance of three different electrode types when used to measure *E. coli* cells in dilution with a commercial potentiostat. The design for a low-cost biosensor prototype designed using the custom IC is also discussed. Section 3.4 discusses the electrical characterisation setup required to characterise the DC, AC, and transient responses of the opamp used in the low-cost biosensor prototype. The section also includes methods to validate the performance of the custom array-based LoCMOS system.

# CHAPTER 4 MICROELECTRONIC CIRCUIT DESIGN

## 4.1 CHAPTER OVERVIEW

This chapter presents the design considerations, equations, simulation results, and layout for the LoC system. Section 4.2 discusses the specifications, design, and layout of the operational amplifier used for the biosensor. This is followed by the design of a single CVC sensor system with electrodes included in the back end of the chip manufacturing process in Section 4.3, after which the requirements and design for the full array are discussed in Section 4.4.

## 4.2 OPERATIONAL AMPLIFIER

Although some biosensor applications avoid using opamps [4], [12] [47], the majority of CVC or CFC applications require an opamp at some stage in the amplification [42], [46], [55].

In the case of CFC applications, op-amps can be especially helpful when considering an array-based approach, such as using the change in capacitance on the electrodes to change the free-running frequency of an oscillator [12] or the use of transmission line crossings at microwave frequencies to extract the mean capacitance change over a matrix [47]. However, the use of operational amplifiers in the CVC or CFC stage of sensing allows for differential measurement [11], [42], [46], while the higher gain available to an opamp-based circuit generally allows for higher detection sensitivity [43].

For a capacitive biosensor measuring single cells, the high sensitivity provided by an opamp is required to distinguish the relative capacitance change [55], but this cannot come at the cost of feature size [12]. In both referenced and reference less applications, the use of multiple gain stages will increase the sensitivity of a capacitive biosensor [43], but at the cost of a larger on-chip footprint.

A larger electrode area will capture larger numbers of cells, and if electrodes are integrated into the layers above the sensing circuitry, a key requirement of the opamp is a footprint small enough to minimise the size of the electrode.

### 4.2.1 Specifications and design considerations

Various parameters of interest in the design of an opamp are related to specific functional blocks within the opamp, each with related design constraints and equations [71].

The parameters that arise from the use of specific functional blocks also affect the performance of functional blocks in higher levels of the opamp hierarchy [72], requiring careful consideration of performance trade-offs when designing the opamp. Three common opamp topologies were considered for the design of the biosensor opamp: two-stage, telescopic, and folded cascode.

Of the three, the two-stage topology presents the highest gain and output swing and the lowest operation speed, as well as the fewest transistors in its design. The telescopic and folded cascode provide similar gains, with the former providing the lowest power consumption and the latter having the highest operating speed [73]. Since the gain is more important than speed in this application, and keeping in mind the condition that the size of the opamp be minimised, the logical choice for this application is the two-stage topology.

With *E. coli* demonstrating a characteristic frequency between 1-2 MHz [27], one main requirement is that the gain-bandwidth product (GBP) exceeds at least 3 MHz.

Further, since the CVC circuitry around the opamp will certainly degenerate the maximum available gain, the low-frequency gain required for this application is chosen to be at least 60 dB. These requirements need to be balanced against the footprint of the opamp, as the application calls for an array of these opamps with their associated CVC circuitry included. CFC-based *E. coli* measurements can be done effectively using electrodes with a 30x30 $\mu m^2$ footprint [12] in a 0.35 µm CMOS process, although the specific method results in an effective sensing area of 120x120 µm per electrode. Based on the results achieved by [12] in a similar CMOS process node, the requirement for this implementation is to include the entire opamp, CVC circuitry, and electrodes in a footprint smaller than 50x50 $\mu m^2$, which can then be implemented in an 8x8 array. Finally, since the CVC circuitry generally requires feedback, stability will be ensured by designing for a 45° phase margin.

### 4.2.2 Opamp design

Fig. 4.1 shows the general topology for a two-stage opamp with Miller feedback ($C_1$) for a single-rail power supply.

An input PMOS differential pair ($M_1$, $M_2$) has their respective NMOS loads ($M_3$, $M_4$). Two factors drive the choice for using a PMOS differential pair: first, noise from the input pair directly affects the noise of the total system. Second, the noise contribution of the NMOS load transistors is reduced by the square of their transconductance [74]. Since PMOS transistors have lower flicker noise than their NMOS counterparts, this makes a PMOS input pair the preferred choice for this application. The output of the first stage is taken from the drain of $M_4$ and drives the gate of the second stage ($M_6$), which is a common-source NMOS amplifier.

Biasing current for the two branches is provided by mirroring the current through $M_8$ by controlling the W/L ratio of $M_5$ and $M_7$. During the development of the opamp, a capacitive load ($C_2$) of 5 pF is used, as this is the typical load seen when driving a pad and a load off-chip. The subsystem that provides the biasing [72] has been omitted, as this can be designed separately to replace the ideal current source $I1$. The feedback capacitor $C_1$ ensures stability at the cost of bandwidth.

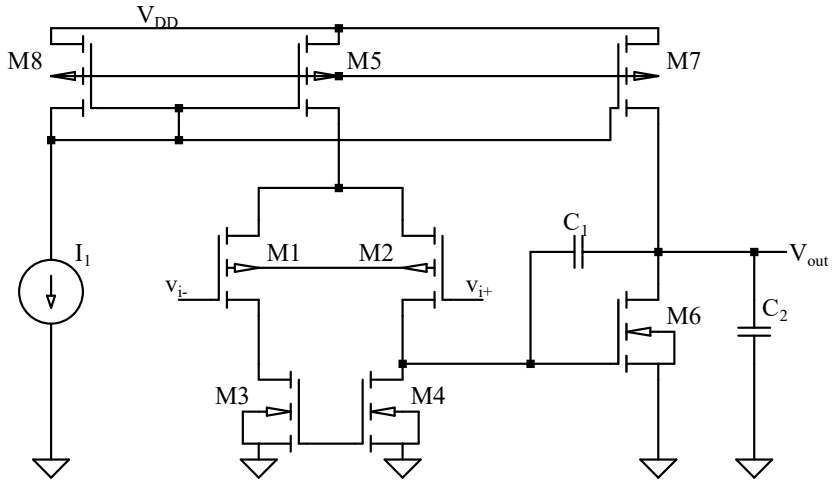



**Figure 4.1.** Schematic for two-stage opamp excluding biasing circuitry.

Using Miller capacitance, as seen in Fig. 4.1, yields a right-half plane zero in the open-loop gain [75], which could be undesirable in certain applications. The performance of the Miller capacitor compens-

ation technique is compared to similar methods in [75]: the addition of a nulling resistor, a voltage buffer in the feedback path, and a current amplifier in the feedback path.

It is found that the voltage buffer is more suitable for higher capacitive loads, while the current amplifier is more suited for moderate capacitive loads. Both solutions, however, require multiple additional transistors and biasing currents, which increase the opamp footprint and power consumption. Using a nulling resistor as a triode-biased NMOS transistor was investigated, but the increased bandwidth caused a severe and unacceptable degradation in the phase margin. Thus, only the Miller feedback capacitor was used. Once the specifications and feedback method are established, design procedures for two-stage opamps were investigated [76]. The method presented in [77] builds on the work done by [76], with [78] further refining both previous methods to enable the use of a smaller feedback capacitor.

This method uses specifications for the bandwidth and output current, along with relations between known quantities, to present design equations in a step-by-step guide and is the method used to find first-order approximations of the correct device dimensions. These equations are adjusted appropriately from [78] for use in a single-rail PMOS-input device opamp. First calculate the value of the feedback capacitor $C_1$ in Fig. 4.1:

$$C_1 = \frac{16kT}{3\omega_u S_n(f)}\left[1 + \frac{SR}{\omega_u(V_{HR}^{CM-} + |V_{tp}|)}\right]. \tag{4.1}$$

The value of the feedback capacitor is determined by the slew rate, $SR$, the unity gain frequency in rad/s, $\omega_u$, the desired input-referred thermal noise spectral density, $S_n(f)$, in $V/\sqrt{Hz}$, and the desired common-mode headroom, $V_{HR}^{CM-}$. Constants include the Boltzmann constant, $k$, and the operating temperature, $T$, which is generally taken to be room temperature in Kelvin. $V_{tp}$ is the turn-on voltage of the specific input pair device (in this case, PMOS transistors), which is process-dependent.

The current in the output branch is then calculated as

$$I_{D7} = SR(C_1 + C_L), \tag{4.2}$$

with $C_L$ the value of the load capacitance value. The current in the output branch is fixed, so the dimensions of $M_6$ can be calculated as

$$L_6 = \sqrt{\frac{3\mu_n V_{HR}^{out-} C_1}{2\omega_u(C_1 + C_L)\tan(\phi_M)}}, \tag{4.3}$$

$$W_6 = \frac{2SR(C_1 + C_L)}{\mu_n C_{ox}\left(V_{HR}^{out-}\right)^2} L_6. \tag{4.4}$$

Equation (4.3) contains $V_{HR}^{out-}$, which is the opamp headroom voltage available at the output, with the - in the superscript indicating this is related to the headroom on the lower end of the output swing. $\phi_M$ is the desired phase margin.

In (4.4), $\mu_n$ is the electron mobility in the inversion layer, specifically for NMOS devices, and $C_{ox}$ is the capacitance of the gate oxide layer. Both these quantities are process-specific. The internal slew rate of the opamp is related to the compensation capacitor $C_1$ and the biasing current in the differential branch. Using the same internal and external slew rate allows this relationship to be used to calculate the required current in the differential branch, provided through $M_5$ with

$$I_{D5} = C_1 SR. \tag{4.5}$$

Assuming $M1$ and $M2$ are identical, $I_{D5}$ is split equally between them. This fact is used, along with the transconductance of $M1$, to calculate the dimensions for the differential pair as

$$(W/L)_{1,2} = \frac{\omega_u^2 C_1}{\mu_p C_{ox} SR}, \tag{4.6}$$

where $\mu_p$ is the hole mobility in the inversion layer specifically for PMOS devices, which is a process-specific parameter.

Next, the dimensions of the current mirrors $M_5$ and $M_8$ are calculated. With the W/L ratio of these equal, $I_{D5}$ is equal to the current provided by the ideal current source $I_1$, which is replaced with a biasing network:

$$(W/L)_{5,8} = \frac{2SRC_1}{\mu_p C_{ox}\left(C_{HR}^{CM+} + |V_{tp}| + \frac{SR}{\omega_u}\right)^2}. \tag{4.7}$$

With the current for the first stage fixed, the current for the second stage branch is fixed by fixing the dimensions for $M_7$:

$$(W/L)_7 = \left(\frac{C_1 + C_L}{C_1}\right)(W/L)_{5,8}. \tag{4.8}$$

Finally, the dimensions for the load devices $M_3$ and $M_4$ are calculated with

$$(W/L)_{3,4} = \frac{(W/L)_6}{2(W/L)_7}(W/L)_{5,8}. \tag{4.9}$$

The value of the compensation capacitor is chosen to be 300 fF in an attempt to satisfy the footprint requirement. operating assumptions for the opamp derived are from parameters adjusted from a commercial 3.3 V CMOS opamp [79]:

1. Room temperature operation (T = 300K),
2. a slew rate of 5 V/µs,
3. a noise spectral density of 80 nV/$\sqrt{Hz}$,
4. Common-mode headroom of 1.7 V,

Using these operating assumptions and the chosen size of the compensation capacitor, (4.1) can be used to calculate the unity gain bandwidth of $f_u = 5.9$ MHz. This meets the specification set in 4.2.1, provided the noise at the input of the opamp is kept below the value assumed above. Noise minimisation is achieved in part by ensuring the layout is immune to noise and keeping the biasing current low. The current through M5 is chosen as 10 µA to achieve this, with the rest of the design steps as outlined above following from there.

#### 4.2.2.1 Biasing network

To generate the bias current required for the opamp while keeping in mind the size constraints, a simple biasing circuit with a few elements is required. For this aim, Wilson and cascode current mirrors are considered [74]. Although the cascode mirror provides larger output resistance, the design simplicity afforded by the Wilson mirror makes the latter the natural choice. From the design procedure followed in the preceding section, the geometry of M5 and M8 are identical, and assuming these devices are perfectly matched, the current through them should be identical.

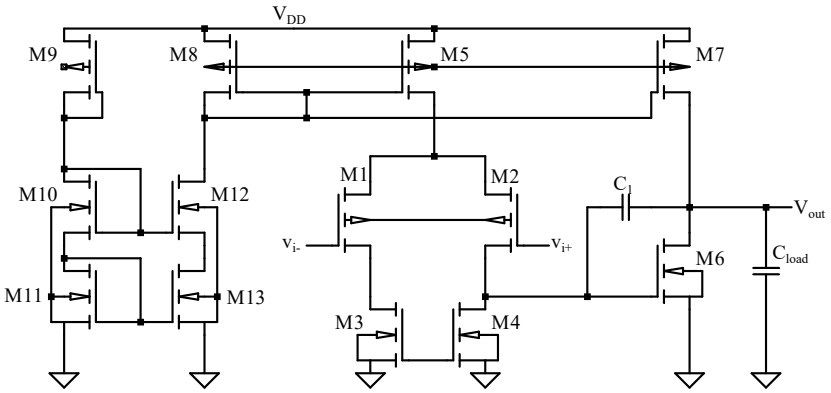



**Figure 4.2.** Schematic for two-stage opamp including biasing circuitry.

Although it would be useful to make the W/L ratio of M9 different from that of M5 and M8 to lower the wasted current drawn through the far left-hand branch, any deviation of current in this branch would then be multiplied through M5, M8, and M7 by their W/L ratios, potentially degrading the

performance of the opamp. This informed the choice to use an identical aspect ratio for M9 as for M5 and M8.

Assuming M9 operates in saturation, the required gate-source voltage is given by

$$V_{GS9} = \sqrt{\frac{2i_{D9}L_9}{\mu_P C_{ox} W_9}} - V_{tP}, \tag{4.10}$$

which can be used to find the required voltage at the drain of M10.

Using $i_{D9} = 10$ µA and the required process-specific parameters, as well as $(W/L)_9 = 1/1$, (4.10) evaluates to

$$V_{GS9} = V_{DD} - V_{D10} \approx 1.41 \text{ V}. \tag{4.11}$$

Assuming $V_{DD} = 3\ V$, the above requires at least a $1.4\ V$ drop over the two active load transistors.

The equation for the drain current for NMOS devices operating in saturation can be rewritten to determine the required W/L ratio:

$$\frac{W}{L} = \frac{2i_D}{\mu_n C_{ox}(V_{GS} - V_{tN})^2}, \tag{4.12}$$

from which the required W/L ratio is calculated as 0.25/1. This can be achieved by using the ratio as is, or by using W = 1, L = 4.

#### 4.2.2.2 Final dimensions

The feature sizes are determined using (4.1) to (4.9), after which optimisations are done once the biasing network is added. These optimisations are mostly aimed at getting the corners of the simulations as close as possible to one another, which ensures proper performance of the opamp regardless of process variation. Table 4.1 shows the dimensions for $C_1$ and the final, optimised W/L ratios of the transistors.

### 4.2.3 Opamp layout

The common-centroid layout is generally used in analog design by matching device characteristics to ensure the design is robust against process variations. This can also be achieved by using smaller feature sizes. By maintaining a common-centroid layout in a design with smaller features, the effect of parasitics on opamp performance can be reduced [80]. Fig. 4.3 shows the layout artwork for the biosensor opamp.

**Table 4.1.** Final features of the biosensor opamp.

| Feature | Dimensions |
|---|---|
| $C_1$ (300 fF) | 35.2 x 9.7 µm |
| $(W/L)_{1,2}$ | 10/1 |
| $(W/L)_{3,4}$ | 1/1.5 |
| $(W/L)_{5,8,9}$ | 1/1 |
| $(W/L)_6$ | 38/3 |
| $(W/L)_7$ | 10.4/1 |
| $(W/L)_{10-13}$ | 0.5/1 |

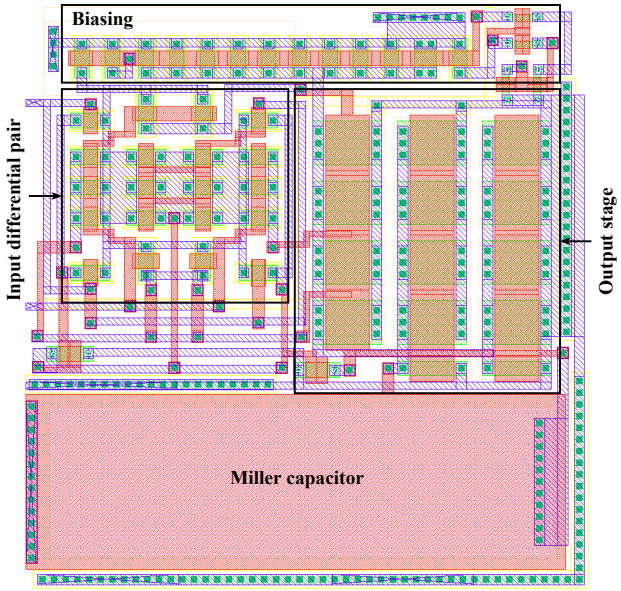



**Figure 4.3.** Annotated layout artwork for the biosensor opamp.

Biasing transistors ($M_5$, $M_7$, $M_8$, and $M_9$, with $M_9$ broken into unit-size transistors) are placed at the top, with the current flowing from source to drain from top to bottom. Below the biasing transistors, to the left, the input pair ($M_1$, $M_2$) has been split into 10 unit transistors each. The N-doped tub required for PMOS transistors encompasses all of these devices.

The output NMOS device, $M_6$, is broken up into 12 3/3 NMOS transistors, which add to give a combined W/L = 36/3. A further two 1/3 transistors are added to obtain the required aspect ratio

of 38/3. Finally, the dimensions of the polysilicon capacitor were adjusted to fit into the remaining area below the active components as a single-shape polysilicon capacitor (as opposed to being split into multiple unit capacitors) are made rectangular to keep the footprint of the opamp approximately square.

### 4.2.4 Simulated opamp performance

Simulations of the electrical performance of the operational amplifier and associated circuits built using it include the nominal performance and the spread of transistor performance according to the variation in carrier mobility and threshold voltage for the manufacturing process used.

These corners encompass the extremes of carrier mobility for NMOS and PMOS transistors in the manufacturing process, with the maximum carrier mobility referred to as "fast" and the minimum referred to as "slow". The combination of these for PMOS and NMOS devices leads to four corners: slow-fast, fast-fast, slow-slow, and fast-slow. These corners are critically evaluated to ensure the device still performs as designed.

Fig. 4.4 shows the nominal and corner simulations of the open loop DC transfer curve for the opamp, obtained by connecting both terminals to a constant 1.5 V (slightly less than halfway between 0 and 3.3 V) and sweeping the DC voltage at the non-inverting terminal while measuring the output voltage.

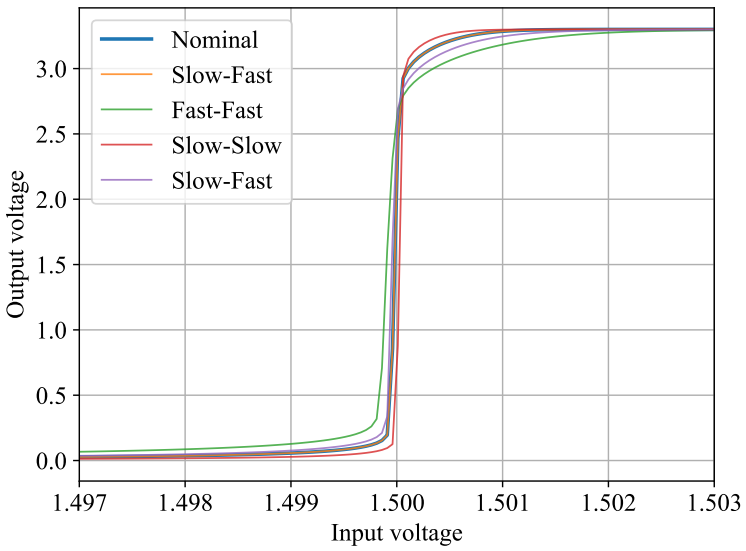



**Figure 4.4.** Simulated DC transfer curve of the opamp used in the low-cost CVC and CVC array.

Fig. 4.4 shows only the region around 1.5 V to study the effect of a differential DC voltage input. The nominal input offset-voltage is measured as the difference between 1.5 V and the value of the input voltage that causes a 1.5 V output voltage, which is 1.4999799. This translates to a nominal input offset-voltage of approximately 20 µV.

The even corners (fast-fast and slow-slow) deviate the most from the nominal case, with offsets of 96 and -25 µV, while the odd corners are closer in performance to the nominal case. Next, the nominal DC gain is characterised by the gradient of the linear portion of the curve around 1.5 V, with the input range defined by the bounds of this linear region.

The nominal linear operating region for both terminals biased at the same voltage is approximately ±75 µV, with the gain DC gain over this region given as

$$A_{V(DC)} = \frac{V_{o,2} - V_{o,1}}{V_{i,2} - V_{i,1}} = \frac{2.947\text{ V} - 0.396\text{ V}}{75\text{ µV} - (-75\text{ µV})} = 16.9\text{ kV/V}.$$

This translates to around 84.5 dB open-loop voltage gain at DC.

A slight offset is present at low input voltages, which limits the nominal output voltage to $V_{SS}$+15 mV and the output to $V_{DD}$-2 µV for $V_{SS}$ = 0 V and $V_{DD}$ = 3.3 V. To characterise the simulated slew rate and check this against the design, Fig. 4.5 shows the response of the opamp to a large signal step input (in this case, 1 V) applied to the noninverting terminal with the inverting terminal tied to 0 V and the amplifier configured in a closed-loop buffer configuration with a 5 pF load.

All of the lines in Fig. 4.5 have offsets when no input signal is applied, with the highest and lowest offset at 86 mV and 20 mV for the fast-fast and slow-slow corners, respectively. This is likely a common-mode offset at the output due to the input offset voltage of around 20 µV being amplified by the 16.9 kV/V gain of the opamp. The slew rate is defined as the voltage difference from 10% to 90% of a step input divided by the time difference taken for the output of the opamp to follow its input.

Using Fig. 4.5 and (3.11), the nominal slew rate can be calculated as

$$SR = \frac{0.9\text{ V} - 0.1\text{ V}}{10.441\text{ µs} - 10.112\text{ µs}} = 2.43\ V/\text{µs}.$$

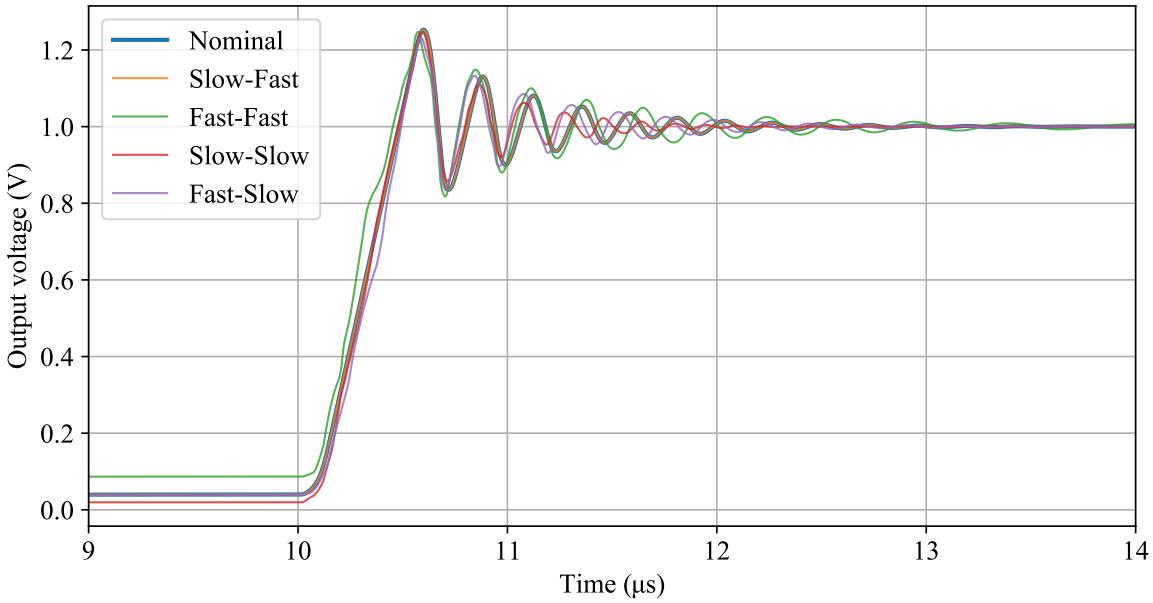



**Figure 4.5.** Simulated transient response to a 1V input signal.

The nominal and corner performances are quite close to one another throughout the response to the step input. The largest difference can be seen in the fast-fast corner, which has the quickest response time but also the least damped response, oscillating at 3.5 MHz around the setpoint for another 1 µs after the others have settled to the correct value. All the corners follow the underdamped response seen in the nominal case, with an almost 20% overshoot past the setpoint before oscillating for another 1.5 µs, corresponding to a frequency of approximately 667 kHz.

This oscillation may be addressed by adjusting the pole introduced by the feedback capacitor using a resistive element that acts as a zero to cancel or minimise the effect of the pole, which can extend the bandwidth of the opamp and reduce oscillations, though this comes at the cost of phase margin and consequently affects the stability of the opamp. This was considered during the opamp design, but to ensure at least a 45° phase margin is maintained, in the final design only a capacitor is used in the feedback path. The simulated AC gain of the amplifier from 10 Hz to 10 MHz, when terminated in a 5 pF shunt capacitor, is shown in Fig. 4.6.

The amplifier demonstrates a flat passband regardless of the corner, with a nominal gain of 88 dB and a -3 dB knee frequency at 700 Hz. This is sufficient for this application, and with a gain bandwidth product in excess of 10 MHz should be a useful opamp for many use cases.

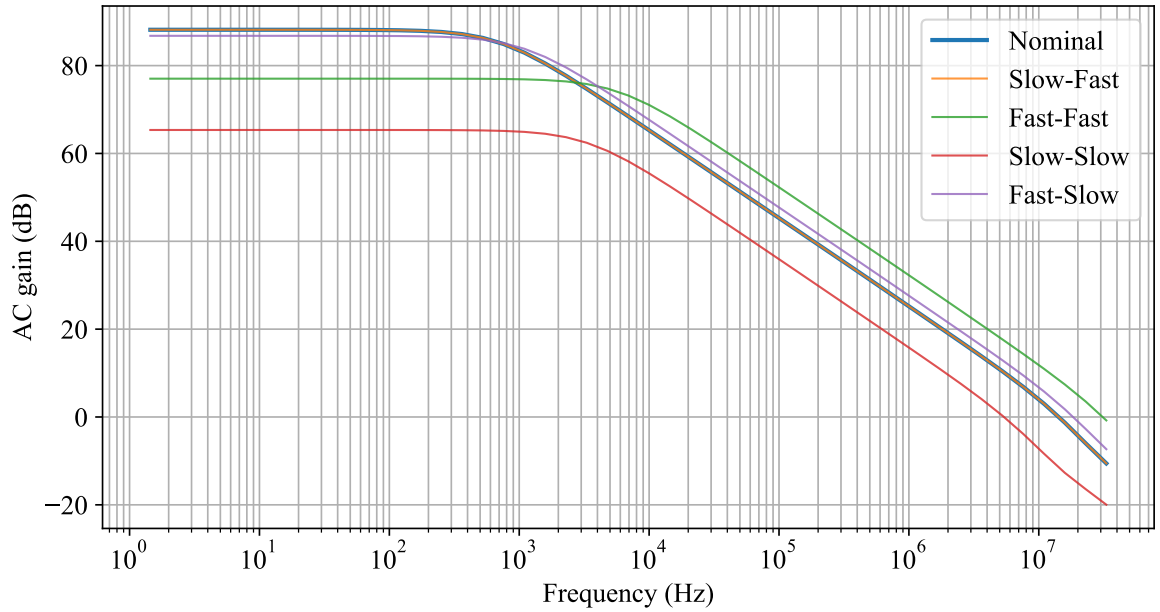



**Figure 4.6.** Simulated AC gain.

As before, the even corners are worst affected, with the gain nearly 11 and 20 dB lower than the nominal or odd-corner cases for the fast-fast and slow-slow corners, respectively. After the knee-frequency, a regular 20 dB/decade decay in gain is seen, as expected for a system with a single pole.

The nominal unity gain frequency occurs at 14.2 MHz, with a spread of between 5.4 MHz to 30.96 MHz in the worst cases. Table 4.2 shows the summarised typical performance of the biosensor opamp. AC gain and frequency measurements are completed with a 5 pF load. Common-mode rejection ratio (CMRR) is measured by dividing the differential-mode gain by the common-mode gain and is constant up to 112 kHz, after which a 20 dB/decade drop is observed.

Gain and transition frequency specifications are exceeded by about 26 dB and 10 MHz respectively, and the opamp is unconditionally stable. This opamp meets the requirements set out in Section 4.2.1.

However, the oscillations seen in Fig. 4.5 shows that the opamp is susceptible to stability degeneration when unity gain feedback is applied. The maximum variation in gain and bandwidth seen in Fig. 4.6 shows that the small-signal properties of the opamp are more affected by process variation than the large signal properties from Figs. 4.4 and 4.5. The simulated slew rate is about half that of the 5 V/µs design aim, which means the current provided by the output branch is also likely half as large as

**Table 4.2.** Summarised nominal electrical characteristics biosensor opamp.

| Parameter | Value | Unit |
|---|---|---|
| DC gain | 16.9 | kV/V |
| Low frequency gain | 88 | dB |
| Unity gain frequency | 17.2 | MHz |
| $f_{-3dB}$ | 700 | Hz |
| Input offset voltage | 20 | µV |
| Low-frequency CMRR | 92 | dB |
| Slew Rate | 2.43 | V/µs |
| Footprint | 1600 | $\mu m^2$ |

intended. In this case, the lower slew rate is likely caused by the lower output current.

## 4.3 CAPACITANCE TO VOLTAGE CONVERTER

Any CVC circuitry will require another on-chip capacitor to convert the charge on the sensing capacitor. The sensing capacitor for the CVC is the electrode, which has to be sized appropriately for the bacterium under consideration. The elliptical shape of *E. coli* varies between 1 and 4 µm on the primary axis, and approximately 0.6 µm on the secondary axis [27] which requires comparable spacing for any form of interdigitated electrodes. Since *E. coli* contamination is potentially deadly at low concentrations [17], the total area of the electrodes also has to be small enough to detect small concentrations of cells [8].

Taking all the above into account, should the application be expanded into a sensing array, the opamp would be too big for a single set of electrodes with the ability to detect small enough concentrations of cells. For electrodes manufactured in the back-end-of-line of the chip, a set of electrodes smaller than the entire CVC system would also not be practical, as the dead space between electrodes would not be able to detect any cells. The compromise, therefore, is the use of multiple smaller sets of electrodes and the required control circuitry for one CVC circuit.

Since the charge deposited on the sensing electrode can be controlled by the driving source, the size of the integrating electrode is under the control of the designer. To ensure that the smaller sets of electrodes can still be made small enough to detect low cell numbers, the size of the entire CVC circuit

has to be limited to 50x50 $\mu m^2$. Using such a small CVC circuit leaves enough area for four sets of electrodes with dimensions of 25x25 $\mu m^2$ each, set in a 2x2 matrix.

The proposed CVC cell design is shown in Fig. 4.7, with all the required interfacing to the rest of the LoCMOS. These ports include:

- $V_{DC}$: DC voltage used to charge the sensing capacitors,
- $V_{put}$: the output voltage of the CVC biosensor,
- $R1_{en}$: the active-low enable signal for the first sub-row,
- $R2_{en}$: the active-low enable signal for the second sub-row,
- $C1_{en}$: the active-low enable signal for the first sub-column,
- $C2_{en}$: the active-low enable signal for the second sub-column,
- $\phi$: the active-high control signal for the switches controlling charge integration and reset. Its inverse, $\overline{\phi}$, is generated inside the CVC cell and is used with $\phi$ to control transmission gate switches $S1$, $S2$, and $S3$.

The four electrode sets, $C_{11}$, $C_{12}$, $C_{21}$, and $C_{22}$, affect one another when measuring if they are not disconnected from the DC excitation source. Therefore, electrode control is provided through the use of active-low control signals to unit-size PMOS transistors switches for the two rows and columns in this biosensor.

The most basic version of the CVC circuit consists of the sensing electrode, the opamp, an integrator capacitor in parallel with a reset switch, and another two switches to control the excitation applied to the sensing electrode.

The first excitation-control switch ($S2$, in Fig. 4.7) is 180°out of phase with the other two switches and connects the excitation side of the electrode set to the DC excitation voltage. The second of these excitation control switches, $S3$, is in phase with the reset switch, $S1$, and connects the excitation side of the electrodes to ground. Ignoring all the sensing electrodes except $C_{11}$, and assuming $S1$, $M_{R1}$, and $M_{11}$ act as ideal short circuits, with $S1$ and $S3$ ideal open circuits, applying Kirchhoff's current law (KCL) at the inverting input of the opamp yields:

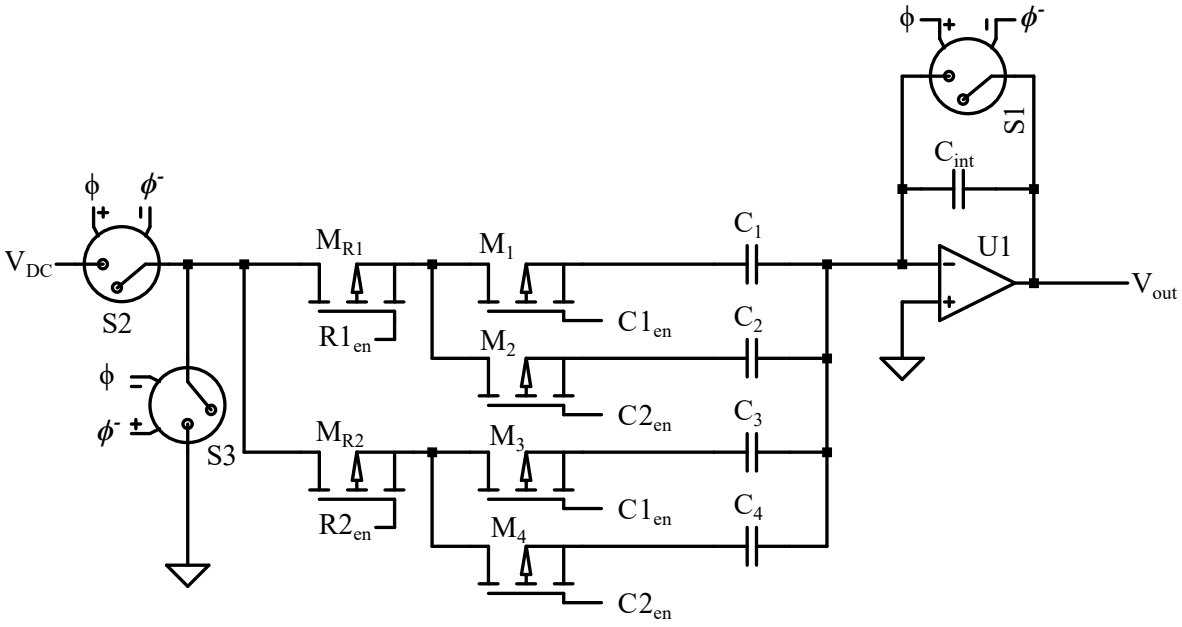



**Figure 4.7.** CVC schematic for 4 sets of electrodes ($C_{11}$, $C_{12}$, $C_{21}$, $C_{22}$).

$$\frac{V^- - V_{DC}}{Z_{11}} = \frac{V^- - V_{out}}{Z_{int}}, \tag{4.13}$$

and from Table 4.2 it can be assumed that $V^- \approx V^+ = 0$ V, which means (4.13) can be rewritten to give the transfer function of the CVC as

$$V_{out} = \frac{Z_{11}}{Z_{int}} V_{DC} \ , \tag{4.14}$$

which simplifies to

$$V_{out} = \frac{C_{11}}{C_{int}} V_{DC} \ , \tag{4.15}$$

for the case of purely capacitive impedances.

The output of the CVC is, therefore, proportional to the ratio between capacitances of the sensing electrode and the integration electrode, and the magnitude of the DC excitation voltage. It is important to note, however, that the switching frequency of the reset switches can be used to measure the capacitance from the cell membrane at higher frequencies, as seen in [11] and [9]. Fig. 4.8 shows the timing diagram of one CVC cell with 4 electrodes. These 4 different electrodes are modelled as 4 capacitors of different magnitudes to demonstrate independent measurements during each sensing cycle.

When the reset clock $\phi$ is high, the feedback capacitor is replaced by a short circuit, transforming the integrator into a buffer to allow output. The active-low enable signals for the first column and row are shown, with the anti-phase enable clock for the second row and column implied. PMOS-based enable switches are required to pass $V_{DC}$, which is close to $V_{DD}$ and is therefore better switched through by PMOS devices. This is the reason for using active-low enable signals for sub-electrode addressing. The sequence for $C_{11}, C_{12}, C_{21}, C_{22}$ is annotated for the first occurrence of each electrode and repeats every time the column 1 and row 1 enable signals are pulled low at the same time.

The values for these capacitors are 10, 150, 50, and 80 fF, respectively, and a full calibration curve of the simulated capacitance can be seen in Chapter 5.

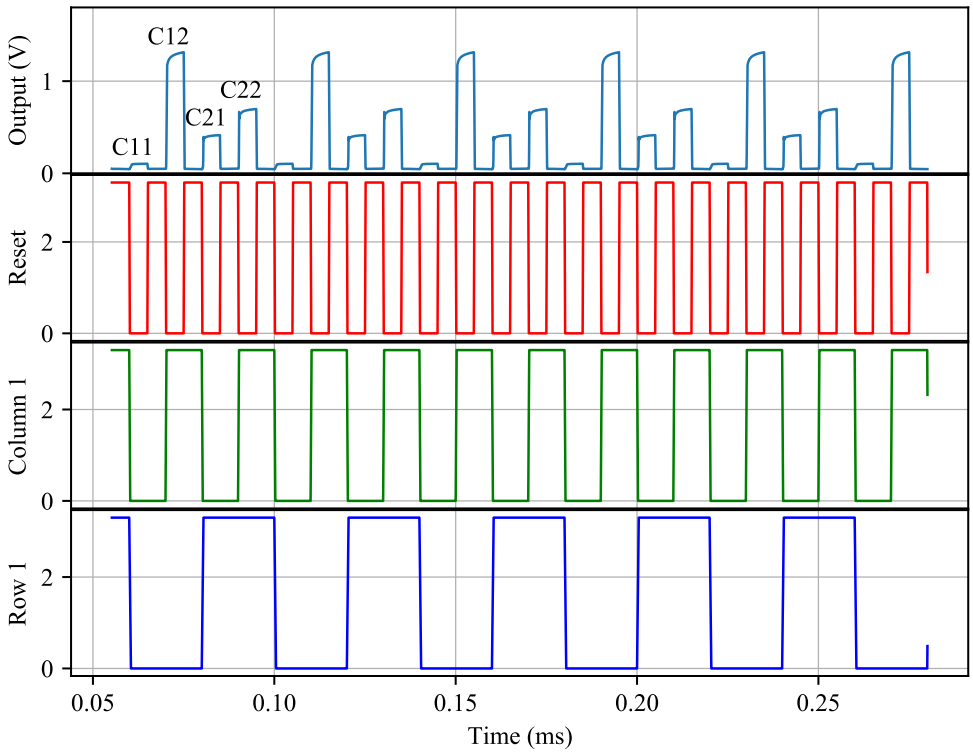



**Figure 4.8.** Timing Diagram of the output of one CVC cell with 4 sets of castellated electrodes.

### 4.3.1 Electrode layout

The next feature that requires attention is the 25 x 25 $\mu m^2$ electrodes used in the sub-cells. Two versions were laid out, namely an IDE version and a castellated version. Since only one set of electrodes could be placed on the manufactured IC, the decision was made to use the castellated layout due to better

expected sensitivity from higher gradient E-fields given by castellated electrodes [50]. The artwork of the castellated electrode is shown in Fig. 4.9.

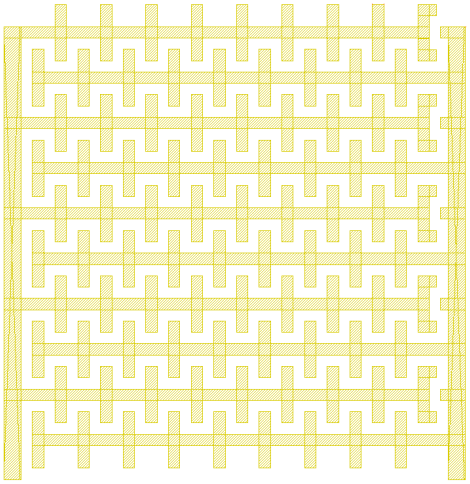


**Figure 4.9.** Layout artwork for one pair of 25x25 $\mu$m castellated electrodes in the third metal layer.

The geometry of the *E. coli* cells and the process limitations were the main guiding factors in determining the finger thickness at this stage of the design. The minimum width for the third metal layer allowable in the process is 0.5 $\mu$m, with the minimum spacing limited to 0.6 $\mu$m.

To ensure that electrodes can be spaced as tightly next to one another as possible, the main fingers on either side were spaced 24.6 $\mu$m apart on their widest separation to account for the spacing required between blocks, meaning no space is lost between adjacent electrode pairs or CVC cells.

## 4.4 ARRAY IMPLEMENTATION AND CHIP LAYOUT

Hierarchical block diagrams are used extensively for further explanation of the interfacing between various components. These interactions will be explained through a bottom-up approach starting with a single CVC cell, working toward the full CVC array, and ending with the logic elements required to activate a single sensing pixel at a time.

### 4.4.1 Capacitance to Voltage Converter Layout

Transmission gate switches are used as integration and reset control switches (S1, S2, S3) in Fig. 4.7. The transmission gate switch consists of the parallel combination of minimum-sized PMOS and NMOS transistors, with the gates of both used as control signals to allow the switch to pass current. This is required since the NMOS transistor passes a strong "0" and a weak "1", while the PMOS transistor

passes a strong "1" and a weak "0". For full conduction, both devices have to be engaged simultaneously, which also requires inverting the active-high control signal $\phi$. Included in the CVC block diagram and the associated circuitry, shown in Fig. 4.10, is a logic inverter for this purpose.

The four capacitors ($C_{11}$, $C_{12}$, $C_{21}$, and $C_{22}$) in Fig. 4.7 are replaced with the castellated electrodes seen in Fig. 4.9.

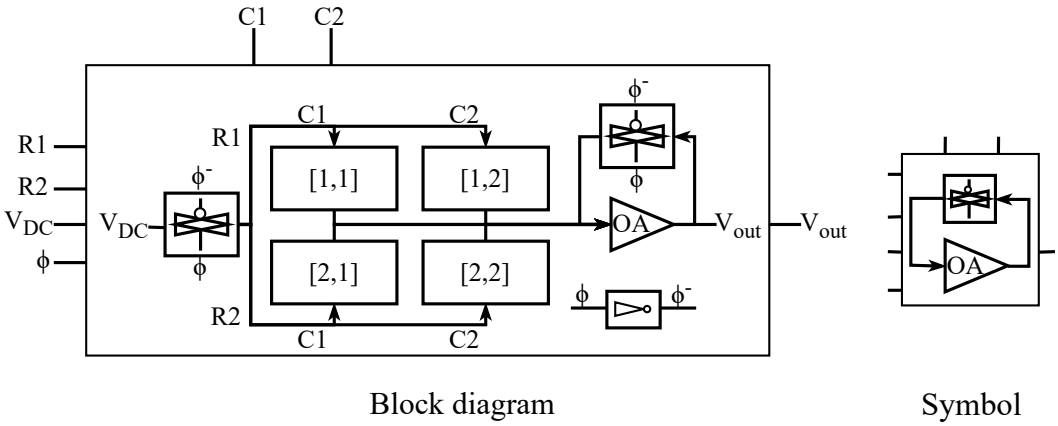



**Figure 4.10.** Hierarchical block diagram of the CVC circuit and the symbol used for this block in higher levels of the hierarchy.

The layout of the CVC comprises the components and circuit elements seen in Figs. 4.7 and 4.10 is limited to 50 x 50 $\mu m^2$ to accommodate four of the electrodes seen in Fig. 4.9. This layout, depicted in Fig. 4.11, shows the opamp from Fig. 4.3 in the top right corner and the integrating capacitor, $C_{int}$, annotated on the left. Control switches for rows and columns are included at the top left and bottom below the opamp, as well as the inverter required to generate $\overline{\phi}$ from $\phi$.

To use this cell as is for all other elements of the 8x8 sensing array, pins are included for enabling rows and columns, $\phi$ control signals, and the DC charging voltage. These pins all enter and exit the cell on either side of the layout at the same location, which allows for simple butting connections between adjacent sensing cells and aligns the sensing cells to a fixed grid.

These connections are annotated, as are the locations of the four sets of electrodes per CVC cell, with $C_{11}$ shown with a dotted-line box.

The connections for the rail voltages, $V_{DD}$ and $V_{SS}$, are included in the layout for the opamp, and as such are also in fixed positions inside the CVC cell.

Checks for design rule and layout versus schematic comparison (DRC and LVS) are used to ensure the layout meets requirements set by the foundry and matches the schematic, after which the CVC cell can be used as a verified component in higher levels of the design hierarchy.

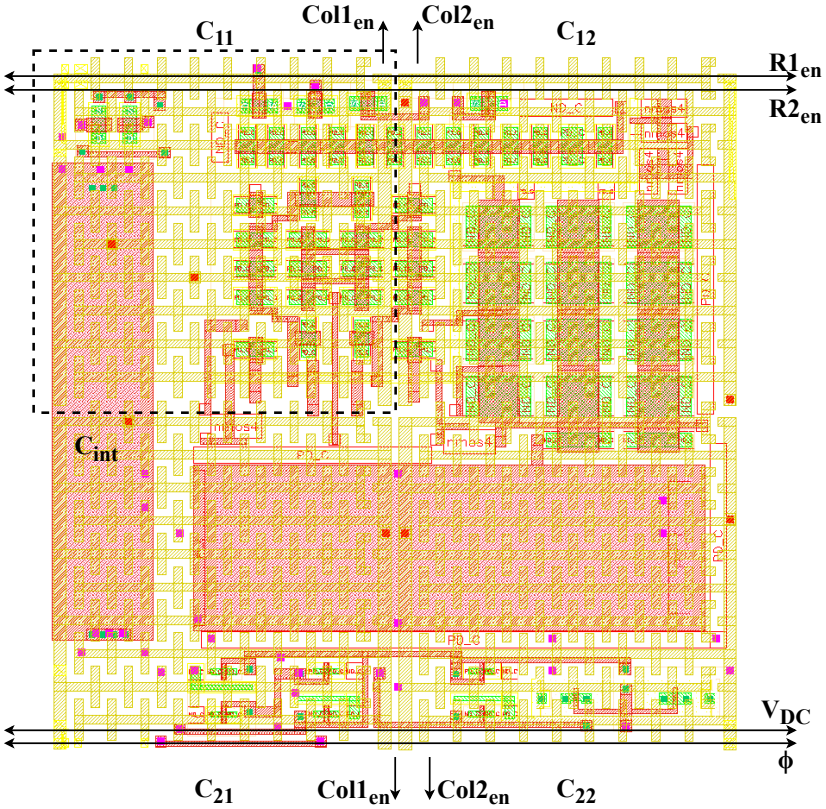



**Figure 4.11.** Layout artwork for one CVC cell, including each of the four sub-electrodes and connections for the row and column control signals.

### 4.4.2 Array control and readout

Eight verified CVC cells form a row of CVC cells with two rows of electrodes.

The row control pins for these two sub-rows, the DC charging voltage, and $\phi$ control signals are connected across all eight cells in the row.

Each CVC cell requires control signals for each of its two columns. The row of 8 CVC cells, therefore, requires 16 column control signals as seen in the hierarchical block symbols in Fig. 4.12(a) and (b). Adding this level in the hierarchy is not strictly necessary, but finishing a row of cells before assembling

an array of cells simplifies debugging potential DRC and LVS problems during integration. This approach to hierarchical design is standard practice in IC design.

Once this row has passed these checks as a verified component, it can be copied 7 more times to create the 8x8 CVC array with 16x16 electrodes.

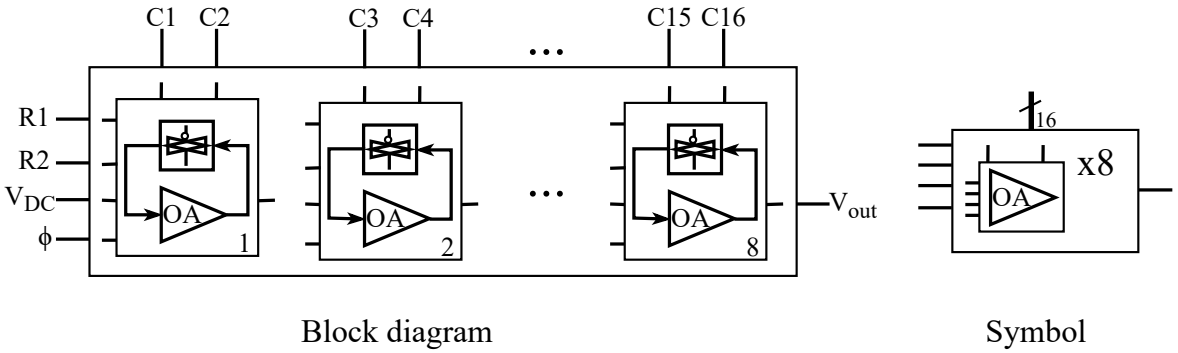



**Figure 4.12.** Hierarchical block diagram of a row of CVC blocks showing pins for interfacing and the symbol used for this block in higher levels of the hierarchy.

Two cyclic shift registers are used for row and column control for the 256 electrodes in the sensing array. These two shift registers are identical and have been designed to be reused as a component. Fig. 4.13 shows 16 D flip-flops, with the the output of one feeding into the input of the next and a common clock source driving them all. The output of the 16th flip-flop and a pin for the starting signal shifting are combined in a logic OR network to ensure that the shift register can start shifting when required and continues shifting once the control **0** has passed through the shift register. The logical OR is implemented using 2 NOR gates: the first calculating the inverse OR of the *start* signal and the output from *D15*, and the second NOR gate with its inputs tied together to act as a logic inverter. This ensures positive logic for the control pulse passing through and prevents its inversion, which would permanently disable the logic-low activated switches from Fig. 4.7.

Eight rows from Fig. 4.12 are aligned using the 16 column enable pins on the sensing cells. These column enable tracks are then connected vertically across all 8 rows. The 16 D flip-flop outputs are taken from each of the circular shift registers and connected to the row and column control signals.

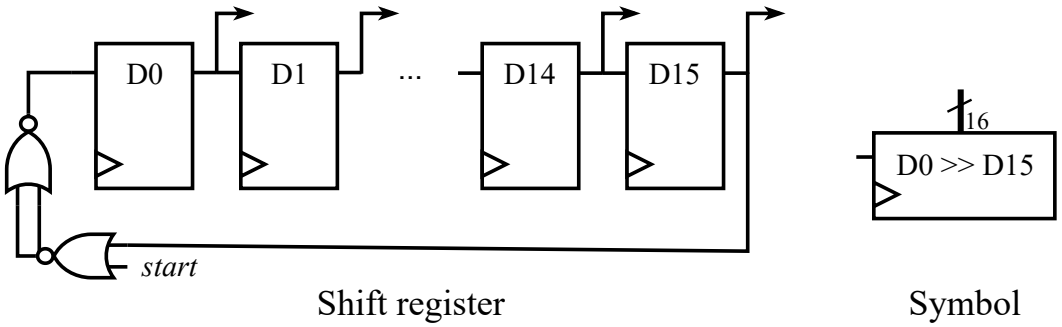



**Figure 4.13.** Cyclic shift register used for CVC array control and the symbol used in higher levels of the hierarchy.

Pins are added for separate row and column clocks from off-chip, with the period of the row clock specified to be as long as 16 rising edges of the column clock. Separate pins for the row and column *start* signals are added for external access off-chip, though in practice these are likely going to be tied together to ensure the rows and columns are synchronised. To ensure this is the case, the first D flip-flop output of both the row and column circular shift register are taken as separate output pins to be read off-chip. These pulses can then be used to verify proper digital functionality and array cycling with an external testing device before the CVC is used. External pins are also added for the reset clock, $\phi$, and the DC charging voltage as seen Fig. 4.7, with these signals being shared across all the sensing cells.

Finally, all 64 opamp outputs are tied together and attached to the non-inverting input of another opamp placed externally to the CVC array itself. The inverting input of this opamp is then attached to a pin that allows for the opamp to be connected in an amplifier of voltage buffer configuration off-chip. Not only does this isolate individual CVC cells from having to drive a larger off-chip resistance, but the freedom to add an extra voltage gain stage before digitising the result allows extension of the sensing range of the CVC cells.

## 4.5 CHAPTER SUMMARY

This chapter discussed the integrated circuit components designed for the AMS 0.35µm CMOS process.

Section 4.2 outlined the specifications and design constraints for the operational amplifier, after which the design and layout of a two-stage Miller compensated opamp with a limited footprint was presented.

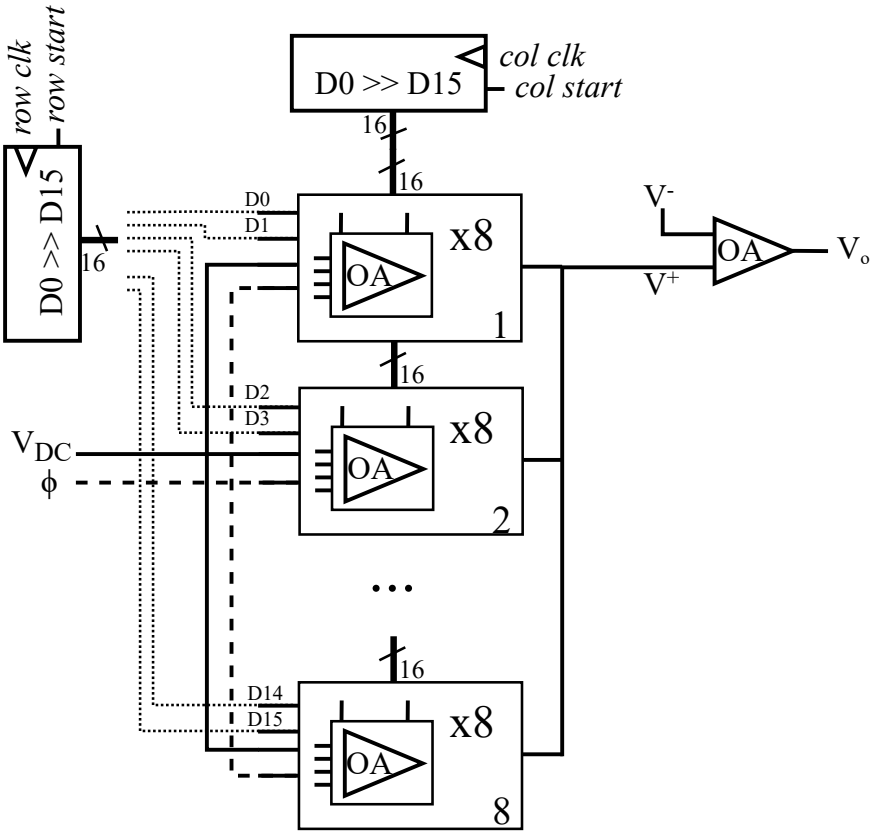



**Figure 4.14.** Top level hierarchy of the CVC sensing array and its control.

This Section also includes post-layout corner simulations of the opamp's DC, AC, and transient performance. Section 4.3 showed the design of an on-chip capacitance-to-voltage converter circuit used in the array-based CVC sensor, including the electrical considerations for interacting with one of these CVC functional blocks, and the layout of electrodes in the third metal layer that is used in the CVC. Finally, Section 4.4 discussed the hierarchical design flow required to deliver a verified layout of the CVC array and its cell-addressing circuitry.

# CHAPTER 5 RESULTS

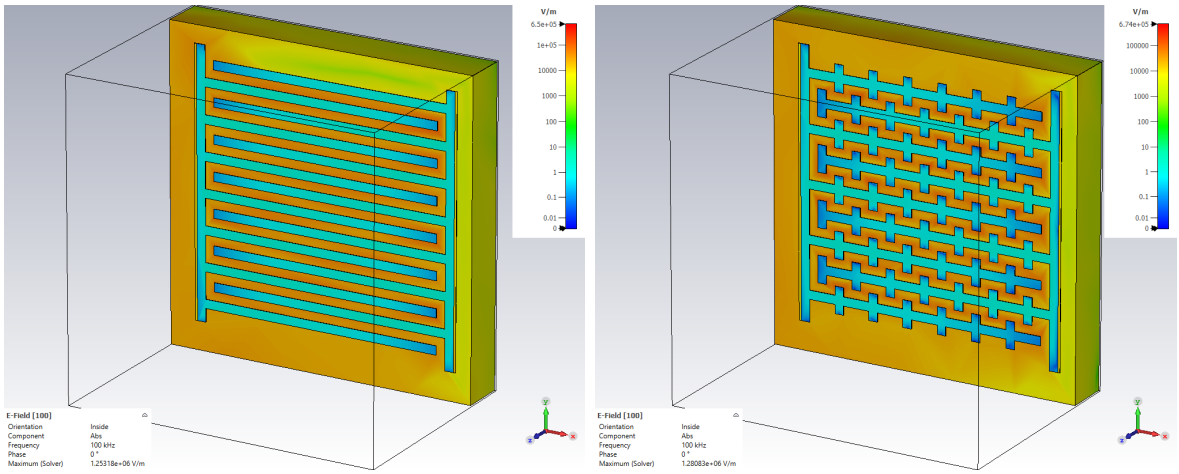
## 5.1 CHAPTER OVERVIEW

This chapter presents the results gathered from the experiments explained in Chapter 3. Section 5.2 shows the results from CST finite element analysis simulations, starting with the distribution and magnitude of electric fields for the various electrodes considered, before presenting and discussing the capacitance and each electrode's response to electrical cell substitutes. Section 5.3 presents the results obtained when classifying the performance of a number of commercial and low-cost electrodes in the presence of 3 µm polystyrene microbeads using a laboratory-based LCR meter, as well as the performance of a subset of these electrodes in the presence of *E. coli* cells at various concentrations, validated using standard bacterial growth monitoring techniques. Section 5.4 provides a comparison of the simulated and measured results of the opamp used in the low-cost biosensor prototype, as well as the results of repeated 3 µm microbead experiments conducted using the biosensor prototype.

## 5.2 SIMULATION RESULTS

### 5.2.1 Electric field distribution

When considering the colours of the electric field distribution shown in Figs. 5.1-5.3, it is important to note that the colours on sub-figures do not necessarily correspond to the exact same electric field magnitude. This is because CST-MWS has an autoscaling function that automatically fits contour colours to the most appropriate range for the specific result. Therefore, since the absolute maxima in the castellated case in Figs. 5.1(b) and 5.2(b) are higher than their respective IDE cases (Figs. 5.1(a) and 5.2(a)), the colour distribution is different and close attention has to be paid to the E-field scaling in the top-right corner. This scaling has been made as close as possible when comparing the subfigures. In Fig. 5.1, the 2 mm droplet placed on top of the electrode has been hidden to show what electric fields on the surface of the electrode look like, while Fig. 5.2 shows a section view through the centre of the electrode and the droplet.



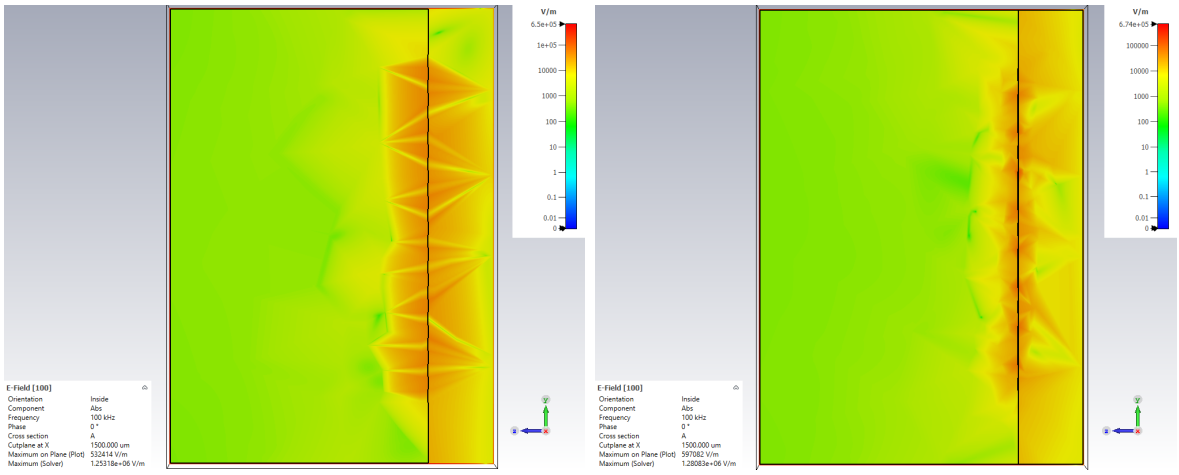
**(a)** Interdigitated electrode (1.25 MV/m). **(b)** Castellated electrode (1.28 MV/m).

**Figure 5.1.** Top view of the electric field distribution of the two 3x3 mm electrodes on the paper substrate with the droplet hidden.

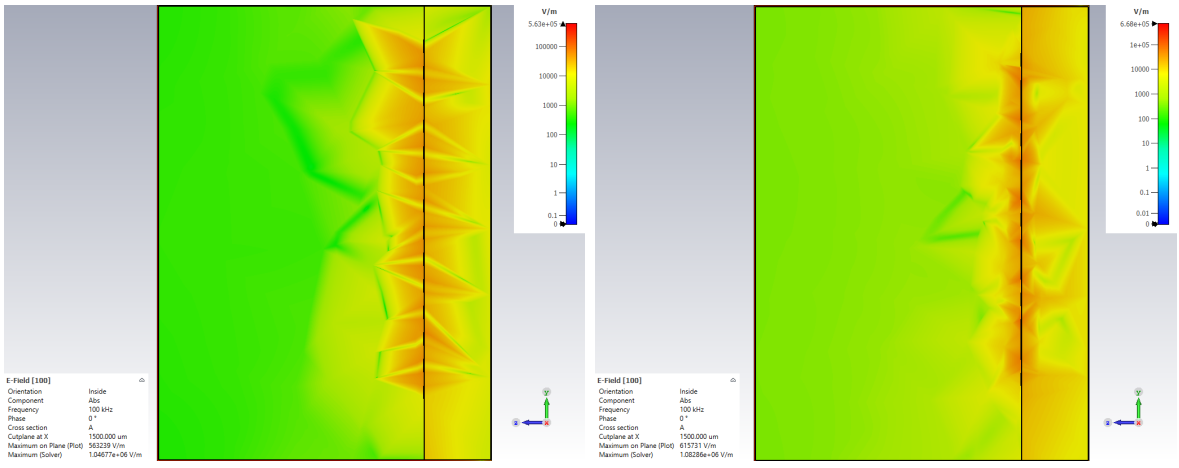
Regardless of feature size, electrode geometry or area, or materials considered, the IDE shows an approximately uniform electric field on the top of, and between the fingers of the electrodes. An example is seen in Fig. 5.1(a) for a gold IDE on a paper substrate. The castellated electrode in Fig. 5.1(b), however, contains non-uniform fields both between and on top of the fingers. Local maxima can be seen at the centre of the substrate between fingers, specifically at the corners of the sub-fingers. An example is seen in Fig. 5.1(b) for a gold castellated electrode on a paper substrate. In both models seen in Fig. 5.1, the 5V stimulus voltage is applied to the set of fingers on the left, but both sets demonstrate the highest field on the surface of the fingers closer to where the horizontal fingers join the vertical main fingers. The castellated electrode, however, demonstrates a higher variation over the width of the fingers than the IDE. Interestingly, the field strength on the surface of the electrodes is approximately 1 V/m in both cases and much larger between fingers. The electrodes shown in Fig. 5.1 are the 100 µm width features on the 3x3 mm paper electrodes.

Using two different substrates, Fig. 5.2 shows sections of an electrode setup that includes the droplet to show the penetration of the E-field into the droplet. The section view is dominated by the 2 mm droplet on the left in both cases, with the 5 µm thick electrodes on the far right at the boundary between the droplet and the 500 µm substrate. Figs. 5.2(a) and 5.2(b) show the same 3x3 mm paper electrode with 100 µm feature sizes of Fig. 5.1. Figs. 5.2(c) and 5.2(d) show the FR4 substrate.

It is immediately evident from the branching of the yellow lines in Fig. 5.2(a) that the mesh generated in the IDE case is not as fine as in the castellated case in Fig. 5.2(b). The reason for this discrepancy is likely due to the built-in mesh optimisation feature optimising the mesh size around the smaller features of the perpendicular sub-fingers in the castellated case. Since these are not included in the IDE, the mesh is not as fine.



**(a)** Interdigitated electrode on paper (1.25 MV/m). **(b)** Castellated electrode on paper (1.28 MV/m).



**(c)** Interdigitated electrode on FR4 (1.04 MV/m). **(d)** Castellated electrode on FR4 (1.08 MV/m).

**Figure 5.2.** Cross section of the electric field distribution of two 3x3 mm electrodes on paper and FR4 substrate. In each instance, the vertical black line denoting the electrodes separates the 2 mm liquid droplet to the left and the 500 µm substrate to the right.

Comparing the distribution of the E-fields between Figs. 5.2(a) and 5.2(b) for the paper substrate,

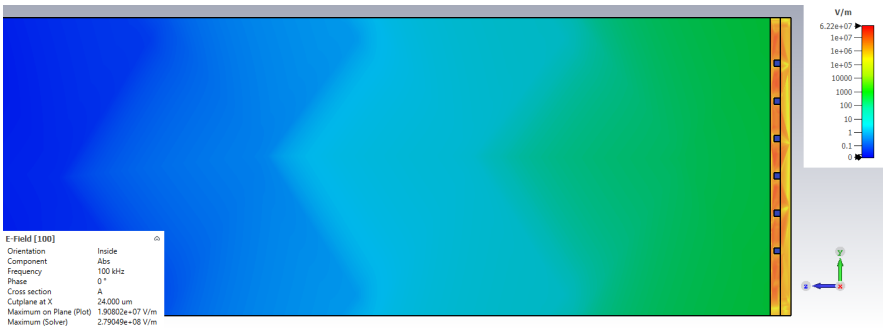
the fields in both cases do not penetrate more than the thickness of the substrate (500 µm) into the droplet. The strength of the E-field decays significantly from the surface of the electrode as seen in [13], which serves as motivation for the use of microfluidics and cell manipulation techniques in other applications as seen in [81]. What this means for droplet-based or electrode-dipping-based measurements is that these methods require proper agitation of the sample before it is measured. It is also evident that a significant portion of the electrical energy applied to the surface of the electrodes goes toward generating an E-field in the substrate to the right of the dividing line, which means this energy is not used in sensing cells near the electrode surface.

For a fair comparison of the effect of the substrate on the electric field distribution, the substrate material in Fig. 5.2 is substituted with FR4. Although the simulated substrate is thinner than the physical FR4 substrate, the distribution of the E-field is the same despite differences in E-field strength. For both geometric cases, the electrode on the FR4 substrate shows a slightly larger maximum: the paper substrate has 597 and 532 kV/m for the castellated and IDE, respectively, and 615 and 563 kV/m on the FR4 substrate. The E-field distribution, in either geometric case, is very similar between substrates, with the castellated electrode showing a higher magnitude in the area immediately surrounding the electrode on both the sample and substrate sides. This high field strength dissipates a short distance into the sample and an even shorter distance into the substrate in both cases, with the FR4 in the castellated case (Fig. 5.2(d)) containing lower field strength in the area underneath the electrodes than its paper counterpart (Fig. 5.2(b)). The E-fields seen in both IDE cases seem to penetrate further into the droplet area than either castellated electrode, though the regular shape of the colour distribution indicates that large local meshing in this area may have contributed to this deep E-field penetration. Further into the droplet, the colour of the paper substrate (Fig. 5.2(a)) suggests that the field strength is higher in this region when compared to the FR4 version (Fig. 5.2(c)), which supports the notion that the FR4 substrate absorbs more of the electrical energy than a paper-based alternative. Although the difference in the castellated case is smaller, the E-field magnitude in the FR4 substrate in Fig. 5.2(d) is slightly higher than its paper-based counterpart. At the scale of these electrodes, the thickness of the substrate itself plays a significant role in the attenuation of electrical energy, as the majority of the electrical energy radiated to the side of the substrate is spent within the first 500 µm, or 100 times the thickness of the electrodes. If the substrate could be made thinner, the fields radiating from the back of the electrode may be considered an extension of the effective sensing volume, though only for an electrode in suspension (such as the setup shown in Fig. 3.6).

Three properties of the distribution of cells in simulation contribute to their negligible effect on the E-field distribution: the cells are an order of magnitude smaller than the smallest feature size considered, they are spaced homogeneously in the water solution rather than appearing in clumps or collections of colonies, and the absolute number of cells in any given simulation is extremely low for the size of the electrode since the simulations are focused on the potential of low cell concentration detection. Zooming in to look at a section view of any particular measurement setup including cells shows that the electric field is homogeneous across the cell. This observation is expected and explained by the fact that the E-fields and capacitance for these simulations were extracted at 100 kHz, a frequency where the permittivity of the outer membrane is constant and distinct [28]. Dielectric dispersion of the cell membrane permittivity seen at frequencies up to 10 MHz means higher frequencies might be appropriate for investigation. Since the model used does not explicitly include the membrane as a separate physical feature, the electric fields are permitted to penetrate deeper than would typically be seen in a more detailed simulation using the complex multi-shell models from [27] or [28].

Looking forward to more expanded use of LoCMOS devices in low-cost biosensor applications, Fig. 5.3 shows the distribution of the E-field through a section of the castellated electrode shown in Fig. 4.9 as designed for the array-based biosensor in CMOS. Cells are distributed in a 100 µm droplet on the surface of the chip electrode shown on the left with the aluminium electrodes embedded between two layers of dielectric on the right.

The majority of the electric field in the cell-less case (Fig. 5.3(a)) is contained in the first third of the droplet closest to the electrode, which corresponds to the result seen in the discrete electrode case in Fig. 5.2. For a droplet of this size, the volume is calculated as 62500 $\mu m^3$, and with a single cell added for simulation, this translates to a concentration of $6.25 \times 10^8$ cells/mL. This has a substantial effect on the maximum observed E-field, increasing from $6.22 \times 10^4$ to $1.06 \times 10^5$ kV/m, with this larger E-field distributed deeper into the droplet in Fig. 5.3(a) than in Fig. 5.3(b). This is the only electrode area with feature sizes comparable to the actual *E. coli* cells, with the single cell seen slightly above the surface of the dielectric layer covering the electrode in Fig. 5.3(b). This section view more clearly shows the gaps between electrode fingers from the castellated geometry, with the gaps corresponding to the length of one sub-finger and the space required between fingers (see (3.2)). From this section through the electrodes, it is also evident that the E-field in the electrode fingers themselves is much lower than in the substrate, similar to the field distributions seen on the electrode surface in Fig. 5.1. The higher conductivity of the electrode materials relative to the substrate materials means that the




**(a)** Section view of the LoCMOS electrode with no cells present.


**(b)** Section view of the LoCMOS electrode with an *E. coli* cell present.

**Figure 5.3.** Section view of the 25x25 µm LoCMOS castellated electrode showing the E-field distribution in a 100 µm droplet. The section view is translated such that the difference can be seen between the absence and presence of an *E. coli* cell.

energy from the voltage applied to the electrodes is mostly consumed within the material surrounding them.

### 5.2.2 Electric field magnitude

The maximum electric field strength is extracted for each of the simulation runs conducted with no cells present, and a summary of these values for the different sizes, substrates, geometries, and materials considered in the simulations is available in Table 5.1. The different electrode setups are grouped according to total area (the footprint of the electrode), the substrate used, the size of the features present on the electrode and the material considered for the electrode. In each instance, the maximum field strength for both the IDE and the castellated electrode is provided side by side for an immediate comparison. LoCMOS electrodes are included at the bottom of the table in a similar fashion. The first of the two LoCMOS electrodes is an electrode that could be used as a single electrode in a bulk solution, similar to the low-cost alternatives and the second LoCMOS electrode has the same

25x25 µm$^2$ footprint for an array-like implementation. The LoCMOS electrodes are embedded inside two 1 µm layers of lossy silicon ($\varepsilon = 11.9$) with the aluminium electrodes themself a thickness of 640 nm. The droplet containing the *E. coli* cell substitutes is placed on top of the intermetal dielectric protecting the electrodes.

**Table 5.1.** Maximum simulated electric field strength for different electrode geometries with no cells present.

| Electrode area (mm x mm) | Substrate material | Finger/gap width (µm) | Electrode material | Maximum electric field (kV/m) | |
|---|---|---|---|---|---|
| | | | | IDE | Castellated |
| 6 x 6 | FR4 | 25 | Gold | 1198.9 | 2825.0 |
| | | 50 | Gold | 981.3 | 1033.5 |
| | | 100 | Gold | 1037.1 | 872.0 |
| | | | Pure copper | 1037.0 | 872.4 |
| | | | Silver | 1037.0 | 872.5 |
| | Paper | 100 | Gold | 1278.9 | 1140.7 |
| 3 x 3 | FR4 | 25 | Gold | 1596.7 | 1844.3 |
| | | 50 | Gold | 1082.5 | 1326.2 |
| | | 100 | Gold | 1134.4 | 1163.7 |
| | | | Pure copper | 1134.4. | 1163.7 |
| | | | Silver | 1134.4 | 1163.7 |
| | Paper | 100 | Gold | 1294.8 | 1325.5 |
| 1 x 1 | FR4 | 25 | Gold | 2315.9 | 2274.4 |
| | | 50 | Gold | 505.1 | 1696.0 |
| | | 100 | Gold | 346.4 | 557.1 |
| | | | Pure copper | 346.4 | 557.1 |
| | | | Silver | 346.4 | 557.1 |
| | Paper | 100 | Gold | 1118.1 | 1096.5 |
| 0.5 x 0.5 | $SiO_2$ | 25 | Aluminium | 106 214.0 | 40 905.1 |
| 0.025 x 0.025 | $SiO_2$ | 0.6 | Aluminium | 692 903 | 279 049 |

From Table 5.1, there appears to be an inversion in the maximum field strength demonstrated if the area of the electrode shrinks while keeping the feature size constant at 100 µm finger widths. For the 1x1 $mm^2$ electrodes, the maximum field strength of the castellated electrode is approximately 200 kV/m higher than the IDE case, while the exact opposite is true for the 6x6 $mm^2$ electrode. The cross-over point seems to be close to the area of the 3x3 $mm^2$ electrode since the difference, in this case, is only about 20 kV/m in favour of the castellated electrode. This would suggest that rather than looking purely at electrode area or geometry independently, the size ratio between these measures can be used as a parameter of interest when designing optimal electrodes, where the ratio is defined as

$$r_s = \frac{w_{electrode}}{w_{fingers}}, \tag{5.1}$$

with $w_{electrode}$ the width of a square electrode and $w_{fingers}$ the width of the fingers on the electrode. Table 5.2 shows the side length of the square electrode and the size of the features used along with the associated size ratio.

**Table 5.2.** Size ratio for low-cost electrodes under investigation.

| Electrode width | Feature size | Size ratio |
|---|---|---|
| 1000 | 25 | 40 |
| | 50 | 20 |
| | 100 | 10 |
| 3000 | 25 | 120 |
| | 50 | 60 |
| | 100 | 30 |
| 6000 | 25 | 240 |
| | 50 | 120 |
| | 100 | 60 |

Comparing the field strength between feature sizes for electrodes of equal area shows that the maximum field strength is at its highest for the smallest feature size. This is unsurprising, since the stimulus voltage (5 V) stays the same across all simulations and a smaller size divisor for the field has to lead to an increase in the field strength. Interestingly, this increase is not proportionally related to the decrease in feature size. The greatest difference can be seen in the 1x1 $mm^2$ IDE: a 50% decrease in feature size from 100 µm to 50 µm leads to a 45% increase in the electric field strength, from 346.4 kV/m to 505.1 kV/m. A further 50% decrease in feature size from 50 µm to 25 µm leads to a 360% increase

in electric field strength. In contrast, the increases in field strength for the castellated electrode are approximately 200% and 30% for the two decreases in feature size, respectively.

The section views in Fig. 5.2 show that there is considerable E-field leakage into the substrate, which is true regardless of the substrate material. Even though the electrical permittivity of paper is approximately half that of the lossy FR4 (4.3 compared to 2.31), the maximum E-field strength between similar geometry electrodes on different substrates is not linearly related to the permittivity. In the 6x6 $mm^2$ case, there is only a 23% and a 26% increase in the case for the IDE and castellated electrodes respectively, while the 3x3 $mm^2$ electrode shows a 14% increase for both electrode geometries. For electrodes with a much smaller total area, however, the difference in maximum E-field strength is significant: the 1x1 $mm^2$ IDE on paper demonstrates a maximum field 2.2 times that seen for FR4, with the field strength on the castellated electrode nearly doubling. This further supports the conclusion that geometry has by far the largest effect on the expected E-field for an electrode.

The LoCMOS electrodes implemented using the topmost metal layer of the 0.35 µm CMOS process were investigated to compare their performance to low-cost off-chip electrodes. The larger of the two electrodes investigated for LoCMOS implementation shows a significantly larger E-field magnitude than its low-cost alternatives with comparable feature sizes, mostly due to its smaller footprint. Although a direct comparison to the 1x1 $mm^2$ electrode would not be a completely fair comparison in this case due to the differing substrate and electrode materials, halving the dimensions leads to an electrode which is a quarter the size of the original while the maximum E-field strength increases by a factor of 10 in the IDE and 40 in the castellated electrode.

Simply, with features much closer in size to the cells targeted, the presence of cells will have a much larger effect on the E-fields. As such, the effect of even a single cell near the electrode surface is much more pronounced than for electrodes of larger footprints. With such small feature sizes, the field strength increases significantly to 692 MV/m and 279 MV/m in the IDE and castellated electrodes respectively, which is an indicator of the effectiveness of such small electrodes in detecting impedance-based changes in the electric field.

### 5.2.3 Simulated Capacitance: low-cost electrodes

The FEM simulations were conducted at 10 kHz - 10 MHz to extract the E-fields and capacitance over this frequency range. All E-field and capacitance results shown are taken from the solver step

at 100 kHz. The permittivity of the outer membrane at this frequency is not yet affected by higher frequency dispersion [28]. Low-cost electrodes with larger areas all demonstrate a capacitance that stays constant from 10 kHz - 1 MHz, with a significantly lower capacitance shown at frequencies above 1 MHz, even when cells are added to the simulation model. Fig. 5.4 shows the capacitance for the low-cost gold electrodes on the FR4 substrate when no cells are present for the different electrode areas, feature sizes, and geometries. Since the vertical capacitance axis uses logarithmic divisions, the changes due to feature size on electrodes with identical areas are slightly obscured, but this is necessary to compare the capacitance of different electrode areas.

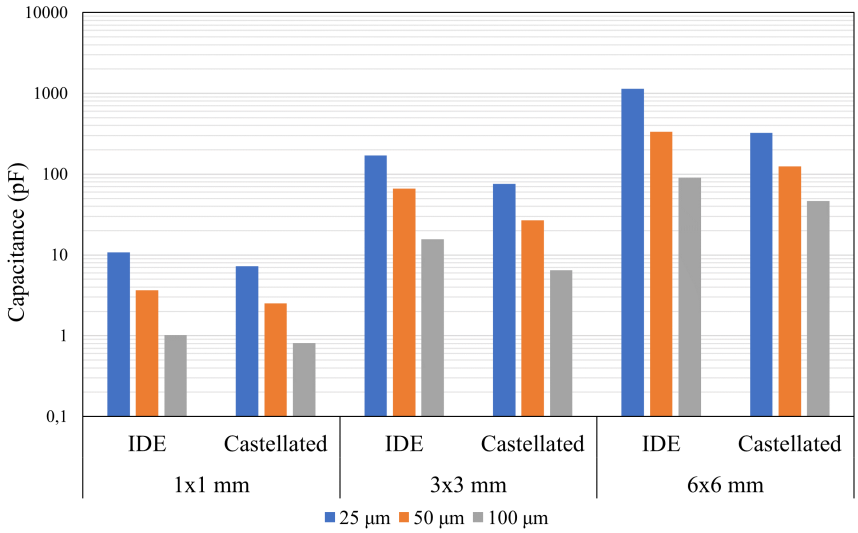



**Figure 5.4.** Capacitance change of low-cost electrodes across various electrode geometries.

Similar to the E-fields seen in Table 5.1, capacitance is lower for larger feature sizes when comparing within identical electrode areas, with the capacitance dropping approximately half a decade in the change from 25 µm to 50 µm, and half a decade further when changing the feature size from 50 µm to 100 µm. This trend is repeated across all electrode areas and both geometries considered. Comparing the two geometries within a constant electrode area, the castellated electrode shows a lower capacitance than its IDE counterpart regardless of the feature size considered. The capacitance of the castellated electrode is between 40% and 45% that of the IDE for the 3x3 $mm^2$ footprint, with its size varying between 67% and 80% over the three feature sizes in the 1x1 $mm^2$ case and between 28% and 51% in the 6x6 $mm^2$ case. This seems to suggest that a more reliable capacitance difference between the two geometries may be obtained for a specific combination of feature sizes and electrode area. Finally, in line with (2.2), more fingers in an electrode will lead to an increase in capacitance, which is supported by the substantial increases in capacitance for electrodes of increasing area. The capacitance of the 100

µm feature-size IDE increased by nearly a decade for each increase in electrode area. The castellated electrode in the same cases showed a similar result, with the change from 1x1 $mm^2$ to 3x3 $mm^2$being slightly larger than from 3x3 $mm^2$ to 6x6 $mm^2$.

As the spread in capacitance for the low-cost electrodes in Fig. 5.4 is from 1 pF to 1 nF, a comparison of electrode performance for increased cell counts is conducted using the relative change in capacitance from the baseline level seen in Fig. 5.4. Further, absolute capacitive change in the larger capacitance electrodes may obscure changes in the smaller capacitance electrodes, so the % of relative change in capacitance from an empty electrode will be used as a metric to assess the effectiveness of the various electrodes. This relative change can will be referred to as the detection sensitivity. Fig. 5.5 shows this relative capacitance change on the 3x3 $mm^2$ electrode with gold fingers for both the FR4 and paper substrates.

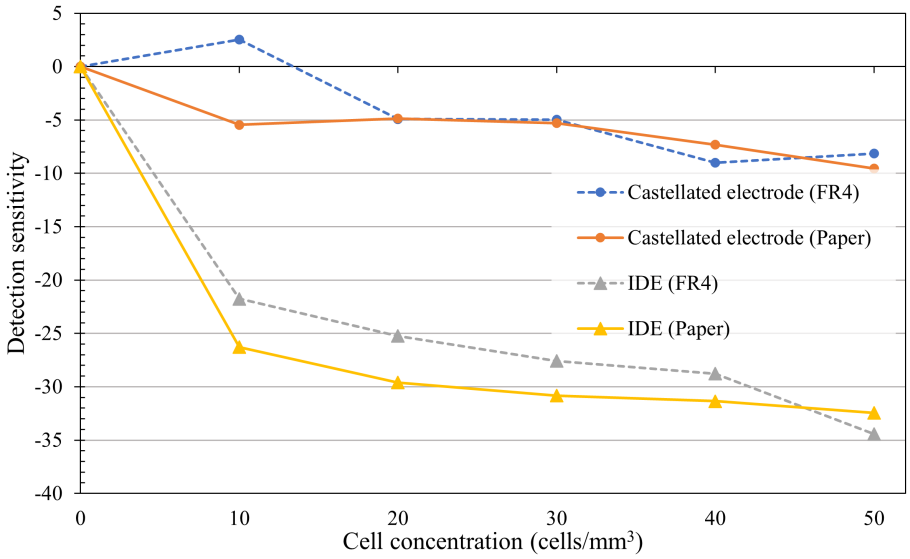



**Figure 5.5.** Relative capacitance change for 100 µm finger width electrodes on 3x3 $mm^2$ FR4 and paper substrates.

A different substrate does not seem to have a significant effect on the capacitance, with the largest difference in Fig. 5.5 attributable to the geometry of the electrode. In both cases, however, the paper substrate shows a larger relative deviation than its FR4 counterpart, suggesting that if an electrode is patterned on paper, its lower relative permittivity may improve the sensitivity of the electrode. This slight improvement in sensitivity when using a paper substrate as opposed to FR4 counts in its favour as a candidate for low-cost electrode manufacturing. Fig. 5.6 shows the relative change in capacitance

for the three electrode materials considered: gold, silver, and copper for both the IDE and castellated 100 µm width electrode on the largest low-cost 6x6 $mm^2$ substrate.

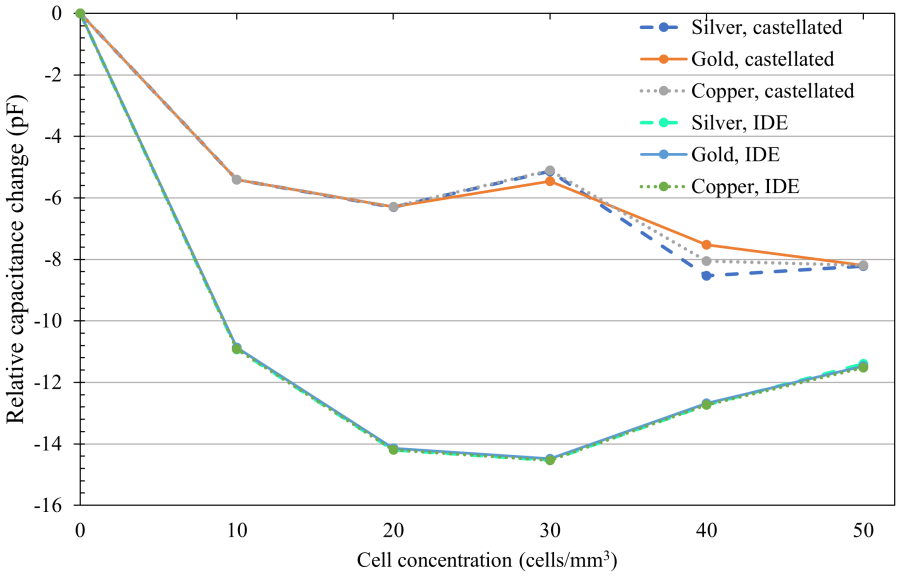



**Figure 5.6.** Relative capacitance change for 100 µm finger width gold, silver, and copper electrodes in 6x6 mm low-cost electrodes.

It is clear from Chapter 3 that the permittivity of gold, silver and copper are fairly close to one another ($4.56\times10^7$, $5.96\times10^7$, $6.3\times10^7$ S/m respectively), which leads to the assumption that results from these different materials should also be fairly close to one another. This is indeed the case, with the traces for the three different materials of the same electrode geometry in Fig. 5.6 nearly on top of one another. The biggest deviation is seen at 40 cells/mL in the castellated electrode, with the capacitance values for the three different materials slightly spread. Any difference in the IDE due to materials is negligible, as all three lines are on top of one another throughout regardless of the cell concentration.

The IDE shows an average relative change of -11% for the first step of 10 cells/mL compared to the -5.8% seen for the same step in the castellated case. This shows initial promise that the IDE is more effective at detecting extremely low cell concentrations than castellated electrodes. A monotonic decrease in the capacitance is seen in the castellated electrode, however, which seems to show this would be the more suitable electrode to use for a larger range of unknown cell concentrations. It is possible that the outlier point on the three castellated lines at 30 cells/mL is related to cell position rather than the material properties, as the positioning of cells relative to the electrode surface has a

significant impact on the mesh generated, and consequently the capacitance results recorded. This theory is supported by the fact that the effect is the same across the three materials considered when the simulation is set up to lower the effect of this phenomenon. The inversion seen in the detection sensitivity in capacitance for the IDE is not isolated to this electrode and can also be seen 100 µm line in Fig. 5.7. Two preliminary conclusions can be drawn from this observation: 100 µm width as a feature size is likely too big in a bulk measurement electrode as large as the low-cost electrodes considered, but also if this is the achievable manufacturing limit for low-cost electrodes it might be beneficial to consider using the castellated electrode for its predictable capacitance response. Confirming that material does not have the biggest effect on the measurement performance of the electrodes, the effect of electrode geometry is studied in Fig. 5.7 for different feature sizes on a 1x1 mm$^2$ electrode. A relative decrease in capacitance suggests that the effect of added cells adds capacitance as a series capacitive element. This relative change is the sensitivity of the electrode.

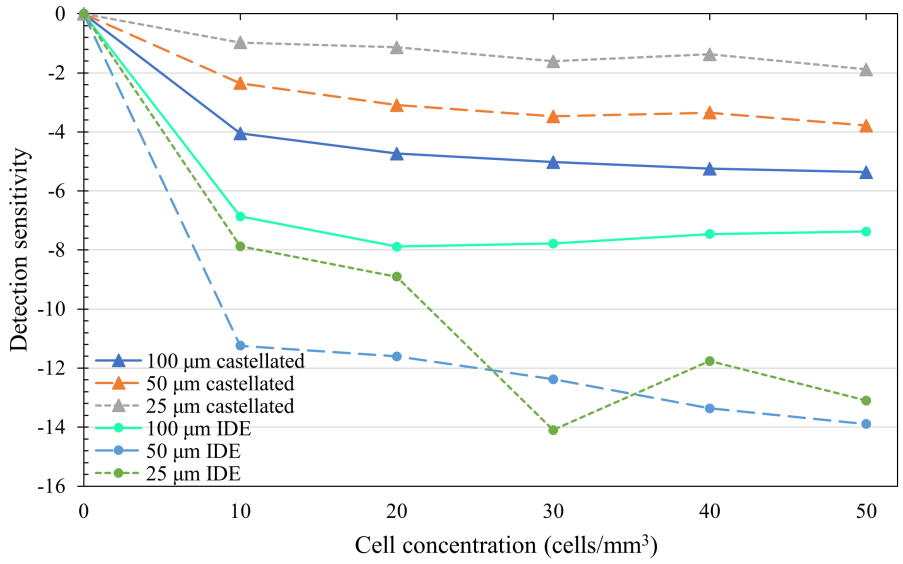



**Figure 5.7.** Sensitivity of different combinations of feature size and geometry in a low-cost 1x1 mm electrode.

Similar to the 6x6 mm$^2$ electrode shown in Fig 5.6, the relative capacitance change of the 100 µm IDE on the 1x1 mm$^2$ substrate shows a minimum at 20 cells/mL before decreasing for higher cell concentrations. As before, the castellated electrode shows a smaller change for increased cell concentration than the IDE, with a decrease in the effectiveness of the castellated electrode seen as the features get smaller. All three variants start with a notable jump in the relative capacitance change

from no cells to a concentration of 10 cells/mL, with the 25 µm and 50 µm showing a slight inversion at 40 cells/mL. The smaller feature size IDEs do not follow the inversion after 20 cells/mL seen in the 6x6 $mm^2$ electrode in Fig. 5.6 or in the corresponding 100 µm fingers shown in this plot. Instead, a monotonic decrease in capacitance is seen for an increase in cell concentration, a finding which supports results initially seen from similar simulations in [13]. This monotonic decrease is broken in the 25 µm case by an outlier data point at 30 cells/mL, which can be explained in the same manner as the outlier seen in Fig. 5.6. If this outlier is not considered, the 25 µm IDE shows the best performance, as it shows the highest deviation with the most regular intervals between measurements. It provides the highest size ratio of 240, with the second-highest size ratio of 120 provided by the 50 µm features. This shows initial promise for the size ratio of electrodes as a tool for quantifying the potential effectiveness of an electrode and simplifying the choice of an appropriate electrode.

For a comparison of performance on different electrode areas, Fig. 5.8 shows the detection sensitivity for different combinations of geometry on the 3x3 $mm^2$ electrode. The performance of the 3x3 $mm^2$ electrode is much less predictable than its 1x1 $mm^2$ counterpart, with the 25 µm castellated electrode showing an increase in relative capacitance for higher cell concentrations, peaking at 8% for 40 cells/mL. By contrast, its 50 µm and 100 µm counterparts show a slight initial increase before inverting and showing a decrease in capacitance from 30 and 10 cells/mL onward, respectively. In the case of the 50 µm castellated electrode, which has a size ratio of 60, the change is so negligible that it cannot reliably be used as a capacitance measurement. An increase in capacitance as seen in all the castellated electrodes is contrary to the results seen in the smaller 1x1 $mm^2$ and the larger 6x6$^2$ mm electrodes.

As before, the larger IDEs on the 3x3 $mm^2$ electrode demonstrate a larger deviation at higher cell concentrations than their castellated counterparts. The 100 µm and 50 µm reach a maximum deviation of -28% and -34% at 40 and 50 cells/mL, respectively. The 50 µm IDE, with a size ratio of 60, shows a significant inversion from 40 to 50 cells/mL, which could be an outlier caused by inconsistent meshing due to the positioning of the cells. From the first increase of 0 to 10 cells/mL, however, these larger IDEs demonstrate what seems like an exceptionally large change in capacitance when compared to the 0 and 7% relative change seen in the other geometries considered in this set, and is even larger than the -12% seen in the 50 µm IDE in Fig. 5.7. The 25 µm IDE, with a size ratio of 120, behaves completely contrary to its larger counterparts, and similarly to the 50 µm castellated electrode cannot reliably be used as an indicator for change in capacitance. Given the sporadic performances of all the

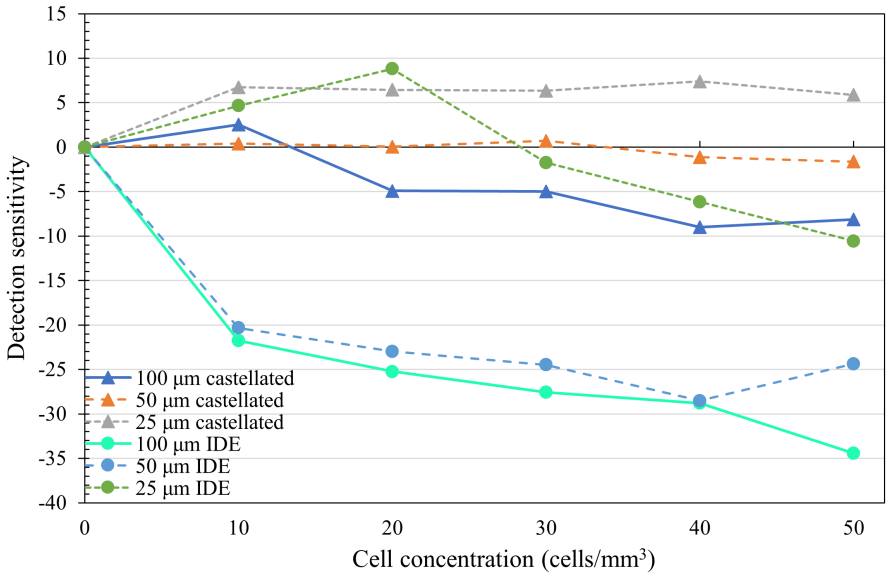



**Figure 5.8.** Sensitivity of different combinations of feature size and geometry in a low-cost 3x3 mm$^2$ electrode.

geometries considered, it is likely that the 3x3 mm$^2$ electrode is simply not suitable as an electrode in the manner it was investigated, further supporting the hypothesis that a smaller footprint electrode is more ideal for measuring *E. coli* cells or bacterial cells in general.

### 5.2.4 Simulated Capacitance: LoCMOS electrodes

Table 5.3 summarises the capacitance of the monolithic 500x500 µm$^2$ and array-like 25x25 µm LoCMOS electrodes. The 500x500 µm$^2$ castellated electrode has a 10% larger capacitance than its IDE counterpart, contrary to the results seen in the larger low-cost electrodes. This could be due to the effect of a smaller electrode combined with a comparably large feature size magnified in the castellated case. With features of 25 µm on an electrode with dimensions of 500 µm, the size ratio is 20, which is the second-smallest ratio next to the 100 µm features on the 1x1 mm electrode, which has a size ratio of 10. The only other electrode with this size ratio is the 50 µm finger width on the 1x1 mm$^2$ electrode, where this phenomenon is likely suppressed due to the larger features and larger electrode. With a size ratio of 41.67, the 25x25 µm$^2$ electrode with 0.6 µm finger width is closest to the 1x1 mm$^2$ electrode with 25 µm finger, which has a size ratio of 40. This is also the only electrode with finger widths that are comparable to the dimensions of a single *E. coli* cell.

Figs. 5.9 and 5.10 show the change in relative capacitance in the presence of cells. Due to the small footprint of these electrodes, the volume of liquid above their surface is significantly smaller than the

**Table 5.3.** Size ratio and simulated capacitance of LoCMOS electrodes.

| Area (μm$^2$) | Size ratio | IDE (pF) | Castellated (pF) |
|---|---|---|---|
| 500x500 | 20 | 0.882 | 0.954 |
| 25x25 | 41.67 | 0.961 | 0.129 |

volume of liquid used for the low-cost electrode simulations, so the cell counts shown in Table 3.1 cannot be used to ensure similar cell concentrations across the electrodes. Instead, both electrodes use a maximum of 5 cells added in integer steps, with the cell concentration adjusted to take the lower liquid volume into account. The droplet on the larger of the two LoCMOS electrodes still has a height of 100 μm and with side lengths of 500 μm, the volume of the cubic water droplet is $25 \times 10^6$ $\mu$m$^3$ or 0.025 mm$^3$. Dividing the integer steps of cells added to the model by this volume gives the cell concentration in mm$^3$ in Fig. 5.9. Similarly, using an electrode area of 25x25 μm$^2$ and a droplet height of 100 μm gives a volume of 62500 μm$^3$ or $6.25 \times 10^{-5}$ mm$^3$, from which the concentrations in Fig. 5.10 are derived.

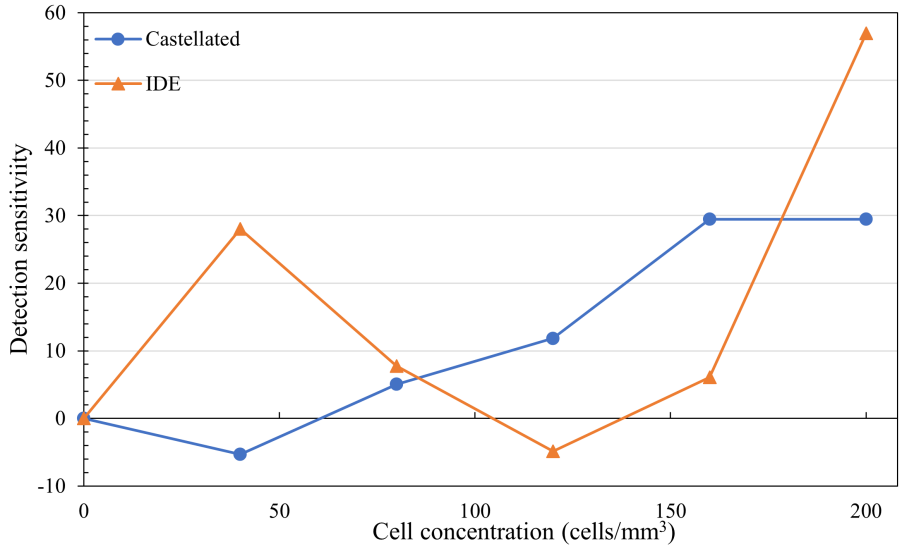



**Figure 5.9.** Sensitivity of the 500x500 μm LoCMOS electrode using 25 μm feature sizes.

The 28% increase in capacitance of the IDE in response to an increase of 40 cells/mL, while contradictory to the results seen for the low-cost electrodes, shows great promise that this electrode could be very sensitive to low cell concentrations. However, the immediate inversion seen between this point and 120 cells/mL lowers confidence in this electrode. This inversion is similar to simulation results

seen for cells positioned between the fingers of an electrode [13], though the simulation parameters differ enough that cell position relative to the electrode may be discounted as a possible explanation. Increases in cell concentration on this electrode lead to large relative capacitance changes due to the low starting concentration seen in Table 5.3, with the 55% increase in capacitance seen from 160 to 200 cells/mL corresponding to 0.7 pF absolute change. From the eventual increase in capacitance at higher cell concentrations, it does seem that cells at such low concentrations add in parallel rather than adding in series such that their electrical effect is increased capacitance.

The castellated electrode in Fig. 5.9 starts with a negative change in capacitance for the first increase in cell concentration from 0 to 40 cells/mL before inverting. This inversion is similar to the IDE inversion in the opposite direction, but unlike the IDE, the response does not invert again. Instead, the capacitance keeps increasing steadily as the cell concentration increases before reaching a plateau of 30% at 160 cells/mL. This might suggest that the castellated electrode reaches a limit of detection before 200 cells/mL, but with finger widths that are only a fraction of the length of *E. coli* cells, there is a high likelihood that the capacitance can still change at higher concentrations.

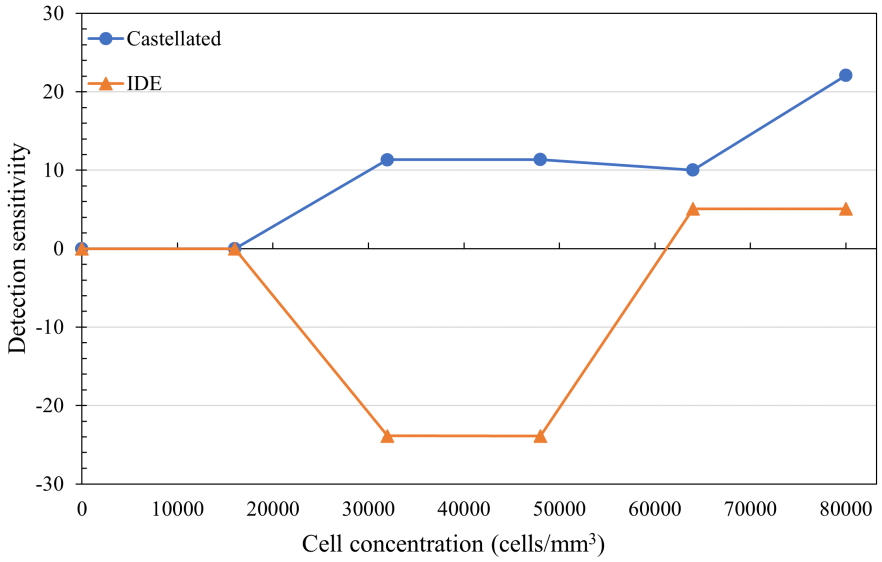



**Figure 5.10.** Sensitivity of the 25x25 µm LoCMOS electrode using 0.6 µm feature sizes.

The electrodes studied for the array-based implementation (shown in Fig. 4.9) are the first electrodes with finger widths that are within an order of magnitude of the size of the cells. Both the IDE and the castellated electrode show almost no change from 0 to 16 000 cells/mL. From there, the castellated

electrode shows a 10% increase in capacitance while the IDE shows a decrease of 24% at 32 000 cells/mL. From there, the castellated electrode stays steady at 11.3% before showing a minor inversion that terminates at 64 000 cells/mL, with higher concentrations showing an upward trend culminating in a final capacitance change of 24%. The change seen in the IDE opposite to that seen in the castellated case, with a 24% decrease from 16 000 to 32 000 cells/mL and a plateau from 32 000 to 48 000 cells/mL. This is followed by an increase in capacitance from -23% to 5%, effectively reversing the change seen at lower concentrations before staying level at the highest concentrations, similar to the performance of the castellated electrode in Fig. 5.10.

The concentrations seen in Fig. 5.10 are much closer to concentrations that might reasonably be measured in a biosensor system without cell manipulation than the concentrations seen in the low-cost electrode simulations. This is a limitation in the manner the simulations were conducted and does not represent a fair comparison to the low-cost electrodes, at least in the 25x25 µm electrode case. A fairer comparison can be made when comparing the performance of the 500x500 µm LoCMOS electrode to the low-cost electrodes. An analysis of the largest relative capacitance change for each size ratio shows that at small size ratios the castellated electrode reacts opposite to the IDE. For larger size ratios of above 20, the largest relative capacitance deviation changes in the same manner in both the IDE and the castellated electrode, with the IDE showing a larger deviation from the capacitance of an empty electrode than the castellated electrode regardless of size ratio. Fig. 5.11 shows these trends for the low-cost electrodes, though it is important to note that this plot is only concerned with the largest capacitance deviation seen, regardless of the cell concentration at which this occurs.

It is evident that the major limitation in finite element analysis of electrodes and cells is the computational complexity required for large concentrations of cells which are often an order of magnitude (or more) smaller than the features of the electrode under consideration. This allows the study of electrode performance at exceptionally low cell concentrations, which might be difficult to achieve in practice. Measurement of electrode performance is therefore paramount in understanding the practical performance of electrodes in a practical measurement setup.

## 5.3 MEASUREMENT RESULTS

This section presents the measurements taken with a GW Instek LCR meter of different commercial and low-cost electrodes as shown in Table 3.4, after which results from experiments with *E. coli* bacteria are shown. The EIS experiments on *E. coli* were conducted using a commercial Metrohm

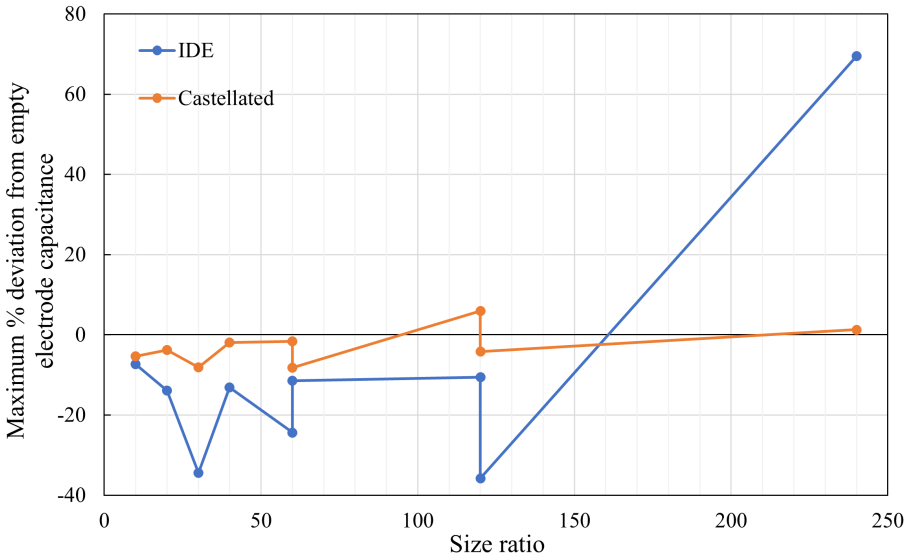



**Figure 5.11.** Maximum relative capacitance change for different size ratios and geometries.

Dropsens µStat-i400s potentiostat with the results exported and processed in Python.

### 5.3.1 Measured Capacitance

A controlled method of quantifying the differences between electrode geometries and sizes (see Table 3.4) is to use polystyrene microbeads suspended in deionised water using the GW Instek LCR meter. This device can be used to give an indication of the expected capacitance for a specific electrode setup, whereupon the low-cost biosensor device described in Section 4.3 may be optimised to sense capacitances in this range. The parallel capacitance and resistance are extracted using a 2 V AC signal at 100 kHz and the low-cost sample jig from Fig. 3.6 as the electrode holder. These measurements are conducted in triplicate to ensure repeatability. Table 5.4 shows the average capacitance of DI water measured with each of the different electrodes. All the commercial electrodes have the same footprint (6x6 $mm^2$) except the concentric 10 µm, which is a circular IDE 6 mm in diameter, and four feature sizes are considered: 5, 10, 50, and 100 µm. The 100 µm electrode includes the low-cost commercial and castellated electrode on the FR4 substrate. When referring to the 100 µm IDE, this is in reference to the low-cost version, and when discussing its commercial counterpart, this will be specifically stated.

The trends seen in simulated capacitance in Fig. 5.4 are supported by the measured results from Table 5.4, showing that an increase in the feature size leads to a decrease in capacitance. The 5 µm IDE shows the highest capacitance at 1.35 nF, which is expected with a size ratio of 1200. With such a

**Table 5.4.** Capacitance of each of the electrodes considered when measuring DI water.

| Finger width (µm) | Note | Capacitance (pF) |
|---|---|---|
| 100 | Low-cost IDE | 3.05 |
| | Low cost castellated | 73.1 |
| | Commercial IDE | 23.6 |
| 50 | Commercial IDE | 3.48 |
| 10 | IDE on glass substrate | 556 |
| | Concentric IDE on glass substrate | 525 |
| 5 | IDE on glass substrate | 1350 |

high capacitance, it may be difficult to extract pF changes in capacitance (as seen in simulation). The simulations used in Section 3.2 use theoretical values for the electrical properties of water and the measured results are for DI water, an order of magnitude difference can be seen between 10 µm and 100 µm features. The 50 µm bucks this trend at 3.48 pF compared to the 23.6 pF from the commercial 100 µm, which is a smaller difference than expected for a 100% increase in the size ratio from 60 to 120. At 70% the area of its square counterpart, the concentric 10 µm IDE has approximately 94% the capacitance, suggesting that capacitance does not necessarily scale linearly with electrode footprint and the size ratio as defined by (5.1) can not be generalised to non-square electrode geometry. The low-cost electrodes were adjusted after manufacturing by filing away some of the tracks to bring their footprint closer to the area of the commercial electrodes for a fairer comparison, and the difference between them might be attributed to differences in the final footprint achieved. The order of magnitude difference seen when comparing the low-cost IDE to the low-cost castellated electrode support the simulation data seen in Fig. 5.4, with the former demonstrating an average blank capacitance closer in magnitude to the commercial 50 µm IDE.

The sensitivity of each of the electrodes is studied using different concentrations of polystyrene microbeads, with those in a comparable capacitance ranges presented against one another: the low-cost 100 µm IDE and commercial 50 µm IDE in Fig. 5.12, the low-cost 100 µm castellated and commercial 100 µm in Fig. 5.13, and the smallest feature-size electrodes in Fig. 5.14. The average capacitance is plotted against the concentration of microbeads in suspension, and each dataset includes a trendline and the $R^2$ value. These trendlines are logarithmic to fit the concentration data presented on a logarithmic

$x$ axis, and the sensitivity of each electrode is determined by the gradient of the best-fit line with units F/bmL$^{-1}$, where bmL$^{-1}$ is beads per mL. This measure indicates how much the measured capacitance increases for a 1 bead per mL increase in concentration.

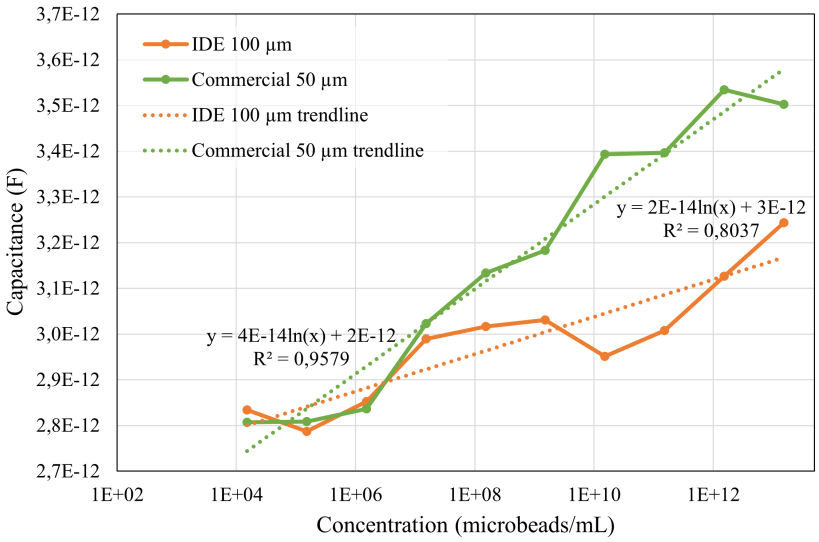



**Figure 5.12.** Capacitance of 3 µm polystyrene microbeads measured using low-cost IDE and a 50 µm commercial IDE on a plastic substrate.

As expected, both electrodes in Fig. 5.12 show an increase in capacitance as the concentration of microbeads increases, with the commercial 50 µm electrode showing the faster increase of the two. With a gradient twice that of the low-cost IDE, the commercial 50 µm is approximately twice as sensitive. The measured data for the low-cost IDE oscillates around its fit line, lowering the confidence that this electrode could be used for accurate biosensing applications. With an associated $R^2$ value of 0.8037, this electrode may likely be more suitable for higher concentrations. The commercial electrode measurements, on the other hand, follow the fit line much more closely, with a correlation coefficient of 0.9579. Further, the data seems to follow a sigmoid curve from the lowest to the highest concentration, though this is likely only due to the outlier datapoint at $1.5 \times 10^{13}$ microbeads/mL. Both electrodes seem to show saturation at concentrations below $10^6$, with the commercial 50 µm even inverting at lower concentrations. The capacitance measured at the highest concentrations approaches the capacitance measured for blanks in Table 5.4.

The capacitance of the low-cost castellated electrode and commercial 100 µm IDE shown in Fig. 5.13 is an order of magnitude larger than the low-cost IDE and commercial 50 µm IDE seen in Fig. 5.12. The electrodes with a larger capacitance values seem to show smaller variance than the electrodes with

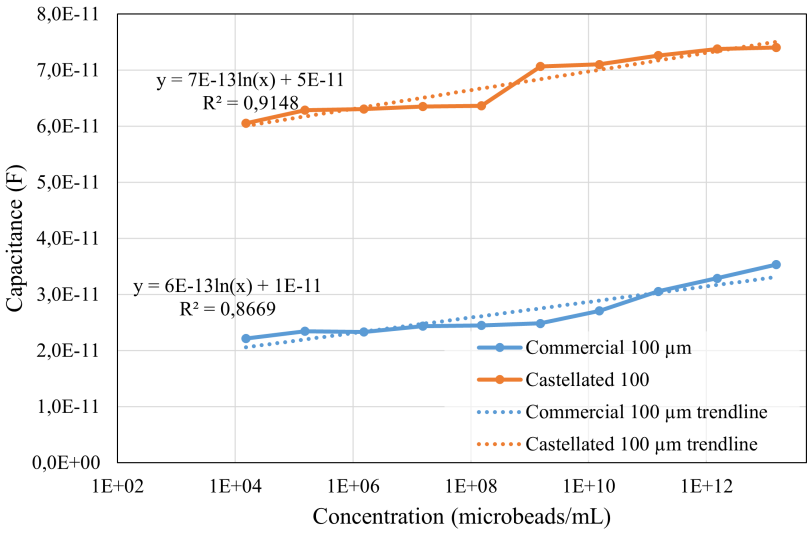



**Figure 5.13.** Capacitance of 3 µm polystyrene microbeads measured using low-cost castellated electrode and a 100 µm commercial IDE on a plastic substrate.

smaller capacitance values, though the $R^2$ value for each of the fit lines suggests this might be mostly due to the scaling on the axes. Both electrodes show a shape that is slightly sigmoidal, though the large variance in the data makes this an unlikely conclusion. Both electrodes show an increase in capacitance as the concentration of microbeads increases, with the low-cost castellated electrode more sensitive and more linear than the commercial IDE by showing a gradient of $7 \times 10^{-13}$ against $6 \times 10^{-13}$ and an $R^2$ of 0.9148 against 0.8669 respectively. The inversion seen in the smaller capacitance electrodes at concentrations below $10^6$ is not present in this data. Further, the capacitance of blank samples as shown in Table 5.4 is lower than the capacitance of the lowest concentration measured - this is expected and is at odds with the observation that the trend in Fig. 5.12 has to invert to take the magnitude of a blank sample into account.

The electrodes in Fig. 5.14 have the smallest feature sizes of the commercial electrodes considered and for this reason, are patterned on a glass substrate. Since the area of these electrodes is similar to the other electrodes used, the smaller feature sizes lead to significantly higher capacitances. Despite this, the sensitivity of these electrodes is comparable to previous electrodes: the square 10 µm IDE has a sensitivity of $3 \times 10^{-2}$ pF/bmL$^{-1}$, which is between that of the commercial 50 µm and 100 µm low-cost interdigitated electrodes. The concentric 10 µm and square 5 µm have slightly lower sensitivity than the 100 µm low-cost castellated and commercial interdigitated electrodes from Fig. 5.13. Although not immediately apparent from the scale of the plot, there is considerable variance in the measured values

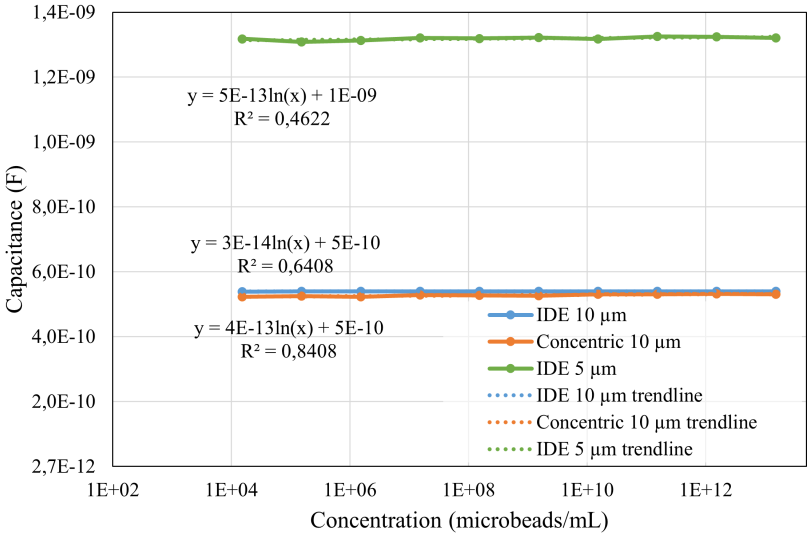



**Figure 5.14.** Capacitance of 3 µm polystyrene microbeads measured using commercial electrodes on a glass substrate.

for the 5 µm IDE, evidenced by the fact that the $R^2$ value is only 0.4, which is by far the worst fit line of the dataset, with the two 10 µm electrodes demonstrating an $R^2$ value of 0.64 and 0.84, respectively. One of the major contributors to the variance in capacitance is the electrode holder in Fig. 3.6 that is only constrained in the vertical and one of the horizontal directions, with the electrode itself allowed to move perpendicular to its surface in the cuvette headroom where the measurement takes place. Great care was taken to ensure the electrode was in the same position for consecutive measurements, and since the feature sizes for the 5 and 10 µm electrodes are so small any change in measurement conditions is magnified more in these electrodes than in their larger feature size counterparts.

The limit of detection (LOD) is the lowest capacitance change that can be picked up by the electrode and is defined by the International Union of Pure and Applied Chemistry (IUPAC) as 3 times the standard deviation of a blank measurement for 90% confidence [82], or

$$\text{LOD} = 3\sigma_{blank}, \tag{5.2}$$

where $\sigma_{blank}$ is the standard deviation of a triplicate measurement of a blank sample, or a sample of only the solution with no analyte. DI water is used as blanks for this experiment since there are no microbeads in the samples prepared for the values in Table 5.4. This gives the limit of detection in terms of capacitance, but a more useful measure is the limit of cell or microbead detection, which requires using the calculated LOD and dividing it by the sensitivity of the electrode (the gradient of the

fit line seen in Figs. 5.12 - 5.14) and rounding up to the nearest integer. Table 5.5 summarizes the LOD in both capacitance and microbead count for the seven electrodes considered as well as the sensitivity extracted from Figs. 5.12 - 5.14 required to convert from one LOD to the other.

**Table 5.5.** Limit of detection and sensitivity level for each of the electrodes considered.

| Finger width (µm) | Note | LOD (pF) | Sensitivity (pF/bmL$^{-1}$) | LOD (bead count) |
|---|---|---|---|---|
| 100 | Low-cost IDE | 0.42 | 0.02 | 22 |
| | Low-cost castellated | 3.68 | 0.7 | 6 |
| | Commercial IDE | 1.87 | 0.6 | 4 |
| 50 | Commercial IDE | 0.54 | 0.04 | 14 |
| 10 | IDE, glass substrate | 2.79 | 0.03 | 93 |
| | Concentric IDE | 5 | 0.4 | 13 |
| 5 | IDE, glass substrate | 0.46 | 0.5 | 1 |

The sensitivity values summarised in Table 5.5 confirm that the low-cost electrodes demonstrate the highest sensitivity of the 7 electrodes considered at 0.7 and 0.6 pF/bmL$^{-1}$ each, followed by the smallest feature size 5µm IDE on the glass substrate. This seems to indicate that the E-field penetration into the FR4 substrate seen in Fig. 5.2 increases both the blank capacitance and the sensitivity if the geometry of the electrode is kept constant. This might suggest that the larger absolute maximum E-field seen on the FR4 substrate in simulation translates to a higher sensitivity, though the difference seen in these measurements may be due to the thickness of the substrate rather than purely its material. Contrary to Fig. 5.8, the low-cost castellated electrode is slightly more sensitive than its IDE counterpart, though due to the castellated square beginning closer to the electrode holder edge, the castellated electrode might not be suspended as deeply as the IDE, which will affect the sensitivity. The adjustments made to bring the total area of the low-cost electrodes closer to that of the commercial electrodes certainly affected their sensitivity in different ways. Fig. 5.7 shows that for constant geometry and substrate, the sensitivity of an IDE increases as the feature size goes down, which is confirmed by the sensitivity increase from 0.02 to 0.04 pF/bmL$^{-1}$ on the two plastic substrate electrodes (a decrease in feature size from 100 to 50 µm) and from 0.03 to 0.5 pF/bmL$^{-1}$ on the two glass substrate electrodes (following the decrease from 10 to 5 µm).

The LOD distribution for the 50 and 100 µm electrodes follows the same distribution as the blank measurement summarised in Table 5.4: the low-cost IDE and 50 µm commercial IDE are the lowest at 0.42 and 0.54 pF respectively, with the 100 µm commercial IDE slightly higher at 1.87 pF, and the low-cost castellated electrode the highest of these four at 3.68 pF. The fact that this trend is not followed in the smaller feature size electrodes seems to suggest that LOD and blank capacitance may be related in electrodes with a small size ratio, but not necessarily in electrodes with a large size ratio. It is also no surprise that the electrodes that operate at higher capacitances have larger standard deviations and consequently higher capacitance LODs. Translating the capacitance LOD to a microbead count requires division by sensitivity, so a more sensitive electrode will result in a larger divisor and a smaller bead count. This is most evident when comparing the 420 and 460 fF LOD from the low-cost 100 µm and 5 µm IDEs that translates to a LOD of 22 and 1 when using their respective sensitivities of 0.02 and 0.5 pF/bmL$^{-1}$. The microbead LOD in this comparison is directly related to sensitivity. A large capacitance LOD can negate the effect of a very sensitive electrode, as seen in the concentric 10 µm IDE, which has the fourth highest sensitivity at 0.4 pF/bmL$^{-1}$ but is let down by its 5 pF LOD, which is the highest of all the electrodes considered. The combination of poor measurable LOD and low sensitivity is seen in the 10 µm IDE, where the 2.79 pF LOD and 0.03 pF/bmL$^{-1}$ result in the highest microbead LOD of the set at 93. The opposite is observed in the low-cost castellated electrode, which has a microbead LOD comparable to that of the 5 µm IDE despite its measured capacitance LOD being 8 times higher. When designing custom electrodes aimed at detecting low cell counts, therefore, sensitivity is the most important feature to consider.

The three 100 µm feature size electrodes show good linearity across the range of concentrations measured and with the comparatively low capacitances, these were expected to perform well when measuring *E. coli* cells. The largest difference in the experimental setup between the electrode characterisation and *E. coli* experiments is the use of deionised water for dilutions of the polystyrene beads while the EIS experiments from Section 5.3.2 use distilled water for preparing dilutions and blanks. The electrical parameters used for EIS measurements can be seen in see Table 3.3.

### 5.3.2 Electrical Impedance Spectroscopy

To ensure the repeatability of any bacterial study, all results are taken in triplicate. As such, three reactors were prepared and grown, with three sets of EIS data gathered for each 1:10 serial dilution and electrode combination. Although it might seem effective to immediately use the average per datapoint to draw conclusions, complex physical phenomena in the *E. coli* may obscure valuable insights in the

magnitude and phase information obtained. To prevent this, the average of the three reactors is only calculated once the capacitance is extracted from reactance. For the EIS results presented before the capacitance is extracted, only one of the three reactors will be shown, as the insights gained from each will be very similar. The magnitude and phase data may be presented as a function of frequency, but a more common method of displaying EIS data is to use a Nyquist plot, which plots the resistance (Z') on the *x* axis and the negative reactance (Z") on the *y* axis. This removes the frequency dependency of the data from the plot and gives a more direct view of the circuit elements that could be used to model a specific chemical or biological reaction [14]. Fig. 5.15 shows the Nyquist plot for a set of dilutions from one of the reactors measured using the commercial 100 µm IDE, starting from the final concentration of the *E. coli* growth process at $10^0$, with eight 1:10 dilutions making up the rest of the traces. Figs. 5.15 to 5.18 show the responses using these serial dilutions, as opposed to inferred cell counts. The concentration of cells for $10^0$ is determined using conventional methods of cell concentration extraction, specifically plated CFU counting, and will be used to infer the concentration at the lower dilutions. Fig. 5.16 shows a comparison of the results obtained from the same reactor using the two low-cost electrodes.

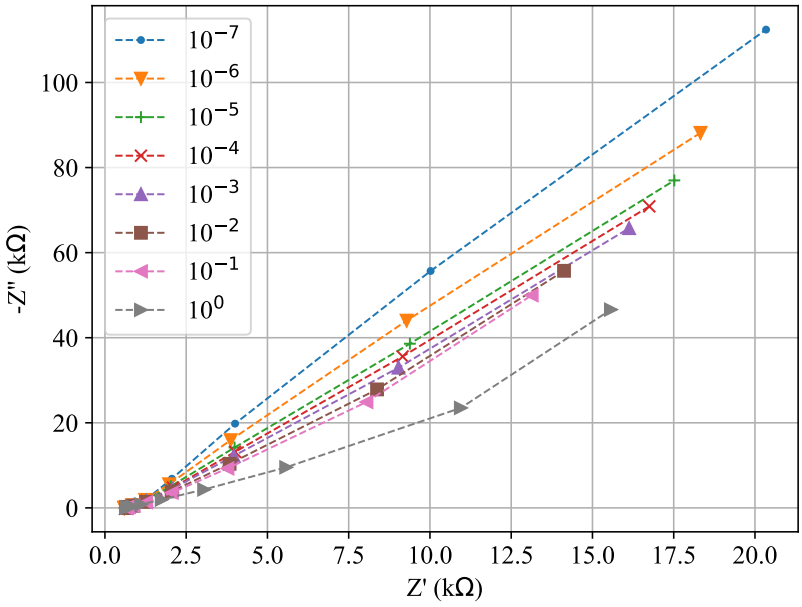
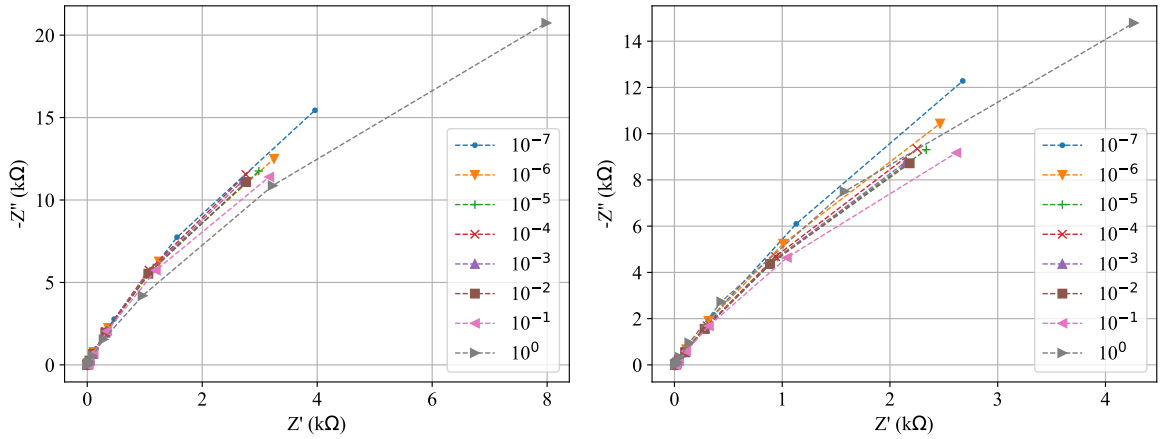



**Figure 5.15.** Nyquist plot of the dilutions from one reactor of *E. coli*, measured using the commercial Dropsens 100 µm IDE.

The markers in Fig. 5.15 correspond to samples taken twice per decade, with low frequencies appearing on the right-hand side and high frequencies on the left. It is immediately apparent that as the sample is diluted more, the effect is much more pronounced at low frequencies than high frequencies, which

likely corresponds to the double-layer capacitance at the electrode-solution interface. This is supported by the dominance of the reactance at low frequencies. Further, at high frequencies the change in impedance is complex - as the solution becomes more diluted, the resistance and reactance both decrease until the impedance is dominated by the resistance of the distilled water used for dilutions which is the $x$ axis intercept at around 600 Ω. There is a monotonic change in the impedance response, with resistance and reactance increasing and decreasing respectively as the measured sample is diluted more.




**(a)** Interdigitated electrode.

**(b)** Castellated electrode.

**Figure 5.16.** Nyquist plot comparison of the same dilutions from one reactor of *E. coli* using the low-cost interdigitated and castellated electrodes.

The total impedance seen by the low-cost electrodes is almost an order of magnitude lower than the commercial IDE used for comparison and the low-frequency resistance of the castellated electrode seen in Fig. 5.16(b) is nearly half that of the IDE in Fig. 5.16(a). The spread of impedance spectra in both cases is tighter than seen in the commercial electrode, so the relative difference between consecutive dilutions is likely much smaller. Neither low-cost electrode shows a monotonic change in resistance, but the IDE does demonstrate a monotonic increase in the negative reactance from $10^{-1}$ to $10^{-4}$ that is not present on the castellated electrode. At the highest frequency, all dilutions on both electrodes tend to a zero reactance value at approximately 50 Ω of resistance, corresponding to the resistance contribution from the distilled water. Interestingly, the measurement at $10^{0}$ on both electrodes is much larger when compared to the further dilutions than its counterpart seen in the commercial electrode. This might be attributed to the electrodes, which are copper traces coated in gold, or it might be the FR4 substrate. As seen in Section 3.2, the permittivity of copper and gold is very close to one another,

so the latter explanation for the difference is more likely than the latter. This observation might also serve to explain the lower solution resistance detected in both low-cost cases.

#### 5.3.2.1 Extracted capacitance

Although insights can be gleaned from the resistance of the sample, simplifying the analysis method to only focus on the reactance and capacitance allows for the simplification of the sensing method required by a low-cost device for point-of-need applications. Since the main interest in this investigation is on using the capacitance to detect *E. coli*, the resistance is neglected and the capacitance is calculated using (3.8). Fig. 5.17 shows the capacitance change of the commercial 100 µm IDE from 10 Hz to 1 MHz. Each data point is the average capacitance of the triplicate measurement, with the error bars representing one standard deviation from the average.

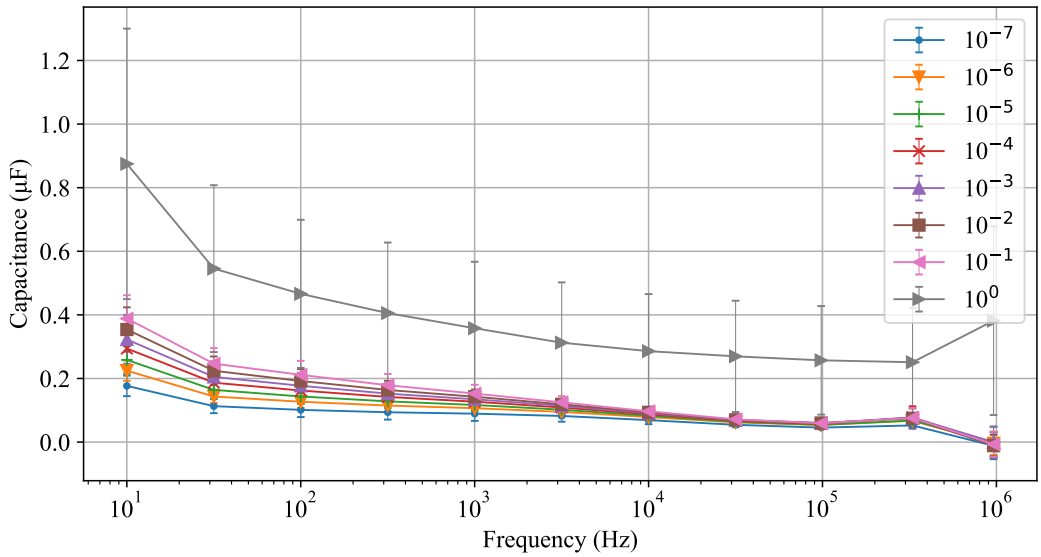



**Figure 5.17.** Triplicate capacitance extracted from the reactance of Fig. 5.15 using (3.8)

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Plotting the change in capacitance against the frequency reveals some of the frequency-dependent characteristics important when measuring capacitance. This includes the double layer capacitance at very low frequencies [41], and the larger relative difference between consecutive dilutions show why it is used as a proxy for bacterial growth as in [10]. One of the problems with using the double layer capacitance as a proxy for *E. coli* is that this is also affected by the products of bacterial metabolic processes, as the measurement of the CFU at these dilutions show that cells almost completely disappear around $10^{-4}$. The capacitance decreases as the frequency is increased, in good accordance with established electrical cell theory [27], [28], though if the capacitance at 100 kHz is assumed to be

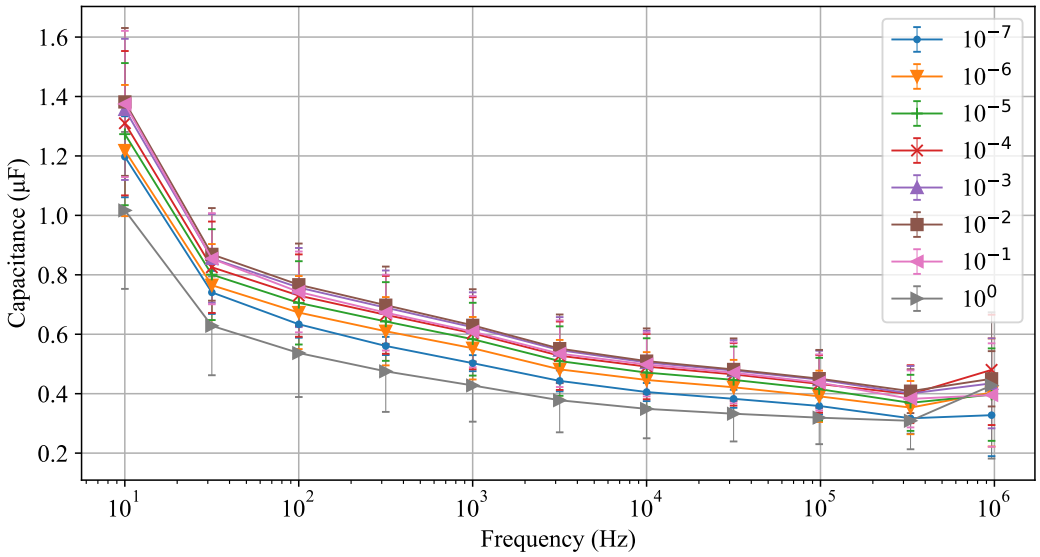
the cell membrane capacitance, the performance of this electrode does not look promising. A more thorough picture of the effectiveness of the electrode at this frequency may be gleaned by comparing its performance to that of its low-cost counterparts for the CFU concentration.

The measurement containing the original concentration of cells taken from the stationary phase of the growth curve is offset from the dilutions by 0.5 µF, which might indicate that the addition of distilled water for dilutions initially contributes significantly to the change in capacitance and the effect is diminished as the cell concentration decreases. This sample point also shows a 180 nF increase in capacitance at 1 MHz, whereas the dilutions show a slightly smaller decrease at the same frequency. Further dilutions introduce a monotonic offset that lowers the capacitance over much of the lower frequency of the spectrum, which supports the assumption that large numbers of cells act approximately like parallel capacitance elements. Smaller error bars on dilutions are an indicator that the addition of distilled water during the dilution process has removed much of the variance from the three reactors, and also instils greater confidence in the measured value.

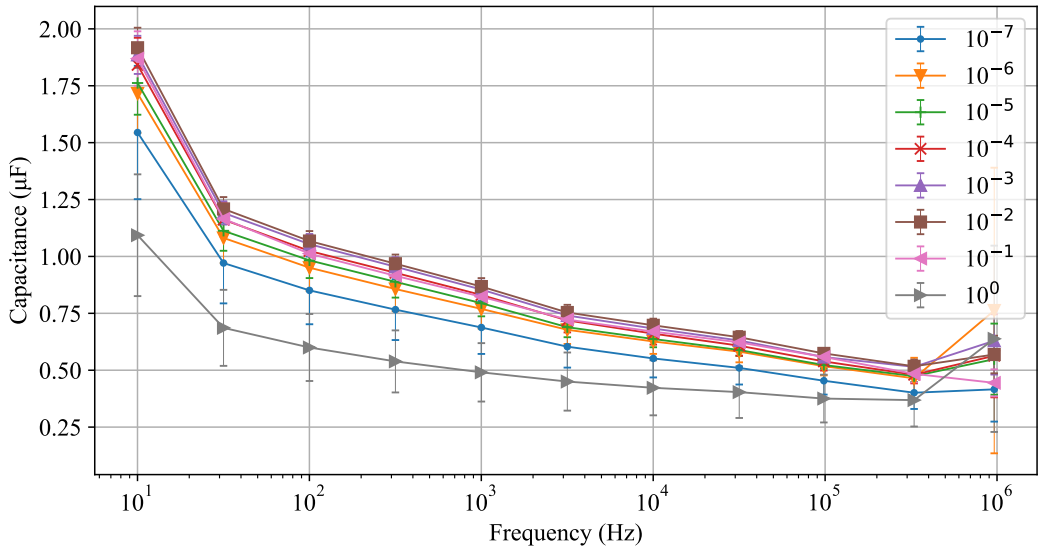
Figs. 5.18(a) and 5.18(b) show the capacitance spectra for the low-cost IDE and castellated electrodes respectively. The capacitance of the original sample, $10^0$, shows a similar magnitude offset on the low-cost IDE when compared to the commercial IDE, though this offset is lower than the associated dilutions as opposed to higher as seen in the commercial IDE. The same is true for the castellated electrode, but the offset in this case is about 1.9 µF lower than its first dilution ($10^{-1}$). From $10^{-7}$ to $10^{-1}$, both the IDE and castellated electrodes show an increase in capacitance, again indicating that the cells add as electrically parallel elements. Contrary to the capacitance of commercial electrodes, the relative difference between consecutive dilutions seems to shrink less, with the effect that at 100 kHz the difference between respective dilutions can be seen with greater clarity than in the commercial IDE. As expected, the low-frequency double-layer capacitance is a significant component in the spectrum, with its magnitude double the high-frequency capacitance in the IDE and nearly three times the high-frequency capacitance in the castellated electrode. Finally, the capacitance at 1 MHz increases in comparison to the rest of the spectrum in all dilutions, which bucks the trend seen in the dilution spectra shown in Fig. 5.17 and potentially discounts the theory that the introduction of distilled water adversely affects the measurement of capacitance at MHz frequencies. The more likely explanation is that the electrodes themselves react slightly differently to the introduction and increased presence of distilled water for more dilutions.

For a fairer comparison to the simulation results from Section 3.2 and to more closely mimic the kind of measurement results that might be achieved from the low-cost biosensor, the spectra from Figs. 5.17 and 5.18 must be simplified to a single frequency measurement. This sample is taken at 100 kHz in accordance with the frequency used for simulations and in testing the polystyrene beads with the low-cost biosensor device. Further, as the CFU for the dilutions can be counted, dilution-based presentation is substituted with plots showing the capacitance against the measured concentration. The CFU on the horizontal axis in Fig. 5.19 correspond to the $10^{-7}$, $10^{-6}$, $10^{-5}$, and $10^{-4}$ dilutions from Figs. 5.17 and 5.18, with the average CFU value for the three reactors used as the data points and the standard deviation shown as error bars for both CFU and capacitance. These dilutions are chosen because these are the only dilutions with CFU counts between 25 and 250 that ensure counting errors are minimised [83]. The *y* axis scaling is changed from µF to nF, and each dataset is annotated with a straight line fit to the measured data, from which its sensitivity may be extracted.

All three electrodes show values slightly lower than in Figs. 5.17 and 5.18, since the capacitance at 100 kHz is lower than the low-frequency capacitance. Each of the electrodes performs as expected from results in Sections 3.2 and 5.3.1, confirming the use of microbeads as a validation tool, and further supporting the expanded use of simulations in electrode design. Similar to Table 5.4, the capacitance from the commercial IDE is offset relative to the low-cost electrodes by slightly less than an order of magnitude, with the castellated electrode showing the higher capacitance of the two low-cost electrodes. The sensitivity extracted from the gradients of the straight lines fit to the data also seems to follow




**(a)** Interdigitated electrode.




**(b)** Castellated electrode.

**Figure 5.18.** Triplicate capacitance of the low-cost electrodes extracted using (3.8).

the trends seen in Table 5.5, increasing in sensitivity from the commercial IDE at 0.52 nF/CFU to the low-cost IDE at 0.82 nF/CFU and the low-cost castellated electrode at 1.323 nF/CFU. The data for this analysis is necessarily truncated to 4 data points due to the requirements set out for CFU counts [83], which naturally lowers the $R^2$ value for each of the fit lines. The highest confidence ($R^2$ = 0.66) is achieved with the commercial IDE, but since this electrode demonstrates the lowest sensitivity, it also has the smallest capacitance change at extremely low CFU, reducing the residual difference between the data and the fit line and increasing $R^2$. Due to the tenfold dilutions, the spacing of data points on the horizontal axis is nearly logarithmic, and the $R^2$ could be improved further by using smaller fraction dilutions to interpolate the data points between these measurements.

It is apparent that the capacitance measured for the different concentrations in Fig. 5.19 is significantly higher than the capacitance seen in Fig. 5.14. Two major contributors to this difference are the use of DI water for dilutions in Fig. 5.14 and the presence of metabolic byproducts, LB broth, and distilled water in the diluted solutions in Fig. 5.19. In the experiments with DI water, only the microbeads introduced in dilution contribute to electrical changes in the solution while actual *E. coli* cells grown in LB broth introduce ionic byproducts from their metabolic process into their environment, which already contains an unknown concentration of diverse chemical compounds necessary for growing *E. coli*. Although this is diluted with distilled water, the ions still present in the distilled water also further

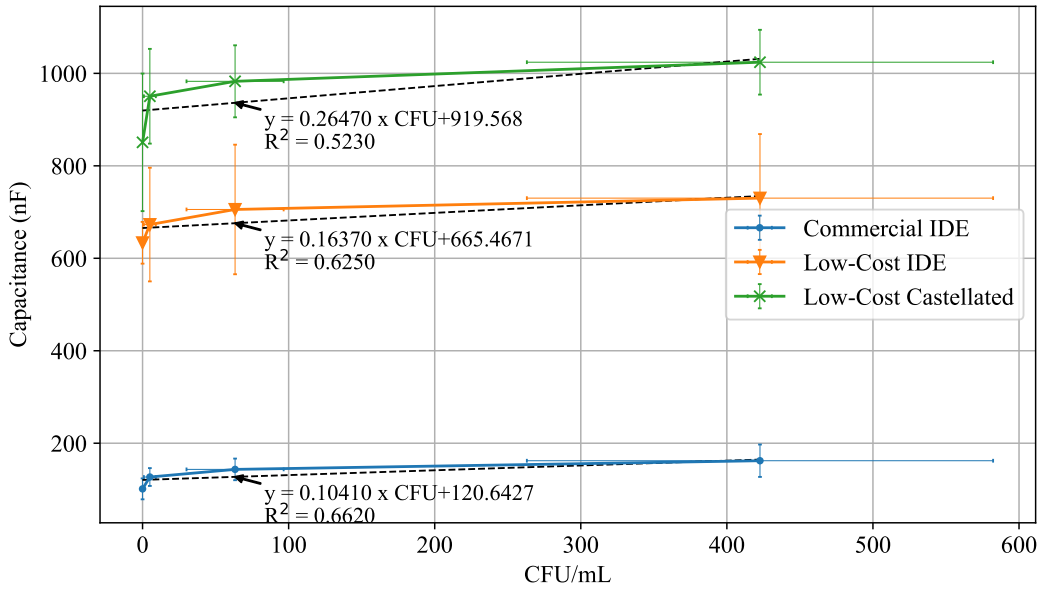



**Figure 5.19.** Capacitance vs CFU/mL of *E. coli* using three electrodes sampled at an excitation frequency of 100 kHz.

contribute to the difference in impedance. The error bars seen in Fig. 5.19 show that the low-cost castellated electrode seems to become more accurate at higher concentrations than its IDE counterpart, which is the more accurate of the two at low concentrations. Neither low-cost electrode is able to match the accuracy achieved by the commercial electrode. Similar to Table 5.5, the limits of detection calculated from the *E. coli* experiment and the sensitivity extracted from Fig. 5.19 are shown in Table 5.6. The LOD as defined by (5.2) requires the capacitance of a blank sample to be multiplied by 3. From Fig. 5.19 it is readily apparent that the $10^{-7}$ dilution contains no cells across the three reactors, so the standard deviation at this point is used. Translating the capacitance LOD to a CFU LOD again requires the division between the capacitance LOD and the sensitivity extracted from Fig. 5.19.

**Table 5.6.** Limit of detection of *E. coli* measured with 100 µm finger width electrodes.

| Electrode | LOD (nF) | Sensitivity (nF/CFUmL$^{-1}$) | LOD (CFU/mL) |
|---|---|---|---|
| Low cost castellated | 446.38 | 0.26 | 1717 |
| Low-cost IDE | 135.39 | 0.16 | 846 |
| Commercial IDE | 67.84 | 0.1 | 679 |

Similar to Table 5.5, the low-cost castellated electrode in Table 5.6 shows the highest capacitance LOD and sensitivity at 446.38 nF and 0.26 nF/CFUmL$^{-1}$ respectively. As before, this combines to result in the castellated electrode demonstrating the worst CFU LOD of the three at 1717 CFUmL$^{-1}$ - twice that of the low-cost IDE and 2.5 times that of the commercial IDE at 846 and 679 respectively. This inverts the microbead LOD trend for the two 100 µm IDEs from Table 5.5. Using lab-grown *E. coli* grown in LB broth allows electrodes to be tested more rigorously than simply using the microbead experiments from Section 5.3.1, and can give valuable insights into their performance at low CFU. Comparing the CFU LOD from Table 5.6 show that the lowest attainable capacitance LOD of 679 for the commercial IDEs is still higher than the highest CFU that was reliably counted, with the horizontal axis ending at 600 due to the error bars in CFUmL$^{-1}$. Using the definition for LOD, therefore, suggests that the electrodes considered are not suitable for measuring the capacitance of samples with such a low CFU. The linear relation seen between CFU and capacitance in Fig. 5.19 is expected. These electrodes may be detecting an increase in metabolic byproducts rather than cells themselves, which can be used as a proxy measurement for *E. coli* [10]. With the limit of detection as high as in Table 5.6 and without the benefit of verified experiments against counted CFUs, the measurement of byproducts may only be useful as an indicator of the recent presence of *E. coli* in the sample.

## 5.4 LAB-ON-CHIP

This section is concerned with the custom chip designed in Chapter 4. First, the layout of the CVC array is briefly discussed using an image of the IC, after which electrical characterisation results from the operational amplifier including DC, AC, and transient characterisation are presented. Results from the array addressing subsystem are also presented. Next, the microbead experiment from Section 5.3.1 is repeated on a subset of the electrodes using the low-cost biosensor device designed in Section 3.3.3.

### 5.4.1 LoC Layout

Fig. 5.20 shows a microscope picture of the completed sensing array, positioned near the corner of the inner ring on the multi-project IMSS Water Quality Monitoring 2021 chip. On the left and top right are diode-based ESD protection structures to protect external inputs from unexpected electrostatic voltages applied to the input pads. Outputs can be applied directly to pads, as can be seen in the metal traces in the top left-hand corner that goes to the top and to pads that are out of the frame. The 64 sensing cells of the 8x8 array can be seen by counting the green blocks corresponding to the Miller capacitor from screenshots of the opamp (see Figs. 4.3 and 4.11).

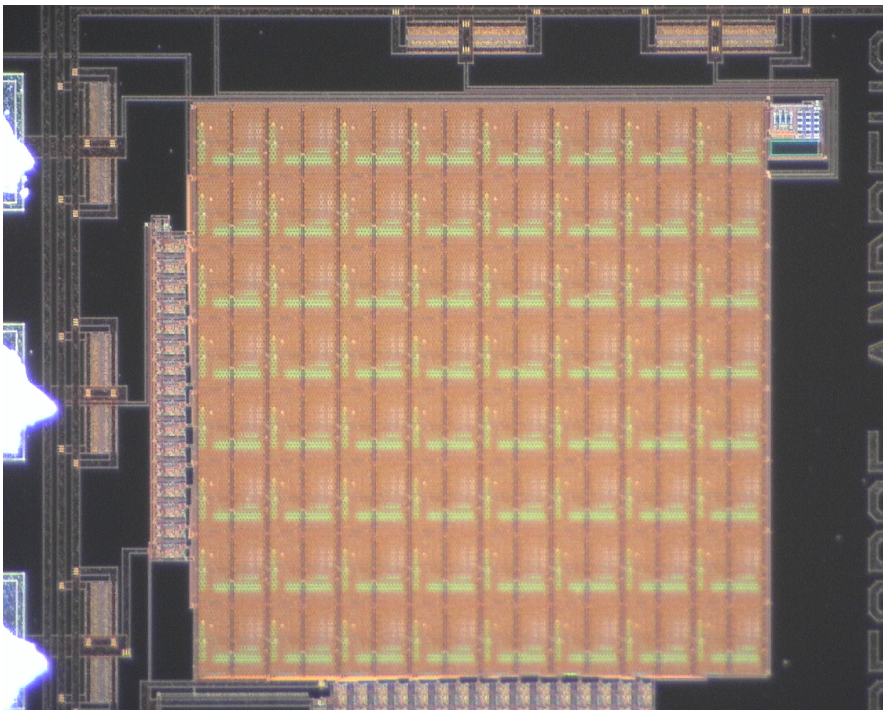


**Figure 5.20.** Image of CVC array including array control and output buffer opamp on packaged chip.

Each of the 64 sensing cells is split into two sub-rows and columns, giving an effective 16x16 array comprising 256 electrodes. This can be seen by the faint grey line running vertically through the middle of each of the 8 columns, corresponding to a gap between the electrodes for each sensing cell. The control shift registers for the 16 rows and 16 columns are to the left and bottom of the array respectively, with the outputs of the first flip-flops in both cases routed to a pad to be read as an output. All 64 opamp outputs are tied together and connected to the non-inverting input of the opamp at the top right next to the array. This prevents off-chip loading from affecting the outputs of any of the array elements, and by ensuring off-chip access to the inverting input of this opamp, it can be connected as a buffer amplifier or a non-inverting amplifier to scale the output as required.

To the left and top of the ESD structures are rails for $V_{DD}$ and $V_{SS}$ that are shared by other components and projects on the chip. Outside these rails are the pads that are wire-bonded to external pins for interfacing with the chip. Using the CVC array as intended by delivering a liquid sample to the surface of the chip will require insulating these wire bonds to prevent the liquid sample from affecting these connections. With the edge of the array placed approximately 100 µm from the pads, this is a significant technical challenge.

### 5.4.2 LoC Electrical Characterisation

#### 5.4.2.1 Calibration curve for LoCMOS array

The transient response seen in Fig. 4.8 shows different peak output voltages for different capacitances. Presenting the CVC response to different capacitances in this way is ineffective, so Fig. 5.21 shows a calibration curve extracted from simulations conducted on Cadence Virtuoso. This calibration curve is achieved by taking the maximum value of the RC charging response seen for one of the capacitors in Fig. 4.8.

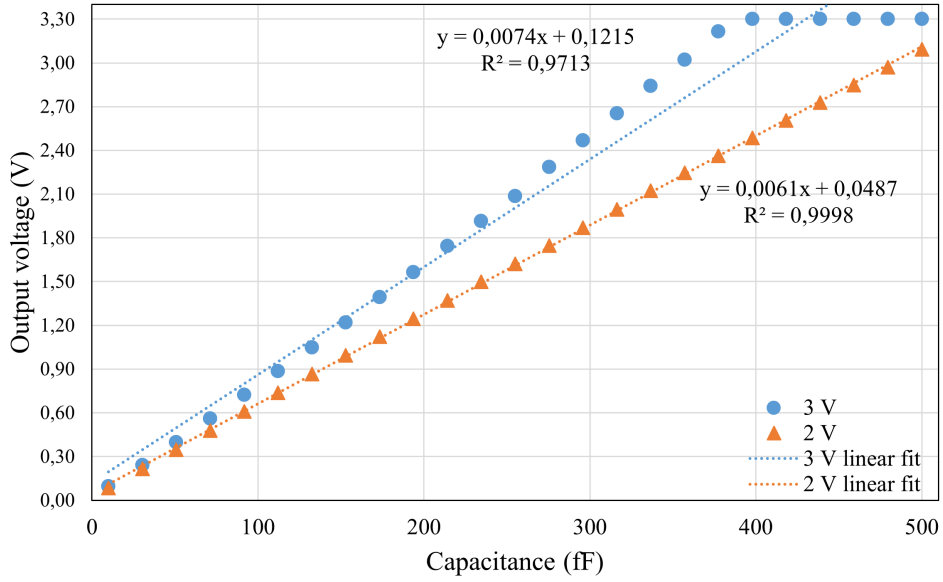



**Figure 5.21.** Simulated calibration curve for LoCMOS CVC cell.

The transfer curve between input capacitance and output voltage for a single sensor cell is nearly perfectly linear for capacitances ranging between 10 fF and 350 fF. Beyond this range, the opamp that the CVC circuit is built around starts saturating and the data points drift away from the calibration curve. This aligns closely with the 129 fF from the FEM simulations of empty 25x25 µm castellated electrodes from Table 5.3, and is more than sufficient to handle the 20% deviation at large cell concentrations seen in Fig. 5.10. The FEM simulations for the IDE, however, show a 961 fF capacitance for an empty electrode, so this LoCMOS CVC circuit will operate in its saturation region unless the DC stimulus voltage applied at the input is lowered using a resistive voltage divider off-chip, which will require re-characterisation of the CVC performance. When lowering the DC stimulus down to 2 V, linearity is maintained up to 500 fF, though from the gradient of the fit line it is evident that a lower stimulus

voltage leads to a less sensitive response - this is in good agreement with the linear relationship between the output voltage and the stimulus voltage seen in (4.15).

#### 5.4.2.2 Biosensor array

Fig. 4.14 shows the top-level hierarchical depiction of the entire CVC array including shift registers used for addressing single cells. The inputs to this array include separate clocks and start signals for the row and column control shift registers, the DC stimulus voltage, the CVC reset clock, $\phi$, and the pins for interfacing with the output buffer opamp. The output pins are the first flip-flop in both shift registers and the final voltage output of the buffer opamp. A simple test to verify that array addressing does work as intended is conducted by applying a clock and a synchronised start pulse to one of the shift registers. The start pulse has a period of 7.5 Hz and a duty cycle of 5%, meaning it will repeat after 31 rising clock edges of the 50% duty cycle, 100 Hz clock driving the flip-flops. The output of the first flip-flop is then measured over time and compared to the clock in Fig. 5.22.

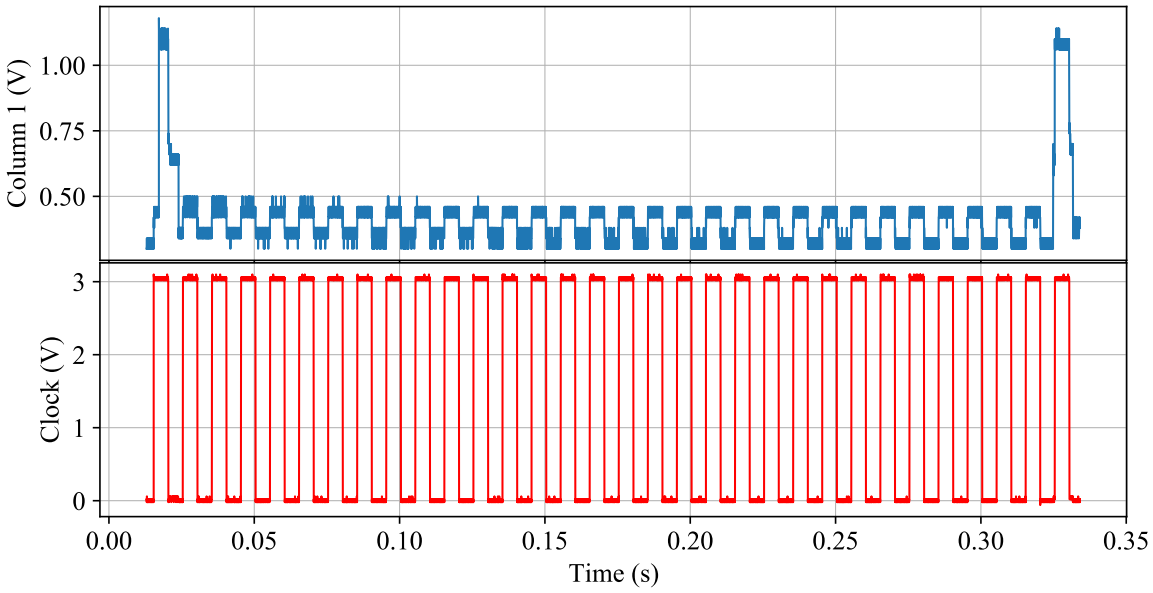



**Figure 5.22.** Output from the first D flip flop of the column control shift register to check column control.

A 3.3 V pulse slightly longer than half the duty cycle of the clock, synchronised to the first rising edge of the latter is provided as the input to the shift register. This is seen on the column 1 output as the 1.1 V pulse output during the first high cycle of the clock, falling to 0.7 V as the clock falls to 0 V. No digital buffers were included between the flip-flops or at the output, which conttributes to degradation of the input pulse between digital components. This is observed when comparing the column 1 output

to the expected output: a 3.3 V logic **1** pulse that repeats after 15 clock cycles (at 16.7 µs), while the output shows an effective logic **0**. Instead, the pulse repeats as expected, only when it has reached its period after 32 µs. An explanation for this behaviour is provided by the layout of the shift register: routing of the clock signal is such that it is transferred between flip-flops in the same direction as the pulse is transferred, meaning any clock delay degrades the integrity of the pulse. Further, there appears to be a 500 mV offset to the output that follows the clock perfectly, indicating that insufficient ground connections in at least the first flip-flop (or in fact around the route to its output pin) may be affecting the output.

#### 5.4.2.3 Opamp

Fig. 5.23 shows the DC transfer function measured using the HP 4155B parameter analyser compared to the nominal simulation from Fig. 4.4. In running the simulation for Fig. 4.4, the opamp has rail voltages $V_{SS} = 0$ V connected to ground and $V_{DD} = 3.3$ V, which is used as the input sweep range for the operational amplifier. Measurements on the parameter analyser, however, were conducted using $V_{SS} = -1.65$ V and $V_{DD} = 1.65$ V. The reason for the difference is that the opamp is aimed at single-supply use and is simulated as such, but for characterising the performance the dual-rail setup allows quick and efficient extraction of offset voltages without having to generate a potentially inaccurate DC offset voltage for the input terminals. Further, the opamp placed on the chip as a lone component can operate in dual-rail mode, since it has no interactions with library-based digital components that require a single-supply for operation. The constant 1.5V input offset from Fig. 4.4 has therefore been removed from its input as well as 1.65 V from its output for this comparison.

A comparison of the simulated DC transfer curve and its measured counterpart shows that the 20 µV offset seen in the nominal simulation translates to a 1 mV offset in the manufactured opamp, which is far outside the worst-case simulation results from Fig. 4.4. This offset could be caused by a systematic offset in the first stage of the amplifier being amplified by the large gain in the second stage. An imbalance between the M6 and M7 used for the second stage of the opamp (see Fig. 4.2) may also contribute to this offset. Over the linear operating region around the 1 mV offset, using an input voltage between -1.2 mV and -0.8 mV, the DC gain is calculated as

$$A_v = \frac{1.339\text{ V} - (-0.78\text{ V})}{-0.799\text{ mV} - (-1.198\text{ mV})} = 5.3\text{ kV/V}, \tag{5.3}$$

which translates to a voltage gain of approximately 74.48 dB. This is in good agreement with the fast-fast corner seen in Fig. 4.6. Further, the output voltage only reaches -0.8 V, which is 0.8 V short of $V_{SS}$ - this difference is slightly more than the threshold voltage of the NMOS transistors for this

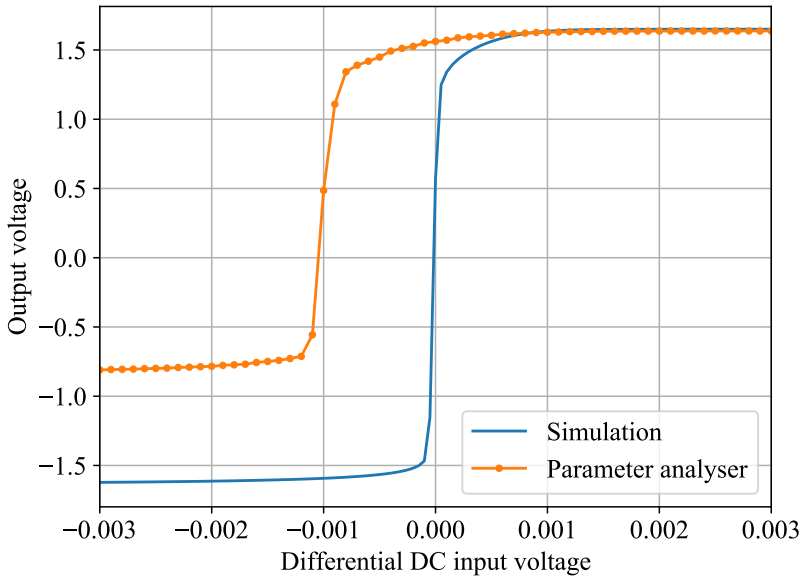



**Figure 5.23.** Comparison of simulated and measured DC transfer curve for the opamp designed in Chapter 4.

process, which may affect the use of active load transistors M3 and M4 in Fig. 4.2. This output offset is the cause of lower gain than seen in simulation due to the diminished output range and may be due to loading of the opamp, though this is unlikely. For large positive input values, the output reaches within 12.5 mV of $V_{DD}$ and follows the transfer gradient of the simulation more closely than the negative case, showing promise for the use of this opamp as long as a proper DC biasing voltage is used at the input to counteract the offset and input-range shortcomings. To this end, to characterise the response of the opamp to large-signal inputs, the non-inverting input is connected to 0 V, and a 1 V pulse is applied at a 1 V offset with the opamp connected in a buffer configuration. The data is collected using a Tektronix DPO 2002B oscilloscope with (with a probe loading of 8 pF). It is then saved and the known 1 V offset is subtracted for comparison to the corresponding nominal simulation response in Fig. 5.24.

Both the simulated and measured results show an underdamped response, and a 20% and 13% overshoot in the simulation and measured results respectively. Although both oscillate around the setpoint, the period of the oscillation in the measured case is twice that of the nominal simulated result. This may be due to the unity gain feedback affecting the transfer function by moving the compensation pole on the Nyquist plot, which translates to less overshoot and a different ringing oscillation frequency. There are fewer periods of oscillation around the setpoint in measured data, but the settling time is still longer than in the simulated case. The rise time measured using the oscilloscope is nearly 4 times that

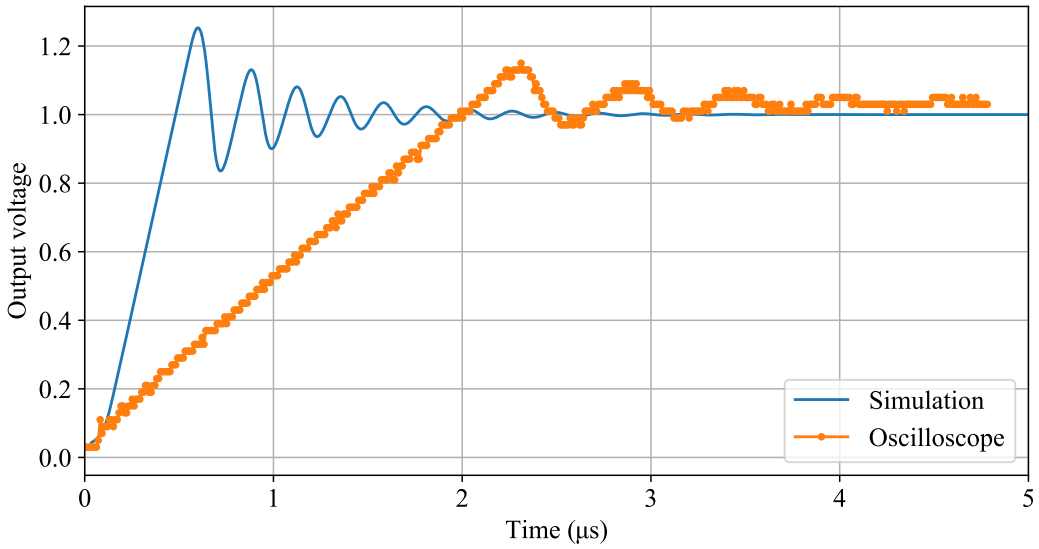



**Figure 5.24.** Comparison of simulated and measured transient responses to a large signal input to the opamp designed in Chapter 4.

of the simulation. The slew rate can be calculated using (3.11) as

$$SR = \frac{0.9 - 0.1}{1.7793\ \mu s - 0.1571\ \mu s} = 0.49\ V/\mu s, \tag{5.4}$$

which is 20% of the simulated slew rate of 2.43 V/µs, though the reason for this is likely the fact that the oscilloscope measurement uses a 50 Ω load as well as an 8 pF input input loading capacitance [84]. The 8 pF load presented by the oscilloscope is slightly larger than the 5 pF load used for simulation, so this might have a larger effect on the output than seen in simulation, or the opamp is adversely affected by a combination of corners. The likely answer is a combination of both of these factors, and this load requires more current than the output stage can provide, leading to slew rate degradation. To measure the frequency response of the opamp, two resistors (1 kΩ and 12 kΩ) are used to connect it in an inverting topology with 12 V/V gain. The measured frequency response of the opamp in dBV is shown in Fig. 5.25.

The frequency response shown in Fig. 5.25 is obtained using the opamp in dual-rail mode with $V_{DD} = 1.65$ V and $V_{SS} = -1.65$ V. A 100 mVpp sinusoid is applied to the non-inverting input while the inverting input is connected to ground via a 1 kΩ resistor and to the output through a 12 kΩ resistor. The frequency of the input sinusoid is swept and the corresponding output RMS voltage is measured and converted to dBV, after which it is recorded for plotting against frequency. At low-frequencies, the output is measured at 2.9 dBV, which translates to an RMS voltage of 1.39 V (or a peak to peak

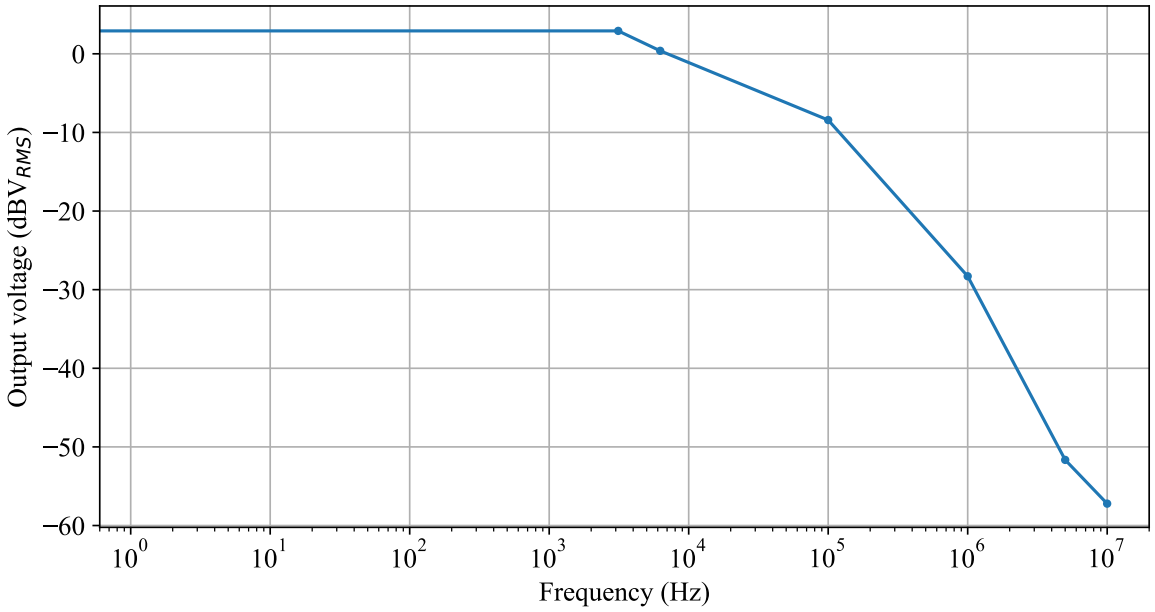



**Figure 5.25.** Frequency response of the opamp designed in Chapter 4 in an inverting topology.

voltage $V_{pp} = 1.96$ V). The theoretical gain for this circuit is 12 V/V, whereas the achieved gain is approximately 20 V/V, which is higher than expected. Unity gain for this setup is reached at 340 kHz, which means the transition frequency (according to (3.12)) for this opamp is approximately 6.8 mHz, which is close to the worst case corner seen in Fig. 4.6. A characteristic -20 dB/decade decay is seen in the output magnitude and the -3 dB knee frequency is still around 10 kHz, signifying that the system is a single-pole system and interactions with external circuitry do not affect the internal feedback compensation of the opamp. With these problems known, if external circuitry requires this opamp, it can be adjusted accordingly to ensure the desired performance. The opamp performs as expected.

### 5.4.3 External low-cost device

Fig. 3.5 shows the circuit diagram for the proof-of-concept low-cost capacitive biosensor device for point-of-need water quality monitoring. Before testing this device using polystyrene microbeads and the electrodes from Section 5.3.1, a calibration curve is required. To that end, a range of electrolytic capacitors are measured using both the device and the GWR Instek LCR meter and the output from the low-cost device is noted. Fig. 5.26 shows the measured capacitance plotted against the corresponding ADC value.

The data in Fig. 5.26 shows an exponential relation between the measured ADC value and the measured

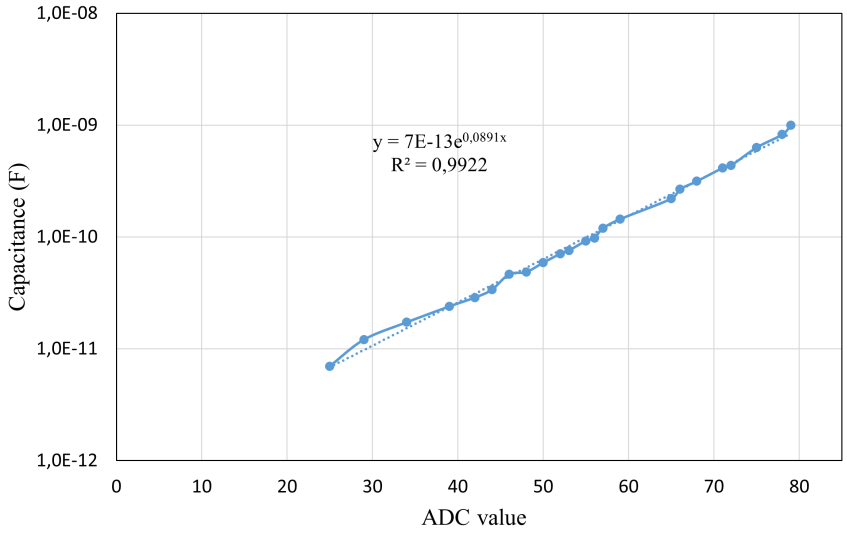



**Figure 5.26.** Capacitance calibration curve for the low-cost biosensor device in the range of 5 pF to 1 nF.

capacitance. Using a logarithmic scale on the $y$ axis shows the closeness of the exponential line fit to the data. This capacitance sensor is most effective at detecting 10 pF to 800 pF, with the exponential nature of the data at the extreme low and high end of the calibration curve forcing the uncertainty higher outside this range. At values lower than 3 pF, the output is dominated by noise causing the data to drift away from the fit line; and at capacitances higher than 1.3 nF, the output voltage starts saturating and the data moves further from the fit line. The exponential nature of the data allows a detection range of

$$R_{\text{detection}} = 20\log\left(\frac{1\text{ nF}}{5\text{ pF}}\right) = 46\text{ dB}. \tag{5.5}$$

The best-fit line equation from Fig. 5.26 is used to extract capacitance from the ADC value output by the Arduino on the serial terminal. This line has an $R^2$ value of 0.9922, showing that it is a very good fit. The experiment from Section 5.3.1 is repeated for a selection of the electrodes, the ADC output from the serial monitor is logged for each different concentration, after which it is substituted into the equation

$$C = 7\times10^{-13}e^{0.0891\times\text{ADC}}, \tag{5.6}$$

with $C$ the capacitance of the sample and $ADC$ the value of the ADC on the serial terminal. The analog value sampled by the Arduino resembles the exponential charging of a capacitor, which is the reason for this exponential relation between ADC value and capacitance. Due to the low sampling rate of the Arduino, the charging waveform cannot be sampled at its peak, which will lead to highly inaccurate values. To address this problem, the sampled value is averaged over 1024 samples before being output

to the serial port. This allows distinct capacitances to be extracted reliably at the cost of possibly including a capacitance offset to the output. The calculated capacitance values for the commercial 50 µm and 100 µm IDEs and the low-cost castellated electrode are shown in Fig. 5.27.

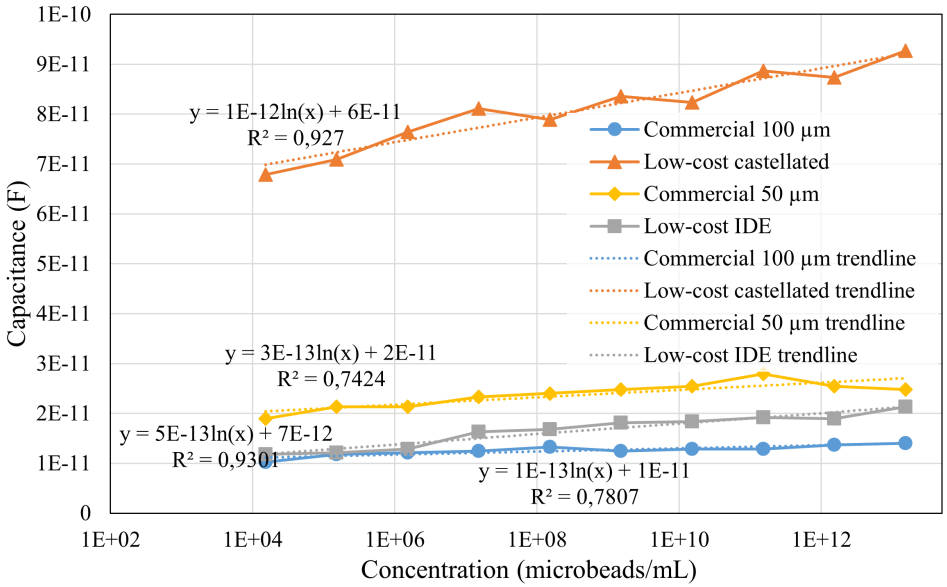



**Figure 5.27.** Capacitance of 3 µm polystyrene beads on commercial electrodes using the low-cost CVC device.

The four electrodes considered in Fig. 5.27 can be compared to their respective LCR measurements from Figs. 5.12 and 5.13. The sensitivity of the commercial 100 µm IDE when compared to Fig. 5.13, changes from 0.6 to 0.1 pF/bmL$^{-1}$, meaning the low-cost device in conjunction with this electrode is about 6 times less sensitive than the LCR meter. When comparing the sensitivity of the castellated electrode to its LCR performance in Fig. 5.12, the sensitivity changes from 0.7 to 0.1 pF/bmL$^{-1}$, a seventh of the former. This trend is inverted in the case of the 50 µm commercial IDE, which increases from 0.04 to 0.3 pF/bmL$^{-1}$, as well as the low-cost IDE, which increases from 0.02 to 0.4 pF/bmL$^{-1}$. At the lowest concentration considered, the commercial 100 µm IDE shows a capacitance of 10 pF, which is half as big as the 20 pF seen in Fig. 5.13. Comparing the capacitance at $1.5 \times 10^4$ microbeads for the low-cost castellated electrode, its value increased from 60 pF in Fig. 5.13 to 70 pF in Fig. 5.27. The largest difference is seen in the 50 µm IDE, which shows an increase in capacitance from 3 pF to approximately 20 pF, and the smallest difference is seen in the low-cost 100 µm IDE, which increases from 2 to 10 pF.

This difference is most likely due to the method used for extracting the capacitance: the LCR uses a 2 V stimulus voltage, whereas the low-cost biosensor device uses a voltage divider at its stimulus input to scale the 3.3 V from the Arduino down to 1.5 V, and the reset clock is set up to operate at 10 kHz. This lower frequency and stimulus voltage, combined with the averaging of sampled points, contribute to the change in capacitance measurements. For the two 100 µm electrodes, the difference between the LCR measurement from Section 5.3.1 is approximately 10 pF, whereas the difference for the 50 µm electrode is 20 pF. The method of capacitance extraction also affects the LOD and sensitivity as summarised in Table 5.7.

**Table 5.7.** Limit of detection and sensitivity level for each of the electrodes considered.

| Finger width (µm) | Note | LOD (pF) | Sensitivity (pF/bmL$^{-1}$) | LOD (bead count) |
|---|---|---|---|---|
| 100 | Low-cost IDE | 1.59 | 0.5 | 4 |
| | Low cost castellated | 15.2 | 1 | 16 |
| | Commercial IDE | 2.65 | 0.1 | 27 |
| 50 | Commercial IDE | 2.28 | 0.3 | 8 |

The capacitance LOD seen Table 5.7 follow the trend seen in Table 5.5, with the low-cost castellated electrode showing a LOD that is much higher than the other electrodes considered. Similarly, as this electrode has the highest sensitivity, this somewhat counteracts the high standard deviation of a blank measurement, leading to a comparable microbead LOD. Using this low-cost device, the commercial 100 µm IDE has the lowest sensitivity at 0.1 pF/bmL$^{-1}$, which lead to showing the highest LOD in bead count. The results using the low-cost device show an inversion in the order of the LOD ranking when measured with the LCR: In the former case, the commercial 100 µm and low-cost castellated electrodes perform the best, whereas in the low-cost case, these are the worst-performing electrodes. As before, a low capacitance LOD in conjunction with a high sensitivity leads to the best performance in microbead LOD.

## 5.5 CHAPTER SUMMARY

This chapter presented and interpreted the main body of results. Section 5.2 showed finite element simulation results of electrodes intended to study the effect of geometry and materials on the electric field distribution and capacitance. A new metric called the size ratio was defined to compare the performance of electrodes with differing total areas and feature sizes. Section 5.3 showed LCR and potentiostat-based measurements of a collection of low-cost and commercial electrodes using

polystyrene microbeads and *E. coli* bacteria, respectively. The sensitivity and limit of detection for the various electrodes across different sample preparation and measurement methods were compared. Section 5.4 provided characterisation results of the opamp designed for the CVC circuit, verification of the cell addressing the functionality of the LoCMOS array, and testing of the low-cost capacitance biosensor prototype using polystyrene microbeads.

# CHAPTER 6 DISCUSSION

## 6.1 CHAPTER OVERVIEW

This chapter presents a discussion, comparison, and interpretation of the results from Chapter 5. Section 6.2 interprets the simulation results from Section 5.2. This section aims to provide broad guidelines from simulation that may be used to guide the design of low-cost electrodes for capacitive biosensing. Section 6.3 discusses two important comparisons in the results from Sections 5.2 and 5.3: simulation results and measured results, and the measured results of commercial and low-cost electrodes. Critically analysing the difference between simulations and measurements allows the refinement of the latter. Analysing the performance of low-cost and commercial electrodes can identify where the latter may be improved. Section 6.4 discusses the shortcomings in the LoCMOS device and the capacitive biosensor prototype with the aim of providing a roadmap for improving both.

## 6.2 TRADE-OFFS IN LOW-COST DEVICES

The results from FEM simulations aimed at studying capacitive sensors are sensitive to a host of simulation settings, including mesh size, mesh optimisation, and solver accuracy. For an accurate comparison of different capacitive sensing electrodes in simulation, these have to be kept constant. The electrical properties of the three electrode materials considered are close enough to one another that Table 5.1 shows their E-fields are nearly identical and Fig. 5.6 shows they do not have a significant effect on the performance of the electrode. Instead, the most important facet to consider in choosing an appropriate material for the electrode traces is whether the metal chosen is inert (like gold). Both silver and copper are cheaper than gold, but more susceptible to corrosion, which may affect their performance over an extended time. A solution to the problem of corrosion is to manufacture the electrode from a cheaper material like copper, before coating the surface in gold to ensure the electrode is inert. This is the approach used in the low-cost IDE and castellated electrodes seen in Fig. 3.3. It is worthwhile to note, however, that silver oxide is still conductive, which makes this an attractive option

for a lower-cost alternative to gold electrode.

Fig. 5.2 shows that the substrate material does not significantly change the distribution of E-fields, especially in the substrate itself - the distribution of fields is affected most by the geometry of the electrode. FR4 has a larger permittivity than paper (4.4 and 2.31 respectively), which is the main reason that the maximum E-field in Table 5.1 is higher in the paper substrate case than its FR4 counterpart regardless of the electrode footprint or geometry. In Fig. 5.5, the higher permittivity paper substrate shows a slight improvement in the sensitivity of an electrode when compared to FR4, while also accompanied by a slightly larger empty-electrode capacitance. Although a trade-off may be considered between substrate materials of different permittivity, it may be more prudent to consider manufacturing and application limitations and choose an appropriate substrate material for the application, then continue refining the design of an appropriate geometry.

Table 5.1 shows that the electric fields in both the IDE and castellated case increase as the size increases from 1x1 $mm^2$ to 3x3 $mm^2$, before decreasing slightly as the size increases further to 6x6 $mm^2$. At small footprints, the capacitance of the empty electrode follows the E-field, but this effect becomes overwhelmed by footprint between the 3x3 and 6x6 mm electrode: the maximum E-field for the IDE in Table 5.1 decreases for all combinations of feature sizes, yet Fig. 5.4 shows an increase in capacitance in accordance with an increase in area. This is repeated in the castellated electrode: as the footprint increases from 3x3 to 6x6 $mm^2$, the maximum E-field increases in all but the 25 µm finger width, but the empty-electrode capacitance in Fig. 5.4 increases. The maximum E-field is, however, directly related to the sensitivity of the electrode - in Fig. 5.11, three of the largest maximum capacitance deviations in the IDE occur at size ratios of 30, 60, and 120, corresponding to the three size combinations on the 3x3 mm electrode. Although the difference is less pronounced, the same trend holds in the castellated electrode with a 3x3 mm footprint. This suggests that a local maximum E-field exists at a footprint size between these considered, and that the E-field may be used as an initial approximate guess at an appropriate electrode footprint. For such an approximate guess to be reliable, however, either the feature size or the size ratio have to be kept constant to ensure a fair comparison between electrode footprints.

The size ratio suggested in Section 5.2 is a useful tool to consider the combined effect of area and feature size - two variables that affect the performance of an electrode in different ways. As can be expected, smaller features on the same footprint electrode leads to higher E-fields and empty-electrode

capacitance regardless of geometry: the conducting plates are closer to one another, which decreases the denominator in the distance measurement of the E-field and in the parallel-plate definition of a capacitor, leading to an increase in both. When deciding on an appropriate footprint and size ratio, the empty-electrode capacitances from Fig. 5.4 have to be taken into account - larger empty-electrode capacitances could affect LOD and sensitivity, as seen when considering comparisons of LOD and sensitivity in Tables 5.5, 5.6, and 5.7. Once the electrode footprint has been established, however, it is more effective to use feature sizes that are fairly close to the size of the analyte. Fig. 5.11 shows that both the IDE and castellated electrode demonstrate reliably high sensitivity at ratios between 10 and 60. The IDE becomes more effective at higher size ratios, though from Fig. 5.4 it is evident that such a combination will result in significantly higher empty-electrode capacitance.

Regardless of the size ratio or electrode footprint, the IDE demonstrates a higher empty-electrode capacitance in simulation than its IDE counterpart. This could be due to the increased spacing between the primary fingers of the castellated electrode to accommodate the characteristic sub-fingers, lowering the effective area of the electrode devoted to fingers and sub-fingers, which contributes to the lower empty-electrode capacitance seen in Fig. 5.4. The castellated electrode also generates a non-uniform electric field that can be seen between fingers and sub-fingers in Fig. 5.1(b), whereas the field for the IDE in Fig. 5.1(a) is spread more uniformly between fingers. The combination of the larger finger spacing and non-uniform E-field are the biggest likely contributors to the lower empty-electrode capacitance, as seen in Fig. 5.4, and the lower average sensitivity when compared to the IDE in Fig. 5.11. As the features become smaller, the difference between the IDE and castellated electrode are magnified, with the maximum E-fields in the LoCMOS IDEs 2.6 and 2.4 times larger than their castellated counterpart.

The majority of the simulations show a decrease in capacitance as the concentration of cells in suspension increases, which aligns with similar simulation results [11]. The two cases where an increase in capacitance is seen are in the LoCMOS electrodes shown in Figs. 5.9 and 5.10. This difference could be due to the manner in which the electrodes are modelled inside a $SiO_2$ substrate, but since geometry has been the biggest factor in the larger footprint electrodes, this is likely the cause in this case as well. At footprints that are within an order of magnitude of the analyte (*E. coli* in this case), the small concentrations considered in Figs. 5.5 - 5.8 are impossible to monitor, with the result that Figs. 5.9 and 5.10 both consider much higher cell concentrations than the larger-footprint electrode simulations. At extremely low cell concentrations there seems to be an initial decrease in capacitance

before a turning point is reached and capacitance increases along with cell concentration.

## 6.3 PERFORMANCE COMPARISONS

To critically evaluate the lessons learned from the FEM simulations, these are compared to real-life measurements as validation of the simulation methodology. This improves the confidence in the simulation results and can identify shortfalls that need to be addressed so simulation results can be used to reliably model electrodes for similar applications. Second, the performance of low-cost electrodes and the low-cost sensor system is compared to the performance of their commercial counterparts to see whether low-cost alternatives can reliably be used for capacitive biosensor applications.

### 6.3.1 Simulations and Measurements

Using a FEM analysis platform to study the effect of increasing concentrations of cells is not an effective method of studying large concentrations of cells, as the inclusion of even a small number of cells quickly increases the complexity of the model to be solved, and the computational power required for such simulations can be better applied in either refining mesh parameters and accuracy for a single electrode, or in comparing a wider range of geometries and materials. Further, one of the main deficiencies in the approach used in this study is the fact that the materials and their properties used in Section 5.2 (especially the liquid the cells are suspended in) do not match those used for measurements exactly. This means that trends in results can be compared rather than the results directly. For example, the LB broth used for *E. coli* growth in Section 5.3.2 consists of an unknown combination and concentration of ions and proteins, which leads to unknown electrical properties when measuring. The same holds for the DI water used for the microbead verification experiments in Section 5.3.1.

Fig. 5.19 shows the capacitance extracted from EIS experiments using *E. coli* cells, with the lowest concentration of cells at 0 CFUml$^{-1}$ effectively measuring an empty electrode. In contrast to the empty-electrode capacitance in Fig. 5.4, the castellated electrode capacitance is higher than the IDE. This difference is 400 nF, which is a similar relative difference seen between the IDE and castellated electrode in Fig. 5.4. Similarly, Table 5.4 shows the empty-electrode capacitance for DI water, and the low-cost castellated electrode has a higher capacitance than its IDE counterpart. The ratio between the simulated empty-electrode capacitance in Fig. 5.4 of the castellated and IDE is approximately 0.2 compared to 23.9 using the values in Table 5.4. This large difference in electrode capacitance can be caused by the difference in the media measured. Fig. 5.4 uses simulated water while Table 5.4 uses DI water, and the simulation model may include the effect of added ions which

are not in the DI water. The gradient of the fit lines seen in Fig. 5.19 show that the castellated electrode is approximately twice as sensitive as the IDE (although the fit is not as close as in the IDE case, with an $R^2$ value of 0.52 compared to 0.62), which contradicts the sensitivity at $r_s = 60$ in Fig. 5.11, where the maximum deviation in capacitance in the IDE is much larger than the castellated electrode. During measurements of the polystyrene microbeads, shown in Figs. 5.12, 5.13, and 5.27, and summarised in Tables 5.5, 5.6, and 5.7, the castellated electrode is more sensitive than its IDE counterpart every time. The castellated electrode is let down by its LOD results by large variance when measuring blank samples. In fact, the IDE only outperforms the castellated electrode in terms of sensitivity in simulation, and the performance of the latter is better in both sets of microbead experiments and in the *E. coli* experiment. One of two conclusions can be drawn from the above: either the simulation has an unknown limitation that affects the results obtained for the castellated electrode, or the expected advantage of the low-cost castellated electrode used in measurements is not taken into account in the simulation. The relative change of the capacitance of the three electrodes used to measure *E. coli* in Fig. 5.19 shows good accordance with the simulation results, changing a maximum of 15, 20, and 60% in the low-cost IDE, low-cost castellated electrode, and the commercial IDE respectively.

The commercial and low-cost electrodes used for the microbead and *E. coli* measurements all have the same dimensions, which means all except the circular concentric IDE have the same area. The areas of the square and circular electrodes are calculated as

$$A_{\square} = l^2, \text{ and} \tag{6.1}$$

$$A_{\bigcirc} = \frac{\pi}{4} l^2, \tag{6.2}$$

where $l$ is the side length of the square electrode and the diameter of the circular electrode respectively, which means that there is only a $\pi/4$ scaling difference between the areas of the two.

Table 5.4 and Fig. 5.4 can be used to compare the empty-electrode capacitances between measurement and simulation. The smaller feature-size electrodes are patterned on glass, and since FR4 is woven fiberglass, it is not unreasonable to assume the substrate of the small-feature size and low-cost electrodes should be close in performance. This leaves the commercial 50 µm and 100 µm electrodes, patterned on transparent and white plastic, respectively, as the only electrodes that can be severely affected by the different substrate material. From the simulation results in Fig. 5.4, it is evident that the capacitance of an electrode increases as the feature size shrinks - a trend that holds up when considering the electrodes with glass and glass-based substrates. The two commercial electrodes with plastic substrates

do not follow this behaviour at all, with the capacitance dropping from 23.6 pF to 3.48 pF as the feature-size is halved. This is likely due to a very large difference in substrate permittivity caused by different materials and substrate thicknesses. Increasing the electrode area using smaller feature-size glass-substrate electrodes shows an increase in the empty-electrode capacitance, as seen from the simulations in Fig. 5.4. The two most sensitive electrodes in Table 5.5 are the low-cost castellated and commercial 100 µm IDEs with sensitivities of 0.6 and 0.7, respectively, despite the identical size ratio of 60 in both cases. Despite a large size ratio of 600, the 10 µm square electrodes have a sensitivity of only 0.03 pF/bmL$^{-1}$, whereas the concentric 10 µm has a similar sensitivity of 0.4 pF/bmL$^{-1}$. The sensitivity and LOD summarised in Tables 5.5 shows that sensitivity is not directly related to feature size or empty-electrode capacitance. From this investigation, the optimal size ratio appears to be between 50 and 100.

### 6.3.2 Commercial and Low-cost

This section discusses two comparisons between low-cost and commercial systems. Firstly, the low-cost and commercial electrodes used in the *E. coli* and microbead verification experiments. Secondly, the devices used for conducting the microbead experiments: the GW Instek LCR meter and the low-cost capacitive biosensor prototype designed for point-of-need applications. The microbead results from the larger feature-size electrodes in Tables 5.5 and 5.7 are compiled in Table 6.1. The comparison between devices is to prove that low-cost capacitive biosensors can be designed for point-of-need applications and to demonstrate the design cycle of such a device.

**Table 6.1.** Comparison of the sensitivity (in pF/bmL$^{-1}$) and LOD (in bead count) between the LCR measurement and the low-cost biosensor prototype.

| Electrode | LCR Sensitivity | Low-cost Sensitivity | LCR LOD | Low-cost LOD |
|---|---|---|---|---|
| Low-cost 100 µm IDE | 0.02 | 0.5 | 22 | 4 |
| Low-cost 100 µm castellated | 0.7 | 1 | 6 | 16 |
| Commercial 100 µm IDE | 0.6 | 0.1 | 4 | 27 |
| Commercial 50 µm IDE | 0.04 | 0.3 | 14 | 8 |

Due to the low LOD for all four electrodes considered in Table 6.1, the performance of the low-cost device (see Fig. 3.6) for use as an in-field capacitance sensor shows great promise. Since it was not designed for general purpose impedance measurement, the low-cost device is able to nearly match

the performance of the highly specialised LCR meter at a much lower cost, with the sensitivities of all the electrodes in Table 6.1 higher when used in the low-cost device with the exception of the commercial 100 µm IDE. Instead of measuring current and voltage (and therefore complex impedance) like the LCR, the CVC circuit in Fig. 3.5 disregards resistance and current and works on the principle of charge transfer between the integrating capacitor and the electrode capacitance. Transferring the charge between the sensing and integrating capacitor in alternating clock cycles and amplifying the difference as a voltage delivers only capacitance information. Variance in the output voltage is reduced by averaging 1024 sampled values, which could serve as an explanation for the improved sensitivity when using the low-cost device.

From Table 6.1, the low-cost electrodes are more sensitive to a change in microbead concentration than both commercial alternatives when using both the benchtop LCR and low-cost capacitive biosensor, with the castellated electrode more sensitive than the IDE. This result is supported by the *E. coli* measurements from Fig. 5.19, further proving the potential of microbeads as a verification technique when designing biosensor systems. Importantly, this sensitivity has to be considered together with the empty-electrode capacitance, as the relative change in capacitance is one of the most effective methods of ensuring contaminants in the aqueous sample. The capacitance of an unquantified sample may be benchmarked against the capacitance of a known uncontaminated sample, from which the potential *E. coli* contamination may be estimated using an electrode-specific calibration curve similar to Fig. 5.19 or Fig. 5.27. In this regard, according to Table 5.4, the low-cost IDE has a lower empty-electrode capacitance than its commercial counterpart (3.05 pF and 23.6 pF, respectively) and in conjunction with the higher sensitivity, this translates to a larger relative capacitance change than the commercial electrode sees for the same increase in cell concentration.

The low-cost castellated electrode outperforms its IDE counterpart when considering the sensitivity in Table 6.1, but the higher empty-electrode capacitance seen in Table 5.4 (73.1 pF against 3.5 pF) slightly counteracts the relative change in capacitance as the concentration of microbeads or cells increases, which supports the IDE vs castellated electrode simulation result seen in Fig. 5.11. This is also true in the case of the commercial 50 µm IDE, which demonstratess a 3.48 pF empty-electrode capacitance from Table 5.4, and a low sensitivity as seen in Table 6.1. These insights leave two options open to the capacitive biosensor designer: design an electrode with an acceptable gain and sensitivity, after which the capacitance sensing circuitry can be designed to provide the appropriate capacitance sensing dynamic range for the application; or design the capacitance sensing front-end with a very wide

dynamic range to accept an arbitrary electrode. The former approach is likely the better of the two, as there is a risk of losing capacitance resolution when using the latter approach. For proof of this, see the logarithmic calibration curve of the low-cost CVC device in Fig. 5.26, where only the relatively small linear portion of the curve contains useful information and large variance at the non-linear portions obscures the expected result.

### 6.4 LAB-ON-CHIP

Fig. 5.20 shows the CVC circuit layout from Fig. 4.11 manufactured on-chip. The biggest shortcoming in the current version of the array sensing system is the shift register-based addressing scheme from Fig. 4.13. Controlling the rows and columns requires two different clocks which need to be synchronised to ensure a single sensing cell is active at a time, as well as a synchronised pulse to start the operation of both cyclic shift registers. Due to the routing of the clock signal line to the flip-flops of the shift register being in the same direction as that of the pulse travelling through the register, delays in the clock signal and delays through the flip-flops are not matched. This mismatch violates setup and hold times in the flip-flop, which means some of the flip-flops do not register the correct logic value at the correct time. The degradation of the signal quality seen in Fig. 5.22 means even the logic **1** value used to keep the unused sub-cells switched off may not switch these off completely, leading to bleeding of the voltage source from one set of electrodes to another, interfering with the output of the sensing cell. This problem may be solved by improving the routing in the shift register and conducting more rigorous mixed-signal simulations. The addressing likely requires a revision in its design, potentially in a new version of the sensing device. Regardless, a carefully designed microcontroller or FPGA-based digital system is required not only to control the array, but also to digitise the output voltage from the array and ensure that the sampled value is associated with the correct sensing sub-cell. It is also possible to measure only the first 25x25 $\mu m^2$ sub-cell by not applying the clock signals at the appropriate pins, effectively isolating the sensing of this first sub-cell, which also removes the clock-related noise in the control output seen in Fig. 5.22.

The electrical characterisation results of the opamp from Figs. 5.23 - 5.25 show that the opamp does not match its simulated performance. The most likely answer for this can be seen in the DC transfer function in Fig. 5.23, as its input does not go low enough to reach the lower supply rail, which affects the results shown in Figs. 5.24 and 5.25 before the voltage step or sinusoidal input voltage can be applied in either case. Since the negative differential input voltage does not reach low enough, it is possible that the NMOS transistors used as the input active load devices ($M_3$ and $M_4$) are not biased

correctly, which affects the achievable gain in the first stage. This problem likely affects all the NMOS devices in the opamp, which means that the output-stage common-source transistor, $M_6$, is also not operating fully in the saturation region, limiting the output current that can be produced and thereby also affecting the current driving ability and output performance of the opamp. Despite this, the gain seen in Fig. 5.25 exceeds the expected gain for the feedback network applied. For an opamp to be used as a component on-chip, however, the current driving capabilities required to drive large capacitive loads off-chip are relaxed, meaning this opamp is still a useful component, especially when taking its relatively small 1600 $\mu m^2$ footprint into consideration. For such a small component, this opamp is ideal for use in a feedback loop as an active noise reducing measure or as an aid to increase stability and extend bandwidth. These are typical uses where exceptional performance at very high frequency operation is not required.

Fig. 5.26 shows that the low-cost CVC device designed using the opamp from Section 4.2 has good capacitance linearity across two orders of magnitude, and follows the results from the benchtop LCR meter. Variation at low pF capacitances introduces uncertainty at the low-end of the output, as does low-nF capacitances at the upper end of the detectable capacitance range. This design, therefore, can accommodate a wide range of electrodes. The CVC sensing system built using the custom IC and an Arduino is installed on a low-cost sensing jig as shown in Fig. 3.6, which is based on a jig (shown in Fig. 3.4) designed for use with the Metrohm Dropsens potentiostat. One of the advantages of using this jig is the possibility to use microcuvettes, a common tool in analytical chemistry, to hold the sample that needs to be measured, which removes the need to be strict about sample volumes, as each microcuvette has a limited volume and samples require the microcuvette to be filled to the top. This jig also positions the electrode reliably in the same position in the cuvette for each sample in two of the three dimensions (vertically and perpendicular to the cuvette in Fig. 3.6), but since the clothes peg in Fig. 3.6 is not fixed in the *y* axis (from left to right), the electrode can still be moved in the bulk liquid in the top of the microcuvette, which has a significant impact on the extracted capacitance. This is a trade-off to ensure the electrode holder is removable from the saddle, which means that the entire saddle does not need to be removed to replace the electrode. The wires connecting the two terminals of the electrode holder to the circuit, as well as the wires connecting the Arduino and external circuitry, are prone to slipping out of the female header pins, a design choice made to maintain the removability of the Arduino for use in other projects. Fixing these wires and the microcontroller permanently is the first step toward improving the low-cost CVC prototype. Readout and power supply occur through the USB port on the Arduino, with readout requiring an external PC to print the capacitance values. This

can be improved by adding an LCD screen to the saddle and incorporating the best-fit equation from Fig. 5.26 into the code to read out the capacitance directly. Removing the need for external readout to a PC also would also free the low-cost CVC device to use a powerbank as a power supply, making it more portable and fit for use in point-of-need settings.

## 6.5 CHAPTER SUMMARY

The results from Chapter 5 were interpreted in this chapter to highlight and discuss important features from which the most important conclusions can be drawn in Chapter 7. Section 6.2 discussed the trade-offs in materials and geometry that can be considered when designing electrodes using simulation tools like CST. Section 6.3 compared the simulated results to measured results, and compared the performance of the commercial and low-cost electrodes and the commercial and low-cost measurement systems. Section 6.4 provided a review of the CMOS design completed in Chapter 4, and discussed the advantages and shortcomings in the low-cost CVC device designed using the custom IC.

# CHAPTER 7 CONCLUSION

Section 7.1 highlights important principles for low-cost design using simulation results to answer the first research question from Chapter 1. Section 7.2 uses discussions of simulation and measurement results to provide a set of requirements for the design of low-cost devices to answer the second research question from Chapter 1. Section 7.3 provides conclusions for low-cost capacitive biosensor devices and answers the third research question. Section 7.4 discusses potential future work that may arise from the research conducted in this project.

## 7.1 PRINCIPLES FOR LOW-COST DESIGN

FEM simulations are useful for simulating small concentrations of cells. The rapid increase in computational complexity arising from the interaction of increasing numbers of cells make them less suitable for simulations containing large cell concentrations. However, the trends identified in Section 6.2 can be used to answer the first research question:

**What assumptions may be made regarding how cells interact with one another and the electrodes and how does this affect design choices surrounding electrode geometry?**

Extremely low cell concentrations are unlikely to be measured because it is simply too difficult to isolate such low cell counts, and conventional bacterial measurement techniques do not necessarily consider such low cell counts reliable [83]. However, from the results presented for the majority of the low-cost electrodes in Section 5.2, it seems that at such extremely low concentrations the capacitance decreases as the cell concentration increases, suggesting each additional cell acts like a series impedance element, which fits with a similar simulation approach seen in [11]. For larger (and more realistic) cell concentrations, the capacitance increases as the cell concentration increases, as can be seen in the LoCMOS simulations, which is more in line with established research [5], [8], [14]. The increase in capacitance is also supported by the measurement results as discussed in Section 6.3, and as such, is the prevailing assumption regarding how cells interact. Simulation tools allow for the

extraction of relative change in capacitance, which has to be considered together with the capacitance of the empty electrode to draw conclusions on the effectiveness of a particular electrode. With higher empty electrode capacitances, the high relative change in capacitance seen in IDE simulations is related to a higher absolute change in capacitance when compared to the castellated electrode. To ensure a sensitive electrode, therefore, requires considering the trade-off between empty electrode capacitance and the associated increase when cells are introduced, which can be used as inputs when setting up specifications for the required dynamic range of a biosensor device.

## 7.2 REQUIREMENTS FOR LOW-COST DEVICES

Although the LoCMOS system is useful in a laboratory setting, access to the infrastructure required to design and manufacture a custom on-chip capacitive biosensor is not ubiquitous. As such, a large section of the investigation was focused on off-chip solutions which may be easier to reach for researchers designing low-cost biosensor systems for resource-limited deployment. This focus on off-chip electrodes is used to answer the second research question:

**How do the materials and geometry of an off-chip electrode affect the accuracy of a device and its associated cost?**

Using the comparison of simulation results and the associated measurements in Section 6.3, it is evident that the material of the electrode itself does not have a significant effect on the measurement performance of the electrode (as long as it is a good conductor) - the main consideration is how the metal that is used interacts with the aqueous sample. Secondly, the permittivity of the substrate material plays a non-negligible role in the empty-electrode capacitance, though not necessarily in the achievable sensitivity. Using a substrate material with a higher permittivity leads to larger E-fields and larger empty electrode capacitance, though the electrode performance is dominated more by geometry than by the substrate material. As such, the electrical properties of the substrate itself need only be considered briefly, with properties like inertness, flexibility, ease of manufacturing, degradation in an aqueous environment, and costs the main drivers when choosing a substrate. Potential substrates regarding electrical properties include FR4, paper, and plastics (which can be manufactured using additive manufacturing techniques).

It is important to note that the relative capacitance change used to classify the effectiveness of electrodes in simulation (most notably Fig. 5.11) does not relate directly to the sensitivity used for measured data. Although the castellated electrode shows a smaller relative capacitance change than the IDE for a similar increase in cell concentration in simulation, the castellated electrode is more sensitive than

its IDE counterpart in both microbead and *E. coli* measurements. For equal feature sizes, there is no difference in manufacturing difficulty between the IDE and castellated electrode, though for extremely small feature sizes, the complexity in the castellated electrode may lead to lower usable electrode yield and consequently, cost per electrode. The optimum footprint is between 3x3 $mm^2$ and 6x6 $mm^2$, with the associated size ratio limited by the available manufacturing techniques. When considering the size ratio, an apparently ideal value seems to be between 50 and 100, but smaller than 50 is acceptable, as is larger than 100. Larger size ratios generally mean smaller feature sizes, which will involve specialised manufacturing and increased costs.

## 7.3 CONCLUSION FOR LOW-COST DEVICES

The combined insights from the simulated and measured capacitance results, as well as those gained from designing the LoCMOS and low-cost capacitive biosensor systems can be used to draw up guidelines for designing similar low-cost biosensor systems.

**What external hardware is required besides the Lab-on-Chip (LoC) to deliver a complete sensing system, and what trade-offs are acceptable to ensure a low-cost point-of-need biosensing device?**

Fig. 7.1 shows the suggested design process for designing a capacitive biosensor, and is kept intentionally broad to allow the design flow to be used for a general biosensor device. The flow starts with mechanical design, and then the electrode itself is designed, after which the electrical system is designed. Each successive step has a feedback path which can be considered if necessary, as well as validation steps that are critical during the design of the electrode and the electrical system. Overall system-level application-specific verification is not included in this diagram, but is a crucial design step for any electronic system.

The mechanical design begins with considering how the electrode itself has to interact with the rest of the electrical system - this includes holding the electrode in place and its connections to the analog front end. Next, the sample delivery method has to be considered: this can be flow-based using microfluidic channels and micropumps; or a non-flow based system similar to the system used in this work can be used. In either case, sample preparation has to be a prime consideration, especially for deployment in low-cost, point-of-need applications. If the sample delivery system requires a redesign of the electrical interfacing, this can be done.

Once the mechanical design has been finalised, the electrode itself can be designed using the insights

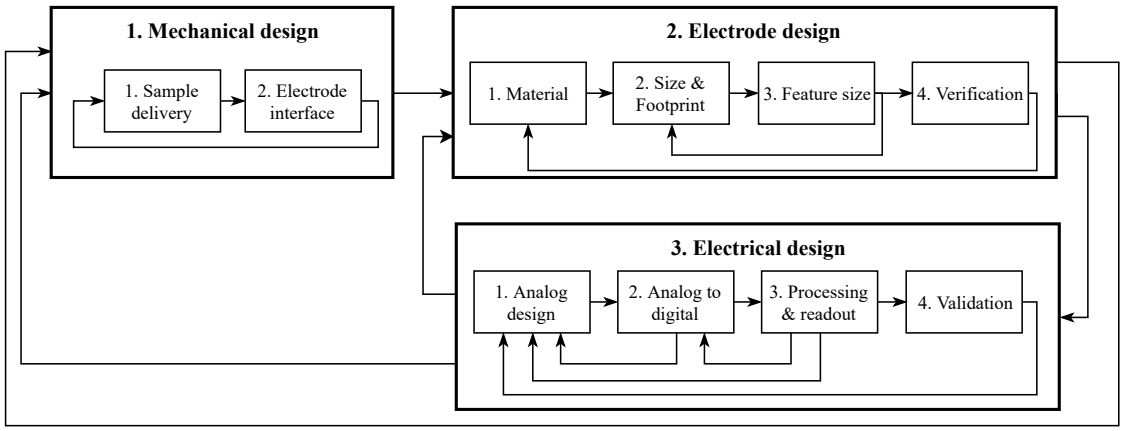



**Figure 7.1.** Design flow of a low-cost capacitive biosensor for point-of-need water quality monitoring applications.

and methods seen in this study, starting with substrate and electrode material considerations, followed by determining the footprint and the size ratio. This is the recommended order, though there may be some revision between footprint and size ratio. With the analytical side of the biosensing system fixed, the electrical design is next.

The analog design requires the design of a circuit that converts capacitance to a voltage or current that can be digitised, after which the requisite signal conditioning can be done before digitisation. An appropriate microcontroller handles signal processing and readout of the capacitance final value. The final step in the design is verifying the performance of the device using commercial high-performance tools (such as the LCR used in this study) and, if necessary, any of the preceding 3 steps can be repeated to ensure the device performs as expected.

The hardware required for a low-cost biosensor device using the LoC designed in this work includes the mechanical design for sample delivery and electrical interfacing (seen in Fig. 3.6), an analog to digital converter, and a microcontroller for processing - implemented together in the Arduino in this work. This provides a complete sensing system that can be deployed in point-of-need settings to assess the quality of water. It is important to note that this solution in its present form does not have the required specificity to be able to identify the presence of *E. coli* alone, but the measured change in capacitance could be an indicator of contamination.

The LoCMOS array-based capacitive sensor requires more complex mechanical design to deliver the sample to the sub-surface electrodes and a more complex processing system to control the array, though this can be implemented in software using an appropriate microcontroller.

## 7.4 FUTURE WORK

Future work in this project includes refining the simulation set by considering the effect of time-varying sinusoidal input voltages in more depth and studying more effective methods of introducing large numbers of cells to the simulation model. The simulation suite can be expanded by comparing non-symmetric electrodes (with differing finger and gap widths) and rigorous verification of a wider range of simulation results by manufacturing a subset of electrodes for measurement.

There is also potential in using the CMOS array-based capacitive sensor despite its shortcomings, though this requires meticulous mechanical design to mount the die and deliver the sample to the sub-surface electrodes while protecting the electrical interfaces to the die from liquid interference. When considering the use of the LoCMOS sub-surface electrodes, a microchannel-based liquid delivery system will have to be designed to ensure the droplet applied to the surface of the IC is delivered to the array sensing area. Although this does not prevent the droplet from spreading across the entire surface of the IC, results can be optimised by ensuring the droplet containing *E. coli* (or microbeads) is localised to the sensing area. This is a good application for additive manufacturing for electronic systems, as this allows rapid and low-cost prototyping of devices. The highly linear response of the capacitance sweep in Fig. 5.21 shows the potential of this LoCMOS CVC circuit to detect *E. coli* cells, and since the detection range can be altered slightly by adjusting the input stimulus voltage, this sensor can be adapted to detect similar bacterial cells by simply changing the external circuitry that interfaces with the LoCMOS system.

Further work can also be conducted using *E. coli* or other bacterial cells with the capacitive sensing system and validating the performance with standard cytometry methods such as agar plating and enzymatic conversions to study cell viability. The system functionality may also be redesigned to include sinusoidal variable-frequency stimulation voltage similar to EIS, which can be used to identify unknown cells in a heterogenous sample using their specific electric properties.

The impact of the trade-offs discussed in this study on the practical implementation of a low-cost point-of-need biosensor device for specific applications also needs to be quantified. This is to ensure

that the cost of a device can be minimised without compromising on the sensing performance thereof in its practical context.

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