energies

MDPI

Article

A Unified Rule-Based Small-Signal Modelling Technique for Two-Switch, Non-Isolated DC–DC Converters in CCM

Lebogang Masike [1,*], Michael Njoroge Gitau [1] and Grain P. Adam [2]

[1] Department of Electrical, Electronic and Computer Engineering, University of Pretoria, Pretoria 0002, South Africa; njoroge.gitau@up.ac.za
[2] Department of Energy, NEOM, Tabuk 49643, Saudi Arabia; grain.adams@neom.com
* Correspondence: lebogang.masike@up.ac.za

Abstract: The inherent non-linear behavior of switch-mode power supplies complicates the task of computing their linear models, which are essential for a model-oriented control design of DC–DC converters. In a model-oriented control design approach, the accuracy of the plant model directly influences the performance of the control system as the plant parameters tend to be linked to the controllers' gains. Moreover, the extractions of linear dynamic models of high-order non-linear plants such as DC–DC converters are laborious and mathematically intractable. Therefore, in this paper, a generalized expression that represents either the audio-susceptibility or the control-to-output voltage transfer function for voltage-mode control is proposed. The proposed generalization reduces the task of computing the small-signal model of a given converter to simple calculations of coefficients of generalized transfer function/expression. It is shown that the coefficients of the generalized model can be deduced by inspection, directly from the circuit diagram, allowing the whole model to be computed by inspection. Additionally, the proposed modelling technique will be shown to have secondary use of verifying accuracy even when conventional modelling techniques such as state-space averaging or circuit averaging are used.

Keywords: DC–DC converter; small-signal modelling; converter dynamics; unified analysis; controller design; generalized model; CCM

Citation: Masike, L.; Gitau, M.N.; Adam, G.P. A Unified Rule-Based Small-Signal Modelling Technique for Two-Switch, Non-Isolated DC–DC Converters in CCM. *Energies* **2022**, *15*, 5454. https://doi.org/10.3390/en15155454

Academic Editors: Vincenzo Di Dio and Valeria Boscaino

Received: 14 June 2022
Accepted: 8 July 2022
Published: 27 July 2022

1. Introduction

DC–DC converters are widely used in DC voltage matching or changing of DC voltage levels, i.e., to perform similar functions as AC transformers. These devices offer several attractive features such as high efficiency and small footprint compared to their predecessor, the linear regulator [1–5]. To maintain a regulated output voltage, it requires a feedback compensation system; which is normally designed employing model-oriented controller techniques. A plant model forms a primary ingredient in the design process of the compensator [6–8]. There are numerous modelling techniques discussed in open literature, which include: network analyzer test, simulations and analytic approach [9–11]. The acquisition of a model for a specified converter topology based on the latter technique, is more intuitive than the former two methods; thus, it is the most preferred method [9,12,13]. Since DC–DC converters are nonlinear systems, semi heuristic analytic methods are employed to compute their equivalent linear models, such that linear control techniques may be used [14,15]. Although based on simple rules (i.e., averaging and linearization), these methods are time consuming and laborious [15,16]. To develop a model that accurately represents the physical system within a particular time-scale or frequency range, model of interest, and effects of all the converter components that affect relevant system electromagnetic transients must be accounted for and only neglect the irrelevant effects [13,17–19].

Presently, proliferation in the application areas of DC–DC converters has complicated the task of regulating the converter for a specified task. This is due to areas of application such as the automotive industry with the advent of the electric vehicle [3,20], HVDC systems

with the advent of converters with fault blocking capabilities, and on-going research into the creation of an optimized DC breaker [21]. Moreover, energy management requirements in micro-grids further complicates the control task. With this in mind, the task to describe the plant model or a component thereof, should (at least for well-known topologies) be of the least complexity.

In [14,15,22–25], the converter modelling process based on the most popular analytic converter modelling techniques such as state-space averaging, circuit averaging, current injected equivalent circuit, and switching flow graphs (SFG) are well described. Two main steps are identified as common amongst these modelling techniques, i.e., averaging and linearization. As such, all these techniques result in the same model for a given converter topology operating under a specified mode of conduction, i.e., continuous conduction mode (CCM) or discontinuous conduction mode (DCM). A slight model discrepancy is noted when using the circuit averaging approach based on how the series resistance of the capacitor is considered, but this does not change the accuracy nor the order of the transfer function [26]. Numerous reviews on these modelling techniques and their respective merits and demerits are also reported [27–32]. The use of one modelling scheme over the other will mainly be a designer's preference and the overall objectives of the design, e.g., if the design aims to highlight model attributes while using well known circuit components and analysis techniques, the circuit averaging modelling scheme will be the best choice. Furthermore, a review of all the popular modelling techniques [22–25] reveals the following limitations or demerits:

- Time consuming: the two main steps (i.e., averaging and linearization) present in all these schemes require increased computational effort, and thus constitute the bulk of the time requirements of the respective scheme;
- Intractable mathematics with higher-order systems: the number of equations increase with an increase in reactive components of a circuit, and the manipulation of such equations can easily become intractable;
- Limited validation of accuracy: To date the only way one can validate the accuracy of the resultant transfer function is mainly limited to model order which is linked to the number of reactive components in a circuit, i.e., four reactive components, implies fourth order circuit. Secondly, the presence of the right-half plane zero (RHPZ) in boost and buck-boost topologies. These methods are not sufficient to verify model accuracy since each coefficient of the transfer function has an influence on the performance of the analysed component. Thus, a more rigorous accuracy verification scheme is needed;
- Lack of unified analysis: Most converters are treated in isolation; fewer works attempt to report a unified approach for DC–DC converter modelling. Even when a unified approach is considered, attributes such as converter cell [26], converter order [26,33] and functionality [22–24] are used as discriminants. Such an approach requires a repeat of the modelling steps and corresponding dynamic analysis for any other converter variant.

To reduce the model computation time, maintain tractability with higher-order converters and subsequently simplify the controller design step when using these inherently laborious modelling techniques, researchers have looked at developing reduced order models [34–37]. These models present a trade-off between accuracy and controller design complexity. It should be borne in mind that models derived using averaged techniques have limited accuracy due to the averaging step which essentially ignores the switching nature of the converters [14,15]. As such, model order reduction techniques serve to further narrow the upper accuracy limit of these models. To reduce computation effort while retaining default model accuracy, unified large and small-signal models for specified basic converter units have been proposed [26,38,39].

Tollik et al. [40] recognised the unnecessarily cumbersome process of modelling DC–DC switching regulators, with the proposal of a new continuous modelling method aimed at reducing the order of the matrices to be inverted. The study made the mathematics more tractable especially for higher order converters but failed to address issues pertinent

to time and effort in the derivation of the model. A substantial amount of tedious algebra still appeared in the new method. The feasibility and benefits of the technique the current study proposes is partially promoted by the work conducted by Abramovitz [41], in which switching flow graphs were used to unify tapped-inductor-based DC–DC converters and elementary DC–DC converters. This work employs what it termed the 'tapped-inductor switcher' (TIS) whose generalized model can be used to compute dynamic models of numerous converters. The main demerit of this work is that it considers a small group of closely related converter topologies. Additionally, the variables of the TIS depend on the original converter topology, which requires initial analysis of a specific converter. Even after computing the correct variables of the TIS, substantial computational effort is still required to compute models of interest from the generalised switching flow graph of the TIS. Lastly, it considers converter functionality as a discriminant when employing the TIS to compute models for basic converters. This technique is extended to include leakage inductance [38], but still maintains the same demerits.

Rico [42] employed the tapped-inductor DC–DC converter topology to show the same results obtained by Abramovitz. In this work, he also considered the discontinuous conduction mode which was negated in the study conducted by Abramovitz. The work further promoted the benefits of unifying the model for a range of DC–DC converters. Although both modes of conduction were considered, they were treated in separate sections as unique converter conditions. No unifying efforts were made. One of the demerits of the study was that converter functionality was still treated as a discriminant. Moreover, a total of six converters were unified into three pairs. Considering the large number of available DC–DC converters, this work failed to be of significant value. The highlight of Rico's work was in showing that the tapped-inductor DC–DC converter was the most general converter topology when compared with elementary converters.

Furthermore, Ref. [16] read together with its correction paper [43], offers an alternative modelling technique based on the computation of energy factor and sub-sequential parameters such as PE (pumped energy), SE (stored energy), CIR (capacitor/inductor SE factor), LE (lost energy), etc., to capture the small and large signal response of DC–DC converters. It can be seen from the accompanying examples in the paper that the computation of the transfer function was still mathematically involved. Moreover, the method failed to adequately justify the second order approximation for higher order circuits.

Generalized large-signal and steady-state circuit models have been proposed for both CCM and DCM [44–47], but small-signal analysis continues to be considered unique for each converter topology. Current research is more focused on improving the frequency band within which the accuracy of a given DC–DC converter is valid [48,49], and continues to negate the requirement to reduce the computational effort seen when analytically deriving DC–DC converter small-signal models. For well-known systems such as DC–DC converters, a less cumbersome method is needed to increase the efficiency in current model-oriented control problems. Software packages that can easily provide the frequency response of a given converter exist, but they fail to provide the necessary intuition pertinent to converter operation, especially for pedagogic reasons. Finer attributes pertinent to a given circuit component giving rise to a pole or a zero and the corresponding exact position and frequency of a pole or a zero in the model are hardly provided by the software packages available. Thus, the objective of the current research to reduce the computational effort in the derivation of DC–DC converter small-signal dynamic models, and also provide a quick accuracy reference, while retaining intuition, proves relevant.

Contributions of the study towards addressing the demerits of the currently-available modelling techniques:

- Time consuming: the proposed modelling scheme results in models similar to those obtained using [22–25] but does not involve the averaging and linearisation steps in the model derivation process. As such, it enables a more rapid model development;

- Intractable mathematics with higher-order systems: the proposed modelling scheme directly computes the coefficients of the numerator and denominator polynomials of the transfer functions, which maintains tractability even for higher order converters;
- Limited validation of accuracy: the inherent coefficient-based derivation process of the proposed modelling scheme achieves a more refined and rigorous accuracy verification scheme as compared with current verification methods;
- Lack of unified analysis: in the proposed modelling scheme, the converter cell, converter order or converter functionality are nullified as discriminants in the derivation process.

The study considers dynamic models of two-switch, both 2nd and 4th order, non-isolated DC–DC converters. These are cells A and C–G in [26]. This range of converters includes well-known and commonly used converters such as the conventional buck, boost and buck–boost converters as well as the cuk, sepic and zeta converters. The rest of the paper is structured as follows: The motivation, operating principles and limitations of the proposed modelling scheme is presented in Section 2. The procedures for computing continuous time small-signal models using the proposed modelling scheme are presented in Sections 3 and 4. Further considerations of the modelling scheme are presented in Section 5. Section 6 validates the advantages presented by the proposed modelling scheme. Discussions and conclusions are presented in Sections 7 and 8, respectively.

2. Development of the Modelling Scheme

Consider the computation of a small-signal model of DC–DC converters employing the method of switching flow graphs as presented in [25]. The following observations can be made from the modelling scheme:

- The same number and form of 'flow graph nodes' are present for converters with an equal number of components, i.e., the flow graph nodes shown in Figure 1 will be the same for the buck and buck–boost converters;
- The establishment of flow graph branches is a function of element position and switching action;
- Small-signal modelling of the switching action is standardized in the derivation process as shown in Figure 2. As such, element position is the only variable which can dictate the form of the resultant model.

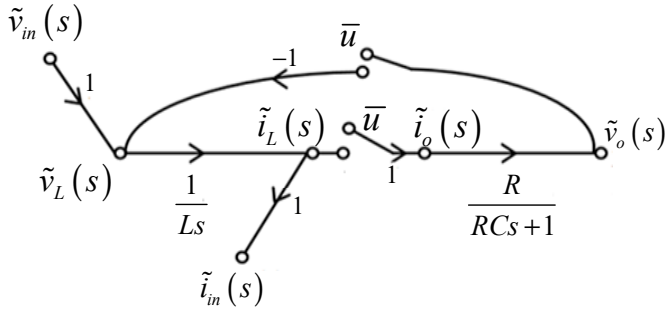

Figure 1. Switching flow graph representation of the conventional boost converter.

This suggests that there is definitive causality between the position of the switches in relation to passive components and the resultant small-signal model. Thus, if the form of the resultant model is fixed to a standard form, the causality will be between the position of the switches and the variables of the standard model. Therefore, it seems as if the task to unify the dynamic model only entails unifying the branches on the SFG diagram. In this study, the aforementioned causality is investigated and modeled into generalized statements which can be used to develop small-signal models for a range of DC–DC converters. The intentions of this study are to first identify the circuit element with the most influence on the final model structure, attempt to study all the possible variants of the identified element together with the corresponding influence of each variant, and finally, develop a unified

theory or set of rules that generalize the influence of the identified element, such that the dynamic model of a given converter may be derived by inspection of the circuit diagram.

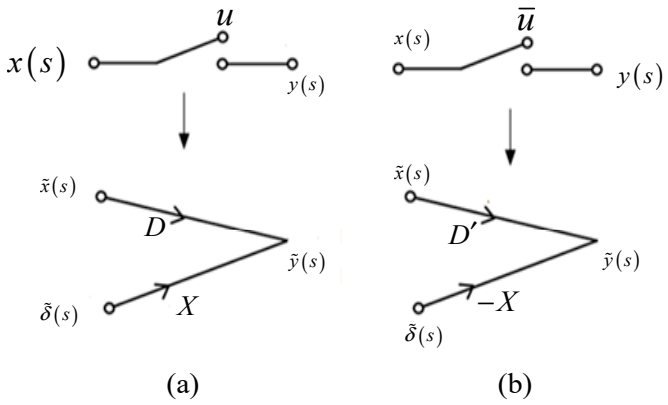

Figure 2. Small-signal switching flow graph for the switch (**a**), and the diode (**b**).

2.1. Identifying Influential Element and Its Variants

Taking note of the influence that the switching elements display throughout all the major modelling techniques, (i.e., state-space, circuit averaging or SFG), it is then more convincing to identify the two switches as the elements with the most influence on the resultant model since they constitute the entire non-linearity of any switching converter [47]. There are two main variants of switching elements for the group of converters considered in this study, i.e., single-pole double-throw (SPDT), commonly known as the PWM switch [47], or single-pole single-throw (SPST), which is a model for any discrete switch. For all converters in groups A and C–F of [26], the operation of the switching matrix, which is comprised of the active switch and the passive switch, can be fully described by an SPDT switch. This feature is seen in 24 converters out of a total of 30 converters considered in the study. The switching matrix for converters in group G of [26] cannot be fully described by an SPDT switch, since it mainly consists of two separate SPST switches. A direct application of the rules developed for the SPDT group on converters in group G results in incorrect models when compared with the corresponding models developed using existing modelling techniques. This observation comes as no surprise, due to the study by M. Veerachary [33] where a generalized large-signal flow graph model of the most popular fourth-order converters is presented. The converters from group G showed unique traits which were subsequently added to the proposed common SFG. As such, the set of rules developed for converters in group G (SPST group), will be different from those developed for converters in groups A and C–F in the proposed modelling procedure.

2.2. Introducing Model's Standard Form

To avoid unnecessary confusion, a standardized form of the resultant dynamic model is established, i.e., all derived converters' models are computed in established standard form. Most transfer functions of interest for any system are often represented as a ratio of two polynomials. As such, the standard form opted for, in this paper, is shown in (1). Its choice was mainly influenced by the fact that some of the coefficients in the model retain the same combination of the circuit component's attributes, irrespective of circuit topology or functionality, as will be shown later. In addition, the task of computing the plant's model is reduced to simple calculations of coefficients; and the order of the model is readily seen from the standardized form. Moreover, the standardized model is more suited for analysis, particularly with software tools which allow a quick log of the model's coefficients.

Since the main task in the proposed dynamic modelling process is now concerned with computing the coefficients of the polynomial of s, the substantial amount of time typically spent in deriving the dynamic model using existing modelling techniques will no longer be necessary. The thought process is that if these coefficients can be computed with

ease, then the entire modelling process is simplified, and will require substantially reduced effort and time for deriving models.

$$G(s) = \frac{A_m s^m + A_{m-1} s^{m-1} + \ldots + A_0 s^0}{B_n s^n + B_{n-1} s^{n-1} + B_{n-2} s^{n-2} + \ldots + B_0 s^0} \quad (1)$$

NB: For converters whose non-ideal parameters are negligible (as in this paper), $m \in (\mathbb{N} < n)$. The value of n is always equal to the number of reactive components in the circuit. Thus, the maximum value of m for a 2nd-order system is 1, and for a 4th-order system is 3.

Component Numbering

Component numbering facilitates easy reference of a component in a circuit. The golden rule in carrying out this task is to note that components are numbered in the direction of conventional power flow, i.e., from left to right, or from top to bottom, as shown in Figure 3. This creates identifiers for a given converter component within any of the converters in this study. It should be noted that the same circuit element-numbering scheme applies to the two main groups of converters considered in the study, i.e., SPDT group and SPST group (group G).

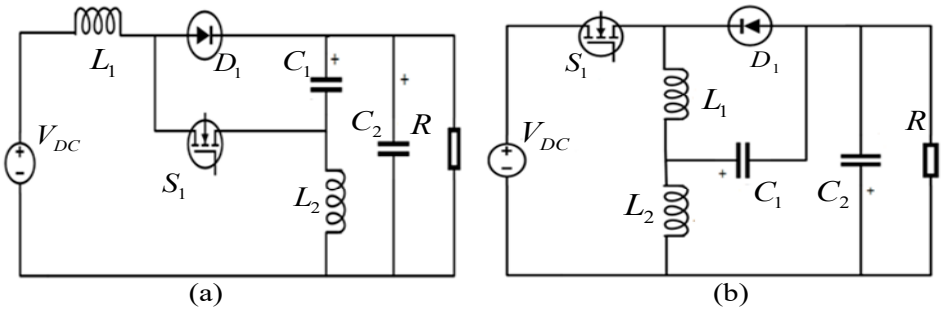

Figure 3. (**a**) Circuit diagram for converter D3 and (**b**) circuit diagram for converter E3 in [26].

2.3. Additional Attributes for Modelling Group G Converters

Although switching sequentially, the physical structure of the switches in group G cannot be forged to a single unit. With that borne in mind, it will be fitting to identify an additional trait which can be used together with the two separate switches in group G to develop a method for determining all the coefficients of the model by inspection of the circuit diagram. The identified trait when employed together with the separate SPST switches should enable accurate determination of the relevant conduction times where required. The output-port current wave-shape, although with three states, is sufficient for use as an additional unique trait, alluded to above. The 'output-port' current wave-shape shows a total of three unique wave-shapes. These are shown in Figure 4 (controlled switch or diode feeds the output-port), Figure 5 (output-port node is fed by an inductor plus a controlled switch or diode), and Figure 6 (inductor feeds the output-port).

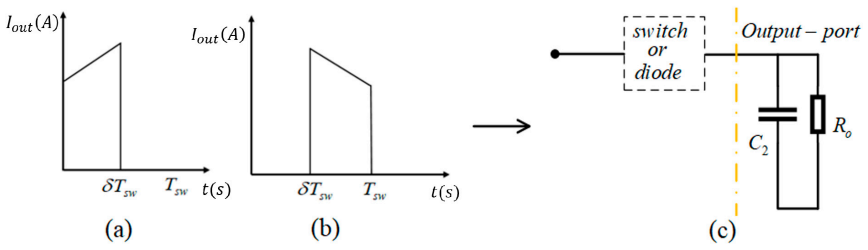

Figure 4. Positive pulsed output-port current component (**a**) active switch current, (**b**) diode current and (**c**) equivalent circuit diagram.

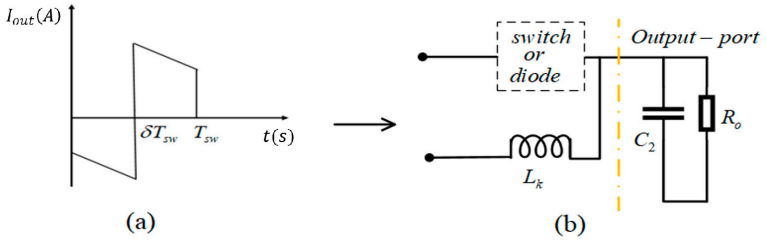

Figure 5. (**a**) Pulsed output-port current with both positive and negative components and (**b**) circuit diagram.

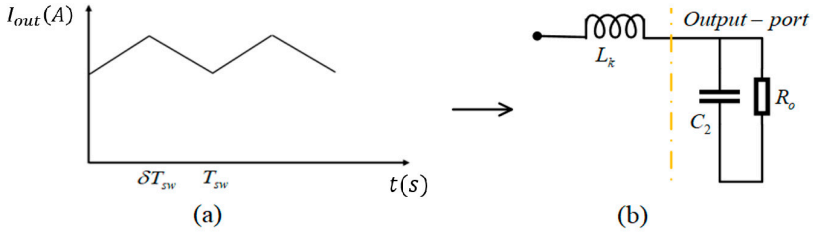

Figure 6. (**a**) Positive non-pulsed output-port current and (**b**) circuit diagram.

2.4. Computing Steady State Votage Convertion Raito

For the group of converters whose switching matrix can be described with an SPDT switch, the steady-state voltage conversion ratio for any given converter topology within the group is given by one of the three main functions. These functions are: bucking function (2), boosting function (3), and buck–boost function (4) with and without polarity inversion [26]. Equations (2)–(4) are prominent steady-state voltage conversion ratios of the three most basic DC–DC converters. This suggests that they are easy to remember since they represent basic voltage conversion functionalities in DC–DC converters. The 'D' in (2)–(4) is the DC quiescent operating point.

$$D \tag{2}$$

$$\frac{1}{1-D} \tag{3}$$

$$\frac{D}{1-D} \tag{4}$$

For the SPST group, with the exception of the zeta and sepic converters whose voltage conversion ratio is given by (4), the remaining converters' voltage conversion ratio expressions are not as common, but they are still classified as either buck, boost or buck–boost in terms of functionality. In either case, at most only two simple average inductor voltage equations are sufficient to compute the voltage conversion ratio of any converter. This is shown in (5) and (6) as examples for second order and fourth-order converters in Figures 7 and 8, respectively. Alternatively, these voltage conversion ratios can be obtained from the tables in [26].

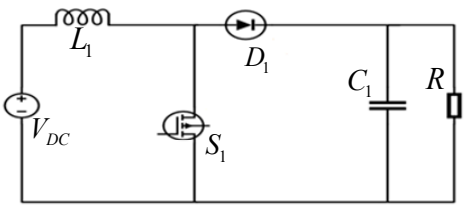

Figure 7. Boost converter circuit diagram.

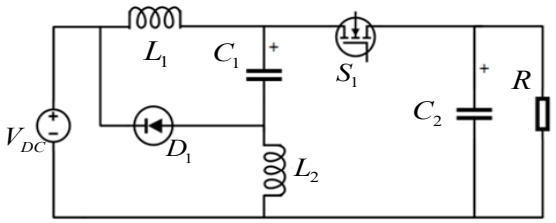

Figure 8. Circuit diagram of one of the converters considered in this study (G2).

$$\left.\begin{aligned} V_{L_1} = L_1 \tfrac{di_{L_1}}{dt} = 0 = V_{in}D + (V_{in} - V_0)(1 - D) \\ \tfrac{V_o}{V_{in}} = \tfrac{1}{1-D} \end{aligned}\right\} \quad (5)$$

$$\left.\begin{aligned} V_{L_1} = L_1 \tfrac{di_{L_1}}{dt} = 0 = (V_{in} - V_o)D + \left(-V_{C_1}\right)(1 - D) \\ V_{L_2} = L_2 \tfrac{di_{L_2}}{dt} = 0 = \left(V_{C_1} - V_o\right)D + (-V_{in})(1 - D) \\ \tfrac{V_o}{V_{in}} = \tfrac{2D-1}{D} \end{aligned}\right\} \quad (6)$$

2.5. Converter Non-Linearity Considerations

The fundamental step in the modelling process of switching converters is averaging. This step takes two models from two sub-interval linear time invariant circuits and merges them into one continuous model over the entire modelling period. This mathematical convenience is achieved at a cost of model accuracy range, i.e., averaging reduces the range of frequency within which the derived model is valid. This is considered to be similar to an application of a low-pass filter with a cut-off frequency of around a third to half of the switching frequency [24]. It can be seen from Figure 9 and accompanying plot in Figure 10 that both the ideal and non-ideal plots are congruent even up to 60 kHz. Figure 9 is a plot for a converter switching at 50 kHz. As such, this averaged model should be valid only up to around 17–25 kHz. This proves that non-ideal attributes may be neglected without a substantial effect on the choice of a compensator. The worst-case scenario of the discrepancy between the ideal and the non-ideal can be suppressed with a simple proportional controller. It will, therefore, make sense for one to only really consider non-ideal behavior when high frequency dynamics are of interest. Given the inherent limitation of averaged models, accurate analysis of high frequency dynamics will require non-averaged models. As such, the incorporation of non-linear behavior when computing averaged models for converters may be neglected, as in the case of the proposed modelling technique.

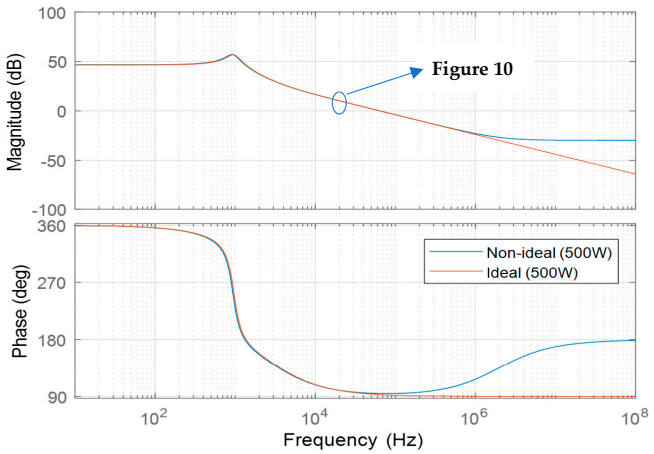

Figure 9. Bode plot showing effects of non-ideal characteristics on the system.

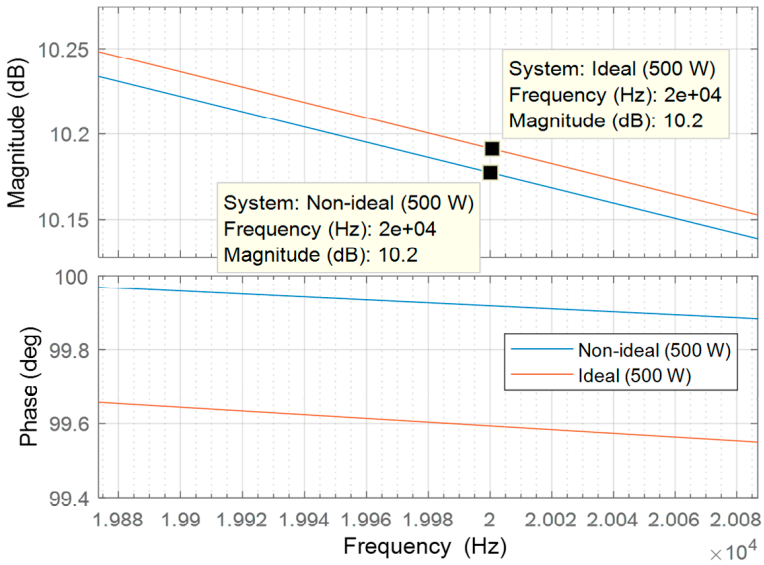

Figure 10. Bode plot showing error incurred when non-ideal characteristics are ignored.

The dynamic model of a conventional boost converter is considered to evaluate the effects of non-ideal behavior on the resultant frequency response. A non-ideal control-to-output voltage transfer function of the conventional boost converter is shown in (7) as derived in [22] using the popular state-space averaging approach. Table 1 captures all the circuit parameters considered in the evaluation. All the circuit parameters were sized based on the voltage and power specifications. The saturation voltage for the active switch of the conventional boost converter was selected from the IXGH100N30C3 datasheet, assuming a 140 °C maximum junction temperature for our operation. The forward voltage of the diode was taken from the RF1501TF3S datasheet.

$$\frac{\widetilde{v}_o(s)}{\widetilde{\delta}(s)} = \frac{-R_L I_L C L r_c s^2 + \left\{\left[(1-D)\left(V_0 + V_{fwd} - V_{ce}\right) - r_l I_L\right] R_L C r_c - R_L I_L L\right\} s + R_L\left[(1-D)\left(V_0 + V_{fwd} - V_{ce}\right) - r_l I_L\right]}{(R_L + r_c) C L s^2 + \left\{L + C r_c (R_L + r_c) + R_L (1-D)^2 C r_c\right\} s + r_l + R_L (1-D)^2} \quad (7)$$

Table 1. Converter parameters to evaluate effects of non-ideal behavior.

Circuit Parameter	Ideal Circuit	Non-Ideal Circuit
V_{in}	48 V	48 V
V_0	100 V	100 V
P_0	500 W	500 W
F_{sw}	50 kHz	50 kHz
$\Delta i_{L,pk\text{-}pk}$	$0.2I_{L,av}$	$0.2I_{L,av}$
$\Delta V_{C,pk\text{-}pk}$	$0.02V_0$	$0.02V_0$
V_{ce}	0 V	1.53 V
V_{fwd}	0 V	1.5 V
r_L	0 mΩ	20 mΩ
r_C	0 mΩ	3 mΩ
D	0.52	0.54
L	≥239.616 µH	≥227.457 µH
C	≥26 µF	≥26.994 µF

The variables in (7) are defined as follows: $R_L \rightarrow$ equivalent load resistance; $I_L \rightarrow$ average inductor current; $C \rightarrow$ capacitance; $L \rightarrow$ inductance; $V_0 \rightarrow$ average output voltage; $r_c \rightarrow$ capacitor series resistance; $V_{fwd} \rightarrow$ diode forward voltage; $V_{ce} \rightarrow$ saturation voltage of the active switch; $r_l \rightarrow$ series inductor resistance; $D \rightarrow$ DC quiescent operating point of the duty cycle; $\widetilde{v}_o(s) \rightarrow$ AC variations of the output voltage; and $\widetilde{\delta}(s) \rightarrow$ AC variations of the duty cycle.

2.6. Final Modelling Considerations

To present the proposed modelling scheme with added simplicity, the standardized transfer function in (1) was further refined by considering the numerator and the denominator polynomials independently. The computation of the numerator and the denominator polynomials' coefficients will be explained in separate sections. The study limits the derived transfer functions to those required for voltage-mode control; therefore, for each converter, two models of interest are control-to-output voltage transfer function, and the audio susceptibility transfer function.

3. Proposed Modelling Scheme for the SPDT Group

This section presents rules for computing coefficients of (1), following an example-based approach. For this group of converters, the example converter is that shown in Figure 11. The voltage conversion ratio of this converter is given by (3).

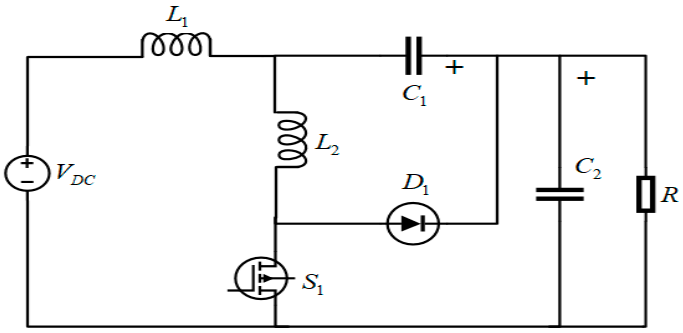

Figure 11. Circuit diagram of one of the converters considered in this study (E1).

3.1. Control-to-Output Voltage Transfer Function

Consider (1) with $G(s) = \left.\frac{\widetilde{v}_o(s)}{\widetilde{\delta}(s)}\right|_{\widetilde{v}_{in}(s)=0}$. In the following sub-sections, the subscript k is used to denote a positive integer introduced through the circuit component numbering scheme alluded to above, and supported by Figure 3. Thus, only two possible values exist for k, i.e., '1' or '2'.

3.2. Numerator Polynomial

Equation (8) is derived from (1)

$$A_m S^m + A_{m-1} S^{m-1} + \cdots + A_0 S^0 \tag{8}$$

1. A_0 is always equal to V_{in} regardless of the converter topology, i.e., $A_0 = V_{in}$;
2. A_1 is given by: $A_1 = \sum I_{L_k} L_k$. Only inductors whose average currents are not equal to the load current comprise A_1. Figure 12 shows the typical connections of inductors that make $A_1 = 0$. The sign of the individual product terms of the sum is positive if the inductor under consideration is charged by a canonical-cell capacitor and feeds power back to the source or to the output port; otherwise, the sign is negative. For this group, this energy exchange is seen when the inductor under consideration shares a node with a capacitor and a diode at one of its terminals; otherwise, the sign is negative;
   - For the circuit in Figure 11, it can be seen that none of the inductors is connected as shown in Figure 12, therefore, the coefficient takes the form of $\pm I_{L_1} L_1 \pm I_{L_2} L_2$. None of the inductors' terminals share a node with a diode and a capacitor. Hence, $A_1 = -I_{L_1} L_1 - I_{L_2} L_2$;
3. A_2 is given by: $A_2 = \sum V_{C_1} C_1 L_k$. A_2 is comprised only of inductors that are not connected directly to the output-port as shown in Figure 12b, where neither of the inductor's terminals is connected to both switches (e.g., Figure 13).The sign of the individual product terms of the sum is positive if, and only if, at any given sub-interval

of the switching period, the inductor and capacitor in the product term are connected in series or parallel when all independent voltage sources are shorted; otherwise, the sign is negative;

- For the circuit in Figure 11, only L_1 conforms to the requirements when V_{DC} is shorted, therefore, the coefficient takes this form: $\pm V_{C_1} C_1 L_1$. L_1 is never connected in series or in parallel with a capacitor at any given sub-interval of the switching period when all independent voltage sources are shorted. Hence, $A_2 = -V_{C_1} C_1 L_1$;

4. A_3 is non-zero if, and only if, at any given sub-interval of the switching period, there is a series connection of one inductor to a parallel combination of another inductor and a capacitor; and neither of the two inductors is in series with the load. This non-zero value is given by: $A_3 = I_{L_{parallel}} L_{parallel} L_{series} C_1$. Figure 14 illustrates graphically how the parallel/series identifiers work. The sign of the term is positive if either of the inductors under consideration shares a node with a capacitor and a diode at one of its terminals; otherwise, the sign is negative;

- For the circuit in Figure 11, such a series-parallel connection exists when the diode D_1 conducts, thus the term is non-zero. L_2 is the inductor in parallel with a capacitor, while L_1 is the inductor in series with the parallel combination, therefore, the coefficient takes the form of $\pm I_{L_2} C_1 L_1 L_2$. None of the inductors' terminals share a node with a diode and a capacitor. Hence, $A_3 = -I_{L_2} C_1 L_1 L_2$;

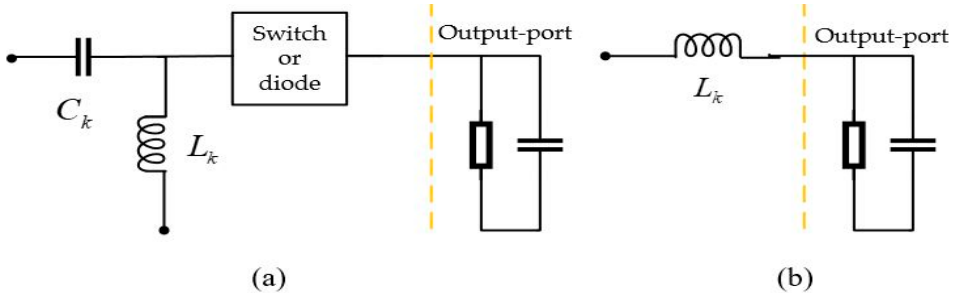

Figure 12. (**a**) First circuit configuration $\boldsymbol{A_1} = 0$, (**b**) second circuit configuration rule for $\boldsymbol{A_1} = 0$.

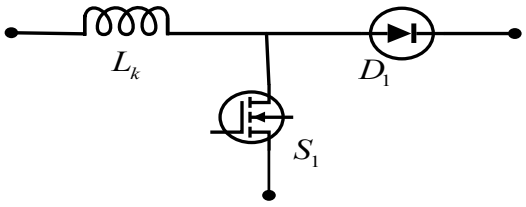

Figure 13. Pictorial representation of double switch connection.

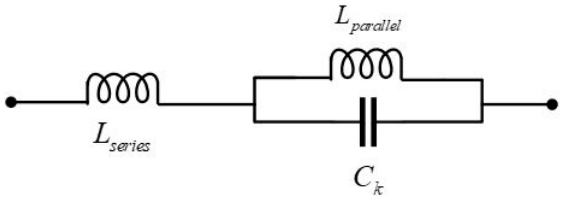

Figure 14. Pictorial representation of the rule for $\boldsymbol{A_3}$.

3.3. Denominator Polynomial

Equation (9) is derived from (1).

$$B_n S^n + B_{n-1} S^{n-1} + \cdots + B_0 S^0 \tag{9}$$

1. All coefficients corresponding to odd powers of 'S' are divided by the load resistance. Moreover, the signs of all the terms in the denominator are positive;
2. In general, B_0 is defined as $B_0 = \{g(D)\}^2$, where the DC voltage conversion ratio, i.e., $\frac{V_o}{V_{in}}$, is represented as a ratio of two functions making its numerator and denominator, i.e., $\frac{V_o}{V_{in}} = \frac{f(D)}{g(D)}$. Thus, for all the converters, irrespective of functionality and order, the value of B_0 is equal to the square of the denominator term of the DC voltage conversion ratio; e.g., $B_0 = (1-D)^2$ for a boost and a buck–boost converter whose DC voltage conversion ratios are given by $\frac{V_o}{V_{in}} = \frac{1}{1-D}$ and $\frac{V_o}{V_{in}} = \frac{D}{1-D}$, respectively, and $B_0 = 1$ for a step-down converter whose DC voltage conversion ratio is given by $\frac{V_o}{V_{in}} = D$;
    - For the circuit in Figure 11, $g(D) = 1 - D$, as can be deduced from (3), therefore, $B_0 = (1-D)^2$;
3. B_1 is a sum of products of the inductances in the circuit and the square of the sum of the conduction times of the semiconductor device(s) to which the inductors are physically connected. For example, if the circuit has an inductor with either of its terminals connected to both switches, then B_1 will have a term in the sum of products with the value given by $L_k t_{L_k}^2 = L_k(D + 1 - D)^2 = L_k$. Figure 15 gives a pictorial description of the relation described above for a range of possible inductor-switch connections. A fourth-order circuit will have two inductors; thus the resultant coefficient will be the sum of the product of an individual inductor with the corresponding squared conduction time, i.e., $B_1' = \sum L_k t_{L_k}^2$, where t_{L_k} represents the conduction time of one switch, or the sum of conduction times of two switches associated with a specified inductor, thus the possible expressions it can assume are: D, $1 - D$ or 1. Since B_1 is a coefficient of an odd power of s, step "1" applies, i.e., $B_1 = B_1'/R = \sum L_k t_{L_k}^2 / R$;
    - For the circuit in Figure 11, L_1 is not connected to any switch, thus, from Figure 15, $t_{L_1} = 1$ and L_2 is connected to both switches, thus, from Figure 15, $t_{L_2} = 1$. Therefore, $B_1 = \frac{1}{R}(L_1 + L_2)$;
4. B_2 is a sum of products of inductances and capacitances in the circuit. These products are such that the output capacitor, i.e., C_2, multiplies with the inductances of the circuit's inductors and their corresponding squared conduction times as described in the preceding step, i.e., if the sum of the product of inductances and squared conduction times in B_1' is given by $\sum L_k t_{L_k}^2$, this then implies that C_2 forms a product term as follows: $C_2\left(\sum L_k t_{L_k}^2\right)$. C_1 only multiplies with inductances whose inductors are never connected in series with the output-port/load at any given sub-interval of the switching period. In addition, the product of C_1 with any of the inductances of inductors, has a non-unity squared conduction time if, and only if, neither the inductor nor the capacitor is connected (as shown in Figure 13 or Figure 16b) to both of the circuit's switches at one or either of its terminals. The conduction time is that of the "absent" switch (where, the "absent" switch is that which is neither connected to the inductor nor the capacitor under consideration). Thus, the resultant expression for B_2 is as follows: $C_2 B_1' + \sum C_1\left(L_k t_{L_k}^2\right)$;
    - For the circuit in Figure 11, both of the inductors meet the criterion, thus C_1 multiplies with both L_1 and L_2. In addition, it can also be seen that $t_{L_2} = 1$, since L_2 is connected to both switches and $t_{L_1} = D$, since neither C_1 nor L_1 is connected to the active switch. Therefore, $B_2 = C_2(L_1 + L_2) + C_1\left(L_1 D^2 + L_2\right)$;
5. B_3 is always given as a product of all the reactive components of the circuit excluding the output-port capacitor. This value is non-zero only for fourth-order converters; it is given as $B_3' = L_1 L_2 C_1$. Since B_3 is a coefficient of an odd power of 's', step "1" applies, i.e., $B_3 = B_3'/R = L_1 L_2 C_1 / R$;

6. B_4 is always given as a product of all the reactive components of the circuit. This value is non-zero only for fourth-order converters; it is given as $B_4 = L_1L_2C_1C_2$.

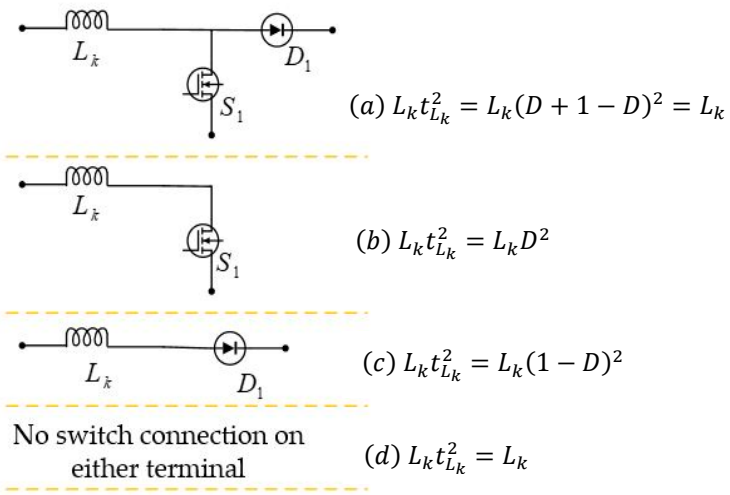

Figure 15. Pictorial representation of the rule for computing coefficient B_1.

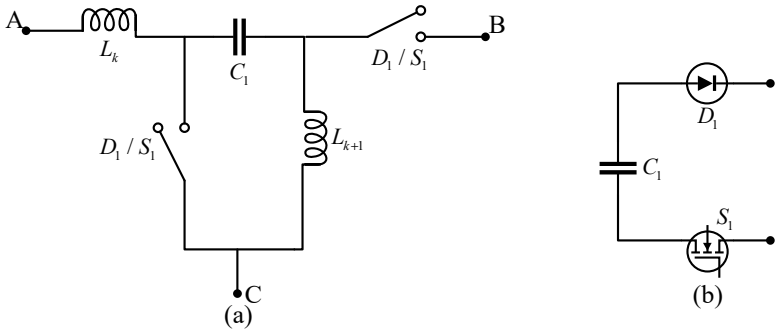

Figure 16. Group G canonical-cell (**a**) and capacitor double switch connection (**b**).

3.4. Audio-Susceptibility

Consider (1) with $G(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)}\Big|_{\tilde{\delta}(s)=0}$.

3.5. Numerator Polynomial

The form of the polynomial in this study is given by (8).

1. In general, $A_0 = f(D) \times g(D)$, where $\frac{V_o}{V_{in}} = \frac{f(D)}{g(D)}$. For example, a step-down converter with $\frac{V_o}{V_{in}} = D$, $A_0 = D \times 1$. The sign for this term is always positive;
   - For the circuit in Figure 11, with reference to (3), it can be seen that $A_0 = 1 \times (1 - D) = 1 - D$;
2. Coefficients to odd powers of s are always equal to zero, i.e., $A_1 = A_3 = 0$;
3. A_2 is given by: $A_2 = \sum C_1 L_k t_{L_k}^2$. C_1 only multiplies with inductances whose inductors are never connected in series with either the load or input-source at any given sub-interval of the switching period. If either the inductor or the capacitor is connected to both switches (as shown in Figure 13 or Figure 16b), t_{L_k} becomes unity, and this is also true when neither the capacitor nor the inductor is connected to a switch. If only one switch is connected to the inductor or the capacitor, the conduction time is that of the "absent" switch (where, the "absent" switch is that which is neither connected to the inductor nor the capacitor under consideration). The sign of this term is positive if, and only if, at any given switching interval, the inductor and capacitor in the product term are connected in series or parallel; otherwise the sign is negative;

- For the circuit in Figure 11, only L_2 meets the criterion, and $t_{L_2} = 1$ since L_2 shares a node with both switches at one of its terminals. Thus, the coefficient is of the form $\pm C_1 L_2$. Since L_2 is connected in parallel with a capacitor when the diode conducts, $A_2 = C_1 L_2$.

3.6. Denominator Polynomial

The denominator for the audio-susceptibility transfer function is always the same as that of the control-to-output voltage transfer function.

4. Proposed Modelling Scheme for the SPST Group

This section presents rules for computing coefficients of (1), following an example-based approach. For this group of converters, the example converter is that shown in Figure 8. The voltage conversion ratio of this converter is given by (6).

4.1. Control-to-Output Voltage Transfer Function

Consider (1) with $G(s) = \left.\frac{\widetilde{v}_o(s)}{\widetilde{\delta}(s)}\right|_{\widetilde{v}_{in}(s)=0}$. In the following sub-sections, the subscript k denotes a positive integer introduced through the circuit component numbering scheme alluded to above and supported by Figure 3. Thus, only two possible values exist for k, i.e., '1' or '2'.

4.2. Numerator Polynomial

The form of the polynomial in this study is given by (8).

1. A_0 is the same as that for the SPDT group, i.e., $A_0 = V_{in}$;
2. A_1 is the same as that for the SPDT group, i.e., $A_1 = \sum I_{L_k} L_k$;
   - For the circuit in Figure 8, L_2 is the only inductor whose average current is not equal to the output current, since average current through C_1 is zero, therefore, the coefficient takes the form of $\pm I_{L_2} L_2$. Since L_2 acquires its energy from a canonical-cell capacitor and drains it to the input port, $A_1 = I_2 L_2$;
3. A_2 is mainly dependent on the output-port current wave-shape as defined by Figures 4–6. If the current is as shown in Figure 4, then A_2 is if of the form: $A_2 = \sum V_{C_1} C_1 L_k$. If the current is as shown in Figure 5, then A_2 is of the form: $A_2 = \sum V_{switch\ block} C_1 L_k$, where $V_{switch\ block}$ is the blocking voltage of the switch connected to the midpoint of an LC circuit as shown in Figure 17. If the current is as shown in Figure 6, then A_2 is given as $A_2 = \frac{\sum V_{C_1} C_1 L_k}{t_{L_k}}$, where t_{L_k} is the conduction time of the switch connected at the midpoint of a capacitor–inductor combination under consideration as shown in Figure 17;

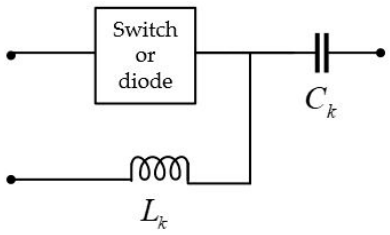

Figure 17. Capacitor–inductor switch/diode tapping equivalent circuit.

NB: These products only consider the inductors, which are not connected in series with the load. The sign of the individual product terms of the sum is always positive, unless involving diode blocking voltages, which are inherently negative.

- For the circuit in Figure 8 both inductors conform to the requirements, therefore, the coefficient takes the form of $A_2 = V_{C_1} C_1 L_1 + V_{C_1} C_1 L_2$;

4. A_3 is non-zero if, and only if, at any given sub-interval of the switching period, there is a series connection of one inductor to a shorted series connection of the other inductor and capacitor; and neither of the two inductors is in series with the load. This non-zero value is equal to the product of the canonical-cell reactive components and the sum of the average inductor currents ($A_3 = \left[I_{L_{series}} + I_{L_{shorted}}\right] L_{series} L_{shorted} C_{shorted}$). Figure 18 graphically illustrates how the series/series-shorted identifiers work. The sign of the term is positive if at least one of the terms in A_1 is positive; otherwise the term is negative;
    - For the circuit in Figure 8, such an inductor–capacitor connection (as shown in Figure 18) exists when the diode conducts, thus the term is non-zero. As seen in Figure 8, the terminals of series connected L_1 and C_1 are shorted, while L_2 is the inductor in series with the shorted combination, therefore, A_3 takes the form of $\pm\left[I_{L_1} + I_{L_2}\right] C_1 L_1 L_2$. Since L_2 is charged by C_1 and feeds power back to the source, $A_3 = \left[I_{L_1} + I_{L_2}\right] C_1 L_1 L_2$.

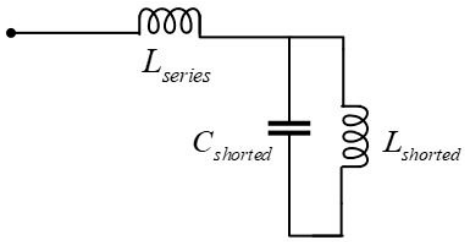

Figure 18. Pictorial representation of the rule for A_3.

4.3. Denominator Polynomial

The form of the polynomial under study is given by (9).

1. All the coefficients corresponding to odd powers of 's' are divided by the load resistance. Moreover, the signs of all the terms in the denominator are positive;
2. This coefficient is the same as that for the SPDT group, i.e., $B_0 = \{g(D)\}^2$, where $\frac{V_o}{V_{in}} = \frac{f(D)}{g(D)}$;
    - For the circuit in Figure 8, this denominator function is D as deduced from (6), therefore, $B_0 = D^2$;
3. B_1 is the same as that of the SPDT group; however, for the SPST group, one inductor might appear to be connected to both switches at its terminals, but only one of the switches is unique to the inductor, with the other switch is connected to both inductors. Only the switch that is unique to a specific inductor is considered when determining the relevant conduction times. For example, in Figure 16a, inductor L_{k+1} appears to have two switches connected to its terminals, but only the switch connected to node "B" of Figure 16a is unique to L_{k+1}, while the switch connected to node "C" is unique to L_k;
    - For the circuit in Figure 8, it can be seen that L_1 is connected to both switches at either terminal, but only the active switch is unique to it, thus $t_{L_1} = D$ and L_2 is only connected to the diode, thus $t_{L_2} = 1 - D$. Therefore, $B_1 = \frac{1}{R}\left(L_1 D^2 + L_2 (1 - D)^2\right)$;
4. B_2 is a sum of products of inductances and capacitances in the circuit. These products are such that the output capacitor, i.e., C_2 in a fourth-order system, multiplies with the inductances of the circuit's inductors and their corresponding squared conduction times as described in the preceding step, i.e., if the sum of the product of inductances and squared conduction times in B_1' is given by $\sum L_k t_{L_k}^2$, this implies that C_2 forms a product term as follows: $C_2\left(\sum L_k t_{L_k}^2\right)$. C_1 only multiplies with inductors that are not connected in series with the load. In addition, the product of C_1 with any

of the inductors includes the square of a switch's conduction time depending on the output-port current wave-shape as follows: If the current coincides with that shown in Figure 4, then t_{L_k} is the type of switch inducing the discontinuity in the current waveform. If the current coincides with that shown in Figure 5, then t_{L_k} is the type of switch not directly connected to the midpoint of the inductor–capacitor combination. If the current coincides with that shown in Figure 6, then t_{L_k} is the sum of the two switches' conduction times, which always sums to unity. Thus, the resultant expression for B_2 is: $C_2B_1' + \sum C_1\left(L_k t_{L_k}^2\right)$;

- From the circuit in Figure 8, both L_1 and L_2 meet the criterion, thus C_1 multiplies with both L_1 and L_2. In addition, $t_{L_1} = t_{L_2} = D$, since the output-port current wave-shape is positive pulsed and the active switch is inducing the pulses (as shown in Figure 4). Thus, $B_2 = C_2\left(L_1D^2 + L_2(1-D)^2\right) + C_1L_1D^2 + C_1L_2D^2$;

5. B_3 is the same as for the SPDT group, i.e., B_3 is always given as: $B_3 = (C_1L_1L_2)/R$;
6. B_4 is the same as for the SPDT group, i.e., B_4 is always given as: $B_4 = C_1C_2\ L_1L_2$.

4.4. Audio-Susceptibility

Consider (1) with $G(s) = \frac{\widetilde{v}_o(s)}{\widetilde{v}_{in}(s)}\Big|_{\widetilde{\delta}(s)=0}$.

4.5. Numerator Polynomial

The form of the polynomial under study is given by (8).

1. A_0 is the same as for the SPDT group, i.e., $A_0 = f(D) \times g(D)$, where $\frac{V_o}{V_{in}} = \frac{f(D)}{g(D)}$;
   - With reference to (6), it can be seen that $A_0 = (2D-1) \times D$;
2. $A_1 = A_3 = 0$, the same as the SPDT group;
3. A_2 is of the form $A_2 = C_1L_kh_k(D)$, where $h_k(D)$ is a function of the switch's conduction times. C_1 only multiplies with inductors that are not connected in series with either the output or input port. The conduction time for the capacitor–inductor term whose inductor is connected to two switches on either of its terminals, is given as the product of the conduction times of all the switches in the circuit, such that no switch is connected to the common rail. If there is a switch connected to the common rail, then the accompanying conduction time is only that of the switch not connected to the common rail. The sign for this term when none of the switches is connected to the rail, is opposite that of the output-port (i.e., if the output is non-inverted, this term is negative, and positive if the output is inverted) while the sign for this term when one of the switches is connected to the common rail follows that of the output-port. The conduction time for the capacitor–inductor term whose inductor is not connected to two switches on either of its terminals is the square of the conduction time of the "absent" switch (where the "absent" switch is that switch which is not connected on either terminal of the inductor under consideration). The sign for this term follows that of the output-port;
   - It can be seen from Figure 8 that both inductors meet the criterion. $h_1(D) = -D(1-D)$ since L_1 is connected to two switches at its terminals with none of the switches connected to the common rail. In addition, the output-port is non-inverted. $h_2(D) = D^2$, since the output port is non-inverted and L_2 is not connected to both switches at either of its terminals, with the active switch being the "absent" switch. Therefore, $A_2 = C_1L_2D^2 - A_2 = C_1L_1D(1-D)$.

4.6. Denominator Polynomial

The denominator for the audio-susceptibility transfer function is always the same as that of the control-to-output voltage transfer function.

5. Further Considerations to Model Entirely by Inspection

Since the canonical-cell capacitor appears in the small signal model, there will be a need to evaluate its numerical value whenever one attempts to analyze system dynamics. The average canonical-cell capacitor voltage can easily be computed from the 'DC-circuit', wherein all inductors are shorted and all semiconductor devices are open. Such a circuit is derived directly from the original circuit diagram. In addition, one need not draw the equivalent circuit since a visual inspection of the original diagram, which treats inductors as shorts and semiconductor devices as open circuit, is sufficient for computing the average voltage of the canonical cell-capacitor in terms of the input and output voltages, or one of them. Figure 19 represents the equivalent circuits for a converter topology, E1 in [26]. It can be seen from the figure that the need for one to draw the equivalent circuit for computing V_{C_1} is immaterial. From Figure 19, it can be seen that the canonical-cell capacitor forms a loop with the input and output voltage such that the average voltage is given by (10).

$$V_{C_1} = V_o - V_{in} \tag{10}$$

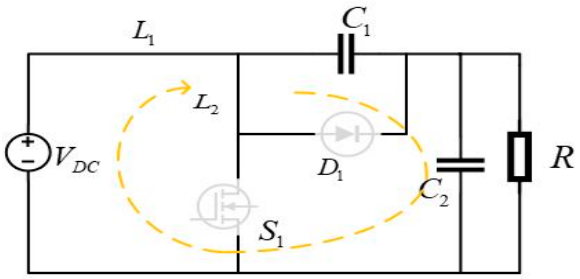

Figure 19. E1 equivalent circuit for computing V_{C_1}.

6. Validation of the Proposed Scheme

6.1. Consistency with Known Models

The initial stage of validating the modelling technique is to gauge the consistency of the models derived using the scheme with known, independently-derived models. For this, PSim's AC sweep function was used to independently compute baseline models for the circuit of interest.

6.1.1. Model of Example Converter (E1)

Equations (11) and (12) show the resultant control-to-output voltage and audio-susceptibility models, respectively, as derived for converter E1 in Section 3.

$$\left.\frac{\widetilde{v}_o(s)}{\widetilde{\delta}(s)}\right|_{\widetilde{v}_{in}(s)=0} = \frac{-I_{L_2}C_1L_1L_2s^3 - V_{C_1}C_1L_1s^2 - I_{L_1}L_1s - I_{L_2}L_2s + V_{in}}{C_1C_2L_1L_2s^4 + \frac{C_1L_1L_2}{R}s^3 + (C_2(L_1+L_2) + C_1L_1D^2 + C_1L_2)s^2 + \frac{L_1+L_2}{R}s + (1-D)^2} \tag{11}$$

$$\left.\frac{\widetilde{v}_o(s)}{\widetilde{v}_{in}(s)}\right|_{\widetilde{\delta}(s)=0} = \frac{C_1L_2s^2 + 1 - D}{C_1C_2L_1L_2s^4 + \frac{C_1L_1L_2}{R}s^3 + (C_2(L_1+L_2) + C_1L_1D^2 + C_1L_2)s^2 + \frac{L_1+L_2}{R}s + (1-D)^2} \tag{12}$$

6.1.2. Comparing the Derived Model with the Baseline Model

MatLab's bode plot function was used to graphically represent (11) and (12). Moreover, PSim was used to independently generate the bode plot for the same converter. For both the PSim and MatLab functions, the bode plots are drawn for the following circuit parameter values: L1 = 0.13 mH, L2 = 0.05 mH, C1 = 10 µF, C2 = 0.13 mF, D = 0.5, R = 2.5 Ω, Vin = 20 V, Vo = 40 V, IL1 = 32 A, IL2 = 32 A, and VC1 = 20 V. Figures 20 and 21 show these results for the control-to-output voltage transfer functions and the audio-susceptibility, respectively, for the converter in Figure 11. The congruency of the two plots in Figures 20 and 21 validates the consistency of the proposed scheme with known modelling techniques.

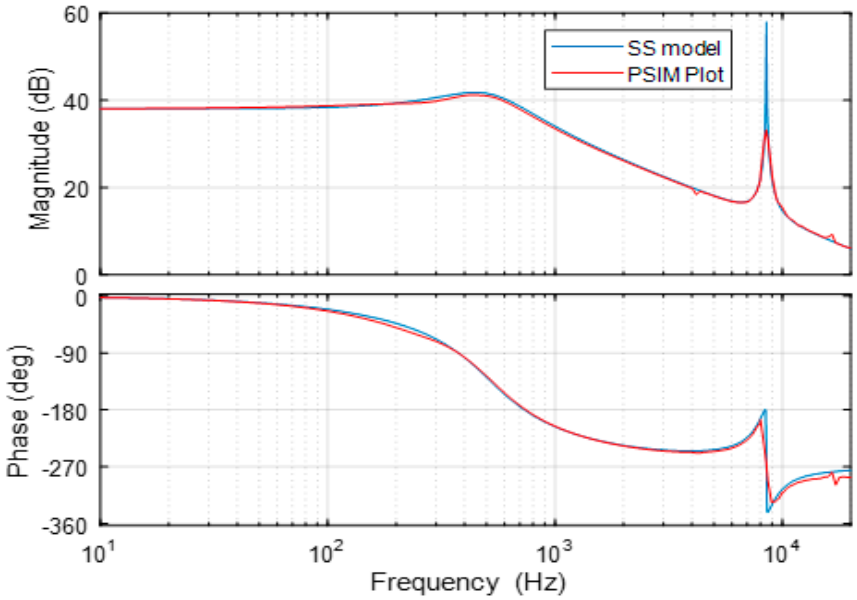

Figure 20. Control-to-output voltage transfer function.

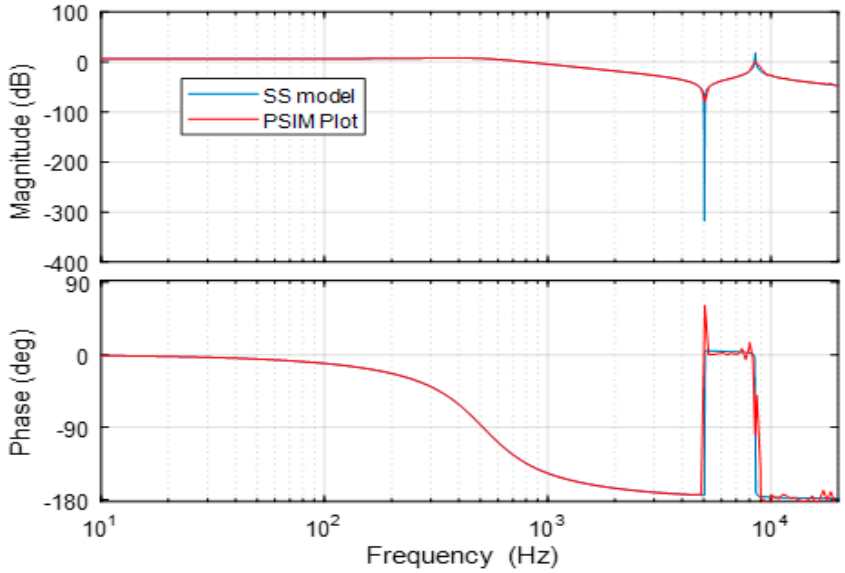

Figure 21. Audio-susceptibility transfer function.

6.2. Proposed Modelling Scheme's Accuracy Verificaiton Capability, Tractibility and Time Requirements

To validate the proposed modelling scheme's capability to easily verify the model accuracy, maintain tractability even for higher-order systems and reduce model computation time, we considered the derivation of the control-to-output voltage small-signal transfer characteristics of the conventional boost converter as an example. The circuit for the boost converter is shown in Figure 7. It can be seen from the figure that it has two reactive components, thus it will result in a model with a second-order characteristic equation. From (1), the value of $n = 2$ and the value of $m = 1$. As such, the coefficients of interest are shown in (13).

$$\frac{\widetilde{v}_o(s)}{\widetilde{\delta}(s)} = \frac{\pm A_1 S^1 + A_0 S^0}{B_2 S^2 + B_1 S^1 + B_0 S^0} \tag{13}$$

The conventional boost converter can be fully described with an SPDT switch, thus the rules presented in Section 3 are applicable.

Numerator coefficients:

- A_0 is always equal to V_{in} regardless of topology;
- A_1 is of the form $\sum I_{L_k} L_k$ and it does not involve connected inductors, as shown in Figure 12. There is only one inductor and it is not connected as shown in Figure 12. As such, $A_1 = -I_{L_1} L_1$. The sign is negative since L_1 does not share a node with a capacitor and a diode.

Denominator coefficients:

- $B_0 = \{g(D)\}^2$ where $\frac{V_o}{V_{in}} = \frac{f(D)}{g(D)}$. For the circuit in Figure 7, this denominator function is $1 - D$ as can be deduced from (5), therefore, $B_0 = (1 - D)^2$;
- B_1 is of the form $\sum L_k t_{L_k}^2 / R$. It can be seen that there is only one inductor, and the conduction time associated with the inductor will be 1 since it is connected to both switches. Thus, $B_1 = L_1 / R$;
- B_2 is of the form $C_2 B_1' + \sum C_1 \left(L_k t_{L_k}^2 \right)$. $C_1 = 0$ since there is no canonical cell capacitor in the boost converter circuit. C_2 is the same as C_1 in Figure 7. Thus, $B_2 = C_1 B_1' = C_1 L_1$.

The resultant model is shown in (14). This model is exactly the same as those derived in [24,26,47] when non-ideal characteristics are ignored.

$$\frac{\widetilde{v}_o(s)}{\widetilde{\delta}(s)} = \frac{-I_{L_1} L_1 s + V_{in}}{C_1 L_1 s^2 + \frac{L_1}{R} s + (1 - D)^2} \tag{14}$$

6.2.1. Accuracy Verification Capability

To verify accuracy of the derived model in (14), currently available tools will be limited to identifying the presence of the RHP zero as indicated by the negative sign in the numerator of (14) and the model order, which ought to coincide with the number of reactive components as indicated in the denominator of (14) and Figure 7. These tools do not definitively validate the accuracy of the model. The proposed modelling scheme's coefficient-based derivation closes this gap. This is because the form and sign of each coefficient is completely defined in the scheme. Moreover, this accuracy verification capability of the proposed modelling scheme may be used even if the model in (14) was derived using a different modelling technique such as state-space, circuit averaging or switching flow graphs.

6.2.2. Tractability and Time Requirements

To assess if tractability is maintained even for higher-order systems when using the proposed modelling technique, consider the derivation procedure as outlined in Sections 3 and 4. The procedure does not involve the averaging and linearization steps which are explicitly carried out in all the currently available techniques. The effects of averaging and linearization are only listed as limitations of the modelling procedure. As such, the absence of these steps and the standardized model expression maintains tractability for any model order. Moreover, the omission of the averaging and linearization steps in the modelling procedure substantially reduces model computation time since these steps constitute the two main operations in the modelling procedure. Once these steps have been carried out, the remaining task is simple manipulation of algebraic equations.

6.3. Proposed Modelling Technique's Unifying Capabilities

According to the converter synthesis technique presented in [26], converters in Figures 7 and 11 are synthesized from different converter cells. This means that there is no immediate or known kinship between them, and any analysis carried out on either converter cell cannot be readily used for the other converter cell. As such, the converter cell can be used as a discriminant in modelling these converters. The difference in their order has also been used a discriminant when analyzing these converters [26]. Moreover, converter functionality has also been used as a discriminant in computing models for these converters [33]. The proposed modelling scheme nullifies all these discriminants. This can

be seen in the derivation of models for a fourth-order converter (E1) and a second-order converter (A2) as indicated in Sections 3 and 6.2.

7. Discussion

It is of great importance to note that even for the rules provided as unique for a specified group, i.e., Sections 3 and 4, the uniqueness of the coefficients is not absolute. There is a strong correlation between the individual rules. For example, consider the denominator coefficient B_2, the rule describing how the output-port capacitor forms product terms with the inductances of the circuit's inductors is the same for both groups. In addition, the rule describing how the product terms of the canonical-cell capacitor and the inductors depend on the connection of the inductors to the output-port, is also similar. It is interesting to notice that the only distinguishing feature is the influence of the circuit's switches in determining corresponding conduction times. Lastly, considering A_2 for the audio-susceptibility numerator polynomial, the disregard of inductors connected in series either with the input or output port, is also similar for both groups. It is again the switch's conduction times which bring uniqueness. Thus, the total number of rules to learn in order to apply the proposed modelling scheme is substantially reduced.

It is also important to note that the transfer characteristics derived using the proposed modelling scheme have the same limitations as those derived using existing averaged modelling schemes such as state-space averaging or injected current, i.e., the proposed scheme also ignores the inherent switching action of the converters resulting in limited accuracy. Additionally, small perturbation assumption still persists. The main advantages of this scheme are in retaining tractability even with higher order converters, nullifying the importance of the converter cell in unifying or showing kinship among converter families, and substantially reducing modelling time in addition to providing accuracy verification capabilities, even for existing modelling schemes. This means that even when existing modelling schemes are used, the proposed modelling scheme may be used solely for verifying accuracy as long as the transfer characteristics are represented in the form of (1). Table 2 gives a direct comparison of popular existing modelling schemes (state-space, circuit averaging, switching flow graphs) with the proposed modelling scheme. The use of the proposed modelling scheme is currently limited to transfer characteristics necessary for voltage-mode control, but since the characteristic equation is the same even for current mode transfer characteristics and output impedance, the modelling scheme may be used to verify stability even for current mode control.

Table 2. Comparison of the proposed modelling technique with existing techniques.

Attribute	Existing Techniques	Proposed Technique
Time requirements	Involves numerous labor-intensive steps which include averaging, linearization and equation manipulation.	At most, the scheme requires two simple inductor voltage equations. The standard form does not require further manipulations.
Accuracy verification capability	Insufficient	Sufficient
Modelling tractability	Not guaranteed for higher order topologies.	Guaranteed

8. Conclusions

The study focuses on addressing issues pertinent to model time requirements and model accuracy verification when computing small-signal models for two switch, non-isolated DC–DC converters. The study presented a small-signal modelling scheme whose operation is based on a generalized transfer function expression and a set of predefined rules. These rules relate the nature of each coefficient in the generalized model, to the

converter's circuit diagram. The simplicity of the rules not only makes possible the derivation of small-signal models by inspection, it also substantially reduces the overall required modelling time. Moreover, the proposed modelling scheme's in-built mechanism to definitively verify model accuracy remains unmatched when compared with existing modelling schemes, which makes it more attractive, as it always guarantees accuracy. The major limitation in the proposed model is in neglecting component non-linearity, which is shown to have minimal effect on the resultant model, unless the purpose of the design is solely on the effects of non-linearity in the system.

Author Contributions: Conceptualization, L.M.; methodology, L.M.; software, L.M.; validation, L.M., M.N.G. and G.P.A.; formal analysis, L.M.; investigation, L.M. and M.N.G.; data curation, M.N.G. and G.P.A.; writing—original draft preparation, L.M.; writing—review and editing, L.M., M.N.G. and G.P.A.; visualization, L.M., M.N.G. and G.P.A.; supervision, M.N.G.; project administration, M.N.G. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: All generated data is contained in the manuscript.

Acknowledgments: The authors would like to thank the National Research Foundation (NRF) for their support during the course of the research.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

References

1. Alhamrouni, I.; Hanis, W.I.; Salem, M.; Albatsh, F.M.; Ismail, B. Application of DC–DC converter for E.V battery charger using PWM technique and hybrid resonant. In Proceedings of the 2016 IEEE International Conference on Power and Energy (PECon), Melaka, Malaysia, 28–29 November 2016; pp. 133–138.
2. Zhang, S.; Li, B.; Cheng, D.; Zhao, X.; Li, G.; Wang, W.; Xu, D.G. A Monopolar Symmetrical Hybrid Cascaded DC/DC Converter for HVDC Interconnections. *IEEE Trans. Power Electron.* **2021**, *36*, 248–262.
3. Sreekumar, A.; Jiji, K.S. A Survey of DC–DC Converters for Fuel Cell Electric Vehicle Applications. In Proceedings of the 2021 2nd International Conference for Emerging Technology (INCET), Belagavi, India, 21–23 May 2021; pp. 1–5.
4. Li, B.; Liu, J.; Wang, Z.; Zhang, S.; Xu, D. Modular High-Power DC–DC Converter for MVDC Renewable Energy Collection Systems. *IEEE Trans. Ind. Electron.* **2021**, *68*, 5875–5886. [CrossRef]
5. Li, L.; Li, B.; Wang, Z.; Yang, M.; Xu, D. Monopolar Symmetrical DC–DC Converter for All DC Offshore Wind Farms. *IEEE Trans. Power Electron.* **2022**, *37*, 4275–4287.
6. Birca-Galateanu, S. Multiple-loop control of DC–DC converters. In Proceedings of the Signals, Circuits and Systems, 2003. SCS 2003. International Symposium on, Iasi, Romania, 10–11 July 2003; Volume 1, pp. 93–96.
7. Lekić, A.; Stipanović, D. Stable switching control of DC–DC converters. In Proceedings of the 2017 25th Telecommunication Forum (TELFOR), Belgrade, Serbia, 21–22 November 2017; pp. 1–7.
8. Hejri, M.; Giua, A. Hybrid modeling and control of switching DC–DC converters via MLD systems. In Proceedings of the 2011 IEEE International Conference on Automation Science and Engineering, Trieste, Italy, 24–27 August 2011; pp. 714–719.
9. Wu, H.H.; Huang, C.H.; Wei, C.L. Investigation and modeling of startup techniques for boost DC–DC converters. In Proceedings of the 19th International Conference on Electrical Machines and Systems (ICEMS), Chiba, Japan, 13–16 November 2016; pp. 1–4.
10. De Pegado, R.A.; Gomes, R.C.M.; Alves, L.F.S.; Vitorino, M.A.; Rodriguez, Y.P.M.; Filho, A.V.M.L. High-frequency switch modeling technique applied to DC–DC converters simulation. In Proceedings of the 2017 Brazilian Power Electronics Conference (COBEP), Juiz de Fora, Brazil, 19–22 November 2017; pp. 1–6.
11. Dong, P.; Cheng, K.W.E.; Kwok, K.W.; Ho, S.L.; Lu, Y.; Yang, J.M. Singular perturbation modelling technique and analysis for class-E DC–DC converter using piezoelectric transformer. *IET Power Electron.* **2008**, *1*, 518–526. [CrossRef]
12. Liao, L.-C.; Chien, K.-W.; Tseng, B. Switching Flow-Graph Modeling Technique for DC–DC Cuk Converters. In Proceedings of the 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, Finland, 26–28 August 2014; pp. 1–10.
13. Li, X.; Ruan, X.; Jin, Q.; Sha, M.; Tse, C.K. Small-Signal Models with Extended Frequency Range for DC–DC Converters with Large Modulation Ripple Amplitude. *IEEE Trans. Power Electron.* **2018**, *33*, 8151–8163. [CrossRef]
14. Cuk, S. Modelling, Analysis and Design of Switching Converters. Ph.D. Thesis, California Institute of Technology, Pasadena, CA, USA, November 1976.
15. Wester, G.W. Low-Frequency Characterization of Switched DC–DC Converters. Ph.D. Thesis, California Institute of Technology, Pasadena, CA, USA, May 1972.

16. Luo, F.L.; Ye, H. Small Signal Analysis of Energy Factor and Mathematical Modeling for Power DC–DC Converters. *IEEE Trans. Power Electron.* **2007**, *22*, 69–79. [CrossRef]
17. Reatti, A.; Corti, F.; Tesi, A.; Torlai, A.; Kazimierczuk, M.K. Effect of Parasitic Components on Dynamic Performance of Power Stages of DC–DC PWM Buck and Boost Converters in CCM. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 26–29 May 2019; pp. 1–5.
18. Wu, J.; Li, X.; Li, X.; Xu, G. Modeling of Non-ideal Buck Converter and Design of Compensation Network. In Proceedings of the IEEE 5th Information Technology, Networking, Electronic and Automation Control Conference (ITNEC), Xi'an, China, 15–17 October 2021; pp. 429–435.
19. Faifer, M.; Piegari, L.; Rossi, M.; Toscani, S. An Average Model of DC–DC Step-Up Converter Considering Switching Losses and Parasitic Elements. *Energies* **2021**, *14*, 7780.
20. Vu, T.A.; Nam, D.P.; Huong, P.T.V. Analysis and control design of transformerless high gain, high efficient buck-boost DC–DC converters. In Proceedings of the 2016 IEEE International Conference on Sustainable Energy Technologies (ICSET), Hanoi, Vietnam, 14–16 November 2016; pp. 72–77.
21. Jie, Z.; Haibin, L.; Rui, X. Research of DC circuit breaker applied on Zhoushan multi-terminal VSC-HVDC project. In Proceedings of the 2016 IEEE PES Asia-Pacific, (APPEEC), Xi'an, China, 25–28 October 2016; pp. 1636–1640.
22. Middlebrook, R.D.; Cuk, S. A general unified approach to modelling switching-converter power stages. In Proceedings of the IEEE Power Electronics Specialists Conference, Cleveland, OH, USA, 8–10 June 1976; pp. 18–34.
23. Chetty, P.R.K. Modelling and analysis of cuk converter using current injected equivalent circuit approach. *IEEE Trans. Ind. Electron.* **1983**, *IE-30*, 56–59. [CrossRef]
24. Wester, G.W.; Middlebrook, R.D. Low-Frequency Characterization of Switched DC–DC Converters. *IEEE Trans. Aerosp. Electron. Syst.* **1973**, *AES-9*, 376–385. [CrossRef]
25. Smedley, K.; Cuk, S. Switching Flow-Graph nonlinear modeling technique. *IEEE Trans. Power Electron.* **1994**, *9*, 405–413. [CrossRef]
26. Tymerski, R.; Vorperian, V. Generation, classification and analysis of Switched-Mode DC-to-DC Converters by the Use of Converter Cells. In Proceedings of the Telecommunications Energy Conference, Toronto, ON, Canada, 19–22 October 1986; pp. 181–195.
27. Yue, X.; Wang, X.; Blaabjerg, F. Review of Small-Signal Modeling Methods Including Frequency-Coupling Dynamics of Power Converters. *IEEE Trans. Power Electron.* **2019**, *34*, 3313–3328.
28. Verma, K.; Gupta, A. A modeling and control functions of grid connected converter for solar photovoltaic system—A review. In Proceedings of the 2016 7th India International Conference on Power Electronics (IICPE), Patiala, India, 17–19 November 2016; pp. 1–6.
29. Padhee, S.; Pati, U.C.; Mahapatra, K. Modelling switched mode DC–DC converter using system identification techniques: A review. In Proceedings of the 2016 IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS), Bhopal, India, 5–6 March 2016; pp. 1–6.
30. Sanders, S.R.; Verghese, G.C. Synthesis of averaged circuit models for switched power converters. *IEEE Trans. Circuits Syst.* **1991**, *38*, 905–915. [CrossRef]
31. Lee, Y.S. A Systematic and Unified Approach to Modeling Switches in Switch-Mode Power Supplies. *IEEE Trans. Ind. Electron.* **1985**, *IE-32*, 445–448. [CrossRef]
32. Francés, A.; Asensi, R.; García, Ó.; Prieto, R.; Uceda, J. Modeling Electronic Power Converters in Smart DC Microgrids—An Overview. *IEEE Trans. Smart Grid* **2018**, *9*, 6274–6287. [CrossRef]
33. Veerachary, M. Analysis of Fourth-Order DC–DC Converters: A Flow Graph Approach. *IEEE Trans. Ind. Electron.* **2008**, *55*, 133–141. [CrossRef]
34. Hasanpour, S.; Baghramian, A.; Mojallali, H. Reduced-order small signal modelling of high-order high step up converters with clamp circuit and voltage multiplier cell. *IET Power Electron.* **2019**, *12*, 3539–3554. [CrossRef]
35. Santos de Carvalho, M.R.; Bradaschia, F.; Rodrigues Limongi, L.; de Souza Azevedo, G.M. Modeling and Control Design of the Symmetrical Interleaved Coupled-Inductor-Based Boost DC–DC Converter with Clamp Circuits. *Energies* **2019**, *12*, 3432. [CrossRef]
36. Zhu, B.; Zeng, Q.; Vilathgamuwa, M.; Li, Y.; Chen, Y. A Generic Control-Oriented Model Order Reduction Approach for High Step-Up DC/DC Converters Based on Voltage Multiplier. *Energies* **2019**, *12*, 1971. [CrossRef]
37. Padhi, B.K.; Padhy, S.N.; Bhuyan, K.C. Controller design for reduced order model of SEPIC converter. In Proceedings of the International Conference on Signal Processing, Communication, Power and Embedded System (SCOPES), Paralakhemundi, India, 3–5 October 2016; pp. 1533–1538.
38. Yao, J.; Li, K.; Zheng, K.; Abramovitz, A. A unified modeling approach to Tapped Inductor Converters Accounting for the Leakage Inductance Effects. *IEEE Trans. Power Electron.* **2022**, in press.
39. Das, M.; Agarwal, V. Generalized Small Signal Modeling of Coupled-Inductor-Based High-Gain High-Efficiency DC–DC Converters. *IEEE Trans. Ind. Appl.* **2017**, *53*, 2257–2270. [CrossRef]
40. Pietkiewicz, A.; Tollik, D. Unified Topological Modeling Method of Switching DC–DC Converters in Duty-Ratio Programmed Mode. *IEEE Trans. Power Electron.* **1987**, *PE-2*, 218–226.
41. Abramovitz, A.; Yao, J.; Smedley, K. Unified Modeling of PWM Converters with Regular or Tapped Inductors Using TIS-SFG Approach. *IEEE Trans. Power Electron.* **2016**, *31*, 1702–1716. [CrossRef]

42. Rico, M.; Uceda, J.; Sebastian, J.; Aldana, F. Static and dynamic modeling of tapped-inductor dc-to-dc converters. In Proceedings of the 1987 IEEE Power Electronics Specialists Conference, Blacksburg VA, USA, 21–26 June 1987; pp. 281–288.
43. Garg, M.M.; Hote, Y.V.; Pathak, M.K. Notes on Small Signal Analysis of Energy Factor and Mathematical Modeling for Power DC–DC Converters. *IEEE Trans. Power Electron.* **2014**, *29*, 3848. [CrossRef]
44. Yang, G.; Zhang, Z. Unified large signal modeling method for DC–DC converters in DCM. In Proceedings of the 7th International Power Electronics and Motion Control Conference, Harbin, China, 2–5 June 2012; Volume 3, pp. 1561–1565.
45. Liu, Y.-F.; Sen, P.C. A general unified large signal model for current programmed DC-to-DC converters. *IEEE Trans. Power Electron.* **1994**, *9*, 414–424.
46. Nirgude, G.; Tirumala, R.; Mohan, N. A new, large-signal average model for single-switch DC–DC converters operating in both CCM and DCM. In Proceedings of the IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230), Vancouver, BC, Canada, 17–21 June 2001; Volume 3, pp. 1736–1741.
47. Vorperian, V. Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode. *IEEE Trans. Aerosp. Electron. Syst.* **1990**, *26*, 490–496. [CrossRef]
48. Al-Baidhani, H.; Kazimierczuk, M.K.; Ordóñez, R. Nonlinear Modelling and Control of PWM DC–DC Buck-Boost Converter for CCM. In Proceedings of the 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, USA, 21–23 October 2018; pp. 1374–1379.
49. Zheng, X.; Ali, H.; Wu, X.; Zaman, H.; Khan, S. Non-Linear Behavioral Modeling for DC–DC Converters and Dynamic Analysis of Distributed Energy Systems. *Energies* **2017**, *10*, 63. [CrossRef]