PERFORMANCE EVALUATION AND CONTROL OF AN MMC ACTIVE RECTIFIER WITH HALF-BRIDGE AND FULL-BRIDGE SUBMODULES FOR HVDC APPLICATIONS

by

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Submitted in partial fulfilment of the requirements for the degree
Master of Engineering (Electrical Engineering)

in the

Department of Electrical, Electronic and Computer Engineering
Faculty of Engineering, Built Environment and Information Technology

UNIVERSITY OF PRETORIA

July 2021

SUMMARY

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Keywords: active rectifier, full bridge submodule, half bridge submodule, high voltage direct current converter, modular multilevel converter, modular multilevel rectifier, power electronic transformer, smart transformer, solid state transformer.

The modular multilevel active rectifier was designed and evaluated, whereby the half bridge and the full bridge DC-DC converters as its submodules for the high voltage direct current transmission were compared. It was found that, by taking advantage of the unipolar modulation scheme in the full bridge converter, the switching losses in the two converters are equal when they are both operated in the linear modulation region. Furthermore, operating the full bridge converter in the overmodulation region does not give it a pronounced advantage over the half bridge converter. The conduction losses in the full bridge converter are two times higher than those in the half bridge converter, due to double the number of semiconductor devices. However, using the half bridge converter in the high voltage direct current modular multilevel converter requires an expensive DC-side breaker, while use of the full bridge converter eliminates the need for such a breaker due to the

intrinsic DC-side fault current blocking capability. The clear choice between the two requires industry cost data.

A design methodology for the submodule capacitor average voltage loop controllers for phase-shifted carrier modulated modular multilevel converters was carried out from first principles. The methodology enables design of such controllers to be carried out in a step by step and straightforward manner without resorting to simulation or guesswork.

A simple but effective submodule capacitor sizing method was proposed. The resulting submodule capacitor size was shown to be smaller than those resulting from other sizing methods proposed in the literature while achieving the submodule capacitor voltage ripple specifications.

A robust DC bus voltage controller design for modular multilevel rectifiers was presented, whereby a design method for multilevel voltage source converters with DC link capacitors was adopted for modular multilevel rectifiers. Since the modular multilevel converters for HVDC application are designed without the DC-link capacitor to mitigate the effects of a possible DC-side fault current, the submodule capacitors in the modular multilevel converter acted as an equivalent DC link capacitor to accomplish the design.

LIST OF ABBREVIATIONS

AC	alternating current
CB	circuit breaker
CCSC	circulating current suppression controller
CSC	current source converter
DC	direct current
EMF	electromotive force
FACTS	flexible alternating current transmission system
FB	full bridge
FID	fault isolation device
FREEDM	future renewable electric energy delivery and management
HB	half bridge
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LFT	line frequency transformer
MMC	modular multilevel converter
PET	power electronic transformer
PWM	pulse-width modulation
SiC	silicon carbide
SM	submodule
STATCOM	static synchronous compensator
SST	solid state transformer
ST	smart transformer
THD	total harmonic distortion

VSC	voltage source converter
WBG	wide band gap

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CHAPTER 1 INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Context of the problem

For transmitting electrical power over long distances, the high voltage direct current (HVDC) lines have been shown to be more efficient than the high voltage alternating current (HVAC) lines for distances of above 500-800 km for overhead lines and for distances of above 50 km for underground cables [1]. The modern HVDC transmission lines are based on voltage source converters (VSCs) since they allow power flow reversal without reversing the terminal voltage polarity, unlike the current source converters (CSVs) [2]. However, the VSC-HVDC systems are vulnerable to DC-side fault currents for two major reasons. First, the lines usually do not have any current filters which would otherwise attenuate the fault current [3]. Second, the antiparallel diodes in the semiconductor switches in the VSCs give a free pathway to the DC-side fault current [4].

The proposed solutions to the DC-side fault current are either to have DC circuit breakers on the lines, similar to those used in the AC lines but designed to specifically cater for the DC line requirements [5], or to develop VSCs capable of blocking the DC-side fault current [6]. Due to the nature of the DC transmission, the DC circuit breakers tend to be expensive and bulky which limits the economic viability of the HVDC lines and tend to not meet the space and weight requirements of areas such as offshore windfarms [7].

The VSCs for HVDC applications can be roughly put into two categories: those that are based on the half bridge (HB) converter and those that are based on the full bridge (FB)

converter. The HB-based converters are claimed to be more efficient (hence more economically viable) since they have fewer semiconductor devices, but they lack the intrinsic capability to block the DC-side fault current. On the other hand, the FB-based VSCs have the inherent ability to block the DC-side fault current but are claimed to be less efficient due to their higher count of semiconductor devices. However, their intrinsic capabilities to block the DC-side fault current promise elimination of the bulky DC breakers from the HVDC lines [8], [9].

In most studies the evaluation of the modular multilevel converter (MMC) for various applications is done using an inverter. Although the MMC rectifier and inverter share a lot in terms of current control, the DC bus voltage control and evaluation in the rectifier has been side-lined for the most part. MMC evaluation in rectifier mode helps to identify issues that are peculiar to the MMC rectifier.

1.1.2 Research gap

The comparison between the HB and the FB converters as SMs of the MMC for use in HVDC networks is unclear. The comparison must consider not only the difference in efficiency but also all the advantages and disadvantages that each converter brings at a system level. Also, an approach to efficiency comparison needs to be carried out beyond the comparison based on the number of semiconductor switches per submodule only, considering factors such as the switching frequency.

The controller design methodology for SM capacitor voltage balancing in phase-shifted carrier modulated MMCs is not elaborate, whereby design of parameters of such controllers depends on simulation or the parameters are quoted to remain the same as suggested by the original literature that proposed the control structure. For optimal control, the SM capacitor voltage balancing loops must be mathematically modelled so that controllers can be designed to compensate the models accordingly.

SM capacitors play a significant role in the cost and physical size of the MMC. The SM capacitors must be optimally designed to keep the cost and size down.

MMC performance evaluation is usually carried out using an inverter. Although the MMC rectifier shares the current control with the MMC inverter, the DC bus voltage control is unique to the rectifier. Evaluation of the MMC in rectifier mode unmasks research opportunities that are unique to the rectifier mode.

1.2 RESEARCH OBJECTIVE AND QUESTIONS

The first objective of this research is to establish the better candidate between the HB and the FB for the HVDC transmission. The comparisons done in the literature do not fully consider all the features of the FB SM. Where the features of the FB SM are considered, they are not put into context to verify if they help the FB SM outperform the HB SM. Apart from DC-side fault blocking capability, the extra features of the FB SM are its ability to be operated at half the switching frequency as that of the HB SM but produce an output waveform of the same effective switching frequency and its ability to be operated in the overmodulation region. The areas of comparison are efficiency, DC-side fault current blocking capability, and the implied cost. Since temporary faults lead only to temporary power outages, converters with fault ride-through capabilities should be able to mitigate them. On the other hand, blocking a permanent DC-side fault may need more than just control-based fault ride-through capabilities.

The second objective is to develop an elaborate controller design methodology for SM capacitor voltage balancing. The main power controller design and modulation for the MMC are straightforward. However, the controller design for the SM capacitor voltage balancing in phase-shifted modulated MMCs is not elaborate, as the controllers are often obtained through intensive simulation or produced without an explanation of how they were obtained.

The third objective aims to achieve a SM capacitor design methodology that results in an optimum capacitor size. SM capacitors contribute significantly to the cost and size of the

converter station. The existing SM capacitor sizing methods in literature, however, do not result into similar capacitor values and are usually an overdesign.

The fourth objective is to evaluate the performance of the MMC in a rectifier mode. The MMC rectifier is usually side-lined in the literature. Evaluation of the MMC performance in rectifier mode unveils the research areas that are unique to the MMC rectifier.

The research questions to be answered are:

- Which is the more suitable DC-DC converter, between the HB and the FB, for use as a SM in HVDC systems MMCs, based on DC-side fault handling capability, efficiency, and cost?
- Can an elaborate and step by step controller design methodology for MMC SM capacitor voltage balancing be established?
- To reduce size and cost of the MMC stations, can an optimum SM capacitor size be achieved?
- Are there research areas unique to the MMC rectifier that are overlooked in the literature?

1.3 APPROACH

The HB-SM and the FB-SM will be compared through analysis and simulations. Expected results will be shown through analysis, which will be confirmed by computer simulations of an MMC rectifier using PSIM software.

A mathematical model for SM capacitor voltage balancing control loops, specifically the average voltage balancing loop, will be derived from first principles, and the resulting Bode plots for a specified system extracted. Controllers will be designed based on these Bode plots and their effectiveness verified through simulation of an MMC rectifier using PSIM software.

A SM capacitor design method will be derived through analysis and the resulting SM capacitor size compared to the SM capacitor sizes out of existing sizing methods, for the same operating conditions. The effectiveness of the resulting capacitor size will be verified through simulation of an MMC rectifier using PSIM software, whereby the resulting SM capacitor ripple voltage must be within a specified value.

By analyzing the simulation results, especially the characteristics of the resulting DC bus voltage of the MMC rectifier, research areas that are specific to the MMC rectifier will be identified.

1.4 RESEARCH GOALS

This research aims at a conclusive comparison of the HB-SM and FB-SM for use in the HVDC MMCs; an elaborate controller design methodology for the SM capacitor voltage control loops for phase-shifted carrier MMCs; an optimum SM capacitor sizing method; and to unveil research areas that are specific to the MMC rectifier.

1.5 RESEARCH CONTRIBUTION

- Detailed evaluation the HB and the FB converters for use in MMCs in HVDC systems based on efficiency, DC-side fault current blocking capability, and cost.
- An elaborate controller design methodology for SM capacitor voltage balancing.
- A simple and straightforward SM capacitor sizing method that results to minimized SM capacitors.
- Identification of research areas specific to the MMC rectifier and a robust MMC rectifier DC bus voltage control method. The research issues identified will be explored in future work.

1.6 RESEARCH OUTPUTS

- A.J. Mbogela and M.N. Gitau, "Control and performance evaluation of the active MMC rectifier with half bridge and full bridge submodules for HVDC application", *IET Power Electronics*, in preparation, July 2021.
- A.J. Mbogela and M.N. Gitau, "An optimal submodule capacitor sizing method for modular multilevel converters for HVDC application", *IEEE Transactions on Power Electronics*, under review, July 2021.

1.7 OVERVIEW OF STUDY

In Chapter 2 a literature study was performed. It was found that the comparison between the half bridge and the full bridge DC-DC converters as candidates for the HVDC-MMC is not clear. There are areas where the half bridge converter has clear advantages over the full bridge converter, and vice versa, as well as some overlapping areas, such as switching losses and component ratings, which need a thorough comparison. It was also found that the controller design for the submodule capacitor voltage balancing loops of phase-shifted carrier modulated MMCs is not well elaborated in the literature, and that the design of such controllers depends on simulation and guesswork combined with fine tuning.

In Chapter 3 the modeling of the MMC was carried out. The model describing the basic operation of the converter was first considered, then the current control, the DC bus voltage control, and the SM capacitor average voltage control (leg average voltage control) models were presented. The leg average voltage control model is part of the contribution of this dissertation.

In Chapter 4 the analysis of the modular multilevel converter with half bridge or full bridge submodules was carried out. The device ratings and the loss analyses were carried out. As expected, it was found that the conduction losses in the FB-MMC are twice as much as those in the HB-MMC. The switching losses, however, were found to be equal. The ohmic losses

in the arm inductors were also found to be equal. In the overmodulation region the FB-MMC processed even higher conduction and ohmic losses while the switching losses could not be predicted.

In Chapter 5 the design of the modular multilevel converter is carried out. The SM capacitor and the arm inductor were sized. A new capacitor sizing method that results into a smaller capacitor size than other methods in the literature was proposed.

In Chapter 6 the control of the MMC was designed. Simulation was used to verify the adapted DC bus control model and the SM capacitor average voltage control model developed in Chapter 3. The robustness of the models and controllers were tested by applying step changes of around 13%.

In Chapter 7 the simulation results were presented. It was found that the HB-MMC and the FB-MMC had minimal differences in the simulated quantities. Although the FB-MMC was operated at half the switching frequency as that of the HB-MMC, the DC bus voltage ripple was at the same frequency as that of the HB-MMC. The SM capacitor voltage ripple, out of the proposed SM capacitor design method, was found to meet the SM capacitor voltage ripple specifications, hence justifying the design method. The conduction losses in the FB-MMC were found to be twice those in the HB-MMC, while the switching losses were found to be equal. In the overmodulation region the FB-MMC processed even higher conduction losses but lower switching losses. Overall, it processed 1.2 times higher losses in the overmodulation region than in the linear modulation region. It was also found that the switches (as well as the diodes) in a SM, for a given power flow direction, do not carry the same amount of current. Also, if a switch carries more current in a given power flow direction, the antiparallel diode carries more current in the other power flow direction (rectifier versus inverter). On average, however, the amounts of current carried by the devices agree with the analysis in Chapter 4, which is the reason the power losses also agree with the analysis. It was demonstrated that although the FB-MMC processes higher losses than the HB-MMC, it has the advantage of the ability to block the DC-side fault current. It was also demonstrated that operating the FB-MMC in the overmodulation region does not

favour it against the HB-MMC. It was further demonstrated that the HB and the FB SMs could be used together in an HVDC-MMC, whereby the FB SMs are used only in the final rectifier stage of the PET, the stage that interfaces the DC bus, while the rest of the stages are constructed using the HB-MMC (the PET may be used to interconnect AC and DC systems. When that happens, there would be at least two rectification stages. The first rectification stage is rectifying the AC voltage before it goes through an inverter then through a high frequency transformer. Then it goes through rectification again to interface the DC bus. All other stages can be built with HB SMs, but the last stage that interfaces the HVDC line must have protection against DC-side faults). That way both the superior efficiency the HB SMs and the fault blocking capability of the FB SMs are harnessed. It was also demonstrated that the DC bus voltage ripple needs to be incorporated in sizing of the SM capacitor, which may require the switching frequency harmonic analysis of the MMC rectifier to find out how the DC bus voltage ripple is related to the SM capacitor size.

In Chapter 8 some concluding remarks were drawn.

CHAPTER 2 LITERATURE STUDY

2.1 CHAPTER OBJECTIVES

This chapter intends to provide background knowledge on the MMC, its modulation and control, the application of the MMC in the HVDC systems in form of a power electronic transformer (PET), an overview comparison between the half bridge (HB) and the full bridge (FB) converters as submodules for the HVDC-MMC, and an overview of the HVDC protection.

2.2 THE MODULAR MULTILEVEL CONVERTER

Multilevel converters show good output wave quality, less common mode noise, and high efficiency [10], [11]. With the modular architecture, multilevel converters excel at high voltage and high power applications, whereby higher voltage and higher power units are constructed from lower voltage and lower power submodules [12]. A converter of such architecture is called a modular multilevel converter (MMC). MMCs operate at relatively low switching frequencies and bear relatively high copper efficiency. They are also easy to construct and are easily scalable due to their modularity [8], [13].

The MMC can be either single phase or multiphase, usually three phases. The MMC is made up of phase legs. In turn, each phase leg is made up of two arms: the *upper* arm and the *lower* arm. Each arm is made up of several submodules [12]. A submodule is a converter in its own right and it can be a two-level or a multilevel converter [14]. The basic submodules are the half bridge and the full bridge converters, illustrated in Figure 2.1. A single leg of an MMC is shown in Figure 2.2 (it can also be interpreted as a single phase MMC). A multiphase

MMC is constructed by connecting an appropriate number of such legs in parallel on the DC side. L_{grid} is the sum of the estimated grid equivalent inductance and the isolation transformer leakage inductance. L_{filter} is connected to minimize the arm inductance value, which should overall reduce the total inductance used in the converter design [15].

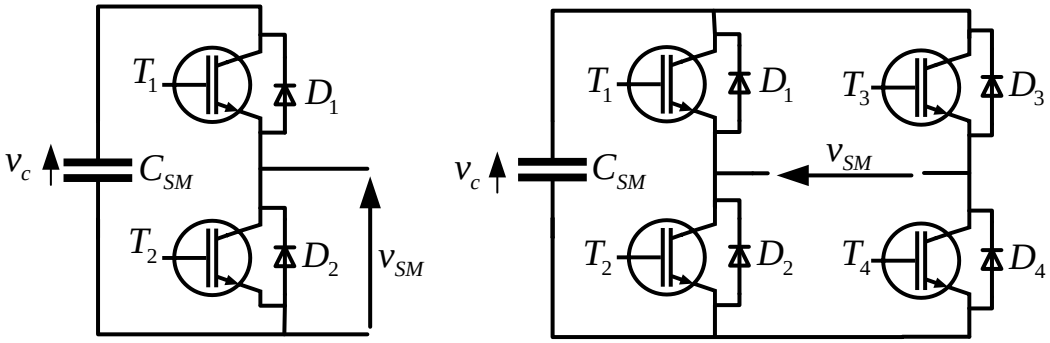

Figure 2.1. The half-bridge (left) and the full-bridge (right) submodules.

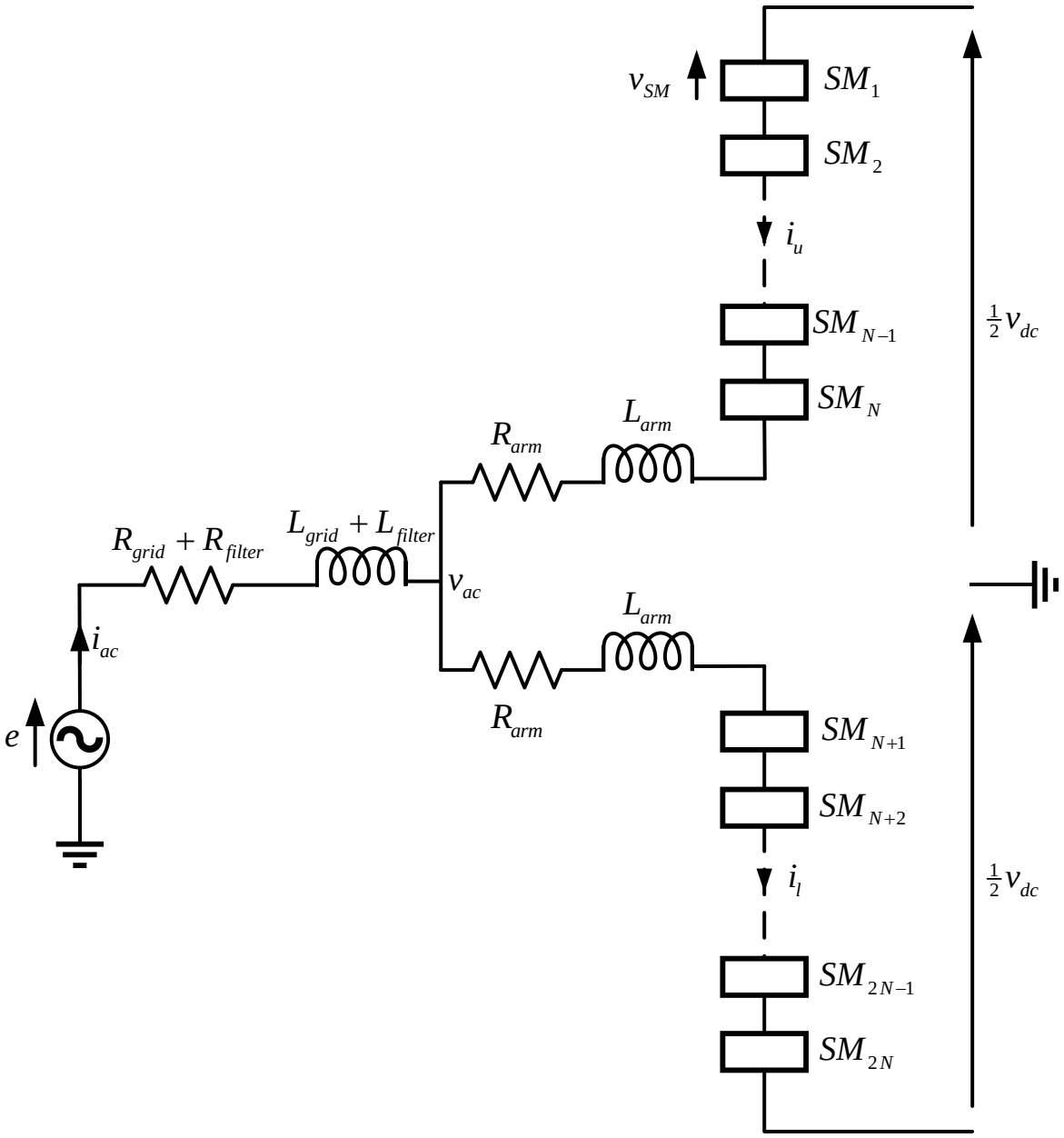

Figure 2.2. A leg of an MMC.

2.3 THE MMC MODULATION AND CONTROL

Generally, the modulation aims to achieve one or more of these objectives, depending on the application: to minimize the harmonic distortion of the output waveform; to minimize the switching losses, the cooling system, and the filter sizes; to maximize the input voltage

utilization; to attain voltage balance among the floating (SM) capacitors; and equal sharing of power and power losses among SMs [16].

Generally, the modulation schemes are classified according to how the switching pulses are obtained: pulse width modulation (PWM) e.g. space vector modulation (SVM) and selective harmonic elimination (SHE), pseudo-modulation e.g. square wave or staircase modulation, and closed loop control methods with implicit modulator e.g. hysteresis current control and finite-states model-predictive control (FS-MPC) [16]. The PWM schemes are further categorized into fundamental frequency (50 Hz or 60 Hz) switching modulations such as SHE and nearest level modulation (NLM); low frequency (< 2 kHz) switching schemes such as the sampled averaged modulation (SAM) and SVM; and high frequency (> 2 kHz) switching schemes such as level-shifted carrier (LSC) modulation and phase-shifted carrier (PSC) modulation [17].

For multilevel converters, PSC and different variations of LSC [18] are used, especially at high frequencies where they result into natural SM capacitor voltage balance. When they are used at low frequencies to minimize switching losses, the main control loop must be used in conjunction with a dedicated SM capacitor voltage balancing control loop [19].

2.3.1 Modulation of the HB-MMC

Among the various modulation schemes, PSC is the most suitable for MMC with fewer levels because it is easier to implement in a microcontroller, and the phase shift required between the contiguous carriers must not be highly accurate for a low number of SMs [20], [21]. PSC also results in an even loss distribution among the SMs [21], [22]. For an MMC with N SMs per arm, N carriers per arm are needed and are shifted from each other by $2\pi/N$ rad, which is done to eliminate the high frequency harmonic component in the arm current [23].

In PSC, the top arm and lower arm SM carriers are shifted from each other by π/N rad if N is even and by 0 if N is odd [24]. This allows for independent modulation of the upper and

the lower arm SMs and is referred to as the $2N + 1$ scheme, as it results to $2N + 1$ AC-side voltage levels. Furthermore, in this scheme the inserted number of SMs in the leg is not constant [25]. Its counterpart is the $N + 1$ scheme, which is achieved by modulating the upper and the lower arms in a complimentary manner, i.e., the upper and lower arm carriers are shifted from each other by π rad [24]. The $2N + 1$ scheme results into a lower total harmonic distortion (THD) of the AC-side voltage, owing to its higher number of levels which also means that the voltage steps are smaller [26]. It however results into higher SM capacitor voltage imbalances [25], which consequently leads to higher arm voltage imbalances, and in turn lead to higher circulating currents and SM capacitor voltage ripple. Furthermore, the eliminated harmonics from the AC-side voltage appear on the DC side [24]. The $N + 1$ scheme ensures that a constant number of SMs is inserted across the leg, resulting to more balanced SM capacitor voltages, hence lower SM capacitor voltage ripple and circulating currents [25]. It however leads to a relatively higher AC-side voltage THD, as its number of levels is almost half of that of the $2N + 1$ scheme [24], [26]. With the $N + 1$ scheme, the AC-side voltage has an effective switching frequency of $N \times f_{sw}$ while with the $2N + 1$ scheme the effective switching frequency is $2N \times f_{sw}$, which has an influence on the size of the AC-side filter — if a filter is installed at all [22], [26]. In a leg, the modulation signals for the lower and for the upper arms are shifted from each other by π rad. This applies to both the $2N + 1$ and the $N + 1$ schemes.

2.3.2 Modulation of the FB-MMC

There are mainly two ways the FB-SM can be modulated. Although they both depend on a unipolar switching scheme, they have different performances.

The first method effectively utilizes only three switches during normal operation, while all switches come into play during blocking state [27]. During normal operation switches T_1 and T_4 are gated so that a positive capacitor voltage is inserted. To bypass the capacitor voltage, either switches T_1 and T_3 or T_2 and T_4 are turned on simultaneously (see Figure 2.1). To balance off voltage and current stress among switches, the bypassing may alternately utilize upper and bottom switches on a cycle-by-cycle basis. Even then, switches T_2 and T_3

would be operated only half the time switches T_1 and T_4 would be. In fact, if bypassing were to utilize only the bottom switches, switch T_3 and its antiparallel diode would be idle all the time during normal operation of the MMC converter. Thus, this scheme has a poor utilization of semiconductor devices. In addition, the semiconductor devices operate at the same frequency as those in a HB do. The only advantage it brings over the HB-SM is that it can block a DC-side fault current.

The second scheme requires two different modulating signals for the left and right arms [28], as in Fig 2.3. This scheme automatically balances the voltage and current stress among the semiconductor devices and effectively doubles the switching frequency. This means that the switches can be operated at half the switching frequency in the HB-SM for the same effective switching frequency. This should significantly reduce the switching losses.

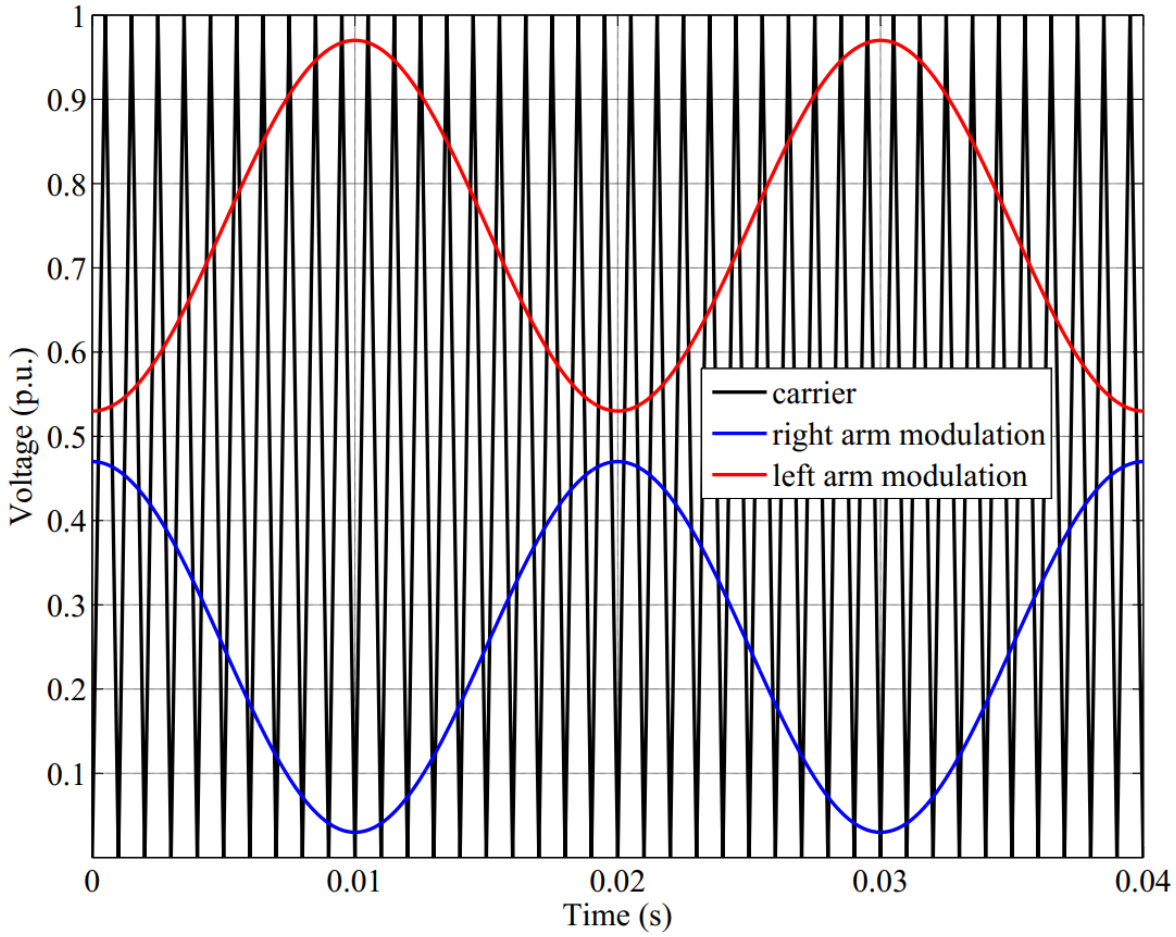

Figure 2.3. A unipolar switching scheme for independent modulation of the left and the right arms of the FB-SM. The top signal modulates the left arm while the bottom signal modulates the right arm.

2.3.3 Submodule capacitor balancing control

Apart from the main power control achieved through the current and the DC bus voltage controllers, SM capacitor voltage balancing control is necessary for the working of the MMC. If the modulation scheme or the conditions of operation do not guarantee self-balancing of the SM capacitor voltages an auxiliary control loop must be added to the main control loop to balance the SM capacitor voltages.

The two common SM capacitor voltage balancing methods are the capacitor voltage sorting [12], [29], which is especially used in converters with a high number of SMs, and the

classical, decentralized closed loop control, which adjusts each SM modulation signal accordingly [30 - 32]. The classical closed loop control is used only with the PSC modulation scheme, and has better controllability if the switching frequency is high enough [17]. Although the sorting method is suited for high number of SMs, the computational burden associated with the sorting process increases with an increasing number of SMs, calling for more efficient sorting algorithms [33]. On the other hand, the decentralized closed loop control method does not have an elaborate method in the literature of determining the controller gains, as the associated transfer functions have not been derived. The pioneering literature on the decentralized closed loop control method admits to the difficulties of establishing these constants and promises to address it in a separate publication [30], which to the date of publication of this dissertation, to the best knowledge of the author, such a publication does not exist yet. The constants have been quoted to remain the same in some studies, regardless of the varying operating conditions, while other studies claim to have obtained them through simulations [22], [34].

The classical SM capacitor voltage balancing control aims to achieve the following objectives, as originally described and illustrated in [31] and [32]:

(i) *Individual SM capacitor voltage balancing*, whereby each SM capacitor voltage follows the reference voltage given by V_{dc}/N.
(ii) *Arm voltage balancing*, whereby the average voltages across the two arms in the leg are forced to follow each other so that there is minimal discrepancy between them.
(iii) *Leg average voltage balancing (averaging)*, whereby the average voltage across the leg is forced to equal the DC bus voltage.

The control aims at reducing the circulating current, especially the second order harmonic, which is the most significant among all the harmonics. The other harmonics are small and can be ignored, depending on the application.

The circulating current can be thought to result from any one or more of the following: an imbalance between the average voltages across the two arms in a leg; an imbalance between any two legs; an imbalance between a leg and the DC bus [35].

The various control loops that may be used in combination to achieve capacitor voltage balancing and to suppress the circulating current are described and illustrated below.

2.3.3.1 Individual SM capacitor voltage balancing loop

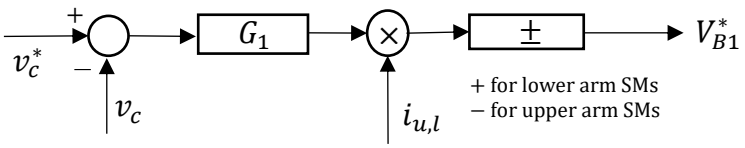

Figure 2.4. Individual SM capacitor voltage balancing. Adapted from [31], © 2011 IEEE.

In Figure 2.4, v_c^* is the reference voltage given by V_{dc}/N, v_C is the sensed capacitor voltage of the SM in question, G_1 is the controller, $i_{u,l}$ is the arm current (upper arm current for upper SMs and lower arm current for lower arm SMs), and V_{B1}^* is the reference control voltage generated by this loop that goes into the modulation of the particular SM capacitor voltage.

2.3.3.2 Arm voltage balancing loop

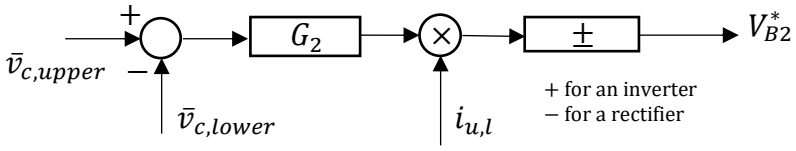

Figure 2.5. Arm voltage balancing. Adapted from [31], © 2011 IEEE .

As explained previously, this controller (see Figure 2.5) forces the average of the lower SM capacitor voltages to follow the average of the upper SM capacitor voltages, so that the voltages across the two arms in a leg are balanced. Thus, $\bar{v}_{C,upper}$ is the average of the upper SM capacitor voltages while $\bar{v}_{C,lower}$ is the average of the lower SM capacitor voltages.

2.3.3.3 Leg average voltage balancing (averaging) loop

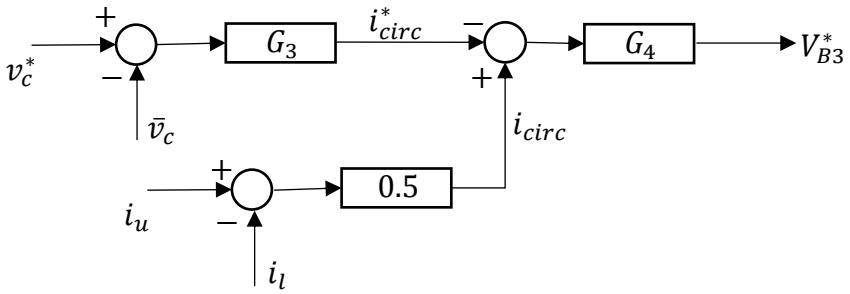

Figure 2.6. Average voltage balancing. Adapted from [31], © 2011 IEEE.

The outer voltage loop sets a reference for the inner loop to follow. In this controller (see Figure 2.6) $\bar{v}_C$ is the average of all SM capacitor voltages in the leg, i_u and i_l are the upper and lower arm currents, respectively. The outer loop shares the reference v_c^* with the individual voltage balancing loop of Figure 2.4, since the required average of all the SM capacitor voltages in the leg equals the required voltage for a single SM capacitor.

2.3.4 Circulating Current Suppression Controller (CCSC)

Ideally, the leg average voltage controller should regulate the circulating current such that the power processing frequencies (DC and the fundamental frequency) are amplified while the harmonics are suppressed. Nevertheless, for suppression of the harmonics, a dedicated separate controller can be implemented for better results. Such a controller is a Quasi Proportional Resonant (QPR) controller, illustrated in Figure 2.7. It is preferred in application over the proportional resonant (PR) controller for better digital realization and noise rejection. The QPR controller allows targeting specific frequencies, with a bandwidth ω_c around such a frequency. The narrow bandwidth allows only those frequencies of interest to be controlled. Such frequencies, whose components are to be suppressed, are the harmonics ω_0, $2\omega_0$, $4\omega_0$, $6\omega_0$, …, $n\omega_0$. The harmonics beyond the n^{th} order are considered insignificant. The reference to this controller is set to 0 [36].

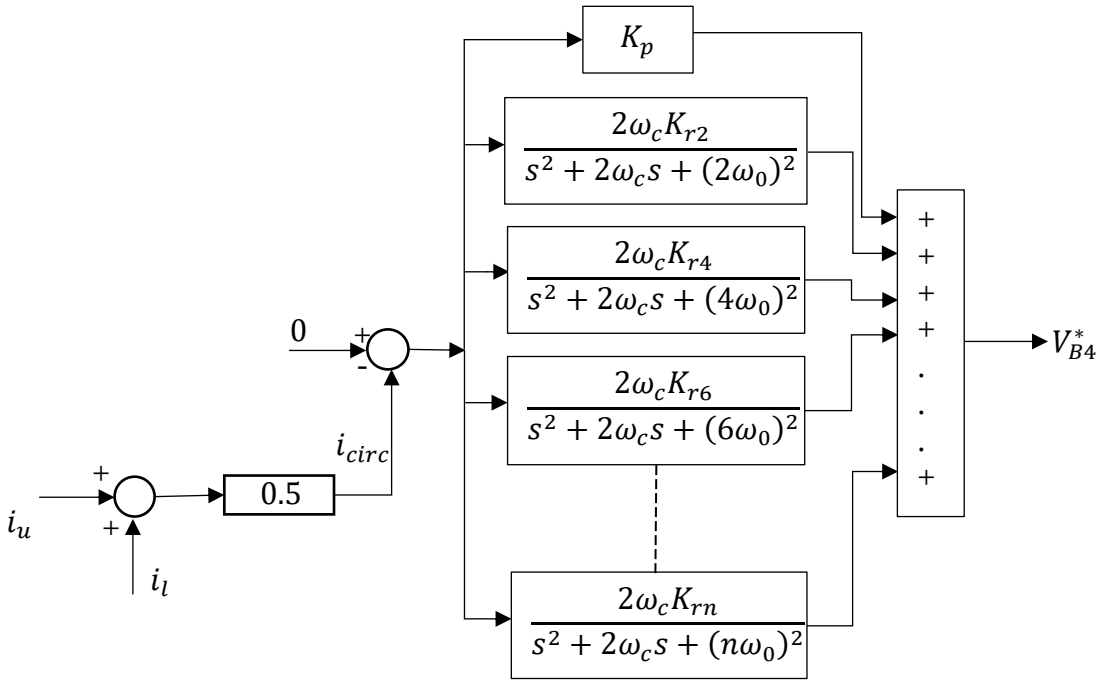

Figure 2.7. Circulating Current Suppression Controller (CCSC). Adapted from [36], © 2012 IEEE.

2.4 THE MMC IN HVDC SYSTEMS AND THE HVDC PROTECTION OVERVIEW

Before addressing the challenge of HVDC protection and how the MMC architecture fits in, it is important to address the concept of the PET and how it utilizes the MMC architecture.

2.4.1 The Power Electronic Transformer and its role in HVDC protection

The main reason the alternating current (AC) power transmission and distribution system has been widely adopted compared to the direct current (DC) counterpart is the voltage transformation ease and convenience brought about by the line frequency transformer (LFT) used in the AC systems [37]. In the LFT, the output voltage directly follows the input voltage and the input current directly follows the output current. With this behaviour, a fault that occurs on either side of the transformer directly affects the other side [38], [39]. Adoption of the DC transmission system would require AC-DC, DC-DC and DC-AC converters that can handle high voltage levels in order to reduce copper losses in the long-distance transmission conductors. For many years, however, the semiconductor technology for such

high voltages has been immature. With the maturing of the semiconductor technology, DC transmission systems, known as the HVDC systems, are slowly replacing AC counterparts for long-distance transmission. Even better, the so called multiterminal HVDC systems bring about flexibility by interconnecting asynchronous AC systems and DC systems of different voltage levels. The distance above which the HVDC transmission systems are more economical than their AC counterparts is above 500-800 km for overhead lines and about 50 km for marine cables [1].

The major challenge in HVDC systems is the DC-side fault detection and isolation. Since a DC voltage signal does not have a zero-crossing, circuit breakers would need to operate at high voltages, which is uneconomical [6]. Research is ongoing to design and manufacture economical circuit breakers to use in HVDC systems. The other alternative is to use transformerless MMCs with fault blocking capability SMs. However, such converters do not galvanically isolate the input and the output sides, which would make other systems connected to the converter, such as the battery energy storage system (BESS), vulnerable [40].

The LFT equivalent for the DC systems is essentially a galvanically isolated DC-DC converter, called the power electronic transformer (PET), also called the solid-state transformer (SST) or simply the smart transformer (ST). It is constituted of several stages, including rectification, inversion, and galvanic isolation. The voltage transformation through switching action and the galvanic isolation prevent direct communication of the input and the output side voltage and current signals [41]. If there is a fault on the output side, the transformer simply reduces the output voltage, with the effect that the input side voltage is maintained and can service other lines [37]. Instead of transforming voltage at the line frequency, the PET does so in the medium frequency range, which reduces the physical footprint and the magnetic material requirement [42], [43]. Using the wide bandgap (WBG) semiconductor devices, General Electric (GE) has been reported to develop a PET prototype that is only 30% in weight of the equally rated LFT, with the volume being 50% of the equivalent dry-type LFT [44]. The size reduction that was achieved is in line with what has

been reported in the literature [45]. The limiting factor for the switching frequency of the PET are the switching losses.

The PET has its weaknesses and strengths against the LFT. When the PET was conceptualized, it would not even be prototyped at relevant power and voltage levels mostly because of the cost, especially that of the semiconductors required for its construction. The limited topologies available with which to design the PET also did not allow scaling up of power and voltage as these topologies subjected semiconductors to relatively higher voltage and current stress levels, [46], [47]; something modern topologies such as multilevel converters can fairly mitigate [10], [48]. But the same cannot be said of the cost of the PET today since the cost of semiconductors has dropped significantly. By the generally accepted Moore's law, the price of semiconductors is expected to continue decreasing with time, pushing the price of PET even further down. Also, once the PET is widely accepted, its cost will be expected to go further down due to the mass-manufacturing effect [42]. Furthermore, the construction cost of the PET is competitive because of the operation at relatively higher frequencies, which in turn demands smaller volume of magnetic materials.

Generally, due to the relatively more complex nature of the PET, it is viewed as far less reliable than the LFT. But the architecture of the PET has a significant implication on the reliability of the PET. If it is constructed based on the modular multilevel converters, the PET will have redundant switching states that would allow bypassing failed submodules. The failed submodules can be reported by the PET for maintenance since measurements and sensing are part of the normal operation of the PET. The measurements can also be used to predict the probability of failure of the components. This information can be used to plan interventions before the failure happens. All this significantly improves the reliability of the PET [37].

In terms of efficiency, the PET, which for a long time has been based on the silicon (Si) semiconductors, has been reported to bear a lower efficiency than that of the LFT [45], [47]. However, with the introduction of WBG devices, the PET stands to achieve efficiencies comfortably above 98% as the WBG device technology continues to improve [44], [49].

Non-linear loads inject a significant amount of current harmonics into the transformer. This has a significant effect on the efficiency of the LFT since the primary side current traces the secondary side current. If the LFT is replaced by the PET, the effect of the non-linear loads on the efficiency of the transformer would be minimal since the input side current does not reflect the output side current. In terms of power quality and protection, this means that the primary side is isolated from the secondary side [50], [51].

Since PETs adjust voltage through switching, their transformation ratio is continuously variable within a given range, unlike in the LFTs whereby this ratio is fixed by the transformer windings. This means that the PETs do not require any mechanical tap-changers, unlike the LFTs. The tap-changing functionality is instantaneously achieved through switching [42], [46], [47].

Apart from voltage transformation, the PET helps to improve the general system power quality. An example is the handling of non-linear loads as alluded to above. Furthermore, since the PET is integrated with active rectifiers, it helps to improve the system's power factor. Also, the PET handles unbalanced loads better than the LFT, in the same way it handles distortions and non-linear loads [51].

Thus, the PET has an edge over the LFT in terms of weight and volume, with its efficiency closely matching that of the LFT, especially if the newer more efficient and more capable semiconductor devices known as the WBG semiconductor devices are considered [44], [49], [52]. However, although a conclusive research on the cost comparison of the PET and LFT has not been published yet, projections do favour the LFT when the comparison is based on isolated units, that is, the PET and the LFT compared without considering the impact of each at a system level [52]. If the projections are based on a system-level comparison, it is well understood that the PET would eliminate the need of many expensive components/functions such as reactive power support (e.g. flexible AC transmission system (FACTS) devices such as the static synchronous compensator (STATCOM) and the static volt-ampere reactive compensator (SVC), to mention a few) [42]. The reason is that the modern PET is based on voltage source converters (VSC), let alone the fact that it is actively controlled, as all other

systems based on power electronics usually are. VSCs enable grid power reversal without reversing the voltage polarity [2], which greatly enhances the controllability of the grid [53]. Equally important, the PET stands to eliminate the bulky and expensive DC-side circuit breaker (CB), if the PET is enabled with the DC-side blocking capability [4], [54]. All this would give the PET a pronounced advantage over the LFT.

If the PET uses the MMC architecture, it has the potential to incorporate distributed sources such as solar and wind electricity generators. This is because its high power-density makes it able to accommodate many inputs in a confined space. Its flexible control makes the PET able to manage distributed sources, distributed storage units, and AC-DC interconnections. Due to its bidirectional power supply, the PET enables energy exchange between the grid and the storage units [39], [55], [56]. This is an advantage of the PET over the LFT.

There is a substantial literature on the adoption of the PET in low and medium voltages, especially in the smart grid area. The future renewable electric energy delivery and management (FREEDM) system, developed by a consortium of universities in the US, is being developed to use the PET together with fault isolation devices (FIDs) in the distribution system [57]. However, FIDs are conceptual devices in research and development. The FID prototypes that have been tested have been shown to be power inefficient hence uneconomical. Also, they cannot be extended to high voltage use as their voltage and current handling capabilities are limited [58].

2.4.2 Overview of the HB and the FB converters as submodules for HVDC-PET-MMC

The DC-side fault isolation and blocking in HVDC systems is an important research topic. The MMC submodules with fault-blocking capability such as the FB and its family have for a long time been deemed lossier than the conventionally used HB-SM [9]. However, new literature on the subject suggest that the FB may not be that less power efficient compared to the HB, especially if one considers that FB devices are operated at half the switching frequency in the HB counterpart for the same effective switching frequency (due to the

unipolar switching scheme), and are subject to lower blocking voltages if the converter is operated in the overmodulation region [59], [60]. This reduces the switching losses in the FB semiconductor devices as these losses are directly proportional to the device switching frequency and the blocking voltage [61]. Also, SMs capable of inserting a negative voltage like the FB-SM have been reported to reduce the SM capacitor ripple [59], [62], driving down the arm circulating currents which drives the system losses further down. Also, the DC-side fault blocking capability of the FB promises elimination of the expensive and bulky DC-CB [4]. All these premises call for a thorough comparison between the HB-based SMs and their FB-based counterparts. In the meantime, new research has been published proposing a control method that enables HB-based MMCs to ride through DC-side faults much like FB-based MMCs, eliminating the need to block the converter during a DC-side temporary fault [54]. However, the nature of the HB-SM does not allow it to block DC-side permanent fault currents. Nevertheless, it has raised the competitiveness of the HB-SM, making the comparison more interesting and probably much more important than before.

2.4.3 The feasibility of the Power Electronic Transformer for fault isolation in an HVDC system

Although the focus of this research is not exactly on protection, one of the required important features of the HVDC transmission line is the ability to protect the system against the DC-side fault currents. Thus, a short overview of the methods proposed/developed for this purpose would be helpful to paint a picture of the state-of-the-art HVDC protection and the influence of the PET and the choice of SM on protection.

The voltage source converter HVDC (VSC-HVDC) systems are, by design, vulnerable to faults [3]. This is because, unlike the line-commutated converter HVDC (LCC-HVDC) counterpart, they do not have any DC inductors to limit a fault current. This means that some faults in VSC-HVDC would not be necessarily perceived as faults in LCC-HVDC. Due to low line inductance the current rises rapidly and the maximum it can rise to is only 2 p.u., due to converter limitations [3], [38], [57], [63]. Another important difference between LCC and VSC is that in VSC the diodes antiparallel to the switches keep feeding the fault current

even after the switches are blocked [4]. The speed at which the fault current rises and the maximum to which it can get imposes a demand for fast fault detection and location methods, and fast-acting circuit breakers. Another requirement is due to the reason that a DC current does not have a zero-crossing. This requires the circuit breaker to be able to dissipate all the energy it absorbs during breaking [64]. Put another way, the circuit breaker must be able to drive the current to zero before breaking. AC breakers meet none of these requirements. They also shut down the entire system, even for single line to ground faults in which the system could continue operating on one pole using the ground as the return path [3].

Some of the VSC-HVDC fault detection and location methods are briefly described below:

a) Current differential protection: A selective protection method where current is measured at both ends of a line using relays [65]. The relays communicate data to each other. They then calculate the current difference between the two ends. If the difference exceeds a given threshold for a set amount of time, a fault is registered. However, it needs a communication link and data processing, which in turn brings about transmission and processing delays, as well as reliability concerns since its reliability depends on the reliability of the telecommunication infrastructure [66].

b) Cable directional protection: An alternative to the current differential protection where only the direction of the fault current is communicated to the other relay. The trip commands are based on the comparison of the directions. Since only the sign of the current is communicated, the method is more robust. It, however, suffers from the same drawbacks as the current differential [67].

c) Overcurrent and Undervoltage: Since faults are characterized by overcurrent and undervoltage, either of the two can be used to detect a fault. Only local measurements are used, eliminating the need for a communication link. This method cannot distinguish between faults internal and external to the converter, thus, it lacks selectivity. However, techniques exist that can relate local measurements to the distance of the fault [68 - 70], although the accuracy of the model affects their precision [6].

d) Travelling-wave-based techniques: These methods analyze the current and voltage wavefronts propagating from the fault location to the line-ends, according to the travelling wave theory on transmission lines. Since the waves travel at speeds close to that of light, these techniques are fast although several successive wavefronts must be measured in order to draw a conclusion on the presence of a fault. Their shortcoming comes when the transmission lines cover a long distance as the wave magnitudes significantly deteriorate [71].

e) Voltage and current derivatives: Similar to the overcurrent/undervoltage method but derivatives of current and voltage are used rather than the magnitudes. This renders them faster. But they are affected by the line distance and the line/converter impedance. The latter affects the selectivity of this method. In particular, methods based on voltage/current derivatives may fail to distinguish between internal and external faults [71 - 73].

f) Wavelet transform: A signal processing technique based on time-scale (not time or frequency domain but simultaneously both) is applied to the travelling wave signals [4], [74]. It works by detecting abrupt changes such as the transients associated with a fault current, and it can discriminate between fault signal-components and non-fault transients. However, it must be combined with other fault-detection methods for accurate results.

g) Hand-shaking method: This method is used to ensure selectivity in multiterminal HVDC (MT-HVDC) systems. Each station converter constantly monitors current in all branches emanating from it. When a fault-level current is recorded, the converter opens a breaker on the line with the highest current away from the converter [4]. This means some lines without a fault will be opened. Even though the healthy lines are reconnected after a reclose process, the momentary isolation of healthy lines is a significant drawback of this method. Furthermore, the method assumes that fast DC switches are available. The DC switches cannot break the fault current, only can isolate the faulty lines after all the AC breakers associated with the converter trip [3]. It is, however, worthy noting that DC switches are more economical than DC breakers [75]. Furthermore, the method is slow and does not satisfy the reliability requirements [76].

h) Converter arm currents: This method aims at protecting the converter. It measures the arm currents of the station modular multilevel converter (MMC) and blocks the converter if the value exceeds a threshold value. However, it cannot locate the fault [6].

i) Inductive fault current limiters: Inductors are connected at the station terminals to increase the fault impedance, which slows down the rate of rising of the fault current hence giving time for slow breakers to act. However, the inductors add to the cost, weight and power losses [6].

j) Artificial-Intelligence-based methods: These methods depend on algorithms that are trained with massive fault data so that they can take appropriate action in the future. However, they need enormous data for the fault scenarios used in training to be comprehensive. They are also complex to develop and have to be adapted to different converter architectures such as two-level, three-level, etc. [4], [76].

Some of the technologies and methods used to block faults and isolate faulty lines are briefly described below:

1) HVDC system protection with AC devices: Instead of breakers acting on the DC side, they act on the AC side of the grid. AC protection devices are less expensive than DC counterparts, they have a shorter lead time, their technology is more mature, and they are more familiar. However, they take longer to interrupt a fault due to their mechanical restrictions. They also tend to shut down the entire converter system, even for ground faults, which could be easily isolated. They are also inconvenient in multiterminal HVDC systems [3], [77], [78].

Protection can be achieved by using a combination of AC circuit breakers and fast action DC switches in a method known as “handshaking” as described above.

Fuses could be used to protect the multiterminal HVDC systems, but they cannot tell apart between temporary and permanent faults – all faults are considered permanent. They are only used as the last resort when other protection schemes fail [3].

2) HVDC system protection with DC devices: DC protection devices act faster than their AC counterparts and can isolate the faulted sections without closing the entire system.

a) DC circuit breaker equipment: Double-ended DC transmission systems use the ability of a thyristor to quickly cut off current to block the DC-side fault current. If the same process is used in multiterminal HVDC systems, however, it would require the entire multiterminal HVDC system to disconnect. Use of AC-side breakers would not be effective to protect the converters as these breakers are not fast enough. Thus, a high-voltage DC circuit breaker needs to be installed on the DC side, if the converters do not have the DC-side fault current blocking capability. Such DC breakers would significantly reduce the recovery time and shutting down the entire multiterminal HVDC system would not be necessary [3]. Since DC current does not have a natural zero-crossing, it should be forced to zero before a circuit breaker can act. Other issues that may arise before the current goes to zero, such as the arc time and overvoltage, should also be considered. Nevertheless, there are two main technologies for DC breakers: superposition oscillation current method and current transfer method.

The superposition oscillation current method utilizes the negative resistance characteristic of the arc to create an artificial zero of the oscillating current. However, the negative resistance characteristic becomes less obvious as the amplitude of the oscillating current increases, placing a limit on the circuit breaker's current capacity. Thus, it is not guaranteed that the breaker will counter the fault.

Current transfer method counters the fault current by discharging a capacitor in a direction such as to drive down the fault current. This method can break the DC-side fault current with a shorter break time compared to the superposition oscillation current method, but it is more complex, which makes it less reliable [79].

b) IGBT circuit breakers: These utilize the blocking capability of the solid-state device. They can block only the DC-side faults, not faults on the converter side. They are used together with fast action DC switches, which are used to isolate the faulted line after the IGBT blocks the fault. This strategy is more effective than the AC devices but also more expensive [3], with the cost close to half the total cost of the converter station [7].

c) Converter embedded devices: These are installed inside the voltage source converters to detect and isolate DC-side faults. They eliminate the use of additional devices, which reduces the converter footprint. However, a converter redesign is required [80].

3) Converters with fault blocking capability: Some converters have the capability to insert either a positive or negative voltage into the circuit. They are referred to as bipolar converters. For example, the FB converter inserts a negative voltage when all its four semiconductor switches are blocked [6]. The path of the current is such that the converter inserts a negative voltage. If a station MMC converter is based on a bipolar converter, it has the capability to block a DC fault by inserting a negative voltage. This voltage acts against the fault and eventually drives it to zero. If two such converters at the ends of a faulted line insert negative voltages and isolate the line through IGBT blocking, then the need for a DC breaker is eliminated. This has been asserted in the literature [4]. It is claimed that the reason the FB-SM and its derivatives are dismissed for use in HVDC systems is the increased semiconductor device count, increased power losses, and initial investment cost, compared to the widely accepted half bridge HB-SM [6 - 9], [81- 85]. But it has been realized that this justification is not necessarily objective. For example, the FB-SM needs to operate at only half the effective switching frequency due to the nature of the unipolar switching scheme used [60]. This drives down switching losses.

Furthermore, insertion of a negative voltage allows overmodulation, which means that the peak of the AC-side voltage gets higher than half of the DC-side voltage. One of the advantages of this kind of operation is the reduction or even elimination of circulating energy between the upper and lower arms, as well as SM capacitor voltage ripple reduction [59], [62]. Conversely, it can be viewed as a way to operate the converter at a lower DC bus

voltage either deliberately or as an optimal method in case of fluctuating energy systems such as wind power generator systems [86]. Deliberately operating the converter at low DC bus voltages through overmodulation implies lower SM capacitor voltages, which in turn implies lower blocking voltages for semiconductor devices. The advantages are the smaller-sized SM capacitors and semiconductor devices and reduced switching losses [60].

Although these observations do not arrive at a generalized conclusion that FB-based MMCs are competitive against or better than the HB-based MMCs, they call for an objective comparison between the two SMs as potential candidates for the HVDC-MMC.

2.5 CHAPTER SUMMARY

In this chapter an overview of the modular multilevel converter, the power electronic transformer, and high voltage DC transmission line protection was provided.
In Section 2.2 the topology and the basic operation of the modular multilevel converter was explored.

In Section 2.3 the modulation and control of the modular multilevel converter was explored. The modulation of the half-bridge and the full-bridge submodules was reviewed. It was seen that the control involved the main power as well as the submodule capacitor voltage balancing. However, it was found that there is not yet an elaborate method to calculate the control gains/constants for the submodule capacitor voltage balancing control loops if the classic control method is used, as opposed to the sorting method.

In section 2.4 the power electronic transformer and its feasibility to replace the line frequency transformer in the transmission lines was explored. It was found that although the power electronic transformer may not outperform the line frequency transformer when the two are compared as standalone units, it may do so if the system-level advantages it brings are considered. Such advantages are the grid stability and reduction or elimination of some of the grid components or functions that are used together with the line frequency transformer e.g. static synchronous compensators. The power electronic transformer also has

a smaller size and weight compared to the line frequency transformer, which may be critical requirements for some installations such as offshore wind farms. A conclusive comparison between the power electronic transformer and the line frequency transformer would be a good research problem.

It was also found that the half-bridge submodule has been deemed better than the full-bridge submodule for use in the high voltage DC modular multilevel converter but some of the converter-level and system-level advantages the full-bridge submodule offers have been overlooked. It has been concluded that if the comparison must be a fair one, all those advantages must be considered. Such advantages are the ability of the full-bridge submodule to operate at half the switching frequency of the half-bridge for the same effective switching frequency which reduces switching losses, the ability of the full-bridge to operate in the overmodulation region which reduces the components size and reduces submodule capacitor ripple, and the ability of the full-bridge to block a DC-side fault which eliminates the need for the expensive and bulky DC circuit breaker.

CHAPTER 3 MODELING OF THE MODULAR MULTILEVEL CONVERTER

3.1 CHAPTER OBJECTIVES

In this chapter the modeling of the MMC is carried out, starting with the basic operation of the converter, then the models pertaining to different control objectives of the MMC. The modeling lays the foundation for the analysis, design, and control of the MMC, to be carried out in subsequent chapters.

3.2 BASIC OPERATION OF THE MMC

With reference to Figure 2.2, the KVL equations of the MMC can be written as follows:

$$-\frac{1}{2}v_{dc}(t)+\sum_{j=1}^{N}v_{c_{mod},j}(t)+L_{arm}\frac{di_u(t)}{dt}+R_{arm}i_u(t)+v_{ac}(t)=0, \tag{3.1}$$

$$-\frac{1}{2}v_{dc}(t)+\sum_{j=N+1}^{2N}v_{c_{mod},j}(t)+L_{arm}\frac{di_l(t)}{dt}+R_{arm}i_l(t)-v_{ac}(t)=0, \tag{3.2}$$

whereby $v_{c_{mod},j}$ is the modulated SM capacitor voltage corresponding to the j^{th} SM and it appears on the AC side of the SM, i.e., across the terminals with the voltage v_{SM} in Figure 2.1 and Figure 2.2. KCL gives

$$i_{ac}(t)=i_l(t)-i_u(t). \tag{3.3}$$

The circulating current is that which circulates among a leg and the DC bus and does not appear on the AC side. It is defined as

$$i_{circ}(t) = \frac{i_l(t) + i_u(t)}{2}. \tag{3.4}$$

The third KVL equation is obtained as

$$-v_{dc}(t) + \sum_{j=1}^{2N} v_{c_{mod},j}(t) + 2R_{arm}i_{circ}(t) + 2L_{arm}\frac{di_{circ}(t)}{dt} = 0. \tag{3.5}$$

If $\sum_{j=1}^{N} v_{c_{mod},j}$ is named v_u, $\sum_{j=N+1}^{2N} v_{c_{mod},j}$ is named v_l, and $\sum_{j=1}^{2N} v_{c_{mod},j}$ is named v_{leg}, (3.1) becomes (3.6), (3.2) becomes (3.7), and (3.5) becomes (3.8).

$$-\frac{1}{2}v_{dc}(t) + v_u + L_{arm}\frac{di_u(t)}{dt} + R_{arm}i_u(t) + v_{ac}(t) = 0, \tag{3.6}$$

$$-\frac{1}{2}v_{dc}(t) + v_l + L_{arm}\frac{di_l(t)}{dt} + R_{arm}i_l(t) - v_{ac}(t) = 0. \tag{3.7}$$

$$-v_{dc}(t) + v_{leg} + 2R_{arm}i_{circ}(t) + 2L_{arm}\frac{di_{circ}(t)}{dt} = 0. \tag{3.8}$$

Accordingly,

$$\begin{aligned} v_{leg}(t) &= v_l(t) + v_u(t) \\ &= v_{dc}(t) - R_{arm}\big(i_l(t) + i_u(t)\big) - L_{arm}\frac{d}{dt}\big(i_l(t) + i_u(t)\big) \\ &= v_{dc}(t) - 2R_{arm}i_{circ}(t) - 2L_{arm}\frac{d}{dt}i_{circ}(t). \end{aligned} \tag{3.9}$$

In a balanced three phase MMC the DC bus current divides equally among the three legs. The circulating current consists of this DC component and the even harmonics of the fundamental component [87], i.e.,

$$\begin{aligned} i_{circ}(t) &= \frac{1}{3}i_{dc}(t) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \theta_n), \\ n &= 2, 4, 6, \ldots \end{aligned} \tag{3.10}$$

In (3.10), θ_n is the phase angle between the harmonic and the reference signal v_{ac}. Using (3.3) and (3.4) to solve for i_l and for i_u gives

$$i_l(t) = i_{circ}(t) + \frac{1}{2} i_{ac}(t) \tag{3.11}$$

and

$$i_u(t) = i_{circ}(t) - \frac{1}{2} i_{ac}(t) \tag{3.12}$$

Substituting (3.10) in (3.11) and in (3.12) gives

$$i_l(t) = \frac{1}{3} i_{dc}(t) + \frac{1}{2} i_{ac}(t) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \theta_n) \tag{3.13}$$

and

$$i_u(t) = \frac{1}{3} i_{dc}(t) - \frac{1}{2} i_{ac}(t) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \theta_n), \tag{3.14}$$

respectively, again with $n = 2, 4, 6, \ldots$

Subtracting (3.6) from (3.7) gives (3.15).

$$\begin{aligned} & v_l(t) - v_u(t) + R_{arm}(i_l(t) - i_u(t)) + L_{arm} \frac{d}{dt}\big(i_l(t) - i_u(t)\big) - 2v_{ac}(t) = 0 \\ \Rightarrow & \frac{v_l(t) - v_u(t)}{2} + \frac{1}{2} R_{arm} i_{ac}(t) + \frac{1}{2} L_{arm} \frac{d}{dt} i_{ac}(t) - v_{ac}(t) = 0 \\ \Rightarrow & v_{refl}(t) + \frac{1}{2} R_{arm} i_{ac}(t) + \frac{1}{2} L_{arm} \frac{d}{dt} i_{ac}(t) - v_{ac}(t) = 0 \end{aligned} \tag{3.15}$$

whereby

$$v_{refl}(t) = \frac{v_l(t) - v_u(t)}{2} \tag{3.16}$$

and is known as the internal EMF of the converter or the reflected DC bus voltage, and it is essentially the inverted DC bus voltage. Thus, the internal AC voltage of the converter can be conceptualized as a result of the switching matrix acting on the DC bus voltage. If the switching function is represented by ψ, then

$$v_{refl,k}(t) = \psi_k(t) V_{dc}, \qquad k \in \{a, b, c\} \tag{3.17}$$

whereby *k* represents the phase of the signal. Ideally ψ is a pure sinusoid. In practice it is a combination of a pure sinusoid and harmonics. In an MMC the harmonics are exacerbated by limited number of levels and significant size of voltage steps. The higher the number of levels and the smaller the steps the closer the switching function and the resulting internal

EMF are to pure sinusoids. From a perspective of an MMC inverter, v_{refl} is filtered by the arm inductors to give a much smoother voltage v_{ac} at the AC terminals, as is evident from (3.15). The simulated v_{ac} and v_{refl} are shown in Figure 3.1.

The average of v_{leg} is controlled to closely match the DC bus voltage average V_{dc}, with the small difference between v_{leg} and v_{dc} appearing across the arm inductor, as expressed by (3.9). Thus, if the AC variations in v_{leg} are ignored, $v_{leg}(t) = V_{leg}$. Ideally, the voltages v_{refl} and V_{leg} are related by [88]

$$v_{refl}(t) = \frac{1}{2} m_a V_{leg} \sin \omega t \tag{3.18}$$

whereby m_a is the modulation index defined as

$$m_a = \frac{2V_{ac}}{V_{dc}} \tag{3.19}$$

Equation (3.9) can be rewritten as

$$V_{leg} = v_l(t) + v_u(t) \tag{3.20}$$

Solving (3.16) and (3.20) for v_l and v_u then substituting (3.18) gives

$$v_l(t) = \frac{1}{2}(1 + m_a \sin \omega t) V_{leg} \tag{3.21}$$

and

$$v_u(t) = \frac{1}{2}(1 - m_a \sin \omega t) V_{leg}. \tag{3.22}$$

The functions $(1 + m_a \sin \omega t)/2$ and $(1 - m_a \sin \omega t)/2$ are equivalent to the SM quantities waveform duty ratio functions, for the lower and the upper arm SMs, respectively. Examples of such quantities are the SM output voltage and the SM capacitor current. This is implied from the analysis carried out in the literature, whereby these functions are used as modulation functions to synthesize capacitor voltages from the arm currents [89], as well as synthesize the SM AC-side voltage from its DC-side voltage [90]. The averages of these functions are 0.5, implying the average waveform duty of MMC quantities is 0.5.

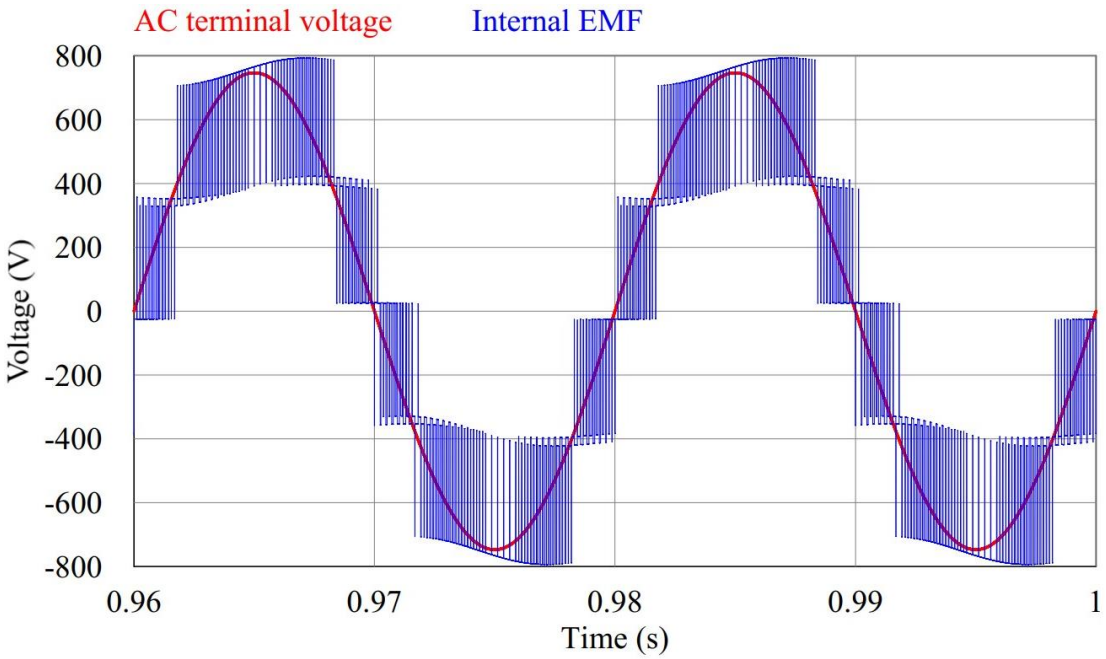

Figure 3.1. Simulated AC terminal voltage and the internal EMF.

3.3 CURRENT CONTROL MODEL

The voltage v_{ac} is given by

$$v_{ac}(t) = e(t) - \left(R_{grid} + R_{filter}\right)i_{ac}(t) - \left(L_{grid} + L_{filter}\right)\frac{d}{dt}i_{ac}(t), \tag{3.23}$$

so that (3.15) becomes

$$\begin{aligned} e(t) = v_{refl}(t) &+ \left(\frac{1}{2}R_{arm} + R_{grid} + R_{filter}\right)i_{ac}(t) \\ &+ \left(\frac{1}{2}L_{arm} + L_{grid} + L_{filter}\right)\frac{d}{dt}i_{ac}(t). \end{aligned} \tag{3.24}$$

Figure 3.2 illustrates (3.24), with the rectification stage also shown for the sake of converter completeness.

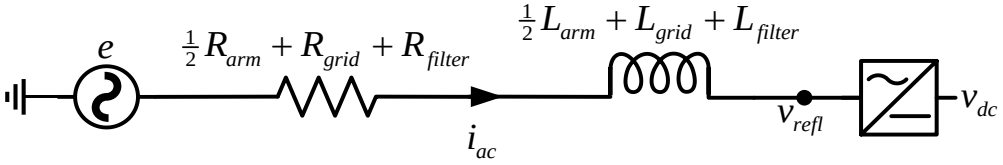

Figure 3.2. Equivalent of the AC-side and arm inductances, with their parasitic resistances. Adapted from [91], © 2015 IEEE.

The converter current control model to be used for the controller design is then illustrated in Figure 3.3. The model does apply to other VSCs other than the MMC [21], [92], [93].

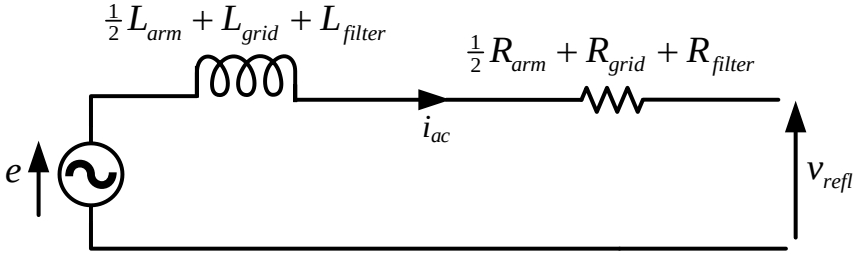

Figure 3.3. Current control model of a voltage source converter.

To simplify the controller design, vector control can be opted for. In this control scheme the circuit variables in the abc stationary-frame are transformed to the dq synchronous-frame. The dq frame is formed by two axes: the direct and the quadrature, which are 90° apart with the quadrature axis leading. The active power can be processed on either of the axes, with the reactive power being processed on the other axis. In the subsequent analysis, for simplicity, the subscript ac is dropped from i_{ac} and $refl$ is dropped from v_{refl}.

A three-phase system can be transformed into an equivalent two-phase system as follows

$$v_\alpha(t) + jv_\beta(t) = \frac{2}{3}K\left(v_a(t) + v_b(t)e^{j\frac{2\pi}{3}} + v_c(t)e^{j\frac{4\pi}{3}}\right) \tag{3.25}$$

with K being the scaling constant according to the type of transformation adopted, as indicated in Table 1 [93].

Table 3.1. Three-phase to two-phase transformation constants.

Type of transformation	Value of K
Amplitude invariant	1
RMS-value invariant	$1/\sqrt{2}$
Power invariant	$\sqrt{3/2}$

For the amplitude invariant transformation,

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}. \tag{3.26}$$

The signals v_α and v_β are still AC. They are further transformed into a synchronous reference frame so that the resulting signals are DC. If θ is the instantaneous angle between the direct-axis and the α-axis, then the dq signals are obtained as follows

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ \sin\theta & -\cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \tag{3.27}$$

Voltages across inductors transform to

$$\begin{aligned} v_{L,d}(t) &= L\frac{di_d(t)}{dt} + L\omega i_q(t), \\ v_{L,q}(t) &= L\frac{di_q(t)}{dt} - L\omega i_d(t), \end{aligned} \tag{3.28}$$

whereby i_d and i_q are the dq components of the AC current and $L = L_{grid} + L_{filter} + 0.5L_{arm}$ is the equivalent inductance. As seen in (3.28), the inductor voltages bring about the coupling of the direct and quadrature axes. A system controller for a closed loop must be designed such that the two axes are decoupled if the two axes must not interfere with each other.

KVL around Figure 3.3 gives

$$e(t) = L\frac{di(t)}{dt} + i(t)R + v(t) \tag{3.29}$$

Transformation of (3.29) into the dq frame gives

$$\begin{aligned} e_d(t) &= L\frac{di_d(t)}{dt} + L\omega i_q(t) + i_d(t)R + v_d(t) \\ e_q(t) &= L\frac{di_q(t)}{dt} - L\omega i_d(t) + i_q(t)R + v_q(t) \end{aligned} \tag{3.30}$$

Choosing the q-axis as the power axis, e_d is zero while e_q is the amplitude of e. For a unity power factor condition, the controller reference of i_d is set to zero so that the system active power is given by

$$P = \frac{3}{2}E_q I_q \tag{3.31}$$

while the reactive power is zero. To decouple the two axes, the following decoupling equations are used [93]:

$$\begin{aligned} v_d(t) &= -v'_d(t) + e_d(t) - \omega L i_q(t), \\ v_q(t) &= -v'_q(t) + e_q(t) + \omega L i_d(t), \end{aligned} \tag{3.32}$$

so that (3.30) becomes

$$\begin{aligned} v'_d(t) &= L\frac{di_d(t)}{dt} + i_d(t)R, \\ v'_q(t) &= L\frac{di_q(t)}{dt} + i_q(t)R. \end{aligned} \tag{3.33}$$

The system transfer function is then G_{system} in (3.34).

$$\begin{aligned} v'(t) = L\frac{di(t)}{dt} + i(t)R \;\leftrightarrow\; V'(s) = I(s)(sL+R) \leftrightarrow \frac{I(s)}{V'(s)} = G_{system}(s) \\ = \frac{1}{sL+R} \end{aligned} \tag{3.34}$$

Due to the switching action of the converter, there is a finite delay before the output voltage is synthesized at each switching instant. The transfer function of the converter is due to this delay and is given by (3.35), whereby T_{sw} is the switching period and $T_{sw}/2$ is the corresponding switching delay [94].

$$G_{delay}(s) = \frac{1}{\frac{T_{sw}}{2}s + 1} \tag{3.35}$$

The current controller is designed based on the product of G_{system} and G_{delay}, defined as G_{curr} in (3.36).

$$G_{curr}(s) = G_{system}(s) \times G_{delay}(s) = \frac{\frac{1}{R}}{\frac{T_{sw}L}{2R}s^2 + \left(\frac{T_{sw}}{2} + \frac{L}{R}\right)s + 1} \tag{3.36}$$

3.4 DC BUS VOLTAGE CONTROL MODEL

In rectifier mode, with a physical capacitor of capacitance C_{eq} connected across the DC terminals, the transfer function of the active power processing current component to the DC bus voltage of a multilevel converter is given as [95]

$$\frac{V_{dc}(s)}{I_q(s)} = \frac{3E_q}{2V_{dc,ref}C_{eq}s}, \tag{3.37}$$

whereby $V_{dc,ref}$ is the desired DC bus voltage. However, for an HVDC-MMC a DC-link capacitor would exacerbate the DC-side fault current. For that reason, the DC terminals are not connected to a filter capacitor. Nevertheless, it has been shown that the equivalent capacitance contributed by the SM capacitors across the DC terminals of a three phase MMC is given by [96]

$$C_{eq} = \frac{6C_{SM}}{N}. \tag{3.38}$$

The transfer function of (3.37) is then rewritten as

$$\frac{V_{dc}(s)}{I_q(s)} = \frac{NE_q}{4V_{dc,ref}C_{SM}s}. \tag{3.39}$$

3.5 SUBMODULE CAPACITOR VOLTAGE BALANCING CONTROL MODELS

The parameters of the individual SM capacitor voltage balancing, the arm voltage balancing, and the leg average voltage controllers have been quoted to remain the same in some studies or to have been obtained through simulation in other studies [22], [34], as alluded to in Chapter 2.

To attain optimal control, it is important that transfer functions for the control loops in question be found, so that the controllers can be designed in a straightforward, step by step manner. This is because, although the MMC structure is the same, design at different power and voltage levels and with different filter sizes imply that the system dynamics are not necessarily the same.

The suggested controller gains for the individual SM capacitor and the arm voltage balancing controllers are simple proportional constants [31], [32]. If it is assumed that indeed the nature of their loops call for proportional controllers, then tuning of these gains has only two

possibilities: increase or decrease the gains. This is simple enough as one can simply change the gain in one direction at a time and observe how the system performance changes.

The circulating current suppression controller is well suited for tuning as it is centred around the harmonic frequency of interest, with constants to adjust the gain and a constant to adjust the bandwidth around the controlled frequency.

The leg average voltage controller, however, is suggested to have either a PI controller for the outer loop and a proportional controller for the inner loop or PI controllers for both the loops. Proper design of these controllers requires transfer functions for the involved loops. The subsequent modeling is part of the contribution of this dissertation.

The loops for the leg average voltage controller can be conceptualized as in Figure 3.4. In this figure, G_{vb} is the outer [voltage] loop controller, G_{cb} is the inner [current] loop controller, G_{PWM} is the PWM block transfer function, given by $G_{PWM}(s) = 1/V_{car}$ (V_{car} is the peak-peak value of the carrier signal), $H_{sen,cb}$ is the current sensor transfer function, $H_{sen,vb}$ is the voltage sensor transfer function, and H_{cb} and H_{vb} are the duty ratio to circulating current and circulating current to SM capacitor voltage transfer functions, respectively, given as $H_{cb}(s) = I_{circ}(s)/D(s)$ and $H_{vb}(s) = V_c(s)/I_{circ}(s)$.

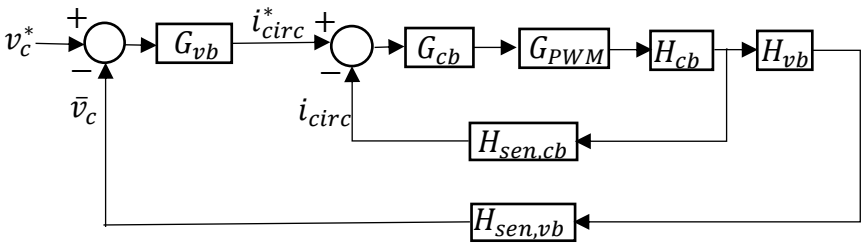

Figure 3.4. The proposed control loops for the leg average voltage controller.

The KVL equation (3.5) linking the DC bus, the arm voltages and the circulating current can be rewritten as

$$v_{dc}(t) = \sum_{j=1}^{2N} v_{c_{mod},j}(t) + 2i_{circ}(t)(pL_{arm} + R_{arm}), \tag{3.40}$$

whereby p is the time differential operator d/dt. Since $v_{c_{mod}}$ is the modulated SM capacitor voltage, it is given by

$$v_{c_{mod},j}(t) = v_{c,j}(t) \times \delta_j(t) \tag{3.41}$$

whereby $v_{c,j}$ is the j^{th} SM capacitor voltage and δ_j is the duty ratio function for the j^{th} SM, so that the KVL equation is now given by

$$v_{dc}(t) = \sum_{j=1}^{2N} \delta_j(t) v_{c,j}(t) + 2i_{circ}(t)(pL_{arm} + R_{arm}). \tag{3.42}$$

Small signal analysis can be used to linearize the term $\delta_j(t)v_{c,j}(t)$ of (3.42), as follows:

$$\begin{aligned} V_{dc} + \tilde{v}_{dc}(t) &= \sum_{j=1}^{2N} \left(D + \tilde{\delta}_j(t)\right)\left(V_c + \tilde{v}_{c,j}(t)\right) \\ &\quad + 2\left(I_{circ} + \tilde{\imath}_{circ}(t)\right)(pL_{arm} + R_{arm}) \\ &= \sum_{j=1}^{2N} \left(DV_c + D\tilde{v}_{c,j}(t) + \tilde{\delta}_j(t)V_c + \tilde{\delta}_j(t)\tilde{v}_{c,j}(t)\right) + 2I_{circ}(pL_{arm} + R_{arm}) \\ &\quad + 2\tilde{\imath}_{circ}(t)(pL_{arm} + R_{arm}). \end{aligned} \tag{3.43}$$

The DC terms are given by

$$\begin{aligned} V_{dc} &= \sum_{j=1}^{2N} DV_c + 2I_{circ}(pL_{arm} + R_{arm}) \\ &= 2NDV_c + 2I_{circ}R_{arm} = NV_c + \frac{2}{3}I_{dc}R_{arm} \end{aligned} \tag{3.44}$$

whereby $D = 0.5$, as discussed previously. If the parasitic resistance R_{arm} is ignored then $V_{dc} = NV_c$, which agrees with the literature. The AC terms are given by

$$\begin{aligned} \tilde{v}_{dc}(t) &= \sum_{j=1}^{2N} \left(D\tilde{v}_{c,j}(t) + \tilde{\delta}_j(t)V_c\right) + 2\tilde{\imath}_{circ}(t)(pL_{arm} + R_{arm}) \\ &= D\sum_{j=1}^{2N} \tilde{v}_{c,j}(t) + V_c\sum_{j=1}^{2N} \tilde{\delta}_j(t) + 2\tilde{\imath}_{circ}(t)(pL_{arm} + R_{arm}), \end{aligned} \tag{3.45}$$

whereby the second order term $\tilde{\delta}_j(t)\tilde{v}_{c,j}(t)$ is ignored as it is significantly smaller than any of the corresponding first order terms $D\tilde{v}_{c,j}(t)$ and $\tilde{\delta}_j(t)V_c$ [97]. The Laplace transform of (3.45) is

$$V_{dc}(s) = DV_c(s)X(s) + V_cD(s)W(s) + 2I_{circ}(s)(sL_{arm} + R_{arm}) \tag{3.46}$$

whereby

$$V_c(s)X(s) = \mathcal{L}\left\{\sum_{j=1}^{2N} \tilde{v}_{c,j}(t)\right\} \tag{3.47}$$

and

$$D(s)W(s) = \mathcal{L}\left\{\sum_{j=1}^{2N} \tilde{\delta}_j(t)\right\}. \tag{3.48}$$

The functions W and X can take different forms depending on the modulation scheme utilized. Since the unipolar modulation scheme used in the FB-MMC is different from the modulation scheme used in the HB-MMC, W_{hb} and X_{hb} are the functions associated with the HB-MMC while W_{fb} and X_{fb} are the functions associated with the FB-MMC.

In the subsequent discussion m_f is the frequency modulation index defined as $m_f = f_{sw}/f = T/T_{sw}$, f_{sw} is the switching frequency and f is the fundamental frequency. $T = 1/f$ is the fundamental period.

In the HB-MMC, the carrier signals in an arm are shifted by $2\pi/N$ $(\equiv T_{sw}/N)$ while the corresponding upper and lower arm carrier signals are shifted by π/N $(\equiv T_{sw}/2N)$, and the lower arm modulating signal is shifted from the upper arm modulating signal by π $\left(\equiv T/2 = m_f T_{sw}/2\right)$, so that

$$\begin{aligned}\sum_{j=1}^{2N}\tilde{\delta}_j(t) &= \tilde{\delta}_1+\tilde{\delta}_2+\tilde{\delta}_3+\cdots+\tilde{\delta}_N+\tilde{\delta}_{N+1}+\tilde{\delta}_{N+2}+\tilde{\delta}_{N+3}+\cdots+\tilde{\delta}_{2N}\\ &= \tilde{\delta}(t)+\tilde{\delta}\left(t-\frac{1}{N}T_{sw}\right)+\tilde{\delta}\left(t-2\times\frac{1}{N}T_{sw}\right)+\cdots\\ &\quad+\tilde{\delta}\left(t-(N-1)\times\frac{1}{N}T_{sw}\right)+\tilde{\delta}\left(t-\frac{1}{2N}T_{sw}-\frac{m_f}{2}T_{sw}\right)\\ &\quad+\tilde{\delta}\left(t-\frac{1}{N}T_{sw}-\frac{1}{2N}T_{sw}-\frac{m_f}{2}T_{sw}\right)\\ &\quad+\tilde{\delta}\left(t-2\times\frac{1}{N}T_{sw}-\frac{1}{2N}T_{sw}-\frac{m_f}{2}T_{sw}\right)+\cdots\\ &\quad+\tilde{\delta}\left(t-(N-1)\times\frac{1}{N}T_{sw}-\frac{1}{2N}T_{sw}-\frac{m_f}{2}T_{sw}\right)\\ &= \tilde{\delta}(t)+\delta\left(t-\frac{1}{N}T_{sw}\right)+\tilde{\delta}\left(t-\frac{2}{N}T_{sw}\right)+\cdots\\ &\quad+\tilde{\delta}\left(t-\frac{(N-1)}{N}T_{sw}\right)+\tilde{\delta}\left(t-\frac{1+Nm_f}{2N}T_{sw}\right)\\ &\quad+\tilde{\delta}\left(t-\frac{3+Nm_f}{2N}T_{sw}\right)+\tilde{\delta}\left(t-\frac{5+Nm_f}{2N}T_{sw}\right)+\cdots\\ &\quad+\tilde{\delta}\left(t-\frac{2N-1+Nm_f}{2N}T_{sw}\right).\end{aligned} \tag{3.49}$$

Generally,

$$\sum_{j=1}^{2N}\tilde{\delta}_j(t)=\sum_{j=1}^{N}\left\{\tilde{\delta}\left(t-\frac{j-1}{N}T_{sw}\right)+\tilde{\delta}\left(t-\frac{2j-1+Nm_f}{2N}T_{sw}\right)\right\}. \tag{3.50}$$

For N = 2,

$$\begin{aligned}\sum_{j=1}^{2N}\tilde{\delta}_j(t) &= \tilde{\delta}(t)+\tilde{\delta}\left(t-\frac{1}{2}T_{sw}\right)+\tilde{\delta}\left(t-\frac{1+2m_f}{4}T_{sw}\right)\\ &\quad+\tilde{\delta}\left(t-\frac{3+2m_f}{4}T_{sw}\right).\end{aligned} \tag{3.51}$$

$$\mathcal{L}\{f(t-t_0)\}=F(s)\exp(-st_0)$$

$$\Rightarrow \mathcal{L}\left\{\sum_{j=1}^{2N} \tilde{\delta}_j\,(t)\right\}$$
$$= D(s)\left(1 + \exp\left(-\frac{1}{2}T_{sw}s\right) + \exp\left(-\frac{1+2m_f}{4}T_{sw}s\right)\right.$$
$$\left. + \exp\left(-\frac{3+2m_f}{4}T_{sw}s\right)\right) = D(s)W_{hb}(s), \tag{3.52}$$

whereby

$$W_{hb}(s) = 1 + \exp\left(-\frac{1}{2}T_{sw}s\right) + \exp\left(-\frac{1+2m_f}{4}T_{sw}s\right)$$
$$+ \exp\left(-\frac{3+2m_f}{4}T_{sw}s\right), \tag{3.53}$$

which can be linearized using a Taylor series expansion or a Padé approximation. In Addendum A equation (3.50) is expanded for other arbitrary values of N, to demonstrate the scalability of the modeling method.

In the case of the FB-MMC, the two signals modulating the left and the right arms of the FB-SM can be viewed as forming one composite modulating signal for the SM, see simulation in Figure 3.5. In that case the lower arm composite modulating signal is phase-shifted by $\pi\ (\equiv T/2 = m_f T_{sw}/2)$ from the upper arm composite modulating signal. Within the arm the carrier signals are phase-shifted by $\pi/N\ (\equiv T_{sw}/2N)$ while the corresponding lower and the upper arm carrier signals are phase-shifted by $\pi/2N\ (\equiv T_{sw}/4N)$, so that

$$\sum_{j=1}^{2N}\tilde{\delta}_j(t) = \tilde{\delta}_1 + \tilde{\delta}_2 + \tilde{\delta}_3 + \cdots + \tilde{\delta}_N + \tilde{\delta}_{N+1} + \tilde{\delta}_{N+2} + \tilde{\delta}_{N+3} + \cdots + \tilde{\delta}_{2N}$$

$$\begin{aligned}
&= \tilde{\delta}(t) + \tilde{\delta}\left(t - \frac{1}{2N}T_{sw}\right) + \tilde{\delta}\left(t - 2\times\frac{1}{2N}T_{sw}\right) + \cdots \\
&\quad + \tilde{\delta}\left(t - (N-1)\times\frac{1}{2N}T_{sw}\right) + \tilde{\delta}\left(t - \frac{1}{4N}T_{sw} - \frac{m_f}{2}T_{sw}\right) \\
&\quad + \tilde{\delta}\left(t - \frac{1}{2N}T_{sw} - \frac{1}{4N}T_{sw} - \frac{m_f}{2}T_{sw}\right) \\
&\quad + \tilde{\delta}\left(t - 2\times\frac{1}{2N}T_{sw} - \frac{1}{4N}T_{sw} - \frac{m_f}{2}T_{sw}\right) + \cdots \\
&\quad + \tilde{\delta}\left(t - (N-1)\times\frac{1}{2N}T_{sw} - \frac{1}{4N}T_{sw} - \frac{m_f}{2}T_{sw}\right) \qquad (3.54)\\
&= \tilde{\delta}(t) + \delta\left(t - \frac{1}{2N}T_{sw}\right) + \tilde{\delta}\left(t - \frac{2}{2N}T_{sw}\right) + \cdots \\
&\quad + \tilde{\delta}\left(t - \frac{(N-1)}{2N}T_{sw}\right) + \tilde{\delta}\left(t - \frac{1+2Nm_f}{4N}T_{sw}\right) \\
&\quad + \tilde{\delta}\left(t - \frac{3+2Nm_f}{4N}T_{sw}\right) + \tilde{\delta}\left(t - \frac{5+2Nm_f}{4N}T_{sw}\right) + \cdots \\
&\quad + \tilde{\delta}\left(t - \frac{2N-1+2Nm_f}{4N}T_{sw}\right).
\end{aligned}$$

Generally,

$$\sum_{j=1}^{2N}\tilde{\delta}_j(t) = \sum_{j=1}^{N}\left\{\tilde{\delta}\left(t - \frac{j-1}{2N}T_{sw}\right) + \tilde{\delta}\left(t - \frac{2j-1+2Nm_f}{4N}T_{sw}\right)\right\}. \qquad (3.55)$$

For N = 2,

$$\begin{aligned}
\sum_{j=1}^{2N}\tilde{\delta}_j(t) &= \tilde{\delta}(t) + \tilde{\delta}\left(t - \frac{1}{4}T_{sw}\right) + \tilde{\delta}\left(t - \frac{1+4m_f}{8}T_{sw}\right) \qquad (3.56)\\
&\quad + \tilde{\delta}\left(t - \frac{3+4m_f}{8}T_{sw}\right).
\end{aligned}$$

$$\mathcal{L}\{f(t-t_0)\} = F(s)\exp(-st_0)$$

$$\Rightarrow \mathcal{L}\left\{\sum_{j=1}^{2N}\tilde{\delta}_j(t)\right\} = D(s)\left(1+\exp\left(-\frac{1}{4}T_{sw}s\right)+\exp\left(-\frac{1+4m_f}{8}T_{sw}s\right)+\exp\left(-\frac{3+4m_f}{8}T_{sw}s\right)\right) = D(s)W_{fb}(s), \tag{3.57}$$

whereby

$$W_{fb}(s) = 1+\exp\left(-\frac{1}{4}T_{sw}s\right)+\exp\left(-\frac{1+4m_f}{8}T_{sw}s\right)+\exp\left(-\frac{3+4m_f}{8}T_{sw}s\right). \tag{3.58}$$

The plots of both $W_{hb}(s)$ and $W_{fb}(s)$ approximated to the first order using the Padé approximation $\exp_{0/1}(x) = 1/(1-x)$, at the same switching frequency, appear in Figure 3.6. The first order terms in (3.53) and (3.58) are collected in the manner of (3.59).

$$W(s) = 1+\exp\left(-st_{0_1}\right)+\exp\left(-st_{0_2}\right)+\exp\left(-st_{0_3}\right) \approx 4 - s(t_{0_1}+t_{0_2}+t_{0_3}) \approx 4\exp\left(-\frac{t_{0_1}+t_{0_2}+t_{0_3}}{4}s\right) \approx \frac{4}{1+\frac{t_{0_1}+t_{0_2}+t_{0_3}}{4}s} \tag{3.59}$$

$X(s)$ is the Laplace transform corresponding to time delays due to phase differences in the SM capacitor voltages in the MMC leg. These phase differences are a result of the SM capacitor voltage being an integral of the product of the duty ratio function and the arm current. If the phase shift introduced by the arm current is ignored, $X(s) = W(s)$. This is justified since the major phase difference observed is that between the upper arm SM capacitor voltages and the lower arm SM capacitor voltages, and it is equal to π, equivalent to half the fundamental period. Additional phase shifts between individual SM capacitor voltages are due to time delays fractional of the switching period, insignificant compared to half the fundamental period.

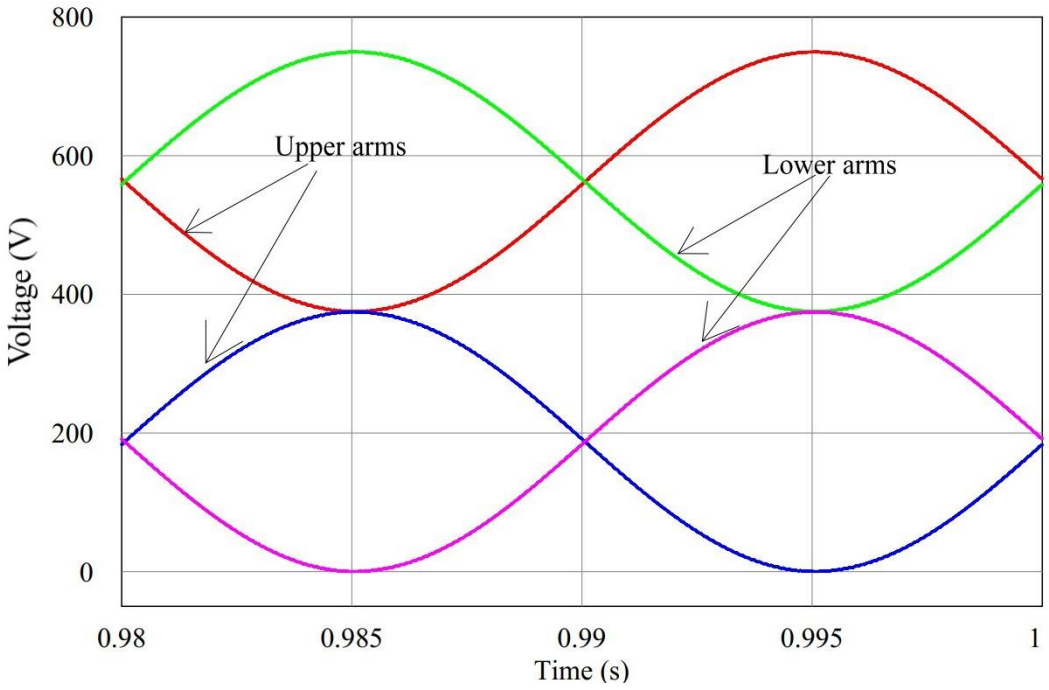

Figure 3.5. Simulated FB-SM modulating signals at a fundamental frequency of 50 Hz.

From (3.46) the transfer function from the duty ratio to the circulating current is obtained as

$$H_{cb}(s) = \frac{I_{circ}(s)}{D(s)} = -\frac{\frac{1}{2}V_c W(s)}{sL_{arm} + R_{arm}} \tag{3.60}$$

and the transfer function from the circulating current to the SM capacitor voltage is obtained as

$$H_{vb}(s) = \frac{V_c(s)}{I_{circ}(s)} = -\frac{sL_{arm} + R_{arm}}{\frac{1}{2}DX(s)} = -\frac{sL_{arm} + R_{arm}}{\frac{1}{4}X(s)} \tag{3.61}$$

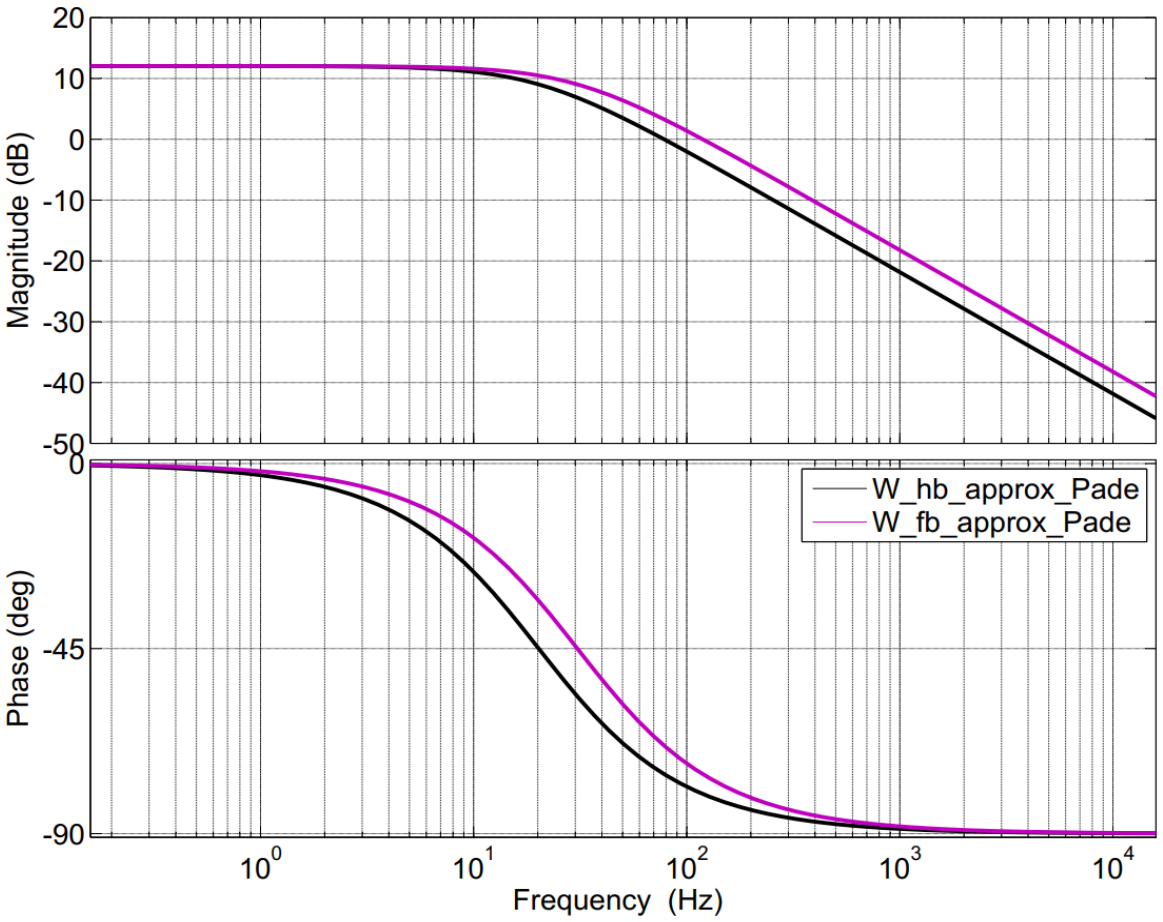

Figure 3.6. $W_{hb}(s)$ and $W_{fb}(s)$ approximated to the first order using the Padé approximation.

3.6 CHAPTER SUMMARY

In this chapter the modular multilevel converter was modeled. Section 3.1 focused on the basic operation of the converter. In section 3.2 the current control model was developed, in section 3.3 the DC bus voltage control model was developed, and in section 3.4 the leg average voltage control model was developed from first principles. The leg average voltage control model makes the respective controller design straightforward and eliminates the dependence on extensive simulation and guesswork to tune the controllers, as it is often done in the literature. The development of the leg average voltage control model is part of the contribution of this dissertation.

CHAPTER 4 ANALYSIS OF THE MODULAR MULTILEVEL CONVERTER WITH HALF-BRIDGE AND FULL-BRIDGE SUBMODULES

4.1 CHAPTER OBJECTIVES

This chapter aims at the device rating and loss analysis of the MMC. The analysis performed in this chapter is part of the contribution of this dissertation.

4.2 INTRODUCTION

The FB-MMC can operate in the overmodulation region, which should be considered when comparing it to the HB-MMC. For the switching losses comparison, the FB-SM semiconductor switches can be operated at half the switching frequency of the semiconductor switches in the HB-MMC for the same effective switching frequency. When overmodulation is considered, the specific modulation index $m_a = \sqrt{2} \approx 1.4142$ is of special interest as it has been shown to minimize the arm circulating currents and SM capacitor ripple voltages, as at this modulation index the converter transfers active power while processing the minimum possible reactive power in the arms [59]. S is the system rated apparent power.

4.3 DEVICE RATINGS

The devices considered are the SM semiconductor switches and the SM capacitors.

For a FB-MMC the peak of the AC voltage is dependent on both the amplitude modulation index and the number of SMs per arm, N. If the average SM capacitor voltage is V_c, then [60]

$$V_{ac} \leq NV_c - \frac{1}{2}V_{dc}. \tag{4.1}$$

The peak of the AC voltage is given by (3.19). Making V_{dc} in (3.19) the subject and substituting it into (4.1) gives

$$\begin{aligned} V_{ac} &\leq NV_c - \frac{V_{ac}}{m_a} \\ \Rightarrow V_c &\geq \frac{V_{ac}}{N}\left(1 + \frac{1}{m_a}\right) \end{aligned} \tag{4.2}$$

If V_{ac} and N are fixed, then V_c is a function of m_a and its minimum required value for given m_a is

$$V_c(m_a) = \frac{V_{ac}}{N}\left(1 + \frac{1}{m_a}\right) \tag{4.3}$$

According to (4.3), the higher the modulation index the lower the voltage the SM capacitor must support. This means a lower voltage rated capacitor. Since this is also the voltage the SM semiconductor switches must block, it also means lower voltage rated semiconductor switches. For example, the SM capacitor designed for $m_a = \sqrt{2}$ is rated at 85.4% of that designed for $m_a = 1$, calculated as follows

$$\frac{V_c(\sqrt{2})}{V_c(1)} = \frac{1 + \frac{1}{\sqrt{2}}}{2} = 0.85355 \text{ p.u.}$$

This also means that the semiconductor switches for an $m_a = \sqrt{2}$ system must block only 85.4% of the voltage blocked by semiconductor switches for a system designed for a unity modulation index. However, their RMS current ratings will be about 1.15 times higher, due to a lower DC bus voltage which makes the DC component of the arm current increase. This is a ratio of the arm RMS current values at the respective modulation indices, keeping in

mind that the switch currents are proportional to these currents, and ignoring the harmonics, i.e.,

$$i_{arm,RMS} = i_{u,RMS} = i_{l,RMS} = \sqrt{\left(\frac{I_{dc}}{3}\right)^2 + \left(\frac{I_{ac,RMS}}{2}\right)^2} = \sqrt{\left(\frac{S}{3V_{dc}}\right)^2 + \left(\frac{S}{2\sqrt{3}V_{LL}}\right)^2}$$
$$= \sqrt{\left(\frac{S}{3V_{dc}}\right)^2 + \left(\frac{S}{2\sqrt{3}m_a\frac{V_{dc}}{2}\sqrt{\frac{3}{2}}}\right)^2} = \sqrt{\frac{S^2}{9V_{dc}^2} + \frac{2S^2}{9m_a^2V_{dc}^2}} \tag{4.4}$$
$$= \frac{S}{3V_{dc}}\sqrt{1 + \frac{2}{m_a^2}} = \frac{S}{6V_{ac}}\sqrt{2 + m_a^2}.$$

For fixed V_{ac}, the arm RMS current is a function of the modulation index and can be expressed as

$$i_{arm,RMS}(m_a) = \frac{S}{6V_{ac}}\sqrt{2 + m_a^2}$$

$$\Rightarrow \frac{i_{arm,RMS}(\sqrt{2})}{i_{arm,RMS}(1)} = \sqrt{\frac{4}{3}} \approx 1.15 \text{ p. u.}$$

This increased arm current will also increase the SM capacitor current ratings, which may lead to larger SM capacitor banks.

An added advantage of operating the MMC in the overmodulation region is the use of a smaller DC bus voltage (a case when an AC voltage is fixed, and the DC bus must be designed such that the output AC voltage will be attained). This means that there is no boosting of the DC bus voltage to achieve the required output, provided that the resulting modulation index does not subject the SMs to higher than rated conditions [6], and does not result into higher than desired harmonics.

4.4 POWER LOSSES COMPARISONS BETWEEN HB-MMC AND FB-MMC

The losses considered are the semiconductor switch and its antiparallel diode conduction losses, the switching losses, and the ohmic losses in the arm inductor parasitic resistance.

The antiparallel diode reverse recovery losses are insignificant compared to the switching losses hence they are not considered in this analysis [98].

4.4.1 Semiconductor switch and antiparallel diode conduction losses

The semiconductor switch (assuming an IGBT) conduction losses, per device, are given by

$$P_{on,sw} = I_{sw,ave} \times V_{ce,sat} = I_{sw,ave} \times V_{ce,0} + {I_{sw,RMS}}^2 \times r_{ce} \tag{4.5}$$

whereby $V_{ce,sat}$ is the voltage drop across the switch during conduction, $I_{sw,ave}$ is the average switch current, $I_{sw,RMS}$ is the switch RMS current, $V_{ce,0}$ is the collector-emitter threshold voltage of the IGBT's forward characteristic approximation, and r_{ce} is the on-state slope resistance of the IGBT's forward characteristic approximation.

To compare the FB-MMC and the HB-MMC losses, the number of devices per SM must be accounted for, i.e., four devices in the FB-MMC and two devices in the HB-MMC. This implies that the conduction losses in the FB-MMC are twice the conduction losses in the HB-MMC, as the arm currents in the two converters are identical and get distributed equally among the devices, on average.

In the overmodulation region the DC arm current is higher than in the linear modulation region. Since $V_{ce,sat}$ in (4.5) is assumed to remain constant regardless of the switch current changes, the switch current increases corresponding to the increase in the arm current, resulting into higher conduction losses.

The analysis for semiconductor switch conduction losses similarly applies to its antiparallel diode, whereby the conduction losses are instead due to the on-state voltage drop V_{fwd}, i.e.,

$$P_{on,diode} = I_{diode,ave} \times V_{fwd} = I_{diode,ave} \times V_{fwd,0} + {I_{diode,RMS}}^2 \times r_{fwd} \tag{4.6}$$

whereby $I_{diode,ave}$ is the diode average current, $I_{diode,RMS}$ is the diode RMS current, $V_{fwd,0}$ is the threshold voltage of the diode's forward characteristic approximation, and r_{fwd} is the on-state slope resistance of the diode's forward characteristic approximation. The

conduction losses in the FB-MMC diode will be twice as much as in the HB-MMC diode in the linear modulation region and will be even higher in the overmodulated FB-MMC.

4.4.2 Semiconductor switching losses

The switching losses per device are given by [61]

$$P_{sw} = \frac{1}{2} \times V_{sw,block} \times I_{sw,pk} \times f_{sw} \times 2(t_r + t_f), \tag{4.7}$$

whereby t_r and t_f are respectively the rise and fall times of the voltage across and the current through the switch (the voltage and current are assumed to have equal rise times and equal fall times). At a given modulation index, over the fundamental period the switch current peak is proportional to the arm DC current, i.e., $I_{sw,pk} = \alpha I_{dc}/3$, since the instantaneous switch current peak varies around the value $\alpha I_{dc}/3$ due to the presence of the AC components in the current (see illustrated simulation in Figure 4.1). The blocking voltage, $V_{sw,block}$, equals the SM capacitor average voltage V_c, as discussed previously. Again, the number of devices must be considered, as well as the switching frequency. The FB-MMC devices are operated half the switching frequency as that in the HB-MMC. Then

$$\frac{P_{sw_{FB}}}{P_{sw_{HB}}} = \frac{4P_{sw}|_{\frac{1}{2}f_{sw}}}{2P_{sw}|_{f_{sw}}}$$

$$= \frac{4}{2} \times \frac{\frac{1}{2} \times V_{sw,block} \times I_{sw,pk} \times \frac{1}{2} f_{sw} \times 2(t_r + t_f)}{\frac{1}{2} \times V_{sw,block} \times I_{sw,pk} \times f_{sw} \times 2(t_r + t_f)} = 1, \qquad m_a \leq 1, \tag{4.8}$$

which indicates that the switching losses are equal for $m_a \leq 1$. It is however unknown if they will be higher in the FB-MMC if it is operated in the overmodulation region. This is because while the switch peak current increases, the blocking voltage decreases, and the changes in the two quantities are not necessarily proportional.

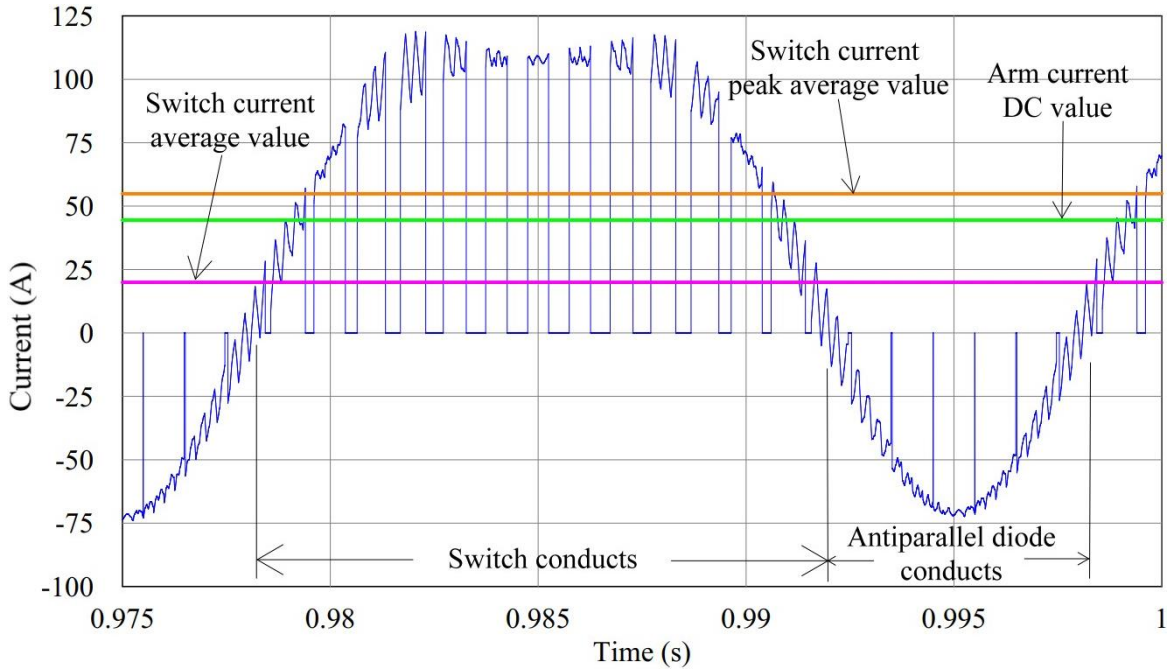

Figure 4.1. Illustrated simulation of current flowing through the switch and its antiparallel diode (which is a modulated arm current).

4.4.3 Arm inductor I^2R losses

Due to the parasitic resistance in the arm inductor, there will be ohmic losses. The losses in one of the arm inductors for an arbitrary modulation index are calculated as in (4.9), with $i_{arm,RMS}$ as derived in (4.4).

$$P_{resistor}(m_a) = i_{arm,RMS}^2(m_a) \times R_{arm} = \frac{S^2}{9\left(\frac{2V_{ac}}{m_a}\right)^2}\left(1+\frac{2}{m_a^2}\right)R_{arm}$$
$$= \left(\frac{m_a S}{6V_{ac}}\right)^2\left(1+\frac{2}{m_a^2}\right)R_{arm} = \left(\frac{S}{6V_{ac}}\right)^2(2+m_a^2)R_{arm} \quad (4.9)$$

Keeping in mind that the HB-MMC can operate only in the linear modulation region, (4.9) indicates that the ohmic losses in the FB-MMC and the HB-MMC will be equal for $m_a \leq 1$. In the overmodulation region the FB-MMC will process higher ohmic losses.

4.5 CHAPTER SUMMARY

In this chapter the HB-MMC and the FB-MMC were compared through analysis. It has been seen that operating the FB-MMC in the overmodulation region allows for a smaller DC bus voltage and smaller SM capacitor and semiconductor switch voltage ratings. It however increases the SM semiconductor switch current ratings by almost the same proportion their voltage ratings are reduced. It has been thought in the literature that operating the FB-MMC in the overmodulation region would help reduce the ratings of its components. The analysis in this chapter shows that it is not the case. The conduction and the ohmic losses both increase with overmodulation while the switching losses cannot be predicted to increase or decrease. In the linear modulation region, the conduction losses in the FB-MMC are twice as much as those in the HB-MMC while the switching and the ohmic losses are equal in both the converters. The detailed power loss analysis is another area this chapter contributes to the wider body of knowledge.

CHAPTER 5 DESIGN OF THE MODULAR MULTILEVEL CONVERTER

5.1 CHAPTER OBJECTIVES

This chapter intends to size the filter components of the converter, that is, the SM capacitor and the arm inductor.

5.2 INTRODUCTION

The design involves SM capacitor and arm inductor sizing. For building a physical converter, ratings of these components would be required, they are however unnecessary for the purpose of simulation to validate the operation of the converter. They may however be needed in simulation of losses to paint a realistic picture of the losses.

The converter processes $S = 200$ kVA at unity power factor with an AC bus at 915 V line-line, a DC bus at 1500 V, and two submodules per arm. The device switching frequency is 1 kHz for the FB converter and 2 kHz for the HB-MMC.

5.3 SUBMODULE CAPACITOR SIZING

The SM capacitors are sized to minimize the capacitor voltage ripple. The capacitor voltage ripple is usually kept at around (or below) 5% of the nominal capacitor voltage [92]. The nominal voltage of a SM capacitor is calculated from (4.3) as

$$V_c = \frac{V_{ac}}{N}\left(1+\frac{1}{m_a}\right) = \frac{915\sqrt{\frac{2}{3}}}{2}\left(1+\frac{1}{0.99613}\right) = 748.5471 \text{ V},$$

the 5% of which is approximately 37.5 V.

In one of the approaches to SM capacitor design the variations in energy stored in the MMC arms are considered. In this approach the submodule capacitor is also sized to accommodate the AC grid voltage magnitude variations permissible by energy regulators and network operators [99]. These variations are permissible usually within $\pm 10\%$ [100], [101]. The SM capacitor is then calculated using (5.1) [99].

$$C_{SM} \geq \frac{1.22S}{3\omega V_{dc}\frac{\Delta v_{c_{pk-pk}}}{2}} \tag{5.1}$$

$$= \frac{1.22 \times 2 \times 10^5}{300\pi \times 1500 \times \frac{37.5}{2}} = 9.2051 \text{ mF},$$

whereby ω is the fundamental angular frequency and $\Delta v_{c_{pk-pk}}$ is the peak-to-peak SM capacitor ripple voltage.

The second method approaches the sizing in a similar manner to the first one but results in a smaller capacitor size. The capacitance is given by [102]

$$C_{SM} \geq \frac{2S}{6Nm_a\omega V_c\frac{\Delta v_{c_{pk-pk}}}{2}}\left(1-\left(\frac{m_a\cos\varphi}{2}\right)^2\right)^{\frac{3}{2}} \tag{5.2}$$

$$= \frac{2 \times 2 \times 10^5}{6 \times 2 \times 0.99613 \times 100\pi \times 748.5471 \times \frac{37.5}{2}}\left(1-\left(\frac{0.99613}{2}\right)^2\right)^{\frac{3}{2}} = 4.9483 \text{ mF}$$

whereby the displacement power factor angle φ is zero due to the unity power factor. If a 10% variation in the AC bus voltage is considered the capacitance becomes 6.0231 mF (obtained by substituting 90% of m_a in (5.2)).

Alternatively, the capacitor can be sized to minimize the fundamental frequency ripple voltage, which is the predominant component (followed by the second order harmonic

component) in the ripple content of the SM voltage. Before the SM capacitor and the arm inductor are sized the magnitude and phase of the second order component of the arm current are unknown, hence the arm current with only the DC and the fundamental components can be used to determine the size of the capacitor. Due to the DC component, the charge transfer durations when the capacitor current is negative and when it is positive are not equal. The shorter charge transfer duration is compensated by longer pulse durations as depicted in Figure 5.1. The capacitor current is assumed to be continuous for the shorter charge transfer duration [22]. The charge transferred can be calculated by obtaining the interval during which i_l in (3.13) is approximately continuous, which is done by equating (3.13) to zero but with the ripple ignored (this could also be done using i_u):

$$\frac{1}{3}I_{dc} + \frac{1}{2}I_{ac}\sin(\omega t + \varphi) = 0. \tag{5.3}$$

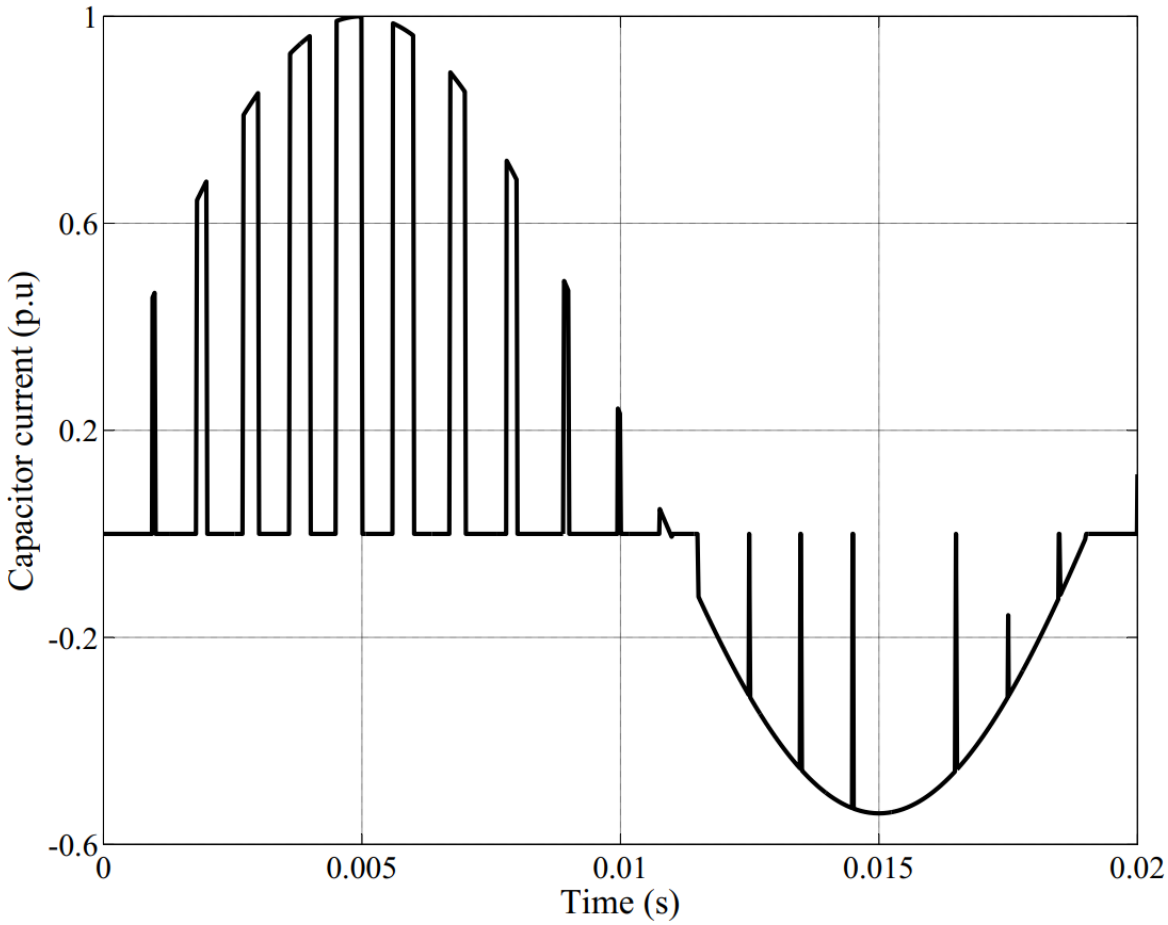

Figure 5.1. Idealized and normalized SM capacitor current depicting unequal charge transfer durations.

Assuming a lossless converter, the DC-link power equals the three-phase side power as follows:

$$\frac{3V_{ac}I_{ac}}{2} = V_{dc}I_{dc}. \tag{5.4}$$

Substituting (3.19) into (5.4) gives (5.5):

$$I_{ac} = \frac{4}{3m_a}I_{dc} \tag{5.5}$$

which makes (5.3) simplify to (5.6), whereby the phase angle φ is zero due to the unity power factor.

$$1 + \frac{2}{m_a}\sin\omega t = 0. \tag{5.6}$$

Equation (5.6) solves to

$$\begin{aligned} \omega t &= \pi + \sin^{-1}\frac{m_a}{2}, 2\pi - \sin^{-1}\frac{m_a}{2} \\ &= \pi + \sin^{-1}\frac{V_{ac}}{V_{dc}}, 2\pi - \sin^{-1}\frac{V_{ac}}{V_{dc}} \\ &= \pi + \sin^{-1}\left(\sqrt{\frac{2}{3}}\frac{V_{LL}}{V_{dc}}\right), 2\pi - \sin^{-1}\left(\sqrt{\frac{2}{3}}\frac{V_{LL}}{V_{dc}}\right) \end{aligned} \tag{5.7}$$

The solution to (5.7) for this design indicates that the time duration for which the capacitor current is approximately continuous is about 33% of the fundamental period.

Equation (5.6) puts an upper limit of 2 p.u. to the modulation index, which means that the condition $V_{dc} \geq V_{ac}$ must be satisfied for this design method to work.

The charge transferred is found by evaluating (5.8). The capacitance is then calculated using (5.9) and for a 5% peak-peak ripple it evaluates to 5.2182 mF. In [22] equation (5.9) is not provided and one has to always solve (5.3) and perform the integral $Q = \left|\int_{t_1}^{t_2} i_l d\tau\right|$ to size the SM capacitor. Reducing the work to equation (5.9) shortens the cumbersome process.

$$Q = \left|\int_{t_1}^{t_2} i_l d\tau\right| = I_{dc}\left|\frac{1}{3}(t_2 - t_1) - \frac{2}{3m_a\omega}(\cos\omega t_2 - \cos\omega t_1)\right|$$

$$= \frac{S}{V_{dc}}\left|\frac{1}{3\omega}\left(2\pi - \sin^{-1}\frac{m_a}{2} - \pi - \sin^{-1}\frac{m_a}{2}\right)\right.$$
$$\left. - \frac{2}{3m_a\omega}\left(\cos\left(2\pi - \sin^{-1}\frac{m_a}{2}\right) - \cos\left(\pi + \sin^{-1}\frac{m_a}{2}\right)\right)\right| \quad (5.8)$$

$$= \frac{S}{3\omega V_{dc}}\left|\pi - 2\sin^{-1}\frac{m_a}{2} - \frac{4}{m_a}\cos\left(\sin^{-1}\frac{m_a}{2}\right)\right|.$$

$$C_{SM}\frac{dv_c}{dt} = i_c \Rightarrow C_{SM}dv_c = i_c dt \Leftrightarrow C_{SM}\Delta v_{c_{pk-pk}} = \left|\int_{t_1}^{t_2} i_c d\tau\right| \approx \left|\int_{t_1}^{t_2} i_l d\tau\right| = Q$$

$$\Rightarrow C_{SM} = \frac{Q}{\Delta v_{c_{pk-pk}}} = \frac{S}{3\omega V_{dc}\Delta v_{c_{pk-pk}}}\left|\pi - 2\sin^{-1}\frac{m_a}{2} - \frac{4}{m_a}\cos\left(\sin^{-1}\frac{m_a}{2}\right)\right| \quad (5.9)$$

Let x be a per unit value obtained as a ratio of the SM peak-peak ripple voltage to the SM capacitor voltage. Based on (3.19) and (4.3),

$$x = \frac{\Delta v_{c_{pk-pk}}}{V_c} = \frac{2N\Delta v_{c_{pk-pk}}}{V_{dc}(1 + m_a)} \Leftrightarrow \Delta v_{c_{pk-pk}} = \frac{V_{dc}(1 + m_a)x}{2N}, \quad (5.10)$$

so that (5.9) becomes

$$C_{SM} = \frac{2NS}{3\omega x V_{dc}^2}\left|\pi - 2\sin^{-1}\frac{m_a}{2} - \frac{4}{m_a}\cos\left(\sin^{-1}\frac{m_a}{2}\right)\right|\frac{1}{1 + m_a}. \quad (5.11)$$

Equations (5.10) and (5.11) apply well to both the HB-MMC and the FB-MMC operating in the linear modulation region. The expression

$$\left|\pi - 2\sin^{-1}\frac{m_a}{2} - \frac{4}{m_a}\cos\left(\sin^{-1}\frac{m_a}{2}\right)\right|\frac{1}{1 + m_a}$$

in (5.11) depends on the modulation index only and its graph is plotted in Figure 5.2, which indicates that the SM capacitor size decreases with an increasing modulation index for an MMC at a given power level. The curve in Figure 5.2 can also be used together with (5.12) to size the SM capacitor.

$$k_{dc} = \frac{3\omega x V_{dc}^2}{2NS}C_{SM} = \left|\pi - 2\sin^{-1}\frac{m_a}{2} - \frac{4}{m_a}\cos\left(\sin^{-1}\frac{m_a}{2}\right)\right|\frac{1}{1 + m_a} \quad (5.12)$$

While Figure 5.2 highlights how the SM capacitor size varies with the modulation index, its curve may not be convenient for SM capacitor sizing at smaller modulation indices. For that

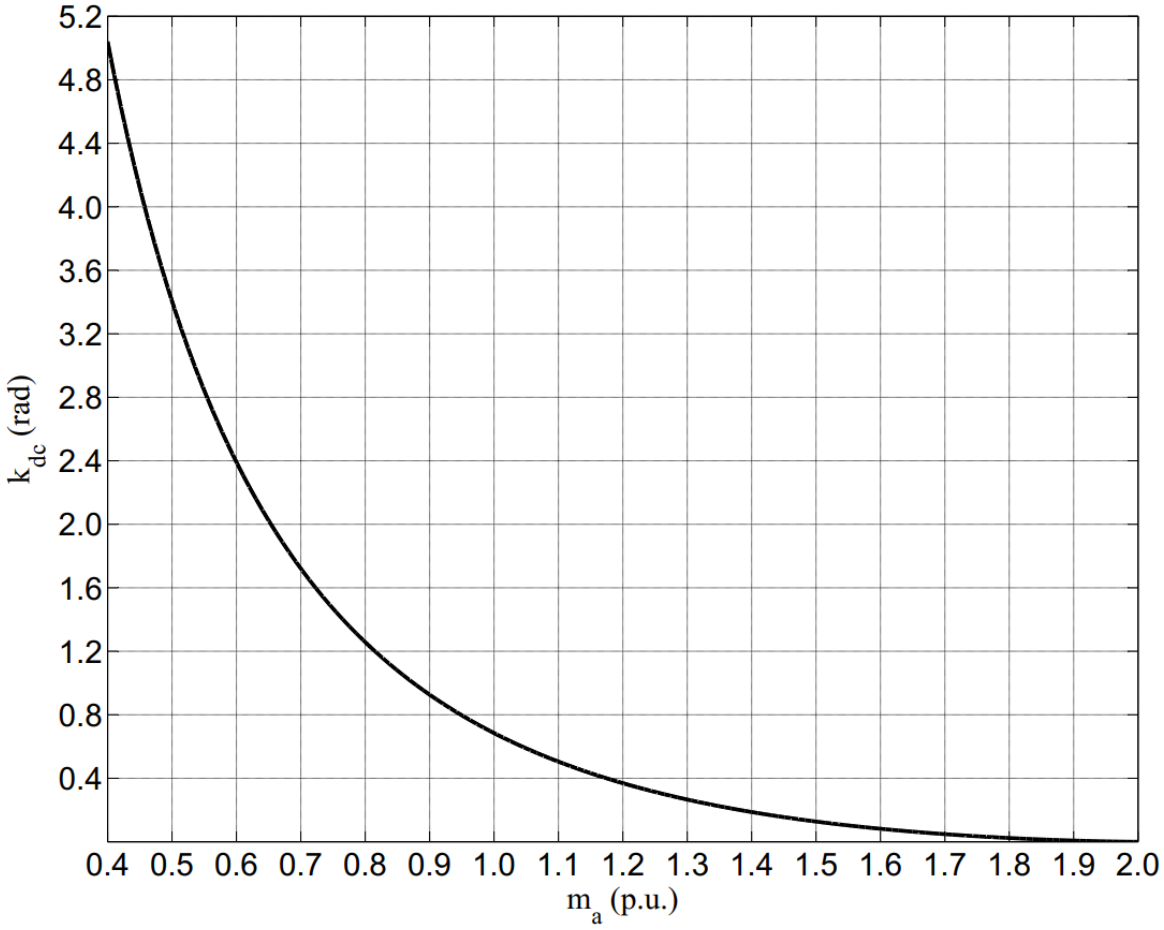

Figure 5.2. SM capacitor design parameter k_{dc} versus modulation index.

reason, V_{dc} in (5.11) is substituted by an equivalent V_{ac}, based on (4.2), and rearranged to formulate (5.13) with the corresponding design curve in Figure 5.3. The curve in Figure 5.3 should give similar results to the curve in Figure 5.2 for the same operating conditions. In Figure 5.3 the maximum point (marked with a red dot) has the value $k_{ac} = 0.86166$ (hereby named $k_{ac,pk}$) and occurs at $m_a = 0.58107$ (hereby named $m_{a,pk}$).

$$k_{ac} = m_a^2 k_{dc} = \frac{6\omega x V_{ac}^2}{NS} C_{SM} = m_a^2 \left| \pi - 2\sin^{-1}\frac{m_a}{2} - \frac{4}{m_a}\cos\left(\sin^{-1}\frac{m_a}{2}\right) \right| \tag{5.13}$$

For example, for the required line-line voltage of 915 V, m_a is 0.9961, which gives $k_{ac} \approx 0.68$. Using (5.12) the SM capacitor works out as

$$C_{SM}|_{0.9961} = \frac{NSk_{ac}}{6\omega x V_{ac}^2} = \frac{2 \times 200 \times 10^3 \times 0.68}{6 \times 100\pi \times 0.05 \times \left(\sqrt{\frac{2}{3}} \times 915\right)^2} = 5.1707 \text{ mF},$$

which is close to 5.2182 mF calculated before.

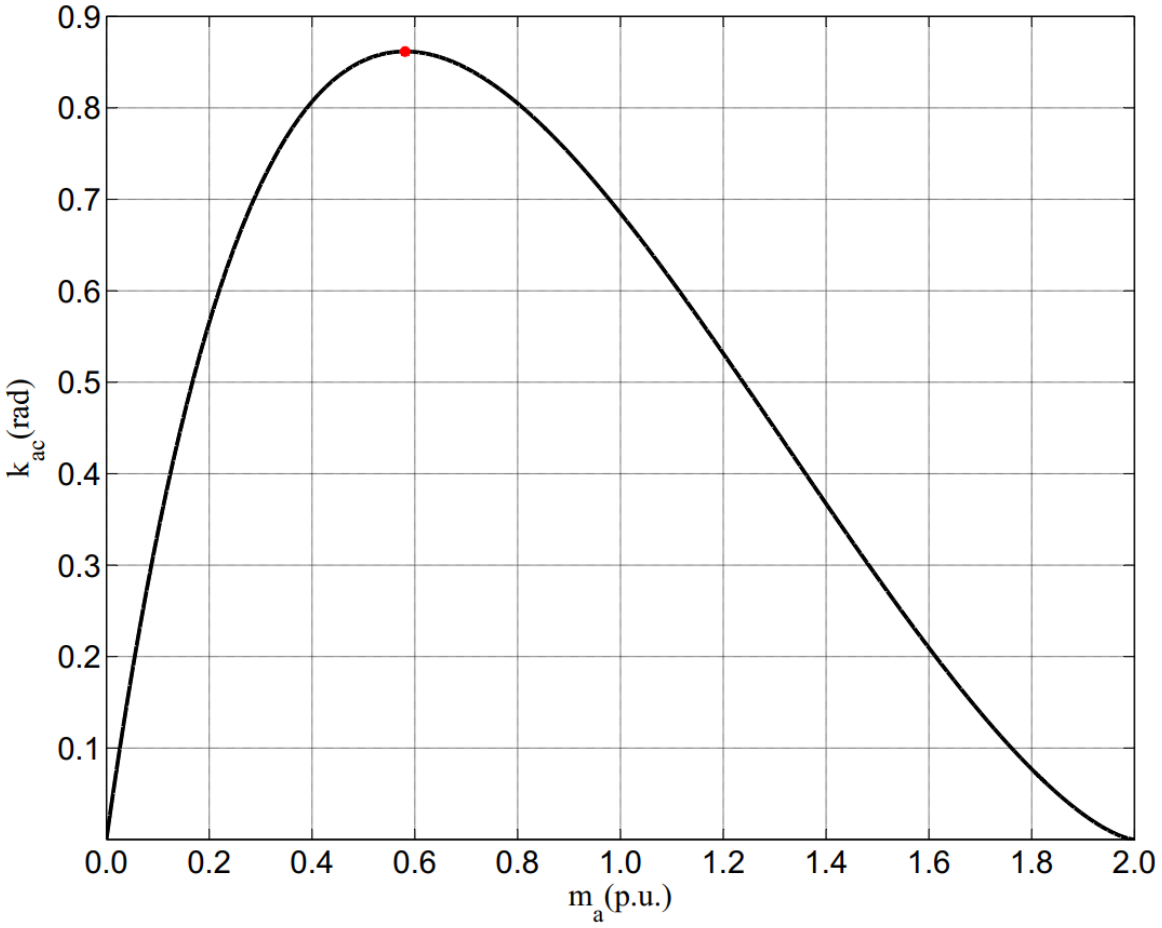

Figure 5.3. SM capacitor design parameter k_{ac} versus modulation index.

If the SM capacitor were to be designed to also accommodate variations in the AC-side voltage, the resulting variations in power would also have to be considered. For an inverter, since it supplies active power and it is synchronized to the grid, $S \propto V_{ac}^2$, which makes the ratio S/V_{ac}^2 in (5.13) stay constant irrespective of the variations in V_{ac}. That makes k_{ac} the only variable in (5.13), which means for an inverter the worst-case scenario to size the SM capacitor for AC-side voltage variations depends on whether the nominal modulation index is to the left or the right of $m_{a,pk}$. If the nominal modulation index is to the left of $m_{a,pk}$, the SM capacitor should be sized for when V_a surges since this makes m_a increase hence increased k_{ac}, which increases the SM capacitor size according to (5.13). On the other hand, if the nominal modulation index is to the right of $m_{a,pk}$, the SM capacitor should be sized for when V_a dips since this makes m_a decrease hence increased k_{ac}. For example, if the above design was for an inverter and $\pm 10\%\, V_{ac}$ must be accommodated, the worst-case

scenario would be when V_{ac} dips by 10% hence m_a would scale down to 90% of the nominal value i.e. $0.9 \times 0.9961 = 0.8965$ which gives $k_{ac} \approx 0.75$. The SM capacitor would then work out to

$$C_{SM}|_{invrt\ @\ 0.8965} = \frac{k_{ac}|_{0.8965}}{k_{ac}|_{0.9961}} C_{SM}|_{0.9961} = \frac{0.75}{0.68} \times 5.1707 = 5.7030 \text{ mF}.$$

For a rectifier, the AC-side voltage variations would not affect the power delivered by the converter since it maintains the DC-side voltage irrespective of the AC-side voltage variations. That means, according to (5.12) and Figure 5.2, the worst-case scenario for sizing a SM capacitor for a rectifier is when the AC-side voltage dips below its nominal value. If the above design were for a rectifier, the SM capacitor would work out to

$$C_{SM}|_{rectf\ @\ 0.8965} = \frac{NSk_{ac}}{6\omega x V_{ac}^2} = \frac{2 \times 200 \times 10^3 \times 0.75}{6 \times 100\pi \times 0.05 \times \left(0.9 \times \sqrt{\frac{2}{3}} \times 915\right)^2} = 7.0407 \text{ mF}.$$

For a bidirectional converter, the larger SM capacitor design between that of an inverter mode and that of a rectifier mode would have to be chosen. In the above case the SM capacitor for a rectifier mode would suit the bidirectional operation design.

Another alternative, hereby proposed, also using the fundamental arm current component to approximate the ripple, is to express the capacitor ripple voltage in its Fourier components, and realize that the fundamental component is dominant. The n^{th} harmonic ripple voltage in a SM capacitor is given by [90]

$$\Delta v_{c,n}(t) = \frac{i_{c,n}(t)}{jn\omega C_{SM}} \tag{5.14}$$

and the total SM capacitor ripple voltage is given by

$$\begin{aligned} \Delta v_c(t) &= \sum_{n=1}^{\infty} \Delta v_{c,n}(t) = \frac{1}{j\omega C_{SM}} \sum_{n=1}^{\infty} \frac{i_{c,n}(t)}{n} \\ &= \frac{1}{j\omega C_{SM}} \left(i_{c,1}(t) + \frac{i_{c,2}(t)}{2} + \frac{i_{c,4}(t)}{4} + \cdots \right). \end{aligned} \tag{5.15}$$

The second most significant component after the fundamental component is the second order component, with the rest of the harmonics being significantly low. Since even the second order component is only a fraction of the fundamental component, the ripple can be approximated by the fundamental component alone as in (5.16). The SM capacitor works out as 3.7872 mF and it is adopted for this design. If for example the second order SM capacitor current component is 25% of its fundamental component (or equivalently, the second order component of the arm current is equal to 25% of the fundamental component of the arm current), the second order capacitor ripple voltage, according to (5.14), would be limited to $200 \times 10^3/\left(8\sqrt{24} \times 100\pi \times 915 \times 3.7872 \times 10^{-3}\right) = 4.6875$ V, which is about only 0.6% of the SM capacitor voltage. With the use of closed loop control to suppress the second order component (and other low frequency harmonics if necessary) in the arm current, the second order component becomes even a smaller percentage of the fundamental component flowing in the arm. This further justifies the use of only the fundamental component current to size the SM capacitor.

$$\begin{aligned} \Delta v_c(t) &\approx \frac{i_{c,1}(t)}{j\omega C_{SM}} = \frac{\delta(t) i_{ac}(t)/2}{j\omega C_{SM}} \\ \Rightarrow \Delta v_{c_{pk-pk}} &\approx \frac{I_{c,1}}{\omega C_{SM}} = \frac{DI_{ac}}{2\omega C_{SM}} \\ \Rightarrow C_{SM} &= \frac{DI_{ac}}{2\omega \Delta v_{c_{pk-pk}}} = \frac{DS}{\sqrt{6}\omega V_{LL} \Delta v_{c_{pk-pk}}} = \frac{S}{\sqrt{24}\omega V_{LL} \Delta v_{c_{pk-pk}}} \end{aligned} \tag{5.16}$$

If $\pm 10\%$ V_{ac} must be accommodated, then according to (5.16) the SM capacitor to handle the worst-case scenario is $3.7872 \times 10^{-3}/0.9 = 4.2080$ mF.

A possible reason for the significant difference between the values out of the last two methods is the assumption made in the former method about the continuity of the capacitor current during the shorter charge transfer duration.

5.4 ARM INDUCTOR SIZING

To avoid resonance of the second order harmonic between the SM capacitors and the arm inductor, the following condition must be satisfied, which also ensures suppression of all other harmonics [15]:

$$L_{arm}C_{SM} > \frac{3N + 2m_a^2 N}{48\omega^2} \tag{5.17}$$

$$\Rightarrow L_{arm} > \frac{2(3 + 2 \times 0.9961^2)}{48 \times (100\pi)^2 \times 3.7872 \times 10^{-3}} = 555.6308\ \mu\text{H}.$$

However, the effective inductance as in Figure 3.3 of the converter model has an upper limit in order to increase the operation range of the rectifier [93], [103]. With the parasitic resistances ignored, the DC link voltage must be greater than the line-line peak of v_{refl} in Figure 3.3, i.e.

$$V_{dc} > \sqrt{3\left(E_q^2 + \left(\omega L_{total} I_q\right)^2\right)} \tag{5.18}$$

whereby $L_{total} = L_{grid} + L_{filter} + 0.5L_{arm}$. This also means that this increased operation range cannot be enjoyed by overmodulated converters operating above $m_a = 2/\sqrt{3} \approx 1.15$.

The value of I_q can be found, using the amplitude-invariant abc-frame to dq-frame transformation, by equating the AC-side power and the DC-side power, assuming insignificant system losses.

$$P_{ac} = P_{dc} \tag{5.19}$$

$$\Rightarrow \sqrt{3}E_{RMS}I_{ac,RMS} = 200\ \text{kW} \Longrightarrow I_{ac,RMS} = \frac{200\ 000}{\sqrt{3} \times 915} = 126.1968\ \text{A}$$

$$\Longrightarrow I_q = \sqrt{2}I_{ac,RMS} = 178.4692\ \text{A},$$

Then L_{total} in (4.3) is calculated as follows:

$$L_{total} < \frac{\sqrt{\frac{V_{dc}^2}{3} - {E_q}^2}}{\omega I_q} = \frac{\sqrt{\frac{1500^2}{3} - \left(915\sqrt{\frac{2}{3}}\right)^2}}{100\pi \times 178.4692} = 7.8121 \text{ mH}$$

It is advised that the arm inductance should be selected to be at least three times the resonant inductance [15]:

$$L_{arm} \geq 3 \times 555.6308 \text{ µH} = 1.6669 \text{ mH}$$

The arm inductor parasitic resistance is set to 0.5 mΩ.

With the SM capacitor and the arm inductor sized, the magnitude and phase of the second order component of the circulating current can be calculated using (4.18) [90]. The magnitude is obtained as 26.8531 A and the phase is obtained as -90°. Compared to the fundamental current component flowing in the arm, the second order current component is $100\% \times I_2/(0.5I_{ac}) = 100\% \times 26.8535/(0.5 \times 178.4692) = 30.1\%$.

$$I_2 = \frac{\sqrt{(A\cos\varphi + B)^2 + (A\sin\varphi)^2}}{1 - \frac{N}{16\omega^2 C_{SM} L_{arm}} - \frac{m_a^2 N}{24\omega^2 C_{SM} L_{arm}}} \tag{5.20}$$

$$\theta_2 = \tan^{-1}\frac{A\cos\varphi + B}{-A\sin\varphi}$$

whereby

$$A = \frac{3m_a N I_{ac}}{64\omega^2 C_{SM} L_{arm}}, \quad B = -\frac{N m_a^2 I_{dc}}{48\omega^2 C_{SM} L_{arm}}$$

5.5 CHAPTER SUMMARY

In this chapter the circuit filters, namely the SM capacitor and the arm inductor, were sized. A graphical method for easy sizing of the SM capacitor, based on a SM capacitor sizing method in literature, was developed. A simple equation was also developed for the same method, which shortens the sizing process which otherwise involves a solution to a trigonometric equation and performing an integral of a trigonometric equation every time

the sizing is done. A new method for SM capacitor sizing was proposed. This method is simple and straightforward, and it achieves smaller SM capacitor size than existing methods in the literature while meeting SM capacitor voltage ripple suppression specifications. In this design the proposed method was compared to three existing methods, which clearly oversize the SM capacitor. The proposed SM capacitor design method is part of the contribution of this dissertation.

CHAPTER 6 CONTROL OF THE MODULAR MULTILEVEL CONVERTER

6.1 CHAPTER OBJECTIVES

This chapter intends to design the various control loops of the MMC. The control system involves the current controller, the SM capacitor voltage balancing controller, and the DC bus voltage controller. The overall control scheme is illustrated in Figure 6.1.

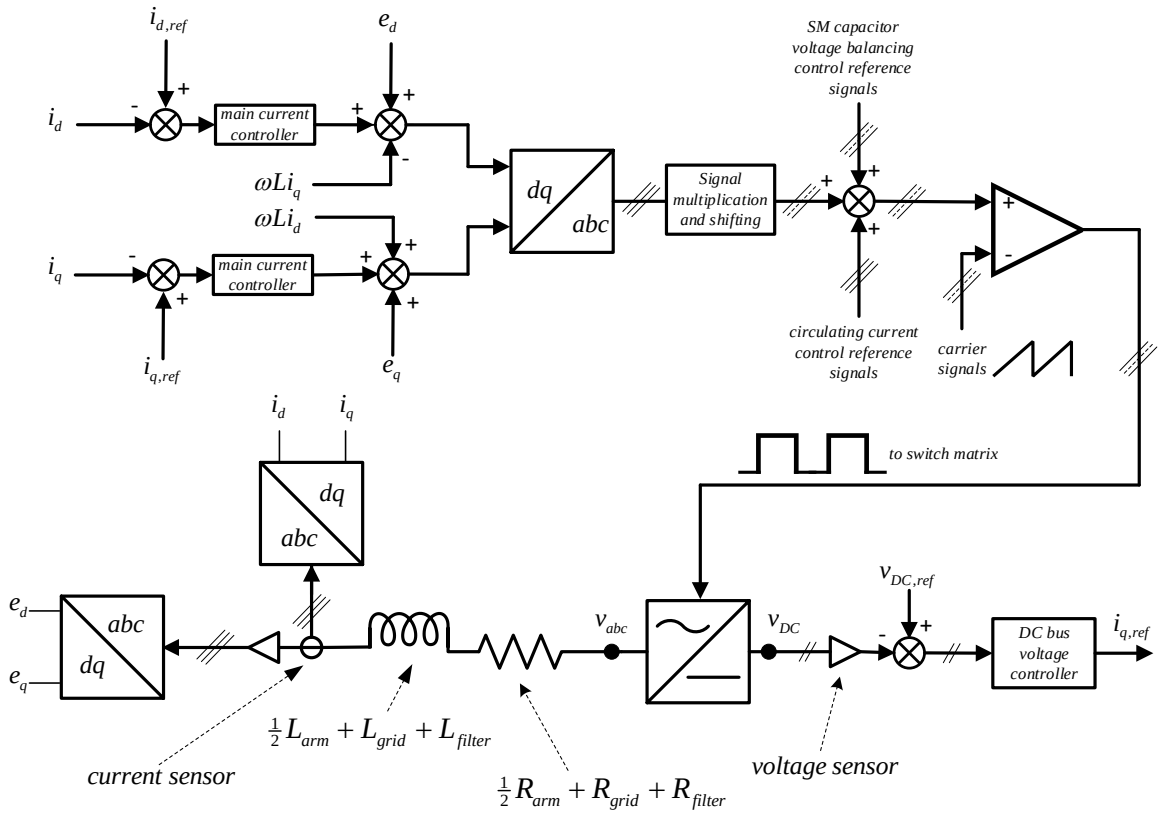

Figure 6.1. Overall control scheme.

6.2 CURRENT CONTROLLER

The current controller is designed to modify the frequency response of (3.36). The Bode plots of this transfer function appear in Figure 6.2. The design process assumes an ideal current sensor of unity gain and zero delay. A practical sensor may require its transfer function to be included in the control loop.

The crossover frequency is chosen to be around 115 Hz for a fast enough [inner] current loop that allows for independent design of the [outer] voltage loop controller. The gain and phase at 115 Hz are -2.08 dB and -110° as seen in Figure 6.2. For elimination of the steady-state error a PI-based controller is required, which requires that the phase margin (PM) of the compensated system should be less than $180° - 110° = 70°$. A PM of 65° is chosen, which makes the phase of the controller $65° + 110° - 180° = -5°$. The required controller must then have a gain of 2.08 dB and a phase of $-5°$. A traditional PI controller of the form

$$G_c(s) = K_c\left(1 + \frac{1}{\tau_c s}\right) \tag{6.1}$$

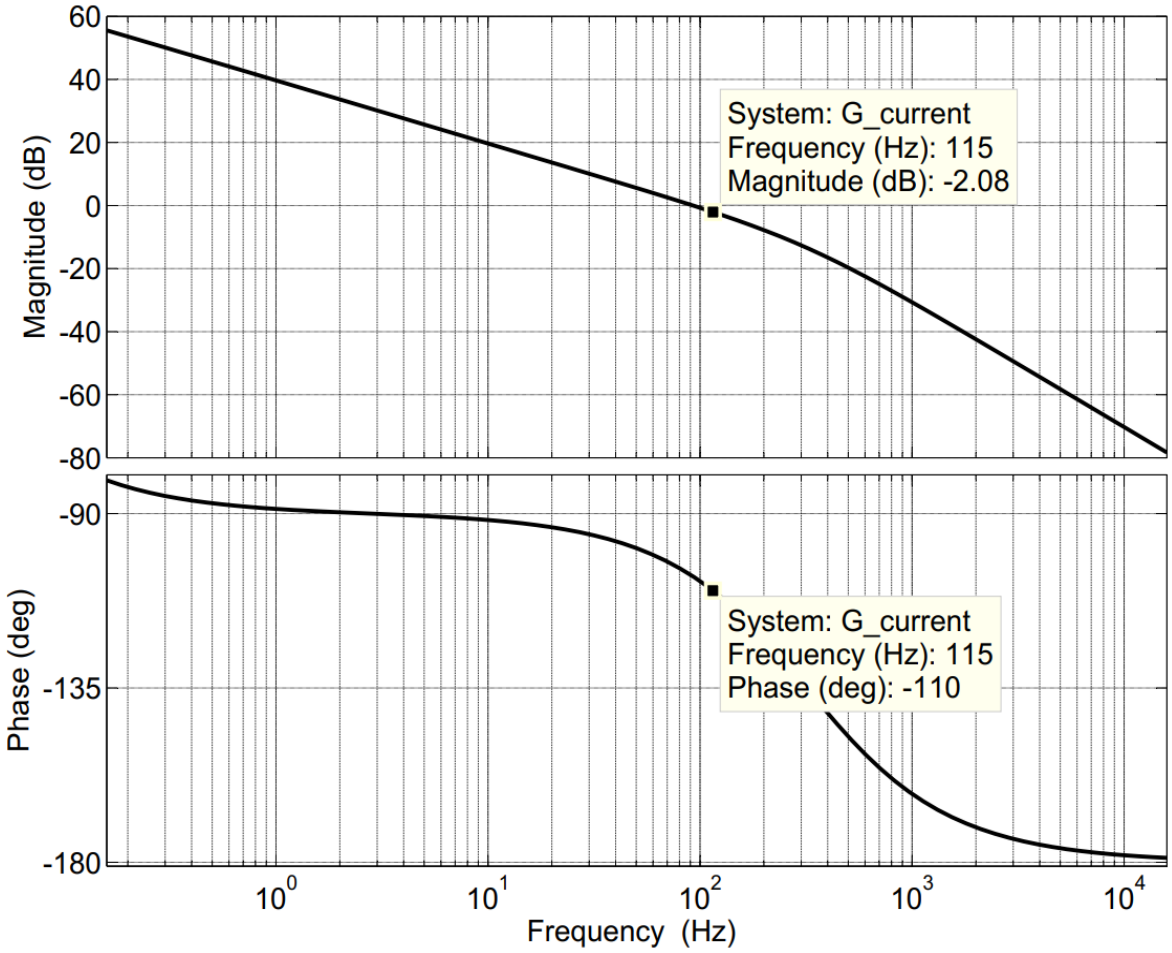

Figure 6.2. Bode plots of the current loop transfer function.

is used. Substituting $s = j\omega$ gives

$$G_c(j\omega) = K_c\left(1 + \frac{1}{j\tau_c\omega}\right) \tag{6.2}$$

$$\Longrightarrow \varphi_c = \angle G_c(j\omega) = -\tan^{-1}\left(\frac{1}{\tau_c\omega}\right)$$

$$\Longrightarrow \tau_c = \frac{-1}{\omega\tan(\varphi_c)}$$

$$= \frac{-1}{230\pi\tan\left(-5°\right)}$$

$$= 15.8187 \times 10^{-3}\text{s}$$

$$(6.2) \Longrightarrow |G_c(j\omega)| = K_c\left|1 + \frac{1}{j\tau_c\omega}\right|$$

$$= K_c\sqrt{1+\frac{1}{\tau_c^2\omega^2}}$$

$$\Longrightarrow K_c = \frac{|G_c(j\omega)|}{\sqrt{1+\frac{1}{\tau_c^2\omega^2}}}$$

$$= \frac{10^{\frac{2.08}{20}}}{\sqrt{1+\frac{1}{(15.8187\times 10^{-3}\times 230\pi)^2}}}$$

$$= 1.2657 \text{ p.u.}$$

The controller is then

$$G_c(s) = 1.2657\left(1+\frac{1}{15.8187\times 10^{-3}s}\right).$$

The Bode plots of G_c appear in Figure 6.3 and those of a compensated loop appear in Figure 6.4. The closed loop is given by

$$G_{curr,closed}(s) = \frac{G_{curr}(s)G_c(s)}{1+G_{curr}(s)G_c(s)}$$

$$= \frac{\tau_c s+1}{\frac{T_{sw}\tau_c L}{2K_c}s^3+\frac{\tau_c R}{K_c}\left(\frac{T_{sw}}{2}+\frac{L}{R}\right)s^2+\tau_c\left(\frac{R}{K_c}+1\right)s+1} \quad (6.3)$$

and its Bode plots are shown in Figure 6.5.

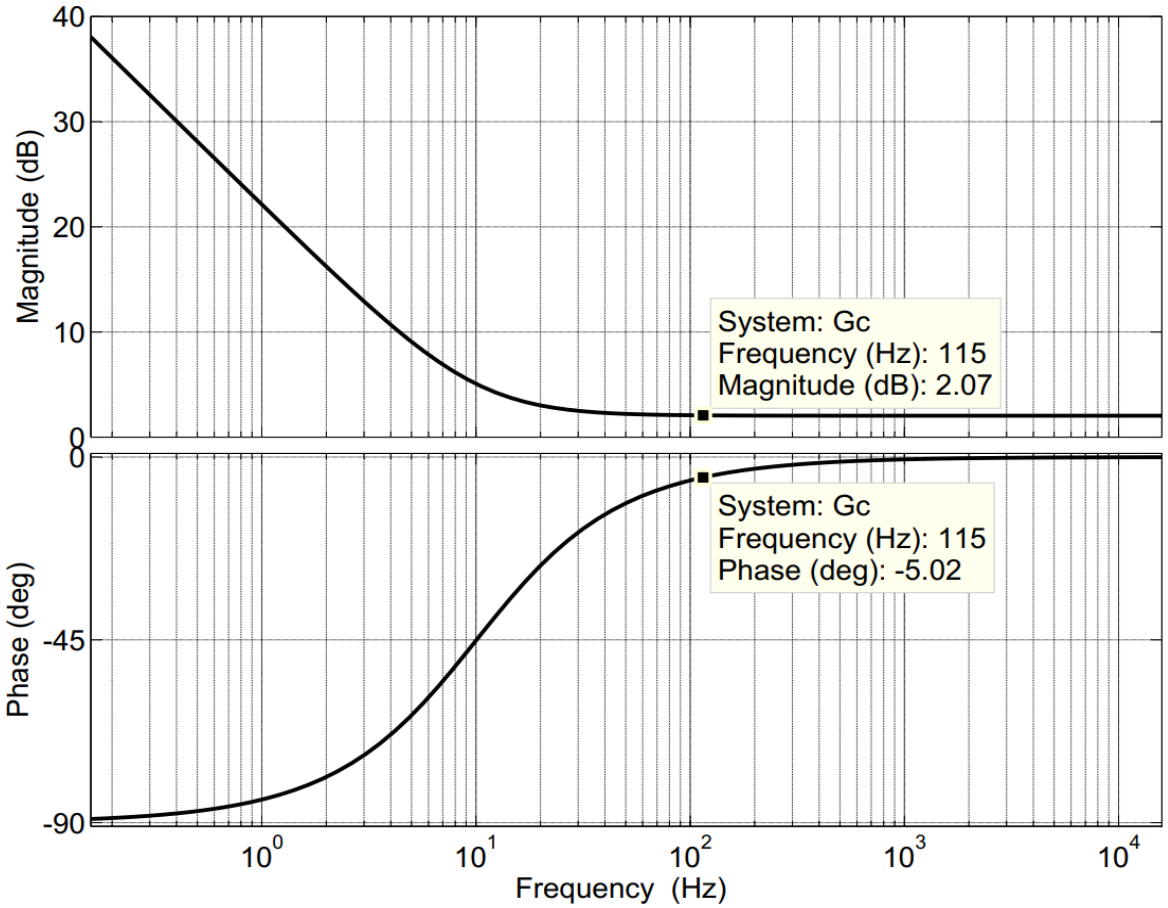

Figure 6.3. Bode plots of the current controller.

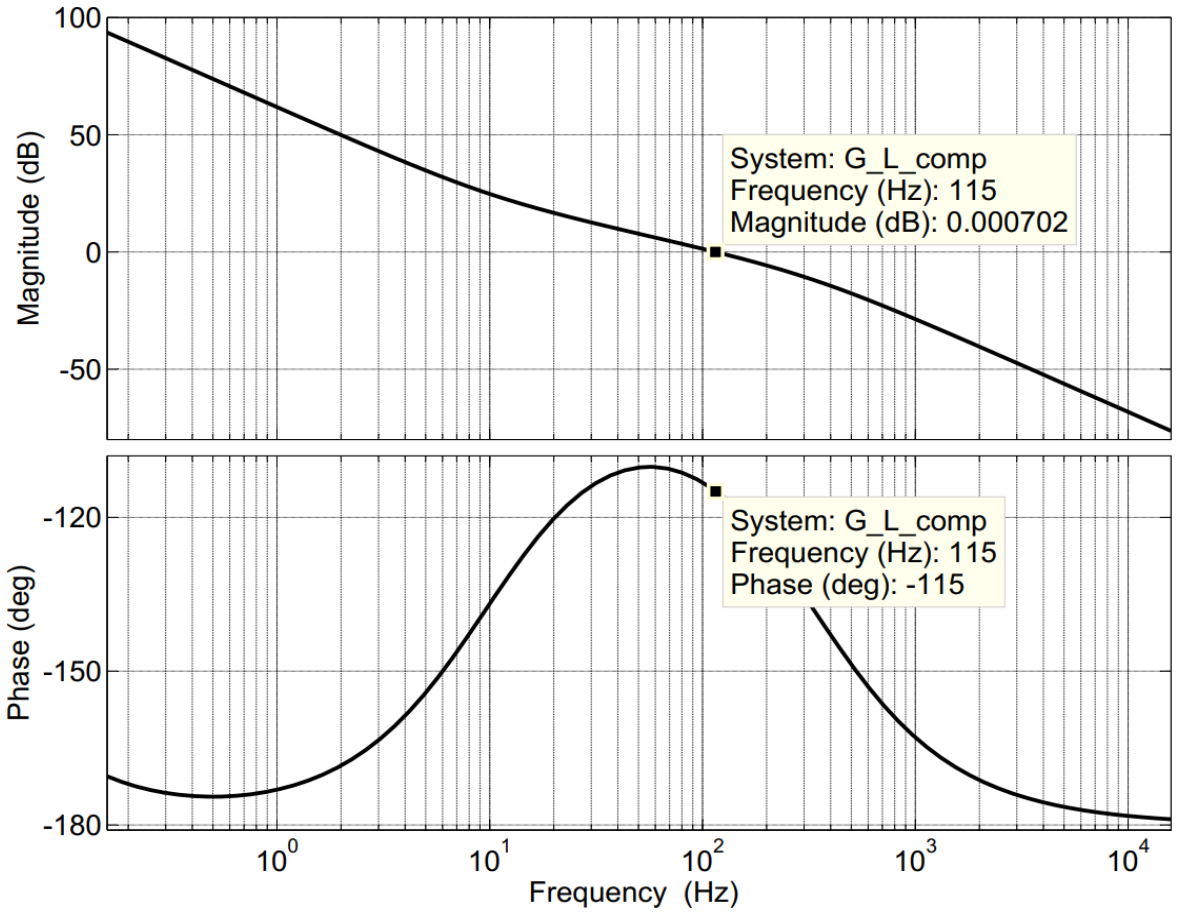

Figure 6.4. Bode plots of the compensated current loop.

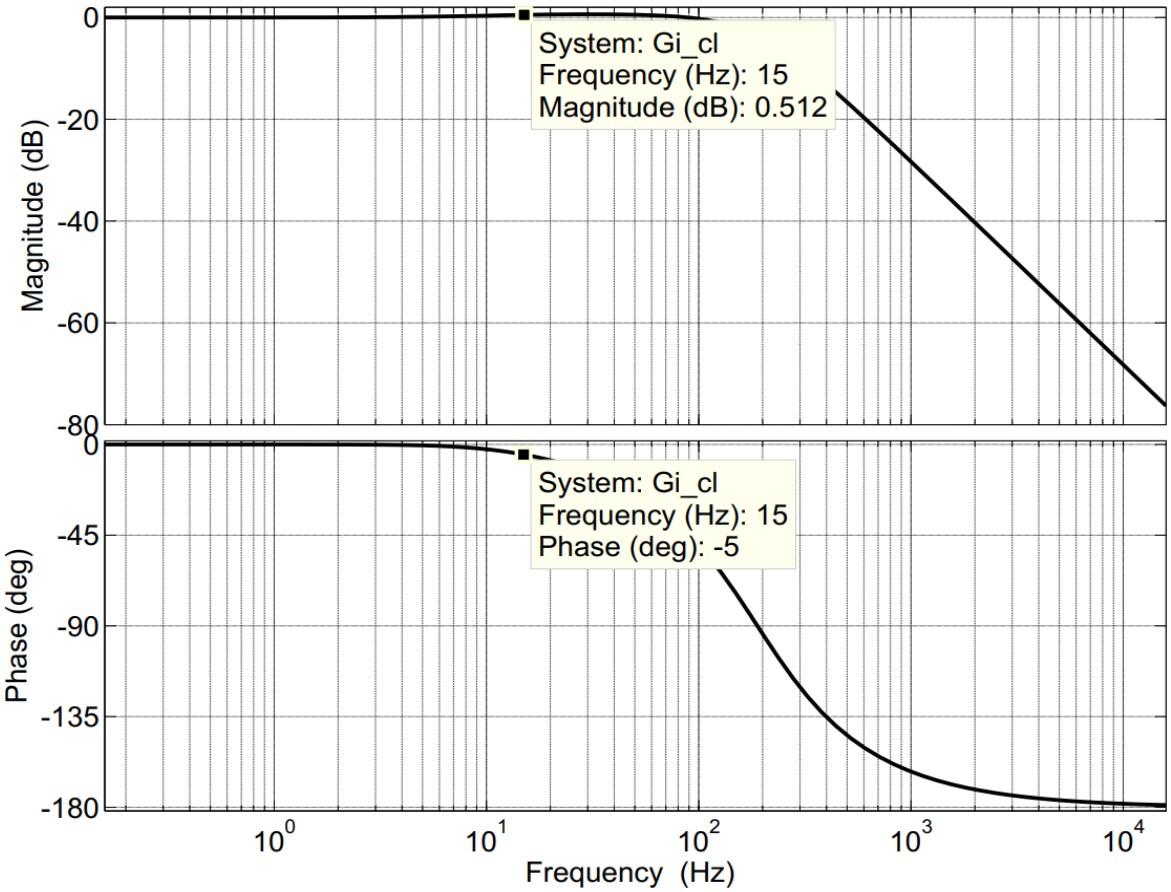

Figure 6.5. Bode plots of the closed current loop.

6.3 DC BUS VOLTAGE CONTROLLER

For an outer voltage loop to be designed independent of the inner current loop, the gain and phase of the compensated inner loop at the crossover frequency of the outer loop must be 0 dB and 0°, respectively. For this design, a crossover frequency of 15 Hz is chosen. In Figure 6.5, the gain is 0.512 dB, and the phase is $-5°$, at 15 Hz. This requires the voltage loop transfer function to be multiplied by the closed current loop transfer function for the voltage loop controller to be adequately designed. This product is expressed in (6.4) and its Bode plots are shown in Figure 6.6. The gain and phase at the crossover frequency are -2.67 dB and $-95°$, respectively. A PI controller is designed, with a PM of 67°, which is chosen for a good balance between an overshoot and the settling time of a step response.

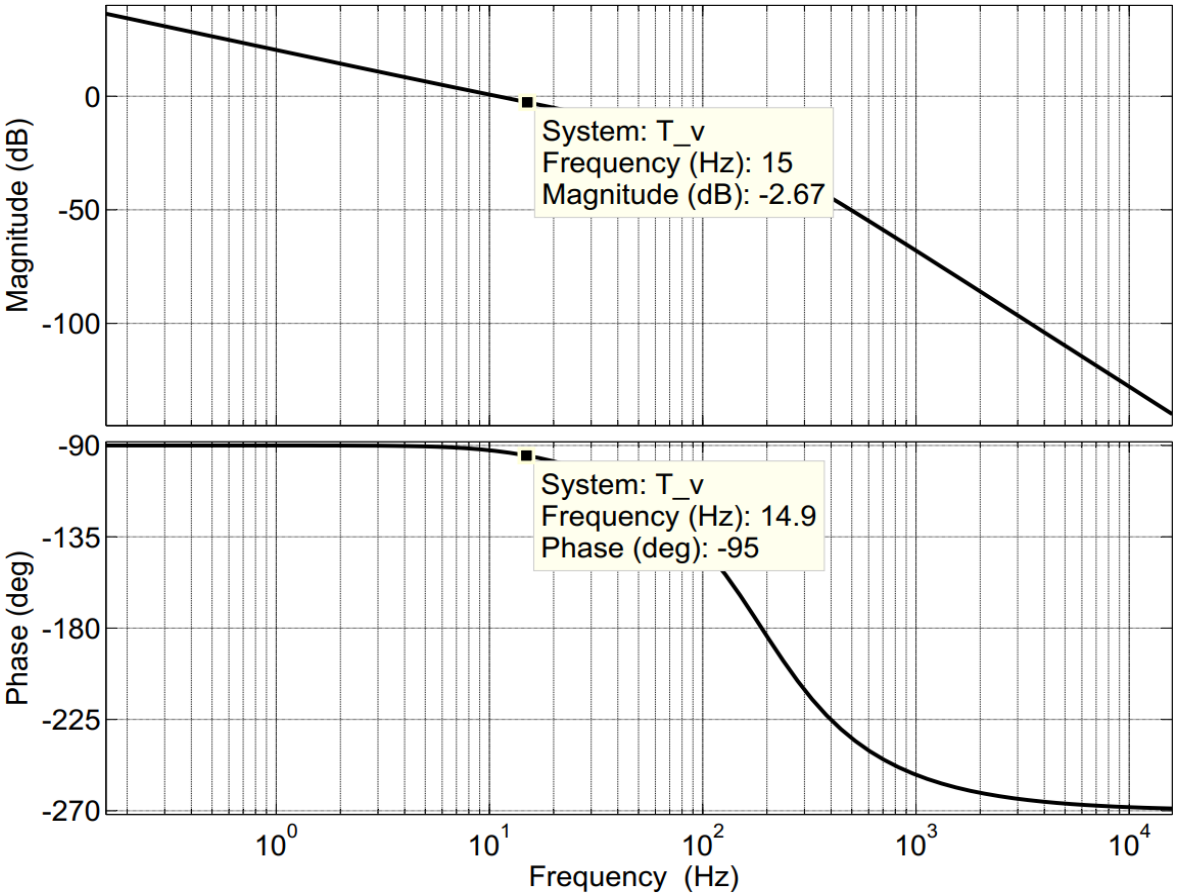

Figure 6.6. Bode plots of the voltage loop.

$$G_{volt}(s) = G_{curr,closed}(s) \times \frac{V_{dc}(s)}{I_q(s)} = G_{curr,closed}(s) \times \frac{3E_q}{2V_{dc,ref}C_{eq}s}$$

$$= \frac{\frac{3E_q}{2V_{dc,ref}C_{eq}}(\tau_c s + 1)}{s\left(\frac{T_{sw}\tau_c L}{2K_c}s^3 + \frac{\tau_c R}{K_c}\left(\frac{T_{sw}}{2} + \frac{L}{R}\right)s^2 + \tau_c\left(\frac{R}{K_c} + 1\right)s + 1\right)} \quad (6.4)$$

Following the same design procedure as that for the current controller, the DC bus voltage controller is obtained as

$$G_v(s) = K_v\left(1 + \frac{1}{\tau_v s}\right) = 1.2933\left(1 + \frac{1}{32.6552 \times 10^{-3}s}\right) \quad (6.5)$$

and its Bode plots appear in Figure 6.7. The Bode plots of the compensated voltage loop appear in Figure 6.8.

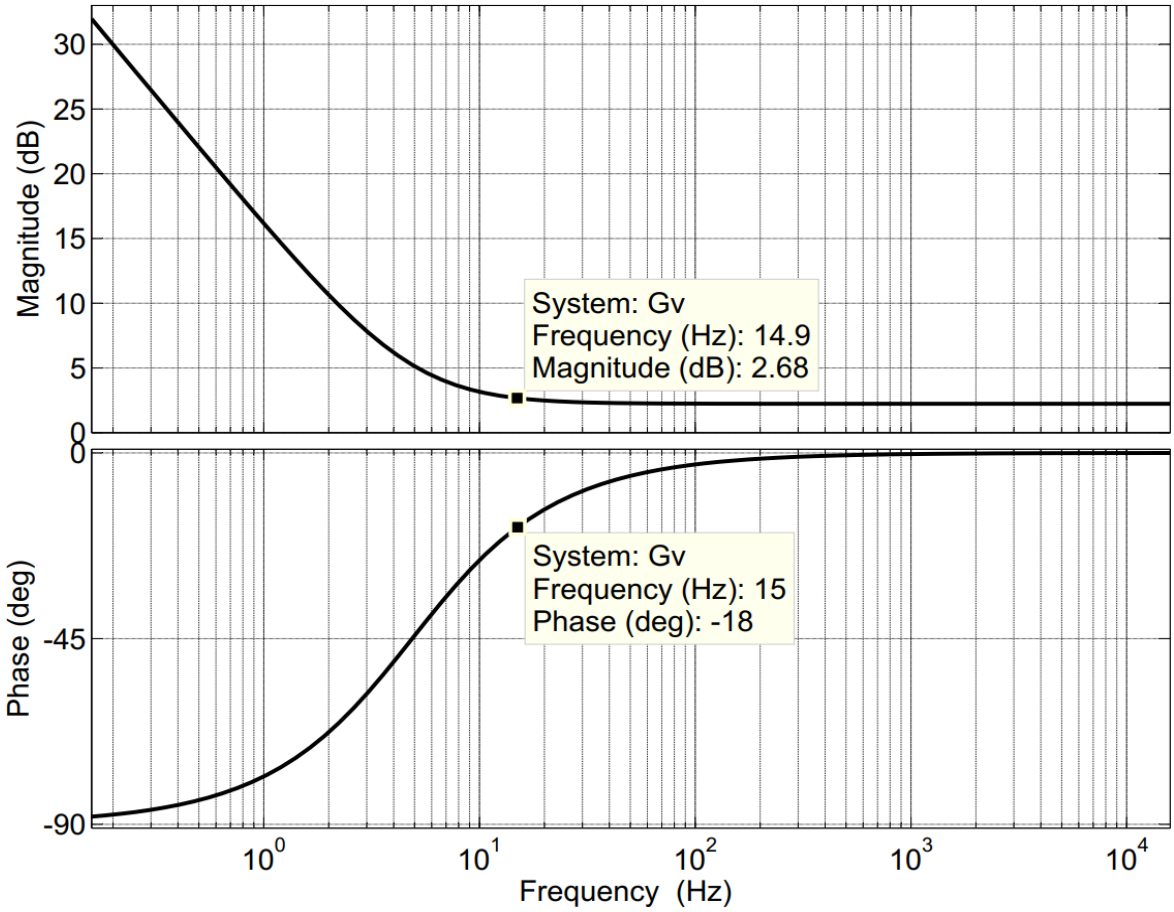

Figure 6.7. Bode plots of the voltage controller.

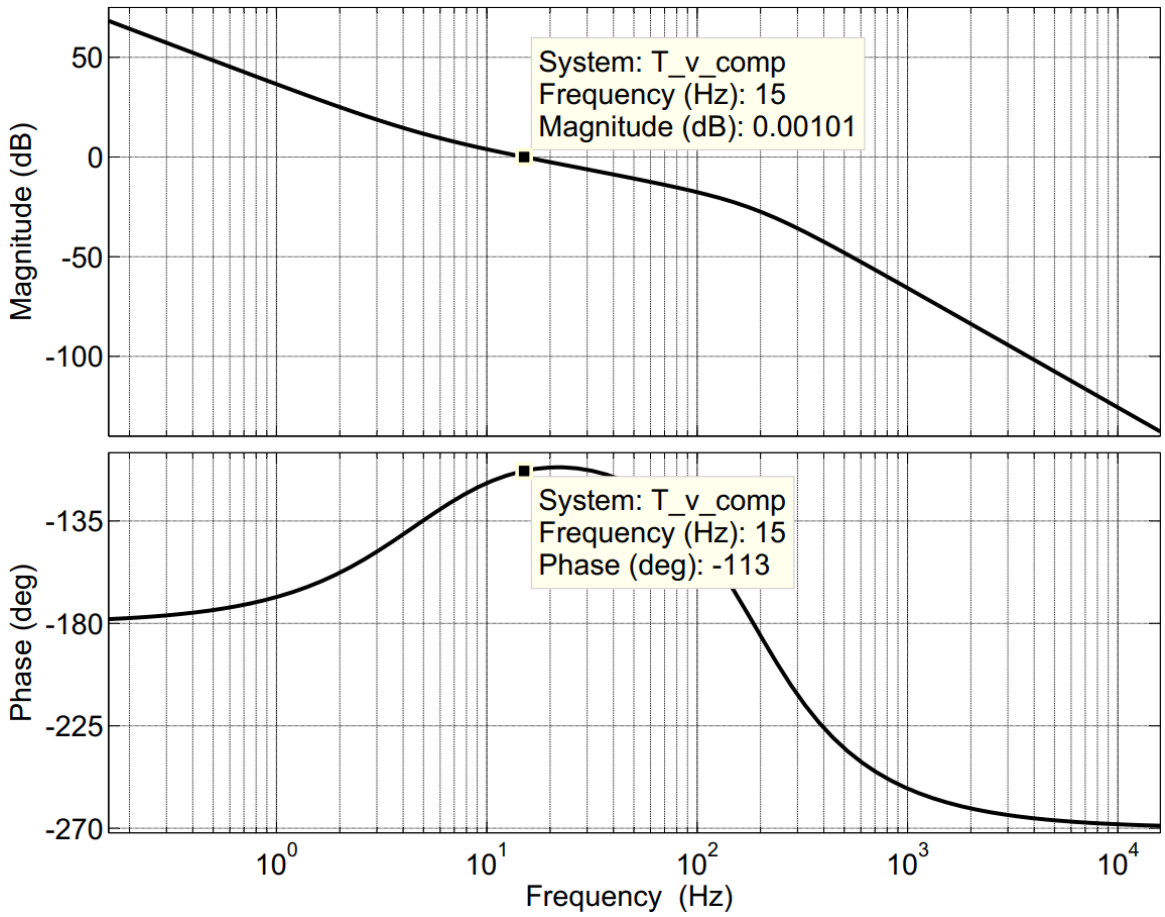

Figure 6.8. Bode plots of the compensated voltage loop.

Although the controller in (6.5) is designed based on a fixed DC bus reference voltage, according to (3.39), it is robust enough to track step changes around the reference value. In the simulation of Figure 6.9 the reference DC bus voltage was changed from 1500 V to 1725 V (= 15% step). The rise time was about 13 ms (about 0.65 times the fundamental period), the overshoot was about 4.5%, and the settling time was about 40 ms (about 2 times the fundamental period).

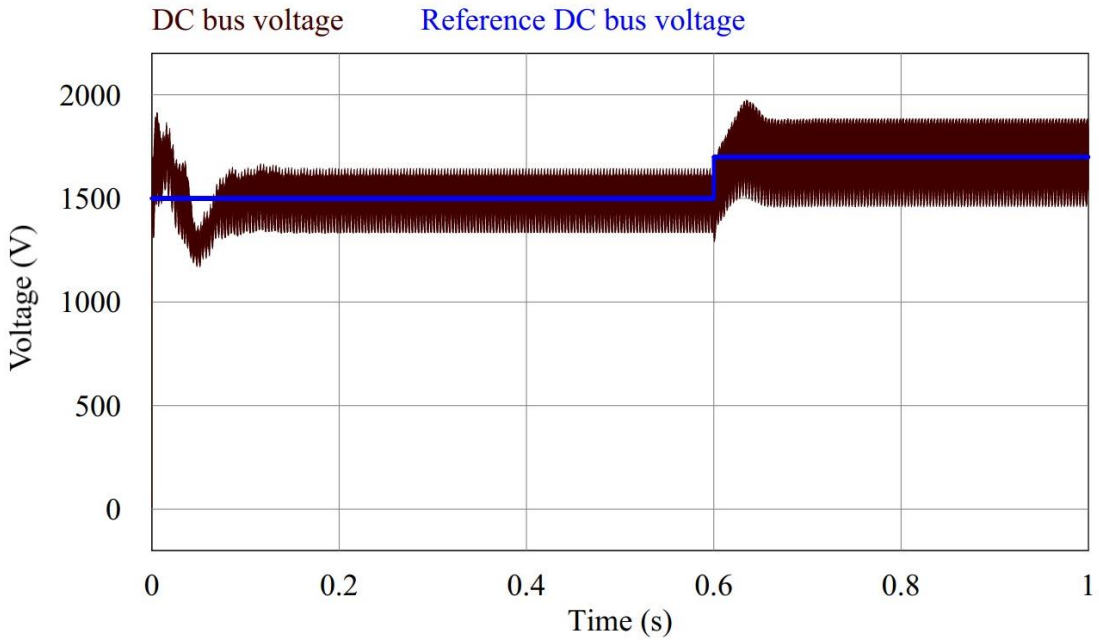

Figure 6.9. Set-point step-change tracking of the DC bus voltage controller.

6.4 LEG AVERAGE VOLTAGE CONTROLLERS

With the transfer functions $H_{cb}(s)$ and $H_{vb}(s)$ found, the step-by-step controller design for the loops in Figure 3.4 can be carried out. Both controllers are designed for a phase margin of 45° at a crossover frequency of 20 Hz (simultaneously designed). They are both PI controllers in order to drive the steady-state errors to zero. For simulation purposes the sensors are assumed ideal, so $H_{sen,cb}$ and $H_{sen,vb}$ are unity gains. The amplitude of the carrier signal V_{car} in G_{PWM} is set to 750 V.

According to Figure 2.6, the error fed to the inner loop controller of Figure 3.4 is given by (6.6) [22], [30 - 34], [104]. This is equivalent to multiplying H_{cb} by -1. Thus, the inner loop controller is designed based on the open loop $H_{open,cb}(s) = -H_{cb}(s)G_{PWM}(s)$, whose Bode plots appear in Figure 6.7.

$$e_{curr,bal}(t) = i_{circ}(t) - i^{*}_{circ}(t) \tag{6.6}$$

Accordingly, the inner loop controller is given by (6.7) and the compensated loop appears in Figure 6.11.

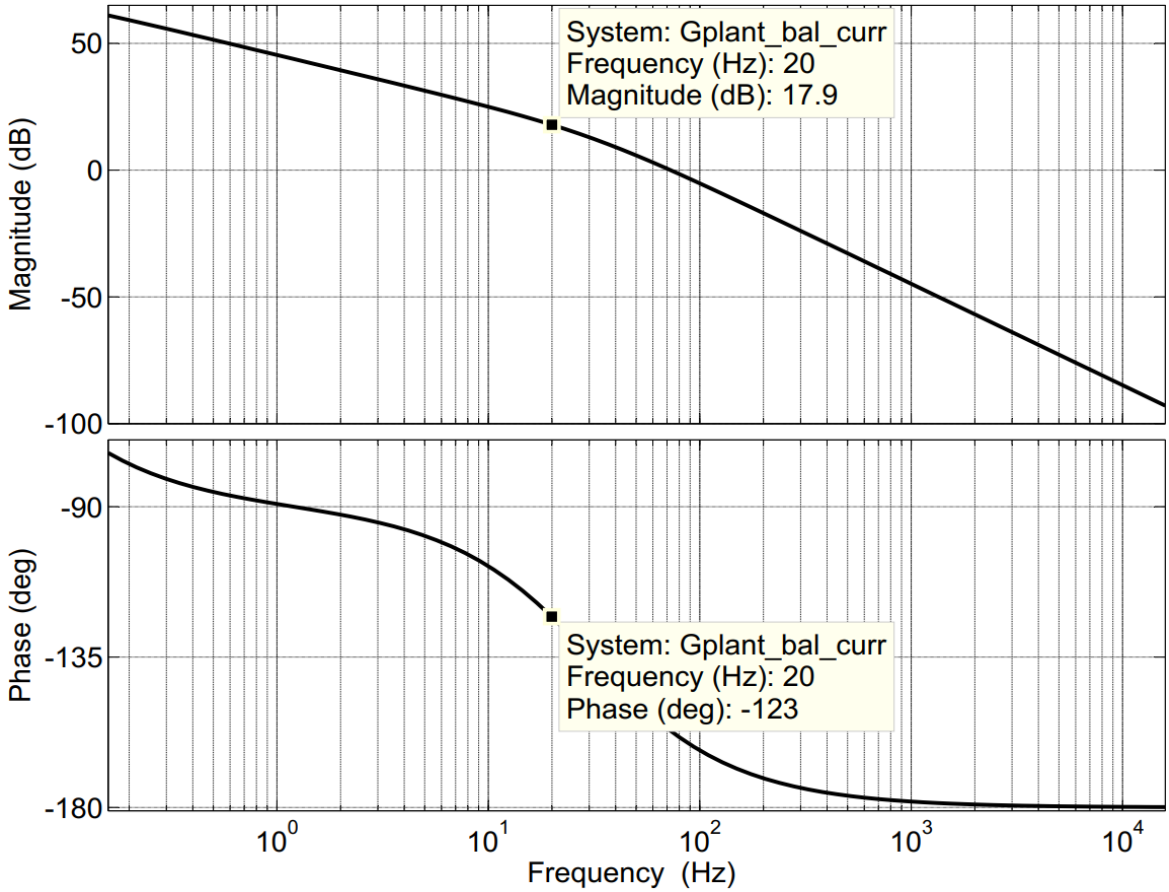

Figure 6.10. Bode plots of the open leg average voltage control inner loop.

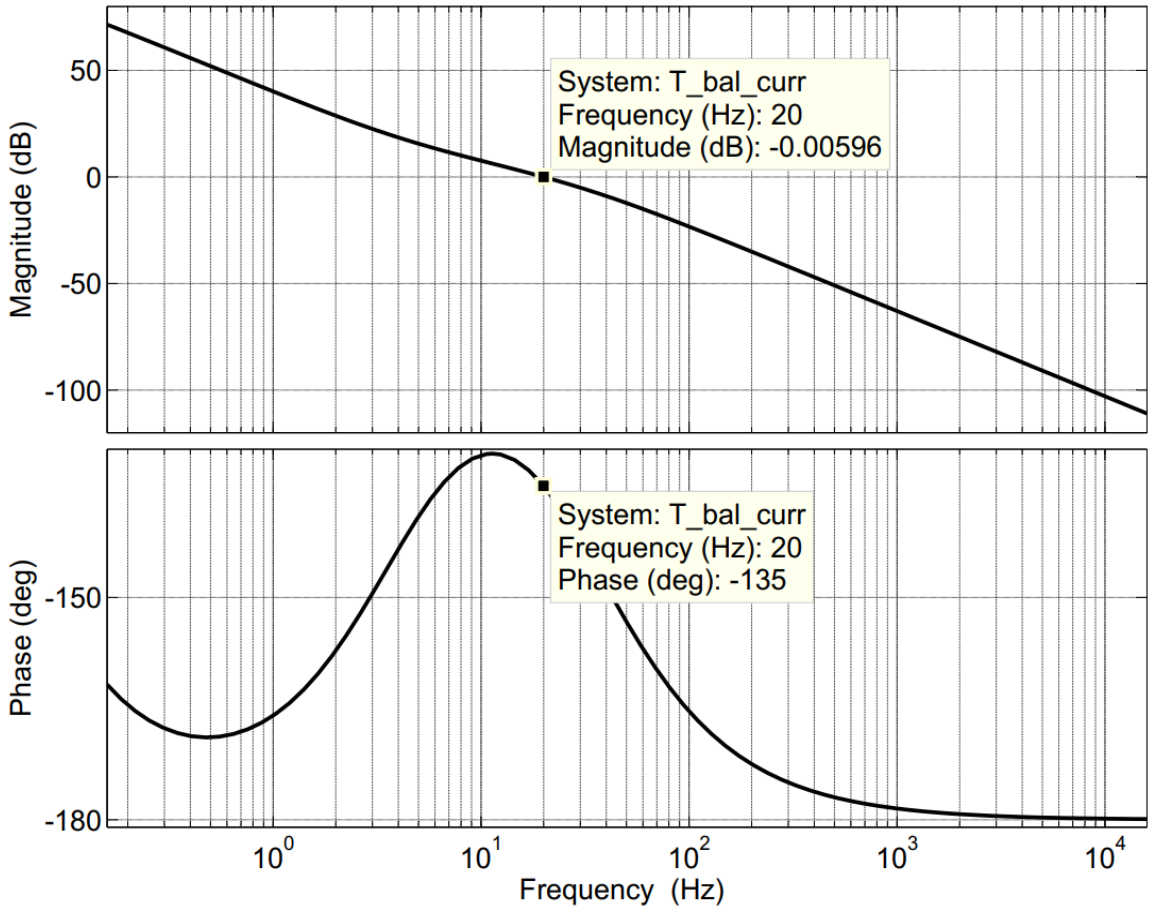

Figure 6.11. Bode plots of the compensated open leg average voltage control inner loop.

$$G_{cb}(s) = K_{cb}\left(1 + \frac{1}{\tau_{cb}s}\right) = 0.1246\left(1 + \frac{1}{3.7438 \times 10^{-2}s}\right) \tag{6.7}$$

The open outer loop is thus given by $H_{open,vb}(s) = H_{vb}(s)H_{open,cb}(s)/\left(1 + H_{open,cb}(s)\right)$ and its Bode plots appear in Figure 6.12. The outer loop controller is then given by (6.8) and the compensated loop appears in Figure 6.13.

$$G_{vb}(s) = K_{vb}\left(1 + \frac{1}{\tau_{vb}s}\right) = 4.2496\left(1 + \frac{1}{4.5131 \times 10^{-2}s}\right). \tag{6.8}$$

To test the setpoint tracking effectiveness of the controllers, the setpoint of the average of the SM capacitor voltages was initially set to the nominal value of about 750 V and step-changed to 862.5 V (= 15% step) at 0.6 s (see simulation in Figure 6.14), with the MMC in rectifier mod. The rise time was about 12 ms (about 0.6 times the fundamental period), the overshoot was about 2.4%, and the settling time was about 30 ms (about 1.5 times the

fundamental period). The SM capacitor voltages (and their average) are observed to track the setpoint accordingly. The DC bus voltage and the AC current are adequately decoupled from setpoint changes in the SM capacitor voltages and reject them as disturbance (see how they regain their original values after the setpoint change in simulation in Figure 6.15). The DC bus voltage settles after about 51.2 ms (about 2.6 times the fundamental period).

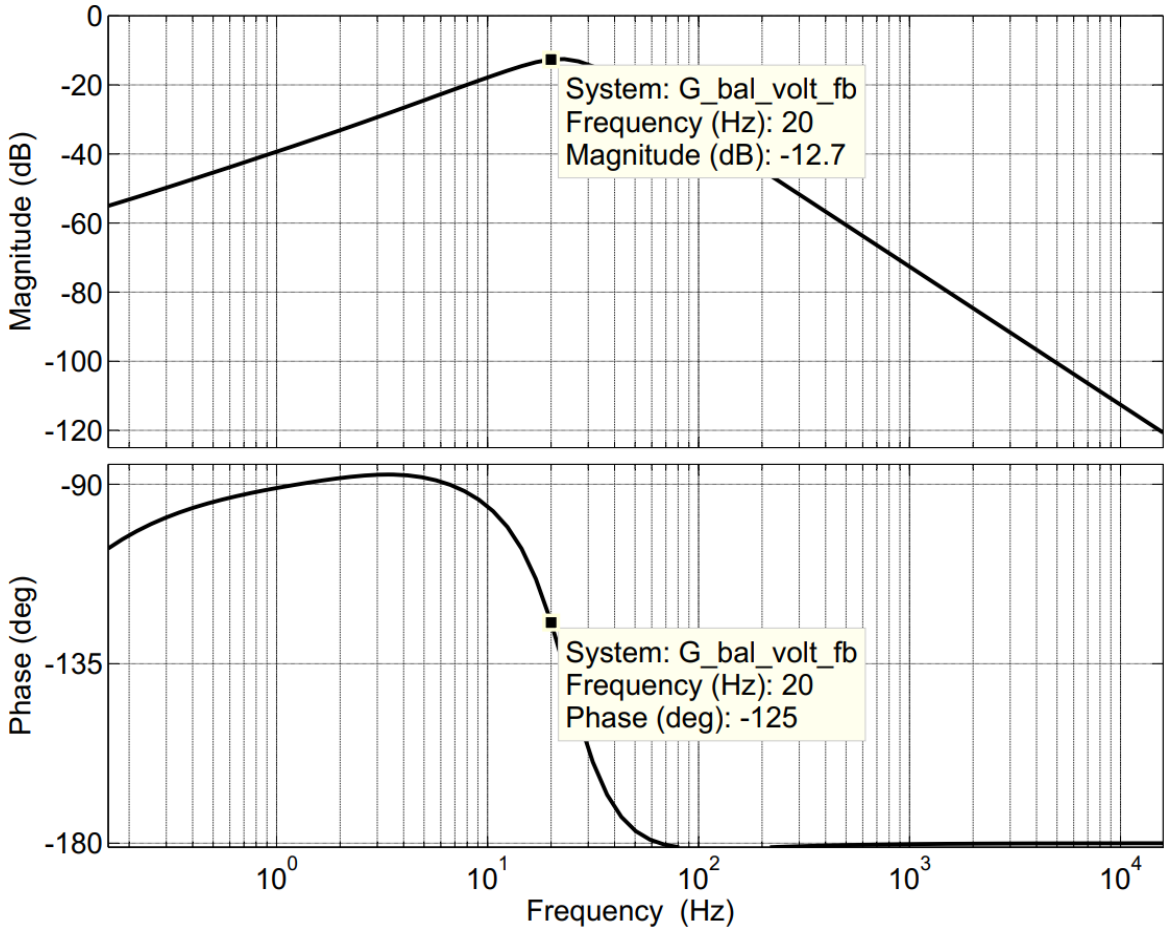

Figure 6.12. Bode plots of the open leg average voltage control outer loop.

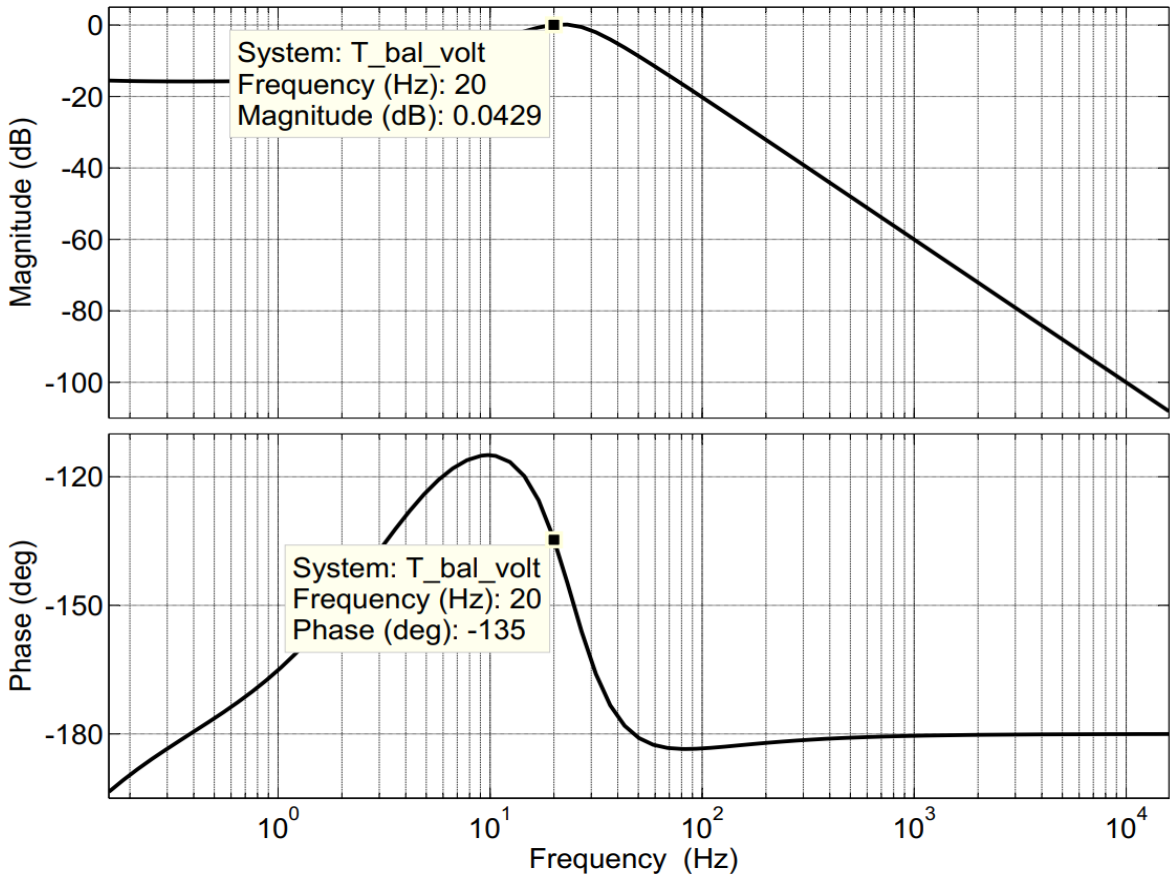

Figure 6.13. Bode plots of the compensated open leg average voltage control outer loop.

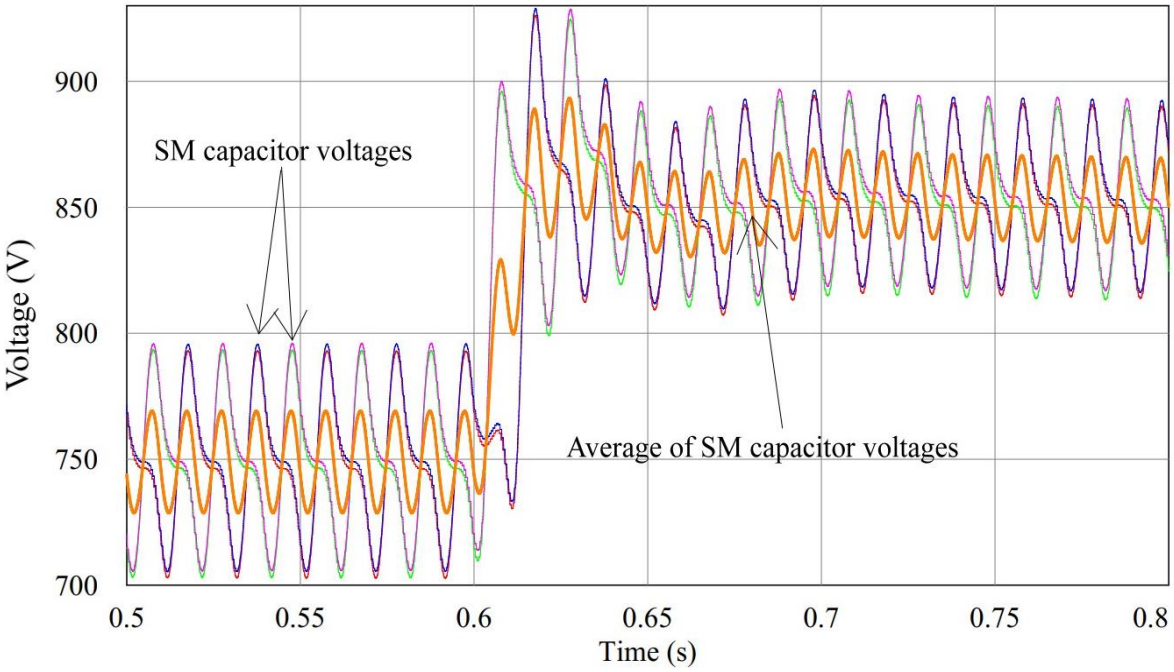

Figure 6.14. Setpoint tracking of the SM capacitor voltages.

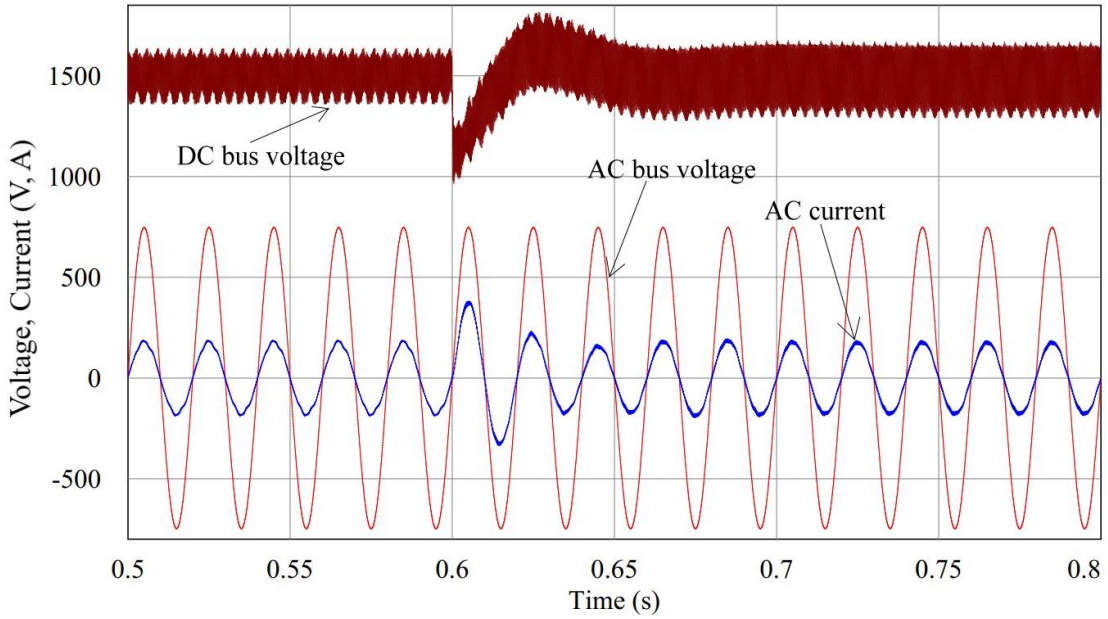

Figure 6.15. The DC bus voltage and the AC current reject the disturbance brought by a step change in the SM capacitor voltage.

6.5 CIRCULATING CURRENT SUPPRESSION CONTROLLER

The circulating current suppression controller was implemented to eliminate the second, the fourth, and the eighth order harmonics. These frequencies were chosen after observing the major harmonics in the simulated circulating current. The design methodology was adapted from [105]. With reference to Figure 2.7, K_p is set high enough for fast transient response, at 0.2. To not deteriorate the resonant frequency gain, ω_c must be set to the smallest value possible. A value of 10 rad/s is chosen. Since in practice ω_c does not affect the bandwidth, K_r is used to raise the gain profile of the controller which effectively boosts the bandwidth. This is helpful when there is a discrepancy between the frequency set in the controller and the actual frequency being controlled i.e., it increases the resonant frequency control robustness. All the K_r values were set to 25, i.e., $K_{r2} = K_{r4} = K_{r8} = 25$. The Bode plots of the controller are shown in Figure 6.16. The cut-off frequency for noise rejection is at around 500 Hz, as highlighted in Figure 6.16.

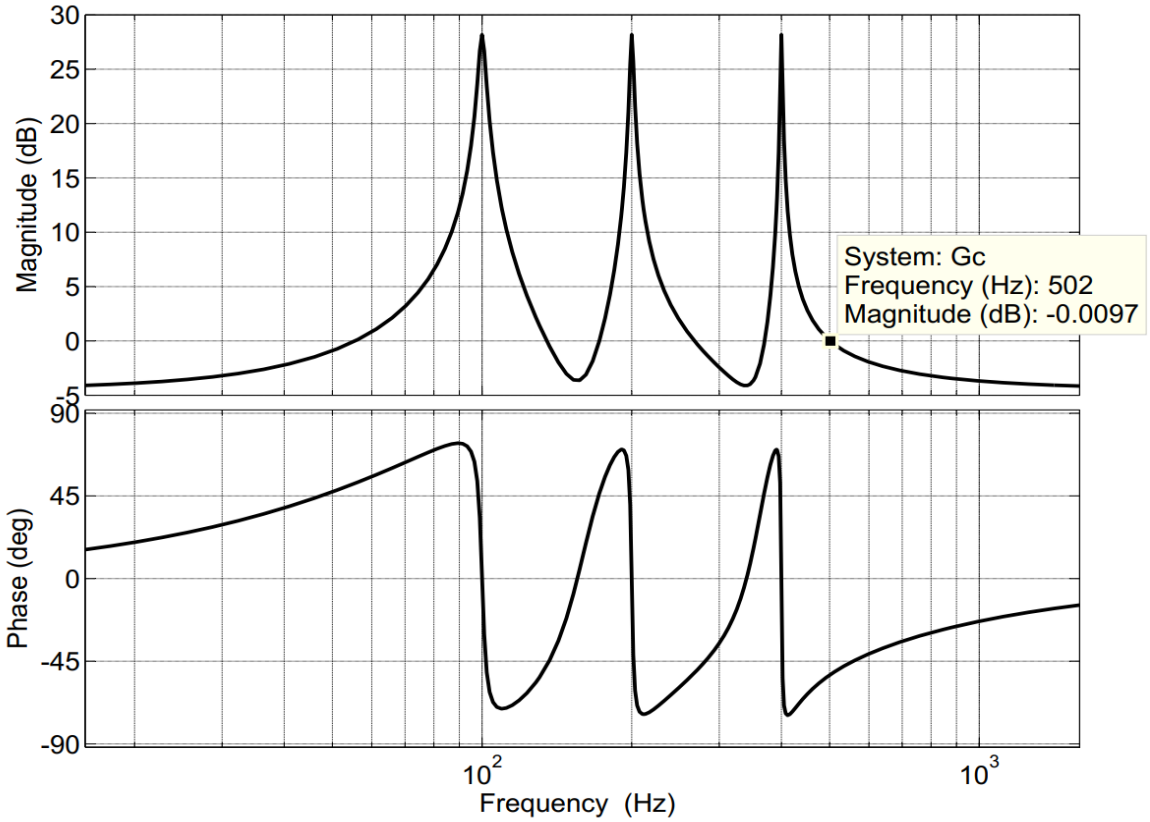

Figure 6.16. Bode plots of the circulating current suppression controller.

6.6 CHAPTER SUMMARY

In this chapter the current, the DC bus voltage, and the leg average voltage controllers were designed based on the models presented in Chapter 3. The control models were verified through simulation of the designed converter using the designed controllers, in PSIM software. The robustness of the DC bus voltage and of the leg average voltage controllers was demonstrated using setpoint step changes of about 15% each. This way the leg average voltage control model presented in Chapter 3, which is part of the contribution of this dissertation, was verified. The adapted DC bus voltage control model was also verified.

CHAPTER 7 SIMULATION RESULTS AND DISCUSSION

7.1 CHAPTER OBJECTIVES

The objective of this chapter is to present the simulation results of the converter modeled and designed in the preceding chapters. The results involve the comparison between the HB-MMC and the FB-MMC, validation of the SM capacitor design method presented in Chapter 5, and the simulated losses in the HB-MMC and the FB-MMC. The comparative study has been done at two operating conditions: in the linear modulation region at an apparent power of 200 kVA, unity power factor, DC bus voltage of 1500 V, and AC bus voltage of 915 V line-to-line; and in the overmodulation region at an apparent power of 200 kVA, unity power factor, DC bus voltage of about 1050 V, and AC bus voltage of 915 V line-to-line.

7.2 INTRODUCTION

The rectifier mode numerical results, comparing the HB-MMC and the FB-MMC, are captured in Table 7.1. The semiconductor switch and diode currents are recorded in Table 7.2 for the HB-MMC versus the linearly modulated FB-MMC. The overmodulated FB-MMC results, alongside those of the linearly modulated FB-MMC are summarized in Table 7.3. The semiconductor switch and diode currents are recorded in Table 7.4 for the linearly modulated MMC versus the overmodulated MMC. The results in Tables 7.2 and 7.4 are for bidirectional converters, in order to make a fair comparison between the HB-MMC and the FB-MMC. This is because for a given power flow direction either the switches or the diodes may carry more current and the currents flowing in the corresponding devices in the HB-

MMC and in the FB-MMC may not be equal, as is evident in Tables 7.2 and 7.4. On the other hand, if bidirectional power flow is considered, the currents are, on average, similarly distributed in the corresponding devices of the two converters. This also enables the power loss comparisons to be fairly carried out. The devices in tables 7.2 and 7.4 were defined in Figure 2.1.

7.3 HB-MMC VERSUS FB-MMC

The results are roughly categorized into AC-side quantities, DC-side quantities, and arm quantities. The simulated results of the two converters are closely matched together and to the analytical values.

In Table 7.1, $i_{arm,f}$ is the fundamental component of the arm current, $i_{circ,DC}$ is the DC component of the circulating current, $i_{circ,2f}$ is the second order component of the circulating current, $i_{arm,RMS}$ is the RMS value of the arm current, and $\Delta v_{dc,pk-pk}$ is the peak-peak ripple of the DC bus voltage. Calculations of the analytical values are shown in Addendum B.

7.3.1 AC-side quantities

The AC current is of interest. Figure 7.1 shows the AC bus voltage and the AC currents for both the HB-MMC and the FB-MMC. The currents are practically equal, whereby the analytical value is 178.469 A while the simulated values are 178.906 A for the HB-MMC and 178.884 A for the FB-MMC. Both the simulated AC-side power factors are about 0.999 p.u.

7.3.2 Arm quantities

The arm and circulating currents are shown in Figure 7.2 and the frequency spectra of the arm currents are shown in Figure 7.3. The arm currents are characterized by the DC, the fundamental, and the switching frequency components; the circulating currents are characterized by the DC and the switching frequency components. The switching frequency

Table 7.1. Analytical and simulated results of HB- and FB-MMC rectifiers.

Parameter	Unit		HB-MMC	FB-MMC
$i_{arm,f}$	A	Analytical	89.235	89.235
		Simulated	89.467	89.446
$i_{circ,DC}$	A	Analytical	44.444	44.444
		Simulated	44.438	44.440
$i_{circ,2f}$	A	Analytical[a]	26.853	26.853
		Simulated	0.753	0.310
$i_{arm,RMS}$	A	Analytical	79.481	79.481
		Simulated	77.484	77.470
V_c	V	Analytical	748.547	748.547
		Simulated	748.540	748.547
$\Delta v_{c,pk-pk}$	%	Analytical	5.000	5.000
		Simulated	2.833	2.824
V_{dc}	V	Analytical	1500.000	1500.000
		Simulated	1499.997	1500.000
$\Delta v_{dc,pk-pk}$	%	Analytical	—	—
		Simulated	6.905	6.699
I_{ac}	A	Analytical	178.469	178.469
		Simulated	178.906	178.884
pf_{ac}	p.u.	Analytical	1.00000	1.00000
		Simulated	0.99975	0.99973

[a] The analytical value assumes no circulating current suppression control. This is the simulated value recorded when circulating current suppression control is inactive, confirming (5.20)

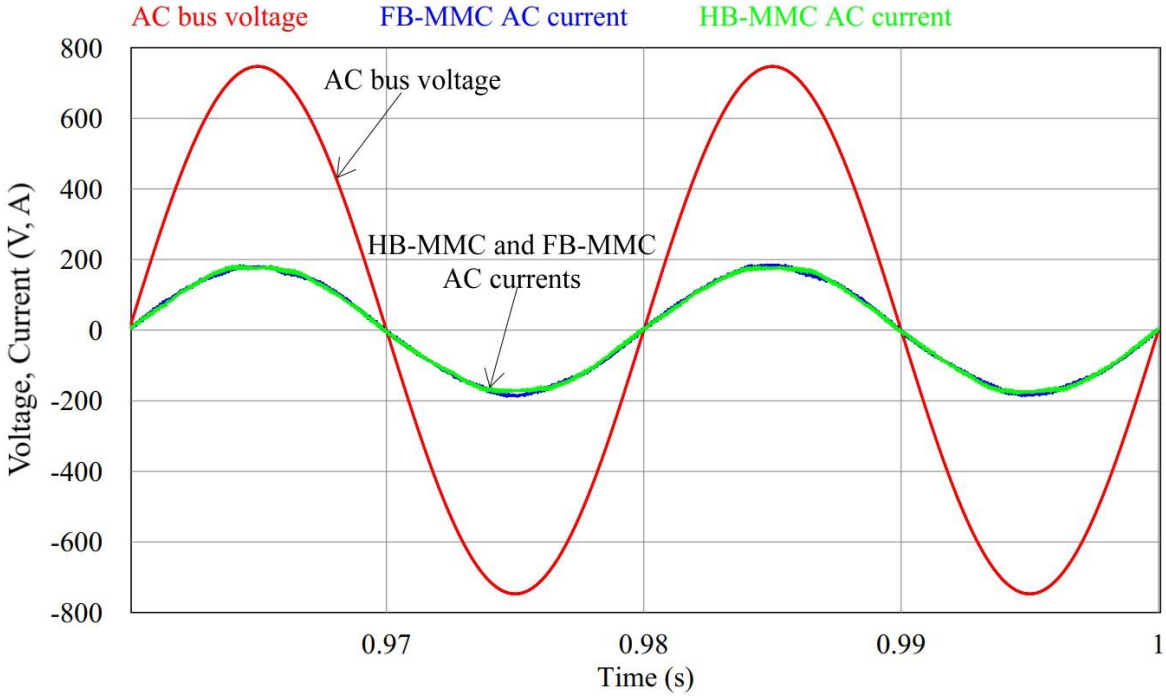

Figure 7.1. The AC bus voltage and the HB-MMC and FB-MMC AC currents.

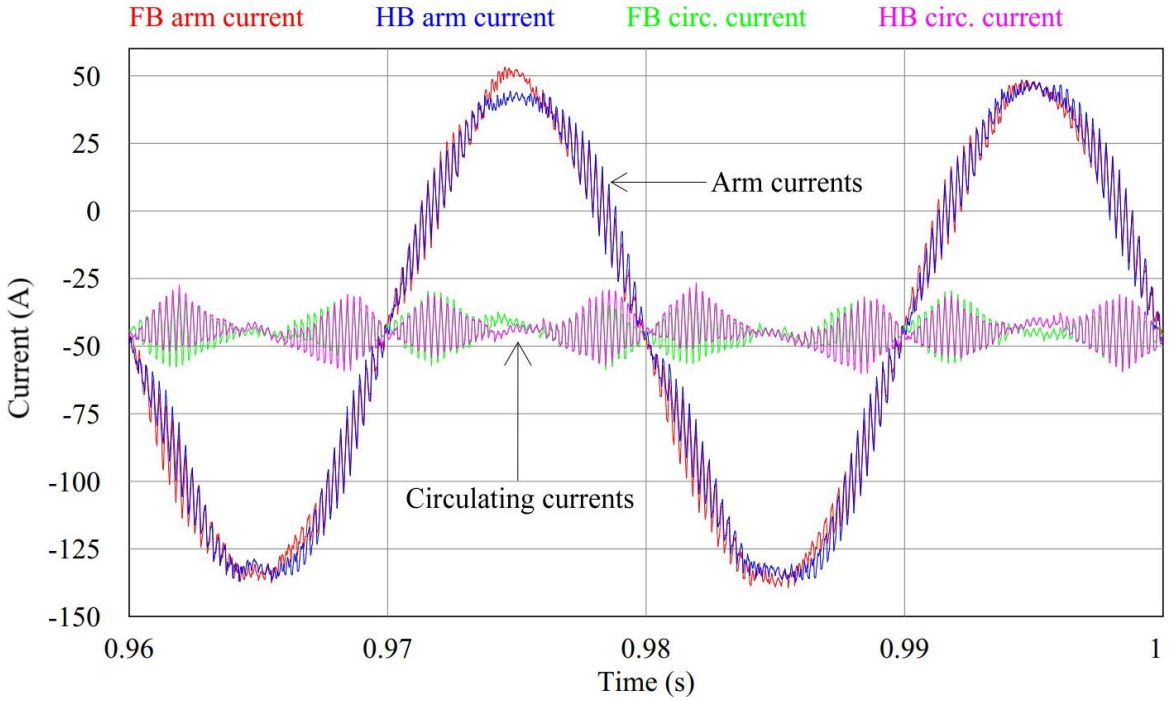

Figure 7.2. Arm and circulating currents in HB-MMC and FB-MMC rectifiers.

components are however not shown in Figure 7.3, but they are not more than 3.9 A per component, and they occur as sidebands of the switching frequency. The second order

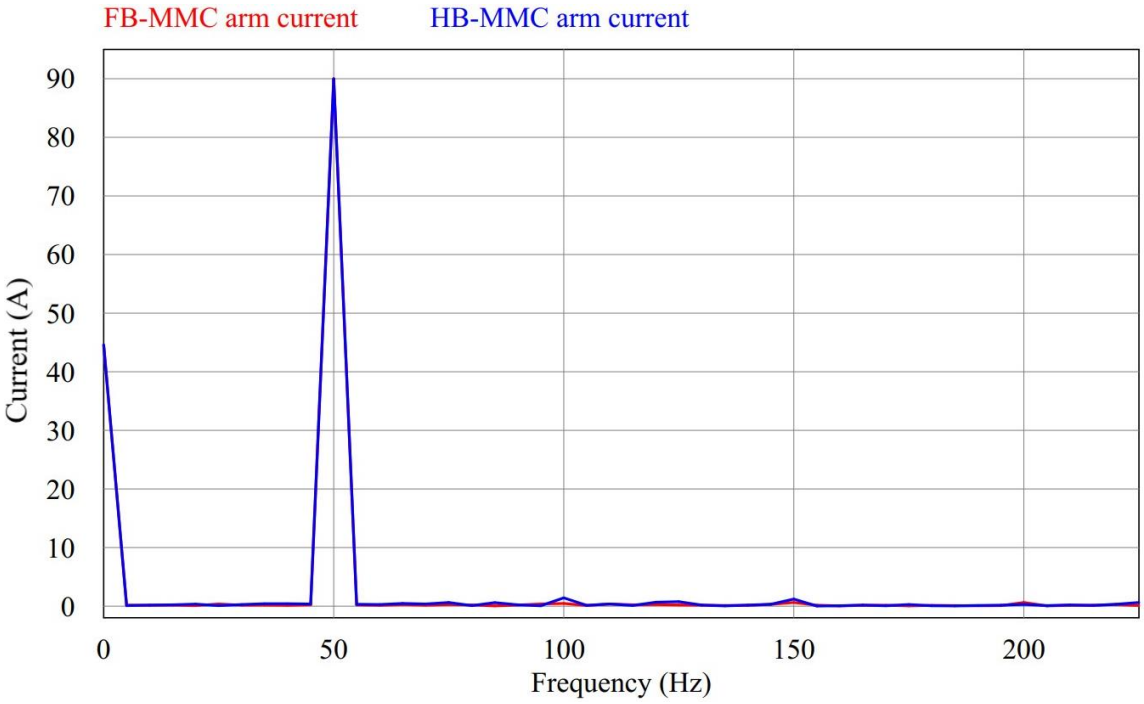

Figure 7.3. Arm currents frequency spectra of the HB-MMC and the FB-MMC rectifiers.

component of the arm current is almost non-existent as it can be observed in Figure 7.3, thanks to the effective circulating current suppression controller. The capacitor voltages of top SMs of phase 'a' for both the HB-MMC and the FB-MMC are shown in Figure 7.4 and their frequency spectra are shown in Figure 7.5. Observation of Figure 7.5 indicates that the SM capacitor voltage ripple is contributed mostly by the first order component as asserted in Chapter 5.

The simulated DC component of the circulating current in the HB-MMC is 44.438 A while that of the FB-MMC is 44.440 A, against the analytical value of 44.444 A. The simulated second order components are 0.753 A in the HB-MMC and 0.310 A in the FB-MMC, against the analytical value of 26.853 A. The simulated fundamental components in the arm current are 89.467 A in the HB-MMC and 89.446 A in the FB-MMC, versus the analytical value of 89.235 A. The arm RMS currents are 77.484 A in the HB-MMC and 77.470 A in the FB-MMC, against the analytical value of 79.481 A. The simulated values are a bit lower than the analytical value due to the suppressed second order component. The capacitor voltages are 748.540 V in the HB-MMC and 748.547 V in the FB-MMC, against the analytical value of 748.547 V. The simulated SM capacitor ripple voltages sit at 2.833% in the HB-MMC

and 2.824% in the FB-MMC, of the average value, well below the design value of 5%. This justifies the SM capacitor design method proposed in Chapter 5.

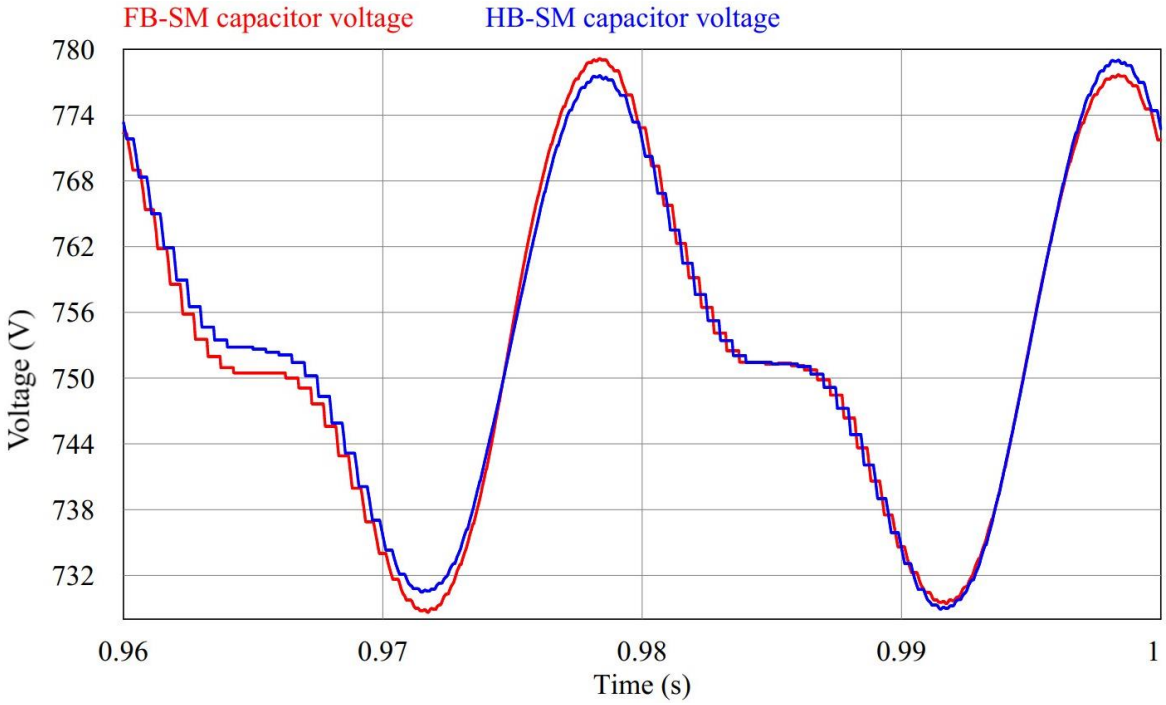

Figure 7.4. SM voltage capacitors of HB-MMC and FB-MMC rectifiers.

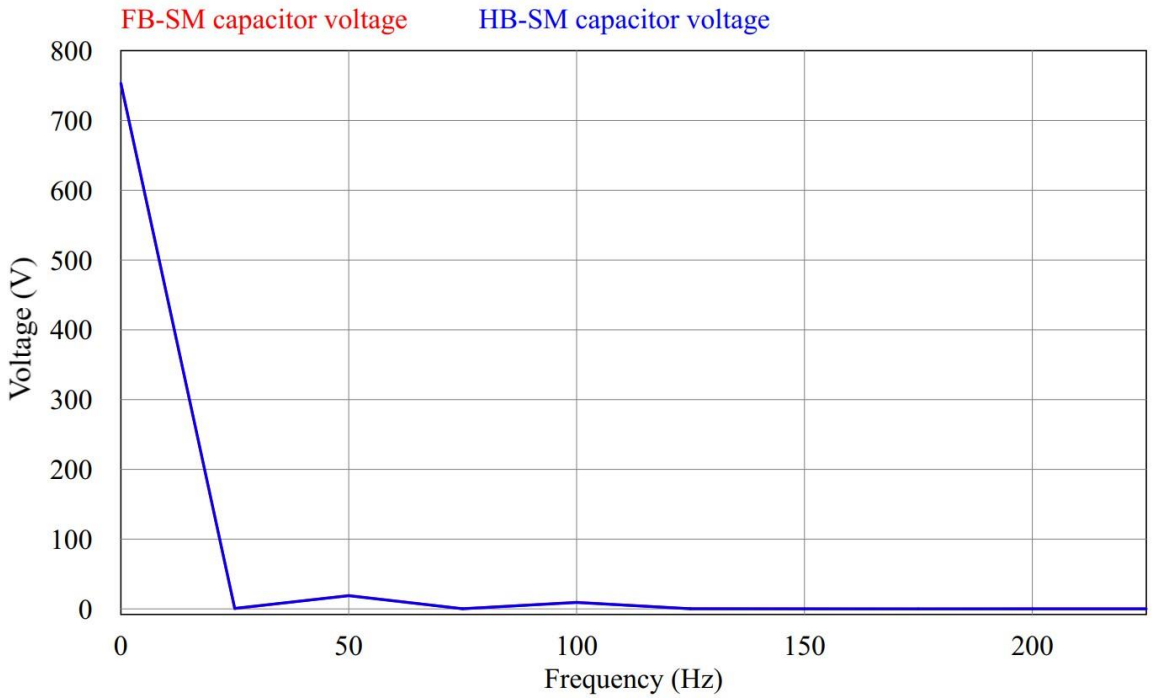

Figure 7.5. Frequency spectra of SM voltage capacitors of HB-MMC and FB-MMC rectifiers.

Table 7.2. Simulated currents of semiconductor devices in HB-MMC and FB-MMC bidirectional converters in the linear modulation region.

Parameter	Mode	Device	HB-MMC		FB-MMC	
			Average (A)	RMS (A)	Average (A)	RMS (A)
i_{sw}	Rectifier	T_1	9.4745	26.1550	31.8501	56.2325
		T_2	0.5684	3.9506	0.2825	2.6704
		T_3	—	—	0.2806	2.6831
		T_4	—	—	31.8456	56.2345
	Inverter	T_1	9.3551	18.4549	9.6254	18.6529
		T_2	44.9809	70.3482	22.4999	49.7598
		T_3	—	—	22.4863	49.7484
		T_4	—	—	9.6239	18.6477
i_{diode}	Rectifier	D1	-9.4745	18.6712	-9.6254	18.7431
		D2	-45.0155	70.3954	-22.5116	49.8103
		D3	—	—	-22.5161	49.8080
		D4	—	—	-9.6425	18.7412
	Inverter	D1	-9.3619	26.0225	-31.8424	56.1294
		D2	-0.5453	3.7543	-0.2714	2.6303
		D3	—	—	-0.2729	2.6668
		D4	—	—	-31.8559	56.1395

7.3.3 DC-side quantities

The DC bus voltage waveforms are shown in Figure 7.6 and their spectra are shown in Figure 7.7. The only harmonics present are the switching frequency harmonics and occur as sidebands of Nf_{sw} for the HB-MMC and as sidebands of $2Nf_{sw}$ for the FB-MMC. Although the FB-MMC is switched at half the switching frequency of the HB-MMC, its harmonics occur at the same frequency as that of the HB-MMC. This is because the unipolar modulation scheme adopted in the FB-MMC doubles the effective switching frequency of the SM output

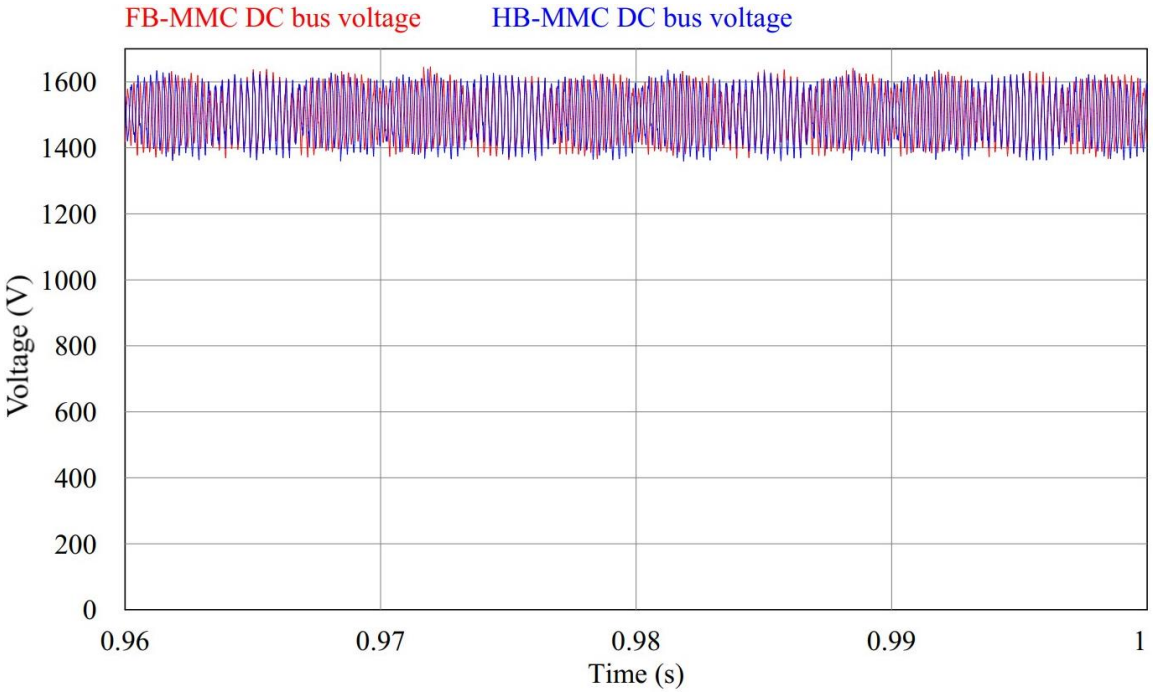

Figure 7.6. DC bus voltages of HB-MMC and FB-MMC rectifiers.

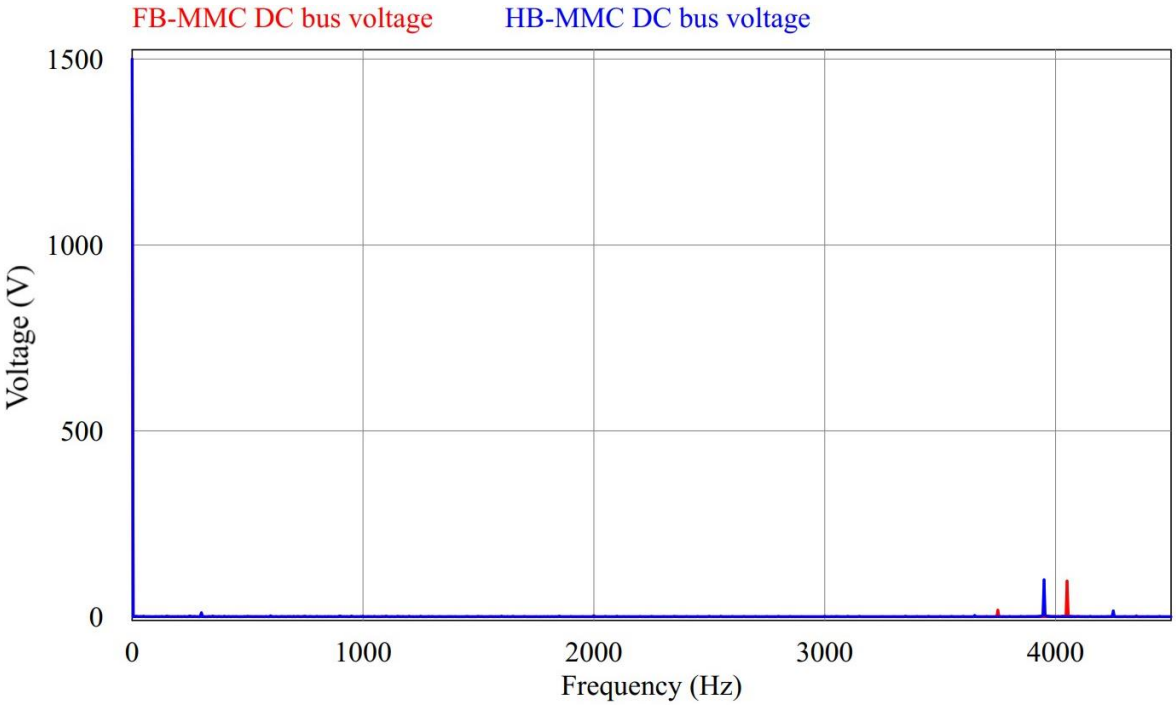

Figure 7.7. Frequency spectra of DC bus voltages of HB-MMC and FB-MMC rectifiers.

voltage. The major harmonic occurs at 3950 Hz ($\equiv (2m_f - 1)f$) for the HB-MMC and at 4050 Hz ($\equiv (4m_f + 1)f$) for the FB-MMC.

The DC voltages are 1499.997 V in the HB-MMC and 1500 V in the FB-MMC, against the analytical value of 1500 V. The DC ripple voltages are at 6.905% in the HB-MMC and 6.699% in the FB-MMC, of the average DC bus voltage. The DC bus voltage percentage ripple is consistently higher than that of the SM capacitor, as is evident from Table 7.1. This implies that the SM capacitor sized to suppress a given SM capacitor voltage percentage ripple may not necessarily meet the DC bus voltage percentage ripple specification. For HVDC applications, the SM capacitor serves the filtering purposes for both the SM capacitor and the DC bus voltages. This is because the DC-link capacitor is avoided to limit the DC-side fault current. Thus, analysis of the relationship between the SM capacitor voltage ripple and the DC bus voltage ripple will help to establish a SM capacitor design method that ensures that both ripples are adequately suppressed. This may involve the switching frequency harmonic analysis of the MMC, as the DC bus voltage ripple is of the switching frequency order.

7.4 LINEARLY MODULATED FB-MMC VERSUS OVERMODULATED FB-MMC

In this section the overmodulated FB-MMC rectifier results are presented ($m_a = \sqrt{2} \approx 1.4142$). To achieve overmodulation in a rectifier the DC bus voltage was lowered while maintaining the AC bus voltage, in line with the analysis carried out in Chapter 4 (this should be an advantage for the overmodulated converter as it can also be operated at a lower DC bus voltage for the same output AC voltage, in case of an inverter). The results of the FB-MMC rectifier operated in the linear modulation region are also presented for comparison. The two converters are operated at the same power level and have the same SM capacitors and the same arm inductors. $i_{c,RMS}$ is the SM capacitor RMS current. The rest of the variables have been defined previously. The results are summarized in Table 7.3. Calculations of the analytical values are presented in Addendum B.

Due to a much higher simulated DC arm current in the overmodulated FB-MMC (63.098 A versus 44.440 A in the linearly modulated FB-MMC), its arm current RMS value is about

Table 7.3. Analytical and simulated results of linearly modulated FB-MMC and overmodulated FB-MMC rectifiers.

Parameter	Unit		Linearly modulated MMC	Overmodulated MMC
$i_{arm,f}$	A	Analytical	89.235	89.235
		Simulated	89.446	89.265
$i_{circ,DC}$	A	Analytical	44.444	63.098
		Simulated	44.440	63.098
$i_{circ,2f}$	A	Analytical	26.853	23.800
		Simulated	0.310	0.352
$i_{arm,RMS}$	A	Analytical	79.481	90.808
		Simulated	77.470	89.356
V_c	V	Analytical	748.547	637.685
		Simulated	748.547	637.685
$\Delta v_{c,pk-pk}$	%	Analytical	5.000	—
		Simulated	2.824	1.752
$i_{c,RMS}$	A	Analytical	—	—
		Simulated	32.050	35.227
V_{dc}	V	Analytical	1500.000	1056.551
		Simulated	1500.000	1056.551
$\Delta v_{dc,pk-pk}$	%	Analytical	—	—
		Simulated	6.699	1.615
I_{ac}	A	Analytical	178.469	178.469
		Simulated	178.884	178.527
pf_{ac}	p.u.	Analytical	1.00000	1.00000
		Simulated	0.99973	0.99929

1.153 times that of the linearly modulated FB-MMC (77.470 A in the linearly modulated FB-MMC and 89.356 A in the overmodulated FB-MMC). This ratio closely matches the ratio obtained in the analysis of Chapter 4, out of equation (4.4). The same number is obtained if the square root of the ratio of the squares of the switch RMS currents in the overmodulation region to the squares of the switch RMS currents in the linear modulation region is calculated from Table 7.4, i.e.,

$$\sqrt{\frac{\left(\begin{matrix}62.4787^2+1.1088^2+1.1505^2+62.4893^2\\+9.5131^2+63.1283^2+63.1608^2+9.5139^2\end{matrix}\right)}{\left(\begin{matrix}56.2325^2+2.6704^2+2.6831^2+56.2345^2\\+18.6529^2+49.7598^2+49.7484^2+18.6477^2\end{matrix}\right)}} = 1.154.$$

The simulated second order component in the overmodulated FB-MMC, at 0.352 A, is not far off from that in the linearly modulated FB-MMC, at 0.310 A. The low values are due to the circulating current suppression controller. The higher arm RMS current and the higher arm current DC component in the overmodulated FB-MMC mean that the conduction and the ohmic losses will be higher in the overmodulated converter, as asserted in the analysis of Chapter 4.

The SM capacitor ripple voltages are at 2.824% in the linearly modulated converter versus 1.752% in the overmodulated converter, a ratio of about 1.612. The lower ripple in the overmodulated FB-MMC supports the findings that overmodulation, especially at the specific modulation index $m_a = \sqrt{2} \approx 1.4142$, minimizes the SM capacitor voltage ripple [59]. Unlike in the linearly modulated MMC (see Figure 7.4 and Figure 7.5), simulation of the overmodulated MMC shows that the SM capacitor voltage is practically free of the fundamental component, with the second order component being dominant. This can be seen from both Figure 7.8 and Figure 7.9.

Table 7.4. Simulated currents of semiconductor devices in linearly modulated FB-MMC and overmodulated FB-MMC bidirectional converters.

Parameter	Mode	Device	Linearly modulated MMC		Overmodulated MMC	
			Average (A)	RMS (A)	Average (A)	RMS (A)
i_{sw}	Rectifier	T_1	31.8501	56.2325	35.8331	62.4787
		T_2	0.2825	2.6704	0.08315	1.1088
		T_3	0.2806	2.6831	0.08608	1.1505
		T_4	31.8456	56.2345	35.8515	62.4893
	Inverter	T_1	9.6254	18.6529	4.2951	9.5131
		T_2	22.4999	49.7598	31.6271	63.1283
		T_3	22.4863	49.7484	31.6586	63.1608
		T_4	9.6239	18.6477	4.2949	9.5139
i_{diode}	Rectifier	D1	-9.6254	18.7431	-4.3050	9.5834
		D2	-22.5116	49.8103	-31.6535	63.1491
		D3	-22.5161	49.8080	-31.6351	63.1386
		D4	-9.6425	18.7412	-4.3020	9.5785
	Inverter	D1	-31.8424	56.1294	-35.8661	62.4647
		D2	-0.2714	2.6303	-0.0800	1.1057
		D3	-0.2729	2.6668	-0.0802	1.0995
		D4	-31.8559	56.1395	-35.8347	62.4318

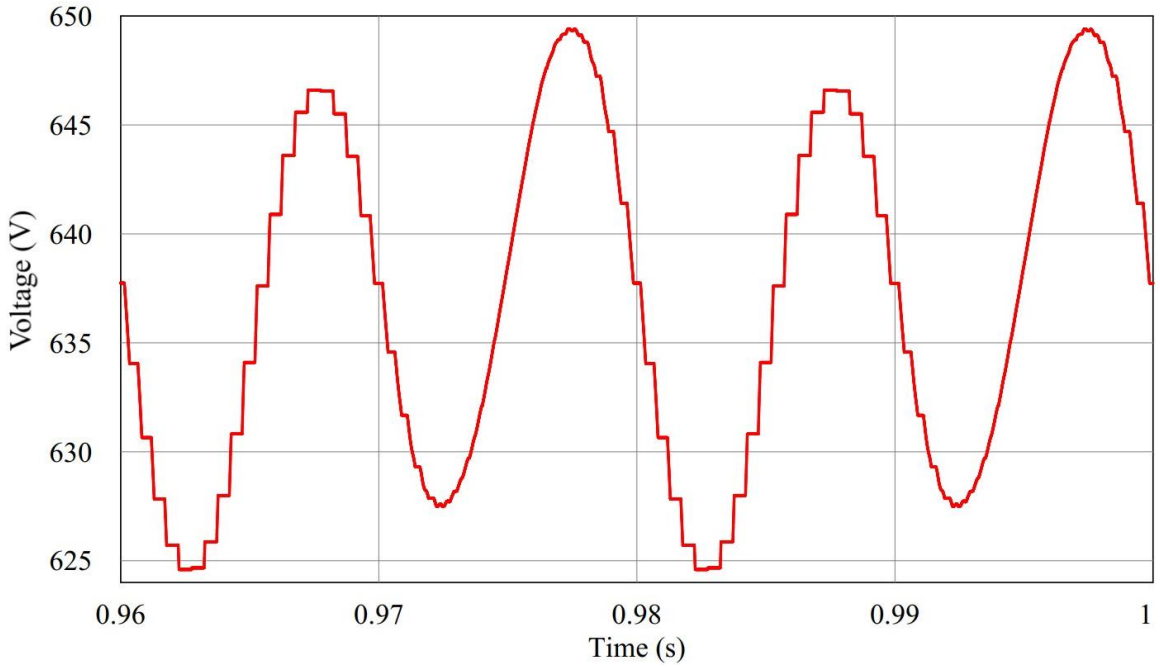

Figure 7.8. SM capacitor voltage of an overmodulated FB-MMC.

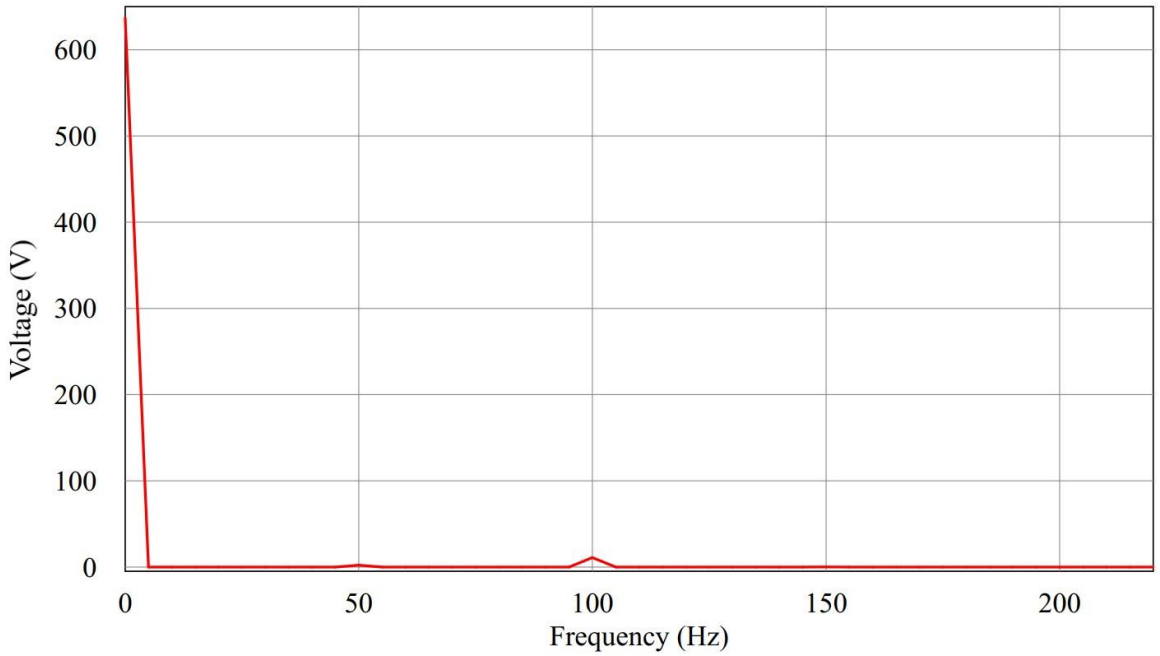

Figure 7.9. Frequency spectra of the SM capacitor voltage of an overmodulated FB-MMC.

The SM capacitor and semiconductor switch voltage rating in the overmodulated FB-MMC is around 0.852 times that in the linearly modulated FB-MMC. This is an advantage for the

overmodulated converter since its SM capacitors must support only a smaller voltage and its semiconductor switches must also block a smaller voltage. However, the SM capacitor RMS current in the overmodulated FB-MMC is about 1.099 times that in the linearly modulated FB-MMC and the semiconductor switch average current in the overmodulated FB-MMC is effectively about 1.119 that in the linearly modulated FB-MMC. The latter is calculated as the ratio of the sum of all the average currents in both directions of the overmodulated converter to the corresponding sum in the linearly modulated converter, see Table 7.4. Similarly, the effective ratio between the switch RMS currents is about 1.07, whereby the current in the overmodulated converter is effectively higher.

If the voltage and current ratings are assumed to have the same effect on cost and size of the capacitor and the switch, then the "effective" reduction in the switch voltage blocking rating is by a factor of only $0.852 \times 1.153 = 0.982$ and that in the capacitor voltage rating is by a factor of only $0.852 \times 1.099 = 0.936$. Thus, the advantage gained in the voltage ratings is partly lost in the current ratings for the same devices.

The peak-peak DC bus ripple voltage in the overmodulated converter is at 1.615%, 0.241 times smaller than 6.699% in the linearly modulated converter. The AC-side power factors are 0.9997 p.u. in the linearly modulated FB-MMC and 0.9993 p.u. in the overmodulated FB-MMC.

Overall, the overmodulated FB-MMC does not stand in a better position against the HB-MMC than the linearly modulated FB-MMC does. The same conclusion can be drawn after the power loss comparison is done, which will be carried out subsequently.

7.5 POWER LOSSES AND NUMBER OF SEMICONDUCTOR DEVICES

For power losses simulation the IGBT and its antiparallel diode must meet the current and blocking voltage specifications, in order to have realistic results for the chosen power level. The specifications were made with a safety factor between 1.5 and 2. For a blocking voltage of 750 V and the switch RMS current of about 70.5 A (see Table 7.2), the practical blocking

voltage must be in or above the range 1125 — 1500 V and the rated current must be in or above the range 106 — 141 A. The IGBT module SEMiX151GB12E4s was selected. It is rated at 1200 V and 150 A for both the IGBT and the diode. The parasitic parameters of interest, at a junction temperature of 150°C, are as follows: $V_{ce,0} = 0.7\,V$, $r_{ce} = 10\,m\Omega$, $V_{fwd,0} = 0.9\,V$, $r_{fwd} = 7.8\,m\Omega$, $t_r = 42\,ns$, and $t_f = 91\,ns$. These parameters were described in Chapter 4. The PSIM software allows simulation of the fall time of the switch current (and concurrently the rise time of the voltage across the switch) but not the rise time. Hence, only the turn-off switching losses were simulated, then multiplied by two, assuming that the turn-on losses are equal to the turn-off losses, in accordance with (4.7). For that reason, the simulation rise and fall times were recalculated as $t_r^* = t_f^* = 0.5(t_r + t_f) = 66.5\,ns$. The ohmic losses in the arm inductors have been excluded since they are insignificant compared to any other losses.

If the sum of all the switch average currents for both the power flow directions of the FB-MMC in Table 7.2 is divided by the corresponding sum of the HB-MMC, the ratio obtained is about 2, i.e.,

$$\frac{31.8501 + 0.2825 + 0.2806 + 31.8456 + 9.6254 + 22.4999 + 22.4863 + 9.6239}{9.4745 + 0.5684 + 9.3551 + 44.9809} = 1.996.$$

About the same ratio is obtained when the sums of the squares of corresponding RMS values are divided, i.e.,

$$\frac{\begin{pmatrix} 56.2325^2 + 2.6704^2 + 2.6831^2 + 56.2345^2 \\ +18.6529^2 + 49.7598^2 + 49.7484^2 + 18.6477^2 \end{pmatrix}}{26.1550^2 + 3.9506^2 + 18.4549^2 + 70.3482^2} = 2.001$$

This should lead to the switch conduction losses in the FB-MMC being twice those in the HB-MMC, as asserted in Chapter 4. This is the case, as the simulated switch conduction losses amounted to 629.21 W in the HB-MMC and 1257.76 W in the FB-MMC, a ratio of 1.999. The simulated diode conduction losses were 667.93 W in the HB-MMC and 1274.59 in the FB-MMC, a ratio of 1.908.

The switching losses were 307.65 W in the HB-MMC and 306.97 W in the FB-MMC, approximately equal, despite the number of semiconductor devices in the FB-MMC being

double those in the HB-MMC. This is because of the adopted unipolar modulation scheme for the FB-MMC whereby only half of the switching frequency in the HB-MMC is used but produces the same effective switching frequency. However, switching losses contribute a smaller percentage to the total losses in an MMC due to the relatively lower switching frequencies utilized, which is confirmed in literature [8], [45]. The switching losses were about 19.17% of the total losses in the HB-MMC and about 10.81% in the FB-MMC.

Overall, the simulated total losses in the FB-MMC were 1.77 times the total losses in the HB-MMC.

The simulated switch conduction losses in the overmodulated FB-MMC were 1554.19 W, which are 1.236 times the 1257.76 W in the linearly modulated FB-MMC. The simulated diode conduction losses in the overmodulated FB-MMC were 1547.51 W, and they are 1.214 times those in the HB-MMC at 1274.59 W. The simulated switching losses in the overmodulated FB-MMC were 292.59 W, compared to 306.97 W in the linearly modulated converter. Thus, the switching losses in the overmodulated converter were 95.32% those in the linearly modulated converter. Overall, the simulated total losses in the overmodulated FB-MMC were 1.2 times those in the linearly modulated FB-MMC.

So far, the FB-MMC trails behind the HB-MMC in terms of number of semiconductor devices per SM and power losses (number of semiconductor devices and conduction losses are double in the FB-MMC). However, the FB-MMC can block the DC-side fault currents, both temporary and permanent. The implications of this fact at a system level are not insignificant. If the HB-MMC is used in HVDC it should then be used with either fast DC circuit breakers or electronic circuit breakers, to avoid tripping of the interlinking AC network breakers (use of AC-side breakers to counter DC-side fault currents require shutting down of all the converter stations, AC breakers are slow for the required DC-side fault current interruption times and require oversized arm inductors and additional AC-side inductors, as discussed in Chapter 2). Of the two options, the electronic circuit breakers are more viable but are still significantly expensive, close to half of the total cost of the station [7]. If the cost of the additional number of semiconductor devices and conduction losses in

the FB-MMC exceeds the cost of a separate DC-side breaker then the HB-SM would be a better candidate. Otherwise using the FB-MMC with its inherent DC-side fault blocking capability would be a more economical choice. Conclusion between the two choices needs a cost-benefit analysis substantiated by industry cost data. It should be noted that since the MMC is used as a building block of the PET, if the intrinsic DC-side fault blocking capability of the FB-MMC is used, only one stage in the PET needs to be constructed using a FB-MMC. Such a stage would be the final rectification stage interlinking the DC network. The rest of the stages can be constructed using HB-MMCs.

7.6 CHAPTER SUMMARY

In this chapter the simulated results of the HB-MMC and those of the FB-MMC, and of the linearly modulated FB-MMC and those of the overmodulated FB-MMC, were compared side by side. It was found that the results of the HB-MMC and those of the FB-MMC were practically equal, confirming that the efficiency comparison of the two SMs in the linear modulation region is subject to the analysis conducted in Chapter 4. The comparison of the simulated results between the linearly modulated FB-MMC and the overmodulated FB-MMC at $m_a = \sqrt{2}$ indicate that the conduction and the ohmic losses in the overmodulated converter are higher than those in the linearly modulated converter – in agreement with the analytical prediction of Chapter 4. The switching losses are lower in the overmodulated FB-MMC. While the SM capacitors in the overmodulated converter are subject to lower ripple voltages as well as lower rated voltages, they must conduct more current. The lower voltages across the SM capacitors also mean lower blocking voltages for the semiconductor switches. However, the SMs in the overmodulated converter are still subject to higher conduction and switching losses, as shown in Chapter 4 and Table 7.4. The simulated DC bus peak-peak ripple voltage in the overmodulated converter was found to be 0.238 times smaller than that in the linearly modulated converter. Although this ratio is by no means constant, it serves to show that operating the MMC in the overmodulation region suppresses the ripple. The SM design method proposed in Chapter 5, which is part of the contribution of this dissertation, was verified by simulation results in this chapter

CHAPTER 8 CONCLUSION

The HB-SM and the FB-SM as building blocks of the HVDC-MMC, particularly the active MMC rectifier, were compared through analysis and simulation. It was found that by taking advantage of the doubling of the effective switching frequency by the unipolar modulation scheme used in the FB-MMC, the switching losses in the FB-MMC are the same as those in the HB-MMC, if the operation is constrained to the linear modulation region. However, switching losses are a small fraction of the total losses in an MMC. The conduction losses (which are the major losses) are higher in the FB-MMC, twice as much as in the HB-MMC. It was also found that operating the FB-MMC in the overmodulation region does not give it an advantage over the HB-MMC. At a system level, the intrinsic capability of the FB-SM to block DC-side fault currents eliminates the need for a DC-side circuit breaker. On the other hand, the HB-MMC must be used with a DC-side breaker for fast DC-side fault current blocking. Industry cost data between the two options must be analyzed to conclusively choose the more suitable option, that is, between a HB-MMC with a DC-side breaker and a FB-MMC with twice the semiconductor devices and twice the conduction losses but with the ability to block the DC-side fault current.

A SM capacitor design method suggested in the literature was expanded on and a graphical design technique resulted. The graphical approach is more convenient as it requires the designer to only calculate the modulation index to size a SM capacitor to limit the ripple voltage to a certain level.

A simple SM capacitor sizing method that results in minimized SM capacitor size was proposed. This method estimates the SM capacitor ripple based on the fundamental component of the capacitor current. The resulting SM capacitor size was significantly

smaller than those of the other methods proposed in the literature. The simulation results confirmed that the sized SM capacitor met the design SM capacitor ripple voltage specification.

A design methodology for SM capacitor average voltage controller in phase-shifted carrier modulated MMCs was proposed. The methodology was tested through simulation and it was shown that the resulting controllers resulted in robust setpoint tracking. The methodology eliminates the guesswork and extensive simulations that have been used in the past to design the leg average voltage loop controller parameters.

Possible future work includes comparison of the PET and LFT as standalone units as well as transmission/distribution system components, based on industry cost data. The cost of the transformer units and that of the devices that must accompany the LFT and those that are eliminated by the PET, such as STATCOM, must be established. Another area, which also needs industry data, is the cost comparison between the HB-SM and the FB-MMC as HVDC-MMC submodules. The cost of the DC circuit breakers that must accompany the HB-MMC and the cost of the extra semiconductors and power losses in the FB-MMC must be established. Lastly, a study to establish how the DC bus ripple voltage is related to the size of the SM capacitor and the SM capacitor voltage ripple. Since a DC link capacitor is avoided in HVDC-MMCs so as to curb the possible DC-side fault current, the SM capacitor size must cater for both the SM capacitor ripple voltage and the DC bus ripple voltage. Such a study may involve the switching harmonic analysis of the MMC since the DC bus ripple voltage is of the switching frequency order.

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ADDENDUM A MODELING OF LEG AVERAGE VOLTAGE CONTROL LOOPS FOR ANY NUMBER OF SUBMODULES

In section 3.5 the modeling of the leg average voltage control loops for any number of submodules was discussed. However, only the model for $N = 2$ was extracted, according to the system design. Equation 3.50 for the HB-MMC will be further expanded for $N = 4$ and for $N = 10$ to show the scalability of the general model in section 3.5. Equation 3.55 for the FB-MMC can be expanded in a similar manner.

Equation 3.50 is copied below as equation A.1.

$$\sum_{j=1}^{2N} \tilde{\delta}_j(t) = \sum_{j=1}^{N} \left\{ \tilde{\delta}\left(t - \frac{j-1}{N} T_{sw}\right) + \tilde{\delta}\left(t - \frac{2j-1+Nm_f}{2N} T_{sw}\right) \right\}. \tag{A.1}$$

For $N = 4$ equation A.1 becomes equation A.2:

$$\begin{aligned} \sum_{j=1}^{2N} \tilde{\delta}_j(t) = \tilde{\delta}(t) &+ \tilde{\delta}\left(t - \frac{1}{4} T_{sw}\right) + \tilde{\delta}\left(t - \frac{2}{4} T_{sw}\right) + \tilde{\delta}\left(t - \frac{3}{4} T_{sw}\right) \\ &+ \tilde{\delta}\left(t - \frac{1+Nm_f}{8} T_{sw}\right) + \tilde{\delta}\left(t - \frac{3+Nm_f}{8} T_{sw}\right) \\ &+ \tilde{\delta}\left(t - \frac{5+Nm_f}{8} T_{sw}\right) + \tilde{\delta}\left(t - \frac{7+Nm_f}{8} T_{sw}\right). \end{aligned} \tag{A.2}$$

For $N = 10$ equation A.1 becomes equation A.3:

$$\sum_{j=1}^{2N}\tilde{\delta}_j(t) = \tilde{\delta}(t) + \tilde{\delta}\left(t-\frac{1}{10}T_{sw}\right) + \tilde{\delta}\left(t-\frac{2}{10}T_{sw}\right) + \tilde{\delta}\left(t-\frac{3}{10}T_{sw}\right)$$
$$+ \tilde{\delta}\left(t-\frac{4}{10}T_{sw}\right) + \tilde{\delta}\left(t-\frac{5}{10}T_{sw}\right) + \tilde{\delta}\left(t-\frac{6}{10}T_{sw}\right)$$
$$+ \tilde{\delta}\left(t-\frac{7}{10}T_{sw}\right) + \tilde{\delta}\left(t-\frac{8}{10}T_{sw}\right) + \tilde{\delta}\left(t-\frac{9}{10}T_{sw}\right)$$
$$+ \tilde{\delta}\left(t-\frac{1+Nm_f}{20}T_{sw}\right) + \tilde{\delta}\left(t-\frac{3+Nm_f}{20}T_{sw}\right)$$
$$+ \tilde{\delta}\left(t-\frac{5+Nm_f}{20}T_{sw}\right) + \tilde{\delta}\left(t-\frac{7+Nm_f}{20}T_{sw}\right) \quad \text{(A.3)}$$
$$+ \tilde{\delta}\left(t-\frac{9+Nm_f}{20}T_{sw}\right) + \tilde{\delta}\left(t-\frac{11+Nm_f}{20}T_{sw}\right)$$
$$+ \tilde{\delta}\left(t-\frac{13+Nm_f}{20}T_{sw}\right) + \tilde{\delta}\left(t-\frac{15+Nm_f}{20}T_{sw}\right)$$
$$+ \tilde{\delta}\left(t-\frac{17+Nm_f}{20}T_{sw}\right) + \tilde{\delta}\left(t-\frac{19+Nm_f}{20}T_{sw}\right).$$

For both (A.2) and (A.3) the Laplace transform can then be carried out normally using the property $\mathcal{L}\{f(t-t_0)\} = F(s)\exp(-st_0)$, as it was done in section 3.5 for $N = 2$.

ADDENDUM B CALCULATION OF ANALYTICAL VALUES

B.1 LINEARLY MODULATED MODULAR MULTILEVEL CONVERTER

$$i_{arm,f} = \frac{1}{2} I_{ac} = \frac{1}{2} \times \sqrt{2} \times \frac{S}{\sqrt{3} V_{LL}} = \frac{1}{2} \times \sqrt{2} \times \frac{200 \times 10^3}{915\sqrt{3}} = 89.2346 \text{ A.}$$

$$i_{circ,DC} = i_{arm,DC} = \frac{1}{3} I_{dc} = \frac{1}{3} \times \frac{S}{V_{dc}} = \frac{1}{3} \times \frac{200 \times 10^3}{1500} = 44.4444 \text{ A.}$$

$$i_{circ,2f} = i_{arm,2f} = I_2 = \frac{\sqrt{(A\cos\varphi + B)^2 + (A\sin\varphi)^2}}{1 - \frac{N}{16\omega^2 C_{SM} L_{arm}} - \frac{m_a^2 N}{24\omega^2 C_{SM} L_{arm}}}$$

whereby

$$A = \frac{3 m_a N I_{ac}}{64\omega^2 C_{SM} L_{arm}}, \quad B = -\frac{N m_a^2 I_{dc}}{48\omega^2 C_{SM} L_{arm}}.$$

Then

$$A = \frac{3 \times 0.996126 \times 2 \times 178.469198}{64(100\pi)^2 \times 3.787234 \times 10^{-3} \times 1.6669 \times 10^{-3}} = 26.749602,$$

$$B = -\frac{2 \times 0.996126^2 \times 133.333333}{48(100\pi)^2 \times 3.787234 \times 10^{-3} \times 1.6669 \times 10^{-3}} = -8.847579,$$

$$i_{circ,2f} = i_{arm,2f} = I_2 = \frac{\sqrt{(26.749602\cos 0° - 8.847579)^2 + (26.749602\sin 0°)^2}}{\left(1 - \frac{2}{16(100\pi)^2 \times 3.787234 \times 1.6669 \times 10^{-6}} - \frac{0.996126^2 \times 2}{24(100\pi)^2 \times 3.787234 \times 1.6669 \times 10^{-6}}\right)}$$

$$= 26.8531 \text{ A.}$$

$$i_{arm,RMS} = \sqrt{i_{arm,DC}^2 + \left(\frac{i_{arm,f}}{\sqrt{2}}\right)^2 + \left(\frac{i_{arm,2f}}{\sqrt{2}}\right)^2}$$
$$= \sqrt{44.4444^2 + \left(\frac{89.2346}{\sqrt{2}}\right)^2 + \left(\frac{26.8531}{\sqrt{2}}\right)^2} = 79.4812 \text{ A.}$$

$$V_c = \frac{V_{ac}}{N}\left(1 + \frac{1}{m_a}\right) = \sqrt{\frac{2}{3}}\frac{V_{LL}}{N}\left(1 + \frac{1}{m_a}\right) = \sqrt{\frac{2}{3}} \times \frac{915}{2}\left(1 + \frac{1}{0.996126}\right) = 748.5471 \text{ V.}$$

B.2 OVERMODULATED MODULAR MULTILEVEL CONVERTER

$$V_{dc} = \frac{2V_{ac}}{m_a} = \frac{2\sqrt{\frac{2}{3}}V_{LL}}{\sqrt{2}} = \frac{2V_{LL}}{\sqrt{3}} = \frac{1830}{\sqrt{3}} = 1056.5510 \text{ V.}$$

$$i_{arm,f} = \frac{1}{2}I_{ac} = \frac{1}{2} \times \sqrt{2} \times \frac{S}{\sqrt{3}V_{LL}} = \frac{1}{2} \times \sqrt{2} \times \frac{200 \times 10^3}{915\sqrt{3}} = 89.2346 \text{ A.}$$

$$i_{circ,DC} = i_{arm,DC} = \frac{1}{3}I_{dc} = \frac{1}{3} \times \frac{S}{V_{dc}} = \frac{1}{3} \times \frac{200 \times 10^3}{\frac{1830}{\sqrt{3}}} = 63.0984 \text{ A.}$$

$$i_{circ,2f} = i_{arm,2f} = I_2 = \frac{\sqrt{(A\cos\varphi + B)^2 + (A\sin\varphi)^2}}{1 - \frac{N}{16\omega^2 C_{SM} L_{arm}} - \frac{m_a^2 N}{24\omega^2 C_{SM} L_{arm}}}$$

whereby

$$A = \frac{3m_a N I_{ac}}{64\omega^2 C_{SM} L_{arm}}, \quad B = -\frac{N m_a^2 I_{dc}}{48\omega^2 C_{SM} L_{arm}}.$$

Then

$$A = \frac{3 \times \sqrt{2} \times 2 \times 178.469198}{64(100\pi)^2 \times 3.787234 \times 10^{-3} \times 1.6669 \times 10^{-3}} = 37.976778,$$

$$B = -\frac{2 \times \sqrt{2}^2 \times 133.333333}{48(100\pi)^2 \times 3.787234 \times 10^{-3} \times 1.6669 \times 10^{-3}} = -25.317852,$$

$$i_{circ,2f} = i_{arm,2f} = I_2 = \frac{\sqrt{(37.976778\cos 0° - 25.317852)^2 + (37.976778\sin 0°)^2}}{\left(1 - \frac{2}{16(100\pi)^2 \times 3.787234 \times 1.6669 \times 10^{-6}} - \frac{\sqrt{2}^2 \times 2}{24(100\pi)^2 \times 3.787234 \times 1.6669 \times 10^{-6}}\right)}$$

$$= 23.8003 \text{ A.}$$

$$i_{arm,RMS} = \sqrt{i_{arm,DC}^2 + \left(\frac{i_{arm,f}}{\sqrt{2}}\right)^2 + \left(\frac{i_{arm,2f}}{\sqrt{2}}\right)^2}$$

$$= \sqrt{63.0984^{\,2} + \left(\frac{89.2346}{\sqrt{2}}\right)^2 + \left(\frac{23.8003}{\sqrt{2}}\right)^2} = 79.4812 \text{ A.}$$

$$V_c = \frac{V_{ac}}{N}\left(1 + \frac{1}{m_a}\right) = \sqrt{\frac{2}{3}}\frac{V_{LL}}{N}\left(1 + \frac{1}{m_a}\right) = \sqrt{\frac{2}{3}} \times \frac{915}{2}\left(1 + \frac{1}{\sqrt{2}}\right) = 637.6849 \text{ V.}$$