A comparison of 3D EM and RC parasitic extraction analysis of mm-wave on-chip passives in SiGe BiCMOS LNAs

Abstract: Layout parasitics significantly impact the performance of mm-wave microelectronic circuits. These effects may be estimated by including foundry-qualified *pcell* interconnect models in schematic with or without additional RC parasitics extraction (RCPE), or by generating an EM simulation (FEM and MoM) of the layout and co-simulating with active device models. In this paper, these methods are compared at by simulating the compression (P1db), gain (S_{21}), and noise figure (NF) of a V-band LNA in 130 nm SiGe BiCMOS and comparing the results of different simulation approaches to measurements. It is found that the FEM co-simulated results agree better with the measurements than the other methods, providing a maximum error of 0.8 dB in gain, 0.18 dB in NF, and 0.6 dB in P1dB. This is a significant improvement over the errors obtained with *pcell*-based schematic (2.6 dB in gain, 0.1 dB in NF, 2.2 dB in P1db), schematic simulation with RCPE (1.55 dB in gain, 1.15 dB in NF, 0.8 dB in P1db) and MoM co-simulation (0.67 dB in gain, 0.72 in NF and 0.67 in P1db). This experiment validates the preference to FEM co-simulation in mm-wave microelectronic circuits yet would indicate that reasonably accurate first-iteration results may be obtained through a combined *pcell*-RCPE approach with significantly shorter simulation time.

Keywords: low-noise amplifier, MMIC design, mm-wave circuits, parasitic capacitance, electromagnetic simulation

1. INTRODUCTION

The mm-wave frequency spectrum (30 - 300 GHz) offers wide, contiguous bandwidth required for future communications and automotive RADAR applications [1]. The high frequency of operation, however, leads to new challenges for monolithic mm-wave integrated circuit (MMMIC) design compared to monolithic microwave integrated circuit (MMIC) design. In RFCMOS and SiGe BiCMOS, electrical performance is impeded by the low-quality factors attainable by lumped components in the back-end of line (BEOL) interconnects [2] due, in part, to the increased impact of surface roughness and skin effect [3]. Even in lower frequency radio frequency integrated circuit (RFIC) devices, parasitic elements significantly affect circuit performance [4] where bondpads, feedlines, fringing fields [5], geometry variations such as line-edge roughness [6] and quasi-TEM propagation [7] are the major contributors.

The short mm-wave wavelengths allow for the use of distributed and transmission line components on-chip. These are typically modeled using 2.5D or 3D electromagnetic (EM) solvers[8–11], both in CMOS / SiGe BiCMOS and III-V technologies such as GaAs[12] and GaN[13]. However, the extreme aspect ratios, a multitude of thin dielectric layers, and dense via arrays often lead to impractically large mesh sizes. Feasible simulation models require major simplifications [11 14 15], including the segmentation of the model into small sectors [16] and the application of 2.5D geometry approximations [17 18]; all of which reduce the accuracy of the simulation. In addition to mesh generation difficulties, EM co-simulation is complicated by the interaction between microelectronic EDA tools and 3D EM tools [19].

An alternative to full-wave analysis of mm-wave interconnects on-chip is RC parasitics extraction (RCPE) for inclusion in the netlist, for which several algorithms have been proposed [20]. Quantus RC (QRC), a popular extension to the Cadence Virtuoso IC IDE, performs parasitic extraction through a 3D random walk field solver to detect interconnect capacitances and resistances [21]. On the other hand, interconnect inductance and transmission line effects (which are of greater importance in MMMIC design than MMIC design) can be accounted for by using appropriate distributed element *pcells* from the foundry PDK in schematic simulation. RC parasitics extraction with foundry *pcells* has been applied successfully at Ka-band [22], V-band [23] and even W-band [24], despite the more recent trend to favor EM-based approaches. Mixed EM-RCPE approaches have also been proposed [11], while EM simulation may be used to manually extract device parasitics for circuit modeling [25 26]. Although design kits for III-V technologies typically do contain active and distributed element *pcells*[27], additional RC parasitics extraction is not commonly followed in published literature. This may be due to the fact that the relevant RC parasitics extraction tools are created for CMOS EDA tools with VLSI integration in mind [28], while III-V design kits are typically created for RF circuit simulators such as Agilent ADS[29 30] or NI AWR Microwave Office[31].

A few works[8,32] in published literature have attempted a direct comparison between EM and RCPE-based approaches to RFCMOS circuit modelling. For the 2.4 GHz LNA[32], it is found that using a MoM-based EM solver leads to greater first-iteration accuracy than a pure RCPE-based approach, but that non-negligible errors persist. In addition, this study does not make use of foundry-qualified *pcells* for transmission line interconnects, as the guided wavelength is far larger than the circuit size. At K-band, RCPE extraction has been applied[8], but found to be less accurate than 2.5D MoM solver. The study did not also consider interconnect *pcells*, nor was the FEM solver's efficacy evaluated.

In this paper, we compare the accuracy of the *pcell*-based schematic simulation, with and without additional RC parasitic extraction, to on-chip FEM and MoM simulation in predicting the performance of a 62-68 GHz LNA in 130 nm SiGe BiCMOS. Results are compared w.r.t. compression (P1db), the input reflected power S11, gain (S21), and noise figure (NF). The work extends on prior studies by considering higher frequencies, including distributed components and their corresponding *pcells*

in the analysis, and including measured NF in the conducting the comparison. The design and modeling approaches are presented in Section II, and are compared to measurement results in Section III. Conclusions and suggestions for future work are presented in Section IV.

2. DESIGN AND MODELING

2.1 Preliminary design and schematic simulation

The circuit under investigation, shown in Figure 1, is a V-band LNA, designed for the GlobalFoundries US 8HP process using the 7-metal layer stack. The design, based on that applied commonly in literature[33] uses two cascaded sections of HBT cascode pairs[33] with emitters dimensioned as shown in Figure 1 and with f_t/f_{max} = 200/260 GHz. Distributed elements are formed as microstrip lines in the AM top metal layer suspended over a large MQ ground plane. Since the application requires the LNA to be packaged individually, GSG interface pads with 150 μm pitch, as well as DC wirebond pads, are explicitly included in the analysis. The signal pad parasitic capacitances were resonated out by connecting RF short-circuited stubs of l = 125 μm across the signal pads, as depicted in Figure 1.

The basic schematic simulation (Figure 1) uses foundry PDK *pcells* for the transmission line elements, the transistors, bondpads, polysilicon collector resistors, and metal insulator metal (MIM) capacitors. Ideal RF choke inductors are used in circuit schematic and were replaced in layout with PDK *rflines* as shown in Figure 2, whose layout properties are similar to distributed element inductors. This approach, which assumes ideal interconnects between pcell elements and no parasitic capacitance, results in a simulation that estimates a circuit response that is impedance matched over the band of interest to below -10 dB (Figure 7) with 1dB gain flatness bandwidth in excess of the 6 GHz under consideration (Figure 6), midband gain of 15.2 dB and NF (Figure 8) of below 7.5 dB, when biased (as shown in Figure 1) with constant base currents and powered by a source of -30 dBm. This draws a collector current equal to 4.5 mA from a 2.3 V supply.

2.2 Layout and parasitic extraction

Based on this schematic simulation, the DRC, LVS and pattern density compliant layout shown in Figure 2 is generated on the 8HP 7 metal layer back-end-of-line (BEOL). Including pads, the design occupies 1.154 × 0.688 mm and uses constant-current biasing.

Based on this layout, the QRC package was used to extract parasitic resistors and capacitors. From this extraction, a new netlist, which includes both *pcells* and the obtained extracted parasitic elements, is generated. These were re-analyzed in circuit simulation (in this case, SpectreRF) using the S-parameter and harmonic balance analyses.

This updated *pcell*-RCPE simulation predicts 1dB flatness gain bandwidth of ≈5.7 GHz, with a midband gain reduced and input reflection, increased to 15 dB and -10.95 dB respectively. The midband NF is also found to be 6.95 dB, which is much lower than what was obtained in schematic simulation using the foundry *pcells* alone.

On-chip antennas, particularly at millimeter-wave frequencies, have been called “the last barrier” in full system-on-chip (SoC) integration [1] because of the many pitfalls associated with their implementation. These challenges include the reduction in their performance because of both the small effective aperture and high silicon losses, as well as the large (and costly) chip area that they occupy. The former problem can be studied and mitigated by effective full-wave electromagnetic (EM) modeling pre-production [2], [3], whilst the latter necessitates a minimum of prototyping cycles and, consequently, a good first-iteration accuracy of 3D EM modeling.

Full-wave 3D EM modeling of large on-chip passives is complicated, complex, time-consuming and resource demanding. This is due to the extreme aspect ratios (include transmission lines of several hundred microns often connected to vias of below a micron in diameter) and a multitude of thin dielectric layers, both of which contribute to large mesh sizes. These challenges are often aggravated by surface roughness and skin depth, demanding for significant model geometries simplifications [4] such as of the omission of some dielectric layers [5]. The consequence of such simplifications is reduced first-iteration accuracy, with a deviation of several hundred MHz [5] for f_0 of resonant antennas above 60 GHz.

In this paper, we investigate how a stack-up can misguide RFIC designers w.r.t the performance estimation of mm-wave on-chip antennas during EM verification. The study is focused on the resonance frequency f_0 drift and S_{11} degradation, as a result of BiCMOS8HP stack-ups simplifications.

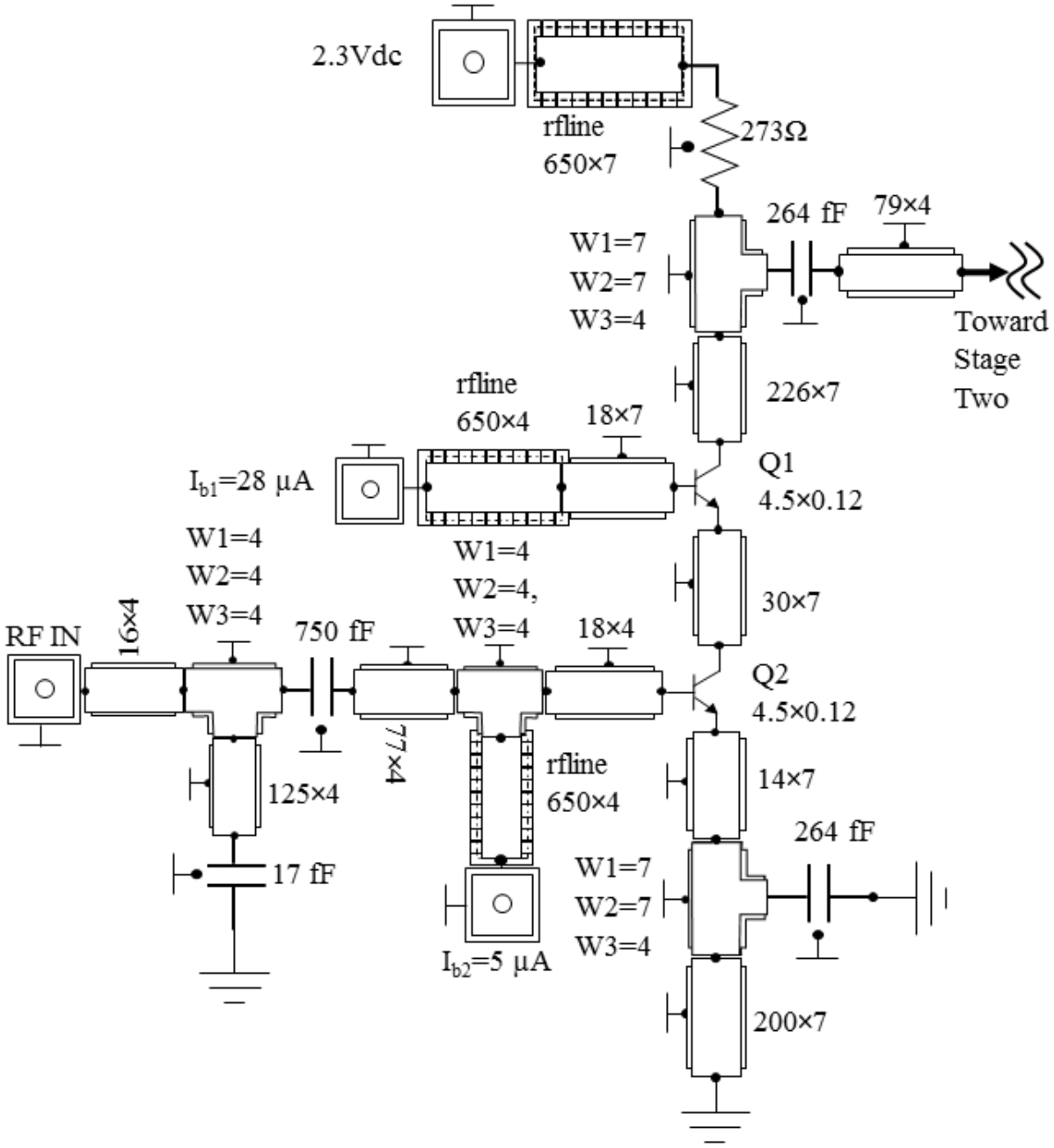

FIGURE 1 LNA schematic simulation of the LNA using *pcells*. The second stage is a duplicate of the first stage. All *pcells* dimensions are in µm.

2.3 EM co-simulation

For EM co-simulation, the layout in Figure 2 is first exported to GDSII and segmented into small transmission line sectors (as indicated in Figure 3) as solution of the full layout in one pass resulted in a mesh too large to solve on a PC, confirming similar observations in literature[16]. As sections are shielded by MQ ground planes and spaced several multiples of microstrip line height apart, minimal stray coupling between sections is anticipated. Each block is then simulated using both FEM and MoM solvers in Ansys HFSS, where MQ metallization is set as a ground plane. HFSS edge ports were placed between AM and MQ layers as depicted Figure 3, where it is also shown that the AM-M1 via stack is meshed to account for interconnect parasitics not modelled in the transistor *pcell*. Radiation boundaries were used as boundary conditions and the analysis was conducted from 62 to 68 GHz using zero-order basis functions, with the mesh size refined to the maximum frequency of interest. Foundry-qualified *pcell* data on MIM capacitors were retained, the lumped-element network approximation was considered appropriate for circuit simulation and insufficient process data was available to replicate the capacitors in FEM. The resulting S-parameters were saved as separate Touchstone files, and the interconnects replaced by their equivalent S-parameter blocks in schematic simulation as shown in Figure 4. This approach effectively replaces the distributed elements and interconnects with EM simulated blocks, noting that the layout parasitics of active devices and lumped components already form part of the foundry-

qualified *pcells*. Since the Touchstone files do not describe the DC and low-frequency AC characteristics of the n-port interconnects, appropriate DC biasing paths are created using ideal 1nH inductors with 1pF capacitors to create AC grounds as shown, to enable accurate harmonic balance analysis. The 17 fF capacitor to ground in Fig. 1 is used to provide a virtual ac ground to the 125 µm long stub, thus behaving as broadband short-circuited stub.

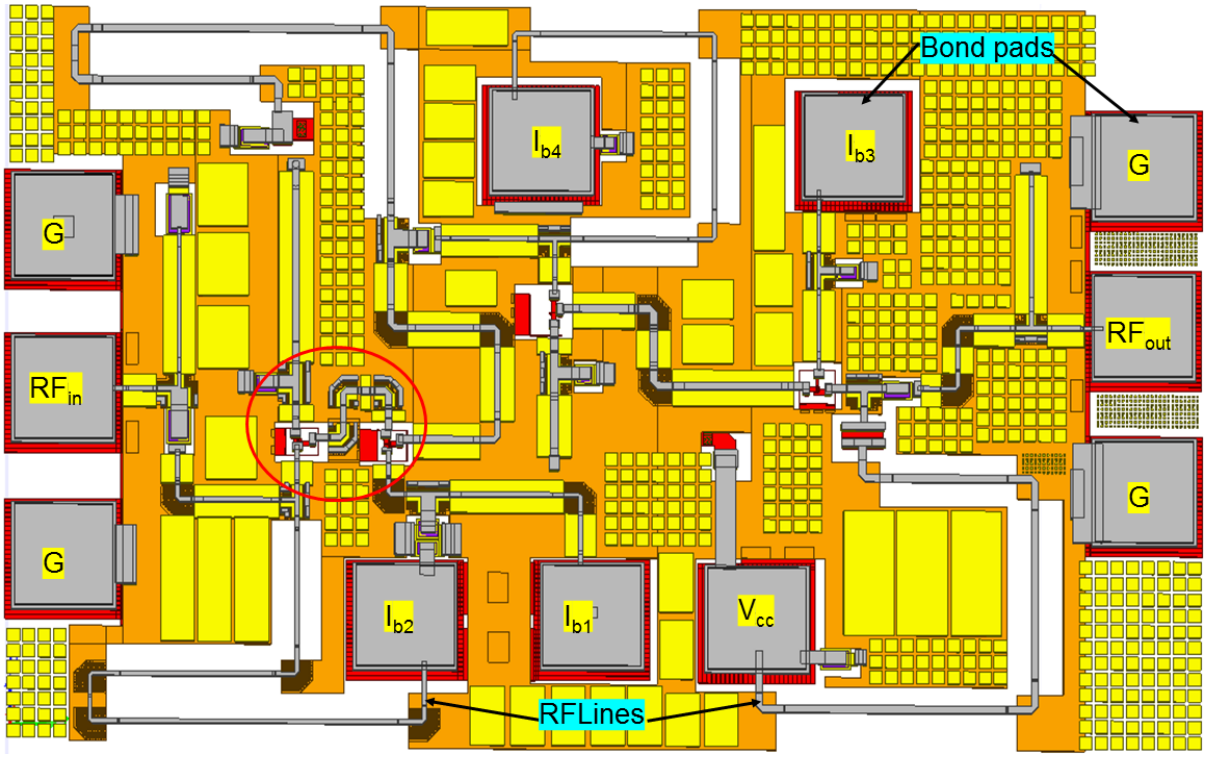

FIGURE 2 On-chip layout of the LNA

The FEM method predicts LNA midband gain and NF of 14.9 dB and 7.53 dB respectively, and a 1dB gain flatness bandwidth of 4.03 GHz, which is a 1.97 GHz reduction from the circuit simulation's estimate. The EM co-simulation estimates input return loss of below -13 dB across the band of interest, which is significantly lower than that estimated from *pcell* and *pcell*-RCPE schematic simulation. The MoM method, in turn, predicts an LNA midband gain of 15.53 dB with the NF of 6.7 dB, 0.72 dB less than the measured value. The MoM also predicts an improved 1dB gain flatness bandwidth as compared FEM based co-simulation, but with center frequency shifted to the low frequency side (63.41 GHz). This shift could be attributed to the inaccuracy of MoM in the modeling of the silicon substrate, while the higher gain may be due to the omission of surface roughness in the simulation.

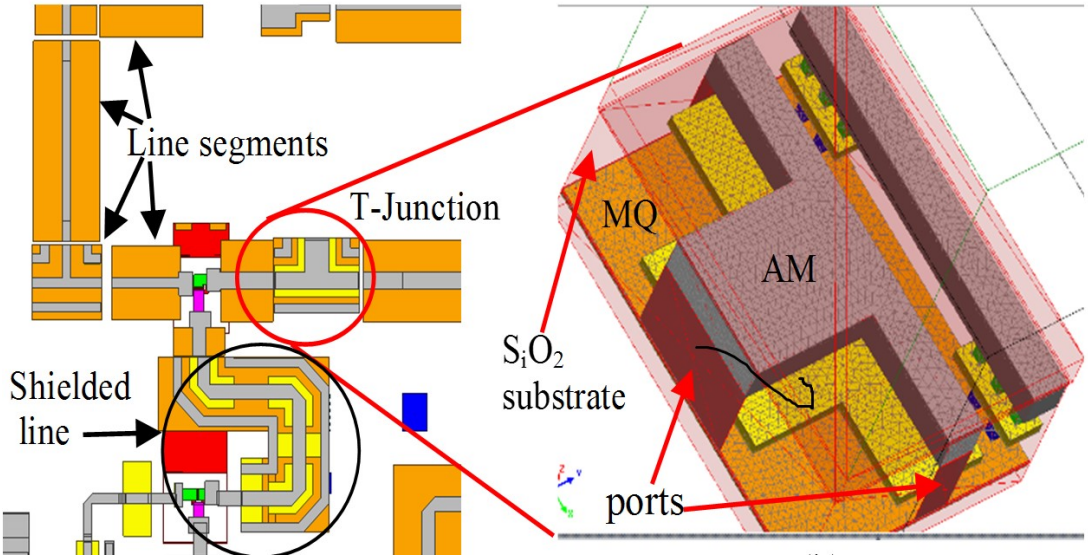

FIGURE 3 Segmentation of the line structure for FEM simulation

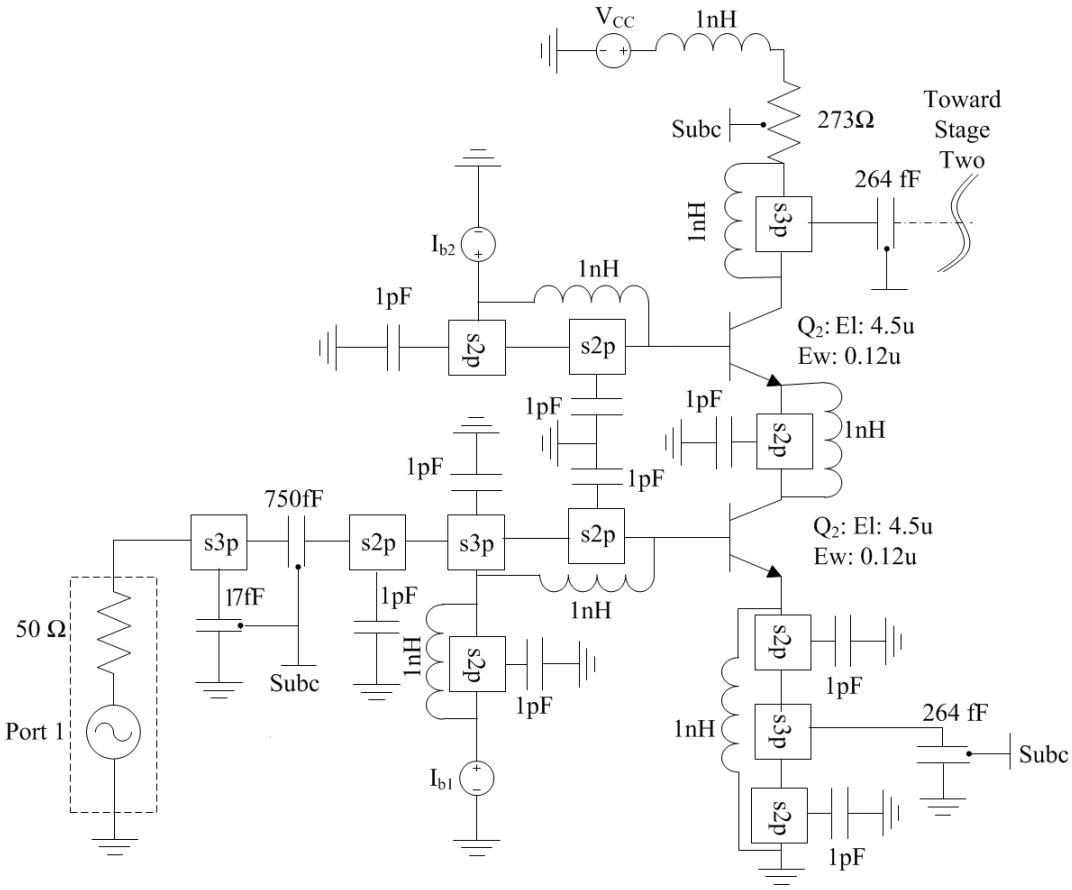

FIGURE 4 Schematic simulation in which transmission lines are replaced with S-parameter files

3. MEASUREMENT AND DISCUSSION

The layout generated in Figure 2 was fabricated (shown in Figure 5) as part of a multi-project wafer run. S-parameters at -30 dBm input power were obtained using an Anritsu ME7828A VNA using single-tier LRM calibration up to the tips of the GGB 110H GSG probes. Noise figure measurements were conducted on a Rohde & Schwartz FSW50 signal analyzer, using an external Sage Millimeter STG-15 noise figure and gain test set. In both cases, external constant bias current was sourced from an HP 4155B parameter analyzer and applied through four DC needles.

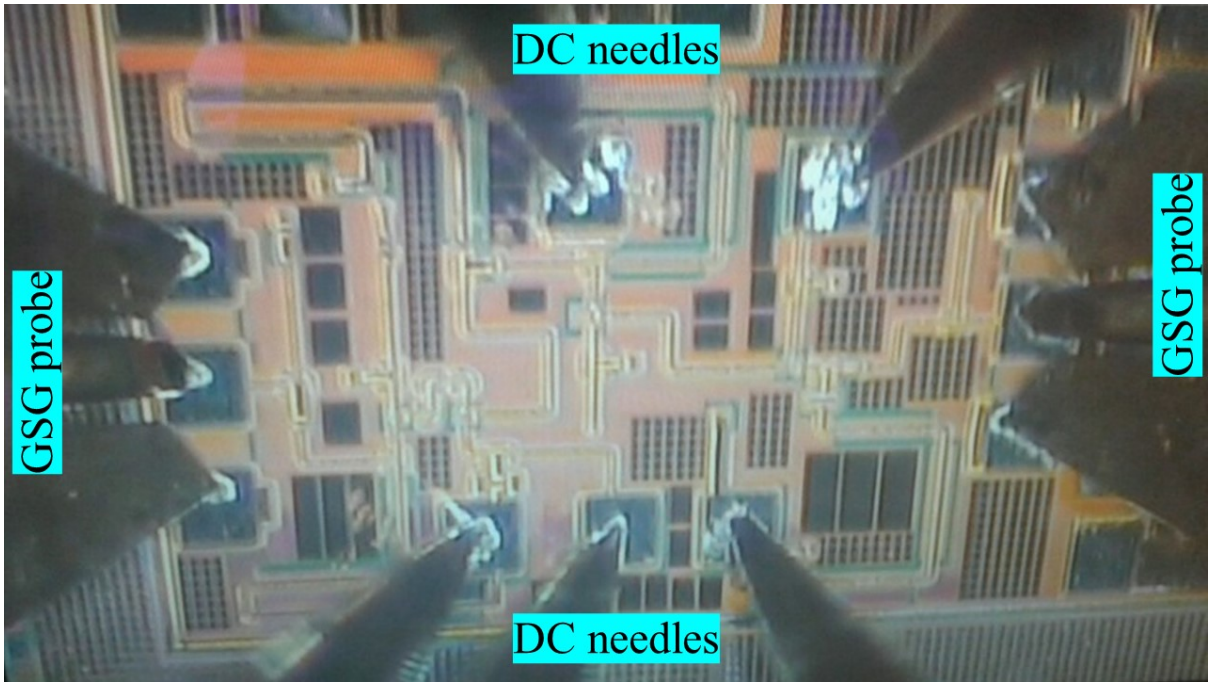

FIGURE 5 Micrograph of the LNA chip under test

The *pcell* schematic simulated, RCPE and EMs co-simulated gain responses are plotted alongside the measured $|S_{21}|$ in Figure 6, while the same comparison is done for $|S_{11}|$ in Figure 7. It is evident that, although the QRC and MoM simulated results also predict a reduction in 1dB gain flatness bandwidth, the FEM based EM co-simulated response best approximates the measurement response at these frequencies (Table 1). A notable difference is that the FEM analysis predicts lower gain and reflected power magnitude at the input port, which may be attributed to consideration of radiated and dielectric loss not considered in the schematic or QRC analyses, as well as the consideration of parasitic inductance. Similarly, the four approaches are compared w.r.t. NF in Figure 8. Here, the RC extraction and MoM based simulation predicts an improved NF compared to pure schematic simulation with *pcells*, while the FEM co-simulation ultimately approximates the measurement results the best over the band of interest. The improved estimates in NF is a direct result of the improved estimate of matching network loss. Likewise, the comparison w.r.t the input-referred 1dB compression points is done in Figure 9. Although all four experiments seem to closely predict P1dB, it is again the FEM approach that best estimates compression. The midband and band-edge errors are tabulated in Table 1, alongside with similar analyses for recent RF and mm-wave integrated LNAs.

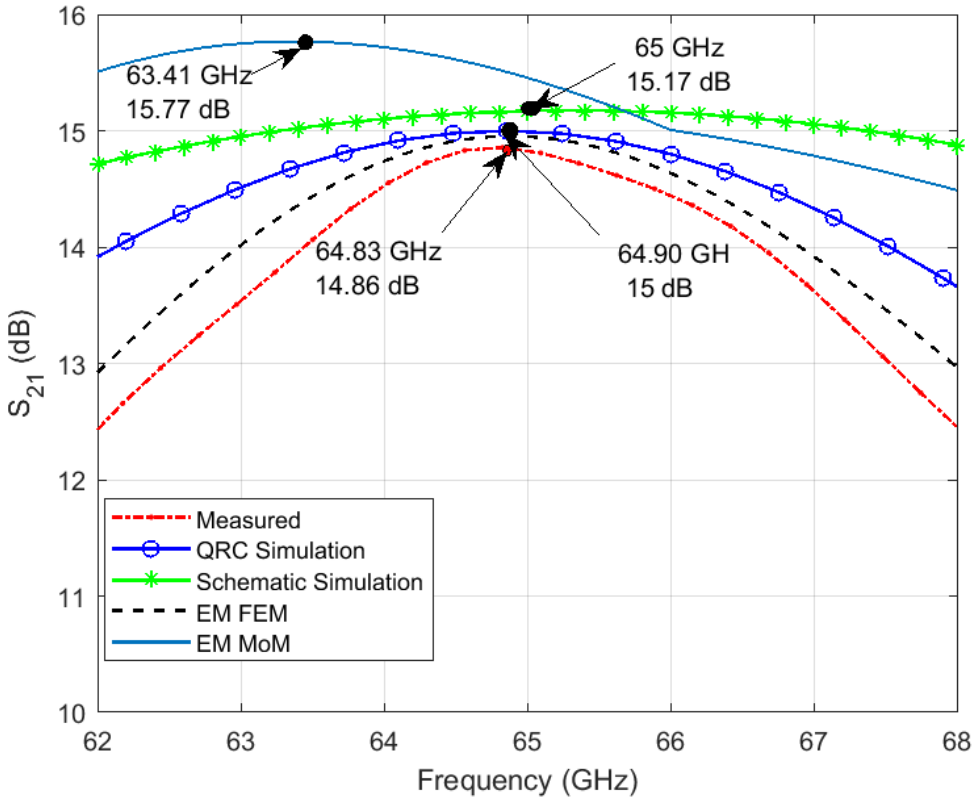

FIGURE 6 Simulation and measured result of S_{21}

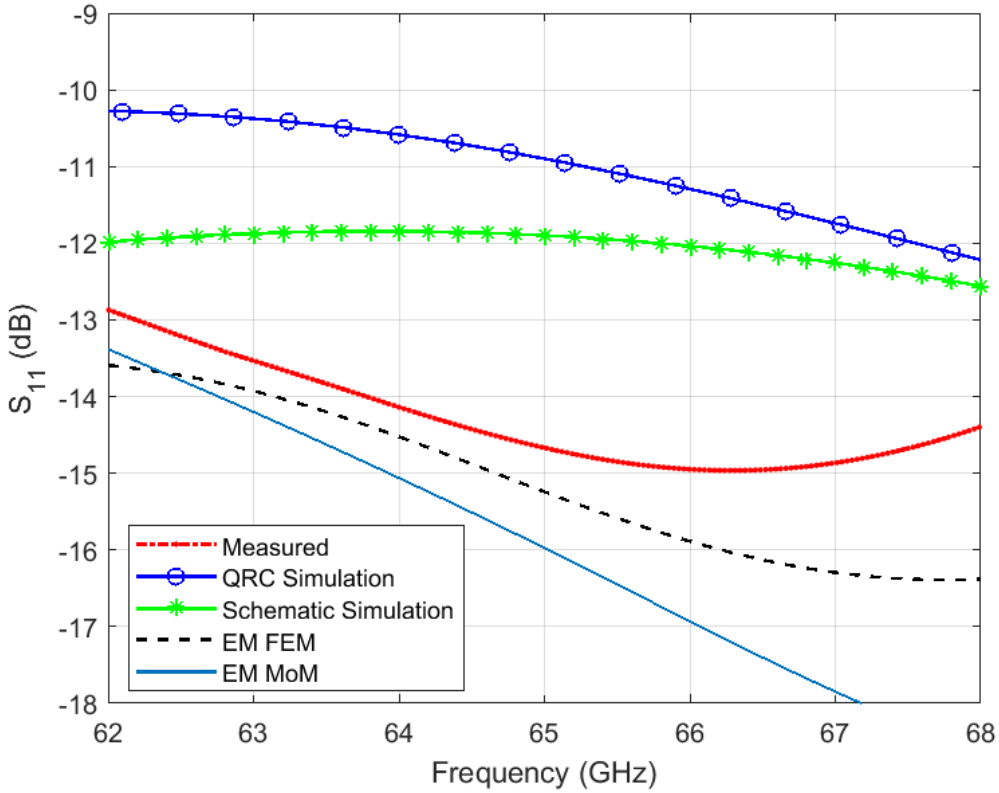

FIGURE 7 Simulation and measured result of input reflection S_{11}

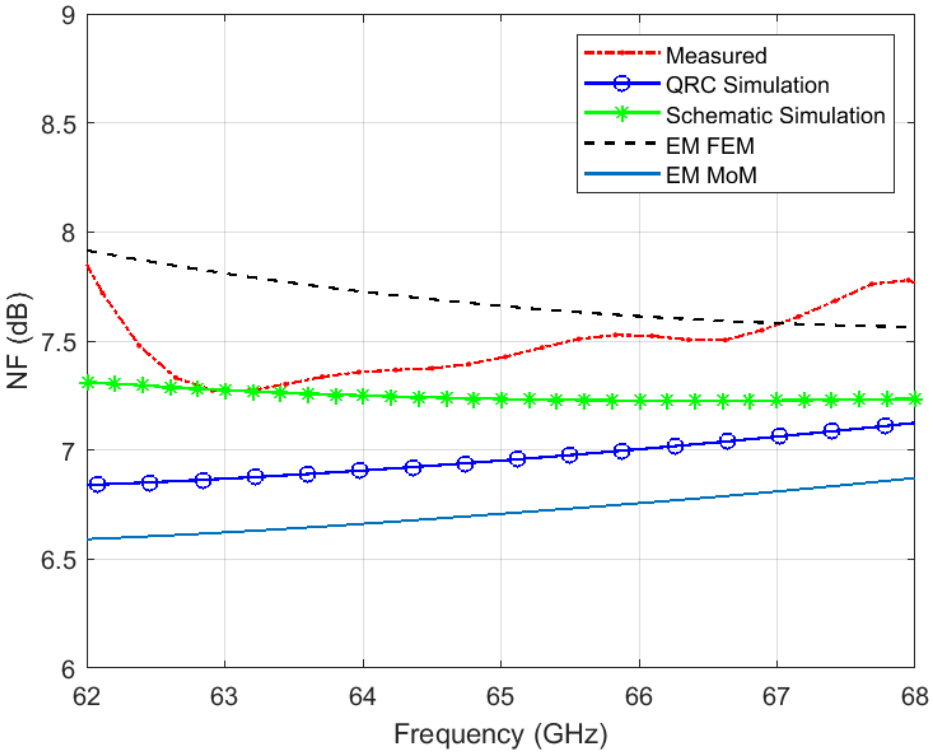

FIGURE 8 Simulation and measured result noise figure

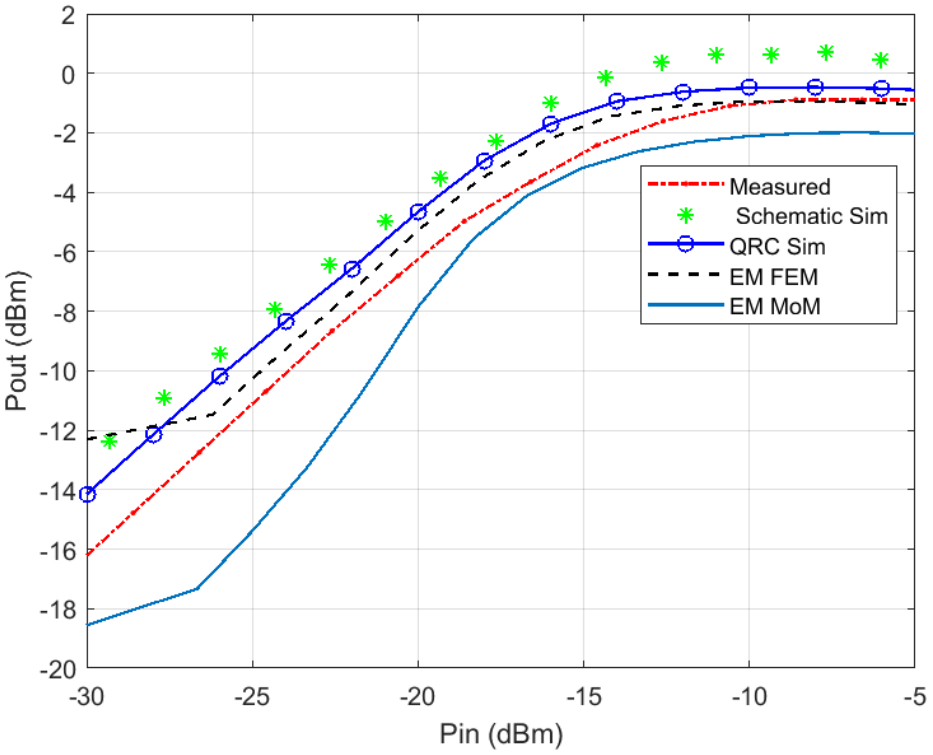

FIGURE 9 Input refered 1 dB compression point

TABLE 1: LNA EM co-simulations vs. RCPE performance comparison

	(GHz)	Approach	Midband gain (dB)	Gain error, midband (dB)	1dB Gain flatness BW (GHz)	Gain BW error (GHz)	Midband NF (dB)	Midband NF error (dB)	Measured P1db, midband (dBm)	P1db error (dBm)
This work	65.2	Pcell schematic	15.2	0.36	>6	>2.44	7.25	0.19	-14	-2.2
	65	Pcell schematic + QRC	15	0.14	5.7	2.14	6.95	0.49	-15.4	-0.8
	65	3D EM co-sim	14.95	≈0.1	4.03	0.47	7.66	-0.23	-15.6	-0.6
	63.4	2.5D EM co-sim	15.77	0.67	>5	1.44	6.7	0.72	-16.84	0.64
[8]	24	3D EM co-sim	8.2	-1.6	4.4	-1.4	*	-	-	-
	23.7	Schematic + RC	4.8	1.8	1.4	1.6	*	-	-	-
[32]	2.5	3D EM co-sim	21.8	4.2	0.2	-0.2	2.3	-	-	-
	2.3	Schematic + RC	24	2	0.5	0.1	2.5	-	-	-
[34]	0-11	Schematic sim	17.2	-0.2	>10	-2.5	*			
	0-11	3D EM co-sim	16.2	0.8	>6	1.5	*	-	-	-

- The measured Noise Figure results were not provided

All the approaches are further compared w.r.t. simulation time in Table 2, as completed on an Intel® Core™ i5 computer with 10 GByte RAM and 64-bit Windows operating system. It is evident that the FEM and MoM simulation approach requires an order of magnitude more simulation time compared to RCPE. These two methods also incur several more processing steps as compared to RCPE. Even then, it is evident that RCPE simulation is better suited to an iterative design optimization process [35], while FEM simulation should be reserved for final design sign-off.

TABLE 2. Post-layout simulation time span for the 2.5D/3D EM, RCPE and HFS

Experiment	Schematic	RCPE	FEM	MoM
File segmentation (min)	0	0	100	100
Analysis setup (min)	20	30	5	5
EM simulation (min)	0	0	610	480
Touchstone import (min)	0	0	45	45
Co-simulation (min)	0	6	100	100
Schematic simulation (min)	30	30	16	16
Total Run Time (min)	50	66	876	746

4. CONCLUSION

The relative accuracies of RC parasitics extraction and EM co-simulation methods are investigated for mm-wave LNA designs where foundry-qualified *pcells* of both lumped and distributed components are applied. It is found that, although RC extraction and MoM co-simulation indicate bandwidth reduction, FEM co-simulation ultimately provides the best estimates of measured gain, noise figure, and linearity (P1dB). This result validates the use of 3D EM co-simulation tools for increasing first-iteration prototyping accuracy in MMMICs but also highlights the increased computational cost. The combined *pcell* and RCPE approach is shown to require an order of magnitude less simulation time, whilst providing reasonably accurate data for optimization of first-pass designs. In particular, it is shown that the addition of RCPE to *pcell* analysis improves the performance estimate significantly with only a minor penalty in additional simulation time. Future work will extend this comparison to III-V processes such as GaAs or GaN, though the addition of RC parasitics extraction would be subject to the availability of process data implemented for a suitable RC parasitics extraction tool. In addition, the applicability of this approach to different LNA circuits such as differential LNA[36,37] and single-ended multistage LNA[38] (not just simple two-stage cascade designs), as well as to mm-wave power amplifiers, should be investigated in future work.

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