MATHEMATICAL MODELLING OF LOW-FREQUENCY BICMOS NEAR-INFRARED DETECTORS

by

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SUMMARY

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Bipolar complementary metal-oxide semiconductor (BiCMOS) technology is the platform of choice for near-Infrared (IR) detector research because of low power consumption, increased operating speed and a high fill-factor. The drawback is poor noise performance which can be attributed to the readout circuitry of the detector. Conventional near-IR detector design is an iterative process. While recognising the value of this approach, rapid prototyping can be achieved by using mathematical modelling that would ensure design repeatability.

Heterojunction bipolar transistor (HBT) and metal-oxide field-effect transistors (MOSFET) models for SiGe process technologies have been documented extensively. However, mathematical modelling of BiCMOS near-IR detectors has not been implemented in a complete working system before. This proposed model can be used to determine the output voltage as well as the noise performance of near-IR detectors.

The focus of this research is to determine how process independent parameters and detector performance can be mathematically modelled. Secondly, and associated to this, is determining how the model can be extended to accommodate multiple feature sizes including short-channel MOSFETs.

An implementation of this model on the three-transistor pixel structure, using reverse-biased diode-connected HBTs as pixels, was done as part of the experimental verification process of this research. The implementation was done in a 2 × 2 gated array detector configuration. The validity of the proposed modelling procedure was verified through comparison of simulations and measured results. The simulations were done in an iterative fashion to show how a deviation in one process independent parameter affects the noise performance, while the other process independent parameters are kept constant. The detector design with optimal noise performance can be achieved in this manner, thereby minimising design time and developing optimised detectors without the need for extensive prototyping.

The main contribution of this research is that a designer can use this mathematical model to tune a detector to achieve desired performance. By changing the temperature, biasing voltage and biasing current and choosing the aspect ratio, noise performance changes. An iterative process in the mathematical model development can achieve optimised parameters for noise performance. Two approaches, namely DC analysis and *y*-parameter representation, were used to develop the mathematical model. Feedback was taken into account using the *y*-parameter representation.

The measured results show that the output voltage behaviour follows the mathematical model developed. The output voltage behaviour also shows that the mathematical model parameters can determine noise performance. As an extension to this work, the same modelling process can be used to develop mathematical models for other detecting structures such as the four-transistor pixel structure.

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LIST OF ABBREVIATIONS

3T	Three Transistor
4T	Four Transistor
ADE	Analogue Design Environment
AR	Aspect Ratio
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
CCD	Charged-Coupled Device
CDS	Correlated Double Sampling
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
DR	Dynamic Range
DRC	Design Rule Check
EDA	Electronic Design Automation
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
IR	Infrared
LVS	Layout Versus Schematic
MOSFET	Metal-Oxide Field-Effect Transistor
NDA	Non-Disclosure Agreement
PCB	Printed Circuit Board
PDK	Process Design Kit
QE	Quantum Efficiency
Si	Silicon
SiGe	Silicon-Germanium

SNR	Signal-to-Noise Ratio
TIA	Transimpedance Amplifier
ZTC	Zero Temperature Coefficient

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CHAPTER 1 INTRODUCTION

1. CHAPTER OVERVIEW

This thesis documents the development of a mathematical model that can be used to optimise near-infrared (IR) bipolar complementary metal-oxide semiconductor (BiCMOS) detectors. The focus is on detector parameters (aspect ratio (AR), temperature, biasing voltage and biasing current) that the designer can change, thereby making it possible to optimise the signal-to-noise ratio (SNR). This chapter outlines the motivation and background of this research and defines the research questions. The research goals and contribution to the body of knowledge is also presented.

1.1 PROBLEM STATEMENT

1.1.1 Context of the problem

Complementary metal-oxide semiconductor (CMOS) array detectors have received significant interest from researchers based on their speed, ease of integration and fabrication costs [1]–[7] [8] [9] . Non-silicon IR detectors have been reported in literature but have difficulties with integration into silicon (Si) integrated circuit (IC) technologies [10]. Silicon-germanium (SiGe) IR arrays offer a low-cost alternative for the development of detectors that do not require cooling [11]. Work in readout circuit have been reported for specific implementations of detectors [12] [13] but a generic mathematical model is lacking. Limitations of these detectors range from detectable radiation to on-chip intrinsic noise, which deteriorates performance. Charged-coupled devices (CCD) present excellent performance in most aspects of sensor technologies but integration with Si electronics is a

shortcoming. BiCMOS detectors, however, have all components housed on a single piece of wafer, which reduces these integration issues significantly, although there are common problems, namely decreased fill-factor and large on-chip noise, associated with BiCMOS gated array detectors. SPICE modelling of SiGe HBTs for operating temperatures down to 77 K have been reported in [14]

The contribution of this research is a mathematical model used to optimise performance of BiCMOS near-IR detectors. In addition to this, since readout circuitry can be prototyped with short-channel devices for high-speed applications, no mathematical modelling has been done to accommodate short-channel devices where velocity saturation has an effect on performance.

Some detector performance parameters are process dependent, which means if the designer wants to change them, the designer has to move to another technology node.

However, there are some parameters that are not process-specific, and a designer can tune them to achieve a specific need. Non-process-specific parameters include emitter length (in the case of a heterojunction bipolar transistor (HBT)) and the AR (in the case of a metal oxide semiconductor field-effect transistor (MOSFET)). In addition to this, biasing voltage, biasing current and temperature can be changed by the designer even after manufacturing for various operating conditions. The process of choice for this work is a BiCMOS process. Table 1.1 compares this work with other implemented detectors found in literature.

Table 1.1 Comparison of other published work with this work.

Reference	**[11]**	**[15]**	**[16]**	**[17]**	**[18]**	**[19]**	**This work**
Technology node	0.35 µm CMOS	180 nm CMOS	180 nm CMOS	130 nm CMOS	130 nm CMOS	45 nm CMOS SOI	**0.35 µm BiCMOS**

Reference	**[11]**	**[15]**	**[16]**	**[17]**	**[18]**	**[19]**	**This work**
Array size	128 × 128	-	64 × 64	-	-	1 × 1	**2 × 2**
Pixel size	40 µm × 40 µm	-	30 µm × 30 µm	-	-	-	**6.6 µm × 11 µm**
Pixel area	-	60 × 60 μm^2	-	-	-	-	**-**
Chip size	6.5 mm × 6.5 mm	-	3 mm × 3 mm	-	-	0.45 mm × 0.45 mm	**1.3 mm × 1.3 mm**
Noise	0.76 $\mu V/\sqrt{Hz}$	72 $\mu V/\sqrt{Hz}$	-	-	50 $nV/\sqrt{Hz}$	20 $\mu V/\sqrt{Hz}$	**2 $\mu V/\sqrt{Hz}$**
Dynamic Range	-	-	54 dB	47 dB	-	-	**66 dB**
Sensitivity	4970 V/W	0.1 A/W	2750 V/W	26.8 mV/dB	5000 V/W	3000 V/W	**180000 V/W or 180 mA/W**
Power consumption	-	23.4 mW	125 mW	0.1 mW	-	200 µW	**10 mW**

Table 1.1 gives the dynamic range (DR) which is the ratio of the pixel saturation level to its signal threshold whereas the focus of this research is to develop a mathematical model to optimise the SNR. DR can be used as a basis to calculate the SNR. The last column "This work" refers to a prototype that was developed by the author for a previous study which was used as a basis for this work [7].

1.1.2 Research gap

The research gap addressed in this work is the mathematical model for a BiCMOS near-IR detector. Through optimisation, the mathematical model yields the required set of process independent parameters (temperature, AR, bias voltage and bias current) for a set of detector performance parameters. This model can be scaled for design detectors making use of different technology nodes by simply replacing the applicable process dependent parameters. One constraint of using standard fabrication technologies is that some parameters have an effect in a CMOS design that cannot be changed, such as doping densities (N_A, N_D) and oxide thickness (t_{ox}). The mathematical model developed for the purposes of this study, will assist designers in modelling the change in output characteristics such that optimised detectors can be developed and simulated pre-manufacturing, by varying the process independent parameters.

The mathematical model of a BiCMOS detector that was developed as a result of this research considers the process dependent and process independent parameters that directly influence the performance of the detector.

1.2 RESEARCH OBJECTIVE AND QUESTIONS

In this research, mathematical equations were used to develop a model that reduces the effect that process independent parameters have on SNR of CMOS-based detector arrays. The models developed with the use of mathematical relations in CMOS technology should aid designers in optimising performance and allowing for the design of specific parameters. This model should reduce design time, because the detector array can then be designed to specification, thereby reducing cost of development and optimising detector design.

The first research question to answer, is how can process dependent and independent parameters and detector performance be mathematically related?

Secondly, how can this set of mathematical relations, used to link process independent parameters (AR, temperature, biasing voltage, biasing current) to detector performance, be utilised to develop a mathematical model for BiCMOS near-IR detectors?

Thirdly, if a mathematical model can be developed to relate process independent parameters to detector performance, how can this relationship be used to develop an equivalent BiCMOS near-IR detector readout circuit by optimising the SNR?

The last research question is, how the model can be extended to accommodate multiple technology nodes? A key aspect considered in this case is the velocity saturation that occurs when small feature sizes are used and the effects it has on performance parameters such as SNR.

To answer the research questions, the following hypothesis was formulated:

> *'If the SNR in SiGe BiCMOS near-IR detectors can be related to process independent parameters, then a mathematical model can be developed which can be used to enhance the performance of these detectors by optimising the output SNR.'*

1.3 APPROACH

To complete the proposed research successfully, a systematic procedure was developed.

Initially a literature review was conducted to confirm the feasibility of the proposed modelling. An understanding of the effects of process independent parameters and noise in CMOS were required to ensure that the proposed mathematical equations are related process independent parameters. Of the different approaches to reduce the noise contribution in BiCMOS detectors, reducing readout circuit noise had the greatest impact [4] [20].

If the developed mathematical model provided acceptable results, IC simulations (with the use of Cadence Virtuoso) were carried out. Some parameters are generally not given in the process documentation of a specific fabrication technology, as they can be obtained with the

use of parameter extraction techniques. Where necessary, parameter extraction was performed to obtain the necessary parameters.

Once these additional parameters were verified, the simulated detector circuit was used to develop the layout of the detector and subsequent prototype IC. Post-layout verification was conducted prior to the prototype IC being sent for fabrication [7].

The prototype IC was then included in a test package circuit soldered onto a printed circuit board designed and developed by the author and thereafter the input and output parameters were measured. The process independent parameters could be selected, and the resulting SNR can be measured experimentally. Optimisation can be done then to improve the SNR with multiple prototyped ICs.

1.4 RESEARCH GOALS

The goal of this research was to develop a mathematical model for near-IR SiGe BiCMOS detectors that includes all the individual IC elements and overall noise. To show how the overall noise model affects the performance of the detector developed as part of the mathematical model (relating performance parameters to process dependent and process independent parameters), single transistor noise models in the application of BiCMOS detectors have been included. Subsequent measurements to confirm the validity of this mathematical model are included.

1.5 RESEARCH CONTRIBUTION

Researchers have shown significant interest in CMOS-based detector arrays because of their integration ability with Si electronics compared to CCD detectors. The contribution of this research to the body of knowledge is a mathematical model which can be used for rapid detector prototyping to optimise for SNR. Designers will be able to estimate the performance of a BiCMOS-based detector before it is sent off for fabrication. A mathematical model of a BiCMOS detector was developed. This model has been developed in such a way that other

process dependent parameters can be inserted directly into the model. A graphical representation of the developed model is given in Figure 1.

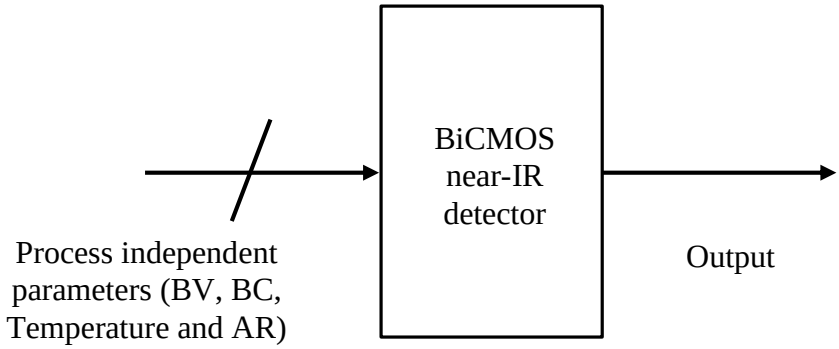


Figure 1. Graphical representation of the detector operation.

where BV is the bias voltage, BC is the bias current, temperature is the operating temperature, AR is the aspect ratio and the SNR is the optimised output parameter which is the information signal comprising of a voltage signal and noise.

Using BiCMOS technology, a detector designer can then obtain a representation of the performance of a detector utilising a fabrication process different from the one used in this research. This is time-consuming and costly exercise to investigate. Since the parameters are documented, the designer can simply insert different values for these process parameters (dependent and independent) and obtain the necessary results. The model developed are assumed to be valid for other processes, but this cannot be documented until experimentally verified.

The outcome of this study is a model that consists of a set of equations that describe the detector performance in relation to process parameters (dependent and independent). The designer can then calculate the process independent parameter values to achieve the desired performance.

A detailed list of the contribution to the body of knowledge is given:

- A detailed set of mathematical equations combine to form a model that illustrates the performance of a near-IR detector. There are several published BiCMOS and CMOS detectors, however, circuits were constructed from first principles with each detector development. This takes up considerable time and it is often not optimised. Designers can develop optimised detectors using this model.
- The derived equations contain process dependent and process independent parameters. Process dependent parameters are parameters that contain process specific values that a designer cannot change unless a designer moves to another fabrication process. Process independent parameters (temperature, biasing voltage, biasing current and AR) can be changed during the development of the detector. The designer can estimate the performance before manufacturing by analysing the resulting SNR. The MATLAB™ `math`-function can be used to calculate a process independent parameter value when an SNR value is chosen. The designer can still change the performance to some extent after manufacturing by changing the temperature, biasing voltage and biasing current.
- The derived equations that forms the model are given in two forms:
    - The first is the DC representation where the output voltage is derived from photon-generated current flow of the pixel using well known large-signal equations for bipolar junction transistors (BJTs) and MOSFETs.
    - The second form is a small-signal representation of the output voltage derived from the photon-generated current flow using *y*-parameter representation. The derived model uses feedback to show the corrective nature of the readout-circuitry which reduces noise.
- A successful implementation of one detector using this model has been demonstrated through design and simulation on a three transistor (3T) pixel structure. Prototyping of this detector was done in a 0.35 µm SiGe HBT process from ams AG (formerly austriamicrosystems AG). Maximum Quantum Efficiency (QE) was obtained at 665 nm wavelength which is also the maximum sensitivity of 180 mA/W for the complete near-IR detector.

- A Si detector prototyped on the same chip measured a sensitivity of 60 mA/W at 665 nm wavelength. The measured noise was 2 $\mu V/\sqrt{Hz}$ with a power consumption of 10 mW. A measured rise of 0.1 V at the lower voltage level is seen when illuminated with a laser emitting radiation with a power output of 1 mW in the 630 nm to 680 nm wavelength band. The corresponding intensity of the laser is 31 mW/cm^2. These measured results show good correlation with simulations where a proportional increase is seen when illuminated.
- The accuracy of this model has been verified through simulations as well as measured results. The measured results correlate with the expected simulated results. Shortcomings such as biasing voltage fluctuations were taken into account and the detector performed as expected.
- This model can be used in electronic design automation (EDA) software where three of the four process independent parameters are kept constant and the last one is varied within acceptable values. This can be done interchangeably with the other parameters.
- Measured results of a single SiGe HBT are presented as a detector at room temperature. They were needed to determine the effect that the readout circuitry would have on the overall performance:
    - For I-V measurements, a current density of 1160 $\mu A/\mu m^2$ was measured at 3 V biasing voltage for the base-emitter shorted HBT where 1740 $\mu A/\mu m^2$ was measured for the base-collector shorted HBT. A flat response was observed for negative biasing voltage for base-emitter shorted HBT and a negative current density was observed for base-collector shorted HBTs.
    - For C-V measurements, a maximum capacitance of 5 $F/\mu m^2$ and 15 $F/\mu m^2$ for base-emitter shorted HBT and base-collector shorted HBT was measured respectively at the built-in bulk potential.
    - A noise voltage of 36.5 $\mu V/\sqrt{Hz}$ and 12.6 $\mu V/\sqrt{Hz}$ was measured for base-emitter shorted HBT and base-collector shorted HBT respectively.

1.6 RESEARCH OUTPUTS

The following is a list of the accepted publications by the author that formed part of this research activities:

- J. Venter and S. Sinha, "Optimization of 4T Pixel Structure BiCMOS Detectors using *y*-parameter Representation," *IEEE 40th International Conference on Electronics and Nanotechnology (ELNANO)*, Kiev, 22 – 24 April 2020.
- J. Venter, S. Sinha and J.W. Lambrechts, "Characterization of diode-connected heterojunction bipolar transistors for near-infrared detecting applications," *Optical Engineering Journal*, vol. 57, no. 11, pp. 1 – 7, Nov. 2018.
- J. Venter, S. Sinha and J.W. Lambrechts, "Characterisation of Diode-Connected SiGe BiCMOS HBTs for Space applications, "*4th Sensors, Mems and Electro-Optic Systems Conference (SMEOS)*, Skukuza, 11 – 14 September 2016.
- J. Venter and S. Sinha, "Noise Reduction by Pixel Circuit Optimisation in 4-T Pixel Structure Detectors Using Integrated Circuit Technologies," *2015 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS)*, Tel Aviv, 2 – 4 November 2015.
- J. Venter and S. Sinha, "Thermal and Flicker Noise Improvement in Short-Channel CMOS Detectors," *3rd Sensors, Mems and Electro-Optic Systems Conference (SMEOS)*, Skukuza, 16 – 20 March 2014.

The following article by the author has been submitted:

- J. Venter, S. Sinha and J.W. Lambrechts, "Characterization of Base-Collector Shorted and Base-Emitter Shorted Diode-Connected SiGe BiCMOS HBTs for Space Applications," submitted to *Journal of Astronomical Telescopes, Instruments and Systems*.

1.7 DELIMITATIONS AND ASSUMPTIONS

Several pixel structures can be found in literature. For the purpose of this research, the derived mathematical model is based on the 3T pixel structure topology. Cost of prototyping is expensive and acceptable results were obtained with one prototype. The 4T structure is left as an extension of this work.

Only a model for low-frequency noise was developed. Medium-to-high frequency noise modelling, even though it is possible, was omitted since low-frequency noise is dominant in low-frequency CMOS detectors.

Short-channel effects will play a major role as the model changes to accommodate these. They are discussed and modelled in Chapter 2 and simulated in Chapter 4. However, since it is a time-consuming and costly process to prototype, no detector was developed and prototyped utilising short-channel effects. Nonetheless the hypothesis was verified for short-channel implementations both in simulations as well as on the basis of a previous multi-project wafer [21].

1.8 THESIS OVERVIEW

In Chapter 1 the research study conducted is introduced. A summary of the challenges of CMOS detector designs is provided. The hypothesis, research goals and contribution of this research are also given.

In Chapter 2 a literature study was performed. Since this research documents the development of a mathematical model for near-IR BiCMOS detectors, a thorough understanding was required into the mechanisms that affect the performance of a detector. Firstly, all four applicable process independent parameters were discussed. In addition to this, the significance of the mathematical model will be illustrated by referencing work done

in this field to identify the research gap. This last section illustrates the significance of the work and how it will benefit researchers and designers of BiCMOS detectors.

In Chapter 3 the research method is discussed. A thorough description of the process used to develop the models is given. Each parameter's physical influence is discussed separately with respect to detectors. A short description of the software used to develop the detector is provided and the equipment used to verify the results are given.

In Chapter 4 the mathematical and simulations is presented. This illustrates the performance of the detector when realistic values are chosen for three of the process independent parameters and the varied parameter. This is done interchangeably to illustrate the effect of all four parameters. These simulations are compared with measured results to determine the validity of the model. The *y*-parameter representation of the detector is also provided as another avenue to determine the performance of these detectors.

In Chapter 5 the results are discussed and main observations provided. Each set of simulations are discussed to document the effect of each parameter. The results are compared to the simulations to verify the validity of the proposed model.

In Chapter 6 concluding remarks are made. A final short discussion of the results is provided to critically evaluate the research findings in relation to the hypothesis by answering the research questions. Finally, suggestions for possible future work that can be carried out from this work is provided.

CHAPTER 2 LITERATURE STUDY

2. CHAPTER OVERVIEW

Each element that makes up the research hypothesis was investigated separately and documented in this chapter. While conducting the research, it was determined that there are four process independent parameters that affect the SNR, namely temperature, bias voltage, bias current and AR. A designer can then select an SNR value and determine the applicable process independent parameters using the `math`-function in MATLAB™.

Secondly, a short overview of noise has been included as applicable to BiCMOS detectors. This is divided into two sections. The first is low-frequency noise models of transistors and the second is medium- to high-frequency noise. The significance of these is to illustrate which noise frequency is degrading the detector performance and the associated assumptions.

A discussion about previous research in the field of noise performance in BiCMOS detectors is provided. The advantages and shortcomings of the referenced work were also discussed.

A short discussion on small feature size processes, including the short-channel effect, for the selected detector configuration, is provided.

Process dependent and process independent parameters are discussed in Section 2.1. Section 2.2 and 2.6 discusses an overview of noise and its impact, respectively. In Section 2.3, previous work done in this field is discussed. Short channel effects as well as DC

mathematical modelling of a 3T and 4T pixel structures are discussed in Section 2.4 and 2.5, respectively. Finally, Section 2.7 summarises and concludes this chapter.

2.1 PROCESS DEPENDENT AND PROCESS INDEPENDENT PARAMETERS

Because the focus of this research is to develop a mathematical model where an SNR value is selected and process parameters can be calculated to achieve desired SNR, it is important to know which process parameters can be tuned in BiCMOS detectors. The two types of parameters that apply are process dependent and process independent parameters. Each of these are discussed below.

2.1.1 Process dependent parameters

Apart from technology node dependency, the process dependent parameters that adversely affect the SNR performance are mobility (μ_n), oxide capacitance (C_{ox}) and threshold voltage (V_t). Each of these parameters is represented by another set of parameters. This set of parameters are included here for illustrative purposes:

For mobility:

$$\mu_n = \frac{K}{C_{ox}} \tag{2.1}$$

For oxide capacitance:

$$C_{ox} = \frac{\varepsilon_r}{t_{ox}} \tag{2.2}$$

For threshold voltage:

$$V_t = V_{to} + \gamma\left(\sqrt{2\varphi - V_{BS}} - \sqrt{2\varphi}\right) \tag{2.3}$$

As seen in (2.1) – (2.3) there are several parameters that are based on the physics and geometry of the process. For example, the relative epsilon (ε_r) is a set parameter of physics

that cannot be changed. The oxide thickness (t_{ox}) is a thickness dependent on the fabrication technology.

The gamma (γ) and phi (φ) used in (2.3) is given in (2.4) and (2.5):

For gamma:

$$\gamma = \frac{\sqrt{2\varepsilon_r q N_A}}{C_{ox}} \tag{2.4}$$

For phi:

$$\varphi = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{2.5}$$

As seen in (2.4) and (2.5), k is Boltzmann constant (1.3806×10^{-23} J/K) and q is the charge of an electron (1.602×10^{-19} C). Then there are the process dependent parameters which are N_A (acceptor concentration) and n_i (intrinsic carrier concentration). There is one parameter that is process independent, however, namely T (temperature).

By changing to another technology node, the process dependent parameters, taken from the process documentation of that specific technology node, have to be inserted. The desired values can be calculated accordingly.

2.1.2 Process independent parameters

The process independent parameters affecting SNR that can be changed are temperature, bias voltage, bias current and AR. There are limits as to how much each process independent parameter can be varied in this application to ensure that the chip does not operate beyond its manufacturer recommended specifications.

2.2 OVERVIEW OF NOISE

Noise, which is prevalent in any system, are non-linear irregular deviations of the intended level of operation due to physical imperfections in the chosen material. These can range in noise frequency from close to 0 Hz up to many GHz. This can be either voltage noise or current noise. The low-frequency noise band and the medium-high frequency noise band are discussed separately.

2.2.1 Low-frequency noise

Since BiCMOS detectors operate mostly by switching at low speeds, low-frequency noise will be most predominant. The two main types of low-frequency noises of which the dominant ones are flicker noise and thermal noise.

2.2.1.1 Flicker noise

Flicker noise (or 1/*f* noise) is caused by traps associated with contamination and crystal defects. Flicker noise is associated with current flow [22] [23]. Equation (2.6) depicts the noise current resulting from flicker noise for a MOSFET:

$$\frac{\overline{i_i^2}}{\Delta f_{flicker}} = \frac{\omega^2 {C_{gs}}^2 K I_D^a}{{g_m}^2 f} \tag{2.6}$$

where g_m is the transconductance at the operating point (A/V), Δf is the noise bandwidth (Hz), K is a constant for the given device, a is a constant between 0.5 and 2, C_{gs} is the gate-source capacitance of the MOSFET, and f is the noise frequency. It is difficult to set parameters for flicker noise, since the parameter K is dependent on crystal imperfections in a given wafer, which can vary from transistor to transistor even if it is on the same wafer.

By using the SiGe HBTs, 1/*f* noise is reduced when compared to other transistors such as gallium arsenide HBTs [24]. Furthermore, the geometry of the SiGe HBTs scales inversely with the emitter area, as seen in (2.7):

$$S_{I_B} = \frac{K}{\beta^2}\frac{1}{A_E}\frac{I_C^2}{f} \tag{2.7}$$

Several deductions can be made from (2.7). The two most striking ones are that the base current noise is inversely proportional to the β squared and also inversely proportional to the surface area of the emitter. The time-domain equivalent of this value is added to the i_{PH} parameter to include noise, since the HBT is in a diode-connected configuration.

2.2.1.2 Thermal noise

Thermal noise is related to the thermal motion of electrons (due to the Brownian movement of charge carriers), which generates unwanted heat. This is related to the transconductance of the device. Thermal noise occurs as a result of the device physics.

Thermal noise is present regardless of the applied voltage. The thermal noise spectral density of a MOSFET is given in the following equations:

$$\frac{\overline{i_i^2}}{\Delta f_{thermal}} = \frac{8kT\omega^2 {C_{gs}}^2}{3g_m} \tag{2.8}$$

$$\frac{\overline{v_i^2}}{\Delta f_{thermal}} = 4kT\left(\frac{2}{3}g_m\right) \tag{2.9}$$

Thermal noise contributes to the reset noise of a detector (only applicable to the 3T) [25]. Thermal noise does not contribute to the four-transistor (4T) pixel structure, since the photodiode is disconnected in the reset phase. The input-referred noise increases exponentially as the amount of radiation increases with both topologies.

The low-temperature characteristics of transistors is improved [24] through bandgap engineering, by combining Si with Ge.

2.2.2 Medium to high frequency noise

Due to the relatively low switching speed of the detector, medium- to high-frequency switching noise will not cause significant degrading. The reason for this is that the conceptual capacitors that are created by the layers with respect to ground do not conduct current and also do not conduct current in between interconnect lines. The fringe capacitances and skin effect are minimal at the fast switching speeds.

Also, since flicker noise is associated with the traps, when the operating speed increases, these traps do not get enough time to collect charge and discharge in a random fashion. However, since thermal noise is related to the thermal motion of electrons, an increased operating speed will increase the thermal noise, since the electrons are more electrically excited.

2.2.3 Other noise sources

Shot noise, which is noise associated due to random fluctuations in direct current flow, is also associated with diodes. This affects BJTs and MOS transistors. This is due to carrier excitation in the junction of a diode which is linearly associated with the bandwidth (in Hz). Since the switching frequency is low, this noise is insignificant when compared to flicker noise for this application.

Avalanche noise is present in almost all pn-junctions and occurs when the depletion region of a reversed biased junction acquires sufficient energy to create electron-hole pairs. These electron-hole pairs collide with Si atoms in a random fashion due to the orientation of these pairs. Noise of this nature is more prevalent in Zener diodes and is generally not used in low-frequency circuits. For this reason, Zener diodes were not used in the application of BiCMOS detectors associated with this research. As reverse-biased diode connected HBTs are used in this research as the detecting element, the effects of avalanche breakdown and its associated noise need to be taken into consideration. Fortunately for this application, the diode is never taken to a forward-biased condition and is mostly fully reverse-biased together with low-

frequency operation. For that reason, avalanche breakdown does not easily occur for full detector operation, and avalanche noise does not pose a significant problem in BiCMOS detectors.

2.2.4 HBT noise models applicable to detectors

Since the base of an SiGe HBT is doped with Ge, a higher β is associated here and the transistor can be operated at much lower collector current for the same gain. It also exhibits higher f_T and f_{max}. This is extremely useful in the biasing current since it requires a lower biasing current to obtain the same gain as with conventional Si BJTs.

2.3 PREVIOUS WORK DONE IN THIS FIELD

This section summarises previous work done in this field to illustrate the significance of this work. The key aspect to note here is that in all the work referenced in this section, individual implementations are given where the development process is done from first principles. This work reduces development time and increases the quality of detectors by maximising the output SNR through a mathematical model derived from first principles.

Noise in BiCMOS detectors results in the degradation of several key factors, such as the DR and sensitivity. Currently literature only focuses on detector implementations for specific detector topologies. Less attention has been paid to the development or implementation of techniques to improve the SNR performance for most type of detectors and those used in array topologies [15]-[18] [26]-[31].

Table 2.1 shows work done in this field of study. The strengths and weaknesses of each of the research projects are briefly. Table 2.1 highlights the validity of this work in the existing body of knowledge also.

Table 2.1 Contextualisation of this research work.

Ref	Journal Impact Factor[1]	Strengths	Weaknesses / Gaps	Relevance
[15]	4.681	Circuit level description of a gated detector and circuit level description of fast-gating electronics are given.	No implementation of an array. Optimisation pre-manufacturing not done or discussed.	Can be extended to develop a detector array. Mathematical model of circuit level description can be derived.
[17]	1.343	Circuit level demonstration of another scheme for quenching has been presented. It also exhibits Correlated Double Sampling (CDS), which is needed to reduce certain noise components.	Not yet adapted for array implementation. Optimisation pre-manufacturing not done or discussed.	Mathematical model of circuit level description can be derived.
[32]	2.553	Circuit level representation of a gated passive quenching circuit for gated detector is given. Additional subsystems needed in a detector system (low pass filter, brightness enhanced film) with emitter-coupled logic are presented.	No implementation of an array. Optimisation pre-manufacturing not done or discussed.	Can be extended to develop a detector array. Mathematical model of circuit level description can be derived.

[1] The Web of Science (WoS) impact factor has been noted on 8 March 2020.

Ref	Journal Impact Factor[1]	Strengths	Weaknesses / Gaps	Relevance
[33]	1.428	Performance parameters are extrapolated and verified for single MOSFETs. Mathematical derivations with a discussion are presented. Noise is influenced by gate length and width. Smaller technology node results than what will be used are presented.	Complete structures are not analysed over multiple technology nodes. Optimisation process mentioned but not analysed. No specific detector structure was analysed.	Single transistor analysis, which is needed to analyse and optimise the full detector structure. Smaller technology nodes consume less power and are linear.
[34]	2.704	An underlying problem of varying bias voltages is mentioned. Classical 3T structure is used.	No optimisation of bias voltages. No circuit level analysis has been done to optimise analogue-to-digital converters by analysing transistor noise levels.	Proposes bias circuits to be used in detector designs but was not analysed to determine optimal parameters.
[35]	2.621	Methods for designing detectors are presented that yield good results. Low noise differential preamplifiers are used (mentioned in other papers). Self-heating problem solved by adjusting current level just before integration.	A thorough analysis of the current level adjustment not given. Temperature stabilisation analysis not done adequately. No bias circuit analysis done. The circuit level analysis	Mathematical modelling is possible.

Ref	Journal Impact Factor[1]	Strengths	Weaknesses / Gaps	Relevance
			of the ROIC also inadequate.	
[36]	2.704	A simple readout scheme is used. A transistor level analysis of pixels is presented, which will assist when analysing the complete spectrum of detectors.	Large pixels are used, which reduces the fill factor.	Transistor level analysis of pixels is presented.
This work	-	Streamlined methodology to design 3T type BiCMOS detectors with SNR performance. Technology-independent. Can be expanded to other BiCMOS detector structures.	This work is only implemented for one technology node/process/detector structure.	Able to simulate before prototyping.

The aim of this research is to develop a mathematical model to improve SNR that can be used under several conditions and for multiple topologies. This is beneficial for a designer, since an SNR value can be selected, and the resulting process independent parameter can be calculated which is of interest in developing detectors to specification.

This mathematical model can be expanded to most topologies in order to improve the overall SNR performance of BiCMOS detectors. This could possibly lead to designers using this methodology as a general design requirement in detector array design to improve parameters such as DR and sensitivity.

2.4 SHORT CHANNEL EFFECTS IN DETECTORS

Since the aim of this research is to develop a model for BiCMOS detectors where SNR optimisation is the focus point and noise is also applicable to short-channel MOSFETs, this is discussed and modelled. Threshold voltage variation is also prioritised in this part of the model development.

The well-known threshold voltage equation will not be valid for short-channel devices ($L \leq 1$ µm) since velocity saturation and hot carrier injection increases noise currents. There are distinguishable short-channel effects such as threshold voltage modification and velocity saturation [37]. Some field lines between the drain and source of the channel terminate on charges in the channel region. A smaller gate voltage is required to bias the MOSFET in inversion mode. This can be directly modelled using (2.10) and (2.11):

$$V_{tO\ (short\ channel)} = V_{tO} - \Delta V_{tO} \tag{2.10}$$

$$\Delta V_{tO} = \frac{\sqrt{2q\varepsilon_{si}N_A|2\phi_F|}}{C_{ox}} \frac{x_j}{2L}\left[\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)\right] \tag{2.11}$$

For threshold voltage modification, there are two designer changeable parameters that will have an influence for a specific technology node. The first is the length of the MOSFET which is indirectly proportional to ΔV_{tO}. As the length is increased more, the value of ΔV_{tO} will decrease until it is infinitesimal and can be ignored. A scientific reason for this is that as the length is increased, the depletion layers will separate such that the variation collapses and a square-law behaviour is observed. Secondly, increases in the source and drain depletion widths as well the depletion overlap with respect to the contacts will increase ΔV_{tO}.

2.5 MODELLING OF DETECTOR OUTPUT VOLTAGE AND OUTPUT CURRENT

The flow of electrical currents should be modelled first to develop the noise model. The current equations of BJTs and MOSFETs are well known and will not be repeated here. However, it was used as a basis to formulate the output voltage and output current. The three transistor (3T) pixel structure and four transistor (4T) pixel structure is used as a basis for the discussion. Although the 4T structure was never implemented, it is included here to show the adaptability of the proposed mathematical model.

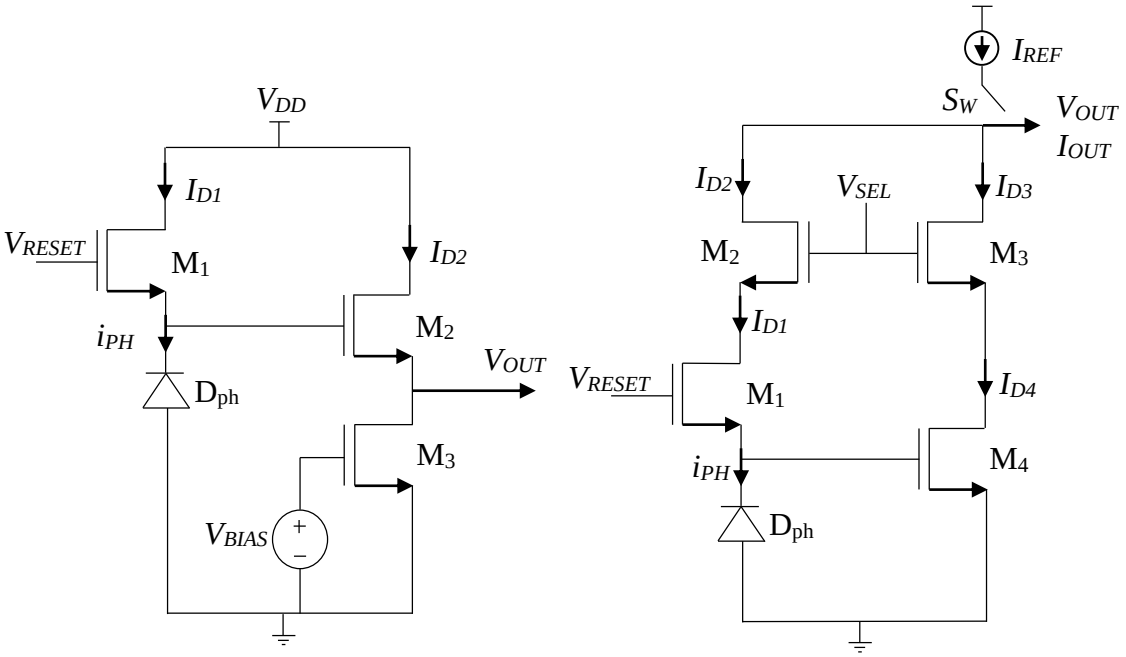


Figure 2. Detector structures (a) 3T and (b) 4T.

Figures 2a and 2b show the 3T and 4T detector structures, respectively. The D_{PH} element is the detecting element (or pixel). There are two types of pixels that can be used. These are reverse-biased diodes and reverse-biased diode-connected BJTs.

2.5.1 Three transistor (3T) pixel structure voltage and current model

The 3T pixel structure operates in a voltage mode. Although current flow is discussed, the final output voltage is of great importance [38]. Classic well-known equations that shows the behaviour of MOSFETs are used in the development of this mathematical model.

In Figure 2a for transistor M_1 the source voltage V_{S1} and optimised I_{D1} is given with velocity saturation taken into account:

$$V_{S1}=V_{DD}-V_{t1}-i_{PH}R_{sx1}-\sqrt{\frac{2i_{PH}L_1}{kW_1}} \tag{2.12}$$

$$I_{D1}=i_{PH}=\frac{k}{2}\frac{W_1}{L_1}\left(V_{DS1}^2-2V_{DS1}V_{t1}-i_{PH}R_{sx}\right) \tag{2.13}$$

where R_{sx} models the velocity saturation of M_1 biased in the linear region of operation given by:

$$R_{sx}=\frac{V_{GS}\text{-}V_T}{2I_D}-\frac{L}{kW(V_{GS}-V_t)} \tag{2.14}$$

For M_2, the transistor is biased in the linear region of operation. Since the source of M_1 and the gate of M_2 is connected, (2.13) is equal to V_{G2}. The optimised drain current I_{D2} is given by:

$$I_{D2}=\frac{k}{2\left[1+k\frac{W_2}{L_2}R_{sx}(V_{t2}+V_{DD}-V_{G2})\right]}\frac{W_2}{L_2}(V_{t2}+V_{DD}-V_{G2})^2 \tag{2.15}$$

For V_{S2}, it can intuitively be seen that $I_{D2} = I_{D3}$. When M_3 is biased in the linear region of operation, V_{S2} is given by:

$$V_{S2}=V_{G2}-V_{t2}-\sqrt{\frac{W_3}{L_3}\times\frac{L_2}{W_2}}(V_{G3}-V_{t3}) \tag{2.16}$$

When M_3 is biased in the triode region of operation and $I_{D2} = I_{D3}$, the following is obtained:

$$\frac{W_2}{L_2}(V_{GS2}-V_{t2})^2=\frac{W_3}{L_3}\left(2(V_{GS3}-V_{t3})V_{DS3}-{V_{DS3}}^2\right) \tag{2.17}$$

Because $V_{S3} = 0$ V, since it is connected to ground and $V_{S2} = V_{D3}$, the following is obtained:

$$\frac{W_2}{L_2}(V_{GS2}-V_{t2})^2=\frac{W_3}{L_3}\left(2(V_{G3}-V_{t3})V_{S2}-{V_{S2}}^2\right) \tag{2.18}$$

V_{S2} can be calculated with the use of the MATLAB™ `math`-function.

2.5.2 Four transistor (4T) pixel structure voltage and current model

For the case pixel structure, the mode of operation primarily is a current-mediated mode. In this case, the output current (I_{OUT}) changes as the photon generated current (i_{PH}) is increased.

In Figure 2b, the first part where detection takes place, the principle current flow remains the same as with the 3T pixel structure. In the latter part, due to the configuration change, the I_{OUT} is the varied output as opposed to the voltage output that the 3T pixel structure produces.

In reset mode, the V_{SEL} and V_{RESET} is ON. The output current is given by:

$$I_{OUT}=I_{REF}-I_{D2}-I_{D3} \tag{2.19}$$

In readout mode, the V_{SEL} ON and V_{RESET} is OFF. The output current is given by:

$$I_{OUT}=I_{D3} \tag{2.20}$$

For transistor M_1, the drain voltage is given by:

$$V_{D1}=V_{t1}+i_{PH}R_{sx1}+\sqrt{V_{t1}^2+\frac{2i_{PH}L_1}{kW_1}} \tag{2.21}$$

For transistor M_2, the drain voltage V_{D2} which is also equal to V_{OUT}, is given by:

$$V_{D2}=V_{S2}+V_{t2}+I_{D2}R_{sx2}+\sqrt{V_{t2}^2+\frac{2I_{D2}L_2}{kW_2}} \tag{2.22}$$

Transistor M_3 operates in the same region of operation as M_2. Therefore, V_{D3} which is also equal to V_{OUT}, is given by:

$$V_{D3}=V_{S3}+V_{t3}+I_{D3}R_{sx3}+\sqrt{V_{t3}^2+\frac{2i_{PH}L_3}{kW_3}} \tag{2.23}$$

For transistor M_4, the drain current using short channel devices, is given by:

$$I_{D4}=\frac{k}{2\left[1+k\frac{W_4}{L_4}R_{sx4}(V_{t4}+V_{D4}-V_{G4})\right]}\frac{W_4}{L_4}(V_{t4}+V_{D4}-V_{G4})^2 \tag{2.24}$$

Since M_1's drain current, which is also equal to the photon-generated current i_{PH}, M_4's gate voltage is given by:

$$V_{G4}=V_{D1}-V_{t1}-i_{PH}R_{sx1}-\sqrt{V_{t1}^2+\frac{2i_{PH}L_1}{kW_1}} \tag{2.25}$$

If long channel devices are chosen, I_{D4} reduces to:

$$I_{D4}=\frac{k}{2}\frac{W_4}{L_4}(V_{t4}+V_{D4}-V_{G4})^2 \tag{2.26}$$

The resistor R_{sx} models the velocity saturation of the devices if short-channel devices are chosen.

2.6 IMPACT OF NOISE IN BICMOS DETECTORS

There are several sources of noise, ranging from low-frequency flicker and thermal noise to high-frequency noise resulting from parasitic capacitances. Low-frequency thermal and flicker noise will be most prevalent because of bias currents and bias voltages present in BiCMOS detectors. The following paragraphs illustrate the mechanisms that influence noise.

The influence of noise in a system can be illustrated by analysing the voltage levels at different points of the 3T topology. The equations for voltages at different points are given below for MOSFET type 3T topology [38]:

$$I_{D2}=\frac{k_2}{2\left[1+k\frac{W_2}{L_2}R_{sx2}(V_{t2}+V_{DD}-V_{G2})\right]}\frac{W_2}{L_2}[V_{t2}+V_{DD}-V_{G2}]^2+noise \tag{2.27}$$

$$V_{S2}=V_{SAT1}-\sqrt{V_{t1}^2+\frac{2\,i_{PH}L_1}{kW_1}}-V_{SAT2}-\sqrt{\frac{2\,I_{D2}L_2}{kW_2}}+noise \tag{2.28}$$

Where $V_{SAT1} = V_{DD} - V_{t1} - i_{PH}\,R_{sx1}$ and $V_{SAT2} = i_{PH}R_{sx2} + V_{t2}$.

Equations (2.27) and (2.28) determine the output voltage and current of the 3T topology with the added noise. Then the transistor sizes can be adjusted in such a way that the effect of noise on this topology is minimised.

Equations (2.27) and (2.28) are applicable for the case where MOSFETs are used in the readout circuitry. A 3T topology using HBT readout circuitry only is also possible but is left for future extensions to this work. The actual pixel element in both cases is a diode-connected reverse-biased HBT, which was used accordingly.

References [15] – [18] [26] – [31] reported that CDS is mostly used to reduce fixed pattern noise and reset noise. This is the only technique used to reduce noise, which is mainly material dependent noise. CDS will also only work under certain conditions, depending on the circuit topology [39] [40].

2.7 CONCLUSION

The literature needed to understand the research and prove the research hypothesis has been introduced in this chapter. A detailed summary of published works in this field has been provided to highlight the significance of this modelling. The background of 3T and 4T pixel structures have been given as a basis to develop the model.

CHAPTER 3 METHODS

3. CHAPTER OVERVIEW

The literature study presented in Chapter 2 provides a background on CMOS detectors and implemented detector examples. A critical aspect of this research is the formulation of the voltage and current models of the chosen 3T pixel structure. Another is how noise influences detector performance and how it fits into the voltage and current models. The nature of this research requires an analysis of the voltage and current flow of the 3T pixel structure and how noise influences the performance of the detector. The research hypothesis (Section 1.2) can thus be proved on a theoretical and simulated level as well as on the basis of measured results.

In addition to this research hypothesis, research questions were also provided. They were answered systematically to prove that the research hypothesis is proven successfully. In this chapter, the process to prove the hypothesis is presented in the form of mathematical derivations, simulations, and experimental setup. Chapter 4 presents the mathematical derivations and simulations as well as the measurements results.

The selected process implementation of this research is the 0.35 µm SiGe BiCMOS process from ams AG (formerly Austria Mikro Systeme). This was made available through Europractice that offers multi-project wafer runs for the 0.35 µm SiGe BiCMOS process. This process has 7 metal layers and can accommodate both HBTs and MOSFETs. The fact that this process can accommodate both HBTs and MOSFETs is essential to prove the hypothesis of this research. The maximum supply voltage for this process is 3.3 V, however

since this is a model where the supply voltage can be varied, one can expand this to other process technologies which includes technologies with short-channel effects.

In Section 3.1 and 3.2, the device specifications and technical packages used to implement the detector are discussed. In Section 3.3 and 3.4, mathematical and SPICE modelling of the detector in software is discussed respectively. In Section 3.5, the schematic design and circuit layout of the detector is provided. Sections 3.6 and 3.7 respectively provide the implemented test structure and packaging of the IC along with the PCB used to obtain the measurements. In Section 3.8, the equipment used to obtain measurements is discussed. Section 3.9 discusses a high-level method to develop detectors. Finally, Section 3.10 summarises and concludes this chapter.

3.1 DEVICE SPECIFICATIONS APPLICABLE TO DETECTORS

The device elements used for this research, with the chosen technology node, are briefly presented in this section. Due to a non-disclosure agreement (NDA), specific details protected under this agreement will not be discussed.

3.1.1 Detecting elements (HBTs)

The most important element of a BiCMOS detector is a reverse-biased diode. Since this process has diodes and BJTs, there are two different ways to implement the detecting elements. The first one is a Si-based reverse-biased diode and the second is a SiGe reverse-biased diode-connected HBT. This research is about near-IR detectors, and hence the detecting element of choice was the SiGe reverse-biased diode-connected HBT. Si-based reverse-biased diodes were nonetheless also analysed and implemented to show the validity of the method.

The location of the diodes and HBTs are in-between the bottom layer on the substrate and the ILD layer. There are seven layers down from the top where incident radiation is projected. Due to this deep location, some radiation is lost due to absorption and reflection.

The top protecting nitride layer located perpendicularly above the detecting element was removed to assist the detecting elements somewhat in absorbing more radiation. In this way, radiation was channelled more effectively to the detecting element. The removal of the nitride layer was achieved in software by exclusion of a software defined layer which will not be repeated due to the NDA.

3.1.2 Resistors

An essential part of the detector is the transimpedance amplifier (TIA) at the output of the detector. TIAs have been documented extensively in CMOS technologies. A component of a TIA is the feedback resistor of which the resistance value (in Ω) is directly proportional to the gain. There are several resistive layers that can be used, each with different characteristics. These typical values are listed in Table 3.1 in order from lowest resistance per square area to highest resistance per square area with actual values omitted due to the NDA.

Table 3.1 Sheet resistances.

Sheet resistances	
Lowest	RPOLY1
	RBLAYER
	RDIFFN
	RDIFFP
	RPOLYE
	RPOLYB
Highest	RNWELL

It is worth mentioning that the RBLAYER is an n^+ buried layer located in the substrate which needs an n^+ sinker to establish connection which can be somewhat difficult to achieve. The same principle holds for RNWELL. For this application, one would use the POLY1, DIFFN, DIFFP, POLYE and POLYB as resistors. One way to achieve a high resistance in a small

area is to use a “snake” resistor formation, which was used in the implementation of this research.

For base- and emitter diffused resistors, the model used to calculate the total resistance is given by (3.1):

$$R_{TOT}=R_{\square}\left(\frac{L}{W}\right) \tag{3.1}$$

where $R_{\square}$ is the sheet resistance per unit area, L is the length of the resistor and W is the width of the resistor.

MOSFETs biased in the triode region of operation can also be used as a resistor of which the model is given in (3.2):

$$R_{TRIODE}=\left(\frac{\delta I_D}{\delta V_{DS}}\right)^{-1}=\frac{L}{W}\frac{1}{k'(V_{GS}-V_t-V_{DS})} \tag{3.2}$$

The only drawback of using this type of resistor is the high degree of non-linearity since the drain-source resistance depends on the drain-source voltage. Since the reset transistor in Figure 2a is a MOSFET-based resistor when OFF, this is essential in the development of the mathematical model.

3.1.3 Bond pads, vias and interconnect lines

The bond pads offered in the 0.35 µm SiGe BiCMOS process is a set size located on the top metal layer. This is then connected to bond-wires for post processing. Since this is a low-frequency application, fringe capacitance and oxide area capacitance were not taken into account in the development of this model. The resistance of a bond pad is very low and is not taken into account when developing the noise model.

In the chosen process, vias is a set size as well. Since the resistance of a via is very low (<5 Ω/via), this was also not taken into account in the development of the noise model. Justification of this choice is the large resistance from a gate to drain/source of a MOSFET.

The interconnect lines used to connect all the devices also exhibits low resistance per unit area (<1 Ω/□) and are not taken into account since they would not significantly affect total resistance.

3.2 TECHNICAL PACKAGES

The implementation of this research requires careful usage of technical software to obtain accurate results in order to validate the formulated hypothesis and provide meaningful results to the proposed research questions. This requires accurate results and a thorough understanding of the correct software and applicable models. The chosen technical packages and functions in this research are given in Table 3.2.

Table 3.2 Software packages used to validate the research hypothesis.

Software	Functionality
Microsoft Excel	Mathematical modelling
Cadence Virtuoso Schematic Editor (IC6.1.3.500.13)	Schematic compiler
Cadence Virtuoso Analog Design Environment (IC6.1.3.500.13)	SPICE-based simulator
Cadence Virtuoso Layout Editor (IC6.1.3.500.13)	IC Layout designer
ams-AG S35D4M7 Process Development Kit (PDK)	Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification

No version of the chosen technical packages is given since the model is developed to be used with any similar type of software package and version within acceptable limits.

3.3 MATHEMATICAL MODELLING

This research made extensive use of modelling to show that the science can be numerically quantified. This was done firstly by analysing the actual circuits to develop a voltage and current equation. Then by interlinking all the equations, a model was developed describing the DC and AC behaviour of the detector. The different noise parameters can then be added in the voltage and current equations, but that is beyond the scope of this study. Only noise parameters applicable to the detecting element are thoroughly analysed. Since some noise parameters can be modelled in another way by performing Norton and Thévenin transformations, the total number of noise parameters were reduced. This also reduced the possibility of errors in the model.

The first part, documented in the previous paragraph, was then plotted in software using Microsoft Excel and can be plotted with the use of MATLAB™. These graphs are shown in Chapter 4.

3.4 SPICE MODELLING

SPICE is mathematical based software, built into Cadence Virtuoso, used to predict the chosen devices' performance with the inclusion of material and interconnection effects. This study made use of electrical parameters of HBTs, MOSFETs and IC layers to develop the mathematical model where first order effects were included. The model used by Cadence Virtuoso produced a more accurate representation since it included second, third and fourth order effects.

3.5 SCHEMATIC DESIGNS AND CIRCUIT LAYOUT

Schematic designs were done in a Cadence Virtuoso Analogue Design Environment (ADE) environment and simulated using the SPICE algorithm (discussed in Section 3.4). These schematic designs were published in a previous study by the same author. The circuits were

represented in Cadence Virtuoso Schematic Editor and then simulated using the ADE to obtain a time-domain representation using the SPICE algorithm. Cadence Virtuoso provides time domain simulations using the ams AG 0.35 µm SiGe HBT (S35D4M7) process design kit (PDK). This simulation environment provides accurate and quick design verification using standard models incorporated in the PDK.

A systematic circuit design approach was adopted to make sure that the circuit functions as intended. Standard optimised cells were used since the peripheral circuitry after the output is needed to obtain the array formation but is not critical in the methodology. Once such cell is the D Flip-Flop. The layout of *instances* is available as is and subsequently used. This modular approach proved extremely useful as several errors were corrected in the design process before the layout phase was started.

The IC layout of this research was done using Cadence Virtuoso Layout Suite which supports physical IC layout for all types of designs on device, cell and block level where the elements are directly available from the libraries. In the unfortunate event where a device is not available in the library, it is possible to design a new device by simply using the appropriate layers and saving the device as a cell.

Since there are several input, supply and output points that need external connections, several bonding pads had to be added in the design. Fortunately, since this is a low frequency application, no electromagnetic simulations or analysis was needed. However, since bonding pads use a large amount of area where *die*-space is limited, this presents a challenge to effective design. Fortunately, the number of bond pads does not increase when increasing the number of pixels.

The Cadence Virtuoso package also includes two layout verification programmes for each PDK. These are design rule check (DRC) and layout versus schematic (LVS). A DRC check is performed to ensure the IC conforms to the requirements of the PDK. Each PDK has its own specific set of design rules. LVS is performed to ensure that the designed layout corresponds to the schematic circuits in ADE. Both of these verification programmes are

critical to ensure correct working of the IC on a schematic level as well as what can be manufactured before submission to foundry.

3.6 TEST STRUCTURES

Since the device of choice for detection is a reverse-biased diode-connected HBT, it is important to understand how it behaves. In order to have measured results, a lone-standing HBT with all the individual connections was prototyped and connected to individual bonding pads. In this way, the detecting element was characterised on its own and, since noise is causal, the noise performance of the peripheral circuitry could be estimated. A 2N2222 temperature sensor was placed on a corner of the chip to ensure that the temperature was documented correctly. The sensor did not influence any part of the circuits post-prototyping. The forward voltage drop of the temperature sensor is indirectly proportional to the temperature and has been calibrated thoroughly. The results of these measurements are discussed in Chapter 5.

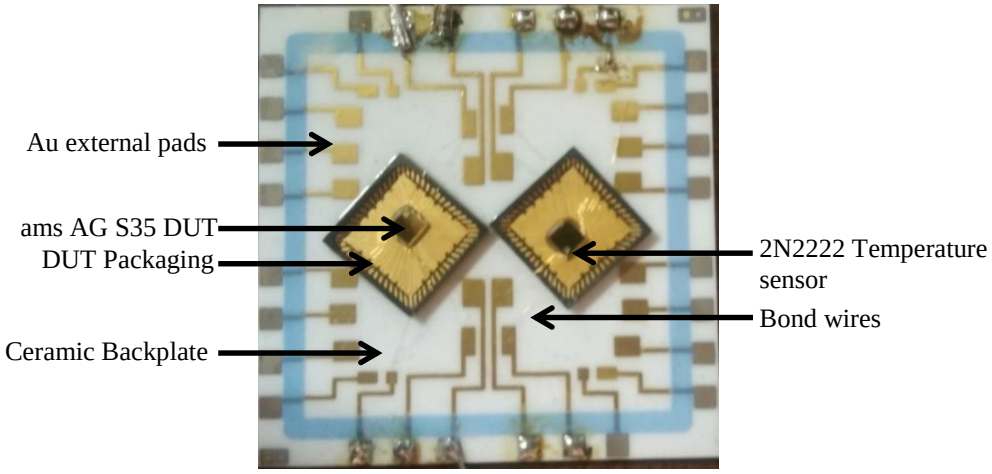


Figure 3.1. IC prototype mounted on a ceramic backplate [41].

Figure 3.1 shows how the IC package was mounted on an Al_2O_3 (alumina) ceramic back plate together with all the connections. The IC was mounted on a gold-plated ground plane using conductive epoxy. This setup was needed to perform noise, I-V and C-V measurements at cryogenic temperatures (77 K). The thermal expansion coefficient of Si is in the same range as the alumina and therefore would not pose problems when cooled to extremely low temperatures. This alumina ceramic backplate is a popular choice for cryogenic

measurements since it can handle the extremely low temperatures effectively and is also cost effective.

The circuit shown in Figure 3.2 was used to measure the noise.

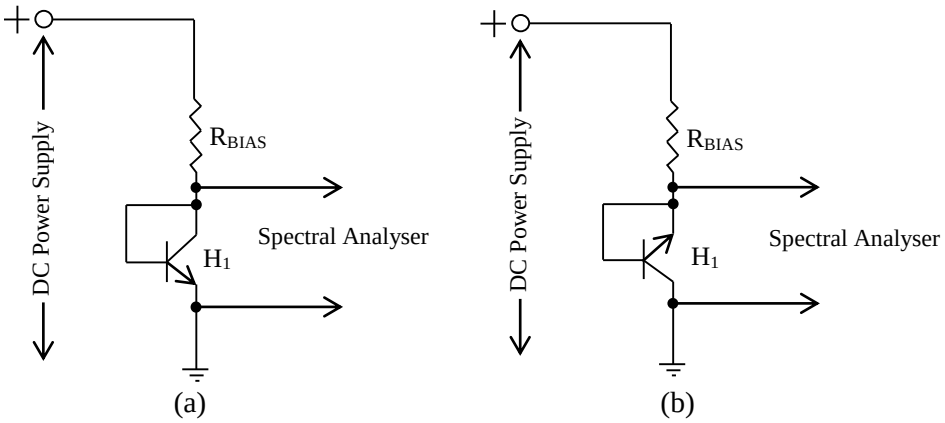


Figure 3.2. Measurement setup for noise performance.

(a) Base-collector shorted measured to emitter and (b) Base-emitter shorted measured to collector.

Figure 3.2 shows the measurement setup and applicable circuits that perform the cryogenic noise measurements. Two of the three terminals of the HBT were shorted where the base terminal is common in both cases. This is to be ensure that only one diode is measured at a time since the other two terminals are at the same potential. On a chip level, the following is observed in terms of diode placements.

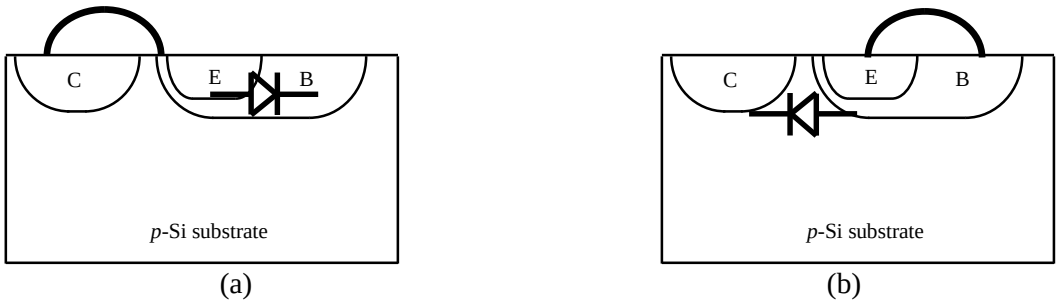


Figure 3.3. Diode formation for the two setups.

(a) Base-emitter diode and (b) Base-collector diode.

The two different formations of diodes are shown in Figure 3.3. Since the doping levels differ from the collector to the base to the emitter, two different noise profiles are obtained. These results are shown in Chapter 5. Also, to perform the I-V and C-V sweeps, the same

shorted setup as shown in Figure 3.3 was used but without the extra resistor and power supply. The analyser biases the diode and thus no extra biasing is required. The semiconductor device analyser and the spectral analyser used are discussed in Section 3.8.

3.7 PACKAGING AND PCB

Since the required power is low and the frequency of operation of the chip is low, a dual in-line package or a quad flat no-lead package will suffice. The chip is shown in Figure 3.4.

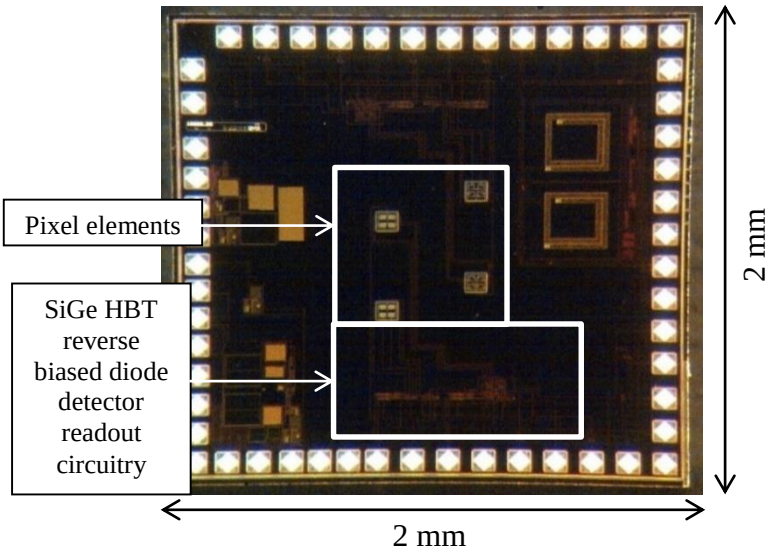


Figure 3.4. Layout and chip photograph of the implemented detector [7].

As shown in Figure 3.4, there are several bond pads on the implemented detector. All these bond pads or points are needed to ensure proper working of the detector through inputs, supply voltages and outputs as well as test points. For this chip, 52 points were needed; hence a 56-pin package was used. The IC was mounted on a gold-plated plane as discussed in Section 3.6.

As there are no high-frequency transmissions and low power requirements, a simple printed circuit board (PCB) as shown in Figure 3.5 was designed for this work to enable easy port access.

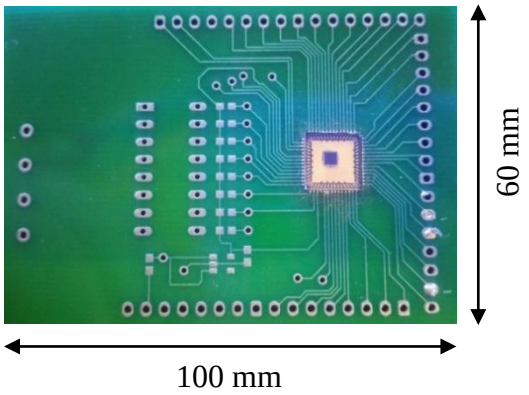


Figure 3.5. Manufactured PCB for detector measurements.

Several connections to measuring equipment needed to be made to perform full detector noise measurement. Also, the noise measurements were done while the detector was illuminated. Full detector noise measurements were therefore done at room temperature only. The PCB was placed in a Faraday cage to cancel out most, if not all, ambient noise. The choice of power supply was a 9 V battery with a voltage divider circuit using resistors to eliminate the 50 Hz noise peak from conventional power supplies.

3.8 MEASUREMENT EQUIPMENT

The equipment needed to measure the two different setups are discussed in this chapter.

3.8.1 Test structure equipment

The setup and measurement were carried out with the assistance of Dr JW Lambrechts at the Detek (which is part of Denel Dynamics (State Owned Company)) based at the CSIR. An HP 3651A Dynamic Signal Analyser and Agilent B1500A Semiconductor Device Analyser were used for the I-V, C-V and noise measurements.

Figure 3.6. HP 3561A Dynamic Signal Analyser.

The signal analyser shown in Figure 3.6 has only one single channel, the Fast Fourier Transform, for the entire frequency range of 100 kHz. It can measure magnitude, phase and transient response of an applied signal. The narrow band noise measuring capability of 250 Hz for a full 100 kHz span and 25.6 µHz for a 0.01 Hz span is quite useful. It also exhibits 80 dBs of DR which enables the measuring of signals within large unwanted signals. The voltage range is from 2.82 mV_{RMS} to 22.39 V_{RMS} which is extremely useful since the average voltage swing of the implemented detector is 1.5 V.

Figure 3.7. Agilent Technologies B1500A Semiconductor Device Analyser.

Figure 3.7 depicts the analyser used to measure the I-V and C-V curves from room temperature down to 77 K. A separate platform was used to deposit liquid nitrogen on, to cool the chip down. The I-V curves could be measured at different temperatures between

room temperature and 77 K by simply holding the chip mounted ceramic plate above the vapours and sweeping the I-V curves at that instant. The exact temperature was noted by jotting down the forward voltage drop of the 2N2222 temperature sensor mounted on the chip.

For conducting C-V measurements, it was difficult to keep the chip at one temperature to do multiple sweeps (for different oscillation frequencies). Only room temperature and 77 K sweeps were therefore performed. The same procedure as described in the previous paragraph was used.

The B1500A analyser has precision voltage and current measuring capabilities (0.5 µV and 0.1 fA resolution respectively). It is an accurate and low-cost solution for performing multi-frequency sweeps (1 kHz to 5 MHz) and capacitance measurements (C-V, C-f and C-t) with fast 100 ns pulse times and a 5 ns sampling rate.

3.8.2 Full detector measurement equipment

The signal analyser model SR785, from Stanford Research Systems, was used to perform the full detector noise measurements. These measurements were done by the author as part of a study abroad programme at the Department of Physics and Astronomy at Georgia State University in Atlanta, USA. The signal analyser is shown in Figure 3.8.

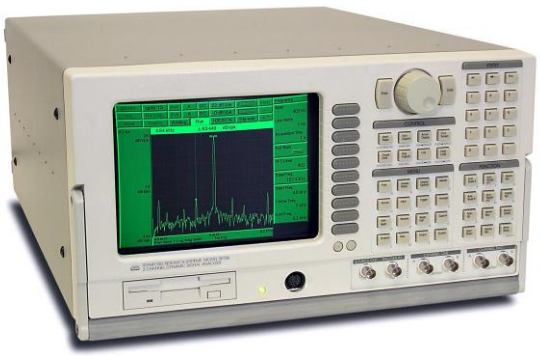


Figure 3.8. Stanford Research Systems SR785 signal analyser.

Figure 3.8 shows the signal analyser used in this research. The amplitude accuracy of the SR785 analyser is 0.2 dB with a harmonic distortion of -80 dB. This system can measure noise effectively up to 102 kHz with an accuracy of 25 parts per million from 20 ºC to 40 ºC. These specifications allowed for accurate noise measurements.

3.9 ANALYSIS AND SUITABLILITY OF METHODOLOGY

Section. 2.5 gave a detailed voltage and current model of the 3T pixel structure. Although separate equations are documented, one can combine all the equations into a final SNR "figure of merit" equation for a complete model of the detector.

Since noise voltage is random in nature, it is additive when the sources are in series or parallel. Each noise source contributes individually to the final output noise. The total noise voltage output is conceptually given by the following equation:

$$\overline{v_{total}^2} = \overline{v_{PSU}^2} + \overline{v_{pixel}^2} + \overline{v_{M1}^2} + \overline{v_{M2}^2} + \overline{v_{M3}^2} \tag{3.3}$$

where $\overline{v_{PSU}^2}$ is the power supply noise.

The following high-level method to develop detectors is introduced in this research that could be used to optimise for SNR:

1. Construct the standard 3T pixel structure detector as illustrated in Figure 2a.
2. Select a suitable SNR value.
3. Calculate the size of the transistors (Pixel, M_1, M_2 and M_3) and the biasing conditions (temperature, bias voltage and bias current) using the selected SNR by calculating the final output voltage using the set of equations given in Section 2.5.1. These calculated process-independent parameters can be inserted into noise equations and then the noise level can be calculated. This noise model derivation is left for future work.
4. Simulate and verify the SNR.

5. Analyse the results and decide accordingly. If the SNR performance is not acceptable, adjust the process independent parameters (temperature, AR, bias voltage and bias current) accordingly. Then reinsert the adjusted values and simulate and analyse.

3.10 CONCLUSION

In this chapter, the methodology of the approach to this research was discussed, as was the software used to model the detector and the hardware needed. The prototype IC as well as the PCB was shown to illustrate the implementation used to obtain the necessary results.

CHAPTER 4 MATHEMATICAL MODELLING AND SIMULATIONS

4. CHAPTER OVERVIEW

This chapter describes the process followed to obtain the mathematical model, the literature for which is described in Chapter 2. Each critical element that the process-independent parameters affect is then plotted to show the influence. Since there are four parameters that affect SNR, in each case three of the four parameters were fixed with realistic values, and the last parameter was calculated. A SNR value can be selected, and the applicable process-independent parameters can be calculated with the use of the MATLAB™ `math`-function.

In Section 4.1, the effect of the chosen process-independent parameters applicable to this thesis is discussed. In Section 4.2, the block layout of the detector is provided. Section 4.3 and 4.4 provides the DC and AC model development respectively, using *y*-parameter representation. Section 4.5 discusses the noise model applicable to the pixel. Section 4.6 and 4.7 discusses temperature variations for the pixel and other MOSFETs respectively in the detector. In Section 4.8, simulations are presented to illustrate the effect that each one of the process-independent parameters has on the performance of the detector. Finally, Section 4.9 summarises and concludes this chapter.

4.1 PROCESS-INDEPENDENT PARAMETERS

Since a standard BiCMOS process is used, the possibility to change process dependent parameters is extremely limited. The focus is therefore on process-independent parameters only. The chosen process-independent parameters are not completely process-independent as there are limits to what can be selected. One such selection is the maximum bias voltage that can be applied which in this case is 3.3 V. The independence range is limited to what the chosen technology node can offer.

4.1.1 Temperature

Temperature was chosen since detectors can be exposed to a wide range of temperatures and there are several types of noise that are temperature dependent. For instance, thermal noise is heavily dependent on temperature which is based on thermal motion of electrons generating unwanted heat. A detector designer has to take this into account for the expected operating temperatures. The temperature range that these detectors are exposed to, can cause a significant change in performance characteristics.

4.1.2 Bias voltage

For low-frequency applications, bias voltage does have an indirect influence in the SNR since the biasing of a transistor is based on voltage and current biasing. The biasing voltage of each active device has to be kept within acceptable limits since extra unwanted switching noise is introduced. This unwanted switch will result in irregular current flow, which will also increase thermal noise.

4.1.3 Bias current

Bias current has a large influence in low-frequency operation and SNR performance. This is due to the movement of electrons through the paths and due to the crystal imperfections of the devices used. As seen in (2.6) and (2.7), bias current affects the noise performance

directly as described in Section 2.5.1 for the 3T structure and in Section 2.5.2 for the 4T pixel structure.

4.1.4 Aspect ratio

AR also has a significant influence since it affects the current flow. Although it is not directly related to the noise performance, a change in AR changes the current flow which in turn changes the noise performance. This is also significant in the SNR representation at the output of the detector. AR will affect the flicker noise since a larger area is used to realise a transistor which contains more crystal defects.

The length of a MOSFET affects the speed of operation. However, since this is a low frequency application, the length is of no concern for the speed of operation.

4.2 BLOCK LEVEL LAYOUT OF A DETECTOR

Each of the stages of processing from the pixel to the final output before post-processing, as well as the accompanying noise models, are modelled in subsequent sections. A block diagram of a detector is given in Figure 4.1 to accompany the discussion of each stage for readability.

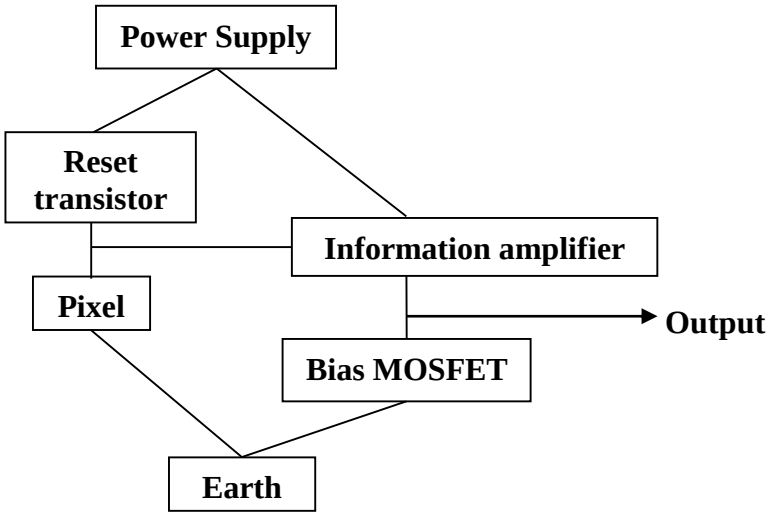


Figure 4.1. Block diagram layout of a 3T pixel structure detector.

The pixel is a reverse-biased diode connected HBT. The reset transistor is included for two functions. The first is to reset the detector which implies completely discharging the detector as well as nullifying the output. The second is to function as a current controlled resistor when the detector is not in reset mode. The information amplifier amplifies the low amplitude voltage signal received from the reset transistor to a larger current. The bias MOSFET is included to bias the output voltage to an acceptable level for post-processing.

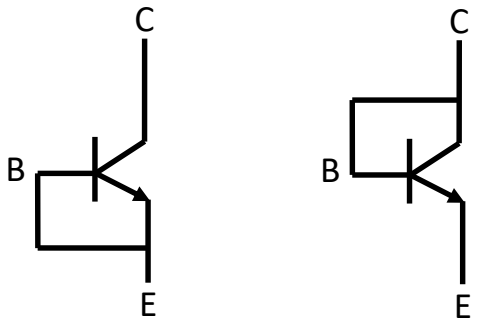
Current and noise have been developed for single devices as basic models for voltage. The exact influence each component will have in a detector is yet to be documented in literature. For this work, the 3T pixel structure was used to illustrate the model given in Section 2.5.1. The method described can be used to model other pixel structures as well that of the 4T structure derivation as given in Section 2.5.2. To develop a noise model, it is imperative that a voltage and current flow model must first be developed as described in Section 4.3.

4.3 VOLTAGE AND CURRENT MODEL DEVELOPMENT

In this section, the voltage and current models of each of the individual elements that make up the 3T pixel structure as given in Figure 2a is discussed with reference to Figure 4.1.

4.3.1 Pixel

The four process-independent parameters focussed on in this research are bias current, bias voltage, temperature and AR. Pixels are formed with reverse-biased diodes. There are two possible ways to form a diode with an HBT. A graphical representation of these two possibilities is given in Figure 4.2.



(a) (b)

Figure 4.2. Graphical representation of the two possible diode-connected HBT topologies.

(a) Base-emitter shorted- and (b) Base-collector shorted HBT.

Since the HBT used in this research is an *npn* transistor, assuming current flows in from the collector, Figure 4.2a represents an *np*-diode and Figure 4.2b represents a *pn*-diode. For a diode to function as a detector, it must be reverse biased. Reverse biasing a *pn*-junction widens the depletion region to such a point that current flow decreases to only leakage or dark current flow. When phonons due to radiation hit the surface of the diode, generation-recombination of electrons result in electron flow over the widened depletion region to the positive side of the diode. Hence current flow occurs where the amount of incident radiation is directly proportional to the current flow. The equation that models the operation of a diode is:

$$I_C = I_S \left(e^{\left(\frac{qV_C}{kT}\right)} - 1 \right) \tag{4.1}$$

where the constant parameters are the elementary charge q (1.602×10^{-19} C) and k (1.38×10^{-23} J/K). The parameters I_C and I_S are the current flow through the diode and the saturation current of the diode respectively. V_C and T are the bias voltage and operating temperature of the diode respectively.

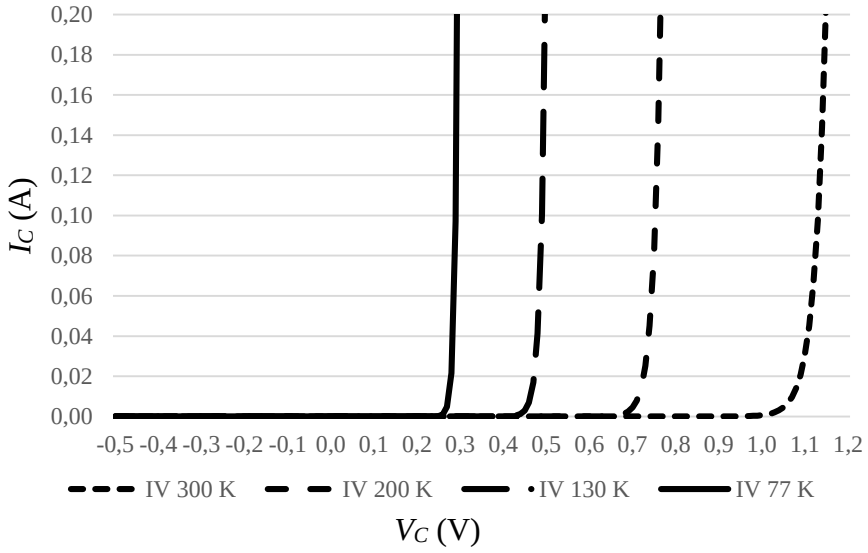


Figure 4.3. *I-V* simulations of a diode at different temperatures.

In Figure 4.3, the current-voltage relationship for different temperatures is given. As the temperature decreases, the forward biased breakthrough voltage decreases. This is indicative of the atoms that move closer to each other, requiring less energy in the form of an electric field, to excite the electrons enough to induce current flow. Since the focus of this research is the development of a mathematical model and because reverse-biased diodes are needed for the pixels, the negative bias voltage was analysed in more detail.

As the bias voltage increase more negatively, the value of $e^{\frac{qV_C}{kT}}$ becomes insignificantly small and I_C converges to I_S regardless of temperature changes. The saturation current I_S is set as a constant in the plot shown in Figure 4.3. Even though temperature appears in the exponent of e, the exponential rise of n_i that is present in I_S due to temperature, dominates.

To illustrate the actual effect of temperature on I_S, factors that directly influence I_S are analysed. The major contributor to this is the current density J_N which dominates in an *n*-type material. The following two equations are well-known but important in the development of the model and therefore included.

$$J_N=\sigma E \tag{4.2}$$

$$J_N = qD_n \frac{d_n}{d_x} \tag{4.3}$$

where σ is the conductivity,

E is the electric field,

q is the charge of an electron (1.602×10^{-19} C),

D_n is the electron diffusion coefficient, and

$\frac{d_n}{d_x}$ is the gradient of the electron concentration in one direction.

D_n is related to mobility (μ_n) and temperature (T) using Einstein's relation given by:

$$D_n = \mu_n \frac{kT}{q} \tag{4.4}$$

Theoretically, I_S is not constant but related to the electron and hole diffusion coefficient by:

$$I_S = qAn_i^2 \left(\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p} \right) \tag{4.5}$$

where A is the cross-sectional area of the diode, n_i is the intrinsic carrier density, L_n and L_p are the length of the *n*-type and *p*-type doped sides of the diode respectively, and N_A and N_D are the acceptor and donor concentrations. The intrinsic carrier density n_i is given by:

$$n_i^2 = BT^3 e^{-\frac{E_g}{k_{ev}T}} \tag{4.6}$$

where B is a material dependent parameter (1.08×10^{31} $K^{-3}cm^{-6}$ for Si), E_g is the bandgap energy in eV (1.12 for Si) and k_{ev} is Boltzmann constant in electron volt (8.62×10^{-5} eV/K). Taking (4.2), (4.3), (4.4), (4.6) and substituting in (4.5) and manipulating it, a detailed mathematical relation showing the strong dependence of the saturation current with temperature is given in (4.7).

$$I_S = BT^4 k e^{-\frac{E_g}{k_{ev}T}} \left(\frac{\mu_n}{N_A L_n} + \frac{\mu_p}{N_D L_p} \right) \tag{4.7}$$

where k is Boltzmann constant (1.3806×10^{-23} J/K). Equation (4.7) shows that I_S is proportional to T^4 which is the strongest dependence in this case. For Si with the following additional parameters (diode length of 1 μm, μ_n = 1150 cm^2/V.s, μ_p = 360 cm^2/V.s, $N_A = N_D$

= 1×10^{16} atoms/cm^3), the saturation current I_S vs T for temperatures between 300 K and 70 K are illustrated in Figure 4.4.

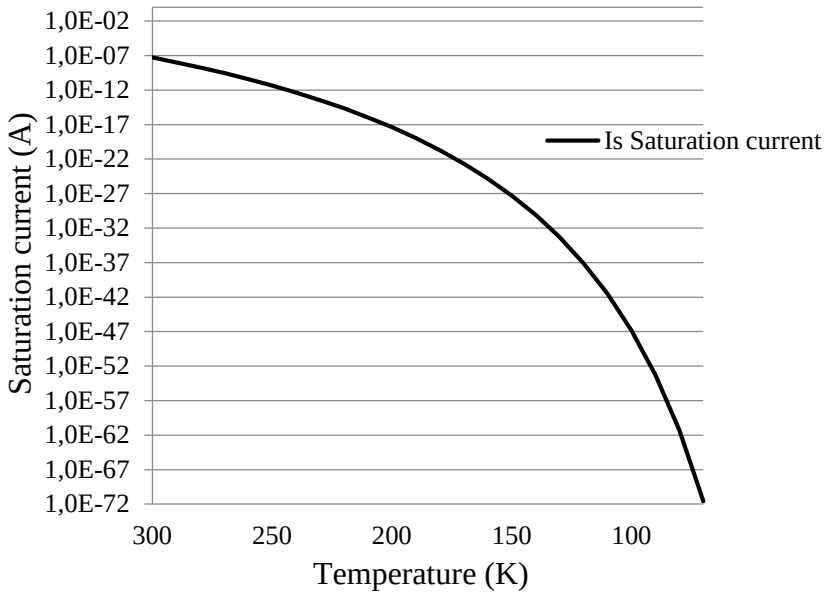


Figure 4.4. Saturation current simulations of a diode at different temperatures.

As it can be seen in Figure 4.4, the saturation current drops exponentially as the temperature is decreased. This shows that I_S has a very strong dependence on temperature. For most practical applications, I_S is kept constant in calculations but this shows that I_S can differ when operating conditions change and depending on the application, one should take this into account.

4.3.2 Reset transistor M_1

The reset transistor is included in this structure for two functions, which is to reset the detector (release any charge build up and nullify the output) in reset mode and to function as a current controlled resistor. Since the resistance changes as the current changes, the voltage drop across the drain and source points changes as well. The result is that as the current flow increases due to incident radiation increase, the voltage between the source of M_1 and cathode of the diode-connected HBT (D_{PH}) changes accordingly. This change is the information part which needs to be modelled correctly in order for the final output to produce the correct information.

This is the case for each stage. The information of the previous stage has to be modelled correctly in order to model the next stage correctly.

When the gate is tied to ground, M_1 is OFF i.e. in reset mode. When the gate of the MOSFET is tied to V_{DD}, it acts as a voltage-controlled resistor. The MOSFET operates in the linear region of operation since the gate is tied to V_{DD}. Thus $V_{GD} < V_t$ since the gate and drain are shorted, and V_{GS} has to be kept larger than the threshold voltage V_t to enable the transistor to operate. If V_{GS} were to drop below V_T, the transistor will be in cut-off region of operation and this is not desired.

For a MOSFET device operating in the active region of operation, the current flow is given by the following well-known equation:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2 \tag{4.8}$$

Since the gate and the drain are shorted, $V_{GS} = V_{DS}$ and therefore can be replaced in (4.8). To develop a model of resistance of this gate-drain shorted MOSFET, the current in (4.8) is differentiated mathematically with respect to V_{DS} and the following is obtained:

$$R_{GDshort} = \left(\frac{\partial I_d}{\partial V_{DS}}\right)^{-1} = \frac{L}{W}\frac{1}{\mu C_{ox}(V_{DS} - V_t)} \tag{4.9}$$

Equation (4.9) describes the resistance of the gate-drain shorted MOSFET. It is strongly dependent on the drain-source voltage. To graphically illustrate the effect of V_{DS} on the resistance, an AR of 2, $\mu_n = 1150$ cm^2/V.s, $C_{ox} = 3.45\times10^{-7}$ F/cm^2 and $V_t = 0.44$ V was chosen. V_{DS} was selected and corresponding resistance values were documented. Since the chosen fabrication technology is a 3.3 V process and the drain-source voltage must be larger than the threshold voltage V_t of 0.44 V to keep the MOSFET in linear region of operation, V_{DS} is swept between 0.5 V and 3 V.

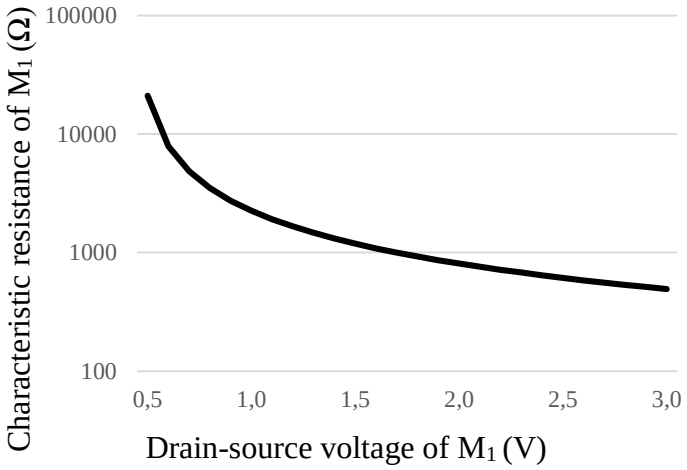


Figure 4.5. Resistance of M_1 as voltage drop changes.

Figure 4.5 shows the characteristic resistance of the gate-drain shorted MOSFET as the voltage drop changes due to current flow resulting from incident radiation on the pixel. The characteristic resistance drops exponentially as the drain-source voltage increases. From a physical science perspective, this is expected as the depletion region gradually opens from the drain to the source as the drain-source voltage increases. This gradual opening results in a decreased characteristic resistance.

4.3.3 Information amplifier M_2

For the information amplifier M_2, the input is on the gate which is connected between the source of M_1 and the characteristic cathode of the D_{PH}. M_2 is biased in the linear region of operation since V_{GD} is equal to the drain-source voltage of M_1 which is kept above the threshold voltage, to enable current flow in M_1. V_{DS} of M_2 is also kept above the threshold voltage.

4.3.4 Mathematical model of 3T pixel structure

In this section, the mathematical model of the information flow is discussed with the aid of equations. This will also illustrate the interlinking operation of the full detector.

For the pixel, the current flow due to illumination is given by:

$$i_{PH} = \eta \times e \times \phi \times A \tag{4.10}$$

where η is the QE,

e is the charge of an electron (C),

ϕ is the photon flux density (electrons/cm^2-s) and

A is the junction area (μm^2).

For transistor M_1, it acts as a non-linear resistor. Since the drain voltage is fixed to the supply, a change in current flow due to illumination derived in Chapter 2 is provided in (4.11):

$$V_{S1} = V_{DD} - V_{t1} - i_{PH} R_{sx1} - \sqrt{V_{t1}^2 + \frac{2 \times i_{PH} \times L_1}{k_1 \times W_1}} \tag{4.11}$$

where V_{S1} is the source voltage of M_1,

V_{DD} is the supply voltage,

V_{t1} is the threshold voltage of M_1,

R_{sx} is the resistance value used to model velocity saturation,

k_1 is equal to $\mu_n \times C_{ox}$, and

W_1 and L_1 is the width and length of the MOSFET respectively.

Since the source of M_1 is directly connected to the gate of M_2, the current flow through M_2 and source voltage of M_2 given in Chapter 2, is provided:

$$I_{D2} = \frac{k_2}{2 \times \left[1 + k_2 \times \frac{W_2}{L_2} \times R_{sx2} \times V_{OV2}\right]} \times \frac{W_2}{L_2} \times {V_{OV2}}^2 \tag{4.12}$$

where $V_{OV2} = V_{G2} - V_{S2} - V_{t2}$ and

$$V_{S2} = V_{G2} - V_{t2} V_{G2} - V_{t2} - \sqrt{\frac{W_3 \times L_2}{L_3 \times W_2}} (V_{G3} - V_{t3}) \tag{4.13}$$

4.4 *Y*-PARAMETER REPRESENTATION OF THE 3-T PIXEL STRUCTURE

This section describes the method to model these detectors using *y*-parameter representation. Y-parameter representation is chosen since the input is a current due to the pixel and the output is a voltage source. Section 4.3 described the DC analysis of the detector. Although the DC representation will work, the small-signal representation is important to understand the AC characteristics.

4.4.1 *y*-parameter model development

This section describes the method to model these detectors using *y*-parameter representation. Y-parameter representation was chosen since the input is a current due to the pixel and the output is a voltage source. Section 4.3 described the DC analysis of the detector. Although the DC representation will suffice, the small-signal representation is required to understand the AC characteristics. Each individual element that makes up the final *y*-parameter representation is developed and illustrated. This aided in the formulation of the final mathematical model.

Using Figure 2a, for the system to operate, V_{G1} must be tied to V_{DD}. Figure 4.6 is obtained by omitting the pixel D_{PH} and replacing the other transistors with their small-signal equivalent.

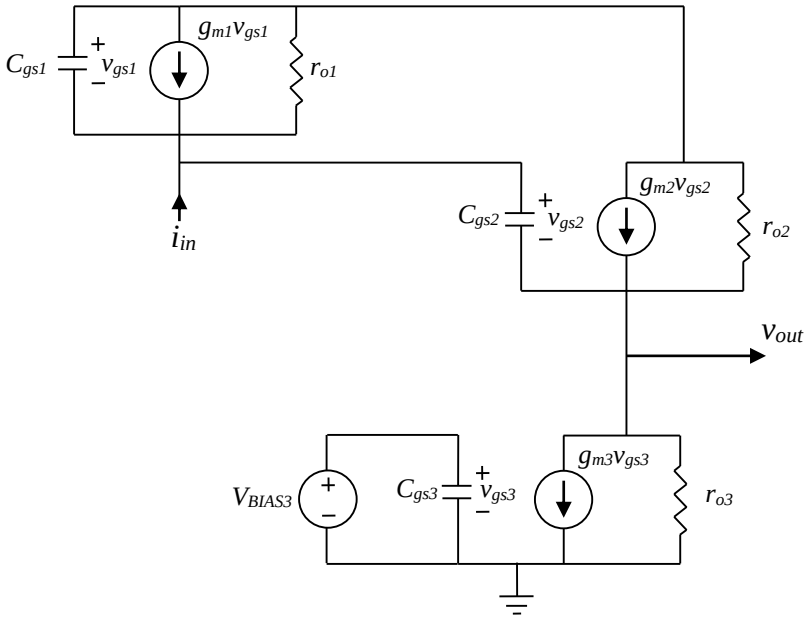


Figure 4.6. Small signal equivalent of the 3T pixel structure.

The supply voltage is quite simply removed since it is a current source at a certain resistance in this configuration. Since V_{BIAS3} is an independent voltage source, it is shorted. Due to this, v_{gs3} = 0 V which results in the capacitor C_{gs3} to be 0 F and is therefore removed. The current generator $g_{m3}\,v_{gs3}$ can also be removed. Rearranging with that, where the *a*-loop and *f*-loop are highlighted, yields:

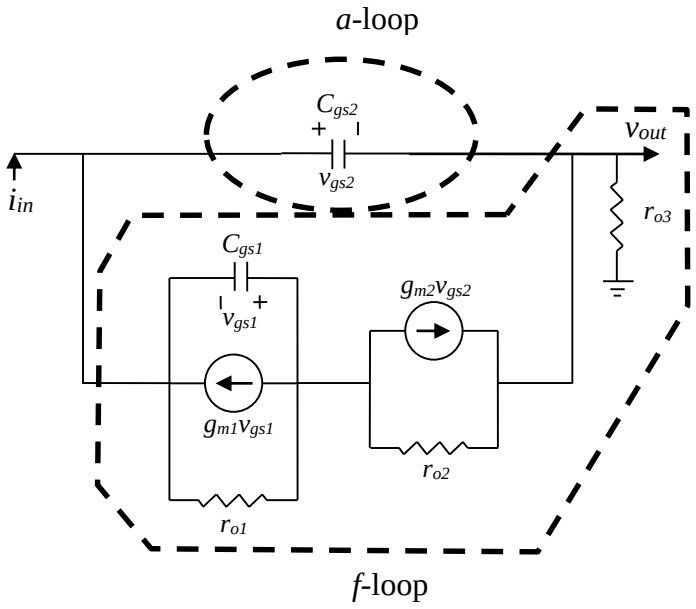


Figure 4.7. *y*-parameter circuit representation.

To develop the *y*-parameter representation, the following four equations must be solved first:

$$y_{11}=\frac{i_1}{v_1}\Big|_{v_2=0} \qquad y_{12}=\frac{i_1}{v_2}\Big|_{v_1=0} \qquad y_{21}=\frac{i_2}{v_1}\Big|_{v_2=0} \qquad y_{22}=\frac{i_2}{v_2}\Big|_{v_1=0} \tag{4.14}$$

Since this system is operated at very low frequencies, the C_{gs2} capacitor can be removed due to negligible current flow and high resistance. Due to this removal, all the *y*-parameters for the *a*-loop will be 0. For the *f*-loop, each case is provided separately.

For y_{11} and y_{21}, v_s is connected to the input (port 1) and the output is shorted to ground (port 2). In this case r_{o3} will have no influence and yielded the following circuit:

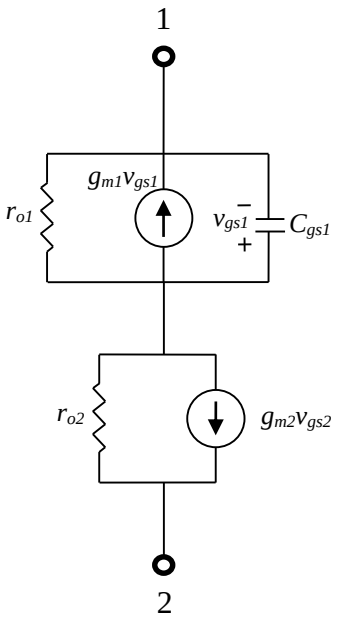


Figure 4.8. y_{11} and y_{21} circuit parameter development.

By manipulating the circuit with the use of Thévenin equivalent circuits and rearranging, the following is obtained:

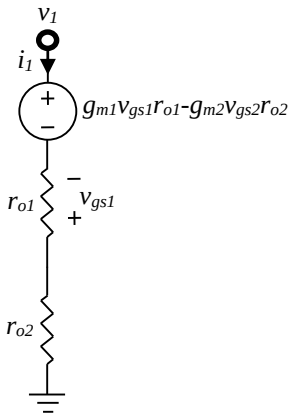


Figure 4.9. Thévenin equivalent of the y_{11} and y_{21} circuit.

The capacitor is removed since it has a high resistance at low frequencies. With this circuit, the voltage drops were added to obtain v_1. This yielded:

$$v_1 = g_{m1}v_{gs1}r_{o1} - g_{m2}v_{gs2}r_{o2} + V_{ro1} + V_{ro2} \tag{4.15}$$

By manipulating (4.15), (4.16) is obtained:

$$v_1 = g_{m1}v_{gs1}r_{o1} - g_{m2}v_{gs2}r_{o2} + i_1(r_{o1} + r_{o2}) \tag{4.16}$$

Applying a test current source of 1 A (i_1 = 1 A), (4.17) reduces to

$$v_1 = r_{o1}\left(1 + g_{m1}v_{gs1}\right) + r_{o2}\left(1 - g_{m2}v_{gs2}\right) \tag{4.17}$$

Thus y_{11} is equal to

$$y_{11} = \frac{i_1}{v_1}\Big|_{v_2=0} = \frac{1}{r_{o1}\left(1 + g_{m1}v_{gs1}\right) + r_{o2}\left(1 - g_{m2}v_{gs2}\right)} \tag{4.18}$$

Using a similar analysis for y_{21}, the following is obtained:

$$y_{21} = \frac{i_2}{v_1}\Big|_{v_2=0} = -\frac{1}{r_{o1}\left(1 + g_{m1}v_{gs1}\right) + r_{o2}\left(1 - g_{m2}v_{gs2}\right)} \tag{4.19}$$

In this case it can be seen that y_{11} is the negative of y_{21} since the same circuit is used but with reverse current flow.

For y_{12} and y_{22}, the input is shorted to ground (port 1) and the output is connected to v_s (port 2). In this case r_{o3} does have an influence. The re-drawn circuit from Figure 4.6 is given:

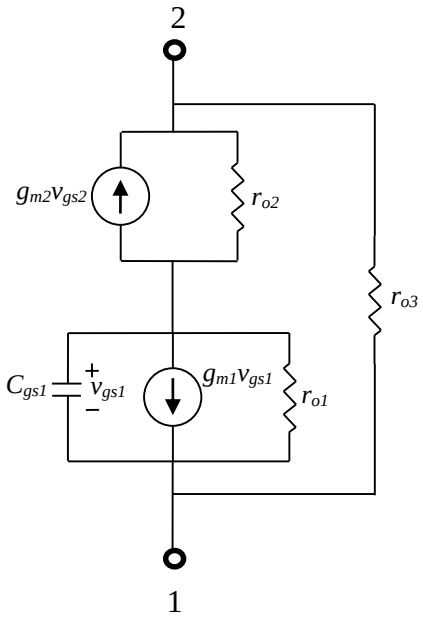


Figure 4.10. y_{12} and y_{22} circuit parameter development.

Transforming Figure 4.10 using Thévenin equivalent circuits and removing the capacitor due to high resistance at low-frequency, yields the following circuit:

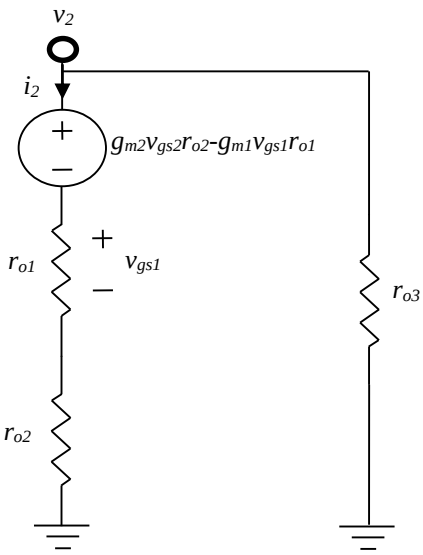


Figure 4.11. y_{12} and y_{22} circuit parameter development.

With further Thévenin manipulation, the following circuit two circuits are obtained:

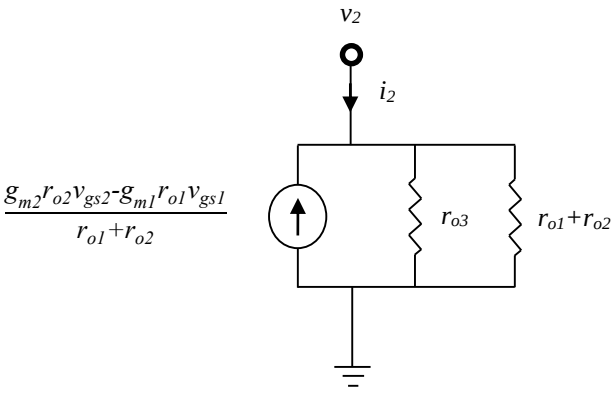


Figure 4.12. y_{12} and y_{22} circuit parameter development.

By combining the resistors and converting back to a voltage source again, the following is obtained:

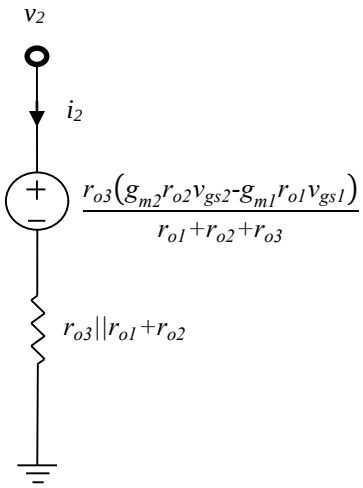


Figure 4.13. Final y_{12} and y_{22} circuit.

Using this circuit, the voltage drops are added to obtain v_2. This yielded:

$$v_2=\frac{r_{o3}\left(g_{m2}r_{o2}v_{gs2}-g_{m1}r_{o1}v_{gs1}\right)}{r_{o1}+r_{o2}+r_{o3}}+i_2(r_{o1}+r_{o2})||r_{o3} \tag{4.20}$$

Applying a test current source of 1 A (i_2 = 1 A) yields the following:

$$v_2=\frac{r_{o3}\left(g_{m2}r_{o2}v_{gs2}-g_{m1}r_{o1}v_{gs1}\right)}{r_{o1}+r_{o2}+r_{o3}}+(r_{o1}+r_{o2})||r_{o3} \tag{4.21}$$

Rearranging (4.21), the final equation for v_2 is obtained:

$$v_2 = \frac{r_{o3}\left(r_{o2}\left(1+g_{m2}v_{gs2}\right)+r_{o1}\left(1-g_{m1}v_{gs1}\right)\right)}{r_{o1}+r_{o2}+r_{o3}} \tag{4.22}$$

Thus for y_{12} and y_{22} respectively the following is obtained:

$$y_{22} = \frac{i_2}{v_2}\Big|_{v_1=0} = \frac{r_{o1}+r_{o2}+r_{o3}}{r_{o3}\left(r_{o2}\left(1+g_{m2}v_{gs2}\right)+r_{o1}\left(1-g_{m1}v_{gs1}\right)\right)} \tag{4.23}$$

$$y_{12} = \frac{i_1}{v_2}\Big|_{v_1=0} = -\frac{r_{o1}+r_{o2}+r_{o3}}{r_{o3}\left(r_{o2}\left(1+g_{m2}v_{gs2}\right)+r_{o1}\left(1-g_{m1}v_{gs1}\right)\right)} \tag{4.24}$$

The parameters required to finalise the model is the y_i and y_o parameters which is:

$$y_i = y_S + y_{11a} + y_{11f} \tag{4.25}$$

$$y_o = y_L + y_{22a} + y_{22f} \tag{4.26}$$

For y_i, it can be reduced by equating v_s to the admittance of the output of the pixel and equating $y_{11a} = 0$, as discussed earlier. When the base and emitter of the reverse-biased HBT is shorted, the small-signal model reduces to a single output resistance ($r_{O_{HBT}}$). For y_o, it can be reduced by assuming $y_L = 0$, since assuming the input to the next stage to be very large limits current flow also by equating $y_{22a} = 0$, as discussed earlier.

By replacing the required parameters, the following is obtained:

$$y_i = y_S + y_{11f} = \frac{1}{r_{O_{HBT}}} + \frac{1}{r_{o1}\left(1+g_{m1}v_{gs1}\right)+r_{o2}\left(1-g_{m2}v_{gs2}\right)} \tag{4.27}$$

$$y_o = y_{22f} = \frac{r_{o1}+r_{o2}+r_{o3}}{r_{o3}\left(r_{o2}\left(1+g_{m2}v_{gs2}\right)+r_{o1}\left(1-g_{m1}v_{gs1}\right)\right)} \tag{4.28}$$

The *y*-parameter representation is given by:

$$\frac{v_o}{i_s} = \frac{a}{1+af} \tag{4.29}$$

where

$$a=-\frac{y_{21a}+y_{21f}}{y_i\,y_o}=-\frac{y_{21f}}{(y_s+y_{11f})y_{22f}} \tag{4.30}$$

$$f=y_{12a}+y_{12f}=y_{12f} \tag{4.31}$$

Thus

$$\frac{v_o}{i_s}=\frac{a}{1+af}=\frac{-\dfrac{y_{21f}}{\left(y_S+y_{11f}\right)y_{22f}}}{1-\dfrac{y_{21f}}{\left(y_S+y_{11f}\right)y_{22f}}y_{12f}} \tag{4.32}$$

Rearranging (4.32), the following is obtained:

$$\frac{v_o}{i_s}=-\frac{y_{21f}}{y_S\,y_{22f}} \tag{4.33}$$

Replacing the *y*-parameters already calculated:

$$\frac{v_o}{i_s}=\frac{a}{1+af}=-\frac{y_{21f}}{y_S\,y_{22f}}=\frac{\dfrac{1}{r_{o1}\left(1+g_{m1}v_{gs1}\right)+r_{o2}\left(1-g_{m2}v_{gs2}\right)}}{\dfrac{1}{r_{O_{HBT}}}\dfrac{r_{o1}+r_{o2}+r_{o3}}{r_{o3}\left(r_{o2}\left(1+g_{m2}v_{gs2}\right)+r_{o1}\left(1-g_{m1}v_{gs1}\right)\right)}} \tag{4.34}$$

Assuming $g_{m1}v_{gs1}\ll 1$ and $g_{m2}v_{gs2}\ll 1$, $\frac{v_o}{i_s}$ reduces to

$$\frac{v_o}{i_s}\approx\frac{\dfrac{1}{r_{o1}+r_{o2}}}{\dfrac{1}{r_{O_{HBT}}}\dfrac{r_{o1}+r_{o2}+r_{o3}}{r_{o3}(r_{o1}+r_{o2})}}=\frac{r_{O_{HBT}}r_{o3}}{(r_{o1}+r_{o2}+r_{o3})} \tag{4.35}$$

With this model, the AC-behaviour of a 3T pixel structure can be easily simulated. This will also determine the behaviour when the detector is illuminated. Intuitively, since current flow increases significantly when illuminated, the output resistance of the pixel reduces significantly. When this happens, v_o/i_s reduces significantly as seen in the plots shown in Section 4.8.6.

4.5 NOISE MODEL APPLICABLE TO THE PIXEL

Since reverse biased diode-connected HBTs are used as the pixel element, the noise model of a diode in relation to the diode-connected HBT is needed.

4.5.1 Diode noise generators

Thermal noise is present in a diode due to the intrinsic nature of a material and is modelled as voltage and current generators. Shot noise and flicker noise are also present which is modelled as a current generator. The small-signal model equivalent circuit for a diode with noise generators is given below:

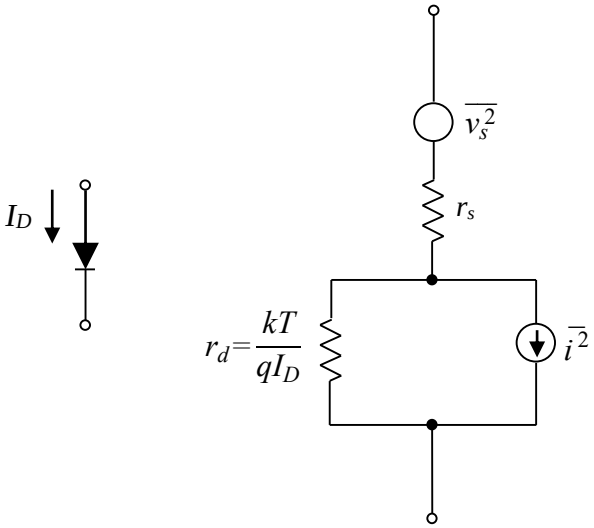


Figure 4.14. Small-signal equivalent model of a junction diode [41].

In Figure 4.14. the characteristic impedances and current generators that make up the small-signal model is shown. The resistance r_d models the shot noise resistance which is the inverse of the transconductance of the diode and r_s models the thermal resistance of the diode. The shot noise and thermal noise models are given below:

$$\overline{v_s^2} = 4kTr_s\Delta f \tag{4.36}$$

$$\overline{i^2} = 2qI_D\Delta f + K\frac{I_D^a}{f}\Delta f \tag{4.37}$$

By using the Thévenin equivalent of (4.37), the total noise of the junction diode can be modelled as a voltage noise.

4.5.2 Heterojunction Bipolar Transistor noise generators

Since the doping levels and the polarity of the three sections of HBTs differ, one cannot simply use the diode noise models to develop the HBT noise model. However, by analysing what circuit elements are eliminated due to the base-collector shorted- and base-emitter shorted configuration, the diode-connected HBT noise generators can be related to that of a junction diode.

The small-signal models of the two proposed configurations (base-collector shorted and base-emitter shorted) are given below:

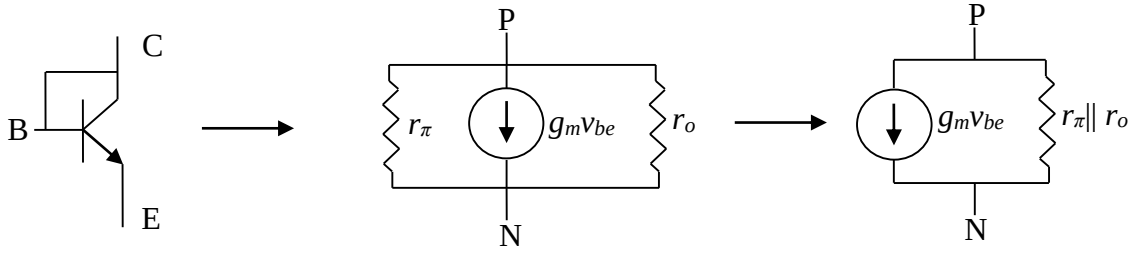


Figure 4.15. Small-signal equivalent model of a base-emitter shorted HBT [41].

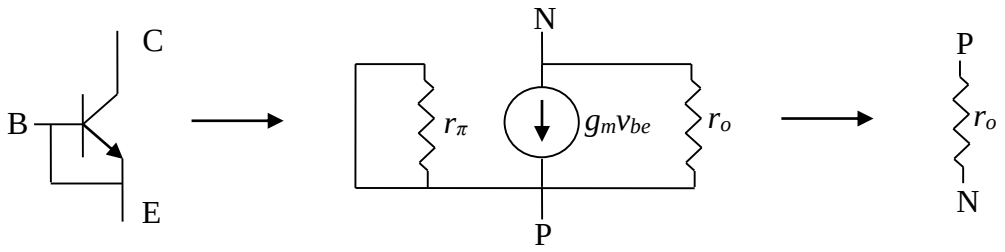


Figure 4.16. Small-signal equivalent model of a base-collector shorted HBT [41].

Figure 4.15 shows the small-signal model of the base-emitter shorted HBT. Since the base and emitter are shorted, the base-emitter voltage (v_{be}) is 0 V. Therefore, the current generator $g_m v_{be}$ is also 0 A. The r_π resistor and $g_m v_{be}$ current generator can therefore be removed completely. The final small-signal model is only the output resistor.

Figure 4.16 shows the small-signal model of the base-collector shorted HBT. Contrary to the base-emitter shorted HBT, all the elements in the small-signal model are present when the base and collector are shorted. The input resistance (r_π) and output resistance (r_o) can be combined. Intuitively, this combined lower resistance will result in a lower noise voltage. The current generator will have an insignificant influence, since the transconductance is usually in the µA range for HBTs in a 0.35 µm process. This result is confirmed in Figure 5.8. Since r_π and r_o are temperature dependent, this parallel combination can be equated to the thermal resistance (contributing to the thermal noise) of the diode. Also, since r_d models the shot noise of the diode requiring a current, r_d is only applicable to the base-collector shorted HBT.

4.6 TEMPERATURE VARIATION FOR D_{PH}

Modifying the well-known current-voltage equation for a BJT such that the base-emitter voltage (V_{BE}) is the subject of the equation and differentiating with respect to temperature, (4.38) is formulated for a constant I_C.

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_{I_C} = \frac{V_{BE} - \frac{E_{G0}}{q}}{T} - \frac{\gamma k}{q} \tag{4.38}$$

where E_{G0} is the band gap of the material used at absolute 0 K (1.17 eV for Si),
γ is a fitting parameter,
k is Boltzmann's constant (1.3807×10^{-23} J/K), and
q is the charge of an electron (1.602×10^{-19} C).

Equation (4.38) is applicable to the base-collector shorted configuration as seen in Figure 4.2 (b). Similarly, for the base-emitter shorted configuration shown in Figure 4.2 (a), $\partial V_{BC}/\partial T$ is given in (4.39).

$$\left.\frac{\partial V_{BC}}{\partial T}\right|_{I_C} = \frac{V_{BC} - \frac{E_{G0}}{q}}{T} - \frac{\gamma k}{q} \tag{4.39}$$

Since the well-known current-voltage equation for a BJT is assumed to be correct for the specified bias range set by the technology node, it is assumed that (4.38) and (4.39) are also correct over the specified bias range.

4.7 TEMPERATURE VARIATION FOR M_1, M_2 AND M_3

The two primary variables of concern for temperature sensitivity are threshold voltage (V_t) and mobility (μ_{eff}). Each of these variables are discussed separately.

For MOSFETs M_1, M_2 and M_3, the threshold voltages are given by (4.40).

$$V_t = V_{to} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right) \tag{4.40}$$

where

$$\phi_f = \frac{kT}{q} ln\left[\frac{N_A}{n_i}\right] \tag{4.41}$$

$$\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_r\varepsilon_o N_A} \tag{4.42}$$

The rate at which threshold voltage differs with temperature is given by (4.43):

$$\frac{dV_t}{dT} = -\frac{1}{T}\left[\frac{E_g}{2q} - \phi_f\right]\left[2 + \frac{\gamma}{\sqrt{2\phi_f}}\right] \tag{4.43}$$

where

$$\frac{\gamma}{\sqrt{2\phi_f}} = \frac{1}{C_{ox}}\sqrt{\frac{2q\varepsilon_r\varepsilon_o N_A}{2\phi_f}} \tag{4.44}$$

The band gap temperature dependence was obtained from Varshni's empirical expression given in (4.45):

$$E_g(T) = E_g(0) - \frac{\alpha_E T^2}{T + \beta_E} \tag{4.45}$$

where E_g (0) is the band gap energy at absolute 0 K and α_E, β_E are material-specific constants.

Equation (4.44) shows the rate at which the threshold voltage changes with respect to temperature when the source-body voltage (V_{SB}) is 0 V. Apart from the temperature parameter T, the fermi-level (ϕ_f) and band gap (E_g) are also dependent on temperature given by (4.42) and (4.45) respectively. A designer can design for a certain temperature range pre-manufacturing provided that V_{SB} is shorted. However, it is possible to make M_1, M_2 and M_3 more dependent to threshold voltage variation by not shorting V_{SB} and rather connecting these points to bond pads. In this way, the threshold voltage can be adjusted post-manufacturing. Where temperature is of great concern, V_{SB} should be connected to bond pads and where temperature is not of great concern, V_{SB} can be shorted pre-manufacturing.

Varshni's empirical relation (4.45) deviates from the theoretical requirement that mobility is proportional to T^4 when $T \rightarrow 0$ K. Thus [42] suggested that Varshni's empirical relation be modified to (4.46) for $T \rightarrow 0$ K.

$$E_g(T) = E_g(0) - \frac{\gamma_E T^4}{T^2 + \delta_E} \tag{4.46}$$

The γ_E and δ_E are different curve fitting parameters comparing to (4.45) that can be experimentally determined. This relation has to be used when $T \rightarrow 0$ K. The implemented detector as shown in Section 3.6, was measured at room temperature and 77 K. Therefore (4.45) applies to this work.

The mobility is relatively constant over a wide range of doping levels, however it is dependent on temperature. The two scattering mechanisms that influence mobility are impurity scattering and lattice scattering.

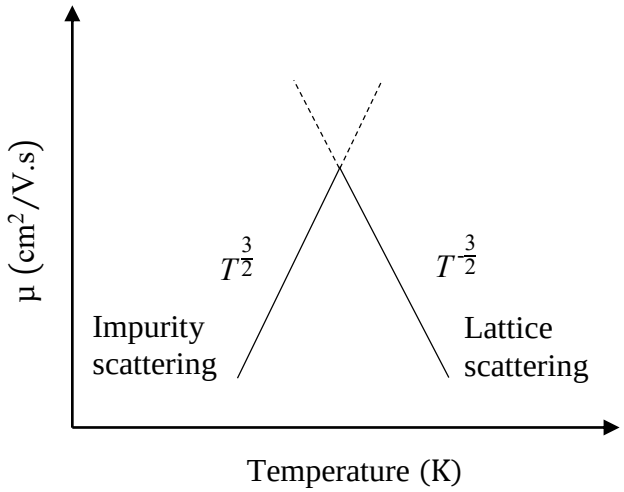


Figure 4.17. Typical μ vs temperature curve.

Figure 4.17 shows how mobility changes with temperature. As the element is heated, electrons start to vibrate and thus mobility increases. Impurity scattering occurs when a doped semiconductor's potential energy of the electron dominates due to ionised impurities. This will increase the mobility even more. However, this will not increase indefinitely as a point is reached where the atomic vibrations increase at the same rate as the electron velocity also increases thereby limiting movement of other electrons and thus decreasing the mobility (lattice scattering). The relationship of mobility and temperature is defined by (4.47):

$$\mu(T)=\mu(T_r)\left(\frac{T}{T_r}\right)^{\mathrm{ku}} \tag{4.47}$$

where T is the absolute temperature in K,

T_r is the room temperature in K,

ku is a fitting parameter (typically 1.5), and

$\mu(T_r)$ is the reference mobility at 300 K (0.14 m^2/V.s).

Threshold voltage and mobility dominates the current flowing through a MOSFET at a different v_{GS}.

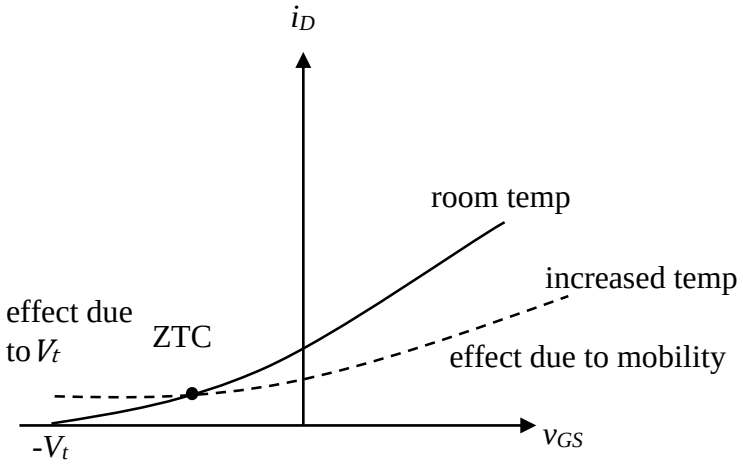


Figure 4.18. Current-voltage curve for temperatures.

Figure 4.18 shows the typical current-voltage curve for different operating temperatures for a MOSFET. At higher v_{GS} values, the effect of mobility, which is dependent on temperature, dominates, and at lower v_{GS} values (negative values included) the effect of threshold voltage dominates. Theoretically, if it is possible to bias a MOSFET close the zero-temperature coefficient (ZTC) point, the MOSFET will be temperature independent.

The effective mobility is proportional to different mobility elements all added together using Matthiessen's rule given in (4.48) [43]:

$$\frac{1}{\mu_{eff}(T,E_{eff})} \propto \frac{1}{\mu_{ph}(T,E_{eff})} + \frac{1}{\mu_{sr}(T,E_{eff})} + \frac{1}{\mu_{cb}(T,E_{eff})} + \frac{1}{\mu_{int}(T,E_{eff})} \tag{4.48}$$

where E_{eff} is the average transverse electric field,

μ_{ph} is the mobility due to phonon scattering,

μ_{sr} is the mobility due to surface roughness scattering,

μ_{cb} is the mobility due to bulk charge Coulomb scattering, and

μ_{ph} is the mobility due to interface charge Coulomb scattering.

[43] suggested the following expressions for the four different mobility elements.

$$\frac{1}{\mu_{ph}(T,E_{eff})} \propto T^{3/2} \times E_{eff}^{1/3} \tag{4.49}$$

$$\frac{1}{\mu_{sr}(T,E_{eff})} \propto T^{-1/\alpha} \times E_{eff}^{2.1} \tag{4.50}$$

$$\frac{1}{\mu_{cb}(T,E_{eff})} \propto T^{-1} \times E_{eff}^{-2} \tag{4.51}$$

$$\frac{1}{\mu_{int}(T,E_{eff})} \propto T \times E_{eff}^{-1} \tag{4.52}$$

where E_{eff} is the applied electric field and $\alpha = 2$ indicated by experimental data. It is evident from (4.49) to (4.52) that μ_{ph} and μ_{int} are more dominant at higher temperatures while μ_{sr} and μ_{cb} are more dominant at lower temperatures.

4.8 SIMULATIONS UNDER NORMAL BIASING

In this section, voltages and currents in the 3T structure are shown to illustrate the behaviour when the detector is illuminated. For all these simulations, the following parameters are used as a starting point and adjusted accordingly. Links to the spreadsheets used to obtain these graphs are given in Appendix A.1.

- AR of $W_1/L_1 = W_2/L_2 = W_3/L_3 = 2$.
- Early voltage (MOS and HBT) = 200 V.
- channel length modulation parameter = 0.005.
- threshold voltage (V_t) = 0.66 V.
- k' = 200 μA/V.
- supply voltage (V_{DD}) = 3 V.

4.8.1 Aspect ratio variation of M_1 for V_{S1}

Using (4.11) without velocity saturation, the source voltage of M_1 (V_{S1}) is plotted against the photon generated current (i_{PH}) for various ARs in Figure 4.19.

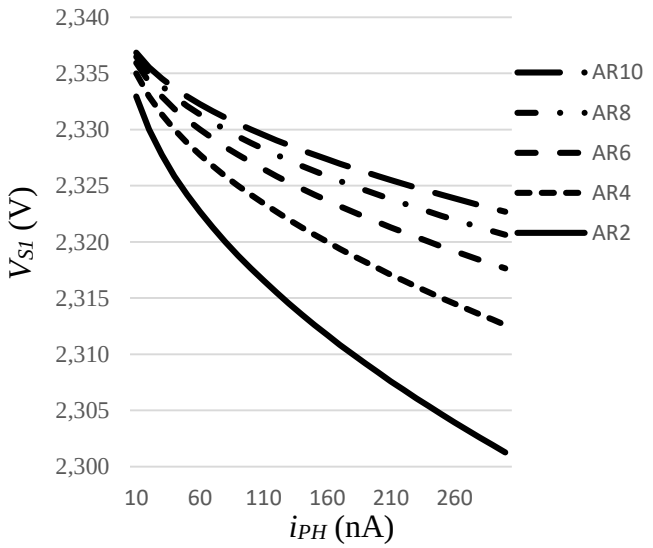


Figure 4.19. V_{S1} versus i_{PH} for various ARs of M_1.

In Figure 4.19, AR denotes the different ARs. As the AR of M_1 is increased, V_{S1} increases. Since M_1 is biased in the triode region of operation and used a non-linear resistor, the resistance is defined in (4.52).

$$R = \frac{L}{W}\frac{1}{k'(V_{GS} - V_t - V_{DS})} \tag{4.53}$$

resulting in:

$$R \propto \frac{L}{W} \tag{4.54}$$

As shown in (4.53), the resistance is indirectly proportional to the AR. Thus, as the AR is increased, V_{S1} decreases.

4.8.2 Supply voltage variation of M_1 for V_{S1}

The supply voltage is considered a process-independent parameter for this application. The process technology used can handle a maximum supply voltage of 3.3 V. Therefore, the chosen V_{DD} is 3.2 V. The chosen AR for M_1 is 2.

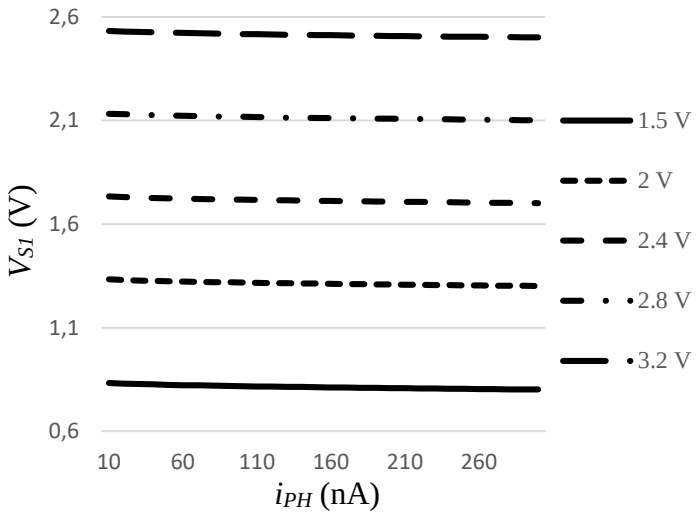


Figure 4.20. V_{S1} versus i_{PH} for varying V_{DD}.

As seen in Figure 4.20, V_{S1} increases as V_{DD} is increased. The amount of supply voltage increase is directly proportional to the increase in V_{S1}. This is to be expected when analysing (2.12). Nevertheless, Figure 4.19 shows that supply voltage variations do have an effect on the operation of the detector.

4.8.3 Aspect ratio variation for M_2 for I_{D2}

For this plot, V_{DD} is set to 3 V and the AR of M_1 is set to 2. Plotting I_{D2} vs i_{PH} for various ARs using (2.15), the plot is given in Figure 4.20.

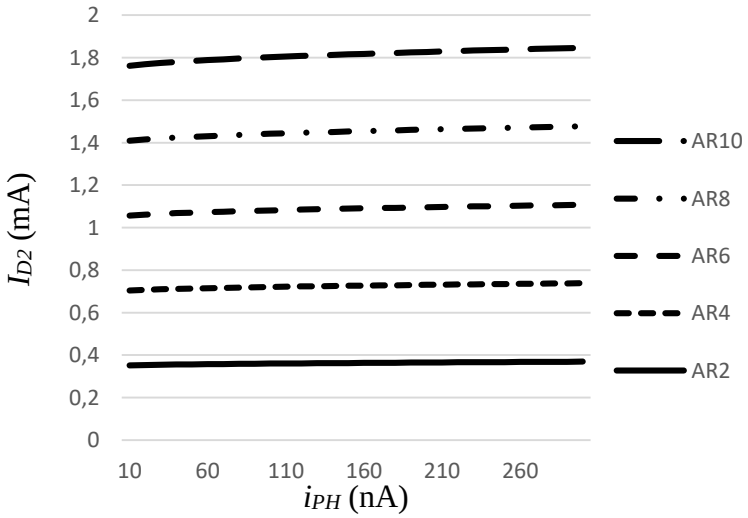


Figure 4.21. I_{D2} versus i_{PH} for various AR of M_2.

As seen in Figure 4.21, the drain current of M_2 increases as the AR increases. The influence of the previous stages (M_1 and D_{PH}) is minimal, however I_{D2} does increase as i_{PH} increases.

4.8.4 Supply voltage variation for M_2 for I_{D2}

In Figure 4.22, the ARs of M_1 and M_2 are kept at 2.

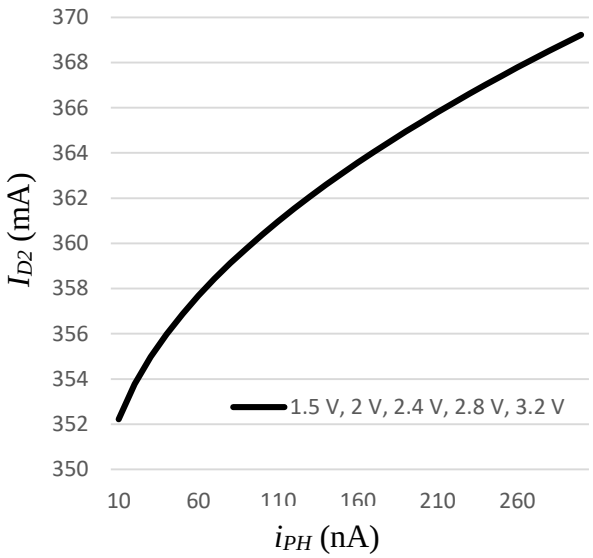


Figure 4.22. I_{D2} versus i_{PH} for varying V_{DD}.

In Figure 4.22, it can be seen that there is no change in I_{D2} when V_{DD} is varied for M_2. This is to be expected since the term V_{DD}-V_{G2} appears in (2.15). Since $V_{G2} = V_{S1}$, V_{G2} increases proportionally as V_{DD} is increased. Therefore, I_{D2} is independent to supply voltage variations.

4.8.5 Aspect ratio variation for M_2 and M_3 for V_{S2}

Plots for various combinations of ARs for M_2 and M_3 as well as V_{G3} are presented in this section. For these plots, M_2 and M_3 are biased in the linear region. It was experimentally determined that V_{G3} should be lower than 1.25 V to keep M_3 in the linear region. For Figures 4.23 to 4.25, the separate figure denominations are (a) M_3 AR 2, (b) M_3 AR 4, (c) M_3 AR 6,

(d) M_3 AR 8, (e) M_3 AR 10 and the different AR values provided in the graph are the AR values of M_2 where AR denotes the AR of M_2 and M_3.

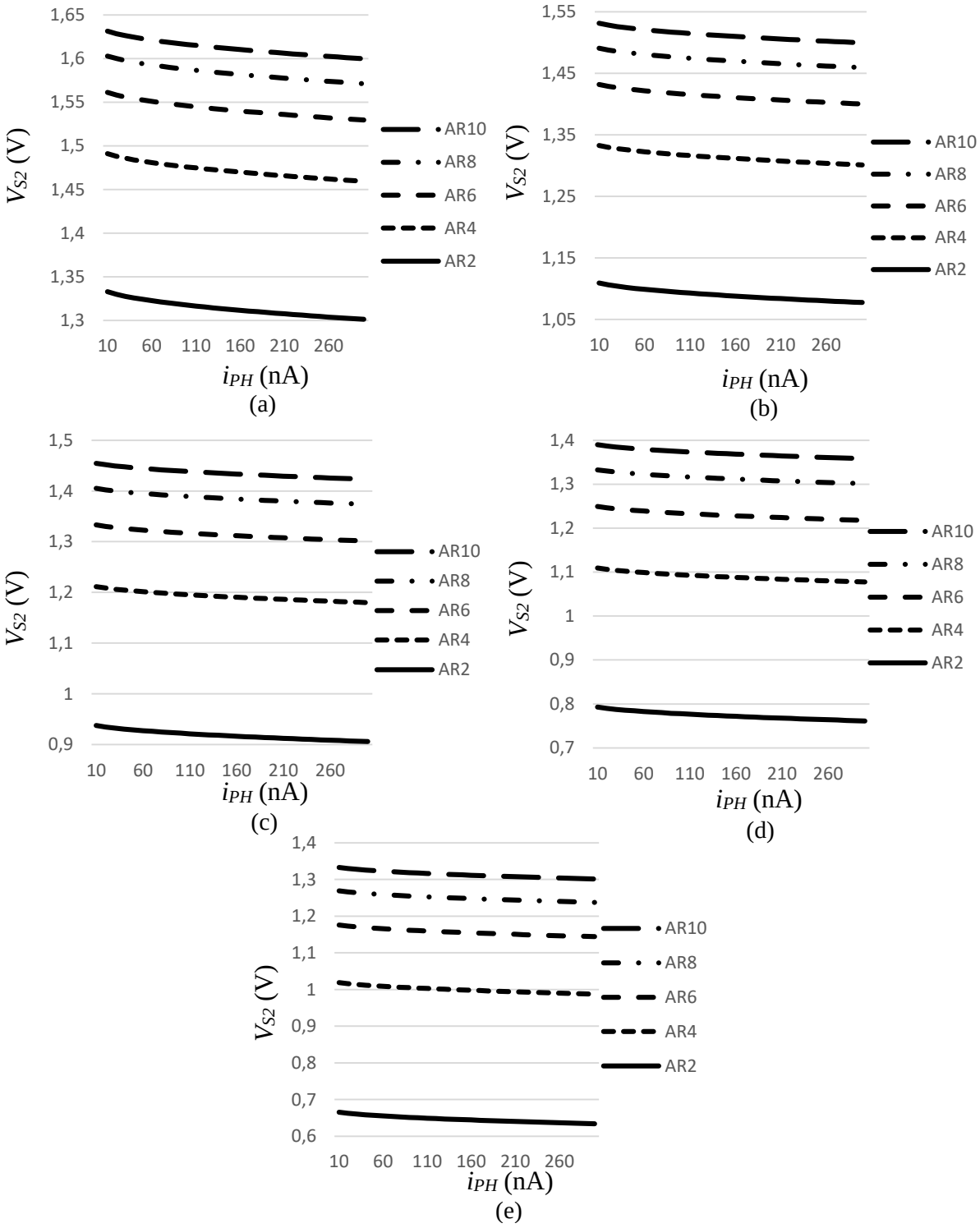


Figure 4.23. V_{S2} versus i_{PH} for varying ARs of M_2 and M_3 for V_{G3} = 1.2 V.

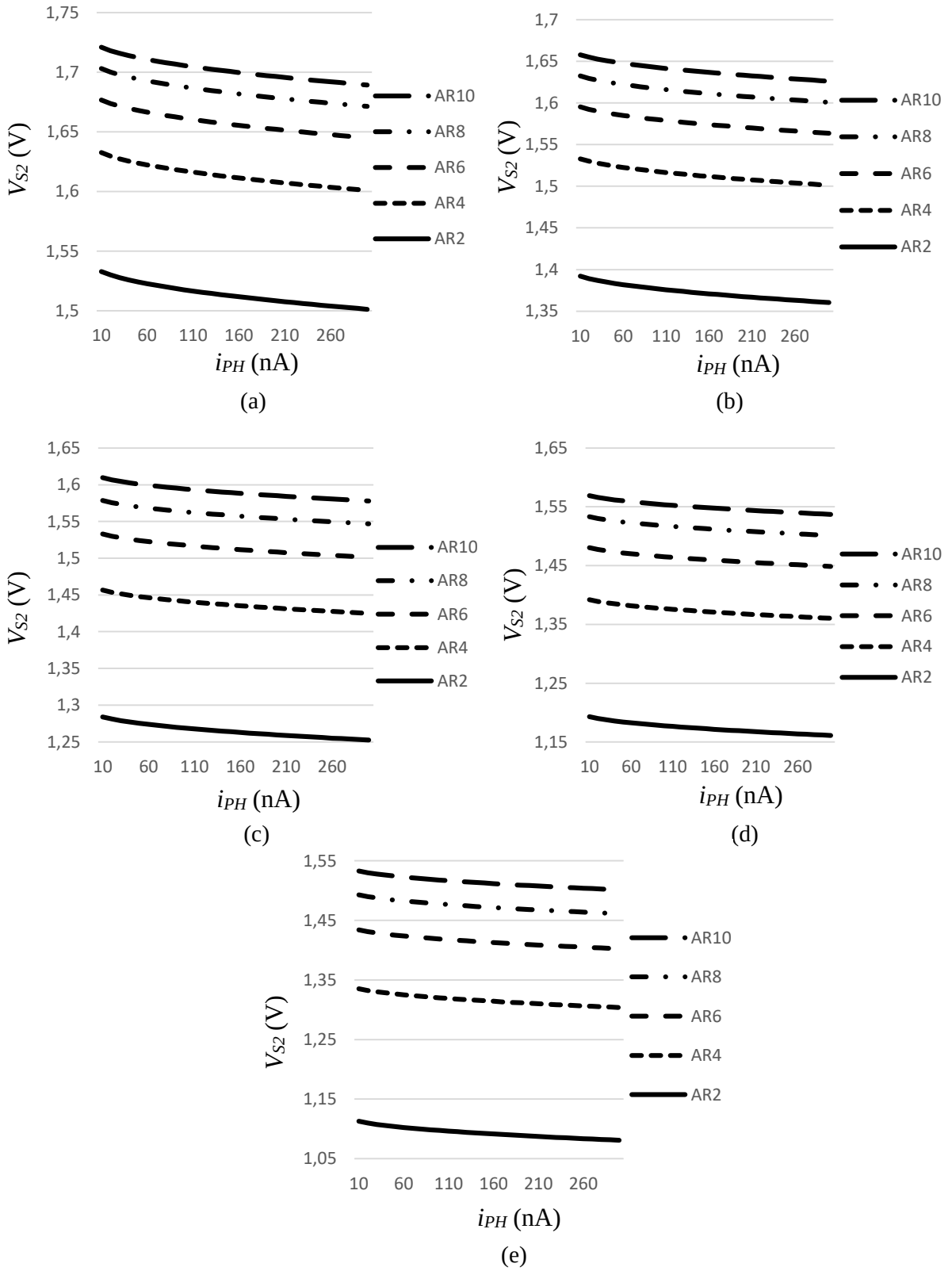


Figure 4.24. V_{S2} versus i_{PH} for varying ARs of M_2 and M_3 for V_{G3} = 1 V.

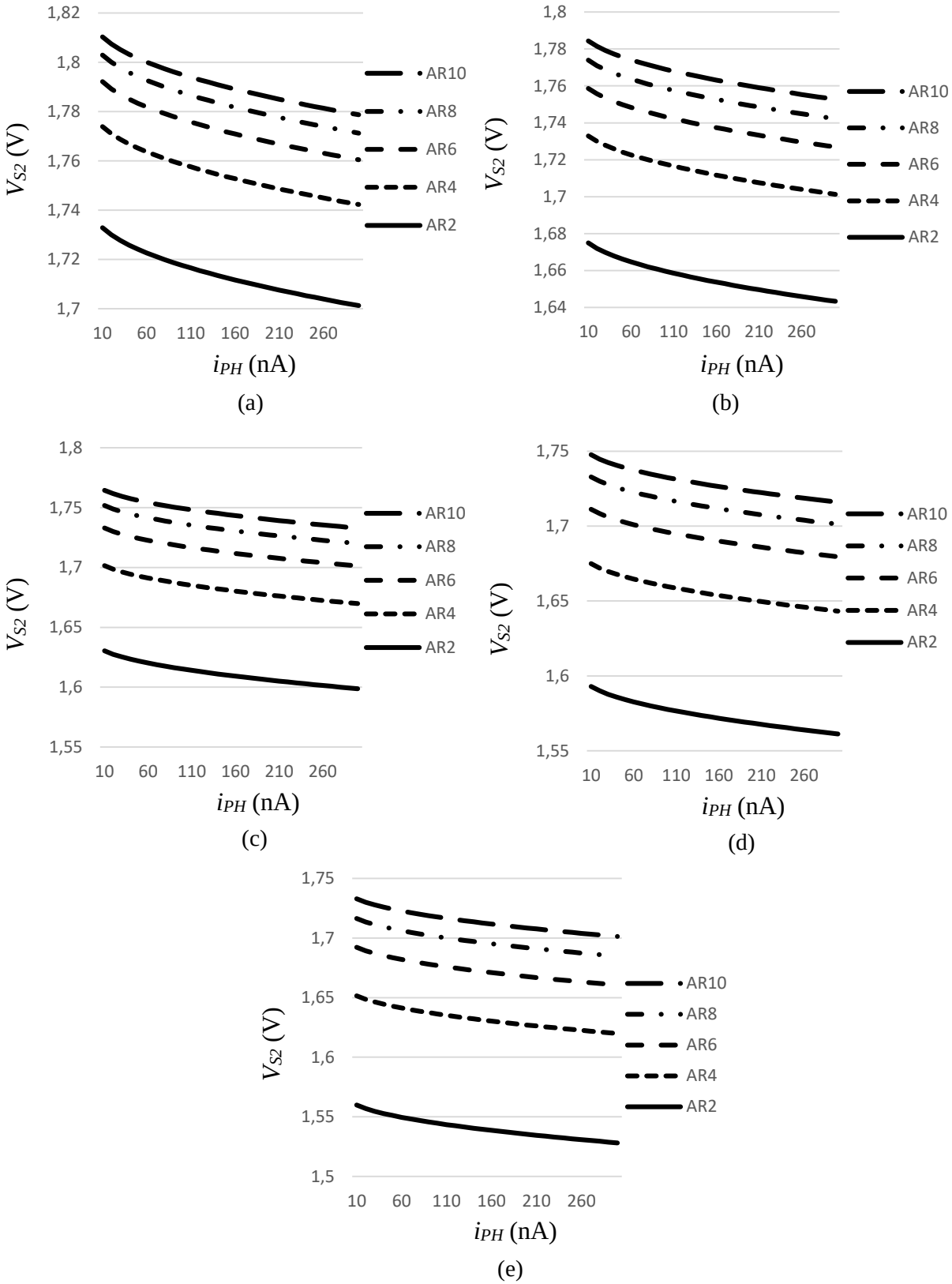


Figure 4.25. V_{S2} versus i_{PH} for varying ARs of M_2 and M_3 for V_{G3} = 0.8 V.

Figures 4.23 to 4.25 show the source voltage of M_2 (V_{S2}), for various combinations of ARs for M_2 and M_3, as well as various gate voltages of M_3 (V_{G3}). It can be seen that V_{S2} decreases as V_{G3} increases. This is to be expected since more current will flow through M_3 when V_{G3} is increased, thereby decreasing the characteristic impedance seen from the drain terminal of M_3.

In addition to this, V_{S2} increases as the AR of M_3 is increased, and V_{S2} decreases as the AR of M_2 is increased. When analysing (4.13), V_{S2} is proportional to the ARs given in (4.55).

$$V_{S2} \propto -\sqrt{\frac{W_3 L_2}{L_3 W_2}} \tag{4.55}$$

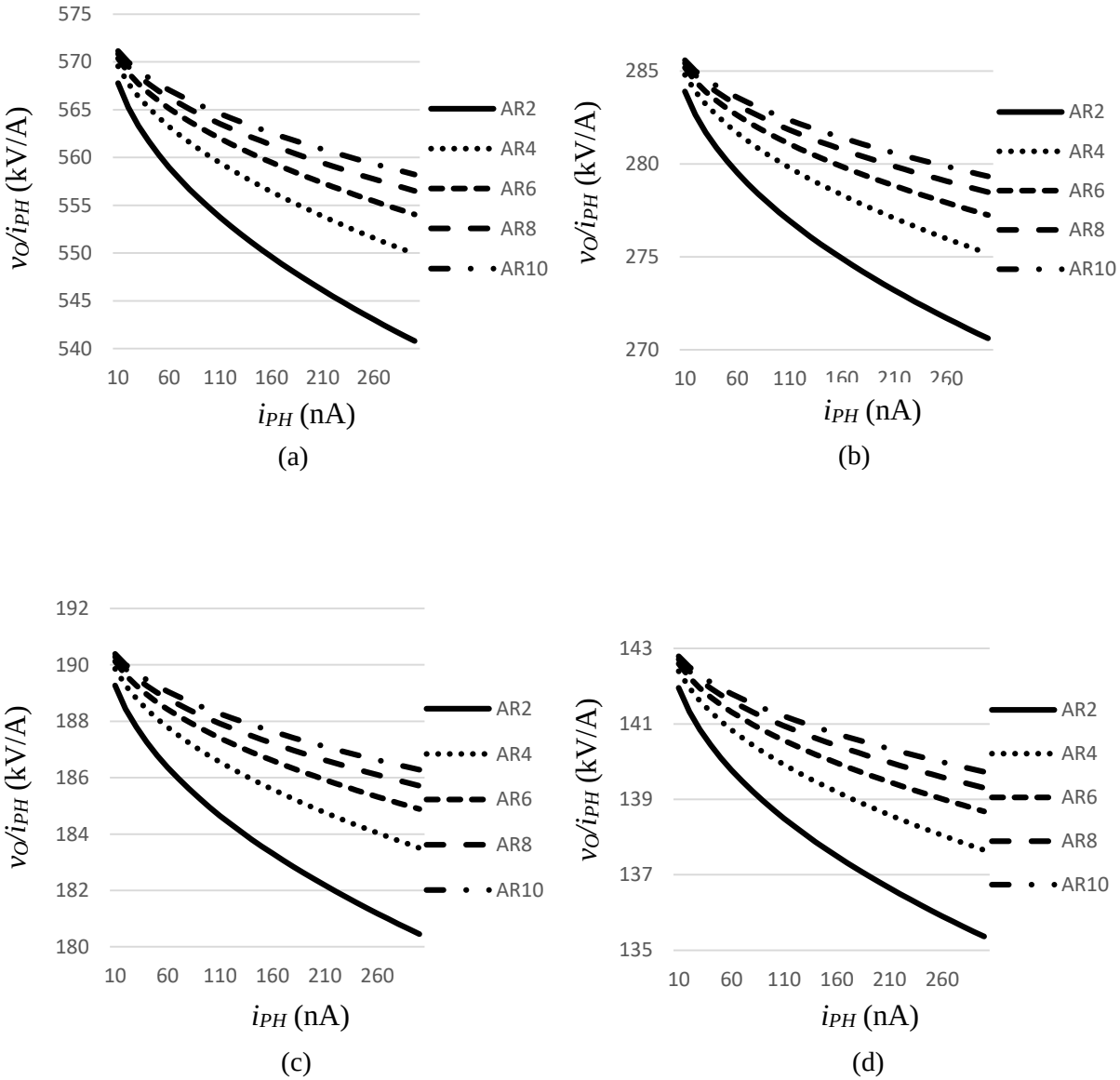
As seen in (4.53), V_{S2} is proportional to the negative of the square root of the ARs. When $\frac{W_3 L_2}{L_3 W_2}$ is less than 1, the impact that the ARs have on V_{S2} is reduced significantly. Experimentally it is determined that $\frac{W_2}{L_2}$ has to be larger than $\frac{W_3}{L_3}$ to have minimal impact on V_{S2}. This is confirmed in Figures 4.23 to 4.25 where an increase is seen as the AR of M_2 is increased and then decreases as the AR is increased to 10. When $\frac{W_2}{L_2} < \frac{W_3}{L_3}$, the impact on V_{S2} is increased significantly. This is to be expected since M_3 limits the current flow to ground and subsequent output voltage V_{S2}.

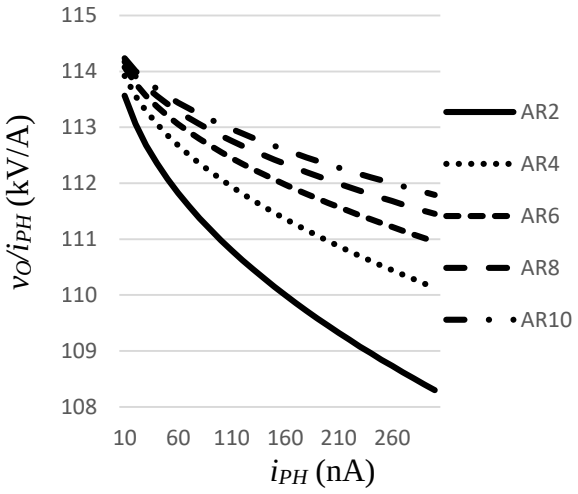
As can be seen in Figures 4.23 to 4.25, various combinations result in varying levels. Different combinations can exhibit the same V_{S2} voltage at a specific i_{PH} and it can change significantly when higher levels of radiation are received.

4.8.6 Aspect ratio variation for M_1, M_2 and M_3 for AC representation

This section illustrates the effect the ARs have on the AC representation of the 3T pixel structure. When analysing the current flow for the 3T pixel structure given in Figure 2a, all the current flowing through M_2 should flow through M_3 to enable negligible current to flow to the output, thus enabling easier impedance matching for the next stage. It is for that reason that I_{D2} is set equal to I_{D3} in the derivation described in Chapter 2. A change in the AR of M_3

does not affect the transresistance gain (v_O/i_{PH}). However, a change in the ARs of M_1 and M_2 affects v_O/i_{PH} significantly. As seen in Figure 4.26, the effect of the AR of M_1 is less than that of M_2 on v_O/i_{PH}.





(e)

Figure 4.26. v_O/i_{PH} versus i_{PH} for various ARs of M_1 and M_2.

(a) M_2 AR 2 (b) M_2 AR 4 (c) M_2 AR 6 (d) M_2 AR 8 (e) M_2 AR 10.

In Figure 4.26 the ARs for M_1 and M_2 were varied and the resulting v_O/i_{PH} values are shown, as i_{PH} is increased. A decrease in v_O/i_{PH} is seen in all the combinations as i_{PH} is increased, which is expected when analysing (4.35). This is due to the reduced $r_{O_{HBT}}$. This effect is confirmed in the experimental measurements provided in Chapter 5.

4.8.7 Supply voltage variation on AC representation

Since the derivation of v_O/i_{PH} was done where I_{D2} is set equal to I_{D3}, V_{DD} appears in both current equations and therefore cancels out. The result is that supply voltage variations do not affect v_O/i_{PH}. Additionally, since this is an AC representation of the circuit, DC variations such as supply voltage variations will not affect v_O/i_{PH}.

4.8.8 Temperature variation simulations on D_{PH}

Since temperature directly influences mobility and mobility influences the base-emitter voltage of the pixel, the rate of change in base-emitter voltage (v_{BE}) with respect to temperature is given in Figures 4.27 (a) and (b) for Si and Ge BJTs respectively.

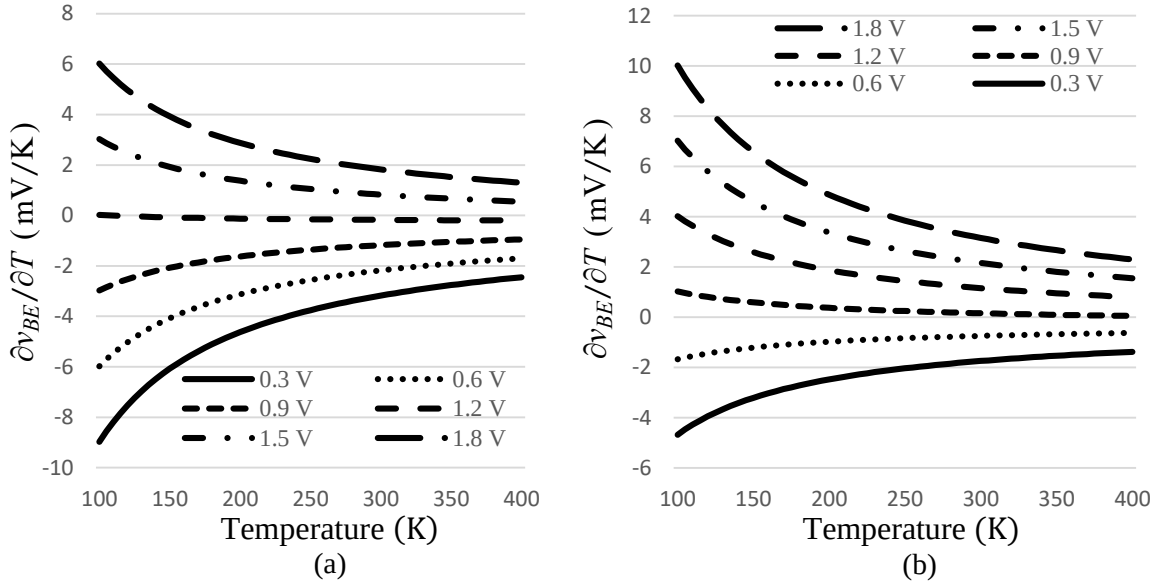


Figure 4.27. $\frac{\partial v_{BE}}{\partial T}$ for different operating temperatures.

(a) Si and (b) Ge.

From Figure 4.27, it can be seen that if v_{BE} is less than the E_g of the material, the $\frac{\partial v_{BE}}{\partial T}$ dependence is negative whereas when v_{BE} is more than E_g, the $\frac{\partial v_{BE}}{\partial T}$ dependence is positive. As the operating temperature is increased, the rate of the $\frac{\partial v_{BE}}{\partial T}$ dependence is also reduced. This is to be expected since the hotter the material, the more energy the electrons exhibit requiring less energy for an outside electron to cross the depletion region. In this work, a hybrid of Si and Ge is used. Typically, when two different materials are used where the one is doped into the other material, the E_g changes proportionally. For Si doped with Ge, doping cannot be done indefinitely as this combination will become brittle and may break. Therefore, the doping levels of Ge are kept low. Figure 4.28 shows the $\frac{\partial v_{BE}}{\partial T}$ dependence against temperature for different levels of Ge where v_{BE} is set at 0.6 V.

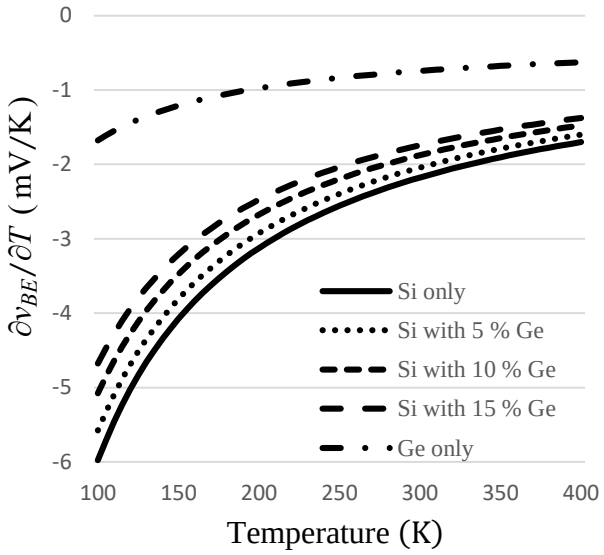


Figure 4.28. $\frac{\partial v_{BE}}{\partial T}$ for different operating temperatures for different band-gaps.

As seen in Figure 4.28, the $\frac{\partial v_{BE}}{\partial T}$ dependence changes proportionally as the band-gap is changed. This can be a critical design point as with improper selection of design parameters, temperature variations may play a big role. Additionally, the band-gap of a material is also dependent on temperature as seen in Figure 4.29.

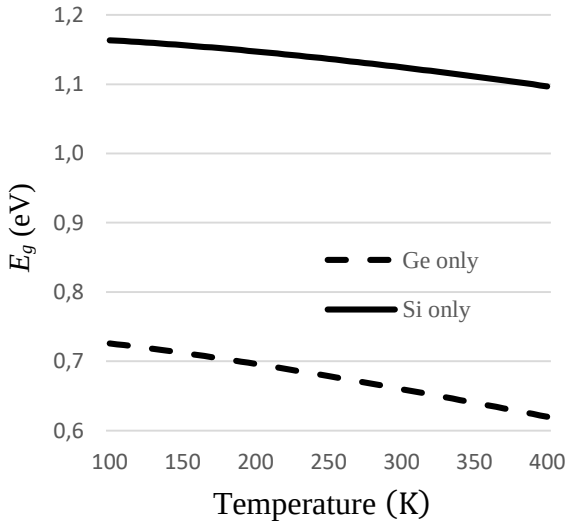


Figure 4.29. E_g (eV) for different operating temperatures.

Figures 4.27 to 4.29 show that temperature has a significant influence in the operation of a reverse-biased diode-connected SiGe HBT used as a pixel. The well-known diode current-voltage equation applies when the base is shorted with the emitter or collector. Intuitively,

since the doping levels of the emitter and collector differs, the I_S parameter in the diode equation will differ as well. This effect is confirmed in Chapter 5 for the measured results of the pixel only.

4.8.9 Temperature variation simulations on M_1, M_2 and M_3

As discussed in Section 4.7, the mobility and threshold voltage varies with temperature for MOSFETs.

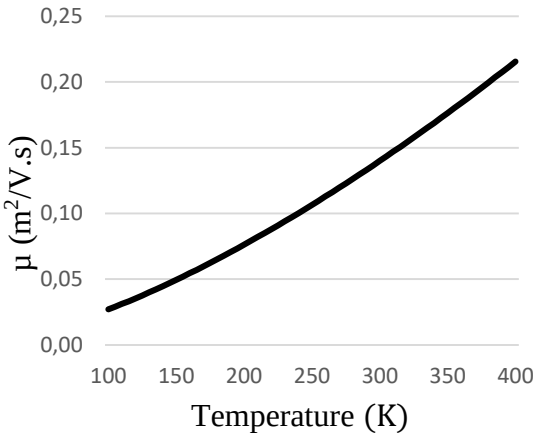


Figure 4.30. μ for different operating temperatures in a MOSFET.

Figure 4.30 shows how mobility increases with temperature for Si for a MOSFET in the chosen process technology for this work. The discussion given in Section 4.7, where the mobility will decrease above a certain temperature, applies. For the purpose of this section, it is assumed that the mobility will increase. Secondly, the threshold voltage differs as the temperature is changed as discussed in Section 4.7. The rate at which the threshold voltage changes with temperature is given in Figure 4.31.

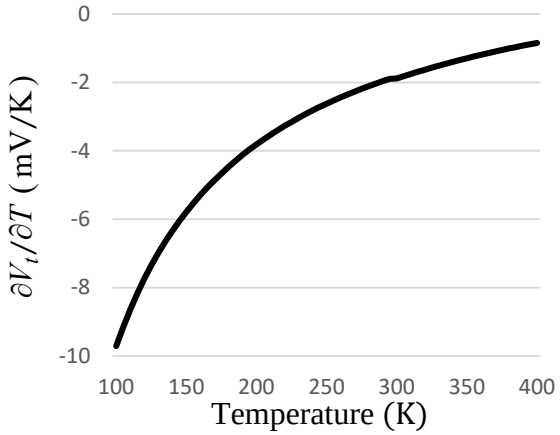


Figure 4.31. $\frac{\partial V_t}{\partial T}$ for different operating temperatures in a MOSFET.

As the temperature is increased, the rate reduces. The negative coefficient shows that the temperature dependence of the threshold voltage decreases as the temperature increases. This phenomenon makes it viable to use Si-based technology for readout circuitry of a CMOS detector at room temperature. The temperature variation at room temperature, although small, will still have an effect on the operation of the detector, however.

Since mobility and threshold voltage are two opposing effects as discussed in Section 4.7, Figure 4.32 shows the current through a MOSFET with the same parameters used in this chapter where the mobility is varied due to temperature variations.

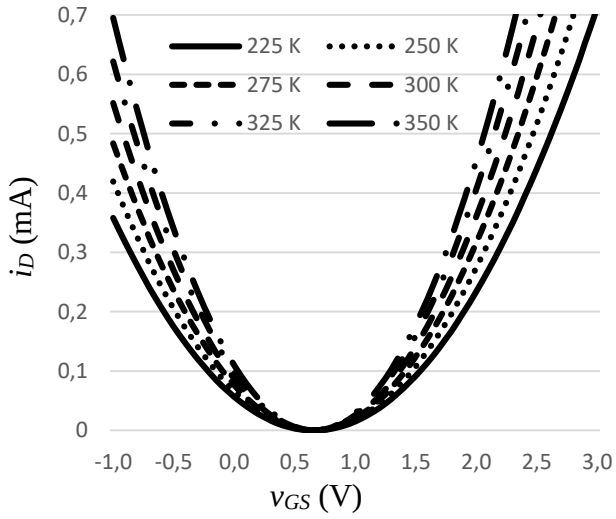


Figure 4.32. Drain current (i_D) versus gate-source voltage (v_{GS}) for different operating temperatures in a MOSFET.

Using Figure 4.32, the ZTC operating point is shown to be that of the threshold voltage. Biasing the MOSFETs such that v_{GS} is close to the threshold voltage, the MOSFETs and subsequent readout circuitry will be temperature independent. Analysing the plots in Sections 4.8.1 to 4.8.7, it is found that the v_{GS} is close to the chosen V_t making the readout circuitry temperature independent.

4.9 CONCLUSION

This chapter provided insight into how the detector will operate when bias voltage, bias current, AR and temperature are varied or selected. The small-signal derivation using *y*-parameters is provided with appropriate assumptions. The temperature sensitivity for the pixel is also discussed.

The SNR value consists of a voltage with a noise value. Therefore, by using the mathematical derivation given in this chapter, the resulting SNR can be calculated using (2.12) to (2.18) and (4.35). Eq. (4.35) is indirectly applicable to the SNR as it depicts the small-signal behaviour of the 3T structure. When designing a detector, the objective of this work is to create the possibility for a designer or researcher to choose a SNR value and then calculate the resulting process-independent parameters. By simply using MATLAB™ `math`-function, one can select a final SNR value (or a voltage value) and then the specific process-independent value can be calculated.

The final output voltage of the full detector is modelled in this chapter together with the noise model of the pixel. The noise model of a MOSFET is well-known and is comparatively much higher than a BJT for the same bias current when analysing the equivalent input noise resistance. There are two feedback loops with M_1 and M_2. However, the noise is reduced because feedback reduces gain in a common-source configuration, resulting in a consistent SNR. For that reason, noise modelling for M_1 and M_2 was not done. The biasing transistor M_3 is also in a common-source configuration where the noise model is well-known and therefore not included.

The modelling procedure should be started by selecting process-independent parameter values and simulating the detector to determine the SNR. Once a realistic value has been obtained, then the detector should be optimised for temperature by selecting the correct temperature. After that step, then the AR ratio needs to be selected to achieve the desired SNR. Once that is done, then the correct bias voltage needs to be selected. As seen in Figure 4.22, the bias voltage does not affect the current through M_2 and M_3 whereas it does affect the final output voltage. Depending on the criteria of optimisation, one would adapt accordingly.

CHAPTER 5 DISCUSSION

5. CHAPTER OVERVIEW

Chapter 4 presented the modelling and simulations of the 3T pixel structure. More specifically, the DC and AC modelling using *y*-parameter representation were presented in detail with equations. Those equations were simulated with certain parameters fixed and one varied. In this way, the influence of each parameter can be determined with respect to the final output.

In this chapter, the measured results are presented. Specifically, the I-V curves and noise voltage of the pixel, as well as the time-domain behaviour of the complete detector is presented. Time domain behaviour shows a reduction in amplitude of the output as the illumination strength increases corresponding to the simulated version in both the DC and the small-signal models developed. Lastly, the noise content of the complete detector is also given. The pixel noise was deducted from the total noise to determine the noise that the peripheral circuitry added in this system.

The current-voltage characteristics and noise measurements are discussed in Section 5.1 and 5.2. In Section 5.3, the time-domain response of the full detector is discussed. Section 5.4 provides the measured noise of the full detector. Section 5.5, summarises and concludes the chapter.

5.1 I-V CURVES OF THE PIXEL

The measured I-V curves of the pixel are given in this section. Figures 5.1 and 5.2, published by the author in 2018, show the I-V curves for the base-emitter and base-collector shorted HBT configurations given in Figures 4.2 (a) and (b). The data points of the measurements are given in Appendix A.2.

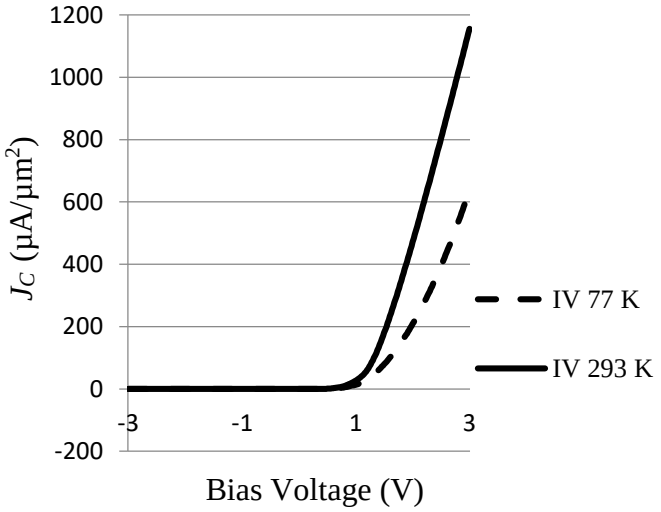


Figure 5.1. J_C vs bias voltage measurements of the base-emitter shorted HBT [41].

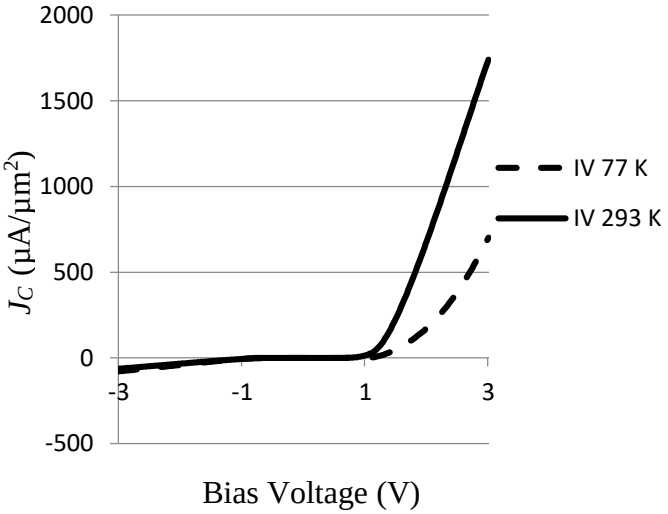


Figure 5.2. J_C vs bias voltage measurements of the base-collector shorted HBT [41].

Figures 5.1 and 5.2 show that the current density (J_C) decreases as the device is cooled. A physical reason for this could be that carrier freeze-out occurs at much higher temperatures in SiGe materials compared to Si-only materials. Doping a material increases the ionization

energy needed to release an electron from the valence band to the conduction band. Cooling the material also increases the ionisation energy required to release an electron. Carrier freeze-out occurs when the ionisation energy is too low to be able to produce carriers in the semiconductor's valence band. The colder the device, the less thermal energy is absorbed, and de-ionisation occurs. The actual measured data points are given in Appendix A.2 and A.3.

Equations (5.1) and (5.2) show the change in donor and acceptor atom ionization energy when doping concentration and temperature changes [44]:

$$\Delta E_D = E_{D0} - 3.1\times10^{-8} N_D^{\frac{1}{3}} + \left(200T^{-1} - 0.66\right) \tag{5.1}$$

and

$$\Delta E_A = E_{A0} - 3.037\times10^{-8} N_A^{\frac{1}{3}} + \left(200T^{-0.95} - 0.88\right) \tag{5.2}$$

Equations (5.1) and (5.2) demonstrate that ionisation energy is directly proportional to the doping concentration and indirectly proportional to the operating temperature. This explains why carrier freeze-out in more heavily doped semiconductors occurs at far colder temperatures. A combination of foreign doping atoms which decreases the ionisation energy and series resistance results in carrier freeze-out occurring in SiGe material at much higher temperatures compared to Si-only materials.

In Figure 5.2, the J_C for reverse biased voltages is increasing as the device is more negatively biased. The current flow is severely restricted due to the lightly doped Si substrate between the base and collector. This created a *p-i-n* diode which gained the interest of researchers in sensor technology due to the ability to change the detecting radiation characteristics by simply changing the size and shape of the layout. A small dip in current flow is seen at 276 K, which reduces to extremely low reverse current flow as the device is further cooled and remains constant as the device is cooled to lower than 186 K. For all practical purposes, the reverse biased current flow can be taken as 0 A when compared to the forward biased current flow.

For the base-collector and base-collector shorted HBT, the current-temperature curves are given in Figures 5.3 and 5.4 for 2 V and 3 V forward bias respectively. Bias voltages smaller than 2 V produced the same trend but 2 V and 3 V figures will suffice for the purpose of the carrier freeze-out discussion.

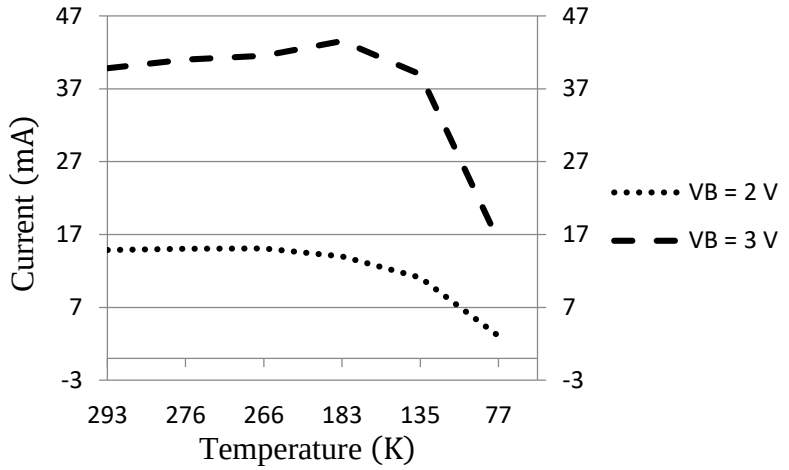


Figure 5.3. Current-temperature measurements for different biasing voltages for base-collector shorted HBT [41].

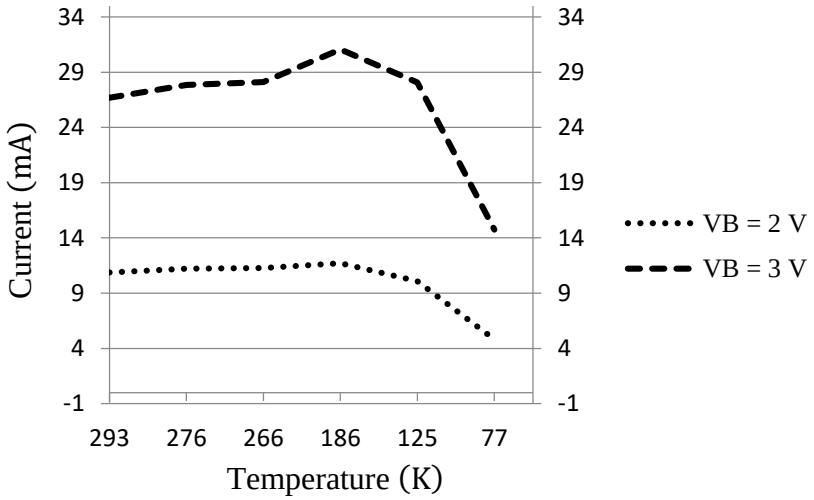


Figure 5.4. Current-temperature measurements for different biasing voltages for base-emitter shorted HBT [41].

Except for the amplitude, the current flow trend in Figure 5.3 follows the same trend of the base-emitter shorted HBT as shown in Figure 5.4. The emitter is more heavily doped than the base and collector, and therefore more electrons are available for conduction. Consequently, the series resistance is reduced and the increased current flow is observed

under the same biasing voltage. At around 186 K temperature, the current flow decreases, showing carrier freeze-out. Since the same trend is observed in both configurations, it validates the method used to perform these measurements, as discussed in Chapter 3.

The current flow seen in Figure 5.4 for the reverse biased base-collector shorted HBT is much larger than that of the base-emitter shorted HBT. This is also due to the reduced series resistance. Since the doping level of the emitter is much higher than the base and collector, the induced electrical field is high and can result in substantial parasitic tunnelling leakage currents which could explain the higher current flow.

There is a trade-off as regards which configuration should be used as a detecting element. The base-collector shorted HBT occupies a smaller area with larger current flow whereas the base-emitter shorted HBT has a smaller current flow with a larger area. The use of an intrinsic region which is applicable to the base-emitter shorted diode-connected HBT has to be decided upon.

5.2 NOISE OF THE PIXEL

In this section, the same two configurations of base-emitter shorted HBT and base-collector shorted HBT are used to illustrate the inherent noise that these configurations exhibit. The chosen bias voltage was 3.3 V. The chosen resistor was 1 kΩ.

Since the spectrum analyser was placed over the HBT, three noise sources are measured (the HBT, the resistor and the power supply). Figure 5.5 shows how the separate noise sources make up the measured noise when biased.

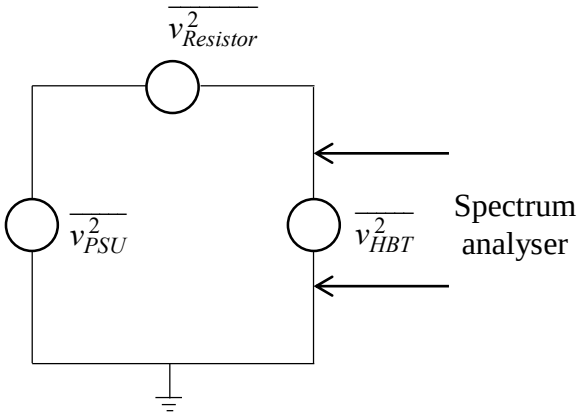


Figure 5.5. Noise sources in the pixel noise measurements.

Figure 5.5 also shows where the spectrum analyser was connected to measure noise. Since each noise source contributes to the total noise separately, the total noise voltage in this measurement setup is equal to:

$$\overline{v_{measured}^2} = \overline{v_{HBT}^2} + \overline{v_{Resistor}^2} + \overline{v_{PSU}^2} \tag{5.3}$$

The noise voltages of the resistor ($v_{Resistor}^2$) and the power supply (v_{PSU}^2) has to be deducted from total measured noise voltage to obtain the noise voltage of the HBT itself. A resistor exhibits thermal noise while the power supply has a white noise spectrum of 20 nV/$\sqrt{\text{Hz}}$ only.

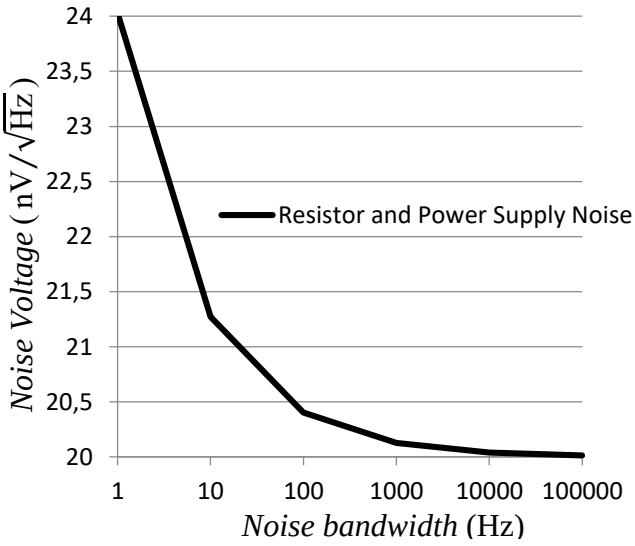


Figure 5.6. Measured power supply and resistor noise voltage.

The noise voltage spectrum of the power supply and resistor used in the measurement setup are given in Figure 5.6. Fortunately, the noise voltage of the power supply and resistor is small enough not to have a significant influence on the measured noise and therefore the measured noise voltage can be taken as the noise voltage of the diode-connected HBT. Figures 5.7 and 5.8 show the noise voltages for the base-emitter shorted and base-collector shorted HBTs.

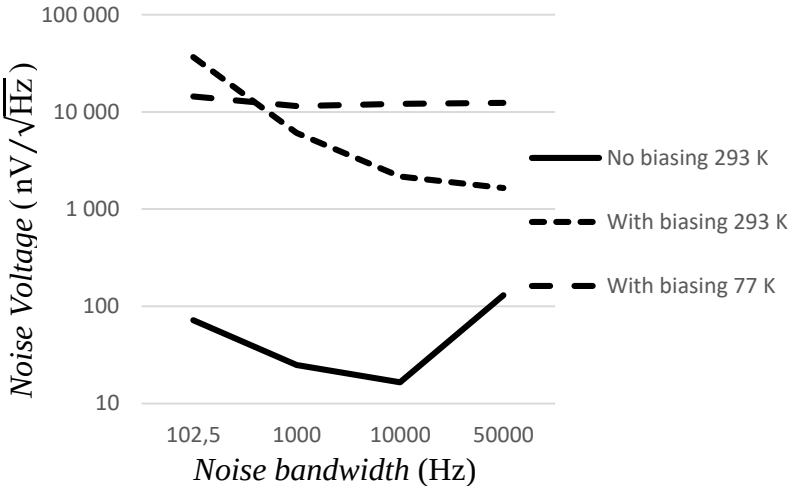


Figure 5.7. Measured noise voltage of base-emitter shorted HBT [41].

The measured current flow of the base-emitter shorted HBT is 800 µA at 293 K, and 548 µA at 77 K. This corroborates the carrier freeze-out phenomenon as seen in Figure 5.4 with reduced J_C. This noise spectrum is consistent with other measured noise results [24].

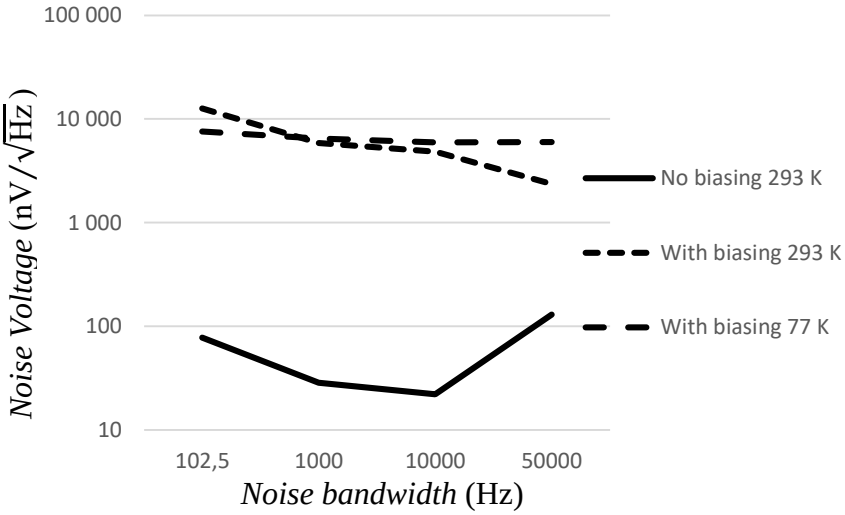


Figure 5.8. Measured noise voltage of base-collector shorted HBT [41].

The measured current flow of the base-collector shorted HBT is 2.13 mA at 293 K, and 2 mA at 77 K.

With biasing at 293 K, the base-emitter shorted HBT has a noise voltage of 36 $\mu V/\sqrt{Hz}$ at 102.5 Hz dropping to 1.515 $\mu V/\sqrt{Hz}$ at 50 kHz, whereas the base-collector shorted HBT has a noise voltage of 12.6 $\mu V/\sqrt{Hz}$ at 102.5 Hz, dropping to 2.228 $\mu V/\sqrt{Hz}$ at 50 kHz.

With biasing at 77 K, the base-emitter shorted HBT has a noise voltage of 14.48 $\mu V/\sqrt{Hz}$ at 102.5 Hz dropping to 12.42 $\mu V/\sqrt{Hz}$ at 50 kHz, whereas the base-collector shorted HBT has a noise voltage of 7.56 $\mu V/\sqrt{Hz}$ at 102.5 Hz, dropping to 5.981 $\mu V/\sqrt{Hz}$ at 50 kHz.

By analysing Figures 5.7 and 5.8, two observations can be made. Firstly, as the device is cooled, the flicker noise is much flatter. Since current flow is heavily restricted due to de-ionization and resulting carrier freeze-out, this is an expected result. The restricted current flow results in a smaller noise voltage at lower noise frequencies. The second observation is that there is lower noise voltage of the base-collector shorted HBT when compared to the base-emitter shorted HBT. This is expected since the emitter is more heavily doped than the base and collector, which results in a smaller series resistance than the base-emitter shorted HBT. This is also confirmed with the small-signal models shown in Figures 4.15 and 4.16 where the base-emitter shorted HBT contains an output resistance of (r_o) only as opposed to the base-collector shorted HBT which contains a current generator and an input resistance (r_π) in parallel with the same output resistance.

This behaviour suggests that the base-collector shorted HBT is the better configuration to use for diode-connected HBTs in detecting applications.

5.3 TIME-DOMAIN RESPONSE OF THE FULL DETECTOR

The time-domain response of the full detector is discussed in this section. The expected behaviour of the transresistance model given in (4.35) is confirmed.

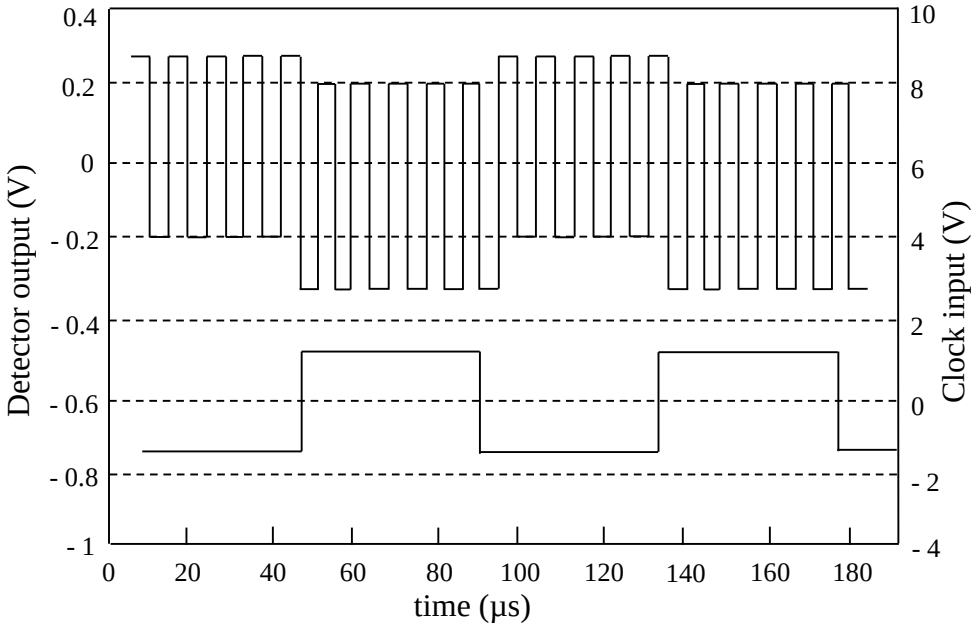


Figure 5.9. Time domain response of the full detector with no illumination [21].

In Figure 5.9, the detector output is shown on top and the clock input is shown at the bottom with no illumination present. The clock input is a square wave input connected to the transmission gate. When the clock input is low, an output is seen. This is due to leakage current through the transmission gate even though the transmission gate exhibits a relatively high series resistance. When the clock input is high, the series resistance is lower and therefore the output is also lower. The voltage swing is also somewhat higher. The output seen is for a multi-pixel detector. The same principles of detector development still apply but there is some energy lost due to current flow in unwanted circuits when the specific pixel is not read. Since this research is about a low-frequency mathematical model, this cross-talk is not addressed. Further work can be done to extend these models to accommodate the cross-talk. In addition to this, the output resistance of the transmission gate is very low when ON, whereas the model was developed by assuming a high input impedance in the subsequent devices connected to the output of the detector.

Since an output is observed when the transmission gate is ON, the removal of the transmission gate is one design improvement that can be made to this specific implemented detector. This removal will not affect the developed model as the transmission gate is placed at the output of the detector.

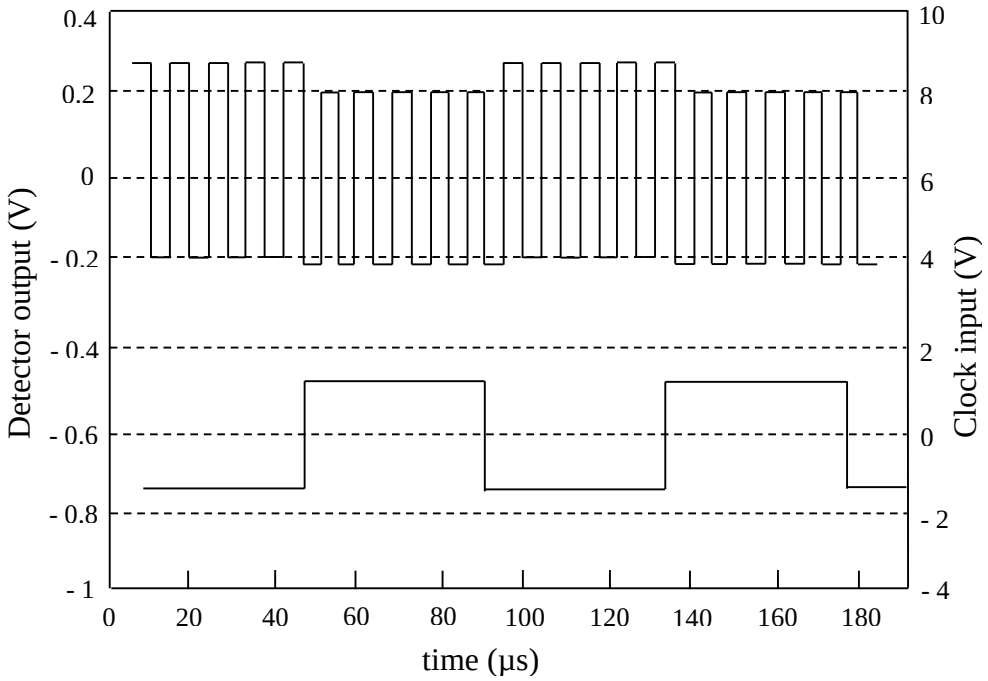


Figure 5.10. Time domain response of detector with illumination [21].

Figure 5.10 shows the time domain response of the detector with illumination. The illumination used is between 630 nm and 680 nm wavelength with an intensity of 31 mW/cm^2. Comparing Figure 5.7 with Figure 5.8, a reduction in voltage swing is observed when the clock is high. This is in line with the *y*-parameter model documented in (4.35) where the transresistance reduces when the pixel is illuminated. At the same time, the bottom part of the voltage swing is reduced, which implies that the DC level of the output increases slightly. This is due to the effects introduced by the transmission gate and TIA to the detector. As the research is about the 3T structure model development itself and not inclusive of the transmission gate and the TIA, this was not analysed further and left for future work.

5.4 MEASURED NOISE OF THE FULL DETECTOR

The measured noise voltage of the full detector is discussed in this section. A prototype chip discussed in a previous publication by this author was used to measure the noise voltage. This prototype included a frequency divider, multiplexer, transmission gate and a TIA amplifier.

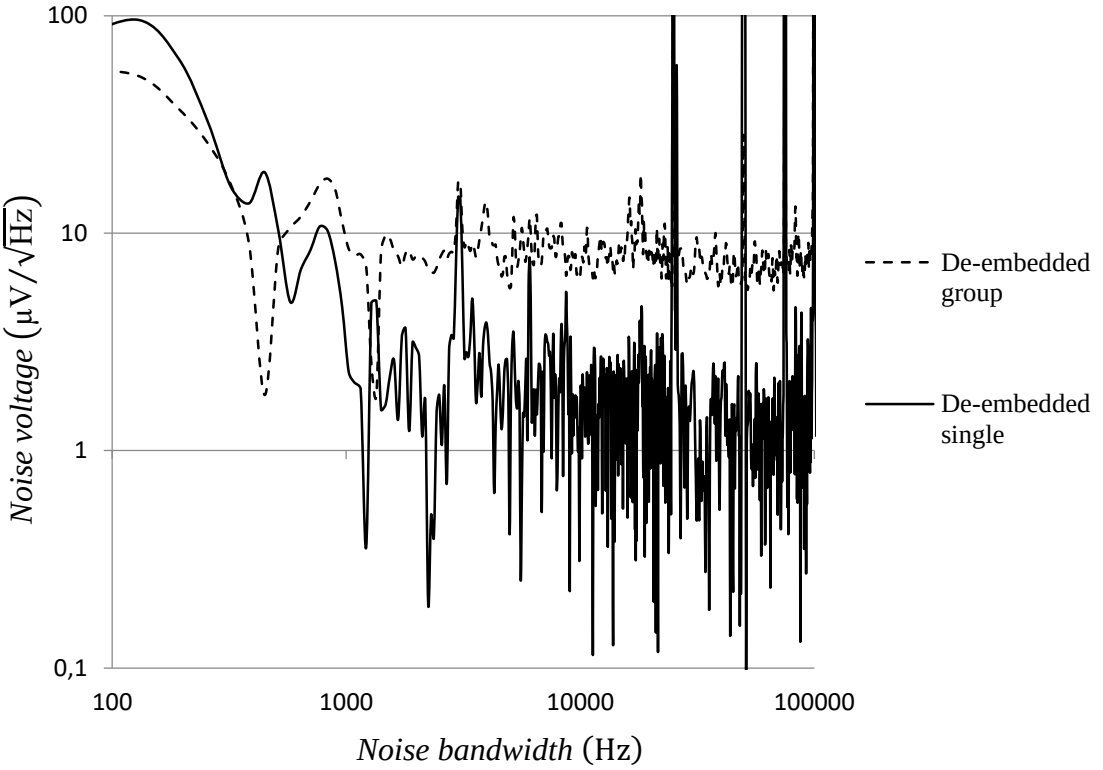


Figure 5.11. Measured noise voltage of the full detector [41].

Figure 5.11 shows the de-embedded noise voltage of the full detector. There are two different detector topologies in the prototype IC used. The first is the multiple-pixel-single-amplifier detector (de-embedded group). The second is the single-pixel-single-amplifier detector (de-embedded single). The multiple-pixel-single-amplifier detector exhibits more noise even though only one pixel is read at a time. This is due to the influence of the peripheral circuitry of the dead pixels when a pixel is read. The single-pixel-single-amplifier is more important

for this research. Figure 5.12 is obtained by superimposing the measured pixel noise voltage of Figure 5.7 onto the total output noise voltage of the single-pixel-single-amplifier detector.

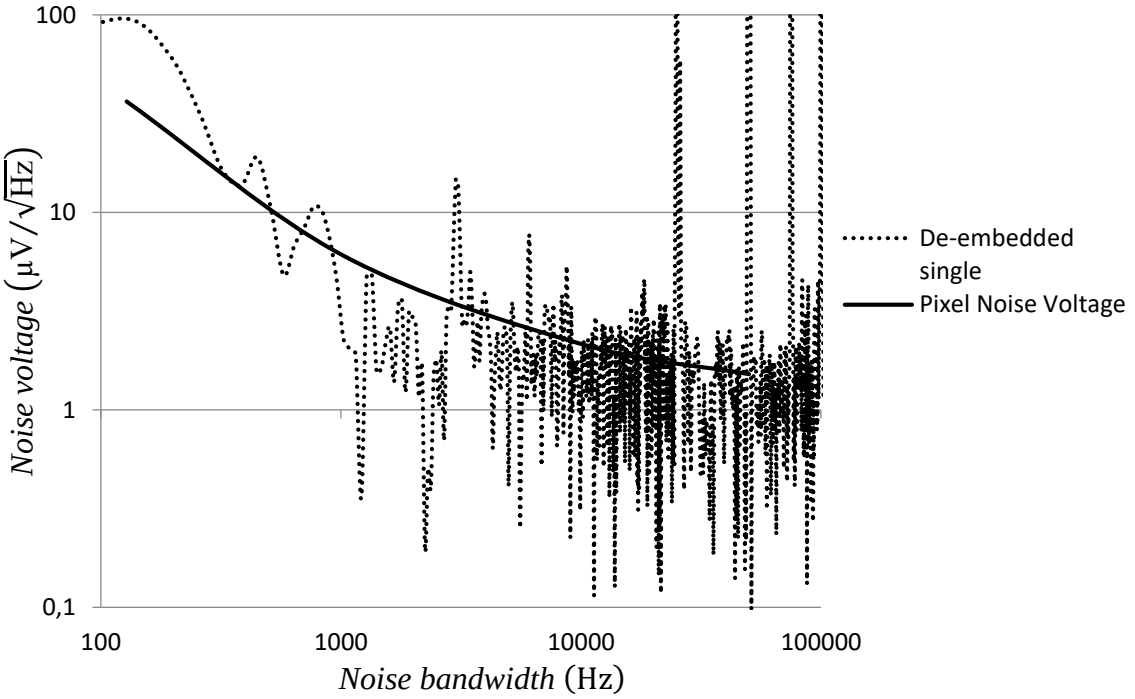


Figure 5.12. Measured noise voltage of the full detector and single diode-connected HBT.

As can be seen in Figure 5.12, the lone-standing diode-connected HBT noise is somewhat reduced at low noise bandwidth and then around 1 kHz is somewhat higher as the noise bandwidth increases. In the full detector, 2 μm × 2 μm reverse-biased diode-connected HBTs were used whereas the size of the lone-standing HBT is 1 μm × 1 μm. To gain an understanding in this, the geometry dependence on base noise current is given [24]:

$$S_{I_B} = \frac{K}{A_E}\frac{I_B^2}{f} = \frac{K}{\beta}\frac{1}{A_E}\frac{I_C^2}{f} \tag{5.4}$$

where A_E is the area of the emitter. Converting (5.4) to a noise voltage, the following is obtained:

$$S_{V_C} = S_{I_B}(R_C\beta)^2 = \frac{K}{\beta}\frac{1}{A_E}\frac{I_C^2}{f}(R_C\beta)^2 \tag{5.5}$$

As can be seen in (5.5), the noise voltage is inversely proportional to the area of the emitter. Since the lone-standing pixel is 4 times smaller than the pixels used in the full detector, the

noise voltage of the pixels of the full detector is much smaller. Taking the causality of the different sub-elements into account and the noise that each sub-element adds independently to the total noise, the total noise in the full detector is somewhat higher. In this case, the noise voltage of the lone-standing HBT is roughly the same as the full detector. Flicker noise, as measured by the K_F factor, scales inversely with the total number of carriers in noise generating elements according to Hooge's theory [24]. This explains the increased noise with the smaller HBTs. This also explains why the noise spectrum flattens when cooled. As the device is cooled, the atoms move closer to each other and movement is restricted.

5.5 COMPARISON OF SIMULATED RESULTS TO MEASURED RESULTS

To compare the simulated results with the measured results, the block diagram of the implemented detector from previous work, completed in 2013 by the author is given as a basis for this discussion.

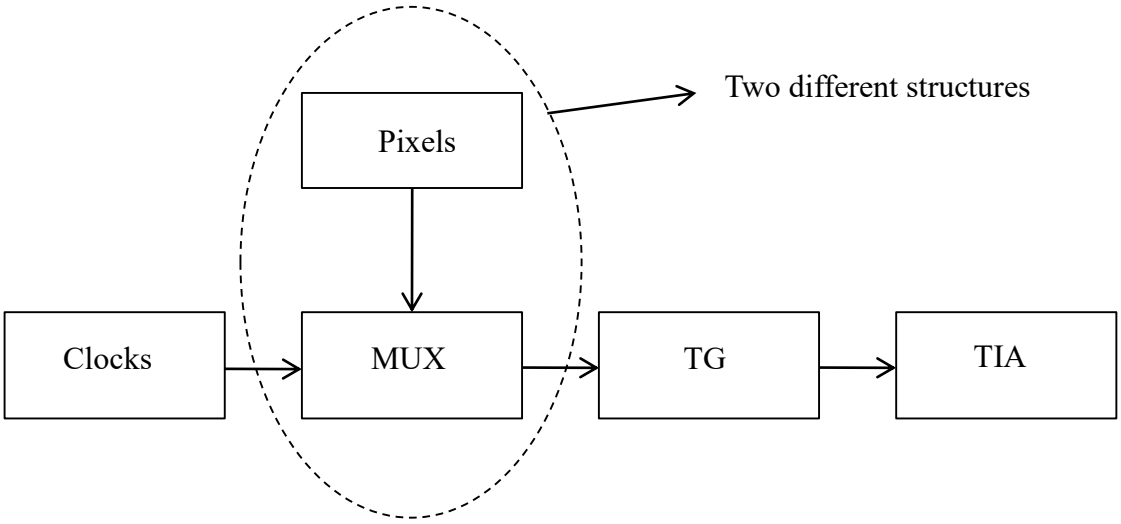


Figure 5.13. Block diagram of the implemented detector [21].

Figure 5.13 depicts the block diagram of the detector. Two different versions of the detector were implemented which are the multiple-pixel-single-amplifier detector and the single-pixel-single-amplifier detector. Both of the implemented detectors are given Figures 5.14 and 5.15.

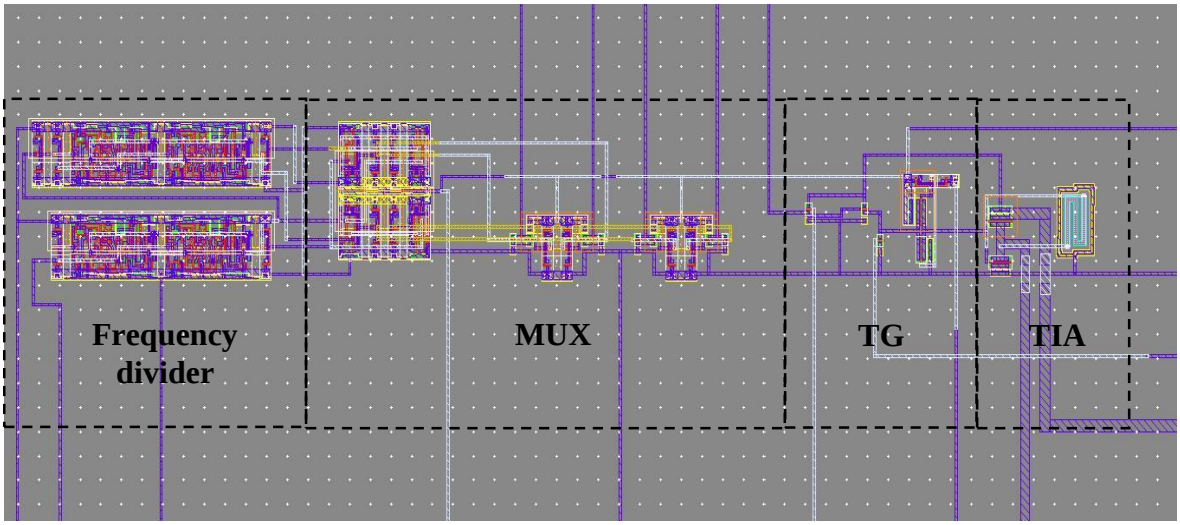


Figure 5.14. Peripheral circuitry of the multiple-pixel-single-amplifier near IR detector.

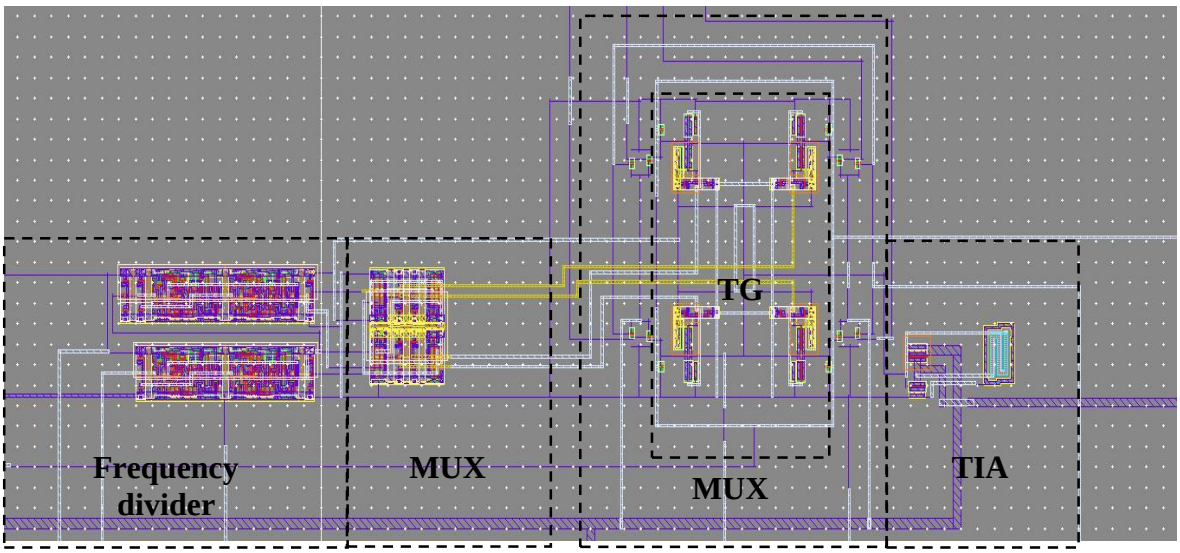


Figure 5.15. Peripheral circuitry of the single-pixel-single-amplifier near IR detector.

As can be seen in Figures 5.14 and 5.15, the peripheral circuitry contains extra sub-systems not incorporated in the mathematical model. First is the clock circuitry which is made up of D flip flop connected in such a way to form a frequency divider. These circuits are default circuits available in the digital library of Cadence Virtuoso which was not focused on in the development of mathematical model. The same applies for the other circuits which are the multiplexer (MUX) and transmission gate (TG). For the research work that this implementation describes, the objective was to develop a gated detector array hence the

reason for the frequency divider. This work focussed on the mathematical model for a single pixel detector where some of the results, such as the noise measurements, are based on this implementation. Simple cascading would not work as one pixel circuit does have an influence on the other circuits.

5.6 CONCLUSION

The measured results of the lone-standing pixel as well as those of the full detector are shown in this chapter.

The J_C versus biasing voltage for both base-emitter shorted HBT and base-collector shorted HBT is given and two observations were made. The first is that the base-collector shorted HBTs J_C is higher than the base-emitter shorted HBT. The second observation is the current flow that occurs at negative bias voltage in the base-collector shorted HBT. This makes a base-collector shorted HBT less suitable than the base-emitter shorted HBT as a reverse-biased diode-connected pixel. For pixels where current flow is not based on applied reverse-bias, modelling is easier since the bias voltage does change as the pixel is illuminated as seen in Figures 4.18 and 4.19. The noise measurements of the pixels with a detailed discussion is provided. The measured time-domain response is given where two main observations were made. The first is that when the clock input is high, the DC level of the output shifts to 0 V which enables better interpretation of the information provided by the detector for subsequent connected systems. The second observation is that the gain is reduced. This is in line with the *y*-parameter model given in (4.35) where the output resistance is reduced when the pixel is illuminated.

CHAPTER 6 CONCLUSION

6. CHAPTER OVERVIEW

This chapter concludes the research conducted and critically evaluates the hypothesis, taking into account the results obtained and a comparison to the simulations as well as the theory.

Chapter 1 introduced the research and documented the research questions used to formulate the research hypothesis. Chapter 2 presented a literature study of the theory needed to understand the research. The first part is a discussion on dependent and independent parameters. This is necessary since a designer who wants a specific SNR will only be able to tune the process independent parameters. These independent parameters are bias voltage, bias current, AR and temperature linked to other applicable parameters in (2.12) to (2.18). Noise theory applicable to this research seen in (2.6) to (2.9) is included in this chapter. The last part presents a discussion of the impact of noise in BiCMOS detectors seen in (2.27) and (2.28). Chapter 3 presents the research methodology used to validate the hypothesis. Chapter 4 presented a detailed discussion of all four applicable process-independent parameters including simulations. A detailed layout of the voltage and current mode model of the 3T pixel structure is presented. This includes *y*-parameter representation seen in (4.14) to (4.35) with simulations. Finally, the noise model applicable to pixels only is presented in (4.36) and (4.37). Chapter 5 documented the measured results by measuring the detector and parts of the detector as illustrated in the experimental setup in Chapter 3. The measured results and simulations are also discussed.

In Section 6.1, the hypothesis was verified for a thorough discussion of the key findings of this research. In Section 6.2 and 6.3, shortcomings and possible future research work are discussed respectively.

6.1 VERIFICATION OF THE HYPOTHESIS

The hypothesis presented in Chapter 1 is repeated here for the reader's convenience:

If the SNR in SiGe BiCMOS near-IR detectors can be related to process-independent parameters, then a mathematical model can be developed which can be used to enhance the performance of these detectors by optimising the output SNR.

The following key findings are used to verify the hypothesis:

- A small-signal model of diode-connected HBTs was developed.
- A DC voltage and current model of the 3T pixel structure was developed.
- A *y*-parameter model of the 3T pixel structure using small-signal models was developed to show the behaviour when a small change is seen at the input pixel.
- The parameters calculated and used in the voltage and current model can be directly inserted in the noise model of the different elements.
- For the pixel, the measured current-temperature results are as follows. At room temperature at 3 V bias, a current of 26 mA and 39.8 mA for the base-emitter shorted and base-collector shorted HBT was measured respectively. This increased to 32 mA and 44 mA respectively at 186 K. This then reduces to 14.75 mA and 16.5 mA respectively at 77 K.
- Carrier freeze-out seen at 186 K has a large effect on the current flow in SiGe material typically not seen in Si based material when cooled down to 77 K.
- The reverse biased base-emitter shorted HBT has almost no current flow whereas the reverse biased base-collector HBT has significant current flow. An average of 0.8 mA was measured.

- The overall noise performance of the base-collector shorted HBT is better than the base-emitter shorted HBT. The key results are given in Table 6.1.

Table 6.1 Critical noise voltage results.

Temperature	**Noise bandwidth**	**Base-emitter shorted HBT noise voltage**	**Base-collector shorted HBT noise voltage**
293 K	102.5 Hz	36.5 $\mu V/\sqrt{Hz}$	12.6 $\mu V/\sqrt{Hz}$
293 K	10 kHz	2.15 $\mu V/\sqrt{Hz}$	4.84 $\mu V/\sqrt{Hz}$
77 K	102.5 Hz	14.5 $\mu V/\sqrt{Hz}$	7.56 $\mu V/\sqrt{Hz}$
77 K	10 kHz	12.2 $\mu V/\sqrt{Hz}$	5.93 $\mu V/\sqrt{Hz}$

- The time-domain measurement of the output voltage shows a decrease in voltage swing and a nominal voltage of 0 V when illuminated. This is in-line with the voltage and current model as well as the *y*-parameter model developed.
- The measured noise voltage of the total detector followed the estimated noise voltage of all the elements added together. When the pixel noise was superimposed over the noise voltage of the total detector, it followed the same trend. This is partly due to the two feedback loops the configuration introduce which reduces noise.
- The high-level design methodology suggested in this work can be used to perform optimisation. The first step is to select an SNR value and then select three of the four process-independent parameters. The remaining process-independent parameter can be determined using a MATLAB™ `math`-function. In this way, a detector can be optimised for maximum SNR (by maximising the voltage signal magnitude or minimising noise voltage) before being sent off to manufacturing, saving design time and enabling designers to develop optimised detectors. Further optimisation is left for future work.

- The model presented in this work does not require a fixed AR for the MOSFETs and can be easily selected. For the HBTs, a different size will still work in this model as no direct relation is made to size of an HBT but the amount of current generated by the pixel was used. There are well-known models that relate collector current flow to HBT size. However, the size does influence the base resistance which will therefore change the I-V curves and noise voltage. The model developed in this research is able to absorb these changes effectively as another feature size's parameters can be used.

Through all of these key findings, the hypothesis was verified. This work will enable researchers to develop detectors by determining the characteristics of detectors with the model introduced in this research.

6.2 SHORTCOMINGS

The ability to change the size of an HBT and the AR of a MOSFET will require multiple IC prototyping cycles, since multiple full detector layouts have to be included. In addition to this, to determine the effects on other topologies, even more prototypes would be required. This comes at a large cost. Only one prototype was implemented, and justifiable results were obtained.

For the I-V curve measurements of the pixel, the ceramic back plate that the IC was attached to, was held above the platform with liquid nitrogen. The forward voltage drop was noted, which corresponded to a temperature with the use of a 2N2222 transistor which was accurately modelled. The I-V curves were measured at discrete points between 293 K and 77 K. A complete degree by degree sweep down to 77 K was not possible with the available equipment. Nonetheless a good number of data points was obtained.

For the noise measurements of the pixel, the measuring time is significantly longer than with the I-V curve measurement. Since for temperatures between 293 K and 77 K the ceramic

back plate has to be held above the platform with liquid nitrogen, a full noise sweep will be difficult to obtain. Therefore, noise measurements were performed at 293 K and 77 K only.

6.3 POSSIBLE FUTURE WORK

Different parts of this work can be used on their own as design blocks and incorporated into EDA software. For instance, the two different configurations of diode-connected HBTs acting as a pixel can be programmed in the EDA software separately. It is also possible to program the *y*-parameter representation as a default configuration (or cell as commonly used in EDA software).

An improved measuring setup can be used to measure additional data points between 293 K and 77 K for specific implementations of detector designs, to overcome shortcomings listed in Section 6.2. This will give a more accurate representation of the I-V curves and noise performance.

A Monte Carlo analysis can be done to determine statistically the accuracy of the model for this prototyping technology used and verified experimentally through the implementation on multiple ICs and multi-project wafers.

Development and measurements in other temperature ranges applicable to environments outside the scope of this work can be done for environments such as space. The robustness of this or other design configurations can be similarly considered. SiGe demonstrates robustness to radiation. The detector, as a whole, can therefore also be evaluated for this and where sophisticated instrumentation is available.

Multiple ICs need to be prototyped with varying ARs and varying sizes of HBTs using other state-of-the-art prototyping technologies. This is to account for velocity saturation effects which were included in this model, yet not measured.

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APPENDIX A SIMULATED AND MEASURED DATA POINTS

A.1 EXCEL SPREADSHEETS USED IN SIMULATIONS

This section provides the method used to obtain the mathematical simulations. An Excel spreadsheet was used and the parameters programmed in. Then the photon generated current was varied and the resulting parameters documented. It is left for future work to generate MATLAB code for this model.

These spreadsheets can be found using the following links
DC simulations: https://tinyurl.com/yx6vjq6l
y-parameter simulations: https://tinyurl.com/ww89duz

A.2 I-V MEASUREMENTS AT ROOM TEMPERATURE AND 77 K

In this section, the data points obtained with the use of the Agilent Technologies B1500A Semiconductor Device Analyser for the base-collector shorted and base-emitter shorted HBT are given. This table, together with the area of the HBT, was used to compile Figures 5.1 and 5.2. The data points given are the bias voltage, series resistance and measured current flow.

Table A2 I-V measured data points.

	Base-collector shorted HBT		**Base-emitter shorted HBT**	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
-3	-1.4543	-1.8053	-0.00164594	-3.52539E-06
-2.98	-1.4406	-1.7885	-0.0016328	-3.49137E-06
-2.96	-1.4267	-1.7714	-0.00161758	-3.40472E-06
-2.94	-1.413	-1.7542	-0.00160482	-3.28716E-06
-2.92	-1.3994	-1.7374	-0.0015896	-3.30291E-06
-2.9	-1.3857	-1.7205	-0.0015759	-3.28305E-06
-2.88	-1.3718	-1.7032	-0.00156114	-2.78062E-06
-2.86	-1.3583	-1.6863	-0.00154812	-1.59883E-06
-2.84	-1.3446	-1.6693	-0.0015331	-3.286E-07
-2.82	-1.3307	-1.6524	-0.00152036	5.0582E-07
-2.8	-1.3172	-1.6354	-0.00150594	3.9266E-07
-2.78	-1.3033	-1.6183	-0.00149362	-5.1502E-07
-2.76	-1.2897	-1.6013	-0.00147856	-1.80228E-06
-2.74	-1.2761	-1.5844	-0.00146562	-2.7677E-06
-2.72	-1.2623	-1.5671	-0.00145112	-3.08612E-06
-2.7	-1.2486	-1.5501	-0.00143834	-2.48234E-06
-2.68	-1.2347	-1.5331	-0.00142418	-1.26326E-06
-2.66	-1.221	-1.5157	-0.00141106	2.116E-07
-2.64	-1.2072	-1.4987	-0.0013971	7.6527E-07
-2.62	-1.1935	-1.4815	-0.00138472	5.2175E-07
-2.6	-1.1797	-1.4641	-0.0013702	-2.0179E-07
-2.58	-1.1662	-1.4471	-0.00135856	-1.62922E-06
-2.56	-1.1523	-1.4298	-0.00134382	-2.58868E-06
-2.54	-1.1385	-1.4123	-0.00133202	-2.79836E-06

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
-2.52	-1.1248	-1.3952	-0.00131788	-2.84566E-06
-2.5	-1.111	-1.3777	-0.00130626	-2.44449E-06
-2.48	-1.0972	-1.3607	-0.00129216	-1.39932E-06
-2.46	-1.0836	-1.3432	-0.00128022	-2.0783E-07
-2.44	-1.0696	-1.3258	-0.00126624	1.3883E-07
-2.42	-1.0559	-1.3085	-0.0012543	8.8704E-07
-2.4	-1.042	-1.2911	-0.0012416	8.8933E-07
-2.38	-1.0283	-1.2738	-0.00122918	-1.1511E-07
-2.36	-1.0147	-1.2563	-0.00121582	-1.42555E-06
-2.34	-1.0008	-1.2387	-0.00120414	-2.42179E-06
-2.32	-0.98706	-1.2213	-0.00119086	-2.04495E-06
-2.3	-0.97333	-1.204	-0.00117898	-2.49648E-06
-2.28	-0.95939	-1.1865	-0.00116566	-2.69336E-06
-2.26	-0.94555	-1.1689	-0.00115392	-2.48547E-06
-2.24	-0.93181	-1.1513	-0.00114022	-1.43619E-06
-2.22	-0.91804	-1.1338	-0.00112894	-1.1922E-07
-2.2	-0.90431	-1.1162	-0.0011163	3.9235E-07
-2.18	-0.89046	-1.0985	-0.00110456	9.9548E-07
-2.16	-0.8768	-1.0811	-0.00109192	4.5397E-07
-2.14	-0.86295	-1.0634	-0.00107988	7.4393E-07
-2.12	-0.8491	-1.0458	-0.00106744	4.8433E-07
-2.1	-0.83541	-1.0281	-0.00105526	8.6672E-07
-2.08	-0.82185	-1.0106	-0.00104346	6.4512E-07
-2.06	-0.80804	-0.99294	-0.00103106	1.00294E-06
-2.04	-0.79427	-0.97523	-0.00102016	8.887E-07

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
-2.02	-0.78063	-0.95769	-0.00100622	4.0382E-07
-2	-0.7669	-0.93997	-0.00099634	8.3254E-07
-1.98	-0.75319	-0.92222	-0.00098364	6.0599E-07
-1.96	-0.73951	-0.90456	-0.00097137	1.05757E-06
-1.94	-0.72597	-0.88707	-0.00096202	7.0317E-07
-1.92	-0.7123	-0.86939	-0.00094797	9.7431E-07
-1.9	-0.69857	-0.85173	-0.00093773	7.2338E-07
-1.88	-0.68505	-0.83413	-0.00092689	6.1036E-07
-1.86	-0.67139	-0.81649	-0.00091294	9.6008E-07
-1.84	-0.6578	-0.79884	-0.00090345	7.1805E-07
-1.82	-0.64422	-0.78113	-0.00089132	9.8478E-07
-1.8	-0.63075	-0.7637	-0.00087933	8.0482E-07
-1.78	-0.61723	-0.74606	-0.00086914	1.06252E-06
-1.76	-0.60372	-0.72841	-0.00085636	8.0157E-07
-1.74	-0.59042	-0.711	-0.00084526	1.28752E-06
-1.72	-0.57687	-0.69334	-0.00083544	1.14092E-06
-1.7	-0.56356	-0.6758	-0.00082235	1.99125E-06
-1.68	-0.55017	-0.65823	-0.00081239	1.51356E-06
-1.66	-0.53694	-0.64092	-0.00080148	1.03416E-06
-1.64	-0.52365	-0.62345	-0.00078876	1.47172E-06
-1.62	-0.51035	-0.60601	-0.00077951	1.00443E-06
-1.6	-0.49733	-0.58871	-0.00076772	1.36122E-06
-1.58	-0.48413	-0.57134	-0.00075576	1.41912E-06
-1.56	-0.47098	-0.55401	-0.00074703	1.54632E-06
-1.54	-0.45801	-0.53684	-0.00073473	1.26684E-06

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
-1.52	-0.44493	-0.51959	-0.00072386	1.56531E-06
-1.5	-0.43197	-0.50245	-0.00071405	1.11804E-06
-1.48	-0.41921	-0.48547	-0.00070142	7.4793E-07
-1.46	-0.40629	-0.46841	-0.00069151	1.08472E-06
-1.44	-0.39352	-0.45145	-0.00068196	1.21529E-06
-1.42	-0.38093	-0.43472	-0.00066934	1.35506E-06
-1.4	-0.36825	-0.41794	-0.00066055	1.21374E-06
-1.38	-0.35579	-0.40134	-0.00064976	1.42713E-06
-1.36	-0.34331	-0.38479	-0.00063788	1.11964E-06
-1.34	-0.33086	-0.36831	-0.00062962	8.7846E-07
-1.32	-0.31863	-0.35206	-0.00061771	1.28041E-06
-1.3	-0.30644	-0.33578	-0.00060732	1.13556E-06
-1.28	-0.2943	-0.31965	-0.00059795	1.46745E-06
-1.26	-0.28235	-0.30382	-0.00058601	9.0388E-07
-1.24	-0.27043	-0.28801	-0.00057682	1.13653E-06
-1.22	-0.25871	-0.27252	-0.00056713	9.5941E-07
-1.2	-0.24703	-0.25706	-0.00055442	1.52208E-06
-1.18	-0.23545	-0.24179	-0.00054632	1.14368E-06
-1.16	-0.22421	-0.22691	-0.00053587	8.312E-07
-1.14	-0.2129	-0.21213	-0.00052463	1.20499E-06
-1.12	-0.20176	-0.19753	-0.00051647	1.08717E-06
-1.1	-0.19082	-0.18337	-0.00050467	1.46458E-06
-1.08	-0.18003	-0.16934	-0.00049489	1.27772E-06
-1.06	-0.16954	-0.15577	-0.00048628	1.47257E-06
-1.04	-0.15907	-0.14241	-0.0004741	1.1292E-07

	Base-collector shorted HBT		**Base-emitter shorted HBT**	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
-1.02	-0.14884	-0.12939	-0.00046552	-1.24074E-06
-1	-0.1389	-0.1169	-0.00045656	-1.65503E-06
-0.98	-0.12906	-0.10465	-0.00044457	-1.82859E-06
-0.96	-0.11952	-0.092948	-0.00043616	-1.46775E-06
-0.94	-0.11025	-0.081808	-0.00042684	-1.8692E-06
-0.92	-0.10117	-0.070984	-0.00041546	-1.83064E-06
-0.9	-0.09249	-0.060856	-0.00040765	-1.27461E-06
-0.88	-0.08398	-0.051201	-0.00039716	1.2273E-07
-0.86	-0.07578	-0.042151	-0.00038692	1.28932E-06
-0.84	-0.068	-0.033915	-0.00037922	9.9398E-07
-0.82	-0.06049	-0.026328	-0.0003677	1.47209E-06
-0.8	-0.05339	-0.019581	-0.00035879	8.9581E-07
-0.78	-0.04672	-0.013882	-0.00035028	1.32399E-06
-0.76	-0.0404	-0.009171	-0.00033916	9.9537E-07
-0.74	-0.03453	-0.0056599	-0.00033047	1.68456E-06
-0.72	-0.02916	-0.00323852	-0.00032242	1.30896E-06
-0.7	-0.02422	-0.00170928	-0.00031089	1.96854E-06
-0.68	-0.01977	-0.00083392	-0.00030303	1.76353E-06
-0.66	-0.01587	-0.00034638	-0.00029377	1.85992E-06
-0.64	-0.01243	-0.00011277	-0.00028312	1.54061E-06
-0.62	-0.00955	-2.96333E-05	-0.00027567	2.23924E-06
-0.6	-0.00715	-7.0078E-06	-0.00026575	1.74411E-06
-0.58	-0.00519	-3.57926E-06	-0.00025561	1.09464E-06
-0.56	-0.00365	-2.47368E-06	-0.00024828	1.37733E-06
-0.54	-0.0025	-1.0366E-06	-0.00023788	1.06019E-06

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
-0.52	-0.00167	7.1551E-07	-0.00022872	1.37992E-06
-0.5	-0.00109	2.14268E-06	-0.00022084	1.19247E-06
-0.48	-0.0007	1.76508E-06	-0.00020997	8.4765E-07
-0.46	-0.00044	2.12778E-06	-0.00020216	1.24807E-06
-0.44	-0.00028	1.70573E-06	-0.00019363	1.97905E-06
-0.42	-0.00018	2.08292E-06	-0.00018298	1.36398E-06
-0.4	-0.00012	1.6779E-06	-0.00017599	0.000001385
-0.38	-8.4E-05	2.06959E-06	-0.00016624	1.91729E-06
-0.36	-6.5E-05	1.64259E-06	-0.00015681	1.39812E-06
-0.34	-5.4E-05	2.03683E-06	-0.00014962	1.65402E-06
-0.32	-4.8E-05	1.60096E-06	-0.00013907	1.3915E-06
-0.3	-4.3E-05	2.00207E-06	-0.0001313	1.67657E-06
-0.28	-3.8E-05	1.53009E-06	-0.00012323	1.22386E-06
-0.26	-3.4E-05	1.94114E-06	-0.0001126	1.7329E-06
-0.24	-3E-05	2.25975E-06	-0.00010573	1.47914E-06
-0.22	-2.6E-05	1.85469E-06	-9.64271E-05	1.14241E-06
-0.2	-2.2E-05	2.17599E-06	-8.79179E-05	1.34913E-06
-0.18	-1.8E-05	1.79032E-06	-7.93302E-05	1.44629E-06
-0.16	-1.4E-05	2.12939E-06	-7.04088E-05	1.63292E-06
-0.14	-9.5E-06	1.69262E-06	-0.000062059	1.20862E-06
-0.12	-7E-06	2.05345E-06	-5.31468E-05	7.4855E-07
-0.1	-3.3E-06	1.58549E-06	-4.48885E-05	1.97486E-06
-0.08	6.69E-07	1.96872E-06	-3.57676E-05	2.26583E-06
-0.06	4.74E-06	2.2717E-06	-2.74045E-05	1.56929E-06
-0.04	9.34E-06	1.90627E-06	-1.81655E-05	1.19555E-06

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
-0.02	1.63E-05	2.22446E-06	-9.3287E-06	1.5718E-06
0	2.46E-05	1.69456E-06	-1.5132E-07	1.12757E-06
0.02	3.48E-05	2.05278E-06	8.97227E-06	1.45146E-06
0.04	4.8E-05	1.62207E-06	0.000019304	1.12269E-06
0.06	6.5E-05	2.02264E-06	2.99809E-05	2.10629E-06
0.08	8.76E-05	1.55463E-06	4.07547E-05	1.52582E-06
0.1	0.000116	0.000001949	5.26311E-05	1.61192E-06
0.12	0.000158	2.26689E-06	0.000065228	1.35655E-06
0.14	0.000209	1.90005E-06	7.90466E-05	1.67633E-06
0.16	0.000272	2.22853E-06	9.40756E-05	1.36814E-06
0.18	0.000355	1.85648E-06	0.000110347	1.09052E-06
0.2	0.000451	2.25194E-06	0.00012774	1.47335E-06
0.22	0.000569	1.90659E-06	0.00015081	1.38512E-06
0.24	0.000709	2.3966E-06	0.00017534	1.85141E-06
0.26	0.00087	2.21697E-06	0.00020748	1.31424E-06
0.28	0.001062	2.97772E-06	0.00025676	1.68355E-06
0.3	0.001262	4.06689E-06	0.0003292	1.3662E-06
0.32	0.001509	5.05818E-06	0.00045824	1.57896E-06
0.34	0.001789	6.45239E-06	0.00068675	1.36626E-06
0.36	0.002097	7.35992E-06	0.00108175	1.13787E-06
0.38	0.002453	0.000008628	0.00176284	1.66583E-06
0.4	0.002848	1.43172E-05	0.00286346	1.63197E-06
0.42	0.003298	1.82791E-05	0.00450956	1.51631E-06
0.44	0.003807	2.73925E-05	0.00687344	1.3413E-06
0.46	0.004384	3.54892E-05	0.00999394	2.61376E-06

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
0.48	0.005044	4.85135E-05	0.014029	8.7421E-06
0.5	0.005801	6.23215E-05	0.018975	5.39036E-05
0.52	0.006649	8.11414E-05	0.02482	0.00024678
0.54	0.007635	0.000104214	0.031581	0.00086371
0.56	0.008723	0.00013504	0.03917	0.0022304
0.58	0.009969	0.00016491	0.047732	0.00494656
0.6	0.011381	0.00021426	0.05718	0.0093843
0.62	0.012985	0.0002951	0.067401	0.015464
0.64	0.014812	0.00040254	0.078631	0.02317
0.66	0.016922	0.00058203	0.090721	0.032143
0.68	0.019417	0.00083603	0.104041	0.042467
0.7	0.0224	0.00118662	0.11877	0.053878
0.72	0.026045	0.0016571	0.13494	0.06616
0.74	0.030701	0.00223888	0.1532	0.079556
0.76	0.036684	0.0029367	0.17364	0.093701
0.78	0.044636	0.00373508	0.19698	0.108802
0.8	0.05504	0.0046459	0.22303	0.12472
0.82	0.068351	0.005641	0.25164	0.1413
0.84	0.085106	0.00674924	0.28312	0.15876
0.86	0.105369	0.00795456	0.31715	0.17694
0.88	0.12877	0.00927434	0.35321	0.1956
0.9	0.1557	0.01070846	0.39183	0.21514
0.92	0.18603	0.012271	0.43276	0.2353
0.94	0.2197	0.013953	0.47602	0.25611
0.96	0.25673	0.01578	0.52129	0.27738

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
0.98	0.29807	0.017834	0.56979	0.2995
1	0.34382	0.020182	0.62117	0.32245
1.02	0.3941	0.02292	0.6752	0.34595
1.04	0.45051	0.026439	0.73337	0.37097
1.06	0.51351	0.031701	0.79557	0.39809
1.08	0.58336	0.041174	0.86162	0.42918
1.1	0.66312	0.056819	0.93358	0.46494
1.12	0.75426	0.077816	1.01156	0.50437
1.14	0.85823	0.102769	1.09591	0.54661
1.16	0.97933	0.13193	1.1898	0.59249
1.18	1.11808	0.16501	1.2928	0.6416
1.2	1.274	0.20195	1.4055	0.69394
1.22	1.4499	0.24354	1.5296	0.75071
1.24	1.6435	0.28926	1.6644	0.81135
1.26	1.8525	0.33837	1.8082	0.87507
1.28	2.0789	0.39135	1.9631	0.94232
1.3	2.3205	0.44757	2.1278	1.01251
1.32	2.5737	0.50601	2.2993	1.08448
1.34	2.8418	0.56783	2.481	1.1596
1.36	3.1228	0.63233	2.6704	1.2369
1.38	3.4145	0.69935	2.8672	1.3165
1.4	3.7143	0.76813	3.0687	1.3974
1.42	4.0262	0.8399	3.2783	1.481
1.44	4.3482	0.91413	3.4937	1.5667
1.46	4.6757	0.98997	3.7125	1.6538

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
1.48	5.0146	1.06886	3.9386	1.7438
1.5	5.3622	1.15002	4.1691	1.8356
1.52	5.7133	1.233	4.4021	1.9288
1.54	6.0749	1.3191	4.6412	2.0252
1.56	6.444	1.4076	4.8848	2.1236
1.58	6.8155	1.4975	5.1295	2.2231
1.6	7.1969	1.5909	5.3795	2.3257
1.62	7.5839	1.6867	5.6331	2.4304
1.64	7.9734	1.784	5.8876	2.5365
1.66	8.3714	1.8852	6.1474	2.6455
1.68	8.7708	1.9877	6.4072	2.7556
1.7	9.1794	2.094	6.6724	2.869
1.72	9.5929	2.203	6.9395	2.9845
1.74	10.0069	2.3133	7.2074	3.101
1.76	10.4293	2.4279	7.4802	3.2209
1.78	10.8512	2.5439	7.7517	3.3416
1.8	11.282	2.6639	8.0288	3.4656
1.82	11.719	2.7868	8.3073	3.5916
1.84	12.151	2.9114	8.5853	3.7189
1.86	12.594	3.0403	8.868	3.8491
1.88	13.038	3.1722	9.152	3.9815
1.9	13.482	3.306	9.4354	4.115
1.92	13.933	3.444	9.7229	4.2517
1.94	14.383	3.5839	10.0097	4.3893
1.96	14.838	3.7285	10.2999	4.5302

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
1.98	15.298	3.8759	10.5927	4.6733
2	15.756	4.0253	10.8839	4.8171
2.02	16.22	4.1792	11.1791	4.9645
2.04	16.684	4.3355	11.4733	5.1125
2.06	17.152	4.4964	11.775	5.2643
2.08	17.625	4.6606	12.074	5.4179
2.1	18.094	4.8274	12.373	5.5724
2.12	18.569	4.9984	12.674	5.7306
2.14	19.047	5.1735	12.978	5.8907
2.16	19.522	5.3505	13.279	6.0517
2.18	20.003	5.5326	13.586	6.2161
2.2	20.481	5.7164	13.889	6.3808
2.22	20.964	5.9061	14.196	6.5497
2.24	21.452	6.0996	14.505	6.7203
2.26	21.935	6.2947	14.812	6.8914
2.28	22.423	6.495	15.123	7.0667
2.3	22.906	6.6973	15.431	7.2422
2.32	23.399	6.9051	15.744	7.4213
2.34	23.892	7.1177	16.057	7.603
2.36	24.38	7.3307	16.369	7.7846
2.38	24.874	7.5492	16.684	7.9701
2.4	25.368	7.7728	17	8.1574
2.42	25.86	7.9972	17.313	8.3456
2.44	26.357	8.2283	17.631	8.5373
2.46	26.854	8.4622	17.949	8.7314

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
2.48	27.346	8.6981	18.265	8.926
2.5	27.844	8.9391	18.585	9.1247
2.52	28.343	9.1848	18.905	9.3253
2.54	28.84	9.4349	19.226	9.5289
2.56	29.336	9.6854	19.545	9.7312
2.58	29.834	9.9424	19.867	9.9381
2.6	30.332	10.2042	20.188	10.1473
2.62	30.826	10.4657	20.508	10.3563
2.64	31.325	10.7337	20.832	10.5694
2.66	31.825	11.0061	21.156	10.7845
2.68	32.319	11.2783	21.477	10.9999
2.7	32.817	11.565	21.803	11.2186
2.72	33.317	11.847	22.128	11.4405
2.74	33.809	12.13	22.451	11.667
2.76	34.307	12.421	22.778	11.891
2.78	34.805	12.715	23.104	12.119
2.8	35.297	13.011	23.426	12.346
2.82	35.791	13.311	23.754	12.578
2.84	36.29	13.616	24.081	12.812
2.86	36.781	13.927	24.409	13.048
2.88	37.27	14.238	24.735	13.282
2.9	37.764	14.555	25.062	13.523
2.92	38.257	14.878	25.392	13.765
2.94	38.745	15.199	25.717	14.005
2.96	39.237	15.529	26.045	14.253

	Base-collector shorted HBT		Base-emitter shorted HBT	
Bias Voltage (V)	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**	**Current flow (mA) at room temperature**	**Current flow (mA) at 77 K**
2.98	39.726	15.862	26.373	14.501
3	40.209	16.195	26.699	14.75

A.3 C-V MEASUREMENTS AT ROOM TEMPERATURE AND 77 K

The base-emitter shorted and base-collector shorted HBT C-V measured data points are given in this section. This can be used to understand the behaviour of the diode-connected HBT. This was measured simultaneously with the I-V measurements presented in Section A.1 at three different oscillation frequencies.

Table A3.1 C-V measured data points base-collector shorted HBT at room temperature.

Base-collector shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-4	2.74896	1.83992	2.71696
-3.881	2.77943	-0.879262	2.71811
-3.761	2.73918	5.66701	2.72986
-3.642	2.78142	-0.18049	2.71276
-3.522	2.73559	6.67799	2.72085
-3.403	2.73233	2.70748	2.71367
-3.284	2.76594	-1.15967	2.72802
-3.164	2.73653	0.583638	2.70936
-3.045	2.76961	-1.74216	2.7215
-2.925	2.76297	2.78592	2.70658

Base-collector shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-2.806	2.75355	2.72294	2.71217
-2.687	2.74011	2.72797	2.71004
-2.567	2.78217	2.73293	2.72632
-2.448	2.74891	2.73346	2.70977
-2.328	2.74449	2.73052	2.72654
-2.209	2.75543	2.73189	2.71402
-2.09	2.7513	2.73555	2.72769
-1.97	2.76876	2.73707	2.7813
-1.851	2.75849	2.73317	2.70834
-1.731	2.75894	2.72782	2.71782
-1.612	2.766	2.73083	2.71612
-1.493	2.74671	2.7308	2.70783
-1.373	2.7601	2.73668	2.67193
-1.254	2.76219	2.7354	2.71983
-1.134	2.76134	2.73181	2.72906
-1.015	2.75044	2.73292	2.64858
-0.896	2.7591	2.7381	2.71493
-0.776	2.75636	2.73431	2.71432
-0.657	2.75718	2.73496	2.70718
-0.537	2.76402	2.73443	2.70884
-0.418	2.76299	2.7367	2.71329
-0.299	2.75463	2.73942	2.70571
-0.179	2.761	2.73735	2.71551
-0.06	2.76919	2.73356	2.71981

Base-collector shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
0.06	2.7716	2.73305	2.72194
0.179	2.99327	2.68276	2.71872
0.299	3.32653	1.21474	2.81692
0.418	20.2525	-1.42191	2.64431
0.537	16.763	1.29215	1.64417
0.657	48.967	-6.84888	-0.385271
0.776	33.3054	-27.4452	-13.3889
0.896	-98.5318	-160.67	-67.9368
1.015	-753.349	-778.962	-257.306
1.134	-3047.93	-2766.87	-771.914
1.254	-7504.96	-6707.91	-1668.81
1.373	-11638.4	-10530.4	-2471.46
1.493	-13833.5	-12497.9	-2968.92
1.612	-14727.4	-13270.5	-3260.64
1.731	-15021.7	-13548.4	-3457.42
1.851	-15062.5	-13603.5	-3595.18
1.97	-15009.3	-13553.2	-3698.42
2.09	-14764.6	-13468.8	-3778.04
2.209	-14553	-13355.9	-3839.14
2.328	-14252.3	-13222.1	-3887.61
2.448	-13901.3	-13077.9	-3924.04
2.567	-13506.7	-12907.2	-3951.64
2.687	-13027.6	-12745.9	-3969.38
2.806	-12631.1	-12557.1	-3980.58

Base-collector shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
2.925	-12135	-12364.5	-3982.57
3.045	-11490.8	-12129.3	-3979.72

From a biasing voltage of 3.164 V and up, no data points were obtained. Data points were obtained for the 77 K measurements, however. This is left for future studies as an extension to this work.

Table A3.2 C-V measured data points base-collector shorted HBT at 77 K.

Base-collector shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-4	33.5113	1.3391	0.731609
-3.881	43.8715	-1.06733	0.770863
-3.761	52.5401	-0.51736	0.786138
-3.642	-2.58923	-1.34218	0.725984
-3.522	51.579	-1.61642	0.79276
-3.403	15.888	-2.90801	0.878288
-3.284	-3.95354	-3.74523	0.757321
-3.164	14.271	-1.70807	1.09245
-3.045	1.70395	-1.68296	1.04078
-2.925	1.35557	-1.93543	1.23608
-2.806	-8.31893	-2.0907	1.26612
-2.687	-5.98387	-1.97512	1.33294

Base-collector shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-2.567	8.39516	0.071917	1.29047
-2.448	-28.1242	-2.3416	1.55553
-2.328	-12.8343	-3.84094	1.60908
-2.209	-21.5627	-1.78642	1.66011
-2.09	-9.04197	-1.68967	1.85323
-1.97	1.34618	0.198499	1.74838
-1.851	-8.37977	-0.0372534	1.86505
-1.731	6.97858	-0.344256	1.98244
-1.612	10.0474	1.28605	2.11242
-1.493	9.12391	1.08804	2.36583
-1.373	9.63879	2.19638	2.46423
-1.254	7.19084	1.43006	2.58724
-1.134	4.62967	2.16068	2.57844
-1.015	5.19285	1.90437	2.71706
-0.896	-0.151735	2.68858	2.74637
-0.776	3.72208	2.49845	2.71778
-0.657	5.49947	3.00974	2.78712
-0.537	5.87969	3.41577	2.84446
-0.418	4.14699	3.30072	2.80372
-0.299	5.91202	2.94356	2.73501
-0.179	1.08814	2.6648	2.64932
-0.06	5.73576	2.44926	2.6769
0.06	5.90056	2.47199	2.70558
0.179	4.92874	3.01247	2.69083

Base-collector shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
0.299	7.72371	3.07012	2.70633
0.418	12.799	2.96011	2.74952
0.537	31.5566	-3.50778	2.74224
0.657	19.6944	1.74207	0.486474
0.776	49.6917	-0.575707	-1.67442
0.896	79.7578	-1.80228	-4.00582
1.015	113.762	-13.5103	-8.08478
1.134	35.8006	-45.8654	-31.9919
1.254	-70.8492	-135.907	-106.562
1.373	-173.191	-264.459	-207.661
1.493	-305.288	-401.303	-306.217
1.612	-474.876	-538.141	-406.464
1.731	-648.445	-688.459	-514.641
1.851	-840.87	-851.872	-633.327
1.97	-1039.04	-1029.26	-765.283
2.09	-1295.99	-1242.24	-914.649
2.209	-1568.68	-1470.33	-1076.05
2.328	-1845.32	-1727.98	-1253.62
2.448	-2191.31	-2008.82	-1443.07
2.567	-2515.01	-2304.32	-1640.01
2.687	-2853.17	-2624.22	-1846.46
2.806	-3192.93	-2953.77	-2055.21
2.925	-3547.66	-3288.8	-2268.96
3.045	-3904.88	-3649.51	-2484.12

Base-collector shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
3.164	-4204.44	-4010.58	-2702.61
3.284	-4620.64	-4398.97	-2922.73
3.403	-4966.22	-4787.79	-3141.99
3.522	-5297.51	-5202.07	-3365.91
3.642	-5735.68	-5624.57	-3591.71
3.761	-6089.59	-6072.3	-3820.43
3.881	-6541.92	-6536.64	-4051.85
4	-6898.16	-6990.62	-4281.24

In Tables A2.3 and A2.4, the C-V measurements of the base-emitter shorted HBT are given for room temperature and 77 K.

Table A3.3 C-V measured data points base-emitter shorted HBT at room temperature.

Base-emitter shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-4	1.98713	1.75251	1.76917
-3.881	1.65677	1.73642	1.75295
-3.761	1.52413	1.77075	1.75528
-3.642	1.57676	1.7432	1.75893
-3.522	1.74238	1.7595	1.75673
-3.403	1.74745	1.73687	1.75723
-3.284	1.79983	1.75197	1.76298

Base-emitter shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-3.164	1.77961	1.653	1.75491
-3.045	1.74379	1.72372	1.77333
-2.925	1.7732	1.74918	1.76152
-2.806	1.76467	1.74965	1.74512
-2.687	1.80524	1.76264	1.74376
-2.567	1.7865	1.76644	1.76124
-2.448	1.68808	1.76519	1.77204
-2.328	1.77636	1.75974	1.77756
-2.209	1.72599	1.75741	1.78853
-2.09	1.73216	1.75847	1.78208
-1.97	1.77153	1.76801	1.76516
-1.851	1.73672	1.75927	1.76484
-1.731	1.73464	1.75845	1.76503
-1.612	1.75947	1.76099	1.76455
-1.493	1.78143	1.76651	1.76293
-1.373	1.738	1.76979	1.76912
-1.254	1.77211	1.76585	1.77224
-1.134	1.75622	1.76002	1.75762
-1.015	1.7718	1.76029	1.76707
-0.896	1.74755	1.7694	1.76634
-0.776	1.77417	1.76677	1.75975
-0.657	1.76418	1.76365	1.75667
-0.537	1.77234	1.76601	1.76698
-0.418	1.75723	1.75778	1.7451

Base-emitter shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-0.299	1.78763	1.77282	1.7631
-0.179	1.76707	1.76962	1.77482
-0.06	1.7821	1.76519	1.76939
0.06	1.78482	1.76123	1.7619
0.179	1.9992	1.71056	1.78889
0.299	2.30514	0.290547	1.85016
0.418	18.9189	2.07388	2.05693
0.537	16.1728	-0.469054	0.691567
0.657	47.8606	-8.09929	-1.20219
0.776	45.1375	-20.2109	-9.85723
0.896	-37.3173	-107.042	-48.0143
1.015	-461.986	-551.682	-188.526
1.134	-2011.75	-1888.58	-562.861
1.254	-4871.81	-4409.58	-1182.29
1.373	-7206.4	-6636.22	-1696.68
1.493	-8140.69	-7594.05	-1956.14
1.612	-8295.08	-7782.74	-2062.79
1.731	-8186.21	-7719.61	-2109.06
1.851	-7972.66	-7587.75	-2129.78
1.97	-7674.54	-7439.03	-2139.25
2.09	-7381.01	-7303.87	-2144.42
2.209	-7083.08	-7177.59	-2147.36
2.328	-6744.69	-7052.65	-2150.81
2.448	-6394.55	-6938.18	-2152.17

Base-emitter shorted HBT			
Capacitance (pF) at room temperature			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
2.567	-6033.17	-6818.25	-2153.4
2.687	-5586.25	-6687.88	-2150.87
2.806	-5147.43	-6548.27	-2147.75
2.925	-4648.44	-6388.12	-2142.14
3.045	-4120.6	-6222.3	-2131.56
3.164	-3475.1	-6038.65	-2119.52
3.284	-2879.61	-5842.17	-2104.06
3.403	-2160.19	-5631.95	-2085.95

Table A3.4 C-V measured data points base-emitter shorted HBT at 77 K.

Base-emitter shorted HBT			
Capacitance (pF) at 77 K			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-4	-1035.15	-103.68	-23.7996
-3.881	-511.49	-55.0149	-14.2307
-3.761	-271.745	-40.978	-9.71472
-3.642	-166.366	-24.4048	-7.14228
-3.522	-105.923	-17.1062	-5.00578
-3.403	-45.434	-12.9669	-3.85782
-3.284	-33.8185	-12.2712	-2.86154
-3.164	-46.9646	-9.97659	-1.95982
-3.045	-33.8027	-8.50557	-1.48029

Base-emitter shorted HBT			
Capacitance (pF) at 77 K			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-2.925	-12.8572	-7.00993	-0.934547
-2.806	-33.1692	-6.68683	-0.423428
-2.687	-18.0561	-4.12338	0.0264907
-2.567	-17.7418	-3.91183	0.377686
-2.448	-4.59976	-1.7587	0.605526
-2.328	0.529769	-1.82303	0.921103
-2.209	-17.9611	-0.753989	1.12442
-2.09	0.583784	-0.235615	1.22772
-1.97	-1.75804	-0.617298	1.41619
-1.851	0.179123	1.35384	1.61071
-1.731	11.164	0.937362	1.62372
-1.612	15.0836	0.838193	1.82073
-1.493	13.2224	0.816423	1.90833
-1.373	5.16974	1.50661	1.9367
-1.254	6.18269	0.92904	2.0409
-1.134	7.46653	2.52107	2.09404
-1.015	10.0887	1.62068	2.19668
-0.896	4.63917	1.92452	2.26722
-0.776	6.81319	2.36949	2.36331
-0.657	7.87223	1.35866	2.42969
-0.537	7.71187	2.58839	2.46131
-0.418	10.2808	2.86344	2.43928
-0.299	9.06303	2.8439	2.40228
-0.179	4.83715	2.51576	2.39569

Base-emitter shorted HBT			
Capacitance (pF) at 77 K			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
-0.06	5.14632	2.20317	2.34063
0.06	7.33159	2.40586	2.39767
0.179	2.78357	2.58662	2.3874
0.299	1.93954	2.4854	2.37585
0.418	4.78004	2.13053	2.37618
0.537	25.2752	-3.70952	2.33447
0.657	20.7686	1.32659	0.738167
0.776	60.1511	1.38628	-0.918615
0.896	71.7026	-4.22386	-3.01632
1.015	56.1938	-24.7755	-8.60675
1.134	6.15308	-51.2836	-30.8978
1.254	-16.985	-117.794	-93.3725
1.373	-66.1968	-216.545	-173.994
1.493	-151.013	-318.74	-248.629
1.612	-239.822	-399.434	-313.045
1.731	-308.233	-474.122	-370.415
1.851	-388.396	-543.261	-425.082
1.97	-459.024	-612.57	-479.228
2.09	-559.438	-680.58	-535.95
2.209	-643.661	-758.641	-593.265
2.328	-742.948	-834.173	-654.028
2.448	-840.147	-912.93	-716.719
2.567	-966.144	-995.792	-782.174
2.687	-1079.51	-1083.23	-851.583

Base-emitter shorted HBT			
Capacitance (pF) at 77 K			
Bias Voltage (V)	**Oscillation Frequency 1 kHz**	**Oscillation Frequency 10 kHz**	**Oscillation Frequency 100 kHz**
2.806	-1210.49	-1174.31	-922.666
2.925	-1347.8	-1273.02	-996.934
3.045	-1512.29	-1372.3	-1073.95
3.164	-1648.06	-1475.39	-1154.17
3.284	-1775.66	-1587.95	-1237.71
3.403	-1989.33	-1693.95	-1323.61
3.522	-2073.21	-1816.41	-1413.04
3.642	-2256.81	-1942.24	-1505.24
3.761	-2462.6	-2074.73	-1602.08
3.881	-2595.94	-2214.55	-1702.56
4	-2823.03	-2360.75	-1806.02