A Capacitive SIW Discontinuity for Impedance Matching

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***Abstract*—We present a shunt capacitive SIW discontinuity for the first time. The discontinuity is parametrically characterised in terms of its reactive impedance and an equivalent circuit model is presented and validated. C-band prototypes are manufactured and measured, confirming simulated results. The utility of the discontinuity is then demonstrated as part of a matching network for an S-band amplifier. A simple synthesis method for the matching networks is presented, which requires minimal numerical optimisation. The amplifier is prototyped and measured, and found to be in good agreement with simulation.**

***Index Terms*—Substrate-Integrated Waveguide, Impedance Matching, Radiofrequency Amplifiers, Circuit Models, S-band, C-band**

I. Introduction

SUBSTRATE-INTEGRATED waveguide (SIW) is an actively-researched transmission medium which combines the advantages of high-performance, high-cost rectangular waveguide and economical planar circuits [1]. SIW has been implemented primarily in the design of passive circuits, such as filters [2]. However, to enable full-system integration in SIW, it has also been used as an integration medium in active circuits such as phase shifters [3], switches [4], isolators [5] and amplifiers.

The first example in literature of an SIW-integrated amplifier is presented at X-band in [6], and demonstrates that impedance matching in SIW is possible using inductive iris-type discontinuities formed by plated through-hole vias. In [7], a power amplifier is designed at S-band using similar inductive discontinuities in SIW (with vias placed either individually or in pairs), and a thorough analysis of the effect of via positioning on the impedance of the network confirmed an electrical response similar to that of a shunt inductor at the centre frequency, as is the case with an inductive post in rectangular waveguide [8].

Subsequently, full-mode [9], [10] and half-mode SIW, with and without inductive posts [11], [12] have been used for matching and harmonic suppression networks in power amplifiers. Corrugated half-mode SIW has also been proposed as an integration medium for distributed amplifiers [13], [14] as it features a floating top conductor, which simplifies DC biasing of the active device. More commonly, SIW is used as a medium for integrating MMIC amplifiers [15], [16], with no specific regard to reactive impedance matching inside the medium.

Several other discontinuities in rectangular waveguide have, however, been shown to act as reactive circuit elements, including the shunt capacitive window [8]. While it has been shown that a longitudinal row of blind vias may be augmented by an embedded copper strip [17] to attain additional capacitance, and that a discrete step in SIW height may be modelled as a shunt capacitive discontinuity [18], [19], the longitudinally-short transversal blind via ridge has never been analysed as a capacitive window in isolation.

In this work, we characterize the capacitive iris discontinuity in SIW (implemented in multi-layer PCB) for the first time (shown in Section II), drawing particular attention to manufacturing processes and shortcomings. The discontinuity is then applied as a matching section for an S-band amplifier (Section III), followed by concluding remarks in Section IV.

In all cases, EM simulations were conducted with CST Microwave Studio 2018 using the Frequency Domain solver, and circuit simulations in NI AWR Microwave Office. The laminate material under consideration is Mercurywave 9350 throughout, with ϵ_r = 3.4 and tanδ = 0.004 at 2.5 GHz.

II. A Capacitive SIW Discontinuity

This section presents the capacitive discontinuity in multi-layer SIW, derive equivalent circuit model values based on the model presented in [8], and verify the circuit model through measurement.

A. Discontinuity geometry

The discontinuity consists of a row of blind vias across the width of the SIW, joined at the blind end by a buried conducting trace which extends through the via sidewalls to ensure that the entire width of the SIW is covered, as shown in Fig. 1. The blind vias are spaced at a distance of approximately $\frac{\lambda}{4}$ (rounded to include an integer number of posts equi-spaced along the SIW width b), thereby approximating a transversal (as opposed to the longitudinal discontinuity in [17]) solid conducting wall. This structure resembles the capacitive window in [8], Fig. 5.9-1, p. 251, and is expected to exhibit similar reactance.

In the figure, the familiar waveguide dimensions a (via-wall centre to centre) and b (height) are shown, along with the dimensions r (blind via radius), d (depth of the discontinuity) and h (height of the discontinuity) which characterise the discontinuity. In this work, d and r were not independently varied; d was consistently sized 0.2 mm larger than $2r$ to ensure a minimum via-track overlap of 0.1 mm, as required

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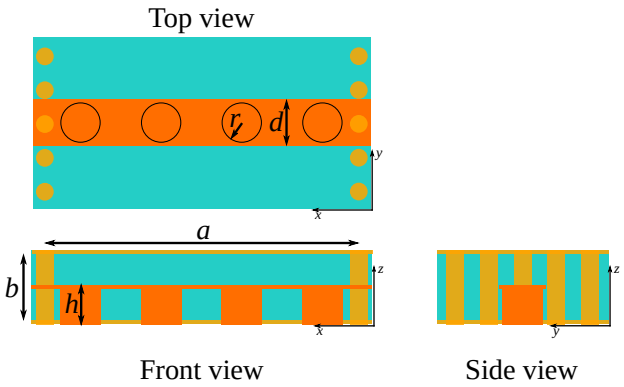
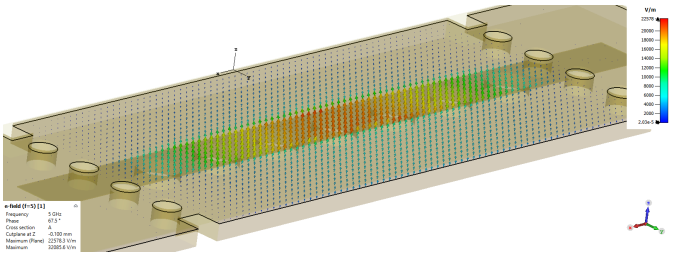


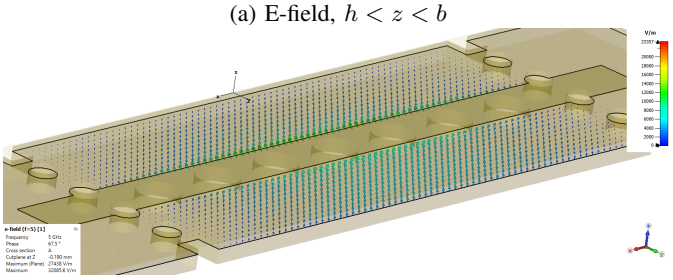
Fig. 1: Diagram of the capacitive SIW discontinuity.

by the PCB process design rules. The number and thickness of substrate-layers in the stack-up constrain both h and b to discrete values.

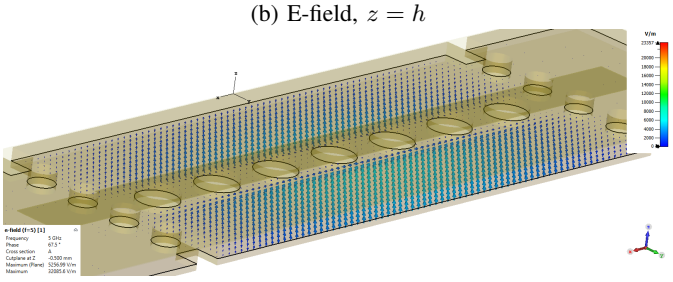
A width of a = 22.5 mm results in a TE_{10} mode cut-off in the SIW of approximately 3.6 GHz. The height of the SIW (b = 0.74 mm) is determined by the thickness of the PCB material stack-up; in this case, two sheets of laminate and one prepreg, all three of thickness 0.211 mm with 0.035mm copper cladding.‘



(a) E-field, $h < z < b$



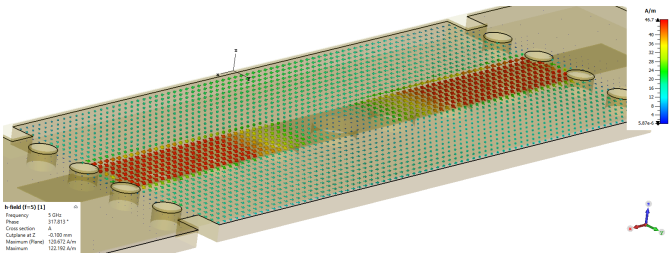
(b) E-field, $z = h$



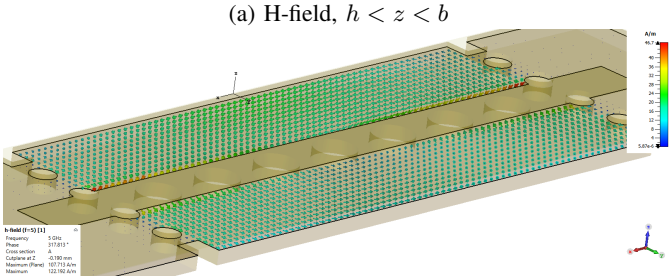
(c) E-field, $0 < z < h$

Fig. 2: E-field at various heights in the discontinuity.

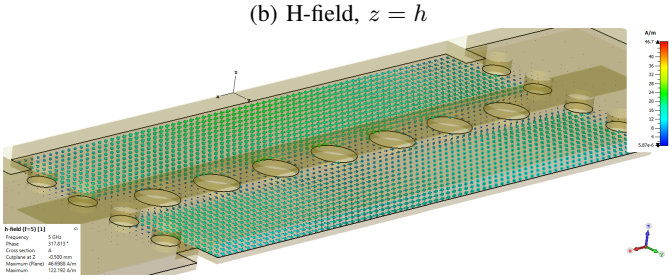
Full-wave 3D electromagnetic modelling was performed, with models excited using waveguide ports de-embedded into the centre of the discontinuity.



(a) H-field, $h < z < b$



(b) H-field, $z = h$



(c) H-field, $0 < z < h$

Fig. 3: H-field at various heights in the discontinuity.

The resulting E-field (Fig. 2) and H-field (Fig. 3) plots around the discontinuity would indicate a concentration in E_z above the discontinuity at $z > h$ and strong H_y components at $x > 0$ and $x < 0$ with a zero at $z = 0$ (where $z = 0$ is the centre-line of the SIW), with a much smaller H_y component in-between the blind vias at $z < h$. This further substantiates the view that the blind via row acts as an electric wall discontinuity and not an inductive discontinuity as exhibited in [6].

B. Equivalent Circuit Model

The proposed equivalent circuit model for the discontinuity is shown in Fig. 4, and is based on the model of the corresponding rectangular waveguide discontinuity given in [8]. As the discontinuity did not exhibit significant H-field storage at the discontinuity plane, the extended Marcuvitz model of waveguide discontinuities ([8], Fig. 6.1-1) was not selected. In addition, as the discontinuity depth $d \ll \lambda_g$, the discontinuity was not modelled as a cascaded section of high-impedance transmission line, as per Cohn's corrugated waveguide filter model [20]. These assumptions should, however, be revisited for cases where elongated discontinuities of multiple cascaded blind via rows.

To validate the model's applicability to the SIW ridge discontinuity, several parameters of the discontinuity were varied in successive 3D EM simulations. The simulated S-parameters of the geometry at each geometric parameter variation were

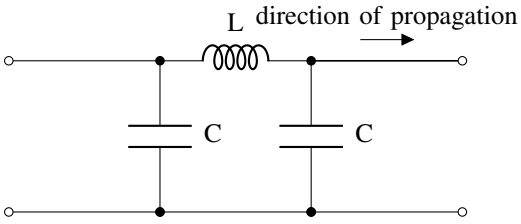


Fig. 4: Equivalent circuit model for inductive SIW discontinuity.

fitted to an equivalent circuit model using National Instruments AWR Microwave Office. The circuit parameters were adjusted, and the S_{11} parameters of the circuit and the 3D solver's results were compared, until good agreement was obtained on the Smith Chart through inspection.

With the initial values in place and all circuit parameters set as optimisation variables, AWR's optimiser was then used to minimise the error between the circuit and the EM-simulated S_{11} parameter (both magnitude and phase, as indicated in Equation 1), using a particle swarm algorithm to avoid converging on a local minimum. In the equation, the subscript CM refers to the circuit model, while EM refers to the full-wave simulation; f_1 and f_2 are, respectively, the start and end of the frequency range. Phase response correspondence is more heavily weighted than magnitude correspondence.

$$\int_{f_1}^{f_2} (|S_{11,CM}| - |S_{11,EM}|)^2 + 2(\measuredangle S_{11,CM} - \measuredangle S_{11,EM})^2 \mathrm{d}f \tag{1}$$

The circuit model was fitted to simulation results over a bandwidth of 600 MHz at a centre frequency of 5 GHz. A typical set of results is shown in Fig. 5, and indicates good correspondence between the proposed model and full-wave simulations over the frequency range of interest. There is, however, some discrepancy outside the band of interest, which would indicate the need for a more complex model if broadband correspondence is sought. The circuit model values, for each geometric variation, are shown in Fig. 6.

These results show a linear relationship between C and r for both values of h, though the gradient is much steeper in the case of h = 0.519 mm than h = 0.211 mm, indicating a greater design value range. It is also observed that the larger h resulted in a much larger capacitance than the smaller h, regardless of the value of r, which is consistent with the data in [8].

It should be noted that a negative series inductance is observed. At a single frequency, a negative inductor is equivalent to a positive capacitor on the Smith chart, but over a frequency range, the negative inductance and a positive capacitance would exhibit dissimilar responses. The negative inductance consistently resulted in a better fit. This is in line with the observation of a capacitive discontinuity in [8], Fig. 5-91, p. 251, and further confirms our view that the discontinuity may be regarded as primarily a shunt capacitor in circuit modelling.

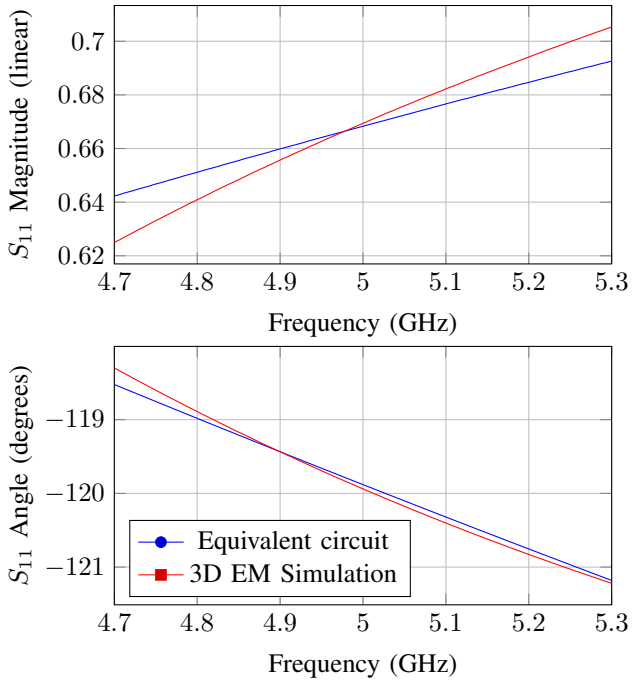


Fig. 5: Correspondence of S_{11} between full-wave and circuit model for capacitive discontinuity, h = 0.519 mm, r = 1.5 mm.

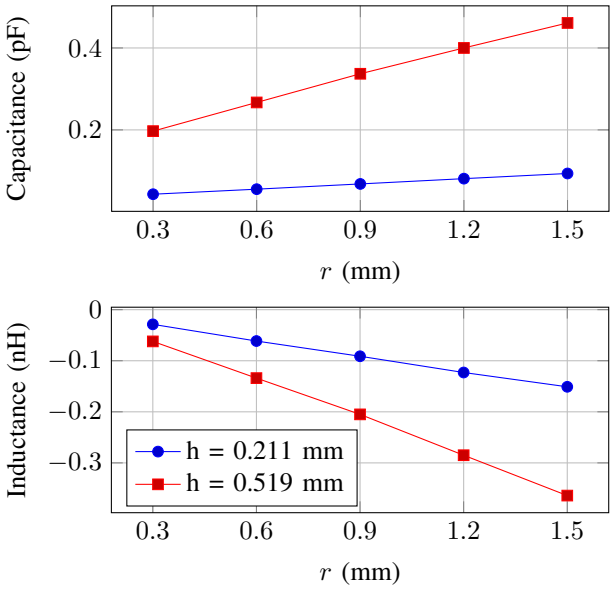
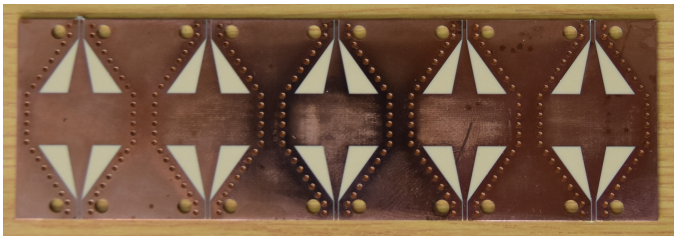


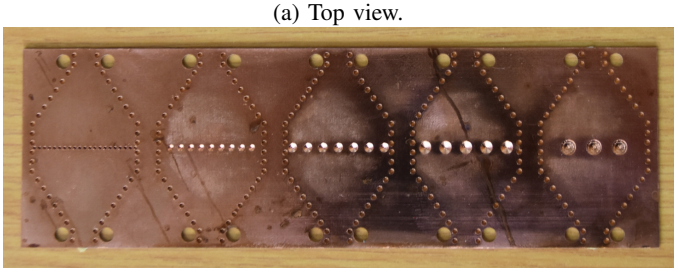
Fig. 6: Fitted circuit parameters for simulated range of dimensions

C. Prototyping and model validation

To validate the simulated results presented above, prototypes were manufactured using a single h value (due to prototyping constraints) but a range of r values corresponding to the parametric sweep presented above. The prototypes are shown in Fig. 7. TRL calibration was used in order to place the measurement reference planes in the middle of the discontinuities as it was in simulation.

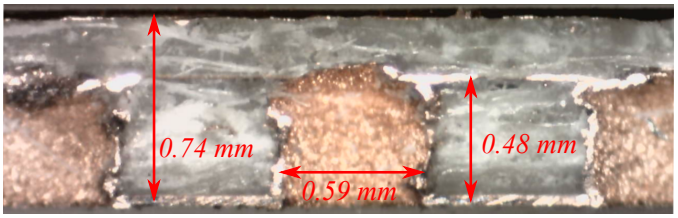


(a) Top view.

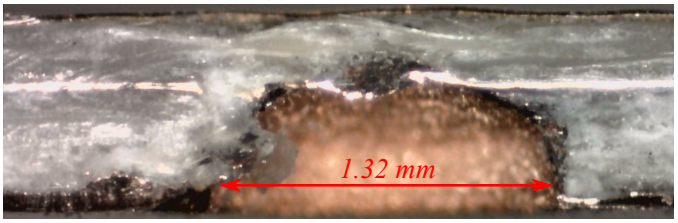


(b) Bottom view.

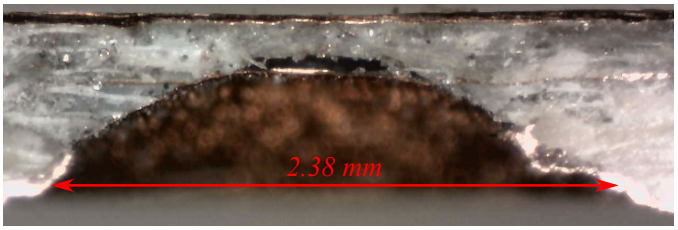
Fig. 7: Photographs of the prototype manufactured shunt capacitive discontinuity in SIW.



(a) r = 0.3 mm



(b) r = 0.6 mm



(c) r = 1.2 mm

Fig. 8: Micrographs of several sections of the capacitive discontinuities.

The cross-sectioned micrographs in Fig. 8 show the manufactured stack-up. The first micrograph indicates the thickness of the board (a), as well as the height of the copper trace forming the ridge (h), while the diameter of the via holes ($2r$) is indicated in each micrograph. The prototypes differed from the simulated stack-up somewhat in that h was reduced from a simulated 0.52 mm to a manufactured 0.48 mm, which corresponds to approximately one copper cladding thickness. It is further evident that the approximation of a cylindrical via holds better for smaller diameter vias than larger vias, which may be better approximated by a semi-sphere. This was, however, found to be a minor consideration when compared to the height variation, as the S-parameter response in EM simulation was not altered appreciably by the via shape.

Smith charts showing the reactive impedances for a range of dimensions of the discontinuity are shown in Fig. 9. Because the height of the discontinuity is the dominant factor in determining its reactive impedance, the discrepancy in h accounts for the decreased impedance of the measured results compared to the simulated data. The data further confirm that the reactive impedance of this discontinuity is determined predominantly by its height, rather than its depth. This is consistent with the results of the inductive discontinuity presented in [7], where the shunt inductance was more sensitive to the offset position than the radius of the of the inductive via post in SIW.

S_{21} results are presented in Fig. 10. Only minor differences between simulation and measurement are evident, of which the most pronounced is the consistent $\approx 15°$ transmission phase offset due to imperfect reference plane positioning in the TRL de-embedding process.

III. A Capacitively-Matched Amplifier

To demonstrate the application of the capacitive discontinuity to impedance matching, an SIW-integrated amplifier is implemented.

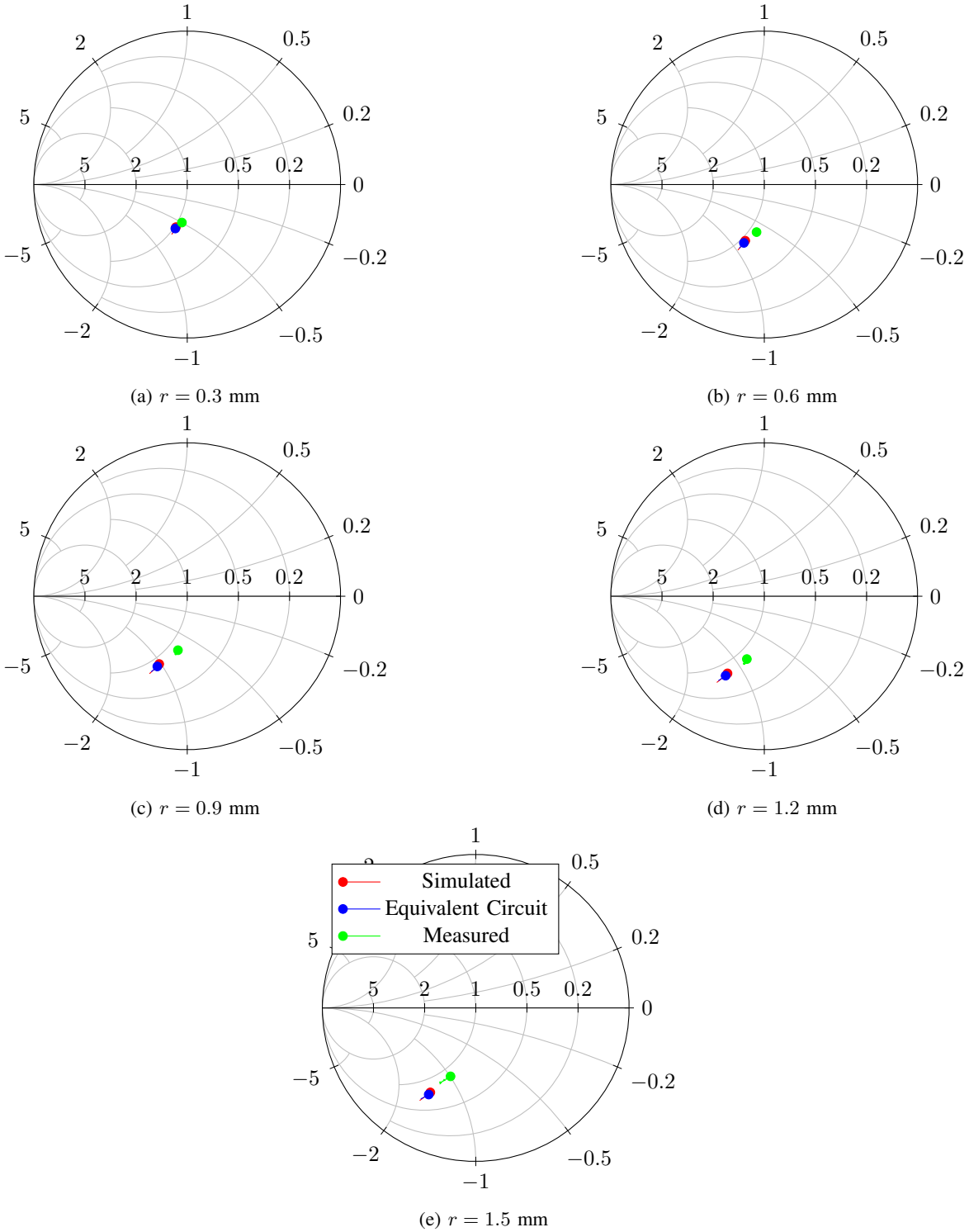
A centre frequency of 2.5 GHz is selected, as the chosen transistor's S-parameters are suitable for impedance matching with the capacitive discontinuity in this frequency range. The Infineon BFP740FESD was selected, biased at V_{CE} = 1.0 V and I_C = 30 mA, and stabilised using a series 50 Ω resistance at the output (as shown in Fig. 11). The S-parameters of the device at the centre frequency before and after stabilisation and AC coupling are given in Table I.

A. Matching Network Synthesis

THe amplifier was implemented in the same thickness (b) SIW as used previously, but a was changed to 50 mm to accommodate the lower freqency range. The size selected for the discontinuity was h = 0.519 mm, and r = 0.6 mm (with d = 1.4 mm). The equivalent circuit parameters fitted to this geometry are L = -0.14 nH, and C = 0.294 pF. To reduce synthesis and production complexity, the circuit under optimization was constrained to use N copies of the same discontinuity, spaced over variable lengths of interconnecting SIW. In principle, however, the technique can be generalised to include the dominant capacitance as a variable in addition to the spacing between the discontinuities, provided that the range of C values is constrained to values achievable with the available discrete values of h and feasible range of r values.

Fig. 12 shows the equivalent circuit model used in matching network synthesis. The synthesis method used for the matching network is as follows:

1) Heuristically select a set of dimensions for the discontinuity and create a model using the circuit parameters



(a) $r = 0.3$ mm

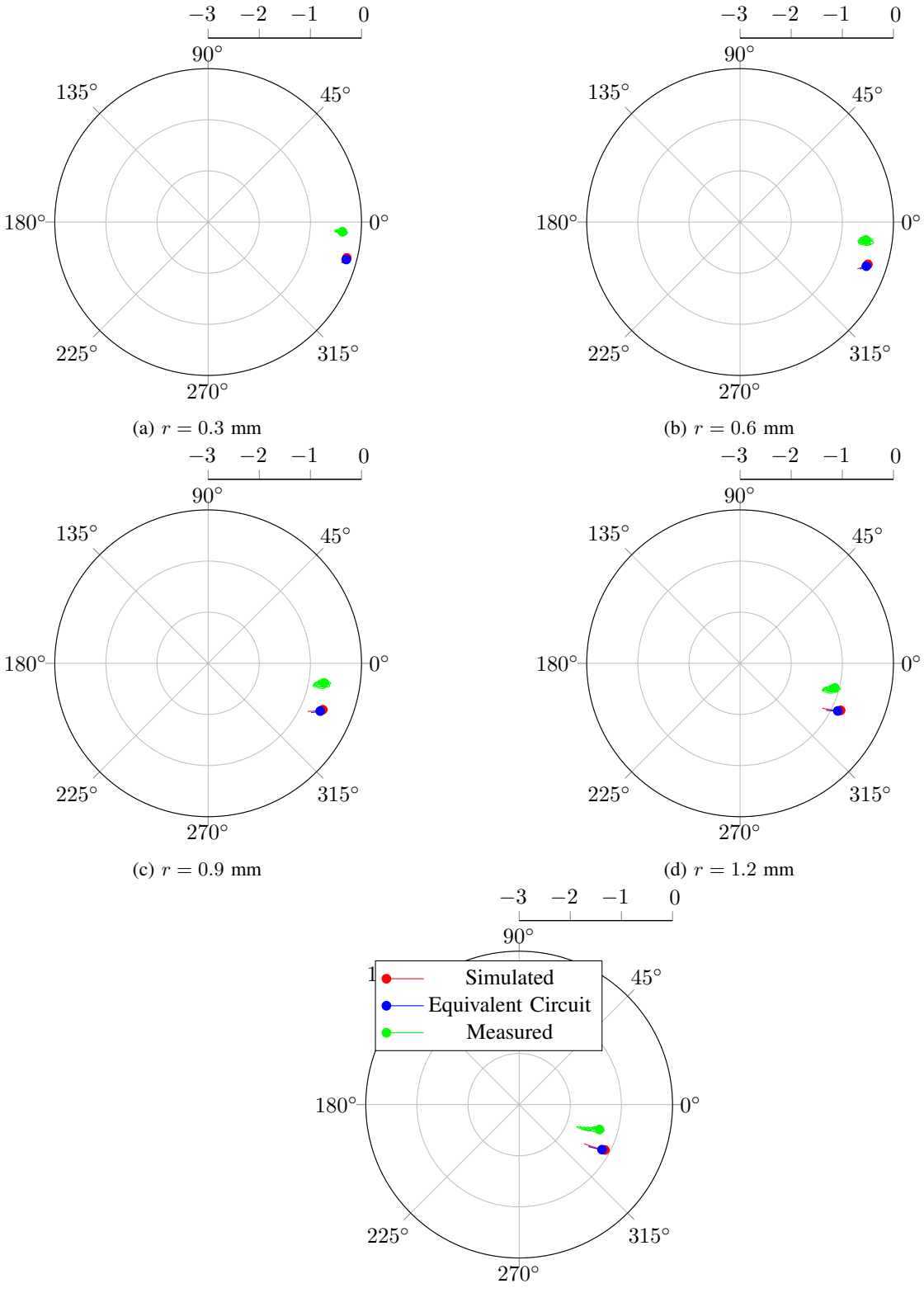
(b) $r = 0.6$ mm

(c) $r = 0.9$ mm

(d) $r = 1.2$ mm

(e) $r = 1.5$ mm

Fig. 9: S_{11} parameters of circuit model, simulation and measurement for the capacitive SIW discontinuity with h = 2 layers, or 0.519 mm, from 4.7 GHz to 5.3 GHz. The dot indicates the start of the frequency range.



(a) $r = 0.3$ mm

(b) $r = 0.6$ mm

(c) $r = 0.9$ mm

(d) $r = 1.2$ mm

(e) $r = 1.5$ mm

Fig. 10: S_{21} parameters of circuit model, simulation and measurement for the capacitive SIW discontinuity with h = 2 layers. The radial axis on each polar plot is in dB units.

corresponding to those dimensions (as described previously).

2) Implement a matching network using a single discontinuity. Select bounds for θ according to reasonable size limits in the desired manufacturing process. If a particle swarm optimiser is used then the starting value for θ can be chosen arbitrarily.
3) Optimise each θ value (in the initial iteration, there will only be one value) in the model in the circuit simulator such that the overall response of the circuit matches as closely as possible to S_{11}^* (or S_{22}^* for the output matching network) of the stabilised active device as given in Table I.
4) Inspect the results on the Smith chart.
5) If necessary to improve the match, add an additional unit of the discontinuity model to the network at an offset of θ_{n+1}, and repeat from step 3. Additional discontinuities can be added either from the source towards the load or vice versa. As previously, the starting values for θ_n can be arbitrarily selected, or can be retained from the previous step for the next optimisation.
6) Iterate over steps 3 through 5 until the addition of a further discontinuity shows no improvement in step 3.

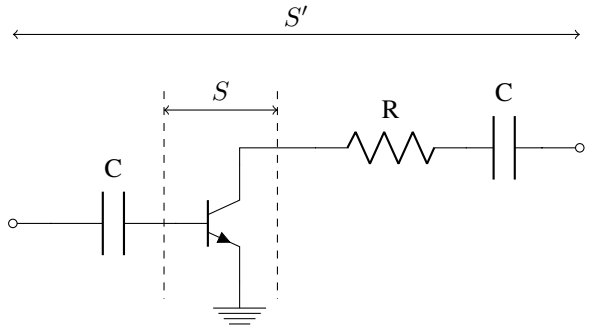


Fig. 11: Circuit diagram of stabilised and DC-decoupled transistor.

TABLE I
S_{11} AND S_{22} PARAMETERS OF THE INFINEON BFP740FESD AT 2.5 GHZ.

	S_{11}	S_{12}	S_{21}	S_{22}
S	0.77∠176.9°	0.0335∠24.7°	5.545∠72.0°	0.20∠-120.7°
S'	0.78∠159.7°	0.02∠13.48°	3.50∠60.54°	0.28∠-8.8°

After the input and output matching networks are synthesised independently (based on a unilateral assumption), a model of the full amplifier including input and output matching networks is assembled, and then both matching networks are re-optimised simultaneously, in circuit simulation, with a goal to achieve input and output matching in the band of of interest, which is below -15 dB input reflection in the band 2.4 - 2.6 GHz in this case.

Following this method, six discontinuities, separated by sections of transmission line, were used in our example for the input matching network, and their electrical lengths and corresponding approximate physical separations are given in Table II. The θ values were converted into physical spacing between discontinuities using the approximate λ_{g0} of 80 mm at 2.5 GHz. The table also shows the lengths as manufactured, after optimisation using full-wave 3D simulation.

TABLE II
θ VALUES FOR THE INPUT MATCHING NETWORK.

	Circuit synth. length (°)	**Circuit opt. length** (°)	**Initial physical length** (mm)	**3D opt. length** (mm)
θ_1	86.06	166.88	37.40	38.76
θ_2	180.00	34.18	7.66	6.688
θ_3	40.71	119.57	26.80	30.61
θ_4	149.18	21.38	4.79	4.391
θ_5	179.84	131.15	29.40	25.16
θ_6	84.89	31.96	7.16	6.978

For the output matching network, three cascaded discontinuities were found to satisfy the goal function, and their lengths and corresponding approximate physical separations are given in Table III. The table also shows the lengths as manufactured, after optimisation using full-wave 3D simulation.

TABLE III
θ VALUES FOR THE OUTPUT MATCHING NETWORK.

	Circuit synth. length (°)	**Circuit opt. length** (°)	**Initial physical length** (mm)	**3D opt. length** (mm)
θ_1	79.10	98.33	22.04	26.03
θ_2	91.37	122.08	27.36	33.38
θ_3	53.78	122.32	27.42	25.15

The S-parameters of the synthesised amplifier in circuit model simulation are shown in Fig. 13. The manufacturer-provided models for the transistor, stabilising resistor and AC coupling capacitors were used in AWR along with the circuit model of the input and output matching networks. The circuit-model amplifier is seen to achieve a gain of 15 dB over a bandwidth of 207 MHz, an input return loss of approximately 8 dB over a slightly narrower bandwidth (154 MHz) and an output return loss exceeding 10 dB over the entire passband.

The amplifier circuit model can now be used as a starting point for 3D simulation and optimisation based on the initial spacings calculated in Tables II and III, as well as the discontinuity dimensions of h = 0.519 mm, r = 0.6 mm, and w = 1.4 mm. This approach of selecting initial values for 3D optimization based on a surrogate circuit model optimization greatly reduces the number of 3D optimisation iterations [21].

B. Planar transitions

An SIW-to-CPW transition based on that presented in [22] was implemented and subsequently adapted to transition from SIW to the footprint of the transistor, making provision for AC-coupling capacitors and stabilising resistor. The layout is shown in Fig. 14. In contrast to the AC-coupled transition of [6] (where the series reactance of the capacitor was utilised in the impedance matching network), the transition presented here was optimised to present a lower series reactance to the transistor, thereby having minimal influence on the reactive

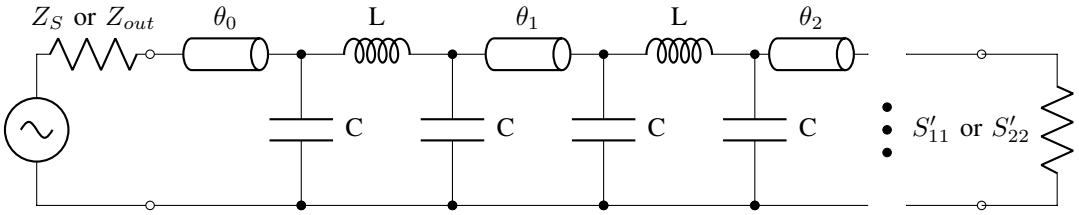


Fig. 12: Circuit model for matching network synthesis.

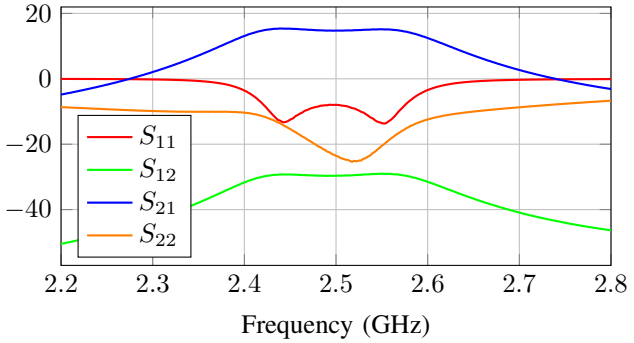


Fig. 13: S-parameters of circuit-model amplifier using simultaneously optimised matching networks.

matching introduced by the discontinuities within the SIW. Also shown in the figure are thin, high-impedance copper traces for biasing. Table IV lists the connections for each port indicated in the figure. s_1, s_2 and s_3, are optimised dimensions used to minimise the reflections seen at port B. The same dimensions were optimised independently for port C in the case of the output transition, with the inclusion of s_4, which was necessary because of the inclusion of the stabilising resistor at the output.

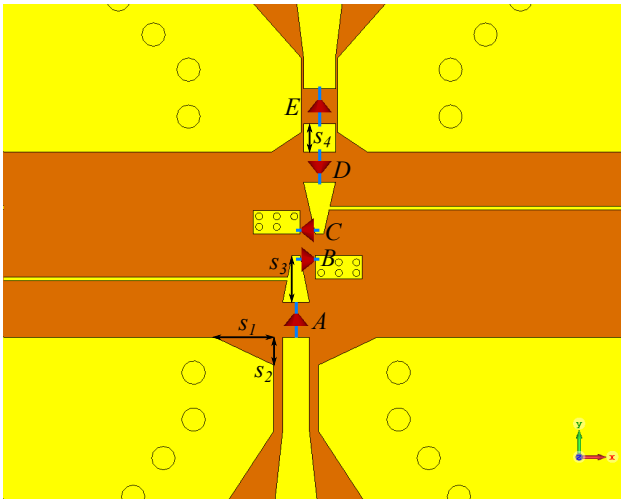


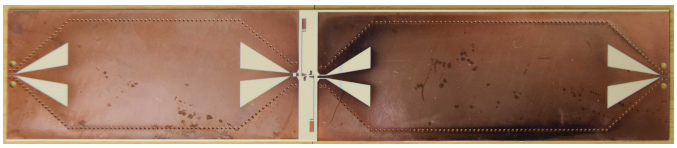
Fig. 14: CAD diagram of the CPW-to-microstrip transition used in the amplifier, including space to accommodate DC-decoupling capacitors.

No consistent equivalent circuit model for the transition could be found. It is found that this transition reduces the effectiveness of the matching compared to the circuit model

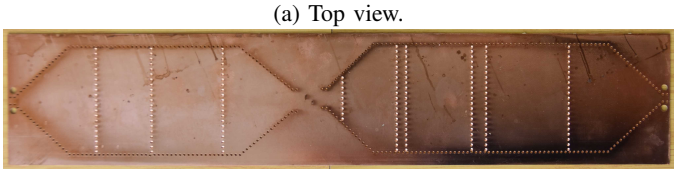
TABLE IV
PORT CONNECTIONS INDICATED IN FIG. 14

Port	Description
A	Connection of input AC-coupling capacitor
B	Connection of base-emitter terminal of transistor
C	Connection of collector-emitter terminal of transistor
D	Connection of stabilising resistor
E	Connection of output AC-coupling capacitor

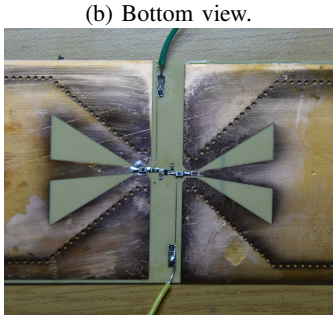
in isolation, which reduces the efficacy of SIW discontinuities as reactive matching elements somewhat.



(a) Top view.



(b) Bottom view.



(c) Detailed top view, PCB populated.

Fig. 15: Photographs of the prototyped amplifier.

C. Prototyping and Results

Photographs of the prototyped amplifier are shown in Figs. 15 and 16. The full-wave simulated and measured S-parameters of the prototype amplifier are shown in Fig. 17. While 3D simulation and measurement compare favourably, the discrepancy between circuit-simulated and EM-simulated results (due to the SIW-microstrip transitions not modelled in the circuit model) is evident when comparing the results in Figs. 13 and 17. Input return loss at the centre frequency

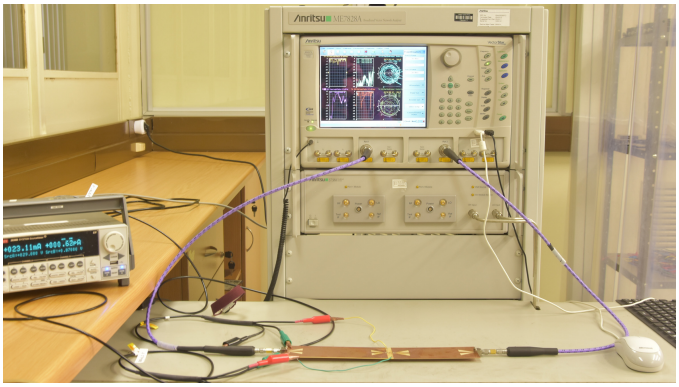


Fig. 16: Measurement setup, showing the VNA, the coaxial cables and the SMA end-launch connectors attached to the prototype amplifier.

is similar in the 3D-simulated and measured cases at approximately 10 dB, but the output return loss is reduced from above 20 dB in circuit simulation to around 10 dB in EM simulation and measurement. An impedance bandwidth of approximately 50 MHz is achieved, compared with 200 MHz in the circuit–simulated case. This is attributed to the effect of the SIW-to-planar transitions, which reduce the efficacy of the SIW-embedded discontinuities as impedance matching elements.

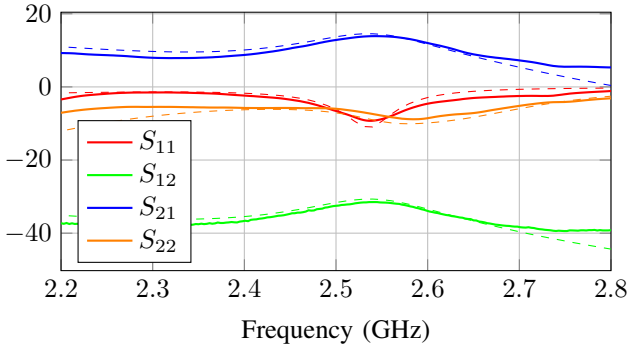


Fig. 17: Measured (solid) vs EM-simulated (dashed) amplifier S-parameters.

IV. Conclusion

In this work, the set of SIW reactive discontinuities suitable to impedance matching has been expanded to include a shunt capacitive discontinuity. An equivalent circuit model (and modelling approach) is presented, and its application demonstrated through implementation in a matching network for an SIW-embedded amplifier.

It is found that the reactance of the capacitive discontinuity is predominantly determined by its height, but can be tuned by its depth. It is anticipated that a shunt capacitive discontinuity may lead to a greater flexibility in impedance-matching to transistors with a substantial inductive input reactance component. It may also be implemented in cases where DC isolation is required between the conducting planes, as is the case with planar groove gap waveguide (PGGWG) [23], where a shunt inductance through-hole via will create a DC path between the planes. As this discontinuity cannot be realised in single-layer SIW, the range of heights available is limited to discrete values based on the number and thickness of substrate layers, which makes tuning by depth variation an important characteristic. A multi-layered stack-up will provide additional flexibility in this regard, but will similarly increase the cost to fabricate.

Table V compares this work to the other small-signal SIW-embedded amplifiers in literature. It is evident that the effectiveness of the matching achieved with the capacitive discontinuity is comparable to that achieved by other works using only inductive discontinuities, whilst maintaining similar sizing relative to wavelength. It should, however, be pointed out that SIW matching generally leads to larger circuits than what is achievable with lumped element matching over a similar band [24] and that the amplifier design presented here is only an example to illustrate how impedance matching could be effected by application of the discontinuity.

Future work will seek to investigate the effect of multiple cascaded via rows ($d \gg 2r$), and derive models similar to Cohn's corrugated waveguide model for these. Their application to impedance matching in SIW will then be investigated further, as d would then be an additional optimization variable independent of r and h. More future work would seek to apply the capacitive discontintinuitiy in other impedance-matching applications, such as antennas [25], or filter design [26], as well as integration of the discontinuity with PGGWG [23].

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TABLE V
COMPARISON OF RESULTS OF VARIOUS SIW-EMBEDDED AMPLIFIERS.

	f_0 (GHz)	**Gain** (dB)	**Input RL** (dB)	**Output RL** (dB)	**FBW** (%)	**Size** (λ_0)	**Matching**
This work	2.5	14	9	9	2.0	≈ 2	Capacitive, SIW
[6]	10.5	9	10	10	28	≈ 0.9	Inductive, SIW
[7]	3.6	13	-	-	-	-	Inductive, SIW
[13]	5.8	10	10	10	80	≈ 1.2	Distributed, corrugated SIW
[15]	24	20	10	10	20	-	Internal active device

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