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Johan Venter, Saurabh Sinha, Wynand Lambrechts, "Characterization of diode-connected heterojunction bipolar transistors for near-infrared detecting applications," *Opt. Eng.* **57**(11), 117104 (2018), doi: 10.1117/1.OE.57.11.117104.

Characterization of diode-connected heterojunction bipolar transistors for near-infrared detecting applications

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Abstract. The characterization of SiGe diode-connected heterojunction bipolar transistors (HBTs) through measurements of two-circuit configurations is presented. Characterization is done to understand the behavior of these diodes for near-infrared detecting applications at room temperature and 77 K. The two configurations that are considered differ; the first is a base-emitter shorted HBT and the second is a base-collector shorted HBT. The parameters measured are current density-voltage, capacitance-voltage, and noise. The two configurations are implemented using the austriamicrosystems AG 0.35- μm process. The base-emitter shorted configuration exhibits a flatter J_C versus V curve when in reverse bias compared with the base-collector configuration. The $C - V$ curves are the same for both configurations. The noise voltage of the base-emitter configuration is 36 and 14.48 $\mu\text{V}/\sqrt{\text{Hz}}$ at 102.5 Hz for 293 and 77 K temperature points, respectively, to 14.48 and 12.42 $\mu\text{V}/\sqrt{\text{Hz}}$ at 50 kHz for 293 and 77 K, respectively. The noise voltage for the base-collector configuration is 12.6 and 7.56 $\mu\text{V}/\sqrt{\text{Hz}}$ at 102.5 Hz for 293 and 77 K, respectively, to 2.228 and 5.981 $\mu\text{V}/\sqrt{\text{Hz}}$ at 50 kHz for 293 and 77 K, respectively. This work is done using a standard Si-based technology, where a detector array with readout circuitry can be prototyped as a single chip. The floating base transistor topology is analyzed and used as a foundation for this work. The characteristics of a floating base configuration result in a wide depletion region, large-series resistance, and small-series capacitance. When shorting the base with the emitter and collector, respectively, compared with a floating base configuration, a smaller depletion region, reduced series resistance, and larger series capacitance are observed. © 2018 Society of Photo-Optical Instrumentation Engineers (SPIE) [DOI: 10.1117/1.OE.57.11.117104]

Keywords: heterojunction bipolar transistor; infrared radiation photodetectors; circuit noise; diode-connected transistor; cryogenic operation.

Paper 181089 received Jul. 29, 2018; accepted for publication Oct. 23, 2018; published online Nov. 8, 2018.

1 Introduction

Imaging is used in a variety of specialized applications and has shown significant progress.¹⁻⁶ Nonsilicon-based infrared detectors are costly to manufacture and exhibit integration issues with conventional integrated circuit (IC) technologies⁷ to realize optoelectronic applications. Silicon germanium (SiGe) IC technology presents a favorable platform for near-infrared photodetector development because of the ease of integration with a standard Si technology.⁸

Characterization of SiGe diode-connected heterojunction bipolar transistors (HBTs) using two configurations with measurements at room temperature (293 K) and cryogenic temperature (77 K) are presented in this paper. Cryogenic small-signal modeling of SiGe HBTs⁹ using non-CMOS-based technology has been reported in the literature. Because of its band gap-engineered base, cooling affects the performance of SiGe HBTs favorably.¹⁰

Specifically, the use of SiGe shows improved performance over other CMOS technologies for dynamic range (DR) and sensitivity.⁸ SiGe HBTs exhibit decreased base resistance, increased maximum oscillation and cutoff frequency, increased Early voltage and increased current gain compared with Si bipolar junction transistors (BJTs). The same collector current density (J_C) and base current

density (J_B) are seen at lower base-emitter voltages (for a 10^{-5} mA/ μm^2 J_B and J_C , measured at 0.7 and 0.55 V, respectively, for SiGe HBTs and at 1.05 and 1 V, respectively, for Si BJTs).¹¹

Ge exhibits higher carrier mobility and decreased band gap. By combining Si with Ge, both material features are combined with mature processing techniques and improved performance. SiGe exhibits a high film reflectivity that impacts the lithography process severely. However, efforts have been made to reduce the reflectivity and aid the lithography process by adding dielectric films. This resulted in an increased interest from researchers for SiGe HBTs.¹²

As CMOS processes have no BJTs available, the detecting element has to be formed with standard available layers as shown in Fig. 1.

In Fig. 1, the layers used in the CMOS technology to form a detecting element are shown. These layers are available in most of the CMOS processes. Depending on the application, the lightly doped intrinsic layer (i) is used or omitted for a specific spectral response. If it is used, then the junction capacitance between p -type and n -type materials is reduced at the cost of detecting processing speed. If the intrinsic layer is not included, then the junction capacitance is increased and the carrier transit time (τ_f) is reduced. Exclusion of

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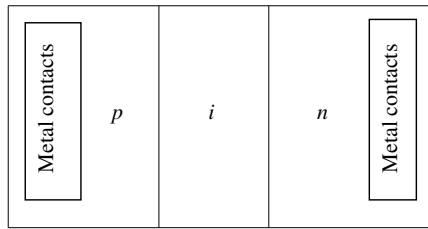


Fig. 1 Top view of the formation of a detecting element in CMOS technology.

the intrinsic layer will result in the *p*-type layer being physically placed next to the *n*-type layer with no space in between forming a *p* – *n* diode. The intrinsic layer will always be present around the formed diode as the wafer is always lightly doped and seen as the intrinsic layer. Detection of elements using *n* – *p* – *n* transistors has been documented where the base terminal is left floating.¹³ The structure of BJTs using the BiCMOS technology and the two different configurations is shown in Fig. 2.

In Figs. 2(c) and 2(d), C_{DEP} and R_S denote the depletion region capacitance and series resistance, respectively. Typical phototransistors using non-BiCMOS technology have a base that is between the collector and the emitter, whereas the emitter is contained within the base in the case of the BiCMOS technology. The characteristics of a floating base configuration are an open loop system with a wide depletion region, large series resistance, small-series capacitance, and a long carrier transit time.

One way to overcome this problem is shorting the base and emitter for one configuration, as well as shorting the base and collector for a second configuration. The characteristics of this configuration, compared with a floating base configuration, are a smaller depletion region, reduced series resistance, larger series capacitance, and reduced carrier transit time. The lightly doped *p*-type substrate will have no effect on the base-collector shorted configuration; however, it will still have some effect on the base-emitter shorted configuration. A *p*–*n* diode is formed for the base-collector shorted configuration; however, for the base-emitter shorted configuration, a *p* – *i* – *n* diode is formed where the lateral lightly doped *p*-type substrate region is very small. The lightly doped *p*-type substrate has a higher resistance owing to a lower number of free electrons and will, therefore, result in a lower reverse biased leakage current. This lower reverse leakage current is desired when used as a detecting element. This theory is backed up by practical measurements as shown in Figs. 9 and 10, respectively.

With the use of the two configurations and a measurement setup as described in Sec. 5, three parameters (current density versus voltage, capacitance versus voltage, and noise voltage) have been measured at 293 and 77 K, respectively.

2 Detector Materials

Several types of detecting elements are available, spanning a wide range of materials. One way to compare detectors is analyzing the quantum efficiency of different elements. The best material to use for near-infrared detecting elements is mercury cadmium telluride ($Hg_{0.22}Cd_{0.78}Te$).¹⁴ This material is expensive and difficult to fabricate. SiGe exhibits acceptable quantum efficiency for near-infrared detection (around 1% at 4- μm wavelength¹²), and the cost of manufacturing is much cheaper. As this work focuses on a set of IC fabrication technology, the limitations brought forward with the technology platform form the basis for this paper. A comparison of detectors using IC fabrication technology is shown in Table 1.

Table 1 shows a comparison of CMOS and BiCMOS detectors. Specifically, the use of SiGe shows improved performance over other CMOS technologies for DR and sensitivity.

3 Capacitance–Voltage Modeling

The junction capacitance determines the capacitance–voltage relationship at a specific bias voltage as shown in Eq. (1):

$$C_j(V_d) = \frac{C_{j0}}{\left(1 - \frac{V_d}{\phi_B}\right)^{m_j}}, \tag{1}$$

where C_j is the junction capacitance at the specified bias voltage (V_d). The parameters (C_{j0}, m_j) are process-dependent parameters and again can be determined using parameter extraction methods. The parameters (C_j, V_d) are variable parameters related to each other according to the relationship in Eq. (1). The parameter m_j (0 – 0.5) is a fitting parameter. This parameter differs in the reverse biased region as opposed to the forward biased region. The parameter ϕ_B is variable, as it has a linear temperature dependence, as shown in Eq. (2):

$$\phi_B = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}, \tag{2}$$

where $n_i = BT^{3/2} e^{\frac{-E_g}{2kT}}$.

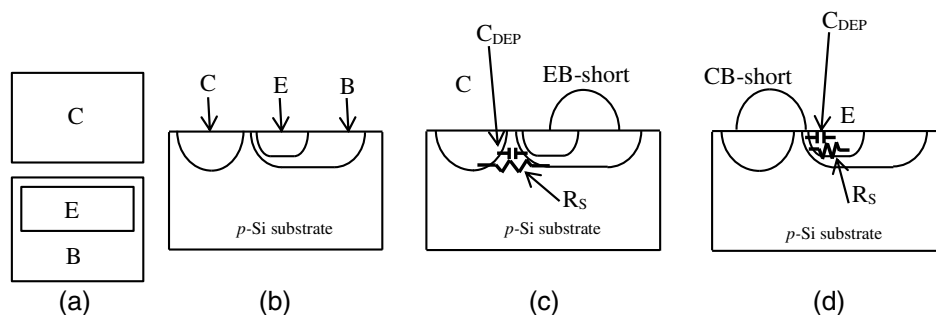


Fig. 2 BJT structure using BiCMOS technology (a) top view, (b) side view, (c) base-emitter shorted configuration, and (d) base-collector shorted configuration.

Table 1 Published BiCMOS/CMOS detector values.

Reference	Ref. 15	Ref. 16	Ref. 17	Ref. 18	Ref. 19	Ref. 8
Technology node	0.35 μm Si CMOS	0.18 μm Si CMOS	0.18 μm Si CMOS	0.13 μm Si CMOS	0.13 μm Si CMOS	0.35 μm SiGe BiCMOS
Array size	128 \times 128	—	64 \times 64	—	—	2 \times 2
Pixel size (μm)	40 \times 40	—	30 \times 30	—	—	6.6 \times 11
Pixel area (μm^2)	—	60 \times 60	—	—	—	—
Chip size (mm)	6.5 \times 6.5	—	3 \times 3	—	—	1.3 \times 1.3
Noise $\mu\text{V}/\sqrt{\text{Hz}}$	0.76	72	—	—	50	2
DR (dB)	—	—	54	47	—	66
Sensitivity	4970 V/W	0.1 A/W	2750 V/W	26.8 mV/dB	5000 V/W	180000 V/W or 180 mA/W
Power consumption (mW)	—	23.4	125	0.1	—	10

As the device is cooled, the built-in bulk potential increases slowly. Using the following set of parameters, ($B = 5.23 \times 10^{15}$, $E_g = 1.1$ eV, Boltzmann constant $k = 8.6 \times 10^{-5}$ eV/K, $N_A = 10^{16}$ cm^{-3} and $N_D = 10^{15}$ cm^{-3}), the built-in bulk potential increased from 0.68 to 1 V when cooled from 273 to 77 K.

4 Noise Applicable to Diode-Connected Heterojunction Bipolar Transistors

In this section, a short overview of the noise generators of diode-connected HBTs is discussed. As two terminals of the HBT are shorted in both topologies, noise generators of diodes and HBTs need to be analyzed thoroughly.

4.1 Diode Noise Generators

As both sides of a $p - n$ junction exhibit resistance due to the intrinsic material, it exhibits thermal noise, which is modeled as a voltage and current generator. Shot noise and flicker noise are also present in a diode and are modeled by a current generator. A small-signal equivalent circuit for a diode with noise generators is shown in Fig. 3.

Figure 3 shows the small-signal equivalent model of a junction diode with noise generators and characteristic impedance elements. The resistance r_d models the shot

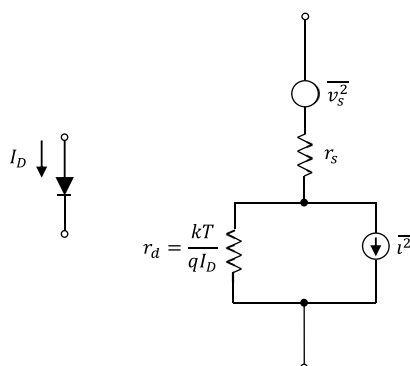


Fig. 3 Small-signal equivalent model of a junction diode.

noise resistance, which is the inverse of the transconductance of the diode, and r_s models the thermal resistance of the diode. The two noise generator models are shown in Eqs. (3) and (4):

$$\overline{v_s^2} = 4kTr_s\Delta f, \tag{3}$$

$$\overline{i^2} = 2qI_D\Delta f + K\frac{I_D^a}{f}\Delta f. \tag{4}$$

Equation (3) represents the thermal noise, which is temperature-dependent. Using the Thévenin equivalent of Eq. (4), a noise voltage model is realized using the characteristic impedance of a diode. This then results in a noise voltage model that is both temperature- and current-dependent. Shot noise and flicker noise, usually associated with current flow, are then represented as a noise voltage.

4.2 Heterojunction Bipolar Transistor Noise Generators

Through the analysis of the small-signal model generators and elements that are eliminated by shorting the base to the collector and emitter, respectively, the noise generators of a junction diode can be related to a diode-connected HBT.

For a base-emitter shorted HBT, the small-signal model is shown in Fig. 4.

As the base and emitter are shorted, v_{be} is 0 V. Therefore, the current generator $g_m v_{be}$ is also 0 V and can be omitted. Consequently, only the output resistance (r_o) remains. This can be equated to the thermal resistance, r_s , as there are no current generators.

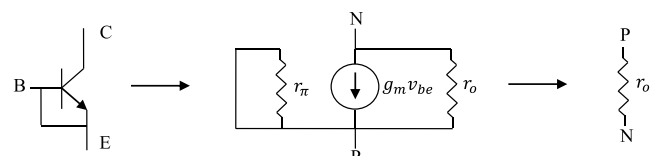


Fig. 4 Small-signal equivalent model of a base-emitter shorted HBT.

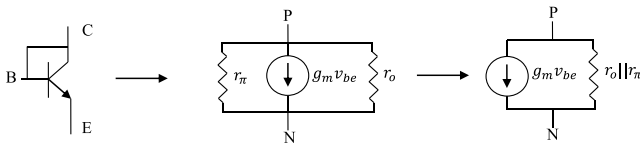


Fig. 5 Small-signal equivalent model of a base-collector shorted HBT.

The base-collector shorted HBT small-signal model is shown in Fig. 5.

In Fig. 5, the small-signal equivalent model of a base-collector shorted HBT is given. The input resistance (r_{π}) and output resistance (r_o) can be combined in parallel. Intuitively, it can be seen that this topology exhibits lower noise because of the current generator and the extra characteristic impedance that is present (r_{π}). This result is confirmed in Sec. 6 through practical measurements. As r_{π} and r_o are both temperature-sensitive, this parallel combination can be equated to the thermal resistance of the diode. As r_d models the shot noise of the diode requiring a current, r_d is only applicable to the base-collector shorted HBT, which is equal to $r_o || r_{\pi}$.

5 Measurement Setup

Prototyping was formerly accomplished and also published.⁸ As shown in Fig. 6, the same prototype has been used and subjected to the experimental findings reported through this paper.

The glass lid was removed to gain access to the IC and enable wire-bonding to measure device characteristics as seen in Fig. 6. A temperature sensor was placed on the IC to determine the operating temperature of the device. All nodes were wire-bonded using 25- μm gold wires. The IC was placed on a ceramic plate, wire-bonds were bonded to the aluminum (Al) metal connections, and thicker wires were soldered on the other ends of those connections. The bare die (labeled as ams AG S35 DUT in Fig. 6) is placed on a package with bonding wires that run to the ends of the package. Connection pins under the ends of the package allow the package to be soldered onto a printed circuit board, similar to a surface mount IC. For this work, no soldering was done under the ends of the package to the ceramic back plate. The original prototype had a glass lid on, but this was removed to place a temperature sensor on the bare die to accurately measure the operating temperature of the bare die. This die is a multiproject wafer where three projects and

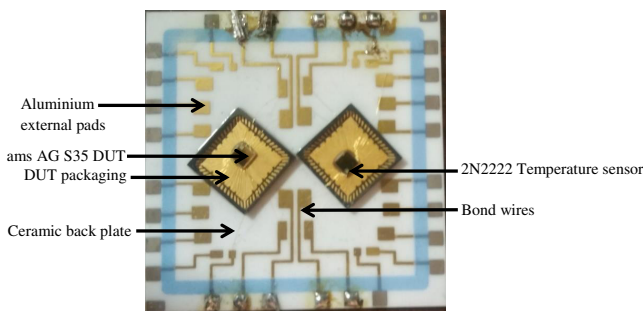


Fig. 6 IC prototype mounted on a ceramic back plate (32 mm \times 32 mm).

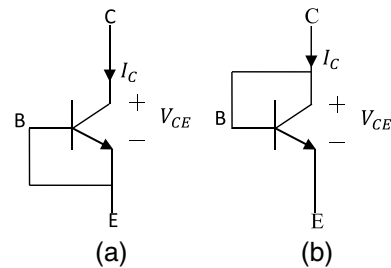


Fig. 7 Measurement circuit configurations for I-V and C-V measurements (a) base-collector shorted HBT and (b) base-emitter shorted HBT.

a lone-standing HBT were included as per the MOSIS Educational Programme (prototyping sponsorship).

The exact doping percentage value of the Ge in ams AG SiGe BiCMOS technology is protected under a non-disclosure agreement. One additional aim of this characterization work is to use standard BiCMOS fabrication technology for near-infrared detectors, and the determination of the percentage doping of Ge is left for future extension of this work.

The IC with ceramic back plate was placed onto a platform on which liquid nitrogen was poured to cool the IC down. Measurements were then obtained at 77 K. The device analyzer used to measure the parameters was an Agilent B1500A semiconductor device analyzer and an HP 3651A dynamic signal analyzer together with a DC power supply.

For the I-V and C-V measurements, the collectors and emitters of the two configurations were directly connected to the inputs of the semiconductor device analyzer. The two configurations are shown in Fig. 7.

For Fig. 7(a), the collector was connected to the positive input terminal of the analyzer and the emitter was connected to the negative input terminal. For Fig. 7(b), the terminals were swapped around. To measure the noise, a resistor was used to limit current flow through the diode.

The two proposed circuits to measure noise are shown in Figs. 8(a) and 8(b). The bias resistor (R_{BIAS}) was not cooled down to 77 K. The input terminals of the dynamic signal analyzer were connected on the collector and emitter of the HBT.

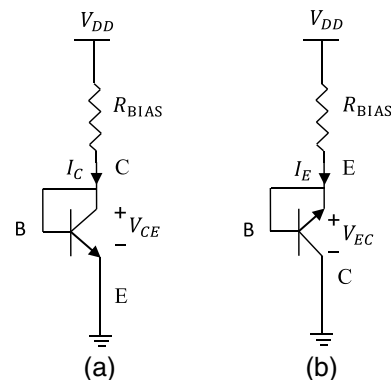


Fig. 8 Measurement circuit configurations for noise measurements (a) base-collector shorted HBT and (b) base-emitter shorted HBT.

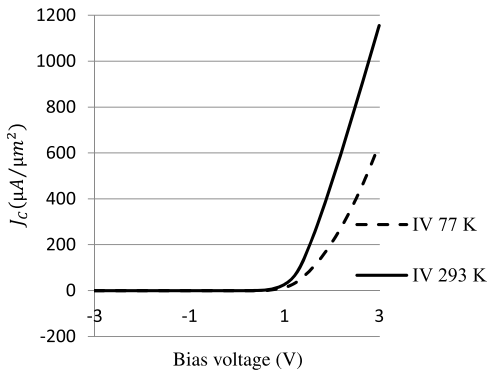


Fig. 9 Collector current density versus bias voltage measurements of base-emitter shorted HBT.

6 I-V Measurements Results

In this section, the measured results are presented for collector current density J_C ($\mu A/\mu m^2$) versus bias voltage at room temperature (293 K) and at 77 K. This is to show the effect temperature has on the current density. In Figs. 9 and 10, the current density versus bias voltage measurements of both configurations are shown.

In both Figs. 9 and 10, the cooler the device, the lower the current density for bias voltages between -3 and 3 V. This could be attributed to carrier freeze-out that happens at much higher temperatures than Si diodes. Conventional doping theory with respect to carrier freeze-out suggests that the higher the doping density, the lower the ionization energy as seen in Eqs. (5) and (6):²⁰

$$\Delta E_D = E_{D0} - 3.1 \times 10^{-8} N_D^{1/3} + (200T^{-1} - 0.66) \quad (5)$$

and

$$\Delta E_A = E_{A0} - 3.037 \times 10^{-8} N_A^{1/3} + (200T^{-0.95} - 0.88). \quad (6)$$

This would suggest that by doping the Si with Ge, the temperature where carrier freeze-out occurs would be much lower than only in Si. In addition, one has to take into account sheet resistance associated with the devices. When Si is doped with Ge, the base resistance increases significantly at around 150 K, which could be the point where carrier freeze-out occurs. Moreover, for low current flow, the sheet resistance is lower at room temperature compared with low temperatures such as 77 K. This supports the results obtained, where the current density for room temperature is

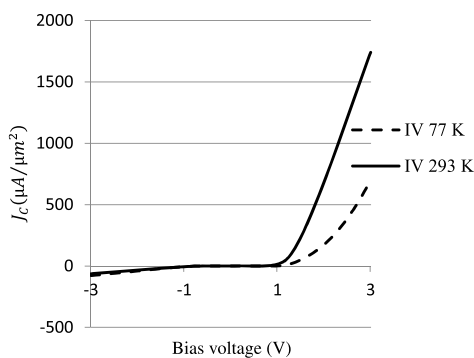


Fig. 10 Collector current density versus bias voltage measurements of base-collector shorted HBT.

much higher than at 77 K. A physical interpretation that would support this claim is that the atomic radius of Ge is slightly larger than that of Si. The amount of contraction when cooled is slightly smaller when a Ge atom is doped in the crystal lattice of the Si structure compared with a Si atom structure. Both interpretations support the results obtained.

The base-emitter shorted HBT has lightly doped p -type substrate with increased resistance due to lower doping. Thus, current flow will be restricted compared with a base-collector shorted HBT. This explains why the measured base-collector shorted HBT current density is higher compared with the base-emitter shorted HBT. As mobility is increased due to the lower base resistance as a result of the germanium doping, sensitivity in the near-infrared range using SiGe HBTs as detecting elements peaked at 665 nm, which is about 9.5 dB higher than a Si pin-diode measured on the same prototype IC.⁸ It must be noted that the given measurements were from two detector arrays with readout circuitry, where the one included SiGe diode-connected HBTs and the other one included Si pin-diodes. In both instances, a 2×2 array was used where the total detecting area was the same. For this work, lone-standing HBTs with no-included readout circuitry was used. This provided insight into the effect of Ge for near-infrared detectors.

For the reverse-biased region, the base-emitter shorted HBT has a low leakage current ($71.3 \text{ nA}/\mu m^2$ at 293 K and $153 \text{ pA}/\mu m^2$ at 77 K for a -3-V bias voltage) with no illumination, whereas the base-collector shorted HBT has some leakage current ($62.95 \text{ }\mu A/\mu m^2$ at 293 K and $78.15 \text{ }\mu A/\mu m^2$ at 77 K) for -3-V bias voltage. Therefore, when current density is the primary factor in the detector design, the base-emitter shorted HBT would function better when used as a reverse-biased pixel where leakage current density is the parameter of concern.

7 C-V Measurements Results

In this section, the C-V results for 293 and 77 K are presented for various oscillation frequencies at bias voltages less than the built-in bulk potential (0.7 V for 293 K and ~ 1 V for 77 K). In Figs. 11 and 12, the capacitance-voltage curves for different oscillation frequencies at 293 and 77 K for both topologies are given.

For Figs. 11 and 12, the peaks of most of the capacitances occur at a built-in bulk potential around 0.7 V. The peak of

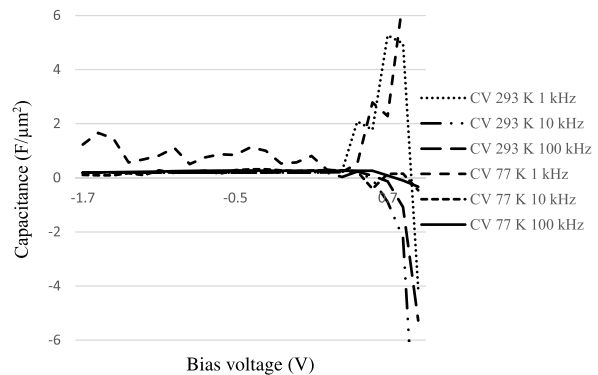


Fig. 11 Capacitance versus bias voltage measurements of base-emitter shorted HBT.

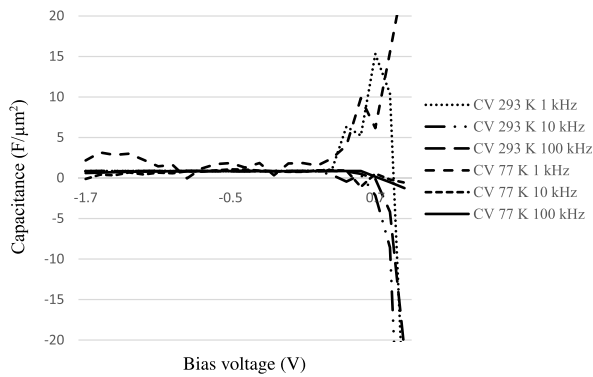


Fig. 12 Capacitance versus bias voltage measurements of base-collector shorted HBT.

the capacitance for 1 kHz oscillation frequency at 77 K for both configurations is reached at a higher built-in bulk potential, thereby confirming the simulated results shown in Sec. 3. For the higher oscillation frequencies (10 and 100 kHz), for both configurations, no peaking is observed. A physical interpretation of this deviation from the expected increase in capacitance is that because of the high rate of charging and discharging of the regions, negligible charge builds up and is released quickly.

Negative capacitance is also observed for most of the curves. Practically there is no such thing as negative capacitance, as capacitance is a measure of how much charge is stored. However, the origin of negative capacitance behavior is attributed to the nonmonotonic or positive-valued behavior of the derivative of the transient current in response to a small voltage step.²¹ This is gathered by analyzing the capacitance model from a transient response point of view with the analysis of the transient currents at bias voltages above the built-in bulk potential and at large negative bias voltages. Semiconductor devices can exhibit negative capacitance behavior even when no significant negative capacitance is present. Physically, when the bias voltage is above the built-in bulk potential, the diode becomes saturated. For that reason, the theoretical model collapses as given in Sec. 3. The measurements, however, show the decrease in capacitance into the negative capacitance region.

There are three possible reasons why the results are observed:

1. They are due to the transient behavior as discussed.²²
2. The diode reacts inductively when analyzing from an impedance perspective.
3. The saturation of the diode causes the result.

Despite reports that the decrease is due to the transient behavior,²² a thorough investigation and model development can be done as an extension to this work to verify this phenomenon from a semiconductor physics point of view. The measurements were done on a semiconductor device analyzer, where a specific C–V curve analysis program was written to measure these curves. The program made use of time-domain transient responses, where specific provisions were made for negative capacitance measurements. It was found that the negative capacitance curves measured under the same conditions as the positive capacitance curves followed a distinct curve as opposed to irregular spikes.

The measurements of positive capacitance below the built-in bulk potential and the steep drop into the negative capacitance above the built-in bulk potential were taken in one sweep. Justification for this behavior is left for future work as this work is focused on the characterization SiGe diode-connected HBTs.

8 Noise Measurements Results

In this section, the measured noise results are presented and analyzed. For the base-emitter shorted case, the positive side of the DC power supply was connected to the collector and the negative one on the base-emitter shorted terminal. The chosen bias voltage and resistor were 3.3 V and 1 kΩ, respectively. The chosen noise bandwidths where the measurements were taken were at 102.5 Hz, 1 kHz, 10 kHz, and 50 kHz, respectively. The current flow measured at 293 K was 800 μA and at 77 K it was 548 μA.

For the base-collector shorted case, the positive side of the DC power supply was connected to the base-collector shorted terminal and the negative side to the emitter. The chosen bias voltage and resistor were 3.3 V and 1 kΩ, respectively. The current flow measured at 293 K was 2.13 mA and at 77 K it was 2 mA.

In Figs. 13 and 14, the measured noise voltage of the base-emitter shorted and that of the base-collector shorted HBTs are shown. With no biasing, the noise performance of both topologies is relatively similar.

With biasing at 293 K, the base-emitter shorted HBT has a noise voltage of 36 μV/√Hz at 102.5 Hz, reducing to

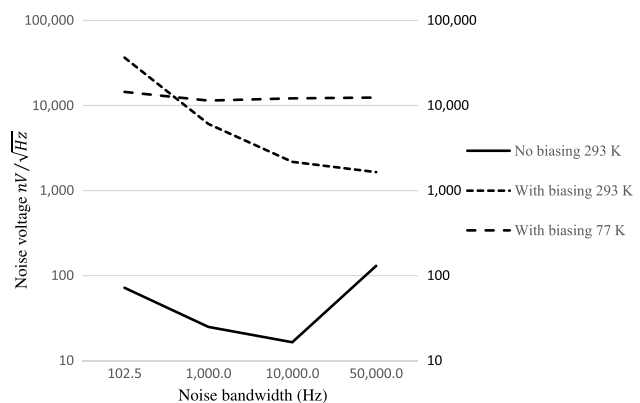


Fig. 13 Measured noise voltage of base-emitter shorted HBT.

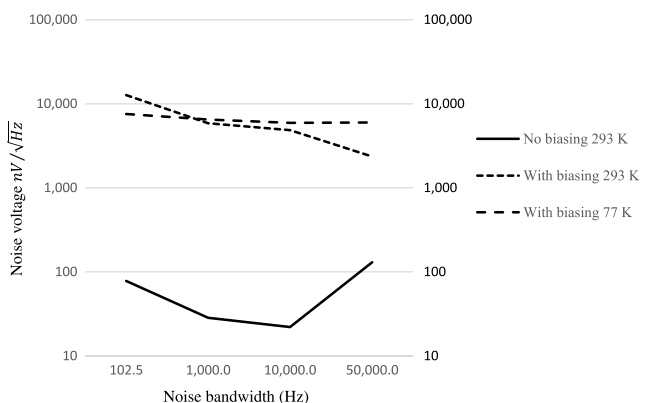


Fig. 14 Measured noise voltage of base-collector shorted HBT.

$1.515 \mu\text{V}/\sqrt{\text{Hz}}$ at 50 kHz, whereas the base-collector shorted HBT has a noise voltage of $12.6 \mu\text{V}/\sqrt{\text{Hz}}$ at 102.5 Hz, reducing to $2.228 \mu\text{V}/\sqrt{\text{Hz}}$ at 50 kHz.

With biasing at 77 K, the base-emitter shorted HBT has a noise voltage of $14.48 \mu\text{V}/\sqrt{\text{Hz}}$ at 102.5 Hz, reducing to $12.42 \mu\text{V}/\sqrt{\text{Hz}}$ at 50 kHz, whereas the base-collector shorted HBT has a noise voltage of $7.56 \mu\text{V}/\sqrt{\text{Hz}}$ at 102.5 Hz, reducing to $5.981 \mu\text{V}/\sqrt{\text{Hz}}$ at 50 kHz.

Three observations can be derived from these results. The first is that with the base-emitter shorted HBT, the noise voltage is much higher than with the base-collector shorted HBT. This is to be expected as the collector is more lightly doped than the emitter, which results in larger series resistance than the base-collector shorted HBT. In addition to this, as the base-emitter shorted HBT is effectively a $p-i-n$ diode, the lightly doped intrinsic region increases the shot noise and thermal noise. This is confirmed by the small-signal model given in Fig. 4, which only exhibits an output resistance (r_o), as opposed to the base-collector shorted configuration where the input resistance (r_π) is in parallel with the same output resistance shown in the base-emitter shorted configuration given in Fig. 5.

The second observation is that in both cases, as the device is cooled, the flicker noise becomes much flatter. This is to be expected, as current flow is severely restricted by carrier freeze-out that occurs at 77 K. Flicker noise, as measured by the K_F factor, scales inversely with the total number of carriers in noise-generating elements, according to the Hooge's theory.²⁰ This confirms that the restricted current flow results in a smaller noise voltage at lower noise frequencies.

The third observation that can be made is that for both configurations with no biasing, the noise curves are relatively similar. This is due to the thermal noise present in the diode, which is unaffected by the presence or absence of DC.

9 Summary

SiGe BiCMOS technology has emerged as a viable platform for many types of detector applications. For this paper, 77 K applications have been the main focus. The I–V, C–V, and noise parameters were measured at 293 and 77 K for two different diode-connected SiGe BiCMOS configurations. This work is an extension on a previous conference publication by the same authors.²³

For I–V measurements where reverse biasing is applied to base-emitter and base-collector shorted HBTs, the results show that little deviation occurs as the device is cooled down to 77 K. This work can be used to estimate the DR and sensitivity of diode-connected SiGe HBTs.⁸ Sensitivity is directly proportional to the current flow.

Acknowledgments

The authors would like to thank DETEK for making their facilities and equipment available to measure the required parameters.

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