WIDEBAND LOW NOISE AMPLIFIER FOR HIGHLY SENSITIVE SQUARE KILOMETRE ARRAY RECEIVERS

by

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SUMMARY

WIDEBAND LOW NOISE AMPLIFIER FOR HIGHLY SENSITIVE SQUARE KILOMETRE ARRAY RECEIVERS

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The noise figure (NF) of a low noise amplifier (LNA), which is the first active element in a receiver chain, determines the sensitivity of the receiver and its output signal-to-noise ratio (SNR). For most applications in radio frequency (RF) communications, a sub-1 dB NF is not required. However, applications in radio astronomy, such as the Square Kilometre Array (SKA), require ultra-low NF LNAs because of the extremely low magnitude of radio signals from space.

The achievement of the desired sensitivity of the SKA at an adequate cost will require original solutions in wideband LNA technology. For several decades, the technologies mostly used for LNAs in radio astronomy have been based on indium phosphide (InP) and gallium arsenide (GaAs). Extremely low NFs (lower than 0.1 dB) can be achieved with InP transistors at cryogenic temperatures [1]. InP and GaAs semiconductors achieve high unity gain frequency, very low noise and offer passives with good performance. However, InP

and GaAs processes have a low integration level, high power consumption and are expensive [1]. Therefore, InP and GaAs devices are not adequate for the SKA and silicon-germanium heterojunction bipolar transistor (SiGe HBT) and CMOS technologies are possible alternatives [1]. The possible alternatives suggest a research gap in the field of low noise RF receivers, which is the topic of this thesis.

The inductively degenerated common-source and common-emitter configurations were identified to be the preferred transistor configurations. The cascode configuration was chosen for the LNA topology, owing to its frequency response and to the low coupling between the output and the input. From the literature, the expected NF for an LNA for the SKA is 0.2 dB. However, such requirement being strongly related to the semiconductor process available for fabrication, the requirement was relaxed and it was proposed to develop a design methodology allowing for achieving the minimum possible NF with possibly a sub-1 dB NF. The preferred LNA topology having been identified, the primary research question was formulated as follows: "How can the inductively degenerated common-source/emitter LNA topology be improved to achieve a sub-1 dB NF for highly sensitive differential wideband LNA for the SKA with on-chip inductors at room temperature?" A secondary research question was formulated as follows: "How can semiconductor technologies, passives optimisation, layout and packaging techniques be combined with the adequate LNA topology and design methodology to achieve the required noise performance for the SKA?" The hypothesis of the research was formulated as follows: "If the NF and the input matching of an inductively degenerated common-source or common-emitter cascode LNA with on-chip inductors are optimised, using an improved methodology coupled to enhanced passives and to an adequate semiconductor technology and packaging, a sub-1 dB NF can be achieved on a wideband LNA for the SKA."

The size of transistors remaining equal, the SiGe HBT technology is superior to the CMOS technology in terms of frequency response, noise performance and power gain, which are performance parameters the optimisation of which is generally desired in RF applications. Taking this into account, the SiGe HBT technology was selected for this thesis.

A research methodology was proposed and a theoretical analysis was done in order to address the research questions. Results from previous studies show that the noise factor of a common-emitter transistor can be minimised through the direct current biasing of the

transistor and the matching of the optimum noise impedance of the amplifier to the impedance of the source. The same results indicate that the noise factor of an integrated common-emitter transistor increases with the width of the emitter, but is weakly related to the length of the emitter and that the optimum source impedance is inversely proportional to the length of the emitter. In this work, it was demonstrated that when identical transistors are connected in parallel, the minimum possible noise factor of the resulting circuit is unchanged, while its optimum source impedance is inversely proportional to the number of transistors in parallel [2]. Therefore, noise matching could be achieved without affecting the noise performance, by changing the length of the emitter or by connecting several identical transistors in parallel [2]. For optimum power transfer from the source to the amplifier, an inductively degenerated common-emitter transistor with an inductor in the base signal path, was proposed. The additional inductors do not significantly affect the noise matching conditions and noise and power matching conditions remain valid when such a circuit is used in a cascode configuration.

From this work, the narrow bandwidth of the inductively degenerated common-emitter cascode amplifier was extended by means of an innovative technique that uses the base-collector capacitance to implement coupled resonant circuits with minimum impact on the NF. An output matching network was investigated and it was proposed to use a fourth order Butterworth approximation; the transfer of RF power from the LNA to a 50 Ω load was optimised by a MATLAB™ script.

Simulations have shown that the NF was significantly impaired when the base inductor was on-chip, contrary to an external high Q inductor, impeding the achievement of a sub-1 dB NF. The use of an on-chip balun to provide a differential input would also result in a significant increase of the NF, due to the low Q of on-chip inductors. The duplication of a single-ended LNA to provide a differential input, would equally impair the NF and complicate the attainment of a sub-1 dB NF. For these reasons, all related to the low performance of on-chip inductors and to the duplication of noise sources when a single-ended LNA is duplicated, the scope of this research was limited to a single-ended LNA with an external high Q base inductor. For further research, it was proposed to test the initial hypothesis of this research on SiGe HBT technologies having an emitter width smaller than 0.13 μm, such as the Global Foundries 90 nm SiGe HBT and the STMicroelectronics 55 nm BiCMOS055.

A design methodology was derived from the theoretical analysis, which was validated by simulation and measurements. The theoretical analysis has allowed responding to the primary research question, for single-ended LNAs with an external base inductor. The LNA prototype that was fabricated for measurements required for the validation of the research hypothesis, was a 1.3 mm^2 single-ended device fabricated in the 0.13 µm IBM 8HP process. A printed circuit board was fabricated to hold two packaged LNAs and their peripheral components. Measurements have shown a bias defect in one prototype and a large signal attenuation in conjunction with parasitic coupling between the signal output and input for the second prototype. The parasitic coupling could possibly result from mutual couplings between relatively long bonding wires and from the layout. The large attenuation could be explained by a short circuit of the output signal by a MOS transistor used as an active resistor in the output circuitry. Hence, the NF of the fabricated ICs could not be measured to enable response to the secondary research question and to validate the research hypothesis by measurements. However, the design methodology could be validated by simulation.

This thesis has analysed the dependence of the NF on the operating frequency, transistor biasing, sizing and paralleling for an inductively degenerated cascode amplifier and derived a design methodology that achieves a NF that is close to the minimum achievable for the semiconductor process of fabrication. A bandwidth extension technique with minimum impact on the NF was developed for the SiGe HBT based cascode amplifier. Finally, an output broadband matching technique was proposed. The proposed methodology allows for designing a wideband LNA with a NF close to the minimum achievable one. Such a single-ended LNA is cost-effective, can achieve a sub-1 dB NF at room temperature, depending on the fabrication process, and can be used in applications for radio astronomy, such as the SKA.

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Enfin j'ai une pensée particulière pour mon frère, Berthuin, disparu tragiquement et à qui je voudrais adresser mes remerciements dans l'espoir qu'il m'entend, là où son âme, enfin libre de tourments et souffrances dont il a été infligés, se repose. Dès mon enfance, il avait suscité mon intérêt dans la compréhension des phénomènes électriques, des techniques de réception radio, de démodulation et d'amplification et était ainsi parvenu à créer une vocation quoiqu'il s'orienta lui-même vers la médecine par la suite. Je lui dois aussi beaucoup d'autres choses, entre autres mon intérêt pour la musique et ma première guitare. Je pense aussi à mon autre frère, Guillaume, disparu pendant que je travaillais encore sur cette thèse. Ayant aussi été exposé très tôt aux techniques de l'électronique, il avait fait des études d'ingénieur en électronique et en avait fait sa profession.

"Applying the calculus concept of limits, the specialist gets to know more and more about less and less until, in the limit, he retires, knowing everything about nothing. The generalist learns less and less about more and more until, in the limit, he retires, knowing nothing about everything. Neither is quite the ideal life."

Lawrence J. Kamm

LIST OF ABBREVIATIONS

AA	Aperture Array
ADE	Analog Design Environment
AC	Alternating Current
ADS	Advanced Design System (Agilent EEsof)
AlGaAs	Aluminium Gallium Arsenide
BiCMOS	Bipolar Complementary Metal-oxide Semiconductor
BJT	Bipolar Junction Transistor
CAD	Computer-aided Design
CB	Common-Base
CE	Common-Emitter
CC	Common-Collector
CG	Common-Gate
CMOS	Complementary Metal-oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
dB	Decibel
DC	Direct Current
DRC	Design Rule Check
FET	Field Effect Transistor
GaAs	Gallium Arsenide
Ge	Germanium
GHz	Giga Hertz
GPS	Global Positioning System
GSM	Global System for Mobile Communications
G-R	Generation Recombination

HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IDCE	Inductively Degenerated Common-Emitter
IDCS	Inductively Degenerated Common-source
IP2	Second-order Intercept Point
IP3	Third-order Intercept Point
InGaAsP	Indium Gallium Arsenic Phosphide
InP	Indium Phosphide
JFET	Junction Field Effect Transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LNA	Low Noise Amplifier
MC	Monte Carlo
MEMS	Microelectromechanical Systems
MIM	Metal Insulator Metal
MHz	Mega Hertz
MESFET	Metal Semiconductor Field Effect Transistor
MHEMT	Metamorphic High Electron Mobility Transistor
MMIC	Monolithic Microwave Integrated Circuit
mm-wave	Millimetre-wave
MOS	Metal Oxide Semiconductor
MOSFET	Metal-oxide-semiconductor Field-effect Transistor
MOSIS	MOS Implementation Service
NDA	Non-disclosure agreement
NF	Noise Figure
OPAR	L'observatoire de Paris, Meudon (Paris Observatory)

PAF	Phased Array Feed
PCB	Printed Circuit Board
PDF	Probability Density Function
pHEMT	Pseudomorphic High Electron Mobility Transistor
PSD	Power Spectral Density
Q	Quality Factor
QFN	Quad Flat No-lead (package)
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RFT	Real Frequency Technique
RMS	Root Mean Square
S	Scattering
SFDR	Spurious-free Dynamic Range
Si	Silicon
SiGe	Silicon Germanium
SGP	SPICE Gummel-Poon
SKA	Square Kilometre Array
SNR	Signal-to-noise Ratio
SOI	Silicon on Insulator
UWB	Ultra-wideband
VNA	Vector Network Analyser
VLA	Very Large Array

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CHAPTER 1 INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Context of the problem

Modern wireless broadband communication systems require wide frequency bandwidths and weak radio frequency (RF) signals because of the increased usage of wireless devices and the demand for data traffic. They require sensitive receivers to enable the detection and resolution of weak signals. The sensitivity of receivers is achieved by the use of a low noise amplifier (LNA). The noise figure (NF) of the LNA, which is the first active element in the receiver chain, controls the sensitivity of the receiver and its output signal-to-noise ratio (SNR).

For most applications in RF communications, LNAs with sub-1 dB NF are not generally required. The typical values of the NF for the global positioning system (GPS) and for the global system for mobile communications (GSM) are 1 dB [3] and 2 dB [4], respectively. For applications in radio astronomy, LNAs with ultra-low NF are required because of the extremely low magnitude of radio signals from space. The design of ultra-low noise amplifiers differs from that of classical LNAs, as the NF of the LNA gets close to the NF of some of its components. For ultra-low noise amplifiers, sub-1 dB NF performance can only be achieved by a judicious choice of transistor technology and size, LNA topology, passive components, impedance matching and minimum noise matching techniques, RF shielding and ground path techniques. The design requirements are more stringent when on-chip inductors are used because of the low quality factor and noise performance of on-chip inductors.

The Square Kilometre Array (SKA) is an international programme initiated in the 1990s with the objective to increase by an order of magnitude of two, the sensitivity of existing radio telescopes. For several decades, the sensitivity and resolution of radio telescopes have improved, with an increase in their effective aperture, through the development of semiconductor technologies and with innovative designs. The improvement of the effective aperture is achieved by increasing the size of the antenna of the radio telescope or by coupling several small antennas. Interferometry techniques are used to synthesise a large effective aperture area from several coupled antennas. Astronomers have recognised that the only avenue left to improve radio telescopes' sensitivity is increasing their effective area. Once the coupling of several antennas has increased the effective area of a radio telescope, its resolution is related to the maximum distance between its receiving elements.

The SKA will have a collecting area of a square kilometre, hence the designation. The collecting area will consist of a large number of receiving elements, in the order of several millions: each element will be connected to an LNA as the first element of the receiver chain. LNAs with differential inputs will be required and differential input impedances of 50, 150 and 300 Ω are expected. It is expected that after the completion of all phases of the SKA project, the number of LNAs will be over 37 million [5]. Therefore, a low-cost integrated receiver is a prerequisite for the feasibility of the SKA.

The SKA will cover frequencies from 70 MHz to 25 GHz. Several antenna technologies will be required for this ultra-wide frequency coverage in order to attain the efficiency and sensitivity requirements of the SKA [6]. In order to spread costs and to start operating before its full completion, the SKA will be implemented in three phases. During Phase 1, 15% to 20% of the array will be deployed at low-band and mid-band frequencies. The full collecting area of the SKA at low and mid-band frequencies from 70 MHz to 10 GHz will be deployed in Phase 2. Low and mid-band frequencies of the SKA are divided in three frequency bands: SKA low band from 70 MHz to 450 MHz, SKA mid-band from 0.3 GHz to 1.4 GHz, and SKA mid-band from 1.4 GHz to 10 GHz. Phase 3 of the SKA will extend the coverage of the SKA to 25 GHz and more. This study will address the frequency band of 0.3 GHz to 1.4 GHz. The main scientific projects that will use the mid-band will involve

research on first galaxies and black holes. The frequency band of 700 MHz to 1400 MHz from the SKA mid-band can be used to observe the emissions of neutral hydrogen from galaxies [7] and determine the Equation of State of the Universe in Cosmology.

One of the SKA areas of research that is critical to the success of the project is related to LNA technology for sub-1 dB NF receivers. The achievement of the desired sensitivity of the SKA at effective cost will require major improvements in wideband LNA technology [1]. For several decades, the technologies mostly used for LNAs in radio astronomy have been based on indium phosphide (InP) and gallium arsenide (GaAs). Extremely low NFs (lower than 0.1 dB) can be achieved with InP transistors at cryogenic temperatures [1]. InP and GaAs semiconductors achieve high unity gain frequency, f_T, very low noise and offer passives with good performance due to their semi-insulating substrate. However, InP and GaAs processes have a low integration level and high power consumption and remain expensive. InP and GaAs devices are not adequate for the SKA [1]. Silicon-germanium heterojunction bipolar transistor (SiGe HBT) and complementary metal-oxide semiconductor (CMOS) technologies are possible alternatives owing to their improved performance, their cost and large design and fabrication infrastructure [1].

1.1.2 Research gap

High sensitivity integrated receivers that can be used for the SKA require LNAs with sufficient gain, adequate linearity and impedance matching and an NF that is better than 20 K. The LNA must operate at ambient temperature rather than cryogenic temperatures to reduce the cost of cryogenic coolers. Also, the LNA must use low-cost transistor technologies with low power consumption because of the large number of receiver arrays. The variation of the performance of the LNA with the ambient temperature is also a critical issue that needs to be investigated. The main sources of noise in bipolar transistors are the base and collector shot noise components ($\overline{i_b^2} = 2qI_B\Delta f$ and $\overline{i_c^2} = 2qI_C\Delta f$) and the base resistance thermal noise ($4kTr_b$). For long-channel MOS transistors, the main sources of noise are the drain-source current noise comprising thermal noise and flicker noise

($\overline{i_d^2} = 4kT\left(\frac{2}{3}g_m\right)\Delta f + K\frac{I_D^a}{f}\Delta f$) and the gate leakage current shot noise ($\overline{i_g^2} = 2qI_G\Delta f$). The noise generated by both bipolar and MOS transistors varies with temperature.

In order to evaluate the noise performance of possible SKA receivers, semiconductors from low noise foundries based on InP, GaAs, SiGe and silicon (Si) using a pseudomorphic high electron mobility transistor (pHEMT), metamorphic high electron mobility transistor (mHEMT), HBT and CMOS technologies have been used to design LNA prototypes for the SKA. The summary of the performance of LNAs that have been designed is provided in Chapter 2, Table 2.2.

In [8], an extremely low NF of 0.2 dB (14K) has been achieved at room temperature from 800 MHz to 1400 MHz using 90 nm CMOS technology. The measured return loss (S_{11}) is better than -11 dB, the gain (S_{21}) into a load of 50 Ω is better than 17 dB, the output 1 dB compression point is 2 dBm, the output IP2 is 22 dBm and the output IP3 is 12 dBm. From the literature review, the NF of the LNA in [8] is the lowest attained by a wideband CMOS LNA at room temperature using power matched optimisation.

The wideband LNA in [8] represented in Figure 1.1 is a cascode amplifier whose first stage is an inductively degenerated common-source topology. The design demonstrates that sub-1 dB NFs can be achieved with CMOS technology at ambient temperature. However, the gate inductor L_G, the biasing inductor L_{BIAS} and the RF choke L_{DC} in Figure 1.1 are all external, on-chip inductor quality factors being too low. The quality factor Q of the external inductor L_G is closer to 100 while for L_{BIAS} and L_{DC}, Q is greater than 60. Because of losses in on-chip passives caused by parasitic resistances and capacitances and of frequency-dependent losses caused by the skin effect and Eddy currents in semi-conductive substrates, the noise performance of the LNA reported in [8] cannot be achieved with on-chip passives. It is then desired to investigate if with superior semi-conductor technology such as SiGe BiCMOS, a sub-1 dB NF can be achieved for an ultra-low noise LNA for the SKA with on-chip passives. It is also suggested to evaluate the use

of microelectromechanical system (MEMS) devices for the gate inductor, biasing and for choke inductors to the noise performance of the LNA.

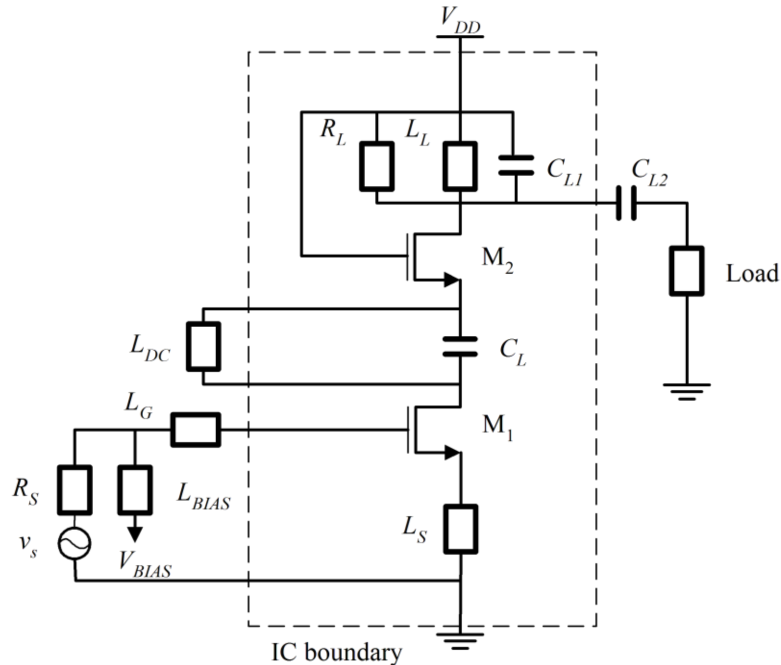


Figure 1.1. Sub-1 dB wideband LNA. Adapted from [8], © 2007 IEEE.

The LNA in [8] is a single-ended device, while some receivers of the SKA will be equipped with differentially fed antennas. A balun can be used to feed the signal from the antenna to a single-ended LNA. Baluns introduce extra loss and the contribution of passive baluns to noise can be higher than 16K [9], degrading the performance of the receiver. An alternative to the balun is the use of a differential LNA, generally achieved by the duplication of single-ended LNAs. The NF is better for single-ended devices than for differential devices owing to the duplication of noise sources and to the difficulty of attaining a low common mode rejection ratio (CMRR). However, the differential topology allows better rejection of on-chip interference and alleviates issues due to parasitic source degeneration, such as bondwires. In [10], the NF of a differential LNA is found to be 3 dB higher than the NF of a singled-ended LNA. The evaluation of topologies and optimisation methodologies for on-chip baluns for highly sensitive wideband single-ended LNAs and of differential LNAs is required in order to propose the appropriate design methodology for SKA receivers.

1.2 RESEARCH OBJECTIVE AND QUESTIONS

This research aims at developing noise and impedance matching optimisation techniques for highly sensitive wideband LNAs in CMOS or SiGe BiCMOS technology at room temperature. The research will assess the feasibility of a fully integrated wideband differential sub-1 dB NF LNA at room temperature for the SKA. Chapter 2 of the study will comprise a review of LNA topologies and their noise models for SiGe BiCMOS and possibly for CMOS technologies. A topology for minimum NF in the mid-frequency band of the SKA will be proposed. Minimum noise and wideband impedance matching techniques for the adequate topology will be developed. It is desired to investigate topologies for ultra-low noise differential LNAs. The study will comprise the development of a design methodology and associated techniques with validation by simulation, circuit design, fabrication and measurements.

The primary research question is formulated as follows: "How can the inductively degenerated common-source/emitter LNA topology be improved to achieve a sub-1 dB NF for a highly sensitive differential wideband LNA for the SKA with on-chip inductors at room temperature?"

The following secondary research question is proposed: "How can semiconductor technologies, passives optimisation, layout and packaging techniques be combined with the adequate LNA topology and design methodology to achieve the required noise performance for the SKA?"

1.3 HYPOTHESIS AND APPROACH

1.3.1 Research hypothesis

The hypothesis that this research proposes to test is formulated as follows: *If the NF and the input matching of an inductively degenerated common-source or common-emitter cascode LNA with on-chip inductors are optimised using an improved methodology*

coupled to enhanced passives and to an adequate semiconductor technology and packaging, a sub-1 dB NF can be achieved on a wideband LNA for the SKA.

1.3.2 Research approach

The initial step of the research will entail the furthering of the literature survey on minimum NF for CMOS and SiGe BiCMOS technologies. A thorough literature and theoretical study will be done on single-ended LNA topologies, on their noise models and on impedance and minimum noise-matching techniques. The selection of the adequate topology may be difficult because of the lack of a structured design process for LNAs. Generally, engineers rely on their experience, insight and creativity. Inductorless LNA topologies and topologies with noise cancellation will be investigated. The design in [8] is of major interest because it is the only CMOS wideband LNA known to achieve the lowest reported NF (0.2 dB) at room temperature. With the on-chip gate inductor L_G, biasing inductor L_{BIAS} and choke in [8], the applicability of [8] to SiGe BiCMOS will be studied.

A study of on-chip inductors, of baluns on Si and of on-chip RF shielding and RF ground path techniques will be done. The objective will be to investigate factors that affect the performance of on-chip inductors and baluns in order to select and possibly improve the type of inductor and balun that may be used to achieve the objectives of the research. Mathematical models will be used to determine parameters that affect performance and the extent to which performance is affected by various parameters for various LNA topologies. The models will be used to investigate the impact of semiconductor technology, transistors and passive components on the performance of the LNA.

A comparative study on the minimum NF that can be achieved by possible wideband topologies in MOS and SiGe technologies will be done. The comparative study will allow selection of the adequate LNA topology, determination of the expected NF and confirmation of SiGe as the semiconductor technology of choice.

Two solutions are possible for differential inputs. The first solution uses a balun at the input of the LNA and the second solution entails a differential LNA. The differential LNA is based on the duplication of an optimised single-ended LNA. The performance of the optimised LNA using a balun for differential inputs will be investigated using simulation tools. The NF of the LNA will be compared to the NF of the differential LNA and the best configuration will be proposed.

Optimisation techniques for noise and impedance matching will be investigated and developed. They will provide a fast and efficient means of selecting inductor values, transistor sizes and bias voltage for the achievement of minimum noise and wideband input matching.

The optimum layout of the transistors of the LNA will be investigated. The work published in [11] shows that circuit performance can be improved by the modification of the layout of transistors. Packaging options for very low noise amplifiers will be evaluated.

The research hypothesis will be tested by design, simulation, fabrication and measurement of the fabricated LNA performance. Layout techniques will be used to shield RF signals from substrate noise. Upon validation of the research hypothesis, a design methodology will be developed. The proposed research methodology is depicted in Figure 1.2.

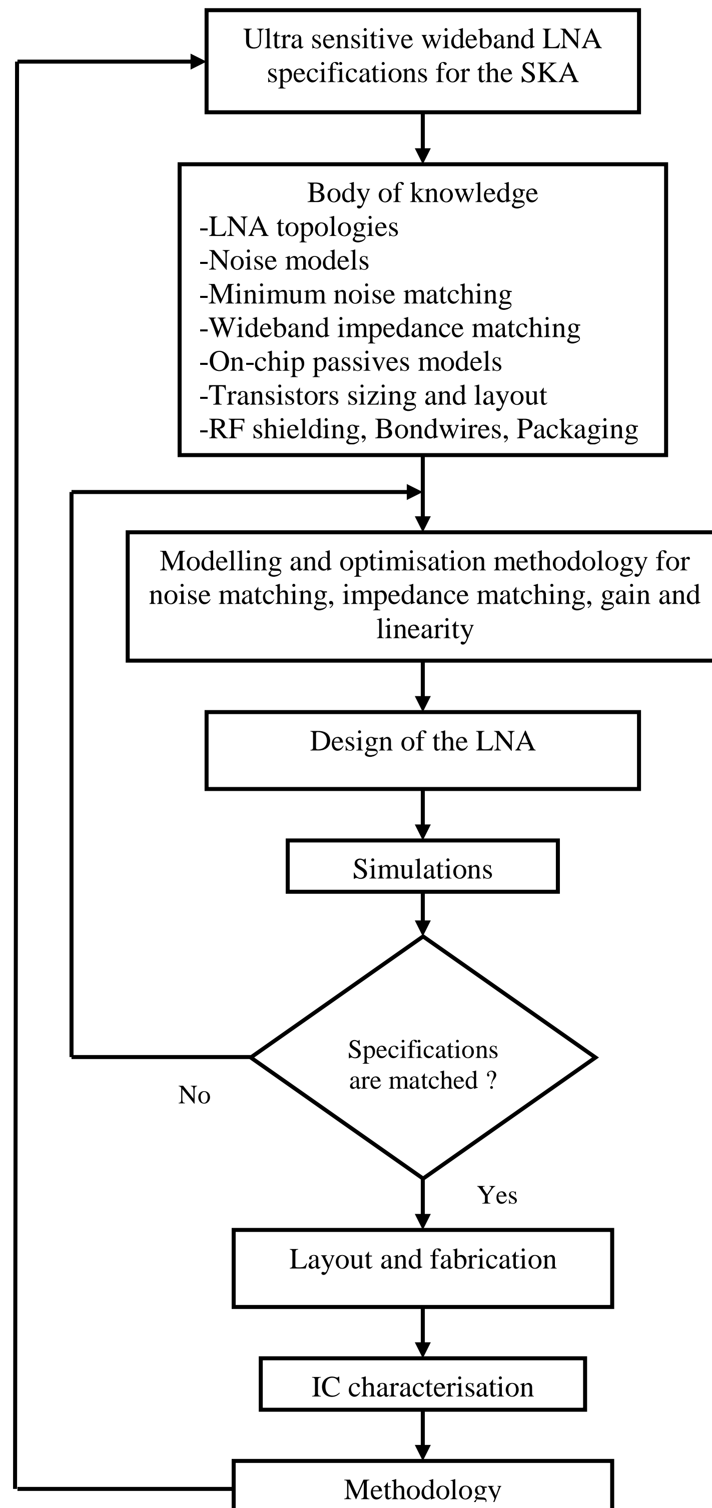


Figure 1.2. Flow diagram of the research methodology.

1.4 RESEARCH GOALS

This research aims at developing an optimisation methodology for noise and impedance matching for highly sensitive wideband LNAs in CMOS or SiGe BiCMOS at room temperature for the SKA using on-chip inductors. The research also aims at possibly improving the quality of on-chip passives and the NF of differential LNAs for ultra-low noise LNAs for the SKA.

1.5 RESEARCH CONTRIBUTION

The methodology and techniques developed will provide fast and optimised methods of selecting bias voltages, transistor size, inductors and balun values, types and sizes. The research is expected to improve or adapt optimisation techniques in [8] to SiGe BiCMOS. The methodology and models developed will be applied to the design of a state-of-the-art CMOS or SiGe BiCMOS LNA for the SKA.

1.6 PUBLICATIONS RESULTING FROM THIS RESEARCH

The following papers have resulted from the research carried out during this work:

- A. Bimana, S. Sinha, “Impact of SiGe parameters to the performance of LNAs for highly sensitive SKA receivers,” 23th Conference Radioelektronika Pardubice, Czech Republic (2013), pp. 50-54.

- A. Bimana and S. Sinha, "Increasing the bandwidth of a SiGe HBT LNA with Minimum Impact on Noise Figure," *Microwave and Optical Technology Letters* (Wiley), Vol. 58, No. 8, Aug. 2016, pp. 1937-1944.

1.7 OVERVIEW OF STUDY

This thesis is structured as follows:

Chapter 1 presents the context of the research topic and outlines the research gap. Research avenues that can possibly address the gap are identified; they allow deriving research objectives, questions, hypothesis and a preliminary schematic representation of the research methodology.

Chapter 2 provides a literature study of the SKA, of LNAs, of their topologies and their performance metrics. Technologies for SiGe HBTs and for on-chip passives are presented. An initial review of electronic noise and NF optimisation techniques for LNAs is given. Finally, the chapter provides the specifications of an LNA for the SKA, in the frequency band of 0.3 GHz to 1.4 GHz.

Chapter 3 is dedicated to the research methodology. Chapter 4 provides the mathematical analysis that allows relating the noise performance of the proposed LNA topology to its active and passive components. Active components being major contributors to the NF of an amplifier, the impact of transistor parameters on noise performance is analysed. The analysis justifies the preferred LNA topology and allows identification of the requirements for an optimal NF and for optimal RF power transfer from the signal source to the LNA. An analysis of noise performance and transistor geometry determines the desired transistor sizing for minimum NF. Similarly, an analysis of a SiGe HBT based cascode LNA demonstrates that the bandwidth of a narrow-band inductively degenerated cascode amplifier can be improved considerably, with negligible impact on NF. The chapter proposes an output impedance matching network that is based on a fourth-order Butterworth filter. The on-chip filter is optimised by a MATLAB™ script. Finally, a design methodology is derived from the studies performed in this chapter.

Chapter 5 describes the design of the LNA and presents simulation results. The determination of the values of the elements of the LNA circuit, including those of the bias

circuit, is presented in this chapter. Performance metrics of the LNA, such as NF, gain, S_{11}, S_{22}, S_{21} and IIP3, are presented. The impact of process variations and device mismatches on the performance of the chip is evaluated by corner and Monte Carlo simulations.

The layout, the packaging of the integrated circuit (IC) and the printed circuit board (PCB) are presented in Chapter 6. Because some components of the LNA are off-chip, a PCB is used to support and connect the IC to the external passive components. Chapter 7 provides the measurement setup, results and their discussion. The conclusion and possible future work are presented in Chapter 8.

A comparison between performance metrics of similar LNAs for radio astronomy and the impact of process, temperature, integration and bandwidth on performance is shown in Table 1.1 [2].

Table 1.1. Performance comparison with similar reported LNA designs. Adapted from [2], with permission.

Property	**[12]**	**[13]**	**[14]**	**[15]**	**[16]**	**This work (simulation)**
Technology (µm)	0.090 CMOS	0.130 IBM BiCMOS8HP	MMIC 0.130 IBM BiCMOS8HP	1, InGaAs/InAlAs/Inp HEMT	MIC Discrete pHEMT	0.130 IBM BiCMOS8HP
Frequency (GHz)	0.7 -1.4	0.7-3	0.1-5	1-3	0.02-1	0.3-1.4
NF (dB)	0.35	< 0.1	1	0.4	0.55	0.46
S_{11} (dB)	< -11	< 0	-8.4 @ 1.4 GHz	8.2 @ 1.4 GHz	< -4.5	< -10
S_{21} (dB)	20.5-16.3	32.8	28.3 @ 1.4 GHz	-16.5 @ 1.4 GHz	> 36	17.8 max
S_{22} (dB)	< -8	< -12	-16 @ 1.4 GHz	-12.5	< -10	< -10
Gain (dB)	17	28	27	30	30	18
Supply (V)	1	0.6	-	1.8	1	2.2
Supply (mA)	45	7.1	-	47	25	6
Source resistance	50	50	50	50	50	50
Single/Balan-ced Ended	S.E.	S.E.	S.E.	S.E.	S.E.	S.E.
Temperature (K)	Room	Cryogenic (15)	Room	Room	Room	Room
Area /λ^2	4E+08	-	-	Results from simulation	-	3.17E+08
External coils	2	3	5 bondwires	0	-	2
Publication year	2007	2007	2009	2010	2014	2016

CHAPTER 2 LITERATURE STUDY

2.1 INTRODUCTION

An extensive review of the literature on the SKA, LNAs, their topologies, their performance metrics, relevant semiconductor active technologies, on-chip inductors and electronic noise is provided in this chapter. The review allows one to determine the specifications of an LNA for the SKA in the frequency band of 0.3 GHz to 1.4 GHz, to identify the preferred topology and related technologies and design techniques.

2.2 THE SKA

Astronomers need to look 10 to 20 billion years back in order to learn about the early universe. They need to study radiations emitted by objects that are some billion light-years away from the earth, such as quasars at the childhood of the universe. Such radiations are extremely weak and their detection requires highly sensitive radio telescopes. A highly sensitive radio telescope requires a large signal-receiving area. The SKA, still under construction, will become the radio telescope with the largest signal-collecting area.

2.2.1 The scientific case of the SKA

Five research areas in radio astronomy are limited by the performance of existing radio telescopes. These areas (The cradle of life, Strong-field gravity tests using pulsars and black holes, The origin and evolution of cosmic magnetism, Galaxy evolution and cosmology, Probing the dark ages) are developed in [17] and have provided research

direction for the SKA. Phase 1 of the SKA, expected to start in 2016, is driven by the following subset of research directions [18]:

- The history of hydrogen from the dark ages.
- The test of gravity theories by detection of pulsars, the study of gravitational waves and the investigation of supra-nuclear matter.

Phase 2 of the SKA will allow improvement of the sensitivity, the timing resolution, the resolution and the sky observable area of Phase 1. The increased resolution and observable area will allow further investigations into the origin of the magnetic field. With improved sensitivity, the SKA is expected to be able to probe all standard and millisecond pulsars in our galaxy, increasing the probability to find the first pulsar-black hole system. The high-frequency end of the SKA in Phase 2 will allow scientists to probe the distribution of organic molecules and to study the origin of life.

2.2.2 Requirements of the SKA

The technical requirements of the SKA have been derived from its science drivers. The frequency bands of the SKA are mapped to frequencies of signals that science will study to achieve the five SKA science drivers and satisfy the technological requirements of SKA receivers. Three frequency bands will be used [19]:

- Low band: 70 – 450 MHz.
- Mid-band: 0.3 – 10 GHz.
- High band: 5 – 25 GHz.

The specifications of the SKA have been evolving; initially low frequency aperture arrays were expected for the low band while for the mid-band, aperture arrays from 0.3 to 1.4 GHz and dish-based arrays from 1.2 to 10 GHz were to be used. Following the revision in [19], it appears that, in order to achieve the major science goals of the SKA setup in Phase 1 (i.e. role of neutral hydrogen in the universe and detection of pulsars to test

fundamental physics), a low-frequency sparse aperture array will be used from 70 to 450 MHz and 15-metre antennas using single-pixel feeds are expected from 0.45 to 3 GHz. Some variations are however still found in the literature. In [20], reference is made to 70 to 300 MHz for the low band, 0.3 to 3 GHz for the mid-band and 3 to 25 GHz for the high band.

The sensitivity of a radio telescope is determined by the ratio of the total effective collecting area (A_e) to the noise temperature of the system (T_{sys}) [6], [21]. The strength of the weakest signal that the SKA can detect in a given time is proportional to T_{sys}/A_e. A_e/T_{sys}, is expected to be close to 20 000 m^2/K. The time of observation required to detect a source within the SKA field of view (FoV) is proportional to $(T_{sys}/A_e)^2$. The FoV is the solid angle where the sensitivity of the antennas is greater than half of the maximum sensitivity. The SKA will achieve a FoV of 1 deg^2 at 1.4 GHz with an angular resolution of 0.1 arcsec [17].

The low-frequency aperture array sub-system will achieve sensitivity (A_e/T_{sys}) of up to 2000 m^2/K. Some of the collecting elements of the array will be located up to 100 km from the core, which will condense most of the elements [22]. Each collecting element of the array is an antenna that will require an LNA as the first element of the receiver chain. LNAs with differential inputs will be required and differential input impedances of 50, 150 and 300 Ω are expected.

2.2.3 The impact of sensitivity on noise figure

The sensitivity of a radio telescope is determined by the minimum flux, ΔS, that the radio telescope can detect. For a radio telescope with a single antenna, ΔS is proportional to $T_{sys}/A_e\sqrt{B\tau}$, where T_{sys} is the noise temperature of the single antenna, A_e is its effective area, B is the bandwidth of the system and τ is the duration of the observation [23], [24], [25]. For antenna arrays, ΔS remains proportional to $T_{sys}/A_e\sqrt{B\tau}$, for a large number N of antennas in the array [26]. In such a case, A_e is the sum of the effective areas of each antenna in the array and is the effective area of the array. T_{sys} is the total noise temperature of the system. The sensitivity of a radio telescope, such as the SKA, increases when ΔS

decreases and is proportional to A_e/T_{sys}. Therefore, there are two ways of improving the sensitivity of radio telescopes: by decreasing T_{sys} and/or by increasing A_e. In today's radio telescopes, the decrease of T_{sys} has almost reached the limit for centimetre wavelengths. Therefore, a major improvement in sensitivity at an effective cost can only be achieved by increasing the radio telescope's signal-collecting area and by achieving a system with optimal noise in a cost-effective way.

The system noise of a radio telescope system is the sum of various noise sources as expressed by (2.1):

$$T_{sys} = T_{rx} + T_{cal} + T_{loss} + T_{spill} + T_{sky} + T_{bg} \quad (2.1)$$

where T_{rx} is the receiver noise temperature, T_{cal} is the contribution of calibration signals, T_{loss} is the noise contribution due to losses in the feed, T_{spill} is the contribution of earth radiation, T_{sky} is the noise contribution from the atmosphere and T_{bg} is the noise contribution from microwave and galactic backgrounds [27]. In practical cases, the contribution of the noise temperature of the radio source that is being observed, T_a, is neglected because $T_{sys} >> T_a$.

In order to achieve the scientific requirements of the SKA, a value of 2×10^4 m^2/K is required for A_e/T_{sys} at 1.4 GHz in addition to a frequency coverage of 0.2 GHz to 20 GHz [28]. In [27], a basic model suggests a value of 50 K for T_{sys}. The model assumes a collecting area of 1 km^2 and a single type of antenna and receiver. Noise models for T_{sky} and T_{bg} are based on [29] and [30]. Other sources of noise in T_{sys} are interpolated from data on the VLA radio telescope in New Mexico from [26]. When calculating T_{rx} by subtracting all other noise contributions from T_{sys}, it is found that the upper limit of T_{rx} at 1.4 GHz is 19 K (0.28 dB). The main contribution to the receiver noise temperature T_{rx} comes from the LNA. Typically, 30% of the total noise budget of the SKA is provided by the LNA [9]. The approximation of the SKA receiver noise temperature from the basic model is close to the 16 K noise temperature allotted to the LNA [9]. The target of a noise temperature of 16 K (0.23 dB) for the LNA is derived from the SKA noise budget in [21], corresponding to a system noise temperature of 40 K (0.55 dB). More stringent requirements are found

in [6]. In [6] the typical NF of the LNA is expected to be lower than 0.2 dB, which is equivalent to 14 K noise temperature. However, such a target is difficult to reach. Recent specifications that have been emerging propose 20 K (0.29 dB) for noise temperature [5] of the LNA of the SKA. According to [5], the expected gain of the LNA is 30 dB and the required power consumption is 30 mW.

2.2.4 LNA for the SKA

The choice of technologies for SKA receivers poses several challenges due to the large bandwidth requirement, the exceptional sensitivity and the very large number of receivers affecting the overall cost of the system. The main challenge in the receiver is to attain an NF close to 0.29 dB for the LNA. In order to obtain such a performance, the analysis of the impact of semiconductor processes and other factors related to the performance of LNAs is required. Such factors include the degree of integration, the cooling of receivers, the use of single-ended or differential LNAs, the input impedance, the performance of passives and LNA topologies.

2.2.4.1 Semiconductor processes

Possible transistor technologies for SKA receivers are from low-noise foundries based on GaAs, on mHEMT, pHEMT, SiGe HBTs, CMOS and InP devices. However, only a few processes have the potential to cater for the SKA requirements because of cost constraints.

Over the past decades, HEMT has been the primary choice for low-noise technology. HEMT devices have high transconductance (g_m) and high unity gain frequency (f_T). They also have extraordinarily low NF and parasitic resistance. The NF of the HEMT LNA is dramatically reduced with InP pHEMT and GaAs mHEMT transistors. InP and GaAs are the most widely used technologies for LNAs in radio astronomy. At cryogenic temperatures, a noise factor of less than 0.1 dB is often achieved with InP transistors [21]. Despite offering a high f_T coupled with high noise performance, InP and GaAs processes have a low integration level, high power consumption and remain expensive. They are not suited to the integration of complex digital logic.

The SiGe HBT process combines the performance of transistors in the III-V technologies (e.g. GaAs and InP) with the maturity, integration level and cost of Si fabrication. SiGe HBT devices of an earlier generation may have an f_T in excess of 50 GHz and an NF of less than 0.7 dB [31]. In [31], the NF of a monolithic microwave integrated circuit (MMIC) LNA operating from 0.5 GHz to 2 GHz is 0.66 dB (48 K) and passives have a quality factor of 12. For a better NF, low-loss passives are required. A combination of SiGe HBT and BiCMOS (SiGe BiCMOS) can be used for on-chip systems. SiGe BiCMOS can integrate passives, a low-noise amplification function and baseband processing on the same chip.

A reduction in the SKA cost inherent to LNAs can be achieved by integrating an entire receiver chain to a single chip. Such a solution has been proposed with a Si CMOS process [32]. However, a Si CMOS process has low f_T and poor RF performances. Moreover, the process has high substrate losses and poor quality passives. Nevertheless, the technology is mature and has attracted important investments in order to improve transistors' speed and integration. As the size of transistors decreases and f_T increases, the CMOS process is becoming applicable for use in radio astronomy receivers. It is proposed in [32] to depart from conventional RF topologies and to use feedback or feed-forward techniques in order to achieve broadband impedance matching without deteriorating the LNA noise matching. Noise cancelling techniques are also proposed in [32].

A qualitative evaluation of various technologies is provided in [33]. InP and GaAs HEMT technologies have the best noise performance but they are very costly. According to [33], the SiGe BiCMOS process has most potential for meeting the performance and cost requirements of the SKA. The NFs of SiGe and GaAs LNAs are comparable but SiGe has lower power consumption and is cheaper, about a third of GaAs cost and about 5% of InP cost. The criteria used for a qualitative evaluation of the most relevant technologies are provided in [33] and summarised in Table 2.1.

Table 2.1. Main performance criteria of front-end circuits.

Technology	RF Noise	1/*f* Noise	Power Consumption	Linearity	Integration Density	Cost
InP	Very good	Poor	Fair	Good	Low	High
GaAs PsHEMT	Very good	Poor	High	Good	Low	High
GaAs HBT	Good	Good	Fair	Very good	Low	High
SiGe	Good	Good	Low	Good	High	Medium
BiCMOS	Fair	Good	Low	Fair	High	Low
CMOS	Fair	Poor	High	Good	High	Low

2.2.4.2 Single-ended and differential LNAs

The main difficulty in differential LNAs' design is attaining a very low CMRR. The NF of LNAs is better for single-ended devices than for differential devices. The outputs of an antenna in the phase array feed being differential, a balun is required when single-ended LNAs are used. The contribution of passive baluns to noise can be higher than 16 K [9]. Therefore, the balun noise will decrease the receiver noise performance. When an LNA with differential inputs is connected directly (without a feeder) to the antenna, the NF of the receiver can be improved. However, the credibility and acceptability of differential amplification for very low noise amplifiers has not been established [9].

2.2.4.3 Input impedance

The input impedance of wide-band receivers in the mid-band of the SKA is expected to be higher than 50 Ω. A typical value for the input impedance for the SKA is 150 Ω [21]. The increase in source impedance can improve the NF for narrow-band LNAs [33], [34]. This has been achieved for wideband LNAs using GaAs transistors [8].

2.2.4.4 The effect of temperature

The main SKA sites are in Western Australia and in South Africa. Yearly temperature variation in Australia can reach 50 °C with important changes during a single day. In South Africa, fluctuations of more than 40 °C can be reached yearly and daily variations are also

important [9]. Significant changes in temperature will change the NF and the gain of the LNA, affecting the calibration of the system. The stabilisation of the temperature needs to be considered to minimise the impact of temperature variation. The standard technique to reduce LNA noise in radio astronomy is cryogenic cooling. When the number of receivers is small, this solution is cost-effective. However, for a very large number of receivers spread over a very large area, cryogenic cooling is not cost-effective. A cost-effective solution will comprise high-performance LNAs at room temperature and integrated into antenna elements in order to reduce losses.

2.2.5 SKA LNA developments

The parameters of LNAs designed for SKA evaluation are shown in Table 2.2, where NT is the noise temperature and RT means "Room Temperature".

Table 2.2. Summary of LNA parameters.

LNA Data	**[35]**	**[36]**	**[8]**	**OPAR**	**[37]**	**[38]**	**University of Manchester**
Gain	42 26	28	7 15	27 4	10	40 27	25
				21		30	
NT (K)	35 35	34	14 25	65 56	123	10 77	35
				10		4	
Frequency (GHz)	0.9 - 2 0.3 - 1	0.7 - 1.8	0.8 - 1.4 0.4 - 1	0.3 - 1.9	0.2 - 2	1 - 12 0.1 - 5	0.7 - 4
Technology	GaAs pHEMT	GaAs pHEMT	90 nm CMOS	0.25 µm SiGe HBT	1 µm InP pHEMT	InP SiGe pHEMT HBT	70 nm GaAs mHEMT
Topology	SE Diff	Diff	SE Diff	Diff SE	SE	Diff SE	SE
Impedance (Ω)	50 150	300	85 100	100 50	50	270 50	50
Tempera-ture (K)	RT RT	RT	RT RT	RT RT 22	RT	12 RT 12	RT

In Table 2.2, the LNA by Astron [35] is a single-ended GaAs device using Avago GaAs pHEMT technology and the 70 nm GaAs mHEMT process from OMMIC. The hybrid 50 Ω LNA operates from 0.9 GHz to 2 GHz and has a flat gain of 40 dB and a noise

temperature of 35 K. The differential LNA resulting from the collaboration between Astron and FG-IGN and using the GaAs pHEMT technology from Avago is a hybrid device with a differential input impedance of 150 Ω, operating from 0.3 GHz to 1 GHz with a gain of 26 dB and a noise temperature below 35 K.

The differential LNA designed by the Commonwealth Scientific and Industrial Research Organisation (CSIRO) in Australia [36] is a hybrid device using the GaAs pHEMT technology from Avago and operating from 0.7 GHz to 1.8 GHz. The device has a gain of 28 dB and a noise temperature of 35 K. The differential input impedance is 300 Ω.

In [8], the LNAs designed by the University of Calgary are MMIC single-ended and differential devices based on 90 nm CMOS technology. A noise temperature of 25 K and a gain of 15 dB in a bandwidth of 0.8 GHz to 1.4 GHz have been reported for the differential LNA at room temperature. The input impedance is 100 Ω and the return loss less than -12 dB. The LNA with single input has a noise temperature of 14 K (0.2 dB), a gain (S_{21}) of 17 dB and a return loss of -11 dB. The output 1 dB compression point is 2 dBm, the output IP3 and IP2 is 12 dBm and 22 dBm, respectively. The power supply is 1 V and the current 43 mA. According to the authors, the NF is the lowest known for a wideband CMOS LNA at room temperature. The topology of the LNA is similar to the topology of [12], but with an NF that is improved by an increase in the input impedance and by using the power-constrained optimisation technique in [32] instead of the bandwidth and power-constrained optimisation technique presented in [33]. The optimum transistor size is also found by a two-port LNA optimisation method [32], which includes second-order parasitics. The gate inductor is external to the chip and has a quality factor close to 100 in order to meet performance requirements. The shielding of the substrate ensures that substrate noise is not picked up by passive components.

The Paris Observatory (OPAR) differential LNA is a MMIC device based on SiGe HBT technology [9]. The LNA has a noise temperature of 65 K, a differential input impedance of 100 Ω and a gain of 27 dB from 0.3 GHz to 1.9 GHz. An LNA with single ends has been reported to have a noise temperature of 56 K and a gain of 24 dB from 0.3 GHz to

1 GHz. This LNA has a noise temperature of 10 K and a gain of 21 dB at 22 K ambient temperature.

According to [37], the Microelectronics and Nanostructure research group of the University of Manchester has developed an LNA based on an InP pHEMT process. The average gain is 10 dB from 0.2 GHz to 2 GHz and the average noise temperature is 123 K from 1 GHz to 2.5 GHz.

The work of the California Institute of Technology has concentrated on SiGe HBT technology at cryogenic temperatures [14]. For a bandwidth of 0.1 GHz to 5 GHz, the noise temperature of an MMIC LNA is 77 K at 300 K and the gain is 27 dB. At 15 K ambient temperature, the noise temperature is 4 K, the gain is 30 dB and the return loss is -14 dB. An InP LNA with a bandwidth of 1 GHz to 12 GHz had a noise temperature of 10 K and a gain of 40 dB at 12 K ambient temperature [38].

The University of Manchester’s single-ended MMIC LNA is based on the 70 nm mHEMT process from OMMIC [9]. The noise temperature is 35 K, the input impedance is 50 Ω and the bandwidth is from 0.7 GHz to 4 GHz at room temperature.

2.3 THE LOW NOISE AMPLIFIER

The role of the LNA is to improve the input signal level without adding significant noise and distortion. As the first and most sensitive element of a receiver chain, the LNA determines the NF and the linearity of the receiver. Performance requirements for LNAs depend on their applications. For applications with a low signal level and large bandwidth, the most important requirements are the NF, the input matching over the bandwidth and the linearity. In the case of the SKA, linearity specifications are less stringent than noise and matching requirements owing to the selection of sites that are free from radio interference.

2.3.1 Background

The architecture of a RF receiver is represented in Figure 2.1 where a pre-selection filter attenuates out-of-band signals and an additional filter after the LNA rejects the image frequency.

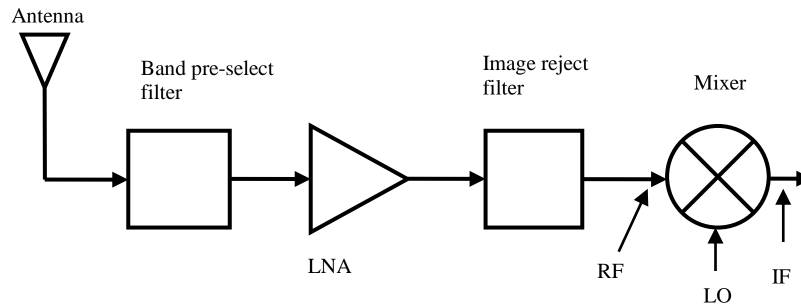


Figure 2.1. RF receiver.

Figure 2.1 is a cascade of noise-inducing stages with a noise factor defined as [39]:

$$F_{cascade} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_{n-2} G_{n-1}} \tag{2.2}$$

where F_n and G_n are the noise factor and the gain of the nth stage of the cascade.

Assuming that the pre-selection filter is noiseless and has a voltage gain of 1, the first stage of the receiver does not contribute to the total noise of the cascade. From (2.2), the noise factor of the receiver can be approximated by the noise factor of the LNA (F_1), the second term and subsequent terms of the equation being negligible when the gain of the LNA (G_1) is high compared to F_n.

NF, bandwidth, gain, linearity, input and output impedance matching and power consumption are the fundamental parameters that characterise the LNA. The NF of an LNA, a measure of the degradation of the SNR introduced by the LNA, is defined as NF = 10.log(F), where F is equal to SNR_i/SNR_o. SNR_o is the SNR at the output of the LNA and SNR_i is the SNR at its input. The gain is defined as a voltage gain ($A_v = v_{out}/v_{in}$)

or as a power gain ($S_{21} = P_{out}/P_{in}$) and is expressed in dB. The bandwidth is defined as the frequency range for which the gain is within 3 dB of the maximum gain. The linearity of the LNA is measured by the 1 dB compression point (IP_{1dB}) and the third order intermodulation product (IIP3). The standard input impedance is 50 Ω. Impedance matching at input is required, whereas output impedance matching is not always required [40].

It is impossible to have peak performance for each of the parameters; trade-offs between parameters are required and are dictated by the application. This is shown in the RF design hexagon in Figure 2.2, where any two adjacent ones of the six parameters trade with each other.

For GSM systems, linearity requirements are stringent owing to the range of the input signal level (from -20 dBm to -110 dBm) whereas less attention is paid to the NF.

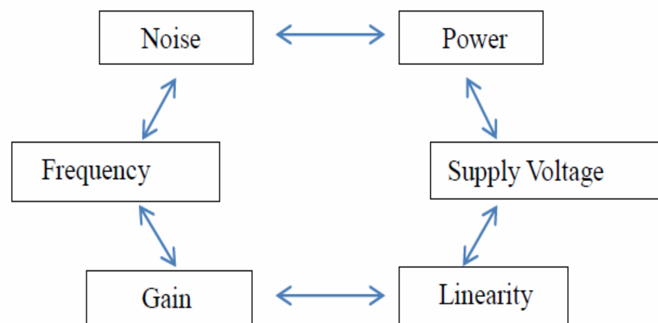


Figure 2.2. RF design hexagon.

For GPS, the noise and gain performances are expected to be very good, typically 1 dB for the noise and 20 dB for the gain [41]. In most cases, the LNA is designed to have a low NF, to provide an acceptable gain and linearity over its bandwidth and to have input and output impedances that are matched to the adjacent blocks of the receiver. For wide-band LNAs, the trade-off between the NF and the input impedance matching limits the NF to

values that are typically higher than 3 dB [42]. This trade-off is not applicable to LNAs with negative feedback. However, negative feedback impairs stability.

2.3.2 Topologies of LNAs

Most LNA topologies are single-ended, the use of differential LNAs being limited by performance impairments. Generally, an LNA with differential inputs is a duplication of a singled-ended LNA and can be analysed as such [43], [44]. Differential LNAs consume more power, have higher NF and require more chip area than their single-ended counterparts. Topologies can be grouped into three categories: single transistor topology, cascode topology and two-stage topologies [45]. Although MOS transistors are used to represent these topologies, their characteristics are also valid for bipolar junction transistor (BJT) circuits.

Single transistor topologies are: inductively degenerated common-source (emitter), dual-loop feedback, improved matching using resistive feedback, programmable multi-LC, wideband resistive feedback and transformer feedback. A detailed description of the topologies above, which are represented in Figure 2.3, is provided in [45]. Single-transistor topologies are simple to analyse, they have low power consumption and occupy a small chip area. Yet they have two major disadvantages: the isolation between the output and the input of the LNA is poor and the simultaneous matching of the input-output impedance and minimum NF is uneasy. The feedback from the output to the input of the LNA is caused by the gate-drain (base-collector) capacitance that makes input and output matching interdependent. Their noise performance is close to the noise performance of the transistor.

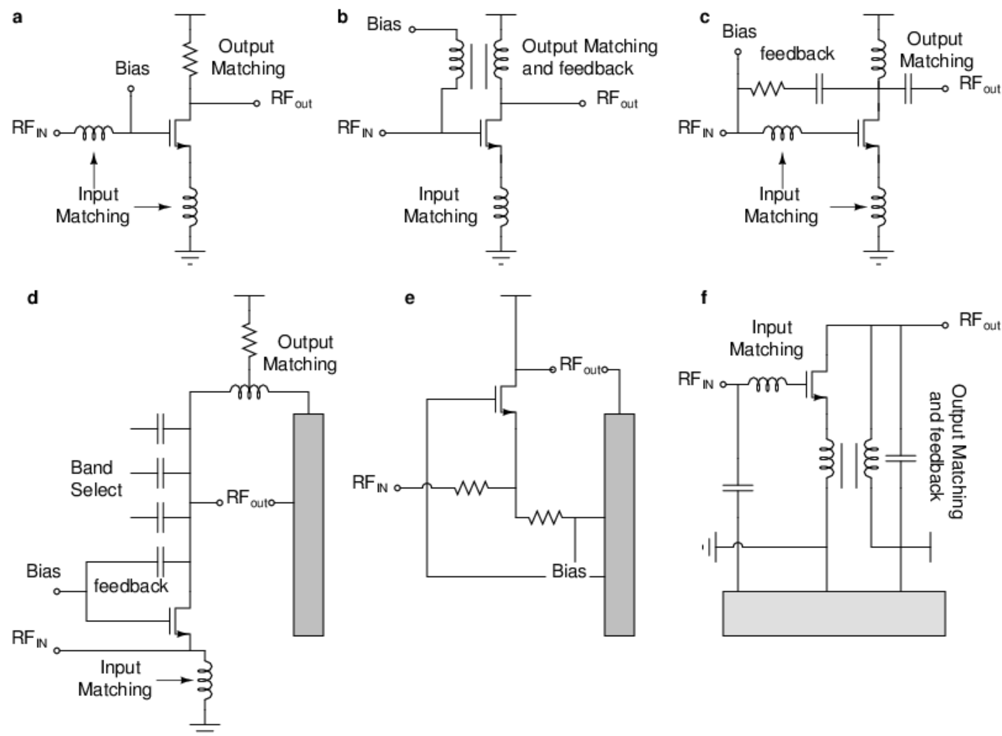


Figure 2.3. Single-transistor LNAs. a) common-source, b) dual-loop feedback, c) resistive feedback and tank output matching, d) programmable multi-LC, e) wideband resistive feedback, f) transformer feedback. Adapted from [45] for quality improvement, with reproduction permission.

Cascode topologies cancel the feedback from the output to the input caused by the gate-drain (base-collector) capacitance due to the common-gate (base) configuration of the second transistor. Input and output impedance matching for minimum noise performance is facilitated. However, the supply voltage is relatively high and the second transistor impairs the noise performance of the LNA. Types of cascode topologies [45] are basic cascode, folded cascode, current reuse cascode, multi-section input cascode, resistive feedback cascode and distributed cascode. They are represented in Figure 2.4.

Two-stage topologies consist of a configuration of two cascaded common-source transistors and a feed-forward configuration; both LNAs are represented in [45]. The feed-forward configuration allows the use of noise-cancelling techniques and an increase in the bandwidth. In addition to noise cancelling, the feed-forward configuration provides simultaneous noise and impedance matching [46].

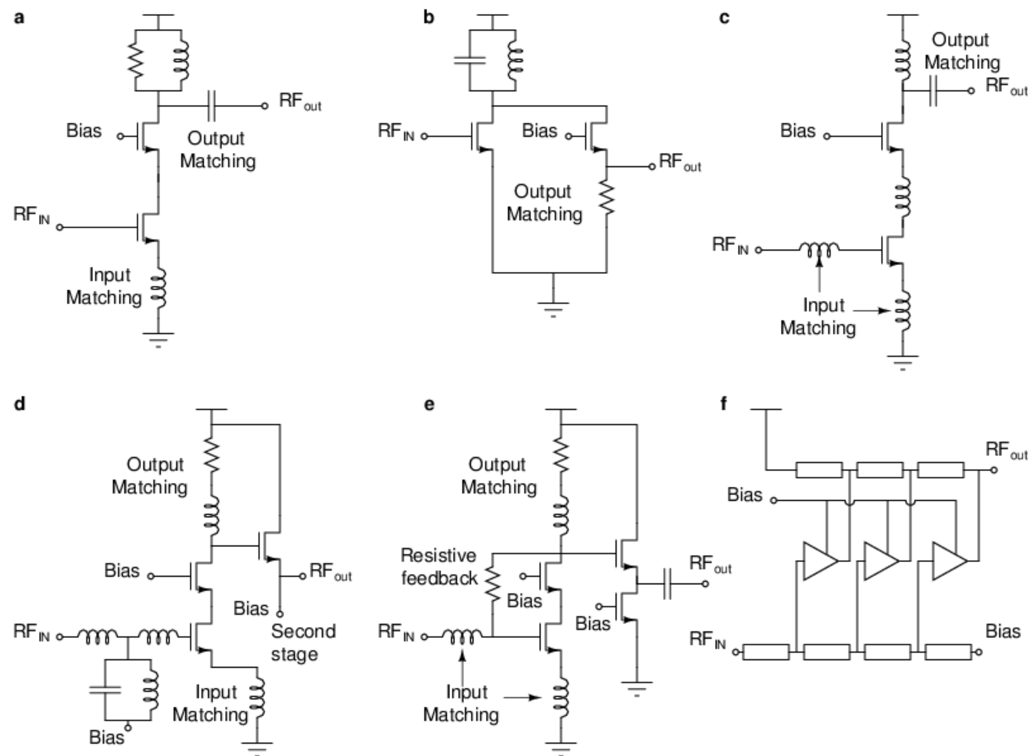


Figure 2.4. Cascode LNAs. a) basic cascode, b) folded cascode, c) current-reuse cascode, d) wideband matching, e) resistive feedback, f) distributed cascade. Adapted from [45] for quality improvement, with reproduction permission.

2.3.3 Wideband LNAs

Wideband LNAs are LNAs for which the ratio between the bandwidth and the centre frequency can be as large as two [46] and having, over the wide bandwidth, a flat gain and good impedance match. The main wideband LNA topologies consist of the common-source (common-emitter) with shunt input resistor configuration, resistive shunt feedback topology, distributed amplifier topology, balanced amplifiers [22], [46] and the common-gate (common-base) configuration. Topologies with shunt input resistor and resistive shunt feedback are represented in Figure 2.5.

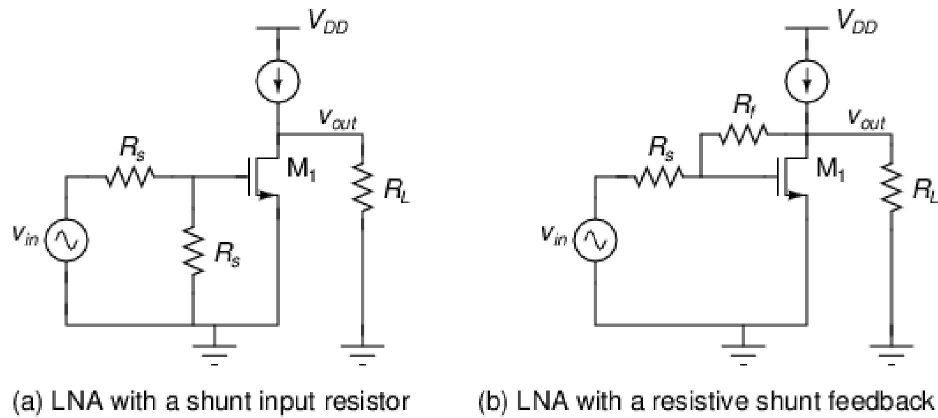


Figure 2.5. Resistive wideband matching topologies.

The common-source topology with shunt resistor provides wideband input matching but impairs the gain and the NF. Typical values of NFs achieved are greater than 6 dB [47]. The resistive shunt feedback topology provides good impedance matching and wideband flat gain, but has poor noise performance and suffers from low gain. The NF deviates from the absolute minimum NF achievable by a MOS transistor (NF_{min}) owing to the noise added by the feedback resistor. The NF achievable (5 dB) is too high for the SKA [48], [49]. For high frequencies, the impedance matching and NF are limited by losses in parasitic capacitances [50]. For distributed amplifiers, transmission lines between amplification stages achieve wideband impedance matching. A variation of this topology is the lumped-element wideband input amplifier represented in Figure 2.6. It requires a large number of components for matching, which is detrimental to the NF [51], [52].

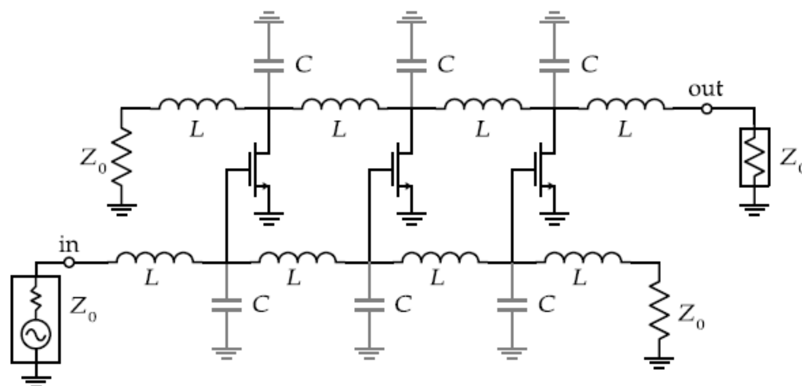


Figure 2.6. Three-transistor distributed amplifier. Taken from [51], with permission.

The common-gate circuit is simple and provides wideband response, but its NF is no better than 2.2 dB, which falls short of the SKA requirements [22]. The circuit offers simple matching because the input resistance of the MOS transistor is inversely proportional to its transconductance (g_m), resulting in wideband impedance matching. The matching of the output impedance is independent from the input matching owing to the negligible capacitive coupling between the output and the input. The main disadvantage of the common-gate LNA is its NF of typically 3 dB [53]. The common-gate topology is unsuitable as the first stage of an LNA because current noise at its output is referred to its input without reduction, the current gain of the circuit being unity.

A topology of interest for differential LNAs is the thermal-noise cancellation LNA that applies feed-forward to minimise the noise [46]. Thermal-noise cancellation designs provide low NF and wideband input impedance matching without instability problems found in feedback systems. A sub-2 dB NF has been achieved in [54]. No reported sub-1 dB NF design using the thermal-noise cancellation topology was found.

The noise factor of a single transistor common-source LNA without degeneration and with R_s as the resistance of the source and R_d the load resistance is expressed by the equation:

$$F = 1 + \frac{2}{3 g_m R_s} + \frac{1}{g_m^2 R_d R_s} \tag{2.3}$$

Equation (2.3) shows that the noise factor decreases when R_s increases and that an arbitrarily low noise factor can be achieved at the cost of power dissipation, which makes the common-source configuration attractive for highly sensitive LNAs. Because the gate of the common-gate configuration in Figure 2.7(a) is grounded, the capacitive coupling between the output and the input is negligible. Similarly, the capacitive coupling between the output and the input of the common-base configuration is negligible. The IDCS LNA in Figure 2.7(b) does not have such an isolation. However, this topology is widely used for narrow-band applications because of its gain and noise performance.

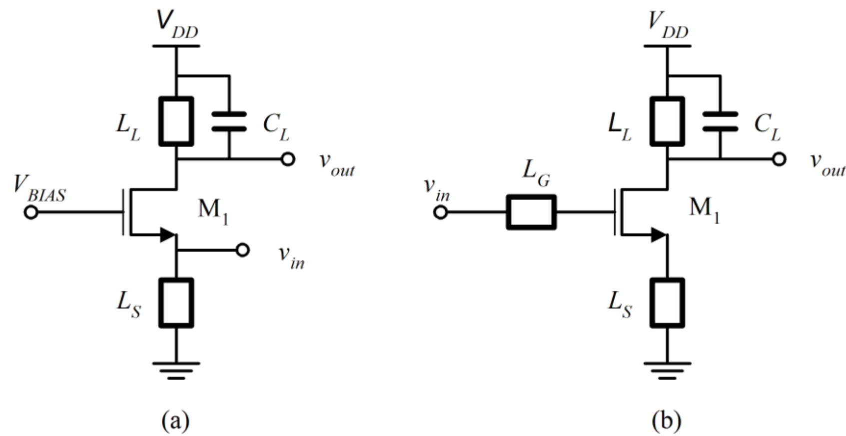


Figure 2.7. (a) Common-gate LNA. (b) Common-source with inductive degeneration.

This topology surpasses the common-gate topology in terms of noise performance. The IDCS topology simultaneously achieves noise and power matching, but the matching is limited to a narrow bandwidth, owing to the gate and source inductors. A Chebyshev matching network can be used to increase the bandwidth, but the Chebyshev matching network requires several inductors, which will degrade noise performance, particularly in case of on-chip inductors. The isolation between the output and the input is improved by using a cascode configuration [55], as shown in Figure 2.8.

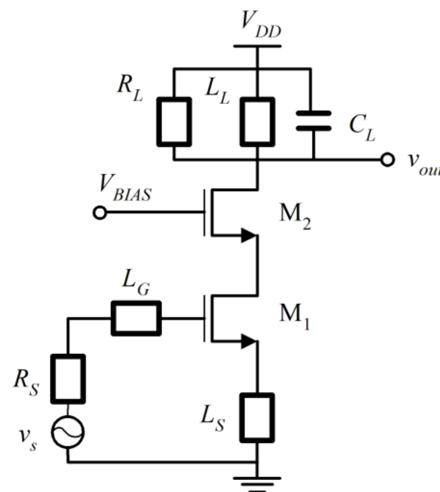


Figure 2.8. LNA with inductively degenerated common-source.

Adapted from [55], © 2007 IEEE.

A wide bandwidth is obtained by adding a capacitor between the drain of the first transistor (M_1) and the source of the cascode transistor without affecting the NF [56]. The cascode transistor M_2 presents low impedance at the drain of M_1. The low impedance reduces the voltage gain of M_1, reducing the Miller capacitance. M_2 increases the reverse isolation between the output and M_1 that facilitates impedance matching.

2.3.4 Performance specifications

The LNA in [56] was designed for the Canadian Large Adaptive Reflector (CLAR), a demonstrator for the SKA radio telescope. The specifications of the demonstrator and the performance of the LNA are presented in Table 2.3 where R_s is the resistance of the source.

Table 2.3. SKA specifications and performance of LNAs.

Parameter	Specifications of the CLAR	[56] (R_s = 50 Ω)	[8] (R_s = 85 Ω)
Technology		CMOS 0.18 µm	CMOS 90 nm
Frequency	0.7-1.4 GHz	0.7-1.4 GHz	0.7-1.4 GHz
Noise temperature	20 K (0.29 dB) max	40 K (0.56 dB) max	14 K (0.2 dB) max
Return loss (S_{11})	10 dB min	-11 dB min	-11 dB max
Power gain (S_{21})	15 dB min	17 dB min	17 dB min
IP1dB	-40 dB min	-10 dBm min	-18 dBm typ
Power consumption	100 mW typ	50 mW typ	43 mW typ

The specifications of the SKA in the sub-band of 0.7 GHz to 1.4 GHz are the same as those of the CLAR. The LNA in [8], a cascode modified inductively degenerated common-source topology, is a single-input device with a noise temperature of 14 K (0.2 dB) at room temperature. The NF of [8] is the lowest known for a wideband CMOS LNA at room temperature.

Performance specifications of the LNA for the mid-band of the SKA targeted for this thesis are based on specifications in [22] for the CLAR provided in Table 2.3 where the

frequency band of 700 MHz – 1400 MHz has been extended to 300 MHz – 1400 MHz. In addition, the NF is set to be less than 1 dB from 300 MHz to 1400 MHz. The LNA must be unconditionally stable and the load impedance is set to 50 Ω, which facilitates measurements with test equipment. The operating voltage is set to 2.2 V.

2.4 PERFORMANCE METRICS OF AN LNA

The sensitivity of an LNA is determined by several parameters such as its circuit topology, the transistor geometry, the semiconductor process, the layout, the grounding and EM shielding, the input and output matching, the package parasitics, the biasing circuit, the supply decoupling and the temperature. The designer can control the sensitivity of the LNA by finding the appropriate trade-off between five characteristics of the LNA: NF, bandwidth, gain and linearity and dynamic range. The five parameters and the power consumption can therefore be used to measure the performance of the LNA and their overview is provided in the following paragraphs. In addition, requirements for an unconditional stability required for adequate performance in the operating conditions are provided.

2.4.1 Insertion loss and return loss: S-parameters

The scattering parameters of a two-port network are the input reflection coefficient (S_{11}), the output reflection coefficient (S_{22}), the forward transmission coefficient (S_{21}) and the reverse transmission coefficient (S_{12}). The insertion loss and the return loss, which are two primary characteristics of an RF two-port network, can be expressed in terms of scattering parameters. The insertion loss is a measure of the attenuation or the gain of the signal power through the network and is defined by (2.4) when the input and output ports, the source and load are all matched to the same impedance. An LNA with high gain is expected; however, high gain can produce intermodulation and instability. The typical LNA gain ranges from 12 dB to 25 dB [40].

$$Insertion\ loss\ (dB) = -20log_{10}|S_{21}| \tag{2.4}$$

The return loss is a measure of the power of the incident signal compared to the signal reflected back to the source because of impedance mismatch. It is measured by (2.5).

$$Return\ loss\ (dB) = 20log_{10}\left|\frac{1}{S_{11}}\right| \tag{2.5}$$

In RF design, the return loss is expected to be better than 10 dB [40], [57]. Although this criterion is not formal, long design experience shows that acceptable input and output matching is achieved when S_{11} and $S_{22} \leq$ -10 dB [58].

2.4.2 Noise Figure

The NF of an amplifier is a measure of the electronic noise added by the amplifier to the output signal. For LNAs, the NF is one of the main performance criteria, as its measures how well the objective of amplifying the input signal with the least possible decrease of its SNR is achieved.

The noise factor F of a receiver is defined by the expression:

$$F = \frac{S_i / N_i}{S_o / N_o} \tag{2.6}$$

where S_i/N_i and S_o/N_o are the SNR at the input and output of the LNA, respectively. The NF is defined by 10 log (F).

2.4.3 Bandwidth

In RF design, the bandwidth is defined in terms of signal power reflection rather than the 3 dB bandwidth. The bandwidth of an LNA corresponds to the frequency band within which the input and output power reflection coefficients are, within a given limit. Generally, reflection coefficients of less than 0.1 at the input and less than 0.2 at the output, corresponding respectively to -20 dB for S_{11} and -13.98 dB for S_{22}, are the accepted standards for reactively matched and broadband amplifiers [59]. In practice, S_{11} and S_{22} of less than -10 dB are accepted for broadband amplifiers.

2.4.4 Gain

Similar to bandwidth, the definition of gain in RF circuits differs from the voltage-related definition used in low-frequency circuits. The gain is defined as the ratio of the output to the input power and is expressed by the expression:

$$Power\ gain(dB) = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \tag{2.7}$$

where P_{out} is the RF output power and P_{in} is the RF input power.

2.4.5 Linearity

Nonlinearities in BJTs and SiGe HBTs are due to nonlinear current sources, transconductance, capacitors and others elements of the small-signal model whose values are dependent on the bias conditions. The gain of an amplifier is linear for small input signals. This linearity ceases as the relative increase of the output starts to decrease with the increase of the input signal. The decrease in gain, referred to as gain compression, is due to the nonlinearity of the amplifier that leads to the degradation of the SNR. The level of the input signal for which the output signal drops by 1 dB from the expected linear value is a measure of the nonlinearity due to gain compression and is referred to as the 1 dB compression point. The 1 dB compression point is also a measure of the input range of an LNA, which is typically comprised between -20 dBm and -25 dBm [60].

Nonlinearities also cause intermodulation products that are a source of SNR degradation when the amplifier operates in the non-linear region of its gain response. These products can be of several orders, e.g. second- and third-order intermodulation and so on. The most critical distortion due to intermodulation is caused by third-order intermodulation products because they cannot be filtered out of the output signal. This intermodulation distortion is measured by the third-order intercept point (IP3). When the power of the input signal P_{in} increases, third-order spurious signals increase much faster than P_{out}, the power of the output signal due to the fundamental signal. The point of intersection between P_{out} as a linear function of P_{in} and the power of third-order spurious signals as a function of P_{in}

defines IP3. The 1 dB compression point and the IP3 are the main figures of merit that are used to assess the linearity of an LNA.

2.4.6 Dynamic range

The dynamic range of an LNA is the difference between the power of the maximum admissible input signal and the power of the minimum detectable input signal that can be distinguished from noise. While the sensitivity of the LNA, which is determined by the minimum detectable input signal, is limited by noise, the maximum input signal is bounded by distortion. The dynamic range is therefore a measure of the ability to detect weak signals and the presence of large signals. The minimum detectable input signal is determined by the noise factor of the LNA and by the minimum required SNR $(S/N)_{min}$ at the output of the LNA. This is shown by (2.8) from (2.6) as follows:

$$S_i = N_i F \frac{S_o}{N_o} \tag{2.8}$$

The noise due to the signal source is thermal with a spectral power density of N_i. The impedance of the source is equal to the conjugate of the input impedance of the LNA when the impedance is matched at the input [2]. It can then be shown that the power of the noise at the input of the LNA is independent of the source resistance and is expressed, at ambient temperature, by the expression:

$$N_i = kT_o B \tag{2.9}$$

where $k = 1.38 \times 10^{-20}$ mW.sec/K is the Boltzmann constant, $T_o = 290$ K is the absolute temperature at 27 ^{o}C and B is the bandwidth of the receiver in Hz.

The absolute thermal noise floor generated by any source into the matched input of an amplifier is then equal to N_i. Hence, the power of the input signal can be expressed by:

$$S_i = kT_o BF\left(\frac{S_o}{N_o}\right) \tag{2.10}$$

The minimum detectable input signal is achieved when S_o / N_o is equal to *(S/N)_{min}*, therefore the input signal can be rewitten as:

$$S_i = kT_o BF \left(\frac{S}{N} \right)_{\min} \tag{2.11}$$

Because $(S/N)_{min}$ is not determined by the receiver, the sensitivity is improved when F is minimised. The minimum detectable input signal in dB is expressed, at 27 ºC (290 K), as:

$$S_i(dB) = -174 dBm + 10\log(B) + NF + 10\log\left(\frac{S}{N} \right)_{\min} \tag{2.12}$$

The upper limit of the input signal is determined by the linearity of the LNA, which can be measured by the input-referred IP3 (IIP3). The IIP3 is the input signal for which the amplitude of the third-order intermodulation product IM3 out of the LNA is equal to the amplitude of the first-order linear output. The power of the IIP3 being P_{IIP3}, the power of the third-order intermodulation product output P_{IM3out} and the power of the input signal P_{in} are related by the expression [60]:

$$P_{IIP3} = P_{in} + \frac{P_{out} - P_{IM3out}}{2} \tag{2.13}$$

where P_{out} is the first-order linear output of P_{in} and all the signal powers are expressed in dBm.

Typically, the dynamic range of an LNA is measured by the spurious-free dynamic range (SFDR), which is defined by the expression:

$$SFDR = \frac{2P_{IIP3} + NF}{3} - 10\log\left(\frac{S}{N} \right)_{\min} \tag{2.14}$$

The SFDR is the difference between the point where the third-order intermodulation product starts to rise above the noise floor and the point where the input power is equal to the noise floor, as shown in Figure 2.9. The noise floor is defined as the noise at the output of the LNA due to all noise sources and to all undesired signals.

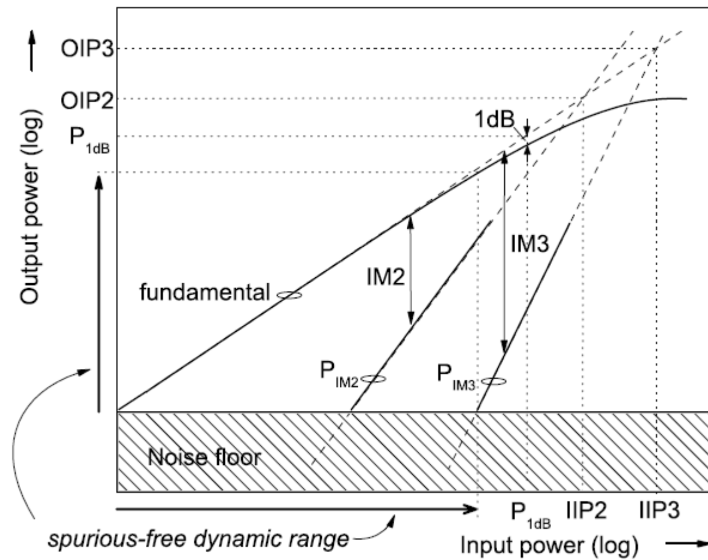


Figure 2.9. The spurious-free dynamic range. Taken from [63], with permission.

2.4.7 Stability

The stability of an LNA is compromised when undesired oscillations are generated in the LNA circuitry. Such oscillations may be caused by internal or external feedback and by high gain out of the frequency band of operation. Internal feedback is caused by parasitic couplings within components or between components on the IC. The LNA must be unconditionally stable; for any input and output load value, the circuit must not oscillate. Stability can be analysed by numerical or graphical methods that are based on the scattering parameters of the LNA. The numerical method is based on the Rollet conditions for unconditional stability:

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.15}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.16}$$

where k is the Rollet stability factor and S_{11}, S_{12}, S_{21} and S_{22} are the S-parameters of the LNA. For $k > 1$ and $|\Delta| < 1$, the LNA is stable for any association of input source and output load at a given frequency and bias current. For graphical analysis, a 3-D Smith chart visualisation tool can be used [61], [62].

The conditions for unconditional stability are better achieved when S_{12} is low. As indicated in Section 2.4.1, S_{12} is a relative measure of the signal transmitted from the output to the input. In a common-emitter transistor amplifier, S_{12} is strongly related to the capacitive coupling between the collector and the base, which is a source of feedback and impairs the bandwidth of the amplifier through the Miller effect. In a cascode amplifier, the grounded base of the common-base transistor prevents the collector output signal from being fed back to the emitter, acting as a shield. Therefore, the cascode amplifier has a lower S_{12} and is more stable than a common-emitter amplifier.

2.5 ACTIVE DEVICES FOR LOW NOISE AMPLIFIERS

2.5.1 Advantages and applications of SiGe HBT technology

The performance of SiGe HBTs has increased exponentially since their first introduction more than 20 years ago: current SiGe HBTs achieve performances that are comparable to III-V technologies. Several parameters can be used to characterise the performance of semiconductor technologies: f_T, breakdown voltage, electrical conductivity, thermal conductivity, integration and cost. The noise performance and gain are closely dependent on the f_T, the maximum power handling of an active device is determined by the breakdown voltage, the electrical conductivity determines substrate losses and for applications requiring high power, the thermal conductivity determinates the reliability of the device. Typically, for low-noise applications, technologies are evaluated in terms of f_T.

In terms of the size of active devices, as most technologies contain Si CMOS devices, the length of the gate of the associated Si CMOS process, implemented on the same die with SiGe HBT devices, is used to characterise SiGe HBT technologies. The evolution of the performance of SiGe HBT devices is shown in Figure 2.10. First-generation devices had a peak cut-off frequency of 50 GHz and CMOS gate length of 0.35 µm. This is the case in the IBM SiGe HBT 5HP process. The Jazz SiGe with a peak f_T of 60 GHz and 0.35 µm CMOS gate length falls in this category. The peak f_T for the second generation is 120 GHz, with a CMOS gate length of typically 0.180 µm. The IBM SiGe 7HBT, 120 GHz peak f_T,

the Jazz SiGe 150 GHz peak f_T and the IHP SiGe SGC25B, 120 GHz peak f_T are second-generation processes. Third-generation processes attain a peak f_T of 200 GHz, such as the IBM SiGe 8HP, with a CMOS gate length of 0.130 µm. Fourth-generation processes achieve more than 400 GHz for peak f_T with a typical gate length of 90 nm.

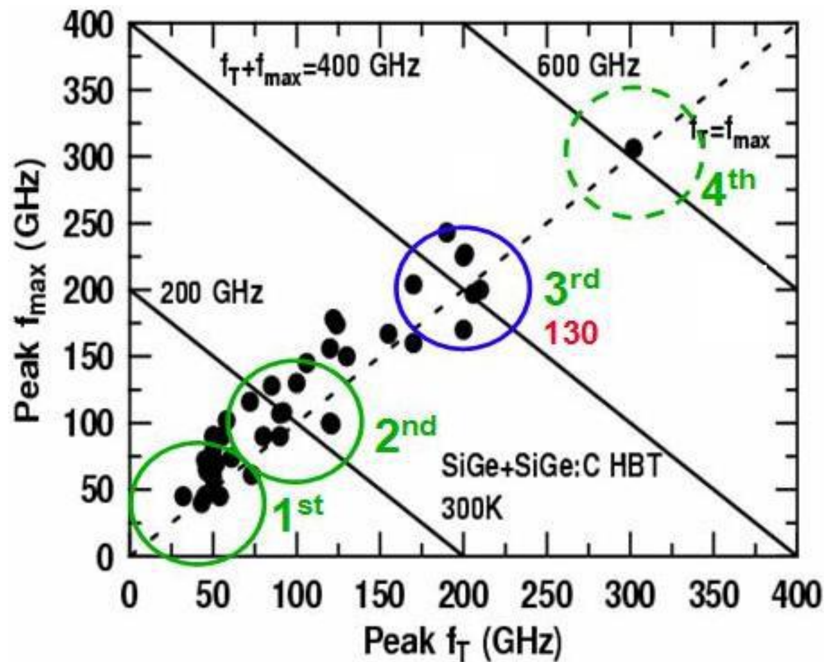


Figure 2.10. SiGe HBT technology performance increase. Taken from [64], with permission.

SiGe HBTs are a compromise between GaAs HBT and RF CMOS active devices. They have the following advantages, compared to Si BJT and RF CMOS:

- The collector bias current for a Si BJT is about three times the bias current for a SiGe HBT for the same f_T. Similarly, for a MOSFET, a higher bias current is required to achieve the same transconductance as for a SiGe HBT.

- SiGe HBTs can sustain higher breakdown voltages than Si BJT for the same f_T. Compared to RF CMOS, they also sustain higher breakdown and operating voltages, RF CMOS devices being limited by the gate oxide breakdown voltage and hot-carrier

injections. In addition, SiGe HBTs can handle breakdown voltages of 1.5 × BV_{CEo} to 2 × BV_{CEo} if the resistance seen from the base is less than 500 Ω [65].

- SiGe HBTs have lower base resistance, higher current gain, f_{max} and f_T for the same collector bias current when compared to Si BJTs. For the same current density bias, SiGe HBTs achieve lower minimum achievable NF than RFCMOS. It follows that SiGe HBTs achieve better noise performances than Si BJT and RFCMOS devices. Owing to their high current gain, feedback techniques can be used to improve linearity with a reduced impact on the total gain.

- For SiGe HBTs devices, the Early voltage can be increased by the profile of Ge concentration in the base. Hence high output resistances can be obtained, improving the gain of the transistor further. Contrary to SiGe HBTs, RF CMOS devices have a lower output resistance.

SiGe ICs are used in wireless communications systems such as cellular base stations and handsets, satellite communications, wireless local area networks and in wireline communication systems such as optical fibre networks. They are also found in defence and navigation systems such as radar and GPS and in automotive applications.

The SiGe HBT technology used in this work is the IBM BiCMOS8HP, a third-generation BiCMOS process. Commercialised in 2005, this process offers a SiGe base with carbon doping. The profile of the Ge concentration is trapezoidal, with an average concentration of 25% [66].

2.6 NOISE SOURCES IN ELECTRONIC SYSTEMS

The types of fundamental noise found in electronic systems are thermal or Johnson noise, shot noise, flicker noise or 1/*f* noise and generation-recombination or G-R noise. Electronic noise is a random process that results from the random movement of electrons. Statistical methods are therefore used to describe the principles underlying the behaviour of

electronic noise and how electronic systems are affected by noise. The intrinsic electronic noise can be modelled by a random Gaussian and ergodic process. For a random noise function $v(t)$, this process has the following properties, where the symbol $< >$ is a time-averaging function:

- The average value of the process is equal to its DC value, $<v(t)>$.
- The square of the average value provides the DC power of the distribution, $<v(t)>^2$.
- The mean square of the process provides the total average power $<v^2(t)>$.
- The variance of the process σ^2 represents its average AC power.
- The root mean square (RMS) value of the process is given by its standard deviation σ.

The power spectral density S_{vv^*} of a stationary random signal $v(t)$ is expressed by the Fourier transform of the autocorrelation function as formulated by the Wiener-Kinchine theorem. It can be shown that S_{vv^*} of is given by (2.17):

$$S_{vv^*} = \lim_{T\to\infty} \frac{|v(f)|^2}{T} = \overline{v(f)v^*(f)} = \overline{vv^*} \tag{2.17}$$

where f represents the frequency and T is a time variable.

The operator $\overline{}$ is a mathematical operator representing the average of $v(f)v^*(f)$, which is the power spectral density of an ergodic signal. The Fourier transform $v(f)$, which is truncated, is over ($-T/2 + T/2$). Equation (2.17) is the cornerstone of AC noise analysis in electronic circuits and will be used through this work. The following properties of the operator will be used throughout the work:

- If a and b are the Fourier transforms of two uncorrelated noise sources with zero mean value, then $\overline{ab^*} = 0$
- $\overline{ab^*} = \left(\overline{ba^*}\right)^*$

For a resistor of value R and with a a noise voltage $v(t)$ on its terminals, the power spectral density is equal to $\overline{vv^*} = 2kTR$, expression that is valid up to 10^{12} Hz [67]. The open circuit voltage v_{rms} equivalent to the total power due to random noise results from the integration of the power spectral density from $-f$ to f, with f approaching infinity. The voltage v_{rms} is given by $v_{rms} = \sqrt{4kTRB}$, where B is the bandwidth under consideration. Thermal noise power spectrum is independent of the material and measurement frequency and varies only with temperature and electrical resistance. Thermal noise in a resistor of value R is measured by the mean square value of the noise voltage v_d on its terminals or by the mean square value of the noise current i_d through the resistor:

$$\overline{v_d^2} = 4kTR\Delta f \tag{2.18}$$

$$\overline{i_d^2} = 4kT\frac{\Delta f}{R} \tag{2.19}$$

where T is the absolute temperature, k is the Boltzmann's constant and Δf is a small bandwidth at frequency f, in Hertz, under measurement.

Equation (2.19) is derived from (2.18) by the substitution of v_d by $R \times i_d$. For a signal u, the mean square value $\overline{u^2}$ is equal to the square of its RMS value u_{rms}, $\overline{u^2} = u_{rms}^2$.

Shot noise is a white noise that occurs when there is a flow of DC due to carriers crossing a potential barrier such as a p-n junction or a Schottky barrier. Shot noise is not found in linear devices and is expressed as:

$$\overline{i_n^2} = 2qI_{DC}\Delta f \tag{2.20}$$

I_{DC} is the DC flowing through the device and q is the charge of the electron (1.6×10^{-19} C). In bipolar transistors and in SiGe HBTs, shot noise is generated by the base current and the collector current. In MOSFETs, shot noise is dominant when the device is in the subthreshold region.

Flicker noise or 1/*f* noise is found in all active devices and in some passive components such as carbon resistors [68]. It is caused by traps and by crystal defects and its spectrum density is inversely proportional to the frequency. Flicker noise is expressed by:

$$\overline{i^2} = K_1 \Delta f \frac{I_{DC}^a}{f^b} \tag{2.21}$$

where f is the frequency, K_1 is a constant for a particular device, a is a constant between 0.5 and 2 and b is a constant close to unity.

2.7 PASSIVE COMPONENTS

Passive components are essential in most RF electronic systems. They can be distributed, such as for transmission lines and waveguides, or they can be made of lumped elements such as resistors, inductors, capacitors, transformers and baluns. Passive components are used for matching networks, for filtering, for signal attenuation, for decoupling, for LC tank circuits and for biasing circuits [69]. Distributed passives are used when the phase shift due to the propagation of the signal cannot be neglected. They are therefore used in high-frequency applications and achieve higher quality factors compared to lumped passives. Lumped passives are discrete components whose size is much smaller than the wavelength of the operating frequency. A good approximation in RF design consists in using a discrete component whose maximum dimension is less than $\lambda/20$ [70]. However, it appears that there is no consensus, since in [71] it is proposed to perform lumped-element analysis for components with a maximum dimension of less than $\lambda/10$.

Despite several years of research, RF passive components such as inductors and capacitors fabricated in standard Si processes have failed to achieve high Q-factors because of parasitic losses. The typical value of the Q-factor of an integrated inductor in a BiCMOS process or bipolar processes is 10 [69]. This value can be increased by the use of complex processing steps (such as the removal of Si under the inductor or the implementation of an insulation layer between the inductor and the Si) up to 20 and 30. However, a Q-factor better than 30 is desired for the RF front end in most wireless applications [72].

Three types of implementation of inductors are generally found for Si LNAs: off-chip inductors, short-stub transmission lines and on-chip spiral inductors. High Q-factor values can be achieved with an off-chip inductor for matching and degeneration [73]. However, depending on the package, the bondwire parasitic inductance can be higher than 0.5 nH and is not well controlled during the wire bonding process. The inductance of the bondwire can become comparable to the LNA input inductance at mm-wave frequencies, rendering the use of off-chip inductors impossible. At mm-wave frequencies (30 GHz to 300 GHz), transmission lines are the most frequently used passive components in III-V technologies. However, they consume large chip areas, hence are prone to high loss and are not adapted to low-frequency (e.g. 1 GHz) applications.

2.7.1 Off-chip inductors

Off-chip inductors achieve high Q and can be used as output loads, for degeneration and for input matching. At mm-wave frequencies, the value of the off-chip inductor can be comparable to the inductance of the bondwire, a typical value being 0.5 nH. The inductance of the bondwire depends on the package and is not easily controlled. Therefore, the use of off-chip inductors does not provide acceptable controllability at mm-frequencies. For lower frequencies, the bond-wire inductance can be neglected when the inductance of the off-chip inductor is relatively high.

2.7.2 On-chip inductors

Conventional on-chip inductors are planar spiral devices implemented on a single metal layer. The cross-section and the equivalent circuit of a square spiral inductor are shown in Figure 2.11 [75]; a simplified equivalent circuit is provided in [76].

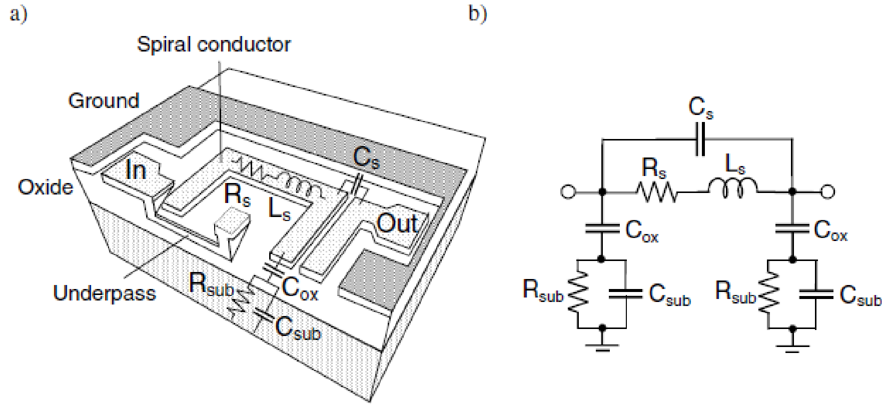


Figure 2.11. Spiral inductor: a) Cross-section, b) Equivalent circuit.

Taken from [75], with permission.

The inductance value is L_s, the resistance of the spiral is R_s, C_s is equivalent capacitance between the lines of the spiral and the centre-tap underpass. The spiral lines are coupled to the substrate through the oxide capacitance C_{ox} and the substrate resistance R_{sub} and capacitance C_{sub}. Theoretically, substrate losses are nil when the substrate resistance is nil or infinite, which results in zero voltage or zero current, hence zero losses. With L_s and R_s, the other two parameters that characterise the inductor are the quality factor Q and the self-resonance frequency f_{SR}.

The mathematical expressions of L_s and R_s are used for initial approximation as their approximation error can attain 25%. Generally, their values are obtained by measurements or simulations with computer-aided design (CAD) tools, such as ADS, SpectreRF, MW office and Genesys.

The quality factor can be approximated by (2.22), when the skin effect is neglected and one terminal of the inductor is grounded, as in the model in [76].

$$Q = \frac{\omega L_S}{R_S} k_{SL} k_{SR} \tag{2.22}$$

where k_{SL} is the substrate loss factor, $k_{SL} \leq 1$ and k_{SR} is the self-resonance loss factor with $k_{SR} \leq 1$.

The expression of the quality factor of a spiral inductor based on the S-parameters for a two-port configuration, with no grounded port, is provided in [74].

It can be shown that, at low frequencies, losses resulting in a low Q are due to R_s while at high frequency, losses are due to substrate coupling through C_{ox} and R_{sub}. Hence, at such frequencies, Q is improved by increasing the distance d_{ms} between the spiral conductor and the substrate. At low frequencies, losses decrease with the increase of the spiral conductor width and thickness. Trade-off between size and performance are required for the improvement of the quality factor. Substrate losses can be reduced by a shielding plate between the spiral and the substrate that prevents the penetration of the magnetic field from the spiral into the substrate. Other techniques to improve performance include a Si on insulator (SOI), MEMS, low dielectric metal stack and copper metal. Possibilities of trade-offs in the design of inductors in RF ICs are improved by the use of several inductor geometries that depart from the square geometry. Circular inductors achieve higher Q compared to octagonal and square inductors.

At low frequencies, the noise due to an on-chip inductor is mainly due to the series resistance R_s. It is shown in [77] that this noise is equal to the thermal noise of a resistance of value $Q^2 R_S$. Hence, the equivalent noise current of the inductor decreases when Q increases.

2.8 OTHER FACTORS AFFECTING THE NF OF AN LNA

The major sources of noise for integrated LNAs have been investigated. At low frequencies, the noise due to integrated capacitors can be neglected. Other sources of noise include the package parasitics [78] and substrate effects. Substrate effects are due to the isolation between components implemented on the same Si substrate, which is not ideal. Parasitic substrate couplings can increase the NF and create feedback paths that may affect the gain. The circuit can oscillate when the feedback is positive [75].

2.9 NF OPTIMISATION TECHNIQUES

One of the most important requirements in LNA design, in terms of noise performance, is to achieve an optimum noise impedance Z_{sopt} that is as close as possible to the source impedance. The concepts of minimum achievable noise factor F_{min}, of optimum noise impedance Z_{sopt}, of optimum noise admittance $Y_{sopt} = (B_{sopt} + jG_{sopt})$ and of noise resistance R_n are introduced in this section and presented in detail in Chapter 4. Generally, the impedance of the source R_s is fixed and the designer must insert a matching circuit between the signal source and the input transistor. For narrow-band LNAs, the matching circuit is simple and perfect matching can be achieved at the centre of the frequency band. For broadband LNAs, the process is much more complicated, as it is impossible to attain perfect matching over the whole frequency band. A mismatch must then occur in the LNA bandwidth.

Under similar power constraints, the inductively degenerated LNA achieves impedance and noise matching with the best noise performance. This topology has therefore been subject to considerable research and several impedance and noise optimisation techniques have been proposed. These techniques are mainly based on the two-port noise theory and on the technique proposed by Shaeffer and Lee in 1997 for CMOS processes. The following paragraphs provide an overview of these techniques. A comparative summary of noise optimisation techniques is provided in Table 2.4.

Table 2.4. Noise optimisation techniques for LNAs.

Criteria	Voinigescu	Shaeffer and Lee	Andreani and Nguyen	Recent approaches	Two-port noise theory	This work
Technology	BJT, SiGe HBT	CMOS	CMOS	SiGe HBT	ANY	SiGe HBT
Topology	IDCE	IDCS	IDCS, shunt capacitor between the gate and the source	IDCE, shunt inductor and capacitor at the input	ANY	Modified cascode IDCE
Matching	Noise and Impedance	Noise and Impedance	Noise and Impedance	Noise and Impedance	Noise and Impedance	Noise and Impedance
Design constraints	None	Power, fixe transistor size	Power consumption	None	None	None
Limitations	Narrow bandwidth	Matching for small transistor sizes, narrow bandwidth	Narrow bandwidth	Narrow bandwidth	For analysis, no topology, can lead to complex expressions	High power consumption: transistor paralleling
Advantages	Noise matching by transistor sizing	Power consumption is a design variable	Matching for small transistor sizes	Matching at high frequencies	Allows determing matching parameters	Broad bandwidth

2.9.1 Voinigescu technique

Voinigescu has investigated HBT noise models and proposed to extract HBT noise parameters from the measurement of Y-parameters instead of on-wafer measurements. His model has provided the expressions of R_{sopt}, X_{sopt}, R_n, F_{min} and was validated by simulations and measurements that resulted in a design method [79]. The noise resistance was matched by varying the length of the emitter, while impedance matching was performed by the emitter and base inductances. Both inductances allowed cancelling out the input reactance at resonance. As proof of concept, four designs where realised with operating frequencies from 1.9 GHz to 5.8 GHz, using a 0.5 μm SiGe HBT process. An input return loss of -30 dB and a gain of 10 dB to 15 dB were reached. The NF was close to the minimum achievable NF.

2.9.2 Shaeffer and Lee's technique

Power consumption is a new design constraint added to this model, which was developed for a CMOS process and which is based on Shaeffer and Lee's paper of 1997 [80]. The overdrive voltage of the MOS transistor was chosen to achieve the best noise performance at a given power consumption and the transistor size determined. The gate and source inductors were used for input matching, with the gate inductor being off-chip. The design was demonstrated with a 0.6 μm process, achieving a gain of 22 dB at a power consumption of 7.5 mW. To this author's knowledge, the lowest NF attained by a CMOS process at room temperature was reported in [8]. This design is based on Shaeffer's technique and achieves an NF of 0.2 dB.

2.9.3 Andreani and Nguyen's technique

The main limitation of the design method of Shaeffer and Lee is the difficulty of performing simultaneous noise and impedance matching when the transistor size decreases [81]. In such a case, the real part of the optimum noise impedance increases faster than the

real part of the input impedance and both quantities cannot be matched. However, these quantities can be matched by the addition of a shunt capacitance between the gate and the source. The design method was validated by a 0.25 µm CMOS process LNA operating at 900 MHz and achieving satisfactory NF, gain and input return loss [55]. A similar technique for bipolar technology was firstly introduced by Girlando and Palmisano in 1999 [40]. The technique achieves noise and impedance matching for common-emitter amplifiers and is based on the addition of a shunt capacitor between the base and the emitter of the input transistor.

2.9.4 Classical two-port noise theory

The classical two-port noise theory, which has little been used in the design of LNAs since its presentation in 1960 [2], allows one to investigate how the NF varies with the source resistance and to introduce the concepts of the achievable minimum noise factor F_{min}, of noise resistance R_n, optimum source conductance and susceptance G_{sopt} and B_{sopt}, with $G_{sopt} + jB_{sopt} = Y_{sopt}$, Y_{sopt} being the source admittance for which the noise is optimum. These parameters, known as the four noise parameters, provide the source impedance R_{sopt} for which the minimum NF is achieved [2]. The two-port noise theory allows determination of F_{min} and the matching conditions, including R_n, the sensitivity of the noise factor to variations of the impedance of the source related to Y_{sopt}. In the case of networks comprising several noise sources, the determination of the NF can be complicated, because of the existence of a correlation component between the voltage and current noises reported to the input. The two-port noise theory approach may lead to cumbersome equations that do not provide insight. The total noise can then be determined by considering the contribution of each noise source to the total output noise of the amplifier and other design methods are required to determine the optimum noise conditions.

The two-port noise theory requires that the impedance of the source matches the optimum noise impedance of a device with fixed characteristics. Generally, this is not possible as the impedance of the source is standardised. In most cases, a matching network is required between the source and the amplifying device, which constitutes a limitation of this

technique. This limitation is overcome as the optimum noise resistance is adjusted to match the impedance of the source by varying the length of the emitter, a technique that is addressed in Chapter 4. It is shown in Chapter 4 that the limitation is also overcome, in particular conditions, by the use of a shunt capacitor. Using the two-port noise theory, the LNA designed in [82] achieves an NF of 0.9 dB at 800 MHz.

2.9.5 Recent approaches

The design of a SiGe HBT LNA using an IBM 0.12 µm process operating in the K_a band (35 GHz) has shown that for high frequencies, the imaginary parts of the input impedance and of the optimal noise impedance, X_{in} and X_{opt}, do not match when a series-series feedback configuration is used through the emitter inductor [83]. The mismatch is caused by the Miller effect, which cannot be neglected at high frequencies. This can be resolved by the use of a shunt capacitor and a shunt inductor connected to the base. Similar to previous cases, matching is obtained by the use of a feedback inductor, a series inductance in the base and a shunt external capacitance and inductance at the input [84].

2.10 CONCLUSION

The main requirements pertaining to the design of cost-effective highly sensitive receivers have been investigated. The sensitivity of a receiver is related to the NF of its LNA and to its power gain. Performance criteria such as the dynamic range, the linearity and stability, although important to ensure an accurate reproduction of the input signal to the output of the receiver, do not affect directly the sensitivity. The review of the literature has shown that three types of receptor are expected: aperture arrays for low frequencies and 10 to 15 m dishes with focal plane arrays or with wideband feeds. The types of receptor indicate that differential and single-ended LNAs are required. The received signal spans from 70 MHz to more than 25 GHz, a frequency range that is divided in three bands, each band depending on the SKA science drivers to be investigated. The noise temperature expected at 1.4 GHz is 16 K, corresponding to a NF of 0.23 dB.

The NF of a receiver being mainly related to its active components and topology, semiconductor technologies and topologies that are relevant to receivers in radio astronomy were discussed. In terms of semiconductor technologies, InP processes perform exceptionally well with regard to noise performance but their level of integration is low and their cost high. SiGe HBT processes outperform BJT and CMOS processes regarding noise performance, at the same level of integration (high) and cost (low). The SiGe HBT technology used in this work is a fourth generation process, with a peak f_T of 200 GHz. Topologies for LNAs were investigated, the IDCE in a cascode configuration was identified as the desired topology for a narrow-band highly sensitive receiver at room temperature.

The noise performance of an integrated LNA is also affected by its passive components, mainly by on-chip inductors. The quality factor of on-chip inductors being in the range of 10 while quality factors better than 100 are achieved by off-chip inductors, the use of different geometries for on-chip inductors, of off-chip inductors and of bondwires as circuit elements, was investigated.

The performances of LNAs for SKA demonstrators are provided in Table 2.2. The table provides, among other parameters, the noise temperature, the power gain and the frequency bandwidth that were achieved and allow to relate the noise performance to the semiconductor technology and to the operating temperature used. A sub-1 dB NF LNA, fabricated in a 90 nm CMOS technology, has been reported in [8]. The considerable improvement of the performances of SiGe HBTs suggests that SiGe HBT based LNAs of a comparable transistor size may achieve sub-1 dB NF at room temperature.

CHAPTER 3 RESEARCH METHODOLOGY

"To no small degree, an important lesson in RF and microwave design is that there are always irreducible parasitics. Rather than conceding defeat, one must exploit them as circuit elements."

- Thomas Lee

3.1 INTRODUCTION

A preliminary high-level methodology for this research has been presented in Figure 1.2. The preliminary methodology indicates that the main findings of this research are expected to lead to the design and fabrication of a sub-1 dB NF SiGe HBT-based LNA. The design phase is the result of numerous investigations that are related to the main performance metrics of an LNA and to its physical implementation. This chapter presents the detailed methodology that was used throughout this research.

In order to test the research hypothesis provided in Chapter 1 of this work, a review of the literature was first done in Chapter 2. The literature review, which is the first phase of this research, has allowed determination of the specifications of SKA receivers, the performance metrics of LNAs, the advantages of SiGe HBT technology and relevant LNA topologies. The research methodology used constitutes developing an approach, based on a theoretical study, which establishes how the noise performance of an LNA is related to its topology, the semiconductor fabrication process, on-chip passive components and external parameters, such as temperature and supply voltage. The theoretical study was validated by simulation and expected to be further validated by prototyping and measurements.

It has been found that the IDCE cascode topology is desired. The topology being determined, the research methodology has entailed investigations into the following topics:

- Electronic noise in two-port networks.
- The IC process.
- Noise modelling in SiGe HBTs and passive components.
- Noise in SiGe HBT CE and cascode amplifiers.
- Noise in IDCE amplifiers.
- Noise matching.
- Input impedance matching.
- Output impedance matching.
- CAD tools for modelling, simulation, optimisation and layout.
- Simulation (NF, gain, linearity, impedance matching, corner, Monte Carlo (MC)).
- Considerations for process, voltage and temperature variations.
- Layout.
- Fabrication.
- Measurements.

The outline of the research methodology is depicted in Figure 3.1, where the design flow is performed in successive phases leading to layout, fabrication and measurements. This process is supported by Cadence design tools and by MATLAB™ scripts.

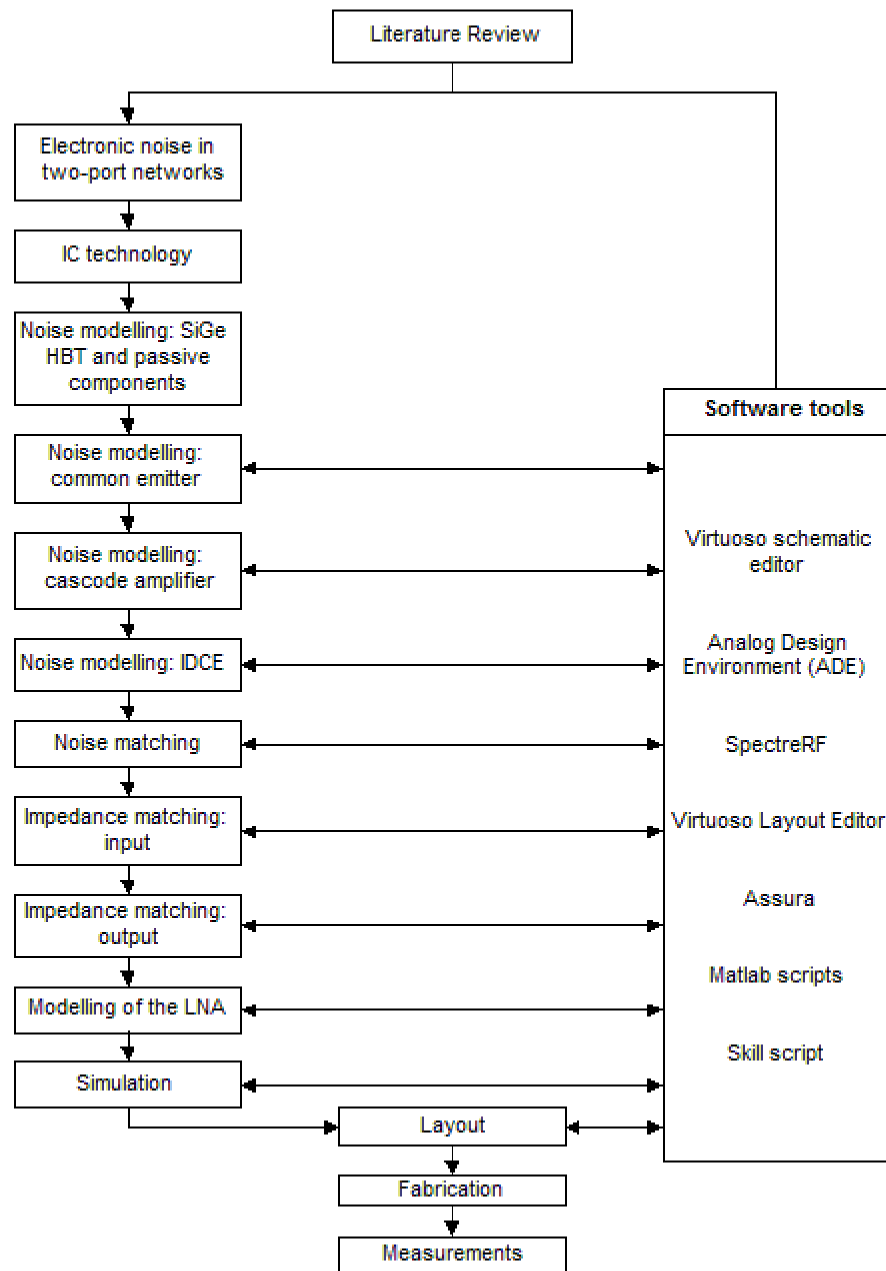


Figure 3.1. Research methodology.

3.2 ELECTRONIC NOISE IN TWO-PORT NETWORKS

The concepts of minimum achievable noise factor F_{min}, noise resistance R_n, optimum source conductance G_{sopt} and susceptance B_{sopt}, developed by the two-port noise theory, were used for noise matching, allowing the researcher to achieve the minimum possible

noise factor at the high end of the frequency bandwidth. The two-port noise theory is presented in Chapter 4 of this thesis.

3.3 THE INTEGRATED CIRCUIT PROCESS

The IBM SiGe 8HP BiCMOS technology, a third-generation SiGe process, was used. The process achieves a peak f_T of 200 GHz and has a CMOS gate length of 0.13 µm. The noise performance of the LNA is strongly related to the process and the same design methodology leads to different noise performances when applied to different processes. The results are different for the following reasons:

- Noise performance is related to the unity gain frequency f_T and to the current gain β of transistors, which are process-dependent.
- The parasitic resistances, such as the base resistance r_b and emitter resistance r_e, are significant to the noise performance.
- Noise in integrated passive components such as inductors is caused by parasitic resistances, losses caused by the skin effect and Eddy currents and substrate losses that are process-dependent.

The details of the IC process [85] cannot be unveiled due to a non-disclosure agreement (NDA) with the foundry. The main features of the IC process are:

- It is a BiCMOS process with high-breakdown and high-performance NPN transistors (f_T up to 200 GHz).
- It has a minimum collector-emitter breakdown voltage (BV_{CEO}) of 3.1 V and 1.5 V respectively for high-breakdown and high-performance NPN transistors.
- It has two configurations for NPN transistors, CBE and CBEBC, the former being the preferred configuration.

- The fixed width of the emitter is 0.12 μm. The emitter length is scalable, from 0.52 μm to 18 μm.
- Three types of capacitors are available: MOS varactors, hyper-abrupt junction diode varactors (HA varactors) and metal-insulator-metal (MIM) capacitors.
- Four types of resistors are available: OP P+ polysilicon resistors, RR polysilicon resistors for high resistance, N+ diffusion resistors and tantalum nitride metal resistors at the uppermost thin metal level.
- Scalable spiral inductors and transmission lines are available.
- It contains up to seven layers of metal: thin copper layers for M1 to M4, a thick copper layer MQ and two top thick aluminium layers, LY and AM, for RF wiring.
- Wirebond pads and C4 pads for ball grid arrays are supported.
- The operating junction temperature range is -55 to 125 ℃.

3.4 NOISE MODELLING FOR SIGE HBTS AND PASSIVE COMPONENTS

The noise model of SiGe HBTs was used to derive the two-port noise model of a single CE transistor amplifier. Noise in a passive inductor is caused by its series and shunt resistances – from its lumped-elements model – and by electromagnetic energy leaks into the substrate. To the best knowledge of the author, a general noise model for spiral inductors has yet to be published. It is assumed in this work that the noise resulting from substrate losses can be neglected and that the noise due to an inductor is mainly thermal and is caused by its series resistance.

3.5 NOISE FOR SIGE HBT CE AND CASCODE AMPLIFIER

The analytical expression of the NF of a common-emitter SiGe HBT has been used to relate noise performance to the parameters and the biasing of the transistor. This has shown

that the NF is related to the collector current and the size of the transistor. It was also shown that NF is directly related to the length of the emitter and weakly related to the width of the emitter. The findings have allowed derivation of a noise matching technique without additional components and without degradation of the noise performance of the transistor of minimum size in the IC process. The findings have also allowed the derivation of parameters and biasing conditions required for minimum NF for a cascode amplifier using the software tools Virtuoso schematic editor, Analog Design Environment (ADE) and SpectreRF from Cadence Design Systems.

3.6 NOISE FOR THE IDCE AMPLIFIERS

It was identified by the review of the literature that the desired topology was the IDCE owing to the possibility of achieving simultaneous noise and impedance matching. The expression of the NF for the IDCE was used to derive the matching conditions based on the two-port noise theory. The results were applied to the IDCE in a cascode configuration and verified by simulation with SpectreRF.

3.7 INPUT IMPEDANCE MATCHING

Although the IDCE amplifier can achieve an NF that is close to the best possible noise performance, input impedance matching is narrow-band. Therefore, a technique to improve the input impedance matching with minimum impact on NF was investigated and developed. This technique was validated by simulation with SpectreRF.

3.8 OUTPUT IMPEDANCE MATCHING

An efficient transfer of RF power to the output load is desired. For this purpose, the output impedance of the IDCE cascode amplifier must be matched to the resistive load through a matching network. A wideband output matching network was investigated. A MATLAB™ script was used to optimise the values of the reactive components of the network for maximum power transfer.

3.9 LAYOUT AND FABRICATION

Floor planning was performed in order to determine the preferred locations of the components of the LNA on a Si chip while optimising its area and limiting possible undesired coupling between RF signals. The fabrication of the IC was sponsored by Metal Oxide Semiconductor Implementation Service (MOSIS) [86] and was part of a multi-project wafer (MPW); the approach was supported through the MOSIS Education Programme (MEP).

3.10 MEASUREMENTS AND EQUIPMENT

Measurements setup includes the E4440 Spectrum Analyser from Keysight Technologies, the Rohde & Schwarz Vector Network Analyser (VNA) ZVA40 and the fabricated printed circuit board. The setup and the experimental results are provided in Chapter 7.

3.11 CONCLUSION

The research methodology was presented in this chapter. The IC process used was discussed, as well as the main research steps required to verify the research hypothesis. These steps, presented and discussed in detail in Chapter 4 and referred to as theoretical analysis, include noise modelling of active and passive components, cascode amplifiers and the proposed noise and impedance matching techniques. The remaining steps of the research methodology and the software tools used for design, simulation and optimisation of the LNA were also discussed.

CHAPTER 4 THEORETICAL ANALYSIS AND DESIGN METHODOLOGY

4.1 INTRODUCTION

The objectives of this chapter are to investigate how the NF of an LNA is related to its active and passive components and to its topology. The theoretical analysis of the NF provided in this chapter allows selection of the topology of the amplifier, identification of the impact of semiconductor technology to noise, and derivation of noise matching conditions. The requirements for power matching are also developed and are shown to be applicable only to narrow-band conditions, which is not in line with bandwidth requirements for the LNA. An analysis of possible techniques improving the bandwidth with limited impact on noise is provided. A technique to increase the bandwidth of the LNA with minimum impact on the NF is then developed. The technique relies on the parasitic capacitance between the base and the collector of the input transistor to increase the bandwidth of the LNA by coupling two resonant circuits.

4.2 NOISE FUNDAMENTALS

A review of noise fundamentals is done before investigating how the NF of a transistor amplifier is related to its design parameters and how the NF can be minimised.

4.2.1 Signals and noise

A signal is a representation of electrical energy when propagating through a circuit. Usually, a signal is used to transmit information. A signal is deterministic when it can be expressed as a function of time; it is stochastic when its values are random in time. The

latter is the case of electronic noise: noise current and noise voltage vary randomly with time, but their statistical characteristics are invariant in time. Electronic noise can be defined as any unwanted stochastic disturbance that can interfere with a desired signal.

The generation of electronic noise is a random process and the study of noise physics entails statistical analysis. Signals and noise can be characterised by the peak value, the mean value, the mean square value, the RMS value and the correlation coefficient. The correlation coefficient between two voltages v_a and v_b is defined by $c = \overline{v_a v_b} / (v_a)_{rms} (v_b)_{rms}$, where the numerator represents the mean value of the product $v_a v_b$ and the terms $(v_a)_{rms}$, $(v_b)_{rms}$ are respectively the RMS values of v_a and v_b.

Because electronic circuits process noise similarly to electronic signals, the principles of signal analysis, of circuit theory, of Fourier transform and of transfer function can be used in noise analysis. Several definitions of noise parameters have emerged, sometimes for the same quantities, because of the various disciplines that involve noise analysis. The definitions found in [68] are used in this thesis.

4.2.2 Two-port noise model

The input signal S_i and noise N_i of a transistor amplifier are subject to the same amplification. The output signal S_o and noise N_o are related to S_i and to N_i by G, the power gain of the amplifier, as shown by (4.1) and (4.2).

$$S_o = GS_i \tag{4.1}$$

$$N_o = GN_i \tag{4.2}$$

The intrinsic noise of the transistor propagates toward the output and degrades the SNR of the amplifier. The degradation is measured by the noise factor, F, which is defined by:

$$F = \frac{S_i}{N_i} \frac{N_o}{S_o} \tag{4.3}$$

Equation (4.4) is derived from (4.3):

$$F = \frac{S_i}{N_i} \frac{N_o}{S_o} = \frac{N_o}{GN_i} \tag{4.4}$$

The noise factor F of the noisy two-port amplifier is given by (4.5):

$$F = F_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{sopt}\right|^2 \tag{4.5}$$

In (4.5), F_{min} is the minimum achievable noise factor of the noisy amplifier, R_n is the noise resistance, Y_s is the source admittance ($Y_s= G_s+jB_s$) and Y_{sopt} is the optimum source admittance. F_{min}, R_n, B_{sopt} and G_{sopt} are the four noise parameters of any two-port noise model, describing completely its behaviour in terms of noise performance. The noise resistance R_n determines the sensitivity of F to deviations of the source admittance from Y_{sopt}. The derivation of (4.5) is provided in Addendum A.

4.2.3 Relation between minimum noise factor and input referred noise sources

It is desired to express the minimum achievable noise factor in terms of the noise parameters of the two-port network. F_{min} is related to the input referred noise current i_n and noise voltage v_n of the two-port network by (4.6). Details of the derivation of (4.6) are provided in Addendum A.

$$F_{\min} = 1 + \frac{\overline{v_n^2}}{2kT}\left(\sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - \mathrm{Im}\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}} + R_e\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}\right) \tag{4.6}$$

4.2.4 Noise correlation matrix

A chain representation of the electrical parameters of the two-port network has been used to derive (4.5). Z-, Y- or H-parameter representations can equally be used for noise analysis. The values of input referred noise sources are related to the Z-, Y- or H-parameters of the two-port network and can be performed as shown in this section. There are six possible configurations of noise sources relative to a noiseless network that can represent any noisy two-port network. In practice, only the three configurations in Figure 4.1, Figure 4.2 and Figure 4.3 are used.

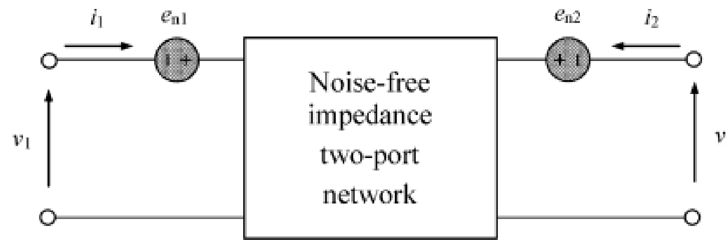


Figure 4.1. Impedance configuration.

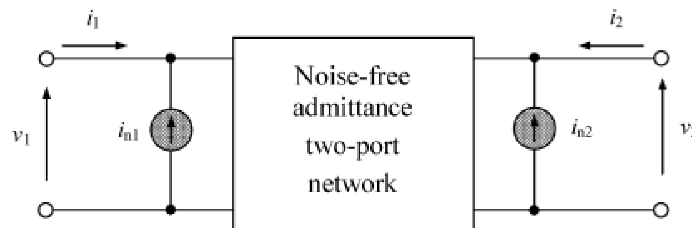


Figure 4.2. Admittance configuration.

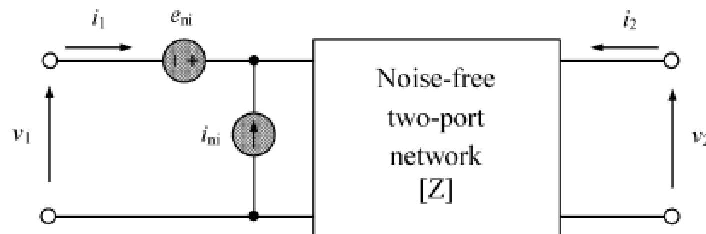


Figure 4.3. Chain representation with Z-parameters.

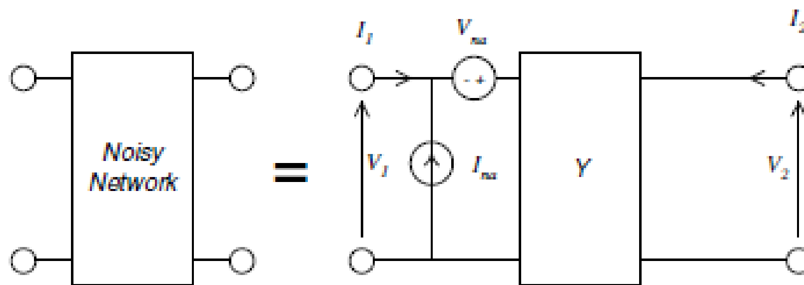


Figure 4.4. Chain representation with Y-parameters.

The noiseless parts of the networks in Figure 4.1, Figure 4.2, Figure 4.3 and Figure 4.4 can be represented by the Z-, Y- and H-parameters.

Using Y-parameters, the voltages and currents in Figure 4.4 are related in the frequency domain as follows:

$$\begin{pmatrix} I_1 + I_{na} \\ I_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 + V_{na} \\ V_2 \end{pmatrix} \tag{4.7}$$

where I_1, V_1 respectively I_2, V_2, are the Fourier transforms of the current and voltage at the input and output.

In some sections of this thesis, noise correlation matrices are used; it is then important to introduce the concept of the noise correlation matrix. Traditionally, noise sources are replaced by sinusoidal sources of the same power that are used to perform AC analysis for noise power calculations. This method is simple but is restricted to cases where noise sources are uncorrelated or totally correlated. A method that can be used in most cases entails representing each noise source by a linear combination of uncorrelated and correlated sources. However, the method can lead to complicated calculations. Moreover, it does not provide a simple solution for the calculation of the minimum possible noise factor F_{min} and the source impedance required for noise matching.

In the correlation matrix method, a two-port network is derived from basic two-port networks with known characteristics. In Figure 4.1, Figure 4.2 and Figure 4.3, the two-port noise networks are fully characterised by their correlation matrix C, whose elements are the self- and cross-power spectral densities of their noise sources in the bandwidth Δf centred in f, the operating frequency. The correlation matrix of two noise sources, v_n and i_n is by definition a 2×2 matrix whose elements are the self- and cross average powers of the noise sources, as shown in (4.10).

The self- and cross-power densities of the noise sources are the Fourier transforms of the self- and cross-correlation functions of the noise sources. The power spectral density of a signal with $F(j\omega)$ as Fourier transform is expressed by $S_\omega = \frac{1}{2\pi}\left|F(j\omega)\right|^2$.

The cross-power spectral density of two signals $s_1(t)$ and $s_2(t)$ of Fourier transforms S_1 and S_2 is defined as the Fourier transform of their cross-correlation function:

$$S_f(s_1,s_2) = \mathrm{F}[R_{s1s2}(\tau)] \tag{4.8}$$

The cross-correlation function of $s_1(t)$ and $s_2(t)$ is defined as follows:

$$R_{S_1S_2}(\tau) = \lim_{T\to\infty}\frac{1}{2T}\int_{-T}^{T} s_1(t)s_2(t+\tau)dt \tag{4.9}$$

For the noise sources v_n and i_n in Figure A.2 from Addendum A, the correlation matrix is shown in (4.10).

$$\xi_A = \begin{bmatrix} \xi_{A11} & \xi_{A12} \\ \xi_{A21} & \xi_{A22} \end{bmatrix} = \frac{1}{2\Delta f} \begin{bmatrix} \overline{v_n v_n^*} & \overline{v_n i_n^*} \\ \overline{v_n^* i_n} & \overline{i_n i_n^*} \end{bmatrix} \tag{4.10}$$

The normalised chain correlation matrix C_A is defined by:

$$\xi_A = 2kTC_A = 2kT \begin{bmatrix} C_{A11} & C_{A12} \\ C_{A21} & C_{A22} \end{bmatrix} \tag{4.11}$$

$$\begin{bmatrix} C_{A11} & C_{A12} \\ C_{A21} & C_{A22} \end{bmatrix} = \frac{1}{4kT\Delta f} \begin{bmatrix} \overline{v_n v_n^*} & \overline{v_n i_n^*} \\ \overline{v_n^* i_n} & \overline{i_n i_n^*} \end{bmatrix} \tag{4.12}$$

The subscript A in C_A refers to the chain representation, the asterix refers to the complex conjugate and the matrix terms $\overline{v_n v_n^*}$, $\overline{v_n i_n^*}$, $\overline{v_n^* i_n}$ and $\overline{i_n i_n^*}$ are the self- and cross-correlation terms between the noise sources referred to the input and are functions of the frequency f.

The mathematical characteristics of the correlation matrix are as follows [68]:

1- The diagonal elements are real: $\text{Im}\{C_{11}\} = \text{Im}\{C_{22}\} = 0$; this is valid for impedance, admittance and chain representations.

2- Elements C_{21} and C_{12} are complex conjugate, hence $C_{21} = C_{12}^*$.

3- The diagonal elements C_{11} and C_{22} are greater than or equal to zero ($C_{11} \geq 0$ and $C_{22} \geq 0$).

4- The determinant of C is greater than or equal to zero: $\det\{C\} = C_{11}C_{22} - |C_{12}|^2 \geq 0$.

In cases where all noise sources are current sources, the elements of the correlation matrix can be determined using the following procedure:

1- C_{11} is equal to the sum of noise sources connected to node 1, the input, C_{22}, is equal to the sum of the node current connected to node 2, the output.

2- C_{12} and C_{21} are negative and equal to the noise source connected between node 1 and node 2.

3- A grounded noise source contributes to only one element in the diagonal of the matrix. A source that is not grounded contributes to all elements of the correlation matrix.

The elements of the correlation matrix can also be obtained by using the equations of the correlation matrix for a two-port network with only passive elements:

$$C_z = 2kTRe\{Z\} \tag{4.13}$$

$$C_y = 2kTRe\{Y\} \tag{4.14}$$

where k is the Boltzmann constant and T is the absolute temperature.

Basic two-port networks can be interconnected in parallel, in series or in cascade to form more elaborated two-port networks. This technique is well adapted to computer-based noise analysis. Noise sources from separate two-port networks are uncorrelated. Therefore, the correlation matrix C_Y of two parallel two-port networks C_{Y1} and C_{Y2}, each network in admittance configuration, can be expressed by the equation:

$$C_Y = C_{Y1} + C_{Y2} \tag{4.15}$$

For two-port networks in series C_{Z1} and C_{Z2}, each using the series configuration, the resulting correlation matrix is expressed by the equation:

$$C_Z = C_{Z1} + C_{Z2} \tag{4.16}$$

In the case of two two-port networks in cascade, of correlation matrices C_{A1} and C_{A2}, each in a chain representation, the correlation matrix of the resulting cascade network is represented by (4.17):

$$C_A = A_1 C_{A2} A_1^* + C_{A1} \tag{4.17}$$

where A_1 is the chain or ABCD matrix of the first two-port network.

The noise factor can be calculated from C_A using the expression [87]:

$$F = 1 + \frac{Z^+ C_A Z}{2kTR_e\{Z_S\}} \tag{4.18}$$

where Z_s is the impedance of the source, $Z = \begin{bmatrix} 1 \\ Z_S^* \end{bmatrix}$ and Z^+ is the Hermitian conjugate of Z. The Hermitian conjugate Z^+ is obtained by transposing Z and converting its elements in their complex conjugates.

In cases where the Y representation is used, the noise factor can also be calculated using the expression:

$$F = 1 + \frac{YC_A Y^+}{2kTR_e\{Y_s\}} \tag{4.19}$$

where $Y = \begin{bmatrix} Y_S \\ 1 \end{bmatrix}$, Y^+ is the Hermitian conjugate of Y and Y_s is the admittance of the source.

4.2.5 Transformation between representations

The analysis of arbitrary two-port networks is simplified by their decomposition in basic two-port networks. After the decomposition, it is often desired to make transformations between series, parallel and chain representations. The transformations allow one to convert a correlation matrix C in a given representation into a new correlation matrix C' in a new representation. The new correlation matrix is obtained from (4.20), referred to as the congruence transformation:

$$[C'] = [T][C][T^+] \tag{4.20}$$

where T is the transformation matrix and T^+ its Hermitian transform.

The table of transformations matrices between impedance, admittance, hybrid and chain representations is provided in Addendum A [67]; additional information on transformation matrices in noise calculations is provided in [87].

4.2.6 Relation between noise parameters and the noise correlation matrix in chain representation

The noise resistance R_n has been defined by the expression $R_n = \overline{v_n^2}/4kT$, which is equivalent to $R_n = \overline{v_n(f)v_n^*(f)}/2kT$. The expression provides the term C_{A11} of the chain correlation matrix C_A, which is equal to $\overline{v_n(f)v_n^*(f)}$. The term C_{A22} of the correlation matrix is derived from $g_n = \overline{i_n(f)i_n^*(f)}/2kT$, with $C_{A22} = \overline{i_n(f)i_n^*(f)}$ and $g_n = R_n\left|Y_{sopt}\right|^2$.

The elements C_{A11} and C_{A22} are:

$$C_{A11} = \overline{v_n v_n^*} = 2kTR_n \tag{4.21}$$

$$C_{A22} = 2kTR_n \left|Y_{sopt}\right|^2 \tag{4.22}$$

The terms C_{A12} and C_{A21} are given by (4.22) and (4.23):

$$C_{A12} = \overline{v_n i_n^*} = 2kT\left[\frac{F_{\min} - 1}{2} - R_n Y_{sopt}^*\right] \tag{4.23}$$

$$C_{A21} = \overline{i_n v_n^*} = 2kT\left[\frac{F_{\min} - 1}{2} - R_n Y_{sopt}\right] \tag{4.24}$$

Therefore, the noise chain correlation matrix C_A is given by:

$$C_A = 2kT\begin{bmatrix} R_n & \left[\frac{F_{\min} - 1}{2} - R_n Y_{sopt}^*\right] \\ \left[\frac{F_{\min} - 1}{2} - R_n Y_{sopt}\right] & R_n\left|Y_{sopt}\right|^2 \end{bmatrix} \tag{4.25}$$

The determination of C_A is provided in Addendum A.

4.2.7 Transfer of noise sources to the input in chain representation

The transfer of noise source to the input is facilitated by the use of a chain (ABCD) representation. A two-port ABCD representation is provided by:

$$v_1 = \mathrm{A}v_2 + \mathrm{B}i_2 \tag{4.26}$$

$$i_1 = \mathrm{C}v_2 + \mathrm{D}i_2 \tag{4.27}$$

A noisy ABCD two-port network, with all noise sources placed at the output, is represented in Figure 4.5.

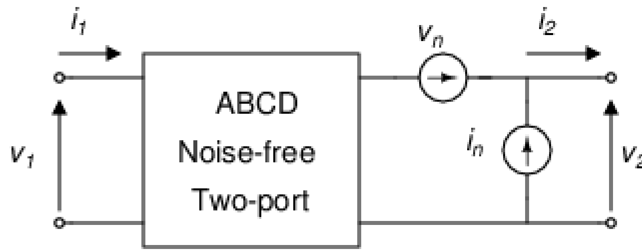


Figure 4.5. ABCD noise free network with noise sources at the output.

Equations (4.26) and (4.27) are rewritten as follows, when noise sources are considered:

$$v_1 = \mathrm{A}v_2 + \mathrm{B}i_2 - \mathrm{A}v_n - \mathrm{B}i_n \tag{4.28}$$

$$i_1 = Cv_2 + Di_2 - Cv_n - Di_n \tag{4.29}$$

Equations (4.28) and (4.29) are equivalent to two voltage noise sources in series Av_n and Bi_n at the input and two current noise sources Cv_n and Di_n at the input. The equivalent voltage and current noise source at the input are correlated. Equations (4.28) and (4.29) will be used in referring to the input the noise sources of a CE SiGe HBT.

4.2.8 Transfer of noise sources to the input–Y representation

In the case of the Y representation, noise sources can be represented by current sources at the input and output of the two-port representation as shown in Figure 4.6. This is the case of the shot noise source for the SiGe HBT.

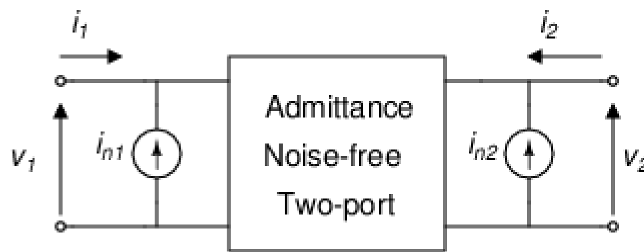


Figure 4.6. Y noise free network with noise sources at the input and output.

The admittance equations of the noise representation in Figure 4.6 are written as:

$$i_1 = Y_{11}v_1 + Y_{12}v_2 - i_{n1} \tag{4.30}$$

$$i_2 = Y_{21}v_1 + Y_{22}v_2 - i_{n2} \tag{4.31}$$

When the noise sources are reported to the input, the two-port noise model is shown in Figure 4.7, where i_{ni} and v_{ni} are the current and voltage equivalent noise sources.

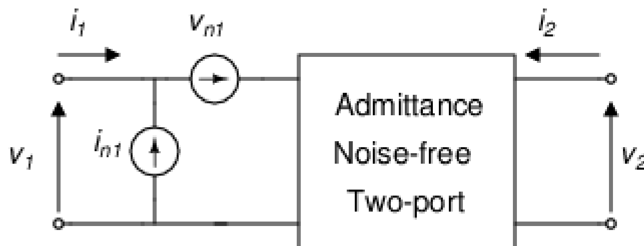


Figure 4.7. Y noise-free network with noise sources at the input.

The admittance equations in Figure 4.7 are written as:

$$i_1 = Y_{11}(v_1 + v_{ni}) + Y_{12}v_2 - i_{ni} \tag{4.32}$$

$$i_2 = Y_{21}(v_1 + v_{ni}) + Y_{22}v_2 \tag{4.33}$$

It is shown in [88] that the equivalent input voltage and current sources referred to the input are given by (4.34) and (4.35), which are derived from (4.30), (4.31), (4.32) and (4.33).

$$v_{ni} = -\frac{i_{n2}}{Y_{21}} \tag{4.34}$$

$$i_{ni} = i_{n1} - \frac{Y_{11}}{Y_{21}} i_{n2} \tag{4.35}$$

4.3 NF VERSUS CE, CC AND CB CONFIGURATIONS

It is recalled that the cascode configuration is widely used in LNA topologies owing to the following:

- Its high isolation between the input and the output, allowing independent input and output matching. When the isolation is low, the matching of the input and the output is performed alternatively until an acceptable result is obtained.
- Improved stability due to a high $|S_{12}|$.
- Its improved bandwidth owing to the reduction of the Miller effect.
- The common-emitter configuration allowing simultaneous noise and power matching.

In addition, an input transistor in common-emitter configuration allows one to minimise the noise due to the cascode transistor. The superior noise performance of the common-emitter configuration for the first stage of the LNA is understood by referring to the input of the LNA, the noise due to the second stage. It can be shown that the noise due to the second stage is low when the transfer parameters of the first stage are large. The common-emitter transistor configuration has the largest transfer parameters when compared to the common-base and common-collector configurations. Hence, the common-emitter configuration is desired for the input stage of the LNA because it minimises, among others, the input referred noise due to the second stage.

4.4 NOISE FACTOR AS FUNCTION OF THE PARAMETERS OF THE SIGE HBT

4.4.1 Small-signal model

The simplified small-signal equivalent circuit of the SiGe HBT in the hybrid-π configuration is represented in Figure 4.8 [89]. The circuit is based on the VBIC model for vertical deep-trench isolated SiGe HBTs in the forward active region, an improvement of the SPICE Gummel-Pon model widely used for bipolar transistors. Advanced compact models, such as the SPICE Gummel-Poon model (SGP) and more recently the VBIC, Mextram and HiCuM, do not lend themselves to simple analytical analysis. Simulation results from advanced and simple models are close in typical applications where current crowding effects, substrate effects, the dependence of the forward transit time, the base-collector capacitance and the output conductance to bias conditions can be neglected.

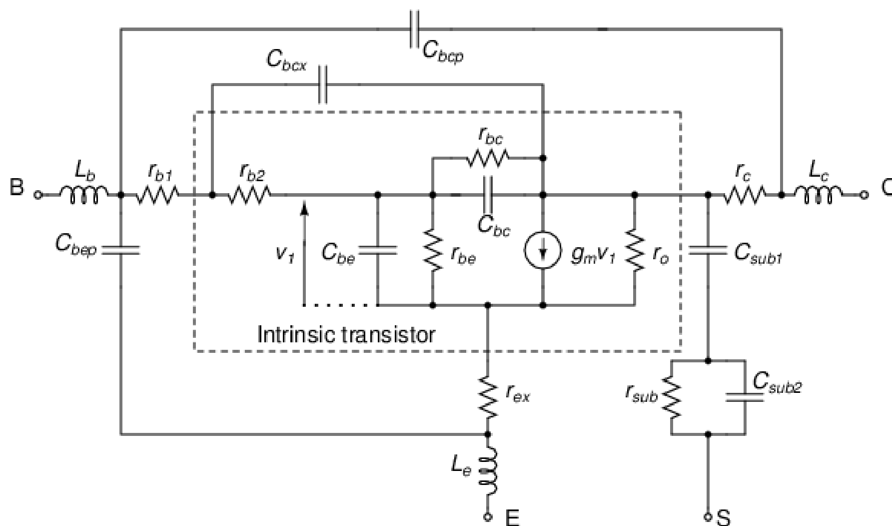


Figure 4.8. Small-signal equivalent circuit of the SiGe HBT. Adapted from [89], © 2006 IEEE.

The base resistors model distributive effets and are not completely resistive components. The resistors can be lumped together by r_b, with $r_b = r_{b1} + r_{b2}$. The error deriving from the approximation of the base thermal noise by the noise due to r_b is insignificant when the transistor is biased in the low injection regime and current crowding is insignificant [90]. Low injection regime and insignificant current crowing are achieved for biasing that are below f_T and f_{max} [91], which is the case for this work. The transconductance is given by the expression $g_m = g_{m0}\exp(-j\omega\tau_d) \approx (1 - j\omega\tau_d)qI_C/kT$, where $g_{m0} = qI_C/kT$ and τ_d is

the total base-to-collector delay time [92]. The delay time is of the order of pico-seconds. For this work, $\omega\tau_d << 1$, hence $g_m \approx qI_C/kT$. The parasitic elements C_{bcx}, C_{sub1}, C_{sub2} and r_{sub} model substrate effects. For frequencies that are much lower than the maximum f_T, the extrinsic parasitic inductances and capacitances L_b, L_e, L_c, C_{bcp} can be neglected [93]. The parasitic capacitor C_{bcx} is associated with the base-collector-substrate junctions. For frequencies below mm-wave frequencies (10 GHz), substrate couplings are not important and can be neglected [94]. The small-signal equivalent circuit in Figure 4.9 is derived from the simplifications in this paragraph.

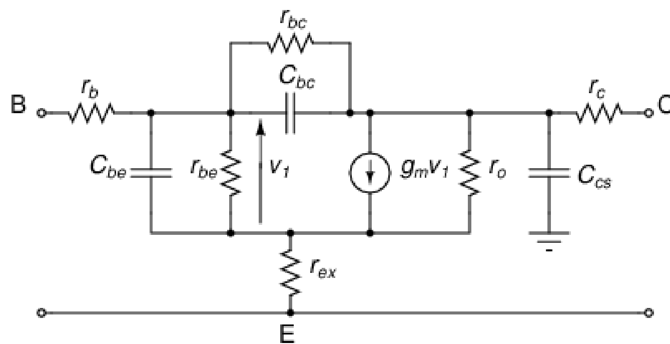


Figure 4.9. Modified small-signal equivalent circuit of the SiGe HBT.

The model in Figure 4.9 includes some extrinsic components as well as base, emitter, collector and substrate parasitic components that account for its high frequency response and noise performance. It is noted that the coupling between the collector and the substrate is represented by C_{cs}. The resistance r_{bc} relates the modulation of the neutral base recombination current to the collector-base voltage and has an insignificant impact on transfert parameters and on noise performance. The contribution of the collector parasitic resistance r_c to the input noise is reduced, owing to the gain of the transistor. Hence, r_c can be neglected. The output resistance r_o can be neglected because the Early voltage is large for SiGe HBTs.

4.4.2 Noise model

The high-frequency modelling of a transistor is not limited to its fundamental physical mechanisms because the effects of parasitic components must be accounted for. Parasitics are represented in the extrinsic model, while the fundamental physical mechanism is

modelled by the intrinsic model. The T-model provides a direct relation between model elements and the device physics, as shown in Figure 4.10 [95] and Figure 4.11 [96].

Figure 4.10. Cross-section of a small-geometry SiGe HBT. Taken from [95], with permission.

Figure 4.11. T-model equivalent circuit for SiGe HBTs.

Despite the correspondence between device physics and the components of the model, the extraction of R_{be} and C_{be} from measurements using the T-model can be difficult. The physical significance of the elements of the Π-model is ambiguous but the model provides an accurate extraction of parameters such as C_{be} and is widely used by designers and simulators. A one-to-one correspondence between the two models is found for frequencies

for which the dependence of the components of the Π-model on frequency is not significant.

A comprehensive noise model of an HBT is shown in Figure 4.12 and comprises six intrinsic and extrinsic noise sources. The extrinsic noise sources are the emitter and collector thermal noise sources and the extrinsic part of the base resistance R_{bx} noise source. Because the base is in sandwich between the emitter and the collector, its temperature is generally higher than the temperature of the emitter and the collector, therefore the noise due to the intrinsic part of the base resistance R_{bi} accounts for most of the base thermal noise. The remaining intrinsic noise sources are the base and collector shot noises. Parasitic capacitors are C_{pbe}, C_{pbc} and C_{pce}. Similarly, parasitic inductors are L_b, L_c and L_e. For analytical noise analysis, extrinsic noise sources and parasitic capacitors and inductors are generally omitted for simplicity.

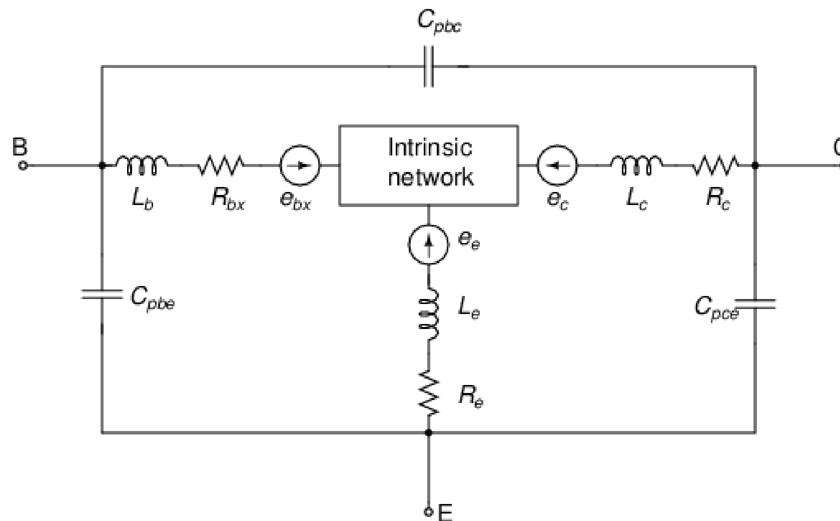


Figure 4.12. Comprehensive noise model for HBTs.

The thermal noises e_{bx}, e_e and e_c are due to the base, emitter and collector parasitic resistances.

The intrinsic noise model of an HBT is depicted in Figure 4.13. The types of noise sources and their qualitative contribution to the total noise are as follows:

1- The shot noise i_c due to the collector direct current.

2- The shot noise i_{cr} is due to the base-collector reverse direct current and is not represented in Figure 4.13. The base-collector reverse current is small and its shot noise can be disregarded.

3- The shot noise i_b is due to the base direct current.

4- The thermal noise e_{bi}, is due to the base parasitic resistance. The resistances R_{be} (r_π), R_{bc} and r_o do not correspond to physical resistors; they only model a physical phenomenon, which does not contribute to the transistor intrinsic noise.

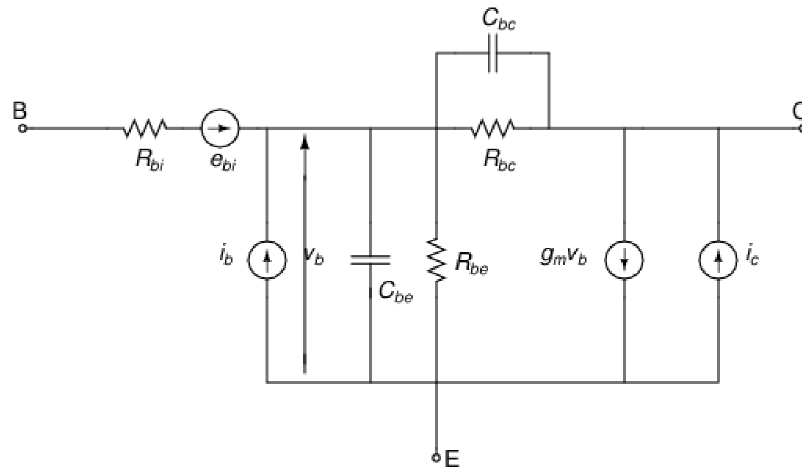


Figure 4.13. Intrinsic noise.

The thermal noise due to R_{bi} and to R_e is not negligible. Hence, intrinsic and extrinsic thermal noise sources are used in the simplified comprehensive noise model in Figure 4.14, where a resistive source is connected to the input of the transistor.

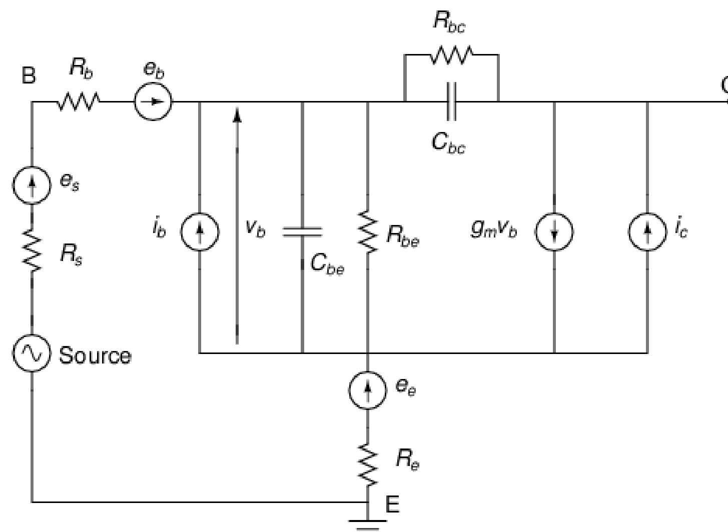


Figure 4.14. Simplified comprehensive noise model of SiGe HBTs.

The base resistance R_b (r_b) is relatively higher than the emitter and collector parasitic resistances shown in Figure 4.12. The latter resistances are low owing to the heavy doping of the emitter and the buried nature of the collector layer. In addition, the collector parasitic resistance, in series with the load and all in parallel with the high output collector resistance r_o, is small and makes a small contribution to the output noise. Hence, the thermal noise due to the collector parasitic resistance can be neglected when reported to the input in vue of the impact of the transistor gain. The noise due to the emitter parasitic resistance R_e is not affected by the transistor gain and should be accounted for. However, the calculation of input referred noise leads to complex equations when the emitter resistance R_e is accounted for. Noise calculations are simplified when R_e is neglected but only its thermal noise is considered. This approximation is valid when $R_e g_m << 1$, which has been verified [97]. The thermal noise source due to R_e is shifted to the transistor input thought a Blakesley transformation. The thermal noise at the input can then be modelled according to the sum of R_b (r_b) and R_e.

The crossing of the forward-biased based-emitter junction by electrons from the emitter and holes from the base is a random process that is at the origin of the base shot noise. However, the drift of the carriers through the reversed biased base-collector junction is a deterministic rather than a random process, because the junction does not constitute a potential barrier. However, electrons crossing the base-collector junction carry a delayed noise component due to the crossing of the base from the emitter.

Generally, it is assumed that the collector and base shot noise are not correlated, which is valid at low frequencies [97]. The correlation between the collector and base short noises is expressed by $\overline{i_b i_c^*} = 2qI_C[\exp(j\omega\tau_n) - 1]$, where τ_n, the noise transit time is the transport time taken by short noise electrons from the base-emitter junction to reach the collector. The noise transit time is different from the total forward transit time, which is the delay between a change of voltage at the base and the time when electrons associated with the change arrive at the collector. The noise transit time is due to DC and does not include the time constant contributions due to the modulation of charge in the base area caused by a change in base voltage. At the operating frequency of the LNA, the noise transit time is assumed to be nil, as for impact, the effective noise due to the base and emitter DC is lower

than the noise resulting from calculations. This can be shown in the expression of F_{min} that takes into account τ_n in (4.36):

$$F_{\min} \approx 1 + \frac{1}{\beta} + \sqrt{\frac{2g_m R_n}{\beta} + (\frac{2R_n(\omega C_i)^2}{g_m} - \omega^2 (C_{be} + C_{bc})\tau_n R_n)(1 - \frac{1}{2g_m R_n})} \quad (4.36)$$

The term in τ_n *is* small compared to other terms and at low frequencies it is negligible. The impact of the correlation component on noise performance increases with f/f_T [91], which results in the reduction of F_{min}. At frequencies higher than 1/10 of the peak f_T, this term decreases F_{min} and a noise model with noise transit time is required. SPICE suffers from this limitation, producing a higher value of F_{min} at high frequency [98].

Gummel-Poon, VBIC, Mextram and Hicum transistor models assume that noise sources in BJT are of the thermal and shot type and the base and collector shot noises are not correlated. For high frequency applications and for high biasing currents, measurements diverge from model data. Models such as the Van Vliet and transport models take into account the correlation between the base and collector shot noise. Semi-empirical models allow accurate modelling of the base and collector shot noise, as well as the effects of high biasing current [99].

4.4.3 Noise figure of the CE SiGe HBT

The noise model in Figure 4.14 is further simplified in Figure 4.15 where the emitter parasitic resistance (R_e) is not shown. The main sources of noise are represented in Figure 4.15(a) where v_b is thermal noise associated with the base resistance r_b, i_b is the base shot noise and i_c is the collector shot noise. The ABCD representation of the two-port noise model in Figure 4.15(a) is shown in Figure 4.15(b).

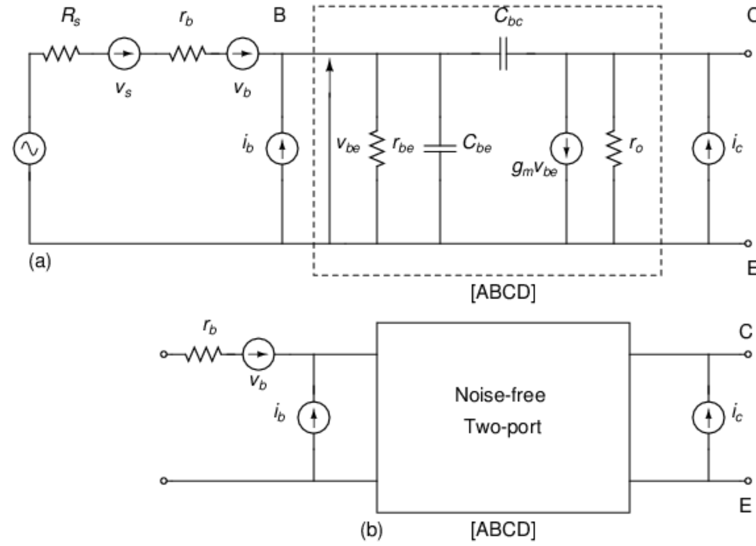


Figure 4.15. Main noise sources of the CE SiGe HBT and Two-port model.

The noise power densities of sources in Figure 4.15(a) are given by the expressions $\overline{i_c^2} = 2qI_C$, $\overline{i_b^2} = 2qI_B$, $\overline{v_b^2} = 4kT(r_b + R_e)$ and $\overline{v_s^2} = 4kTR_s$. The ABCD representation of Figure 4.15(b) is first calculated because the matrix will be used to report to the input the collector shot noise source using (4.28) and (4.29). In addition, an important property of the ABCD representation, which will be used in the calculations, is related to the ABCD representation of a cascade network, which is equal to the product of the ABCD matrix of each two-port network forming the cascade network. The base resistance r_b is neglected in the calculations of the ABCD matrix.

The chain matrix due to r_{be} (r_π) at the input of the noiseless port is equal to:

$$M_1 = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1/r_\pi & 1 \end{bmatrix} \tag{4.37}$$

The chain matrix due to C_{bc} (c_π) at the input of the noiseless port is expressed by:

$$M_2 = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ sC_\pi & 1 \end{bmatrix} \tag{4.38}$$

where s is the complex frequency, $s = j\omega f$.

The transmission matrix M_3 due to C_μ, to r_o and the current source g_m is derived from the results of Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL) to Figure 4.15.

$$M_3 = \begin{bmatrix} A_3 & B_3 \\ C_3 & D_3 \end{bmatrix} = \begin{bmatrix} \dfrac{sC_\mu(sC_\mu r_o + 1)}{sC_\mu r_o(sC_\mu - g_m)} & \dfrac{1}{sC_\mu - g_m} \\ \dfrac{sC_\mu(g_m r_o + 1)}{r_o(sC_\mu - g_m)} & \dfrac{sC_\mu}{sC_\mu - g_m} \end{bmatrix} \quad (4.39)$$

Because the output resistance r_o is very high and $g_m r_o >> 1$ and $sC_\mu r_o >> 1$, M_3 can then be approximated by:

$$M_3 = \begin{bmatrix} A_3 & B_3 \\ C_3 & D_3 \end{bmatrix} = \begin{bmatrix} \dfrac{sC_\mu}{sC_\mu - g_m} & \dfrac{1}{sC_\mu - g_m} \\ \dfrac{sC_\mu g_m}{sC_\mu - g_m} & \dfrac{sC_\mu}{sC_\mu - g_m} \end{bmatrix} \quad (4.40)$$

The ABCD matrix M is the product of M_1, M_2 and M_3, with M=[M_1][M_2][M_3], therefore:

$$M = \begin{bmatrix} \dfrac{sC_\mu}{sC_\mu - g_m} & \dfrac{1}{sC_\mu - g_m} \\ \dfrac{(1 + r_\pi sC_\pi)sC_\mu}{(sC_\mu - g_m)r_\pi} + \dfrac{sC_\mu g_m}{sC_\mu - g_m} & \dfrac{1 + r_\pi sC_\pi}{r_\pi(sC_\mu - g_m)} + \dfrac{sC_\mu}{sC_\mu - g_m} \end{bmatrix} \quad (4.41)$$

The terms of the transmission matrix are A, B, C and D and are given by:

$$A = \frac{sC_\mu}{sC_\mu - g_m} \quad (4.42)$$

$$B = \frac{1}{sC_\mu - g_m} \approx \frac{1}{-g_m} = -r_e \text{, for } g_m >> \omega C_\mu \quad (4.43)$$

$$C = \frac{sC_\mu(1/r_\pi + sC_\pi + g_m)}{sC_\mu - g_m} \quad (4.44)$$

$$D = \frac{1 + r_\pi sC_\pi}{r_\pi(sC_\mu - g_m)} + \frac{sC_\mu}{sC_\mu - g_m} = \frac{1/r_\pi + sC_\pi + sC_\mu}{sC_\mu - g_m} \quad (4.45)$$

Because $g_m >> \omega C_\mu$, (4.45) can be approximated by:

$$D = -\frac{1/r_\pi + sC_\pi + sC_\mu}{g_m} = \frac{-1}{r_\pi g_m} - j\omega\frac{C_\pi + C_\mu}{g_m} \quad (4.46)$$

The product $r_\pi g_m$ is the small-signal gain, $\beta_o = r_\pi g_\pi$ and the second term of (4.46) are related to the unity current gain frequency f_T, with $f_T = \frac{1}{2\pi}\frac{g_m}{C_\pi + C_\mu}$. Therefore, (4.46) can be rewritten as (4.47), with $\beta_o = \frac{\beta_F}{1 + j\beta_F\left(\frac{f}{f_T}\right)}$, β_F being the DC or low-frequency current gain:

$$D = -\left(\frac{1}{\beta_o} + j\frac{f}{f_T}\right) \tag{4.47}$$

Since the transmission matrix M is known, it is now possible to report to the input the shot noise contribution due to the collector current I_C. This is done by using (4.28) and (4.29), which show that the equivalent voltage and current noises due to the collector DC are given by (4.48) and (4.49), where the negative signs are irrelevant because the noise of the power at the input is related to the square of v_{ci} and i_{ci}.

$$v_{ci} = -Bi_c \tag{4.48}$$

$$i_{ci} = -Di_c \tag{4.49}$$

The total intrinsic voltage noise of the transistor is given by:

$$v_n = v_b + i_b(R_s + r_b) + Bi_c + (R_s + r_b)Di_c = v_b + Bi_c + (R_s + r_b)(i_b + Di_c) \tag{4.50}$$

$$v_n = v_b + r_e i_c + (R_s + r_b)[i_b + (\frac{1}{\beta_o} + j\frac{f}{f_T})i_c) \tag{4.51}$$

The noise factor F is equal to the ratio of the total noise at the input to the source noise:

$$F = \frac{\overline{v_s^2} + \overline{v_n^2}}{\overline{v_s^2}} = 1 + \frac{\overline{v_n^2}}{\overline{v_s^2}} \tag{4.52}$$

The noise sources v_b, i_b and i_c being uncorrelated, as discussed in Section 4.4.2, the power density of the noise due to v_n is expressed by:

$$\overline{v_n^2} = \overline{v_b^2} + \overline{i_b^2}(R_s + r_b)^2 + \overline{i_c^2} r_e^2 + \overline{i_c^2}(R_s + r_b)^2 \frac{1}{\beta_o^2} + \overline{i_c^2}(R_s + r_b)^2 \frac{f^2}{f_T^2} \tag{4.53}$$

$$\overline{v_n^2} = 4kT(r_b + R_e) + 2qI_B(R_s + r_b)^2 + 2qI_C r_e^2 + 2qI_C(R_s + r_b)^2 \frac{1}{\beta_o^2} + 2qI_C(R_s + r_b)^2 \frac{f^2}{f_T^2} \tag{4.54}$$

$$F = 1 + \frac{r_b + R_e}{R_s} + \frac{qI_C}{2kTR_s\beta_o}(R_s + r_b)^2 + \frac{qI_C}{2kTR_s} r_e^2 + \frac{qI_C}{2kTR_s}(R_s + r_b)^2 \frac{1}{\beta_o^2} + \frac{qI_C}{2kTR_s}(R_s + r_b)^2 \frac{f^2}{f_T^2} \tag{4.55}$$

Equation (4.55) can be simplified by introducing r_e, with $g_m = \frac{qI_C}{kT} = \frac{1}{r_e}$.

$$F = 1 + \frac{r_b + R_e}{R_s} + \frac{1}{2r_e R_s \beta_o}(R_s + r_b)^2 + \frac{1}{2R_s} r_e + \frac{1}{2r_e R_s}(R_s + r_b)^2 \frac{1}{\beta_o^2} + \frac{1}{2r_e R_s}(R_s + r_b)^2 \frac{f^2}{f_T^2} \quad (4.56)$$

Because $\beta_o >> 1$, (4.56) can be simplified as:

$$F = 1 + \frac{r_b + R_e}{R_s} + \frac{1}{2r_e R_s \beta_o}(R_s + r_b)^2 + \frac{1}{2R_s} r_e + \frac{1}{2r_e R_s}(R_s + r_b)^2 \frac{f^2}{f_T^2} \quad (4.57)$$

Equation (4.57) is equivalent to (4.58).

$$F = 1 + \frac{r_b + R_e}{R_s} + \frac{g_m}{2R_s \beta_o}(R_s + r_b)^2 + \frac{1}{2R_s g_m} + \frac{g_m}{2R_s}(R_s + r_b)^2 \frac{f^2}{f_T^2} \quad (4.58)$$

The second term of (4.58) is due to the base and emitter thermal noise sources; the third term is due to the base shot noise caused by the base DC bias and the fourth and last terms are due to the shot noise contribution from the collector bias DC.

Equation (4.58) shows that the noise factor increases with frequency, with the base and emitter parasitic resistances, but decreases when the DC gain and the unity frequency increase. At moderate frequencies, the noise factor is dominated by the base resistance, as shown by the second term. SiGe HBTs achieve better noise performance than BJTs owing to lower base resistance, higher DC gain and higher f_T. In addition, HBTs are smaller than BJTs, because of their higher current density. They are therefore subject to less parasitics. At high frequencies, the noise factor is dominated by the collector shot noise. The collector shot noise and g_m are proportional to the collector bias current. Hence, when the bias current is low and increases, the noise factor decreases until the gain reaches a maximum. When the peak gain has been reached, the noise factor increases with the collector current.

4.4.4 Relationship between R_n, F_{min}, Y_{opt} and the parameters of a SiGe HBT

For the designer, it is important to evaluate F_{min}, Y_{opt}, and possibly the noise resistance R_n. Knowledge of F_{min} allows derivation of the minimum possible noise that is achievable under optimum noise matching conditions, while Y_{opt} allows derivation of the noise

matching network that is required at the input. For this purpose, the noise parameters F_{min}, R_n and Y_{opt} must be related to (4.58). F_{min} can be derived from the correlation matrix elements using the equation $F_{\min} = 1 + 2(\mathrm{Re}\{C_{A12}\} + C_{A11}G_{sop})$ from Addendum A (A.63). The noise correlation matrix is calculated after reporting to the input the collector shot noise and deriving the elements of C_A from (4.12). However, the determination of the correlation matrix can lead to cumbersome calculations. A desired approach entails using the Y representation of the transistor circuit and converting the C_Y noise correlation matrix into a C_A correlation matrix using (4.68). This approach simplifies calculations because the noise currents at the input and at the output are assumed to be uncorrelated at the operating frequency. Also, the Y representation is preferred for nodal analysis. Equations (A.58), (A.59) and (A60) from Addendum A are then used to calculate the four noise parameters of the two-port noise model. This approach is used in the following section for the calculation of two-port model noise parameters.

The transformation is done using the transfer function T, where B and D are elements of the chain matrix ABCD.

$$T = \begin{bmatrix} 0 & B \\ 1 & D \end{bmatrix} \tag{4.59}$$

The Y representation of a SiGe HBT amplifier, when the base resistance r_b is neglected, is shown in Figure 4.16.

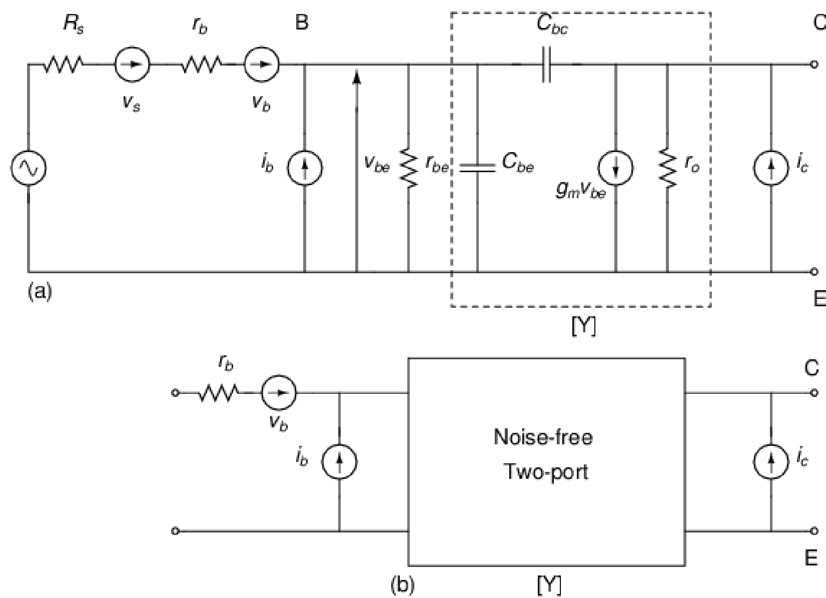


Figure 4.16. Y representation of a SiGe HBT amplifier.

The Y-parameters of Figure 4.16 are given by:

$$Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{r_\pi} + s(C\pi + C_\mu) & -sC_\mu \\ g_m - sC_\mu & sC_\mu \end{bmatrix}$$

(4.60)

The noise correlation matrix in admittance representation is not related to r_b and is equal to:

$$\begin{bmatrix} \overline{i_b i_b^*} & \overline{i_b i_c^*} \\ \overline{i_b^* i_c} & \overline{i_c i_c^*} \end{bmatrix} = 2kT \begin{bmatrix} \frac{g_m}{\beta} & 0 \\ 0 & g_m \end{bmatrix} = 2\Delta f \xi_Y = 4kT\Delta f C_Y \tag{4.61}$$

ξ_Y is the admittance correlation matrix and C_Y is the normalised admittance correlation matrix.

$$\xi_Y = 2kTC_Y \tag{4.62}$$

The ABCD matrix M being the product of M_1, M_2, M_3, and M_4, M=[M_1][M_2][M_3][M_4], with:

$$M_1 = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} = \begin{bmatrix} 1 & r_b \\ 0 & 1 \end{bmatrix} \tag{4.63}$$

$$M_2 = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1/r_\pi & 1 \end{bmatrix} \tag{4.64}$$

$$M_3 = \begin{bmatrix} A_3 & B_3 \\ C_3 & D_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ sC_\pi & 1 \end{bmatrix} \tag{4.65}$$

$$M_4 = \begin{bmatrix} A_4 & B_4 \\ C_4 & D_4 \end{bmatrix} = \begin{bmatrix} \frac{sC_\mu}{sC_\mu - g_m} & \frac{1}{sC_\mu - g_m} \\ \frac{sC_\mu g_m}{sC_\mu - g_m} & \frac{sC_\mu}{sC_\mu - g_m} \end{bmatrix} \tag{4.66}$$

When r_b is not neglected, the elements of the chain representation of Figure 4.16 are given by (4.67).

$$C = \begin{bmatrix} \left\{ \frac{sC_\mu}{sC_\mu - g_m} + \frac{r_b sC_\mu (g_m + 1/r_\pi + sC_\pi)}{sC_\mu - g_m} \right\} & \left\{ \frac{1}{sC_\mu - g_m} + \frac{r_b (1/r_\pi + sC_\pi + sC_\mu)}{sC_\mu - g_m} \right\} \\ \left\{ \frac{sC_\mu (g_m + 1/r_\pi + sC_\pi)}{sC_\mu - g_m} \right\} & \left\{ \frac{(1/r_\pi + sC_\pi + sC_\mu)}{sC_\mu - g_m} \right\} \end{bmatrix} \tag{4.67}$$

Using a Y representation to chain representation conversion, the noise correlation matrix is given by:

$$\left[C_A{}'\right] = 2kT[T][C_Y][T]^{+} \tag{4.68}$$

$$\text{where } T = \begin{bmatrix} 0 & \left\{\dfrac{1}{sC_\mu - g_m} + \dfrac{r_b(1/r_\pi + sC_\pi + sC_\mu)}{sC_\mu - g_m}\right\} \\ 1 & \left\{\dfrac{(1/r_\pi + sC_\pi + sC_\mu)}{sC_\mu - g_m}\right\} \end{bmatrix} \tag{4.69}$$

Therefore, C_A is equal to (4.70):

$$C_A = \begin{bmatrix} 0 & \left\{\dfrac{1}{sC_\mu - g_m} + \dfrac{r_b(1/r_\pi + sC_\pi + sC_\mu)}{sC_\mu - g_m}\right\} \\ 1 & \left\{\dfrac{(1/r_\pi + sC_\pi + sC_\mu)}{sC_\mu - g_m}\right\} \end{bmatrix} 2kT \begin{bmatrix} \dfrac{g_m}{\beta} & 0 \\ 0 & g_m \end{bmatrix}$$
$$\begin{bmatrix} 0 & 1 \\ \left\{\dfrac{1}{sC_\mu - g_m} + \dfrac{r_b(1/r_\pi + sC_\pi + sC_\mu)}{sC_\mu - g_m}\right\}^* & \left\{\dfrac{(1/r_\pi + sC_\pi + sC_\mu)}{sC_\mu - g_m}\right\}^* \end{bmatrix} \tag{4.70}$$

But C_A is also equal to:

$$C_A = 2kT \begin{bmatrix} R_n & \left[\dfrac{F_{\min} - 1}{2} - R_n Y_{sopt}^*\right] \\ \left[\dfrac{F_{\min} - 1}{2} - R_n Y_{sopt}\right] & R_n \left|Y_{sopt}\right|^2 \end{bmatrix} \tag{4.71}$$

Applying (A.60), (A.61) and (A.62) to (4.70), the noise parameters for the two-port noise model are given by:

$$R_n = r_b\left(1 + \frac{1}{\beta}\right) + \frac{1}{2g_m} + \frac{g_m r_b^2}{2}\left(\frac{1}{\beta^2} + \frac{f^2}{f_T^2}\right) \tag{4.72}$$

$$G_{sopt} = \frac{\left[\dfrac{1}{\beta^2} + 2g_m r_b\left(1 + \dfrac{1}{\beta}\right)\left(\dfrac{1}{\beta^2} + \dfrac{f^2}{f_T^2}\right) + (g_m r_b)^2\left(\dfrac{1}{\beta^2} + \dfrac{f^2}{f_T^2}\right)^2\right]^{\frac{1}{2}}}{\left[\dfrac{1}{g_m} + 2r_b\left(1 + \dfrac{1}{\beta}\right) + g_m r_b^2\left(\dfrac{1}{\beta^2} + \dfrac{f^2}{f_T^2}\right)\right]} \tag{4.73}$$

$$B_{sopt} = \frac{f/f_T}{\left[\frac{1}{g_m} + 2r_b\left(1+\frac{1}{\beta}\right) + g_m r_b^2\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right)\right]} \tag{4.74}$$

with $Y_{sopt} = G_{sopt} + \mathrm{j}B_{sopt}$

$$R_{sopt} = \frac{\left[\frac{1}{g_m} + 2r_b\left(1+\frac{1}{\beta}\right) + g_m r_b^2\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right)\right]\left[\frac{1}{\beta^2} + 2g_m r_b\left(1+\frac{1}{\beta}\right)\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right) + (g_m r_b)^2\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right)^2\right]^{\frac{1}{2}}}{\left[\frac{1}{\beta^2} + 2g_m r_b\left(1+\frac{1}{\beta}\right)\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right) + (g_m r_b)^2\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right)^2 + \left(\frac{f}{f_T}\right)^2\right]} \tag{4.75}$$

$$X_{sopt} = \frac{\frac{f}{f_T}\left[\frac{1}{g_m} + 2r_b\left(1+\frac{1}{\beta}\right) + g_m r_b^2\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right)\right]}{\left[\frac{1}{\beta^2} + 2g_m r_b\left(1+\frac{1}{\beta}\right)\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right) + (g_m r_b)^2\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right)^2 + \left(\frac{f}{f_T}\right)^2\right]} \tag{4.76}$$

with $Z_{sopt} = 1/Y_{sopt} = R_{sopt} + \mathrm{j}X_{sopt}$

$$F_{\min} = \frac{1}{2g_m R_s} + \left(1+\frac{1}{\beta}\right)\left(1+\frac{r_b}{R_s}\right) + \frac{g_m}{2R_s}(r_b + R_s)^2\left(\frac{1}{\beta^2}+\frac{f^2}{f_T^2}\right) \tag{4.77}$$

The approach used to determine noise parameters assumed for simplification that r_b by itself is not a noisy two-port network and only the contribution of r_b to the transfer function is taken into account in the calculations. A different approach that considers r_b and the CE transistor circuit as two cascaded two-port networks has been investigated. The analytical expressions obtained for both methods for the noise resistance R_n are close and provide the same results when $f_T >> f$.

4.4.5 Two-port noise parameters of the CE SiGe HBT based on admittance parameters

The admittance parameters of the CE SiGe HBT can be determined accurately taking into account the base and emitter parasitic resistances r_b and r_e as well as the base-collector

capacitance C_μ. This approach allows provision of accurate analytical expressions of the two-port noise parameters. The admittance matrix of the CE SiGe HBT is given by:

$$Y = \frac{\begin{bmatrix} g_\pi + j\omega C_\pi + j\omega C_\mu\left(1 + r_e\left(g_\pi + j\omega C_\pi + g_m\right)\right) & -j\omega C_\mu\left(1 + r_e\left(g_m + g_\pi + j\omega C_\pi\right)\right) \\ \left(g_m - j\omega C_\mu\right) & j\omega C_\mu\left(1 + \left(r_e + r_b\right)\left(g_m + g_\pi + j\omega C_\pi\right)\right) \end{bmatrix}}{1 + r_b\left(g_\pi + j\omega C_\pi + j\omega C_\mu\right) + g_m r_e\left(j\omega C_\mu r_b + 1\right)} \tag{4.78}$$

Details on the determination of admittance parameters of the CE SiGe HBT are provided in Addendum B.

From (4.34) and (4.35), the power density due to the noise sources at the input of Figure 4.7 are given by the expressions:

$$\overline{i_{ni}^2} = 2qI_B + 2qI_C \frac{\left|Y_{11}\right|^2}{\left|Y_{21}\right|^2} \tag{4.79}$$

$$\overline{i_{ni} v_{ni}^*} = 2qI_C \frac{Y_{11}}{\left|Y_{21}\right|^2} \tag{4.80}$$

After adding the noise power due to the base parasitic resistance r_b and to the emitter parasitic resistance r_e (Blakesley transformation), the noise due to voltage noise sources referred to the input is given by:

$$\overline{v_{ni}^2} = 4kT\left(r_b + r_e\right) + 2qI_C \frac{1}{\left|Y_{21}\right|^2} \tag{4.81}$$

where I_B and I_C are the base and collector bias currents.

Using the expression of Y, the above equations become:

$$\overline{i_{ni}^2} = 2qI_C\left[\frac{1}{\beta} + \frac{1}{\beta^2} + \left(\frac{\omega C_i}{g_m}\right)^2\right] \tag{4.82}$$

$$\overline{v_{ni}^2} = 4kT\left(r_b + r_e + \frac{\left|Y_r\right|^2}{2g_m}\right) \tag{4.83}$$

$$\overline{i_{ni} v_{ni}^*} = 2kT\left\{\frac{1 + g_\pi\left(r_b + \beta r_e\right)}{\beta} + \frac{\omega^2 c_\pi^2\left(r_b + \beta r_e\right) + j\omega C_{be}}{g_m}\right\} \tag{4.84}$$

where $|Y_r|^2 = (1 + g_\pi(r_b + \beta r_e))^2 + (\omega C_\pi(r_b + \beta r_e))^2$ (4.85)

Using the equations of the noise parameters in Section 4.4.4 and calculated in Addendum A from (A.60), (A.61) and (A.62), the following expressions are derived:

$$R_n = \frac{V_T|Y_r|^2}{2I_C} + r_b + r_e \quad (4.86)$$

$$Y_{sopt} = \frac{f}{f_T R_n}\left[\sqrt{\left(\frac{I_C}{2V_T}\right)(r_b + r_e)\left(1 + \frac{f_T^2}{f^2}\right)\left(\frac{1}{\beta} + \frac{1}{\beta^2}\right) + \left(\frac{f_T}{f}\right)^2\left(\frac{1}{4}\left(\frac{1}{\beta} + \frac{1}{\beta^2}\right)\right) + \frac{|Y_r|^2 - 1}{4}} - j\frac{1}{2}\right] \quad (4.87)$$

$$F_{min} = 1 + \frac{1 + g_\pi(r_b + \beta r_e)}{\beta} + \frac{\omega^2 C_\pi^2(r_b + \beta r_e)}{g_m} + \frac{f}{f_T R_n}\left[\sqrt{\left(\frac{I_C}{2V_T}\right)(r_b + r_e)\left(1 + \frac{f_T^2}{f^2}\right)\left(\frac{1}{\beta} + \frac{1}{\beta^2}\right) + \left(\frac{f_T}{f}\right)^2\left(\frac{1}{\beta} + \frac{1}{\beta^2}\right) + |Y_r|^2 - 1}\right] \quad (4.88)$$

4.4.6 Main two-port noise analytical models for the CE BJT and SiGe HBT

The expressions of F_{min}, B_{sopt}, G_{sopt}, R_{sopt} and X_{sopt} found so far are complex and not open to simple interpretation. It is therefore desirable to investigate noise models for the SiGe HBT that lend themselves to simple interpretation. From the Nielsen transistor noise model in 1957 and the improved noise model by Van der Ziel, several noise models for the BJT have been developed, including the Fukui model for microwave BJTs and the Motchenbacher model in 1973, which was based on the Giacoletto's equivalent circuit. More recently, the Voinigescu model was proposed in 1997. This model, also based on the Giacoletto's equivalent circuit, is scalable and allows the optimisation of noise matching by changing the geometry of the transistor. This means that noise matching can be achieved without an additional circuit around the transistor, which is desired to optimise the NF.

The main recent analytical models relating two-port noise parameters to noise sources and to the small-signal equivalent circuit of the BJT are provided in this paragraph. For simplicity, these models generally omit the extrinsic base-collector capacitance as well as

parasitic capacitances and inductances. These assumptions ignore couplings that can create feedback paths and affect the accuracy of the model. The noise models are:

1- Escotte model [100]

   Noise sources are uncorrelated. Parasitic inductances and capacitances are not used and the base-collector capacitance C_{bc} is not included in the analysis.

2- Basaran model [101]

   This is a simplified transport model; parasitic inductances and capacitances are not included.

3- Jahan model [102]

   Parasitic inductances and capacitances are not used; voltage noise source are in series with the emitter resistance and there is only one shot noise source.

4- Rudolph model [103]

   Simplified transport model; parasitic inductances and capacitances are not included.

5- Gao model [104], [105].

   Transport model; the chain correlation matrix is used to derive noise parameters. The dependency of intrinsic noise parameters on frequency is not simplified.

6- Niu model [106]

   The extrinsic network is not included in the analysis; noise parameters are derived from simplified Y-parameters.

7- Voinigescu model [79]

   Shot noise sources are uncorrelated and only intrinsic parameters are used, except for the base and emitter parasitic resistances. The model is based on Y-parameters and has been verified for optimum NF design.

4.4.7 Voinigescu model

The model by Sorin Voinigescu and Osama Shana allows the performance of noise matching by changing the geometry of the input transistor rather than adding a passive matching network [79]. This model is based on [107] and has provided satisfactory results for SiGe transistors. For its simplicity, its verification results and the way in which the model allows one to relate R_{sopt} and F_{min} to the size of a transistor, this model has been selected for this thesis.

The noise parameters that result from the model are:

$$R_n \approx \frac{V_T}{2I_C} + r_b + R_e \tag{4.89}$$

$$F_{\min} = 1 + \frac{n}{\beta_o} + \frac{f}{f_T}\sqrt{\frac{I_C}{2V_T}(r_b + R_e)(1 + \frac{f_T^2}{\beta_o f^2}) + \frac{n^2 f_T^2}{\beta_o f^2}} \tag{4.90}$$

where r_b is the base parasitic resistor, R_e the emitter parasitic resistor and n the ideality factor.

$$R_{sopt} \approx \frac{\beta_o}{g_m\left(1 + \beta_o \frac{f^2}{f_T^2}\right)}\sqrt{\frac{1}{\beta}\left(1 + 2\frac{g_m(r_b + R_e)}{n}\right) + 2\frac{g_m(r_b + R_e)}{n}\frac{f^2}{f_T^2}} \tag{4.91}$$

$$X_{sopt} \approx \frac{\beta_o}{g_m}\frac{f/f_T}{1 + \beta_o(f/f_T)^2} \tag{4.92}$$

where $Z_{sopt} = R_{sopt} + \mathrm{j}\, X_{sopt}$.

A detailed derivation of the model was not found in the literature. The derivation of (4.90), (4.91) and (4.92) was done in this work and is presented in Addendum C.

4.4.8 Dependence of F_{min} on the collector current, I_C

A more complex signal model taking into account the delay due to the emitter and the collector parasitic resistances shows that the unity gain frequency in (4.90) is given by [108]:

$$f_T = \frac{1}{2\pi\left\{\tau_F + \frac{kT}{qI_C}(C_{be} + C_{bc}) + C_{bc}(R_e + r_c)\right\}} \tag{4.93}$$

where C_{bc} and C_{be} are the base-collector and base-emitter depletion capacitances and τ_F is the forward transit time, R_e is the emitter parasitic resistance and r_c the collector parasitic resistance.

$$\tau_F \cong \tau_B + \tau_C \tag{4.94}$$

where τ_B is the base transit time and τ_C is the base-collector depletion layer delay.

Equation (4.93) can also be written as follows, w_e and l_e being the width and the length of the emitter:

$$f_T = \frac{1}{2\pi\left\{\tau_B + \tau_C + \frac{kT}{qI_C w_e l_e}\left(C_{be} + C_{bc}\right)w_e l_e + C_{bc}\left(R_e + r_c\right)\frac{w_e l_e}{w_e l_e}\right\}} \tag{4.95}$$

Using the relations $J_C = I_c/W_e l_e$, $C_{beo} = C_{be}/w_e l_e$, $C_{bco} = C_{bc}/w_e l_e$, $r_{el} = R_e l_e$ and $r_{cl} = r_c l_e$, (4.95) becomes:

$$f_T = \frac{1}{2\pi\left\{\tau_B + \tau_C + \frac{kT}{qJ_C}\left(C_{beo} + C_{bco}\right) + C_{beo}\left(r_{el} + r_{cl}\right)w_e\right\}} \tag{4.96}$$

J_C is the collector current density; C_{beo} and C_{bco} are C_{be} and C_{bc} capacitances per emitter area. The emitter and collector series resistances R_e and r_c are inversely proportional to the length of the emitter l_e [1]. For this reason, the terms $R_e l_e$ and $r_c l_e$ are independent of the emitter length and are technology constants [1]. As stated in [1], "this characteristic is the foundation of the sizing of the transistor for minimum noise".

The base resistance r_b has two parts, r_{b1} and r_{b2}, with the first part (r_{b1}) being the resistance between the base contact and the edge of the emitter diffusion [1]. This part varies only with the length of the emitter. The second part r_{b2} is beneath the emitter and can be neglected at moderate and high currents [109]. Equation (4.96) shows that f_T is mostly determined by J_C and is independent of l_e, the transistor emitter length [1]. Equation (4.90) becomes (4.97), taking into consideration the expressions of the current density and of the depletion capacitances as functions of the size of the transistor [1]:

$$F_{\min} = 1 + \frac{n}{\beta_o} + \frac{f}{f_T}\sqrt{\frac{J_C w_e}{2V_T}(r_{bl} + r_{el})(1 + \frac{f_T^2}{\beta_o f^2}) + \frac{n^2 f_T^2}{\beta_o f^2}} \tag{4.97}$$

The minimum noise factor is a function of the current density J_c, of f_T and βo which are also functions of J_c. F_{min} is independent of l_e when the ratio l_e/w_e is larger than ten [79]. At constant emitter current density, devices with a smaller emitter width achieve a lower noise factor. A plot of F_{min} versus J_c shows that F_{min} has a minimum at J_{opt}. The density current for the minimum noise factor is achieved at about one-eighth of the density current required for maximum f_T [110]. A simulation by SpectreRF shows the dependency of NF on the base voltage V_B in Figure 4.17, for a 0.120 nm × 2.5 nm SiGe HBT. The collector

current, hence the collector current density, is controlled by V_B. The value of the NF is 0.247 dB, the collector current is 44.9 µA, the base voltage V_B is 0.763 V and the operating frequency is 1.4 GHz.

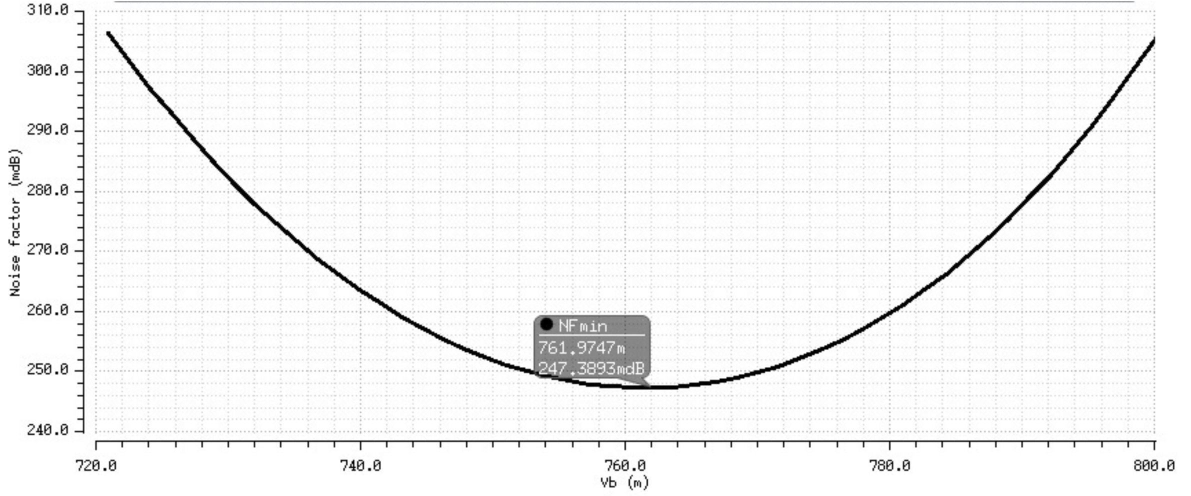


Figure 4.17. NF versus base voltage V_B.

Since βo, n and r_b are remotely related to I_C at low bias currents, it is assumed that they are constant when J is closer to J_{opt}. The minimum of F_{min} is F_{opt} and is found by equating to zero the derivative of F_{min} with respect to J_c [111].

The expression of J_{opt} is shown by (4.98):

$$J_{copt} \cong 2\pi(C_{beo} + C_{bco})V_T f \sqrt{\beta_o} \tag{4.98}$$

Equation (4.98) assumes that $4\pi^2 \beta_o \tau_F^2 f^2 << 1$ and shows that J_{copt} is directly proportional to the frequency and the absolute temperature through V_T [1]. The current density is also dependent on β_o and varies with foundries and technology nodes [1].

By replacing the current density by (4.98), (4.97) becomes [112]:

$$F_{\min} \cong 1 + \sqrt{f}\sqrt{\frac{8\pi^2 r_b (C_{be} + C_{bc})}{\beta_o^{1/2}}} \tag{4.99}$$

Using w_e and l_e, the expression of R_n in (4.89) becomes (for $n \neq 1$):

$$R_n \cong \frac{n^2 V_T}{2 J_c w_e l_e} + (r_{bl} + r_{el})\frac{1}{l_e} \tag{4.100}$$

As already shown in previous paragraphs, R_n is directly related to the base and emitter resistances and is not dependent on frequency when the transistor bias current is fixed [1]. R_n is also directly related to the thermal voltage, hence to the absolute temperature T [1]. R_{sopt} is inversely related to the size of the transistor (w_e, l_e), and to the bias current. R_n is inversely proportional to l_e.When J_c and w_e are fixed, the input impedance matching can be achieved by selecting l_e under the conditions discussed in the following section.

4.4.9 Dependence between R_{sopt} and the emitter length

It has been indicated that F_{min} is not related to the length of the emitter when the ratio l_e/w_e is larger than ten. At constant current density, when the width of the transistor increases by a factor of N, the collector current also increases by the same factor and consequently the transconductance g_m. The capacitances C_{bc} and C_{be} also increase by the same factor N and the unity gain frequency remains constant, as shown by equation $f_T = g_m / 2\pi(C_{be} + C_{bc})$.

In cases where the emitter length increases by a factor of N at constant current density, the unity gain frequency is unchanged while g_m increases and r_b decreases by the same factor. If the emitter parasitic resistance is small and the DC gain is high, (4.97) shows that F_{min} is constant, but, R_n, X_{sopt} and R_{sopt} decreases by a factor of N, as shown by (4.100) and the expression of Y_{sopt} in Addendum C (C.16).

Generally, R_{sopt} is found by measurement or by simulation. A script for the simulation of R_{sopt} in SKILL is provided in Addendum D.

4.4.10 Noise in parallel transistors

The performance of a transistor amplifier can be improved by the use of parallel identical transistors. The main advantages of transistor paralleling are:

- The NF can be improved under the conditions that are discussed in this section.
- The optimum noise resistance R_{sopt} as well as the output impedance, decreases proportionally to the number of transistors.

- The linearity of a transistor increases with its size. In terms of linearity, n parallel transistors are equivalent to a larger transistor having an emitter length of n times the emitter length of a single transistor.
- The gain increases with the paralleling of transistors.

The impact of the paralleling of transistors on output noise is intuitively understood by considering the statistical nature of electronic noise: the total output signal is proportional to the number of transistors while the total output noise is proportional to the square root of the number of transistors because noise outputs from the transistors are uncorrelated. If S_o/N_o is the SNR at the output of one transistor, then this ratio becomes $S_o\sqrt{n}/N_o$ when n transistors are in parallel [58]. Hence, the SNR increases by 3 dB when n doubles. In practice, this increase is less than 3 dB because the total output noise is due in part to the source thermal noise. The increase is close to 3 dB, as the resistance of the source is small compared to the base resistance r_b of each transistor [113].

Primarily, transistor paralleling allows the reduction of r_b, which is one of the main noise sources. For $R_s >> r_b$, the improvement in the noise performance is marginal at best when n increases, which is the case with SiGe HBTs. The decrease in the NF is however limited: the NF reaches a minimum, after which it increases when the number of parallel transistors n increases.

While the SNR increases with the paralleling of CE transistors, the optimum noise resistance (as well as impedance) is inversely proportional to the number of parallel transistors, as represented in Figure 4.18.

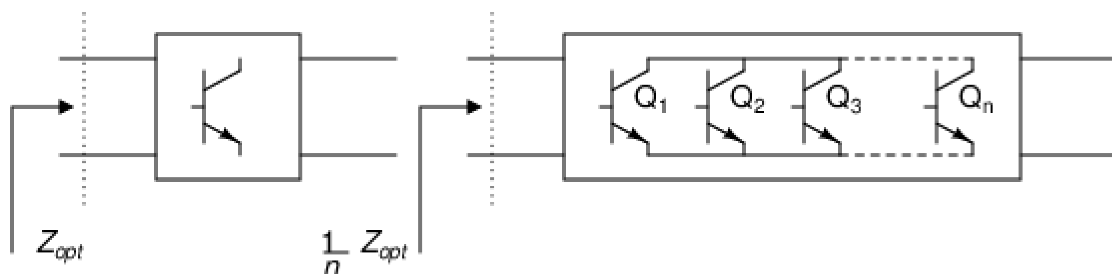


Figure 4.18. Optimum noise impedance of parallel transistors.

It is shown in this work that, when n identical transistors are in parallel, as depicted in Figure 4.18, and the collector current per transistor is equal to I_c, the noise resistance R_n and the optimum noise impedance Z_{sopt} (R_{sopt}) are divided by n, while the noise conductance and the correlation admittance are multiplied by n and F_{min} remains unchanged. This is used in this work for noise matching and demonstrated in Addendum E. In addition, the SNR can improve by a factor whose maximum value is $\sqrt{n}$.

4.4.11 Impact of the base-emitter capacitor on R_{sopt}

It was shown that R_{sopt} is inversely proportional to the transistor size. Hence, small devices tend to have a large R_{sopt}. Because R_{sopt} is also inversely related to the operating frequency, the optimum resistance is larger at low frequencies. In the case of the IBM8HP process, for a 2.5 μm emitter length, R_{sopt} is in the range of 900 Ω at 1.4 GHz and optimum collector current biasing. It has been indicated in previous sections of this work that the IDCE in a cascode configuration is recognised as the state-of-the-art topology for LNAs. For this topology, simultaneous noise and impedance matching is obtained under the condition:

$$Z_s = Z_{sopt} = Z_{in}^* \tag{4.101}$$

where Z_s is the impedance of the source, Z_{in}^* is the complex conjugate of the input impedance Z_{in} and Z_{sopt} is its optimum noise matching impedance. R_s and R_{sopt} are the real parts of Z_s and Z_{sopt}.

Generally, R_{sopt} is lower than 50 Ω for frequencies of several GHz, except for large devices or low frequencies. In such a case, the noise matching can be achieved by the addition of a capacitor C_{BE} in parallel with the base and emitter of the input transistor, as shown in Figure 4.19. The noise matching condition is given by (4.102), when Z_s is real.

$$\frac{1}{R_s} + j\omega C_{BE} = \frac{1}{Z_{sopt}} \tag{4.102}$$

Equation (4.102) yields (4.103). The imaginary part of the optimum noise matching impedance Z_{sopt} is assumed to have been cancelled by an inductor in the base circuit:

$$\frac{R_s}{1 + C_{BE}^2 \omega^2 R_s^2} = R_{sopt} \tag{4.103}$$

Equation (4.103) can be achieved only when $R_s > R_{sopt}$. Therefore, the parallel capacitance C_{BE} allows one to obtain noise matching only when $R_s > R_{sopt}$. When $R_{sopt} > R_s$, noise matching can be achieved either by the addition of a matching network at the input or by connecting several identical transistors in parallel. Both solutions are sub-optimal as they require additional active or passive components as well as interconnects that increase losses and the NF. An optimal solution consists in sizing the transistor to achieve noise matching without additional external components. This approach is however limited by the range of R_{sopt}, which is related to the variation range of the emitter length of a transistor for a given process.

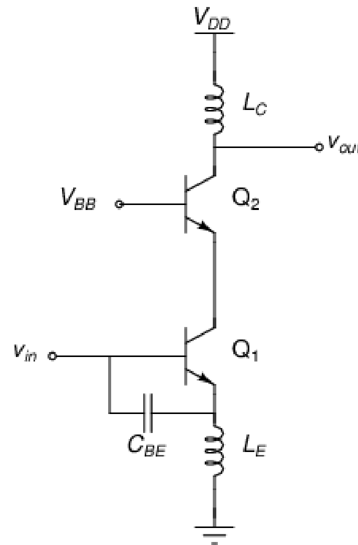


Figure 4.19. Noise matching by base-emitter capacitor C_{BE}.

4.4.12 Extraction of transistor parameters from Y- and Z-parameters

The parameters used in intrinsic noise calculations for BJT and SiGe HBT devices cannot be obtained easily from the design kit, nor from SpectreRF, the simulator from Cadence Design Systems used in this work. Using the small-signal model parameters, r_b, r_e, g_m, C_μ and C_π can be extracted from the expressions of Y- and Z-parameters. The values of the Y- and Z-parameters used to determine the parameters of the small-signal model are obtained by simulation. The derivation of the expressions of the small-signal model parameters in (4.104), (4.105), (4.106), (4.107) and (4.108) is provided in Addendum F.

$$C_\mu = \frac{-1}{\omega \Im(Z_{22} - Z_{21})} \tag{4.104}$$

$$C_{\pi} \cong \frac{\Im(Y_{11} + Y_{12})}{\omega} \tag{4.105}$$

$$g_m = |Y_{21} - Y_{12}| \tag{4.106}$$

$$r_b = Z_{11} - Z_{12} \tag{4.107}$$

$$r_e \cong \lim_{\omega \to 0} \{\Re(Z_{12})\} - \frac{1}{g_m} \tag{4.108}$$

4.5 BASIC CONCEPTS IN LNA DESIGN

LNAs have relatively few components but their simplicity is misleading, as their design requires several trade-offs [2]. Their performance metrics cannot be optimised simultaneously and complicated concessions are required between NF, bandwidth, gain, power consumption, supply voltage, dynamic range, linearity, stability and input and output matching [2]. The main design performance requirement for this work is the NF, which in a receiver is mainly determined by its first stage, the LNA [114]. The noise due to subsequent stages being inversely proportional to the power gain of the first stage, as shown by Friis' formula, a high-gain LNA is desired.

To achieve minimum NF and high power gain, three sets of impedance values derived from the two-port noise model must fulfil noise and impedance matching conditions. The impedance of the source is equal to R_s + jX_s, where R_s and X_s are its real and imaginary components. In most applications, R_s is equal to 50 Ω and X_s is nil. The input impedance of the LNA whose real and imaginary parts are respectively R_{in} and X_{in} constitutes the second set, while the last set is the real and the imaginary components of the optimum noise impedance, $Z_{sopt} = R_{sopt} + jX_{sopt}$.

The LNA can be viewed as a device generating a noise signal toward the source. Reflections of the signal back to the LNA will occur, unless the conditions below derived from the two-port noise model are fulfilled. It is noted that, contrary to power matching,

the impedance of the source must be equal to the optimum noise impedance and not to its conjugate. This is expressed by the equations:

$$R_s = R_{sopt} \tag{4.109}$$

$$X_s = X_{sopt} \tag{4.110}$$

Similarly, the transmission of the signal from the source to the LNA is optimal under the conditions in (4.111) and (4.112), derived from the maximum power transfer theorem and referred to as power matching requirements:

$$R_s = R_{in} \tag{4.111}$$

$$X_s = -X_{in} \tag{4.112}$$

In case power consumption is the main design constraint and the collector current I_c is fixed, either the emitter length or J_{sopt} can be used as design variables. In such a case, the minimum possible noise factor and noise matching cannot be achieved simultaneously.

For a cascode LNA, the main source of third-order intermodulation products due to non-linearities is the input transistor [111]. The non-linearity of semiconductor devices is not always undesirable; in applications that require frequency translation, such as mixers, non-linear behaviour is required. The small-signal model of a SiGe HBT, a non-linear device like all semiconductor devices, shows that several elements of the model are the source of its non-linear response, including:

- The exponential dependence of the collector current on the base voltage.
- The dependence between the base current and the collector current ($I_B = I_C / \beta$, where β is not constant).
- The avalanche multiplication current, which has a non-linear dependence with the base-emitter and base-collector voltages.
- The base-emitter capacitance, which is related to I_C.
- The base-collector capacitance.

However, SiGe HBTs achieve superior linearity due to interactions between various non-linear elements from their small-signal and large-signal models. Using an analysis based on the Volterra series, it is shown in [115] that the third-order intermodulation product IIP3

improves with the increase of the transconductance and with inductive degeneration. As a matter of fact, the linearity of a transistor depends on its bias circuitry and termination. Linearity is improved by negative feedback as well as by the increase in the size (g_m) of the transistor, by transistor paralleling (g_m) and by the increase in the biasing current (g_m). Negative feedback decreases the gain, while the increase in the biasing current increases the NF when biasing has been optimised for minimum noise. Because such requirements are conflicting, the simultaneous achievement of low NF, high gain, high linearity and a high 1 dB compression point using a single stage is difficult.

To overcome this limitation, an alternative involving the design of a two-stage amplifier is proposed in [116]. The first stage provides low NF, high gain and low return loss. The second stage is designed for high linearity, high 1 dB compression and output impedance matching. In case two stages are not desired and several design constraints exists, such as power consumption, gain and linearity, design constraints are prioritised first, such as NF, linearity and power consumption; contours of constant NF, constant linearity and constant power consumption are plotted in a 2D design space as functions of two design variables, such as the emitter length and the collector current. To determine the bias current and the emitter length, the designer selects a point in the 2D design space that offers the best compromise between the design constraints [112].

It has been shown that the lowest NF for a transistor is achieved when the source impedance is equal to Z_{sopt}. In addition, maximum power is transmitted from the source to the input of the amplifying transistor when the source impedance is matched to the complex conjugate of the input impedance. In general, both requirements are not met simultaneously and a trade-off between noise and impedance matching is desired [1]. Hence, the basic requirements in LNA design are noise and impedance matching.

The IDCE circuit represented in Figure 4.20 is widely used owing to, among others, its gain and noise performance. Although this topology achieves simultaneous noise and power matching, the matching is limited to a narrow bandwidth, because of the input tuned circuit resulting from the base and emitter inductors and from the base-emitter capacitance.

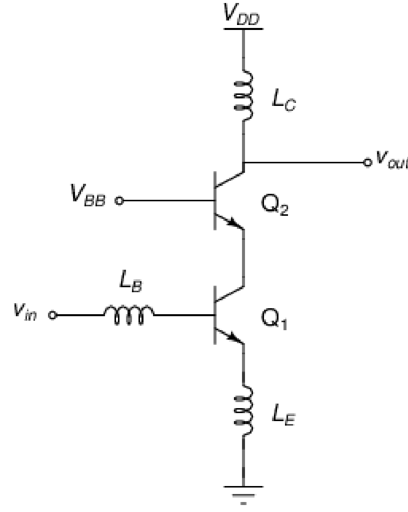


Figure 4.20. Inductively degenerated cascode amplifier.

The inductors L_B and L_E are ideals, with nil resistances, capacitances and no energy radiation. Therefore, L_E introduces a series-series feedback without degrading noise performance [1]. It can be shown that noise matching conditions remain valid when L_B and L_E are introduced [117]. A simplified expression of the input impedance of Figure 4.20 is shown by the equation:

$$Z_{in} = r_b + \frac{I_C q}{kT} L_E + j\omega(L_B + L_E) - \frac{j}{\omega C_{be}} \cong r_b + \omega_T L_E + j\omega(L_B + L_E) - \frac{j}{\omega C_{be}} \quad (4.113)$$

The expression of the real part of the input impedance can be used to calculate L_E:

$$R_{in} = r_b + \omega_T L_E \quad (4.114)$$

The input reactance is expressed by:

$$X_{in} = \omega(L_B + L_E) - \frac{1}{\omega C_{be}} \quad (4.115)$$

Power matching conditions are, for a resistive source, $R_{in} = R_s$ and $X_{in} = 0$. Hence,

$$L_B = \frac{1}{\omega^2 C_{be}} - L_E \quad (4.116)$$

Because the inductor L_E is ideal, F_{min} is unchanged. The IDC can be represented as two two-port network in a series-series configuration as shown in Figure 4.21.

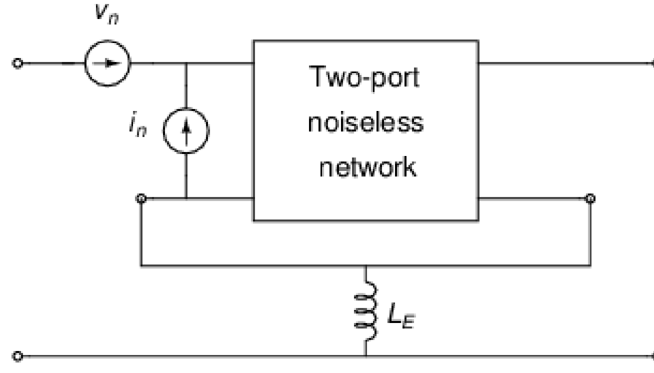


Figure 4.21. IDCE as a combination of two two-port networks.

Assuming that C_{ZA} is the noise correlation matrix in Z representation of the common-emitter transistor circuit and C_{ZB}, the noise correlation matrix of the two-port network formed by the parallel inductor L_E, the noise correlation matrix of the resulting network is given by the expression $C_{ZC} = C_{ZA} + C_{ZB}$.

The noise correlation matrix C_{ZA} is obtained by the transformation $C_{ZA} = TC_{AA}T^{+}$, where C_{AA} is the noise correlation matrix of the two-port network A in chain representation and T is the respective transformation matrix from Addendum A.

The chain representation of C_{ZC} is given by $C_{AC} = MC_{ZC}M^{+}$.

$$T = \begin{bmatrix} 1 & -Z_{A11} \\ 0 & -Z_{A21} \end{bmatrix} \tag{4.117}$$

$$M = \begin{bmatrix} 1 & -A_{C11} \\ 0 & -A_{C21} \end{bmatrix} \tag{4.118}$$

where Z_A is the Z representation of the network A (CE transistor) and A_C is the chain representation of the network C (IDCE transistor).

$$C_{AC} = \begin{bmatrix} 1 & -A_{C11} \\ 0 & -A_{C21} \end{bmatrix} \left\{ \begin{bmatrix} 1 & -Z_{A11} \\ 0 & -Z_{A21} \end{bmatrix} C_{AA} \begin{bmatrix} 1 & 0 \\ -Z^{*}_{A11} & -Z^{*}_{A21} \end{bmatrix} + C_{ZB} \right\} \begin{bmatrix} 1 & 0 \\ -A^{*}_{C11} & -A^{*}_{C21} \end{bmatrix} \tag{4.119}$$

Noise parameters F_{min}, R_{sopt} and Y_{sopt} can be extracted from C_{AC}. The expression of C_{AC} is complex and, after lengthy calculations involving (4.119), (A.61) and (A.62), noise parameters of the IDC are given by the expressions:

$$F'_{\min} \cong F_{\min} \tag{4.120}$$

$$R'_{sopt} \cong R_{sopt} \tag{4.121}$$

$$X'_{sopt} \cong X_{sopt} - \omega L_e \tag{4.122}$$

The optimum noise reactance in (4.92) can be further simplified when $2R_n\beta/g_m >> 1$, leading to the equation:

$$X_{sopt} \cong \frac{1}{\omega(C_{be} + C_{bc})} \cong \frac{1}{\omega C_{be}} \tag{4.123}$$

$$X'_{sopt} \cong \frac{1}{\omega C_{be}} - \omega L_e \tag{4.124}$$

Therefore, the base inductance that achieves noise matching is given by:

$$L'_B = \frac{X'_{sopt}}{\omega} = \frac{1}{\omega^2 C_{be}} - L_E \tag{4.125}$$

Comparing (4.125) and (4.116), it is found that $L'_B \cong L_B$. Hence L_E and L_B allow the achievement of simultaneous power and noise matching [90].

A question arises on the effect of the cascode transistor on the NF and on how this transistor can be sized to achieve the best NF for the LNA. It is assumed generally, for reasons of simplicity, that the contribution of the cascode stage to the NF can be neglected [1]. The assumption is valid if the gain of the first stage of the LNA is high enough to reduce the noise due to subsequent stages significantly. At low frequencies, typically below 5 GHz, a high power gain can be reached by a single-stage LNA [1]. In this case, the noise due to the cascode transistor can be neglected.

4.6 BANDWIDTH OF THE IDCE LNA

In RF design, the bandwidth of an LNA is determined by the frequency bandwidth through which the transfer of energy between the source and the LNA is optimum, rather than by the power gain or the NF. The transfer of energy depends on the impedance of the source and on the LNA input impedance; optimum power transfer is achieved when the source impedance is equal to the complex conjugate of the input impedance of the LNA. This requirement is verified at a single frequency but the input bandwidth corresponds to a frequency bandwidth set by an accepted range of signal reflection corresponding to the parameter S_{11}. As the bandwidth increases, the impedance matching is impaired according

to the Bode-Fano criterion which implies that a trade-off between bandwidth and power reflection is required. The bandwidth of an inductively degenerated SiGe HBT amplifier is evaluated in this section.

Equation (4.113) is equivalent to the RLC circuit in Figure 4.22 with $R_{IN} = g_m L_E/C_{be}$, $L_{IN} = L_E + L_B$ and $C_{IN} = C_{be}$. At resonance, the voltage across C_{IN} can be used to determine the gain of the amplifier; this voltage is Q_{in} times larger than the voltage across the source resistance.

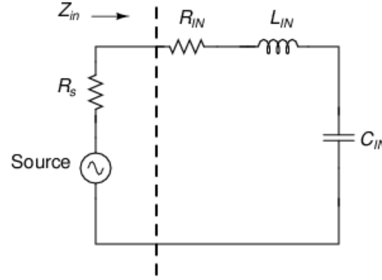


Figure 4.22. Input RLC series network.

The input impedance can be rewritten as:

$$Z_{in} = sL_{IN} + R_{IN} + \frac{1}{sC_{IN}} \tag{4.126}$$

where s is the complex frequency.

In RF design, it is desired to achieve an input return loss S_{11} that is better than -10 dB across the frequency band. The input return loss resulting from the signal source of resistance R_s represented in Figure 4.22 is given by (4.127).

$$S_{11} = \frac{Z_{in} - R_S}{Z_{in} + R_S} \tag{4.127}$$

where R_s is the internal resistance of the source.

Substituting (4.126) in (4.127) yields (4.128),

$$S_{11} = \frac{s^2 + \omega_o^2}{s^2 + s\,\omega_o / Q_{in} + \omega_o^2} \tag{4.128}$$

where $\omega_o = 1/\sqrt{C_{IN} L_{IN}}$ and $Q_{in} = \omega_o L_{IN} / (R_{IN} + R_S)$, Q_{in} is the quality factor and ω_o is the angular frequency of resonance.

The 3 dB bandwidth Δf_{3dB} is expressed by:

$$\Delta f_{3dB} = \frac{\omega_o}{2\pi Q_{in}} \tag{4.129}$$

The return loss must be superior to 10 dB, which is expressed by (4.130):

$$20\log\left|S_{11}\right| \leq -10 \text{ dB} \tag{4.130}$$

Equations (4.128) and (4.130) are combined to provide the bandwidth Δf_{10dB} for which the impedance matching condition is satisfied, yielding the expression of the circuit bandwidth:

$$\Delta f_{10dB} = \frac{\omega_o}{6\pi Q_{in}} \tag{4.131}$$

The bandwidth Δf_{10dB} is three times smaller than the 3 dB bandwidth and 10 dB return loss corresponds to reflected power of only 0.4 dB. For the mid-band of the SKA (300 MHz – 1400 MHz), the centre frequency is 850 MHz. Assuming that R_s = 50 Ω and R_{IN} = 50 Ω, (4.131) is rewritten as:

$$\Delta f_{10dB} = \frac{R_{IN} + R_s}{6\pi L_{IN}} = \frac{100}{6\pi L_{IN}} \tag{4.132}$$

It is assumed that 14 parallel transistors of 0.120 μm for the emitter width and 18 μm for the emitter length are required for noise matching in the IBM BiCMOS8HP process. The unity gain frequency f_T is 25.49 GHz and L_E = 0.312 nH. Using (4.132), the matched bandwidth is equal to 177 MHz. Although this value is an approximation, it provides insight into the bandwidth of the LNA, which is more than five times smaller than the desired bandwidth.

4.7 BANDWIDTH INCREASE WITH MINIMUM IMPACT ON NF

Sections 4.7 to 4.11 are extracted from this author's prior publication [2], with permission. The noise performance of an LNA is strongly related to the noise caused by the input matching network, whereas the impact of the output matching network on noise performance is small and may be negligible. The desired input impedance can be attained by noiseless or noisy input matching networks or by the use of feedback networks. For

narrowband applications, simple matching can be achieved by the use of L, T or Π networks.

Bandwidth is easily increased by a shunt resistance at the input or by resistive feedback. However, the shunt and feedback resistances increase the NF and reduce the gain. Typically, the NF increases by more than 6 dB in the case of resistive shunt, while the impairment is smaller for resistive feedback, the resistance used in the resistive feedback generally being high. It may then appear that wideband matching for ultra-low noise amplifiers can only be achieved by complex matching networks and by configurations such as balanced amplifiers, distributed amplifiers and transmission lines. The power consumption of these configurations is high and they occupy large areas of the chip. In addition, balanced amplifiers demand large quadrature couplers that increase losses [118]; their noise performance is no better than 3 dB [50].

Bandwidth increase can also be attained by impedance transformers, by emitter degeneration with resistive and capacitive loading [115] and by input matching networks such as ladder filters [119]. In [120], broadband matching is obtained by resonating the input reactance of an inductive degeneration common-source with a three-section Chebyshev filter over the LNA bandwidth.

It has been shown that traditional techniques used for bandwidth expansion require additional components at the input, components that impair the noise performance of the LNA. Such techniques include the use of an impedance transformer and of various types of broadband matching networks. As any additional component in the input network affects the NF, it is desirable to reduce the number of matching components to the strict minimum. In addition, to limit the impact of bandwidth increase to the NF, resistive components cannot be used in the signal path, through matching or feedback networks.

4.7.1 Bandwidth extension technique

An approach of particular interest for bandwidth extension consists in coupling two resonant circuits, each with its own resonant frequency [121]. This technique is used in RF

design and allows the sharing of the energy of each tuned circuit by the other. A typical double-tuned bandpass circuit is shown in Figure 4.23, where C_3 is the coupling capacitor.

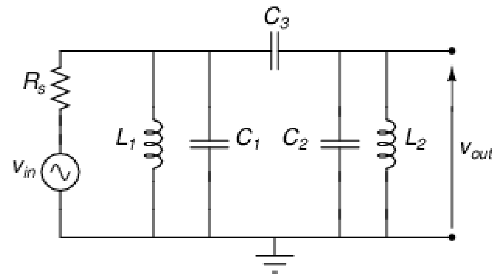


Figure 4.23. Double-tuned bandpass circuit.

The input matching of the broadband common-source inductively degenerated LNA in [122] is investigated in [123]. It is found that, for low frequencies, input matching is achieved by the capacitive feedback from the capacitive load in series with a resistor through the gate-drain capacitance. For high frequencies, matching is obtained owing to the inductive feedback in the source circuit. The LNA requires few components at its input and uses the intrinsic gate-drain capacitance coupled to a capacitor between the drain of the input transistor and the source of the cascode transistor to increase the matching bandwidth. The design strategy constitutes using unfavourable circuit characteristics such as parasitics as circuit elements. This is well paraphrased by Thomas Lee in the preface of [120]: "To no small degree, an important lesson in RF and microwave design is that there are always irreducible parasitics. Rather than conceding defeat, one must exploit them as circuit elements." A detailed analysis of the bandwidth expansion of a SiGe HBT based LNA with minimal impact on noise performance is provided in this section.

A simplified small-signal model of a cascode amplifier is shown in Figure 4.24, where the parasitic base and emitter resistances are neglected and the input impedance of the cascode transistor is Z_L. The input impedance has been estimated in (4.113), where the base-collector capacitance $C_{bc} = C_\mu$ has been neglected. Neglecting the base resistance as well, the input impedance at the base is given by the expression:

$$Z_{in} \cong \omega_T L_E + j\omega(L_E) - \frac{j}{\omega C_{be}} \tag{4.133}$$

Taking into account the effect of the base-collector capacitance, the input impedance is equal to $Z_{in} \parallel \frac{1}{Y_b}$ where Y_b is the admittance seen at the base, after the input capacitor C_{be} as shown in Figure 4.24.

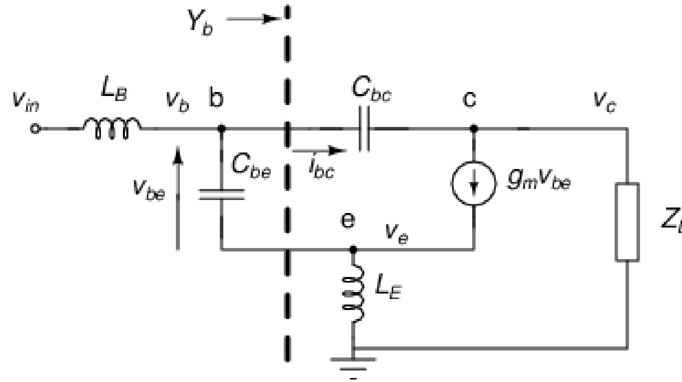


Figure 4.24. Simplified small-signal model of the IDCE cascode amplifier.

The admittance Y_b is calculated by dividing the current i_{bc} by the voltage v_b and it can be shown that Y_b is given by:

$$Y_b = j\omega C_\mu + \frac{j\omega C_\mu g_m Z_L}{1 + j\omega L_E g_m} \tag{4.134}$$

Hence, the admittance Y_b is given by $Y_b = Y_1 // Y_2$ with $Y_1 = j\omega C_\mu$ and $Y_2 = \frac{j\omega C_\mu g_m Z_L}{1 + j\omega L_E g_m}$.

Therefore, Y_b is the result of a capacitor C_μ in parallel with the impedance $Z_2 = 1/Y_2$.
The impedance Z_2 is rewritten as:

$$Z_2 = \frac{(1 + j\omega L_E g_m) Y_L}{j\omega C_\mu g_m} \tag{4.135}$$

where $Y_L = 1/Z_L$.

A capacitor of value C_L is added between the collector of the input and the emitter of the cascode transistor. Z_L is then seen as r_o in parallel with C_L in series with $1/g_m$, $1/g_m$ being the input resistance of the common-base cascode transistor. The transconductances of both the input and cascode transistors are identical. The impedance Z_L is represented in Figure 4.25.

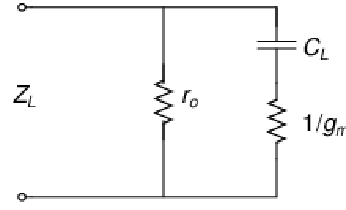


Figure 4.25. Impedance at the output of the input transistor.

The expression of Z_L is given by:

$$Y_L = \frac{1}{r_o} + \frac{j\omega g_m C_L}{g_m + j\omega C_L} \tag{4.136}$$

In replacing Y_L by its expression in (4.136), (4.135) becomes (4.137):

$$Z_2 = \frac{1}{j\omega C_\mu g_m r_o} + \frac{L_E}{C_\mu r_o} + \frac{(1 + g_m j\omega L_E)}{g_m j\omega C_\mu} \frac{j\omega C_L g_m}{(g_m + j\omega C_L)} \tag{4.137}$$

Equation (4.137) shows that Z_2 is formed by a capacitor of value $C_\mu g_m r_o$, a resistance of value $L_E / C_\mu r_o$ and an impedance Z_3 equal to the last term of (4.137), all in series.

The impedance Z_3 is given by:

$$Z_3 = \frac{C_L}{C_\mu (g_m + j\omega C_L)} + \frac{L_E j\omega C_L g_m}{C_\mu (g_m + j\omega C_L)} \tag{4.138}$$

The impedance Z_3 is equal to the sum of Z_4 and Z_5, given by the relations:

$$Z_4 = \frac{C_L}{C_\mu (g_m + j\omega C_L)} \tag{4.139}$$

$$Z_5 = \frac{L_E j\omega C_L g_m}{C_\mu (g_m + j\omega C_L)} \tag{4.140}$$

The impedance Z_4 is equivalent to a resistor of value $C_L / C_\mu g_m$ in parallel with a capacitor of value C_μ. The impedance Z_5 is equivalent to a resistor of value $L_E g_m / C_\mu$ in parallel with an inductance of value $L_E C_L / C_\mu$. Combining Z_{in} and the successive

impedance transformations of Z_L, the input impedance of the cascode amplifier is represented in Figure 4.26.

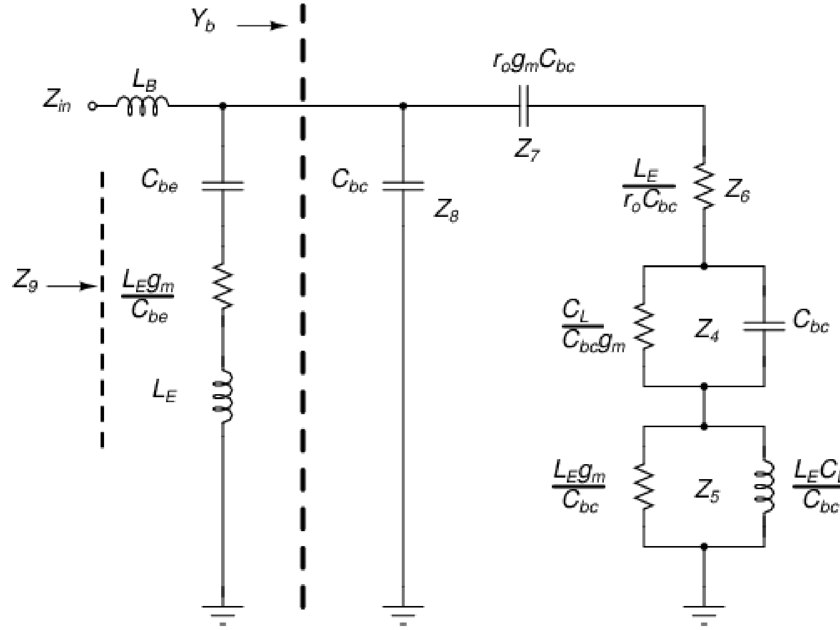


Figure 4.26. Input impedance of the modifier cascode amplifier.

The circuit in Figure 4.26 is a double-tuned resonant circuit with the inductance L_B in series with the impedance Z_9, being the first RLC tuned circuit. The resonant frequency f_1 of this circuit is given by:

$$f_1 = \frac{1}{2\pi\sqrt{(L_B + L_E)C_\pi}} \tag{4.141}$$

The order of magnitude of passive components of Figure 4.26 is evaluated from the typical parameters of a six-finger SiGe HBT [124], where C_{cs} is the parasitic capacitance between the collector and the substrate. The transistor is biased at three different V_{BE} voltages (0.828 V, 0.867 V and 0.921 V) and the area of the transistor is 0.12 × 6 × 1 μm^2.

The Early voltage V_A of SiGe HBTs is generally large compared to Si BJTs when the base Ge profile is graded towards the collector [124]. A typical value of V_A is 50 V, therefore the output resistance $r_o = V_A/I_C$ is also large, in the order of 29 kΩ for I_c = 1.7 mA. The value of the emitter inductance L_E is assumed to be 5 nH and the collector current is 1.7 mA. The capacitor of reactance Z_7 is large compared to C_π, in the order of 15 pF. The value of the resistance Z_6 is 18 Ω, the resistance in Z_4 is 1.9 kΩ and the resistance in Z_5 is 2.9 kΩ. The value of the inductance in Z_5 is 526 nH.

For an operating frequency of 1 GHz, Z_4 is mainly resistive and Z_5 is inductive. Hence, Z_7, Z_4 and Z_5 form the second tuned RLC circuit. The frequency f_2 of this tuned circuit can be approximated by:

$$f_2 = \frac{1}{2\pi\sqrt{r_o g_m L_E C_L}} \tag{4.142}$$

Resonance at f_2 is due to capacitive feedback and f_2 is lower than f_1, the values of the capacitance of Z_7 and of the inductance in Z_5 being higher than C_π and $L_B + L_E$. Owing to an adequate determination of f_1 and f_2, the combined impedance of the coupled tuned circuits can achieve an input reflection coefficient S_{11} that is less than -10 dB in a wide band.

4.7.2 Impact on NF

The second stage of the cascode amplifier being coupled to the first stage through the capacitor C_L, the question of the impact of this coupling on the NF arises. Assuming that the gain of the input stage is high, the contribution of the second stage (Q_2) to the NF is neglected. The bandwidth-enhanced cascode LNA is represented in Figure 4.27 as a cascade of two two-port networks formed by Q_1, the input transistor, and C_L.

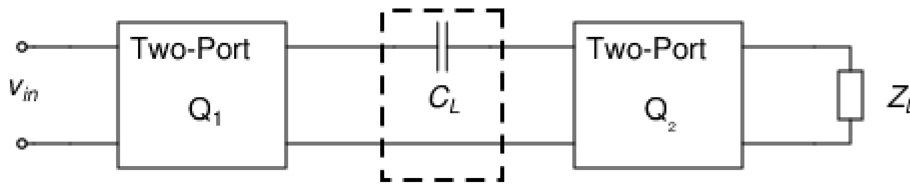


Figure 4.27. Bandwidth-enhanced cascode LNA.

It can be shown that, because the capacitor C_L is noiseless, C_L does not impair the noise factor of the LNA.

4.8 SIMULATION RESULTS

SiGe HBTs of maximum size (0.12×18 μm^2) from the 130 nm IBM BiCMOS8HP process are used for the cascode configuration. F_{min} and R_{sopt} for the cascode LNA are determined by simulation with SpectreRF. Noise matching is done at the high end of the frequency band as, F_{min} being an increasing function of frequency, the minimum achievable noise is better than F_{min} in the bandwidth of the LNA. It is found that $F_{min} = 0.337$ dB and that the

base bias voltage V_B required for minimum NF is 0.7705 V at 1.4 GHz. The plot of F_{min} as function of V_B is shown in Figure 4.28.

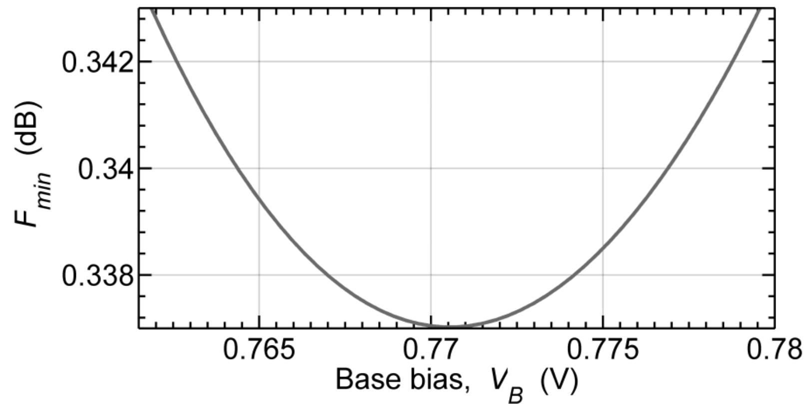


Figure 4.28. Optimum base bias voltage for the cascode amplifier.

A parametric plot of R_{sopt} as function of frequency allows one to determine that 14 parallel transistors are required for noise matching at 1.4 GHz. R_{sopt} is chosen to be slightly higher than 50 Ω because of the parasitic resistance of the base inductor L_B. The impact of transistor paralleling on F_{min} is negligible, F_{min} is unchanged when 14 transistors are connected in parallel at the input and at the output, as shown in Addendum E. The base inductor is approximated by matching the reactive part X_{sopt} of the noise impedance to L_B. Hence, at 1.4 GHz, the noise factor is F_{min}. The emitter inductor is calculated from (4.114) and then fine-tuned by simulation of S_{11}, as shown in Figure 4.29.

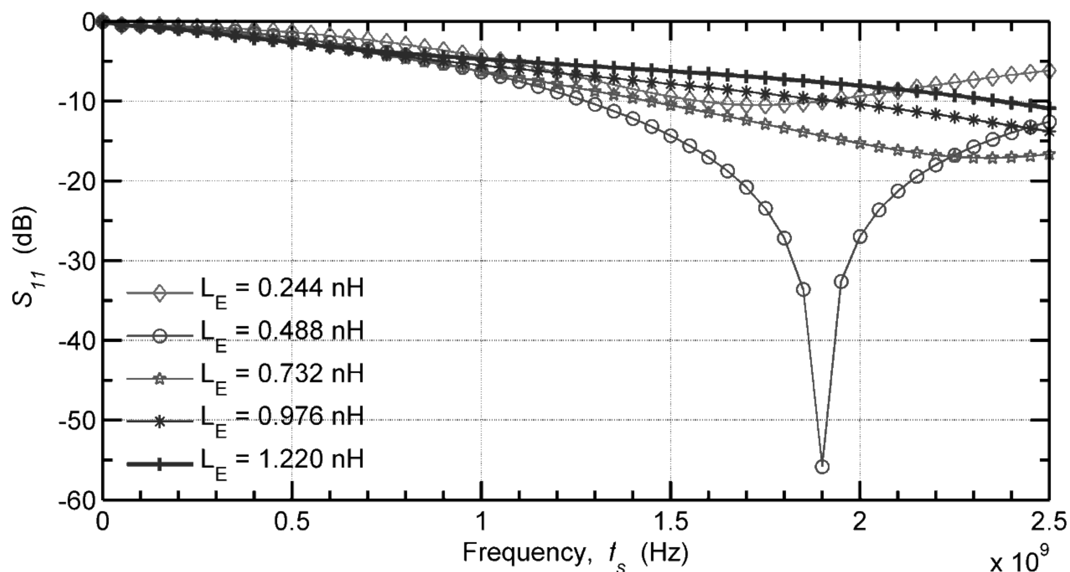


Figure 4.29. S_{11} versus frequency and L_E.

As L_B has been determined on the basis of noise matching only, the addition of L_E cancels the noise matching at 1.4 GHz and the relation between L_B and L_E is determined by (4.125). Therefore, the imaginary part of Z_{in} is not nil at 1.4 GHz. A new value of L_B is determined by a parametric simulation of NF as a function of frequency and of L_B. The resonant frequency of the input matching circuit is found by simulation of S_{11} as a function of frequency. It is found that S_{11} is minimal at 1.89 GHz, a frequency higher than 1.4 GHz at which noise matching has been performed. Therefore, noise is matched at 1.4 GHz while power is matched at 1.89 GHz, which improves bandwidth extension according to Figure 4.29. The latter frequency corresponds to f_1, as predicted in 4.7.1 and given by (4.141).

Narrowband matching being achieved, a capacitor C_L is introduced between the collector of the input transistor and the emitter of the cascode transistor. The value of C_L is found by seeking a flat response for S_{11} in the operating bandwidth.

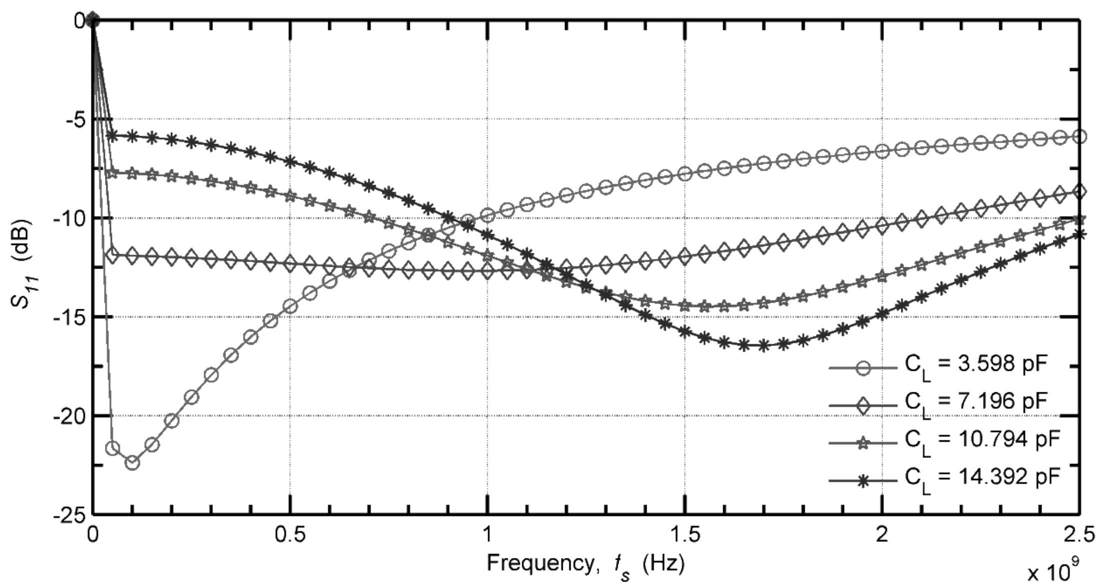


Figure 4.30. Determination of C_L by parametric simulation of S_{11} versus frequency.

For C_L equal to 7.196 pF, S_{11} is near-flat and is less than –10 dB in a wide input frequency bandwidth of the LNA, from 300 MHz to 1.4 GHz. For low values of C_L, the lower resonant frequency f_2 is dominant in S_{11} response. For high values of C_L, S_{11} tends to its minimum value, as shown in Figure 4.30, and the frequency f_1 tends to 1.89 GHz.

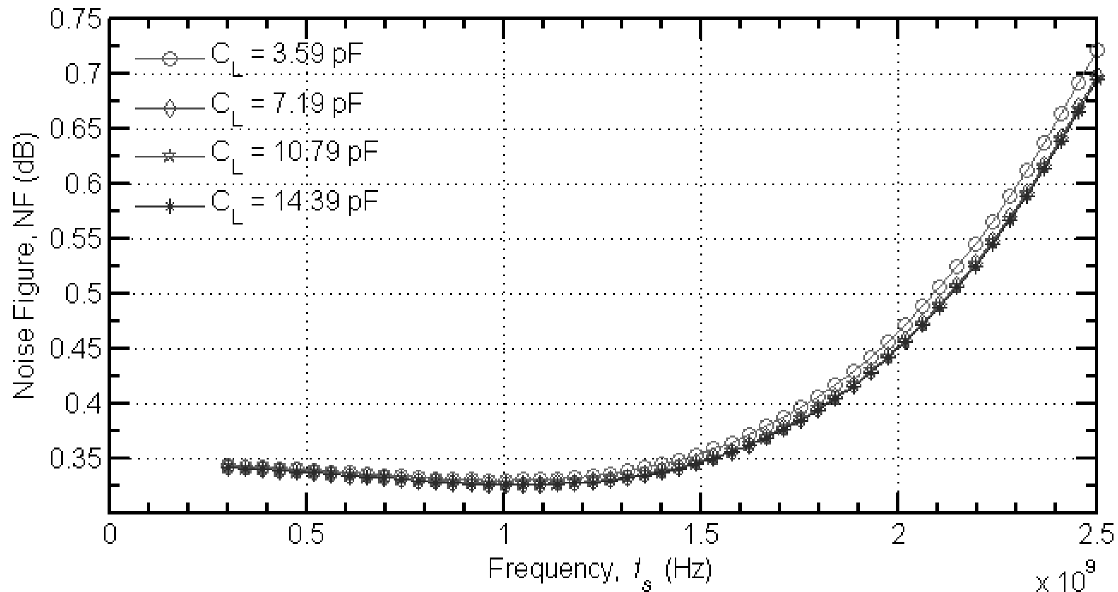


Figure 4.31. NF versus frequency and C_L.

The plot of the NF shows in Figure 4.31 that the effect of C_L on the NF is very small and that the NF varies slightly in the LNA bandwidth. At 1.4 GHz, the NF increases by about 0.002 dB. However, for low values of C_L, the NF increases significantly.

4.9 FREQUENCY SELECTION FOR OPTIMISATION

For applications where very low NFs over a large bandwidth are required, such as in radio astronomy, LNAs are generally designed to achieve the minimum NF at the high end of the frequency range [125]. This is justified by the direct dependence of the NF on the operating frequency. In case power matching is achieved near the high-end frequency, the matching deteriorates at any other lower frequency. However, achieving power matching in the middle of the frequency band may provide optimum results through the whole bandwidth.

It can be seen from Figure 4.30 that the bandwidth extension resulting from coupled resonant circuits is improved with the difference between the resonant frequencies of the tuned circuits. In the case power matching is achieved in the middle of the frequency band, simulation shows that the matching deteriorates significantly in the higher half of the frequency band. It is then desired to perform both power and noise matching at the high-

end of the frequency band. The resonant frequency f_2 of one of the resonant circuit being very low compared to f_1, the resonant frequency of the second tuned circuit, $f_1 - f_2$ is greater than the bandwidth of the LNA and, by coupling the tuned circuits, a wideband matching can be achieved. Therefore, for minimum NF and optimal power matching in a wide bandwidth, it is proposed in this work to perform noise and input power matching at the high end of the LNA input frequency range.

4.10 OUTPUT MATCHING

Impedance matching, especially when required in a large bandwidth, has always been considered a difficult task and feared by many designers. The transfer of power from the LNA to the load is maximised when the output impedance of the LNA is matched to the resistance of the load, which is 50 Ω. The most frequently used output matching networks found in RF and microwave design are of L, Π and T types. Matching networks of the L type are two-element networks whose Q factor is the minimum possible and is only determined by the output and load resistances according to the expression:

$$Q = \sqrt{\frac{R_L}{R_o} - 1} \tag{4.143}$$

where R_L and R_o are respectively the load and output resistances.

An improved Q factor can be obtained by using matching networks of the Π and T types, which are three-elements networks, as shown in Figure 4.32 where X_1, X_2 and X_3 are passive reactive elements. Matching networks of the Π and T types result from back-to-back L networks and are analysed as combinations of L networks. Networks built with single L networks and back-to-back L networks are narrow-band, with a limited bandwidth improvement obtained from the decrease of the Q factor. A further decrease of the Q factor can be achieved by using a cascaded L network instead of back-to-back L networks. It can be shown that the maximum bandwidth is obtained when the virtual resistance between two cascaded L networks is equal to the geometrical mean of the output resistance and the resistance of the load.

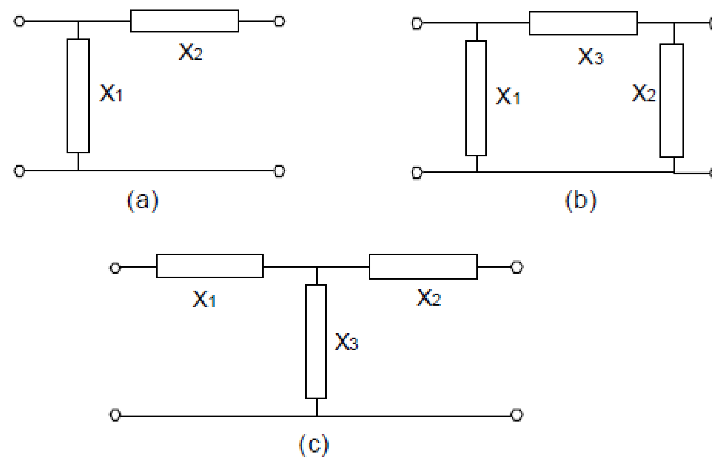


Figure 4.32. Matching networks: (a) L - (b) Π - (c) T.

The output matching resulting from two cascaded L networks requires four passive components, including two inductors. A further bandwidth increase is possible owing to additional cascaded L networks, hence additional inductors. When on-chip inductors are used, the impact of several inductors in the LNA output matching network can impair the NF significantly. It is then desired to reduce the number of inductors required for output matching to the minimum possible.

4.10.1 Output impedance of the cascode LNA

The small-signal model of the cascode transistor is shown in Figure 4.33 where Z_i is the output impedance of the input transistor, C_L is the coupling capacitor between the collector of the input transistor and the emitter of the cascode transistor and Z_o is the output impedance of the LNA. The output impedance Z_o is calculated by applying the signal v_o at the output and measuring the ratio $Z_o = v_o/i_c$. Z_o is equal to two parallel impedances, as shown by the expression:

$$Z_o = Z_o^{'} \,||\, \frac{1}{j\omega C_\mu} \tag{4.144}$$

where $Z_o^{'}$ is the impedance seen from the collector of the cascode transistor when the base-collector capacitance C_μ is not included in the calculations.

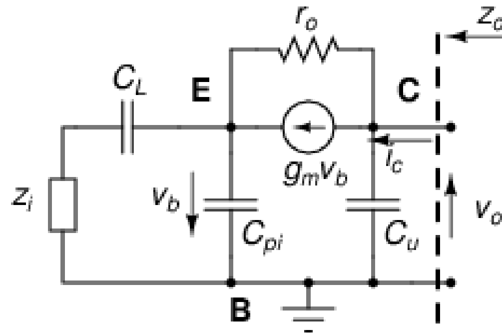


Figure 4.33. Small-signal model of the cascode transistor.

In applying KVL between nodes E and C and KCL at node E, it can be shown that the impedance $Z_o^{'}$ is given by:

$$Z_o^{'} = r_o \left(1 + \frac{g_m + \frac{1}{r_o}}{\frac{1}{Z_i + \frac{1}{j\omega C_L}} + j\omega C_\pi} \right) \tag{4.145}$$

with $C_\pi = C_{pi}$

Generally, r_o is very high and $|Z_i| >> \left| \frac{1}{j\omega C_L} \right|$, and assuming that $\omega C_\pi |Z_i| >> 1$, (4.145) is approximated by the equation:

$$Z_o^{'} = r_o \left(1 + \frac{g_m}{j\omega C_\pi} \right) \tag{4.146}$$

The assumptions above are justified because the output impedance of the input transistor with inductive degeneration is equal to $Z_i = r_{o1}(1 + j\omega g_{m1} L_E)$, where r_{o1} is the output resistance - generally very high - and g_{m1} is the transconductance of the input transistor, L_E being the emitter inductor.

The Smith chart in Figure 4.34 shows that the impedance trace is at its outer boundary, which corresponds to a coefficient reflection whose absolute value is unity, hence to an infinite output resistance, as shown by the equation $\Gamma = Z_L - Z_o / Z_L + Z_o$, where Z_L is the impedance of the load, Z_o is the impedance at the output of the cascode LNA and Γ is the

coefficient of reflection. At low frequencies, the output impedance Z_o is infinite and resistive. Recent tools such as 3D Smith chart (www.3dsmithchart.com), available since 2017, can be used for this analysis.

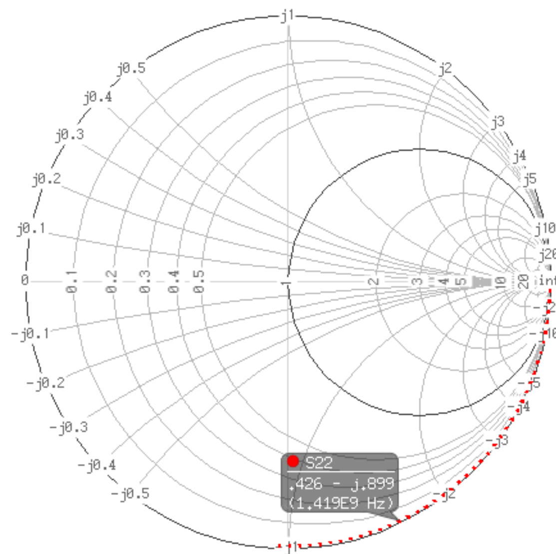


Figure 4.34. Plot of the output impedance with highly inductive load (1 mH).

The output circuitry of the cascode amplifier for impedance matching is represented in Figure 4.35, where Z_o results from the capacitance C_μ in parallel with the resistance r_o in series with the capacitance $r_o g_m / j\omega C_\pi$. At the operating frequency, Z_o is much higher than 50 Ω, therefore the requirement is to match a very high impedance to a load of 50 Ω with minimum impact on the NF. In the case of a cascode amplifier without inductive degeneration and without C_L, the output resistance R_{out} is equal to $(\beta+1)r_o$ at low frequencies, a very large expression.

In order to limit the impact of the broadband matching network on the NF, the proposed matching network should mostly be built from reactive components. The collector of the cascode transistor is biased from V_C through the input of the matching network, which serves as load for the output transistor.

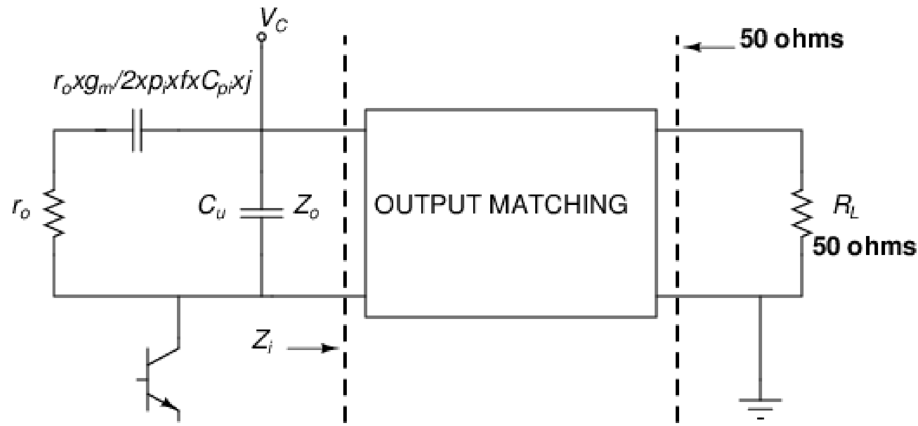


Figure 4.35. Cascode output impedance and output matching.

It is noted that a DC path between the output of the LNA and the load should be avoided. In case the output is directly connected to R_L, a direct DC path from the amplifier to the ground may exist; good practice requires blocking any DC from the amplifier to the load. The diagram in Figure 4.34 is realised with a highly inductive load of 1 mH. However, such a value is very high and not practical for a realisation on Si. A typical value of 10 nH is used for Figure 4.36 which shows that the trace of the impedance remains at the outer boundary of the chart. As long as this trace is at the outer boundary, Z and Y circles of constant resistance on the chart cannot be used to move the impedance line to the centre of the chart because the impedance trace is tangent to such circles at the edges of the horizontal line of nil reactance.

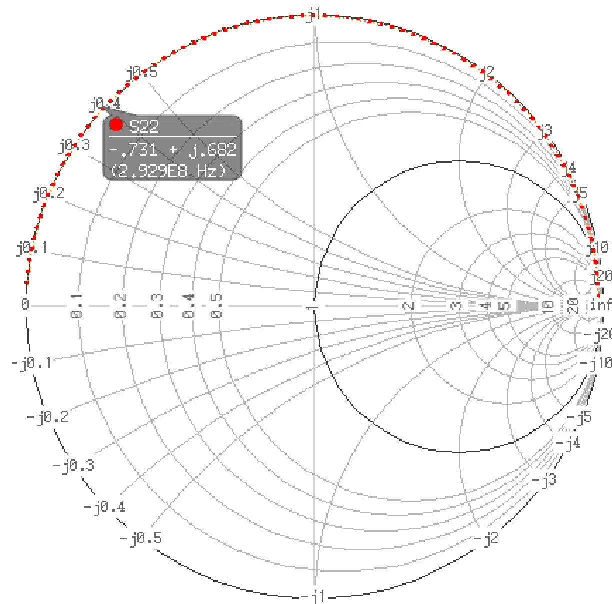


Figure 4.36. Plot of the output impedance at low inductive load (10 nH).

The impedance trace can be moved within the chart by the use of a shunt resistance at the output of the cascode transistor. Generally, the output of the transistor is a tank circuit whose resistance determines the gain of the amplifier. The contribution of this resistance to the NF may be negligible when its value is high. This is shown by simulation for values that are higher than 50 Ω. The trace can also be displaced by using an inductive peaking circuit, which may in addition improve the bandwidth of the tuned circuit connected to the collector of the output transistor significantly. Inductive peaking originated from valve television technology and was used extensively up to the 1970s to provide a flat response over a 4 MHz bandwidth for video amplifiers [126]. Although acceptable matching has been achieved, the impairment of the NF is high and simulations show a deterioration of at least 0.1 dB for a peaking resistance of only 15 Ω. Because the resistance is in series with the collector inductor, its value is small, which has a significant impact on the NF and defeats the objective of this work [127].

Finally, active devices can be used for impedance transformation. An emitter follower at the output of the LNA can be used for such a function. However, the impact on power consumption and on NF is a justifiable deterrent to this approach. It appears that the tank circuit is the appropriate alternative, as it allows the achievement of broadband matching with little impact on the NF.

4.10.2 Output matching network

Filter design can be seen as an impedance matching problem, whose objective is to maximise the transfer of power between a source and a load within the operating frequency band. It is desired to design the filter in such a way that the 50 Ω load will be a far-end element of the filter. In this way, the number of additional components is minimised, as well as the impairment of the NF due to the filter.

Three approaches can be used for solving an impedance matching problem: the assistance of the Smith chart approach, the analytical approach and the CAD approach. In the Smith chart approach, matching is simply done with only the assistance of the Smith chart. The analytical approach has limitations due to the complexity of numerical methods used; this complexity is increased by complex sources and loads and when the matching bandwidth

is large. Furthermore, this approach may not reach a solution. The CAD approach, preferred by most designers, uses computer-based numerical optimisation and can be divided into two techniques: brute force and the real frequency technique. In the brute force technique, a CAD tool optimises the elements of a matching network for a known topology provided by the designer. Contrary to the brute force technique, the real frequency technique generates a possible topology for which it optimises the elements. This highly mathematical technique, introduced in 1977 by Prof. H.J. Carlin, leads to stable and convergent solutions and has recently inspired considerable research. The approach used in this work is based on the Smith chart approach and on the brute force technique using MATLAB™.

The impedance to be matched to a 50 Ω load is derived from simulation and entered in a MATLAB™ script running under the MATLAB™ RF toolbox environment. Based on ripple and attenuation requirements, the topology of the filter from which the matching network is derived is also entered in the script. The script uses an objective function –in the case of this study the reflection coefficient at the plane between the matching network and the 50 Ω load - to search for all possibilities that maximise the transfer of power between the cascode transistor and the resistive load in the bandwidth of the LNA. The best matching solution is found when the algorithm converges and when the average of reflection coefficients at discrete frequencies is minimal.

The frequency response of an analogue filter can be evaluated by four main approximations of its transfer function H(s): Inverse Chebyshev, Chebyshev, elliptic, and Butterworth functions. Butterworh filters provide the best smooth response in the passband and stopband frequency range. The approximation also provides the best phase response in terms of linearity. However, a higher order is required to match the transition offered by Chebychev and elliptic filters. For filters of the same order, in terms of the transition between the passband and the stopband, the fastest transition is achieved by the elliptic approximation, then by the Chebyshev and the inverse Chebyshev approximations. The slowest transition is achieved by the Butterworth approximation, which is mostly preferred when moderate selectivity is required [128].

In view of their existing ripple in the stop band, inverse Chebyshev and elliptic approximations are not desired for the output matching of the LNA. Despite the low attenuation achieved by the Butterworth approximation, this approximation is used for the output matching network owing to its phase response and its smooth pass-band response. Details on the design of the matching network are provided in Chapter 5 and the MATLAB™ optimisation script is provided in Addendum G.

4.11 PROPOSED DESIGN METHODOLOGY

This chapter has identified and analysed the main elements affecting the noise performance of an integrated LNA based on SiGe HBTs. The findings of the analysis allow the derivation of a design methodology for a sub-1 dB LNA that can be used for the SKA. The design of a sub-1 dB LNA based on SiGe HBTs starts with the selection of the relevant semiconductor process. The preferred semiconductor process should have high β, high f_T and low base and emitter parasitic resistances. In addition, from (4.98), it is desired to use a process with a low emitter width, w_e. The preferred topology is the IDCE and noise matching is achieved by the sizing of a single transistor or by the paralleling of several identical transistors, depending on the operating frequency. Broadband input impedance matching is performed by L_E, L_B and by the addition of a capacitor C_L between the collector of the input transistor and the emitter of the cascode transistor. The capacitor is in parallel with an external choke for biasing. Finally, broadband output impedance matching is performed by a fourth order Butterworth based approximation that is optimised for power transfer by a MATLAB™ script. The complete steps of the methodology are:

1- Prerequisites: Frequency band (F_1 to F_2), fabrication SiGe HBT process, supply voltage, source and output impedances are real and are respectively R_s and R_{out}. The minimum and maximum emitter lengths for the process are respectively l_{emin} and l_{emax}.

2- Determine by simulation the base bias voltage V_{B1} and the collector current I_{C1} for a single CE transistor for a minimum noise factor F_{min} at F_2. The transistor of minimum size in the process is used. Determine V_B and the collector current I_C for two identical transistors of minimum emitter length in a cascode configuration. The voltages V_{B1} and V_B should be close.

3- Plot R_{sopt} as function of frequency for the transistor and find its value for a bias value of V_B at F_2. If $R_s > R_{sopt}$, then add a capacitor C_{BE} between the base and the emitter. The value of the capacitor is determined by (4.103). If $R_s < R_{sopt}$, considering that R_{sopt} is inversely proportional to the length of the emitter, determine if there is an emitter length l_e for which $R_{sopt} = R_s = \Re\{Z_{in}\}$ and $l_{emin} =< l_e =< l_{emax}$. If l_e exists, then the length of the emitter that achieves noise matching is l_e. If l_e does not exist and $R_{sopt} > R_s = \Re\{Z_{in}\}$ for the transistor of maximum emitter length in the fabrication process, determine the number of transistors in parallel required to achieve $R_{sopt} = R_s = \Re\{Z_{in}\}$. This number is m. At this point, the real part of the noise optimum noise impedance is matched to the source resistance.

4- Extract r_b and C_π from Z- and Y-parameters of the m parallel transistors at a frequency equal to F_2 and for the optimum bias voltage V_B. Z- and Y-parameters are determined by simulation.

5- Estimate by calculation L_E and L_B using (4.114) and (4.116). The inductor L_E is on-chip, the inductor L_B is off-chip.

6- Fine-tune L_B by parametric simulation of the NF of the IDCE amplifier at 1.4 GHz as a function of frequency at V_B, L_B being the parameter. Fine-tune L_E by parametic simulation of S_{11} as a function of frequency, the parameter being L_E. The fine-tuning of L_B and L_E is completed when the noise factor is equal to F_{min} at 1.4 GHz, for a bias voltage of V_B.

7- The capacitor C_L is added between the collector of the input transistor and the emitter of the cascode transistor. A parametric simulation of S_{11} as a function of frequency and of C_L - the parameter - allows one to determine the value of C_L for which S_{11} is flat in the frequency band. This value corresponds to the best possible input impedance matching.

8- For output matching, the output impedance of the cascode amplifier is first determined by simulation of S_{22} and derivation of $Z_{out} = Z_{22}$ from the equation $Z_{out} = Z_{22} = R_o \dfrac{1+S_{22}}{1-S_{22}}$, where $R_o = 50\ \Omega$.

9- Assuming a moderate gain (~ 20 dB), a value R_L is chosen based on the gain in the expression: $G = \frac{\beta^2 R_L}{\left[1 + \left(\omega\beta/2\pi f_T\right)\right]^2 R_s}$, where R_s is the source resistance [90].

10- Simulation of the NF and the gain as functions of R_L allows determination of a trade-off between the NF and the gain in such a way that the NF is not significantly degraded.

11- The frequencies F_1 and F_2, Z_{out} and R_L are used as inputs of a MATLAB™ script that optimises power transfer between the output transistor(s) and the 50 Ω load through the matching network and provides the values of the components of the network.

4.12 CONCLUSION

This chapter provided the basics of the electronic noise theory that are required for the analysis of electronic noise in SiGe HBTs and linear networks. Using the two-port noise theory, the relationships between the four noise parameters and the parameters of a SiGe HBT were investigated. The investigation allowed identification of the parameters of a SiGE HBT process that are most relevant to low NF: high β, high f_T, low base and emitter parasitic resistances, and a small emitter width. Using the IDCE topology, the requirements for optimum NF for an integrated LNA were identified. The main design performance parameter being the NF, the chapter investigated the possibility of achieving simultaneous noise matching and broadband impedance matching in a case where additional components for the matching networks are reduced to the strict minimum. It was shown and demonstrated that noise matching can be achieved through the paralleling of identical transistors, while broadband input impedance matching can be performed by the use of an additional on-chip noiseless component, a capacitor between the collector of the input transistor and the emitter of the cascode transistor. An on-chip circuit for broadband output matching was proposed; the circuit is optimised by a MATLAB™ script. Finally, a designed methodology for LNAs was proposed.

CHAPTER 5 IMPLEMENTATION AND RESULTS

5.1 INTRODUCTION

As a result of the theoretical analysis provided in the previous chapter, this chapter describes and justifies the design steps of the LNA. Design steps are validated by simulations that also serve to verify the theoretical models.

The first implementation step is the determination of the collector current for minimum NF for a single transistor. The bias conditions are determined, as well as the minimum achievable noise factor, F_{min}. For transistors in cascode configuration, the optimum bias conditions differ slightly from the single transistor case, because of the dependence of NF on power gain, in compliance with Friis' equation.

The optimum noise matching resistance for a cascode amplifier with transistors of minimum size for the length of the emitter (2.5 μm), is evaluated by simulation. It is found that, at 1.4 GHz, an optimum noise resistance of 50 Ω cannot be achieved. The matching of R_{sopt} to a source of 50 Ω is derived from the conclusions of Section 4.4.10. The initial sizing of the emitter and base inductors L_E and L_B for impedance matching is performed after the determination of f_T and C_{be}, C_{be} is extracted from the Z- and Y-parameters of the input transistor.

5.2 DESIGN AND SIMULATION

The cascode amplifier is biased at constant emitter current density; it then operates as class A. This is desired, as class A amplifiers are highly linear. Despite having low efficiency, a high voltage swing can be achieved by the simulation circuit in Figure 5.1, with a maximum swing of $2V_{DD}$, where V_{DD} is the supply voltage. The values of coupling capacitors C_1 and C_2 are in the range of µFs, R_s and R_{out} are the source and load resistances and are equal to 50 Ω.

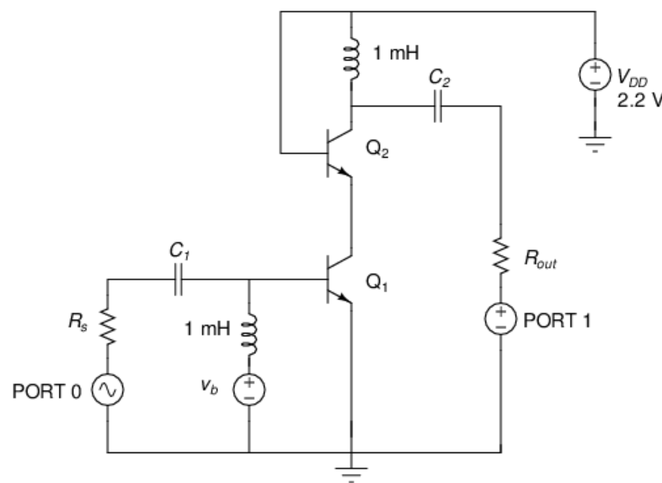


Figure 5.1. Simulation circuit for the cascode LNA.

5.2.1 Biasing of transistors

The IBM BICMOS8HP process provides CBE and CBEBC configurations for NPN transistors. The CBE configuration has traditionally been used for SiGe HBT devices. For operating frequencies in the 100 GHz region or when the impact of parasitic resistances on performance is significant, the CBEBC configuration is preferred because f_T and f_{max} are higher. This improvement is explained by the symmetric spreading of the collector current, resulting in the decrease of the Kirk effect, the parasitic resistances r_b and r_c and the charging time of carriers. The layout of an NPN CBEBC transistor with base, emitter and collector contacts is represented in Figure 5.2.

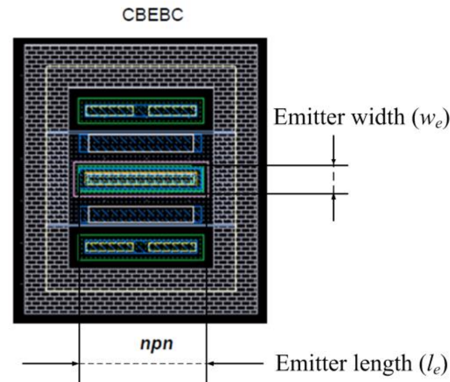


Figure 5.2. Transistor layout: CBEBC (w_e = 0.120 µm, l_e = 18 µm).

Taken from [129], with permission.

It is shown in [130], that the performances of the CBEBC (0.12 × 12) and CBE (0.12 × 12) devices are closely similar. These devices provide good extrinsic *re,* r_b and r_c as well as intrinsic r_b and r_c, with slightly better performances for the CBEBC (0.12 × 12) configuration. The process offers a single emitter strip with an emitter length of 0.52 µm to 18 µm. Regular high-performance and enhanced high-performance devices are available in both CBE and CBEBC configurations. The characteristics of SiGe HBT NPN devices for several generations of the same BiCMOS technology, including the BICMOS8HP process, are shown in Table 5.1 [131].

Table 5.1. Nominal characteristics of NPN devices in IBM BICMOS8HP.

SiGe HBT Parameters	IBM 5HP	IBM 7HP	IBM 8HP
Drawn Emitter Width (µm)	0.5	0.2	0.12
Peak β	100	200	460
V_A (V)	65	120	> 150
BV_{CEO} (V)	3.3	2.5	1.8
BV_{CBO} (V)	10.5	7.5	6
Peak f_T (GHz)	48	120	210
Peak f_{max} (GHz)	69	100	285
min NF_{min} (dB)	0.8	0.4	< 0.3

Table 5.1 shows the characteristics of high-performance transistors only, for which the following typical values are used (IBM 8HP): f_T = 200 GHz, BV_{CEO} = 1.8 V and BV_{CBO} = 6 V. For high-breakdown devices, f_T = 57 GHz, BV_{CEO} = 3.55 V and

BV_{CBO} = 12 V. For this thesis, high-performance transistors have been selected owing to their high f_T.

The base DC voltage being around 0.7 V, the voltage chosen for the collector is 1.8 V. Circuits for which the output voltage operates above BV_{CEO} are found in RF applications requiring relatively large voltage swing and most BJTs do not suffer permanent damage after operating in the avalanche region. It is noted that generally, the base is not opened and that in such a case the collector-emitter breakdown voltage is between BV_{CBO} (6 V) and BV_{CEO} (1.8 V). In operation, BV_{CEO} is then higher than the collector-emitter voltage used for the simulation in order to avoid the increase in the NF possibly caused by avalanche. The simulation circuit for a single transistor is shown in Figure 5.3.

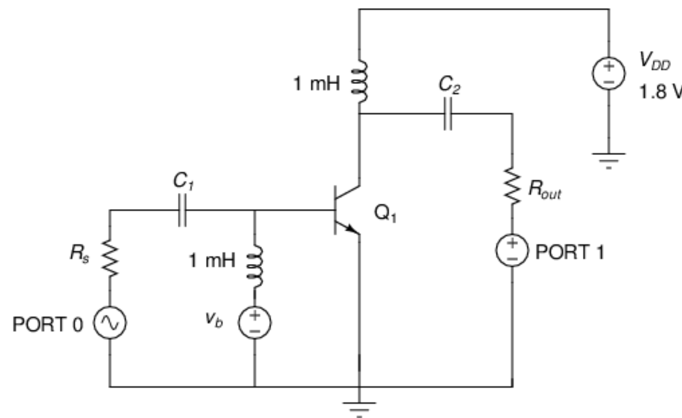


Figure 5.3. Simulation circuit for a single transistor.

The graph in Figure 5.4 provides the simulation results for a single transistor (npn_inh) of minimal size (width of 120 nm and length of 2.50 µm). The NF_{min} is 0.298 dBm at 1.4 GHz for a base bias voltage of 762.6 mV. The base voltage is swept from 745 mV to 780 mV and, at minimum NF, the collector current I_C is 45.36 µA and the collector current density is 151.2 µA/µm^2. The version of the design kit is V1.6.0.1HP, the library model is 1.6.0.1HP and the configuration of the NPN transistor is CBEBC.

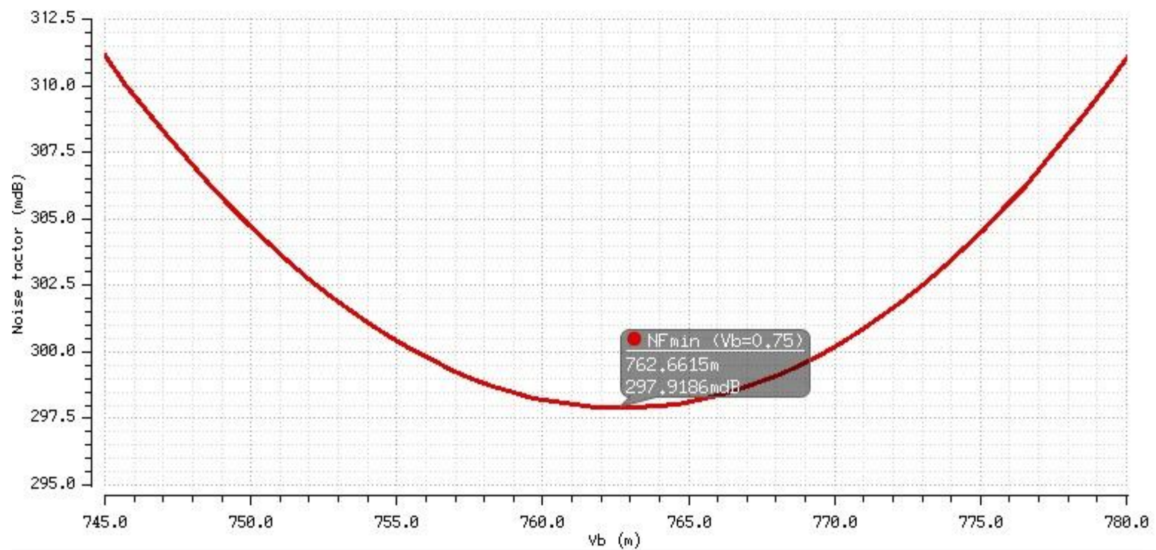


Figure 5.4. Optimum base bias voltage for a single transistor.

The next step is evaluating the optimum collector current in a cascode configuration. The input and output transistors Q_1 and Q_2 are equal in size in order to ensure that both transistors are biased at the same collector current density for minimum NF. However, Q_2 can be larger than Q_1 in order to improve the gain and the linearity, but with a small degradation of the NF [132]. As shown in Figure 5.5, the optimum base bias voltage for the cascode configuration is 775.14 mV, corresponding to an NF_{min} of 0.325 dBm and a collector current of 71.86 µA. The base voltage is swept from 753 mV to 800 mV.

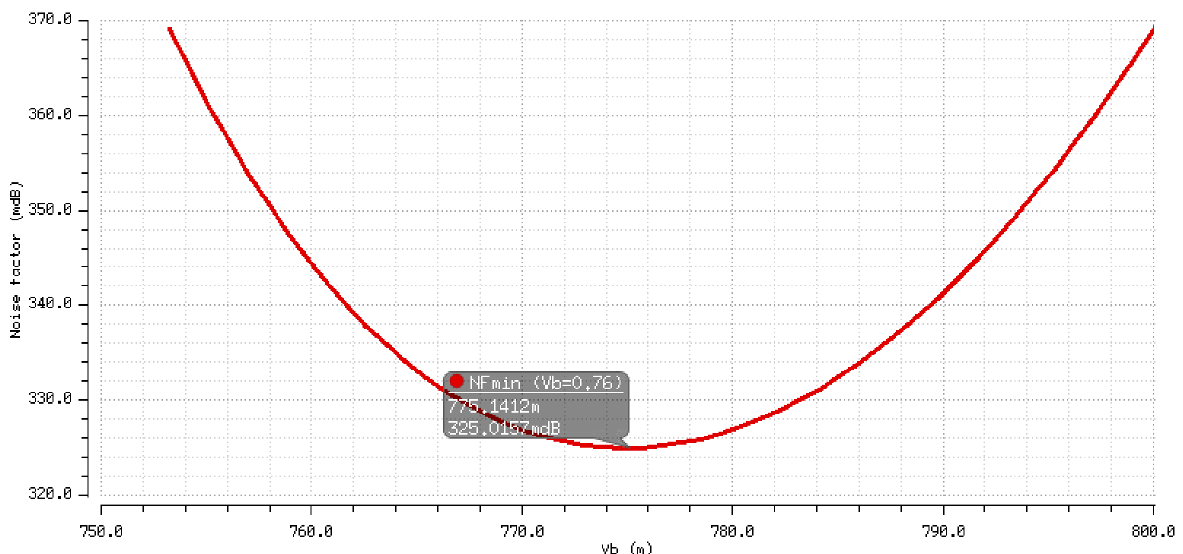


Figure 5.5. Optimum base bias voltage for a cascode amplifier.

For amplifiers with stages in cascade such as the cascode LNA, the low NF of the first stage is useful only if combined with a high power gain G_A. Therefore, the noise measure parameter $M = (F_{min}\text{-}1)/(1\text{-}1/G_A)$ is a better metric when compared to F_{min} as it combines both the minimum noise factor and the gain of the first stage. This parameter was first defined in [133]. The graph of M and NF_{min} as function of V_B is represented in Figure 5.6. It is found that both NF_{min} and M (dB) lead to very close values of V_B, the gain G_A being high at the operating frequency of 1.4 GHz.

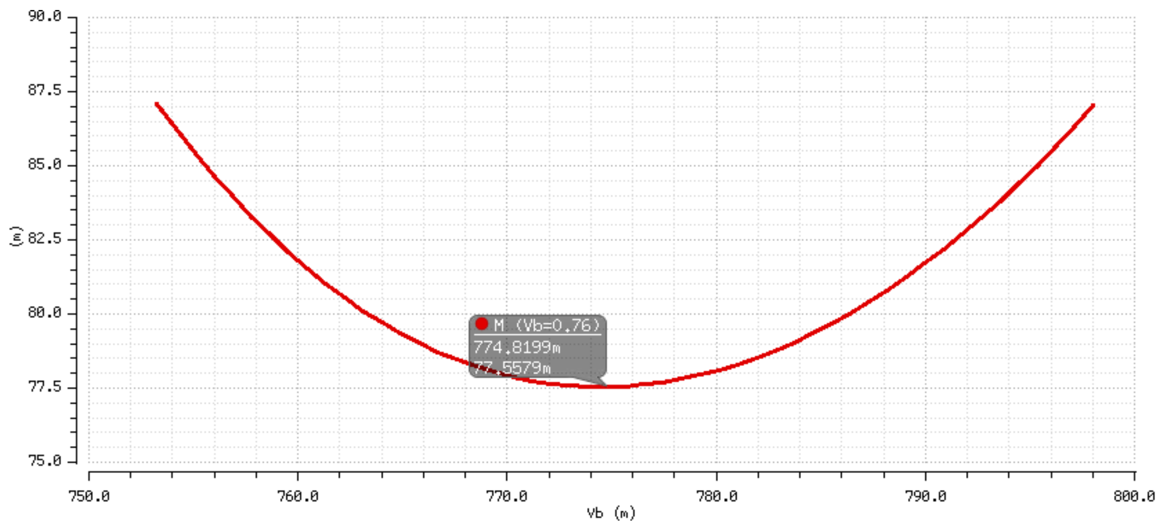


Figure 5.6. *M* versus base bias voltage.

The M curve reaches a minimum for V_B = 774.81 mV, which corresponds to an NF_{min} of 0.325 dB. The collector current through Q_2 and Q_1 is 70.8 µA and the size of both transistors is 120 nm × 250 nm. The supply voltage is 1.8 V. Q_1 is not biased at the absolute optimum current density anymore: the minimum NF for the cascode is achieved by increasing the gain of Q_1, which decreases the noise contribution due to Q_2 but increases the noise due to Q_1 slightly.

5.2.2 Sizing of transistors

It has been shown in Chapter 4 that noise matching can be achieved by varying the length of the emitter. The optimum noise resistance being inversely proportional to the emitter length, simulation of the NF is performed using maximum size transistors, in order to determine the minimum value of R_{sopt} in a cascode configuration.

Using the release V1.6.0.1HP of the IBM BiCMOS8HP design kit, the bias parameters for minimum NF for the cascode amplifier are: V_B = 0.7705 mV, NF_{min} = 0.337 dBm, I_C = 480.3 µA; the size of the transistors is 0.120 µm × 18 µm. The DC operating parameters provided by SpectreRF are for Q_1: g_m = 20.06 m, beta = 529.8, I_C = 548.1 µA, C_{be} = 85.07 fF, C_{bc} = 30.94 fF, r_{bi} = 1.934 Ω, r_e = 0.537 Ω, r_{bx} =11.44 Ω, f_T = 28.84 GHz. The DC operating parameters for Q_2 are: g_m = 20.06 m, beta = 462.1, I_C = 548.1 µA, C_{be} = 84.9 fF, C_{bc} = 33.59 fF, r_{bi} = 1.886 Ω, r_e = 0.537 Ω, r_{bx} = 11.43 Ω, f_T = 28.46 GHz. The plot of NF_{min} versus V_B is shown in Figure 5.7.

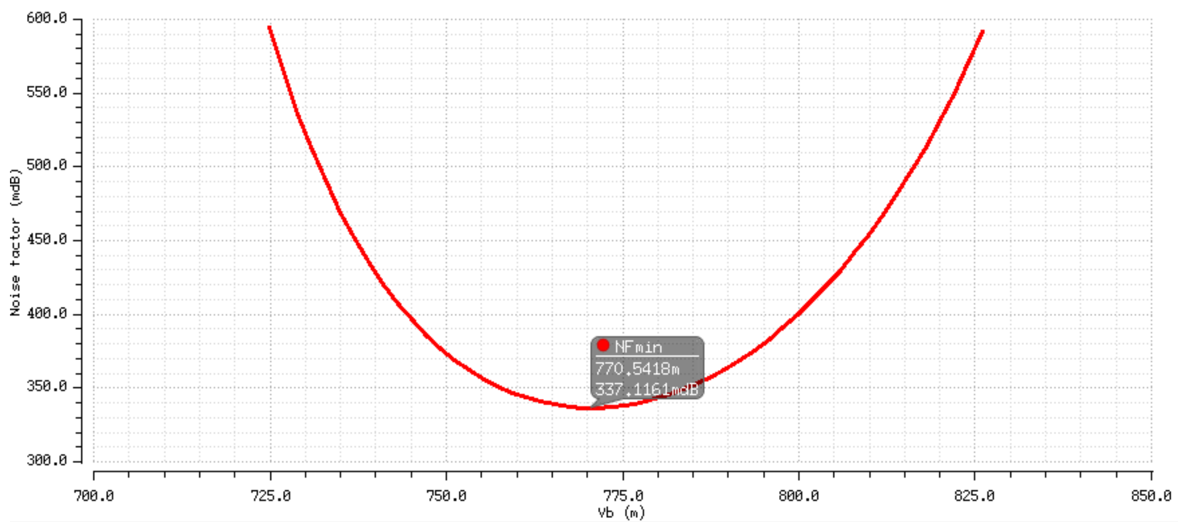


Figure 5.7. NF_{min} versus V_B.

The optimum noise resistance R_{sopt} is approximated by sweeping the source resistance R_s; the graph in Figure 5.8 shows that the minimum NF is achieved for R_s = 921.5 Ω.

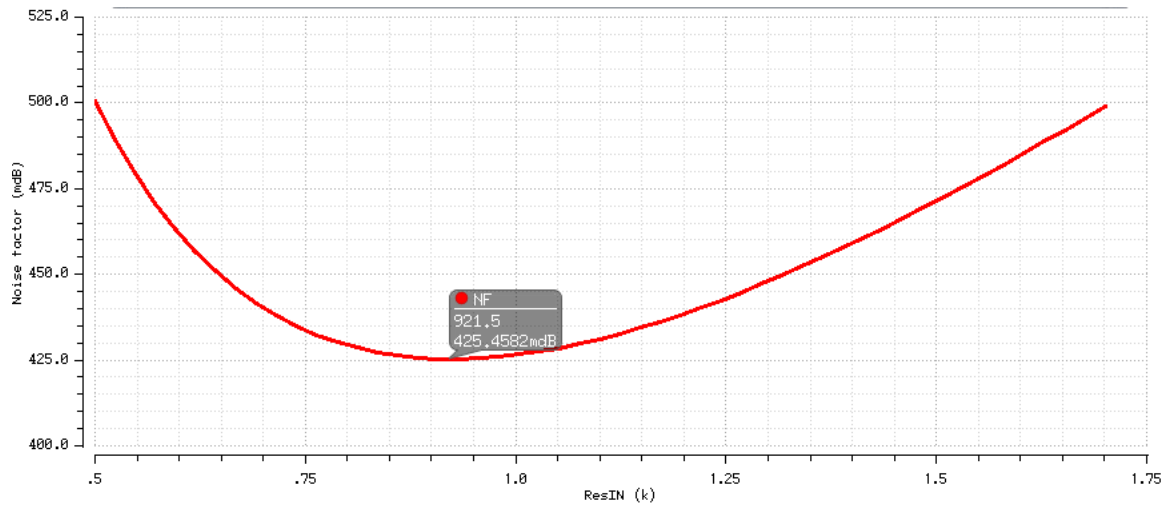


Figure 5.8. NF versus R_s (m=1).

Therefore, for a multiplicity factor m of 1, a R_{sopt} of 50 Ω cannot be achieved at 1.4 GHz. Using the conclusions of Section 4.4.10, it is found that in order to achieve an input noise resistance of 50 Ω, 18 transistors of 0.120 µm × 18 µm and one transistor of 0.120 × 7.73 µm, all in parallel, are required. It is proposed to use only 18 transistors of 0.120 µm × 18 µm, which will provide an R_{sopt} of 51.66 Ω. It is expected that the parasitic resistance of the input inductor L_B will add to the source resistance of 50 Ω, hence R_{sopt} will be slighty higher than 50 Ω. This initial approximation of R_{sopt} is shown in Figure 5.9.

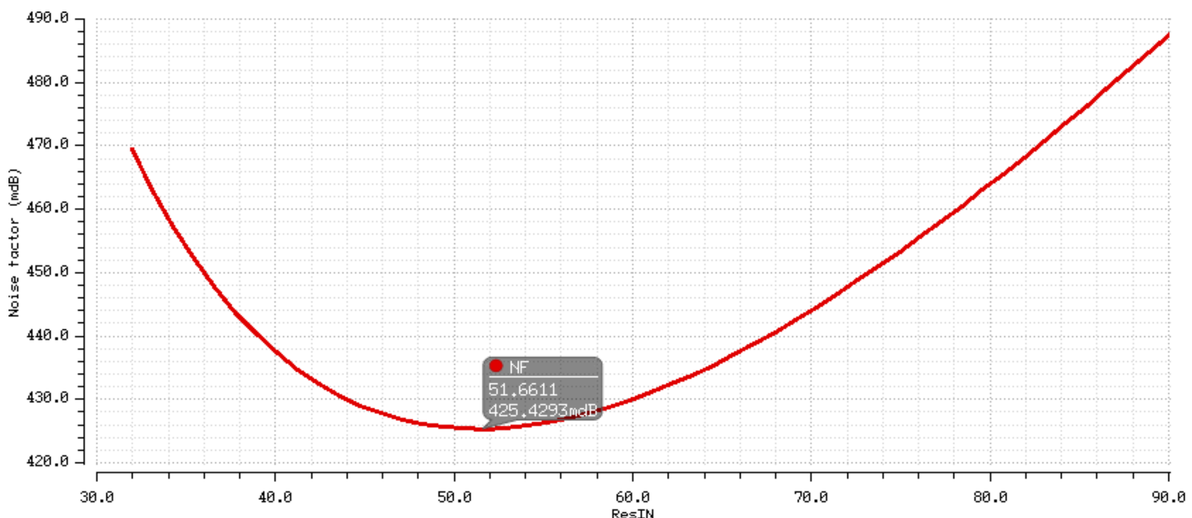


Figure 5.9. NF versus R_s (m = 18).

The determination by simulation of the optimum noise resistance in sweeping R_s does not take into account the reactive part of the optimum noise impedance Z_{sopt}. A better approximation of R_{sopt} can be obtained by plotting the value of R_{sopt} calculated by the R_{opt}/X_{opt} SKILL script in Addendum D. The values of R_{sopt} and X_{sopt} are respectively 37.7 Ω and 32 Ω. Therefore, in order to achieve a R_{sopt} close to 50 Ω, the number of transistors in parallel is reduced from 18 to 14.

The simulation of the NF, R_{sopt} and X_{sopt} as functions of R_s shows that for 14 transistors in parallel, R_{sopt} = 51.14 Ω (blue line), X_{sopt} = 41.78 Ω (red line). The NF shows in Figure 5.10 that minimum NF is achieved when the source resistance is equal to 65.55 Ω (the minimum NF is not achieved at 50 Ω because of the reactance part of Z_{sopt}).

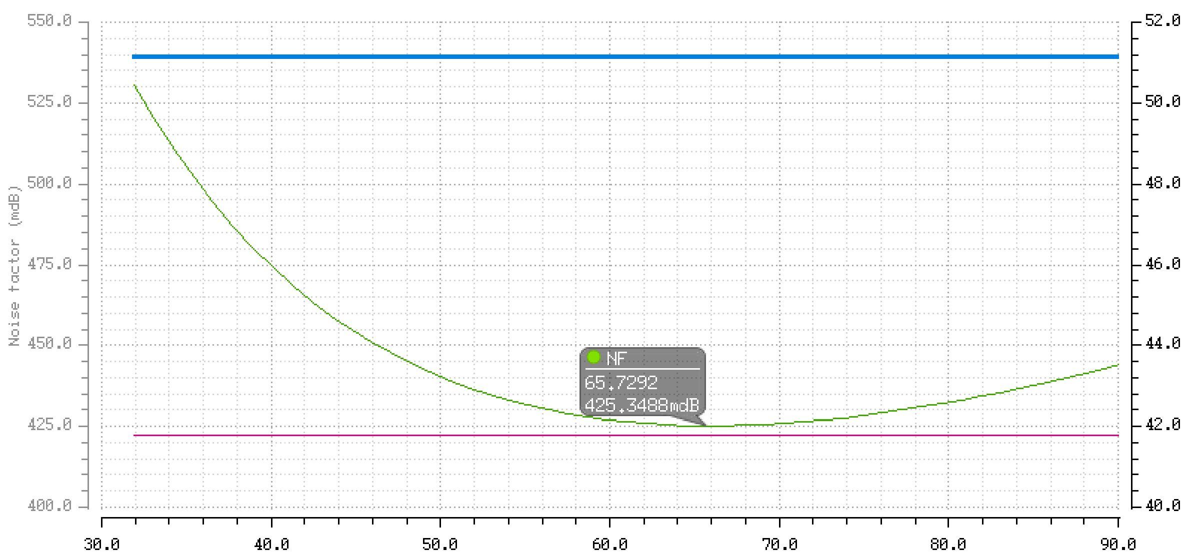


Figure 5.10. Simulation of R_{sopt} and X_{sopt} (m = 14).

5.2.3 Determination of the emitter and base inductors

The extraction of the small-signal model parameters of the input transistor at the optimum bias conditions (V_B = 0.7705 V, V_{DC} = 2.2 V) is required for the calculation of L_B and L_E, as L_E is related to f_T and L_B is related to L_E and C_{be}.

A single transistor configuration is required to extract the value of r_b, r_e, C_{be} and C_{bc}. It is noted that, when the emitter length of a single transistor increases from 2.5 µm to 18 µm, the NF_{min} increases only slightly, from 0.3 dB to 0.307 dB, the simulation being done with Cadence ADE-L. For a supply voltage of 1.2 V, NF_{min} is achieved at $V_B = 0.763$ V. The Z- and Y-parameters are simulated at 1.4 GHz in order to extract C_{be}, C_{bc}, r_{bi}, r_e and g_m.

At the V_B bias voltage of 0.763 V, $I_C = 338$ µA and at 1.4 GHz, the minimum achievable NF, NF_{min}, is 0.307 dB, as shown in Figure 5.11.

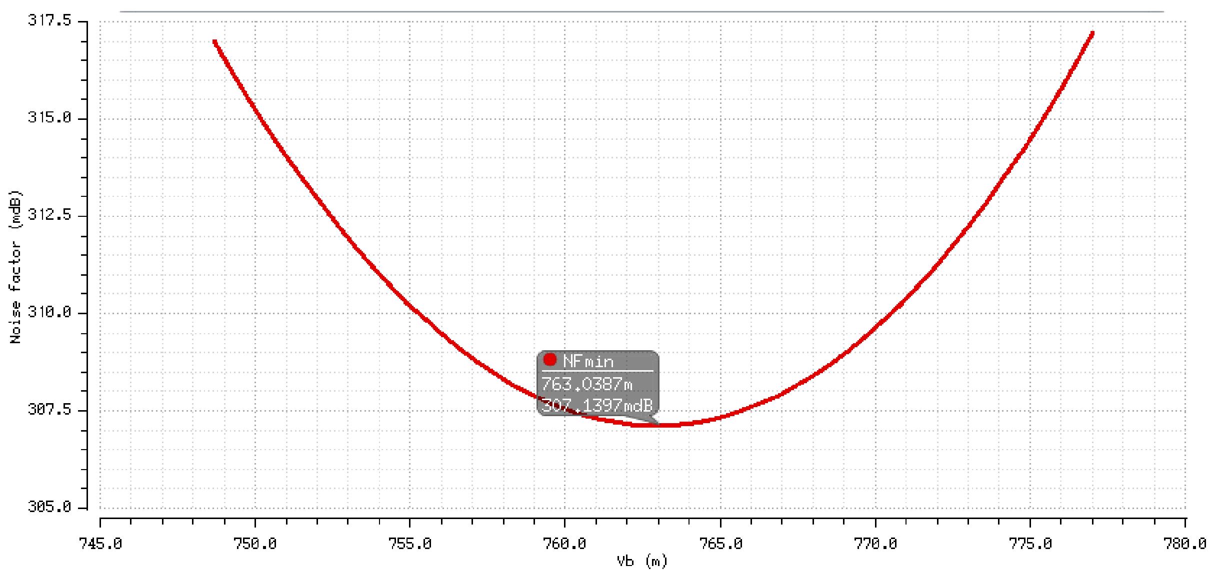


Figure 5.11. NF of a single transistor as function of V_B.

At minimum NF and at 1.4 GHz, simulated values of Z-parameters are as follows:

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} (81.698 - 3.564j) & (75.440 - 3.564j) \\ (312.41 + 4415j) & (316.77 - 25.46j) \end{bmatrix} \quad (5.1)$$

At minimum NF and at 1.4 GHz, simulated values of Y-parameters are as follows:

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} (37.46472 + 37.464j) \times 10^{-6} & (-1.54899 - 225.139j) \times 10^{-6} \\ (13189.1 - 402.349j) \times 10^{-6} & (847323 + 243.6123j) \times 10^{-6} \end{bmatrix} \quad (5.2)$$

The values of the extracted small-signal model parameters are calculated from the equations in Section 4.4.12, yielding C_{bc} = 2.56 E-14 F, C_{be} = 2.13 E-14 F, r_b = 6.258 Ω. The extraction of g_m and r_e yields values that are far away from the expected ranges (g_m = 0.000250 s, r_e = 3990 Ω), because of the approximations used in the derivation of their analytical expressions. Therefore, g_m and r_e are extracted from ADE-L (RESULTS ⇒ PRINT ⇒ DC OPERATING POINT).

The value of V_B found by simulation in the cascode configuration differs from the case of a single transistor. The parameters of the input transistor are found by measuring Z- and Y-parameters for V_B = 0.7705 V, the base bias voltage required for optimum NF_{min}, for the cascode configuration. The values of Z- and Y-parameters obtained by simulation for V_B = 0.7705 V, I_C = 478 μA and at 1.4 GHz are used for the determination of new values for Z- and Y-parameters.

At minimum NF and at 1.4 GHz, simulated values of Z-parameters are as follows:

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} (63.615 - 2.017j) & (57.446 - 2.07j) \\ (241.2183 + 4417j) & (246.91 - 19.26j) \end{bmatrix} \tag{5.3}$$

At minimum NF and at 1.4 GHz, simulated values of Y-parameters are as follows:

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} (47.77 + 970.426j)\times 10^{-6} & (-1.6295 - 225.353j)\times 10^{-6} \\ (16729 - 463.855j)\times 10^{-6} & (0.964157 + 249.883j)\times 10^{-6} \end{bmatrix} \tag{5.4}$$

From the equations $C_{bc} = \dfrac{1}{\omega \operatorname{Im}(Z_{22} - Z_{21})}$, $C_{be} \cong \dfrac{\operatorname{Im}(Y_{11} + Y_{12})}{\omega}$, $g_m = |Y_{21} - Y_{12}|$, $r_b = Z_{11} - Z_{12}$ and $r_e \cong \lim_{\omega \to 0}\{\operatorname{Re}(Z_{12})\} - \dfrac{1}{g_m}$, it is found that:

C_{bc} = 2.56 E-14 F, C_{be} = 8.47 E-14 F, r_b = 6.169 Ω, g_m = 0.000337, r_e = 2964.783 Ω where the values of g_m and r_e are far from their expected ranges and are not used.

Because the calculation of C_{bc} is accurate (no approximations), C_{bc} is extracted from the Z-parameters. In the calculation of C_{be}, the contributions of r_b and r_e have been neglected. However, without providing an accurate result as for C_{bc}, the expression of C_{be} allows one

to obtain an initial estimation of the value of the emitter inductor. Other parameters of the single transistor are extracted from ADE-L (RESULTS ⇒ PRINT ⇒ DC OPERATING POINT). These parameters are: β = 529.8, I_C = 548.1 µA, C_{be} = 85.07 fF, C_{bc} = 30.94 fF, r_e = 0.537, f_T = 28.84 GHz, f = 1.4 GHz. Note that the values of C_{be} and C_{bc} from SpectreRF are close to the values extracted using Z- and Y-parameters.

The graph in Figure 5.12 shows that the NF_{min} at V_B = 0.7705 V is 0.310 dB. This result validates the expression of F_{min}, $F_{\min} = 1 + \frac{n}{\beta_o} + \frac{f}{f_T}\sqrt{\frac{I_C}{2V_T}(r_b + R_e)(1 + \frac{f_T^2}{\beta_o f^2}) + \frac{n^2 f_T^2}{\beta_o f^2}}$, that provides a value of 0.317 dB.

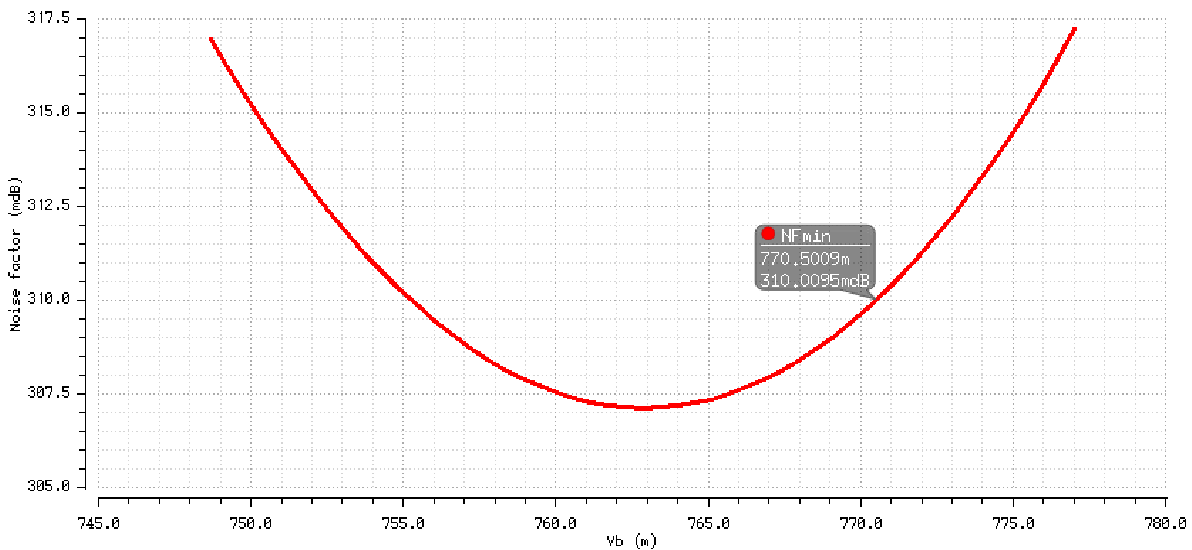


Figure 5.12. NF_{min} at V_B = 0.7705 V.

The emitter inductor L_E is derived from the equation $L_E = R_s/2\pi f_T$, which yields 0.276 nH for a multiplicity m of 1, with f_T = 28.84 GHz. For m = 14 (14 transistors in parallel), f_T = 25.49 GHz. Hence, L_E = 0.312 nH. At the bias base voltage for which noise matching is achieved, the second term of (4.5) is nil and the NF is equal to NF_{min} as shown in Figure 5.13. Matching is achieved for L_B = 5 nH and L_E = 0.312 nH. The operating frequency is 1.4 GHz and the bias voltage V_B is 0.7705 V.

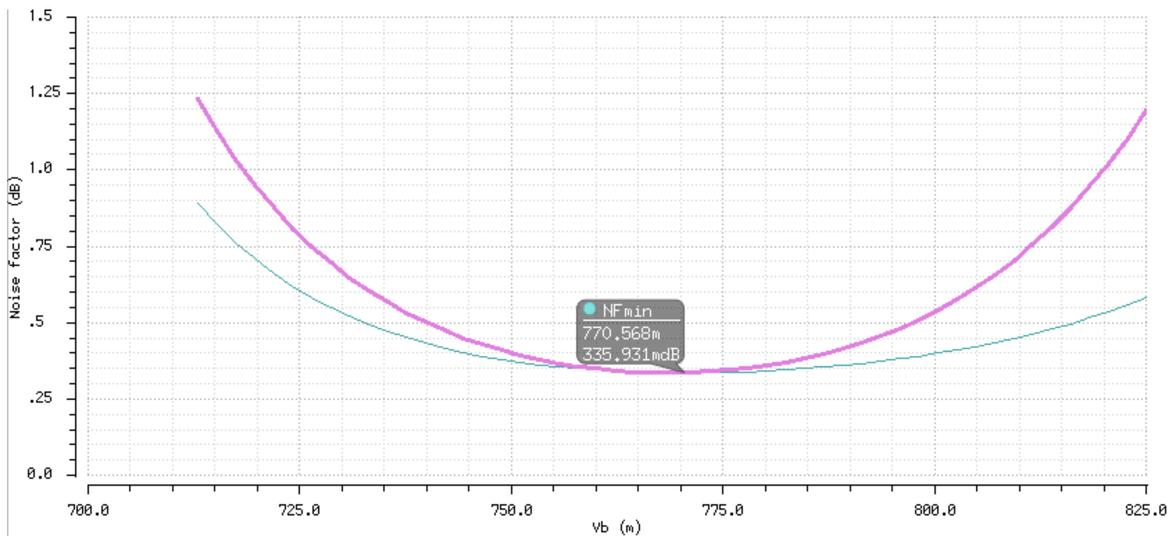


Figure 5.13. NF and NF_{min} at optimum noise matching.

A sweep of the source resistance R_s at the operating frequency of 1.4 GHz shows in Figure 5.14 that the minimum NF is obtained when R_s = 52.4 Ω. The red line is the plot of NF_{min}.

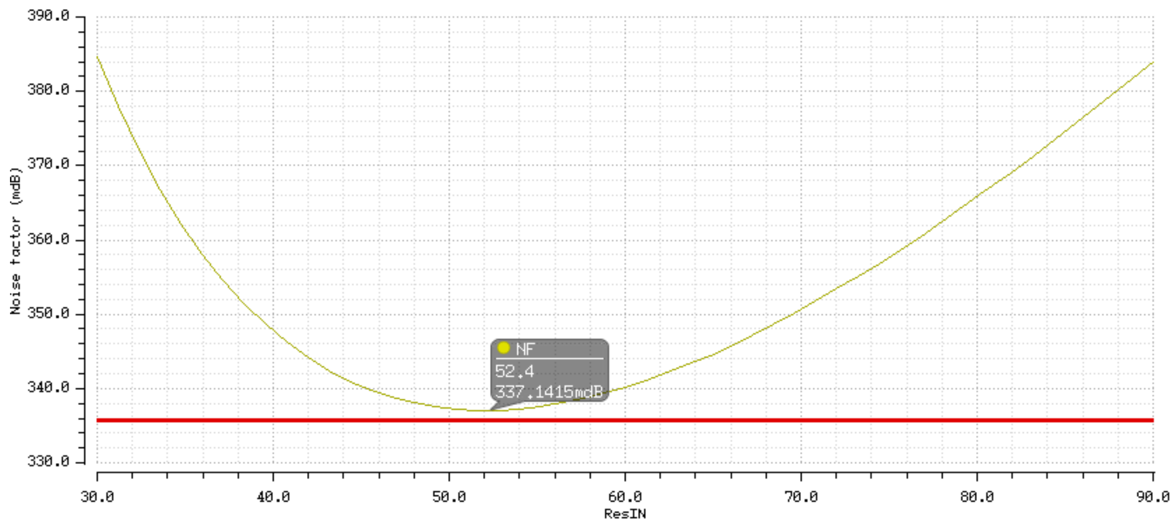


Figure 5.14. NF and NF_{min} versus R_s.

The plot in Figure 5.14 shows that the NF can be improved. This is done by tuning the value of L_B. Improved matching is shown in Figure 5.15, for L_B = 4.5 nH and L_E = 332 pH.

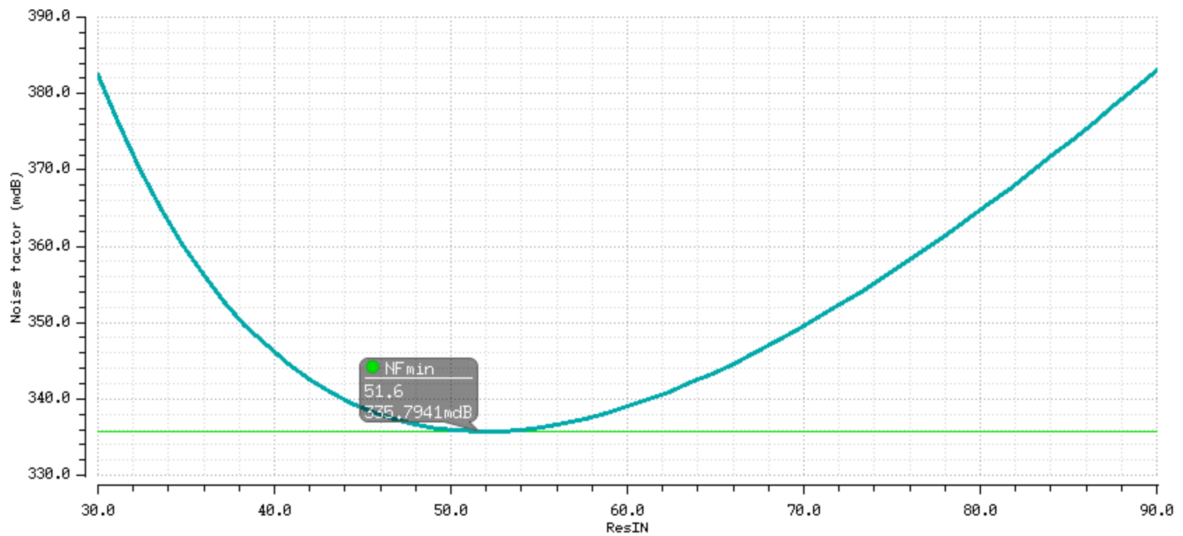


Figure 5.15. Improved NF matching.

The dependence of the NF and NF_{min} with frequency is shown in Figure 5.16 where NF_{min} is plotted in red. It is noted that the NF and NF_{min} are equal at 1.4 GHz.

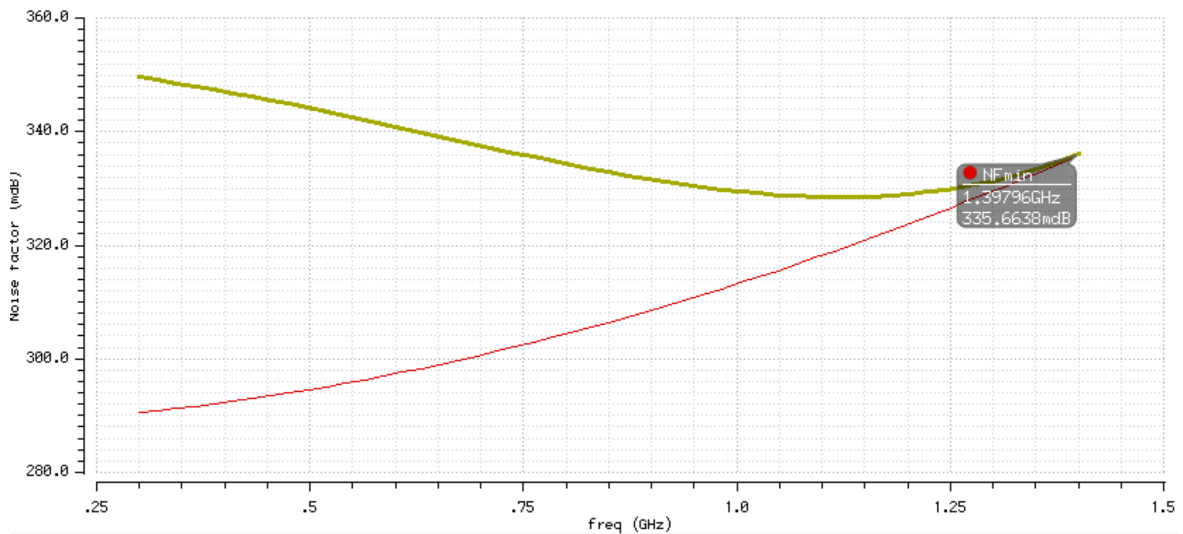


Figure 5.16. Dependence of NF and NF_{min} with frequency.

5.2.4 Improvement of power matching

The value of L_E was derived from R_s and from f_T. This value can be validated and adjusted by simulation of S_{11} as a function of the bias voltage or the operating frequency. The value of L_E for which S_{11} is the minimum results from a simulation of S_{11}, the sweep variable

being the frequency and the value of L_E a variable parameter, as shown in Figure 5.17. It is noted that the minimum value of S_{11} is achieved at 1.89 GHz, which is outside of the bandwidth of interest.

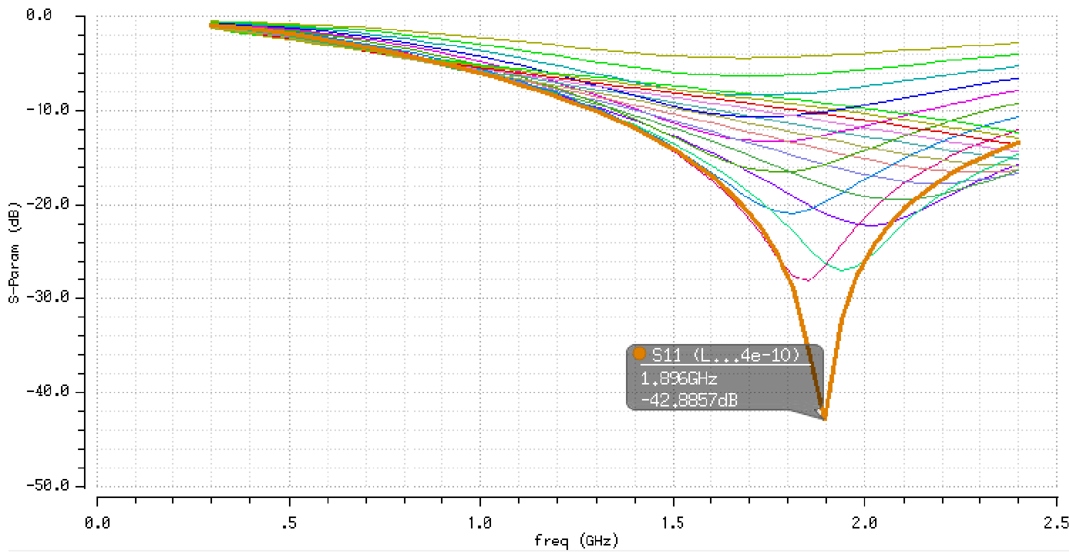


Figure 5.17. S_{11} versus frequency.

The minimum value of S_{11} is -42.9 dB and is obtained for L_E = 0.47894 nF. After the change of the value of L_E, a new simulation is done for R_{sopt} and NF. It shows, in Figure 5.18, that R_{sopt} = 52.2 Ω at 1.4 GHz. The NF is 0.336 dB at 1.4 GHz and near flat in the bandwidth.

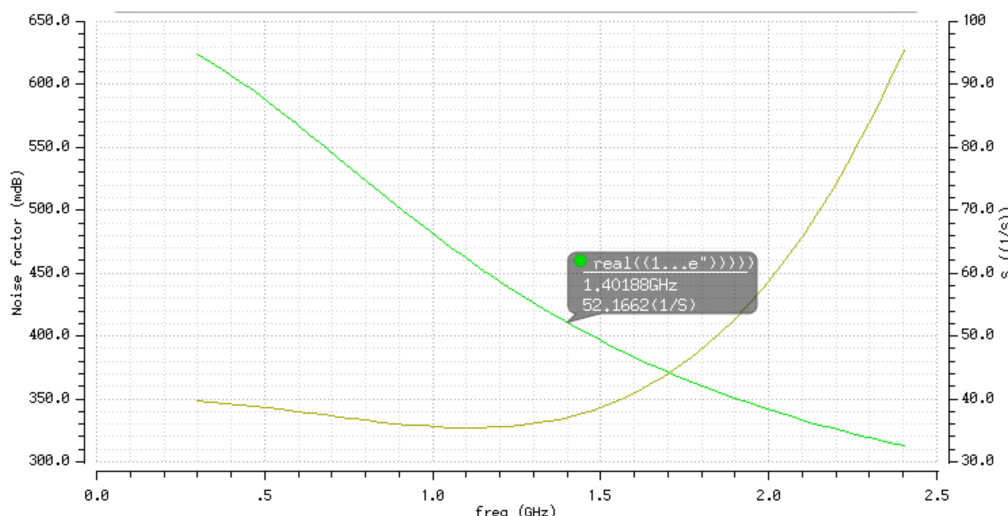


Figure 5.18. R_{sopt} and NF versus frequency.

5.2.5 Bandwidth extension

It is shown in Section 4.7 that the bandwidth of the LNA can be extended by the addition of a capacitor C_L between the input and the cascode transistors. Simulation shows that f_2 is 89.8 MHz, for which C_L is 3.867 pF, corresponding to a value of –24.5 dB for S_{11}. The resonant frequency f_1 of the second tuned circuit is 1.845 GHz, which is weakly related to C_L. The value of S_{11} is strongly related to C_L. The value of C_L is determined by simulation and the value C_{Lopt} corresponding to a near-flat response of S_{11} in the frequency band of the amplifier is 7.196 pF. For a value of C_L of 7.196 pF, S_{11} is less than -10 dB in a wide input bandwidth of the LNA, from 300 MHz to 1.4 GHz. For very high values of C_L compared to C_{Lopt}, S_{11} tends to its minimum value shown in Figure 5.17, and the frequency f_1 is almost invariant. The plot of S_{11} as a function of frequency and of C_L obtained by parametric simulation of S_{11} is represented in Figure 5.19. The capacitance C_L is swept from 0.538 pF to 30.499 pF in 10 steps.

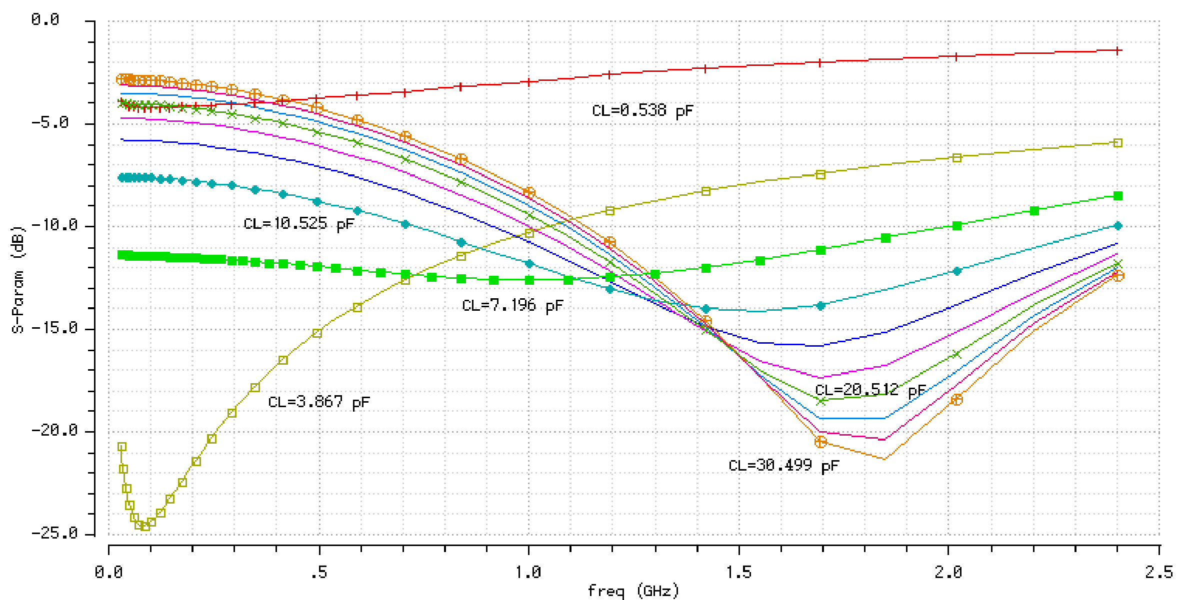


Figure 5.19. Determination of C_L by simulation of S_{11} versus frequency.

The plot of the NF shows in Figure 5.20 that the effect of C_L on the NF is very small and that the NF varies slightly in the LNA bandwidth. At 1.4 GHz, the NF decreases by about 0.002 dB. However, for low values of C_L, the NF increases significantly.

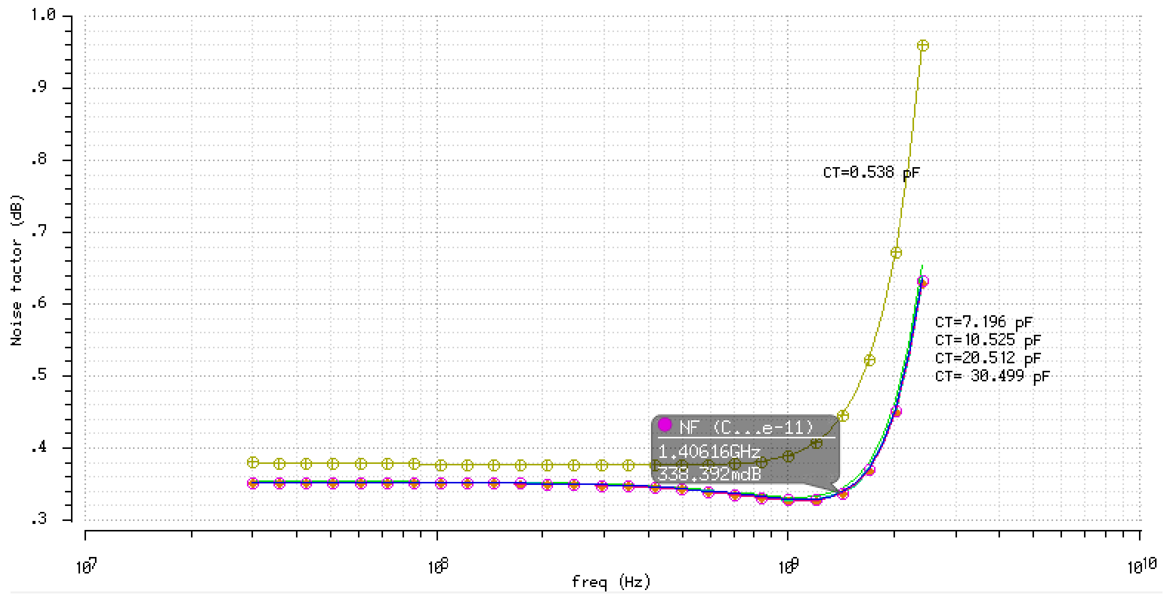


Figure 5.20. NF versus frequency and C_L.

5.2.6 Output matching network

The matching network was first designed using a graphical methodology based on the Smith chart and was proposed by Richard Chi-Hsi Li in 2005 [58]. The topology of the network resulting from this preliminary design is a fourth-order pass-band filter shown in Figure 5.21, where a shunt resistor will be added at the input in order to ensure that the trace of the reflection coefficient can move in circles of constant resistance on the Z and Y circles of the Smith chart.

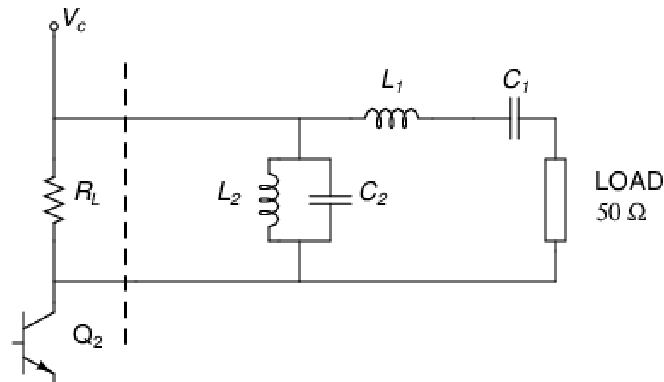


Figure 5.21. Fourth-order pass-band filter.

The LC network in Figure 5.21 is a band-pass filter, possibly of the Butterworth or Chebyshev type, depending on the values of its components. This network can be derived from a low-pass to a band-pass transformation of the second-order Butterworth or Chebyshev ladder network formed by a shunt capacitor and a series inductor shown in Figure 5.22. This transformation converts an inductor in a series LC circuit and a capacitor in a parallel LC circuit. The roll-off rate of the low-pass is 40 dB/decade, which becomes 80 dB/decade after the transformation.

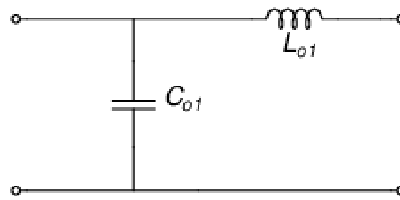


Figure 5.22. Second-Order low-pass filter.

The normalised values of the Butterworth low-pass filter, for an input resistance and output load resistances of 1 Ω, are C_{o1} = 1.41421 and L_{o1} = 1.41421 [134]. The classical low-pass to band-pass transformation is applied to the network in Figure 5.22 and the shunt capacitor C_{o1} is transformed into the capacitor C_2 in parallel with the inductor L_2. Similarly, L_{o1} is transformed into the capacitor C_1 in series with the inductor L_1 [135]. The relationships between C_{o1}, L_{o1}, C_1, L_1, C_2 and L_2 are given by the equations:

$$C_2 = \frac{C_{o1}}{B} \tag{5.5}$$

$$L_2 = \frac{B}{\omega_o^2 C_{o1}} \tag{5.6}$$

$$L_1 = \frac{L_{o1}}{B} \tag{5.7}$$

$$C_1 = \frac{B}{\omega_o^2 L_{o1}} \tag{5.8}$$

where B is the bandwidth of the filter in radians and ω_o is the geometric mean of $2\pi\omega f_1$ and $2\pi\omega f_2$, the low and high frequencies cut-off angular frequencies of the band-pass filter.

The normalisation of the band-pass filter is still not completed, source and output impedance being still equal to unity. The final values of the reactive components of the filter are obtained from the expressions:

$$C_2 = \frac{C_{o1}}{B} k \quad (5.9)$$

$$L_2 = \frac{B}{\omega_o^2 C_{o1} k} \quad (5.10)$$

$$L_1 = \frac{L_{o1}}{B} k \quad (5.11)$$

$$C_1 = \frac{B}{\omega_o^2 L_{o1} k} \quad (5.12)$$

where k is by definition a real value equal to the resistance of the source (50 Ω).

Because k is real and the output impedance of the LNA is of type $R_L - j/\omega C_{out}$ and the load is resistive, the equations above cannot be used to denormalise the filter. However, the filter being a reciprocal two-port network, matching can be performed by reversing the direction of the signal: the load is replaced by a 50 Ω source and the source is replaced by a complex load whose impedance is equal to the output impedance of the common-base transistor at the output of the LNA. For this analysis, the matching network is represented in Figure 5.23, where the reflection plane is between the network and the resistive load.

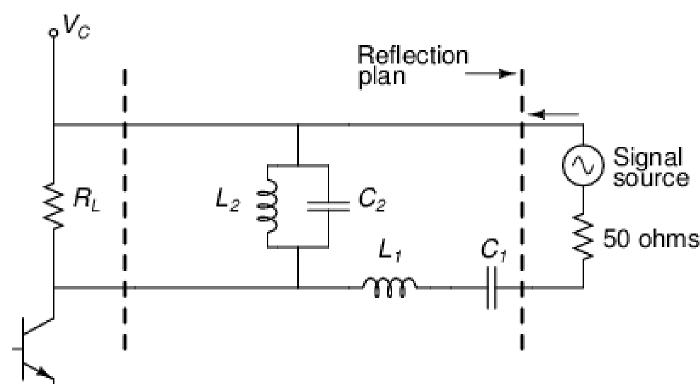


Figure 5.23. Reflection plan of the matching network.

The values of passive components obtained from (5.9), (5.10), (5.11) and (5.12) correspond to a pass-band filter with input and output impedances of 50 Ω. These values

are to be changed to maximise power transfer from the resistive source to the reactive load. Such modifications are necessary, as impedances at both ends of the filter are not resistive and not equal. For normalised filters, as for frequency conversion, it is assumed that input and output impedances are real and equal to unity.

The technique proposed for the optimisation of the transfer of power is referred to as the grid approach to broadband impedance matching. This approach recognises that the broadband matching problem constitutes minimising power loss between a source and a load, providing better results – simplicity, reliability and optimal results – in contrast, the classical method utilises complex polynomial functions. The strength of the technique is its simplicity, reliability and in the attainment of an optimal solution; the technique is superior to the real-time technique [136]. The approach maximises the transfer of power between a source and a load by analysing the impedance data at discrete frequencies. The impact of all components to the power transfer being analysed, an optimised solution is found using an "objective function" as shown in the MATLAB™ script in Addendum G.

It is noted that the change of the values of the elements of the matching network will affect the frequency response of the filter from which the broadband matching network is derived, and the result may not correspond to the classical definition of a pass-band Butterworth filter anymore. This impact can be limited by reducing the number of components to be analysed; in the case of this work, only the inductive elements at the ports of the matching network are analysed.

In the frequency transformation technique used in band-pass filter design, the angular frequency ω_o is a geometric mean, which is justified because in filter design, the frequencies of interest fall in the 3 dB bandwidth [137]. Since this requirement is not applicable in impedance matching, ω_o is rather the arithmetic mean calculated from f_1 and f_2 in order to achieve minimum reflection at the centre of the bandwidth. Furthermore, in order to guarantee that S_{22} < -10 dB, the bandwidth is increased by 50%, as 3 dB power loss at the edges of the bandwidth is not acceptable.

5.2.7 Determination of the cascode output impedance

The output impedance is calculated from the readings of reflection coefficients from a Smith chart simulation. The open-circuit output impedance Z_{22} can be derived from S-parameters using the relation:

$$Z_{22} = R_o \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \tag{5.13}$$

Assuming that the isolation between the output and the input is complete, the assumption that is justified for the cascode configuration, $S_{12} = 0$, Z_{22} and Z_{out} can then be evaluated by the expression:

$$Z_{out} = Z_{22} = R_o \frac{1 + S_{22}}{1 - S_{22}} \tag{5.14}$$

where $R_o = 50\ \Omega$.

The simulation result of S_{22} by SpectreRF at the output of the cascode transistor, in parallel with a 2 mH inductor, is shown at 30 MHz in Figure 5.24.

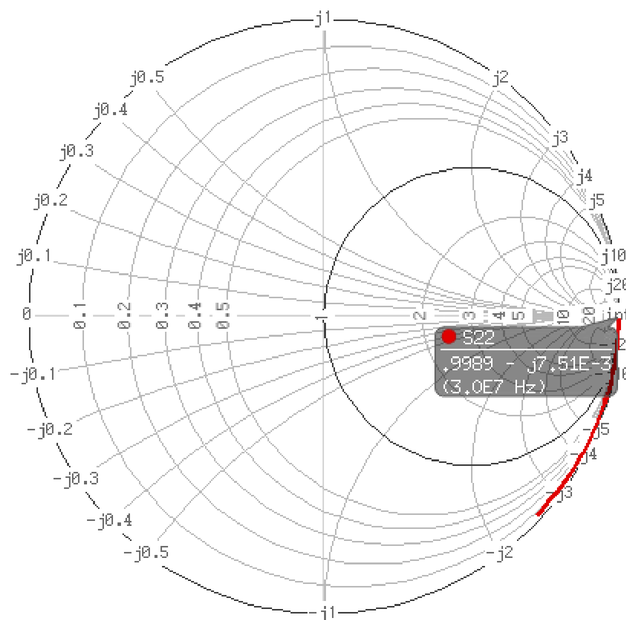


Figure 5.24. S_{22} at the output of the cascode at 30 MHz.

The output impedance at 30 MHz is equal to:

$$Z_{out} = 1.8994e{+}03 - 1.3024e{+}04i \tag{5.15}$$

The simulation of S_{22} by SpectreRF at the output of the cascode transistor, in parallel with a 2 mH inductor, is shown at 2.07559 GHz in Figure 5.25.

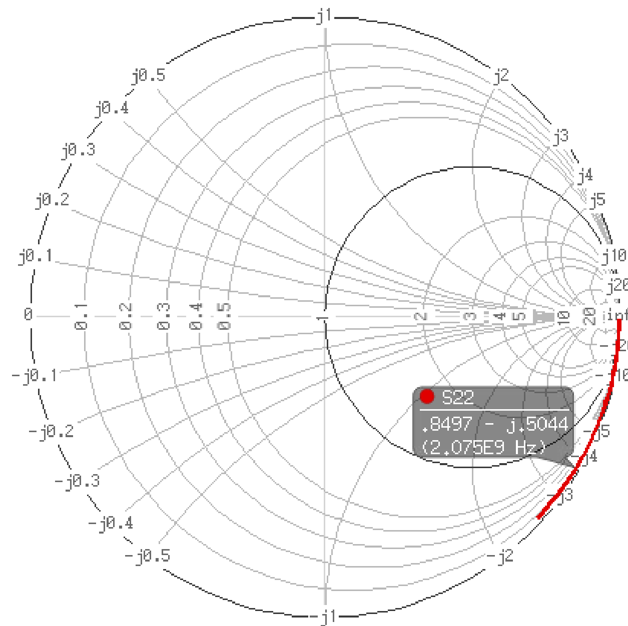


Figure 5.25. S_{22} at the output of the cascode at 2.07559 GHz.

The output impedance at 2.07559 GHz is given by:

$$Z_{out} = 4.2564e{+}00 - 1.8209e{+}02i \tag{5.16}$$

The Smith chart in Figure 5.24 shows that the imaginary part of Z_{out} is negative and decreases when the frequency increases. Therefore, Z_{out} is formed by a capacitor C_{out} in parallel with an inductor L_{out}. The expression of the imaginary part of Z_{out} is given by the equation:

$$\operatorname{Im}\{Z_{out}\} = \frac{j\omega}{1 - \dfrac{\omega^2}{\omega_o^2}} \tag{5.17}$$

$$\text{with } \omega_o^2 = \frac{1}{C_{out} L_{out}} \tag{5.18}$$

Equations (5.17) and (5.18) can be solved at 30 MHz and at 2.07559 GHz, resulting in C_{out} = 0.42 pF and L_{out} = 2.04 mH. The gain of the LNA is determined by $R_L = R_{out}$, represented in Figure 5.23. It has been indicated in previous sections that R_L is also required in order to be able to have an S_{22} response that can be brought closer to the centre

of the Smith chart. However, R_L increases the NF and it is desired to have R_L high, as its thermal noise current is inversely proportional to its square root. A parametric simulation of the NF of the LNA, as function of frequency and of R_L, is represented in Figure 5.26.

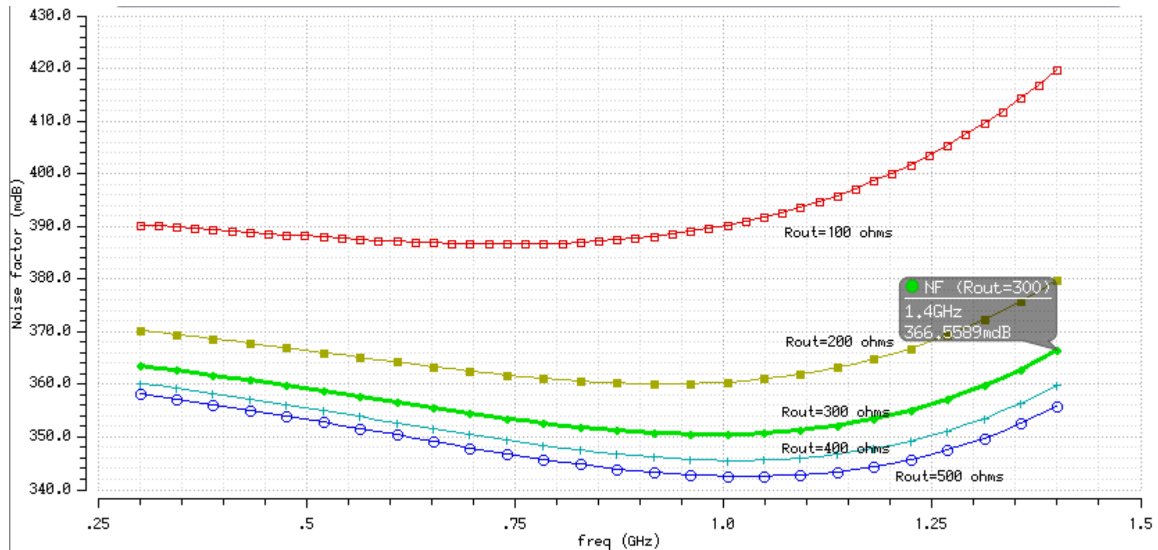


Figure 5.26. NF as function of frequency and R_L.

Preferably, the value of R_L should not affect the NF significantly. Simulation results show that the NF increases from 0.337 dB to 0.367 dB for R_{out} = 300 Ω. For values of R_{out} that are lower than 300 Ω (e.g. 200 Ω or 100 Ω), the NF increases significantly. Therefore, the impact on NF is small for R_{out} = 300 Ω. However, simulation shows that S_{22} > -10 dB for R_{out} = 300 Ω. In order to achieve S_{22} < -10 dB in the bandwidth from 300 MHz to 1.4 GHz, a value of 90 Ω for R_{out} is selected.

5.2.8 Simulation results of the matching network

The values of C_{out} and R_{out} are used as input for the MATLAB™ script. The optimisation is performed from 300 MHz to 1850 MHz. After optimisation, the values of the matching network calculated by the script are: L_1 = 8.710 nH, C_1 = 3.0189 pF, L_2 = 8.5106 nH, C_2 = 2.9042 pF. The parameter S_{22} is represented, before and after optimisation, in Figure 5.27.

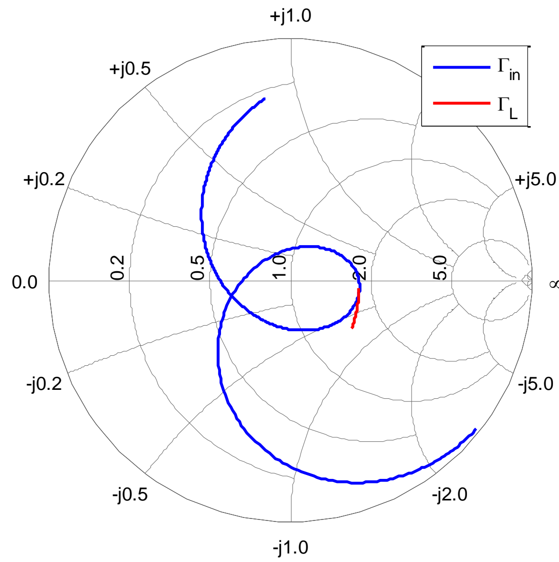


Figure 5.27. S_{22} before (red) and after (blue) optimisation.

The impact of the matching network on the transmission of RF power between the cascode LNA and the load, as a function of the operating frequency, is shown in Figure 5.28.

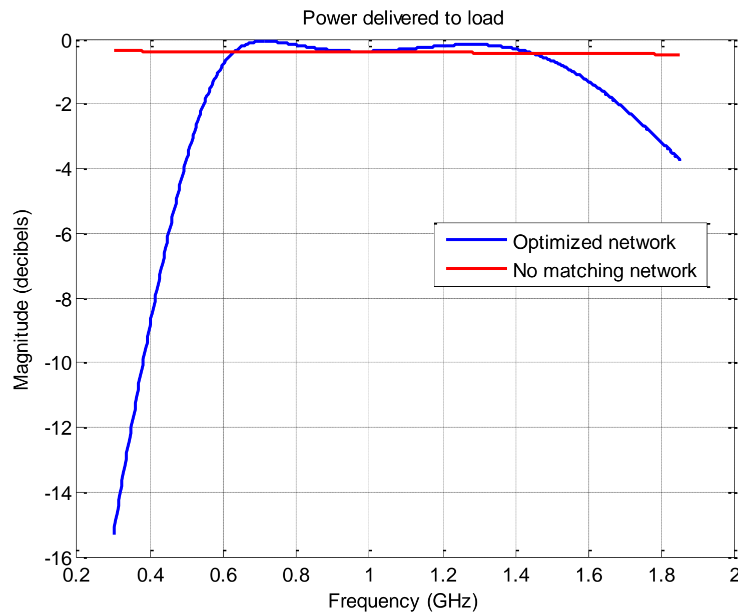


Figure 5.28. Power transfer to the load before and after matching.

Results from MATLAB™ are further optimised using SpectreRF by parametric simulation. It is found that the response is optimum for the values: L_1 = 8.710 nH, C_1 = 3.3684 pF, L_2 = 8.5106 nH, C_2 = 2.9042 pF. The graph in Figure 5.29 shows that S_{22} varies from – 15 dB at 700 MHz to – 10.4 dB at 1.4 GHz. At 940 MHz, the value of S_{22} is –11 dB.

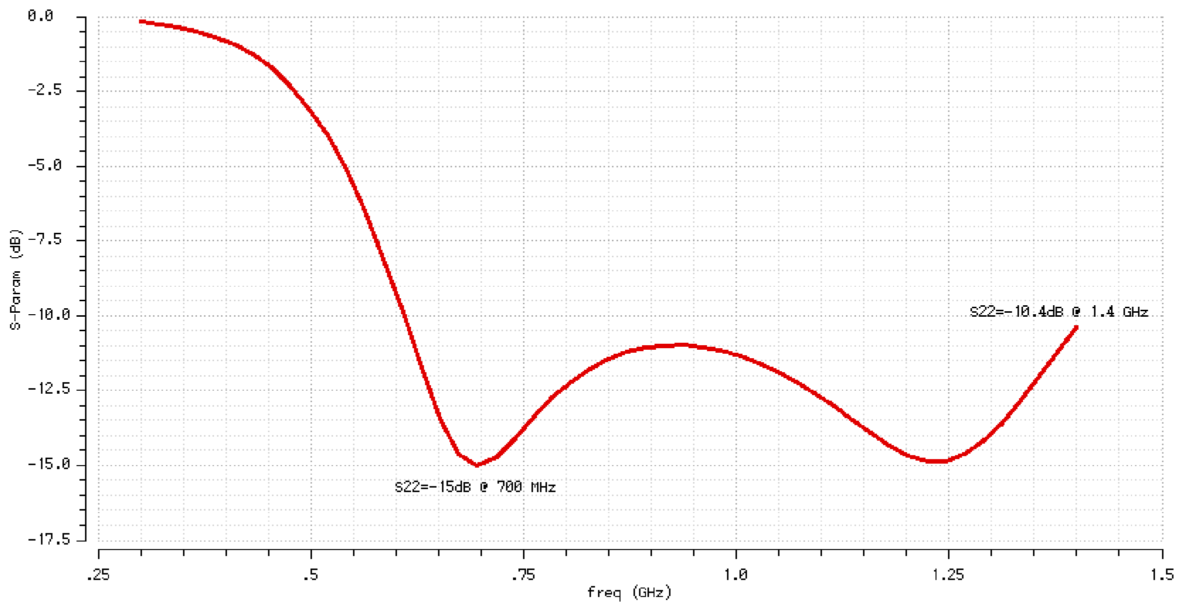


Figure 5.29. Simulation of S_{22} by SpectreRF.

5.2.9 Optimisation of the LNA

It is desired to improve the bandwidth, the NF and the power gain G_A of the LNA. As indicated previously, the NF is impaired by the resistor R_L. For R_L > 90 Ω, the NF decreases but S_{22} and G_A increase. Although a higher gain is desired, the increase in S_{22} reduces the bandwidth of the LNA. It has been found that the noise generated by some FET used as active resistor is lower that the thermal noise from a resistor of the same value. It is then considered to replace R_L by an active resistor.

To increase G_A, an additional amplification stage can be considered. It is shown in [59] that a wideband resistive output impedance can be achieved by the CC amplifier when the output impedance of the preceding stage is ohmic-capacitive and its cut-off frequency is equal to the cut-off frequency of the CC transistor. In this way, the transistor can be used

for power amplification and for output matching. However, the output impedance of the CC circuit is extremely low compared to 50 Ω, while its input impedance is very high, resulting in a high ratio of impedance transformation. Such a transformation can be done for low frequencies (e.g. below 60 MHz), but for high frequencies, the impedance transformation network will incur high losses due to the high ratio of impedance transformation.

Simulation with an 18 μm (emitter length) SiGe HBT shows that the output impedance ($1/g_m$) is in the range of 2 Ω. Although a high gain has been achieved (~35 dB) with moderate increase of the NF (0.400 dB from 0.366 dB), the output impedance is resistive but extremely low and requires an additional matching network at the output. Finally, the use of the CC circuit in LNA design is undesirable owing to its drawbacks and high noise.

A performance improvement may be expected in replacing R_L by a FET, used as a "cold resistor". It is found by simulation that, for W = 14 μm and L = 120 nm, S_{22} improves from 10.8 dB to 11.5 dB and NF_{min} from 0.429 dB to 0.428 dB at 1.4 GHz. This change is insignificant and indicates that the MOS transistor does not have a "cold resistor" response. Simulation results show that the NF of the LNA is unchanged when the load resistor R_L is replaced by a CMOS transistor, as per [138]. It is shown in [139] that a FET used as resistor may generate less total noise than the thermal noise of a resistor of equivalent value. This is achieved when $R_n/R_{in} < 1$, where R_n is the noise resistance of the FET and R_{in} is the real part of its input impedance when the drain AC output signal is fed back to the gate. Simulations done with MOS devices from the IBM BiCMOS8HP process show that R_n is much higher than R_{in}, except when the transistor is in the cut-off region corresponding to subthreshold conduction. The use of a FET as a "cold active resistor" seems rather to be applicable to GaAs devices.

5.2.10 The base inductor

The base inductor has a critical impact on the noise performance of the LNA. Simulation indicates that the NF increases by 0.2 dB when the 4.5 nH base ideal inductor is replaced

by an inductor of the same value from the design kit. The increase is due to conduction and dielectric losses. Conduction losses are due to conductor strips and can be derived relatively more easily than dielectric losses that are more complicated to estimate. Dielectric magnetic and electric substrate losses are mainly due to the low resistivity of Si, from 0.1 to 100 Ω.cm and they increase with frequency. The device used from the design kit is of the indp type, a spiral inductor with M1 ground and two parallel strips to reduce the series resistance. The highest quality factor for indp inductors is 20. If dielectric losses are neglected at the operating frequency a quality factor of 10 is assumed; the parasitic resistance of the inductor can be estimated by the expression $r_{Lb} = (2\pi f L_b)/Q_{Lb}$, which is equal to 3.96 Ω.

The value of the base inductor can decrease if a capacitor C_{BE} is added between the base and emitter at the input. However, such an arrangement increases C_{be} in (4.93) which in turn decreases in turn f_T. The decrease in f_T increases F_{min} which impairs the NF. Another alternative may be an additional capacitor C_B, in parallel with the base inductor L_B. Although this arrangement decreases the value of L_B and the resulting reactance remains equal to 4.5 nH at 1.4 GHz, simulation shows that the NF increases.

The proposed solution is to use an external high Q inductor. The impact of the bondwire must therefore be considered. An attractive feature of the IDCE configuration is the possibility to use package parasitics as circuit elements. Hence, they can be included in the design, which requires the modelling of bondpads, bondwires and the package. The typical length and diameter of bondwires are 100 µm and 25 µm. The inductance of a bondwire is given by the expression $L = 0.2\ln(2h/r)$, where L is the inductance in nanohenries, r is the radius of the wire and h is the distance between the bondwire and the ground plane. The typical values of h and L are 1 mm and 1 nH/mm. Because of the logarithmic expression of L, the dependence of L on r is small and the approximation 1 nH/mm can be used for larger bondwires. The main disadvantage of using bondwires as circuit elements is their lack of reproducibility and predictability.

5.2.11 Choice of inductors

Two types of inductors are available in the IBM BiCMOS8HP process. The inductors use a 4 µm-thick topmost metal (AM), but different ground planes. A deep trench is used as ground plane for DT inductors. For M1 inductors, the ground plane is the metal-1 layer. This ground plane shields the spiral inductor from substrate noise.

Two chokes are used by the LNA to block AC small signals. Although a high *Q* is not generally a selection criterion for chokes, chokes with low parasitic losses are required for the LNA in order to reduce their impact on the NF. In general, selection criteria for inductors are the configuration in which the inductance is used [74], the inductance value, the self-resonant frequency and the parasitic series resistance. For a choke, inductor with a high value is desired, typically more than 1 µH. The parasitic resistance is typically between 1 Ω and 10 Ω. The impedance of inductors becomes capacitive at frequencies above the self-resonant frequency. However, for chokes the impedance may remain inductive for frequencies that are much higher than the self-resonant frequency, owing to their high skin effect, wire resistance and other parasitics. They can therefore be used for broadband applications. Typical devices are the 4310LC-132KEB (1.3 µH, 15.1 mΩ) and 4310LC-353KE (3.5 µH, 49 mΩ) from coilcraft, which can be used up to 6 GHz.

5.2.12 Choice of capacitors

In the IBM BiCMOS8HP process, three capacitor types are available: HA junction varactors, MOS varactors and MIM capacitors. The capacitance of varactors varies with voltage, which introduces nonlinearities when they are used in the signal path. Varactors also require their own biasing, separate from the bias circuit used for active devices. MIM capacitors are therefore preferred in this thesis. For MIM capacitors, the top plate is on the layer metal-5 and the bottom plate on the layer metal-6. The capacitor per unit of area is 1.0 fF/µm^2.

5.2.13 DC bias

The biasing of the LNA is key for the stabilisation of the emitter density current in view of process and temperature variations. It also affects the linearity of the LNA, as the DC operation point may vary when the input signal is large.

The DC bias voltage is 0.7705 V, corresponding to a collector current of 6.47 mA for the 14 input transistors, and a density current of 0.214 mA/μm^2. The 14 transistors at the input of the LNA form the second branch of a current mirror. The current input of the current mirror is equal to 6.47/14 = 0.462 mA. Because the voltage drop is 0.7705 V at the junction base-emitter of the current mirror transistors, the value of the collector resistance for the mirror is 1424 Ω, the supply voltage being 2.2 V. This value is fine-tuned to 1572 Ω by simulation. It is found subsequently that the minimal NF of 0.452 dB is achieved at 1250 Ω, at a collector bias current of 7.93 mA for the 14 parallel transistors.

The bias circuit is represented in Figure 5.30, where N_2 represents the 14 input transistors of the cascode. It is shown in [140], that linearity is not impaired by large input signals. It is noted that the emitter current density corresponding to F_{min} is directly related to V_T. Hence, a band-pass temperature stabilised current is not desired for the constant current source.

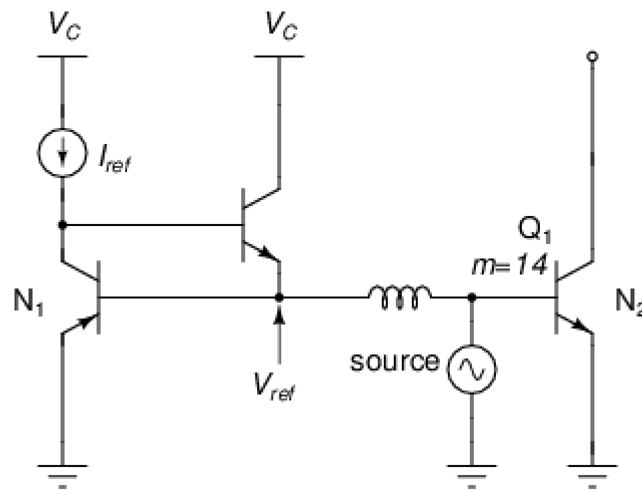


Figure 5.30. Bias circuit.

5.2.14 Improvement of the output matching

It is desired to achieve output matching from 300 MHz to 1.4 GHz. The Chebyshev approximation achieves the desired outband response and has an acceptable inband ripple, but requires inductors in the range of 30 nH, which will consume large space on the IC and impair the NF. The elliptic approximation is difficult to implement and is not considered. Acceptable results are found using a Butterworth approximation that assumes that the source resistance is very low and the resistance of the load is very high. The coefficients of the second order low-pass Butterworth approximation are replaced by 1.41422 and 0.70711 in the MATLAB™ script in Addendum G instead of 1.41421 and 1.41422. The values of the components of the matching network are L_1 = 9.5578 nH, L_2 = 23.594 nH, C_2 = 2.0462 pF, C_1 = 5.8949 pF. Simulation with MATLAB™ shows in Figure 5.31 that power losses of 0.8 dB can be attained at the edges of the desired bandwidth, at 300 MHz and 1.4 GHz.

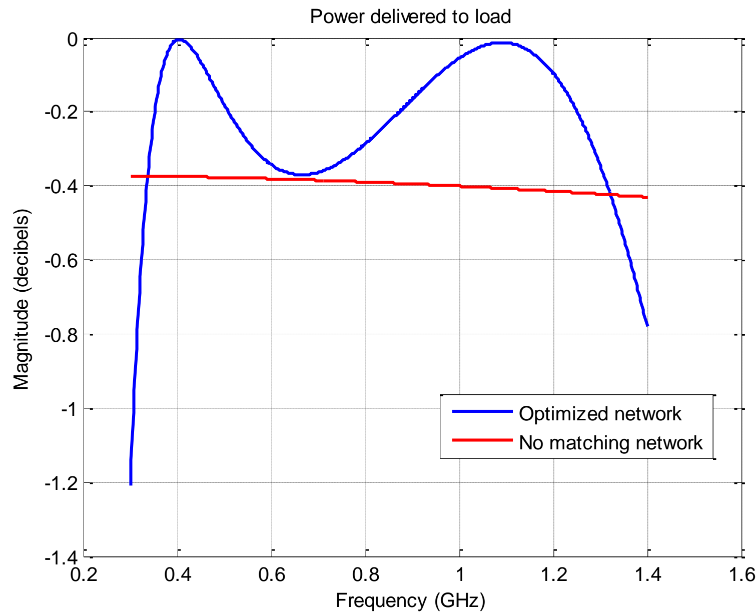


Figure 5.31. Power transfer to the load.

The graph of S_{22} with the LNA using the optimised matching network is represented in Figure 5.32.

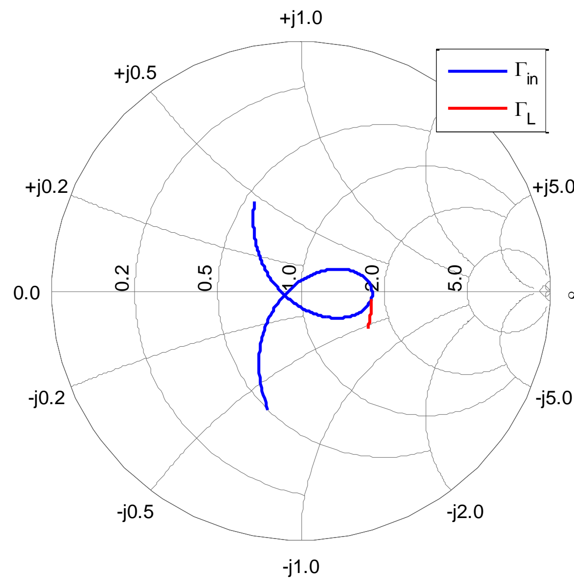


Figure 5.32. S_{22} before (red) and after (blue) optimisation.

A further optimisation of C_l is done with SpectreRF, with C_l = 8.579 pF. The simulation of the NF, of S_{11} and S_{22} by SpectreRF is shown in Figure 5.33, with an NF of less than 0.462 dB, S_{11} and S_{22} are less than -10 dB from 300 MHz to 1.4 GHz. All components are from the design process, except the base inductor L_B and the two chokes. The technology file used corresponds to eight layers of metal.

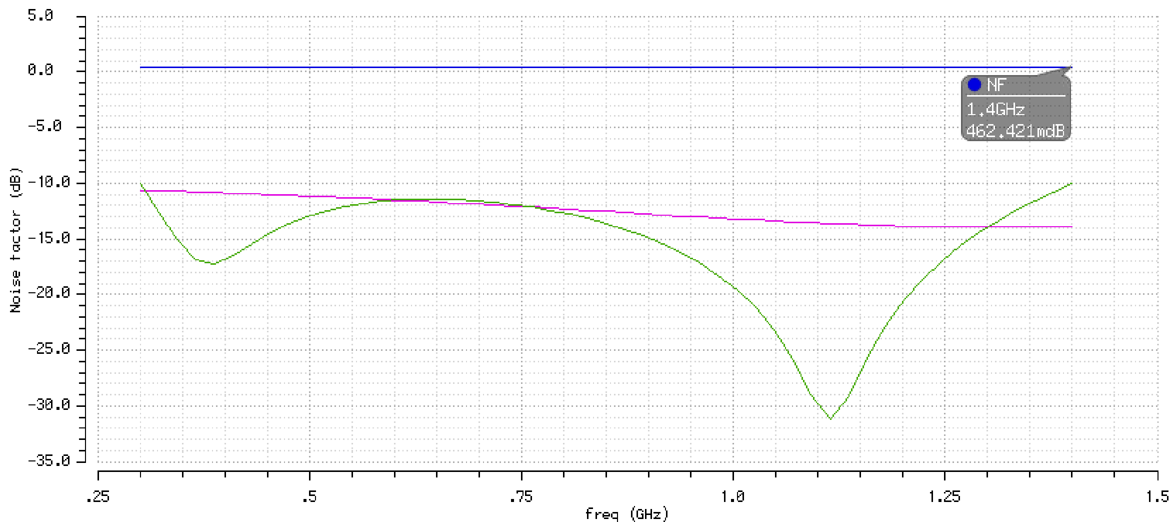


Figure 5.33. NF, S_{11} and S_{22} simulation by SpectreRF.

Fabrication constraints require seven layers of metal. Inductors in previous simulations use an eight-metal-layer technology file. They have two parallel metal lines, leading to the highest Q. These inductors are replaced by a single metal line, leading to an increase in the NF and to the impairment of the power gain of S_{22}. It is found that performance impairment is mainly due to L_E and to the tank circuit inductor. Further optimisations lead to new values for C_L, for C_l (output matching circuit) and for the bias resistor R_{bias} which becomes 1.444 KΩ (from 1.25 KΩ). The new value of C_L is 6.315 pF (from 7.197 pF) and the new value of C_l is 6.6842 pF (from 8.579 pF).

5.2.15 Stability

Stability is verified by simulation, with SpectreRF, of the Rollet conditions for unconditional stability, $k > 1$ and $|\Delta| < 1$, from (2.15) and (2.16).

It is found that the LNA is unconditionally stable in the operating frequency band. Simulation graphs of k and $|\Delta|$ are shown in Figure 5.34 and Figure 5.35.

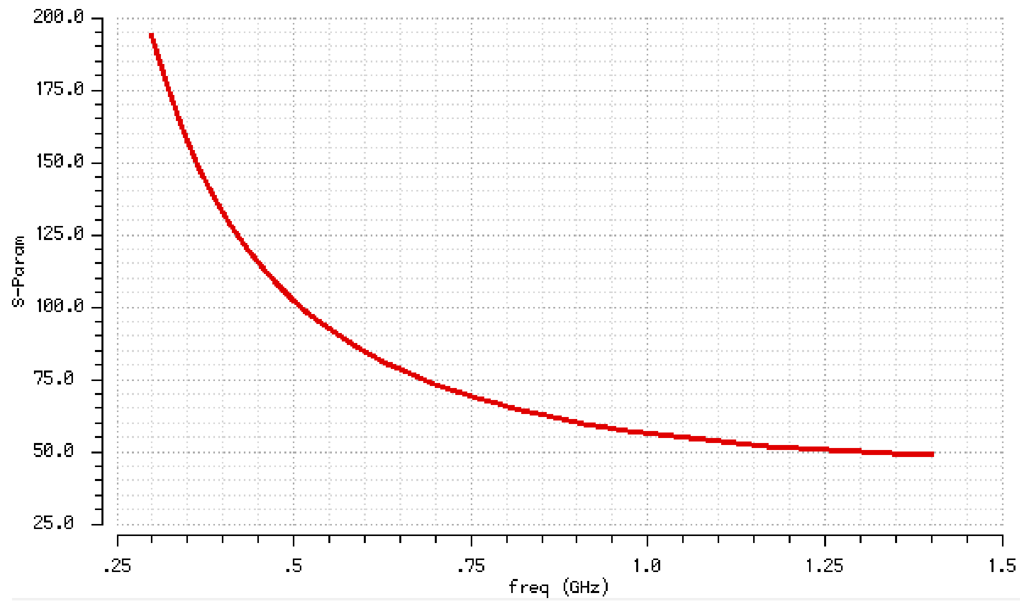


Figure 5.34. k versus operating frequency.

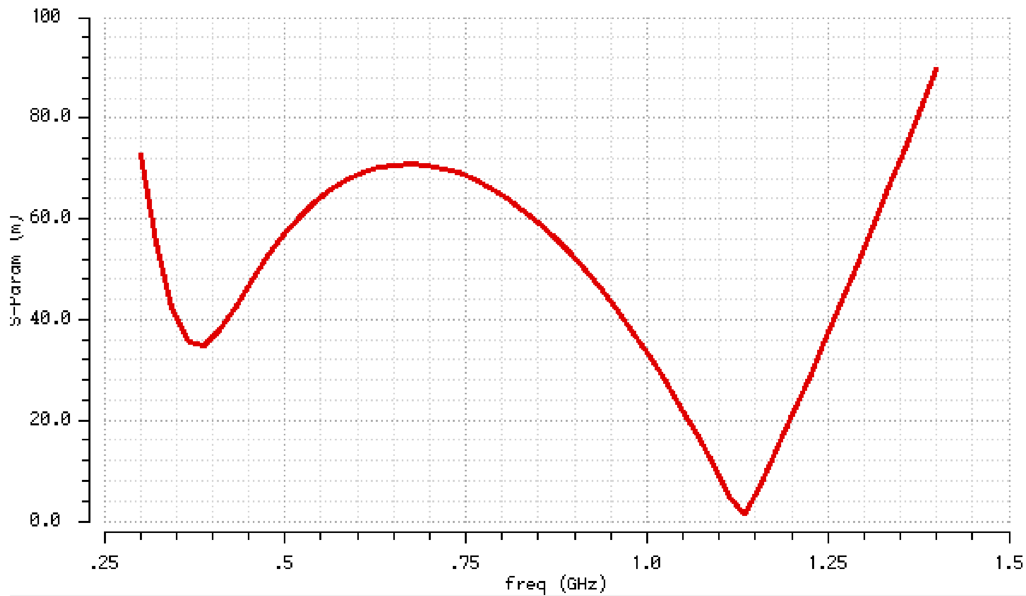


Figure 5.35. $|\Delta|$ versus operating frequency.

5.2.16 Linearity

The linearity of a receiver is not determined mainly by the LNA, but rather by subsequent stages. The LNA is still required to amplify the input signal with minimal distortion for reasons detailed in this section. This is generally achieved in the case of expected signals, signals for which the LNA has been designed. In the case of broadband LNAs, large unexpected signals are likely to be received and to cause various adverse effects. These effects are due to non-linearities in the response of LNA. The non-linearities may result in gain compression, in phase distortion, in non-desired frequencies in the output signal due to harmonic distortion and to intermodulation, and in desensitisation. Desensitisation, also known as blocking, occurs when a strong interfering signal overshadows the desired signal. The power of such a strong signal spreads across the LNA bandwidth owing to third-order intermodulations, increasing the noise floor.

In narrow-band receivers, filtering can reduce harmonic and intermodulation distortion not falling in the input signal bandwidth. For broadband receivers and especially for UWB receivers, harmonic distortion and various orders of intermodulation distortion may fall in the bandwidth of the receiver. For such systems, desensitisation can be improved by dividing the bandwidth in sub-channels, each sub-channel having its own dedicated LNA.

The measure of linearity is generally based on the IIP3 owing to its importance in narrowband receivers. Hence, the relevance of the use of the IIP3, as the main merit factor for linearity, is questionable for UWB systems. The response of the LNA can be modeled by a truncated power series transformation relating the output signal *y(t)* to the input signal *x(t).* The output signal is given by the expression [126]:

$$y(t) \approx c_0 + c_1 x(t) + c_2 x^2(t) + c_3 x^3(t) + \ldots c_n x^n(t) \tag{5.19}$$

where c_n are the Taylor coefficients of the transfer function *y(t)* at the operating point X_0; the Taylor coefficients c_n can be neglected for $n > 3$.

Assuming that the input signal is $A_1 \cos \omega_1 t$ and that the interfering signal is $A_2 \cos \omega_2 t$, the expression of IIP3 components, which are cubic terms in $\cos(2\omega_1 - \omega_2)t$ and $\cos(\omega_1 - 2\omega_2)t$, shows that their amplitude is directly related to c_3. It can be shown that n^{th} harmonics are derived from n^{th}-order terms, hence second harmonics are proportional to c_2 and third harmonics are proportional to c_3.

The response of the LNA $y(t)$ also has quadratic terms in $\cos(\omega_1 + \omega_2)t$ and $\cos(\omega_1 - \omega_2)t$. Furthermore, cubic terms in $\cos(2\omega_1 + \omega_2)t$ and in $\cos(\omega_1 + 2\omega_2)t$ exist and are proportional to c_3. Both quadratic and cubic terms may fall in the bandwidth of the UWB receiver [126]. The third-order intercept point A_{IIP3} is given by the expression:

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{c_1}{c_3}\right|} \tag{5.20}$$

It can be shown that distortions due to blocking, cross-modulation, cubic terms (including IIP3) and third harmonics are all directly related to c_3 [126]; only second-order harmonics and quadratic terms are not related to c_3. Therefore, these distortions decrease with c_3 and IIP3 can still be used as a measure of the linearity of a UWB receiver [141].

Two tones of equal amplitude and of close frequencies f_1 and f_2, with a frequency spacing of 2 MHz are used to extrapolate the IIP3 by SpectreRF. SpectreRF offers various methods to determine IIP3. The method used is based on PSS and PAC analysis owing to its efficiency, compared to other methods based on QPSS and PSS analysis.

The plots of the 1 dB compression and IIP3 points at the low end, middle and top of the bandwidth are shown in Figure 5.36, Figure 5.37 and Figure 5.38.

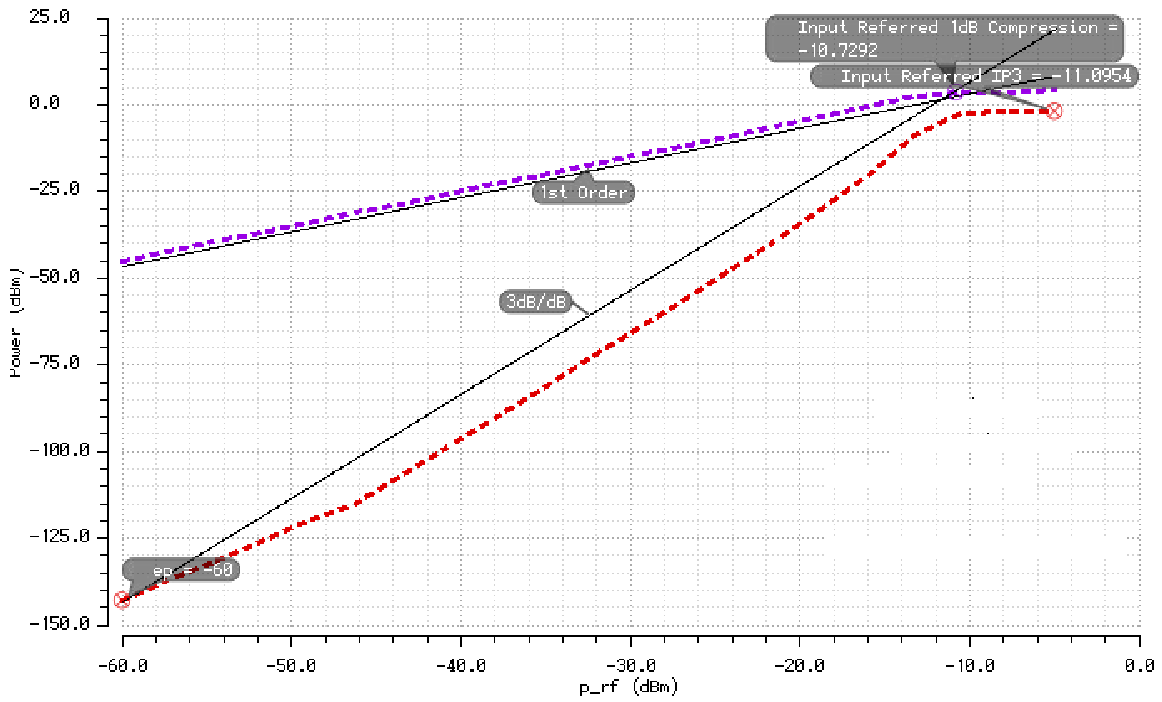


Figure 5.36. 1 dB compression point and IIP3 at 300 MHz.

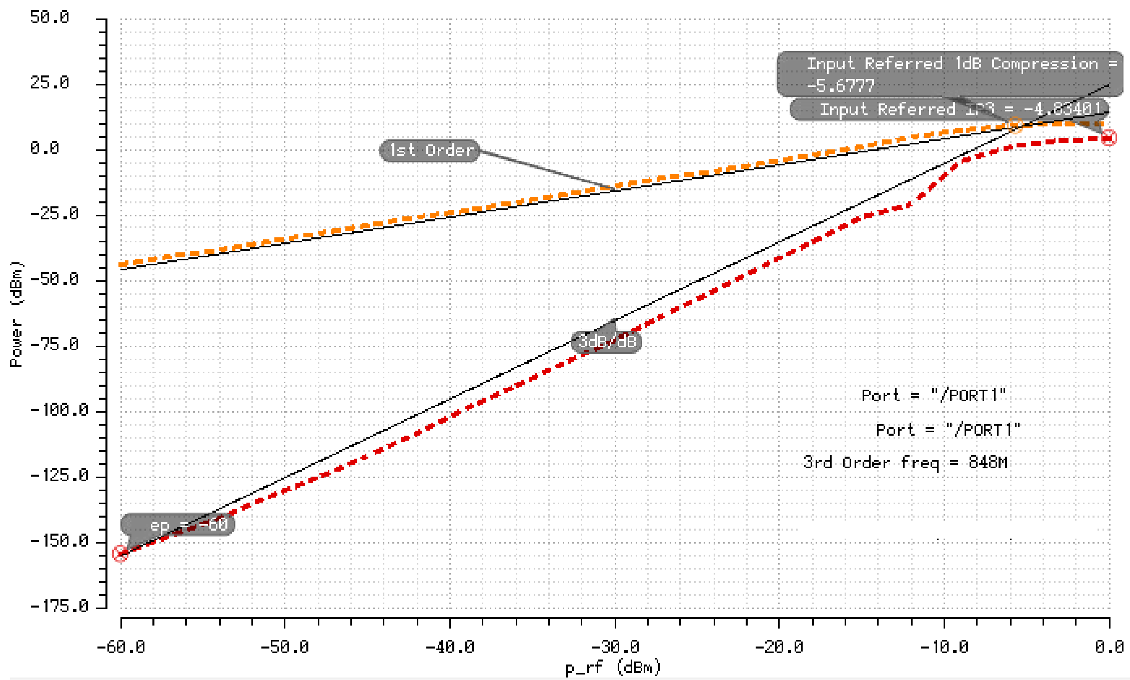


Figure 5.37. 1 dB compression point and IIP3 at 850 MHz.

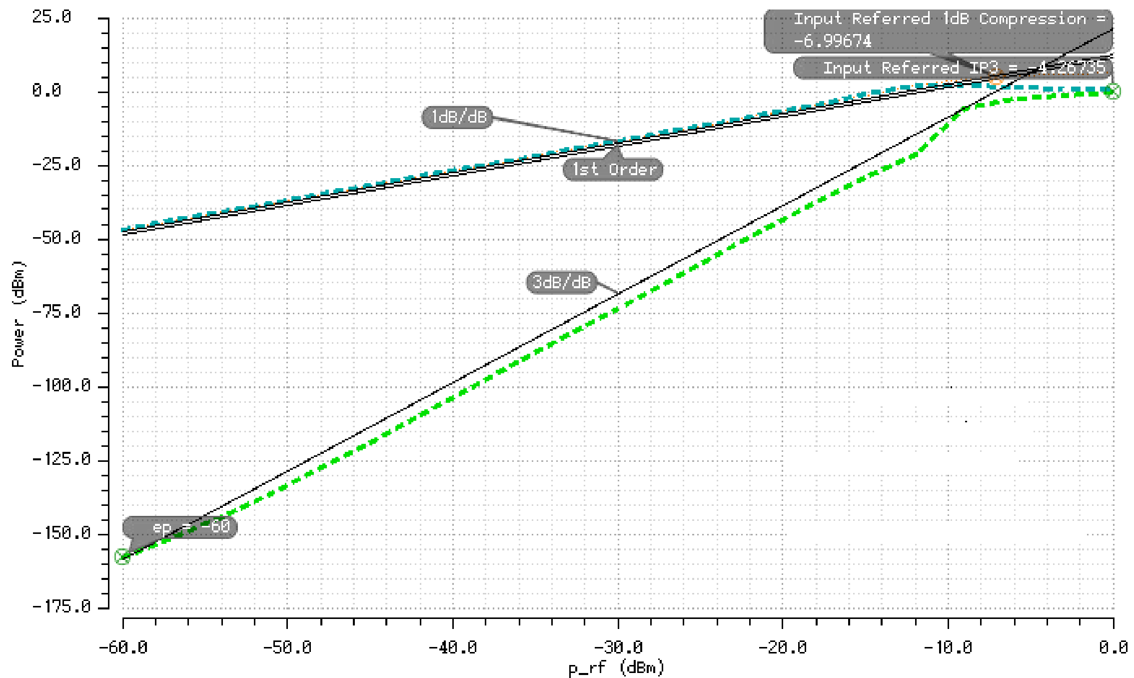


Figure 5.38. 1 dB compression point and IIP3 at 1.4 GHz.

The graphs show that the 1 dB compression point increases from –10.7 dBm at 300 MHz to –7 dBm at 1.4 GHz. The IIP3 increases from –11 dBm at 300 MHz to -4.2 dBm at 1.4 GHz. In the centre of the frequency band, the 1 dB compression is -7 dBm and the IIP3 is -4.2 dBm. Hence, the 1 dB compression point and the IIP3 are constant at least in the top half of the frequency band.

5.2.17 Monte Carlo and corner analysis

The Monte Carlo (MC) analysis allows evaluation of the impact of a large number of random parameters on few measurable outputs. In analog ICs fabrication, several changes in fabrication parameters, such as variations in doping levels, the quality of used materials and the fineness of the etching, can result in relatively large changes of performance parameters such as NF, S_{11}, S_{22} and gain. These changes, which can be random or systematic, are referred to as process variations and their effects increase as the size of active and passive devices in ICs continue to shrink. The variations are due to wafer inconsistencies (e.g. oxide thickness) and manufacturing inconsistencies (e.g. anisotropic etching, optical shadows, etc.), resulting in changes in pattern sizes for the same device;

they reflect the statistical nature of the semiconductor fabrication process. These variations should be managed by the designer, as their effects on yield and performance may be detrimental.

The total variance resulting from a fabrication process can be divided into:

- Lot-to-lot variance. This variance is generally the largest one and results from variations between raw material batches, variations due to adjustments, upgrades, aging tools and several other process and time-related changes.
- Wafer-to-wafer variance. These variations are due to differences between wafers that result from their processing.
- Die-to-die variance that may be a result of the lithography process or wafer uniformity.

Devices on a die are equally affected by lot-to-lot, wafer-to-wafer and die-to-die variances. These variances are called global or process variances. Device-to-device variance is found between two instances of the same device on a die. This variance is a result of variations in edge definitions, dopant level, junction areas, and so on. It is referred to as local variation or mismatch variation. Analog ICs are particularly sensitive to mismatch between intra-die devices and between devices from different production runs. It is shown in [142] that device mismatch can be reduced by increasing the area of critical components. Environmental variations, such as temperature and voltage, and process variations are described within process models.

The probability that an IC operates within specifications can be estimated by the MC analysis. MC analysis allows determination of the yields – typically 95% to 99.86% for RFICs - of a given design and is based on statistical models provided with the process library. The impact of physical parameters such as the thickness of metal layers and the resistance of metal contacts to performance is analysed through numerous iterations. For each iteration, random values related to process parameters are used in the calculation of the value of the signal under investigation. For significant statistical results, 500 to 1000 iterations are required. The statistical distribution of the parameters of an output signal of

an IC is Gaussian, with σ as standard deviation and $\overline{X}$ as mean. For a Gaussian distribution, the probability that the value of a parameter is between $\overline{X} - \sigma$ and $\overline{X} + \sigma$ is 67%, 95% for $\overline{X} - 2\sigma$ and $\overline{X} + 2\sigma$ and 99% for $\overline{X} - 3\sigma$ and $\overline{X} + 3\sigma$.

A point in the variation space is referred to as a corner. Corner analysis allows analysis of the impact of random extreme variations in fabrication processes on the performance of ICs and is based on the same statistical distributions used in MC analysis. However, mismatch analysis of the same device at different locations of the die is not performed. Hence the number of iterations is much smaller and the analysis is much quicker: the main factors affecting performance can be identified quickly. Following the analysis, the circuit can be redesigned in order to reduce the dependency of performance parameters on the variability of fabrication processes and of parameters such as temperature, operating voltage and circuit elements. In this way, the manufacturing yield can be improved. During the design cycle, corner analysis takes precedence over MC analysis.

The accuracy of corner analysis, that uses fixed corners from the process worst-case variations, is limited. In addition, when the number of corners is large, their selection is not trivial and may be arbitrary. Fixed corners are related to the measure of speed and power in digital circuits and are not adequate for analog circuits, as critical failure conditions related to analogue behaviour can be overlooked. Finally, as referred to in the previous paragraph, local variations are not addressed by corner analysis. Corner analysis is therefore desired when mismatch variations are small and when performance metrics are related to speed and power consumption.

In the IBM BiCMOS8HP process, corner simulations can be classified into two groups: timing simulations and other simulations. Timing simulations relate to NMOS and PMOS extreme speeds. Seven configurations are available: tt, ss, ff, sf, fs, fff and ssf, where the first letter refers to NMOS devices and the second letter to PMOS devices. The corner fff refers to Fast-Fast-Functional, corresponding to fast NMOS and PMOS, but with limited variations of transistor parameters (-1σ to +1σ instead of -3σ to +3σ), corresponding to

67% of devices. Generally, tt, fff and ssf corners provide an acceptable indication of the dependence of performance on the speed of transistors. For maximum yield, the designer should take into account variations between -3σ and +3σ. Other simulations take into account devices such as inductors and capacitors, resistors, doping levels and circuit input variables. Generally, for quick simulation and for ease of analysis, process parameters and two additional parameters – supply voltage and operating temperature - are used for the simulation. This analysis is referred to as PVT simulation. The simulation is first done with the following corner parameters, whose combination results in 27 corners:

- Process:
    - For BJT, only tt (typical), ssf (slow slow functional) and fff (fast fast functional).
    - For resistors and inductors, only tt, ssf and fff.
    - For PMOS, slow (ssf or fsf) and fast (sff or fff) are used, as the circuitry does not use NMOS transistors.
- Temperature: -40° and 125° C.
- Supply voltage variation of 10%, from 2 V to 2.4 V (V_{DD} = 2.2 V).

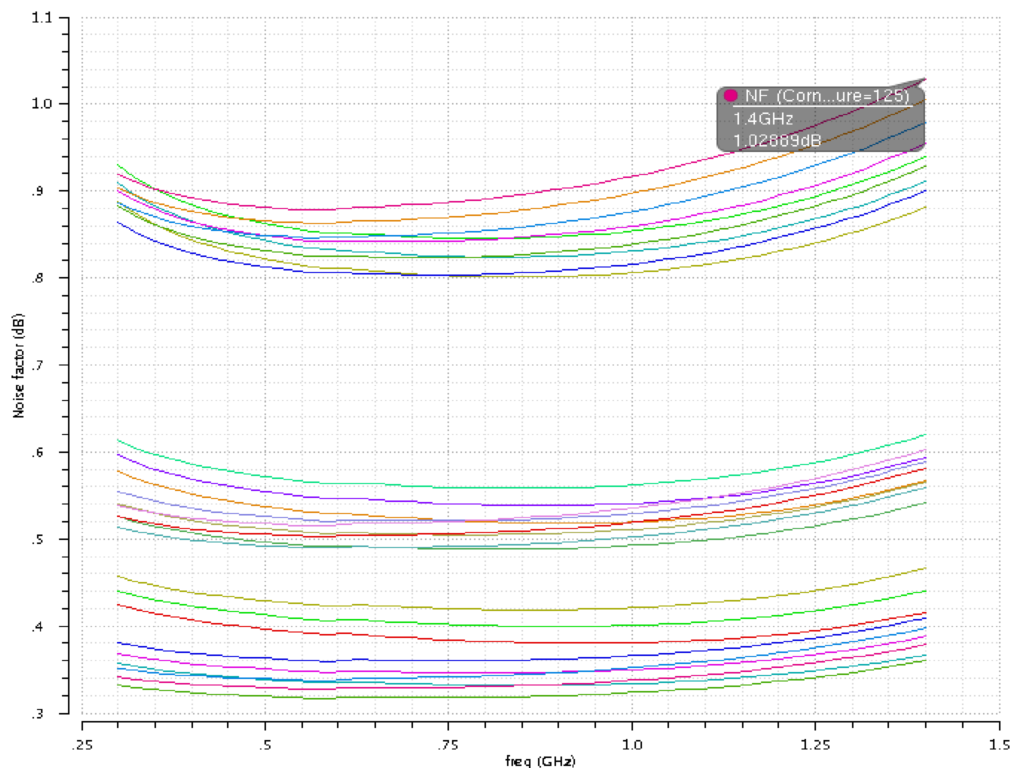


Figure 5.39. NF versus frequency and corner parameters.

The most favourable corners for the NF correspond to ssf for the process, -40° C for the temperature, and 2.4 V for the power supply. The NF at 1.4 GHz is 0.360 dB and the minimum NF in the bandwidth is 0.3168 dB at 586 MHz. The most unfavourable corners for the NF correspond to fff for the process, an operating temperature of 125° C and a supply voltage of 2.4 V. The NF at 1.4 GHz is 1 dB and the minimum NF in the bandwidth is 0.8785 dB at 564 MHz. The plot of the NF as function of the frequency for the 27 corners is shown in Figure 5.39, where the traces in the centre of the graph correspond to an operating voltage of 2.2 V.

Similarly, the plots of S_{11}, S_{22} and of the gain G_A for the corner are represented in Figure 5.40, Figure 5.41 and Figure 5.42. For S_{11}, the worst performance (-8 dB) is achieved for the corner fff, for an operating temperature of -40° C and an operating voltage of 2 V at 300 MHz. The best performance (-20 dB) for S_{11} is achieved under the same corners at 1.4 GHz. The desired S_{11} performance corresponds to a flat response (-11 dB) in the bandwidth of the LNA and to the corner tt, 27° C and 2.4 V.

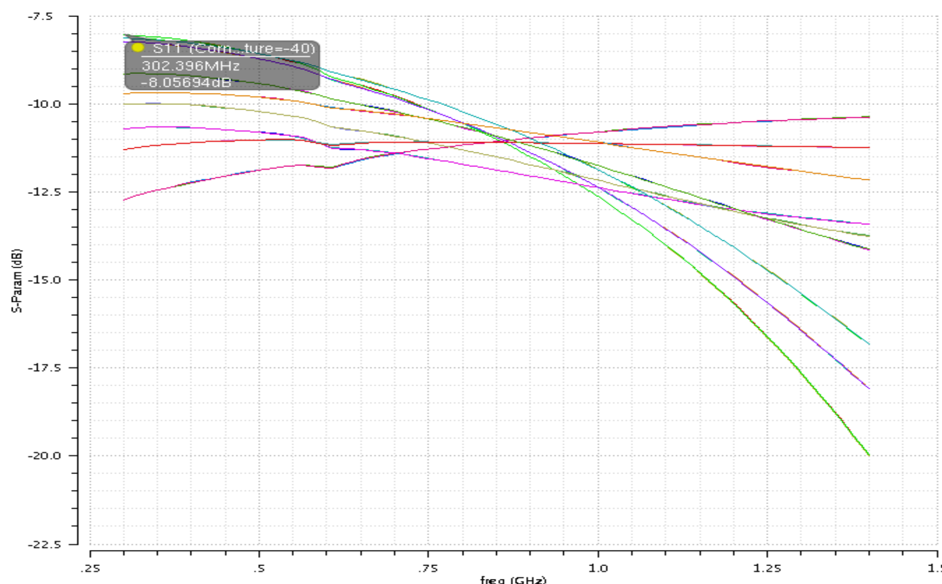


Figure 5.40. S_{11} versus corner parameters.

For S_{22}, the worst performance (-7.5 dB at 300 MHz and -6.4 dB at 1.4 GHz) is achieved for fff and at -40 °C and 2.4 V. The best performance (-11 dB at 300 MHz and -7.1 dB at 1.4 GHz) is achieved for ssf, at 125° C and 2.2 V.

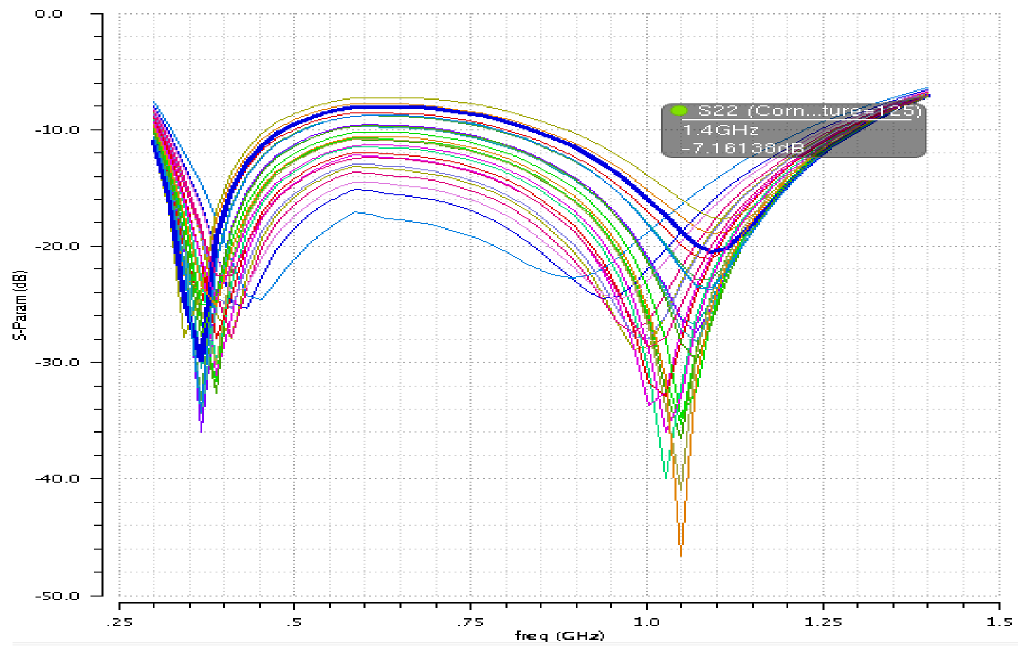


Figure 5.41. S_{22} versus corner parameters.

Finally, the maximum gain is 18 dB, which is achieved for ssf, at 2.4 V and -40° C at 556 MHz. The lower gain is 12 dB at 1.4 GHz and corresponds to the corner fff, at 2 V and at -40 °C.

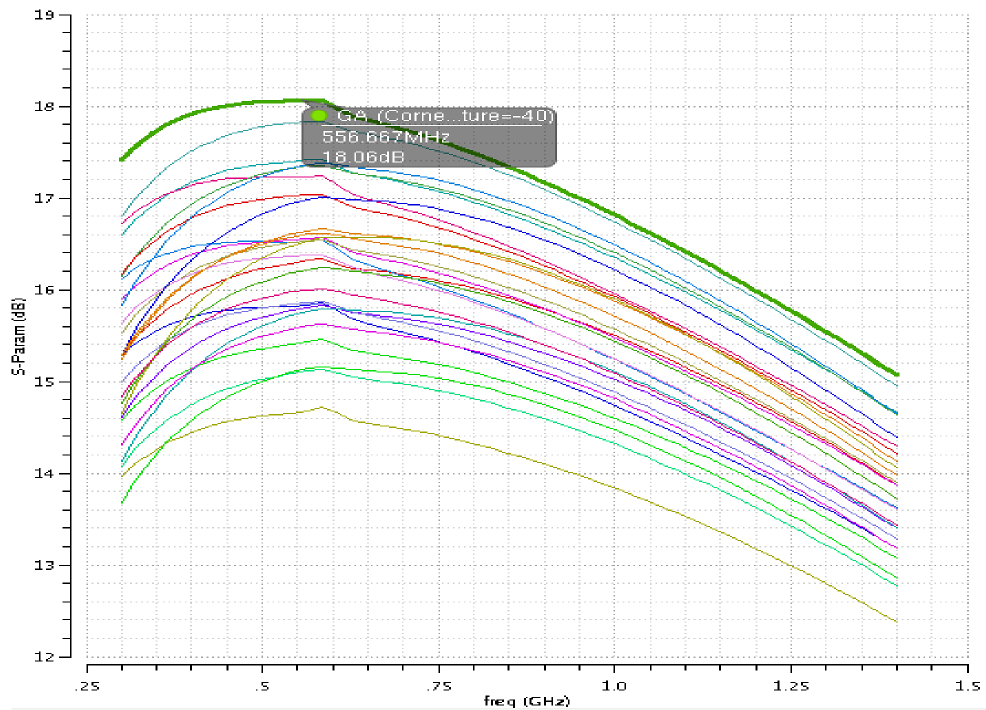


Figure 5.42. G_A versus corner parameters.

In summary, when die mismatches are not considered and under the given voltage and temperature corners, 67% of devices will have, at 1.4 GHz, an NF between 0.360 dB and 1 dB, 67 % of devices will have a maximum S_{11} that varies between -8 dB and -11 dB, 67 % of devices will have a maximum S_{22} between -6.4 dB and -11 dB. For the gain, 67 % of devices will have a maximum gain between 18 dB and 15 dB.

The variation in performance (NF, S_{11}, S_{22}, G_A) can be improved by using a fixed supply voltage of 2.2 V and by reducing the temperature range (-10 °C to 70 °C). Targeting a yield of 99 %, and still not considering die mismatch the number of corner parameters used in this work are reduced to nine, which become:

- Process:
  - For BJT, only tt (typical), ss (slow) and ff (fast)
  - For resistors and inductors, tt, ss and ff
  - For PMOS, the slow (ss or fs) and fast (sf or ff) are used; the circuitry does not use NMOS transistors.
- Temperature: -10 °C and 70 °C.

The simulation shows that at 1.4 GHz, the maximum possible NF is 0.725 dB and the minimum possible NF is 0.447 dB. When the maximum temperature is 125 °C, the values expected for NF (0.447 dB to 0.944 dB) are close to the results of an MC simulation. MC simulation results are shown in Figure 5.43, Figure 5.44, Figure 5.45 and Figure 5.46.

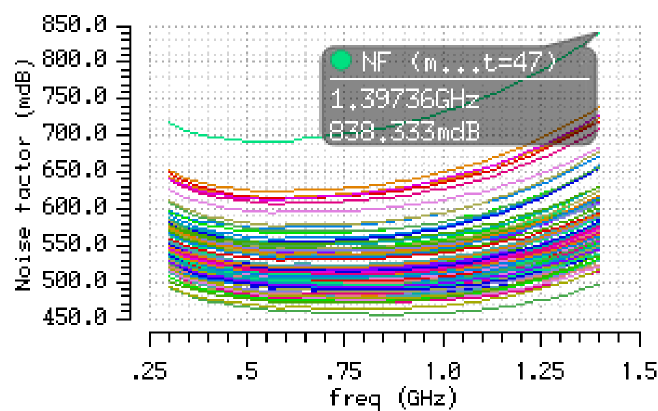


Figure 5.43. Monte Carlo analysis (process and mismatch) for NF.

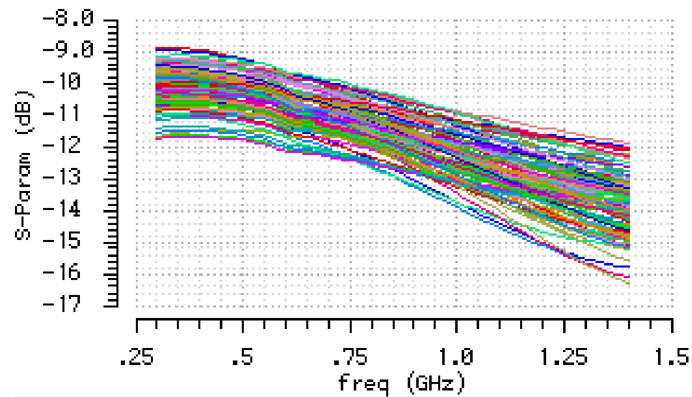


Figure 5.44. Monte Carlo analysis (process and mismatch) for S_{11}.

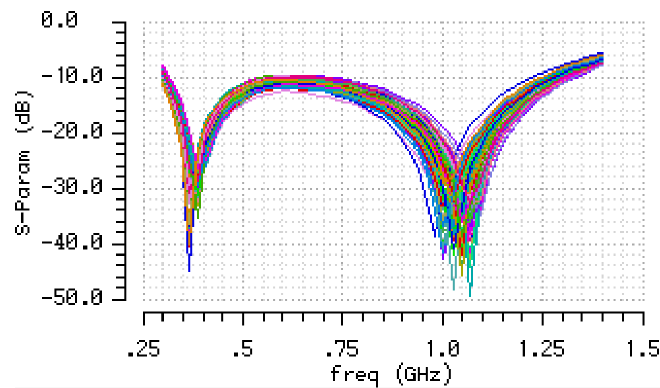


Figure 5.45. Monte Carlo analysis (process and mismatch) for S_{22}.

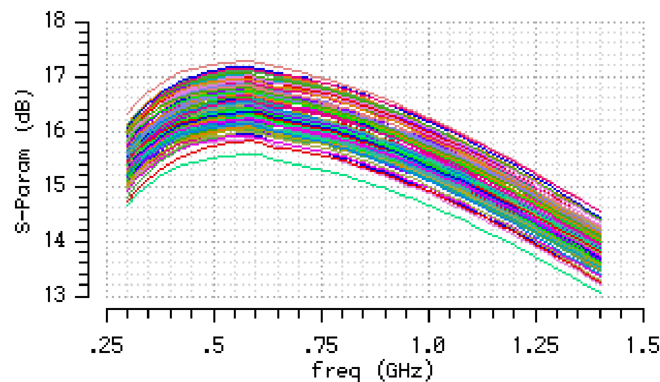


Figure 5.46. Monte Carlo analysis (process and mismatch) for G_A.

5.2.18 Sensitivity analysis

Simulations using PVT corners have shown that temperature and voltage are major sources of NF variation. The variation of the NF being large, a sensitivity analysis is required in order to determine the main sources of variation and possibly to improve the design. In

order to identify the main sources of global and local variations, an MC analysis is required. These could not be performed before the submission of the layout for fabrication, because the design process was subject to the deadlines of additional projects.

5.3 CONCLUSION

This chapter has presented the implementation of the LNA, which includes the sizing of the cascode transistors and of the matching and bias networks. This is done by several simulations allowing for verification of the stability and linearity of the LNA. The variations of the main performance parameters of the LNA in function of process, temperature, voltage and device mismatches are shown and result from corner and MC simulations.

CHAPTER 6 LAYOUT, PACKAGING AND PCB

6.1 INTRODUCTION

The layout of digital ICs can be fully automated, using a schematic or a hardware description language as inputs to place and route programs that generate the layout. The performance of analogue ICs is very sensitive to their layout; their layout is generally manual, iterative and very intensive. In addition, manual layout ensures an efficient use of the chip area and is one of the most important steps in analog IC design. Such work requires advanced understanding of the layout requirements for all devices in the design and of how their layout relates to their performance and to the fabrication process. An example of such a case is the requirement to tied down the plates of MIM capacitors to avoid damage during fabrication. To the experienced designer, the layout of an analogue IC may appear as an art, as it relies on intuition, insight and experience; hence book titles such as “The art of analogue design” [143] and “Crafting a chip”. This chapter presents the layout of the LNA with the relevant design rule check (DRC) results, its packaging and the design of its mounting PCB for measurements. It is noted that, because of issues related to the unavailability of some Cadence functionalities, layout-versus-schematic checks were not performed.

6.2 FLOOR PLANNING

The first step in floor planning is analysing the schematic to identify critical functional blocks whose response can be affected by the layout. Such blocks are the lower and higher

14 parallel transistors of the cascode amplifier, the output matching network and the current mirror for the biasing network. The transistors of the current mirror must be matched and in perfect symmetry (same orientation and in the same isolation well-guard ring). The impact of the relative locations of these blocks must be considered, as well as the size and structure of interconnection tracks.

Following the analysis, components are positioned on the floor plan in the area allocated to the IC, devices that belong to the same functional block are grouped and space is allocated for interconnections. Special attention is required for on-chip inductors, which are large and expected to be distant from signal sensitive devices and interconnections. A safe distance between metal lines and between inductors is required to reduce magnetic coupling. It is desired to use the same direction of interconnections (vertical or horizontal) on the same metal layer. Signal interconnections have finite impedance that can affect gain and noise performance, hence they must be minimised. It is desired to shorten the signal path from the input bondpad to the input transistors and the path from the output transistor to the output bond pad. Ground interconnections can also cause losses. A uniform and continuous ground plane running through the chip area can reduce the signal path and ground losses. Grounded components such as decoupling capacitors are then directly connected to the ground plane, which reduces the signal path. The ground plane is also used to reach the minimum percentage of metal level required by DRC.

6.3 LAYOUT

The lower and higher cascode transistors are as close as possible to the RF input pad. The thickest metal track AM (with the lowest resistance) is used to connect the RF input pad to the bases of the 14 input transistors. The AM metal track is used for the signal in order to reduce losses and noise coupling owing to its low resistance and large distance from the substrate. The connection of transistors to the top metal is done through vias. The vias are as close as possible to the ports of transistors and are as wide as the AM metal layer. The current mirror transistors are symmetrical and in close proximity to improve their matching during fabrication and ensure equal characteristics. They are also placed close to the input

transistors. A critical requirement in the layout of analog ICs is the matching on Si of devices that are expected to be identical. Such devices may differ after fabrication because of process variations. While digital ICs use transistors of a minimum size for a small area, low consumption and high speed, devices that are larger than the minimum size can be used in analog design, as illustrated in this work. Such large devices are used to obtain the required gain or NF but are affected more by process variations. In addition, devices of large size are less affected by device mismatches. Methods to reduce the impact of device mismatch include interdigitised and common centroid layouts.

The base and the choke coils are off-chip, while the remaining coils such as the degeneration inductor and the coils from the output matching network are on-chip and shielded to prevent parasitic noise coupling with the substrate. The inductive degeneration coil is in close proximity to the common-emitter transistors to reduce losses in interconnections. The pads for the capacitive coupling between the lower and higher cascode transistors are in close proximity to the transistors. The output matching network is close to the RF output pad but distant from the input signal pad and tracks. In order to reduce mutual electromagnetic coupling between bondwires, the RF input bond pad is surrounded by bondpads that are AC grounded. Signal routing is performed by higher level metal tracks. Interconnections between metal tracks are done by low-resistance vias. The bias current of the 14 parallel transistors measured by simulation is 6.05 mA at the collector of the input transistors. For the dimensioning [85] of power tracks, a track that can handle 10 mA for the 14 transistors is used; hence the track for each transistor can handle up to 0.714 mA. Several MIM capacitors are used in the design.

The chip is shared by several projects, therefore issues related to multi-project IC design, such as the size of the area required by each project on the chip, the location of each project relative to the pad ring, the number of required input and output pins per project, the use of “C4” type bondpads and the implementation of the power grid for each project have been addressed. Bondpads have a size of 101 μm × 101 μm, which is in line with the minimum size of 100 μm × 100μm recommended by the foundry. For V_{DD}, two bondpads are used around the periphery of the chip. DRC errors were generated for bondpads when

M1 (recommended to decouple the noise from the substrate) was used as backplane for bond pads. The errors were cleared when NS was used. The schematic of the LNA is shown in Figure 6.1. The outline of the layout of the LNA is shown in Figure 6.2.

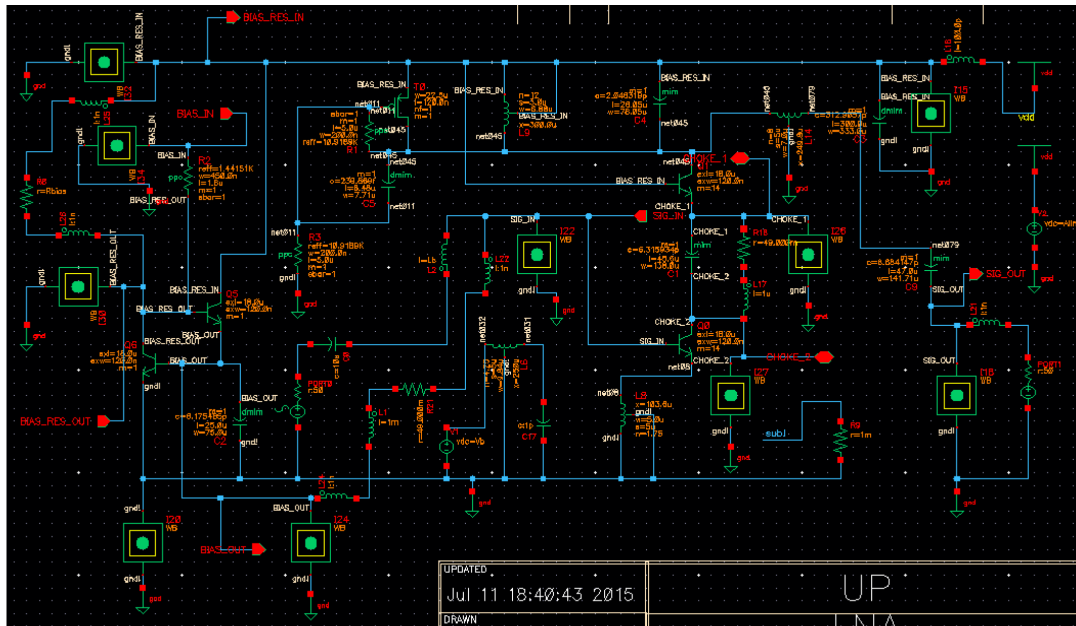


Figure 6.1. Schematic of the LNA.

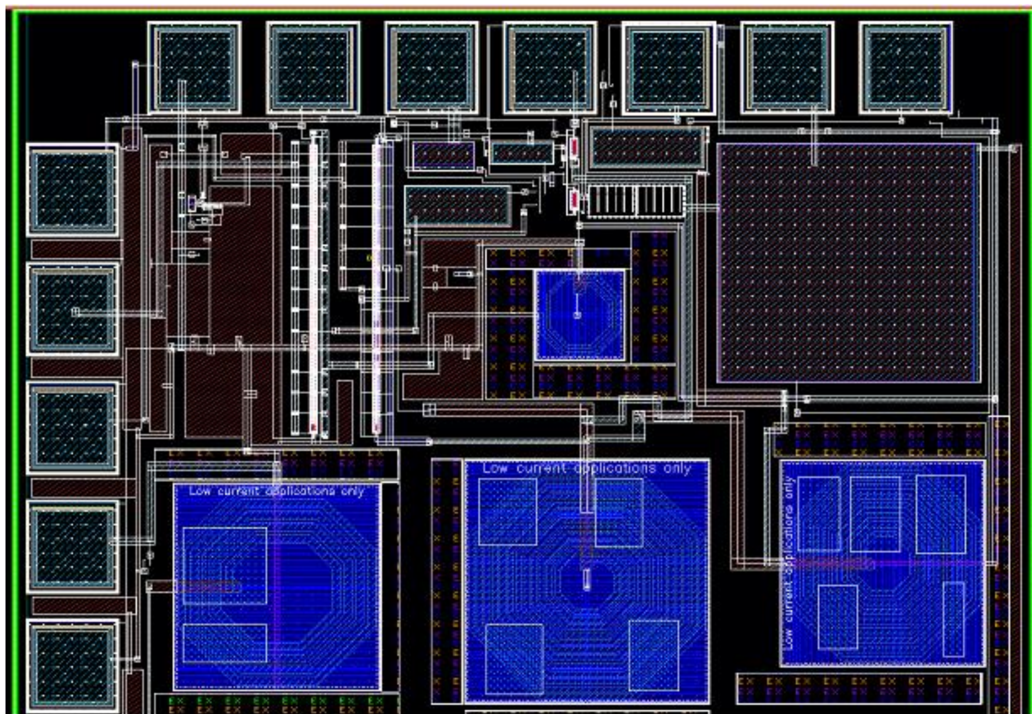


Figure 6.2. Outline of the layout of the LNA.

6.4 CHIP BONDING AND PACKAGING

On-chip measurement equipment was available but the LNA requires external chokes, an off-chip input inductor and other external components for biasing. For this reason, the chip was designed with bonding pads rather than with test pads (C4) even if a flip-chip package could have been used, but this solution was not chosen for reasons provided in this section. Bonding wires were used to connect the bonding pads to the pins of the IC package. The packaged IC with related external components was mounted on a PCB. The fabricated IC was a multi-project wafer run from MOSIS. The multiproject IC is shown in Figure 6.3 where the LNA is implemented in the top left corner.

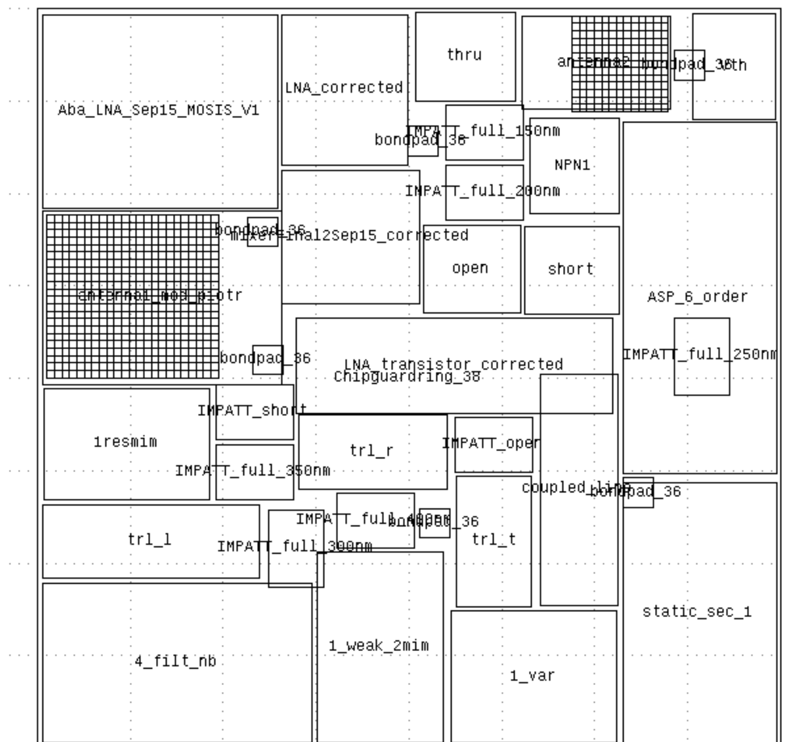


Figure 6.3. Fabricated multi-project IC.

In general, bondwires are used for the packaging of LNAs. For ultra-sensitive LNAs, the parasitic resistance, capacitance and inductance of bondwires, as well as the mutual magnetic coupling between bondwires can impair their performance. It is therefore desired to evaluate how the packaging of the die affects the noise performance of the LNA. Possible packaging options are bonding wires packaging and flip-chip packaging. Flip-chip

packaging adds shunt capacitance to the die input, but it is found in [144] that losses due to flip-chip bonding can be neglected for operating frequencies of a few GHz. It is also found that when flip-chip bonding is used, the PCB ground plane can impair the performance of on-chip inductors through induced currents in the ground plane on the PCB that creates additional losses. In addition, flip-chip bonding may be subject to cracking due to mechanical stresses as a result of uneven heat distribution. It was therefore desired to use a quad flat no-lead (QFN) package, which is preferred for RF applications. However, QFN packages were not available and DIL packages were used instead.

The typical diameter of gold bondwires is 25 μm and the typical parasitic inductance can be roughly estimated as 1nH/mm. It is desired to use the parasitic inductance of the bond wire connected to the base input as circuit element. Because the value of the base inductor is 4.5 nH, a bond wire of 4.5 mm is desired. However, the exact length of a bondwire is uncertain and its inductance cannot be determined beforehand with exactitude. It is also desired to have a second type of package for which the bond wire to the base input is the shortest possible. The test board will then comprise two packages: the first package for which a 4.5 mm bond wire will replace the external base inductor and the second package that will require an external base inductor.

6.5 PADS DESCRIPTION AND SCHEMATIC

The PADs of the IC are represented in Figure 6.4. Their description is as follows:

- SIG_IN: the RF signal input, to be connected to the 4.5 nH external inductor.
- BIAS_OUT: the DC bias current to be connected to SIG_IN through a choke.
- BIAS_IN: when connected to V_{DD}, the bias current is fixed.
- BIAS_RES_OUT: can be used to adjust the bias current when connected to V_{DD} through a variable resistor when BIAS_IN is floating.
- SIG_OUT: the RF signal output of the LNA.
- CHOKE_1: to be connected to CHOKE_2 through an external choke.
- CHOKE_2: to be connected to CHOKE_1 through an external choke.

- Lb_IN1: first lead of an internal 4.5 nH on-chip inductor for testing.
- Lb_IN2: second lead of the internal 4.5 nH on-chip inductor for testing.
- V_{DD}: 2.2 V power supply.
- GND: Ground.

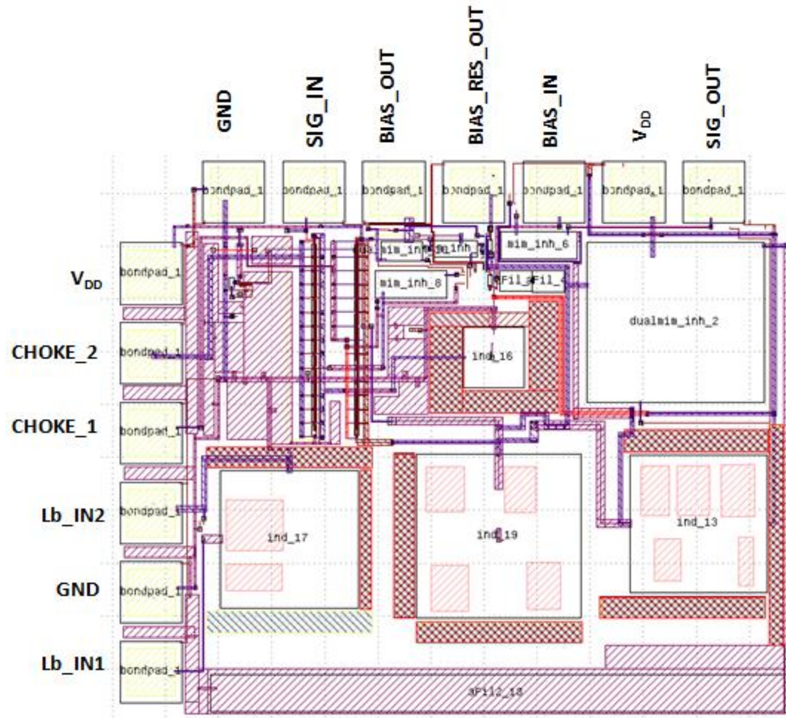


Figure 6.4. PADs of the IC.

6.6 THE PCB

For low frequencies and general-purpose applications, the most commonly used PCB material is the flame retardant formulation number 4 (FR4). This material results in binding glass fibres with epoxy and its cost is a very low. FR4 has high dielectric losses at microwaves and is not manufactured according to stringent specifications, leading to variations in specifications of up to 10%. The relative dielectric constant ε_r varies considerably and over frequency and is typically 4.5 at 1 GHz. Furthermore, ε_r can vary from manufacturer to manufacturer. Being a very good isolator, this material is however used for non-critical RF applications, up to a few GHz.

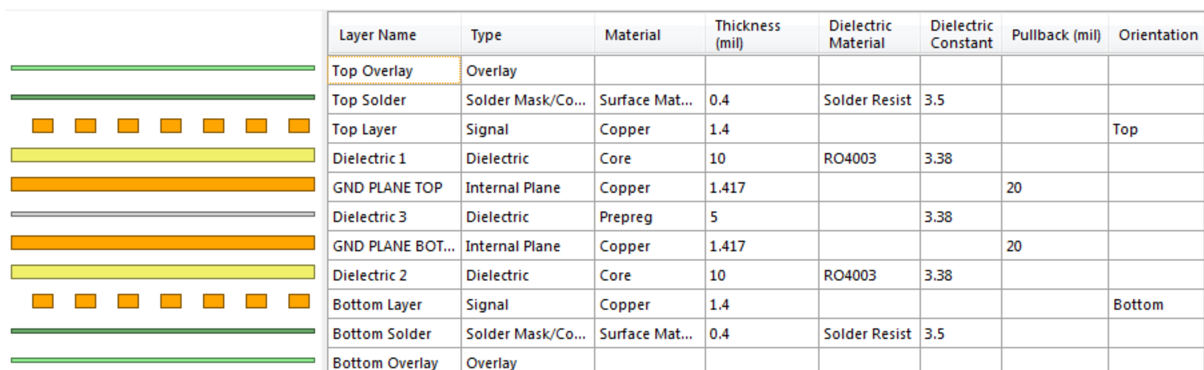
PCB materials based on Teflon™ (polytetrafluoroethylene), such as RO4003 from Rogers Corporation, achieve lower losses than FR4 and have a relative dielectric constant of 3.38 with a possible variation of 1.5%. In this work, a four-layers RO4003 PCB was used. Four layers are used because a ground plane is required for RF tracks that are routed as microstrip transmission lines using the impedance-based routing feature of the CAD tool.

The characteristic impedance is better determined by PCB manufacturers because the impedance equation used for impedance-based routing is an estimate and may not provide realistic results, as factors such as temperature, the dielectric coefficient of all parts, shapes of the etched traces or thickness of the solder mask are not taken into account. Although some CAD tools can provide impedance-based routing, the results are approximate and may lack the required accuracy for critical applications. For such application, fabrication houses add a sample coupon on the PCB that corresponds to the track geometry to be used for the required characteristic impedance.

The parameters of the PCB are:

- Material: RO4003.
- Dielectric coefficient: 3.38.
- Four metal layers: Top layer, Ground Plane 1, Ground Plane 2, Bottom Layer.
- Dielectric: Core, Prepreg, Core.

The thickness of the PCB layers is given in Figure 6.5 and the outline of the PCB layout in Figure 6.6.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Mat...	0.4	Solder Resist	3.5		
Top Layer	Signal	Copper	1.4				Top
Dielectric 1	Dielectric	Core	10	RO4003	3.38		
GND PLANE TOP	Internal Plane	Copper	1.417			20	
Dielectric 3	Dielectric	Prepreg	5		3.38		
GND PLANE BOT...	Internal Plane	Copper	1.417			20	
Dielectric 2	Dielectric	Core	10	RO4003	3.38		
Bottom Layer	Signal	Copper	1.4				Bottom
Bottom Solder	Solder Mask/Co...	Surface Mat...	0.4	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 6.5. Thickness of PCB layers.

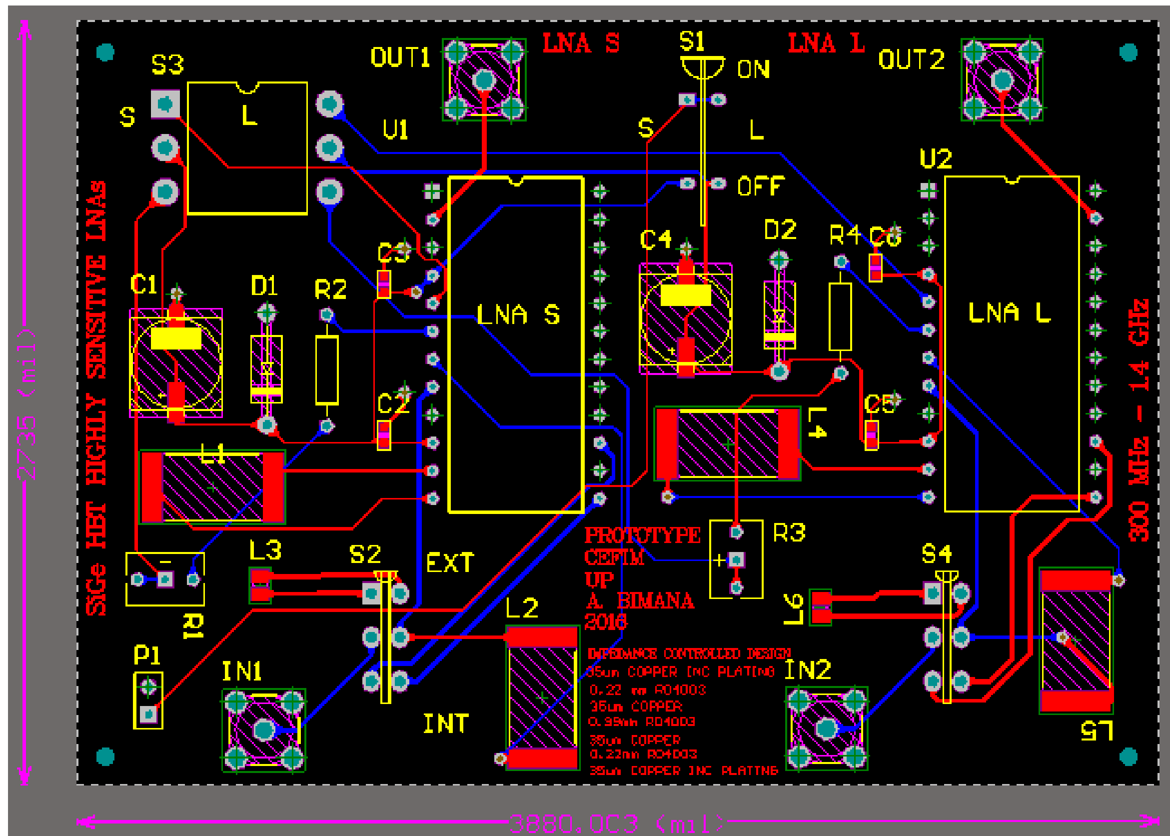


Figure 6.6. Outline of the test PCB.

6.7 CONCLUSION

The LNA has been fabricated by MOSIS as part of the MEP. Its size is 1.022 × 1.041 mm^2, the size of the multiproject IC is 4.010 × 4.002 mm^2. Because of the non-availability of QFN packages, 24 pins ceramic DIL packages were used. Two LNAs were packaged: one with an input bonding wire of 4.5 mm and one with the shortest possible bonding wires. The LNAs were mounted on a PCB for testing. The layout, bonding and packaging of the LNA with the PCB have been presented in this chapter.

CHAPTER 7 MEASUREMENT RESULTS

7.1 INTRODUCTION

This chapter was written last; it is short because measurement results were not satisfactory and NF measurements could not be done. The chapter describes the initial test setup, provides possible causes of the lack of amplification and presents the debugging results. Two possible causes of signal attenuation are identified: a defect in the layout or a signal short between the source and the drain of a MOS transistor in the output matching circuit.

7.2 MEASUREMENT SETUP

The measurement of S-parameters is required to describe the behavior and the properties of the packaged LNA. Such measurements were expected to be performed by the Rohde & Schwarz Vector Network Analyser (VNA) ZVA40 shown in Figure 7.1.

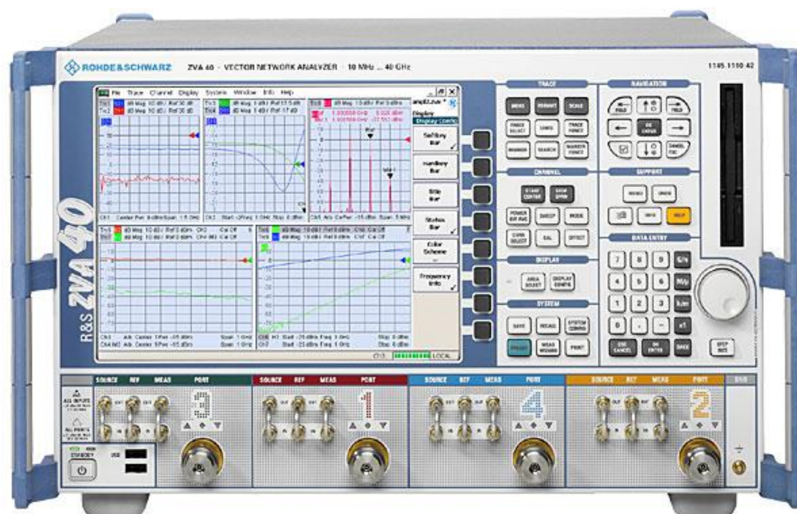


Figure 7.1. Rohde & Schwarz VNA ZVA40.

The Keysight Technologies Spectrum Analyser E4440 in Figure 7.2 was available for NF measurements. Provided with the HP 346A noise source in Figure 7.3, the spectrum analyser can measure the NF using the Y-factor method.

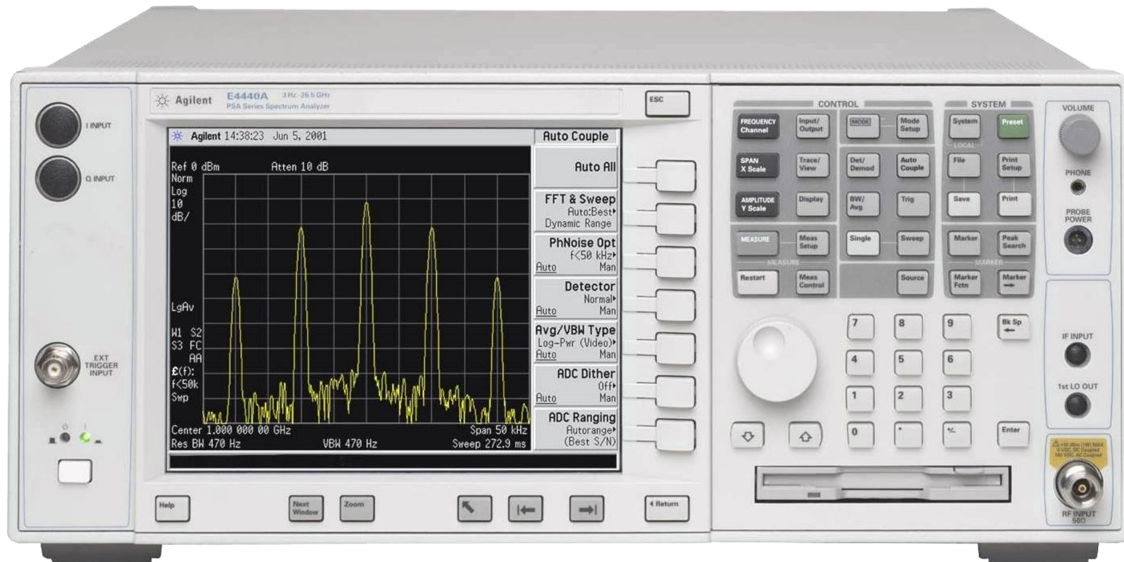


Figure 7.2. E4440 Spectrum Analyser.

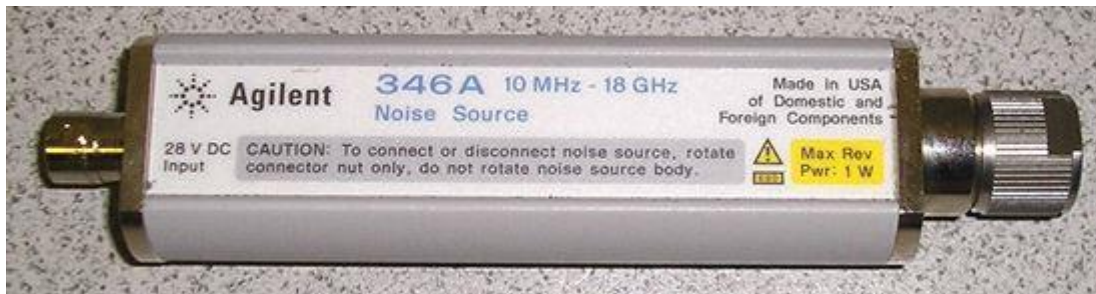


Figure 7.3. HP 346A noise source.

The Y-factor method solves the gain-noise equation $N_1 = GkT_o\Delta f + N_A$ derived from (4.4), where G is the power gain of the device under test (DUT), N_A is the intrinsic noise of the two-port device at room temperature and kT_o is the input noise power at room temperature, with T_o = 290 K. The noise source is switched between two levels of noise power, referred to as cold noise temperature and hot noise temperature, and the noise factor is given by the expression $F = ENR/(Y - 1)$, where ENR is the excess noise ratio of the

noise source and *Y* is the ratio between the hot noise power and the cold noise power at the output of the two-port DUT. It is obvious that, when there is no output signal or when the input signal is attenuated at the output owing to a malfunction of the DUT, the noise factor cannot be measured.

7.3 MEASUREMENTS

The schematic of the circuit under test, including the IC and external components on the PCB, is shown in Figure 7.4.

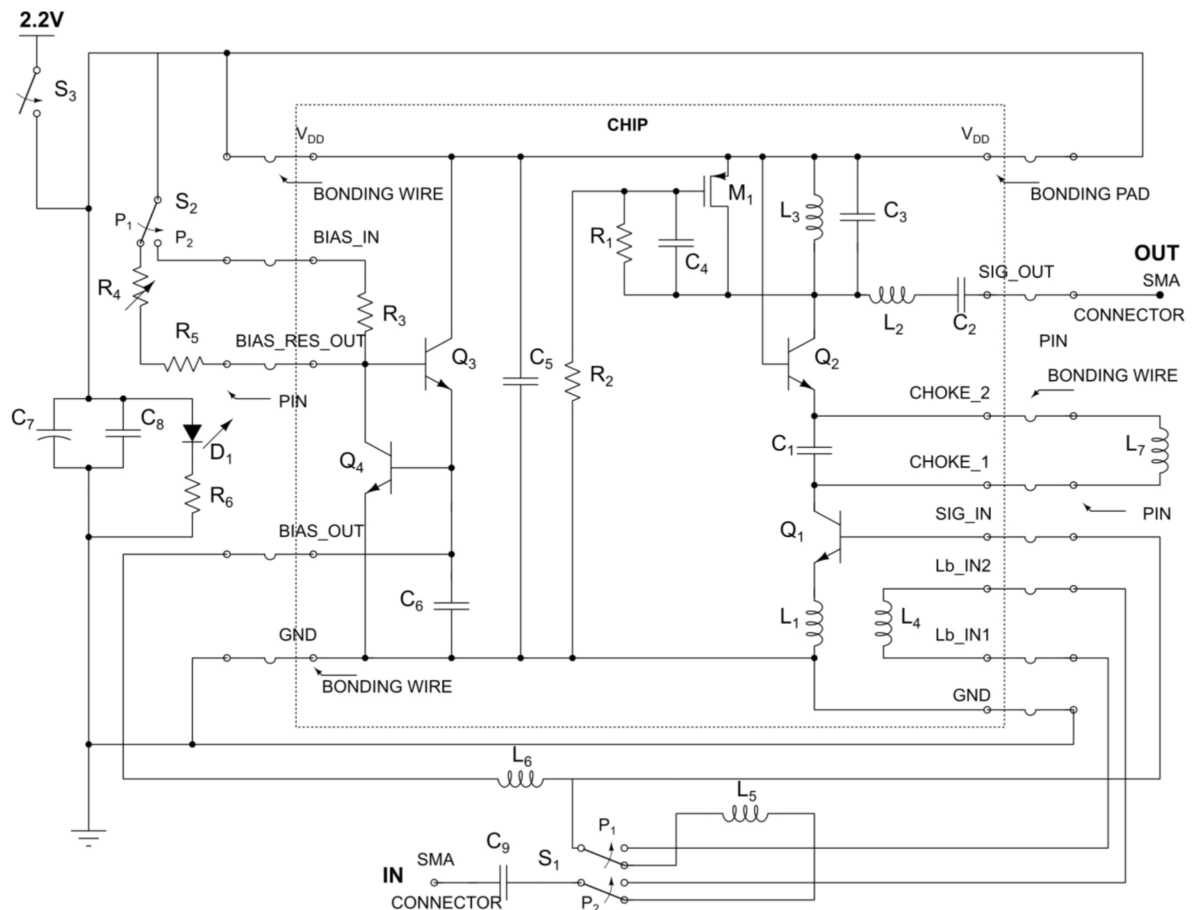


Figure 7.4. Schematic of the LNA (CHIP) and the PCB.

7.3.1 DC measurements

The PCB holds two LNAs: an LNA with a short bonding wire for the signal input pad, referred to as LNA-S, and an LNA with a bonding wire of 4.5 mm for the signal input pad, referred to as LNA-L. For simplicity, only one LNA is represented in Figure 7.4. The base inductors L_4 and L_5 are not required for LNA-L because they are replaced by the inductive bonding wire on SIG_IN.

The switch S_3 is used to supply DC power (2.2 V) to the LNA and the LED D_1 is on when the device is powered. The current source for the biasing of the LNA is formed by Q_3, Q_4 and Q_1. The base current of Q_1 is determined by the on-chip resistor R_3 but can be controlled by the external resistors R_4 (adjustable) and R_5. External control is selected by the switch S_2.

The base bias voltage on Q_1 for LNA-S is equal to 28 mV when the current source is controlled by the external resistors R_4 and R_5. When the current source is controlled by R_3, the base voltage is 8 mV. This indicates a malfunction of LNA-S.

For LNA-L, the total DC measured is 12.3 mA, which includes 6.4 mA for the LED D1. Hence, the collector current for Q_2 is 5.9 mA, which compares favourably to simulation results (6.05 mA). The base bias voltage for Q_1 is 775.4 mV when the current source is controlled by R_4 and R_5. This voltage is very close to simulation results (770.5 mV). When R_3 is used for the current source, the base bias voltage for Q_1 is 43 mV, which indicates a malfunction. The voltage on the pads CHOKE_1 and CHOKE_2 is 1.4791 V.

In summary, in terms of DC bias, the LNA-S shows a malfunction. This indicates a failure related to R_3 due possibly to damage to the IC during the wire bonding process, to R_3 or to the layout of the IC related to R_3. It is recalled that the LVS test was not performed during the design of the IC. The collector current and base bias voltage for LNA-L are in line with simulation values when the IC current source uses R_4 and R_5 (external biasing).

7.3.2 RF measurements

The first step in RF measurements consists in checking the RF power at the output of LNA-L when a signal is applied to its input but the unit is not powered. It is found that this signal is present at the output but attenuated (5 dB to 40 dB). The attenuation decreases when the DUT is powered and power gain is present in a small part of the bandwidth, as shown in Figure 7.7. The plots of the transfer of RF power from the input to the output of the LNA are shown in Figure 7.5, Figure 7.6 and Figure 7.7.

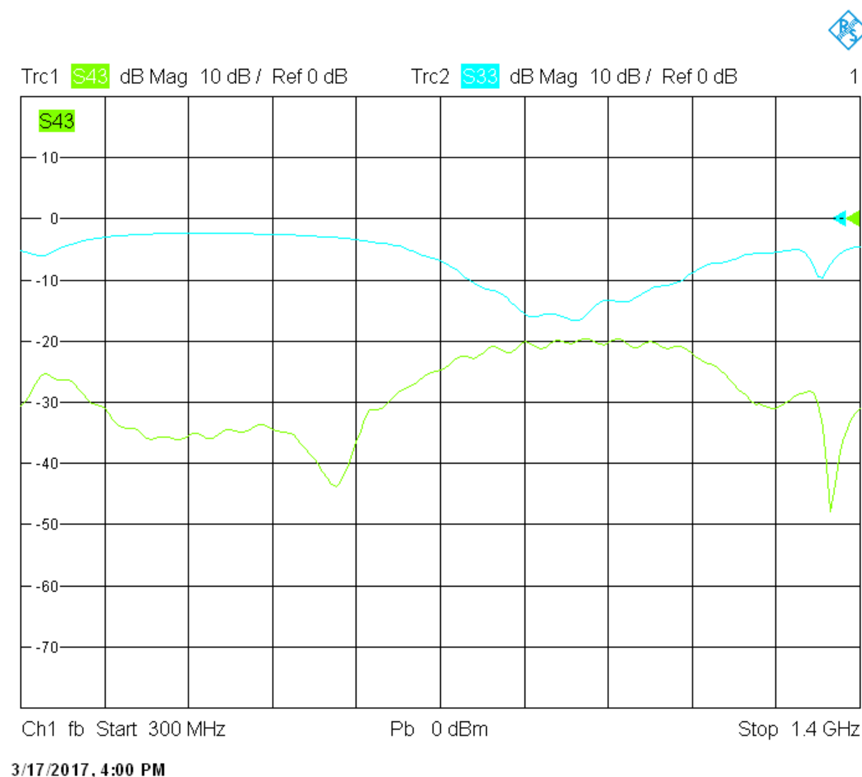


Figure 7.5. Output (green) versus input (blue) and frequency (no DC).

The output signal (without DC supply) shows that there is a parasitic coupling between the output and the input of the DUT. The signal may also indicate a faulty ground. Because there is no proximity between output and input tracks on the PCB and because of the use of two ground planes as middle layers for the four metal layers PCB (only an even number of metal layers could be used owing to the PCB fabrication process), the possible source of parasitic coupling is restricted to couplings between bonding wires and on-chip parasitic couplings. The ground planes ensure a high isolation between PCB signal tracks.

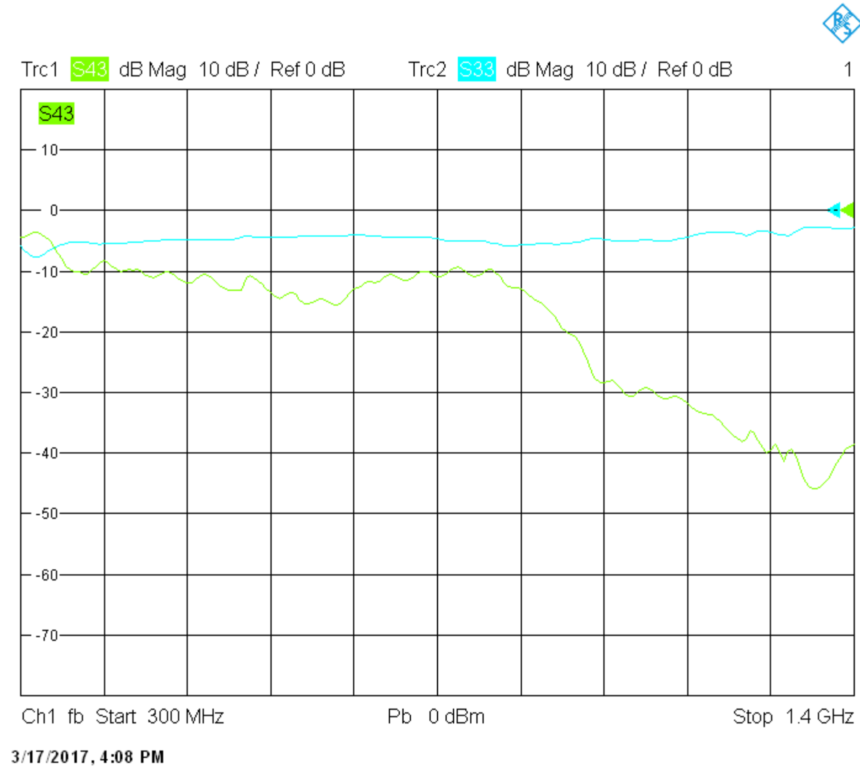


Figure 7.6. Output (green) versus input (blue) and frequency (external base inductor).

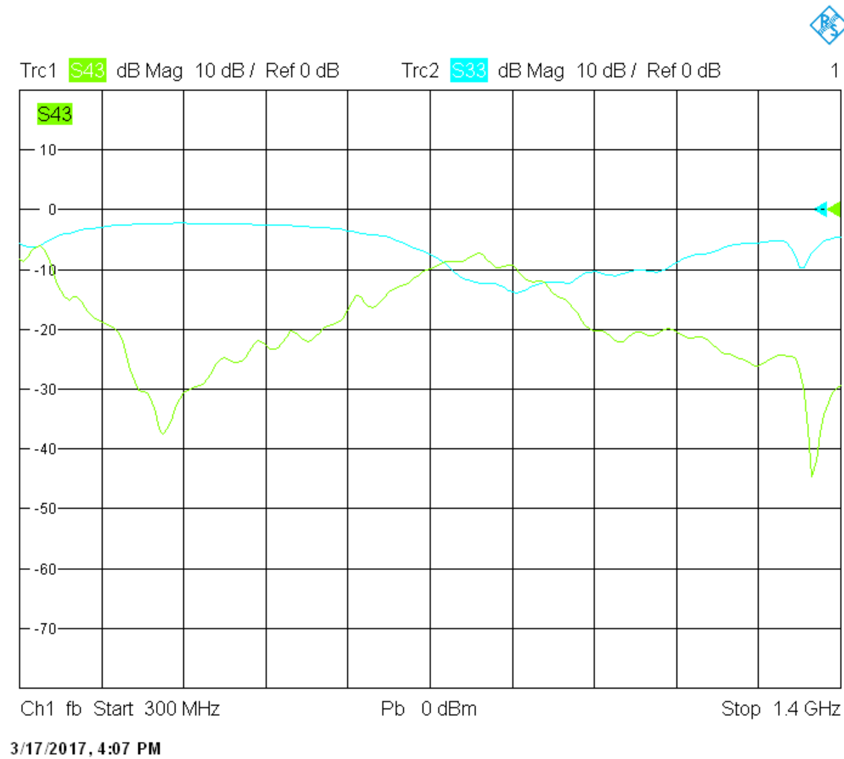


Figure 7.7. Output (green) versus input (blue) and frequency (internal base inductor).

A QFN package was desired but since it was unavailable, a 24-pin DIL package was used as an alternative, leading to long bonding wires because of the small size of the chip and the large size of the DIL package. A photo of the chip with bonding wires is shown in Figure 7.8, where the GND wire is the top left, the SIG_IN wire is second from the top on the left and the SIG_OUT wire, not shown here, is expected to be the topmost right wire. Packaging choice was also a function of the MPW approach and the accommodation of other projects.

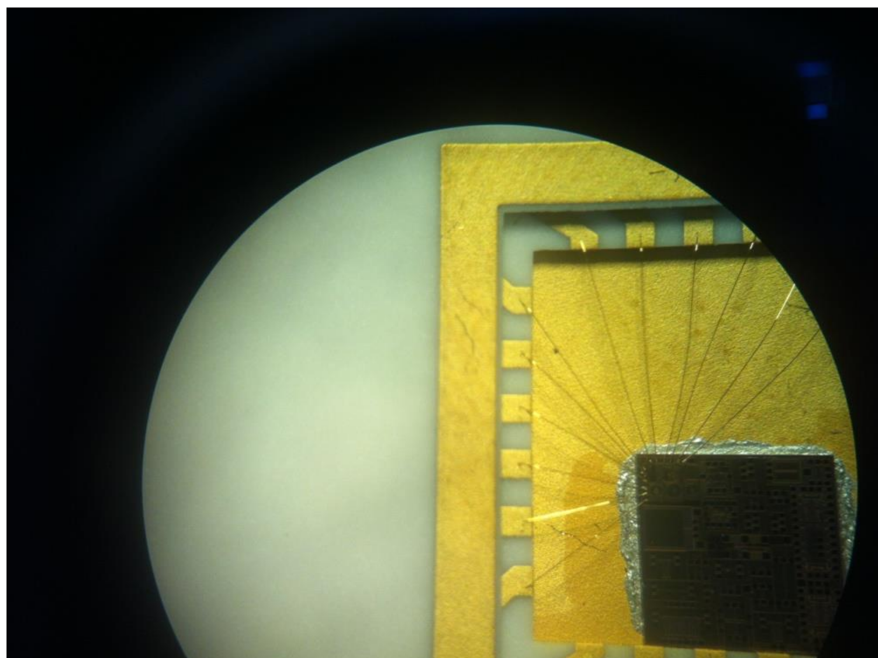


Figure 7.8. Chip and bonding wires.

The size of the chip being of 4 mm × 4mm, the length of the bonding wires from the top is more than 4 mm. The fifth wire from the top on the left side is the second GND bonding wire. Its length is close to 2 mm. The combined inductance of the GND bonding wires is expected to be close to 1.5 nH.

Substrate effects can create feedback paths between components implemented on the same Si substrate that can affect the gain, as indicated in Chapter 2. The couplings between the signal output and input pins of the packaged LNA due to on-chip parasitic couplings can be represented in Figure 7.9.

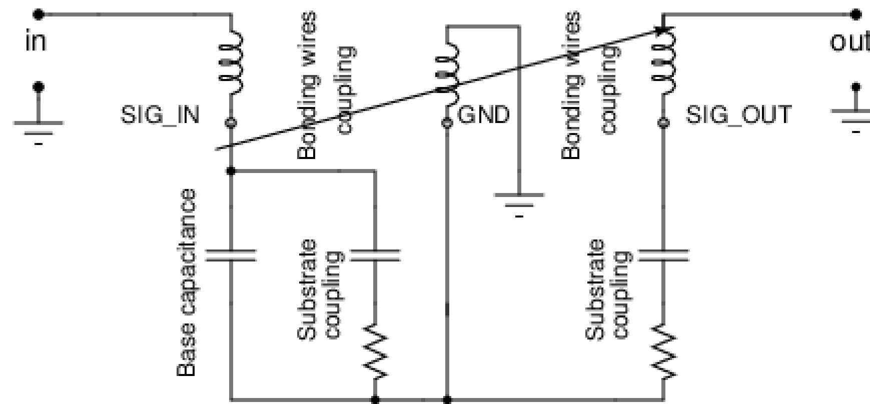


Figure 7.9. Couplings between the output and the input of the IC.

The circuit in Figure 7.9 allows explaining the presence of an output signal at the output of the LNA without power supply. The same circuit may also provide justification to some of the signal attenuation measured when the DUT is powered: the inductance of the ground bonding wire may create a negative feedback that decreases the gain.

7.4 TESTS FOR DEBUGGING

It is desired to identify the origin of the parasitic couplings between the output and the input of the DUT and the causes of signal attenuation. Tests that can be performed for these purposes are selected depending on their feasibility (e.g. the tests on mutual impedance couplings between bonding wires are excluded because they are difficult to perform), the availability of access to test points and the impact on gain. Tests performed are intended to identify issues that may originate from the PCB and from the chip.

7.4.1 PCB issues

- Input signal attenuation could possibly be caused by C_9, L_5 and L_6 that may operate as a band-pass filter.
- No issues related to the parasitic coupling between the output and input of the DUT were identified.

7.4.2 Prototyping issues

The distributed effects due to layout tracks have been neglected during the layout because the minimum wavelength of the input signal more than 200 times the size of the IC (1 mm × 1 mm, BiCMOS 0.130 nm technology). Access to some critical nodes, such as the collector of Q_2 and the gate of M_1, is not available because the number of pins was limited. Hence, the output matching circuit comprising L_2, C_2, L_3, C_3 cannot be tested; nor can the biasing of M_1, used in the circuit as an active resistor. The lack of access to such nodes stresses the importance of design for testability prevalent in digital design. Although digital design methodologies such as the so-called boundary scan can be extended to mixed-signal circuits, there are no general test methodologies for analog design. In addition, the testability of analog circuits may increase the complexity of the design and the size of the chip significantly, depending on the operating frequency. Performance issues that can be tested are:

- Feedback due to GND bonding wires
- Gain of Q_1
- Impact of C_1 and L_7 to gain.

7.4.3 Tests

Tests that can be performed for better understanding of performance issues listed in Sections 7.4.1 and 7.4.2 are described below:

- Input signal attenuation possibly due to C_9, L_5 and L_6, on the PCB. The DUT is powered. A low-frequency signal (60 MHz, 150 mV p-p) generated by the Rohde & Schwarz SME03 is applied to the SMA input of the PCB. A high-impedance RF probe is used to compare the signal level at the input SMA connector centre pin to the level of the signal at the SIG_IN pin of the LNA package using the HP 54503A oscilloscope. Because the peak-to-peak value remains 150 mV, it is concluded that there is no attenuation due to C_9 and L_6 for a signal of 60 MHz or higher.

- Measurement of the output signal (without DC power) using an input signal provided by a test probe at SIG_IN, a ground probe at GND directly on the chip, a test probe for the output signal at SIG_OUT and an oscilloscope. To reduce the effects of parasitic signals due to the probes, a signal with a frequency of 300 MHz and a level of -20 dBm is desired. This measurement, intended to verify if the coupling between the output and the input was mainly due to the chip, could not be carried out because of the unavailability of microscopic probes that could be used on bonded pads. Measurements done entailed providing a 210 MHz signal to the SMA input connector. An output signal of -72 dBm was found at the output when the input signal was equal to -22 dBm. When DC power is applied to the DUT, the level of the output signal becomes -58.9 dBm, which indicates a gain of 13 dB.

- Output attenuation possibly due to the feedback caused by the ground bonding wires on the pad GND. The measurement of the feedback signal can be done with a high-impedance microscopic RF probe and an oscilloscope to measure the amplitude of the signal on GND pads on the chip. If such a signal exists, it contributes to the deterioration of the gain. The -20 dBm input signal is provided by a 300 MHz signal generator connected to the input SMA connector.

- Measurement of the RF signal gain due to Q_1. The voltage gain of the common-emitter transistor of a cascode amplifier is less than unity. This measurement allows verifying if the input signal is present at the collector of Q_1 and if its attenuation is significant. The measurement is done by an oscilloscope and a high-impedance RF probe on the pin CHOKE_1 of the packaged IC. A peak-to-peak voltage of 70 mV at 60 MHz is measured on CHOKE_1 for an input signal of 150 mV, indicating significant attenuation. The attenuation may originate from the emitter inductor and the ground bonding wire.

- Measurement of signal attenuation due to C_1 and to the choke L_7. This measurement is performed by a high-impedance RF probe on the pin CHOKE_2 of the packaged IC and an oscilloscope. The levels of the signals at CHOKE_2 and CHOKE_1 are compared. A large attenuation will indicate a significant cause for gain loss.

- Measurement of the DUT output signal versus the input signal. The DUT is powered (2.2 V) and a network analyser is used for the measurements.

7.5 CONCLUSION

The bias values measured (base voltage and collector current) were aligned to simulated values. However, two major issues were found and NF measurements could not be performed.

In the absence of DC power, a coupling between the output and the input of the DUT was found. The coupling could have originated from bonding wires and substrate couplings. The impact of capacitive and mutual inductance couplings between bonding wires can be reduced by using an appropriate QFN chip package. Substrate couplings can be reduced by ensuring that the substrate is grounded and that minority carriers are not injected into the substrate owing to a faulty biasing.

The DUT showed gain, but much more attenuation, which cancelled the gain. It was identified that the attenuation was caused by the chip rather than the PCB. Possible causes of signal attenuation were investigated. Although the signal voltage at the collector of Q_1 was attenuated, such attenuation cannot explain by itself the large attenuation at the output of the DUT. It was verified that the attenuation was not due to C_1 and L_7. The possibility of attenuation due to an opening in the output matching circuit could not be excluded. In addition, an attenuation that might be caused by coupling between bonding wires was excluded in view of the low operating frequency of the DUT.

It appeared then that two causes of gain loss remained possible: layout issues and a signal short due to the transistor M_1. Because of the limitation of the number of pins available and the duration of the cycle of the submission of the layout for fabrication (one year), the once-off MOSIS prototyping sponsorship, the design for testability approach was not taken. It is then critical to have the main functionalities of the IC available after the first fabrication iteration: this can be achieved for future designs by LVS verification.

CHAPTER 8 CONCLUSION AND FUTURE WORK

8.1 CONCLUSION

This thesis has proposed a design methodology for highly sensitive wideband SiGe HBT-based LNAs. The methodology, which can also be applied to bipolar junction transistors, is process-independent and is based on a modified cascode configuration, identified as the state-of-the-art LNA topology owing mainly to the possibility of simultaneous noise and impedance matching, its high isolation between the output and the input and the reduction of the Miller effect.

The analysis of the noise performance of the cascode LNA is based on the two-port noise model. The four noise parameters (F_{min}, R_n, G_{sopt}, $B_{sopt,}$) of the CE transistor are expressed as functions of the parameters of its small-signal model. The expression of F_{min} allows one to determine that there is an emitter current density J_{opt} for which F_{min} is minimal, which corresponds to the minimum achievable NF of the CE BJT or SiGe HBT. It was also shown that F_{min} increases with frequency and is directly related to the emitter width $w_{e,}$ but unrelated to the emitter length l_e for on-chip transistors. The expression of R_{sopt}, where $R_{sopt} = \Re\{Z_{sopt}\}$ with $Z_{sopt} = 1/Y_{sopt}$ and $Y_{sopt} = G_{sopt} + jB_{sopt}$, shows that R_{sopt} is inversely proportional to l_e. It was shown that, when identical transistors are connected in parallel, F_{min} is invariant but R_{sopt} is inversely proportional to the number of parallel transistors n. Therefore, noise matching conditions for the CE could be achieved by varying l_e or n, depending on the operating frequency, without increasing F_{min}.

Narrow-band impedance matching was achieved by the addition of an emitter inductor L_E and a base inductor L_B to the CE transistor. It was shown that the impact of L_E and L_B on the noise matching condition could be neglected; hence the findings of the analysis could be extended to the IDCE topology. Furthermore, it was shown that these findings could be extended to the cascode topology. The increase in the bandwidth of the LNA was investigated and it was found that most traditional wideband impedance matching techniques deteriorate the NF. Wideband impedance matching was achieved by the addition of a capacitor between the collector and the emitter of the cascode pair, which resulted in two coupled tuned circuits and increased the bandwidth. The impact on the NF was negligible.

It was shown that the NF of the LNA could be close to the minimum NF achievable at the high end of the operating frequency because the SiGe HBTs were biased at an emitter current density of J_{opt} corresponding to minimum noise and the number of additional on-chip components for noise and impedance matching were reduced to the strict minimum. Output matching was performed by a modified fourth-order Butterworth approximation. A MATLAB™ script was used to optimise the transfer of power from the cascode to a 50 Ω load through the output matching network.

A design methodology was derived from the findings of this research and the methodology was used to design a prototype. Corner and MC simulations were done in order to identify changes in performance due to process variations and device mismatches. The layout was guided by the optimisation of the NF and a PCB housing two LNAs was fabricated for measurements.

8.2 CONTRIBUTION

The dependence of the NF on the operating frequency, transistor biasing, sizing and paralleling was developed and used to propose a design methodology that achieves NF that is close to the minimum achievable for a single transistor for the semiconductor process of fabrication. A bandwidth extension technique for a cascode SiGe HBT based amplifier

with minimum impact on NF was developed. Finally, an output broadband matching technique was proposed. The proposed methodology allows the design of a wideband LNA with an NF close to the minimum achievable one. Such a single-ended LNA is cost-effective, can achieve a sub-1 dB NF at room temperature depending on the fabrication process, and can be used in applications for radio astronomy, such as the SKA.

8.3 FUTURE WORK

The initial objective of this thesis was to achieve a sub-1 dB NF using a fully integrated differential LNA. However, it was found that on-chip inductors, especially the base inductor, could be a significant impairment to the noise performance. Hence, an external high Q base inductor was required. In addition, a single-ended LNA was desired instead of a differential LNA because of high losses in on-chip inductors and baluns and the lack of standard equipment for NF measurement for differential RF amplifiers. Because the noise performance of active devices is improved by their scaling, it is anticipated that the NF of the LNA will naturally improve when using 90 nm or 55 nm SiGe HBT technologies, such as the GlobalFoundries 90 nm SiGe HBT or the BiCMOS055 55 nm from STMicroelectronics. The performance of the LNA can also improve significantly when inductors with double metal layers are used. It is expected that using the fastest SiGe HBT process (BiCMOS055) and inductors with double metal layers, a fully integrated differential sub-1 dB LNA will be achieved. Such inductors can be realised using CAD tools such as CST microwave studio and imported in the layout, when they are not available in the semiconductor process design kit.

Although corners and MC analysis were performed, their results were not used to improve the performance of the LNA. The dependence of performance on process variations and mismatches can be reduced by sensitivity analysis. For the sake of simplicity, the main functional blocks of the LNA were analysed and optimised separately, therefore possible interactions between them could not be analysed. Such interaction can be analysed in future work by modelling the complete LNA circuitry with MATLAB™.

The main design parameters used were the NF, S_{11} and S_{22}. Other performance metrics such as the gain, linearity and stability were simulated and found to be acceptable. The question arises how the most appropriate trade-offs between performance metrics can be achieved. A multi-objective optimisation algorithm can improve the performance of the LNA and provide the desired trade-offs between the performance metrics. Such optimisation can be performed by the Genetic Algorithm using a MATLAB™ script.

REFERENCES

[1] A. Bimana and S. Sinha, “Impact of SiGe parameters to the performance of LNAs for highly sensitive SKA receivers,” 23th Conference Radioelektronika Pardubice, Czech Republic (2013), pp. 50-54.

[2] A. Bimana and S. Sinha, "Increasing the bandwidth of a SiGe HBT LNA with Minimum Impact on Noise Figure," *Microwave and Optical Technology Letters* (Wiley), Vol. 58, No. 8, Aug. 2016, pp. 1937-1944.

[3] P. Leroux, J. Janssens, and M. Steyaert, “A 0.8-dB NF ESD-protected 9-mW CMOS LNA operating at 1.23 GHz,” *IEEE J. Solid-State Circuits*, vol. 37, pp. 760–765, Jun. 2002.

[4] Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, “The impact of scaling down to deep submicron on CMOS RF circuits,” *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1023–1035, Jul. 1998.

[5] S. Bhaumik, M. Roy, and D. George, “Comparative Study of HEMTs for LNAs in Square Kilometre Array Telescope,” *2011 IEEE MTT-S Int. Microw. Symp. Dig.,* pp. 1-4, Jun. 2011.

[6] P. Dewdney, P. Hall, R. Schilizzi, and T. Lazio, “The square kilometre array,” in *Proceedings of the IEEE*, vol. 97, no. 8, pp. 1482–1496, Aug. 2009.

[7] P.J. Hall, “The Square Kilometer Array: An international engineering perspective,” *Experimental Astronomy*, vol. 17, no. 1-3, pp. 5-16, Jun. 2004.

[8] L. Belostotski and J.W. Haslett, “Sub-0.2 dB Noise Figure Wideband Room-Temperature CMOS LNA with Non-50 Ω Signal-Source Impedance,” *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2492-2502, Nov. 2007.

[9] S. Bhaumik and D. George, “Review of Square Kilometre Array LNA technologies and topologies,” in *Widefield science and technology for the SKA*, Château de Limelette, Belgium, Nov. 2009.

[10] B. Godara and A. Fabre, "State of the Art for Differential Circuits in Wireless Transceivers; A New Wideband Active Balun in SiGe BiCMOS Technology," Turkish Journal Electrical Engineering and Computer Sciences, vol. 14, no. 3, pp. 355-386, 2006.

[11] B. Heydari, M. Bohsali, E. Adabi, and A.M. Niknejad, "Low-power mm-wave components up to 104 GHz in 90 nm CMOS," in *ISSCC Dig. Tech. Papers,* San Francisco, Feb. 2007, pp. 200–201.

[12] L. Belostotski and J.W. Haslett, "Wide Band Room Temperature 0.35-dB Noise Figure LNA in 90-nm Bulk CMOS," in *Proc. 2007 IEEE Radio and Wireless Symp*., Long Beach, CA, Jan. 2007, pp. 221-224.

[13] S. Weinreb, J.C. Bardin and H. Mani, "Design of cryogenic SiGe low-noise amplifiers," *IEEE Trans. Microwave Theory Tech.,* vol. 55, pp. 2306-2312, Nov. 2007.

[14] J.C. Bardin and S. Weinreb, "A 0.1-5 GHz Cryogenic SiGe MMIC LNA," *IEEE Microwave and Wireless Comp. Lett.*, vol. 19, no. 6, pp. 407-409, Jun. 2009.

[15] Z. Hamaizia, N. Sengouga, M. Missous, and M.C.E. Yagoub, "A 0.4 dB noise figure wideband low-noise amplifier using a novel InGAs/InAlAs/InP device," *Materials Science in Semiconductor Processing*, vol. 14, no. 2, pp. 89-93, June 2011.

[16] M. Panahi, S. Bhaumik and D. George, "Power-efficient ultra wideband LNAs for the world's largest radio telescope," *Experimental Astronomy*, vol. 38, no. 3, pp. 359-379, December 2014.

[17] C. Carilli and S. Rawlings, Eds., *Science with the Square Kilometre Array*. Amsterdam, The Netherlands: Elsevier, 2004.

[18] R.T. Schilizzi. (2011, Jan.). SKA project execution plan, Pre-Construction Phase for the Square Kilometre Array. SKA project document MGT-001.005.005-MP-001(K).[Online].Available: https://www.skatelescope.org/uploaded/38221_SKA_Project_Execution_Plan.pdf.

[19] M.A. Garrett, J.M. Cordes, D. De Boer, J.L. Jonas, S. Rawlings, and R.T. Schilizzi. (2010). Concept Design for SKA Phase 1 (SKA1). SKA Memo Series 125, SPDO.

[20] D.G. York, O. Gingerich, S.N. Zhang, *The Astronomy Revolution: 400 Years of Exploring the Cosmos*. CRC Press, New York, 2012.

[21] J.G. Bij De Vaate, R.H. Witvers, and E.E.M. Woestenburg, “Front-end Integration Requirements for the Square Array Radio Telescope,” in *IEEE CSICS*, Oct. 2010.

[22] L. Belostotski, “Wide-Band CMOS Low Noise Amplifier for the Square Kilometer Array Radio Telescope,” Ph.D. Thesis, University of Calgary, Department of Electrical and Computer Engineering, Sep. 2007.

[23] B.F. Burke and F. Graham-Smith, *An Introduction to Radio Astronomy*. Cambridge: Cambridge University Press, 1997, p. 28.

[24] K. Rohlfs, *Tools of Radio Astronomy*. Berlin: Springer-Verlag, 1986, pp. 132-136, 142, 146.

[25] J.D. Kraus, *Radio Astronomy*. New York, NY: McGraw-Hill Book Company, 1966, pp. 258, 223.

[26] P.C. Crane and P.J. Napier, “Sensitivity in Synthesis Imaging in Radio Astronomy,” in *Astronomical Society of the Pacific Conference Series*, vol. 3. San Francisco, CA: Astronomical Society of the Pacific, 1989, pp. 139-165.

[27] A.P. Chippendale, "Technology Issues for square kilometre array receiver design," in *Proc. Workshop on Applications of Radio Science (WARS 2002)*, Leura, Feb. 2002.

[28] A.R. Taylor and R. Braun. (1999). *Science with the Square Kilometer Array*. Calgary, Alberta: University of Calgary. [Online]. pp. 9. Available: https://www.skatelescope.org/uploaded/55267_scienceSKA.pdf.

[29] A.A. Penzias and R.W. Wilson, “Determination of the Microwave Spectrum of Galactic Radiation,” in *Astrophysical Journal*, vol. 146, pp. 666.

[30] Myriad Data Reduction Software. [Online]. Available: http://www.atnf.csiro.au/computing/software/miriad/.

[31] J.D. Cressler, “SiGe HBT Technology: A New Contender for Si-Based RF and Microwave Circuit Applications”, *IEEE Transactions on microwave theory and techniques*, vol. 46, no. 5, May 1998.

[32] S.A. Jackson, “RF design of a wideband CMOS integrated receiver for phased array applications,” *Experimental Astronomy*, vol. 17, no. 1-3, pp. 201-210, Jun. 2004.

[33] J.G.B. De Vaate, “RF-IC Developments for Wide Band Phased Array Systems,” in *Perspectives on Radio Astronomy: Technologies for Large Antenna Arrays*, Netherlands Foundation for Research in Astronomy, pp. 143-147, Apr. 1999.

[34] J. Janssens and H. Steyaert, "MOS noise performance under impedance matching constraints," *Electron. Lett.,* vol. 35, no. 15, pp. 1278–1280, Jul. 1999.

[35] O. Garcia-Perez, "FIDA3: A Novel Active Array Design for the Mid-Frequency Range of the SKA," 2010, in *Proc. Wide Field Science and Technology for the SKA*, pp. 1-4, Apr. 2010.

[36] R. Shaw, S. Weinreb, J. Bardin, H. Mani, and G. Jones, "Matched wideband low-noise amplifiers for radio astronomy," *Review of Scientific Instruments*, vol. 80, no. 4, p. 044702, 2009. [Online]. Available: http://linl.aip.org/link/?RSI/80/044702/1.

[37] P. J. Hall, "An SKA Engineering Overview*," White Papers by the Task Forces of the International Engineering Working Group*, Nov. 2006.

[38] J.D. Pandian, L. Baker, and S. Weinreb, "Low-noise 6-8 GHz receiver," *IEEE Microwave Magazine*, vol. 7, no. 6, pp. 74-84, Dec. 2006.

[39] A.A. Abidi and J.C. Leete, "De-embedding the noise figure of differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 882-885, Jun. 1999.

[40] G. Girlando and G. Palmisano, "Noise figure and impedance matching in RF cascode amplifiers," *IEEE Transactions on Circuits and Systems-II, Analog and Digital Signal Processing*, vol. 46, no. 11, pp.1388–1396, Nov. 1999.

[41] Q. Huang, P. Orsatti, and F. Piazza, "GSM transceiver front-end circuits in 0.25 μm CMOS," *IEEE J. of Solid-State Circuits*, vol. 34, no. 3, pp.292–303, Mar. 1999.

[42] E.A.M. Klumerink, B. Nauta, and F. Bruccoleri, "Thermal Noise Cancelling in LNAs: A Review," in *Proceedings of the 2004 Asia-Pacific Microwave Conference*. University of Delhi South Campus, 2004.

[43] S. Hazenboom, T.S. Fiez, and K. Mayaram, "A comparison of substrate noise coupling in lightly and heavily doped CMOS processes for 2.4 GHz LNAs," *IEEE J. of Solid-State Circuits*, vol. 41, no. 3, pp. 574–587, Mar. 2006.

[44] D.J. Cassan and J.R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18-μm CMOS," *IEEE J. of Solid-State Circuits*, vol. 38, no. 3, pp. 427–435, Mar. 2003.

[45] B. Godara and A. Fabre, "Low-noise amplifiers in wireless communications: state of the art, two new wideband all-active LNAs in SiGe-BiCMOS," *Analog Integr Circ Sig Process.*, vol. 60, no. 3, pp. 169-193, Nov. 2009.

[46] F. Bruccoleri, E. Klumperink and B. Nauta, "Wideband CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. of Solid-State Circuits*, vol. 39, no. 2, pp. 275-282, Feb 2004.

[47] S. P. Voinigescu, T. O. Dickson, T. Chalvatzis, A. Hazneci, E. Laskin, R. Beerkens and I. Khalid, "Algorithmic design methodologies and design porting of wireline transceiver IC building blocks between technology nodes*," in IEEE Custom Integrated* Cir*cuits Conf.,* Sep. 2005, pp. 111–118.

[48] J. Borremans, P. Wambacq, and D. Linten, "An ESD-protected DC-to-6 GHz 9.7 mW LNA in 90 nm digital CMOS," *in IEEE International Solid-State Circuits Conf*., San Francisco, Feb. 2007, pp. 422–423.

[49] R. Ramzan, S. Andersson, J. Dabrowski and C. Svensson, "A 1.4 V 25 mW inductorless wideband LNA in 0.13μm CMOS," in *IEEE International Solid-State Circuits Conf.*, San Francisco, Feb. 2007, pp. 424–425.

[50] A. Bevilacqua and A.M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1–10.6 GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259-2268, Dec. 2004.

[51] B. Machiels, "Distributed amplification in CMOS," Ph.D. Thesis, Catholic University of Leuven, Department of Electrotechnics, July 2012.

[52] A. Kopa, "Low Noise distributed amplifiers in broadband communication systems," Ph.D. Thesis, Cornell University, Department of Electrical and Computer Engineering, January 2011.

[53] J. Kaukovuori, M. Kaltiokallio, and J. Ryynanen, "Analysis and design of common-gate low-noise amplifier for wideband applications," *Int. J. Circ. Theor. Appl.,* vol. 37, no. 2, pp. 257-281, Aug. 2008.

[54] F. Bruccoleri, E. Klumperink, and B. Nauta, "Noise cancelling in wideband CMOS LNAs," *in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers,* vol. 45*,* San Francisco, CA, Feb. 2002, pp. 406–407.

[55] P. Andreani and H. Sjöland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Trans. Circuits Syst.*, vol. 48, pp. 835–841, Sept. 2001.

[56] L. Belostotski, J. Haslett, and B. Veidt, "Wide-band CMOS low noise amplifier for applications in radio astronomy," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2006, pp. 1347–1350.

[57] Y.-T. Lin, H.-C. Chen, T. Wang, Y.-S. Lin, and S.-S. Lu, “3-10-GHz Ultra-Wideband Low-Noise Amplifier Utilizing Miller Effect and Inductive Shunt-Shunt feedback Technique,” *IEEE Transactions on Microwave theory and Techniques,* vol. 55, no. 9, Sept 2007.

[58] R. Chi-Hsi Li, *RF Circuit Design*. Hoboken, N.J: John Wiley & Sons, Inc., 2009.

[59] U. Tietze, Ch. Schenk, and E. Gramm, *Electronic Circuits: Handbook for Design and Applications*. Springer, Berlin, 2008.

[60] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1997.

[61] A.A. Muller, E. Sanabria-Codesal, A. Moldoveanu, V. Asavei, P. Soto, V.E. Boria, and S. Lucyszyn, “Appollonius unilateral transducer constant power gain circles on 3D Smith charts,” *IET Electron. Lett.,* vol. 50, no. 21, pp. 1531-1533, Oct. 2014.

[62] A.A. Muller, E. Sanabria-Codesal, A. Moldoveanu, V. Asavei, and S. Lucyszyn, “Extended capabilities of the 3-D Smith chart with group delay and resonator quality,” *IEEE Transactions on Microwave Theory and Techniques,* vol. 65, no. 1, pp. 10-19, 2017.

[63] M. van der Heijden, “RF Amplifier Design Techniques for Linearity and Range,” PhD thesis, Delft university of technology, May 2005.

[64] S. Seth, “Using complementary silicon-germanium transistors for design of high-performance RF front-ends,” PhD thesis, Georgia Institute of Technology, Aug. 2012.

[65] N. Kinayman, A. Jenkins, D. Helms, and I. Gresham, “Design of 24 GHz SiGe HBT balanced power amplifier for system-on-a-chip ultra-wideband applications,” *Digest of Papers IEEE Radio Frequency Integrated Circuits Symposium*, no. 1, pp. 91—94, Jun. 2005.

[66] J. Bardin, “Silicon-Germanium Heterojunction Bipolar Transistors for Extremely Low-Noise Applications,” Ph.D. Thesis, California Institute of Technology, May 2009.

[67] L. Moura and I. Darwazeh, *Introduction to Linear Circuit Analysis and Modelling*. Newnes: An imprint of Elsevier, 2005.

[68] G. Vasilescu, *Electronic Noise and Interfering Signals: Principles and Applications*. Heidelberg, Germany: Springer-Verlag, 2005.

[69] H.A. Tilmans, W.D. Raedt, and E. Beyne, “MEMS for wireless communications: from RF-MEMS components to RF-MEMS-Sip,” *Journal of Micromechanics and Microengineering*, vol 13, pp. 139-163, 2003.

[70] I.J. Bahl, *Fundamental of RF and Microwave Transistor Amplifiers*. Hoboken, NJ: Wiley, 2009.

[71] M. Golio and J. Golio, *RF and Microwave Passive and Active Technologies*. Taylor and Francis Group, Boca Raton: Taylor and Francis Group, 2008.

[72] V. Zhurbenko, *Advanced Microwave Circuits and Systems*. CC BY-NC-SA, ISBN 978-953-307-087-2, Apr. 2010.

[73] X. Duo, L.-R. Zheng, M. Ismail, and H. Tenhunen, "On-chip versus off-chip passives analysis in radio and mixed-signal system-on-package design," in *Proceeding of the Sixth IEEE CPMT Conference on High Density Microsystem Design and Packaging and Component Failure Analysis, 2004. HDP '04.*, Hong Kong, China, pp. 109-116, June 2004.

[74] T.-S. Horng, K.-C. Peng, J.-K. Jau, and Y.-S. Tsai, “S-parameter formulation of quality factor for a spiral inductor in generalized two-port configuration,” *IEEE Trans. Microw. Theory Tech.,* vol. 51, no. 11, pp. 2197-2202, Nov. 2003.

[75] F. Ellinger, *Radio Frequency Integrated Circuits and Technologies*. New York: Springer-Verlag, 2007.

[76] C. P. Yue, C.R.J. Lau, T.H. Lee, and S.S. Wong, “A physical model for planar spiral inductors on silicon,” in *IEDM Tech. Dig*., pp. 155-158, Dec. 1996.

[77] B. Leung, *VLSI forWireless Communication*. Upper Saddle River, NJ: Prentice-Hall, 2002.

[78] N. Donuwan and L. Belostotski, "Evaluation of packaging options for very low noise amplifiers," In *Electrical and Computer Engineering (CCECE), 2010 23rd Canadian Conference on*, pp. 1-4. IEEE, 2010.

[79] S.P. Voinigescu, M.C. Maliepaard, J.L. Showell, G.E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D. Harame, “A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise Amplifier Design,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 1430–1438, Sept. 1997.

[80] D. Shaeffer and T. Lee, “A 1.5 V, 1.5 GHz CMOS low noise amplifier,” *J. Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.

[81] T.K. Nguyen, C.H. Kim, M.S. Yang, and S. G. Lee, “CMOS Low-Noise Amplifier DesignOptimization Techniques”, *IEEE Trans. Microwave Theory and Techniques*, vol. 52, No.5, pp. 1433-1442, 2004.

[82] J. Goo, H. Ahn, D. J. Ladwig, Z. Yu, T.H. Lee, and R. W. Dutton, “A noise optimization technique for integrated low-noise amplifiers,” IEEE J. Solid-State Circuits, vol. 37, pp. 994–1002, Aug. 2002.

[83] B.W. Min and G.M. Rebeiz, “Ka-Band SiGe HBT Low Noise Amplifier Design for Simultaneous Noise and Input Power Matching,” *IEEE Microwave and Wireless Components Letters*, vol. 17, No. 12, 2007.

[84] G. Vandersteen, L. Bos, and P. Dobrovolny, “Scaling Friendly Design Methodology for Inductively Degenerated RF Low-Noise Amplifiers”, in *Proceedings of the 2nd European Microwave Integrated Circuits Conference*, pp. 223-226, 2007.

[85] IBM Microelectronics, “BiCMOS8HP Design Manual,” 19 August 2013.

[86] Anon, 2011. MOSIS Integrated Circuit Fabrication Service [Online]. Available from: http://www.mosis.com/ [Accessed: 18 January 2016].

[87] H. Hillbrand and P. H. Russer, “An Efficient Method for Computer Aided Noise Analysis of Linear Amplifier Networks,” *IEEE Trans. Circuits and Syst.*, vol. CAS-23, pp. 235–238, Apr. 1976.

[88] A. Grebennikov, *RF and Microwave Transmitter Design*. Hoboken, N.J: John Wiley & Sons, 2011.

[89] H.-Y. Chen, K.-M. Chen, G.-W. Huang, and C.-Y. Chang, “Small-signal modelling of SiGe HBTs using direct parameter-extraction method,” *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2287-2295, Sep. 2006.

[90] J. Cressler and G. Niu, Silicon-Germanium Heterojunction Bipolar Transistors. Boston, MA: Artech House, Mar. 2003.

[91] K. H. K. Yau, “Noise modelling of silicon germanium heterojunction bipolar transistors at millimetre-wave frequencies,” Master of Applied Science Thesis, University of Toronto, 2006.

[92] F. Jun, “Small-signal model parameter extraction for microwave SiGe HBTs based on Y- and Z- parameter characterization,” *Journal of Semiconductors*, vol. 30, no. 8, Aug. 2009.

[93] K. Lee, K. Choi, S.-H. Kook, D.-H. Cho, K.-W. Park, and B. Kim, “Direct parameter extraction of SiGe HBTs for the VBIC bipolar compact model,” *IEEE Trans. Electron Devices*, vol. 52, no. 3, pp. 375-384, Mar. 2005.

[94] A. Pawlak, S. Lehmann, P. Sakalas, J. Krause, K. Aufinger, B. Ardouin, and M. Schroter, “SiGe HBT modeling for mm-wave circuit design,” in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, pp. 149-156, Oct. 2015.

[95] M. Sotoodeh, L. Sozzi, A. Vinay, A. Khalid, Z. Hu, A. Rezazadeh, and R. Mennozzi, “Stepping toward standard methods of small-signal parameter extraction for HBT’s,” *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 1139–1151, Jun. 2000.

[96] X. Xing, “Small-Signal Modeling and Microwave Noise Characterization of InGaP/GaAs HBTs,” Master of Science in Electrical Engineering thesis, University of Notre Dame, 2007.

[97] L. C. N. de Vreede, H. C. de Graaff, A. M. Hurkx, J. L. Tauritz, and R. F. Baets, “A figure of merit for the high-frequency noise behaviour of bipolar transistors,” *IEEE J. Solid-State Circuits*, vol. 29, pp. 1220–1226, Oct. 1994.

[98] P. Sakalas, J. Herricht, A. Chakravorty, and M. Schroter, “Compact modeling of high frequency correlated noise in HBTs,” in *Proc. Bipolar/BiCMOS Circuits Technol.* Meeting, pp. 1–4, 2006.

[99] N. Guofu, K. Xia, D. Sheridan, and S. Sweeney, "RF Noise Modeling in SiGe HBTs." In *AIP Conference Proceedings*, vol. 780, p. 247. IOP Institute of Physics Publishing, Ltd, 2005.

[100] L. Escotte, JP. Roux, and R. Plana “Noise modelling of microwave heterojunction bipolar transistors,” *IEEE Trans. Electron Devices*, vol. 42, no. 5, pp. 883-889, May. 1995.

[101] U. Basaran, N. Wieser, G. Feiler, and M. Berroth, “Small-signal and high-frequency noise modelling of SiGe HBTs,” *IEEE Trans. Microw. Theory Tech.* vol.53, no.3, pp. 919-928, Sep. 2005.

[102] M.M. Jahan, K.W. Liu, and A. F. M. Anwar, “Bias dependence of highfrequency noise in heterojunction bipolar transistors,” *IEEE Trans. Microw. Theory Tech.,* vol.51, no.3, pp.677-681, Mar. 2003.

[103] M. Rudolph, R. Doerner, L. Klapproth, and P. Heymann, “An HBT noise model valid up to transit frequency,” *IEEE Electron Device Lett.*, vol. 20. no. 1, pp. 24- 26, Jan. 1999.

[104] J. Gao, “Direct extraction of InP HBT noise parameters based on noise figure measurement system”, *IEEE Trans. Microw. Theory Tech*. vol. 53, no. 1, pp. 330-335, Jan 2005.

[105] J. Gao, X. Li, H. Wang, and G. Boeck, “Microwave noise modelling for InP-InGaAs HBTs,” *IEEE Trans. Microw. Theory Tech.,* vol. 52, no. 4, pp. 1264-1272, Apr. 2004.

[106] G. Niu, “Noise in SiGe HBT RF Technology: physics, modeling, and circuit implications,” *Proceedings of the IEEE*, vol. 93, no. 9. pp. 1583-1597, Sep. 2005.

[107] G. Dambrine, H. Happy, F. Danneville, and A. Cappy, “A new method for on wafer noise measurement,” *Microwave Theory and Techniques, IEEE Transactions on*, vol. 41, no. 3, pp. 375-381, Mar 1993.

[108] C.C. Hu, *Modern Semiconductor Devices for Integrated Circuits*. Englewood Cliffs, NJ: Prentice Hall, 2009.

[109] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. Fifth Edition, New York: Wiley, 2010.

[110] J. Rogers and C. Plett, *Radio Frequency Integrated Circuit Design Second Edition*. Norwood, MA: Artech House, ch. 4, pp. 87, 2010.

[111] O. Shana, I. Linscott, and L. Tyler, “Frequency-scalable SiGe bipolar RF front-end design” *IEEE J. Solid-State Circuits,* vol.36, pp. 888-895, Jun. 2001.

[112] J. Cressler, *Silicon Heterostructure Handbook.* London: Taylor and Francis, pp.446, 2006.

[113] W.M. Leach, Jr., “Fundamentals of low-noise analog circuit design,” *Proc. IEEE,* vol. 82, pp. 1515–1538, Oct. 1994.

[114] H.T. Friis, “Noise figure of radio receivers,” *Proc. IRE*, vol. 32, pp. 419-422, July 1944.

[115] K. Fong and R. Meyer, "High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages," *IEEE J. Solid-State Circuits*, vol. 33, pp. 548–555, Mar. 1998.

[116] B. Banerjee, "Development of Broadband Noise Models and Radio Frequency Integrated Circuits using Silicon Germanium HBTs," PhD thesis, Georgia Institute of Technology, Dec. 2006.

[117] S. Voinigescu and D. Neculoiu, "Noise in electronic receivers - Design problems," (in Romanian), Lecture notes, Polytechnic Institute of Bucharest, ch. 4: Design of Low-Noise Feedback Amplifiers, pp. 51–64, 1989.

[118] D.M.P. Smith and B.E.M. Woestenburg, "Technique for reduction of noise resistance in a balanced low-noise amplifier for beam-steering applications," *Int J. Microw. Wirel. Technol*, Cambridge University Press and the European Microwave Association, 2013.

[119] A. M. Niknejad, *Electromagnetics for High-Speed Analog and Digital Communication Circuits*. Cambridge Univ. Press, Cambridge, UK, 2007.

[120] T. Lee, *Planar Microwave Engineering: A Practical Guide to Theory, Measurement and Circuits*. Cambridge Univ. Press, Cambridge, UK, 2004.

[121] L. Besser, R. Gilmore, *Practical RF Circuit Design for Modern Wireless Systems*. Norwood, MA: Artech House, 2003.

[122] N. Wadefalk, A. Mellberg, I. Angelov, M. Barsky, S. Bui, E. Choumas, R. Grundbacher, E. Kollberg, R. Lai, N. Rorsman, P. Starski, D. Stenarson, J. Streit, and H. Zirath, "Cryogenic wide-band ultra-low-noise IF amplifiers operating at ultra-low DC power," *IEEE Trans. Microwave Theory Tech.*, vol. 51, pp. 1705–1711, 2003.

[123] R. Hu and M. S. C. Yang, "Investigation of different input-matching mechanisms used in wide-band LNA design," *Int. J. Infrared Millimeter Waves*, vol. 26, no. 2, pp. 221–245, Feb. 2005.

[124] K. Xia, "Improved RF noise modelling for silicon-germanium heterojunction bipolar transistors," PhD dissertation, Auburn University, Alabama, 2006.

[125] S. Mass, *Noise in Linear and nonlinear Circuits*. Boston: Artech House, Inc., 2005.

[126] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd Ed. New York: Cambridge University Press, 2004.

[127] M.T. Hsu, S.Y. Hsu, and Y.H. Lin, “Low-power CMOS LNA based on dual resistive-feedback structure with peaking inductor for wideband application,” *Int J. Microw. Wirel. Technol*, vol. 5, no. 1, pp. 65-70, 2013.

[128] L. Thede, *Practical Analog and Digital Filter Design*. Boston: Artech House Publishers, 2004.

[129] IBM Microelectronics, Design kit and Technology Training BiCMOS8HP V1210, September 2011.

[130] IBM Microelectronics, BiCMOS8HP Model Reference Guide, 24 July 2007.

[131] C.M. Grens, “A Comprehensive Study of Safe-Operating-Area, Biasing Constraints, and Breakdown in Advanced SiGe HBTs,” Msc Thesis, Georgia Institute of Technology, Aug 2007.

[132] T.K. Thrivikraman, "Analysis and Design of Low-Noise Amplifiers in Silicon-Germanium Hetrojunction Bipolar Technology for Radar and Communication Systems," Master of Science, Georgia Institute of Technology, 2007.

[133] H. A. Haus and R.B. Adler, “Optimum Noise Performance of Linear Amplifiers,” *Proceedings of the IRE 46*, no. 8, pp. 1517-1533, Aug. 1958.

[134] S. Winder, *Analog and Digital Filter Design, Second Edition*. Elsevier Science, 2002.

[135] D.E. Johnson, *Introduction to filter theory*. Englewood Cliffs, N.J., Prentice-Hall, 1976.

[136] T.R. Cuthbert, *Broadband direct-coupled and matching RF networks*. Greenwood Arkansas, TRCPEP Publications, 1999.

[137] L.P. Huelsmann, Active and Passive Analog Filter Design, New York: McGraw-Hill, 1993.

[138] J. Sturn, M. Groinig, and X. Xiang, “Tunable Balun Low-Noise Amplifier in 65 nm CMOS Technology,” *Radioengineering*, vol.23, no. 1, pp.319-327, April 2014.

[139] R. Forward and T. Cisco, “Electronically Cold Microwave Artificial Resistors,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 31, no. 1, pp. 45-50, 1983.

[140] E. Taniguchi, T. Ikushima, K. Itoh, and N. Suematsu, “A dual bias-feed circuit design for SiGe HBT low-noise linear amplifier,” *IEEE Microw. Theory Tech.*, vol. 51, no. 2, pp. 414-421, Feb. 2003.

[141] L. Bu, “Linearity and Interference Robustness Improvement Methods for Ultra-Wideband Cmos Rf Front-End Circuits,” PhD dissertation, The Ohio State University, 2008.

[142] P. R. Kinget, “Device Mismatch and Tradeoffs in the Design of Analog Circuits,” *IEEE Journal of Solid-State Circuits,* vol. 40, no. 6, pp. 1212-1215, 1990.

[143] A. Hastings, *The Art of Analog Layout, 2nd Edition*. Prentice Hall, 2006.

[144] F.-Y. Han, K.-C. Lu, T.-S. Horng, J. Lin, H.-H. Cheng, C.-T. Chiu, and C.-P. Hung, “Packaging effects on the figure of merit of a CMOS cascode low-noise amplifier: Flip-chip versus wire-bond,” in *IEEE MTTS International Microwave Symposium*, (Boston), pp. 601–604, 7–12 June 2009.

[145] H. Rothe and W. Dahlke, “Theory of noisy four poles,” *Proc. IRE*, vol. 44, no.6, pp. 811-818, Jun. 1956.

ADDENDUM A TWO-PORT NOISE MODEL

The NF of the amplifier is defined by $10\log_{10}(F)$ and is expressed in decibels (dB). The main sources of intrinsic noise in bipolar and in CMOS transistors are the thermal noise, the shot noise and the flicker noise or 1/*f* noise. The flicker noise is a low-frequency noise that can be neglected in the frequency range of the LNA that is the subject of this research. The noise model of the two-port transistor amplifier is represented in Figure A.1.

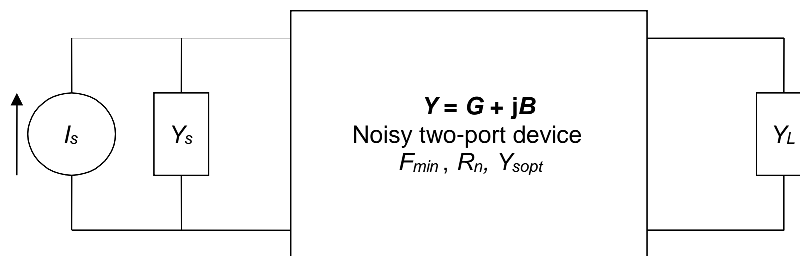


Figure A.1. Two-port noise model.

The two-port noisy amplifier is equivalent to a noiseless device with equivalent current and voltage noise sources reported to the input, as shown in Figure A.2. Such representation is convenient because it allows represention of all possible internal noise sources, which are generally distributed in a circuit, by only two noise sources. In addition, the representation allows one to evaluate the sensitivity of the amplifier and to describe its noise performance by four measurable parameters, as shown by the noise correlation matrix. The measurable parameters are the noise spectral power densities of the current and voltage noise sources at the input and the real and imaginary parts of the correlation of their spectral power densities.

The current and voltage noise sources represent the intrinsic noise of the amplifier and are expressed by the square of the RMS values of the equivalent input noise current ($\overline{i_n^2}$) and input noise voltage ($\overline{v_n^2}$) [145].

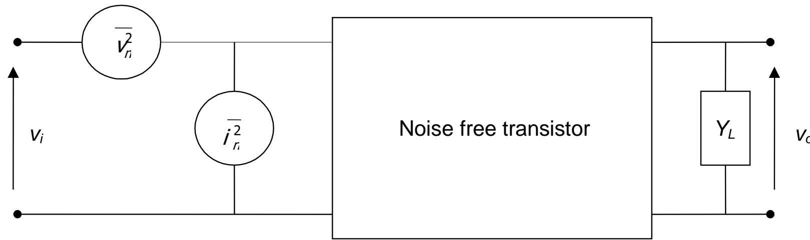


Figure A.2. Equivalent noise model of a transistor.

If $N(i_n,v_n)$ is the total intrinsic noise of the amplifier referred to the input, then

$$N_o = GN_i + GN(i_n, v_n) \tag{A.1}$$

After the substitution of (A.1) in (4.4), the noise factor can be expressed as follows:

$$F = \frac{S_i}{N_i}\frac{N_o}{S_o} = \frac{GN_i + GN(i_n, v_n)}{GN_i} = 1 + \frac{N(i_n, v_n)}{N_i} \tag{A.2}$$

The equivalent input referred voltage noise is given by

$$v_{eq} = v_n + Z_s i_n \tag{A.3}$$

where Z_s is the source impedance and $Z_s = \frac{1}{Y_s}$.

In general, v_n and i_n are correlated because they are derived from the same physical noise sources as shown in Figure A.2. In practice, the correlation is small [109] and, in order to quantify it, a technique used in noise analysis involving splitting a noise source in two components can be applied. Using this technique, the input referred current i_n can be split into two components: a component i_c that is correlated to the input referred noise voltage v_n and a component i_u that is uncorrelated to v_n [126]. These conditions can be expressed by the following expressions:

$$i_n = i_c + i_u,\ i_c = Y_c v_n,\ i_u v_n = 0 \qquad \text{(A.4), (A.5), (A.6)}$$

where Y_c in (A.5), is the complex correlation admittance.

After combining (A.3), (A.4), (A.5) and (A.6), the equivalent input referred voltage can be written as:

$$v_{eq} = v_n(1 + Z_s Y_c) + Z_s i_u \tag{A.7}$$

The variance of the random voltage v_{eq} is $\overline{v_{eq}^2}$. Because v_{eq} is equal to the sum of uncorrelated variables, its variance is equal to the sum of the variances of its uncorrelated components. Hence, the equations:

$$\overline{v_{eq}^2} = \overline{v_n^2}|1 + Z_s Y_c|^2 + |Z_s|^2 \overline{i_u^2} \tag{A.8}$$

$$N(i_n, v_n) = \overline{v_{eq}^2}\,,\, N_i = |Z_s|^2 \overline{i_s^2} \tag{A.9}$$

where $\overline{i_s^2}$ is the variance of the thermal noise of the source.

$$F = 1 + \frac{\overline{v_n^2}|1 + Z_s Y_c|^2 + |Z_s|^2 \overline{i_u^2}}{|Z_s|^2 \overline{i_s^2}} \tag{A.10}$$

The noise factor can also be calculated using the equivalent input referred current noise, which is given by:

$$i_{eq} = i_n + Y_s v_n \tag{A.11}$$

After combining (A.11), (A.4), (A.5) and (A.6), the equivalent input referred current can be written as:

$$i_{eq} = v_n(Y_s + Y_c) + i_u \tag{A.12}$$

The variance of i_{eq} can be expressed as:

$$\overline{i_{eq}^2} = \overline{v_n^2}|Y_s + Y_c|^2 + \overline{i_u^2} \tag{A.13}$$

$$N(i_n, v_n) = \overline{i_{eq}^2}\,,\, N_i = \overline{i_s^2} \tag{A.14}$$

$$F = 1 + \frac{\overline{v_n^2}|Y_s + Y_c|^2 + \overline{i_u^2}}{\overline{i_s^2}} \tag{A.15}$$

Equations (A.10) and (A.15) are equivalent.

The source has a conductance and a susceptance that are equal to G_s and to B_s, its admittance is equal to $Y_s = G_s + jB_s$. The correlation admittance Y_c is complex and can be

expressed by its real and imaginary components, with $Y_c = G_c + jB_c$. The current power density of the source thermal noise is given by:

$$\overline{i_s^2} = 4kTG_s \tag{A.16}$$

The noise voltage v_n referred to the input can be described by the power density of a thermal noise due to a theoretical resistance R_n, therefore:

$$\overline{v_n^2} = 4kTR_n \tag{A.17}$$

The power density of the uncorrelated component of the noise current reported to the input can be expressed as a function of a conductance G_u

$$\overline{i_u^2} = 4kTG_u \tag{A.18}$$

After combining (A.18), (A.17) and (A.16) in (A.15), the expression of the noise factor becomes:

$$F = 1 + \frac{R_n\left[(G_s + G_c)^2 + (B_s + B_c)^2\right] + G_u}{G_s} \tag{A.19}$$

The noise resistance R_n, the correlation admittance Y_c and G_u are determined by the noisy network. The noise factor F is a function of the source conductance and is minimal under the conditions:

$$\frac{\partial F}{\partial G_S} = 0 \Rightarrow G_S^2 = G_C^2 + \frac{G_u}{R_n} \quad \text{and} \quad \frac{\partial F}{\partial B_S} = 0 \tag{A.20}$$

Resolving (A.20) gives the source admittance Y_s for which the two-port network in Figure A.1 achieves the minimum noise factor [126]. The minimum of (A.19) is achieved when equalities (A.21) and (A.22) are satisfied, B_c and G_c being the real and imaginary parts of the noise correlation admittance.

$$B_s = B_{sopt} = -B_c \tag{A.21}$$

$$G_s = G_{sopt} = \sqrt{\frac{G_u}{R_n} + G_c^2} \tag{A.22}$$

$$Y_{sopt} = G_{sopt} + jB_{sopt} \tag{A.23}$$

$$F_{\min} = 1 + 2R_n\left(G_{sopt} + G_c\right) \tag{A.24}$$

$$F = F_{\min} + \frac{R_n}{G_s}\left[\left(G_s - G_{sopt}\right)^2 - \left(B_s - B_{sopt}\right)^2\right] \quad \text{(A.25)}$$

Equation (A.25) can be rewritten as:

$$F = F_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{sopt}\right|^2 \quad \text{(A.26)}$$

In (A.25), F is the noise factor of the two-port amplifier, F_{min} is the minimum achievable noise factor of the noisy amplifier, R_n is the noise resistance, Y_s is the source admittance ($Y_s = G_s + jB_s$) and Y_{sopt} is the optimum source admittance. F_{min}, R_n, B_{sopt} and G_{sopt} are the four noise parameters of any two-port noise model, describing completely its behaviour in terms of noise performance. The noise resistance R_n determines the sensitivity of F to deviations of the source admittance from Y_{sopt}. The first term of (A.26) is due to the intrinsic noise of the two-port device, the second term is due to the mismatch between the admittance of the source Y_s and the optimum noise matching admittance, which is dependent only on the two-port device. The equation shows that the minimum possible noise factor is equal to F_{min} and it is achieved when the source admittance is equal to Y_{sopt}. The admittance of the source and the optimum noise matching admittance being frequency-dependent, the second term of (A.26) is nil at only one frequency. Hence, R_n should be minimised and G_s maximised to reduce the noise due to source noise mismatch. Equation (A.26) can be expressed in terms of noise temperature by:

$$T_e = T_{\min} + T_o \frac{R_n}{G_s}\left|Y_s - Y_{sopt}\right|^2 \quad \text{(A.27)}$$

where T_e is the equivalent noise temperature, with $F = 1 + T_e/T_o$ and T_o = 290 K (room temperature).

Relations between noise parameters and input referred noise sources

The noise current i_n is related to the noise voltage v_n, to Y_c and to i_u by the relation (A.28), from (A.4) and (A.5):

$$i_n = Y_c v_n + i_u \quad \text{(A.28)}$$

By multiplying each side of (A.28) by v_n^* and taking the average, (A.28) yields:

$$\overline{i_n v_n^*} = Y_c \overline{v_n^2} \quad \text{(A.29)}$$

Equation (A.30) is derived from (A.29) as follows:

$$Y_c = \frac{\overline{i_n v_n^*}}{\overline{v_n^2}} \tag{A.30}$$

The correlation impedance is defined by $Z_c = \overline{v_n i_n^*} / \overline{i_n^2}$, hence $Z_c \neq 1/Y_c$. The correlation coefficient is a normalized quantity defined by (A.31).

$$c = \frac{\overline{v_n^* i_n}}{\sqrt{\overline{v_n^2}\,\overline{i_n^2}}} = Y_c \sqrt{\frac{\overline{v_n^2}}{\overline{i_n^2}}} \tag{A.31}$$

The noise resistance R_n is derived from (A.17), which is equivalent to (A.32):

$$R_n = \frac{\overline{v_n^2}}{4kT} \tag{A.32}$$

$$B_{sopt} = -\mathrm{Im}\{Y_C\} = -\mathrm{Im}\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\} \tag{A.33}$$

$$G_{sopt} = \sqrt{\frac{\overline{i_u^2}}{\overline{v_n^2}} + R_e^2\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\}} = \sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - \mathrm{Im}\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}} \tag{A.34}$$

$$F_{\min} = 1 + \frac{\overline{v_n^2}}{2kT}\left(\sqrt{\frac{\overline{i_u^2}}{\overline{v_n^2}} + R_e^2\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}} + R_e\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}\right) \tag{A.35}$$

$$F_{\min} = 1 + \frac{\overline{v_n^2}}{2kT}\left(\sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - \mathrm{Im}\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}} + R_e\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}\right) \tag{A.36}$$

Relation between noise parameters and the noise correlation matrix in chain representation

The noise resistance R_n has been defined by (A.32). Equation (A.32) provides the term C_{A11} of the correlation matrix in chain representation. The term C_{A12} of the correlation matrix is equal to $\overline{i_n i_n^*}$ which is the noise conductance, $g_n = \overline{i_n i_n^*}/4kT$, and is calculated as follows.

The equivalent current noise at the input is given by:

$$i_{neq} = v_n/Z_s(\omega) + i_s + i_n \quad \text{(A.37)}$$

The power density of the noise is given by:

$$\overline{i_{neq}i_{neq}^*} = \frac{\overline{v_n v_n^*}}{Z_s^2(\omega)} + \frac{\overline{(i_n^* v_n)^*}}{Z_s(\omega)} + \frac{\overline{v_n i_n^*}}{Z_s(\omega)} + \overline{i_n i_n^*} + \overline{i_s i_s^*} \quad \text{(A.38)}$$

$$\overline{i_{neq}i_{neq}^*} = \overline{v_n v_n^*} Y_s^2(\omega) + 2\,\mathrm{Re}\{\overline{v_n i_n^*} Y_s(\omega)\} + \overline{i_n i_n^*} + \overline{i_s i_s^*} \quad \text{(A.39)}$$

$$\overline{i_s i_s^*} = 4kT\,\mathrm{Re}\{Y_s(\omega)\} \quad \text{(A.40)}$$

$$F = 1 + \frac{\overline{v_n v_n^*} Y_s^2(\omega) + 2\,\mathrm{Re}\{\overline{v_n i_n^*} Y_s(\omega)\} + \overline{i_n i_n^*}}{4kT\,\mathrm{Re}\{Y_s(\omega)\}} \quad \text{(A.41)}$$

$$F = 1 + \frac{R_n(G_s^2 + B_s^2)}{G_s} + 2\frac{\mathrm{Re}\{\overline{v_n i_n^*}\}}{4kT} - 2\frac{\mathrm{Im}\{\overline{u_n i_n^*}\}}{4kTG_s} B_s + \frac{g_n}{G_s} \quad \text{(A.42)}$$

From (A.41), it can be seen that when Y_s tends to zero, the term in $\frac{\overline{i_n i_n^*}}{4kT\,\mathrm{Re}\{Y_s(\omega)\}}$ tends to infinity and when Y_s tends to infinity, the term $\frac{\overline{v_n v_n^*} Y_s^2(\omega)}{4kT\,\mathrm{Re}\{Y_s(\omega)\}}$ tends to infinity. As F tends to infinity when Y_s tends to zero and when Y_s tends to infinity, there is a value of Y_{sopt} for which F reaches a minimum.

The admittance of the input is $Y_s = G_s + jB_s$. The optimum source admittance Y_{sopt} is calculated by differentiating F as follows:

$$\frac{\partial F}{\partial G_s} = 0 \text{ and } \frac{\partial F}{\partial B_s} = 0 \quad \text{(A.43)}$$

The differentiation of F versus B_s provides the second condition for minimum F:

$$B_{sopt} = \frac{\mathrm{Im}\{\overline{v_n i_n^*}\}}{4kTR_n} \quad \text{(A.44)}$$

The differentiation of F versus G_s provides the first minimum condition:

$$G_{sopt}^2 = \frac{\overline{i_n i_n^*} + \overline{v_n v_n^*} B_s^2}{\overline{v_n v_n^*}} \quad \text{(A.45)}$$

$$G_{sopt} = \sqrt{\frac{g_n + R_n B_s^2 - \frac{\operatorname{Im}\{\overline{v_n i_n^*}\}}{kT} B_s}{R_n}} \quad \text{(A.46)}$$

$$g_n = R_n (G_s^2 + B_s^2) \quad \text{(A.47)}$$

$$g_n = R_n \left| Y_{sopt} \right|^2 \quad \text{(A.48)}$$

The term C_{A22} of the correlation matrix is then:

$$C_{A22} = 4KTg_n \quad \text{(A.49)}$$

$$C_{A22} = 4KTg_n = 4KTR_n \left| Y_{sopt} \right|^2 \quad \text{(A.50)}$$

The terms $\overline{v_n i_n^*}$ and $\overline{v_n^* i_n}$ are determined as follows:

For $Y_s = Y_{sopt}$, (A.42) can be rewritten as (A.51) after introducing the expression $g_n = R_n (G_s^2 + B_s^2)$:

$$F_{\min} = 1 + \frac{2g_n}{G_{sopt}} + \frac{G_{sopt} \operatorname{Re}\{\overline{v_n i_n^*}\}}{2kTG_{sopt}} - \frac{\operatorname{Im}\{\overline{v_n i_n^*}\}}{2kTG_{sopt}} B_{sopt} \quad \text{(A.51)}$$

Using the relation $B_{sopt} = \frac{\operatorname{Im}\{\overline{v_n i_n^*}\}}{4kTR_n}$, (A.53) yields (A.54):

$$F_{\min} = 1 + \frac{4kTg_n}{2kTG_{sopt}} + \frac{G_{sopt} \operatorname{Re}\{\overline{v_n i_n^*}\}}{2kTG_{sopt}} - \frac{4kTR_n B_{sopt}^2}{2kTG_{sopt}} \quad \text{(A.52)}$$

$$\operatorname{Re}\{\overline{v_n i_n^*}\} = 2kT\left[\frac{F_{\min} - 1}{2} - R_n G_{sopt}\right] \quad \text{(A.53)}$$

Using again the expression $B_{sopt} = \frac{\operatorname{Im}\{\overline{v_n i_n^*}\}}{4kTR_n}$, (A.53) becomes (A.54):

$$\operatorname{Re}\{\overline{v_n i_n^*}\} + j\operatorname{Im}\{\overline{v_n i_n^*}\} = 2kT\left[\frac{F_{\min} - 1}{2} - R_n (G_{sopt} - jB_{sopt})\right] \quad \text{(A.54)}$$

Therefore:

$$\overline{v_n i_n^*} = 2kT\left[\frac{F_{\min} - 1}{2} - R_n Y_{sopt}^*\right] \quad \text{(A.55)}$$

and because $\left(\overline{v_n i_n^*}\right)^* = \overline{i_n v_n^*}$

$$\overline{i_n v_n^*} = 2kT\left[\frac{F_{\min} - 1}{2} - R_n Y_{sopt}\right] \tag{A.56}$$

The chain correlation matrix is defined in (4.40) by the two-port noise parameters.

$$C_A = 2kT\begin{bmatrix} R_n & \left[\frac{F_{\min} - 1}{2} - R_n Y_{sopt}^*\right] \\ \left[\frac{F_{\min} - 1}{2} - R_n Y_{sopt}\right] & R_n\left|Y_{sopt}\right|^2 \end{bmatrix} \tag{A.57}$$

Inversely, the two-port noise model parameters can be obtained from the chain correlation matrix by the relations:

$$R_n = C_{A11}/2kT \tag{A.58}$$

$$Y_{sopt} = \sqrt{\frac{C_{A22}}{C_{A11}} - \left[\mathrm{Im}\left(\frac{C_{A12}}{C_{A11}}\right)\right]^2} + j\,\mathrm{Im}\left(\frac{C_{A12}}{C_{A11}}\right) \tag{A.59}$$

$$F_{\min} = 1 + \frac{C_{A12} + C_{A11}Y_{sopt}^*}{kT} \tag{A.60}$$

Equation (A.60) can also be written as [67], [79]:

$$F_{\min} = 1 + 2(\mathrm{Re}\{C_{A12}\} + C_{A11}G_{sop}) \tag{A.61}$$

with $C_{A11} = \frac{\overline{v_n v_n^*}}{4kT\Delta f}$ and $C_{A12} = \frac{\overline{v_n i_n^*}}{4kT\Delta f} = \frac{\overline{v_n^* i_n}}{4kT\Delta f}$.

Noise correlation matrix transformations

Table A.1. Transformation of noise correlation matrices.

	Original Representation			
	C_Y	C_Z	C_A	C_H
C_Y'	$\begin{bmatrix}1 & 0\\0 & 1\end{bmatrix}$	$\begin{bmatrix}Y_{11} & Y_{12}\\Y_{21} & Y_{22}\end{bmatrix}$	$\begin{bmatrix}-Y_{11} & 1\\-Y_{21} & 0\end{bmatrix}$	$\begin{bmatrix}-Y_{11} & 0\\-Y_{21} & 1\end{bmatrix}$
C_Z'	$\begin{bmatrix}Z_{11} & Z_{12}\\Z_{21} & Z_{22}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\0 & 1\end{bmatrix}$	$\begin{bmatrix}1 & -Z_{11}\\0 & -Z_{21}\end{bmatrix}$	$\begin{bmatrix}1 & -Z_{12}\\0 & -Z_{22}\end{bmatrix}$
C_A'	$\begin{bmatrix}0 & A_{12}\\1 & A_{22}\end{bmatrix}$	$\begin{bmatrix}1 & -A_{11}\\0 & -A_{21}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\0 & 1\end{bmatrix}$	$\begin{bmatrix}1 & A_{12}\\0 & A_{22}\end{bmatrix}$
C_H'	$\begin{bmatrix}-h_{11} & 0\\-h_{21} & 1\end{bmatrix}$	$\begin{bmatrix}1 & -h_{12}\\0 & -h_{22}\end{bmatrix}$	$\begin{bmatrix}1 & -h_{11}\\0 & -h_{21}\end{bmatrix}$	$\begin{bmatrix}1 & 0\\0 & 1\end{bmatrix}$

ADDENDUM B Y- AND Z- PARAMETERS FOR THE CE AMPLIFIER

Y-parameters are expressed in terms of device parameters.

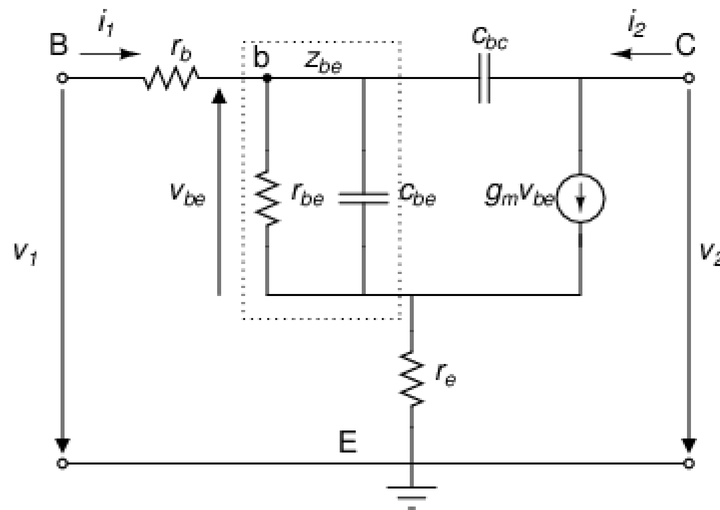


Figure B.1. Transistor equivalent circuit.

Calculation of Y_{11}

$$Y_{11} = \frac{i_1}{v_1}|_{v_2=0} \tag{B.1}$$

$$i_i = v_b Y_{bc} + \frac{v_{be}}{Z_{be}} \tag{B.2}$$

$$v_1 = i_1 r_b + v_b \tag{B.3}$$

where v_b is the voltage at node (b).

$$v_e = v_b \frac{r_e + Z_{bc} r_e g_m}{Z_{be} + r_e + Z_{bc} r_e g_m} \tag{B.4}$$

$$v_{be} = v_b \frac{Z_{be}}{Z_{be} + r_e + Z_{bc} r_e g_m} \tag{B.5}$$

$$Y_{11}=\frac{i_1}{v_1}=\frac{g_{be}+j\omega C_{be}\left(1+r_e\left(g_{be}+j\omega C_{be}+g_m\right)\right)}{1+r_b\left(g_{be}+j\omega C_{be}+j\omega C_{bc}\right)+g_m r_e\left(j\omega C_{bc}r_b+1\right)} \quad \text{(B.6)}$$

where $g_{be}=1/r_{be}$.

Calculation of Y_{12}

$$Y_{12}=\frac{i_1}{v_2}|_{v_1=0} \quad \text{(B.7)}$$

$$v_b=-i_1 r_b \quad \text{(B.8)}$$

$$i_1=\left(v_b-v_2\right)Y_{bc}+\frac{v_{be}}{Z_{be}} \quad \text{(B.9)}$$

$$i_1\left(1+r_bY_{bc}+\frac{r_b}{Z_{be}+r_e+Z_{be}r_eg_m}\right)=-v_2Y_{bc} \quad \text{(B.10)}$$

$$Y_{12}=\frac{i_1}{v_2}=\frac{-j\omega C_{bc}\left(1+r_e\left(g_m+g_{be}+j\omega C_{be}\right)\right)}{1+r_b\left(g_{be}+j\omega C_{be}+j\omega C_{bc}\right)+g_m r_e\left(j\omega C_{bc}r_b+1\right)} \quad \text{(B.11)}$$

Calculation of Y_{21}

$$Y_{21}=\frac{i_2}{v_1}|_{v_2=0} \quad \text{(B.12)}$$

$$v_e=v_b\left(j\omega C_{bc}+\frac{1}{Z_{be}+r_e+Z_{bc}r_eg_m}\right) \quad \text{(B.13)}$$

$$v_1=v_b+i_1r_b \quad \text{(B.14)}$$

$$v_b=v_1\Big/\left[1+r_b\left(j\omega C_{bc}+\frac{1}{Z_{be}+r_e+Z_{be}r_eg_m}\right)\right] \quad \text{(B.15)}$$

$$v_{be}=v_1\left(\frac{Z_{be}}{Z_{be}+r_e+Z_{be}r_eg_m}\right)\Big/\left[1+r_b\left(j\omega C_{bc}+\frac{1}{Z_{be}+r_e+Z_{be}r_eg_m}\right)\right] \quad \text{(B.16)}$$

$$i_2=g_mv_{be}-v_{be}\left(j\omega C_{bc}\right) \quad \text{(B.17)}$$

$$Y_{21}=\frac{i_2}{v_1}=\frac{g_m-j\omega C_{bc}}{1+r_b\left(g_{be}+j\omega C_{be}+j\omega C_{bc}\right)+g_m r_e\left(j\omega C_{bc}r_b+1\right)} \quad \text{(B.18)}$$

$$Y_{22}=\frac{i_2}{v_2}|_{v_1=0} \quad \text{(B.19)}$$

$$i_2=g_mv_{be}+\frac{v_b}{r_b}+\frac{v_{be}}{Z_{be}} \quad \text{(B.20)}$$

$$\frac{v_b - v_2}{Z_{bc}} + \frac{v_b}{r_b} + \frac{v_{be}}{Z_{be}} = 0 \tag{B.21}$$

$$v_b = v_2 \frac{r_b\left(Z_{be} + \beta^{'} r_e\right)}{r_b\left(Z_{be} + \beta^{'} r_e\right) + Z_{bc}\left(r_b + Z_{be} + \beta^{'} r_e\right)} \tag{B.22}$$

where $\beta^{'} = 1 + Z_{be} g_m$

Calculation of Y_{22}

$$i_2 = v_b\left[\left(\frac{Z_{be}}{Z_{be} + r_e\beta^{'}}\right)\left(g_m + \frac{1}{Z_{be}}\right) + \frac{1}{r_b}\right] \tag{B.23}$$

$$Y_{22} = \frac{i_2}{v_2} = \frac{j\omega C_{bc}\left(1 + \left(g_{be} + j\omega C_{be} + g_m\right)\left(r_e + r_b\right)\right)}{1 + r_b\left(g_{be} + j\omega C_{be} + j\omega C_{bc}\right) + g_m r_e\left(j\omega C_{bc} r_b + 1\right)} \tag{B.24}$$

Calculation of Z_{11}

$$Z_{11} = \frac{v_1}{i_1}\bigg|_{i_2=0} \tag{B.25}$$

$$v_e = \left(\frac{v_{be}}{Z_{be}} + g_m v_{be}\right) r_e \tag{B.26}$$

$$v_{be} = v_b\left(\frac{1}{1 + r_e\left(g_{be} + j\varpi C_{be} + g_m\right)}\right) \tag{B.27}$$

$$v_1 = i_1 r_b + v_b \tag{B.28}$$

$$i_1 = g_m V_{be} + \frac{v_{be}}{Z_{be}} \tag{B.29}$$

Substituting (B.27) in (B.29) yields the expression of i_1:

$$i_1 = v_b \frac{g_m + g_{be} + j\omega C_{be}}{1 + r_e\left(g_{be} + j\omega C_{be} + g_m\right)} \tag{B.30}$$

Combining (B.28) and (B.30) gives:

$$v_b = v_1 \frac{1 + r_e\left(g_m + g_{be} + j\omega C_{be}\right)}{1 + \left(r_e + r_b\right)\left(g_{be} + j\omega C_{be} + g_m\right)} \tag{B.31}$$

Substituting (B.31) in (B.30) yields:

$$Z_{11} = \frac{v_1}{i_1} = \frac{1 + \left(r_e + r_b\right)\left(g_{be} + j\omega C_{be} + g_m\right)}{g_m + g_{be} + j\omega C_{be}} \tag{B.32}$$

Calculation of Z_{12}

$$Z_{12} = \frac{v_1}{i_2}\Big|_{i_1=0} \tag{B.33}$$

$$i_2 = g_m v_{be} + \frac{v_{be}}{Z_{be}} = (v_1 - v_e)(g_m + 1/Z_{be}) \tag{B.34}$$

$$v_e = \frac{\left(g_m + \frac{1}{Z_{be}}\right)}{1 + \left(g_m + \frac{1}{Z_{be}}\right)} v_1 \tag{B.35}$$

$$Z_{12} = \frac{v_1}{i_2} = \frac{1 + r_e\left(g_{be} + j\omega C_{be} + g_m\right)}{g_m + g_{be} + j\omega C_{be}} \tag{B.36}$$

Calculation of Z_{21}

$$Z_{21} = \frac{v_2}{i_1}\Big|_{i_2=0} \tag{B.37}$$

$$g_m v_{be} = (v_b - v_2)/Z_{bc} \tag{B.38}$$

$$v_{be} = v_b\left(1/\left(1 + r_e\left(g_{be} + j\omega C_{be} + g_m\right)\right)\right) \tag{B.39}$$

Substituting (B.39) in (B.38) gives:

$$v_b = v_2 \frac{1 + r_e\left(g_{be} + j\omega C_{be} + g_m\right)}{1 + r_e\left(g_{be} + j\omega C_{be} + g_m\right) - g_m Z_{bc}} \tag{B.40}$$

$$i_1 = g_m v_{be} + \frac{v_{be}}{Z_{be}} = v_{be}\left(g_m + g_{be} + j\omega C_{be}\right) \tag{B.41}$$

Substituting (B.39) in (B.38) and (B.41), and substituting (B.40) in (B.38) yields (B.42).

$$Z_{21} = \frac{v_2}{i_1} = \frac{1 - \frac{g_m}{j\omega C_{bc}} + r_e\left(g_{be} + j\omega C_{be} + g_m\right)}{g_m + g_{be} + j\omega C_{be}} \tag{B.42}$$

Calculation of Z_{22}

$$Z_{22} = \frac{v_2}{i_2}\Big|_{i_1=0} \tag{B.43}$$

$$i_2 = g_m v_{be} + \frac{v_{be}}{Z_{be}} = v_{be}\left(g_m + 1/Z_{be}\right) \tag{B.44}$$

$$i_2 = v_b \left(\frac{Z_{be}}{Z_{be} + r_e + Z_{be} r_e g_m} \right)\left(g_m + 1/Z_{be}\right) \tag{B.45}$$

$$\frac{v_{be}}{Z_{be}} = \frac{\left(v_2 - v_b\right)}{Z_{bc}} \tag{B.46}$$

$$v_b = v_2 \left(\frac{Z_{be} + r_e + Z_{be} r_e g_m}{Z_{bc} + Z_{be+} r_e + Z_{be} r_e g_m} \right) \tag{B.47}$$

Substituting (B.47) in (B.46) yields:

$$Z_{22} = \frac{v_2}{i_2} = \frac{1 + C_{be}/C_{bc} + g_{be}/j\omega C_{bc} + r_e\left(g_{be} + j\omega C_{be} + g_m\right)}{g_{be} + j\omega C_{be} + g_m} \tag{B.48}$$

ADDENDUM C VOINIGESCU MODEL

The Voinigescu model is based on the Giacoletto's equivalent circuit in Figure C.1. A detailed derivation of the model is presented in this section.

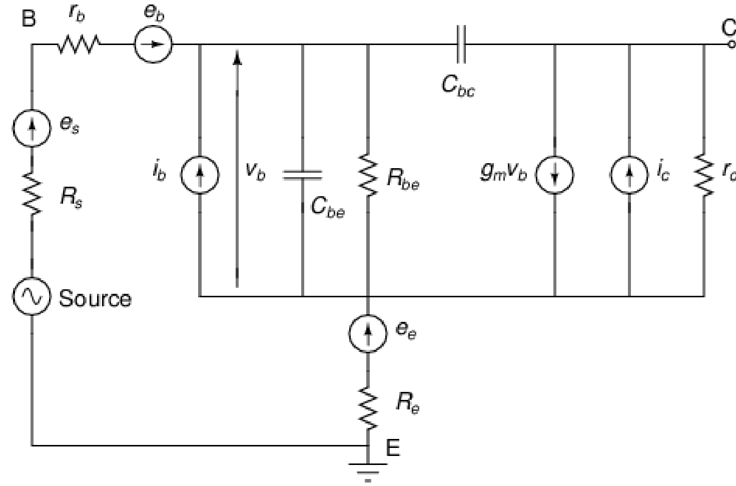


Figure C.1. Small-signal circuit for Voiginescu's noise model.

The base and collector shot noise sources are assumed to be uncorrelated. From (4.33) and (4.34), resulting in (4.80), (4.81), (4.82), and using a Blakesley transformation that reports the parasitic resistance R_e to the base, the power of the noise voltage v_n, the noise current i_n and their cross-correlation reported to the input are given by:

$$\overline{v_n^2} = 4kT\left(r_b + R_e\right) + \frac{\overline{i_c^2}}{\left|Y_{21}\right|^2} \tag{C.1}$$

$$\overline{i_n^2} = \overline{i_b^2} + \frac{\left|Y_{11}\right|^2 \overline{i_c^2}}{\left|Y_{21}\right|^2} - 2\Re\left(\frac{Y_{11}\,\overline{i_b^* i_c}}{Y_{21}}\right) \tag{C.2}$$

$$\overline{v_n i_n^*} = \overline{v_n^* i_n} = \frac{Y_{11}\,\overline{i_c^2}}{\left|Y_{21}\right|^2} - \frac{\overline{i_b i_c^*}}{Y_{21}^*} \tag{C.3}$$

The correlation admittance is given by:

$$Y_c = \frac{\overline{v_n i_n^*}}{\overline{v_n^2}} = \frac{Y_{11}\overline{i_c^2} - Y_{21}\overline{i_b i_c^*}}{2kTR_n|Y_{21}|^2} \quad \text{(C.4)}$$

where $R_n = \frac{\overline{v_n^2}}{4kT}$.

Because, at the operating frequency, the correlation between the base shot noise and the collector shot noise can be neglected, the terms in $\overline{i_b i_c^*}$ and $\overline{i_b^* i_c}$ in (C.2), (C.3) and (C.4) are small and can be neglected. Furthermore, (C.4) can be simplified assuming $\frac{\overline{i_c^2}}{|Y_{21}|^2} >> 4kT(r_b + R_e)$ and $\overline{v_n^2} \approx \frac{\overline{i_c^2}}{|Y_{21}|^2}$, hence

$$Y_C = \frac{Y_{11}\overline{i_c^2}}{\overline{v_n^2}|Y_{21}|^2} \approx Y_{11} \quad \text{(C.5)}$$

The collector DC is given by

$$I_C = I_S\left(e^{\frac{V_B}{nV_T}} - 1\right) \quad \text{(C.6)}$$

where n is the collector current ideality factor, V_T the thermal voltage and I_S the reverse saturation current. Because C_{bc}, r_{bc} and r_o are neglected, the derivative of I_C relative to the base voltage is given by:

$$g_m = |Y_{21}| = \frac{\partial I_C}{\partial V_B} = \frac{I_C}{nV_T} \quad \text{(C.7)}$$

R_n is given by:

$$R_n = \frac{1}{4kT}\left(4kT(r_b + R_e) + \frac{\overline{i_c^2}}{|Y_{21}|^2}\right) = (r_b + R_e) + \frac{qI_C}{2kT|Y_{21}|^2} \approx (r_b + R_e) + \frac{n^2 V_T}{2I_C} \quad \text{(C.8)}$$

The optimum noise admittance and F_{min} are calculated from (A.35), (A.36) and (A.38). Hence, $Y_{sopt} = G_{sopt} + jB_{sopt} = \sqrt{\frac{\overline{i_u^2}}{\overline{v_n^2}} + \Re^2\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\}} - \Im\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}$

because $i_n = Y_C v_n + i_u$, $\overline{i_u^2} = \overline{i_n^2} - |Y_C|^2 \overline{v_n^2}$. Therefore,

$$\frac{\overline{i_u^2}}{\overline{v_n^2}} = \frac{\overline{i_n^2}}{\overline{v_n^2}} - |Y_C|^2 \tag{C.9}$$

The real part of the optimum noise admittance becomes:

$$G_{sopt} = \sqrt{\frac{\overline{i_u^2}}{\overline{v_n^2}} + \Re^2\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\}} = \sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - |Y_C|^2 + \Re^2\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\}} = \sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - \Im^2\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\}} \tag{C.10}$$

Using (C.10), the optimum noise admittance is rewritten as:

$$Y_{sopt} = G_{sopt} + jB_{sopt} = \sqrt{A + B^2} - \Im B \tag{C.11}$$

Using (C.1), (C.2) and (C.3),

$$A = \frac{\overline{i_b^2}|Y_{21}|^2 + \overline{i_c^2}|Y_{11}|^2}{\overline{i_c^2} + 4kT(r_b + R_e)|Y_{21}|^2} \tag{C.12}$$

$$B = \frac{\overline{i_c^2}\Im(Y_{11})}{\overline{i_c^2} + 4kT(r_b + R_e)|Y_{21}|^2} \tag{C.13}$$

The effect of the base parasitic resistance to the transfer function is small, therefore when r_b is neglected, the Y-parameters of Figure 4.15, are given by the matrix in (C.14)

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \frac{g_m}{\beta} + j\omega(C_{be} + C_{bc}) & -j\omega C_{bc} \\ g_m & j\omega C_{bc} \end{bmatrix} \tag{C.14}$$

Replacing the base and collector shot noises $\overline{i_b^2}$ and $\overline{i_c^2}$ by $2qI_B$ and $2qI_C$, (C.11) becomes

$$Y_{sopt} = \sqrt{\frac{I_B|Y_{21}|^2 + I_C|Y_{11}|^2}{2V_T|Y_{21}|^2(r_b + R_e) + I_C} - \left(\frac{I_C\Im\{Y_{11}\}}{2V_T|Y_{21}|^2(r_b + R_e) + I_C}\right)^2} - j\frac{I_C\Im\{Y_{11}\}}{2V_T|Y_{21}|^2(r_b + R_e) + I_C} \tag{C.15}$$

where I_B and I_C are the base and collector DC bias currents.

Reporting in (C.15) Y-parameters in (C.14),

$$Y_{sopt} \approx \frac{f}{f_T R_n}\left\{\sqrt{\frac{I_C}{2V_T}(r_b + R_e)(1 + \frac{f_T^2}{\beta_o f^2}) + \frac{n^2 f_T^2}{4\beta_o f^2}} - j\frac{n}{2}\right\} \tag{C.16}$$

$$R_{sopt} \approx \frac{R_n f_T}{f} \frac{\sqrt{\frac{I_C}{2V_T}(r_b + R_e)(1 + \frac{f_T^2}{\beta_o f^2}) + \frac{n^2 f_T^2}{4\beta_o f^2}}}{\frac{I_C}{2V_T}(r_b + R_e)(1 + \frac{f_T^2}{\beta_o f^2}) + \frac{n^2}{4}\left(1 + \frac{f_T^2}{4\beta_o f^2}\right)} \tag{C.17}$$

The minimum NF is calculated from the expression in (4.6):

$$F_{\min} = 1 + \frac{\overline{v_n^2}}{2kT}\left(\sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - \left(\Im\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}\right)^2} + \Re\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}\right)$$ which is rewritten as:

$$F_{\min} = 1 + C + D \text{ with } C = \frac{\overline{v_n^2}}{2kT}\sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - \left(\Im\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}\right)^2} \text{ and } D = \frac{\overline{v_n^2}}{2kT}\Re\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\} \tag{C.18}$$

Using (C.1) and (4.89) in (C.18), and because $\frac{\overline{i_c^2}}{|Y_{21}|^2} >> 4kT(r_b + R_e)$, D is given by:

$$D = \frac{I_C}{V_T}\frac{\Re\{Y_{11}\}}{|Y_{21}|^2} \tag{C.19}$$

Using the expression $\frac{\overline{v_n^2}}{2kT} = 2R_n$, the first factor of C, $\frac{\overline{v_n^2}}{2kT}$, is evaluated as follows:

$$R_n = \frac{\overline{i_c^2}}{4kT|Y_{21}|^2} + (r_b + R_e) = \frac{I_C}{2V_T|Y_{21}|^2} + (r_b + R_e) \tag{C.20}$$

$$\frac{\overline{v_n^2}}{2kT} = \frac{I_C}{V_T|Y_{21}|^2}\sqrt{\left(\frac{\overline{i_c^2} + 4kT(r_b + R_e)|Y_{21}|^2}{\overline{i_c^2}}\right)^2} \tag{C.21}$$

From (C.1), (C.2) and (A.12), $\frac{\overline{i_n^2}}{\overline{v_n^2}} = A$.

The quantity $\Im\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\}$ in the expression C is calculated as follows from (C.1) and (C.3):

$$\frac{\overline{i_n v_n^*}}{\overline{v_n^2}} = \frac{\overline{i_c^2} Y_{11}}{\overline{i_c^2} + 4kT(r_b + R_e)|Y_{21}|^2} \tag{C.22}$$

$$\Im\left\{\frac{\overline{i_n v_n^*}}{\overline{v_n^2}}\right\} = \frac{\overline{i_c^2}\Im\{Y_{11}\}}{\overline{i_c^2} + 4kT(r_b + R_e)|Y_{21}|^2} \tag{C.23}$$

Combining (C.12), (C.19), (C.20) and (C.23) in (C.18), the minimum noise factor is given by:

$$F_{\min} = 1 + \frac{I_C}{V_T|Y_{21}|^2}\left(\sqrt{\left(\frac{\overline{i_b^2}}{\overline{i_c^2}}|Y_{21}|^2 + |Y_{11}|^2\right)\left(\frac{4kT(r_b + R_e)}{\overline{i_c^2}}|Y_{21}|^2 + 1\right) - (\Im\{Y_{11}\})^2} + \Re\{Y_{11}\}\right) \tag{C.24}$$

Replacing the base and collector shot noises $\overline{i_b^2}$ and $\overline{i_c^2}$ by $2qI_B$ and $2qI_C$, (C.24) becomes:

$$F_{\min} = 1 + \frac{I_C}{V_T|Y_{21}|^2}\left(\sqrt{\left(\frac{I_B}{I_C}|Y_{21}|^2 + |Y_{11}|^2\right)\left(\frac{2V_T(r_b + R_e)}{I_C}|Y_{21}|^2 + 1\right) - (\Im\{Y_{11}\})^2} + \Re\{Y_{11}\}\right) \tag{C.25}$$

Reporting the Y-parameters from (C.14) in (C.25) and with $1/\beta_o^2 << 1/\beta_o$ and $f_T = 1/2\pi(C_{be} + C_{bc})$, (C.25) becomes:

$$F_{\min} = 1 + \frac{n}{\beta_o} + \frac{f}{f_T}\sqrt{\frac{I_C}{2V_T}(r_b + R_e)(1 + \frac{f_T^2}{\beta_o f^2}) + \frac{n^2 f_T^2}{\beta_o f^2}} \tag{C.26}$$

where n is the collector current ideality factor or junction grading factor from 1 to 1.2, r_b and R_e are the base and emitter parasitic resistances, β_o is the small-signal gain and V_T is the thermal voltage (~26 mV). For SiGe, the collector current ideality factor can be approximated by unity, except for high bias current.

The four noise parameters for the CE are given by (C.8), (C.16), (C.25). Equation (C.17) is derived from (C.16) and allows analysis of how the optimum source resistance R_{sopt} is related to the size of the transistor. Because, $n \approx 1$, (C.8) and (C.25) can also be written as:

$$R_n \approx \frac{V_T}{2I_C} + r_b + R_e \tag{C.27}$$

$$F_{\min} = 1 + \frac{1}{\beta_o} + \sqrt{\frac{I_C}{2V_T}(r_b + R_e)\left(\frac{f^2}{f_T^2} + \frac{1}{\beta_o}\right) + \frac{1}{\beta_o}} \tag{C.28}$$

Equation (C.28) shows that F_{min} increases with the parasitic base and emitter resistances. At low frequencies, F_{min} is weakly related to the base resistance and mainly related to β_o.

The minimum noise factor starts to increase as the frequencies get higher and the dependence is a quasi-linear function of the frequency that is inversely proportional to f_T. At low bias current, the main component of f_T is the base transit time. Therefore, f_T increases with the collector current. The ratio I_C / f_T^2 decreases as $1/I_C$ and F_{min} decreases when I_C increases. As I_C increases, f_T reaches a maximum and becomes flat and the term I_C / f_T^2 becomes proportional to I_C. Therefore, there is a value of the collector current I_{COPT}, for which F_{min} is at the minimum. This value is in the range of 1% to 20% of the current value for peak f_T.

ADDENDUM D SKILL CADENCE SCRIPT FOR THE PLOT OF R_{OPT}

The procedure in this section uses the results of a SP Noise Analysis to obtain the Optimum Noise Impedance Z_{opt}. The procedure is performed by a SKILL script that is loaded through the Cadence command interpretation window (CIW) and run by executing the procedures RoptCB for Ropt and XoptCB for Xopt. These procedures add respectively the functions "*Ropt*" and "*Xopt*" in the Cadence calculator.

```
procedure(Ropt()
      selectResults('sp_noise)
      Gopt = getData("Gopt")
      Bopt = getData("Bopt")
      Yopt = Gopt+sqrt(-1)*Bopt
      Zopt = 1/Yopt
      RoptReal = real(Zopt)
      plot(RoptReal))
procedure(RoptCB()
      calCalcInput('expression "Ropt()"))
procedure(RoptRegSpecialFunction()
      calRegisterSpecialFunction(
      list("Ropt" 'RoptCB)))
procedure(Xopt()
      selectResults('sp_noise)
      Gopt_ = getData("Gopt")
      Bopt_ = getData("Bopt")
      Yopt_ = Gopt_ +sqrt(-1)*Bopt_
      Zopt_ = 1/Yopt_
      RoptIm = imag(Zopt_)
      plot(RoptIm))
procedure(XoptCB()
      calCalcInput('expression "Xopt()"))
procedure(XoptRegSpecialFunction()
      calRegisterSpecialFunction(
      list("Xopt" 'XoptCB)))
```

ADDENDUM E R_{SOPT} FOR PARALLEL TWO-PORT NETWORKS

Consider the noise correlation matrix C_A of a two-port network, which consists in this case of a CE BJT or SiGe HBT. Using the ABCD representation, the noise correlation matrix can be expressed as:

$$C_A = \begin{bmatrix} C_{A11} & C_{A12} \\ C_{A21} & C_{A22} \end{bmatrix} \tag{E.1}$$

The elements of the correlation matrix C_A can be expressed as functions of the two-port noise parameters, as shown in Chapter 4:

$$C_A = 2kT\begin{bmatrix} R_n & \left[\dfrac{F_{\min}-1}{2} - R_n Y_{sopt}^*\right] \\ \left[\dfrac{F_{\min}-1}{2} - R_n Y_{sopt}\right] & R_n\left|Y_{sopt}\right|^2 \end{bmatrix} \tag{E.2}$$

The chain correlation matrix C_A can be transformed into an admittance noise correlation matrix C_Y, using the transformation matrix T, with:

$$T = \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix} \tag{E.3}$$

Using the congruence transformation, the transformation is done using the equation:

$$[C_Y] = [T][C_A][T]^+ \tag{E.4}$$

It comes that:

$$C_Y = \begin{bmatrix} (\left|Y_{11}\right|^2 C_{A11} - Y_{11}C_{A12} - Y_{11}^* C_{A21} + C_{A22}) & (Y_{11}Y_{21}^* C_{A11} - Y_{21}^* C_{A21}) \\ (Y_{21}Y_{11}^* C_{A11} - Y_{21}C_{A12}) & (\left|Y_{21}\right|^2 C_{A11}) \end{bmatrix} \tag{E.5}$$

Therefore, the elements of C_Y are given by:

$$C_{Y22} = \left|Y_{21}\right|^2 C_{A11} \tag{E.6}$$

$$C_{Y21} = Y_{21}Y_{11}^* C_{A11} - Y_{21}C_{A12} \tag{E.7}$$

$$C_{Y12} = Y_{21}^* Y_{11} C_{A11} - Y_{21}^* C_{A12} \tag{E.8}$$

$$C_{Y11} = \left|Y_{21}\right|^2 C_{A11} - Y_{11} C_{A12} - Y_{11}^* C_{A21} + C_{A22} \tag{E.9}$$

The elements C_{Y22} and C_{Y11} are real. When n identical two-port networks are connected in parallel, the values of the Y-parameters of the resulting network are n times the values of the Y-parameters of a single two-port network. In addition, the values of elements of the admittance noise correlation matrix of the resulting network are n times the values of the elements of the admittance noise correlation matrix of a single two-port network. From (E.6), it is derived that:

$$R_n = \frac{C_{Y22}}{2kT\left|Y_{21}\right|^2} \tag{E.10}$$

Therefore, R_n is proportional to $1/n$.

From the expressions of C_{Y21} and C_{Y12}, which are complex conjugate, the elements C_{A12} and C_{A21} of the chain noise correlation matrix are given by:

$$C_{A12} = Y_{11}^* \frac{C_{Y22}}{\left|Y_{21}\right|^2} - \frac{C_{Y21}}{Y_{21}} \tag{E.11}$$

and $$C_{A21} = Y_{11} \frac{C_{Y22}}{\left|Y_{21}\right|^2} - \frac{C_{Y12}}{Y_{21}^*} \tag{E.12}$$

The values of C_{A12} and C_{A21} remain unchanged when identical two-port networks are connected in parallel. Because $C_{A21} = \frac{F_{\min} - 1}{2} - R_n Y_{sopt}$, this expression is not related to n and remains constant for parallel networks.

From (E.9), it is found that C_{A22} is proportional to n. Because $C_{A22} = R_n \left|Y_{sopt}\right|^2$ and R_n is proportional to $1/n$, Y_{sopt} is proportional to n, R_{sopt} is proportional to $1/n$. Therefore, $R_n Y_{sopt}$ is not related to n and F_{min} remains unchanged when n identical two-port networks are connected in parallel. The noise factor is given by:

$$F_n = F_{\min} + \frac{R_n}{nG_s}\left|Y_s - nY_{sopt}\right|^2 \tag{E.13}$$

ADDENDUM F SMALL-SIGNAL PARAMETERS FOR THE CE

Some parameters of the IBM SiGe BiCMOS8HP process cannot be obtained directly from SpectreRF. These parameters are extracted from the Z- and Y-parameters.

Extraction of C_{bc}

The base-collector capacitance can be extracted from the expressions of Z_{22} and Z_{21} in (B.48) and (B.42).

$$Z_{22} - Z_{21} = \frac{\frac{C_{be}}{C_{bc}} + \frac{g_{be}}{j\omega C_{bc}} + \frac{g_m}{j\omega C_{bc}}}{g_m + g_{be} + j\omega C_{be}} = \frac{\frac{j\omega C_{be} + g_{be} + g_m}{j\omega C_{bc}}}{g_m + g_{be} + j\omega C_{be}} = \frac{1}{j\omega C_{bc}} \tag{F.1}$$

$$C_{bc} = -\frac{1}{\omega \Im\{Z_{22} - Z_{21}\}} \tag{F.2}$$

Extraction of C_{be}

From (B.6) and (B.11),

$$Y_{11} + Y_{12} = \frac{g_{be} + j\omega C_{be}}{1 + r_b\left(g_{be} + j\omega C_{be} + j\omega C_{bc}\right) + g_m r_e\left(j\omega C_{bc} r_b + 1\right)} \tag{F.3}$$

If the base and emitter resistances r_b and r_e are neglected,

$$\Im\left(Y_{11} + Y_{12}\right) \approx \omega C_{be} \tag{F.4}$$

$$C_{be} \approx \frac{\Im\left(Y_{11} + Y_{12}\right)}{\omega} \tag{F.5}$$

Extraction of r_b

The base parasitic resistance r_b can be extracted by subtracting Z_{12} from Z_{11}.

$$Z_{11} - Z_{12} = \frac{r_b\left(g_{be} + j\omega C_{be} + g_m\right)}{g_m + g_{be} + j\omega C_{be}} = r_b \tag{F.6}$$

Extraction of r_e

$$Z_{12} = \frac{Z_{be} + r_e\left(1 + j\omega C_{be} Z_{be} + g_m Z_{be}\right)}{g_m Z_{be} + 1 + j\omega C_{be} Z_{be}} \tag{F.7}$$

Assuming that $\left|g_m Z_{be}\right| >> 1$, Z_{12} is approximated by the expression:

$$Z_{12} \cong \frac{Z_{be} + r_e\left(j\omega C_{be} Z_{be} + g_m Z_{be}\right)}{g_m Z_{be} + j\omega C_{be} Z_{be}} \tag{F.8}$$

$$Z_{12} \cong r_e + \frac{1}{g_m + j\omega C_{be}} = r_e + \frac{g_m - j\omega C_{be}}{g_m^2 + \left(\omega C_{be}\right)^2} \tag{F.9}$$

$$\Re\left\{Z_{12}\right\} \cong r_e + \frac{g_m}{g_m^2 + \left(\omega C_{be}\right)^2} \tag{F.10}$$

$$r_e \cong \lim_{\omega -> 0}\left\{\Re\left\{Z_{12}\right\}\right\} - \frac{1}{g_m} \tag{F.11}$$

Extraction of g_m

The transconductance can be evaluated easily when r_b and r_e are assumed to be negligible. The expressions of Y_{12} and Y_{21} are simplified as follows:

$$Y_{12} \cong -j\omega C_{bc} \tag{F.12}$$

$$Y_{21} \cong \left(g_m - j\omega C_{bc}\right) \tag{F.13}$$

$$g_m = \left|Y_{21} - Y_{12}\right| \tag{F.14}$$

ADDENDUM G MATLAB™ CODE: OUTPUT MATCHING

```
% MAIN SCRIPT. AN UNCONSTRAINED NONLINEAR OPTIMISATION BASED ON A
% MATLAB RF Toolbox DESIGN EXAMPLE IS USED:
% TITLE: Designing Broadband Matching Networks (Part 1: Antenna)
% MATLAB RF Toolbox R2017a, The MathWorks, Inc., Natick,
% Massachusetts, United States.
% AVAILABILITY: http://www.mathworks.com/help/rf/examples

% MATCHING NETWORK SETUP PARAMETERS
F_low      = 300e6;                    % Lower frequency(Hz)
F_high     = 1400e6;                   % Higher frequency(Hz)
B_W        = F_high - F_low;           % Bandwidth(Hz)
cfreq      = (F_low + F_high)*0.5;     % Center Frequency(Hz)
rad_H      = 2*pi*F_high;              % Higher frequency(rad/s)
rad_L      = 2*pi*F_low;               % Lower frequency(rad/s)
rad_0      = sqrt(rad_L*rad_H);        % Geometric mean(rad/s)

% IMPEDANCE PARAMETERS
Z0       = 50;        % Reference impedance (ohm)
Rs       = 50;        % Source resistance (ohm)
Cout     = 4.2e-13;   % Measured output capacitance of the cascode
Ro       = 90;        % Output resistance of the cascode in
% parallel with Cout (ohm)
N_points = 512;       % Number of frequency points to analyse

% SETTING VARIABLES
F_array      = linspace(F_low , F_high, N_points); % Array of
% N_points frequencies equally spaced from F_low to F_high to be
% analysed
F_rad        = 2*pi*F_array; % Frequency array in radians/sec
Ys = 1./Ro  + (1i*F_rad*Cout); % Complex source admittance(1/ohm)
Zs = Rs               % The signal is comes from the 50 ohms load
% side(as per Figure 5.23 from Chapter 5 of the thesis)
Zl = 1./Ys            % The load is the output impedance of the
% cascode (as per Figure 5.23 of the thesis)
 R_Load = (Zl - Zs)./(Zl + Zs);    % Reflection coefficient(Load
% plane), no matching network
P_Load = 10*log10(1 - abs(R_Load).^2);  % Power to load, no
```

```
% matching network

% PLOT THE REFLECTION COEFFICIENT ON A SMITH CHART
fig1  =  figure;
l     =  smithchart(R_Load);
%l.LineWidth = 2;
set(l, 'LineWidth', 2);
%l.Color = 'r';
set(l, 'Color', 'r');
legend('\Gamma_L'); %

% PLOT DELIVERED POWER VERSUS FREQUENCY
fig2   = figure;
plot(F_array.*1e-6, P_Load, 'r');
grid on;
title('Power delivered to load - No matching network')
xlabel('Frequency (MHz)')
ylabel('Magnitude (decibels)')
legend('G_t','Location','Best')

% THE INITIAL TOPOLOGY IS A LOW-PASS SECOND-ORDER BUTTERWORTH
% FILTER WITH A SHUNT CAPACITOR ON THE CASCODE SIDE AND AN
% INDUCTOR ON THE LOAD SIDE. THE PASS-BAND FILTER RESULTS FROM A
% LOW-PASS TO BAND-PASS TRANSFORMATION (SHUNT CAP => SHUNT CAP +
% SHUNT INDUCTOR, SERIE IND => SERIES CAP + SERIES INDUCTOR

% SETTING INITIAL VALUES OF THE PASSBAND FILTER AND CREATE THE
% MATCHING OBJECT
N = 2;                     % N is the order of a low-pass filter
LCprototype = [1.41422 0.70711]; % Coefficients of a 2nd order
% normalised low-pass Butterworth filter in a vector for an
% infinite load impedance

% CREATE AND INITIALISE TWO VECTORS EACH WITH N ELEMENTS
Lvalues = zeros(N,1);      % Values of inductors for the topology
Cvalues = zeros(N,1);      % Values of capacitors for the topology

% EXTRACT, DENORMALISE AND ALLOCATE ODD ELEMENTS OF LCprototype
% TO Lvalues & Cvalues. ODD ELEMENTS ARE IN SERIES BRANCHES
% THE FIRST ELEMENT IS AN INDUCTOR
Lvalues(1:2:end)=LCprototype(1:2:end).*Zs./(rad_H - rad_L);
% Series L's (H)and denormalisation
Cvalues(1:2:end)= (rad_H -
rad_L)./(Zs.*(rad_0^2).*LCprototype(1:2:end));
% Series C's (F)and denormalisation

% EXTRACT, DENORMALISE AND ALLOCATE EVEN ELEMENTS OF LCprototype
% TO Lvalues & Cvalues. EVEN ELEMENTS ARE IN SHUNT BRANCHES
Lvalues(2:2:end) = ((rad_H -
rad_L)*Zs)./((rad_0^2).*LCprototype(2:2:end)); % Shunt L's and
% denormalisation
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Cvalues(2:2:end) = LCprototype(2:2:end)./((rad_H - rad_L).*Zs);
% Shunt C's and denormalisation

% CREATE A TEE BAND-PASS NETWORK FROM THE VALUES RESULTING FROM
% THE LOW TO BAND-PASS TRANSFORMATION
MatchingNW = rfckt.lcbandpasstee('C',Cvalues,'L',Lvalues);
% MatchingNW is the created matching object
L_Initial  = Lvalues;       % Copy initial L values for comparison
C_Initial  = Cvalues        % Copy initial C values for comparison


% OPTIMISE THE MATCHING NETWORK
nIter    = 512;             % Max No of Iterations
options  = optimset('Display','iter','MaxIter',nIter);  % The
% structure with optimisation options is set
% Default values are used for the optimisation parameters
% TolX(1×e-04)and TolFun (1×e-04)
% The objective function is broadband_matching()

L_Optimized = [Lvalues(1)  Lvalues(end)]; % Series and shunt
% inductances are the variables to optimise
L_Optimized = fminsearch(@(L_Optimized)
broadband_matching(MatchingNW,L_Optimized,F_array,Zl,Zs,Z0),L_Opti
mized,options);

MatchingNW.L(1)= L_Optimized(1); % Update the matching network
% inductor L1
MatchingNW.L(end)= L_Optimized(2);% Update the matching network
% inductor L2

% ANALYSE AND DISPLAY OPTIMISATION RESULTS
analyze(MatchingNW,F_array,Zl,Zs,Z0);
hold all;
hline = smithchart(R_Load);
% hline.Color = 'r';
set(hline, 'Color', 'r');
set(hline, 'LineWidth', 2);
legend('\Gamma_i_n','\Gamma_L');
hold off;

% PLOT THE POWER DELIVERED TO THE LOAD, THROUGH THE MATCHING
% NETWORK
fig3  = figure;
h1    = plot(MatchingNW, 'Gt');
set(h1,'LineWidth', 2);
hold on;
h2    = plot(F_array.*1e-9, P_Load, 'r');
set(h2,'LineWidth', 2);
grid on;
title('Power delivered to load')
xlabel('Frequency (GHz)')
ylabel('Magnitude (decibels)')
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legend('Optimized network','No matching
network','Location','Best');

% PRINT THE VALUES CALCULATED
L1_Initial   = L_Initial(1)
L1_Optimized = L_Optimized(1)
L2_Initial   = L_Initial(end)
L2_Optimized = L_Optimized(end)
C1_Initial   = C_Initial(1)
C2_Initial   = C_Initial(end)

% FUNCTION "broadband_matching.m" CALLED BY THE MAIN SCRIPT
function output =
broadband_matching(MatchingNW,Lvalues,F_array,Zl,Zs,Z0
)
% ADAPTED FROM ANTENNAMATCHOBJECTIVEFUN, AN OBJECTIVE
% FUNCTION OF RF Toolbox DEMO:
% Designing Broadband Matching Networks (Part I: Antenna)

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% ALL Lvalues MUST BE POSITIVE
if any(Lvalues<=0)
    output = Inf;
    return;
end

% UPDATE VALUES IN THE BAND-PASS NETWORK NETWORK
MatchingNW.L(1)   = Lvalues(1);
MatchingNW.L(end) = Lvalues(end);

% ANALYSE THE NETWORK TO DETERMINE ITS PARAMETERS
Npts  =  length(F_array);
analyze(MatchingNW, F_array, Zl, Zs, Z0);

% DETERMINE THE REFLECTION COEFFICIENT(INPUT)'gammaIn'
[GammaGt]  = calculate(MatchingNW, 'gammain', 'Gt', 'none');
gammaIn    = zeros(Npts,1);
gammaIn(1:Npts, 1) = GammaGt{1}(1:Npts, 1);

% THE COST FUNCTION IS THE MEAN OF THE |REFLECTION COEFFICIENTS|
output  = mean(abs(gammaIn));

% ANIMATE
l = smith(MatchingNW,'gammaIn');
set(l, 'LineWidth', 2);
set(l,'DisplayName','Optimizing \Gamma_i_n');
drawnow;
```