ON THE IMPROVEMENT OF PHASE NOISE IN WIDEBAND FREQUENCY SYNTHESIZERS

by

Pandelani Reuben Munyai

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SUMMARY

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Pandelani Reuben Munyai

Supervisor(s):	Prof. B.J.T Maharaj
Department:	Electrical, Electronic and Computer Engineering
University:	University of Pretoria
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Wireless communication systems are based on frequency synthesizers that generate carrier signals, which are used to transmit information. Frequency synthesizers use voltage controlled oscillators (VCO) to produce the required frequencies within a specified period of time. In the process of generating frequency, the VCO and other electronic components such as amplifiers produce some unwanted short-term frequency variations, which cause frequency instability within the frequency of interest known as phase noise (PN). PN has a negative impact on the performance of the overall wireless communication system. A literature study conducted on this research reveals that the existing PN cancellation techniques have some limitations and drawbacks that require further attention.

A new PN correction technique based on the combination of least mean square (LMS) adaptive filtering and single-loop single-bit Sigma Delta ($\Sigma\Delta$) modulator is proposed. The new design is also based on the Cascaded Resonator Feedback (CRFB) architecture. The noise transfer function (NTF) of the architecture was formulated in way that made it possible to stabilize the frequency fluctuations within the in-band (frequency of interest) by locating its poles and zeros within the unit circle.

The new design was simulated and tested on a commercially available software tool called Agilent

Advanced Design System (ADS). Simulation results show that the new technique achieves better results when compared with existing techniques as it achieves a 104 dB signal-to-noise (SNR), which is an improvement of 9 dB when compared with the existing technique accessed from the latest publications. The new design also achieves a clean signal with minimal spurious tones within the in-band with a phase noise level of -141 dBc/Hz (lower phase noise level by 28 dBc/Hz) when compared with the existing techniques.

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converters
ADS	Advanced Design System
AR	Auto-Regressive
AWGN	Additive White Gaussian Noise
BPSK	Binary Phase Shift Keying
BER	Bit Error Rate
BS	Base Station
CPE	Common Phase Error
CRFB	Cascade of Resonators with Feedback
DAC	Digital to Analog Converters
DSS	Direct Digital Synthesis
EKF	Extended Kalman Filter
FDC	Frequency-to-Digital Converter
FNPLL	Fractional-N Phase locked Loop
HSPA	High Speed Packet Access
ICI	Inter Carrier Interference
i.i.d	Independent Identically Distributed
IBN	In-band Noise
ISI	Intersymbol Interference
KF	Kalman Filter
LMS	Least Mean Square
LOS	Line Of Sight
LS	Least Square
LTE	Long Term Evolution
MASH	Multi-stAge noise SHaping
ML	Maximum Likelihood
MLE	Maximum Likelihood Estimation
MMSE	Minimum Mean Square Error
MS	Mobile Station
MSE	Mean Square Error
NPM	Normalized Projection Misalignment
NTF	Noise Transfer Function

OFDM	Orthogonal Frequency Division Multiplexing
OBG	Out of Bound Gain
OSR	Oversampling Ratio
PLL	Phase-Lock Loop
PDF	Probability Distribution Function
PSD	Power Spectral Density
PN	Phase Noise
PSK	Phase Shift Key
QAM	Quadrature Amplitude Modulation
RLS	Recursive Least Square
RF	Radio Frequency
SISO	Single Input Single Output
SQNR	Signal to Quantization Noise Ratio
SNR	Signal to Noise Ratio
STF	Signal Transfer Function
VCO	Voltage Control Oscillator

PN Phase Noise
PSK Phase Shift Key
QAM Quadrature Amplitude Modulation
RLS Recursive Least Square
RF Radio Frequency
SISO Single Input Single Output
SQNR Signal to Quantization Noise Ratio
SNR Signal to Noise Ratio
STF Signal Transfer Function
VCO Voltage Control Oscillator

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CHAPTER 1 INTRODUCTION

1.1 BACKGROUND

The emergence of phase noise (PN) at the transceiver ends affects the performance of modern wireless communication systems negatively. Wireless communications systems use frequency synthesizers to generate carrier signals that contain useful information to be transmitted. Frequency synthesizers consist of signal generator components (voltage control oscillator (VCO), local oscillator (LO), Phase Frequency Detector (PFD), Charge-Pump (CP) and Loop Filter (LF)). The LO generates unwanted time-varying and randomly distributed waveforms that form the basis of the PN errors that emerge in the baseband signal as an additional phase and amplitude modulated waveform propagated through a dissipative Additive White Gaussian Noise (AWGN) channel.

Estimating the received data sequence in the presence of PN and additive white noise poses major challenges to the receivers and it is a problem that requires attention to enhance the performance of modern wireless communication system.

The signal to noise ratio (SNR), which provides immunity to a wireless system in a multipath fading environment, gets impacted by the emergence of PN in the transceiver ends. The reduction of SNR causes the wireless communication systems to degrade as the bit error rate of the system increases. PN errors also affect symbol or data sequence synchronization, which causes the receiver to misinterpret the received data. It is for these reasons that PN remains a major problem in modern wireless communication and it is very critical for researchers and design engineers to have a better understanding of the behavior of PN to be able to design wireless communication systems with low levels of PN.

1.1.1 Fundamentals of Phase Noise

PN can be realized as nothing else but the short-term random fluctuations in the phase or frequency of a signal, which can be expressed in terms of a sinusoid waveform as;

$$V(t) = \Big[V_o + \lambda(t)\Big] \cos\Big(2\omega_o t + \phi(t)\Big). \tag{1.1}$$

The V_o, λ, ω and ϕ terms in equation (1.1) are defined as follows;

$$\begin{aligned} V_o &= \text{The Peak amplitude in Volts} \\ \lambda(t) &= \text{Time-varying amplitude or noise amplitude.} \\ \omega_o &= \text{Natural frequency of the signal in rad/sec.} \\ \phi(t) &= \text{Time-varying PN or phase fluctuation of the output signal.} \end{aligned} \tag{1.2}$$

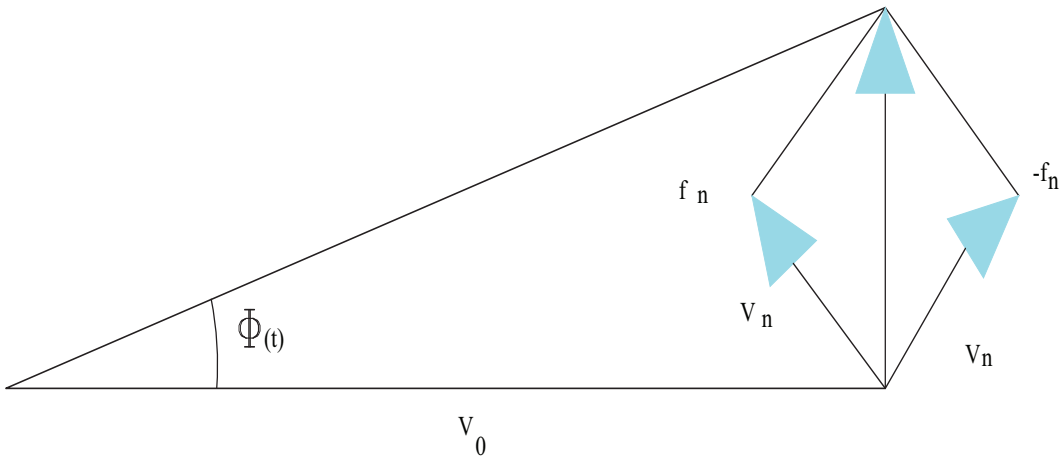

Figure 1.1: Phasor diagram representing two noise components at offset $\pm f_n$.

From Equation (1.1) and Figure 1.1 it is possible to model the PN contribution as narrowband Frequency modulation (FM), where the corresponding phase modulation is given by [1];

$$\begin{aligned}\phi(t) &= \frac{2V_n \sin(\omega_n t)}{V_o} \\ &= \frac{2V_n \sin(2\pi f_n t)}{V_o}.\end{aligned} \tag{1.3}$$

If the sinusoidal waveform in (1.1) is assumed to follow a random process, the PN can be defined in terms of its power spectral density function as;

$$L(f_m) = \frac{S_v(f_m)}{\lambda^2(t)/2}. \tag{1.4}$$

$$\begin{aligned}S_v(f_m) &= \text{The Power Spectral Density of the sinusoidal signal , V(t).} \\ \lambda(t) &= \text{Time-varying amplitude or noise amplitude.}\end{aligned} \tag{1.5}$$

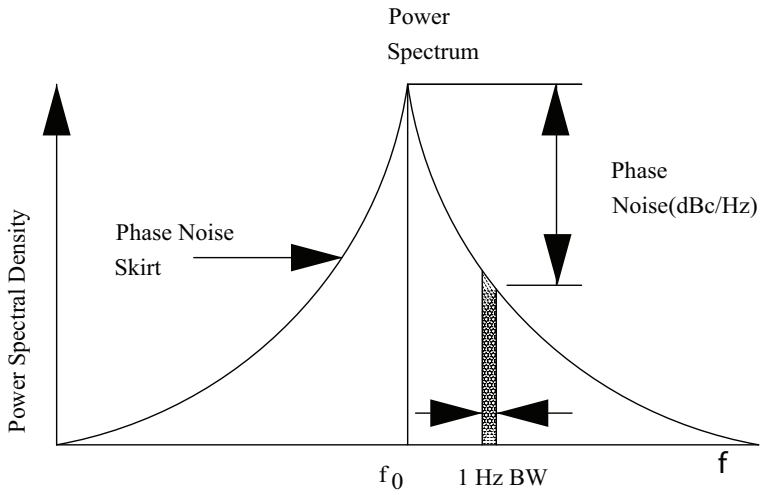

Figure 1.2: PN power spectrum.

As shown in Figure 1.2, PN can be expressed as a ratio of noise contained in a 1-Hz bandwidth at a certain frequency offset, f_m, to the amplitude of the oscillator signal with a carrier frequency f_o.

The power spectral density of a single side-band noise of Figure 1.2 is given by;

$$(\Delta\omega) = 10\log\left[\frac{P_{SSB}(\omega_0+\Delta\omega,1Hz)}{P_{signal}}\right]. \tag{1.6}$$

where

$P_{SSB}(\omega_0+\Delta\omega,1Hz)$ = SSB power of an output frequency spectrum with respect to $\Delta\omega$ measured from 1Hz

P_{signal} = Total carrier power of the output spectrum

(1.7)

1.1.2 Components of PN

Various PN components are normally modeled with the Leeson model, which suggests that PN consists of white noise, flicker PN, random phase walk, flicker frequency noise and random frequency walk. The Leeson model is given by [2, 3];

$$\begin{aligned} L(fm) &= 10\log\frac{FKT}{2P_{avg}}\left[1+\frac{f_c}{f_m}+(\frac{f_o^2}{2fmQ})^2(1+\frac{fc}{fm})\right] \\ &= 10\log\frac{FKT}{2P_{avg}}\left[1+\frac{f_o}{f_m}+\frac{1}{f_o^2}(\frac{f_o^2}{2Q})^2+\frac{f_o}{f^3}(\frac{f_o}{2Q})^2\right]. \end{aligned} \tag{1.8}$$

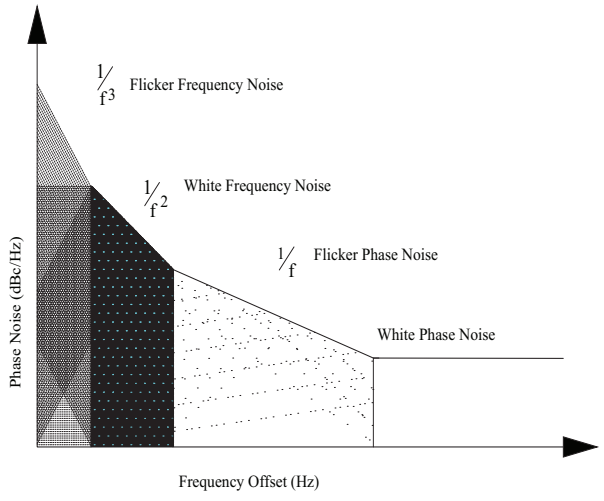

Figure 1.3: Representation of PN components

The Leeson model suggests that PN may be improved by increasing the signal power, reducing the device flicker frequency (f_o) and the half bandwidth term $(f_o/2Q)$.

However, the main challenge with PN is that oscillators tend to amplify any noises that are closer to their harmonics and oscillation frequency, which makes it more complicated for modern communication systems that use multiple transmitters and receivers.

The single side-band (SSB) noise spectral density can be used to determine the maximum allowable PN required to achieve the desired signal-to-noise ratio (SNR) by estimating the in-band noise relative to the carrier using Figure 1.4 as follows;

$$P_{noise} = \int_{\Delta f_L}^{\Delta f_U} (\Delta f) d(\delta f). \tag{1.9}$$

The slope $(1/f^2)$ can be determined from Figure 1.3 as $(\Delta f) = k/\delta f^2$ such that;

$$\begin{aligned} P_{noise} &= \int_{\Delta f_L}^{\Delta f_U} \frac{k}{\Delta f} d(\Delta) \\ &= \frac{k(\Delta f_U - \Delta f_L)}{\sqrt{(\Delta f_L - \Delta f_U)^2}} \\ &= (\sqrt{\delta f_L \times \delta f_U})(\Delta f_U - \Delta f_L). \end{aligned} \tag{1.10}$$

If the minimum SNR is known, the maximum allowable PN can be determined from Equation (1.11);

$$10\log(P_{noise}) = 10\log(P_{signal}) - 10\log(SNR) - 10\log(P_{Interfere} - 10\log(\Delta f_U - \Delta f_L)). \tag{1.11}$$

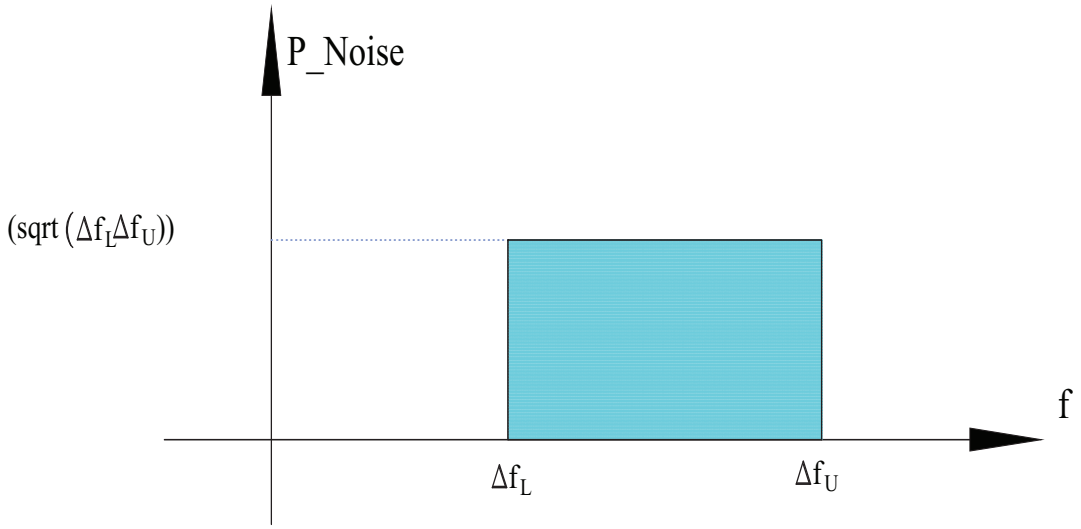

Figure 1.4: Representation of PN.

1.1.3 Frequency Synthesizers

Frequency synthesizers that are used to generate carrier waves employ local oscillators that use ΣΔ fractional PLL to eliminate phase noise components in the wide-band (GHz) frequency range. The wide-band PLL is very useful in many applications due to its ability to filter the flicker noise $(\frac{1}{f^3})$ generated by the oscillator component. The range of frequencies generated by the fractional PLL are used for up-converting and down-converting the transmitted and received data sequences.

There are two types of fraction PLL synthesizers that are used to generate a wide range of frequency bands, namely;

- Interger-N PLL
- Fractional-N PLL

1.1.3.1 Integer-N PLL

The desired frequency output (f_{vco}) is generated by multiplying the reference frequency with the negative feedback path as follows;

$$f_{vco} = f_r \times N. \tag{1.12}$$

1.1.3.2 Fractional-N Frequency synthesis

The multiplication of the reference frequency by an integer N has some unintended consequences as it raises the phase margin of the signal by a factor of $20\log(N)$ dB. For example, of a channel spacing of 30 kHz (for cellular) is assumed, a noise of about 90 dB will be added to the PFD $(20\log(30,000))$. To avoid this situation a fractional-N synthesis is adopted, which uses division by fractional ratios as opposed to integer ratios.

1.1.4 Sigma Delta Quantization Noise

The fundamental principle of quantization noise (error) is depicted in Figure 1.5, which shows a classic noise shaping characteristics of a sigma delta modulator.

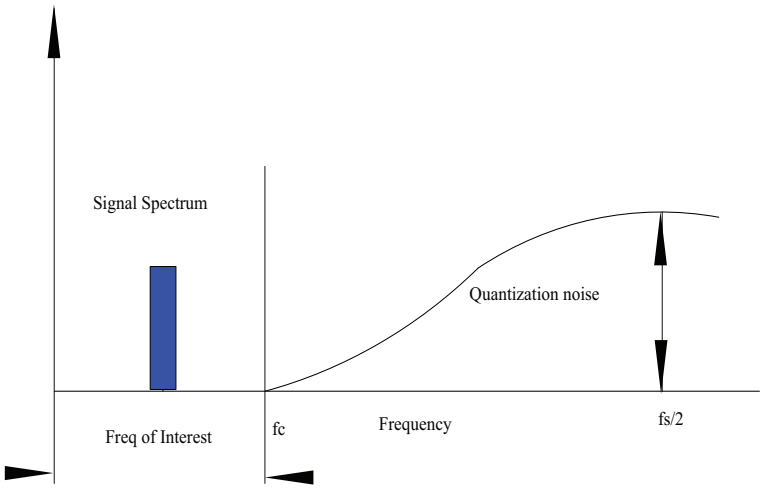

Figure 1.5: Depiction of Frequency of Interest and quantization noise.

The quantization noise is eliminated by the implementation of the digital filter (low pass filter) at the end of the signal delta modulator, which retains the signal of interest and eliminates quantization noise by pushing them to the higher frequency portion.

1.1.5 Performance criteria for PN reduction techniques

Several studies conducted in the field of noise cancellation techniques employed the mean square error (MSE), convergence rate, tracking capability and normalized projection misalignment (NPM) as performance measures [4, 5, 6].

1.1.5.1 Mean Square Error

If the source signal is assumed to be uncorrelated with the emerging random sequence noise, the filter algorithm such as adaptive filter, will seek to minimize the square of the error output. The adaptive filter reduces the noise part of the contaminated signal by subtracting the undesired signal from the main or reference signal. The mean square error (MSE) for the convergence parameters of the error and estimated signals is statically modeled as;

$$MSE = \frac{1}{N}\sum_{n=0}^{N}\left[x(n) - (\hat{x})\right]^2. \tag{1.13}$$

where

$x(n) =$ is the original signal.

$(\hat{x}) =$ is the filter output.

The adaptive algorithm seeks to minimize the MSE between the error and the estimated signal. An algorithm is deemed to have better performance if it convergences faster at less MSE. Larger MSE values implies that the algorithm fluctuated about the filter coefficients after undergoing a high sample rate or iteration number.

1.1.5.2 Convergence rate

Many PN cancellation techniques that are based on adaptive algorithms are said to have high performance if they converge faster within few iterations [5]. In other words, it is desirable to design an algorithm that achieves the steady state MSE within few iteration.

1.1.5.3 Tracking capability

The tracking capability is a performance measure that indicates the ability of the algorithm to track statistical variations within a non-stationary environment.

1.1.5.4 Normalized Projection Misalignment (NPM)

The normalized projection misalignment (NPM) performance criterion provides a means of measuring separation between the estimated and original impulse responses. The closeness between these two impulse responses can be determined by Equation(1.14).

$$NPM(n) = 20\log\left[\frac{1}{\|y\|}\frac{\|y - y^T\hat{y}(n)\|}{\hat{y}^T\hat{y}(n)}\right]. \tag{1.14}$$

where

$y =$ The impulse response to the original signal to be estimated.

A well designed filter should approximate 0 dB NPM, meaning that the estimated and original impulses are closely aligned.

1.1.5.5 Computational complexity

Although many algorithms perform well at a cost of high complexity, it is normally desirable to reduce the complexity as higher computational complexity requires higher storage capacity which comes at a cost. Another problem of higher computational complexity is that it takes longer computation time, which may result in some errors and affects the quality of the proposed solution.

1.1.5.6 SNR and SNDR

The SNR and signal to noise and distortion ratio (SNDR) are important performance metrics that are widely used in the performance analysis of $\Sigma\Delta$ modulators. The SNR is used to measure the sensitivity of the transceiver. The greater the difference between the signal power and the noise power the better the performance of the transceiver sensitivity. This justifies why it is necessary to have a transceiver with higher SNR for better performance. SNDR is even a better performance metric than SNR in that it takes signal harmonics into consideration and compares them with the power of the noise signal or residual signal. The performance level of these metrics are depicted in Figure 1.6.

The spurious free dynamic range (SFDR) is the minimum level of signal power that can be identified from a dominant interfering signal. As shown in Figure 1.6, the SFDR can be determined as the difference between the root mean square (rms) value of the carrier power (dBc) and the rms value of the next signal with the highest visible spur. This implies that dynamic range is free of spurious frequencies. SFDR is normally represented as full-scale (dBFS) or with the actual amplitude of the carrier (dBc). The SNDR is another important metric which is given by the ratio of the rms signal amplitude to the mean value of the root-sum-square (rss) of all harmonics and spectral components. The significance of the SNDR is that it includes all components that cause signal distortion. SNDR is almost

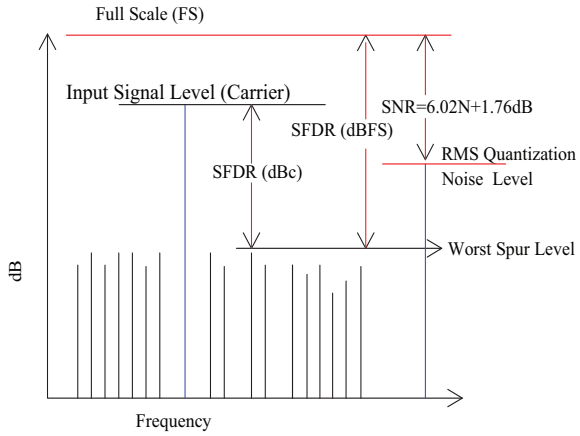

Figure 1.6: Phase Noise performance metrics.

the same as the SNR except that the frequency harmonics are excluded from the SNR calculation, which makes it easier to deal with noise terms only. SNR is used to measure the noise performance of the receiver by comparing the signal and noise level of the known signal level [7].

The effective number of bits (ENOB) is another metric that is used to measure the dynamic range where the associated bits are used to specify the system resolution. The effective number of bits (ENOB) is given by;

$$ENOB = \frac{SNDR - 1.76dB}{6.02} \tag{1.15}$$

$$SNR = 6.02 \times ENOB - 1.767.$$

where the 6.02 term is used to convert decibel $(\log_{10} x)$ to $(\log_2 x)$, i.e., $(6.02 = 20log_2)$.

1.2 RELATED WORK

Multi-carrier systems are hailed as high capacity systems that enhance the data rates of broadband networks (3G, HSPA+, and LTE). However they are very sensitive to PN as they cause severe signal degradation in multipath fading environments [8]. In [9, 10, 11, 12] the impact, influence and effects of PN on multi-carrier system were analyzed where it was shown that PN errors remain the major cause of impairments in wireless communication systems. In [13] the term PN is described as the short-term random fluctuations of a signal caused by the transmitter and receiver oscillators. The lack of synchronization at both the receiver and transmitter oscillator causes random PN that can be described by the Brownian motion process where the zero mean, line-width and variance terms of the PN are discussed in [13]. PN causes sub-carrier signals to lose orthogonality patterns that results in common phase error (CPE) and inter-carrier interference (ICI) [13], which causes interference among sub-carriers and reduce the performance of overall system. The correction techniques that cancels CPE in multi-carrier systems such as orthogonal frequency division multiplex (OFDM) was presented in [11] , which increases the theoretical SNR marginally. However this technique is limited by the radio symbol rate, which makes it difficult to correct LO PN for the system whose LO's frequency offset is closer to the actual radio symbol rate.

Several noise cancellation techniques (such least mean square, recursive least mean square, Kalman filter, phase locked loop) have been proposed to mitigate the effect of PN on multi-carrier systems [14, 15, 16, 17, 18, 19].

Recently Kaned [20] investigated the effect of PN on the equalization of communication channels using least mean square (LSM) and recursive least square (RLS), where it was observed that LSM and RLS techniques improved the bit error performance (BER) of the communications when compared to the system that operates without any PN correction technique. Awachat and Godbole [21] evaluated the performance of LMS algorithm as a technique for noise cancellation in speech signals. LMS has been shown to be more stable within the in-band. Although LMS has the desirable stability characteristic with less signal fluctuation in the in-band, it takes some time to filter the noise completely. This results in a lengthy convergence rate that can be improved by varying the step size of the algorithm through trial and error. In a bid to improve the performance of the LMS, an RLS technique was introduced and later evaluated by Dhubkarya *et al*. [4]. In their investigations, Dhubkarya *et al*. simulated and evaluated the performance of adaptive algorithms (RLS and LMS) in terms of the performance

criteria (mean square error, convergence rate, computational complexity, stability and signal to noise improvement) and observed that RLS estimates errors quicker with a faster convergence rate albeit at a cost of high complexity.

Another adaptive filter that had been used as a noise cancellation technique is the Kalman Filter [22], a technique that was designed on the premise of the recursive least square error (RLSE) with low and efficient computational complexity. Recent studies by Bhattacharjee and Das [22] on the performance evaluation of the Wierner and Kalman Filters show that Kalman Filter is an efficient noise reduction technique although it achieved significant results when used in combination with the Wierner Filter.

In [14], a decision directed Extended Kalman Filter (EKF) was proposed for tracking the PN errors in wireless sensor networks due to its ability to filter and track random signal, where it was found that the BER performance results show some encouraging performance as they were close to that of synchronous case. However, a fundamental drawback of this technique is that it is limited to linear and Gaussian assumptions [14]. Although the Kalman Filter is widely used to correct and estimate PN errors it does not achieve optimal performance due to the complex receiver structure that makes it difficult to align all model coefficients. While the EKF might be an ideal method to deal with PN caused by channel imperfections, it lacks some intelligence to correct PN errors caused by the imperfections of the local oscillators in the transmitter and receiver ends respectively [23].

Another technique that estimates the carrier phase from the received signal is the Phase-Lock Loop (PLL). PLL was proposed to filter unwanted PN in multiple channel applications [24]. Since PLL schemes are based on sets of linear equations, interpreting and analyzing the results of PLL in terms of physical behavior of the system becomes very difficult and time consuming due to the structure of their complicated and difficult designs [25]. Although PLL technique is very popular in correcting PN errors, it's suitability to correct PN errors has been widely applied in SISO systems and to some extent in multicarrier systems such as OFDM.

The effect of PN can be eliminated by improving the performance of the voltage control oscillator (VCO). Unfortunately, the improvement of the VCO tends to be a costly exercise, which further strengthens the case for the proposal of a robust PN correction method that is simple to implement.

The squaring loop carrier phase recovery technique discussed in [26] tracks the phase of the incoming

signal perfectly. However it should be pointed out that the significant BER results achieved by this technique were based on simple modulation schemes (such as BPSK, PSK) and have not been tested for a multicarrier system.

A low noise-phase modulator with a finite impulse response filtering and sigma delta (ΣΔ) modulator fractional-N Phase locked loop (FNPLL) frequency synthesizers was introduced and investigated in [27] and found to be capable of generating carrier waves with well-defined carrier frequencies that are free of spurious tones. The requirement to design systems that have less or no spurious tones with the frequency of interest necessitated further frequency synthesizer's evolution and more advanced architectures that seek to minimize spurious tones to the lowest level.

As shown in Figure 1.7, the output of the ΣΔ modulator controls the divide modulo, which realizes the fractional division and converts local oscillator (LO) frequency and frequency step to fractional multiples of reference frequency, which is normally tuned within the frequency of interest. The signal is controlled by the fractional division, D, which is obtained from the output of the ΣΔ modulator's accumulator.

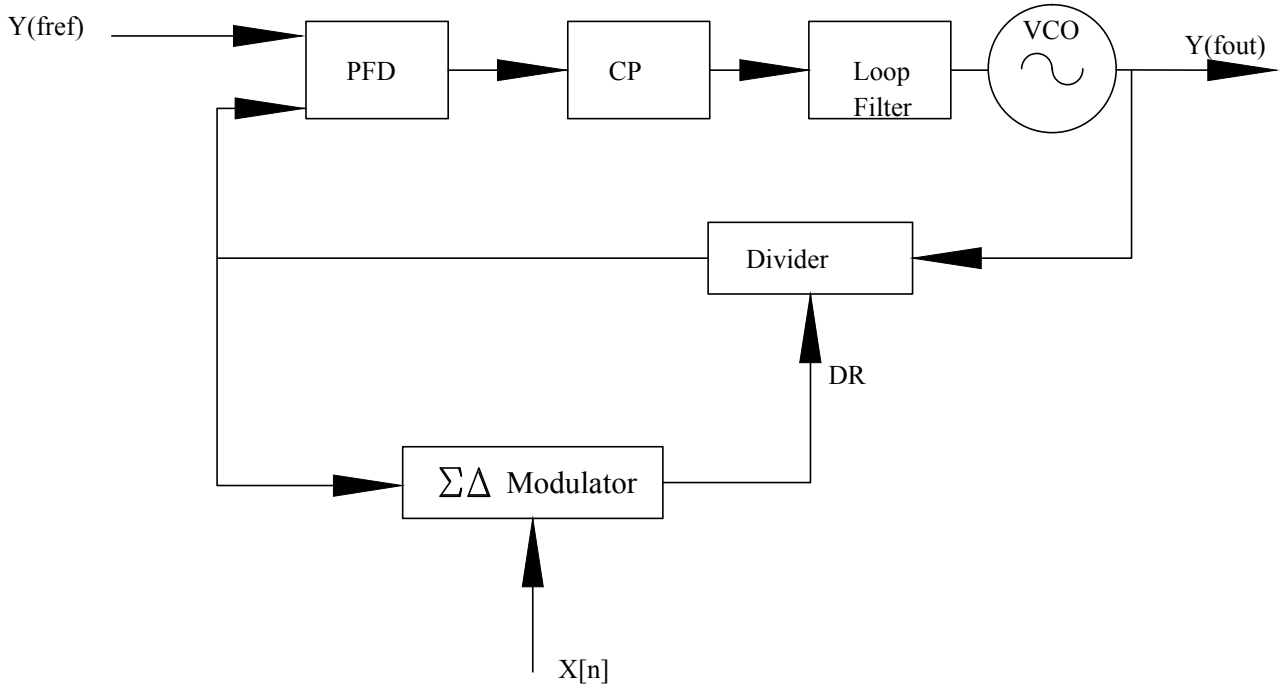

Figure 1.7: Schematic representation of ΣΔ Fractional-N PLL [28].

The reference output is determined by assuming that the synthesizer divides the reference output by D_0+1 every C_0 cycles and by D_0 the rest of the times, the average ratio will be $D_{avg} = D_0 + \frac{1}{C_0}$ and the resulting VCO reference output will be given by Equation (1.16);

$$\begin{aligned} Y_{fref} &= \left[(D_0+1)(\frac{1}{C_0}) + N(1-\frac{1}{C_0})\right] \\ &= \left(D_0 + \frac{1}{C_0}\right) Y_{fout}. \end{aligned} \tag{1.16}$$

Equation (1.16) shows that the output bit stream is cyclical and repetitive, which may result in unnecessary visible harmonics.

This approach has a drawback where the output is completely locked to the reference frequency of the PLL. It is also noted in [29] that an attempt to reduce the reference frequency has undesired consequences as it increases settling time, which in turn decreases the bandwidth of the overall system and introduces system instability. When the bandwidth is reduced significantly it becomes difficult to flatten and reduce noise with the in-band or frequency of interest.

The ΣΔ modulator as shown in Figure 1.7 was included to take advantage of its ability to move the quantization noises away from the frequency of interest, which in turn can be removed by the loop filter (LF). The FNPLL's ability to handle the additional ΣΔ component gives them the flexibility to operate within a more flexible wider range of step-sizes that result in better control and elimination of spurs within the frequency of interest. However, one fundamental drawback that needs to be pointed out is that when implemented at low-order ΣΔ, FNPLL's capability to shape and randomize noise is minimal.

Generally, higher order ΣΔ modulators have better noise shaping characteristics and they are often used to shift the quantization noise from the frequency of interest to higher frequencies. Their main constraint is that the signal is highly dependent on the gain of the quantizer, where a high gain (that is introduced by the digital to analog converter) normally degrades the smooth noise-shaped spectra. A proposal was made in [30] to control the gain of the quantizer, which employs LMS algorithm to match the gain adaptively. This technique controls the gain effectively when the LMS bandwidth is low enough to enable the quantization error-term to be suppressed.

A technique that optimizes the gain and loop coefficients of the ΣΔ modulator architecture's transfer

functions was proposed in [31], which allows for the selection of the suitable noise transfer function that gives the required SNR. A major advantage of introducing poles in the signal band is that the out-of-band gain (OBG) can be reduced by moving and adjusting poles within the unit circle [32]. It is through this technique where loop filters are treated as quantization noise and get minimized by adjusting the coefficients of the loop filters. However, this technique has a challenge in that suppressing quantization noise in low frequency bands may results in spurs emerging at higher frequencies, which normally causes signal instability.

Table 1.1: Phase noise performance of reviewed techniques.

Summary of reviewed PN Cancellation Techniques			
Authors	Techniques	Achieved PN (dBc/Hz)	Output Frequency
[33]	Single VCO +Div/MUX	-111 @ 5 GHz	6.25 GHz
[34]	PLL DSS	-90 @ 10 kHz	$2.06-2.16$ GHz
[35]	Analog Feed-Forward Adaptive PN cancellation	-105 @ 1 MHz	5 GHz
[36]	Dual Path Control Scheme with smoothed Varactors	-113 @ 1 MHz	5 GHz
[27]	FIR with ΣΔ Modulators	-120 @ 400 kHz	1.8 GHz
[37]	Fractional-N Frequency Synthesizer	-92.27 @ 600 kHz	$832-936$ MHz
[38]	Digital Fractional-N PLL based on 2nd Order FDC	-123 @ 1 MHz	3.5 GHz
[39]	Hybrid Fractional-N Frequency with Noise Filtering	-113 @ 1MHz	2.41 GHz
[40]	Cascaded PLL with an Integer-N digital bang-bang PLL	-53.9 @ 50 MHz	$2.55-3$ GHz
[41]	Fractional-N Synthesis for UHF Transceiver	-120 @ 1 MHz	900 MHz

Table 1.1 summarizes the PN performances of the existing techniques. It is important to note that the techniques presented in [35], [36], [38], [39] and [41] were based on 1 MHz offset frequency. The techniques presented in [38] and [41] performed better than others as they achieved low levels of PN of about -123 and -120 dBc/Hz respectively at 1 MHz frequency offset.

1.3 RESEARCH HYPOTHESIS

The hypothesis of this masters study was framed as follows: "Is it possible to reduce the spurious tones within the frequency of interest to achieve a low phase noise level that is better than those achieved by the existing phase noise correction techniques?" Simulation results of the proposed phase noise cancellation technique were expected to show a phase noise improvement with the minimal spurious tones within the frequency of interest when compared to the existing techniques..

1.4 RESEARCH METHODOLOGY

To gain insight into the limitation of the conventional phase noise cancellation techniques, an in-depth literature review on current techniques was conducted. Existing techniques were analyzed where the simulation results were used to identify the weakness or limitations of these techniques (research gap).

Several modifications were made to the existing architectures, which resulted in a completely new model that seeks to improve and enhance the limitations of the existing techniques. The proposed technique was implemented and tested on the Agilent ADS LTE Downlink (DL) test set-up [42], which is a leading electronic design software tool for high speed digital automation. ADS has built in modules LTE standards-based design and verification with wireless libraries and circuit-system-EM co-simulation in an integrated platform. The simulations results were compared with those of the existing techniques to check if there is an improvement that is realized.

1.5 RESEARCH CONTRIBUTION

Detailed literature review on the cancellation of phase noise within the frequencies synthesizers was conducted, which forms part of the body of knowledge in the area of wireless communication systems.

The following distinct contributions were made:

- A comprehensive literature review was conducted where the limitations of the existing PN schemes were presented.

- Key performance metrics that are used to evaluate the performance of PN were reviewed.
- Theoretical analysis and performance evaluations of current phase noise techniques were conducted.
- Specification (design parameters for the proposed system) for the implementation of a PN correcting techniques developed.
- A new architecture that produces a clean spectrum without spurious tones is presented.
- Existing literature resolves the short periodic cycle by using a random dither sequence to disrupt the periodic cycles [43]. Although this process results in smooth noise-shaped spectra it adds noise to the spectra. The proposed approach uses an adaptive filtering algorithm to control the data sequence, which allows flexibility even at wider bandwidth.
- The mathematical expressions for the proposed architecture are formulated and presented in this dissertation.
- The proposed technique was simulated and tested for a long-term evolution (LTE) communication system where it is shown to outperform the existing techniques.

1.6 PUBLICATIONS

The following articles were authored based on the work presented in this dissertation;

1.6.1 Conference Article

The following published peer reviewed paper won the best paper award at the IEEE AFRICON 2015 conference held at the United Nations Conference Center (UNECA) in Addis Ababa, Ethiopia from 14-17 September:

(i) P.R. Munyai and B.T. Maharaj, "On the Improvement of phase noise errors in wireless communication systems"; *12th IEEE AFRICON Conference on Communications Systems*,14-17 September, 2015.

1.6.2 Journal Article

The following journal article was submitted to the International Journal of Communication systems:

(i) P.R. Munyai and B.T. Maharaj, "A Phase Noise Improvement Technique For Wireless Communication System", *International Journal of Communication systems*, November 2016 (in review).

1.7 DISSERTATION OUTLINE

Chapter 1 (Introduction) a comprehensive background to phase noise concepts and its components. The fundamentals of phase noise and metrics that are used to evaluate the performance of wireless communication systems are presented. This chapter also covers a comprehensive literature review of the published journal articles on phase noise cancellation techniques.

Chapter 2 (Phase noise cancellation techniques) presents the analysis of existing phase noise cancellation techniques that are based on adaptive filtering (MSE, LSM, RLS) algorithms. The performance results of these techniques are analyzed, compared and discussed in this chapter. The chapter also presents phase noise cancellation techniques that are based on phase-locked loop (PLL) concepts, which include ΣΔ modulators embedded on PLL architectures.

Chapter 3 (Research Methodology) describes the research strategy that was followed to achieve the objective and hypothesis of this research. This chapter discusses and presents all parameters (Frequency range, frequency divider, voltage control gain of the VCO, the gain at the PFD, capacitor and resistor values of the loop filter, etc) that were used during simulation.

Chapter 4 (Description of proposed technique) discusses the architecture and circuit design of the new technique. This chapter presents all mathematical expressions that were formulated to describe the behavior of the proposed architecture.

Chapter 5 (Discussion of Results) presents the schematic layout of the proposed model as implemented and simulated in Advanced Design System (ADS). This chapter also presents the comparison table of the achieved results and those obtained from the existing literature.

Chapter 6 (Conclusions and recommendations for future research) summarizes the achieved objectives, hypothesis and solved problem statement. This chapter concludes by suggesting possible areas for future research.

CHAPTER 2 PHASE NOISE CANCELLATION TECHNIQUES

2.1 CHAPTER OBJECTIVES

Several studies were conducted on the performance of phase noise cancellation techniques that are based on adaptive filtering (such as mean square error, least mean square, recursive least mean square Algorithms) [20] and phase locked loop methods [4]. This chapter presents the analysis of the existing phase noise cancellation techniques. Furthermore, the limitations and challenges of the existing techniques will be highlighted.

2.2 ADAPTIVE FILTER NOISE CANCELER

The main aim of the adaptive filter noise canceler (ANC) is to minimize the difference between the desired and output signal, $e(i) = d(i) - y(i)$, where the computed difference is passed through the adaptive algorithm stage to adjust the time-varying tap weights that can be expressed in vector form as;

$$w(i) = [w_0(i), w_1(i), \cdots, w_{M-1}(i)] \tag{2.1}$$

The input and output data sequences are given by;

$$x(i) = [x(i), x(i-1), \cdots, x(i-M+1)]^T \tag{2.2}$$

$$\begin{aligned} y(i) &= \sum_{i=0}^{M-1} w_m(i)x(i-m) \\ &= w^T(i)x(i). \end{aligned} \tag{2.3}$$

where

$$M = \text{Number of adaptive tap filters}$$

$$w = \text{Filter coefficients}$$

Now the errored-signal can be tracked by making use of the following expression

$$e(i) = d(i) - w^T(i)x(i). \tag{2.4}$$

where

$x(i) =$ Column vectors of the input signal that are updated iteratively until e(i) reaches the minimum value.

2.2.1 Performance criteria

The most widely used criterion for judging the performance of the adaptive filter is the minimization of the mean square error (MSE), $E\{e^2(k)\}$, which is given by;

$$E = \text{Represent the expectation of operation}$$

$$e(k) = d(k) - y(k)$$

$$d(k) = \text{Desired signal}$$

$$y(k) = \text{Output of the filter response.}$$

The MSE is normally defined as the expectation of the squared error, which is given by;

$$\begin{aligned}
\mathbf{J} &= E\left[e^2(i)\right] \\
&= E\left[(d(i) - w^T \cdot x(i))^2\right] \\
&= E\left[d(i)^2 - 2d(i) \cdot w^T \cdot x(i) + w^t \cdot x(i) \cdot x^T(i) \cdot w\right] \\
&= E\left[d(i)^2 - 2\rho_{xy}^T w + w^t \rho_{xx} w\right].
\end{aligned} \tag{2.5}$$

where

$\rho_{xx} = Ex(i)x(i)^T$, is the NxN correlation matrix (2.6)

$\rho_{xy} = Ed(i)x(i)$, is the $Nx1$ cross-correlation matrix vector between the input and the desired signal. (2.7)

The auto-correlation vector is given by;

$$\begin{aligned}\rho_{xx} &= E\{x(i)x^T(i)\} \\ &= E \times \begin{bmatrix} x(i)x(i) & x(i)x(i-1) & \cdots & x(i)(i-N+1) \\ x(i-1)x(i) & x(i-1)x(i-1) & \cdots & x(i-1)(i-N+1) \\ \vdots & \vdots & \ddots & \vdots \\ x(i-L+1)x(i) & x(i-N+1)x(i-1) & \cdots & x(i-N+1)(i-N+1) \end{bmatrix}\end{aligned} \tag{2.8}$$

The cross-correlation vector takes the following form;

$$\begin{aligned}\rho_{xy} &= E\{y(i)x(i)\} \\ &= E \times \begin{bmatrix} y(i)x(i) \\ y(i)x(i-1) \\ \vdots \\ y(i)x(i-N+1) \end{bmatrix}\end{aligned} \tag{2.9}$$

Equation 2.5 indicates that the MSE cost function behaves like a quadratic equation, which makes it easier to analyze and measure its performance by means of plotting a hyperbolic figure in Matlab [44] as shown in Figure 2.1, which is also referred to as performance surface of the MSE.

Figure 2.1 is also referred to as the performance surface of the MSE.

The MSE filter is designed in such a way that it operates at this minimum point by taking the derivative of equation (2.5) as follows;

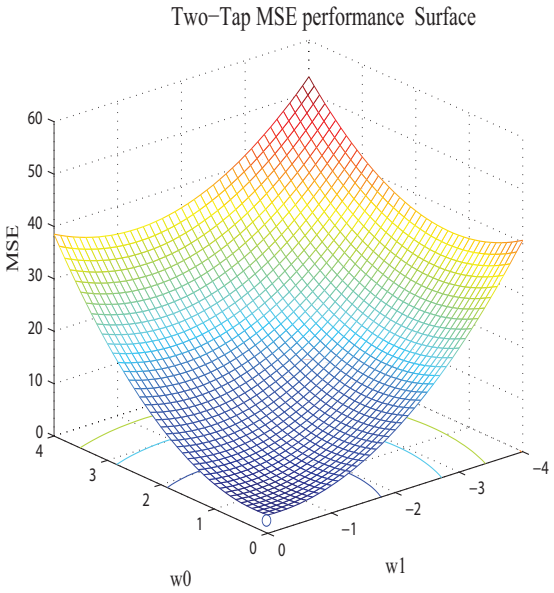

Figure 2.1: Schematic representation of MSE performance surface simulated at M=2 with filter weights w_0 and w_1.

$$\frac{jw}{dw}(d^2(i)) = 0 \tag{2.10}$$

where $d^2(i)$ is a constant variance

$$\begin{aligned} \frac{jw}{dw}(\rho_{xy}^T w) &= 0 \\ \frac{jw}{dw}(\rho_{xx} w^T) &= 2 \\ \frac{jw}{dw}(w\rho_{xx} w^T) &= 2\rho_{xx} w. \end{aligned} \tag{2.11}$$

The gradient of the MSE (Δ) with respect to the tap-weight w is;

$$\begin{aligned} \Delta &= \frac{jw}{dw} \\ &= -2\rho_{xy} + \rho_{xx} w. \end{aligned} \tag{2.12}$$

Equation (2.12) approaches zero at the bottom of the surface, such that the autocorrelated and cross-correlated input sequences are linked by the filter coefficients as follows;

$$\rho_{xx} w_0 = \rho_{xy} \tag{2.13}$$

$$w_0 = \rho_{xx}^{-1} \rho_{xy}. \tag{2.14}$$

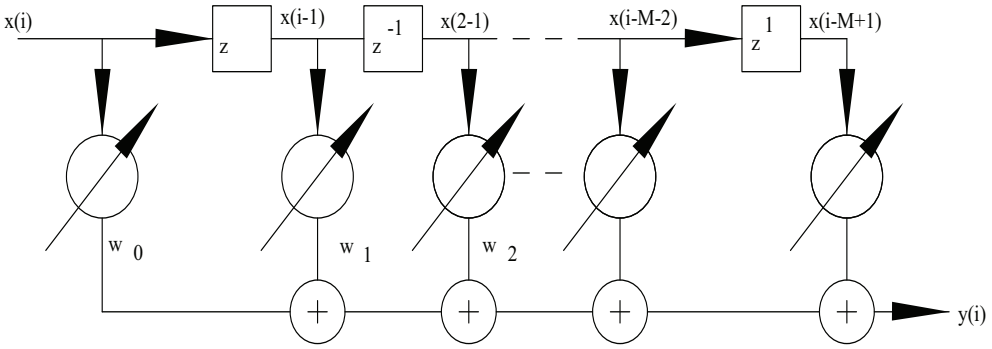

Figure 2.2: Schematic representation of M-tap adaptive filter.

At this point the filter, (w_0), is able to deal with noise decisively.

The weight vectors $\vec{w} = [w_0, w_1, \vec{\cdots}, w_{M-1}]^T$ shown in Figure 2.2 are computed in such a way that the performance surface has a single minimum MSE centered at the optimum vector, $\vec{w_0}$ [45].

2.2.2 Least Mean Square Algorithm

ANC is a commonly used technique that cancels noise by adding an alternating signal noise that is 180 deg out of phase with the original signal. This opposing signal dampens the energy of the original signal noise. As shown in Figure 2.3 the LMS algorithm has the filtering and adaptive processes and the main components. The filtering process generates the output signal and the estimation error. The adaptive process adjusts the filter tap weights automatically.

LMS has attracted a lot of attention [21, 46] due to its flexibility that makes it possible to operate as an automatic control system. The LSM algorithm is derived from the fact that MSE seeks to minimize $Ee^2(i)$ until the Wierner solution is optimized such that;

$$\begin{aligned} \lim_{i\to\infty} W(i) &= W_{MMSE} \\ &= (\rho_{xx})^{-1}\rho_{xy}. \end{aligned} \tag{2.15}$$

The Wierner solution is normally determined from the Newton and Steepest Descent Methods proposed in [47].

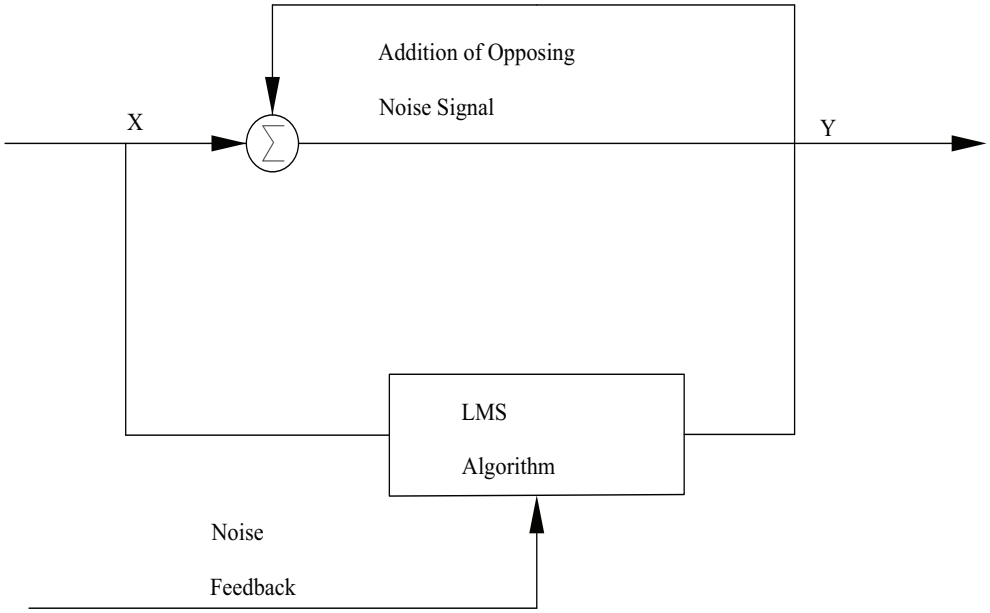

Figure 2.3: Schematic representation of ANC with LMS algorithm.

2.2.2.1 Newton Method

A Newton Method seeks to optimize the filter weights as follows [48];

$$\Delta W(i) = \mu \rho_{xx}^{-1} \left[\frac{\partial E\{e^2(i)\}}{\partial W(i)} \right]. \tag{2.16}$$

The LMS algorithm is obtained by substituting $e(i)$ and $W(i)$ into (2.16) as follows [48]

$$\begin{aligned} W(i+1) &= W(i) - \mu \rho_{xx}^{-1} \left[\frac{\partial E\{e^2(i)\}}{\partial W(i)} \right] \\ &= W(i) - \mu \rho_{xx}^{-1}.2(\rho_{xx} W(i) - \rho_{xy}) \\ &= (1-2\mu)W(i) + 2\mu \rho_{xx}^{-1} \rho_{xy} \\ &= (1-2\mu)W(i) + 2\mu W_{MMSE}. \end{aligned} \tag{2.17}$$

The filter weights are set from the initial $W(0)$ condition to the optimum setting W_{MMSE} as follows;

$$W(i) = W_{MMSE} + (1-2\mu)^i [W(0) - W_{MMSE}]. \tag{2.18}$$

where

$\mu =$ Is the step size that controls the convergence rate and stability of the filter.

2.2.2.2 Steepest Descent Method

The Steepest Descent Method seeks to reduce computational complexity by avoiding the matrix inversion as follows;

$$\begin{aligned}
\Delta W(i) &= -\mu\left[\frac{\partial E\{e^2(i)\}}{\partial W(i)}\right] \\
W(i+1) &= W(i) - \mu\left[\frac{\partial E\{e^2(i)\}}{\partial W(i)}\right] \\
&= W(i) - \mu.2(\rho_{xx}W(i) - \rho_{xy}) \\
&= (I - 2\mu\rho_{xx})W(i) + 2\mu\rho_{xx}W_{MMSE} \\
&= (I - 2\mu\rho_{xx})[W(i) - W_{MMSE}] + W_{MMSE}. \qquad (2.19)
\end{aligned}$$

Finally, the LMS algorithm is obtained by applying the Widrow method [48] to the Steepest descent expression where the estimation operator is omitted as follows;

$$\begin{aligned}
W(i+1) &= W(i) - \mu\left[\frac{\partial e^2(i)}{\partial W(i)}\right] \\
&= W(i) - \mu\left[\frac{\partial e^2(i)}{\partial e(i)}\right].\left[\frac{\partial e(i)}{\partial W(i)}\right] \\
&= W(i) - 2\mu e(i).2\frac{[d(i) - W(i)^T.X(i)]}{2W(i)} \\
&= W(i) + 2\mu e(i)X(i). \qquad (2.20)
\end{aligned}$$

Now filter weights can be modeled as;

$$W_0(i+1) = W_0(i) + 2\mu e(i)X(i) \qquad (2.21)$$

$$W_1(i+1) = W_1(i) + 2\mu e(i)X(i-1). \qquad (2.22)$$

As seen from Equation (2.20), the algorithm has low complexity as it does not depend on the signal statistics or metric inversion (i.e., ρ_{xx}^{-1} and ρ_{xy}).

The LMS algorithm consists of the filtering and adaptive process, which involves automatic adjustment of the filter parameters $w(i+1)$ until all weights are updated. The algorithm is given by;

$$w(i+1) = w(i) + \mu x(i)e(i). \qquad (2.23)$$

where

$$\mu = \text{Step-size (convergence factor).}$$

$$w(i) = \text{tap-weights.}$$

$$w(i+1) = \text{Updated tap-weight vectors.}$$

The LMS algorithm seeks to adapt the filter tap weights until the error signal $e(i)$ is minimized in accordance with the MSE process. Equation 2.23 confirms that the LMS iterative process does not depend on prior knowledge of the correlation coefficients ρ_{xx} and ρ_{xy}. Instead it uses instantaneous estimations, which makes it more robust and fast to converge. When simulating the LMS algorithm the following convergence condition is useful in defining the convergence range;

$$0 < \mu < \frac{1}{\lambda_{max}}. \tag{2.24}$$

where

$$\lambda_{max} = \text{Is the largest Eigenvalue of the correlation matrix } \rho_{xx}.$$

A faster rate of convergence can be realized through the following convergence range that resolve the instability problems and adjusts the step size to [21];

$$0 < \mu < \frac{2}{\lambda_{max}}. \tag{2.25}$$

The earlier work conducted by Rajesh and Sumalatha [49] demonstrates the performance and effectiveness of the stepsize as a tool to improve voice quality of a telephone call. As shown in (2.25), the larger the step size the faster the convergence rate. However some larger stepsizes may cause signal instability.

Table 2.1: Parameters used for the analysis of LMS algorithm.

Design Parameters		
Parameters	Symbol	Calculated values
Step Size(Convergence factor)	μ	0.05
Filter Order	N	10
Filter length	L	150
No. Of Iterations	i	1000

2.2.2.3 Simulation of LMS Algorithm

The LMS algorithm was evaluated for convergence criterion where the optimum complex weights were simulated using Equation (2.20) and Table (2.1).

Figure 2.4 is a plot of weight convergence where the magnitude of the weights is plotted against the number of iterations, indicating the convergence of the weights to their optimum values. Here the magnitudes of the weights (W_0) are seen to converge after 600 iterations whereas those of (W_1) converge after 700 samples.

The step size parameter was also selected by trial and error with the guidance of Equation (2.24). After several simulations and different selections of μ it was found that the convergence rate tends to be slow for small values, which results in high error signals. The best case scenario for this study was found when $\mu = 0.005$ that causes the LMS algorithm to settle at an MSE of about $10^{-2.9} = 0.001585$ and progresses until it reaches a steady-state error. As seen from (2.24), LMS is highly unstable and take too long to reach a steady-state error value.

However, the faster convergence can be obtained by varying the step size, μ, which improves the convergence rate significantly. It was also observed through this simulation study that a smaller step size reduces the instability for larger filter orders. On the other hand, low filter orders requires higher step sizes to attain stability. This confirms that stronger signals requires small step sizes whereas weak signals require larger step sizes.

As shown in Figure 2.1, the MSE criterion always dictates that for the noise cancellation technique to exhibit excellent performance the error signal should approach zero as the number of iterations

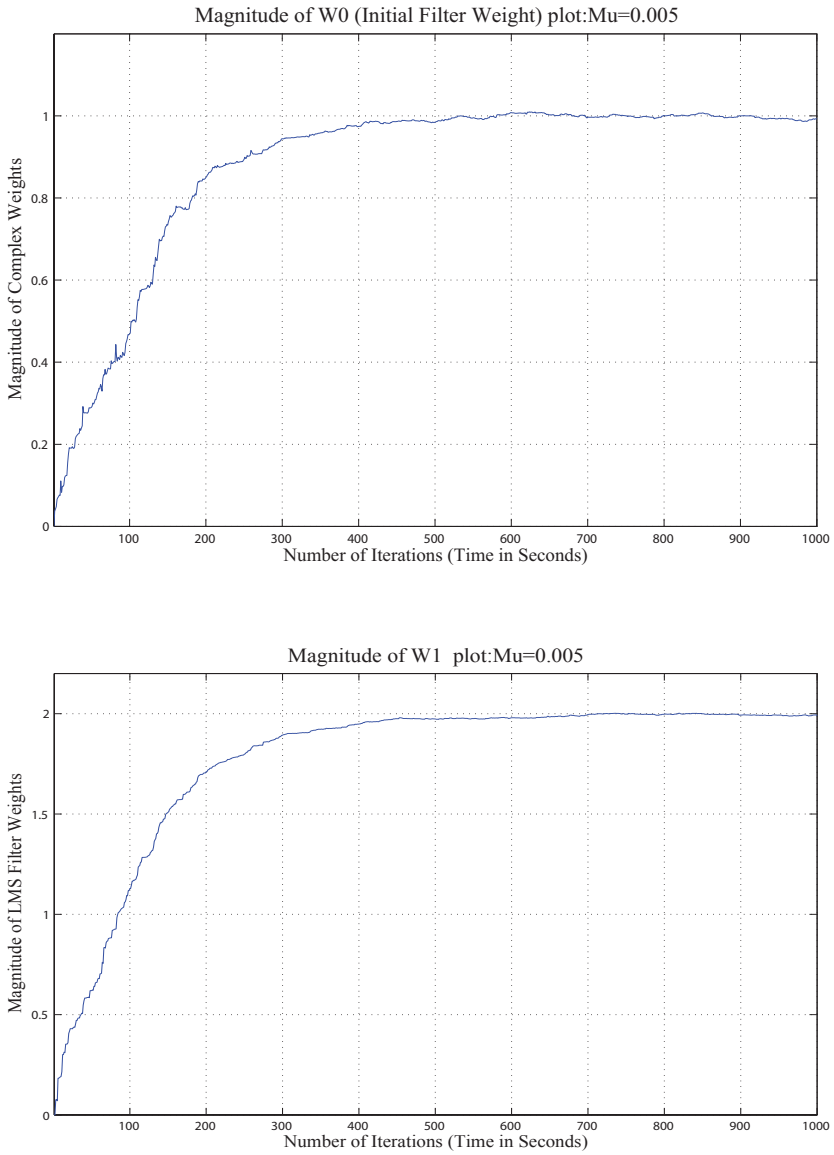

Figure 2.4: Magnitude of Weights W_0 and W_1 versus Number of Iterations.

progresses.

The simulation results show that although the LMS algorithm finally achieves the steady state-error it does so after several iterations, which implies that the LMS has a long convergence rate [50]. From this simulation it is concluded that although LMS has lower complexity it takes longer to converge at fixed step sizes although the convergent rate can be improved by changing step sizes (variable step sizes) through trial and error.

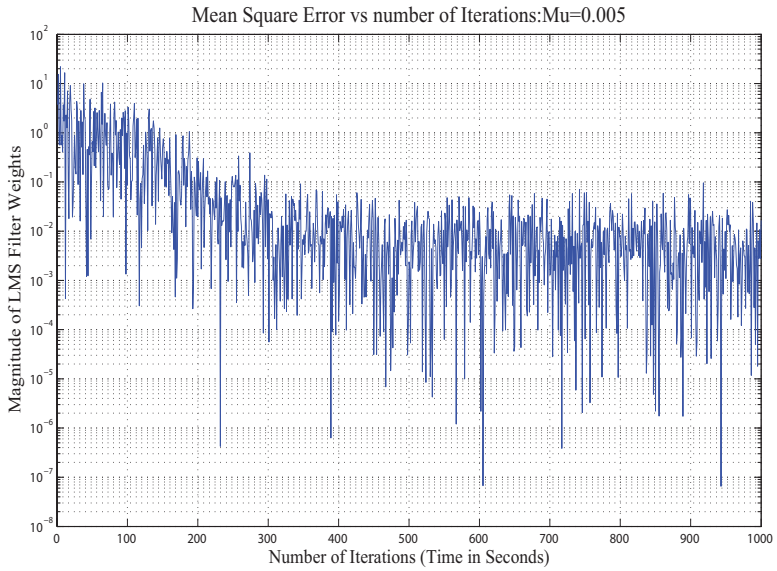

Figure 2.5: MSE Estimation in dB vs no. of iterations (mu=.005).

2.2.3 Recursive Least Square

The performance of recursive least square (RLS) algorithm has been studied in [4], where it was shown that the RLS's performance is slightly better than LMS. However, Iliev and Kasabov [51] conducted a study on adaptive filtering with averaging in noise cancellation for voice and speech recognition and observed that the main drawback for RLS is the instability problem.

Figure 2.6 shows a schematic representation of an adaptive noise canceler, where the output of a filter is computed from;

$$y(i) = X^T W(i). \tag{2.26}$$

The error signal is given by;

$$\begin{aligned} e(i) &= s(i) + n(i) - y(i) \\ &= s(i) + n(i) - [X^T W(i)]. \end{aligned} \tag{2.27}$$

Changes in signal characteristics can be very fast and sometimes uncontrollable. This problem can be resolved by implementing a recursive algorithm that adjusts the filter coefficients. The recursive algorithm is able to achieve a faster rate of convergence through the adjustment of filter coefficients. The RLS tap weights are given by;

$$w(i) = \bar{w}^T(i-1) + k(i)\bar{e}_{i-1}(i). \tag{2.28}$$

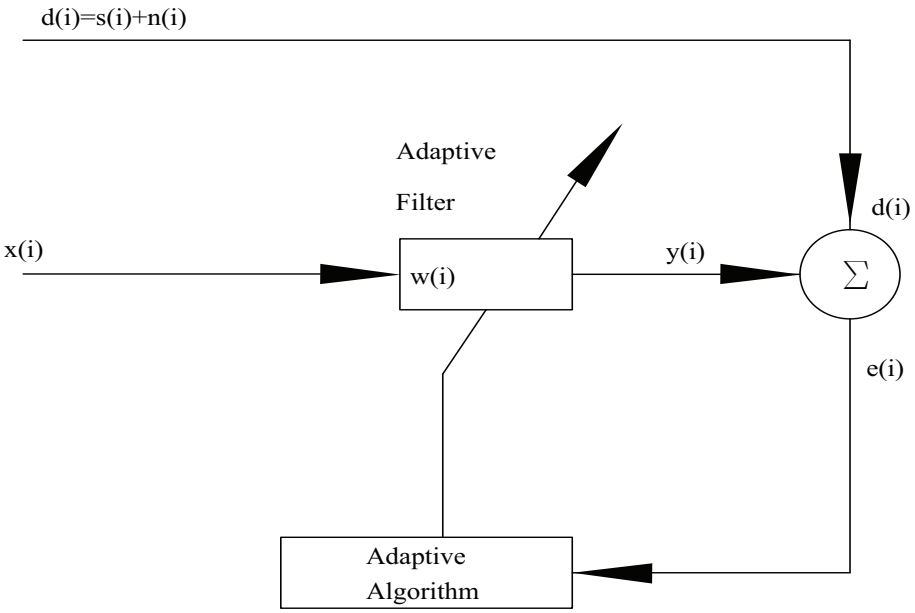

Figure 2.6: Schematic representation of adaptive noise canceler with RLS.

where the gain vectors $k(i)$ and $x(i)$ are given by;

$$k(i) = \frac{x(i)}{\lambda + x^T(i)x(i)}$$
$$x(i) = \frac{(i-1)x(i)}{\bar{w}_\lambda}. \tag{2.29}$$

The fact that RLS algorithm computes filter weights by estimating previous samples of output signals, $(\bar{y}_{i-1}(i) = \bar{w}^T(i-1)x(i))$, leads to computational complexity.

Table 2.2: Parameters used for the analysis of RLS algorithm

Design Parameters		
Parameters	Symbol	Calculated values/Specifications
Step Size(Convergence factor)	μ	0.05
Filter Order	N	10
Filter length	L	150
No. Of Iterations	i	8000

2.2.3.1 Simulation of RLS Algorithm

The RLS algorithm was implemented in Matlab with the reference signal assumed to follow a white Gaussian noise distribution of 1-dB. The noise was assumed to be random and was implemented in matlab using *randn* function. The errored signal of Equation 2.27 was evaluated. The main algorithm specification is given in Table 2.2.

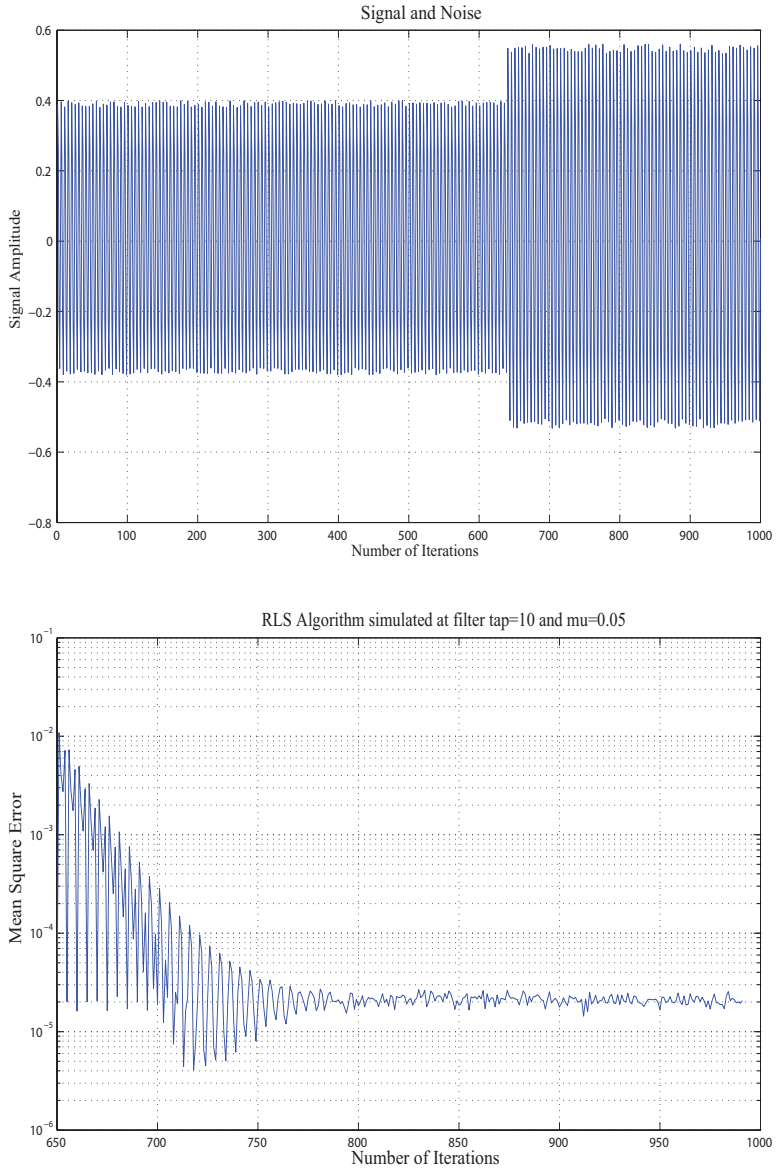

Figure 2.7: The top plot of Figure 2.7 shows the simulated signal with noise while the bottom plot shows the convergence characteristic of the RLS algorithm.

It can be observed from Figure 2.7 that at first the signal experiences high amplitude oscillations but converges faster at smaller iterations [52]. Figure 2.7 shows a very fast convergence rate that is achieved barely after 100 iterations $(750-650)$ and the steady state errors continues with the number of iterations. The convergences characteristic of the RLS algorithm is more effective as it takes a smaller number of iterations when compared with the LMS although there are some high amplitude fluctuations at the beginning due to the recursive nature of the RLS algorithm. From the simulation results it is seen that RLS converges faster than the LMS algorithm. These results are in agreement

with observation made in [53]. As compared to LMS, the RLS algorithm was able to settle within 100 iterations and remain stable throughout until 1000 iterations. By selecting 10 as the tap weight and 0.05 as the step size the RLS algorithm reduced the mean square error by 0.0099 (0.01 to 0.0001), which is roughly 20dB.

However the RLS achieves a remarkable faster convergence rate at the cost of high complexity.

2.2.4 Kalman Filter

Kalman Filter can be thought of as an adaptive Filter that seeks to combine the strength of the least square error (LSE) and RSE to provide a more efficient algorithm with more computational efficiency [22, 54, 55, 56]. The KF uses mathematical techniques to model the observed values that contain noise to estimate the values that are closer to the true values.

The basic operation of the KF is that it generates estimates values of the true (and calculated values) by predicting a value, calculate the uncertainty of the value and then determine the weighted average of the predicted and measured values. The KF corrects the phase noise through the prediction of a new state from the previous estimation by introducing a correction term that is proportional to the prediction error. This allows the KF to reduce the effects of phase noise on the required signal by minimizing mean square error (MSE) between the desired signal and the filter response.

2.2.4.1 Signal Estimation

The KF estimates the values that are closer to the true values by making use of the linear stochastic difference equations as follows;

$$x_i = Ax_i + Bu_i + w_i. \tag{2.30}$$

$$y_i = Cx_i + v_i. \tag{2.31}$$

where

$$\begin{aligned} x_i &= \text{n-dimensional state vector.} \\ A &= \text{State transition matrix.} \\ y_i &= \text{m-dimensional measurement vector.} \\ C &= \text{Observation matrix.} \\ w_i &= \text{Process noise.} \\ v_i &= \text{Measurement noise vector.} \end{aligned} \tag{2.32}$$

Here the sequence v_i and w_i are assumed to be uncorrelated and independent of each other. The noise is normally modeled as white noise with normal probability distributions, where the process,$\mathbf{Q}$, and

measurement, **R**, noise covariances are given by;

$$p(w) \approx \aleph(0, Q) \tag{2.33}$$

$$p(v) \approx \aleph(0, R). \tag{2.34}$$

2.2.4.2 Error Computation with KF

The KF computes errors by making use of *a priori* state estimate at time *i* by assuming that the process prior to step *i* is known such that;

$$e_i^- \equiv x_i - \hat{x}_i. \tag{2.35}$$

and *a posteriori* estimate at time *i* after taking a measurement, such that;

$$e_i \equiv x_i - \hat{x}_i. \tag{2.36}$$

The covariances of the *a priori* and *a posteriori* errors are respectively given by;

$$P_i^- = E\left[e_i^- \quad e^{-T}\right]. \tag{2.37}$$

$$P_i = E\left[e_i \quad e^T\right]. \tag{2.38}$$

Now *a posteriori* estimate is computed as a linear combination of *a priori* estimate and the weighted average between the actual and predicted measurement by Equation (2.39);

$$\hat{x}_i = \hat{x}_i^- + K(y_i - C\hat{x}_i^-). \tag{2.39}$$

The KF gain , K, in 2.39 is given by;

$$\begin{aligned} K &= P_i^- C^T (C P_i^- C^T + R)^{-1} \\ &= \frac{P_i^- C^T}{C P_i^- C^T + R}. \end{aligned} \tag{2.40}$$

2.2.5 Simulation results of KF

The performance evaluation of KF was conducted with Matlab where the Gaussian noise was implemented as a process and the amplitude was estimated using the KF procedure discussed in the preceding sections. The estimated and original signals were analyzed to determine if the estimation process was effective.

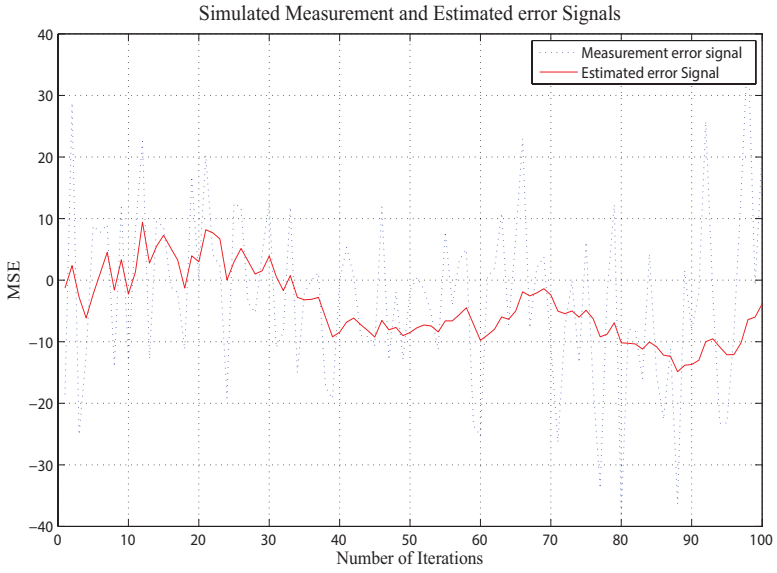

Figure 2.8: Signal Error Estimation with Kalman Filter.

Figure 2.8 shows that the at lower sample values the measurement and estimated signal errors track each other very well. However as the number of iterations progress, misalignment of the two signals becomes more visible. As seen in Figure 2.8, KF does not perform well at larger filter gains in that the amplitudes measurement error signal are much higher than that of the estimated signal. The height transients in the measurement error signal can be reduced by changing the covariance of the error signal.

Figure 2.9 shows that the variance of the estimation error can be controlled to force the estimation signal to track the measurement signal error properly.

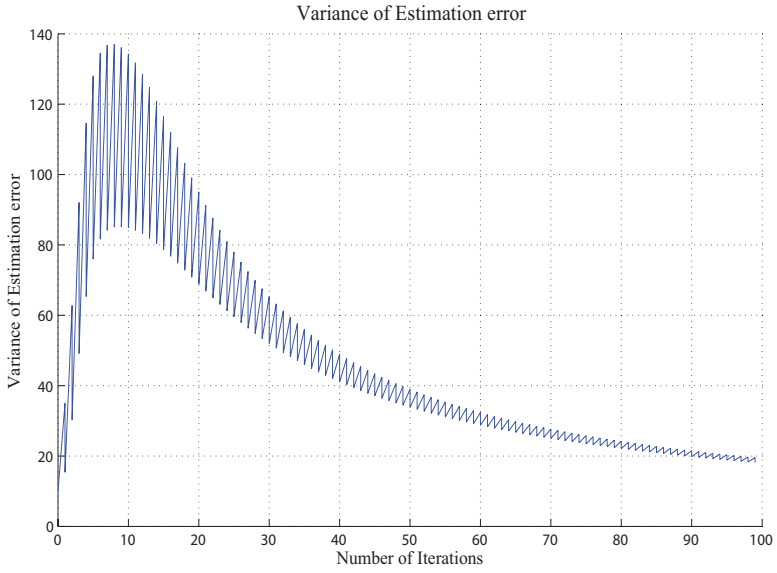

Figure 2.9: Variance of the estimation error.

As seen in figure 2.9, the main drawback of the KF is the requirement to establish the initial condition of mean and variance to initiate the recursive process. In this simulation the KF was initialized by starting $\hat{x}_0$ state at the initial time and the initial estimation error covariance, $\hat{P}_0$. The problem in initializing $\hat{x}_0$ and $\hat{P}_0$ is that if $\hat{P}_0$ is unknown with known $\hat{x}_0$, then $\hat{P}_0$ will be too small. And if $\hat{x}_0$ is initially assumed to be unknown, then $\hat{P}_0$ becomes large. After some time, these initialization values become more difficult to be recognized in the overall filter performance.

Figure 2.10 indicates that the KF converges at about 80ms when the step size is at 0.01 and converges at 100ms when the step size is 0.05. This implies that the KF converges on the 100th sample, which is far much faster when compared with the LMS that converges on the 400th sample.

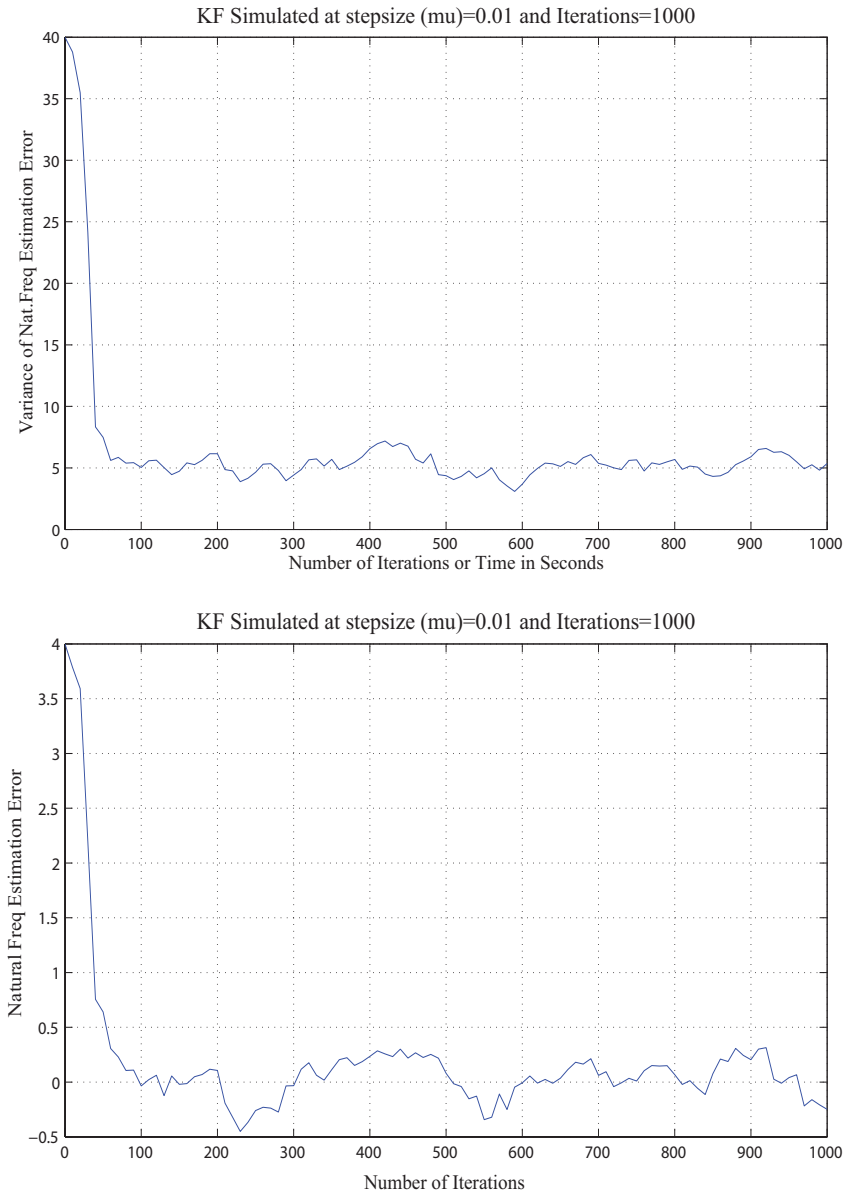

Figure 2.10: MSE of Natural Frequency and it's variance.

The most widely used techniques (LMS, RLS, Kalman and PLL) were evaluated for performance using the performance criteria (MSE, Convergence rate, NPM, Stability and computational complexity. Table 2.3 gives a summary of the results of investigation, where the limitations and drawbacks of each technique are displayed.

Table 2.3: Comparison of key performance metrics.

Performance criteria	LMS	RLS	KF
MSE(dB)	-5.990	-20	-5.11
Convergence Rate (seconds)	490	100	80
Computational Complexity	Low	High	High

It can be seen from Table 2.3 that the convergence rate of LMS is very high. Although RLS and KF show excellent convergence rate, they do so at the expense of high computational complexity.

2.3 PHASE LOCKED LOOP TECHNIQUE

A phase locked loop (PLL) controlled circuit is used to provide synchronization to the frequency and phase of the signal detected by the receiver.

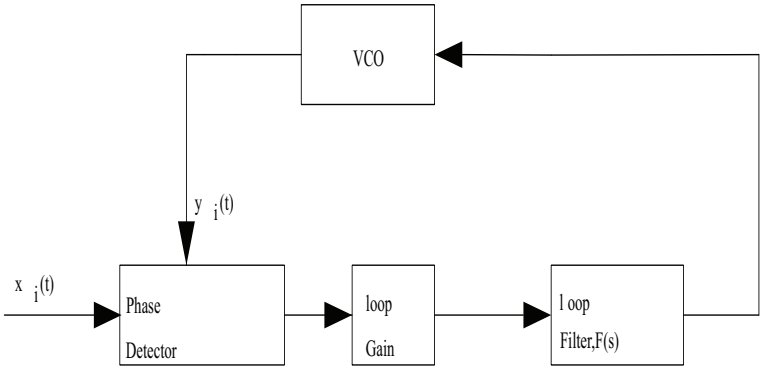

Figure 2.11: Basic Model of PLL.

A PLL control circuit uses the negative feedback to lock the phase and frequency of the input signal. The main fundamental block is the Phase Detector (PD) that compares the phase of the output signal with that of the input signal. If it detects the difference between the two phases (output and input) it generates a voltage that is proportional to the phase errors of the input and output signals, which is then passed through the Loop Filter and goes through the voltage controlled oscillator. This process creates a self-correcting technique that results in the input and output signals being in phase. This process leads to carrier phase recovery or synchronization.

2.3.1 PLL Noise Blocks

All PLL blocks (PFD, LPF, VCO and FD) contribute to the total noise in different forms. The noise contribution of each individual block to the PLL system is depicted in Figure 2.12

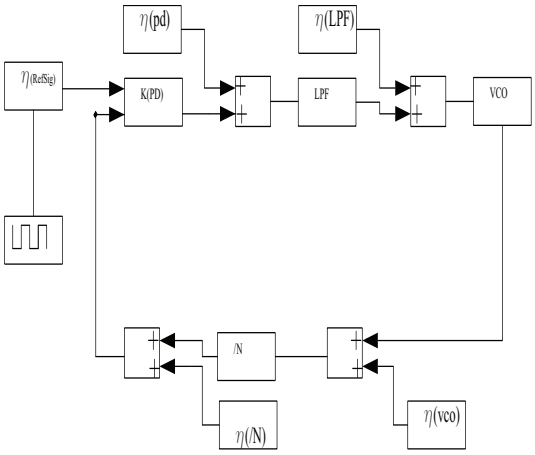

Figure 2.12: Noise contribution by individual blocks.

The total noise can be calculated by summing the individual noise contribution as follows;

$$\eta_{Total} = \eta_{PD} + \eta_{LPF} + \eta_{vco} + \eta_{FDN} + \eta RefSig. \tag{2.41}$$

where

η_{RefSig} = Noise contribution from the reference signal.

η_{PD} = Noise contribution from the PD.

η_{LPF} = Noise contribution from the LPF.

η_{FDN} = Noise contribution from the FDN.

η_{vco} = Noise contribution from the VCO.

2.3.1.1 Frequency Divider Noise

The most commonly used divider is a regular programmable counter that uses the complementary $metal-oxide-semiconductor$ (CMOS) technology, which oscillates up to 100MHz. The application of frequency dividers is very useful as they reduce the phase noise at all offsets by a factor of

$20\log(N)$. The frequency divider can be expressed in equation form as;

$$(f)_{out} = (f)_{in} - 20\log(N). \tag{2.42}$$

Although this type of divider consumes relatively low power , it generates noise that contributes to the total PLL noise. The transfer function of the frequency divider is given by;

$$H(s) = \frac{2\pi\Gamma_{vco}\Gamma_{PD}(1+sR_2C_2)}{s^3C_1C_2R_2 + s^2(C_1+C_2)(1+sR_2C_2)(\Gamma_{PD}\Gamma_{vco}\Gamma_{Amp})/N}. \tag{2.43}$$

2.3.1.2 Reference Noise

The reference noise is normally generated by the crystal oscillator. The transfer function of the reference noise is modeled by;

$$\begin{aligned} H(s) &= \frac{eta_{out}}{\eta_{RefSig}} \\ &= \frac{\Gamma_{vco}F(s)/s}{1+\Gamma_{vco}}F(s)/Ns \\ &= \frac{N(1+1/\omega_2)}{Ns^2/\Gamma_{vco} + s^2/\omega_2 + 1}. \end{aligned} \tag{2.44}$$

From Equation (2.44) it is observed that if s is very small, the reference noise equals N such that $\frac{\eta_{out}}{\eta_{RefSig}} = N$.

2.3.1.3 VCO Noise

Phase noise originates from the local oscillators in which individual component noise contributes into an infinite number of noise with different frequency ranges. At Intermediate Frequency (IF), different signals generated from different oscillator components are combined to form an amplified phase noise signal. The phase of a noise signal is related to the time-shifted carrier frequency as follows;

$$\begin{aligned} \theta &= \omega_c(t) \\ &= 2\pi(f_c)\theta(t). \end{aligned} \tag{2.45}$$

If the noise source is assumed to be white Gaussian, the phase shift, θ, can be redefined as;

$$\theta(t) = \sqrt{B}W_n(t). \tag{2.46}$$

where B and W_n denote the oscillator quantity and Wierner or Brownian process respectively. The frequency of the time-varying oscillator sinusoid is related to the phase noise by

$$f(t) = f_c + \frac{d}{dt}\frac{\theta}{2\pi}. \tag{2.47}$$

From (2.47) the phase noise can be defined as the fractional frequency deviation from the carrier frequency and is given by;

$$\begin{aligned}\Delta_f(t) &= \frac{f(t) - f_c}{f_c} \\ &= \frac{d}{dt}\frac{\theta(t)}{\omega_c}.\end{aligned} \tag{2.48}$$

For a system that is free running (i.e., the system where the frequency is locked whereas the phase is not locked), the fractional deviation Δ_f is modeled as zero mean white Gaussian random process.

Electronic components of the PLL cause different types of noises such as thermal noise, short noise and flicker noise. These phase noises can be modeled by the Leeson expression as follows;

$$\begin{aligned}L(fm) &= 10\log\frac{FKT}{2P_{avg}}\left[1 + \frac{f_c}{f_m} + (\frac{f_o^2}{2fmQ})^2(1 + \frac{fc}{fm})\right] \\ &= 10\log\frac{FKT}{2P_{avg}}\left[1 + \frac{f_o}{f_m} + \frac{1}{f_o^2}(\frac{f_o^2}{2Q})^2 + \frac{f_o}{f^3}(\frac{f_o}{2Q})^2\right].\end{aligned} \tag{2.49}$$

From Equation (2.49), it can be observed that the oscillator phase noise can be controlled by reducing the device flicker frequency (fo). Furthermore the phase can be controlled by reducing the half bandwidth term $(fo/2Q)$. The half bandwidth term can be reduced by choosing the appropriate active device (Gunn or IMPATT Diodes, bipolar and field transistors).

Oscillators tend to amplify any noises that are closer to their harmonics and oscillation frequency . The transfer function of the VCO is given by ;

$$H(s) = \frac{1}{1 + \Gamma_{Amp}\Gamma_{PD}\left[\frac{1+sR_2C_2}{s^2R_2C_1C_2+s(C_1+C_2)}\right]\left[\frac{\Gamma_{vco}}{Ns}\right]}. \tag{2.50}$$

where

$$\Gamma_{PD} = \text{Gain at the phase detector.} \tag{2.51}$$

$$\Gamma_{vco} = \text{Gain at the VCO.} \tag{2.52}$$

$$\Gamma_{LF} = \text{Gain at the loop filter.} \tag{2.53}$$

$$\Gamma_{tot} = \text{Total loop gain.} \tag{2.54}$$

The magnitude of the phase noise can be controlled by choosing suitable RC components to achieve an optimum tuning range. A very wide tuning range results in poor phase noise while careful selection of RC components can suppress and correct phase noise. Like any linear time-invariant system, the VCO excess phase can be expressed as

$$\theta_{out} = \Gamma \int_{-\infty}^{t} V_{cont} dt. \tag{2.55}$$

In designing a proper system that will lock and provide the required phase offset it is necessary to increase the loop gain ($\Gamma_{tot} = \Gamma_{PD}\Gamma_{VCO}$) such that;

$$\begin{aligned} \theta_o &= \frac{V_1}{\Gamma_{PD}} \\ &= \frac{\omega_1 - \omega_2}{\Gamma_{PD}\Gamma_{VCO}}. \end{aligned} \tag{2.56}$$

From Equation(2.56) it is observed that the phase errors can be reduced by increasing the total loop gain of the system. The loop gain is therefore a very critical parameter in the design of PLL and proper selection of the loop gain parameter leads to better loop stability that settles at shorter times.

The significance of the loop gain is so vital that the transfer function and phase error are also dependent on this parameter as shown in Equation (2.57);

$$\begin{aligned} H(s) &= \frac{y_{out}(t)}{x_{in}(t)} \\ &= \frac{\Gamma_{PD}}{1 + \Gamma_{Tot}(s)}. \end{aligned} \tag{2.57}$$

$$\theta_e(s) = \frac{x_{in}(s)}{1+\Gamma_{Tot}(s)}. \tag{2.58}$$

2.3.1.4 Phase Detector

The phase detector (PFD) is mainly used to generate the error signal needed by the feedback path of the PLL loop. The signal is multiplied by the integer ratio and the results are compared with the reference frequency signal ($F_r = \frac{F_{vco}}{N}$). The PLL plays a very important role in PLL as it detects the phase and frequency of the signal. For example, if it detects that the phase of the signal is greater than 2π, the divide will be deemed to be in a frequency detect mode and in phase detect mode if it is less than 2π. As shown in Figure 2.13, the PFD generates a digital pulse with a width that is equal to the phase error.

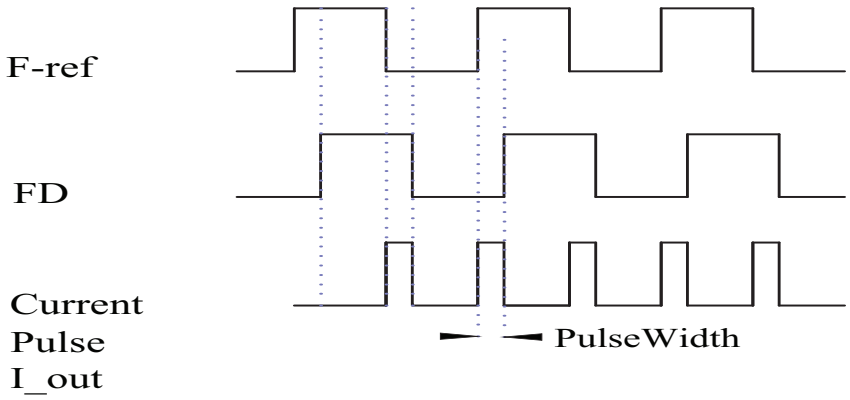

Figure 2.13: Frequency divisions and reference waveforms [57].

The phase detector compares the phases of the incoming signals and computes the generated error as follows;

$$e_v(t) = \Gamma_{PD}[\theta_{out} - \theta_{in}]. \tag{2.59}$$

If the two input signals are assumed to be;

$$\alpha(t) = \alpha\cos(\omega_o t + \theta_{alpha}). \tag{2.60}$$

$$\beta(t) = \beta\cos(\omega_o t + \theta_{beta}). \tag{2.61}$$

the error signal can be derived by taking the product of the two input signals as follows;

$$e_v(t) = \alpha \times \beta \tag{2.62}$$

$$= \frac{\alpha\beta}{2}[\cos(2\omega + \theta_\alpha + \theta_{beta}) + \cos(\theta_\alpha - \theta_{beta})]. \tag{2.63}$$

The most significant observation about the PLL error signal is that the input signals contain two identical frequencies at the time the loop locks. Again the error signal has a double frequency component that will be removed by the low pass filter. The transfer function of the PD is given by [58];

$$H(s) = \frac{\left[\frac{1+sC_2R_2}{s^2R_2C_1C_2+s(C_1+C_2)}\right]\frac{\Gamma_{vco}}{s}}{1+\Gamma_{Amp}\Gamma_{PD}\left[\frac{1+sR_2C_2}{s^2R_2C_1C_2+s(C_1+C_2)}\right]\left[\frac{\Gamma_{vco}}{Ns}\right]}. \tag{2.64}$$

2.3.1.5 Loop Filter

In many cases, passive loop filters made of resistor-capacitor (RC) components are used to control phase in PLL systems. For many wireless applications, the RC elements are connected directly to the PLL current source and VCO, where the output of the current source generates the control voltage with noise that is directly proportional to the phase noise error.

The simplest way to realize the loop filter in PLL simulation is through the implementation of a suitable resistor and capacitor. The RC parameter must be carefully determined to ensure the correct cut-off frequency $f_c = \frac{1}{2\pi RC}$ that is (just) above the modulating wave to allow the whole signal to pass-through.

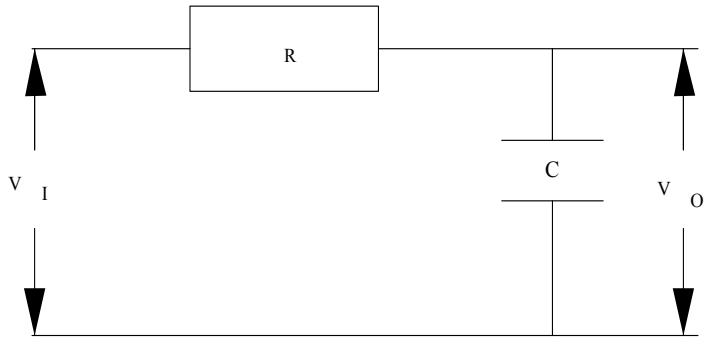

Figure 2.14: Schematic representation of PLL simulation parameters.

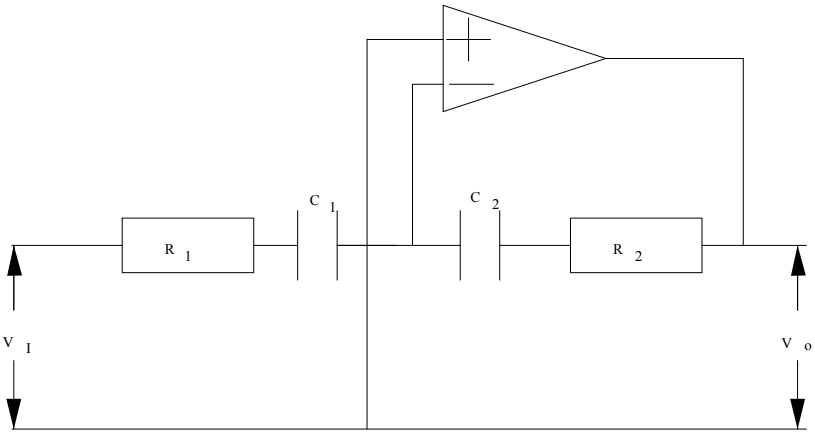

Figure 2.15: Schematic representation of active lead-lag filter.

The first order transfer function for a passive filter is given by;

$$H(s) = \frac{s+\omega_z}{s+\omega_p} \tag{2.65}$$

$$= \frac{1+s/2\pi f_z}{1+s/2\pi f_p}. \tag{2.66}$$

Although higher order loops have stability problems, they offer far better flexibility when it comes to the selection RC components. The most commonly used loop filter is the second order Butterworth low filter with the transfer function given by;

$$H(s) = \frac{b}{s^2+as+b}. \tag{2.67}$$

where the filter parameters

$$a = \frac{\omega_o}{0.707}. \tag{2.68}$$

$$b = \omega_o. \tag{2.69}$$

The transfer function of the current source loop filter is given by;

$$H(s) = \frac{\Gamma_{vco}/s}{1+\Gamma_{Amp}\Gamma_{PD}\left[\frac{1+sR_2C_2}{s^2R_2C_1C_2+s(C_1+C_2)}\right]\left[\frac{\Gamma_{vco}}{Ns}\right]}. \tag{2.70}$$

2.3.2 Phase error tracking with PLL

The PLL technique is concerned with the tracking of phase errors with respect to the incoming signal. The advantage of using PLL is that it has a narrow bandwidth that makes it impossible for the sideband components to perturb the carrier signal.

The basic operation of the PLL is that a phase-locked loop circuit responds to the phase and frequency of the input signal at the same time and adjusts the frequency of the VCO until it matches the reference signal with respect to the frequency and phase. The PLL is specified by the capture or lock range, input frequency range and the acquisition time as follows;

- By locking the frequency range: it specifies the frequency range over which the PLL can lock on the signal or drop synchronization.
- Input frequency range: it specifies the input frequency signal in which the PLL works correctly.
- Acquisition time: it specifies the time needed by the PLL to generate the desired frequency within the required precision.

The acquisition mode is specifically set to synchronize the frequency and phase of the voltage control oscillator (VCO) output with that of the input signal.

The complexity of operating a PLL in an acquisition mode gets more noticeable as the phase errors between the input and output signals increase. For these reason, the acquisition mode does not enjoy more popularity as it is difficult to reduce phase errors. On the other hand the tracking mode is characterized by small phase errors that can be analyzed through simple linear models. As shown later in the simulation results, PLL has the following drawbacks;

- At low order LPF, the loop shows high frequency ripples, which leads to the instability of the PLL loop.
- The tracking range of the PLL increases with the order of the LPF.
- All PLL need a settling time before they can recover the carrier signal.

The transfer function of the PLL can be modeled in terms of it's output and input phases as fol-

lows;

$$H(s) = \frac{\theta_{out}}{\theta_{in}} = \frac{\Gamma_{PD}\Gamma_{vco}F(s)/s}{1+\Gamma_{PD}\Gamma_{vco}F(s)}. \tag{2.71}$$

and the difference between the output and input phases can be used to compute phase errors as follows;

$$\theta_e(t) = \theta_{in} - \theta_{out} = \frac{s\theta_{in}}{s+\Gamma_{PD}\Gamma_{vco}F(s)}. \tag{2.72}$$

$F(s)$ is the Filter Transfer function given by

$$F(s) = \frac{1}{1+s/\omega_1}. \tag{2.73}$$

where $\omega_1 = \frac{1}{RC}$.

Now the second order loop gain can be altered slightly to a new form given by

$$\Gamma(s) = \frac{\Gamma_{tot}}{s(1+s/\omega_1)}. \tag{2.74}$$

2.3.3 PLL with Additive Noise

Assume the receiver detects a signal (with amplitude A and period T_s) that is corrupted by AWGN $(\eta(t))$ with normal distribution $\aleph(0,\sigma^2)$, the received signal can be expressed as;

$$y(t) = A\sqrt{2}T_s\cos(\omega_c + \phi) + \eta(t). \tag{2.75}$$

The phase of the received signal can be estimated by multiplying $y(t)$ by $\sqrt{2/T_s}\cos(\omega_c t)$ and $-\sqrt{2/T_s}\sin(\omega_c t)$ to yield;

$$\begin{aligned} y_I(t) &= \int_0^T sy(t)\sqrt{2/Ts}\cos(\omega_c t)dt\sqrt{2/Ts}\cos(\omega_c t)dt \\ &= A\cos\phi + \eta_I. \end{aligned} \tag{2.76}$$

Similarly

$$y_{Q(t)} = A\sin\phi + \eta_Q. \tag{2.77}$$

The PDF of the sample values y_I and y_Q given ϕ is;

$$P_{y_I,y_Q|\phi}(y_I,y_Q|\phi) = \frac{1}{2\pi\sigma^2}exp(y_I - A\cos\phi)^2 + (y_Q - A\sin\phi)^2/\sigma^2. \tag{2.78}$$

where the *posterio* PDF of the detected signal phase ,ϕ, is given by;

$$P_{\phi|y_I,y_Q}(\phi|y_I,y_Q) = \frac{P_{y_I,y_Q|\phi}(y_I,y_Q|\phi)P_\phi(\phi)}{P_{y_I,y_Q}(y_I,y_Q)}. \tag{2.79}$$

The phase estimate, $\hat{\phi}$, can be realized by following the same method used in [59] and also applying the maximum likelihood estimation (MLE) technique, where the value of ϕ that maximizes the posteriori pdf can be found by taking the derivatives of the conditional pdf that contain the ϕ terms as, such that;

$$\ln P(\phi) = \frac{2A}{\sigma^2}(y_I\cos\phi + y_Q\sin\phi)\frac{\partial}{\partial\phi}\ln(P) \tag{2.80}$$

$$= \frac{2A}{\sigma^2}(-y_I\sin\phi + y_Q\cos\phi) = 0 \tag{2.81}$$

$$\tan\phi = \frac{y_Q}{y_I}. \tag{2.82}$$

The phase estimate is therefore given by;

$$\hat{\phi} = \arctan \frac{y_Q}{y_I} \tag{2.83}$$

$$= \arctan - \int_0^{T_s} y(t)\sin(\omega_c t)dt \int_0^{T_s} y(t)\cos(\omega_c t). \tag{2.84}$$

Furthermore $\hat{\phi}$ can be tracked by setting $\int_0^{T_s} y(t)\sin(\omega_c t + \hat{\phi})dt = 0$, so that $V_{LF} = \int_0^{T_s} y(\tau)\sin(\omega_c \tau + \hat{\phi})d\tau$.

Consider the basic PLL model where the output of the phase detector $e_{PD}(t)$ is amplified by the loop amplifier gain, Γ_{LA}, and passed through the loop filter to generate;

$$e_{PDO}(t) = A_i A_j[sin(\hat{\theta} - \theta)] + \eta(t). \tag{2.85}$$

where

$$\eta(t) = \frac{\eta_d(t)}{A_i}\sin(\theta(t)) + \frac{\eta_q(t)}{A_i}\cos(\theta(t)). \tag{2.86}$$

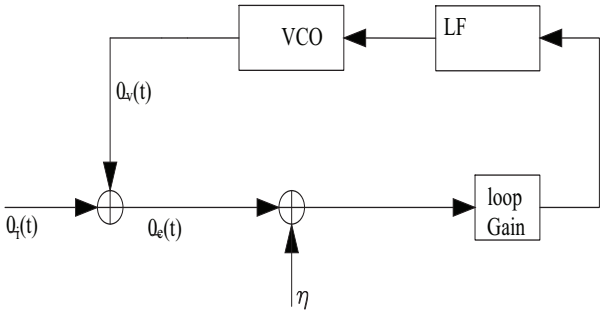

Figure 2.16: Structure of PLL phase noise model with additive noise.

In the presence of noise, $\eta(t)$ has a zero mean and variance given by;

$$\sigma_\eta = \frac{\sigma_n^2}{A_i^2} \tag{2.87}$$

The signal to noise ratio is defined by $(SNR_i = \frac{A_i/2}{\sigma_n^2})$. This implies that the phase variance can be

expressed in terms of the SNR as follows;

$$(SNR) = \frac{A_i^2/2}{2N_0BW}. \tag{2.88}$$

The noise bandwidth can be modeled by means of the transfer function that relates the phase of the $VCO, \theta(t)$ and Loop Filter with the noise ηt. Such a transfer function is given by;

$$\begin{aligned} H(s) &= \frac{\Gamma_{vco}F(s)/s}{1+\Gamma_{vco}F(s)/Ns} \\ &= \frac{N(1+s/\omega_2)}{Ns^2/\Gamma_{vco}+s/\omega_2+1}. \end{aligned} \tag{2.89}$$

The VCO noise can be controlled by making use of Equation (2.90);

$$\begin{aligned} H(s) &= \frac{\theta_{out}}{\theta_{ref}} \\ &= \frac{1}{1+\Gamma_{vco}F(s)/Ns} \\ &= \frac{Ns^2/\Gamma_{vco}}{Ns^2/\Gamma_{vco}+s/\omega_2+1}. \end{aligned} \tag{2.90}$$

From Equation (2.90), it can be seen that the VCO noise can be controlled by adjusting the value of (s). For example, if (s) increases substantially, the magnitude of the VCO phase noise approached 1, which confirms that the PLL can be used to remove the noise caused by the local oscillators.

The VCO phase has a spectral density given by;

$$S_{\theta_{\eta}(t)} = S_{\eta}\|H(f)\|^2. \tag{2.91}$$

The variance of the VCO noise with respect to noise is determined from Equation 2.94;

$$\sigma_{\theta_n} = \int_0^{\infty} \|H(f)\|^2 df \tag{2.92}$$

$$= \frac{2N_0}{A_i^2}\int_0^{\infty} \|H(f)\|^2 df \tag{2.93}$$

$$= \frac{2N_0}{A_i^2}BW. \tag{2.94}$$

where $BW = \int_0^{\infty} \|H(f)\|^2 df$ is the noise bandwidth. It can be shown the noise for the first, second and third order PLL are modeled by;

$$BW_{1st} = \frac{\Gamma}{4} \tag{2.95}$$

$$BW_{2nd}(Perfect) = \frac{\Gamma}{4}\left(1+\frac{a}{\Gamma}\right) \tag{2.96}$$

$$BW_{2nd}(Imperfect) = \frac{\Gamma}{4}\left(\frac{\Gamma+a}{\Gamma+\lambda a}\right) \tag{2.97}$$

$$BW_{3rd} = \frac{\Gamma}{4}\left(1+\frac{a}{\Gamma}+\frac{b}{\Gamma a}\right)\left(1-\frac{b}{\Gamma a}\right). \tag{2.98}$$

Figure 2.17 shows the PDF of the phase noise error. If the SNR is increased significantly enough, the PDF of phase noise looks like a Gaussian distribution. But if the SNR is reduced drastically, the PDF becomes uniformly distributed such that $p(\theta - e) = 1/2\pi$, where $-\pi < \theta_e < \pi$.

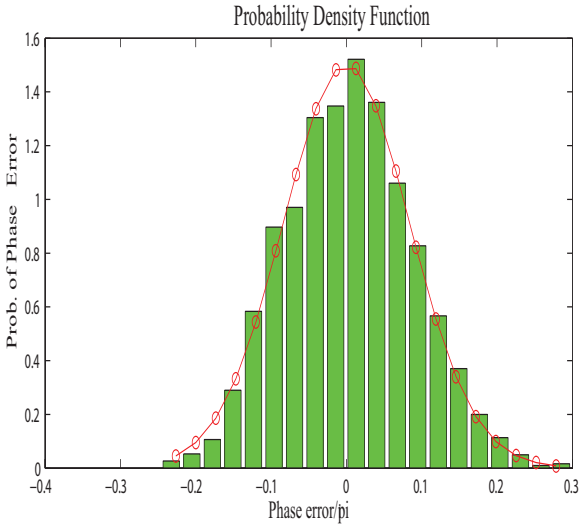

Figure 2.17: Probability Density Function of Phase Error

2.3.4 Phase error tracking with 2^{nd} order PLL

The transfer function of a second order PLL is given by;

$$H_2(s) = \frac{\Gamma(s+a)}{s^2+\Gamma s+\Gamma a}. \tag{2.99}$$

The denominator of the transfer function $H_2(s)$ is normally expressed in a standard second-order linear system to yield [59];

$$S_L(s) = s^2 + 2\zeta(2\pi f_n)s + (2\pi f_n)^2. \tag{2.100}$$

where ζ and f_n (Hertz) are the damping factor and natural frequency of the loop respectively. By following the same procedure applied in [60] the ζ and f_n terms can be set as;

$$\omega_n = \sqrt{\frac{\Gamma}{2\tau_1}} \tag{2.101}$$

$$\zeta = \frac{\Gamma\tau_2}{4\omega_n\tau_1}. \tag{2.102}$$

Where τ_1 and τ_2 and the loop parameters. The loop gain Γ is defined by;

$$\Gamma = 4\pi\zeta f_n. \tag{2.103}$$

The filter parameter is determined from the loop gain expression (2.103) and is given by;

$$P_f = \frac{2\pi(f_n)^2}{\Gamma} = \frac{\pi f_n}{\zeta}. \tag{2.104}$$

A control circuit in which the frequency is tuned by adjusting the reverse bias on the varactor diode is presented in [19], where suitable frequency tracking parameters are proposed in [61] .

2.3.5 Analysis of phase error tracking using PLL

The tracking mode assumes that the PLL is locked to the signal. In this case the tracking mode can be defined as a process whereby the PLL seeks to align itself with the incoming signal in light of the frequency and phase disturbances. If a second order transfer function is considered, the phase error transfer function can be shown to be [59];

$$\theta_e(t) = \frac{s\theta_i(s)}{s + A_{VCO}A_dF(s)}. \tag{2.105}$$

where $\theta_e(t)$ denotes the PLL phase error, $\theta_i(s)$ denotes the phase of the input signal, $F(s)$ represent the transfer function of the filter, A_{VCO} and A_d represent the gains of the VCO and phase detectors respectively.

To determine the steady state response of a PLL system, the Final Value Theorem (FVL) from the Laplace Transform function is applied as follows:

$$\lim_{t\to 0}\theta(t) = 0. \tag{2.106}$$

Equation (2.106) indicates that the phase and frequency errors are corrected by setting and controlling the phase and frequency of the input signal to a unit step.

The phase tracking model seeks to correct phase errors that may arise as a result if frequency and phase disturbances, which could result when;

- The input experiences sudden phase shift.
- There is a jump in the input frequency.
- The input frequency experiences a slow variation due to Doppler effect.

2.3.6 Phase change at the input

Any sudden phase change at the input can be modeled by assuming a unit step function $u(t)$ with $\Delta\theta$ representing the size of the step such that;

$$\theta_i(t) = u(t)\Delta\theta. \tag{2.107}$$

The Laplace transform is applied to Equation (2.107) to generate Equation (2.108);

$$\theta_i(t) = \frac{\Delta\theta}{s}. \tag{2.108}$$

Application of the final value theorem and taking the limit of Equation 2.108, yields;

$$\lim_{t\to 0}\theta_e(t) = \lim_{s\to 0}\frac{s^2}{s + A_{VCO}A_d F(s)}\frac{\Delta\theta}{s} = 0. \tag{2.109}$$

This simply means that when the unit step is applied to the PLL systems, the error signal will suddenly approach zero in time. However, a fundamental problem that needs to be addressed is the duration it takes to track the phase error. Equation (2.110) can be used to address this problem.

$$\theta_e(t) = \Delta\theta[\cos\sqrt{1-\zeta^2}\omega_n t - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\omega t]e^{-\zeta^2\omega_n t}. \tag{2.110}$$

where the damping factor $\zeta < 1$.

From Equation (2.110), it can be observed that at higher dumping factor, ζ, the system experiences higher oscillations. The optimal dumping factor for wireless communication systems is 0.707.

2.3.7 Shift in Input frequency

If there is a sudden shift in frequency (input), the phase change observed by the PLL becomes a ramp instead of a step such that the input phase can be expressed as a function of time as follows;

$$\theta_i(t) = \Delta\omega t. \tag{2.111}$$

$$\theta_i(s) = \frac{\Delta\omega}{s^2}. \tag{2.112}$$

The expression for tracking phase errors as result of a sudden frequency shift at the input is given by;

$$\theta_e(t) = \frac{\Delta}{\omega_n}[\frac{1}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\omega_n t]e^{-\zeta^2\omega_n t}. \tag{2.113}$$

2.3.8 Analysis of Results

The simulation study was conducted to compare the effectiveness of the Loop Filter parameter and the Integrator. Figure 2.18 shows the simulation results where the phase estimated using a LF parameter with a high frequency gain, where it is observed that the estimator takes a longer time to track the phase signal. However, when the LF parameter is replaced with an integrator $\frac{\Gamma_{tot}}{s}$, it takes a shorter time to estimate and track the signal. This is confirmed in Figure 2.19.

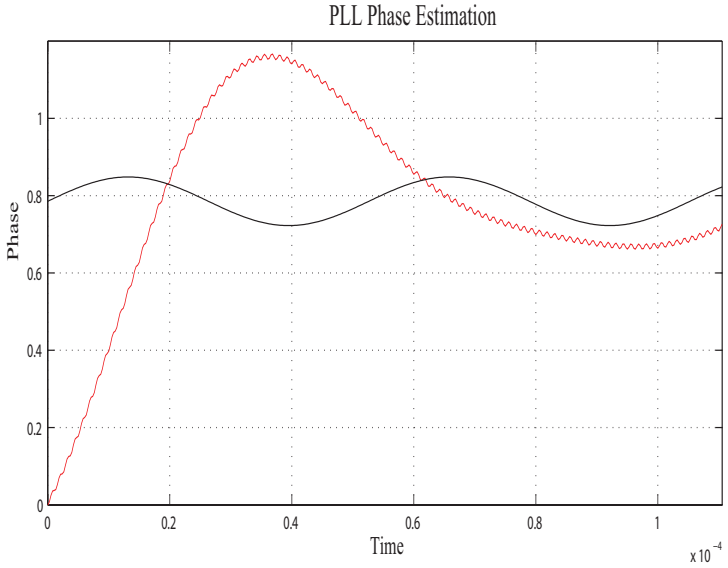

Figure 2.18: Simulation of PLL phase error estimation with loop filter parameter.

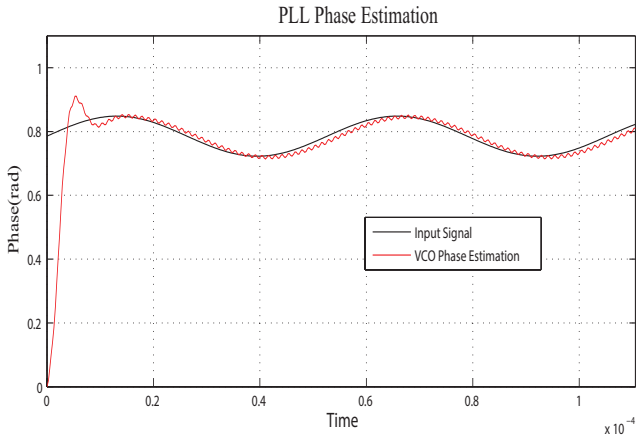

Figure 2.19: Simulation of PLL phase error estimation using an integrator.

The loop gain(Γ) and filter parameters in Equation (2.104) are significant parameters that are normally manipulated to get better results. By carefully selecting and controlling the loop gain, damping factor and the natural frequency a perfect second order PLL Figure 2.20 is generated, where it is observed that based on the selected loop gain and filter parameters it takes only one cycle to achieve phase lock with zero steady phase errors.

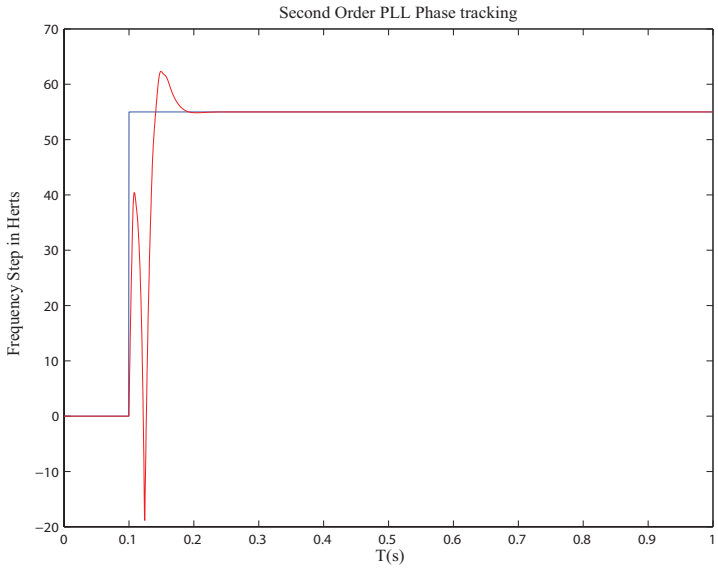

Figure 2.20: Phase error tracking with second-order PLL.

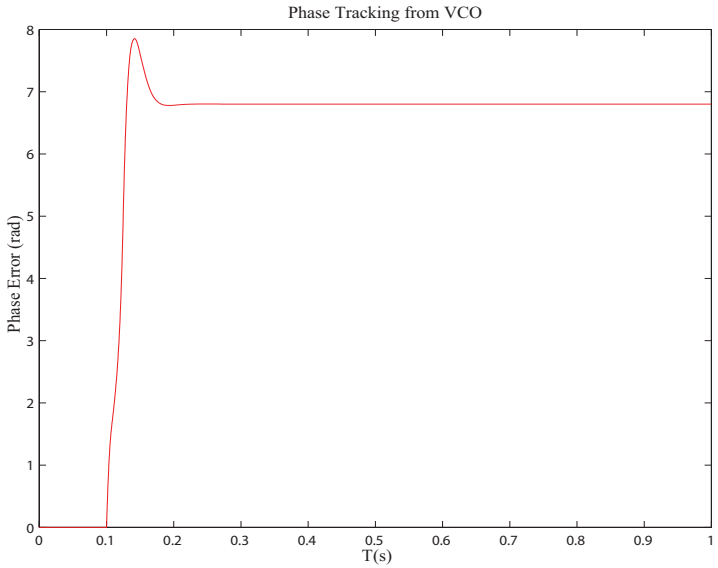

Figure 2.21: Corresponding phase error plot.

A possible drawback to second-order PLL is that in reality it takes excessive time to stabilize and requires careful and advanced designs to realize its full potential. The excessive or longer times

taken to settle can be mitigated by implementing the transport delay block. Figure 2.22 depicts the frequency deviation as a result of the implemented transport delay.

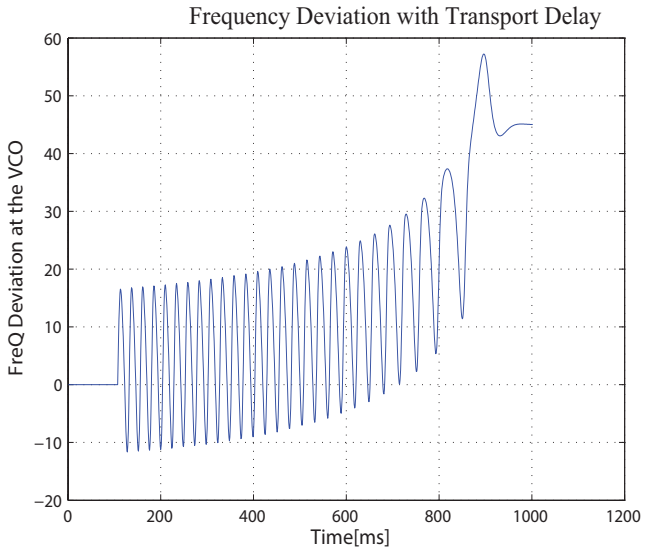

Figure 2.22: Frequency deviation with transport delay.

It can be observed from Figure 2.22 that it takes roughly 900ms to acquire the signal in response to the input frequency step. The relationship between frequency and phase error is governed by Equation (2.114). From Equation (2.114), it can be observed that if the operating point equals zero, i.e., $\frac{d\theta_e(t)}{dt} = 0$,

$$\sin[\theta_e(t)] = \frac{2\pi\Delta f}{\Gamma}. \tag{2.114}$$

and the fact that $\sin[\theta_e(t)]$ cannot be greater than 1 implies that;

$$2\pi\delta f \leq \Gamma. \tag{2.115}$$

Equation (2.115) is significant in the study of phase noise tracking as it implies that the loop can only lock when $2\pi\delta f \leq \Gamma$. Since the steady-operating point is realized at $\frac{d\theta_e(t)}{dt} = 0$, the steady-state phase error can be modeled as;

$$\Gamma \sin\theta_{ss}(t) = 2\pi\Delta f \tag{2.116}$$

$$\theta_{ss}(t) = \arcsin[\frac{2\pi\Delta f}{\Gamma}]. \tag{2.117}$$

Simulation results for a first-order PLL (with $\Gamma = 55$ and $Frequencyerror = 25 radians/seconds$) shows that for $2\pi\Delta f < \Gamma$ the frequency error decreases rapidly until it reaches zero, which implies that there is a loop lock as expected.

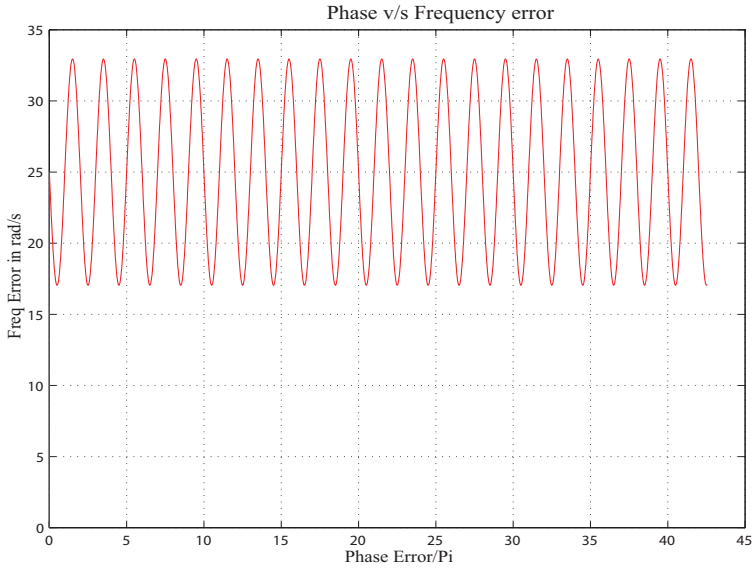

Figure 2.23: Phase error versus frequency error plot for first order PLL.

2.4 PLL WITH SIGMA DELTA MODULATOR

A basic PLL architecture does not provide a means to shape the noise error resulting from the quantization process, which causes significant amount of noise floor to appear on the baseband signal. The emergence of noise on the baseband signal reduces the SNR.

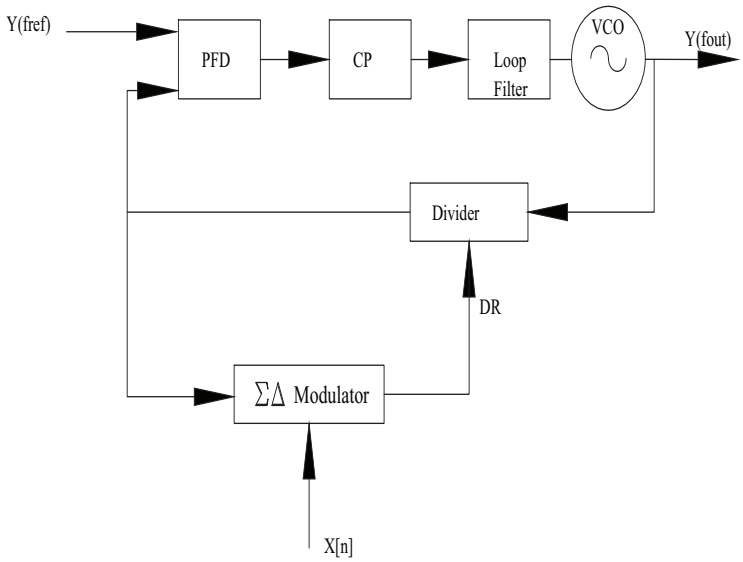

Figure 2.24: PLL with digital ΣΔ modulator.

Figure 2.24 illustrates a typical PLL with Sigma Delta modulator that is used to cancel quantization error. The sigma delta modulator ΣΔ over-samples the input signal, which allows the quantized noise to be shaped and shifted to higher frequencies, where higher frequencies can be removed by the LPF [41].

2.4.1 Phase error as main cause of Spurs

Assume a wordlength $(n_0 = 5)$ and the input signal $(X = 4)$ with $(N = 200)$ fractional divisions where the reference frequency is $(f_{ref} = 1.25MHz)$. The output frequency is calculated as follows;

$$F_o = \left[200 + \frac{4}{2^5}\right] * 1.25MHz \tag{2.118}$$

$$= 250.156MHz. \tag{2.119}$$

Assume 10 periodic cycles such that the frequency steps are $\frac{1}{10}f_{ref} = 0.1 * 1.25 = 0.125MHz$. During division process and when the carry out signal is unity, the actual signal divider value is set to 250 or 250.2, which is different from the modulus (250.156MHz) and this appears at the input of the PFD as *Phase error*. The periodicity in the resulting phase error causes spurious tones in the output spectrum. It is easy to deal with spurs that are outside the PLL bandwidth as they can be eliminated by LPF. However, removing those that appear inside the PLL bandwidth can be tricky as they modulate the VCO frequency and cause undesirable spurs in the output spectrum.

2.5 LOW ORDER ΣΔ MODULATOR

The main drawback of the PLL is that they tend to generate some white noise portions that are integrated within the PLL's bandwidth. If the bandwidth of the PLL is large, the white noise tends to make a significant contribution to the phase noise. Fortunately, ΣΔ modulators are helpful in generating a well-shaped noise control sequence with noise power completely pushed outside the PLL bandwidth. As shown in Figure 1.7 the input to the ΣΔ modulator is X, which gives an output whose spectrum is attenuated at low frequencies but amplified at higher frequencies. Frequency attenuation at lower frequencies is necessary in that the portion of the power spectrum that passes through the LPF is rejected. The essence of ΣΔ modulators is to remove the unnecessary fractional tones.

ΣΔ modulators are normally modeled with discrete-time integrators and the resulting quantization noise errors, Q_e.

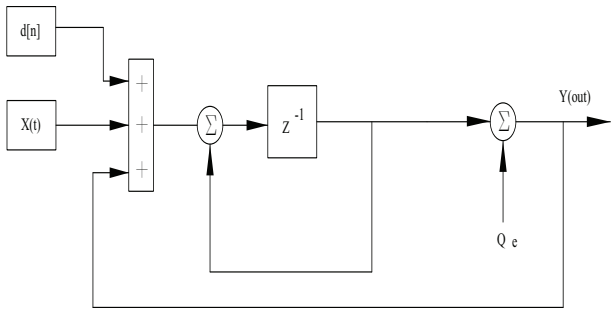

Figure 2.25: First Order ΣΔ modulator

The output of the first order ΣΔ modulator can be derived by employing a standard discrete-time signal analysis method as follows;

$$Y(Z) = Q_e Z + I(Z)[X(x) - z^{-1}Y(z)]. \tag{2.120}$$

Solving for Y, yields;

$$Y(z) = \frac{I(z)}{1+I(z)z^{-1}}X(z) + \frac{1}{1+I(z)z^{-1}}. \tag{2.121}$$

Since the integrator is defined by $(I(z) = \frac{1}{1-z^{-1}})$, the output of the first order ΣΔ modulator is simplified to;

$$Y(z) = X(z) + (1-z^{-1})Q_e(z). \tag{2.122}$$

The signal and noise transfer functions are given by

$$\begin{aligned} STF &= \frac{Y(z)}{X(z)} \\ &= \frac{H(z)}{1+H(z)} \\ &= z^{-1}. \end{aligned} \tag{2.123}$$

$$\begin{aligned} NTF &= \frac{Y(z)}{Q_e(z)} \\ &= \frac{1}{1+I(z)} = (1-z^{-1}). \end{aligned} \tag{2.124}$$

The significance of the differentiator is that it pushes the error towards high frequencies, the high frequency quantization noise can be eliminated by the high pass filter.

A major advantage of ΣΔ modulators is that they use large multiples of sample rates (e.g., 128 times sample rates of a given signal), which results in better anti-aliasing and higher resolution. The over-sampling ratio (OSR) is commonly defined as the ratio of the sampling frequency and the Nyquist bandwidth ($OSR = \frac{f_s}{2f_B}$), which implies that the quantization noise can be reduced by 3dB per octave. The power of the quantization noise can be can be expressed in terms of the OSR as;

$$N_Q^2 = \frac{1}{f_s}\int_{fB}^{f} B\sigma_Q^2 df \tag{2.125}$$

$$= \frac{\sigma_Q^2}{OSR}. \tag{2.126}$$

The generalized form of calculating the quantization noise power is given by;

$$N_Q^2 = \frac{\sigma_Q^2 \pi^{2M}}{2M+1}\frac{1}{OSR^{2M+1}}. \tag{2.127}$$

For example, a first order ΣΔ has a quantization noise given by;

$$N_Q^2 = \frac{\sigma_Q^2 \pi^2}{3}\frac{1}{OSR^3}. \tag{2.128}$$

From Equation (2.128), it can be seen that if the OSR is increased by a factor of 2, the in-band noise will decrease by a 9dB/Octave.The ΣΔ for a second order quantization noise given by;

$$N_Q^2 = \frac{\sigma_Q^2 \pi^4}{5}\frac{1}{OSR^5}. \tag{2.129}$$

This implies that if the OSR is increased by a factor of 2, the in-band noise will decrease by 15 dB. From Equations 2.128 and (2.129), it can be deduced that the quantization noise can be reduced to $3(2M+1)dB$ by doubling the OSR or the sampling frequency.

The noise error due to the quantization process is determined as follows;

$$\begin{aligned}\bar{Q_z^2}(kT) &= \int_{q/2}^{q/2} Q_e dQ_e \\ &= \frac{q^2}{12}.\end{aligned} \tag{2.130}$$

The inband quantization noise is given by;

$$\begin{aligned}\bar{N_I} &= \int_B^B N_Q(f)|NTF(z)|^2 df \\ &= \int_{fs/2M}^{fs/2M} \frac{1}{fs}\frac{q^2}{12}(2\sin\pi fT)^2 df \\ &= \frac{\pi^2}{3}\frac{1}{M^3}\frac{q^2}{12}.\end{aligned} \tag{2.131}$$

For an ideal M^{TH} order modulator, the inband noise power is given by

$$N_I^2 = Q_e^2 \frac{\pi^{2M}}{2^{M+1}} OSR^{-[2M+1]}. \tag{2.132}$$

Equation 2.132 implies that the output noise depends on the OSR, system order and actual quantization error. For example, adding an extra integrator to the modulator loop reduces the output noise by an extra factor (OSR/π^2).

From Figure 2.26 it can be observed that up to f_B, the baseband noise is smaller than that of the ideal low pass filter or Nyquist bandwidth.

2.5.1 Simulation of Low order ΣΔ modulator

The following simulation study was conducted in a bid to investigate and analyze how ΣΔ modulators eliminate spurious tones. The wordlengths were varied from $n_o = 9, 10, 14, 16, 18$ and the input signal, X, was simulated at 128 and 256. The PSD spectrum was plotted on a logarithmic scale.

The main drawback of the low order ΣΔ is that the quantization noise is dependent on the main signal. In other words, the quantization noise is correlated to the desired signal. In this case (first order ΣΔ modulators) the state variable of the system is determined from the output of the single

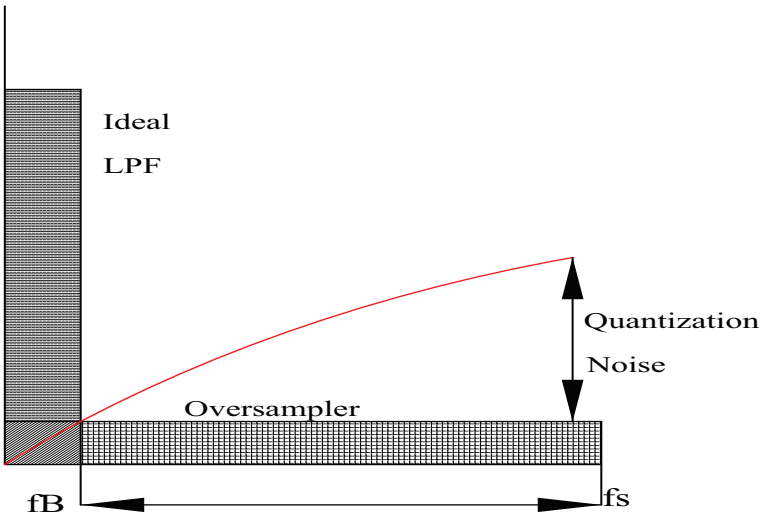

Figure 2.26: Representation of the first order ΣΔ noise shaper.

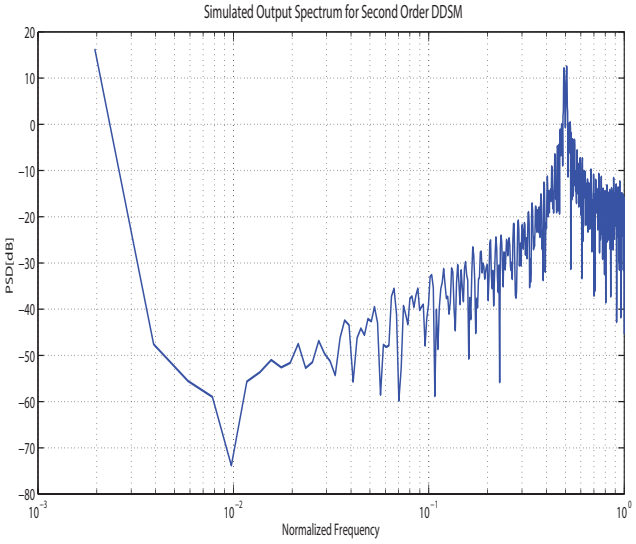

Figure 2.27: Simulated Output Spectrum of low order ΣΔ modulator.

integrator. Since this ΣΔ has a single integrator, the single variable causes the output bit streams to repeat themselves within a loop causing a large amount of energy of the output spectrum to be concentrated at multiples of repetition frequencies [62].

As seen from Figure 2.27, the output spectrum has some periodic quantization noise with spurs all over. This problem can be solved by dithering, normally implemented at the input of PLL loop. Another noticeable drawback of the low order ΣΔ is the lower resolution, which can be addressed by

the implementation of high-order ΣΔ architectures.

2.5.2 Higher-order ΣΔ modulators

From Equation 2.132, it was shown that adding the one integrator to the modulator loop reduces the output power by a factor of (OSR/π^2). It is also observed that doubling the OSR reduces noise by another factor of $2^{[2m+1]}$. The main advantage of higher order modulators is that they randomize the error sequence, which breaks short periodic cycle patterns. The second order modulator outputs can be obtained by assuming Q_{e1} and Q_{e2} as inputs to the second and third stage ΣΔ loops such that the output of the second-order ΣΔ modulator is;

$$\begin{aligned} Y_2(z) &= Q_{e1}(z) + (1-z^{-1})Q_{e2}(z) \\ &= X(z) + (1-z^{-1})^2 Q_{e2}(z). \end{aligned} \tag{2.133}$$

Similarly, the output of a third order modulator can be shown to be;

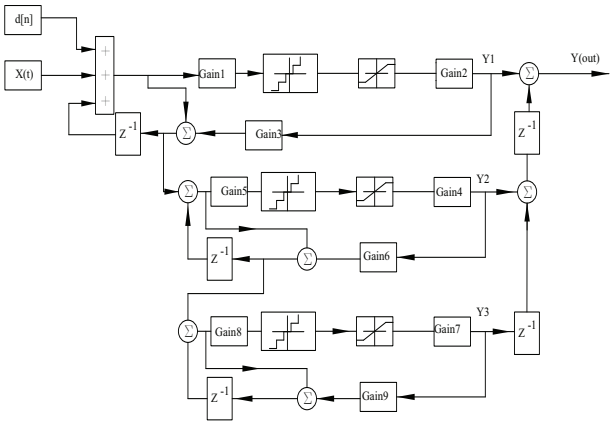

Figure 2.28: Third Order MASH 1-1-1 with digital ΣΔ modulator.

$$Y(z) = X(z) + (1-z^{-1})^2 Q_{e3}(z). \tag{2.134}$$

The output of the higher-order ΣΔ modulator can be generalized from Equations 2.133 and 2.158 as follows;

$$Y(z) = X(z) + (1-z^{-1})^N Q_{eN}(z). \tag{2.135}$$

where Q_{eN} is the quantization noise generated by the $N-th$ ΣΔ loop.

2.5.3 N^{th} Order ΣΔ modulators

A standard ΣΔ modulator is composed of the transfer function H(z), the quantizer, Q(z) and the digital to analog converter (DAC). The loop filter (LF) of low order ΣΔ can be modeled by the forward Euler integrators' transfer function given by;

$$H(z) = \frac{z^{-1}}{1-z^{-1}}. \tag{2.136}$$

The output of the multistage architecture is modeled in by Leslie and Singh [63] as;

$$Y(z) = STF.H_{dec}(z)U(z) + NTF_D.H_{dec}(z).Q_2(z) \tag{2.137}$$

Where STF and NTF are the signal transfer and noise transfer functions respectively, which are given by;

$$\begin{aligned} NTF &= (1-z^{-1})^M \\ STF &= H(z) = 1 \\ H_{dec} &= \frac{1}{N^M}\frac{(1-z^{-N})^{M1}}{(1-z^{-1})^{M1}}. \end{aligned} \tag{2.138}$$

Where

$$\begin{aligned} N &= \text{The decimation factor} \\ M1 &\geq M. \end{aligned}$$

Kirk *et al.* [62] modified and presented the overall system function that can be used to model higher order architectures.

$$Y(z) = H_x(z)X(z) + H_E(z)E(z). \tag{2.139}$$

where

$$H_x(z) = \frac{\sum_{i=0}^{M} A_i(z-1)^{M-i}}{z[(z-1)^M - \sum_{i=1}^{M} B_i(z-1)^{M-i}] + \sum_{i=0}^{M} A_i(z-1)^{M-i}} \tag{2.140}$$

$$H_E(z) = \frac{(z-1)^M - \sum_{i=0}^{M} B_i(z-1)^{M-i}}{z[(z-1)^M - \sum_{i=1}^{M} B_i(z-1)^{M-i}] + \sum_{i=0}^{M} A_i(z-1)^{M-i}}. \tag{2.141}$$

The noise transfer function (NTF) of a higher order ΣΔ architecture is modeled by;

$$NTF = \frac{\prod^{M}((z-1)^2+g_j)}{\prod^{M}((z-1)^2+g_j)+\sum_{i=1,j=1}^{n,m}(z-1)^{j-1}(a_{2j-1}(z-1)+a_j)\prod^{M}((z-1)^2+g_k)}. \quad (2.142)$$

Where

$$n = \text{number of integrators.}$$
$$m = \text{number of local oscillators.} \quad (2.143)$$

The coefficients A_i and B_i are determined by first setting the feedback coefficients to zero, which is achieved by computing the s-domain poles and converting them into z-domain by using the bilinear transform. The coefficients determine the stability of the modulator.

Although high order ΣΔ cancels the quantization noise as the order (M) increases, it does so with increasing system instability. System instability can be resolved by introducing the poles of the NTF. With the inclusion of poles, the NTF expression takes the following form;

$$NTF = \frac{(z-1)^n}{P(z)}. \quad (2.144)$$

The output of the third order high pass noise shaping ΣΔ modulator is given by;

$$Y(z) = X(z)z^{-2} + [D_1(z)z^{-1} - D_2(z) + E_2(Z)](1-z^{-1})^3. \quad (2.145)$$

Now the NTF can be determined using the z-transform as follows;

$$\begin{aligned} NTF(z) &= \frac{V(z)}{Q(z)} \\ &= \frac{1}{1+H(z)} \\ &= 1-z^{-1}. \end{aligned} \quad (2.146)$$

Higher order ΣΔ modulators have some limitations that can be observed from the signal transfer function ($STF = z^{-M}$) of the multistage system, which implies that there is a delay of M sampling periods. As the ΣΔ loop minimizes the difference between the input and output signal the delay

causes some errors, which leads to the creation of unnecessary harmonic components on the input signal.

The main drawback of the ΣΔ modulator is the mismatch between the integrating capacitors and the sampling, which normally results in some gain errors resulting from the cascaded switched-capacitors of the integrators. The transfer function with gain errors, Γ_e can be determined from;

$$H(z) = \frac{1+\Gamma_e}{z-1}. \tag{2.147}$$

where

$$\begin{aligned} \Gamma_e &= \Delta C \\ &= \frac{\Delta C_2}{C_2} - \frac{\Delta C_1}{C_1}. \end{aligned} \tag{2.148}$$

2.6 PHASE NOISE CANCELLATION WITH DIGITAL ERROR CORRECTION

Fischer and Davis presented a wideband cascade ΣΔ modulator with digital correction network [64] where the double third-order cascade modulator with digital noise cancellation was shown to be a potential candidate for correcting quantization noise.

In addition to the work presented in [64] the higher order ΣΔ modulator proposed by Kirk *at al.* [62] was modified by the addition of the modified noise cancellation network or correction factor, which corrects the quantization errors, remove non-linearities, suppresses harmonics and improves the SNR. Figure 2.29 depicts a cascaded multi-stage noise shaping (MASH) ΣΔ modulators consisted of two identical error feedback modulators (EFM). Each EFM has its own quantizer (Q) and unit delay z^{-1}. The error signal at the first stage is determined by subtracting u_1 from y_1 $e_1 = u_1 - y_1$ and this error is then carried over to the second EFM stage as follows:

$$u_1(z) = STF_1(z)S(z) + NTF_1(z).e_1(z). \tag{2.149}$$
$$u2(z) = STF_2(z)S(z) + NTF_2(z).e_2(z).$$

Since there are two identical EFM paths, the NTF of the first path must be equal to the signal transfer function (STF) of the second path such that;

$$NTF_1.H_1 = STF_2.H_2. \tag{2.150}$$

In this case H_1 and H_2 are digital filters that can be matched together and used as noise correction factor (NCF). The different stages of the MASH architecture are linked together by means of the coupling coefficients $C_i s$ such that the NTF at any stage can be expressed as;

$$NTF(z) = \frac{(1-z^{-1})^N}{\pi_{i=i}^{M} c_i}. \tag{2.151}$$

The coupling coefficients at different stages introduce some in-band noise (IBN) given by;

$$IBN = \frac{\Delta_e^2}{\pi}\int_0^{OSR}\frac{|NTF_1(e^{j\omega})|^2 \times NTF_2(e^{j\omega})|^2}{\pi_i c_i^2} = \frac{IBN_o}{\pi_i c_i^2}. \tag{2.152}$$

The significance of the NTF is that it allows the in-band noise to be controlled by making sure that the coupling coefficients are always greater than 1 $(c_i > 1)$.

Placing the correction factor outside the loop makes it possible to realize low latency by ignoring the latencies of the preceding integrators. The error correction factor of the architecture is $(-az^{-1} + z^{-M})$.

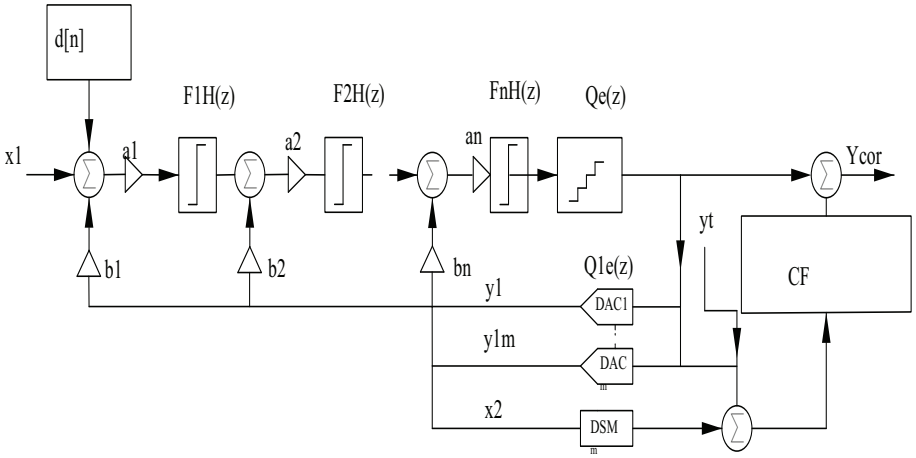

Figure 2.29: Higher-order ΣΔ modulator with error correction function $(-2z^{-1} + z^{-M})$.

In this case a correction scheme based non-linearity transfer function ($CF = -2z^{-1} + z^{-M}$) is added to correct the quantization errors and other non-linearity including harmonics. The output of the quantizer is given by;

$$Y_1(z) = X(z)Z^{-M} + Q_e(z)(1 - z^{-1})^M. \tag{2.153}$$

The corrected output, i.e., after the correction factor (CF) is given by

$$Y_{corr}(z) = X(z)Z^{-M} + Q_e(z)(1 - z_{-1})^M + (az^{-1} + z^{-M})Q_e(z)Y_1(z). \tag{2.154}$$

To improve the resolution, stability and efficiency of the proposed model, input signal was dithered. The inclusion of the random dither sequence was intended to break up the cycles and increase the effective cycle length, resulting in a well-shaped spectrum with minimum spurs or tones.

Table 2.4: Coefficients of the loop filter shown in Figure 2.29.

a_i	a_1	a_2	a_3	a_4	a_5
Coefficient Values	0.8653	1.1920	0.3906	0.06926	0.005395
b_i	b_1	b_2	b_3	b_4	b_5
Coefficient Values	0.000	$-3.5x10^{-3}$	$-3.547x10^{-3}$	$-3.134x10^{-6}$	$1.567x10^{-6}$

2.6.1 System stability

The system is stabilized by proper design and selection of the coefficients of the loop filters. There are several techniques that are used to design and find optimum coefficient values that can improve the stability of the system. In an effort to stabilize the system, Kirk *at al* [62] presented an approach for determining the optimum coefficients. The coefficients in Table (2.4) were obtained by trial and error with the approach presented in [62] used as a guideline.

2.7 RESEARCH GAP AND PROBLEM FORMULATION

Frequency synthesizers are expected to generate carrier waves that allow information signals to be transmitted at different frequencies. Several advancements made in the transceiver designs introduce different challenges that result in carrier frequencies being generated with unwanted spurious tones. The challenge of unwanted spurious tones within the frequencies of interest have attracted a lot of interest, which led to the development of several PLL frequency synthesizers architectures such as Integer-N frequency synthesizers and fractional-N frequency synthesizers that are known for producing low phase noise carriers [65, 66, 67, 68]. As shown in Figure 2.30, an output frequency is generated by multiplying the reference input with the negative feedback path $(f_{out} = f_{ref} + N \times N)$,where f_{out} is the output frequency and f_{ref} is the reference frequency.

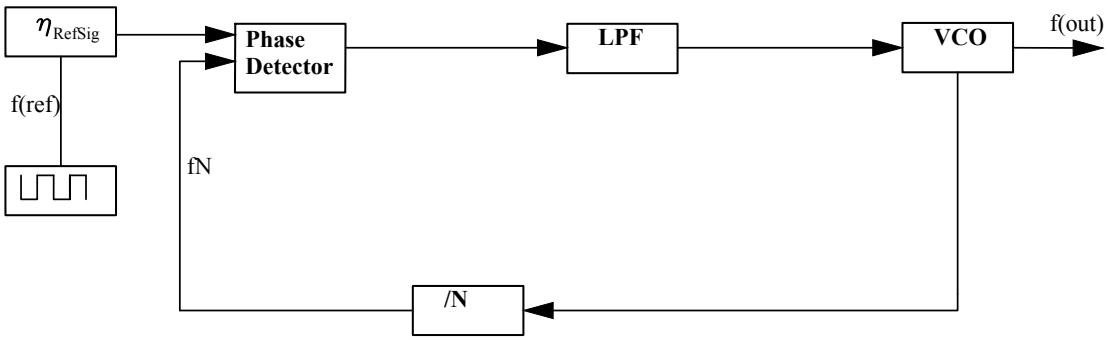

Figure 2.30: Schematic representation of PLL-based fractional-N integer frequency Synthesizer [28].

The integer-based frequency synthesizer has a fundamental limitation (long settling times) in that the minimum spacing channel is limited to the reference frequency, which is derived from the external crystal oscillator [69]. This implies that the resolution of the VCO will be exactly equal to that of the reference input at locked state. This limitation can be resolved by expressing the output frequency as follows [70]:

$$f_{out} = \left(N + \frac{X_i}{2^{b_o}}\right) \times f_{ref}. \tag{2.155}$$

The term X_i in Equation (2.155) represents the digital input, which is given by $(_i = 2^{b_0})$, where b_0 represents the number of bits. The relationship between the bit length and the frequency resolution is given by;

$$\Delta f = \frac{1}{2^{b_o}} \times f_{ref}. \tag{2.156}$$

Equation (2.156) implies that the frequency resolution can be improved by increasing the bit length only without being limited by the reference frequency. The addition of ΣΔ to the PLL frequency synthesizer block allows the FNPLL to have a wide range of step size and leads to better control and reduction of spurious tones within frequency of interest [71, 72, 73].

The main drawback of this technique can be demonstrated by making use of Equation (2.155), where the word length is taken as $(b_0 = 5)$, input signal $(X_i = 4)$, $(F = 200)$ and the reference frequency $(f_ref = 1.25)$, then the resulting frequency at the output of the FNPLL will be;

$$f_o = \left[200 + \frac{4}{2^5}\right] * 1.25MHz = 250.156MHz.$$

If a periodic cycles of 10 is assumed, the frequency steps can be determined as follows;

$$\begin{aligned} \frac{1}{10} f_{ref} &= 0.1 * 1.25 \\ &= 0.125MHz. \end{aligned} \tag{2.157}$$

If the carry out signal is set to unity during the division process, the actual signal divider value is rounded off and set to 250 or 250.2, which appears at the input of the phase detector frequency detector (PFD) as different value. Since the expected modulus was 250.156, the PFD records this as an error. The resulting phase error exhibits a periodicity that causes spurious tones in the output spectrum.

2.7.1 Analysis and evaluation of the FNPLL drawback

Assume the third order multi-stage noise shaping (MASH) 1-1-1 Digital ΣΔ modulator (shown in Figure 2.31). The MASH 1-1-1 digital ΣΔ modulator is realized by cascading the integrators.

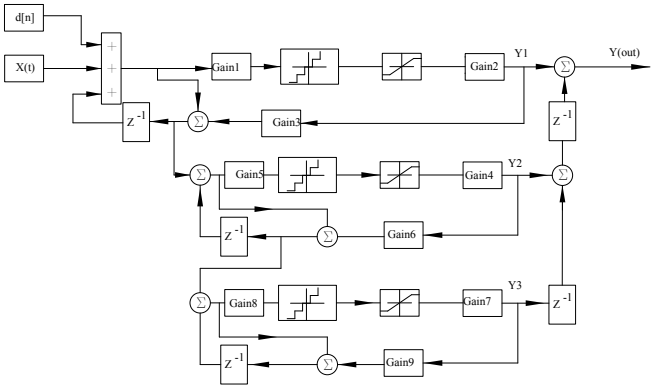

Figure 2.31: Third order MASH 1-1-1 digital ΣΔ modulator.

In the process of cascading the integrators in the modulator loop the output power is reduced by (OSR/π^2). By doubling the oversampling ratio (OSR), one can reduce the quantization noise by $2^{[2m+1]}$, where m represents the order of the modulator.

Every time an integrator is added an extra quantization noise is added, which can be subtracted from the output of the previous stage. A process of treating quantization noise was suggested in [74], where the quantization noise is whitened to prevent spectral tones.

Higher order modulators were introduced to take advantage of their ability to correct the error sequence, which breaks short periodic cycle patterns. A second order modulator output is realized by taking quantization errors Q_{e1} and Q_{e2} as inputs to the second and third stage ΣΔ loops where the output of the second-order ΣΔ modulator is given by [75];

$$Y(z) = X(z) + (1 - z^{-1})^2 Q_{e3}(z). \tag{2.158}$$

A generalization of the higher-order ΣΔ modulator expression can be realized as;

$$Y(z) = X(z) + (1 - z^{-1})^N Q_{e(N+1)}(z). \tag{2.159}$$

In Equation (2.159), $Q_{e(N+1)}$ represents the quantization noise that comes from the N^{th} ΣΔ

loop.

A standard ΣΔ modulator is composed of the transfer function H(z), the quantizer, Q(z) and the digital to analog converter (DAC). The loop filter of low order ΣΔ can be modeled by the forward Euler integrators transfer function given by;

$$H(z) = \frac{z^{-1}}{1-z^{-1}}. \tag{2.160}$$

The output of the multistage architecture is modeled as;

$$Y(z) = STF.H_{dec}(z)U(z) + NTF_D.H_{dec}(z).Q_2(z). \tag{2.161}$$

where STF and NTF are the signal transfer and noise transfer functions respectively, which are given by;

$$NTF = (1-z^{-1})^M. \tag{2.162}$$

$$STF = H(z) = 1. \tag{2.163}$$

$$H_{dec} = \frac{1}{N^M}\frac{(1-z^{-N})^{M1}}{(1-z^{-1})^{M1}}. \tag{2.164}$$

where

$$N = \text{The decimation factor}$$

$$M1 \geq M$$

The system function for modeling higher order architectures is presented in [62] as follows;

$$Y(z) = H_x(z)X(z) + H_E(z)E(z). \tag{2.165}$$

$H_x(z)$ and $H_E(z)$ are given by;

$$H_x(z) = \frac{\sum_{i=0}^{M} A_i(z-1)^{M-i}}{z[(z-1)^M - \sum_{i=1}^{M} B_i(z-1)^{M-i}] + C_i}. \tag{2.166}$$

where

$$H_E(z) = \frac{(z-1)^M - \sum_{i=0}^{M} B_i(z-1)^{M-i}}{z[(z-1)^M - \sum_{i=1}^{M} B_i(z-1)^{M-i}] + C_i}. \tag{2.167}$$

$$\begin{aligned} C_i &= \sum_{i=0}^{M} A_i(z-1)^{M-i} \\ D_i &= \sum_{i=0}^{M} A_i(z-1)^{M-i} \end{aligned} \tag{2.168}$$

Meison rule [76] is applied to model the noise transfer function (NTF) of a higher order ΣΔ architecture as follows;

$$\begin{aligned} NTF = & \frac{\prod^{M}((z-1)^2+g_j)}{\prod^{M}((z-1)^2+g_j)+\sum_{i=1,j=1}^{n,m}(z-1)^{j-1}} \times \\ & \frac{1}{(a_{2j-1}(z-1)+a_j)\prod^{M}((z-1)^2+g_k)}. \end{aligned} \tag{2.169}$$

where

$n =$ number of integrators

$m =$ number of local oscillators

The coefficients A_i and B_i are determined by first setting the feedback coefficients to zero, which is achieved by computing the s-domain poles and converting them into z-domain by using the bilinear transform. The coefficients determine the stability of the modulator.

In the process of noise cancellation as the order (M) increases, high order ΣΔ introduces some instability, which can be corrected through the introduction of poles [76] on the NTF.

The main drawback of higher order ΣΔ modulators can be seen from the STF ($STF = z^{-M}$) of the multistage system where there are some delays of M sampling periods. This implies that unnecessary harmonic components are generated when the ΣΔ loop tries to minimize the difference between the input and output signal. The mismatch between the cascaded switched-capacitors of the integrators causes some gain errors, which results in high signal fluctuations.

A third order MASH 1-1-1 digital ΣΔ modulator was simulated in Agilent-ADS to study its capability to eliminate spurious tones. Simulation results as shown in Figure 5.5 indicate that the high loop gains causes some fractional tones that appear within the frequency of interest. The main causes of the spurs is the mismatch in the integrators, which causes a large amount of energy to be concentrated at the output spectrum.

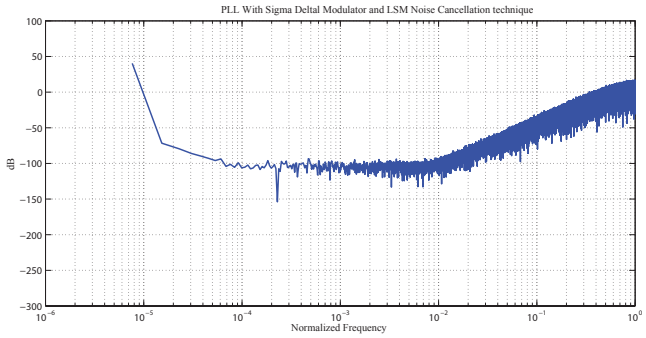

Figure 2.32: Simulated output spectrum of low order ΣΔ modulator.

2.7.2 Conclusion

This chapter discussed and analyzed the performance of existing phase noise cancellation techniques. The key performance metrics that are used to evaluate the performance of the PN techniques were discussed and analyzed in detail with the aid of Matlab simulation tool. The main drawbacks and limitations of the existing phase noise cancellation techniques were identified and presented. The main drawbacks presented in this chapter form the basis of the research gap and can be summarized as follows;

- Higher order $(M \geq 4)$ FNPLL exhibit short periodic cycles, which cause undesirable tones and unwanted spurious tones within the frequency of interest.

- Another challenge with higher order $(M \geq 4)$ FNPLL is that they have multistage systems composed of cascaded-switched-capacitors that act as integrators. Any mismatch in the cascaded-switched-capacitors results in gain errors that cause high signal fluctuations and instability within the signal in-band.

CHAPTER 3 RESEARCH METHODOLOGY

3.1 CHAPTER OBJECTIVES

This chapter discusses the research methodology that was followed in designing the new phase noise correction technique for a 2.4 GHz wideband frequency synthesizer.

3.2 ADOPTED RESEARCH STRATEGY

Existing phase noise correction techniques were reviewed and their performance were evaluated using Matlab simulation tool. Simulation results were analyzed using the key performance metrics (mean square error (MSE), Convergence rate, normalized projection normality (NPM), stability and computational complexity). The limitations and drawbacks of the existing techniques were highlighted and translated into a research gap areas that require further attention, which led to the formulation of a problem statement. The main steps followed are as follows

- A considerable amount of time was spent on analyzing the existing literature where some Matlab simulations were conducted to get a deeper insight into the existing techniques.
- The analysis was conducted with intentions of identifying limitations of the existing techniques.
- The limitations and drawbacks of the existing techniques were converted into problems statement and areas that require further studies.
- A new technique was designed that seeks to address the limitations and drawbacks of the existing techniques.
- Mathematical formulations for the new technique were derived and presented.

- The proposed technique was simulation in ADS where simulation results were compared with the existing technique to check if there is significant improvement.

The above-mentioned procedure is summarized in a flow diagram depicted in Figure 3.1.

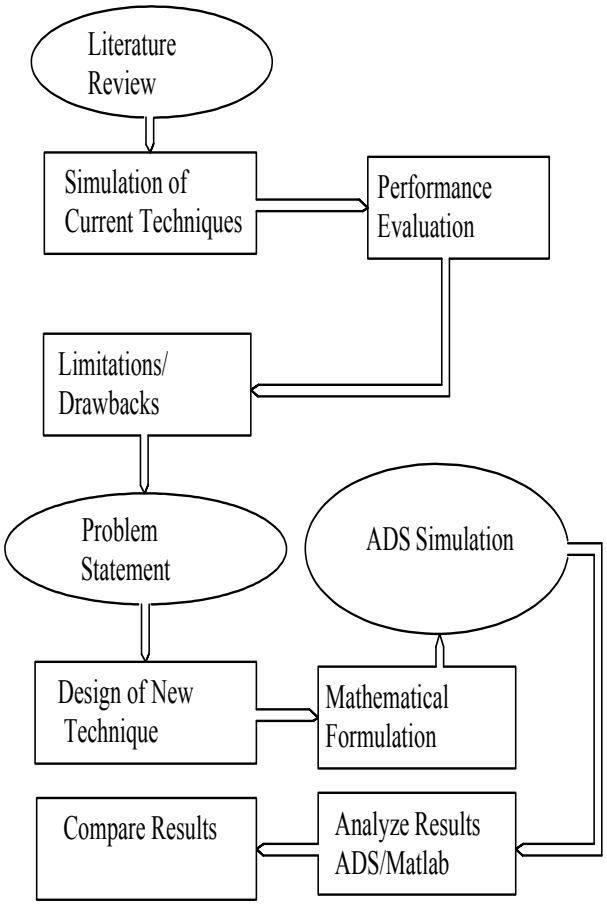

Figure 3.1: Research methodology flow diagram.

3.3 SIMULATION PROCEDURE

A new PN correction technique was designed where the system instability of higher order ($4^{th} - order$) ΣΔ modulator was improved through a new architecture that makes it possible for the poles and zeros to be located within a unit circle to realize system stability. LMS algorithm was also modified to stabilize the input sequence within the frequency of interest. Mathematical expressions for the new model were formulated where all poles and zeros that were used to stabilize the systems were determined.

The proposed method was simulated in Matlab and Agilent Advance Design System (ADS) [42]. ADS was chosen because of its component behavioral modeling capability, which makes it easier to mimic the real lab environment. A co-simulation approach was followed that allows numeric processing of sub-circuits within the main circuit. The parameters of the sub-circuits (FNPLL, Formulator, ΣΔ modulators, etc) were designed as will be discussed below.

3.3.1 Frequency Range

The frequency range specifies the frequency band needed for various applications. In this case a 2.4 GHz FNPLL frequency synthesizer with the reference frequency of 50 MHz and bandwidth of 200 kHz was implemented.

3.3.2 Frequency Divider

A divider is normally a pulse counter that can count to different values before it resets itself. In this case the frequency divider, N, was determined as follows;

$$N_{max} = \frac{F_{Out}max}{F_{Step}} = \frac{3.5MHz}{200KHz} = 17.5 \tag{3.1}$$

$$N_{min} = \frac{F_{Out}min}{F_{Step}} = \frac{1MHz}{200KHz} = 5. \tag{3.2}$$

The counter is made flexible to allow it to convert any input into binary number. The mean of the counter cab be calculated as follows;

$$N_{mean} = \sqrt{N_{min} * N_{max}} \tag{3.3}$$

$$= \sqrt{18 * 5} \tag{3.4}$$

$$= 9.49 \approx 9. \tag{3.5}$$

3.3.3 VCO

The VCO frequency is controlled varying the DC voltage across the varactor diode. The VCO is normally specified by its tuning gain Γ_v, which signifies the amount of frequency deviation in MHz. The specified frequency deviation resulted from a 1-volt change in control voltage, which is normally expressed in Megahertz per volt(MHz/V). Since the noise level on the VCO control line is determined by active devices, a lower Γ_v will result in lower phase noise. This implies that by selecting the Γ_v parameter one can reduce the phase noise of the loop. If the operating range of the VCO is assumed to be between 1MHz and 3.5MHz, with control voltages between 1 and 2.5 v, voltage gain can be determined as follows

$$\Gamma_v = \frac{3.5MHz - 1MHz}{2.5 - 1} V * 2\pi$$
$$= \frac{10.47 * 10^6}{s}.$$

where the denominator s is included to convert the frequency characteristic of the loop into phase.

3.3.4 Phase Frequency Detector

The PFD can be realized by making use of the simulink block diagram shown in Figure 3.2, which depicts a circuit that generates a voltage that is proportional to the difference between the Phase/Frequency and the input signals.

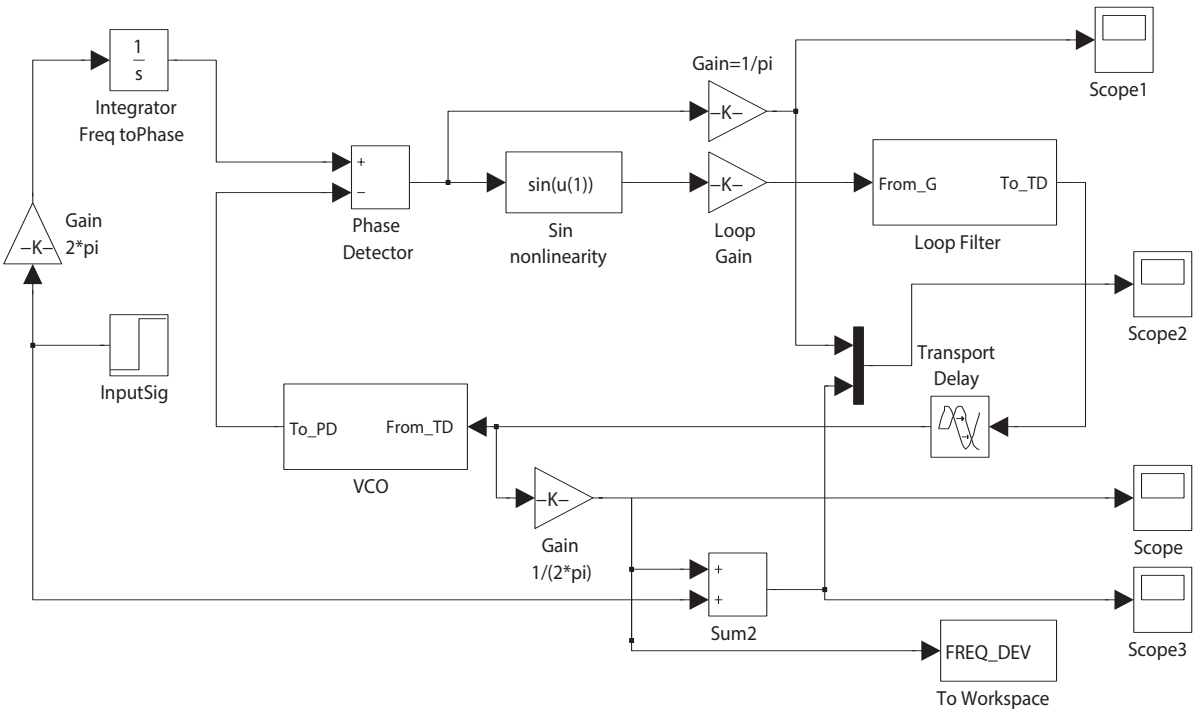

Figure 3.2: A phase frequency detector block diagram drawn in Matlab (simlink) package.

The Phase/Frequency detector gain is determined as follows;

$$\begin{aligned}\Gamma_{PD} &= \frac{V_1 - V_2}{4\pi} \\ &= \frac{2.5 - 1}{4\pi} \\ &= 0.119 v/rad.\end{aligned}$$

Assume the modulating signal of amplitude 1 at 25 kHz and a carrier signal amplitude of 1.1 at 1.5 kHz are applied to the PFD block diagram shown in Figure 3.2 with a cutoff frequency of 30 kHz and

an $8k\Omega$ resistor, the capacitor can be determined as follows;

$$\begin{aligned} C &= \frac{1}{2\pi R f_c} \\ &= \frac{1}{2\pi \times 8 \times 10^3 \times 30 \times 10^3} \\ &= 6.63 \times 10^{-10} F. \end{aligned} \tag{3.6}$$

Figure (3.3) shows the transfer characteristics of a LPF simulated at a cut-off frequency (30kHz).

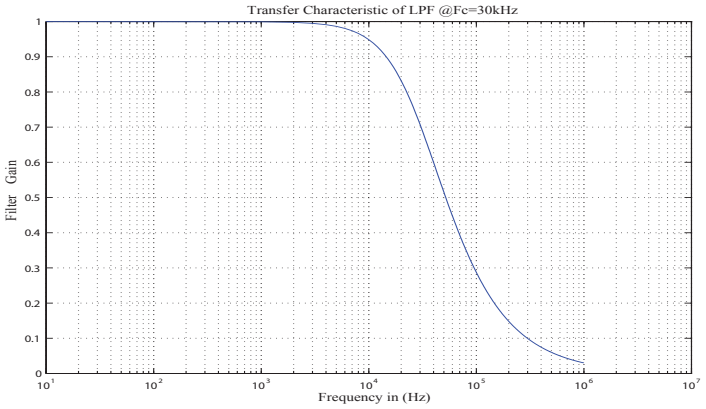

Figure 3.3: Transfer characteristic of a low pass filter.

Now if an active filter is considered where there gain of the amplifier is large, the filter gain Γ_f is determined from;

$$\Gamma_f = \frac{R_2 C + 1}{R_1 C}. \tag{3.7}$$

To account for the fact that most of the circuitry are finite, correction factor is applied to (3.7) such that

$$\Gamma_{fc} = \Gamma_f \Gamma_c \tag{3.8}$$

$$= \Gamma_p \times \left[\frac{R_2 C + R1}{R_1 C}\right]. \tag{3.9}$$

The total loop transfer function can now be modified in terms of the loop gains as

$$G(s)H(s) = \Gamma_{PD}\Gamma_{fc}\Gamma_{VCO}\Gamma_n \tag{3.10}$$

$$= \Gamma_{PD} * 0.5 * \left[\frac{R_2C + R1}{R_1C}\right] * \frac{\Gamma_{VCO}}{s}\frac{1}{N}. \tag{3.11}$$

Application of the second order characteristic equation into (3.11) yields

$$C.E = 1 + G(s)H(s) \tag{3.12}$$

$$= s^2 + \frac{0.5\Gamma_{PD}\Gamma_{VCO}R_2}{R_1N} * s + \frac{0.5\Gamma_{PD}\Gamma_{VCO}}{R_1CN} \tag{3.13}$$

$$= s^2 + 2\zeta\omega_n s + \omega_n^2. \tag{3.14}$$

where

$$\omega_n^2 = \frac{0.5\Gamma_{PD}\Gamma_{VCO}}{R_1CN} \tag{3.15}$$

$$2\zeta\omega_n = \frac{0.5\Gamma_{PD}\Gamma_{VCO}R_2}{R_1N}. \tag{3.16}$$

The damping factor and natural frequency of the loop needs to be defined upfront by making use of the denominator of the transfer function $s^2 + 2\zeta\omega_n s + \omega_n^2$ which can be written as

$$Den = \frac{s^2}{\omega_n^2} + 2\frac{\zeta}{\omega_n}s + 1. \tag{3.17}$$

If the loop gain Equation (2.103) discussed in Chapter 2 is applied into Equation (3.17), the following important expression is obtained;

$$Den = s^2 + \omega_1 s + \Gamma_{tot}\omega_1. \tag{3.18}$$

Now the damping factor and angular frequency parameters can be determined from;

$$\omega_n = \sqrt{\Gamma_{tot}\omega_1} \tag{3.19}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{\Gamma_{tot}}}. \tag{3.20}$$

These parameters ω_n and ζ are significantly used in simulating and controlling the frequency and transient responses of the PLL system. As observed from (3.20), when the total loop gain is increased, Γ_{tot}, the damping factor ζ is reduced, which affects the stability of the settling time. Hence it is

desirable to have a better transfer function and optimum parameters to design a proper PLL system that will track phase errors.

To achieve a damping factor $\zeta = 0.707$ that will allow a loop to overshoot by no more than 20 percent, a step response that settles within 5 percent at minimal time of 1 ms is required such that $\omega_n t = 3.5$.

The natural frequency parameter can therefore be obtained as;

$$\begin{aligned} \omega_n t &= 3.5 \\ \omega_n &= \frac{3.5}{0.001} \\ &= 3.5 * 10^3 rad/s. \end{aligned}$$

The loop filter for an active filter can be modeled as;

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}. \tag{3.21}$$

where

$$\tau_1 = R_1 C.$$

$$\tau_2 = R_2 C.$$

Now, with N_{max} and $\tau_1 + \tau_2$ can be determined from the maximum shoot expression as;

$$\begin{aligned} (\tau_1 + \tau_2) &= \frac{\Gamma_{VCO}\Gamma_{PD}/N_{max}}{\omega_n^2} \qquad (3.22) \\ &= \frac{10.47 * 10^6 * 0.119/18}{(3.5 * 10^3)^2} \\ &= 5.65 * 10^{-3} \\ \tau_2 &= \frac{2\omega_n \zeta(\tau_1 + \tau_2) - 1}{\Gamma_{VCO}\Gamma_{PD} 1/N} \qquad (3.23) \\ &= \frac{2 * 3.5 * 10^3 * 5.65^{-3} - 1}{10.47 * 10^6 * 0.119 * 1/9} \\ &= 2.785 * 10^{-4}. \end{aligned}$$

Now the value the capacitor is normally chosen to achieve optimum noise immunity of the loop.

Assume $C = 590 * 10^{-9}$, then;

$$R_2 = \frac{2\omega_n \zeta(\tau_1 + \tau_2) - 1}{\Gamma_{VCO}\Gamma_{PD}(1/N) * C2} \tag{3.24}$$

$$= \frac{2 * 3.5 * 10^3 * 0.707 * 5.65 * 10^{-3} - 1}{10.47 * 10^6 * (0.119/9) * 590 * 10^{-9}}$$

$$R_2 = 330\Omega \tag{3.25}$$

$$R_1 = \frac{\tau_1 + \tau_2}{C} - R2 \tag{3.26}$$

$$= \frac{5.65 * 10^{-3}}{490 * 10^{-9}} - 330 \tag{3.27}$$

$$= 9.25k\Omega. \tag{3.28}$$

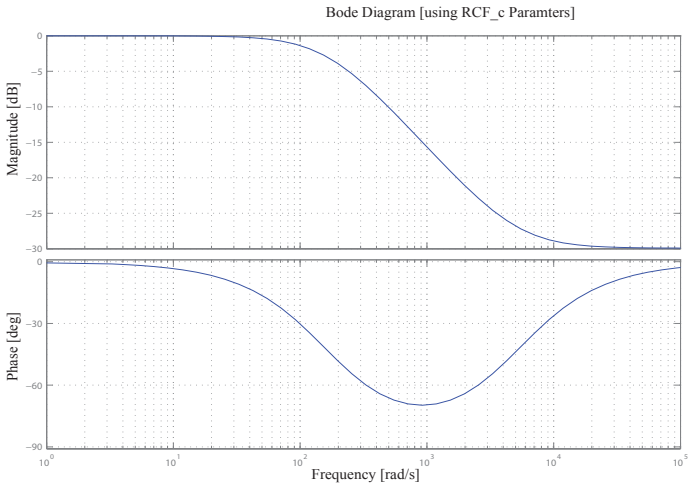

Figure 3.4: Bode Plot of a second a transfer function.

Figure 3.4 shows the simulated Phase noise PSD of the PLL system. The simulation results indicate that most of the phase noise in the PLL system come from the VCO block followed by the PFD block. The high phase noise on the VCO block are attributed to the high VCO gain, Γ_{vco} parameter.

Table 3.1: Design Parameters.

Design Parameters		
Parameters	Formula	Calculated values/Specifications
Output Frequency	LTE Frequency band	2.4 GHz
Bandwidth	Frequency spacing	200 kHz
N	Frequency Divider or Counter)	18
ω_n	(3.21)	3500 rad/sec
Γ_m	based on Peak to peak Voltage	$1Vpp$
Γ_{vco}	$\frac{\Delta f}{\Delta v}$	$10.47 * 10^6 rad/sec/v$
Γ_{PD}	$\frac{\Delta V}{4\pi}$	$0.199v/rad$
R_1	(3.28)	$10k\Omega$
R_1	(3.28)	330Ω
C	(3.28)	$590 * 10^{-9}\Omega$

The rest of design parameters and PLL specifications are shown in Table (3.1).

Table (3.1) depicts the design parameters that were used when simulating the proposed system. Table (3.1) also depicts the formulas that were used to determine the values of the components (resistors and capacitors), which achieved optimum noise immunity in the loop.

3.4 CONCLUSION

This chapter presented the detailed research methodology that was followed in this research study where the simulation procedure was discussed in detail. The procedure followed is the co-simulation approach that allows numeric processing of the sub-circuits within the main circuit. This chapter presented the design parameters that were used in the simulation of the proposed system.

CHAPTER 4 DESCRIPTION OF PROPOSED TECHNIQUE

4.1 CHAPTER OVERVIEW

This chapter presents the circuit designs and schematic layouts that were used to implement the new PN correction technique in Agilent ADS and Matlab simulation tools. The chapter begins by presenting the LMS adaptive filtering process that controls the high gain introduced by the DAC. Then the mathematical expressions that are used to resolve short periodic cycle problems are presented. A modified Fourth-Order cascade resonator feedback (CRFB) 1-bit ΣΔ modulator is discussed. Finally, the chapter discusses the method of controlling the stability of the modified architecture.

4.2 DESIGN AND SYSTEM DESCRIPTION

Adaptive filtering as a means of improving system stability and suppressing spurious tones in ΣΔ modulator was discussed in [77] and further enhanced in [64] where a digital correction network term was added to the wideband cascade delta sigma modulator. This correction network (CN) is given by;

$$CN = -az^{-1} + z^{-M}. \tag{4.1}$$

The purpose of the correction network is to remove non-linearities and improve the signal to noise ration (SNR) through the suppression of harmonics within the in-band signal. From this advancement, a modified FNPLL frequency synthesizer with an adaptive filtering added after the ΣΔ modulator is proposed.

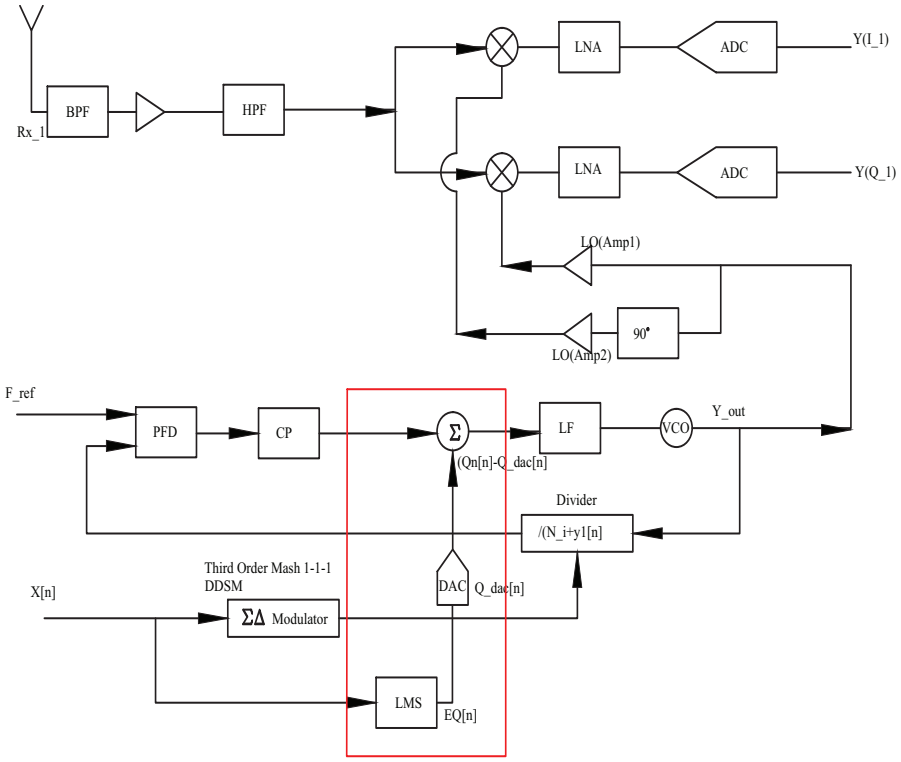

Figure 4.1: Proposed FPLL FS ΣΔ modulator and adaptive filtering module.

As shown in Figure 4.1, the adaptive filter is connected to the digital to analog converter (DAC), charge-pump (CP) and then filtered by the loop filter. Thereafter the output is passed through the voltage controlled oscillator and the phase frequency detector (PFD). The ΣΔ modulator is used to move the high frequencies outside the in-band [78]. A least mean square algorithm (LMS) is included to control the high gain introduced by the DAC.

4.3 RESOLVING SHORT-PERIODIC CYCLE PROBLEM

One of the main problems of the FNPLL frequency synthesizers that are based on ΣΔ modulators is that they have short periodic cycles that are the main sources of harmonics and spurs within the in-band. Dithering has been applied for sometime as a stochastic process that randomizes and disrupts the short periodic cycles [79]. A fundamental problem with the deterministic approach is that they seek to minimize short periodic cycles by setting the initial conditions of the internal registers, which happens to work perfectly when there is no mismatch at different stages (otherwise there might be excessive noise leakages).

4.3.1 Proposed method to resolve short periodic cycles

Adaptive filtering is implemented to allow zeros and poles of the NTF to be placed anywhere within the unit circle to make a noise components flat within the in-band [80]. Adaptive filtering allows mean square criteria statistical performance measures to be used as they allow coefficients of the NTF to be measured as a quadratic performance index. Figure 4.2 shows coefficients of the adaptive filter that is implemented to control the gain caused by the ΣΔ modulators.

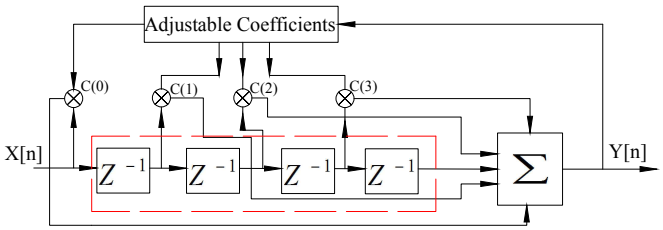

Figure 4.2: Coefficients of Adaptive filtering.

Let the input sequence $x(n)$ represent the short periodic cycle. Its output sequence is modeled by;

$$y(n) = \sum_{l=0}^{M-l} C(l)x(n-l), \quad n = 0, \cdots, N. \tag{4.2}$$

In this case the adjustable coefficients are $(C(l), \quad 0 \leq l < M-1)$, an adaptive algorithm can be used

to estimate the errored sequence $(r_s(n))$ as follows;

$$e(n) = r_s(n) - y_{out}(n), \quad n = 0, \cdots, N. \tag{4.3}$$

Assume that the input sequence, $x_s(n)$, and the required sequence, $r_s(n)$, are uncorrelated, then the white power spectrum of $r_s(n)$ can be added directly to $x_s(n)$ and the coefficients of the filter can be used to minimize the sum of the square errors, $(\sum e^2)$;

$$\begin{aligned}
\sum e^2 &= \sum_{n=0}^{N} e^2(n) \\
\sum e^2 &= \sum_{n=0}^{N} r_s(n) - \sum_{n=0}^{M-1} C(l)x(n-l) \\
\sum e^2 &= \sum_{n=0}^{N} r_s^2(n) - 2\sum_{n=0}^{M-1} C(l)\rho_{xy}(l) \\
&\quad + \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} C(l)C(j)\rho_{xx}(i-j).
\end{aligned} \tag{4.4}$$

The terms ρ_{xy} and ρ_{xx} represent the cross-correlation and auto-correlation between the required and the short-period input sequence respectively. This relationship is expressed by;

$$\begin{aligned}
\rho_{xy}(j) &= \sum_{n=0}^{N} r_s(n)x(n-j); \quad 0 \le j < N-1. \\
\rho_{xx}(j) &= \sum_{n=0}^{N} x(n)x(n+j); \quad 0 \le j < N-1.
\end{aligned} \tag{4.5}$$

The reason why the LMS algorithm is chosen here is that it is easy to perform a simple computation of the ρ_{xy} and ρ_{xx} terms by making use of the recursive steepest descent given in Equation (4.4), where the set of optimum filter coefficients that can be used to correct step sizes are generated as follows;

$$C_n(j) = C_{n-1}(j) + \mu.e(n).x(n-j); \quad 0 \le j < N-1. \tag{4.6}$$

The terms μ and the $(n-j)$ in Equation (4.6) represent the stepsize and the sample of the input sequence at the j^{th} filter tap respectively. One can minimize the sum of square errors through this

approach, which essentially reduces the short periodic cycles of the input sequence as required. The stepsize parameter, μ, is also used to control the rate of signal convergence, which is critical in determine the portion of the high frequencies that need to be cut off from the in-band. A quick simulation study was conducted where several mean square error (MSE) parameters as depicted in Table (4.1) were used to estimate the number of iterations at which the steady state is reached.

Table 4.1: MSE Estimation based on number of iterations.

MSE Estimation		
Parameters	Symbol	values
Step Size	μ	0.05
Filter Order	N	10
Filter length	L	150
No. Of Iterations	i	1000

An interesting trend was observed where the convergence rate tends to be slow at small step size values. Several simulations were run to establish the best case scenario where it was found that the LMS algorithm settles at about a step size of 0.005.

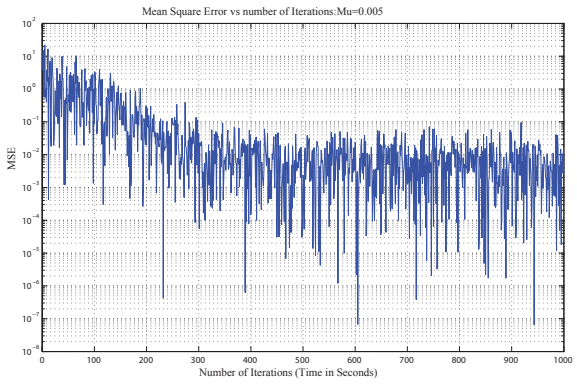

Figure 4.3: MSE Estimation in dB vs no. of Iterations $(\mu = .005)$.

As observed in Figure (4.3), the LMS algorithm achieves the steady state-error after several iterations, indicating long convergence rate. Although the convergence rate is long, it does not really matter in this case as the area of concern is signal stability within the in-band.

4.3.2 Maintaining stability of the input data within the in-band

The long convergence rate of the LMS algorithms that causes instability within the frequency of interest can be resolved by treating the input data sequence as eigenvalues where LMS can achieve the optimum convergence rate when the autocorrelation term (ρ_{xx}) is taken as the eigenvalue spread with the minimum value of 1 [6, 81]. This allows the input sequence to be transformed to white spectrum ($x(n) \rightarrow w(n)$) by means of the $N \times N$ orthogonal transform T, ($\rho_{ww} = \mathbf{T}\rho_{xx}\mathbf{T}^T$) which produces a new form of ρ_{ww} ;

$$\rho_{ww} = \begin{pmatrix} \sigma_1 & 0 & \cdots & 0 \\ 0 & \sigma_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & \sigma_{N-1} & \cdots & 0 \\ 0 & \cdots & 0 & \sigma_N^2 \end{pmatrix} \tag{4.7}$$

It is required to have eigenvalues modified to have a resultant matrix having identical eigenvalues as follows;

$$\rho_{ww}(modified) = \begin{pmatrix} \sigma^2 & 0 & \cdots & 0 \\ 0 & \sigma^2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & \sigma^2 & \cdots & 0 \\ 0 & \cdots & 0 & \sigma^2 \end{pmatrix} \tag{4.8}$$

The remaining task is to model the whitened and transformed input sequences as follows;

$$\begin{aligned} \mathbf{W}(n) &= \mathbf{T}.\mathbf{X}(n). \\ \mathbf{X}(n) &= [x(n)x(n-1)\cdots,x(n-N+2)x(n-N+1)]^T. \\ \mathbf{W}(n) &= [w_1(n)w_2(n)\cdots w_{N-1}(n)]^T. \end{aligned} \tag{4.9}$$

The new algorithm for the proposed architecture can be formulated by making use of the whitened input sequence ($\mathbf{W}(n)$) and transformed input sequence $\mathbf{X}(n)$ as follows;

$$\mathbf{C}(n+1) = C(n) + 2\sigma e(n)\Delta^2 W(n). \tag{4.10}$$

where

$$\Delta^2 = \begin{pmatrix} \frac{1}{\sigma^2} & 0 & \cdots & 0 \\ 0 & \sigma^2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & \frac{1}{\sigma^2} & \cdots & 0 \\ 0 & \cdots & 0 & \frac{1}{\sigma_N^2} \end{pmatrix} \tag{4.11}$$

A new output sequence can be expressed in terms of the whitened data and transformed input sequences as follows;

$$\begin{aligned} \mathbf{y(n)} &= C(n).W(n) \\ &= W^T(n).T.X(n). \end{aligned} \tag{4.12}$$

The input data sequence $\mathbf{X}(n)$ has now taken a new form with minimal periodic cycles that does not allow power to be distributed amongst spurious tones at the output of the $\Sigma\Delta$ modulator. This now allows for the cycle lengths to be maximized to guarantee the minimum power distribution within the frequency of interest by making use of the following modulo operator: $([(\alpha \bmod M)+\beta) \bmod M = (\alpha+(\beta \bmod M) \bmod M = (\alpha+\beta) \bmod M])$

The error function can then be expressed as follows;

$$\begin{aligned} \hat{e}(n) &= (\hat{(}x)+\hat{(}n-1)+\cdots\hat{x}(0)+\hat{C}(n)) \bmod M \\ &= (\hat{C}(0)+\sum_{j=0}^{n}\hat{x}(j)). \end{aligned} \tag{4.13}$$

The initial conditions, $C(0)$, can be set by assuming that the input sequence is at DC level, such that $(\hat{e}(n) = (\hat{C}(0)+(n+1)\hat{x}) \bmod M), \forall n \geq 0$.

Assume the signal error has a fundamental period, T_1, then the error signal takes the following new form;

$$\begin{aligned} \hat{e}(n) &= e[n+T] \\ &= [\hat{C}(0)+(n+T_1+1)\hat{x}] \bmod M \\ &= [\hat{C}(0)+(n+1)x+T_1\hat{x}] \bmod M. \end{aligned} \tag{4.14}$$

Now the most important term is the $T_1\hat{x}$, which is an integer multiple of M such that $(T_1\hat{x} \bmod M = 0)$ [79]. This implies that for an even M, the maximum cycle length $(N = M = 2^{\hat{x}})$ is realized when the input sequence assumes an odd number.

4.3.3 Application of higher order ΣΔ modulator and LMS to filter noise

After maximizing cycle lengths, it is required to shape the resulting quantization noise by making use of the ΣΔ modulator, which shifts the portion of the noise from the in-band to higher frequencies. Higher order modulator topologies (say $M \geq 4$), have the capability to achieved the required signal to quantization noise ratio (SQNR) and the oversampling ratio (OSR) [31]. The OSR plays an important role in that it becomes very difficult to achieve required SQNR at low OSR irrespective of the order of the loop filter. The concept of using digital cancellation of noise by cascading ΣΔ modulators was introduced in [76] as depicted in Figure 4.4, where the two outputs ($v1$ and $v2$) are combined to obtain the output signal.

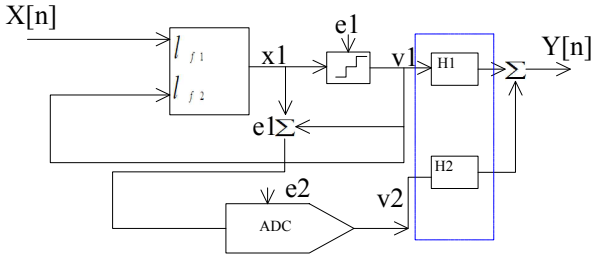

Figure 4.4: Multistage (Cascade) ΣΔ modulator.

It can be observed from Figure 4.4 that the second quantization noise is introduced in the process of extracting the error signal $((e_1 = v1 - y1)$ and after converting e_1 from analog to digital by a single bit ADC. The multiStage noise shaping (MASH) technique combines several integrators that allows the cancellation of quantization noise in each stage through the digital paths (H_1 and H_2). This process can introduce a latency on the second stage that can be matched by $H_1(z) = z^{-k}$.

The main challenge with this approach is that the second stage quantization noise must have low noise distortion to process the input sequence **X[n]** successfully. As confirmed in [82],the problem with MASH configuration is that it requires all stages and components to be properly match in order to cancel the noise errors of the previous stages as any mismatch leads to noise leakages of the first stage to the second stage. The MASH architecture given in Figure 4.4 have the noise and signal

transfer functions given by

$$NTF(z) = \frac{1}{1 - l_{f1}(z)}. \tag{4.15}$$

$$STF(z) = \frac{l_{f2}(z)}{1 - l_{f1}(z)}. \tag{4.16}$$

The NTF and STF may be expressed in terms of the loop transfer functions (LF)as follows;

$$l_{f1}(z) = \frac{STF(z)}{NTF(z)}. \tag{4.17}$$

$$l_{f2}(z) = 1 - \frac{1}{NTF(z)}. \tag{4.18}$$

From loop transfer functions (LTF) expressions it can be observed that by making NTF significantly low in the signal band results in larger values $l_{f2}(z)$ with a low-pass response. From the $l_{f1}(z)$ expression it can be observed that the only way to make STF close to unity is to make $l_{f1}(z)$ take on larger values in the signal band. This implies that to other maintain system stability, the poles of $l_{f2}(z)$ and $l_{f1}(z)$ must be closely packed to each [83] within the following signal range: $(f_0(=0)tof_B(=\frac{f_s}{2.OSR}))$, where the in-band noise can be determined from the following expression (if OSR is greater than 1);

$$\sigma_n^2 = \frac{\sigma_q^2 \pi^{2l}}{(2l+1)OSR^{2L+1}}. \tag{4.19}$$

The transformed output of the higher order architectures is given by;

$$Y(z) = H_x(z)X(z) + H_E(z)E(z). \tag{4.20}$$

In Equation (4.20), $H_x(z)$ and $H_E(z)$ represent the transfer functions and are given by;

$$H_x(z) = \frac{\sum_{i=0}^{M} a_i(z-1)^{M-i}}{z[(z-1)^M - \sum_{i=1}^{M} b_i(z-1)^{M-i}] + c_i}. \tag{4.21}$$

$$H_E(z) = \frac{(z-1)^M - \sum_{i=0}^{M} b_i(z-1)^{M-i}}{z[(z-1)^M - \sum_{i=1}^{M} b_i(z-1)^{M-i}] + d_i}. \tag{4.22}$$

where

$$c_i = \sum_{i=0}^{M} a_i(z-1)^{M-i}.$$

$$D_i = \sum_{i=0}^{M} b_i(z-1)^{M-i}. \tag{4.23}$$

Assume (n,m) are the number of integrators and local oscillators respectively, then the noise transfer function (NTF) of a higher order ΣΔ architecture is modeled by using the Meison rule [84] as follows;

$$NTF = \frac{\prod^{M}((z-1)^2+k_j)}{\prod^{M}((z-1)^2+k_j)+\sum_{i=1,j=1}^{n,m}(z-1)^{j-1}} \times \frac{1}{(a_{2j-1}(z-1)+a_j)\prod^{M}((z-1)^2+k_l)}. \tag{4.24}$$

Higher ΣΔ modulators cancel noise at the expense of system instability. The instability problems can be corrected by introducing poles at the NTF [84], which can be computed in the s-domain and then converted to the z-domain by using bilinear transforms. From the STF ($STF = z^{-M}$) of the multistage system it can be seen that there are some delays of M sampling periods, which cause some errors and unnecessary harmonic components on the input signal.

4.4 MODIFIED FOURTH-ORDER CASCADE OF RESONATORS WITH FEEDBACK

Figure 4.5 depicts a fourth order CRFB with feedback and the coupling coefficients where multiple signals are summed by the active adder. The drawback with this configuration is that the incoming multiple signals that are added at the same time introduces additional and long processing times, which normally leads to the disorientation and displacement of poles location [85]. Furthermore, concentrating multiple signals at the same active adder introduces an additional phase component that reduces the processing time for the DAC linearization.

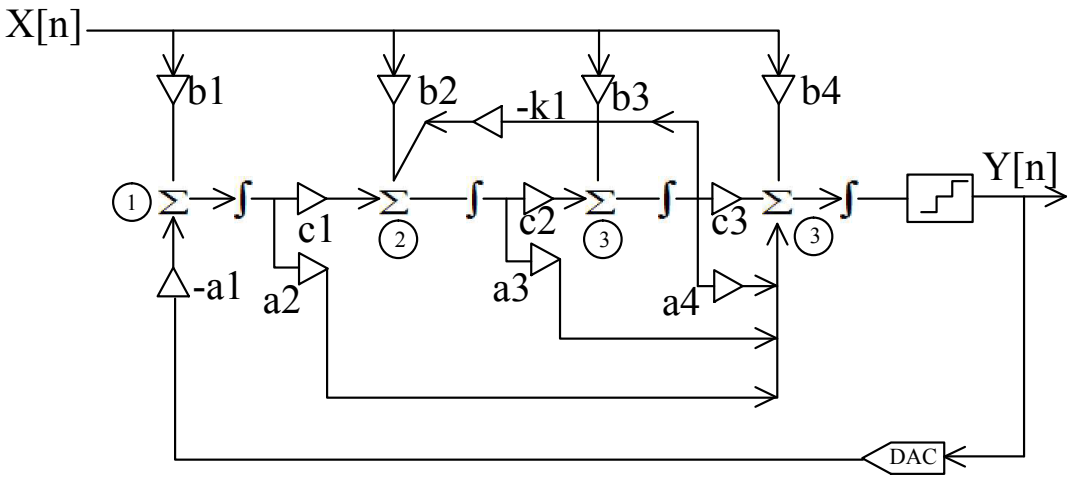

Figure 4.5: Fourth-Order CRFB 1-bit ΣΔ modulator.

The challenges associated with summing multiple signals entering the same adder can be resolved by separating the input signals into different adders as shown in Figure 4.6.

Now the zeros of the loop transfer function, l_{f1}, are given by the feedback coefficients, $a_i's$ that generate the poles of the NTF and STF [86]. The zeros of the l_{f2} and the STF are determined from the feed-in coefficients. System stability can be realized by computing and locating the complex poles and zeros within the unit circle. A resonator with two complex poles can be realized from the feedback path $(-k1)$ and the first two integrators leading to poles and zeros located within the unit

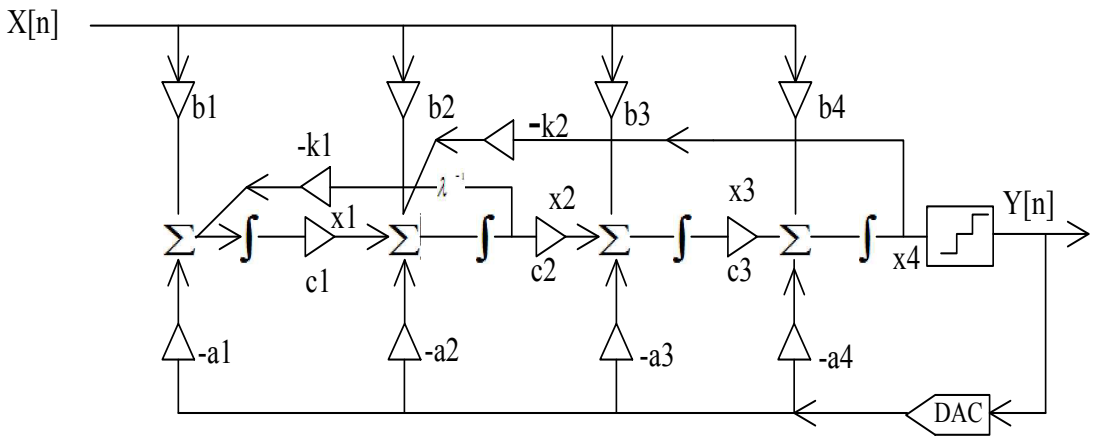

Figure 4.6: Modified 4^{th}-order with both NTF coefficients (feedforward, feedback and the coupling coefficients).

circle defined by $(z^2-(z-k_1)z+1)$.

The poles and zeros of the NTF that will bring the required stability (i.e., required SNR), which is required to be significantly higher within the in-band are determined from the following equation;

$$NTF(z)=\frac{\prod_{i=0}^{m}(z-1)^2}{\prod_{i=0}^{m}(z-1)^2+k_j+\sum_{i=1}^{n,m}[(z-1)^{j-i}+(a_{2j}-1(z-1)+a_i)\times\prod_{i=0}^{m}(z-1)^2+k_l]}. \quad (4.25)$$

The angular frequencies of poles that are located with the unit circle can be determined from

$$\cos\omega_1 = 1-k1/2. \quad (4.26)$$

$$\cos\omega_2 = 1-k2/2. \quad (4.27)$$

The processing speed of the proposed architecture was enhanced by introducing a sample delay in one of the feedback loops, while the feedback path left without any delay feedback. The mismatch between the integrating capacitors and the sampling delay that normally causes high gain errors can be resolved by passing the output of the feedforward path through the digital filter $H_{R1}(z)$ and the feedback path through $H_{R2}(z)$ respectively. The output of the two digital filters (shown in Figure 4.4)

are then combined to generate the output signal $Y[n]$. $H_{R1}(z) = z^{-k}$ with high SNQR values. The poles and zeros of the modified architecture are modeled as follows:

$$\begin{aligned} H_{R1}(z) &= \frac{x_1(z)}{y(z)}|_{X(z)=0} \\ &= \frac{-a_1 z + a_2(z-1)}{z^2 - (2-k_1)z + 1}. \end{aligned} \tag{4.28}$$

$$\begin{aligned} H_{R2}(z) &= \frac{x_1 4z)}{y(z)}|_{X(z)=0} \\ &= \frac{z}{z^2 - (2-k_2)z + 1} \\ &= H_{R1}(z)[\frac{z}{z^2 - (2-k_2)z + 1}]. \end{aligned} \tag{4.29}$$

4.5 CONTROLLING THE STABILITY OF THE MODIFIED ARCHITECTURE

The weights of the adaptive filters were modeled and determined through simulations to find optimal values that resulted in minimized gain caused by the DAC. Another major challenge with the VCO PLL (specifically for LTE) is that the strict and stringent requirement for the design of loop filter parameters that will results in required control sensitivity [87]. It was for this reason that the adaptive filters and feedback paths for the proposed model were modeled as follows to realize the required control sensitivity level;

$$x_4(z) = W(z)[c(z) - Y(z)]. \tag{4.30}$$

where

$$c(z) = \frac{c_1 c_2 c_3 c_4}{N(z)}. \tag{4.31}$$

$$W(z) = \frac{N(z)}{(z-1)^4}. \tag{4.32}$$

$$N(z) = (z-1)^3 + a_2 c_1 (z-1)^2 + a_4 c_1 c_2 c_3. \tag{4.33}$$

The proposed architecture's coefficients were determined as follows;
$(C_1 = 0.15, C_2 = 0.54, C_3 = 1.2, C_4 = 0.9)$.

These coefficients allowed the input data sequence to be modeled as the fourth-order auto-regressive process that satisfies the following equation;

$$x(n) = 0.15x(n-1) + 0.54x(n-2) + 1.2x(n-3) + 0.9x(n-0.9) + w(n). \tag{4.34}$$

For this to work, the white noise term, $w(n)$, must satisfy the following auto-correlation expression;

$$\rho_{ww} \in w(n)w(n+m). \tag{4.35}$$

$$\rho_{ww} = \begin{cases} \mu^2 & \text{if } m = 0 \\ 1 & \text{otherwise} \end{cases}$$

The maximum cycles for the input data sequence can be computed from the LMS algorithm as follows;

$$\begin{aligned} \hat{x}(n) &= \sum_{i=1}^{4} C_i x(n-i) \\ &= c_1(n)x(n-1) + c2x(n-2) + c3x(n-3) + c4x(n-4). \end{aligned}$$

$$\begin{aligned} C_1(n+1) &= c_1(n) - \frac{\mu}{2}\frac{\partial e^2(n)}{\partial c_1(n)} \\ &= c_1(n) - \frac{\mu}{2}\frac{\partial^2 e^2}{\partial e(n)} . \frac{\partial e(n)}{\partial c_1(n)} \\ &= c_1(n) + \mu e(n)x(n-1). \end{aligned} \tag{4.36}$$

Similarly

$$C_2(n+1) = c_2(n) + \mu e(n)x(n-2). \tag{4.37}$$

$$C_3(n+1) = c_3(n) + \mu e(n)x(n-3). \tag{4.38}$$

$$C_4(n+1) = c_4(n) + \mu e(n)x(n-4). \tag{4.39}$$

The actual coupling coefficient values of the proposed model will be computed on Matlab simulation tool. The coefficients will be computed in such a way that the final values should guarantee the stability and provide a modulator with high SNDR. The feedback loop coefficients play a critical role as they have a impact on the SNR.

4.6 CONCLUSION

This chapter discussed the system model of the proposed technique. The enhancement and improvements made on the existing Fourth-Order CRFB 1-bit ΣΔ modulator were discussed in detail. A modified CRFB 1-bit ΣΔ modulator where the short periodic cycle's problems have been resolved using the LMS adaptive filtering was demonstrated using mathematical expressions. The chapter also presented the method employed in resolving the additional long delay processing times that cause disorientation and pole dislocation. This method involves separating the input signal and applying different adders to improve the processing speed.

CHAPTER 5 RESULTS AND DISCUSSION

5.1 CHAPTER OVERVIEW

This chapter presents the implementation and simulation of the proposed architecture and mathematical formulas that were presented in section 4.1. The chapter begins by presenting the numerical calculations of parameters that were used in the simulation process. The system model presented in section 4.1 is implemented in ADS simulation tool where the proposed model is simulated using the behavioural model, which allows the system design parameters (such as reference frequency, offset frequency, gain, step size, etc.) to be set and configured. The fourth-Order CRFB 1-bit ΣΔ modulator was implemented via a set of accumulators. The adaptive LMS block was implemented in the FNPLL subcircuit.

5.2 IMPLEMENTATION OF THE PROPOSED ARCHITECTURE

The proposed architecture was implemented in a behavioral model that contains various (ΣΔ modulator, PFD, FD, CP, etc.), which simplify and reduce long simulation times. Figure 5.1 shows a high-level schematic representation of the FNPLL implemented in ADS. The Accumulator block represents the fourth-Order CRFB 1-bit ΣΔ modulator that was implemented via the set of accumulators available on the ADS component library. The implementation of the fractional-N PLL synthesizer will be discussed in detail in the proceeding section.

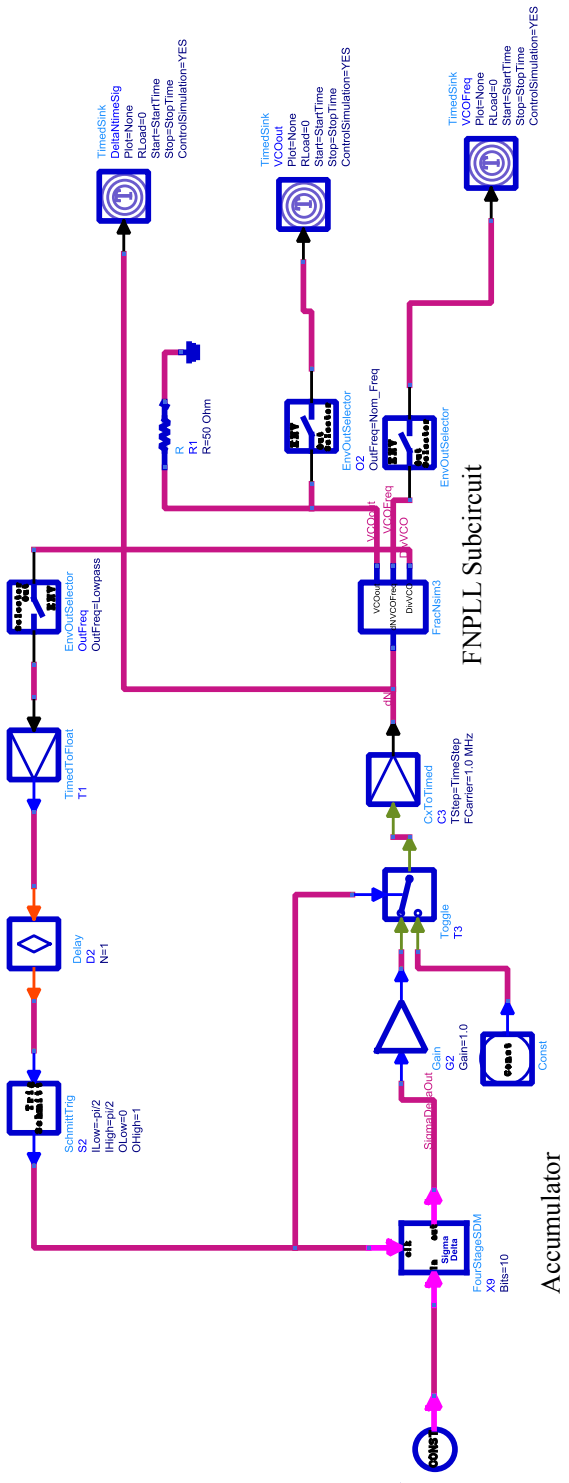

Figure 5.1: Implementation of the proposed architecture in ADS.

The behavioural model allows the ADS simulation tool to perform numeric processing of the PLL subcircuits and their associated equations [42].

5.2.1 Implementation and Simulation of $4^{th}order-\Sigma\Delta$ modulator with accumulators and differentiators

Figure 5.2 depicts a fourth-order stage ΣΔ modulator implemented via accumulators (with clock inputs and overflow outputs that could be either 0 or 1) and differentiators.

The differentiators are cascaded in such a way that the quantization noise of the first stage is fed into the input of the second stage and so forth.

Accumulators were employed to dynamically change the N divisor value when the PLL is at the locked state. As soon as there is an accumulator overflow, the carryout changes from low to high and the carryout forces the N divide by $N+1$ for any single reference cycle. For instance, if P is the value to be divided by $N+1$ in a full fractional cycle, C, is the size of the counter (or bit number) and V is the value that is added to at the end of the reference cycle, the average divide ratio will be $(N+\frac{V}{P})$. The presence of the phase noise error is detected by the absence of the non-zero values at the accumulator output. That is, if the average divide ratio is not zero, it implies that there is a phase error between the reference frequency at the VCO and the feedback signal. Furthermore, the phase noise will continue to increase until the accumulator overflows. This process generates spectral tones that cannot be filtered for any communication system that operates at a channel spacing between 10 and 200 kHz.

As shown in Figure 5.3, the phase of VCO remains constant at the beginning of the cycles. As soon as the division occurs, the phase changes at the rate of 360 degrees per $0.1\mu sec$ (10 MHz).

The implemented accumulators consist data registers, adders and bus rippers obtained from the ADS display library, which operate as follows: the first bus ripper's output is set at "1"to make sure that the output of the adder is greater than "1", i.e., if the output of the adder is greater than "1", the overflow will be "0". The second bus ripper is set to feed the fractional part of the adder. For instance, if the required fraction to be summed was $200 \div (2^{10}) = 0.1953125$, then after several additions (say 5 repeated additions), the output at the adder will be (6×0.1953125) 1.171875 with an overflow of "1" and 0.171875 will be fed-back as the input to the adder.

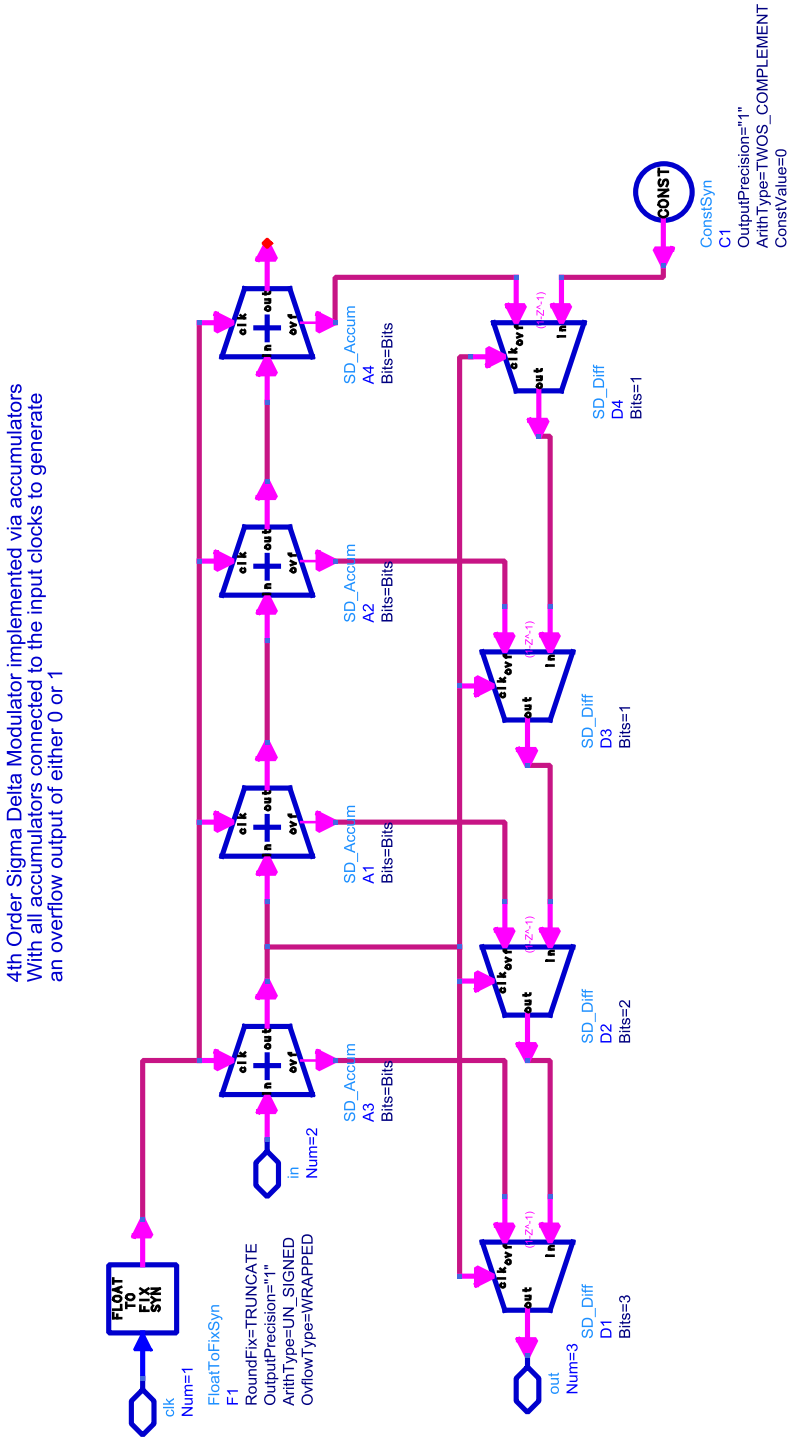

Figure 5.2: Implementation of 4^{th}-order $\Sigma\Delta$ modulator via accumulators.

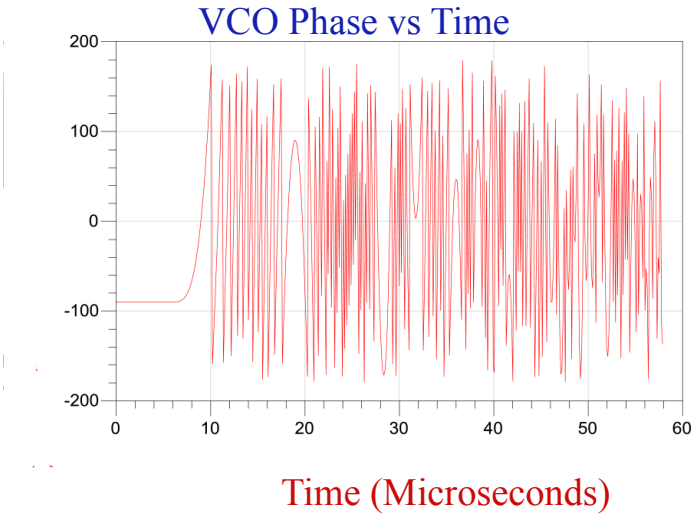

Figure 5.3: Phase noise fluctuation at the VCO.

Figure 5.4 shows the simulation result results of the accumulator divided output, which is a sawtooth waveform that represents the divided signal phase in radians.

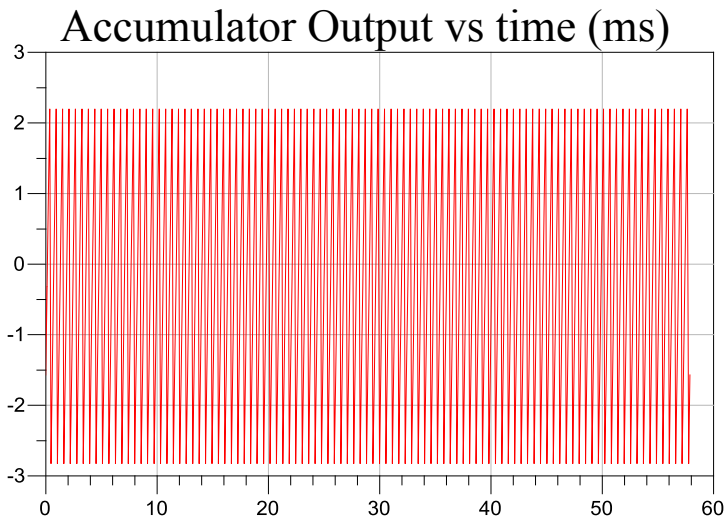

Figure 5.4: Simulated sawtooth waveform of the accumulator output.

The best way to obtain the divide ratio that has the quantization noise with high-pass shaped frequency that is not affected by the periodicity of a single accumulator is to use multiple accumulators and

differentiators' components denoted by SD_{Accumm} and SD_{Diff} respectively as depicted in figure 5.2. This results in the quantization noise at the fourth stage being randomized in such a way that it can be filtered by the term $(1-z^{-1})^4$.

As expected and shown in Figure 5.5, the simulated spectrum has a high-pass filter shape but still shows a lot of spectral tones and signal instability within the frequency of interest.

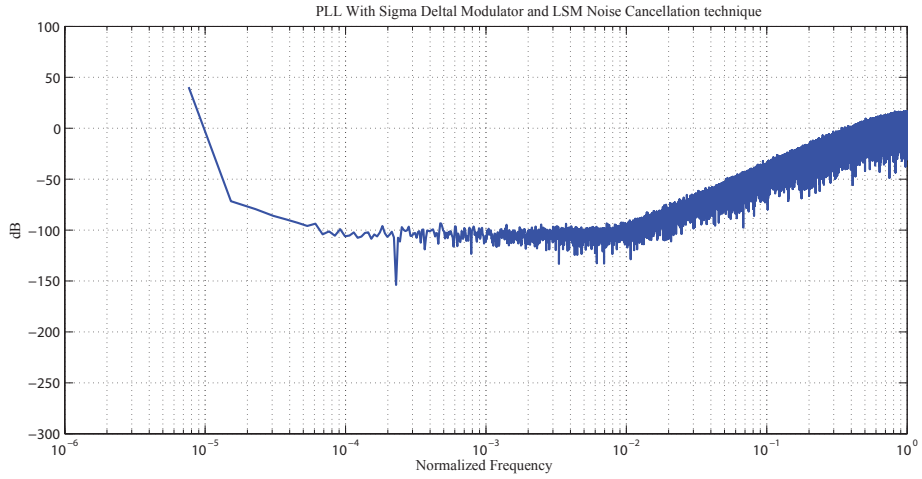

Figure 5.5: Simulated Output Spectrum of low order ΣΔ modulator.

It is desirable to have the shape of spectrum raising up at a normalized frequency (frequency of interest) of about 10^{-3} as it will make it easier to filter the rest of the unwanted noisy signal. This implies that the noise spectrum flattens within the required bandwidth. The requirement is to have the noise spectrum flattening out above the offset frequency. Figure 5.6 depicts the corresponding VCO noisy spectrum where the phase noise is clearly shown to be very high at about -80 dBc/Hz.

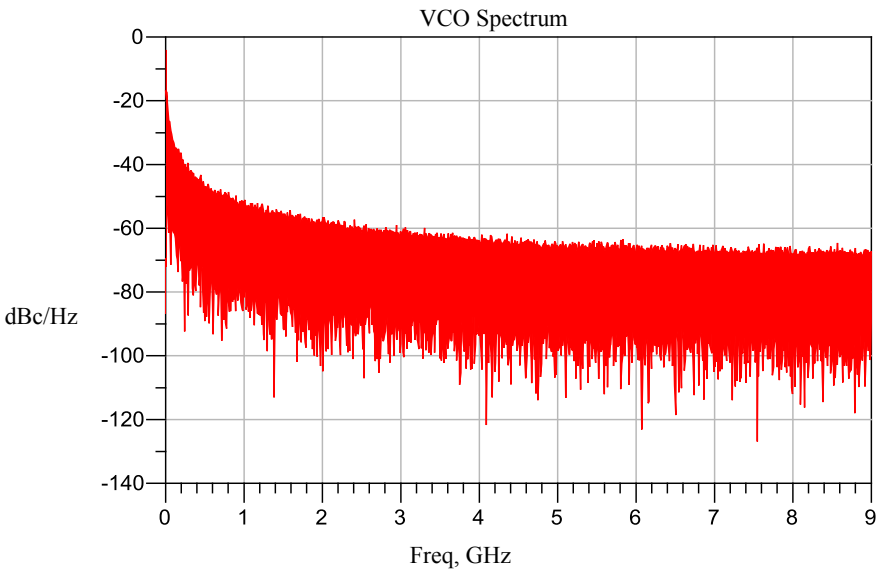

Figure 5.6: Simulated output spectrum of a VCO ΣΔ modulator.

5.2.2 FNPLL sub-circuit

Figure 5.7 depicts the behavioral model of the fractional-N PLL synthesizer that includes the following main components;

- Phase frequency detector (PFD).
- Charge pump (CP).
- Voltage controlled oscillator (VCO).
- Adaptive LMS filter.

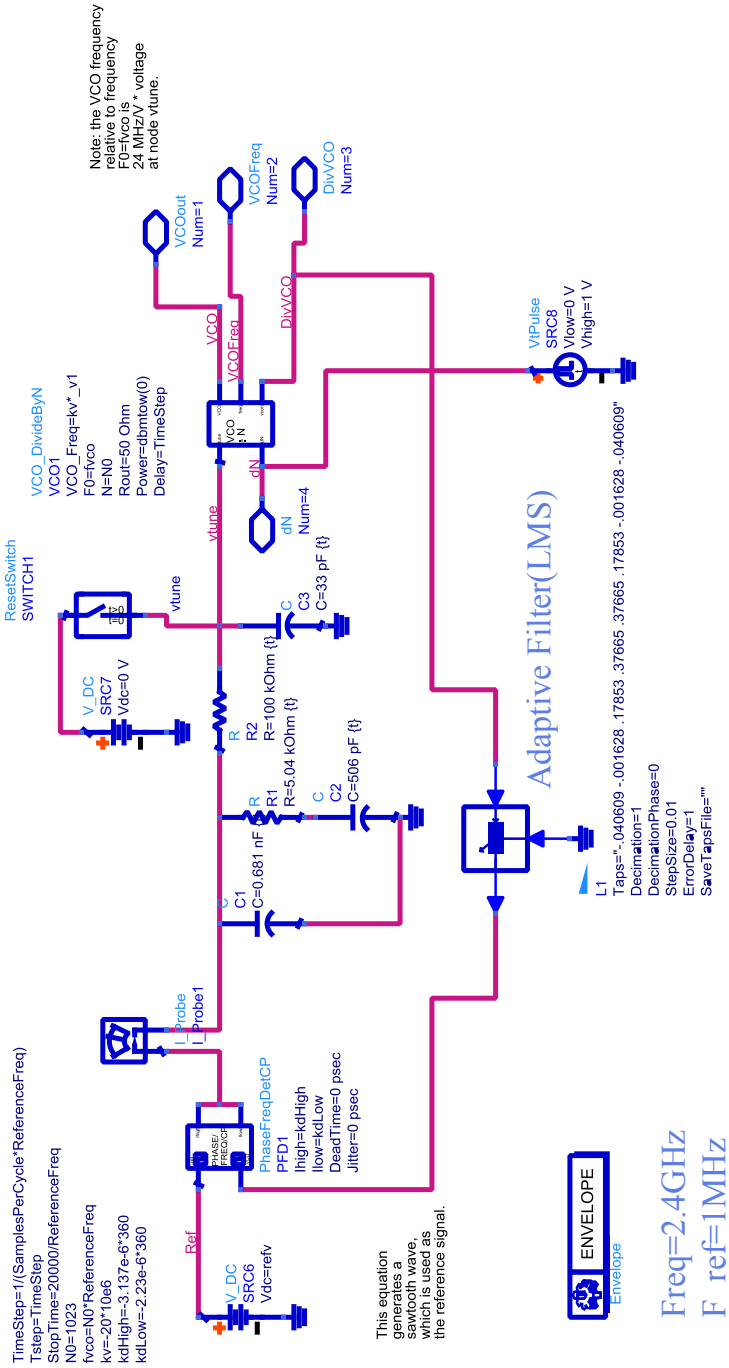

Figure 5.7: Implementation of FNPLL sub-circuit.

5.2.2.1 Adaptive LMS filter

The LMS component $(LMS_CxTkplotandLMS_Tkplot)$ available in the ADS display library was used to implement the adaptive filter that uses least mean square algorithm. The filter coefficients determined in section 4.5 are used to determine the size of the adaptive filter. The essence of implementing the adaptive filter was to minimize the mean square error of the input data sequence.

Figure 5.8 shows the simulated output signal of the modulator in time domain after the transformation of the input data sequence to a white spectrum using LMS adaptive filtering component.

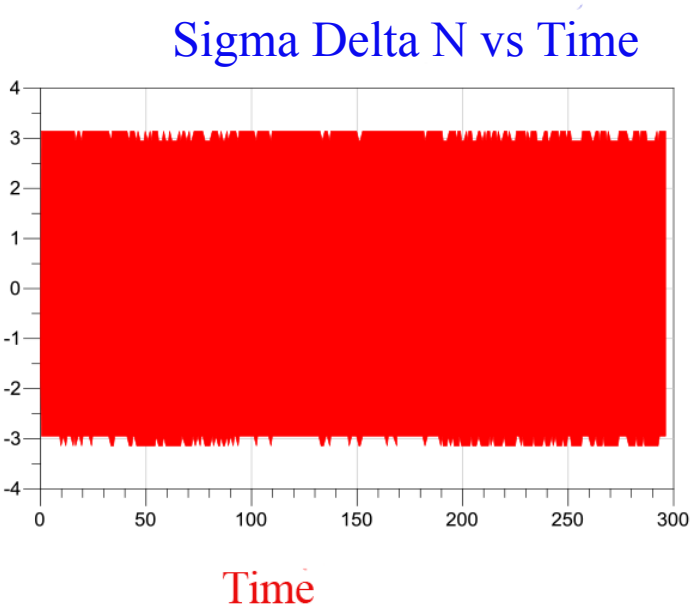

Figure 5.8: Sigma N modulator versus time (ΣΔ input signal).

The simulated output spectrum as shown in Figure 5.9 is a clean signal without any spurious tones within the in-band. The noisy contents of the signal are pushed outside the frequency of interest.

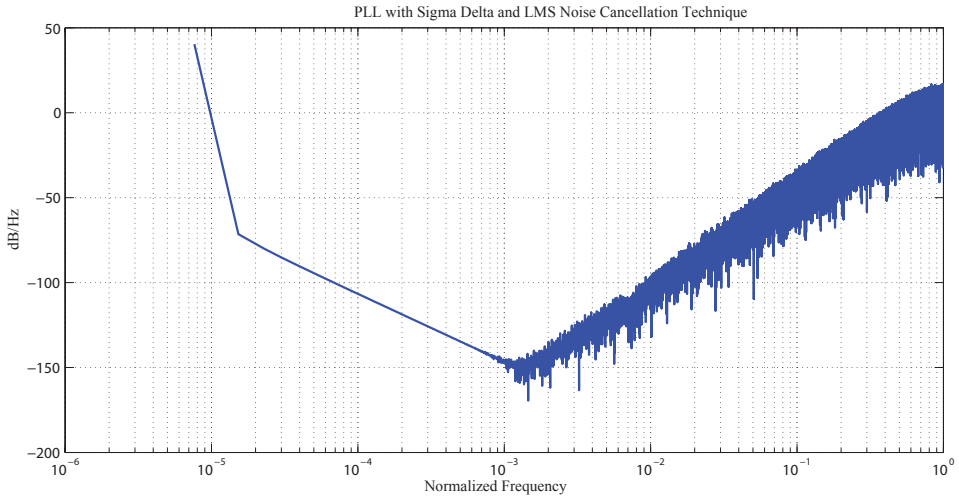

Figure 5.9: Simulated Output phase noise Spectrum of FNPLL with ΣΔ modulator and LMS Adaptive.

One noticeable observation from Figure 5.9 is that the frequency spectrum does not flatten out within the frequency of interest. In fact, it is encouraging to note that the results presented in Figure 5.9 confirms and has the same shape as Figure 1.5 presented in Chapter 1 under the *Fundamental principle of quantization noise*.

Although LMS has a longer convergence rate, it convergences with high signal stability within the in-band. Figure 5.10 shows the output spectrum simulated at a bandwidth of 200 kHz and reference frequency of 50 MHz.

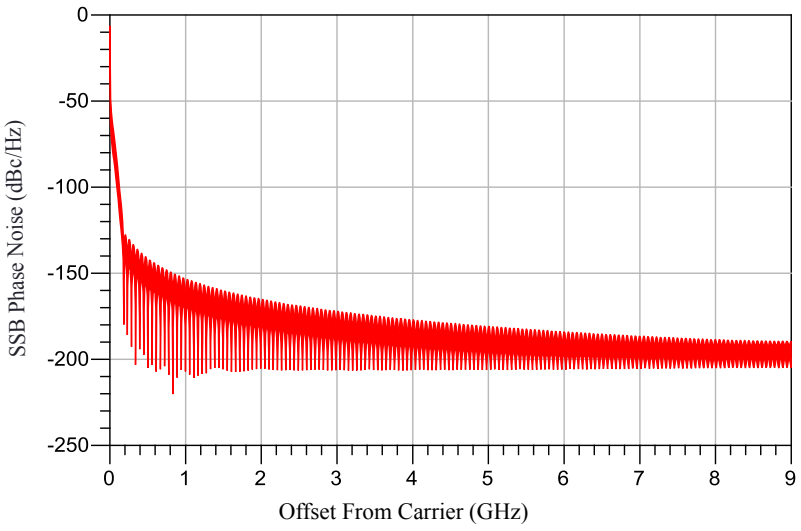

Figure 5.10: Simulated Output Phase Noise Spectrum of FNPLL with ΣΔ modulator and LMS Adaptive filter.

5.2.3 Stabilization of Signal fluctuation within the in-band

The well-shaped high-pass noise spectrum obtained and shown in Figure 5.10 may have understandable consequences if the filter is poorly designed, which may lead to the signal exceeding the maximum amplitude value for each frequency component beyond which the noise shape and SNR are destroyed. As soon as the maximum stable amplitude (MSA) value is exceeded the poles and zeros move out of the unit circle. The coefficients of the proposed model were computed by means of the Delta-Sigma Toolbox found in Matlab functions [88].

Filter stabilization was achieved by locating the poles and zeros within the unit circle, where they were treated as linear quantization noise. Table 5.1 depicts the computed NTF coefficients of the modified architecture. This process allows the Butterworth filter to be applied as it flattens the NTF notch in the in-band.

Table 5.1: Coefficients of the proposed sigma delta modulator architecture.

Loop coefficients of the designed model		
a	b	c
$a_1 = 0.157899$	$b_1 = 0.157899$	$c_1 = 1.0000$
$a_2 = 0.543330$	$b_2 = 0.000000$	$c_2 = 1.0000$
$a_3 = 1.194241$	$b_3 = 0.000000$	$c_3 = 1.0000$
$a_4 = 0.889446$	$b_4 = 0.000000$	$c_4 = 1.0000$

The resulting poles and zeros located within the unit circle and spread in the in-band to optimize the signal-to-quantization noise ratio (SQNR) are depicted in Figure 5.11. The significance of locating poles and zeros within the unit circle is that the signal had a maximum stable amplitude that ensures signal stability. Several simulations were conducted to check the behavior of the signal when poles are outside the circle it was found that beyond the MSA the required noise shape shown in Figure 5.9 is destroyed.

The Sigma-Delta Toolbox function $(NTF = synthesizeNTF(order, OSR, opt, OBG))$ was used to determine the NTF (Equation (5.1) of the proposed architecture (where, $order = 4, OSR = 23.62, n = 16, OBG = 3$).

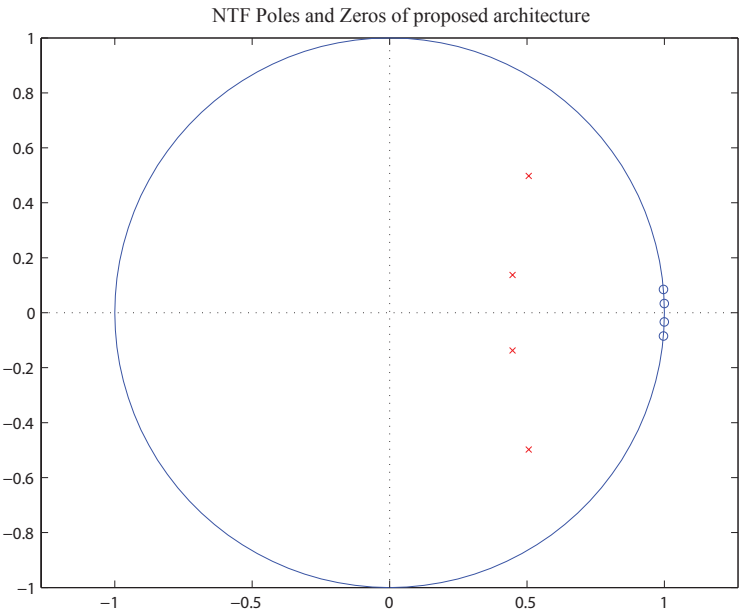

Figure 5.11: NTF poles and zeros location within the Unit circle.

$$NTF = \frac{(z^2 - 1.999z + 1)(z^2 - 1.9993z + 1)}{(z^2 - 0.8952z + 0.2192)(z^2 - 1.0133z + 0.5043)}. \tag{5.1}$$

Figure 5.12 shows the NTF of the new model simulated by means of the Sigma-Delta Toolbox in Matlab. This figure shows that the SNR in the in-band can be increased by pushing noise away from lower frequencies to higher frequencies.

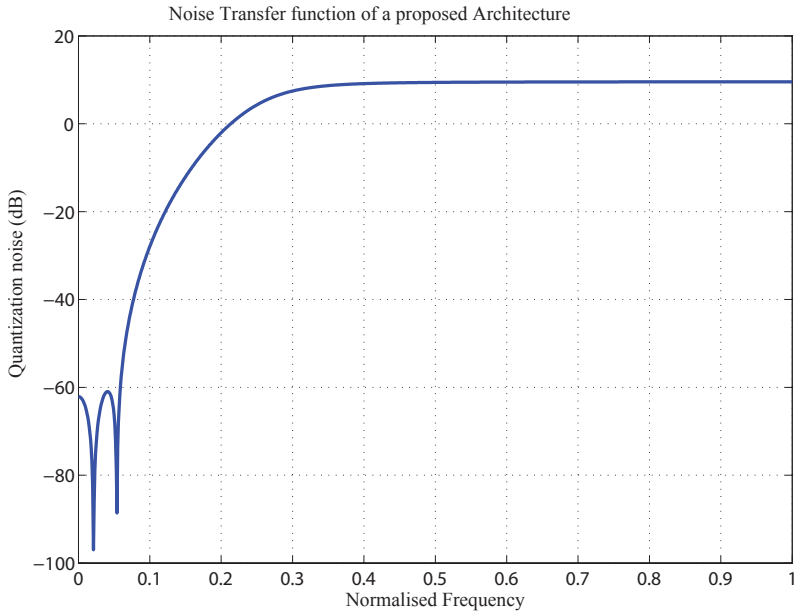

Figure 5.12: Quantization Noise of NTF with different coefficients.

5.2.4 Performance Results

The signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SNDR) are the most important metrics used to analyze the performance of the ΣΔ modulators. The only difference between the SNR and SNDR is that SNDR includes residual signal part only, which makes SNR slightly higher than SNDR values. For this case a 12-bit ADC converter (AD9228), mostly used in GSM and wideband code division multiple access (WCDMA), was simulated with the OSR of $\left[OSR = 10\log_{10}\frac{f_s}{2\times BW} = 10\log_{10}\frac{92.16\times10^6}{2\times200\times10^3}\right]$ 24, bandwidth of 200 kHz and a sampling rate of 92.16 MHz.

The theoretical SNR is calculated as;

$$SNR = 6.02\times12+1.76+24 \tag{5.2}$$
$$= 97dB.$$

The importance of the SNR values is that they give an idea about the error that occurred during the

signal conversion from analog to digital. Most high performing systems require a high level of SNR to minimize the error rates.

The model was simulated at different bandwidths to check impact of bandwidth on effective number of bits (ENOB), SNDR and SNR.

As shown in Figure 5.13, ENOB, SNDR and SNR decrease with an increase in bandwidth. This observation is supported by the following relationship;

$$SNR = 3 \times \left(\frac{BW}{2F_s}\right)^3 \times CNR. \tag{5.3}$$

The terms BW, F_s and CNR represent the transmission bandwidth, signal bandwidth and carrier to noise ratio respectively. From (5.3) it can be observed that if the BW is reduced, the SNR should increase to maintain the same channel capacity. Simulation results obtained at different bandwidths are summarized in Table 5.2, which shows higher ENOB and SNR values at 40 kHz and 200 kHz. The ENOB and SNR values are low at higher bandwidth (1500 kHz).

Table 5.2: Simulation results conducted at different bandwidths.

Simulation results			
BW (kHz)	ENOB (bits)	SNDR (dB)	SNR (dB)
40	19.44	118.8	115.26
200	17.58	107.6	104.1
1500	8.12	50.6	47.12

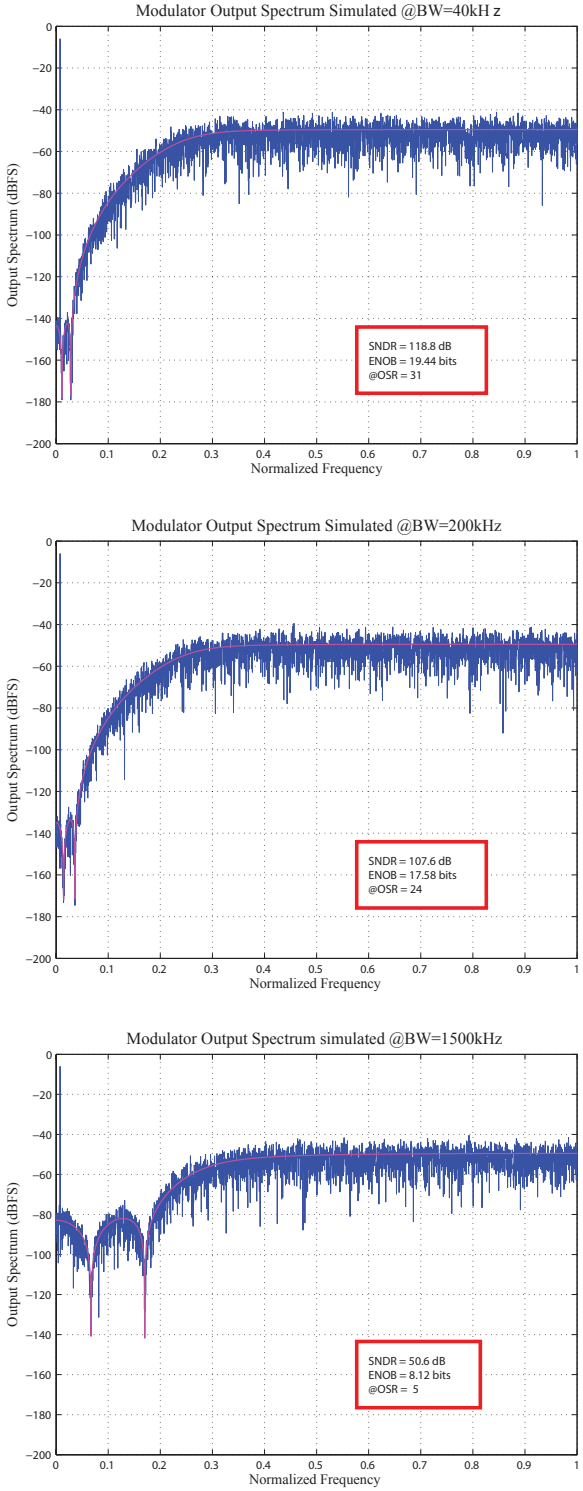

Figure 5.13: Output Spectrum of NTF zeros and poles Optimized Sigma Delta Modulator simulated at different values of OSR.

5.3 COMPARISON OF THE SIMULATED RESULTS WITH EXISTING LITERATURE

The simulation results of the proposed technique were compared with the existing literature. Table 5.3 shows that the simulation results of the proposed technique performs better than those of the existing literature. The ENOB and SNR values of the existing techniques ([39], [38] and [89]) were determined from the following relationships;

$$ENOB = \frac{SNDR - 1.76dB}{6.02}.$$
$$SNR = 6.02 \times ENOB - 1.767. \tag{5.4}$$

The determination of the ENOB and SNR from Equation (5.4) was based on the assumption that the input signal is at full-scale, which implies that any reduction of the SNDR decreases the ENOB.

The proposed technique achieved a phase noise level of below -141 dBc/Hz (as shown in Figure 5.10) and a significant SNR of 104 dB. The Texas Instruments [90] has recently published an application note on high speed ADC [ADS5294], which indicates that the ADS5292 consumes very low power but requires a significantly high amount of SNR to counteract the effects of clock jitters. These high speed ADCs have very high noise figures that require a significant amount of SNR to improve the signal quality. It is for this reason that the high SNR achieved in this simulation results is useful for high speed ADCs. From Table 5.3 it can be seen that the proposed technique achieved a significantly high SNR by 9 dB when compared with the existing literature [39], which makes it an ideal candidate for the wireless communication systems that uses high speed ADCs to digitize the analog signal in the transceiver.

Table 5.3: Performance Comparison.

Comparison				
Parameters	This work	[39]	[38]	[89]
Output Freq (GHz)	2.4	2.4	3.6	8.9
Ref Freq (MHz)	50	50	26	48
Bandwidth (kHz)	200	200	40	1500
ENOB	18	18	194	15
SNR (dB)	104	95	100	91
SNDR (dB)	108	98	103	94
PN (dBc/Hz)@1MHz	-141	-113	-123	-92

5.4 VERIFICATION OF THE PROPOSED TECHNIQUE ON 3GPP-LTE RECEIVER

The ADS LTE-A verification test bench, which provides access to the LTE parameter display library was used to validate the performance of the proposed model. The test bench is pre-configured to allow signal measurements to be carried for reference sensitivity level, dynamic range, etc. The proposed model was configured on the test bench as a device under test (DUT) were the design parameters of the proposed model were set.

The key performance metrics for the LTE standard (such as error vector magnitude (EVM) and bit error rate (BER)) were analyzed to check the impact of phase noise on EVM. The test bench allows the design verification of the RF-physical layer for the 3GPP-LTE wireless standards [91, 92, 93].

The wireless library contains a comprehensive list of pre-configured simulation setups.

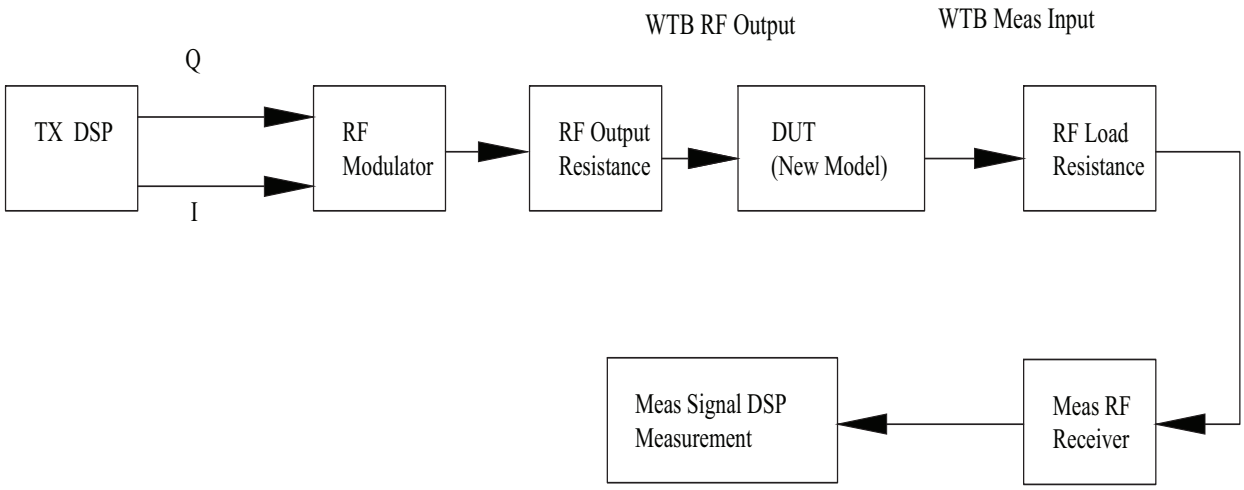

Figure 5.14: Block diagram of a 3GPP-LTE wireless receiver.

Figure 5.14 shows the block diagram of the 3GPP-LTE receiver test. The LTE users were connected to the DUT (proposed model) where the performance of the DUT were determined using the design parameters. The design parameters were set in place of the pre-configured parameters.

The LTE users were connected on the ADS test bench depicted in Figure 5.15 where the performance of the DUT (proposed model) was determined using the pre-configured signal measurements parameters that are based on the 3GPP-LTE technical specification and the design parameters of the proposed model presented in Table 3.1. Table 5.4 depicts the basic design parameter information required by the ADS test bench to perform required simulation measurements. These are the main and critical parameters that are required for the test bench setting, simulation performance and displaying performance results.

Table 5.4: ADS parameter information required for signal measurement.

Design Parameters		
Parameters	Parameter Name	Values/Specifications
Carrier Frequency	FSource	2.4 GHz
Resistance	SourceR	50 Ohm
Frequency offset	$Blocking - ModFreqOffset$	1 MHz
Resistor temperature	SourceTemp	16.85 deg

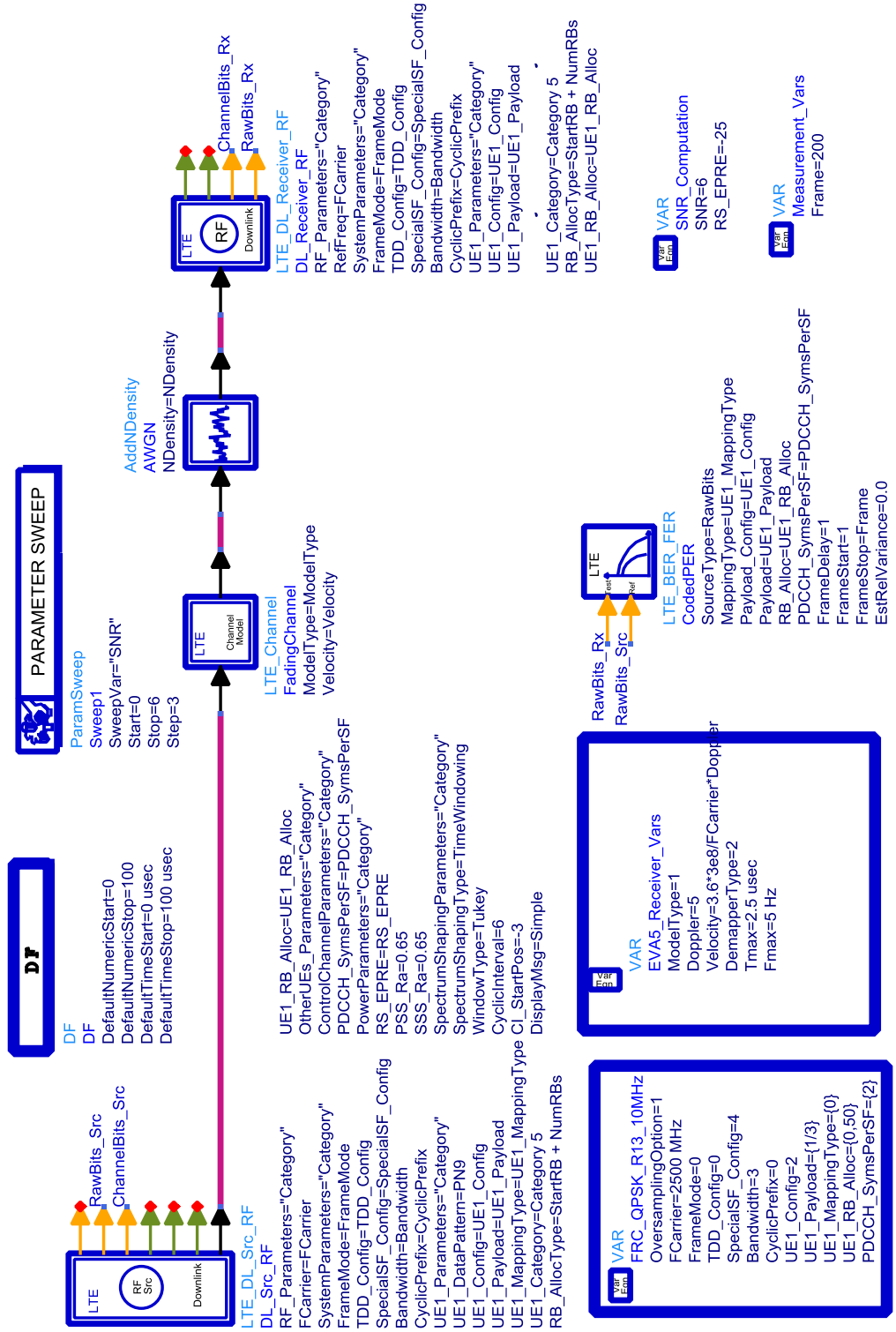

Figure 5.15: ADS 3GPP-LTE receiver test bench.

5.4.1 Phase noise performance

The phase noise performance of the proposed technique is depicted in Figure 5.10, which was obtained after conducting simulation in the ADS LTE DL test-bench set-up. The phase noise plot depicted in Figure 5.10 shows that the power level drops to -141 dBc/Hz at an offset of 1MHz in the region where the slope is 20dBc/dec and holds until it flattens out. It can be seen from Figure 5.10 that there is a significant phase noise improvement with a clean spectrum in frequency of interest without any visible spurious tones.

5.4.2 BER performance evaluation

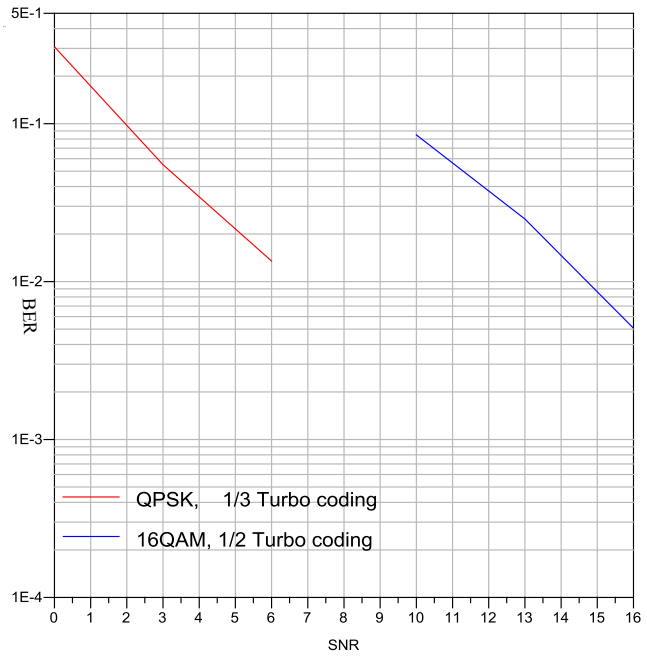

Figure 5.16: BER Performance evaluation of the proposed model on Agilent ADS LTE DL source.

The BER performance depicted in Figure 5.16 was obtained after the implementation of the parameterized model of the LTE DL test-bench set-up where the phase noise values were swept from 0 dBc/Hz to -200 dBc/Hz. The Performance evaluation of the proposed technique was conducted for the coded QPSK and 16 QAM. Figure 5.16 shows that the 16QAM signal degrades more with the swept phase noise values than the QPSK and QPSK signal produces a far much better performance with less SNR when compared to 16 QAM. The theoretical minimum SNR for the 16QAM (1/2) signal specified by the LTE 3GPP standard Rev10 is 7.9 dB and the proposed model achieved a SNR of 9 dB, which is slightly above the specified minimum value by 1.1 dB.

5.5 CONCLUSION

This chapter presented the simulation results of the proposed technique. Chapter 5 presented the behavioural modeling and system simulation of the proposed technique, which allows various design parameters to be set. The implementation of the four stage ΣΔ modulator via accumulators and differentiators available from the ADS component library was presented. The FNPLL subcircuit, which allows a behavioural model of different components (VCO,PFD and FD) to be simulated efficiently (overcoming long simulation hours) was discussed.

CHAPTER 6 CONCLUSION

The main objectives of this research were to:

- Develop a new phase noise cancellation technique that achieves low phase noise level with minimal spurious tones within the frequency of interest.
- Formulate mathematical models for the proposed architecture.
- Simulate the proposed model and compared simulation results with the existing techniques.

The findings and achievements of this research work are summarized in the following sections.

6.1 NEW PN ARCHITECTURE

A new phase noise cancellation architecture based on the single-loop, single-bit ΣΔ modulator, LMS adaptive filtering and cascaded resonator feedback (CRFB) was presented. The proposed method relies on the adaptation of the quantizer step-size (through LMS algorithm) to control the fluctuation of the quantization noise within the frequency of interest. The weights of the LMS adaptive filter were modeled in such a way that they resulted in a better control of the out-of-bound gain (OBG, caused by the DAC).

6.2 SUPPRESSION OF SPURIOUS TONES

The main problem with the FNPLL is that it experiences short periodic cycles that are generated by the ΣΔ modulators, which cause harmonics and spurious tones within the frequency of interest. This problem was resolved by implementing an LMS adaptive filter, which allows coefficients of the noise transfer function to be modeled in such a way that the poles and zeros of the NTF are located within

the unit circle to avoid high signal fluctuation and instability within the frequency of interest. Placing poles and zeros of the NTF within the unit circle makes it possible to achieve a stable and high SNR while maintaining the maximum stable amplitude (MSA) of the signal.

6.3 ACHIEVED RESULTS

The proposed model was simulated in Matlab and implemented in ADS. Simulations results show the proposed model achieves a significant low phase noise level (-145) dBc/Hz [94], which is an improvement of 9 dB compared with the existing technique. Simulation results were also conducted for other performance metrics (SNR, SNDR and ENOB) where it was found that the new technique has achieved a better SNR of 104 dB, which makes it an ideal candidate for a high speed ADC (ADS5292) application that consumes very low power.

6.4 RECOMMENDATIONS FOR FUTURE RESEARCH

The proposed model for phase noise cancellation is based on adaptive filtering LMS and cascaded resonator feedback architecture that achieved significant phase noise level of -145 dBc/Hz and high SNR (104 dB). This method was based on the simulation of the LMS adaptive filter component that was obtained from the ADS component library. Although recently published application note by Texas Instruments on high speed [ADS5294] suggests that the high speed ADC require high SNR and consumes low power, a further investigation is required to confirm if the proposed technique can perform well under low power conditions. This can be done by implementing different LMS components available from the ADS library and compare their energy consumptions at higher SNR.

6.4.1 Implementation of the proposed solution on NMLS and RLS

The phase noise cancellation architecture proposed in this study can be extended and implemented in ADS with normalized LMS (NMLS) and RLS components to compare the achieved phase noise level with that obtained in this study.

6.4.2 Implementation of the proposed technique on a 65 nm CMOS technology

While the results of the comprehensive benchmarking with other techniques were presented in Table 5.3, the implementation of the proposed technique on a 65 nm CMOS technology where the limitation of the substrate is taken into account might show a much improved results. The limitations imposed by the substrate that need to be modeled include but not limited to;

- Insensitivity to supply noise.
- Parasitic coupling.

Furthermore, it is recommended that the proposed technique be implemented on the chip design to compare the theoretical and simulation results with real-measured performance.

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