UNIVERSITEIT VAN PRETORIA
UNIVERSITY OF PRETORIA
YUNIBESITHI YA PRETORIA

DIFFERENTIAL CURRENT SENSOR LINEARISATION IN LOW-VOLTAGE CMOS

by

Neil Naudé

Submitted in partial fulfilment of the requirements for the degree
Master of Engineering (Electronic Engineering)

in the

Department of Electrical, Electronic and Computer Engineering
Faculty of Engineering, Built Environment and Information Technology

UNIVERSITY OF PRETORIA

January 2017

SUMMARY

DIFFERENTIAL CURRENT SENSOR LINEARISATION IN LOW-VOLTAGE CMOS

by

Neil Naudé

Supervisor:	Prof S. Sinha
Department:	Electrical, Electronic and Computer Engineering
University:	University of Pretoria
Degree:	Master of Engineering (Electronic Engineering)
Keywords:	Low-voltage, CMOS, monolithic current sensor, SenseFET, linearisation, folded cascode, DC-DC converter, bias current equalisation, wireless sensor networks, CMOS process characteristics

The viability of low cost, distributed, and autonomous wireless sensor networks is determined by the affordability of the integration and operation of each sensor node. Self-sufficient nodes which harvest energy from the local environment decrease operating and maintenance costs over extended periods of time. This affordability can be achieved by increasing the power usage efficiency of designs implemented in an older and cheaper CMOS process. This circumvents the use of a more compact technology node which trades increased efficiency for cost. The efficiency of power conversion is determined by topology, component quality, control scheme, and internal measurement accuracy.

This research focuses on improving internal measurement during the power conversion process, in order to reduce conversion loss from the internal control error. A current sensing integrated circuit was proposed which is insensitive to dominant process characteristics which degrade the performance of other sensing solutions. In particular, the detrimental effect of channel length modulation is compensated for. This compensation is achieved by decoupling the sensor biasing and differential steering pair from being influenced by the external current being measured. Widely used solutions were studied and analysed in the context of implementation in a low cost and low-voltage CMOS process. Key process characteristics which negatively influenced these solutions were identified and formed the basis of developing an improved integrated current sensor. Current research in the literature

is tightly focused on improved accuracy without the constraints of process costs, low operating voltage (800mV – 1.2 V), and prevalent second order effects of device operation.

A study of the literature on CMOS-based integrated current sensing demonstrates a common goal towards improving sensor accuracy by developing either new topologies or augmenting known topologies. New and augmented topologies focus on novel analogue networks which aim to improve the linearity of CMOS based current sensing. The colloquially named SenseFET circuit is a foundation for many variations of integrated current sensor. This integrated circuit generates an estimate of the current flowing into a DC-DC boost-buck converter by sampling the current sourced into the converters inductor. The low maximum operating voltage of the chosen CMOS process restricts the application of typical published solutions. The sensitivity of other solutions to second order effects limits application as well. The proposed solution is based on such a sampling topology with a focus on achieving linearity in a process with pronounced channel-length modulation effects as well as a relatively low operating voltage. The goal of the improved design is to test if linearity can be improved by developing a circuit which is robust towards second-order process effects.

Discreet and integrated boost-buck converters were studied and analysed to form the basis of further sensor developments. An integrated non-inverting converter topology suitable for single rail operation was identified and designed as the system environment for which an integrated sensor would be developed. This would allow for comparison of sensor designs in a known environment, both in simulation and in prototyping of the integrated system. The proposed integrated current sensor was developed analytically before being simulated both mathematically and at transistor gate level. This iterative process was applied to a known design as a performance baseline and to demonstrate the improvements achieved.

A prototype integrated circuit and test boost-buck converter were implemented in a 130 nm BiCMOS process to test and verify the sensor design against simulated results. Integrated circuits implemented include a reference and improved current sensor, boost-buck converter without closed loop control, and a boost-buck converter using current feed-forward control. The total proposed sensor area is 12 µm × 17 µm. The improved sensor performed well when operated over a more constrained range than what was designed for. Measured linearity compared favourably with simulation, with the exception of linearity at switching cycle boundaries. The improved sensor operates from 800mV to 1.2 V and has a transresistance gain of 5 V/A on both the charge and discharge portions of the power conversion cycle. The

designed gain was 2 V/A. Inductor current inversion at the conversion cycle boundaries resulted in unexpected but explicable behaviour.

ACKNOWLEDGEMENTS

I would like to thank the Eskom Tertiary Education Support (TESP) programme for its financial sponsorship in the preliminary stages of this study. Through the work done for the TESP, I was able to lay the foundations of this study and work that followed.

The MOSIS Educational Programme (MEP) was instrumental in facilitating this work. The MEP's sponsorship of the chip prototyping allowed my ideas and work to be tested. Prototyping through the MEP enabled practical outcomes from the study, adding credibility to my work for which I am thankful.

Professor Saurabh Sinha has been a source of guidance and knowledge throughout the majority of my academic career. His support and drive has been a positive influence throughout the course of this work, motivating me to continue working despite the challenges of balancing my professional career, personal life, and academic activities. I am not only grateful for his involvement and patience, but motivated to keep improving and diversifying my engineering, professional, and academic skills.

Dr Melissa Adendorff not only provided her excellent proofreading and editing skills, but offered a wealth of knowledge and advice that I relied on to successfully complete this dissertation. Her continual support and criticism were indispensable, allowing me to approach aspects of this work with insight and understanding. As my partner, her support was invaluable and I only have the greatest appreciation for her efforts.

I would also like to thank my family for their patience and support from the start and throughout this work.

Finally, I would like to thank the following individuals and organisations for their time and resources:
Dr Mladen Božanić for his advice and assistance at the start of this study,
Dr Tinus Stander and the staff of the Carl and Emily Fuchs Institute of Microelectronics (CEFIM) at the University of Pretoria, for allowing me to use their facilities.
My employer and colleagues at GEW Technologies (Pty) Ltd, for their support and laboratory resources.

LIST OF ABBREVIATIONS

BiCMOS	Bipolar CMOS
CMC	Current mode control
CMOS	Complementary metal oxide semiconductor
DC	Direct current
DRC	Design rule check
DMM	Digital multi-meter
DUT	Device under test
ESR	Effective series resistance
FET	Field effect transistor
IC	Integrated circuit
KCL	Kirchhoff's current law
LDO	Low drop out
LVS	Layout versus schematic
MEP	MOSIS education program
MDO	Mixed domain oscilloscope
MPW	Multi-project wafer
NDA	Non-disclosure agreement
OPAMP	Operational amplifier
PA	Power amplifier
PCB	Printed circuit board
PSU	Power supply unit
PVT	Process, voltage, and temperature
PWM	Pulse-width modulation
QFN	Quad flat no-lead
RF	Radio frequency
SCE	Short channel effects

SMD	Surface mount device
SPICE	Simulation program with integrated circuit emphasis
TE	Test equipment
VMC	Voltage mode control
WSN	Wireless sensor network

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION

1.1 CHAPTER OVERVIEW

This dissertation investigates integrated circuit (IC) current measuring techniques as a method of improving the efficiency of integrated switched mode power converters. This chapter provides the contextual background and motivation for this investigation, as well as an overview of subsequent research. The presentation of the development of relevant research questions follows, as well as an explanation of the relevance of the research, and the scope of the investigation. This chapter finally presents an overview of the study's methodology and the structure of this dissertation.

1.2 BACKGROUND OF THE RESEARCH

Autonomous wireless sensor networks (WSN) are able to perform long-term data acquisition of environmental factors in the region in which they are deployed [1]. Sensor nodes that do not require maintenance, and which could be produced inexpensively, allow for the construction of affordable sensor networks. Affordability allows for the detailed characterisation of environments, whether they be industrial, agriculture, or urban in nature.

Sensor networks may be broadly characterised as either structured sensor networks, or as unstructured sensor networks [1]. Each node in the network gathers data within its measurement range, and this data is either stored or transmitted to a data collection point. Structured networks utilise few sensor nodes at selected, or lumped, points in the environment of interest. In such sensor networks, the sensor nodes do not gather data from the entire environment, but from specific planned locations. Unstructured networks utilise a ubiquitous and ad hoc sensor distribution in the environment of interest. This distinction in terms of node distribution drives the functional requirements of each node. The relatively sparse nodal distribution in a structured network relaxes the cost and energy constraint of each sensor node. In an unstructured network, the number of sensor nodes required to provide full coverage of the environment of interest is high, requiring low cost sensors that remain effective. For a sensor node to be effective as an unstructured network element, it needs to be self-sufficient, maintenance free, and inexpensive enough to be replaced instead of repaired. Integrated circuit (IC) technology is suitable for meeting these requirements.

Figure 1.1 depicts an overview of a sensor node's functional requirements in an unstructured network, as well as additional detailed requirements that are part of the focus of this dissertation.

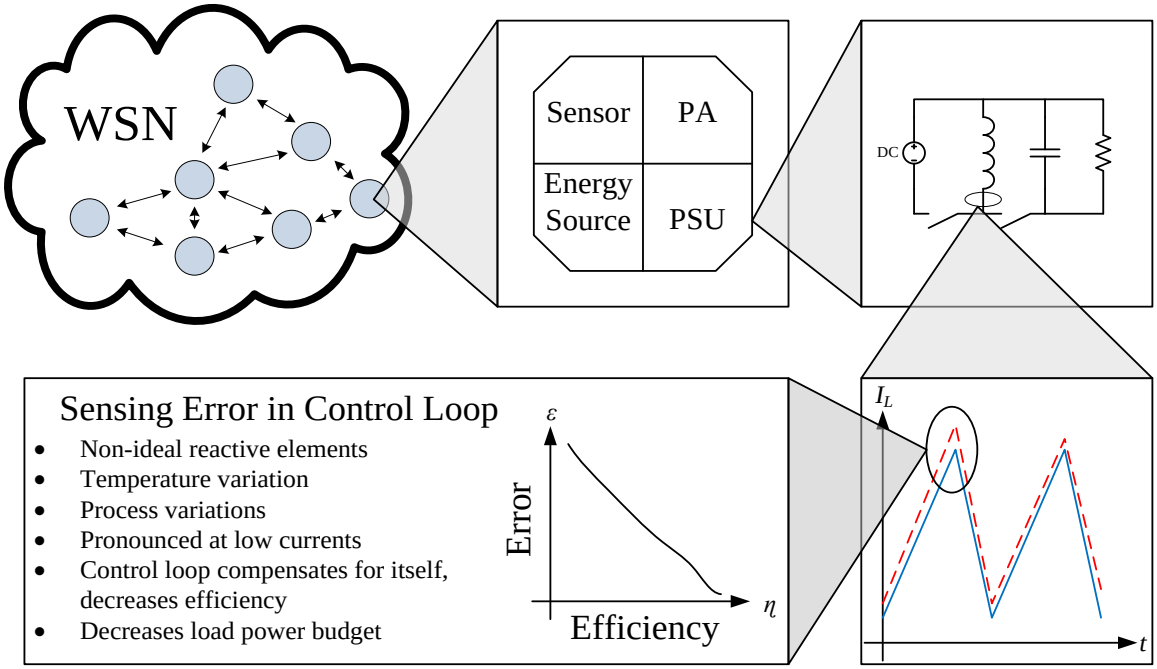

Figure 1.1. Unstructured WSN node requirement breakdown.

The sensor node diagram in Figure 1.1 consists of an energy source, power supply unit (PSU), power amplifier (PA), and the sensor [2]. Each functional unit in the node is powered by the energy source. The PSU converts the energy from the energy harvesting source to a DC power source for the sensor and PA. The sensor sub-system contains the sensing circuitry as well as digitisation and processing, storage, and radio frequency (RF) up-converter. The PA sub-system consists of the amplifier and antenna required to connect wirelessly to the rest of the sensing network. The amount of energy that the energy source can supply and the efficiency of the PSU determines the overall power budget for the entire sensor node. Each of these four sub-systems has operational and design aspects which can be improved on to achieve the core design mandate.

Operational efficiency may be improved by migrating the sensor node design to a more compact integrated process [3]. This is done at a greater expense, threatening the low-cost requirement. An alternative is to improve efficiency in a lower cost process. This dissertation presents this approach as applied to the PSU.

The PSU comprises several aspects which determine the overall efficiency of operation. These aspects may be classified as being influenced either by design or by component and environmental characteristics. Figure 1.1 demonstrates how one such design aspect can be the source of inefficiency. Effective switched mode power conversion relies on internally measuring the flow of energy through the conversion process, and using this information to steer internal control schemes. The accuracy of this measurement is influenced by multiple factors, including process and temperature variations, non-ideal reactive components, and low voltage operation. An inaccurate internal measurement introduces erroneous information into PSU control loop. The processed error leads to control loop inaccuracies.

1.3 HYPOTHESIS AND RESEARCH PROBLEMS

Integrated PSU design and research focuses on three key areas. These are internal measurement, control scheme topology, and improved reactive networks. Reactive networks are off-chip. Effective control schemes are well understood [4], [5], and the analogue subsystems used to implement these schemes make extensive use of operational amplifiers (OPAMP). Similarly, analogue signal processing using OPAMP implementations of the required control transfer functions is well documented [6]. Internal measurement is an area of active research with several techniques being developed for modern CMOS processes [7], [8] and [9]. These techniques are not commonly implemented in low-voltage technologies which are of interest for sensor node implementation. This alludes to a potential area where improvements and adaptations could be made to make a low-voltage implementation feasible.

The implementation and necessary improvement of these internal measurement techniques in a low-voltage process could lead to viable solutions for deploying PSU designs that compete in performance with known designs implemented in a more compact technology node. The performance characteristics of internal current measurement techniques implemented in an available low-voltage 130 nm CMOS process must be determined. The available CMOS process has a low maximum gate-oxide breakdown voltage, and the device's performance is strongly influenced by channel length modulation effects. This dissertation considers low operating voltage and non-negligible second order effects on the linearity of known current sensing techniques.

Using the aforementioned rationale and the outcome of analysis and simulation of current techniques in the available CMOS process, the research hypotheses may be stated as follows:

> *If integrated circuit topologies for measuring current using CMOS devices were improved to be resilient to second order effects and low voltage operation, the linearity of the measurement would improve.*

The following key research problems complement the aforementioned hypothesis:

1. Determine the extent of the effect of second order effects on the linearity of integrated current sensing circuits.
2. How will the non-linearity be modelled using traditional analytical models? How could such models be used to gain additional insight into circuit operation and be used to derive solutions that address non-linearity? How well do these models agree with gate level simulation?
3. How robust are the solutions to process, temperature, and voltage (PVT) variations?
4. Determine if it possible to significantly improve linearity in comparison to other designs.

A prototype implementing both a reference design as well as an improved design will be used to draw comparison between implementation and theoretical analysis and modelling. Outcomes of this comparison are used to verify or refute the hypothesis. The differences between theoretical and practical implementations are subjected to additional analysis to determine the origin of discrepancies.

1.4 JUSTIFICATION FOR THE RESEARCH

The rationale for improving design efficiency at a specific CMOS technology node is to obtain equivalent power performance from a larger[1] and more cost-effective process than that of a smaller, lower power, and expensive process [3]. The aim of this research is to decrease the cost of production without a significant reduction in power efficiency. If the requirements for implementing an unstructured WSN are considered, then a high efficiency at reduced cost is paramount to the viability of such networks.

[1] The terms “larger” and “smaller” refer to the minimum aspect ratio possible in a CMOS process.

This study focuses on improving the efficiency of the power converter which converts a variable DC input to a fixed DC output. Improving the conversion efficiency allows for an increased power budget from which other systems in the sensor node must draw power. This work therefore focuses on the internal sensing used by DC-DC switched mode converters to monitor the current flowing through the converter.

The techniques presented in this dissertation are justified by the poor transferability of current designs to the target 130 nm process. The relatively low operating voltage (0.8 V to 1.2 V) and prominent second order effects in the 130 nm process are detrimental to the linearity of current designs by reducing the dynamic range of these designs. The reduction in dynamic range introduces an internal measurement error which causes the internal control loop to either under or over compensate during the conversion cycle. The non-linearity renders these designs unsuitable solutions for internal current sensing. This dissertation presents possible techniques which may be used to improve the linearity of these internal current sensor designs by utilising networks which are resistant to process parameters introducing errors.

Finally, this study demonstrates improved linearity, strengthening the justification for using the low cost and low-voltage 130 nm CMOS process as a platform for the development of sensor nodes in a WSN.

1.5 RESEARCH METHODOLOGY

Figure 1.2 diagrammatically demonstrates the methodology used to approach the work in this dissertation. The methodology has three phases, with each phase focusing on a collection of sequential and iterative tasks specific to the goals of the phase.

The first phase comprises the problem definition which is focused on defining and refining the research questions which must be asked. The primary task is a detailed literature study of relevant material to identify the research value. The literature study is an iterative process, starting with a broad investigation into switched mode design principles and their application in the integrated circuit environment. On each iteration of the literature study, the study becomes more focused until the specific research value can be identified in terms of the broader research goals. For this work, the functional components of integrated switched mode supplies are studied to identify which component is a candidate for improvement with the overall goal of improving system performance of the switched mode converter.

The implementation of the internal current sensing circuit in a 130 nm process was identified as viable candidate for improvement. This process was available to students at the University of Pretoria through the MOSIS educational program (MEP). The IBM 8HP BiCMOS process at the 130 nm technology node offers a process which is affordable and operates at low-voltage. The feature size of this process is also in accordance with the trending features size of other work in the literature. These characteristics of the IBM 8HP BiCMOS process make it a suitable candidate to test and develop the concepts in this dissertation.

The second phase is focused on familiarisation with fundamentals and development of techniques which may be used to test the hypothesis. This includes the creation of a baseline, which is developed from designs in the current literature as a performance reference. The design research focus also requires an integrated test bench which is used to stimulate the proposed design and reference. Development is an iterative process alternating between high level mathematical models and low level device simulation.

The designs are developed from analytical models which form the basis for the mathematical models implemented in MATLAB[2]. The outcomes of these models form the basis of the development of the required sensing and test circuits in a 130 nm BiCMOS process through the MOSIS educational program[3]. The circuits are designed and tested using Cadence Virtuoso[4]. Once the development is able to demonstrate an improvement in software simulation, the second phase is complete.

[2] MATLAB is supplied by Mathworks (www.mathworks.com), developers of technical computing software for scientists and engineers.
[3] More information on scheduled multi-wafer projects from the MOSIS service is provided at (https://www.mosis.com/).
[4] *Cadence Virtuoso* is a visualisation and analysis tool for simulating and analysing the performance of analogue, RF, and mixed-signal designs

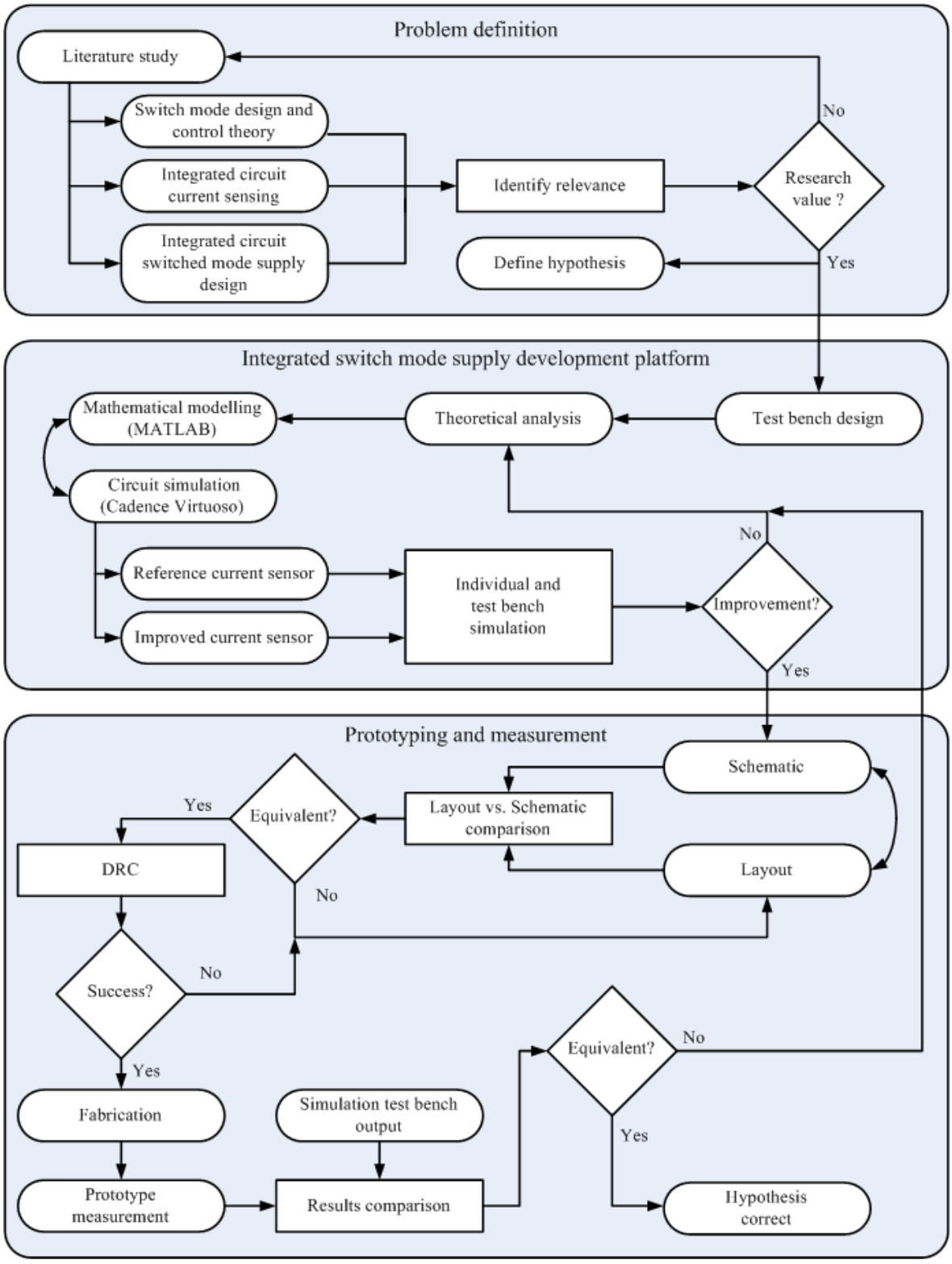

Figure 1.2. Outline of research methodology.

The third and final phase focuses on real-world prototyping and testing of the hypothesis. The integrated circuit layout of the designs to be tested is done in Cadence Virtuoso. Cadence Virtuoso is also used to test electrical equivalence between the design schematic and physical

layout. Once the layout satisfied the equivalence requirement a final design rule check (DRC) must be run to verify whether the layout is suitable for manufacture.

The final fabrication is achieved through the MOSIS service. The fabricated IC is mounted to a printed circuit board (PCB) which serves as an interface between the final IC and external circuit components and test equipment. Measurement data are thus captured using a mixed domain oscilloscope. The captured data is processed in MATAB and compared with simulation and analytical outcomes. These comparisons are then used to test whether the hypothesis is correct, and to draw additional conclusions.

1.6 DELIMITATIONS AND ASSUMPTIONS

It is assumed that the circuit behaviour described and the techniques that were developed and applied are transferable to technologies with a similarly low operating voltage and influential channel modulation effects. This should be verifiable through research, comparing process parameters and simulation using alternate process models. Implementation in an alternate process operating at a higher process voltage is not possible using the available resources, and the techniques implemented in such technologies are thus transferred to the available CMOS process to draw comparison. Analytical models are used to show the influence of various process parameters and operational conditions on the developments in this dissertation.

The focus of this study is on the development of an improved integrated current sensor for integrated switched mode power supplies. The design of the test circuits prioritises basic functionality. The integration with off-chip components did not focus on a high level of integration. High quality common components are thus selected to implement external circuit elements.

Prototype hardware in this study is limited to a single iteration over the course of this study. This limitation stems from limited availability of silicon real-estate through the MOSIS education program. Furthermore, the iterative process takes several months.

In practice, a completely integrated sensor node would make use of a power source that harvests energy from its environment, using additional circuitry to condition this energy to comply with the limits of the 130 nm process used. In this study, the external power is provided by a digitally controlled power supply to provide predictable and consistent power

for measurement and evaluation of the prototype. In a similar manner, the switching signal used to drive the switched mode converter test bench is provided by an external signal source.

1.7 CONTRIBUTION

The primary contribution in this dissertation is the application of techniques used in differential amplifiers and current references to supress the significant influence of non-linear effects on a current sensing circuits operation.

The 130 nm CMOS process used has a relatively low maximum operating voltage of 1.2 V with significant channel length modulation. Relevant designs [10] in the literature make use of CMOS technologies with a higher maximum operating voltage. The higher operating voltage allows for integrated current sensors to be linearised using operational amplifier based designs. These solutions are not easily transferrable to the low-voltage 130 nm CMOS process. This dissertation utilises an alternative approach that introduces a compensating network suppressing the effects of channel length modulation on current sensor operation. This network additionally provides a degree of immunity to external network voltages influencing current sensor biasing.

1.8 PUBLICATIONS FROM THIS RESEARCH

The work in this dissertation also resulted in an accepted publication for the peer reviewed journal, Microelectronics International [11]. The paper, accepted for publication in August, 2016 is titled: *Linearized differential current sensor in low-voltage CMOS.*

This technical paper focused on the techniques used to linearise the current sensing SenseFET circuit as well as experimental results from the prototype.

1.9 OUTLINE OF THE DISSERTATION

Chapter 1 provides context and motivation for the work in this dissertation. The research hypothesis is formulated and justified. The research methodology that is applied to test the hypothesis is presented. Delimitations and assumptions are discussed and justified to constrain the scope of this study. Finally, the research contribution is discussed.

Chapter 2 presents a review of the literature relevant to the development of the hypothesis. A summary of techniques and approaches is presented in clarify the void in current

knowledge that the hypothesis is testing. This chapter primarily discusses current sensing techniques developed by other researchers and the technologies in which these techniques were implemented.

Chapter 3 focuses on the applied methodology and tools used to test the hypothesis. Analytical and mathematical models are described in terms of the definition of the predominant research questions in the realm of circuit analysis and design. The application of these models and tools is also described.

Chapter 4 has two areas of focus. Firstly, the chapter discusses the outcomes from the application of the methodology and models in Chapter 3. The models developed are applied and tested in a simulation environment. The first order results are evaluated against model outcomes and used to refine designs. The refinements are discussed and simulation is used to demonstrate differences. The second part of the chapter focuses on the implementation and development of a prototype in the available CMOS process. This area of focus discusses transferring circuit designs in terms of layout, and motivations for layout choices.

Chapter 5 documents the measurement process and evaluation of the prototype performances. It presents a comparison of these results with simulation results, as well as a discussion of the similarity and differences in performance and behaviour between simulation, analytical, and practical domains.

Chapter 6 collates the information from the preceding chapters to draw conclusions and answer the predominant research questions. The result of the hypothesis test is formally stated. This chapter also discusses shortcomings of the test, contributions made to the body of knowledge, successes and failures, and the potential for future research.

1.10 CONCLUSION

This chapter provided an introduction to the work covered in this dissertation. The problem context was described as well as how a research hypothesis was developed. The justification for this research was presented. The research methodology used to test the hypothesis within the constraints of the available resources was described. A summary of the research contribution was provided. The outline of the dissertation provides the reader with an overview of the material covered in each chapter.

CHAPTER 2 LITERATURE STUDY

2.1 CHAPTER OVERVIEW

This Chapter presents concepts from the literature used to develop and define the research hypothesis. The wider research context is investigated and refined in order to establish a clear focus for subsequent work needed to test this hypothesis. This Chapter also provides an overview of the concepts and mathematical models which the study utilises to formally define the research questions.

Energy harvesting techniques and switched mode DC-DC converter topologies are investigated, alongside control schemes for effective switched mode power supply design. It is necessary to investigate the implementation of these converter topologies in CMOS technology, in order to determine areas of improvement. The process limitations of the available technology are considered. The outcomes of this investigation are used to develop both the test and the development environment used in this work. The hypothesis tested in this research calls for the development of new internal current sensing circuits to be evaluated against solutions from the literature. This Chapter presents an investigation of such current sensing circuits.

2.2 DISTRIBUTED SENSOR NETWORKS

Wireless sensor networks (WSNs) are sensor networks with multiple interconnected nodes. Each node in the network is wireless and interacts with neighbouring nodes through a wireless interface. This connectivity may be used to create a wireless sensor network which is distributed throughout a target environment. WSNs do not typically feature an extensive support infrastructure. The networks are designed to be deployed in inaccessible regions with little or no maintenance support.

WSNs are categorised as either structured or unstructured. Structured networks have a predetermined structure with each node in a planned location. Unstructured networks do not have a planned structure and sensor nodes are distributed randomly throughout an environment [1]. The advantage of structured networks is that they require fewer sensor nodes to be effective, allowing a limited degree of maintenance and supervision. Unstructured networks have too many nodes (thousands to tens of thousands) for supervision

and maintenance actions to be practical. For this reason, unstructured networks need to be autonomous.

A typical wireless sensor node comprises a power source, one or more sensors, memory and processor, and a radio transceiver. Each of these aspects of the sensor node is constrained by the cost and functional requirement for the WSN. These constraints include limited power, communication range, hardware cost effectiveness, limited processing power, and memory.

2.3 ENERGY HARVESTING

Practical WSNs have sensor nodes which do not require maintenance, and this is also applicable to the node's power source. Discrete sensor nodes can have power consumption as low as 0.3 mW [12] but still rely on battery power, limiting the nodes operational life to several years. The low power requirements of integrated devices allow energy harvesting from the environment to be a viable source of renewable power. The typical power usage for an integrated sensor node is between 1 µW and 20 µW [13] with complex sensors requiring up to 100 µW [14]. Sources from which energy can be harvested fall into five general categories, namely motion and vibration (kinetic), thermal gradients, photovoltaic sources, RF energy [15], and electrochemical processes.

Energy harvesting from motion and vibration utilise electrostatic, piezoelectric, or electromagnetic transducers to convert kinetic energy into electric energy [16]. Electrostatic transducers convert the relevant motion between polarised and overlapping terminals of a capacitive device to a stored charge as the potential between terminals changes. The charge generated by the deformation of materials under mechanical stress is used in piezoelectric transducers. Electromagnetic transducers utilise electromagnetic induction which arises from the relative motion of a conductor through an electromagnetic field.

If two lengths of dissimilar conductors are connected, the unconnected terminals will develop an open circuit voltage, if the temperature of each conductor is different. This is known as the Seebeck Effect, and it is used to harvest energy from thermal gradients. Energy may be harvested from light using a transducer incorporating photovoltaic cells. The effectiveness of the photovoltaic cell is strongly dependent on the available incident light.

RF energy harvesting harnesses ambient RF energy in a desired band using an antenna. The primary obstacle to harnessing RF energy is that RF energy attenuates rapidly as it

propagates through the atmosphere and other environmental elements. Obtaining a meaningful amount of energy requires a large collection area, or a localised RF energy source designed specifically to distribute power to a WSN [15].

Energy harvesting is possible in an environment where natural electrochemical processes could be exploited. Such a potential environment is a WSN deployed over and within a living organism. The fluids in such an environment have electrolytic properties, allowing for the construction of a rechargeable battery as the electrolytic fluid is replenished. Such a battery is demonstrated in [17] and develops 1.5 mW at 1.2 V.

2.4 DC-DC CONVERTER FUNDAMENTALS

This section presents an overview of DC-DC converter fundamentals, specifically the buck-boost topology, which is able to develop an output voltage either larger or smaller than the input [18]. This presentation comprises a description of the operation of this topology, as well as its two modes of operation. Figure 2.1 presents a diagram of a basic inverting buck-boost DC-DC converter.

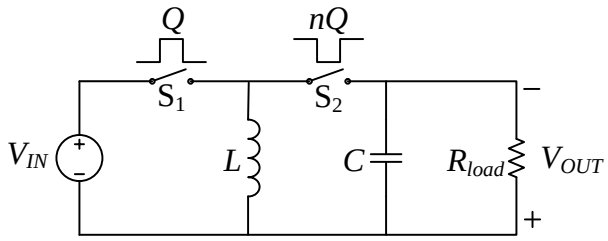

Figure 2.1. Buck-boost voltage converter topology.

The converter shown in Figure 2.1 is classified as an inverting buck-boost converter because the polarity on the output is reversed to that of the input. The converter works on a cyclic basis. Switches S_1 and S_2 alternate being opened and closed with S_2 open while S_1 is closed. During the first phase of each switching cycle, energy is transferred from the source to the inductor L. In the second phase of the switching cycle the energy stored in the inductor is transferred to capacitor C and R_{load}.

At the start of a switching cycle ($t = 0t_T$ s) Q is on and closes S_1. Therefore, nQ is the logical complement of Q and S_2 is open. In the second part of the switching cycle Q is off and S_1 is open. Similarly, nQ is on and switch S_2 is closed. This creates two distinct circuit behaviours. From time $t = 0t_T$ s to $t = Dt_T$ s, S_1 is closed and S_2 is open, allowing power from the DC

source to be passed through inductor L. From time $t = Dt_T\,s$ to $t = t_T\,s$, S_1 is open and S_2 is closed and L is connected capacitor C and a resistive load R_{load}. The currents and voltages in the circuit are shown in Figure 2.2.

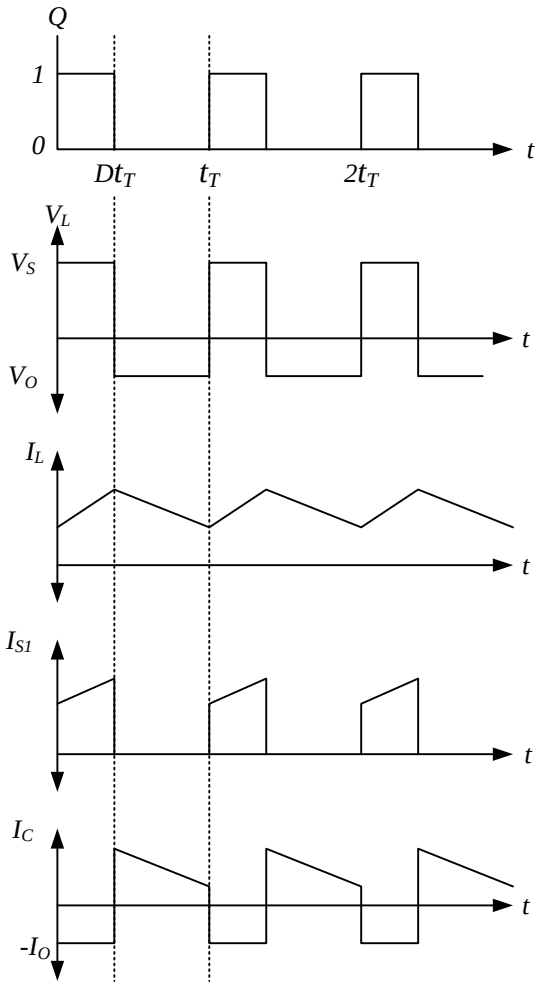

Figure 2.2. Buck-boost converter waveforms.

In Figure 2.2, Q is the switching clock signal which is high for a percentage D of the total switching interval. V_L is a plot of the voltage over the inductor where V_S is the source voltage and V_O is the output voltage. I_L is a plot of the current flowing through the inductor L. The gradient of the current flow is positive as energy is stored in L and negative as L discharges into the load. The current through S_1 is equivalent to I_L when L is charging. S_1 does not conduct when L discharges into the load. I_C is a plot of the current into the load and is equivalent to the discharge current of L. I_O is the output current drawn by the load while L charges.

In the on state with S_1 closed the change in inductor current is given by:

$$\frac{di_L}{dt} = \frac{V_{IN}}{L} \tag{2.1}$$

This leads to a total change in current by $t = Dt_T$ of:

$$\Delta i_{Lon} = \int_0^{Dt_T} di_L = \int_0^{Dt_T} \frac{V_{IN}}{L} dt = \frac{V_{IN} D t_T}{L} \tag{2.2}$$

Where D is the duty cycle of Q and $0 < D < 1$.

Similarly, in the off state with S_2 closed:

$$\Delta i_{Loff} = \int_0^{(1-D)t_T} \frac{V_{OUT}}{L} dt = \frac{V_{OUT}(1-D)t_T}{L} \tag{2.3}$$

2.4.1 Continuous mode

Continuous conduction is defined as the inductor current not being 0 A for any appreciable length of time during the entire switching cycle. By this definition, and assuming a perfect inductor, the total energy entering the inductor for $t = 0t_T$ s to $t = Dt_T$ s must be equal to energy transferred out of the inductor for the remainder of the switching cycle. This is expressed as:

$$\Delta i_{Lon} + \Delta i_{Loff} = 0 \tag{2.4}$$

Substituting (2.2) and (2.3) into (2.4) yields:

$$0 = \frac{V_{IN} D t_T}{L} + \frac{V_{OUT}(1-D)t_T}{L} \tag{2.5}$$

Solving for V_{OUT}/V_{IN} yields:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{-D}{1-D}\right) \tag{2.6}$$

(2.6) shows that the conversion ratio is determined only by the duty cycle D. Varying the value of D allows the output to be larger, smaller, or equal to in magnitude to the input. The effect of D is summarised in Table 2.1. V_{OUT} is expressed as a magnitude because the base buck-boost converter topology is an inverting converter.

Table 2.1 Effect of duty-cycle on V_{OUT}.

Duty cycle	Converter output	Conversion type
$0 < D < 0.5$	$\|V_{OUT}\| < V_{IN}$	Buck
$0.5 < D < 1$	$\|V_{OUT}\| > V_{IN}$	Boost
$D = 0.5$	$\|V_{OUT}\| = V_{IN}$	None

Table 2.1 categorises the conversion behaviour as either buck, boost, or none. When $0 < D < 0.5$, the converter 'bucks' the input voltage such the output voltage is less than the input. For $0.5 < D < 1$, the converter 'boosts' the input voltage such that the output voltage is larger than the input. When $D = 0.5$, the converter neither bucks nor boosts the input and the output voltage is equal to the input.

2.4.2 Discontinuous mode

Discontinuous conduction is defined as an operating mode where the inductor current is 0 A for an appreciable amount of time in the switching cycle. The derivation of a continuous operation assumes energy is transferred continuously through the entire cycle. The derivation of equations of the discontinuous mode must account for the time in the cycle during which there is no conduction. This maximum inductor current with S_2 closed and S_1 open is given by:

$$0 = \frac{V_{OUT}\delta t_T}{L} + \frac{V_{IN}Dt_T}{L} \tag{2.7}$$

Where δ is the differential time that the inductor current is 0 A. The maximum current in the on state with S_1 closed is given by:

$$I_{L_{MAX}} = \frac{V_{IN}Dt_T}{L} \tag{2.8}$$

And the load current I_{OUT} in the off state with S_2 closed is given by:

$$I_{OUT} = \frac{I_{L_{MAX}}}{2}\delta \tag{2.9}$$

Substituting (2.8) and (2.9) into (2.7) allows the output voltage to be expressed as:

$$V_{OUT} = -\frac{V_{IN}D^2t_T}{2LI_{OUT}} \tag{2.10}$$

(2.10) shows that in the discontinuous conduction state, the output voltage is a function of the output current. The discontinuous mode is unable to operate effectively in practice unless the effect of variable I_{OUT} is considered.

Two techniques may be used to account for the dependence on I_{OUT}. The maximum current that can be sourced by the converter can be constrained, allowing for L to be chosen such that the converter does not enter the discontinuous mode. Alternatively, a closed loop controller can be used to modulate the value of D such that the converter remains in the continuous mode.

To keep the converter in continuous mode, the minimum value for L is given by:

$$L_{MIN} = \frac{(1-D)^2 R_{load}}{2f} \tag{2.11}$$

Where f is the switching frequency of the converter in Hz and R_{load} is the effective load resistance seen by the converter for a given output voltage V_{OUT}.

The minimum capacitance required for a desired output voltage ripple, V_r, is given by:

$$C_{MIN} = \frac{DV_{OUT}}{V_r R_{load} f} \tag{2.12}$$

Appropriate choice of L and C will yield a converter which does not enter discontinuous conduction operation if second order and parasitic effects are negligible. However, this is not applicable in practice, and the operation of both continuous and discontinuous modes benefit from external control.

2.5 DC-DC CONVERTER FEEDBACK CONTROL

Two popular techniques for feedback control for buck-boost converters may be classified as either current mode control, or voltage mode control [19]. A simplified topology for each is shown in Figure 2.3.

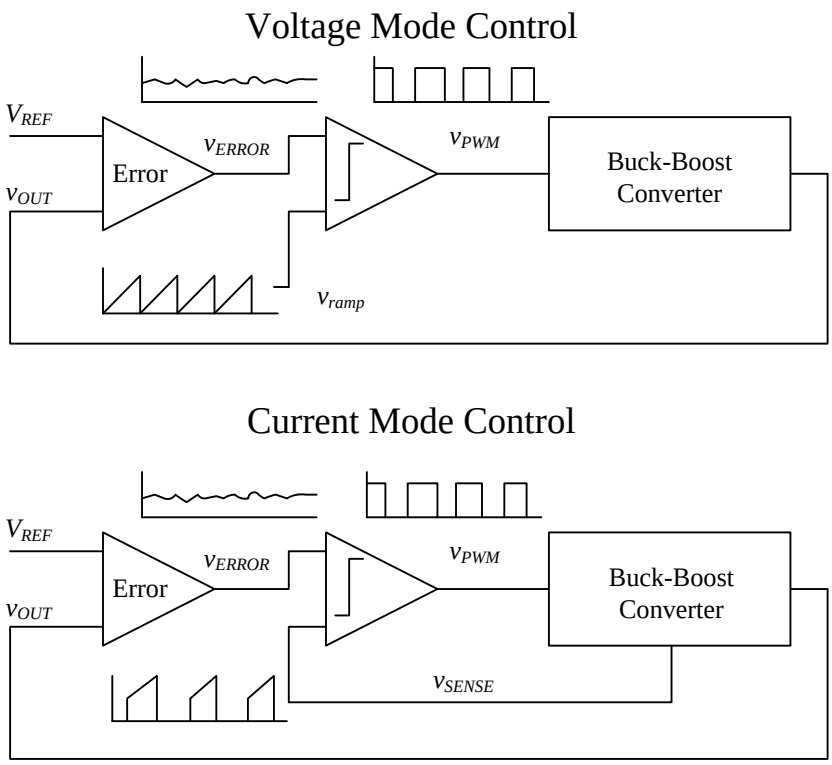

Figure 2.3. Voltage mode control and current mode control topologies.

As in Figure 2.3, voltage mode control (VMC) senses a scaled value of the output voltage which is compared to a reference voltage by an error amplifier. The result, v_{ERROR}, is compared to a fixed ramp which is modulated through a comparator to create the pulse width modulated (PWM) control signal for the converter. VMC benefits from simple implementation both from a hardware and control theory perspective. VMC also provides excellent load regulation, since variations in loading are quickly compensated for by the error amplifier. Line regulation is hampered by changes in the line voltage needing to propagate to the output before being accounted for in the control loop.

Current mode control (CMC) alleviates the delayed reaction to line changes by incorporating a feed forward network, where the input is sensed and forms part of the control network. The current in the inductor is sensed and used to generate the periodic ramp signal required for PWM. This improves the dynamic response of the converter to changes at its terminals at the cost of additional complexity, both in controller design and hardware implementation. Current mode control is well suited to applications with variable input voltage, such as a sensor node in a WSN which is powered through energy harvesting.

2.6 CMOS CONVERTER DESIGNS

There has been extensive research and development of CMOS DC-DC converters. Researchers focus on alternative converter control topology, application specific improvements, and converter optimisation.

2.6.1 Inverting and non-inverting DC-DC converters

DC-DC converters are classified as either inverting or non-inverting. The output of non-inverting DC-DC converters has the same polarity as that of the input relative to the input's ground reference [18]. The output of an inverting DC-DC converter has inverted polarity relative to the input's ground reference. The circuit in Figure 2.1 is an example of an inverting DC-DC converter. The DC-DC converter topology in Figure 2.4 makes use of additional switching to generate a non-inverted output [20].

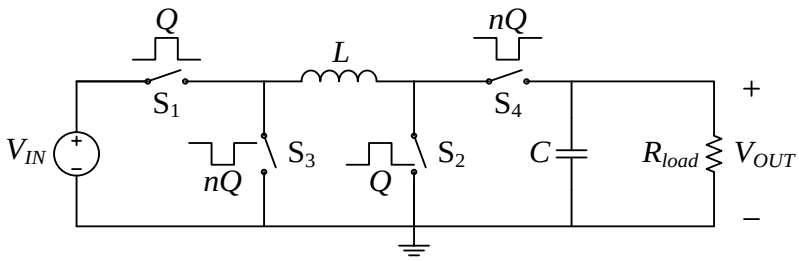

Figure 2.4. Non-inverting DC-DC converter topology.

This DC-DC converter shown in Figure 2.4 uses two additional switches to effectively reverse the polarity of L during the second phase of the conversion cycle. S_1 and S_2 are closed (S_3 and S_4 are open) for the first phase of the conversion, charging L. S_3 and S_4 (S_1 and S_2 are open) are closed for the second phase of the conversion. The output voltage of this non-inverting DC-DC converter is given by:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{D}{1-D}\right) \tag{2.13}$$

This non-inverting design is frequently used in fully integrated designs where the cost and complexity of additional devices is negligible. The non-inverting configuration also allows for a common ground reference between input and output.

2.6.2 Alternative CMOS converter control topologies

An integrated DC-DC converter will often have a single power source, such as a battery or power reservoir, and must efficiently transform the stored energy to the voltage levels required by several different subsystems. Such a system is presented in [21] where a single inductor boost converter drives four low dropout regulators (LDOs). The buck-boost converter may be integrated with other system elements to improve its overall efficiency. Such a design is presented in [22], where the converter topology is combined with a power amplifier to improve overall efficiency by dynamically adjusting converter output as required by the PA.

In mobile applications, there are stringent requirements of DC-DC converters. Power sources such as batteries have variable output voltage which require the converter to have a wide input and output range with good line and load regulation. The portable, compact, or integrated device being powered has multiple power usage modes varying from low to high. The highly variable load must also be accommodated by the converter. These requirements have driven the development of multimode control schemes which offer efficiency over the wide range of input and output conditions [23]. [24] presents a minimum energy tracking loop which actively monitors the converter load and dynamically adjusts the output voltage of the converter to deliver the minimum amount of power.

Analogue control schemes are prevalent in converter designs, with current mode control being used extensively. Analogue control schemes are susceptible to internal variations which influence the closed loop response of the control network. Digitally controlled DC-DC converters have been developed to counter these variations and to introduce additional multimode operation [25].

2.6.3 Integrated CMC converters

The inherent low-cost per device in IC technology counters any cost factors when implementing CMC. The primary disadvantage of CMC is the additional expense associated with the increased complexity of the CMC. This expense is not a limiting factor for integrated implementations.

[26], [27], and [20] present typical CMC based DC-DC converters with the control loop implemented with rudimentary analogue circuits and sensors. Figure 2.5 shows a generalised integrated buck-boost converter with analogue CMC control.

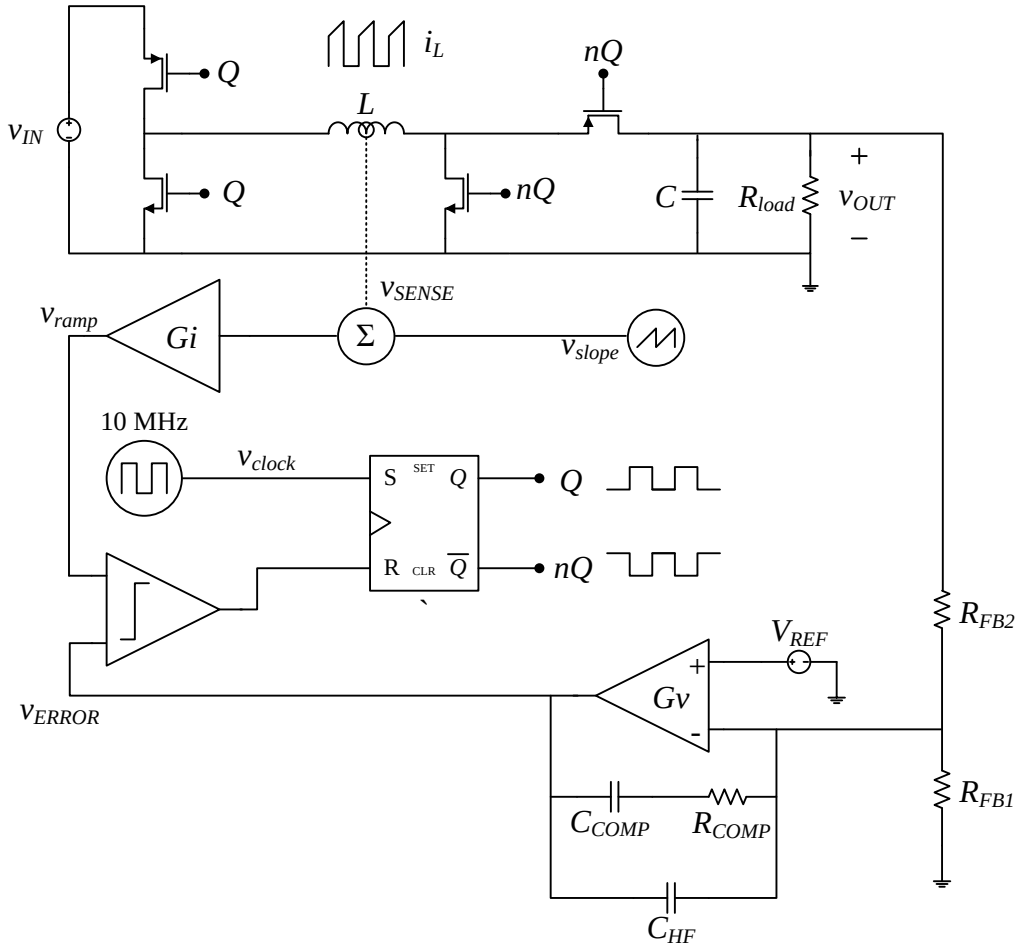

Figure 2.5. Generalised non-inverting buck-boost converter with analogue current mode control.

The simplified CMC topology of Figure 2.3 has been expanded in Figure 2.5 to show the primary circuits required for an IC implementation. The DC-DC converter by [28] improves on the typical designs by identifying the internal CMOS current sensor, which converts the inductor current to a scaled sensed voltage, as one of the circuits which can be improved to increase overall efficiency. The converter is implemented in a 0.6 µm process with a maximum input of 5.2 V.

Chapter 4 demonstrates that these designs – which are effective in their respective technology nodes – become ineffective when scaled down to 130 nm. The techniques used in these implementations need to be updated or changed to maintain functionality.

2.7 CMOS BASED CURRENT SENSING

Current sensing circuits range from simple passive networks to active current sensor sensors. A summary of common sensor types is presented in [29]. The purpose of these circuits is to measure the current in the converters inductor. Current sensing circuits perform either a direct measurement of the current in the inductor or infer the current through indirect measurement of another circuit parameter.

2.7.1 General current sensing techniques

The circuit in Figure 2.6 uses the most rudimentary form of current measurement by placing a resistor R_{SENSE} in series with the inductor.

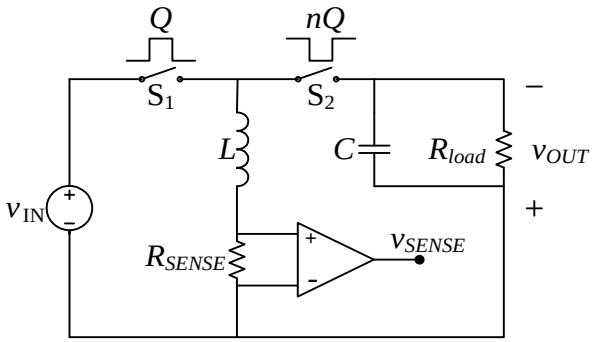

Figure 2.6. Rudimentary current sensing network.

The current in the resistor will be the same as that of the inductor and the sense current can be converted to a voltage (v_{SENSE}) by applying Ohm's Law to the voltage drop over R_{SENSE}. The primary disadvantage of this technique is that in each switching cycle power is lost through R_{SENSE}, which loads the converter and reduces the overall efficiency. To circumvent this power loss, lossless current sensing techniques have been developed.

In integrated switch mode converters, switches S_1 and S_2 in Figure 2.6 are implemented with power transistors. This integration allows the on resistance of the device to be used to replace R_{SENSE} without introducing additional losses. This technique is inexpensive, but inaccurate, as the device on resistance is susceptible to PVT variations [30].

There are several techniques which infer the inductor current by measuring the voltage across the inductor L with varying degrees of accuracy. The simplest approach is to have a series RC network in shunt with the inductor, as shown in Figure 2.7. If the effective series

resistance (ESR) of the inductor *L* and the inductance of L are known, then the inductor current can be determined for appropriate values of R_f and C_f [31].

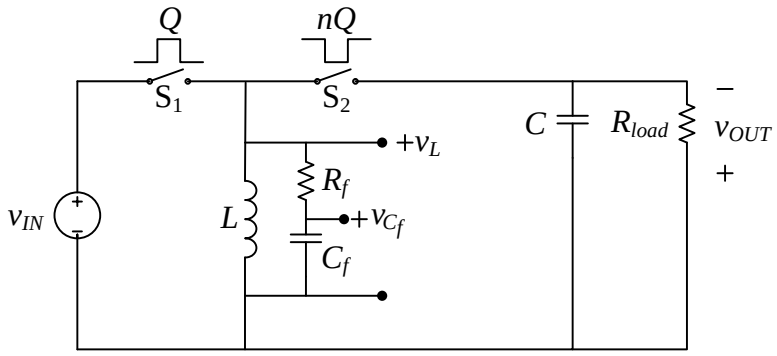

Figure 2.7. Voltage filtering network in shunt with converter inductor.

The technique employed by the circuit of Figure 2.7 relies on the designer knowing the characteristics of the inductor used in order to select R_f and C_f. Integrated switch mode converters which are not designed for a specific value of L would also need R_f and C_f to be selected. Additionally, the accuracy of this technique is susceptible to variation in component values. This limitation is overcome by integrated circuits which measure the inductor value and the inductor effective series resistance (ESR) [9]. A DC-DC converter that is able to measure the value of the power inductor used can adapt the converter control loop to provide accurate control.

Sensorless current sensing techniques, such as those employed by [32], determine the current in the inductor by integrating the differential voltage over the inductor. This technique is shown in figure and directly applies the current voltage relationship for inductors given by:

$$i_L = \frac{1}{L}\int_{t_0}^{t_1} v_L(\tau)d\tau + i_L(t_0) \qquad (2.14)$$

With t_0 to t_1 the period over which the current is being sensed. $i_L(t_0)$ is the initial current value.

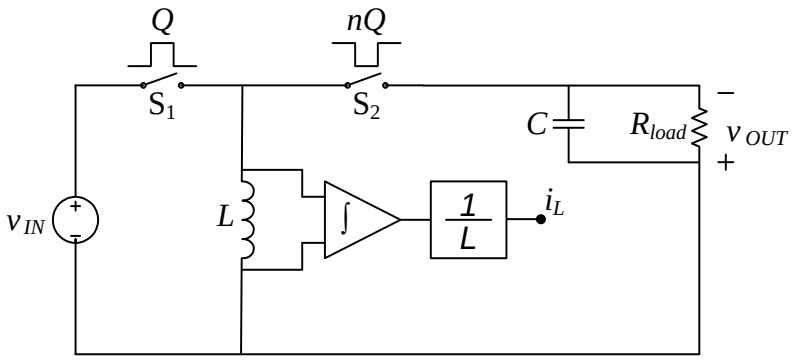

Figure 2.8. Sensorless current sensing circuit.

The application of (2.14) requires, in Figure 2.8, the value of L to be known, which is practically cumbersome for integrated circuits, and is also susceptible to variations in the value of L.

2.7.2 Integrated current sensing – The SenseFET

In CMOS applications where the switches in the DC-DC converter are implemented with integrated power transistors on the same die as the integrated controller, the SenseFET[5] approach to current sensing offers many advantages [29].

The SenseFET fundamental circuit is shown in Figure 2.9.

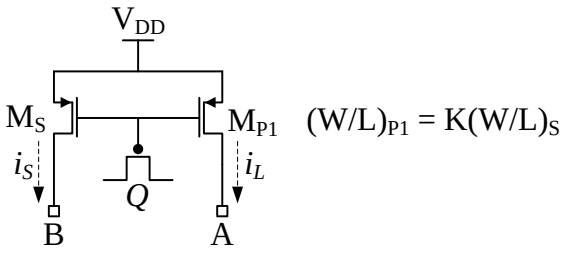

Figure 2.9. Fundamental SenseFET circuit.

In Figure 2.9, the aspect ratio of M_{P1} is chosen to be much larger than that of M_S, effectively negating the power consumption of M_S. The gates of M_S and M_{P1} are driven by the same signal. In a DC-DC converter application, the gates are driven by the converter's internal switching signal.

[5] SenseFET is a concatenation of the word sense and the abbreviation for field effect transistor (FET).

If the voltage at nodes A and B is held constant, and ideal transistors are assumed to be operating in saturation, then the current i_S is given by:

$$i_S = \frac{k_p'}{2}\left(\frac{W}{L}\right)_S (v_{GS} - V_t)^2 \text{ and } i_L = \frac{k_p'}{2} K \left(\frac{W}{L}\right)_S (v_{GS} - V_t)^2 \tag{2.15}$$

$$i_S = \frac{i_L}{K} \tag{2.16}$$

The gates of M_S and M_{P1} driven by the same signal source and the devices only differ in aspect ratio. This configuration results in i_S being a scaled version of i_L by (2.15) and (2.16).

A simple SenseFET implementation is shown in Figure 2.10. The opamp is used to equalise the drain voltages of M_S and M_{P1}.

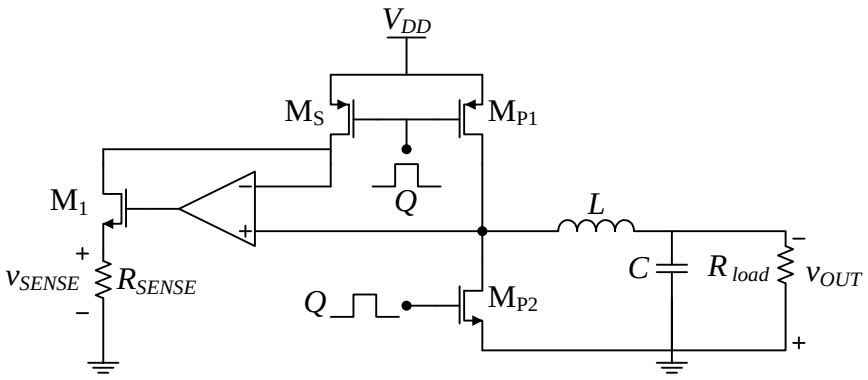

Figure 2.10. Simple SenseFET implemented with idealised components.

The circuit in Figure 2.11 is also commonly used [28]. Transistor pair M_1 and M_2 form a simple differential amplifier. M_2 provides biasing for M_1. The gates of M_{1A} and M_{1B} are connected and M_{1B} is diode connected.

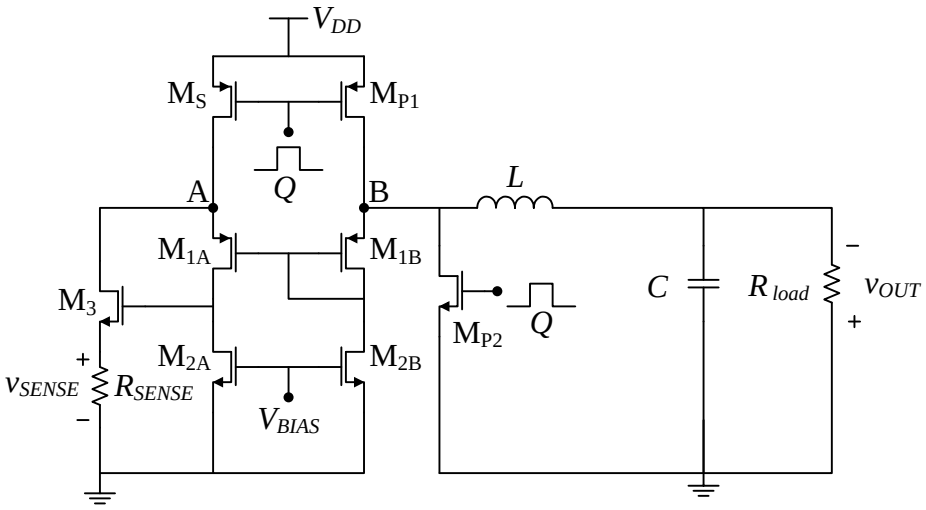

Figure 2.11. SenseFET implemented with a greatly simplified amplifier.

If all transistors are assumed to be ideal, then on every cycle circuit operation is given by applying Kirchhoff's Current Law (KCL) at nodes A and B:

$$i_{DSM_{P1}} = K i_{DSM_S} \tag{2.17}$$

$$i_L = i_{DSM_{P1}} - i_{DSM_{1B}} \tag{2.18}$$

$$i_{DSM_3} = i_{DSM_S} - i_{DSM_{1A}} \tag{2.19}$$

Since (2.20)

$$i_{DSM_S} = \frac{i_L + i_{DSM_{1B}}}{K} \tag{2.21}$$

$$i_{DSM_3} = \frac{i_L}{K} + \frac{i_{DSM_{1B}}}{K} - i_{DSM_{1A}} \tag{2.22}$$

$$i_L \gg i_{DSM_{1B}} \tag{2.23}$$

From Ohm's Law

$$v_{SENSE} = R_{SENSE} i_{DSM_3} \tag{2.24}$$

$$v_{SENSE} \approx R_{SENSE} \left(\frac{i_L}{K} - i_{DSM_{1A}} \right) \tag{2.25}$$

Whereas in Figure 2.9, K is the scaling factor applied to the aspect ratio of M_{P1} in terms of M_S. The derivation of v_{SENSE} in (2.25) assumes and ideal device with negligible second order effects. v_{SENSE} is thus only a function of i_L, with R_{SENSE}, K, and i_{DSM1A} constants.

(2.17) to (2.25) are derived assuming the current through a transistor from source to drain (i_{DS}) in saturation is given by:

$$i_{DS} = \frac{k'}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \tag{2.26}$$

Where:

k'	Process transconductance parameter
$\left(\frac{W}{L}\right)$	Transistor aspect ratio
v_{GS}	The gate source voltage
V_t	Device threshold voltage

The inclusion of channel modulation effects to (2.26) results in:

$$i_{DS} = \frac{k'}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \tag{2.27}$$

Where v_{DS} is the drain source voltage and λ is a process parameter representing the effect of channel length modulation in i_{DS}. This inclusion significantly effects the derivation of v_{SENSE} in terms of i_L. The effect of channel length modulation on SenseFET performance is considered in Chapter 4.

2.7.3 Improved SenseFETs

Application specific improvements to the standard SenseFET design are prevalent in literature. Improvements address the basic SenseFET circuit topology by increasing measurement bandwidth, increased linearity, low-voltage operation, and to combat process specific parameters. In the concluding section of this Chapter summarises contributions from the literature and contextualises the work in this dissertation.

2.8 TECHNOLOGY SHORTCOMINGS

The characteristics of the CMOS process which has been utilised need to be accounted for in the integrated circuit design. The available low-voltage process through the MOSIS program is the IBM 8HP BiCMOS process at the 130 nm technology node. The maximum allowable voltage in this process is below that of technologies used in the literature. This subsection discusses the predominant process and device characteristics which influence the work in this dissertation.

2.8.1 Channel length modulation

The idealised large-signal model of a field effect transistor (FET) operating in saturation has the drain to source current, i_{DS}, given by (2.26). Assuming a linear device, i_{DS} when the transistor is operating in the triode region is given by:

$$i_{DS} = \mathrm{k}'\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \tag{2.28}$$

A plot of i_{DS}-v_{DS} for the idealised large signal model is shown in Figure 2.12.

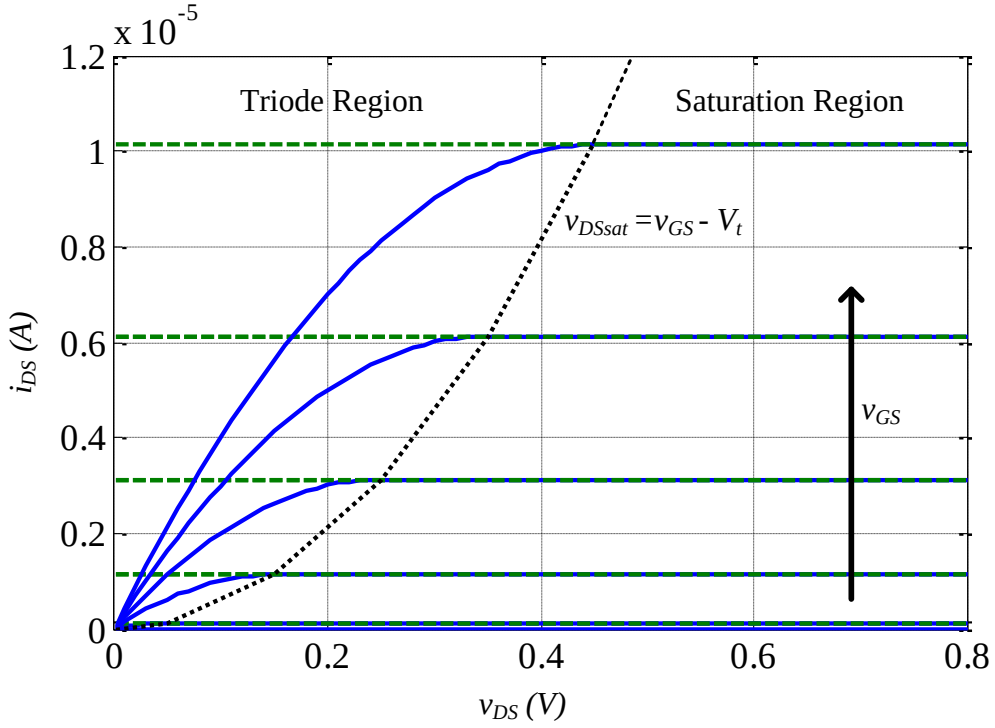

Figure 2.12. Idealised i_{DS}-v_{DS} characteristic curves.

In Figure 2.12 the value of i_{DS} in saturation has been extrapolated to illustrate that the i_{DS}-v_{DS} gradient in saturation is 0. This model also assumes an infinite output resistance. The basis of this assumption is that once $v_{DS} = v_{DSsat}$ further increases in v_{DS} has no physical effect on the conduction channel of the FET. The output resistance in saturation is defined by the i_{DS}-v_{DS} gradient in saturation with constant v_{GS} or:

$$r_O = \frac{\Delta v_{DS}}{\Delta i_{DS}} \tag{2.29}$$

Since increasing v_{DS} beyond v_{DSsat} in saturation does not affect i_{DS}, r_o must be infinite [33].

In practice the idealised large signal model is inadequate because an increase in v_{DS} beyond v_{DSsat} physically effects the conduction channel in the FET. Increasing v_{DS} beyond v_{DSsat} modulates the channel length, causing i_{DS} to vary with v_{DS} in saturation. The significance of channel length modulation in a target process should be considered when developing circuit designs. Channel length modulation is modelled by including a weighting factor of $(1+\lambda v_{DS})$ as in (2.27). Figure 2.13 illustrates the effect of severe channel length modulation on the i_{DS}-v_{DS} characteristic curves.

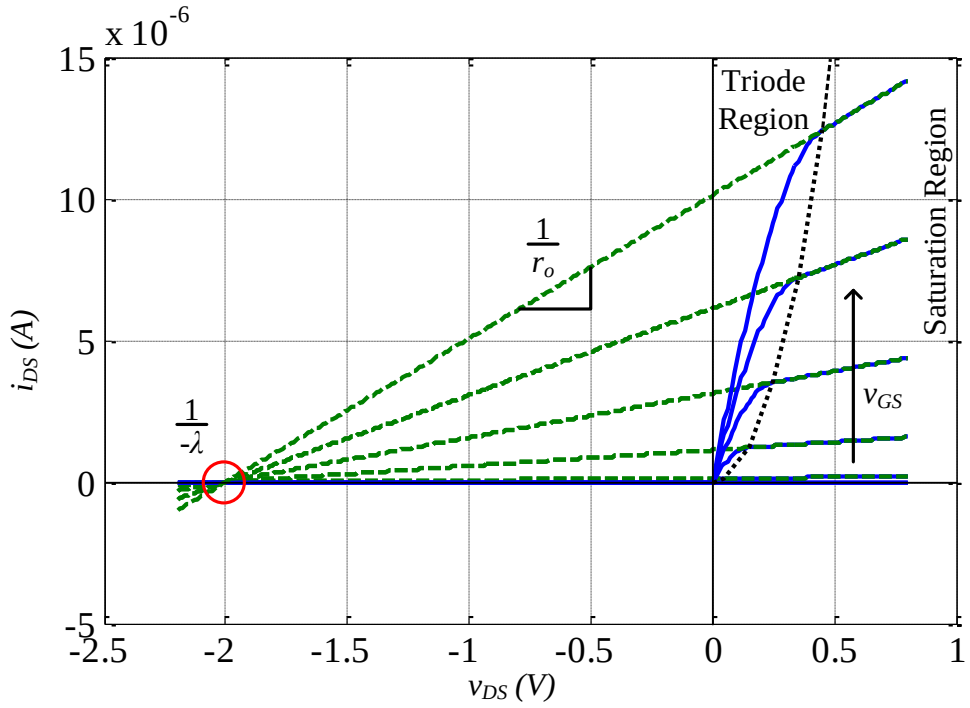

Figure 2.13. i_{DS}-v_{DS} characteristic curves with channel length modulation incorporated.

In Figure 2.13 the value of i_{DS} has once again been extrapolated to illustrate effect of channel length modulation, which introduces a finite output resistance r_o. r_o may behave dynamically in circuits where i_{DS} and v_{DS} fluctuate. The output resistance is defined by:

$$r_O = \left[\lambda \frac{k'}{2}\frac{W}{L}(v_{GS} - V_t)^2\right]^{-1} \tag{2.30}$$

$$r_O \simeq [\lambda I_{DS}]^{-1} \tag{2.31}$$

$$r_O \simeq \frac{V_A}{I_{DS}} \; with \; V_A = \frac{1}{\lambda} \tag{2.32}$$

V_A is a process parameter referred to as the Early voltage. I_{DS} is the instantaneous DC drain to source current for a fixed V_{DS} and V_{GS}. In practice the determination of V_A is difficult and is usually derived from experimental data [30].

Figure 2.14 illustrates a simple CMOS differential amplifier with active load.

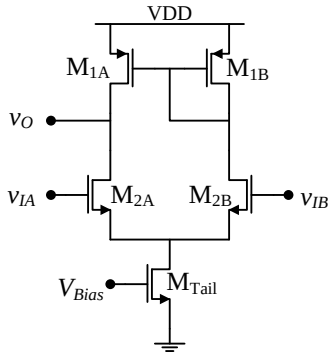

Figure 2.14. Simple CMOS differential amplifier with active load.

The large-signal gain of the differential pair M_2 is given by:

$$A_{M_2} = -g_m\left(r_{oM_1} || r_{oM_2}\right) \tag{2.33}$$

Where $r_o = \frac{V_A}{I_{DS}}$ and

$$g_m = \frac{k_n^`}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)(1 + \lambda v_{DS}) \tag{2.34}$$

(2.33) and (2.34) are both functions of V_A with (2.33) being a strong function of i_{DS}. This dominance manifests as an unbalanced operation of the differential pairs, as variance in i_{DS} causes the small-signal and large-signal parameters of the transistors to vary with i_{DS}.The effects of V_A on circuit performance is discussed further in Chapter 4 of this dissertation.

2.8.2 Velocity saturation

The average horizontal electric field in a FET device is V_{DS}/L [30]. At low field strengths, the relationship between field strength and carrier velocity in the transistor is linear. As field strength increases, either by increasing V_{DS} or decreasing L, the carrier velocity does not increase, however, rather approaching the scattering-velocity limit.

If the horizontal electric field is small, the drift velocity is given by:

$$v_d(y) = \mu_n E(y) \tag{2.35}$$

$$E(y) = \frac{dV}{dy} \tag{2.36}$$

Where *E(y)* is the horizontal electric field, *y* is the axis along the length of the device from source to drain, *dV* is the incremental voltage drop along *dy*, and μ_n is the average electron mobility. (2.35) shows that the v_d behaves linearly with *E(y)*.

At higher field strengths, this linear relationship is no longer valid and the drift velocity is instead approximated by:

$$v_{dsc} \approx \frac{\mu_n E}{1 + \frac{E}{E_c}} \tag{2.37}$$

Where E_c is the critical field value with $E_c \approx 1.5\times10^6$ V/m.

The plot in Figure 2.15 is of (2.35) and (2.37).

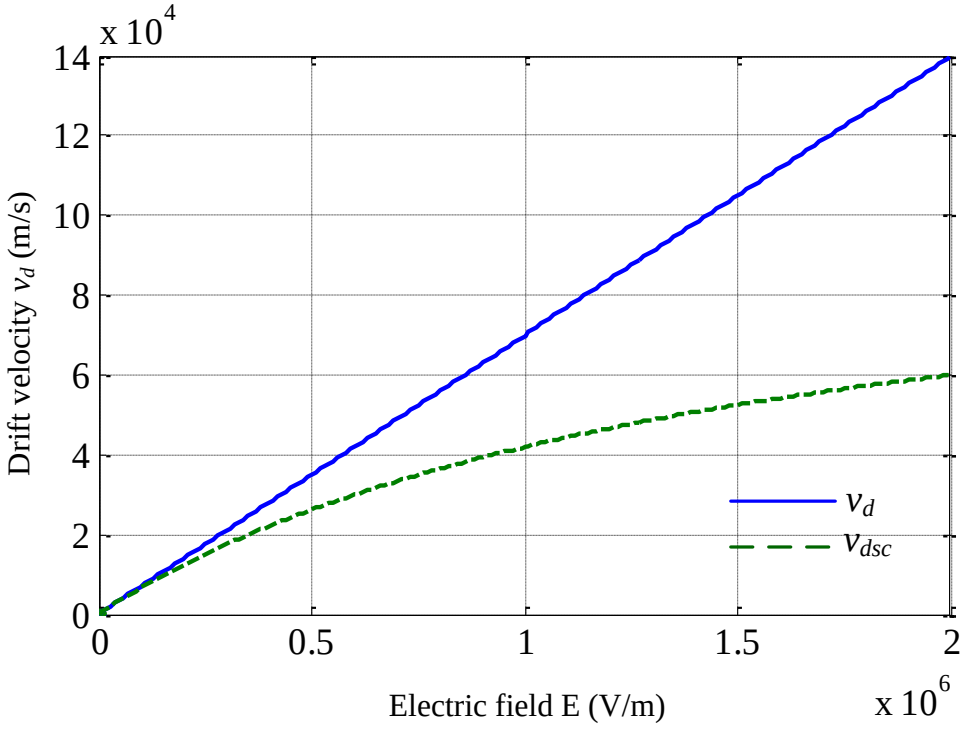

Figure 2.15. Electron drift velocity for linear and approximate models.

In Figure 2.15 it can be seen that for low electric field strength ($E < 2\times10^5$) the linear approximation of v_d agrees with v_{dsc}. At higher field strengths, the linear approximation is no longer accurate. At a field strength of $E = 1.5 \times 10^6$ V/m, the drift velocity predicted by the linear approximation of (2.35) is nearly double that of the more accurate prediction of (2.37). In a process with a gate length of 130 nm, applying (2.36) show that $v_{DS} > 200$ mV is enough to generate an electric field larger than the critical field value E_c.

From [30], I_{DS} in the triode and saturation regions (assuming fixed V_{DS}) is given by:

$$i_{DS} = \frac{k'_n}{2\left(1+\frac{v_{DS}}{E_c L}\right)}\frac{W}{L}[2(v_{GS}-V_t)v_{DS}-v_{DS}^2] \tag{2.38}$$

$$I_{DS} \cong \frac{k'_n}{2\left(1+\frac{v_{GS}-V_t}{E_c L}\right)}\frac{W}{L}(v_{GS}-V_t)^2 \tag{2.39}$$

With (2.38) applying to the triode region and (2.39) applying to the saturation region.

The overall effect of velocity saturation is that it reduces the expected drain-source current in the device as predicted by (2.27) and (2.28). In devices with short channel lengths this effect becomes more pronounced as the electric field strength increases as channel lengths become shorter.

2.8.3 Low-voltage limitations

In low-voltage processes such as the IBM 8HP 130 nm BiCMOS process, analogue circuits must be able to operate with a low voltage supply rail to prevent voltages in the circuit from exceeding the oxide breakdown voltage of each device. This low-voltage limitation restricts available headroom for cascaded designs. Low-voltage processes also have reduced device thresholds voltages (V_t) which can increase static power dissipation [34]. Designing for low-voltage requires the application of more complex circuits using folded structures [30] or new design approaches that make use of FETs that operate in the sub-threshold ($v_{DS} \ll V_t$) region [35].

2.8.4 Other device limitations

The process utilised in this study is primarily affected by channel length modulation and low operating voltage. These are not the only short channel effects (SCEs) which degrade the performance of FET devices with sub-micron and deep sub-micron gate lengths. Strong electrical fields in the vicinity of the device gate, and thinner oxide layers as technology scales down has resulted in gate leakage or tunnelling currents becoming significant [30],

[36]. The device design is complicated when scaling down for a lower supply voltage by the non-scaling Si bandgap potential. Thus, device design choices which account for the bandgap potential tend to increase V_t when it is preferred to have a lower V_t [36].

2.9 CMOS CASCODE TECHNIQUES

CMOS processes with sub-micron gate lengths are susceptible to significant channel length modulation [34]. (2.30) - (2.32) show that the increased prevalence of channel length modulation decreases the finite output resistance. In analogue amplifier stages, the output resistance, $g_m r_o$, is a key parameter in determining the large- and small-signal gain of the amplifier. $g_m r_o$ Can be increased by using active load cascodes which effectively multiply $g_m r_o$ [30]. The cascoding technique vertically stacks additional active load devices in an amplifier to increase gain. Figure 2.16 expands the simple differential amplifier of Figure 2.14 to include a cascoded active load.

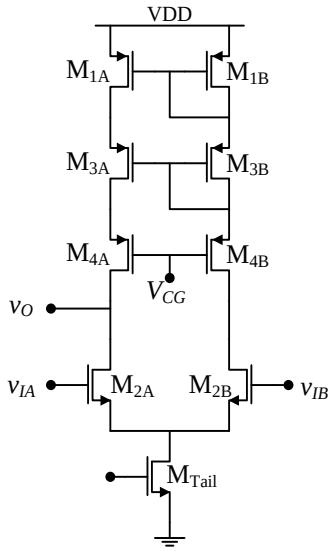

Figure 2.16. Simple CMOS differential amplifier with active load employing cascoded stages.

The primary disadvantage of this technique is reduced headroom as M_1, M_3, and M_4 introduce an additional v_{DS} drop over M_3 and M_4. This is problematic in CMOS processes which already have a low operating voltage. The reduction in headroom can be remedied by using folded cascode techniques, which collapse the vertical stack formed by M_1, M_3, and M_4 into alternating PFET and NFET devices. The collapsed or folded stack can be made as deep as required without introducing an additional v_{DS} drop for each cascode stage. This technique is considered in Chapter 4.

2.10 RESEARCH CONTRIBUTION

The research hypothesis and research questions developed from the literature attempt to address untested applications of SenseFET ICs in a low-voltage BiCMOS implementation. The literature is surveyed to identify these areas of incomplete knowledge. Table 2.2 summarises the fabrication nodes and sensing topology used by several published sources.

Cimno [37] presents a current sensing topology at a relevant technology node but uses a non-switching topology unsuited to the current magnitudes present in an integrated DC-DC converter. Forghani-zadeh [9] applies a completely different current sensing topology which characterises the inductor used and provides insight into lossless sensing in DC-DC converters. Du [7], Rao [10], and Lee [28] each use a different approach to approximate the ideal operation of the fundamental SenseFET but do not address low-voltage operation. These published works only partially provide insight into SenseFET behaviour at low-voltage in a submicron process. This work attempts to expand on the application of SenseFET topologies in low-voltage submicron technologies.

Table 2.2. Summary of contributions of relevant literature.

Reference	Journal	Impact factor	Fabrication node (µm)	Maximum Voltage (V)	Sensing topology	Primary contribution
Cimino [37]	*Journal of Electronic Testing*	0.519	0.6 0.13	3.3 1.2	Radiometric SenseFET	Presents a variant of the SenseFET topology migrated to a 130 nm process from a 600 nm process. Utilises a single cascode and longer channels to counter channel modulation. This design is not suitable for buck-boost converters.
Du [7]	*IEEE Transactions on Circuits*	2.403	0.35	3	SenseFET with dynamically biased shunt feedback	Enhances the classical SenseFET by increasing the bandwidth and DC loop-gain of the sensing circuit to allow for high frequency operation.
Rao [10]	*International Journal of Electronics*	0.459	0.25	4.7	SenseFET with common gate cascade	Introduces a common gate amplifier into each branch of the classic SenseFET to increase loop gain such that ideal operation is approximated.
Forghani-zadeh [9]	*IEEE Journal of Solid-State Circuits*	3.009	0.5	3.5	Self-Learning CMOS current sensing Scheme	Characterises the power inductor used in a converter during start-up and uses this characterisation to perform an accurate and lossless current measurement.
Lee [28]	*IEEE Journal of Solid-State Circuits*	3.009	0.6	5.2	SenseFET with integrated feedback opamp	Utilises an opamp to force the voltage in each branch of the SenseFET fundamental circuit to the same voltage.
Naudé [11]	*Microelectronics International*	0.519	0.13	1.2	Folded Cascode SenseFET	Utilises folded cascode techniques to increase loop-gain and introduce immunity to channel modulation effects.

2.11 CONCLUSION

This Chapter provides an overview of literature and concepts that have been consulted for this dissertation. Phase one of the methodology focuses on problem definition, or defining the hypothesis, and relevant research questions. The literature study forms the core of this process. The information in this Chapter also forms the theoretical basis of the work presented in subsequent Chapters.

Distributed sensor networks, or WSNs, and their classification are discussed. The distinction between structured and unstructured networks is defined and the general requirements of a WSN and the sensor nodes that comprise them are discussed. Various methods of providing power to sensor nodes are surveyed with energy harvesting from the sensor's environment as the leading candidate for long term autonomy. The structure of a sensor node in a WSN is detailed with a focus on internal power circuits.

DC-DC converter fundamentals are briefly examined in order to define the application area of the hypothesis. DC-DC converters implemented in IC technology are reviewed to expand upon this definition, by expanding on the issues of implementation and performance. Internal current sensing is identified as an area of improvement, and where there is potential research value. A survey of integrated and discrete current sensing is presented.

Technological limitations of the target technology are discussed, with emphasis on the dominant influence of channel length modulation over other SCEs. Low-voltage operation of ICs and general design problems associated with low-voltage design are discussed. Finally, the techniques which can be used to address these limitations are briefly described.

CHAPTER 3 METHODOLOGY

3.1 CHAPTER OVERVIEW

Section 1.5 in Chapter 1 briefly describes the methodology used to define the hypothesis and research questions, the approach used to develop the environment in which these ideas could be tested and iterated on, as well as the prototyping and testing phase during which the hypothesis is practically tested. Chapter 2 contextualises the work in this dissertation against relevant published work, presenting a survey of the literature. Chapter 2 furthermore presents the concepts from the literature which have been utilised to both define this study's hypothesis and test it.

This Chapter presents and elaborates on the research methodology applied in this dissertation. The application of concepts identified in Chapter 2 are presented, alongside the description of the software tools which were used to model and test the hypothesis. The software and hardware used to develop and test a prototype are presented and explained, including a brief overview of the technology used to create the prototype.

3.2 RESEARCH METHODOLOGY OVERVIEW

Figure 1.2 is reproduced in Figure 3.1 for ease of reference. Figure 3.1 depicts a flow diagram of the methodology used to develop the hypothesis, the outline of a process for testing the hypothesis, and the implementation of a hardware prototype for assessment.

Tasks are grouped into one of three phases with each phase culminating in an outcome which is considered to be the collective goal of the grouped tasks. Phase one is a grouping of tasks that need to be completed in order to define a hypothesis and research questions. The tasks in phase two focus on applying the concepts reviewed in the literature to develop an analytical and simulation model which forms the basis of a hardware prototype. Phase three focuses on developing a prototype to be assessed in a test environment in order to test the hypothesis.

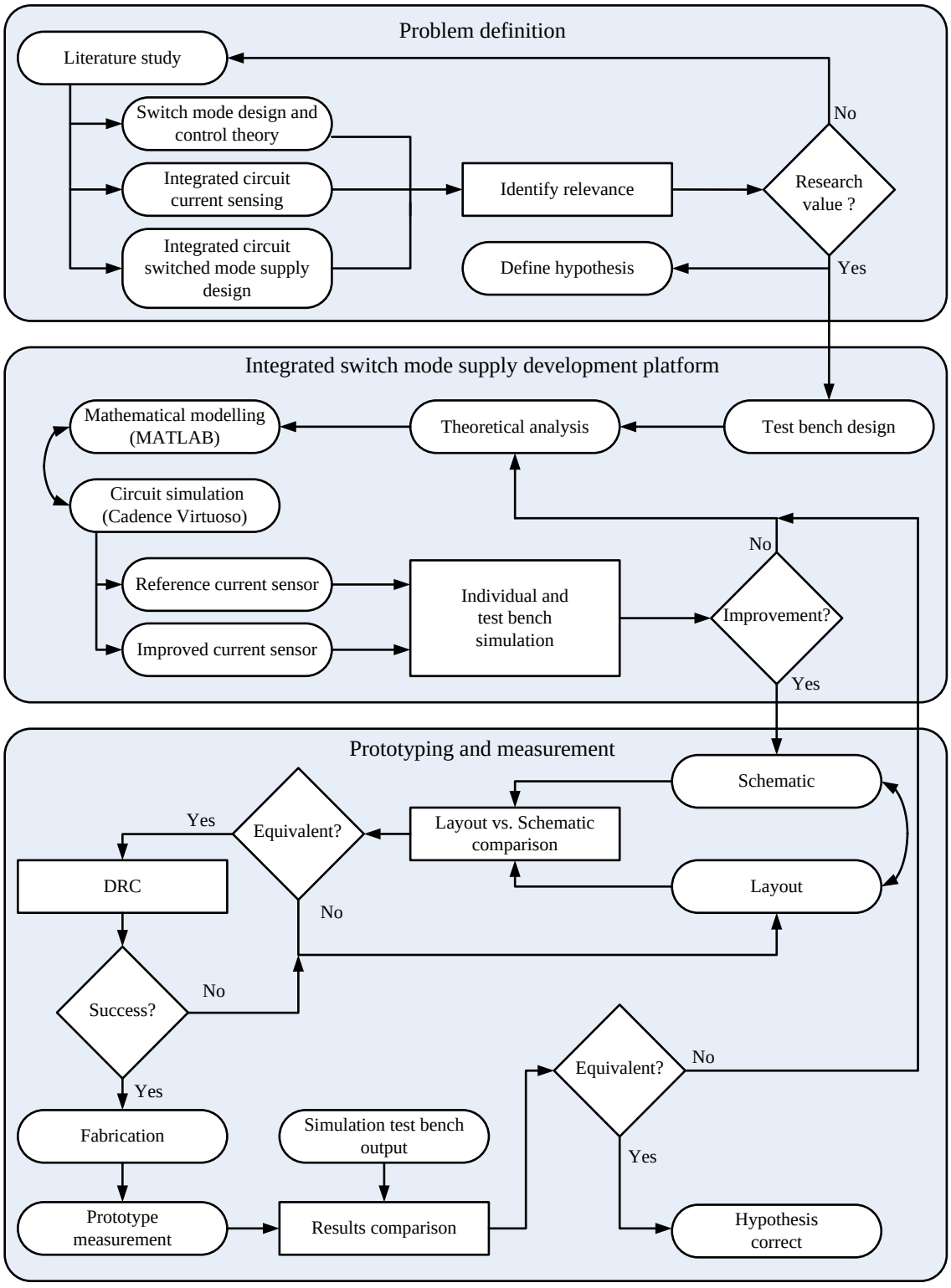

Figure 3.1. Research methodology flow diagram.

3.3 RATIONALE

This methodology is structured to allow for rapid iteration and testing in a computational environment before committing to a hardware prototype. Analytical concepts are tested numerically and in high level simulation, allowing for the design space surrounding the hypothesis to be explored. The iterative nature of transferring a design from numerical to simulation and simulation to hardware prototyping environments is time consuming. This methodology allows for effort to be expended on viable solutions.

3.4 PROBLEM DEFINITION AND LITERATURE STUDY

The initial phase of the research methodology constitutes the literature study and problem definition. These form the basis of the following phases, not only as a firm knowledge base, but also as a reference for further investigation during the research process. The literature study has the following four objectives:

1. To gain an understanding of integrated power supply design in the context of a sensor node in a WSN;
2. To examine the body of knowledge on integrated power supply design to identify shortcomings or problematic factors faced in design and implementation;
3. To isolate an area where knowledge is lacking and develop a hypothesis with research value. For this work, linear low-voltage current sensors are identified as this area;
4. To explore the body of knowledge and to develop experiments to identify and characterise shortcomings of current designs, identify and test improvements, and to test the hypothesis.

The literature study of Chapter 2 led to the development of the hypothesis and research questions as stated in Section 1.2. To approach the hypothesis and research questions, a reference SenseFET, an improved SenseFET, and a test bench for consistent testing are necessary.

3.5 TECHNOLOGY

In addition to outlining current sensing techniques used, the literature study identifies a CMOS technology node suitable for the research in this dissertation. A sensor node in a WSN should be fabricated using an inexpensive process that can operate at low power. The literature does not present significant work at the sub 1.2 V power range in deep sub-micron

CMOS processes. The IBM BiCMOS 8HP 130 nm process node satisfies these requirements within the possible parameters of a research contribution, which are contextualised in Table 2.2. Table 3.1 provides the basic technology features of this process which not covered by the non-disclosure agreement (NDA)[6] with MOSIS.

Table 3.1 IBM BiCMOS 8HP 130 nm process features.

Feature	**Value**	**Detail**
V_{DD}	1.2 V	1.2 V is chosen to be safely within the maximum allowable supply voltage
V_{DDMAX}	1.6 V for thin oxide 2.7 V for thick oxide	V_{DDMAX} is the maximum allowable supply voltage. Thick oxide FETs have a higher allowable V_{DDMAX}.
Operating temperature range	-55 °C to 125 °C	Minimum to maximum operating temperature range
Minimum feature size	120 nm (gate only)	120 nm is the smallest lithographic feature possible in the process
Metallisation	5, 6, 7	The process supports 5 – 7 metal layers but foundry requirements are for 7 layers only

Table 3.1 provides broad design constraints for fabrication based on process limitations. Additional constraints and process parameters are derived from the process models provided by IBM through MOSIS.

3.6 ANALYSIS, MATHEMATICAL MODELLING, AND CHARACTERISATION

3.6.1 Analysis

Preceding mathematical modelling and simulation, the DC-DC converter was identified as a test bench and the fundamental SenseFET circuits were analysed from first principles to form the analytical framework for further development. This analysis not only facilitates the

[6] MOSIS only releases process information to customers who agree to the NDA, which requires process information to remain confidential. The work in this dissertation is subject to the NDA with MOSIS. Confidential information is withheld to prevent it entering the public domain with this document.

understanding of the circuits identified to test the hypothesis, but also provides insight into potential problems and their solutions.

A first order analysis (assuming ideal devices) is performed to formalise the ideal circuit operation. The first order analysis is followed by a more detailed analysis which considers dominant second order and non-linear effects. A comparison of first and second order analyses assists in identifying which factors cause a deviation from ideal circuit operation. Analytic expressions for the DC-DC converter and SenseFET have been introduced in Chapter 2, and are expanded upon with a more in-depth analysis in Chapter 4.

3.6.2 Mathematical modelling and computational evaluation

Analytical expressions for the fundamental SenseFET circuit and test DC-DC converter are used to create scripts in MATLAB which numerically evaluate the analytical expressions. Numerical evaluation allows rapid iteration of design expressions and facilitates the generation of graphical representations of an expression's behaviour.

Designing a non-inverting buck-boost converter with CMC requires the iterative evaluation of several equations and bode plot analysis. Modelling in MATLAB allows for rapid iteration and calculation of the circuit design parameters required for device level design. Similarly, analysis of second order device effects on the fundamental SenseFET design can be graphically analysed.

The Virtuoso schematic editor from Cadence is used for device and gate level schematic design and analysis. Virtuoso allows schematic designs to be computationally analysed using detailed device models provided by MOSIS for the IBM BiCMOS 130 nm 8HP process. Schematic designs are compared and evaluated against the developed mathematical models. Iterative feedback is used to verify the validity of mathematical models and the design choices that were derived from the outcome of numerical analysis.

Once the analytical, numerical, and computational models had an acceptable level of similarity, a virtual test bench was constructed within Virtuoso in which different SenseFET topologies could be instanced and thoroughly tested. Chapter 4 elaborates on how the numerical models were scripted and the analysis of the results, and expands upon the concept of computational analysis using Virtuoso.

3.6.3 Device characterisation

MOSIS provides process parameters at specific operating points for the IBM 130 nm 8HP process. The work in this dissertation operates at a distinctly different operating point, with lower currents and near minimum gate length. For this reason, the device models used in Virtuoso need to be characterised. This characterisation allows relevant process parameters to be used during design and testing of a SenseFET circuit and test bench, which may then be used to test the stated hypothesis.

Velocity saturation and channel length modulation are prevalent in processes with gate lengths in the sub-micron range. The effective gate length of 120 nm is a strong indicator that these effects must be taken into consideration in the early stages of development. Channel length modulation is characterised by V_A for a FET operating in saturation. This parameter is not provided and varies with operating point. For a specific operating point, this parameter can be determined by applying the principles set out in Section 2.7.1. Constructing the i_{DS}-v_{DS} characteristic curves as in Figure 2.13 for both NFET and PFET devices using the detailed foundry models allows V_A to be determined. The characterisation of NFET and PFET devices is presented in Chapter 4.

3.7 SCHEMATIC SIMULATION

Simulation program with integrated circuit emphasis (SPICE) is a software tool for describing and simulating circuits. The Virtuoso schematic editor generates a netlist describing the circuit in SPICE format, which can be imported into a SPICE simulator. The SPICE simulation is able to simulate circuit behaviour in both the time and frequency domain, determine DC operating point, and vary circuit and process parameters during simulation. The SPICE output generated by Virtuoso incorporates detailed models of instanced devices, allowing gate level simulation to obtain accurate results.

During the design and development phase, the outcomes of the mathematical and numerical analysis are used to design a simulation model of the test bench, reference SenseFET, and improved SenseFET. The simulation model allows for a detailed analysis of circuit behaviour and comparative analysis of different SenseFET circuit topologies. The mathematical and numerical analysis are useful for guiding design decisions, but gate level simulation allows for design refinement.

3.7.1 Constraints from simulation and experiment design

The experimental and measurement requirements were defined using device characterisation, simulation, and the process datasheet. Simulated experiments are used to test ideas on improving the SenseFET after the initial analysis. The simulation environment also assists in designing practical experiments for real-world measurement. Experiment design and constraints are discussed in section 3.8.

The simulation environment allows for hypothesis testing and research question assessment prior to the development of a hardware prototype. Simulation is the final task in the second phase of the research methodology before the process either iterates to refine a design, or a decision is made that the designed circuits are successful at answering the research questions.

3.8 EXPERIMENTAL DESIGN

The experiments for the hypothesis testing were designed to characterise, test, and compare SenseFET type circuits. Initial experimental procedures are implemented in simulation to assist with designing and improved SenseFET. Practical procedures are thus necessarily designed based on simulated outcomes. These procedures serve to measure or verify a simulated procedure. Key experimental procedures are tabulated in Table 3.2. The detailed experimental setup is provided in Chapter 4 and Chapter 5.

Table 3.2 Summary of experimental procedures designed for simulation.

Target Parameter	**Objective**	**Procedure**	**Purpose**
V_A FET Early Voltage	To characterise this parameter at an alternate operating point	I_{DS} is simulated for increasing V_{GS}	V_A determined from I_{DS}-V_{DS} curve. V_A is required for design.
i_A and i_B SenseFET branch currents in A	To determine the current in each branch of the SenseFET	The SenseFET input is excited by simulating an inductive element which is charging and discharging. The gate-level simulated currents are recorded.	The ideal SenseFET has symmetrical branch currents. Asymmetry for the non-ideal circuit is evaluated.
v_{SENSE} SenseFET output in V	To measure the output voltage of the SenseFET	The SenseFET input is excited by simulating an inductive element which is charging and discharging. The gate-level simulated output is recorded.	The output is used as a control input. The output is used to calculate the linearity of the SenseFET.
R_m Transresistance gain in V/A	To determine the transresistance gain of the SenseFET	The SenseFET output voltage is divided by the inductor current being measured. The result is the transresistance gain. This is a direct application of (3.1).	The variation of the transresistance gain over a switching cycle is evaluated. Linearity is determined from the change in gain over a cycle.
V_{DDmin} Minimum operating voltage in V	To determine the lowest voltage at which the SenseFET still operates	V_{DD} is reduced until an appreciable change in SenseFET output is observed. This voltage is noted.	In practice the available voltage may be below the designed 1.2 V. Low voltage behaviour is characterised.

The experimental procedure in Table 3.2 summarises procedures tailored for a detailed gate level simulation environment. This allows for directly observing internal currents and direct determination of circuit gain.

Table 3.3 Summary of experimental procedures designed for prototype evaluation.

Target Parameter	Objective	Procedure	Purpose
v_{SENSE} SenseFET output in V	To measure the output voltage of the SenseFET	The SenseFET is incorporated into a non-inverting DC-DC converter, sensing the current of the inductor.	To capture the SenseFET output over several switching cycles of the DC-DC converter.
R_m Transresistance gain in V/A	To determine the transresistance gain of the SenseFET	(3.1) is applied using captured data of v_{SENSE}, v_L, and numerical analysis.	The variation of the transresistance gain over a switching cycle is evaluated. Linearity is determined from the change in gain over a cycle.
V_{DDmin} Minimum operating voltage in V	To determine the lowest voltage at which the SenseFET still operates	V_{DD} is reduced until an appreciable change in SenseFET output is observed. This voltage is noted.	To verify the designed operating range of the SenseFET.

Table 3.3 summarises experimental procedures design for real-world measurement of a prototype. These experiments are based on those of Table 3.2 with modifications to the procedures to facilitate measurement and data capture.

3.9 LAYOUT AND LAYOUT VERIFICATION

To manufacture the designed circuit, the schematic design is converted to a layout in the Virtuoso layout editor. The layout describes the physical orientation of devices and metal layers on the silicon die and is used by the foundry to manufacture the designed IC.

3.9.1 Layout considerations

The final design step, prior to layout verification, is the physical layout of each device in a circuit. The SenseFET circuits make extensive use of matched transistor pairs, to improve matching between devices, transistor pairs are physically laid out together with shared symmetry. Transistor grouping and symmetry assists in minimising the effects of process variations across the silicon die.

3.9.2 Layout versus schematic

Layout versus schematic (LVS) is an automated process where a SPICE netlist is extracted from the layout geometry and compared to the netlist generated from the schematic capture tool. LVS highlights differences between the two netlists. The primary purpose of LVS is to verify that the layout circuits are equivalent to their schematic counterpart.

For the purposes of this study, the LVS process was implemented on each circuit cell prior to integration into the global layout. LVS for the global layout was not possible at the time of integration because not all schematic derived netlists were available. Individual LVS ensures circuit equivalence in the global layout.

3.9.3 Design rule check

The design rule check (DRC) is a software driven process where the circuit layout is scrutinised against a manufacturing ruleset provided by the foundry. The DRC ensures that the geometric structures created during layout satisfy the manufacturing constraints of the IBM 130 nm 8HP process. DRC does not check for circuit validity, only manufacturability.

3.10 MANUFACTURING

The manufactured prototype has two parts, the fabricated IC, and the printed circuit board (PCB) which provides support circuitry.

3.10.1 Chip fabrication

Once LVS and DRC were satisfied, the final design files were sent to MOSIS. The foundry performed an additional in-house DRC before commencing with chip fabrication. The fabricated IC was also packaged by the foundry.

Several research projects within the research group share a single silicon die as part of a multi-project wafer (MPW), allowing for effective use of the prototyping facility provided by MOSIS. The IC is mounted in a 52 lead 8 mm × 8 mm MLP package from SEMPAC[7]. The package format is quad flat no-lead (QFN). This package has a larger cavity than would be required[8] and provides ample leads for all projects on the IC. Leadless packages minimise mounting parasitics, making them suitable for all projects requiring an external analogue RF

[7] SEMPAC (http://www.sempac.com) is a manufacturer of pre-moulded open cavity plastic packages for IC devices.
[8] The final IC dimensions are 2.5 mm × 2.5 mm. The selected package can accommodate a 6 mm × 6 mm IC.

connection. The prototype and integrated test circuits for this dissertation are active circuits, requiring external stimulus and power, making use on internal test points impractical. This package was soldered to the test PCB, creating a connection to the packaged IC. The PCB and dimensions are presented in Figure 3.2.

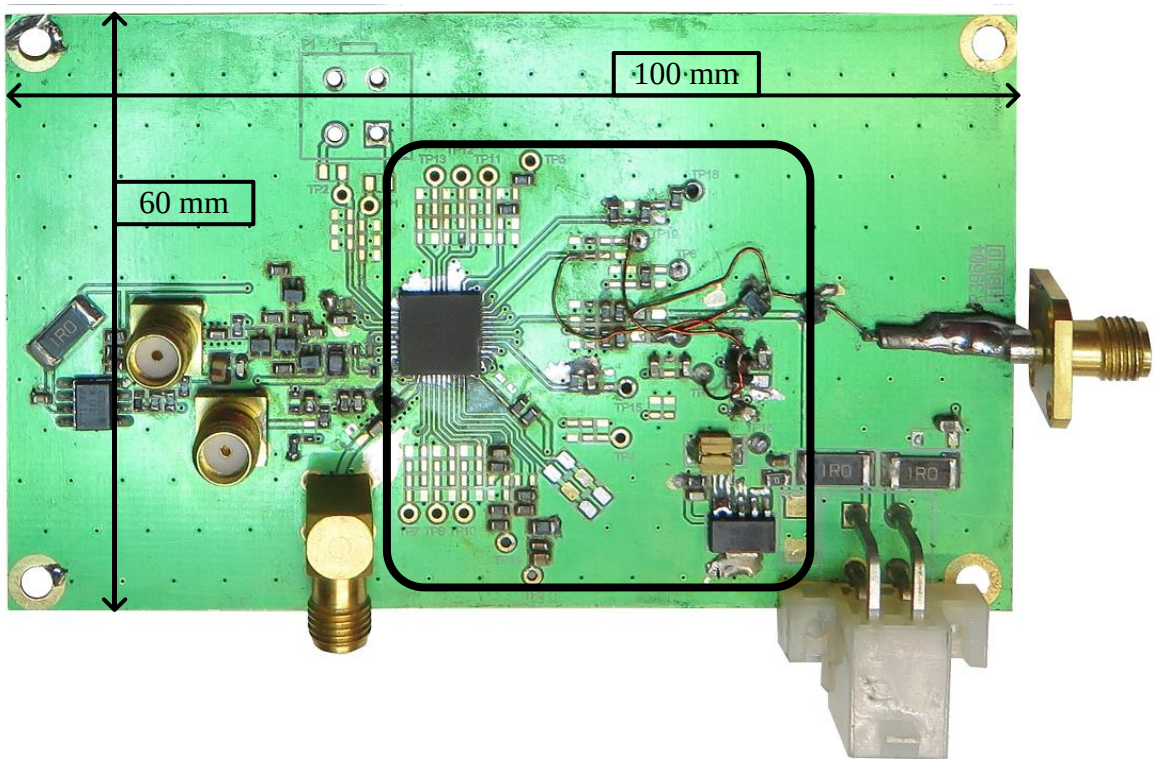

Figure 3.2. Photograph with dimensions of the PCB used to test the prototype IC.

Figure 3.2 is a photograph of the test PCB with dimensions indicated in mm. The external test circuitry and IC are bordered by the rounded square.

3.10.2 PCB design and fabrication

A PCB containing support circuitry for the fabricated IC was also manufactured. The PCB contains discrete circuit elements which are required for test and measurement. Chapter 4 contains additional details of the test PCB.

3.11 MEASUREMENT

Practical assessment of the hypothesis and research questions requires that the prototype's performance is quantified. During the analysis and design phases, mathematical and simulated testing is used to evaluate design performance. These tests form the basis for real-world testing and measurement. An advantage of basing real-world tests on simulated tests

is that meaningful comparison is possible between theory and practice. The measurements taken and tests performed are derived from the hypothesis and research questions. The hypothesis as stated in Chapter 1 is:

> *If integrated circuit topologies for measuring current using CMOS devices were improved to be resilient to second order effects and low voltage operation, the linearity of the measurement would improve.*

Measurements and tests must address each aspect of the hypothesis. The performance of both the reference SenseFET and improved SenseFET must be quantified individually using the same measurement techniques. The quantified results must then be compared in terms of circuit linearity.

3.11.1 Measurement setup

A simplified diagram of the test equipment (TE) used is shown in Figure 3.3. In Figure 3.3, the measurement setup was grouped into external stimulus, the test PCB, and external measurement. External stimulus refers to equipment used to power and provide input stimulus to the test PCB. The test PCB provides support and test circuitry to the device under test (DUT). Test circuitry include test circuits for the classic and improved SenseFET, buck-boost converter, and test points which can be used to probe the circuits with measurement instrumentation. External measurement comprises a grouping of instruments used to measure circuit characteristics and outputs.

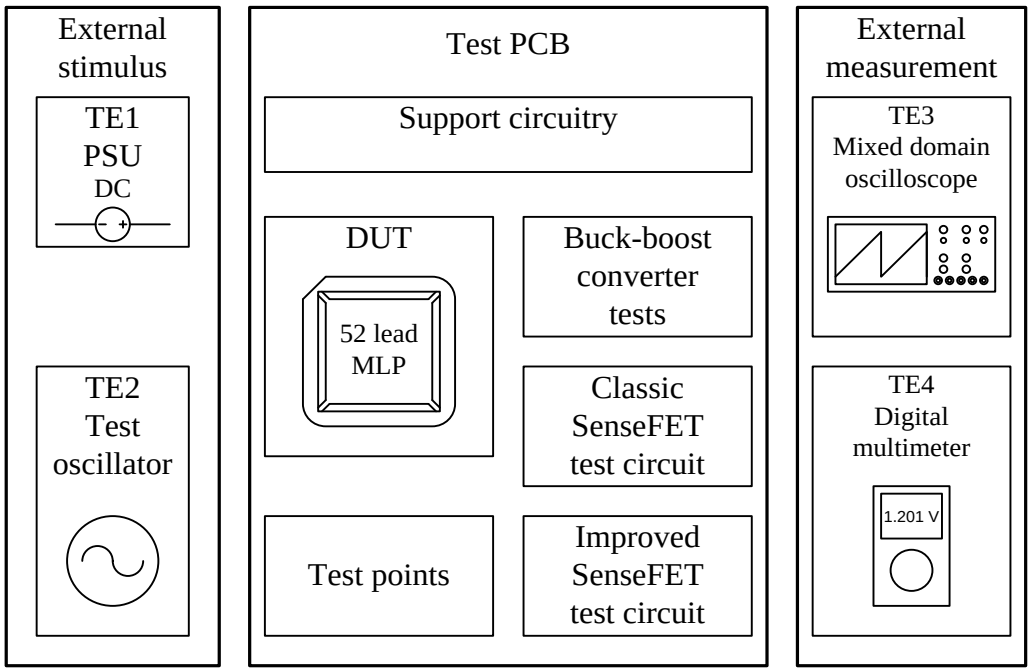

Figure 3.3. Simplified diagram of the test setup and test equipment.

The test equipment is summarised in Table 3.4.

Table 3.4 Summary of test equipment used.

	Type	**Model**	**Test function**
TE1	Digitally controlled PSU	Agilent E3644A	Provides power to support circuitry and variable and controlled input power to the buck-boost converter. The output voltage of this PSU is adjustable in 10 mV increments.
TE2	Signal generator	Rohde and Schwarz SMB100A	Generates the switching signal used to test individual current sensors. The RF output of the generator is used to drive the test converter power transistors.
TE3	Mixed domain digital oscilloscope	Tektronix MDO4104B-6 TPP1000 Probes	Digitisation and capture of measured characteristics. Verification of test circuit operation.
TE4	Digital multi-meter (DMM)	Agilent U1241B	Measurement of DC characteristics

Table 3.4 describes the test equipment used in Figure 3.3. The equipment type, model, and general test functions are described. These TE descriptions are provided as part of the

measurement environment definition. Equivalent or better TE may be used to perform measurements. Specific applications of the test equipment are described with each test procedure.

3.11.2 Test setup 1: SenseFET characterisation

The purpose of this test setup is to characterise the reference and improved SenseFETs under different operating conditions. SenseFET linearity is evaluated by quantifying the gradient of the trans-resistance gain of the sensor throughout a complete measurement cycle. The test setup is designed to manipulate the current in *L* and the switching frequency of *Q*. The data collected using this test setup is used to directly test the hypothesis. Figure 3.4 presents a diagram of the test setup used to gather data required to test the hypothesis.

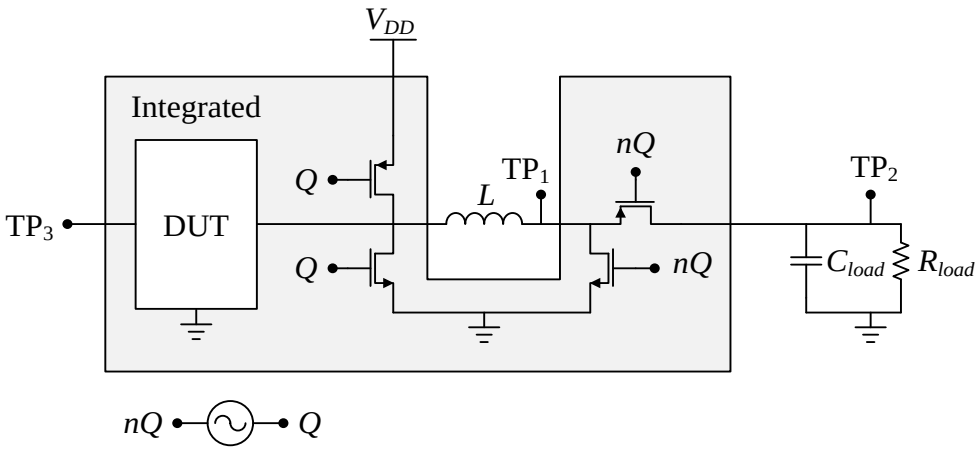

Figure 3.4. Test setup for measuring SenseFET characteristics.

The test setup depicted in Figure 3.4 was used to characterise both the reference and improved SenseFET circuits. The SenseFET circuits are tested in the context of their application in a DC-DC converter. The test bench consists of the power transistors used in a noninverting converter and the reactive components required. The test setup is designed to accept a DUT which is either the reference SenseFET or the improved SenseFET. This allows both SenseFETs to be tested using the same test circuit. The remainder of the test bench consists of a combination of integrated and discrete components. The power transistors are integrated on the same silicon die as the DUT but the inductor and load components are implemented discretely on the test PCB. An external oscillator (TE2) provides the switching signals *Q* and *nQ*.

The external configuration of L, C_{load}, R_{load}, and Q allows these parameters to adjusted. These adjustments allow the performance of the DUT to be tested under various operating conditions. The test bench has three test points (TP) from which measurements are taken using TE3. Measurements are taken by sampling and capturing the voltage at each TP throughout the switching cycle. TP_1 is used to capture the change in v_L. TP_2 is used to capture the change in v_{OUT}. TP_3 is used to capture v_{SENSE}.

The SenseFET circuits are designed to operate in a cyclic system. The test circuits are cyclic to test SenseFET behaviour during both the charge and discharge phases of L. The discrete circuit elements and switching frequency are varied to test the SenseFET performance under various operating conditions. Table 3.5 summarises the range of variation.

Table 3.5 Range of parameter adjustment on test bench.

Parameter	Range	Description
V_{DD}	0.8 V to 1.2 V	V_{DDmax} = 1.2 V is a process limitation V_{DDmin} = 0.8 V is a design choice to test operation in sub 1 V applications
L	330 nH to 3.3 µH Q ≈ 30	This range was derived from (2.11) and (2.12) for f = 10 MHz. These values yield inductor currents in the mA range.
R_{load}	10 Ω to 1 kΩ	This range was derived from (2.11) and (2.12) for f = 10 MHz.
C_{load}	100 nF to 1 µF	
Q and nQ	10 MHz Square Wave Pk-pk: 1.2 V 50% duty cycle	f = 10 MHz is a design choice based on (2.11) and (2.12) to yield the ranges for L, R_{load}, and C_{load} in commonly available surface mount device (SMD) formats.

3.11.3 Test setup 2: Buck-boost converter

This test setup is designed to evaluate the performance of an integrated buck-boost converter incorporating a SenseFET. Data collected from this test setup is used to verify the design principles applied to develop an integrated DC-DC converter. Figure 3.5 is a diagram of the test setup used to test and characterise the integrated buck-boost converter.

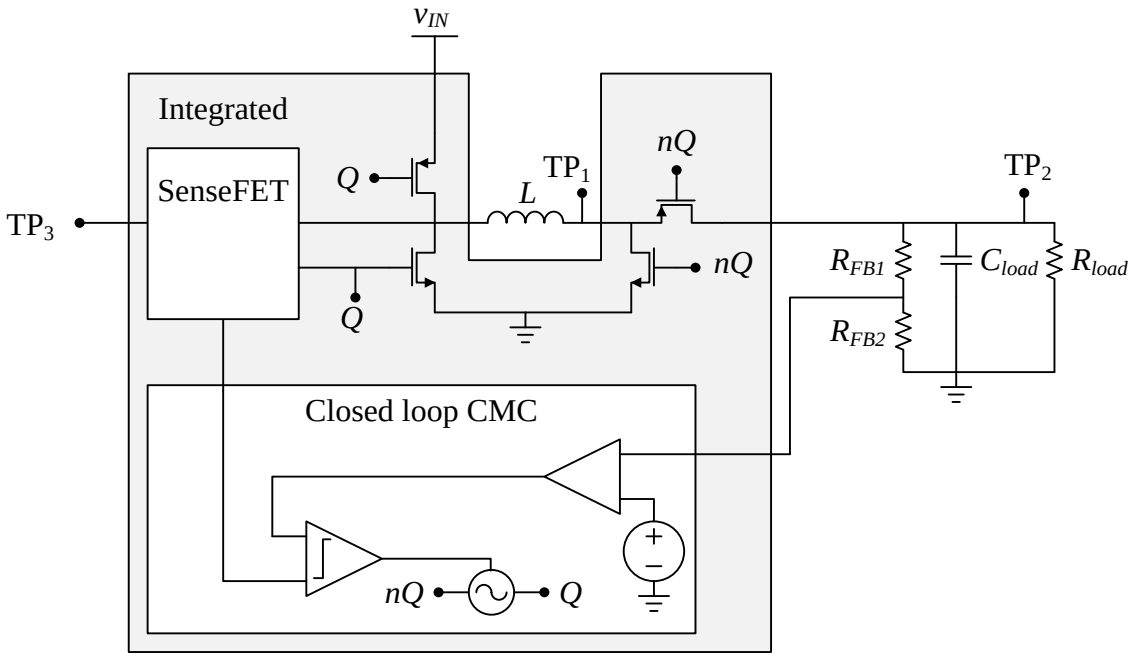

Figure 3.5. Test setup for measuring buck-boost converter.

The test setup shown in Figure 3.5, similarly to Figure 3.4, consists of IC and discrete components. The buck-boost converter is fully integrated with the exception of the switching inductor L and the reactive load. Voltage feedback resistors R_{FB1} and R_{FB2} are discrete to allow for adjustable output voltage. TP_1 to TP_3 are used as in test setup 1.

3.11.4 Data analysis

The mixed domain oscilloscope (MDO) is used to digitise the signals at each test point. High impedance probes are used to prevent the MDO from loading the test circuit. Data is sampled over several complete cycles to ensure that at least one complete cycle is captured, including the boundaries of each cycle. Data digitised by the MDO is stored locally on the MDO before being transferred to a computing environment.

The primary parameter for determining the linearity of the SenseFET is tested using test setup 1. This parameter is the transresistance gain (r_m) of the SenseFET and is given by:

$$R_m = \frac{v_{SENSE}}{i_L} \tag{3.1}$$

Calculating R_m in (3.1) requires the inductor current i_L to be known. i_L is determined by numerically integrating the voltage over L that is measured at TP_1 in Figure 3.4. i_L is given by:

$$i_L = \frac{1}{L}\int_{t0}^{t1} v_L(\tau)d\tau \tag{3.2}$$

Where v_L is the voltage drop over the inductor. MATLAB is used to perform the numerical integration and other post-processing operations. The output of the AMS SPICE simulations are imported into MATLAB, allowing for direct comparison of the simulated and measured data for both reference and improved SenseFETs.

3.12 TECHNICAL SOFTWARE

Table 3.6 summarises the technical software used in this dissertation as well as the application of each package.

Table 3.6 Table of technical software used in this dissertation.

Package	**Version**	**Software Developer**	**Description**
MATLAB	R2012a	Mathworks	MATLAB is a technical computing software package developed for engineering and science.
Virtuoso S-Edit	(2007)	Cadence	S-Edit is used for schematic capture.
Virtuoso L-Edit	(2007)	Cadence	L-Edit is used for the creation and editing of circuit layout.
AMS	(2007)	Cadence	AMS generates SPICE netlists and circuit simulation
Assura	(2007)	Cadence	Assura parses layouts to perform the DRC for the selected process.

MATLAB was used to script and execute numerical implementations of analytical work. Measurement data and data captured from simulation were also analysed and compared using MATLAB. The MATLAB scripts used are presented in Addendum A.

Virtuoso S-Edit is a schematic capture tool used to graphically instance SPICE models and generate SPICE netlists of circuits. The tool is able to incorporate simple SPICE models and complete gate level models of integrated devices.

Virtuoso L-Edit, similarly to S-Edit, is a layout capture tool. Circuit elements are graphically represented and manipulated. L-Edit is used to generate data for fabrication in conjunction with Assura. Assura parses the layout generated by L-Edit and identifies violations of the process design rules.

AMS is a simulation package which uses the SPICE netlist generated by S-Edit as input to run a large variety of SPICE based simulations. AMS also provides tools to perform time and frequency domain data analysis, parametric sweeps, Monte-Carlo analysis, and mathematical manipulation of data.

3.13 CONCLUSION

This Chapter provided an overview of the research methodology applied for this dissertation. The chosen methodology has three distinct phases, with each phase comprised of iterative processes designed to realise the goal of the phase. This approach is advantageous because of an emphasis on design space exploration prior to focussed hardware development.

Phase one comprises the literature study and problem definition. The literature on integrated DC-DC converters is surveyed within the scope of WSNs. The literature study is used to identify where there is research value and the hypothesis was developed. The initial design boundaries are determined based on the chosen CMOS process limitations.

Phase two focuses on experimentation and design. Experimental procedures are developed from design equations and process limitations. These procedures are used to identify shortfalls in designs from the literature and to develop and refine test circuits. The goals of phase two are the development of an integrated buck-boost converter, a reference SenseFET, and an improved SenseFET in a simulation environment. The results of this phase form the

basis of prototype development in phase three. Phase three is centred around the application of phase two's results to developed, fabricate, and evaluate a prototype.

The measurement setups were designed to obtain data of parameters that can be used to test the hypothesis using the experimental procedures developed in phase two. Two test setups are discussed. Test one is designed to measure the transresistance gain of the SenseFET, which is used to evaluate the linearity of the sensing circuit. Test one is the primary test used to evaluate the hypothesis. Test two is designed to evaluate an integrated DC-DC converter making use of a SenseFET, testing the application of converter theory utilising a SenseFET to measure internal current. Finally, the technical software used is briefly discussed.

CHAPTER 4 DESIGN AND FABRICATION

4.1 CHAPTER OVERVIEW

This Chapter presents the detailed design for all circuits used in this dissertation which contribute to the hypothesis. The design detail presented describes the analytical, numerical, simulation, implementation, and fabrication stages of the systems and circuits used in this dissertation. The Chapter first presents process characterisation. Process characterisation is required to develop the analytical and numerical designs of the SenseFETs.

Two SenseFET designs are presented, a reference design based on a commonly used circuit, and the improved design which is the contribution of this dissertation. Each design provides an overview of the primary design goals as well as the design itself. Design information provided includes mathematical design, transistor implementation, layout, and simulated performance metrics.

The Chapter concludes with measurement setup, test circuits, and fabrication details.

4.2 PROCESS CHARACTERISATION

4.2.1 Process characterisation overview

Section 2.8 in Chapter 2 describes several mechanisms in the IBM 8HP 130 nm BiCMOS process that cause the behaviour of the transistors to diverge from the first order approximation. It is possible to model these identified factors into the first order approximation of the transistors behaviour given by (2.26) and (2.28). The disadvantage of this is that the more accurate the model, the more cumbersome it becomes to design circuits by hand. Regardless of the design equation complexity, the designs must be simulated using comprehensive process and device models in SPICE.

An effective design cycle will compromise the accuracy of the design equations to quickly deliver a coarse design which may be refined using accurate device models and CAD.

The transistor current is primarily affected by two primary mechanisms, namely, velocity saturation and channel length modulation. The effect of these mechanisms on transistors operating in saturation is repeated below for reference.

Velocity saturation is modelled by:

$$i_{DS} \cong \frac{k'_n}{2\left(1+\frac{v_{GS}-V_t}{E_c L}\right)}\frac{W}{L}(v_{GS}-V_t)^2 \tag{4.1}$$

Channel length modulation is modelled by:

$$i_{DS} = \frac{\mathrm{k}'}{2}\left(\frac{W}{L}\right)(v_{GS}-V_t)^2(1+\lambda v_{DS}) \tag{4.2}$$

The channel modulation effect is included in the design equations because it has a more dynamic effect on the SenseFET behaviour because of the dependence on v_{DS}, which can vary significantly in the SenseFET design. The reduction in i_{DS} from velocity saturation is determined by ($v_{GS} – V_t$), which is either chosen to be small or remains constant in paired transistors. It is for these reasons that the effect of channel modulation is used in coarse designs, but the effect of velocity saturation is relegated to the simulation tool.

4.2.2 Deriving channel length modulation parameters from process characteristic curves

The chosen process offers two gate oxide thicknesses for use by designers. The thicker gate oxide allows for higher gate voltages, whereas the gate voltage of the thinner oxide devices must be substantially lower. In accordance with the low voltage requirement, thin gate oxide devices are used.

The process datasheet only provides process characteristic curves at under certain operating conditions. The SenseFET designs operate at a significantly different operating point, rendering the provided data insufficient. To correctly include the channel modulation effect, the effect must be characterised at the desired operating point.

The characterisation is achieved by using the detailed transistor device level SPICE models provided by the foundry. These models are based on empirical data and can be used to derive device parameters at a chosen operating point. The test circuits used to derive the device characteristics are shown in Figure 4.1.

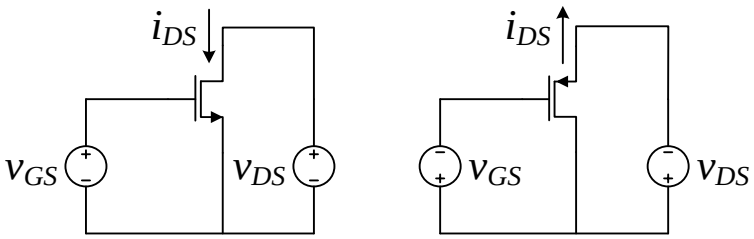

Figure 4.1. Channel length modulation characterisation circuit.

In Figure 4.1 a single NFET or PFET device is excited by two voltage sources to derive the $i_{DS} - v_{DS}$ characteristic curves. The weighting factor $(1 + \lambda v_{DS})$ is derived from the transistor $i_{DS} - v_{DS}$ curves.

The curves are generated by holding v_{GS} at a constant value and sweeping v_{DS} across the operating range that will be used in the SenseFET designs. v_{GS} is incremented and the simulation repeated to generate a family of curves which can be used to derive λ. The characterisation setup is summarised in Table 4.1.

Table 4.1 NFET and PFET characterisation setup.

Parameter	**Description**
Thin gate NFET	W/L = 6 W = 720 nm, L = 120 nm
Thin gate PFET	W/L = 6 W = 720 nm, L = 120 nm
v_{GS} sweep range	0 mV – 1200 mV
v_{DS} sweep range	0 mV – 1200 mV

The NFET and PFET aspect ratios in Table 4.1 were chosen to be representative of the aspect ratio used in the SenseFET designs. The maximum v_{GS} and v_{DS} are chosen to be within the acceptable range to prevent gate oxide breakdown.

The results of the characterisation are presented in Figure 4.2 and Figure 4.3.

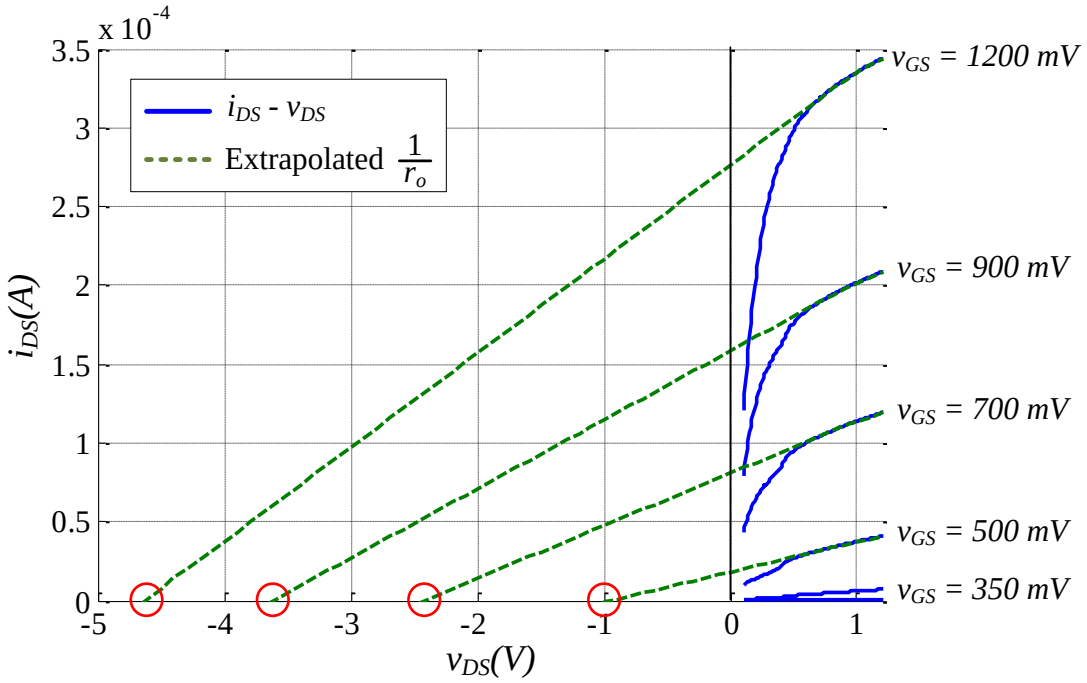

Figure 4.2. NFET $i_{DS} - v_{DS}$ characteristic curves for W/L = 6.

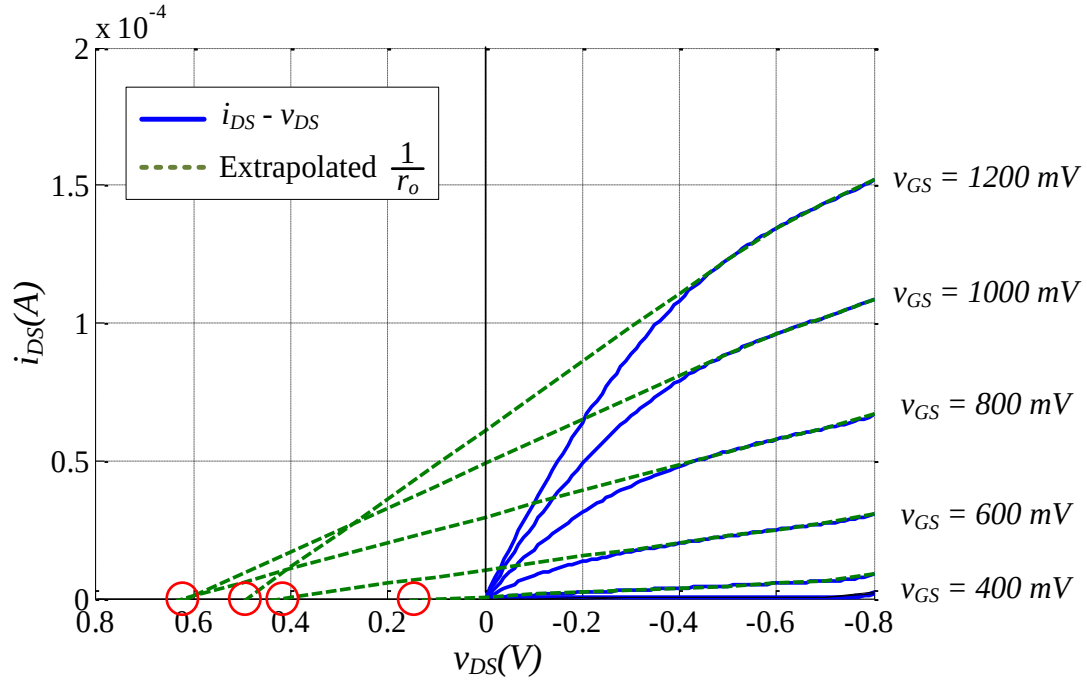

Figure 4.3. PFET $i_{DS} - v_{DS}$ characteristic curves for W/L = 6.

Figure 4.2 shows the $i_{DS} - v_{DS}$ characteristic curves for an NFET device with the $i_{DS} - v_{DS}$ slope in saturation extrapolated to intercept with the v_{DS} axis. Figure 4.3 shows the $i_{DS} - v_{DS}$ characteristic curves for a PFET device. In both Figure 4.2 and Figure 4.3 the intercept with

the v_{DS} axis is indicated with a red circle. From Figure 2.13, this intercept point indicates -1/λ for the device. 1/λ for the NFET and PFET is summarised in Table 4.2.

Table 4.2 Summary of device V_A.

NFET		
v_{GS} (mV)	**V_A (V)**	**$\lambda = 1/V_A$**
500	1	1
700	2.5	0.4
900	3.6	0.28
1200	4.6	0.22
PFET		
v_{GS} (mV)	**V_A (V)**	**$\lambda = 1/V_A$**
400	0.15	6.67
600	0.4	2.5
800	0.6	1.67
1000	0.6	1.67
1200	0.5	2

Table 4.2 shows λ varying from 0.22 to 1 for the NFET and from 2 to 6.67 for the PFET device. The narrow range of λ means that first-order design equations use an average value of λ.

4.3 REFERENCE SENSEFET

4.3.1 Overview

The reference SenseFET [29] design used is described in detail in Chapter 2, section 2.7.2. The reference is implemented in the same CMOS process as the suggested improved SenseFET to provide a measurement base line.

4.3.2 Design concepts

The reference design and a test circuit are shown in Figure 4.4.

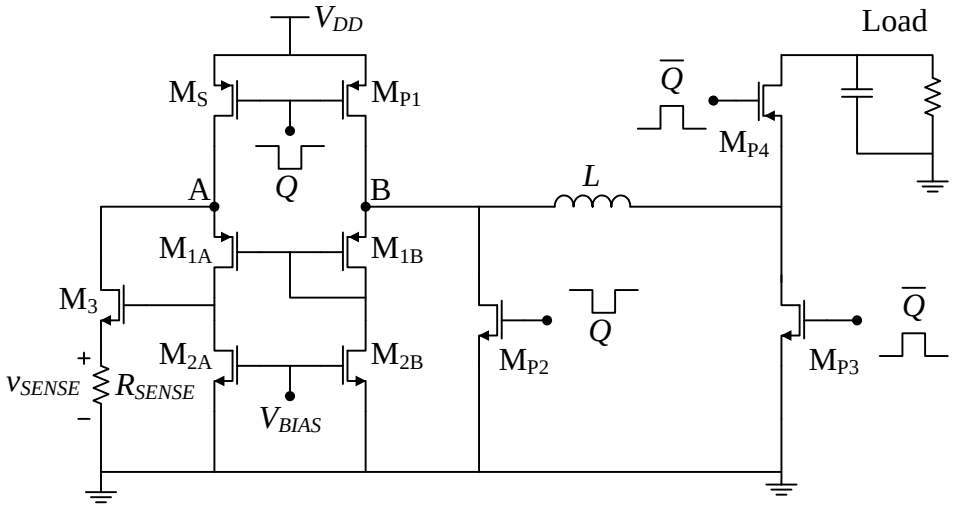

Figure 4.4. SenseFET implemented with a greatly simplified amplifier.

In Figure 4.4 the reference SenseFET design is shown to be connected to a non-inverting DC-DC converter test circuit. In this state power transistors M_{P1} and M_{P3} are on, allowing current to flow from V_{DD} and through L. In this state the SenseFET is configured to sample the current through L as power is drawn from V_{DD}.

From Chapter 2 and assuming ideal devices, the output voltage of the sensor, v_{SENSE} is given by:

$$v_{SENSE} \approx R_{SENSE}\left(\frac{i_L}{K} - i_{DSM_{1A}}\right) \tag{4.3}$$

Equation (4.3) is used as the starting point for the design. The selection of v_{SENSE}, with a suitable range is enabled through the knowledge of the value of L and the choice of a value for R_{SENSE} an output. This allows for the determination of a value of K. These values, in combination with the process limitations, may then be used to derive aspect ratios for M_S, M_1, M_2, and M_3.

The premise of the derivation of (4.3) and the operation of the circuit in Figure 4.4 is that nodes A and B are held at equal voltage by the matched pair M_1. Equations which incorporate second order effects are not used to test the validity of this premise on which the design is

based. This is motivated by the requirement to show and test how the classical SenseFET design performs when simply scaled to the IBM 8HP 130 nm process node.

4.3.3 Implementation

4.3.3.1 Design constraints

Process parameters, which influence design constraints, are confidential under the NDA with MOSIS.

The design space is constrained prior to any design. To prevent any voltages in the design from exceeding the gate oxide breakdown voltage of the process, V_{DD} is chosen to be no more than 1.2 V. 1.2 V is comfortably within the process limit for thin oxide devices.

The value of L is determined by the switching frequency of Q and the maximum allowable current through power transistors M_{P1} and M_{P3}. The maximum current through an inductor is given by:

$$i_{L\,Max} = \frac{v_L t}{L}\Big|_{t0}^{t1} \tag{4.4}$$

With V_{DD} limited to 1.2 V and a switching frequency of 10 MHz, the maximum current through a 1 µH inductor is 600 mA. The switching frequency of 10 MHz was chosen to yield a 1 µH inductor. 1 µH inductors in a surface mount form factor are readily available and of comparative size to a chip containing a full buck-boost converter.

R_{SENSE} in Figure 4.4 is an integrated poly-silicon resistor. Poly-silicon resistors have a moderate sheet resistance, allowing for relatively compact resistors with a resistance in the range of a few kΩ while keeping width and length limited to less than 10 µm.

4.3.3.2 Power transistor design

The aspect ratio of power transistor M_{P1} determines the aspect ratio of the sensing transistor M_S. In the non-inverting buck-boost converter shown in Figure 2.4, four switches are required to realise the non-inverting DC-DC conversion. For the buck-boost test circuit used, these switches are implemented by transistors M_{P1}, M_{P2}, M_{P3}, and M_{P4} in Figure 4.4.

M_{P1} to M_{P4} are designed for a maximum current of 1000 mA, exceeding the requirement of 600 mA. The permitted current density in the transistors is a process parameter. Using data provided by MOSIS, the power transistors are designed to have an aspect ratio which ensures

the devices can conduct the necessary current. The aspect ratios are summarised in Table 4.3.

Table 4.3 Summary of power transistor aspect ratios.

Transistor	**Aspect ratio**		**On-State**
	(W/L)	**nm**	
MP1	1000	120000/120	*D*
MP2	666.6	80000/120	1-*D*
MP3	666.6	80000/120	*D*
MP4	1000	12000/120	1-*D*

Table 4.3 summarises the aspect ratios of the power transistors. The aspect ratio of each transistor is provided as a simplified (W/L) ration and as ration of the actual device width and length. The on-state column indicates during which phase of the DC-DC conversion the device is turned on. From Chapter 2, section 2.3, *D* represents the duty cycle of the clock, *Q*, driving the power transistors.

NFET devices M_{P2} and M_{P3} require a smaller aspect ratio than the PFET devices, M_{P1} and M_{P4}. NFET devices have a higher carrier mobility than PFET devices and support a higher current density per µm.

4.3.3.3 Reference SenseFET design obstacles

Once the aspect ratio of the power transistor M_{P1} is known, the aspect ratios of M_S and the remaining transistors can be determined. The reference design is based on the design detailed provide in Chapter 2, section 2.7.2. As per the derivation of the ideal SenseFET operation, it is noted in the literature that the voltage at node A must track the voltage at node B in order for the SenseFET to operate correctly. In various implementations in the literature, the circuit of Figure 4.4 is used. The only design decision other than that of the voltage tracking between nodes A and B is the magnitude of the bias currents in the branches of the SenseFET. The design in [28] suggests that the bias currents be in the µA range for correct operation.

The reference SenseFET was designed without factoring in non-ideal effects of the devices. This was done in accordance with the examples of SenseFET designs presented in Chapter 2, which did not take non-ideal effects into account.

Equation (4.3) is applied to determine the scaling factor, *K*, of the SenseFET. If *K* = 1000 then this allows for µA currents in the sensor circuit compared to the mA currents that will be measured. For the maximum possible inductor current of 600 mA, the transresistance gain of the SenseFET is chosen such that the maximum output, v_{SENSE}, is less than V_{DD}. With a maximum V_{DD} of 1.2 V and R_m = 2, v_{SENSE} is constrained by (3.1) to a maximum of 1.2 V.

Initial design with the values derived in the preceding paragraphs did not yield a working SenseFET from design equation (4.3). Once the SenseFET was incorporated with the test circuit, diode-connected M_{1B} caused the branch bias currents to vary to a large extent, with branch B currents and order of magnitude larger than branch A. The deviation in current in branch B exceeds the variation expected from deviation in the device aspect ratio. In the absence of the converter test circuit, the branch currents are approximately equal. The large branch current differential prevented the voltage at node A from tracking the voltage at node B. By reducing the maximum possible current to be measured by an order of magnitude, it was possible to use this topology to design a functional SenseFET.

4.3.3.4 Reference SenseFET design details

The final design that was tested was designed for a maximum measurable current of 10 mA. For the maximum possible current of 10 mA, the transresistance gain of the SenseFET is chosen such that the maximum output, v_{SENSE}, is less than V_{DD}. With a maximum V_{DD} of 1.2 V and R_m = 120, v_{SENSE} is constrained by (3.1) to a maximum of 1.2 V.

Equation (4.3) is applied to determine the scaling factor, *K*, of the SenseFET. If *K* = 80 then this allows for µA currents in the sensor circuit compared to the mA currents that will be measured. Applying (4.3) and assuming $\frac{i_L}{K} \gg i_{DSM_{1A}}$, yields R_{SENSE} = 10 kΩ.

The bias currents in the reference SenseFET are determined by M_2. M_2 is designed such that:

$$I_{DSM2} = I_{DSM1} = 25\ \mu A \tag{4.5}$$

M_S will conduct a current of 200 µA during each switching cycle. By selecting a bias current and order of magnitude less than i_{DSMS}, the assumption that $\frac{i_L}{K} \gg i_{DSM_{1A}}$ holds true. 25 µA is an order of magnitude less than the current conducted by M_S.

V_{BIAS} was chosen to be 500 mV to ensure that transistor pair M_2 remain in saturation. By direct application of (2.15), the aspect ratio of M_2 was determined. The aspect ratio of M_3

was chosen to be equal to M_2. The aspect ratio of M_1 was chosen to limit the influence of variations in v_{GSM1} on the bias currents in each branch.

Once initial transistor aspect ratios and bias voltages for all devices were determined analytically, gate level simulation was used to refine bias voltages. Both the aspect ratio and the bias voltages for the cascoded SenseFET are summarised in Table 4.4.

Table 4.4 Summary of reference SenseFET aspect ratios and biasing.

Parameter	**Aspect ratio**	
	(W/L)	nm
M_{P1}, M_{P4}	1000	120000/120
M_{P2}, M_{P3}	666.6	80000/120
M_S	50	6000/120
M_1,	6	720/120
M_2, M_3	26.7	3200/120
	Voltage	
V_{BIAS1}	500 mV	
	Resistance	
R_{SENSE}	10 kΩ	

Table 4.4 summarises the aspect ratios and biasing used in the reference SenseFET design. Aspect ratios are expressed in terms of the dimensionless ratio $\left(\frac{W}{L}\right)$ and as a ratio of width and length in nm. The bias voltage is expressed in mV.

4.3.4 Layout

4.3.4.1 Reference SenseFET

The reference SenseFET layout which was designed and generated in CAD is presented in Figure 4.5.

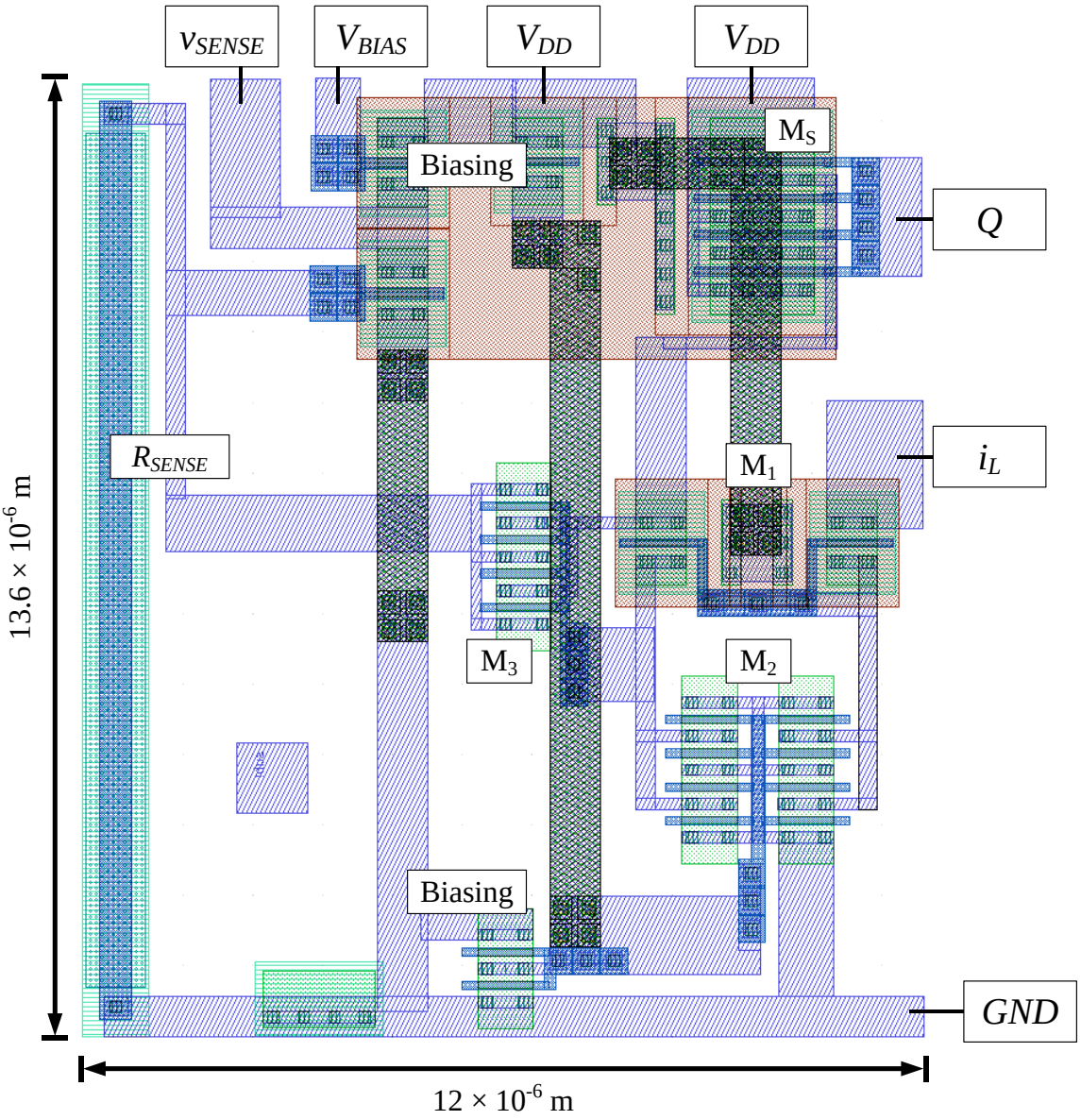

Figure 4.5. CAD Layout of the reference SenseFET.

Figure 4.5 is an annotated diagram of the reference SenseFET device layout. Inputs and outputs are indicated on the periphery. Transistors corresponding to Figure 4.4 are also indicated. The total dimensions of the reference SenseFET layout are 12 µm by 13.6 µm, with a total area of 163 µm^2.

The reference SenseFET makes use of matched pairs M_1 and M_2. To improve matching over temperature and process variations, the transistor pairs are grouped physically, with the PFETs of pair M_1 in the same *n*-type well.

Wide transistors, such as M_S, make use of a fingered gate structure. The structure of M_S is shown in Figure 4.6.

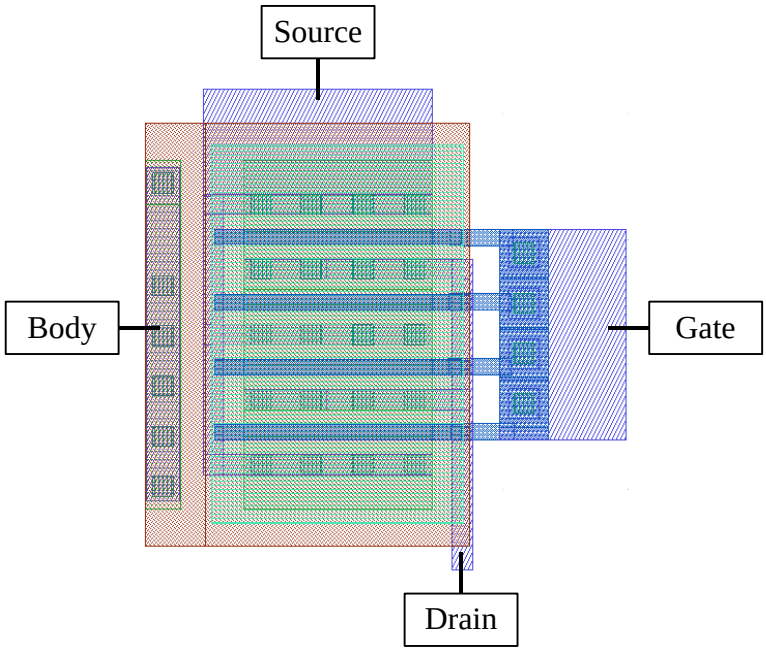

Figure 4.6. PFET Transistor with a fingered gate implementation.

Figure 4.6 shows a PFET device with a fingered gate, the device terminals are annotated. This device layout makes use of multiple gate, drain, and source terminals to "fold" the wide transistor into a more compact form. The primary advantage of this layout structure improved switching performance. The reduced gate capacitance increases the device bandwidth and thus improves the transient response of the transistor. This approach is used throughout the layout, resulting in a more uniform distribution of diffusion areas. The uniform and compact layout approach using multi-gate devices has the added benefit of not having the integrated devices spread over large area, which would increase the susceptibility to process variation.

The proximity of devices in the overall layout is determined by the design rules of the process. The reference SenseFET is laid out to have the circuit terminals on the same metal layer on the perimeter of the circuit, allowing for ease of integration into more complex circuits, such as a fully integrated buck-boost converter.

4.3.4.2 Power transistors

The power transistors used to test both the reference SenseFET and the improved SenseFET directly influences the design of the SenseFET, specifically the aspect ratio of the power transistor. The power transistor layout is presented in Figure 4.7.

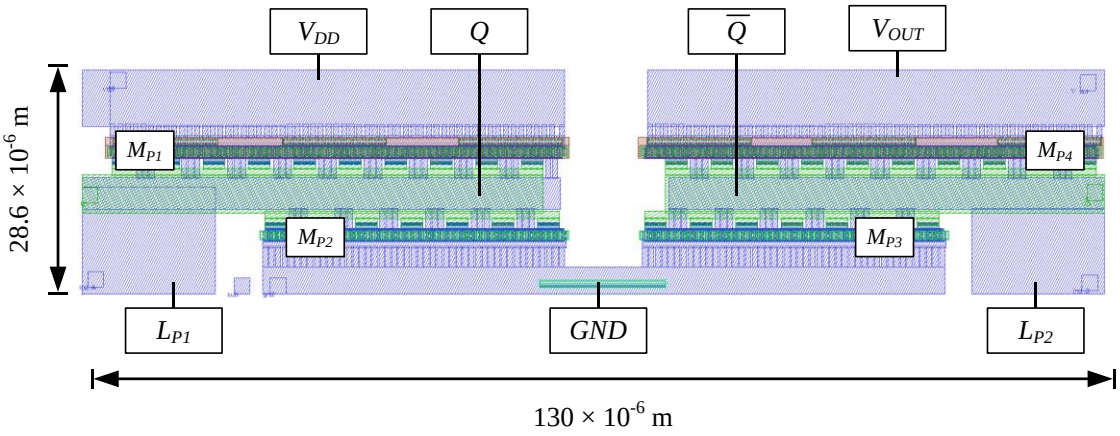

Figure 4.7. Power transistor layout.

Figure 4.7 shows the layout of power transistors M_{P1} to M_{P4} with annotations. L_{P1} and L_{P2} refers to the two terminals of the inductor L.

M_{P1} to M_{P4} makes use of heavily fingered gates. This structure is used to improve the transient response of the power transistor as it switches by reducing the RC load seen by the power transistor gate drivers. As with the structure in Figure 4.6, the overall layout of the power transistors is more compact.

4.3.5 Simulated performance

Two key parameters that characterise the performance of the SenseFET are the branch symmetry and the transresistance gain of the SenseFET.

Branch symmetry is used to evaluate the performance of the circuit which allows the voltage at node A to track the voltage at node B. From Chapter 2, section 2.7.2, A variation in the voltage at B will have an associated change in current in that branch. If the voltage at node A tracks the voltage at node B then the current changes associated with the voltage change at B will be replicated at node A. Branch current symmetry indicates how well the changes in branch B are reflected in branch A.

The transresistance gain (R_m) is simply the SenseFET output divided by the input. Characterising the gain over a range of inputs is used to measure the linearity of the sensor, the more linear the sensing circuit, the more accurately changes in the input will be manifest as scaled changes at the output.

4.3.5.1 SenseFET branch current symmetry

The operation of the SenseFET requires that the voltages at nodes A and B in Figure 4.4 are equivalent. The gates of transistor pair M_1 are tied together, as are the gates of the bias transistor pair M_2. By tying the gates of these devices together, the SenseFET branch connected to node A should track the branch connected to node B, assuming ideal device behaviour.

The branch symmetry may be characterised by considering the transient behaviour of the current in each branch as the current through the inductor changes. The simulated branch currents over a single cycle are shown in Figure 4.8.

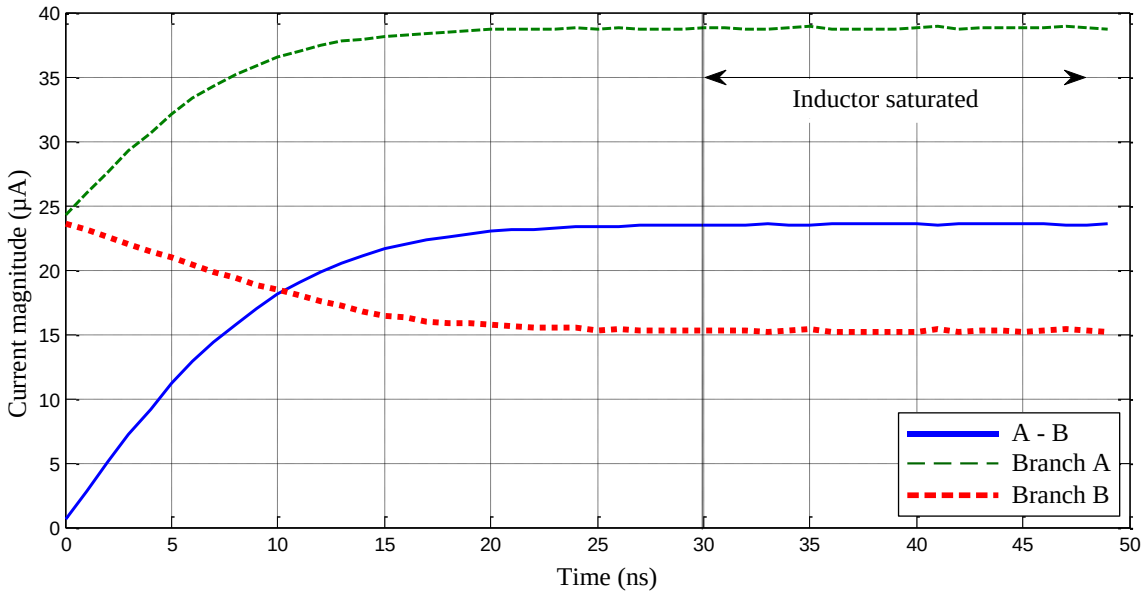

Figure 4.8. Branch currents in reference SenseFET.

Figure 4.8 shows the currents in the branches of the reference SenseFET as well as the absolute delta between the branches. The switching cycle starts at 0 ns. At 0 ns, both branches are at the bias current of 25 µA. The branch currents diverge from the designed bias current as the inductor current increases, with the current in branch A increasing and

the current in branch B decreasing. After 30 ns of the 50 ns charging cycle the inductor starts to saturate and the branch currents reflect this behaviour through stabilisation.

The divergent behaviour of the branch currents through the cycle result in a branch current delta that increases as the cycle progresses. The variable delta between the branch currents is an indication that the currents in the branches do not track, despite the gates of the transistor pairs M_1 and M_2 being tied together.

4.3.5.2 Transresistance gain

The SenseFET's overall performance can be quantified by evaluating the transresistance gain of the current sensing circuit. The transresistance gain is given by:

$$R_m = \frac{v_{SENSE}}{i_L} \tag{4.6}$$

In (4.6), R_m is the transresistance gain, v_{SENSE} is the SenseFET voltage output, and i_L is the current through the inductor. R_m has units of V/A. V/A is a more insightful use of units than the simplification of V/A to Ω. By analysing the behaviour of the SenseFET's R_m over a switching cycle it is possible to characterise the linearity of the sensor.

A simulated plot of R_m for the reference SenseFET is shown in Figure 4.9.

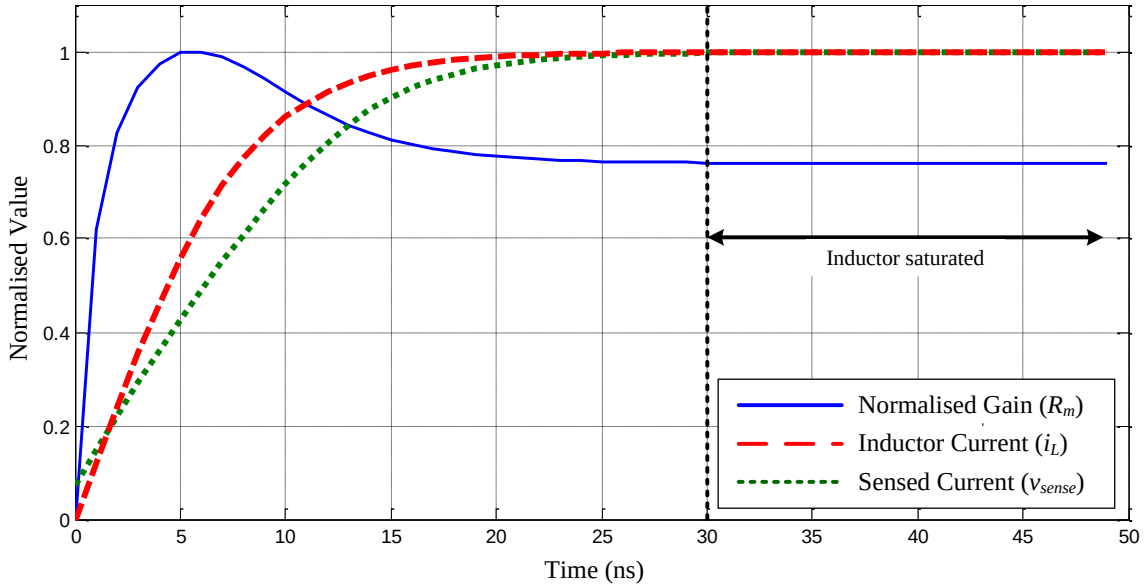

Figure 4.9. Transresistance gain, normalised inductor current, and sensed current of the reference SenseFET.

Figure 4.9 is a normalised plot of R_m, v_{SENSE}, and i_L. The plots have been normalised to emphasise the deviation of v_{SENSE} relative to i_L. During the first 15 ns of the cycle, the gain of the reference SenseFET has a distinctive non-linear behaviour. The rapid increase in gain from 0 ns to 2 ns is caused by the transient response of the SenseFET at the switching boundary of the test circuit. In this region of the switching cycle, the input of the SenseFET is pulled to 0 V by v_L, driving M_{1B} out of saturation and into cut-off.

The region of non-linear behaviour from 3 ns to 15 ns corresponds to the large deviation in branch currents in Figure 4.8. The correlation between divergent branch currents and the deviation of R_m reinforces that poor tracking between branch A and branch B is responsible for poor sensor performance. As the deviation between branch currents stabilises, the gain also starts to normalise. The reduction in gain deviation becomes more pronounced as the dynamic behaviour of the inductor is reduced as the inductor approaches saturation.

The gain profile of the reference SenseFET is indicative of a sensing circuit which is able to sense steady-state currents in a linear manner but is unable to correctly sense dynamic current behaviour.

4.4 CASCODED SENSEFET

4.4.1 Overview

The reference SenseFET has a non-linear transresistance gain. From circuit analysis and simulation this non-linearity can be ascribed to asymmetrical behaviour in the two branches of the reference SenseFET.

The cascoded SenseFET design improves the linearity by making the base SenseFET circuit more robust to external stimuli and process behaviours. External stimuli in tandem with process characteristics degrade the linearity of the reference circuit. The primary circuit mechanism constitutes a combined biasing and current mirror circuit in a folded cascoded configuration. This configuration isolates the biasing from external stimulus that disrupts the branch symmetry in the SenseFET, in conjunction with second-order effects in the CMOS process.

4.4.2 Design Concepts

The improved SenseFET which linearises the transresistance gain of the reference SenseFET is shown in Figure 4.10.

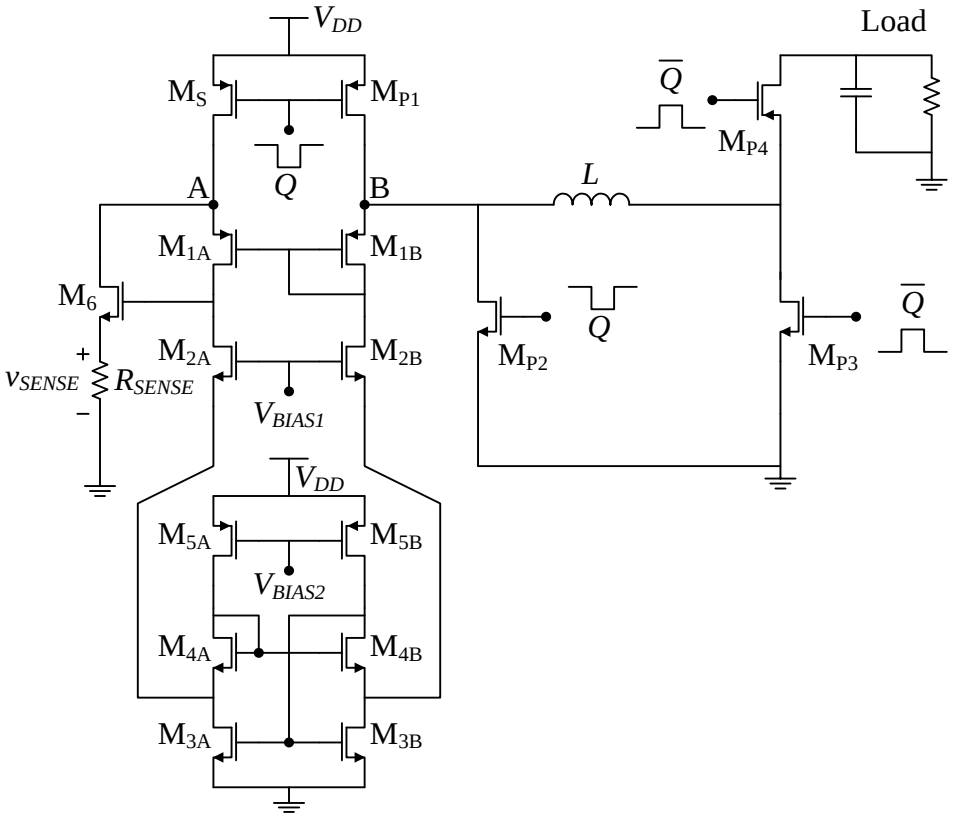

Figure 4.10. Schematic diagram of a SenseFET that has been linearised using a cascode structure.

Figure 4.10 shows a schematic of the improved SenseFET as well as the non-inverting buck-boost converter. The buck-boost converter consists of M_{P1} to M_{P4}. The remaining transistors constitute the sensing circuit. The circuit shares a sensing topology with the reference SenseFET in Figure 4.4. Both SenseFETs make use of a sensing transistor M_S, with additional transistors, to equalise the voltages at nodes A and B. The improved design introduces transistor pairs M_3, M_4, and M_5.

4.4.2.1 Reference SenseFET design disadvantages

The reference SenseFET design equations assumed ideal devices and device behaviour, with the SenseFET operation described by (2.17) to (2.25). If the SenseFET equations are reconsidered with the inclusion of terms which model non-ideal effects, then origin of branch asymmetry becomes apparent.

Chapter 2, section 2.8.1 illustrates the effect channel length modulation has on large- and small-signal behaviour of a transistor. Additionally, process characterisation in section 4.2 illustrates that the i_{DS} characteristics of transistors in the IBM 8HP BiCMOS process stray far from the ideal device assumption. Incorporating this information into an analysis of the saturation current in M_{1B} yields:

$$i_{DS} = \frac{k_p^{`}}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \tag{4.7}$$

$$\text{Since } v_{GS} = v_{DS} \text{ for } M_{1B} \text{ and } v_{SM_{1B}} = v_L \tag{4.8}$$

$$i_{DSM_{1B}} = \frac{k_p^{`}}{2}\left(\frac{W}{L}\right)_{M_{1B}}(v_{GS} - V_t)^2(1 + \lambda v_{GS}) \tag{4.9}$$

$$i_{DSM_{1B}} = \frac{k_p^{`}}{2}\left(\frac{W}{L}\right)_{M_{1B}}\left(v_G - V_t - L\frac{di_L}{dt}\right)^2\left(1 + \lambda\left(v_G - L\frac{di_L}{dt}\right)\right) \tag{4.10}$$

Equation (4.7) defines the current in M_{1B} when it operates in saturation. Non-ideal effects are approximated by $\lambda = 1/V_A$. For small λ the effect on v_{DS} and thus, i_{DS}, is also small and can be ignored. As λ increases the effect on v_{DS} and i_{DS} becomes more severe. From Table 4.2, the λ extracted from the process empirical model is significant and cannot be neglected in circuit analysis.

The inclusion of channel length modulation effects in (4.10) shows that i_{DS} is modulated by v_L. v_L both directly varies the gate voltage of M_{1B} and effects i_{DS} through the channel modulation effect.

Similarly, (4.7) also applies to M_{1A} and pair M_2. Despite the v_{GS} of pair M_2 being fixed to a bias voltage, variation in i_{DS} in this pair manifests through channel length modulation. If pair M_2 is considered a differential pair with fixed input, the small-signal gain is given by:

$$A_{M_2} = -gm\left(r_{oM_1} || r_{oM_2}\right) \tag{4.11}$$

$$\text{Where } r_o = \frac{V_A}{I_{DS}} \quad \text{and} \tag{4.12}$$

$$gm = \frac{k_n^{`}}{2}\left(\frac{W}{L}\right)_{M_{1B}}(v_{GS} - V_t)(1 + \lambda v_{DS}) \tag{4.13}$$

Equations (4.11) and (4.13) are both functions of V_A with (4.11) being a strong function of i_{DS}. This dominance manifests as an unbalanced operation of the differential-pair even though the gates are tied together. The variance in i_{DS} causes both the large- and small-signal parameters of the transistors to change throughout the SenseFET measurement cycle.

The transistor behaviour is also affected by velocity saturation in the device as described in Chapter 2, section 2.8.2. Analysing i_{DS} in M_{1B} and factoring in velocity saturation yields:

$$i_{DSM_{1B}} \cong \frac{k'_p}{2\left(1+\frac{v_G - V_t - L\frac{di_L}{dt}}{E_c L_{M_{1B}}}\right)}\left(\frac{W}{L}\right)_{M_{1B}}\left(v_G - V_t - L\frac{di_L}{dt}\right)^2 \quad (4.14)$$

Channel length modulation can be reduced by increasing the length of the transistor, which reduces the value of λ. From (4.14), increasing the length of the transistor significantly will reduce the net effect of velocity saturation. In (4.14), velocity saturation is represented by the term:

$$\left(1+\frac{v_G - V_t - L\frac{di_L}{dt}}{E_c L_{M_{1B}}}\right) \quad (4.15)$$

The disadvantage of increasing L_{M1B} is that very long transistors will be required to make the $E_C L_{M1B}$ term large enough to drive (4.15) to a negligible value. For this reason, simply altering the device aspect ratio to minimise non-ideal effects will not practically offset the dominance of velocity saturation.

This susceptibility to non-ideal effects suggests that a topological change to the SenseFET would yield more practical solutions than simply upscaling the transistor aspect ratios to impractical values.

4.4.2.2 Improvements from a cascode topology

The proposed circuit in Figure 4.10 addresses the reference SenseFET design shortcomings which arise in a low voltage, 130 nm CMOS process. This circuit consists of two parts, the basic sensing transistor with differential pair of the reference SenseFET, and a secondary network that augments the biasing pair, M_2. The secondary network serves to generate robust bias currents in branch A and branch B which are resistant to variations introduced through non-ideal mechanisms. By stabilising the bias current in branches A and B, the network can more easily equalise the voltages at nodes A and B, more closely approximating the ideal SenseFET behaviour.

Transistor pairs M_3, M_4, and M_5 form a current biasing network in a folded cascode configuration. This configuration is called a folded cascode because the additional network is implemented in parallel with original biasing network as shown in Figure 4.11.

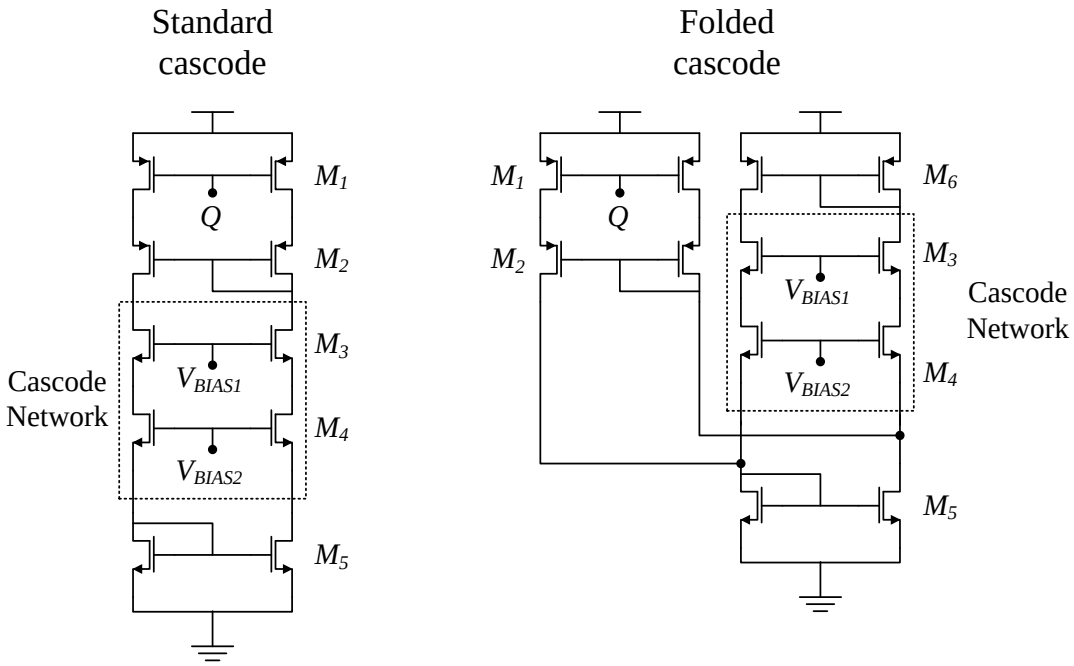

Figure 4.11. Topological difference between standard and folded cascode configurations.

Figure 4.11 shows the difference between the standard and folded cascode configurations. In the standard configuration, the additional network is introduced in series between the supply rails. In the standard configuration, the total voltage headroom available for the differential pairs is distributed along transistor pairs M_1 to M_5. This decreases the available headroom for analogue signal swing. Additionally, any deviation in the voltage at a node in the branches will affect all devices if non-ideal device behaviour is considered. This is demonstrated in section 4.4.2.1.

In the folded configuration, the additional network is implemented as a separate parallel network which is connected to the circuit being augmented. The advantages of the folded cascode network is an increase in available headroom for analogue signal swing and a degree of bias isolation between the parallel networks. In the folded cascode network, the total voltage headroom is now only split between pairs M_1, M_2, and M_3. The number of devices used in the parallel or folded network will no longer reduce the available headroom for M_1, M_2, and M_3. Finally, voltages variations at nodes in the M_1 and M_2 network are isolated from influencing the folded network.

When applied to the SenseFET, every additional transistor pair in a cascode configuration with M_1 and M_2 diminishes the effect of v_L on v_{DS} for pairs M_1 and M_2. By Kirchoff's voltage law (KVL) the sum total of v_{DS} over each cascode pair must be equal to the voltage at node

A (or node B for the corresponding branch). The disadvantage of this approach is that it decreases the headroom available for v_{GS} with each additional transistor pair. The reduced headroom restricts the dynamic range of the sensor by limiting values of v_{GS} required to maintain each device in saturation. This limitation is circumvented by using a folded cascode topology which allows for branch currents to be biased independently of v_L without limiting the headroom for v_{GS} of M_1 and M_2.

The configuration used in Figure 4.10 diminishes the effect of small V_A and velocity saturation on the bias currents in the SenseFET by isolating the biasing network from external stimuli such as v_L. In the reference SenseFET the bias currents are determined by M_1 and M_2, which led to asymmetrical bias currents. The folded cascode bias topology promotes symmetrical bias currents between branch A and branch B. An additional advantage of the folded configuration is that the network formed by M_3, M_4, and M_5 can be implemented without significantly diminishing the supply voltage headroom available to the SenseFET.

4.4.2.3 Cascoded SenseFET operation

Applying (4.7) to bias transistor M_{2B} of the reference SenseFET in Figure 4.4:

$$i_{DSM_{2B}} = \frac{k_n^{`}}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2\left(1 + \lambda\left(L\frac{di_L}{dt} - v_{DS1}\right)\right) \tag{4.16}$$

Equation (4.16) shows that the bias current generated by M_{2B} is susceptible to variation as v_L varies.

If KCL is applied to the source of the same transistor (M_{2B}) in the improved SenseFET of Figure 4.10 then:

$$i_{DSM_{3B}} = i_{DSM_{4B}} + i_{DSM_{2B}} \tag{4.17}$$

$$i_{DSM_{4B}} = i_{DSM_{5B}} \tag{4.18}$$

$$i_{DSM_{2B}} = i_{DSM_{3B}} - i_{DSM_{5B}} \tag{4.19}$$

Equation (4.17) shows that the current at the source of M_{2B} is now determined not only by M_{2B}, but by the difference between i_{DSM3B} and i_{DSM4B}. Additionally, i_{DSM4B} is determined by M_5. Substituting (4.18) into (4.17) yields (4.19), which shows that i_{DSM2B} is determined by M_3 and M_5.

i_{DSM5} is determined by the aspect ratio of M_5 and the bias voltage v_{BIAS2}. The gates of M_3 and M_4 are also tied to the drain of M_5, providing a stable v_{GS} to M_3 and M_4. In the network formed by M_3, M_4, and M_5, i_{DSM2} is determined by M_3 and M_5, with M_4 serving as a buffer to isolate M_5 from variations in branch B. This is achieved by tying the gate of M_4 to the drain of M_{5A}. Branch A of the SenseFET is not directly connected to the external current being measured at node B and is thus less affected by any variations introduced in branch B.

The design of the cascoded SenseFET focuses on creating a biasing network that is independent of the inductor current being measured. If the bias currents in the secondary network (M_3 to M_5) are chosen to be an order of magnitude larger than the current variance in the SenseFET, then from (4.19), the bias current will be predominantly determined by M_3 and M_5.

The result of bias currents which are resilient to variations in i_{DSM1} is that the SenseFET is better able to hold nodes A and B at similar voltages.

4.4.3 Implementation

4.4.3.1 Design constraints

Process parameters, which influence design constraints, are confidential under the NDA with MOSIS.

As with the design constraints of the reference SenseFET in section 4.4.2.1, the SenseFET design is constrained by the choice of power transistor M_{P1}. For ease of comparison, the cascoded SenseFET is designed for the same DC-DC converter circuit used in the reference design. The reference design makes use of a 1 µH inductor being switched at a frequency of 10 MHz with V_{DD} = 1.2 V.

4.4.3.2 Cascode SenseFET detail design

The three primary parameters that need to be chosen to design the cascoded SenseFET are R_m, K, and the bias current in the folded cascode network.

Equation (4.3) is applied to determine the scaling factor, K, of the SenseFET. If K = 1000 then this allows for µA currents in the sensor circuit compared to the mA currents that will be measured. For the maximum possible inductor current of 600 mA, the transresistance gain

of the SenseFET is chosen such that the maximum output, v_{SENSE}, is less than V_{DD}. With a maximum V_{DD} of 1.2 V and R_m = 2, v_{SENSE} is constrained by (3.1) to a maximum of 1.2 V.

Applying (4.3) and assuming $\frac{i_L}{K} \gg i_{DSM_{1A}}$, yields R_{SENSE} = 2 kΩ.

The bias current in the cascode network is determined by M_5. M_5 is designed such that:

$$I_{DSM5} = I_{DSM4} = I_{DSM3} = 100\ \mu A \tag{4.20}$$

This ensures that the bias currents in the cascode are an order of magnitude larger than the currents in the SenseFET. Direct application of (2.15) is used to determine the aspect ratio of M_5.

M_3, M_4, and M_6 are chosen so that the required v_{GS} to keep the transistors in saturation is 100 mV higher than the device threshold voltage (350 mV) at a bias current of 100 µA. This is done through direct application of (2.15). Finally, pairs M_1 and M_2 have their aspect ratios set equal to M_3. This is done because the branch currents are now primarily determined by the cascode network and not the differential pairs in the SenseFET.

Transistor ratios were chosen to have the minimum length allowed by the 8HP process. Current-switching transistors M_{P1} to M_{P4} were chosen to have an aspect ratio of 4000, but after simulation there was no distinct difference in performance between aspect ratios of 1000 and 4000. The result of this is a reduction in K from 1000 to 250.

Once initial transistor aspect ratios and bias voltages for all devices were determined analytically, gate level simulation was used to refine bias voltages. The aspect ratio and the bias voltages for the cascoded SenseFET are summarised in Table 4.5.

Table 4.5 Summary of cascode SenseFET aspect ratios and biasing.

Parameter	**Aspect ratio**	
	(W/L)	nm
M_{P1}, M_{P4}	1000	120000/120
M_{P2}, M_{P3}	666.6	80000/120
M_S	4	1600/400
M_1, M_2, M_3, M_4. M_6	6	720/120
	Voltage	
V_{BIAS1}	720 mV	
V_{BIAS2}	400 mV	
	Resistance	
R_{SENSE}	2 kΩ	

Table 4.5 summarises the aspect ratios and biasing used in the cascode SenseFET design. Aspect ratios are expressed in terms of the dimensionless ratio $\left(\frac{W}{L}\right)$ and as a ratio of width and length in nm. The bias voltages are expressed in mV.

4.4.4 Layout

The cascoded SenseFET layout is provided in Figure 4.12.

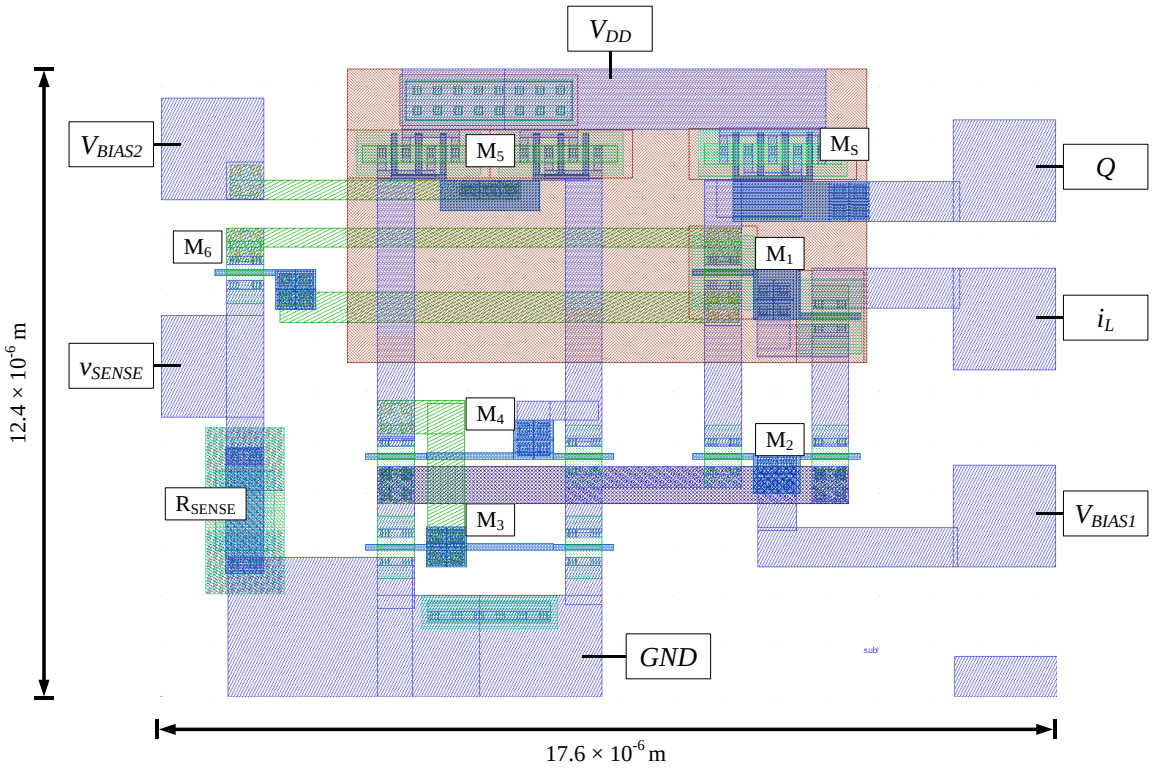

Figure 4.12. CAD Layout of the Cascoded SenseFET.

Figure 4.12 is an annotated diagram of the improved SenseFET layout. The input and output ports are indicated, in addition to the location of the transistors as per Figure 4.10. As with the reference SenseFET, the inputs and outputs are arranged on the perimeter of the SenseFET for ease of integration.

To improve resilience to process variations, transistor pairs are grouped as closely as possible. PFET devices are grouped in the same *n*-type well reducing the effect of variations from different *n*-type wells. Wide transistors, such as M_S and pair M_5, make use of a fingered gate structure which allows for a more compact device layout. Compact layouts are less susceptible to process variations because the gradient of the variation is less severe over the span of the layout.

The total dimensions of the improved SenseFET are 17.6 µm by 12.4 µm, with a total area of 218 μm^2.

4.4.5 Simulated performance

As with the reference SenseFET, the cascoded SenseFET is characterised by its branch current symmetry and its transresistance gain.

4.4.5.1 Cascoded SenseFET current branch symmetry

The branch symmetry can be characterised by considering the transient behaviour of the current in each branch as the current through the inductor changes. The simulated branch currents over a single cycle for the cascoded SenseFET are shown in Figure 4.13.

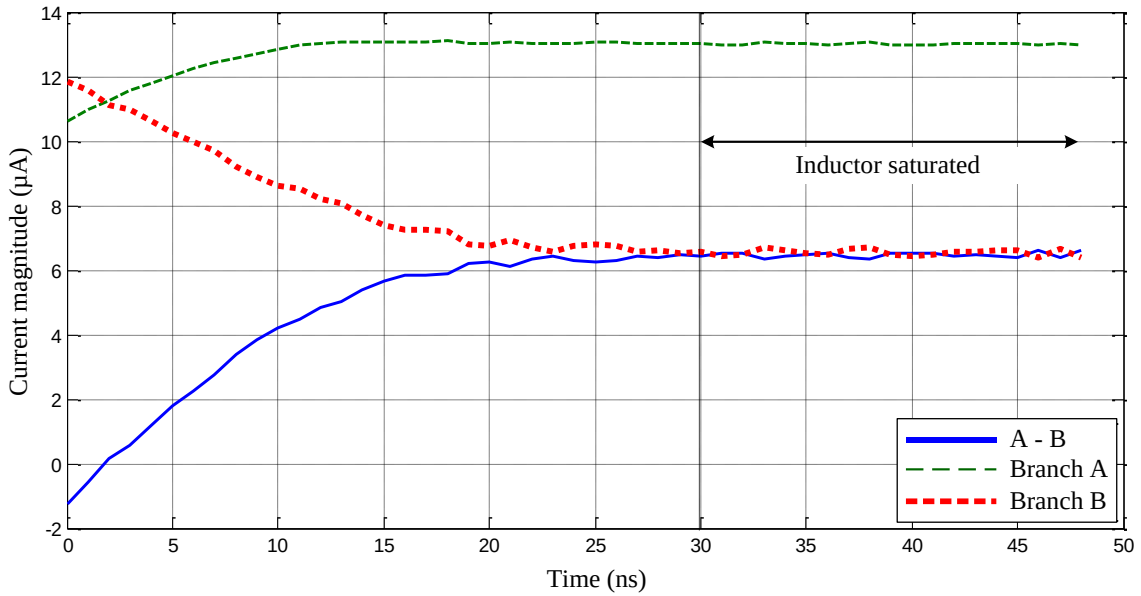

Figure 4.13. Branch currents in cascoded SenseFET.

Figure 4.13 shows the currents in the branches of the cascoded SenseFET as well as the absolute delta between the branch currents. The switching cycle starts at 0 ns. At 0 ns, both branches are at a bias current of approximately 10 µA. As the cycle progresses and the inductor current increases, the branch currents start to diverge from the designed bias current. The current in branch A increases and the current in branch B decreases. After approximately 15 ns, the branch currents cease to diverge and stabilise.

The divergence of the currents in branch A and branch B characterised calculating the delta between branch A and branch B currents. At the start of the switching cycle, the difference is 1 µA, by 15 ns the difference has increased approximately linearly to 6 µA. Since the currents stabilise after 15 ns, so does the difference between branch currents. Divergent currents are an indication of branch asymmetry.

4.4.5.2 Transresistance gain

The SenseFET's overall performance can be quantified by evaluating the transresistance gain of the current sensing circuit as given by (4.6).

In (4.6), R_m is the transresistance gain, v_{SENSE} is the SenseFET voltage output, and i_L is the current through the inductor. R_m has units of V/A. V/A is a more insightful use of units than the simplification of V/A to Ω. By analysing the behaviour of the SenseFET's R_m over a

switching cycle, it is possible to characterise the linearity of the sensor. A simulated plot of R_m for the cascoded SenseFET is shown in Figure 4.14.

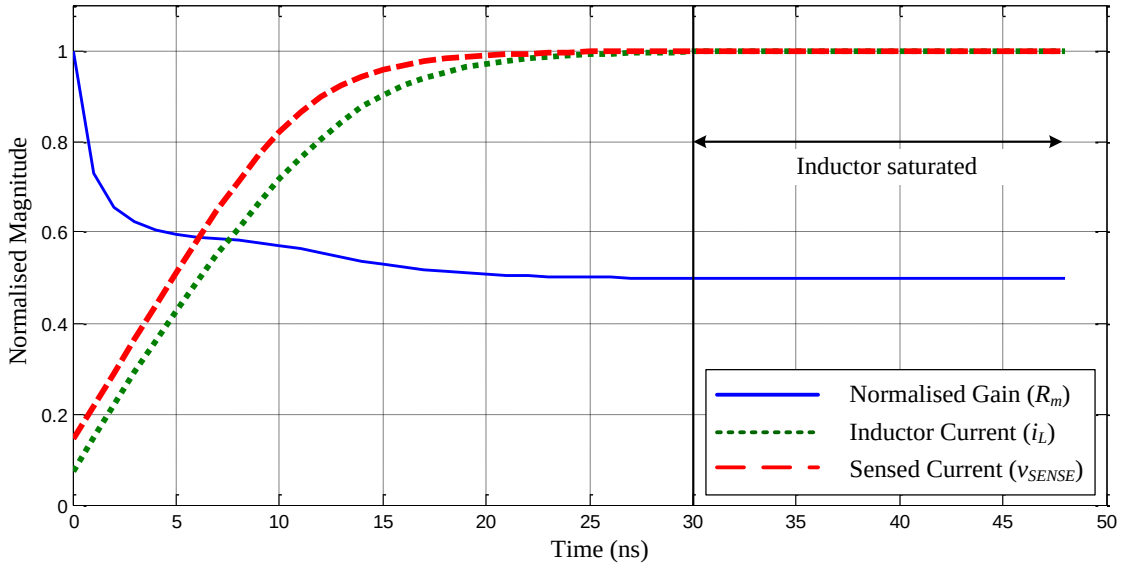

Figure 4.14. Transresistance gain (R_m), normalized inductor current, and sensed current of the cascoded SenseFET.

Figure 4.14 is a normalised plot of R_m, v_{SENSE}, and i_L. The plots have been normalised to emphasise the deviation of v_{SENSE} relative to i_L. During the first 4 ns of the cycle, the gain of the cascode SenseFET is highly non-linear. The high non-linearity is partially attributed to a discontinuity in the data at 0 ns. At 0 ns, the SenseFET output, v_{SENSE}, is non-zero. i_L at 0 ns is close to 0 mA. As i_L increases though the cycle, the normalised gain rapidly approaches 0.5. After 5 ns in the cycle, R_m varies by less than 10 % from its nominal value.

In comparison to the reference SenseFET output in Figure 4.9, the SenseFET with cascoded biasing has an improved dynamic response to the behaviour of the inductor. The gain profile varies by 10 % as the inductor approaches saturation.

4.5 FABRICATION

4.5.1 Overview

Fabrication of the prototype circuits was through the MOSIS educational program (MEP). This program offers students at academic institutions avenues to prototype integrated circuits at no cost to the student.

4.5.2 Fabrication preparation

Several prerequisites must be fulfilled before the chip can be manufactured. These prerequisites include the acceptance of research proposals for the circuits to be manufactured as well as compliant CAD files which describe the design layout.

After schematics were finalised, layouts were generated and verified using LVS and DRC. The silicon die was shared with other research projects within the research group as part of a multi-project wafer. All designs had to be collated into a single set of design files for the entire chip. Once designs had been verified for manufacturing, a packaging solution was specified. The manufactured prototype was packaged in a 52 pin QFN package. The manufactured die was wire-bonded to the pins of the package. MOSIS also provided unpackaged dies for direct chip measurements.

To accommodate all the research group circuits on a single die, the manufactured die had dimension of 2.5 mm by 2.5 mm, with a total area of 6.25 mm^2.

4.5.3 Fabricated integrated circuit

The fabricated die is shown in Figure 4.15.

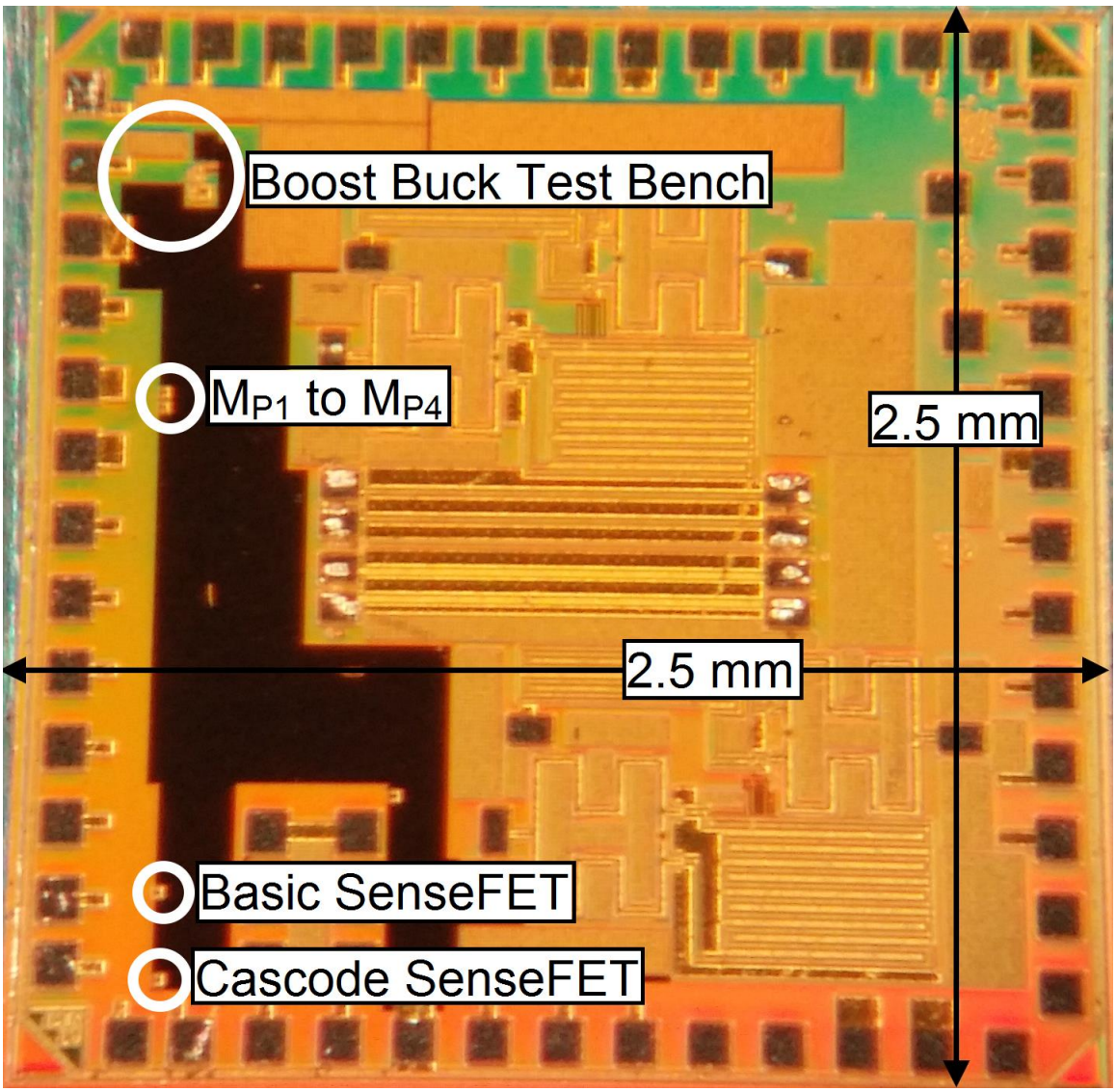

Figure 4.15. Annotated photograph of the manufactured die.

Figure 4.15 is an annotated photograph of the manufactured die. Annotations are provided to indicate the dimensions of the die, the locations of prototype circuits, and the location of the power transistor test circuit. Unmarked circuits and elements are research projects which share the die space.

The DC-DC converter (M_{P1} to M_{P4}) used by the reference and cascoded SenseFETs was implemented separately. This allowed for the same converter circuit to be used to measure and test both SenseFETs.

4.6 MEASUREMENT SETUP

4.6.1 Overview

The measurement setup consists of three distinct components, namely the internal test circuitry, external test circuitry, and measurement equipment.

The test setup and methodology is detailed in Chapter 3, section 3.10. This section provides additional information regarding the practical implementation of the test circuits and measurement setup.

4.6.2 Additional integrated circuitry for measurement

Figure 3.4 is reproduced in Figure 4.16.

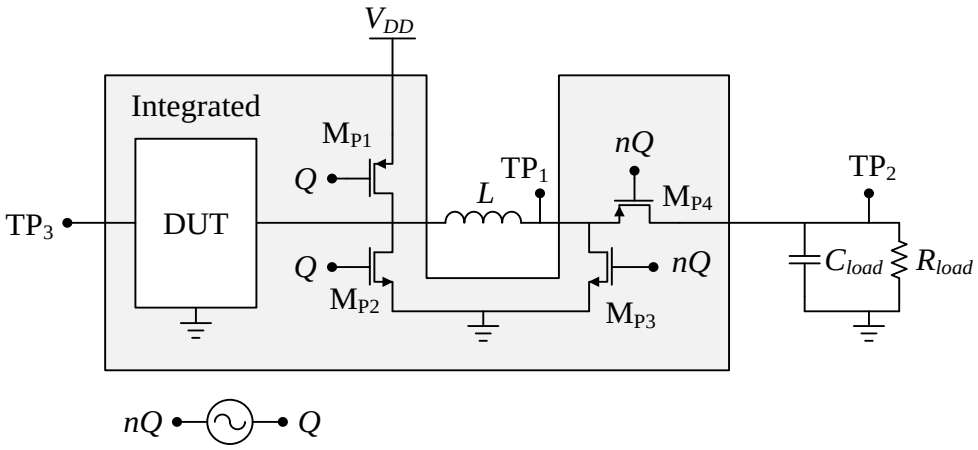

Figure 4.16. Test setup for measuring SenseFET characteristics.

Figure 4.16 shows the test circuit used to measure the SenseFET characteristics. In addition to describing the test setup, the power transistors used to implement the non-inverting DC-DC converter are labelled to correspond with the SenseFET schematics Figure 4.4 and Figure 4.10. The design of these power transistors is described in section 4.3.3.2.

4.6.3 Additional external circuitry for measurement

An overview of the external test circuitry is shown in Figure 4.17.

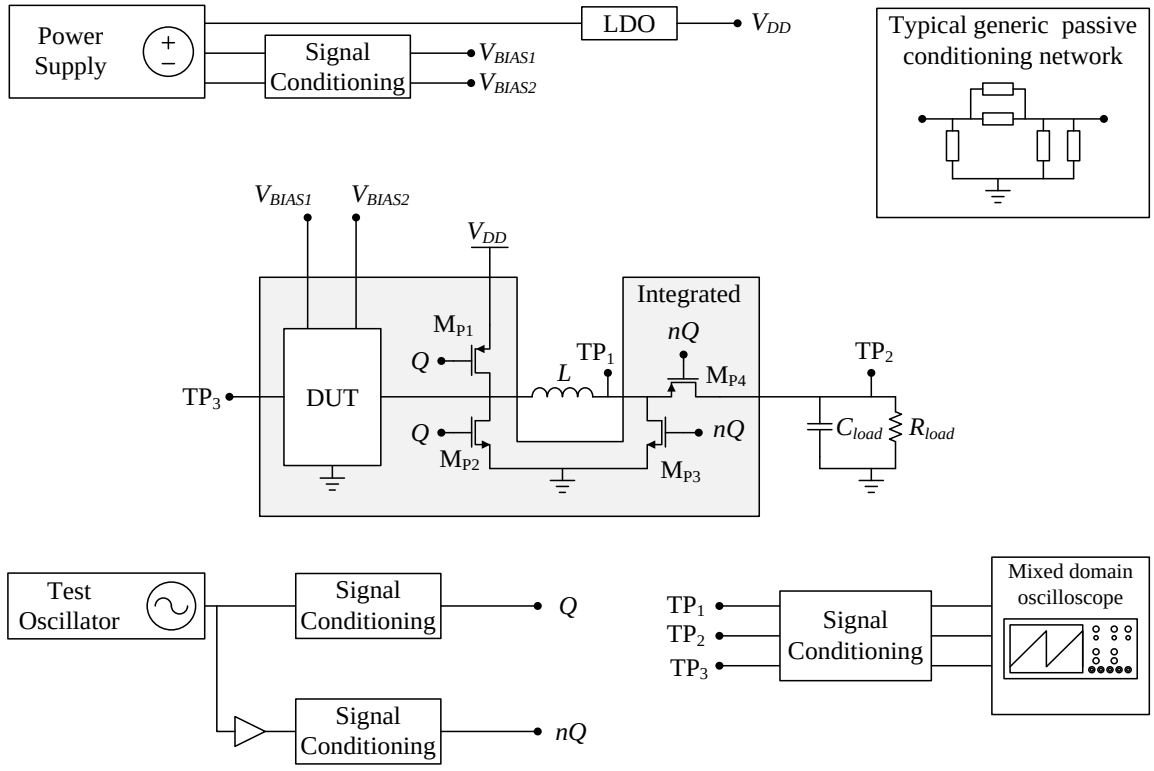

Figure 4.17. Simplified overview of the external test circuit.

Figure 4.17 shows a simplified diagram of the external test circuitry. A multi-output digital power supply provides power for V_{DD} and the SenseFET bias voltages, V_{BIAS1} and V_{BIAS2}. The test oscillator signal is sourced from a signal generator. An inverter is used to generate nQ from Q. Test signals TP_1 to TP_3 are captured using a MDO. The test circuit makes use of a generic passive conditioning network where an external device interfaces with a signal on the board. The conditioning networks all make use of the same general topology but vary from interface to interface. The external test circuitry is detailed in Addendum B.

Schematics and layout of the PCB were done in Altium Designer[9].

[9] Altium Designer (http://www.altium.com/) is an advanced and comprehensive CAD package for designing PCBs.

4.6.4 Printed circuit board

The printed circuit board shown in Figure 3.2 is reproduced in Figure 4.18.

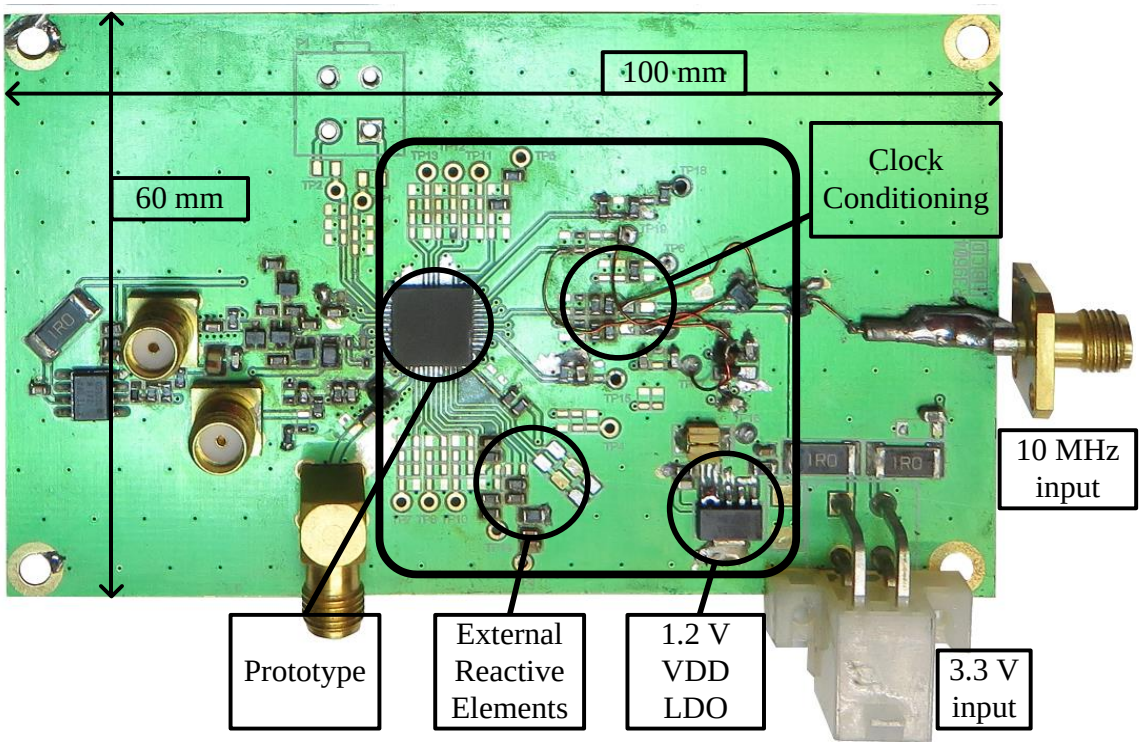

Figure 4.18. Photograph with dimensions of the PCB used to test the prototype IC.

Figure 4.18 is a photograph of the test PCB with dimensions indicated in mm. The external test circuitry and IC are bordered by the rounded square.

4.6.5 Laboratory setup

A photograph of the laboratory test setup is shown in Figure 4.19.

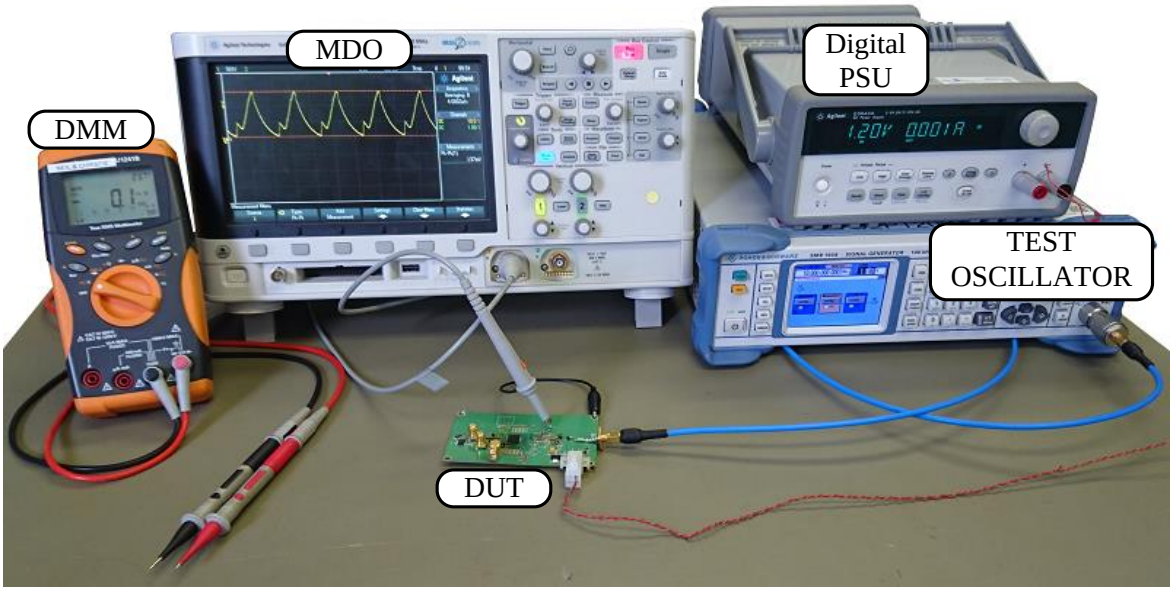

Figure 4.19. Photograph of laboratory setup.

Figure 4.19 is an annotated photograph of the laboratory test setup for Test 1. Indicated are the test PCB of Figure 4.18, the digital power supply, the DMM, test oscillator, and the MDO used to capture data.

4.7 CONCLUSION

This Chapter provides the design detail and fabrication of the reference and cascoded SenseFETs. NFET and PFET devices in the IBM 8HP BiCMOS process are also characterised to derive the extent of channel length modulation in the process. The design of the power transistors used in the DC-DC converter is presented, and the fabrication of the prototype chip is discussed. Finally, the Chapter discusses additional aspects of the measurement and test setup introduced in Chapter 3.

Process characterisation was performed to determine the extent of measurable non-ideal effects in the transistors at the operating point of interest. Characterisation showed that channel length modulation was significant. Further analytical evaluation of the effect of non-ideal device behaviour on SenseFET operation showed that other effects such as velocity saturation can impact the linearity of the sensing circuit.

A reference SenseFET was designed using information from the literature. This SenseFET serves to form a baseline against which any improvements can be benchmarked. The design procedure is presented as well as the design detail. Simulation results are presented which

characterise the performance of the design. This characterisation was used to develop the improved design.

An improved SenseFET design is presented utilising information gained from analysis of the reference SenseFET and knowledge of folded cascode networks. This Chapter presents the improved SenseFET design and motivates design decisions. The final improved design is presented, alongside simulation results which characterises design performance.

A brief overview of the process followed to have the prototype designs manufactured under the MEP on a multi-project wafer.

Chapter 3 provided detail on the test and measurement methodology. Chapter 4 expands on this by focussing on the practical implementation of the test methodology.

CHAPTER 5 DATA ANALYSIS

5.1 CHAPTER OVERVIEW

This Chapter presents the study's data collection and analysis. The data collection is detailed, and the data processing, measurement from data, analysis of the measurements, and observations from measurements are presented and discussed.

Data collection focuses on the methods and equipment used to capture data from the test and measurement setup. Data processing comprises the methodology employed to condition and process the data into a format which may be measured.

Processed data from the reference and cascoded SenseFET prototypes are presented and used to derive measurements of the prototype circuits performance. These measurements are analysed and observations are made and presented.

5.2 DATA COLLECTION

The measurement methodology is described in Chapter 3 and the measurement setup is described in Chapter 4. Chapter 3 describes two test procedures. The primary testing procedure focussed on characterising the performance of the reference and cascoded SenseFETs. A secondary test procedure is described which tests an implementation of the reference SenseFET in a CMC buck-boost converter.

For the primary test, the SenseFET output and other circuit parameters were sampled and captured from the prototype using a MDO and test circuitry. The measurement setup from Figure 3.4 is repeated in Figure 5.1.

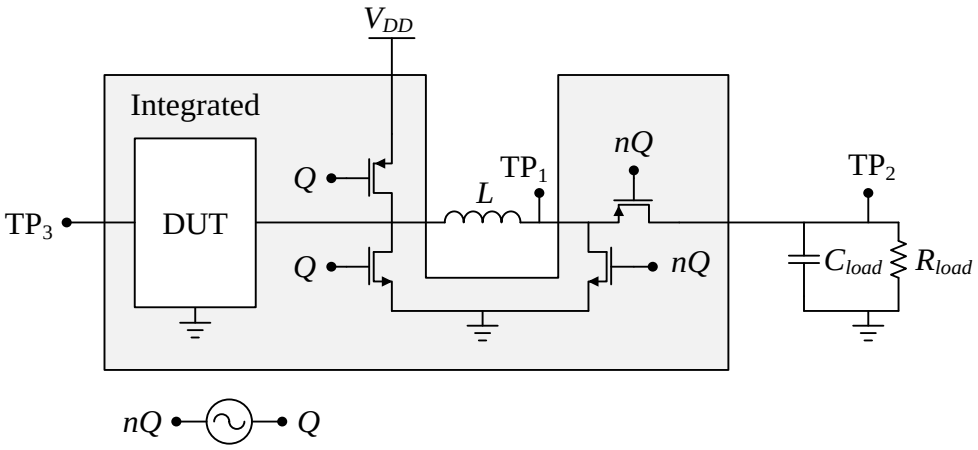

Figure 5.1. Test setup for measuring reference and cascode SenseFETs.

Figure 5.1 is a diagram of the test setup used to evaluate the reference and cascode SenseFET prototypes. Voltage data is captured at TP_1, TP_2, and TP_3. The test setup comprises the SenseFET to be tested and a buck-boost converter test circuit. The primary function of the test circuit is to simulate the inductive element in a DC-DC converter. The current through the inductor is measured both by the SenseFET to be tested and an external instrument.

For the convenience of the reader, the secondary test setup from Figure 3.5 is repeated in Figure 5.2.

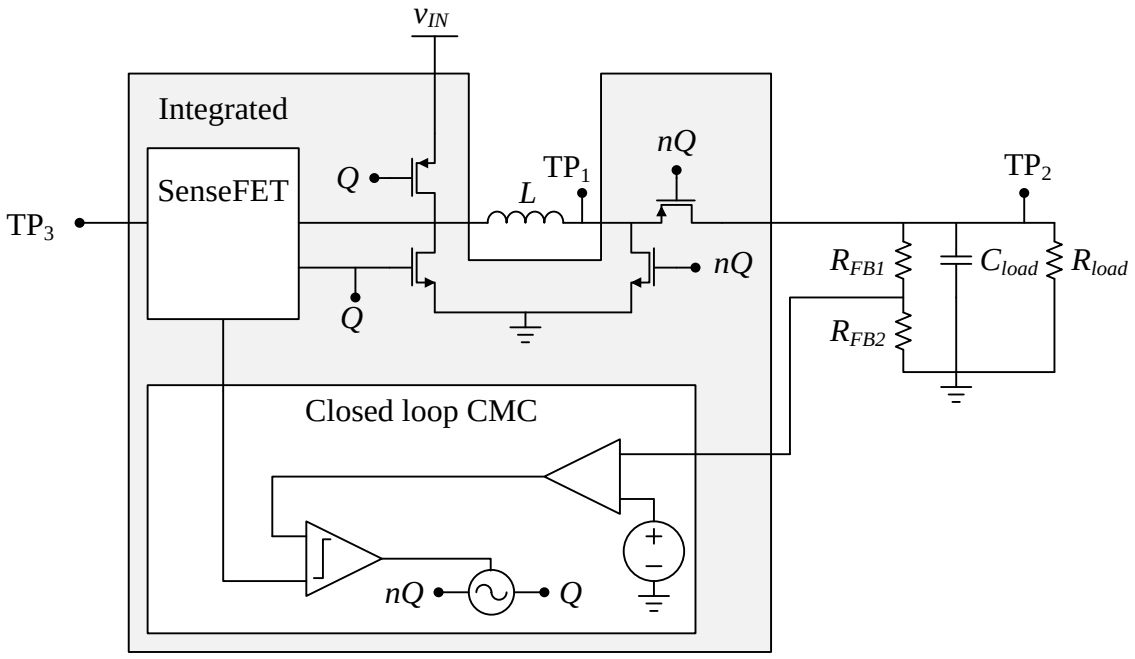

Figure 5.2. Test setup for measuring CMC buck-boost converter performance.

Figure 5.2 expands on the test setup of Figure 5.1 by including the reference SenseFET in an integrated CMC buck-boost converter. The SenseFET output, v_L, and converter output are all sampled and captured at TP_3, TP_1, and TP_2 respectively.

Captured data was stored and transferred to a MATLAB computing environment where the data was sorted and processed for measurement. The MATLAB scripts which processed the raw data are provided in Addendum A.

5.3 DATA PROCESSING

The data processing approach is shown as a flow diagram in Figure 5.3.

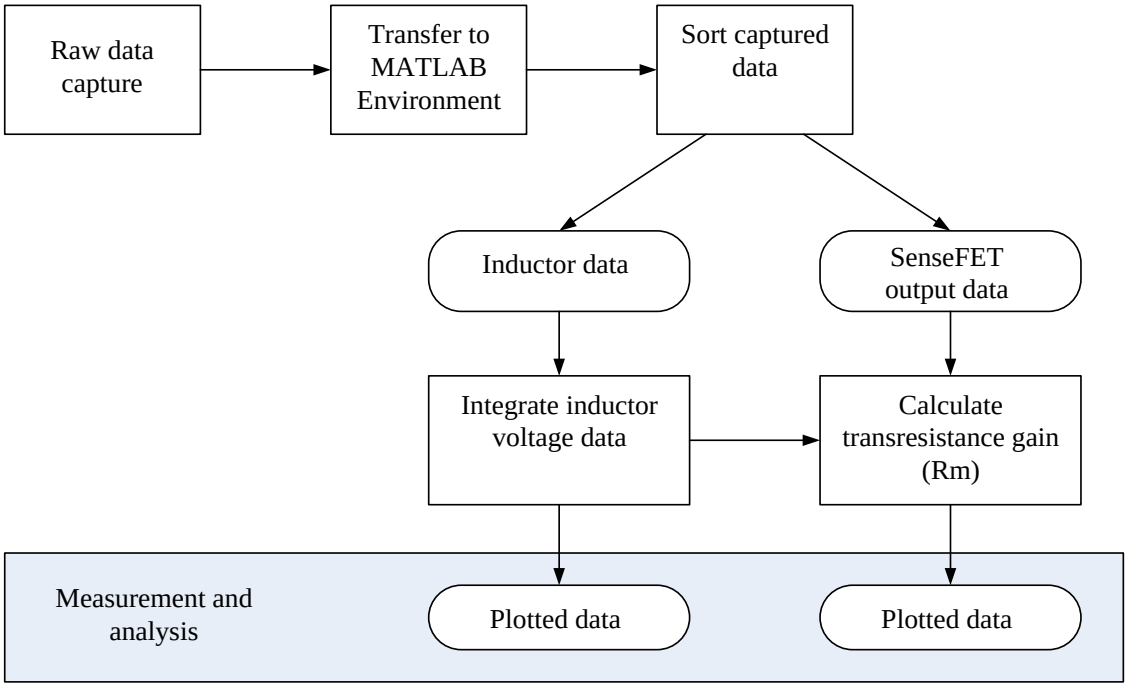

Figure 5.3. Flow diagram describing processing of captured data.

Figure 5.3 presents a flow diagram describing the processing and sorting of the captured data prior to measurement. Raw voltage probe data is captured on the MDO and transferred to a personal computer within a MATLAB software environment. The captured data is subsequently sorted into different data sets, with each set representing a channel of the MDO. Each dataset was processed and plotted, and the plotted data was used to measure the SenseFETs performance.

The SenseFET gain is given by (3.1), repeated below:

$$R_m = \frac{v_{SENSE}}{i_L} \tag{5.1}$$

Equation (5.1) is used in Chapter 4 to quantify the transresistance gain of the SenseFET in a simulation environment. (5.1) is also used on captured data to determine the transresistance gain of the SenseFETs.

v_{SENSE} is a direct measurement of the SenseFET output. i_L is not measured directly but is derived from the inductor voltage characteristic using (3.2), repeated below:

$$i_L = \frac{1}{L}\int_{t0}^{t1} v_L(\tau)d\tau \tag{5.2}$$

From (5.2), i_L may be derived by numerically integrating v_L over a single switching cycle. The numerical integration technique used to calculate i_L is the cumulative trapezoidal technique. The cumulative trapezoidal algorithm used is part of the MATLAB standard function library. The MATLAB script is provided in Addendum A.

The calculated i_L, directly captured v_{SENSE}, and time data from the capture sample rate are used to evaluate (5.1) and (5.2) and generate plots of the SenseFET behaviour over a switching cycle.

5.4 TEST 1 MEASUREMENT DATA

This section presents data captured from the primary test setup. The captured outputs of the SenseFETs (v_{SENSE}), the captured inductor voltage (v_L), and the inferred inductor current (i_L) from numerically integrating v_L are presented. Data for the reference SenseFET and cascoded SenseFET are presented separately.

5.4.1 Reference SenseFET

The raw data captured for the reference SenseFET is shown in Figure 5.4.

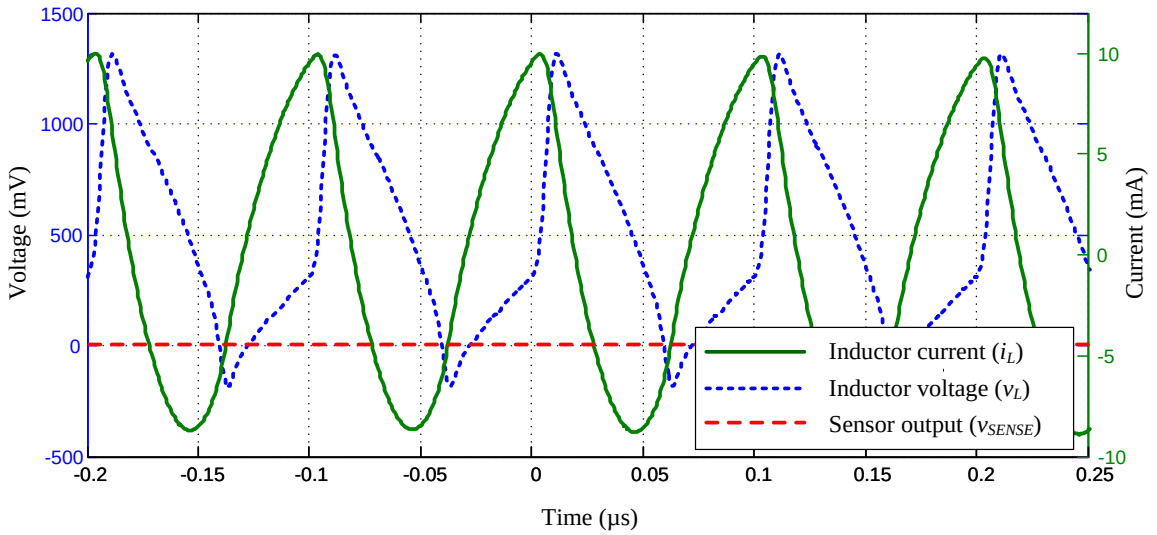

Figure 5.4. Unprocessed data captured from the reference SenseFET.

Figure 5.4 plots the captured data for the reference SenseFET. The graph plots i_L, v_L, and v_{SENSE} of the reference SenseFET. The plot legend identifies each trace of the plot. The inductor plot is created by numerically integrating v_L over each sampling interval.

The inductor voltage and current mirror the cyclic behaviour of the buck-boost converter test bench used to charge and discharge the inductor. The period of the clock driving the FET switches in the converter was 100 ns. The inductor current reverses every 50 ns as the inductor charges from V_{DD} and discharges into the load.

The reference SenseFET had no measurable output. The lack of output was consistent across multiple prototype dies, indicating an unfortunate design problem with the prototype. This is further discussed in Section 5.7.

5.4.2 Cascoded SenseFET

The raw data captured for the cascoded SenseFET is shown in Figure 5.5.

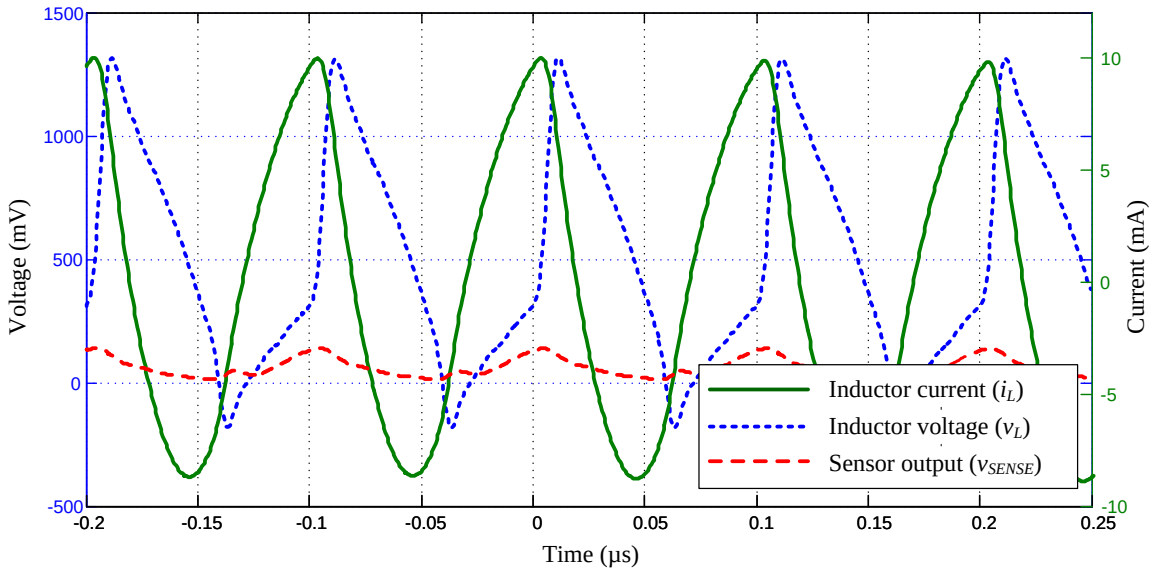

Figure 5.5. Unprocessed data captured from the cascoded SenseFET.

Figure 5.5 plots the captured data for the cascoded SenseFET. The graph plots i_L, v_L, and v_{SENSE} of the cascoded SenseFET. The plot legend identifies each trace of the plot. The inductor plot is created by numerically integrating v_L over each sampling interval.

The inductor voltage and current mirror the cyclic behaviour of the buck-boost converter test bench used to charge and discharge the inductor. The period of the clock driving the FET switches in the converter was 100 ns. The inductor current reverses every 50 ns as the inductor charges from V_{DD} and discharges into the load.

The cascode SenseFET output, v_{SENSE}, adopts a cycle behaviour which increases and decreases every 50 ns. This behaviour bares a notable similarity to the inductor current. The cascode SenseFET output is isolated in Figure 5.6.

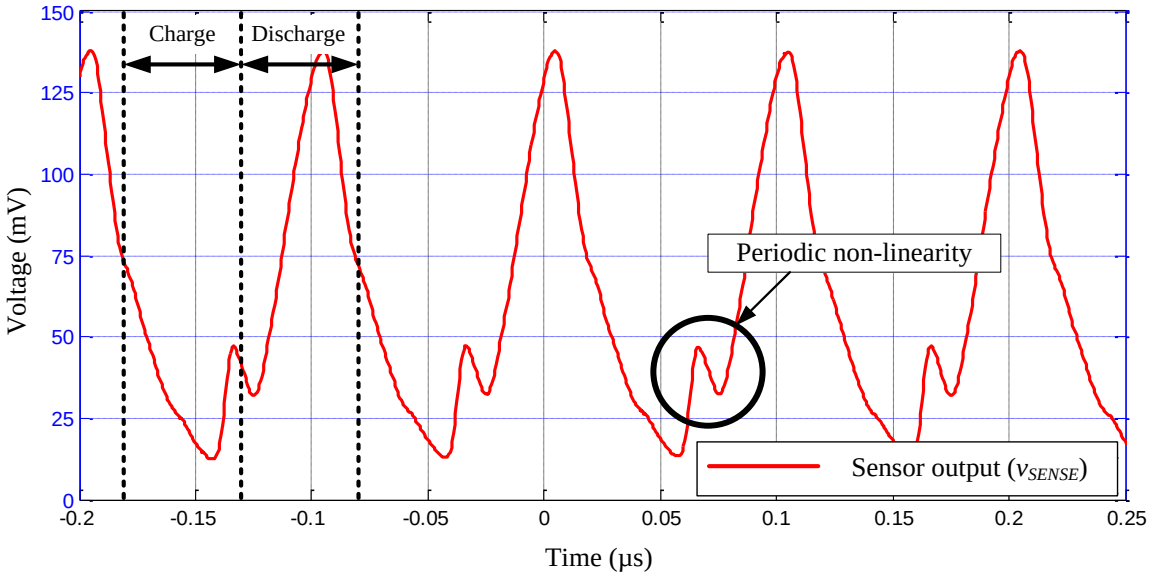

Figure 5.6. Annotated plot of v_{SENSE} for the cascoded SenseFET.

Figure 5.6 plots v_{SENSE} for the cascode SenseFET in isolation. This plot is annotated to indicate the charge and discharge boundaries and a periodic non-linearity in the SenseFET output. The charge and discharge boundaries correspond to a change in inductor voltage polarity. The non-linearity in the output corresponds to a transition from charge to discharge. This behaviour is further discussed in Section 5.6 and Section 5.7.

5.5 TEST 2 MEASUREMENT DATA

Test 2 is an extension of Test 1, with the reference SenseFET integrated into CMC buck-boost converter. The failure of the reference SenseFET is the primary reason that there was no meaningful result from Test 2. Failure analysis is focused on the reference SenseFET as this directly affects the hypothesis as stated in Chapter 1, section 1.3.

5.6 PROCESSED DATA AND OBSERVATIONS

This section presents the same data as that of Section 5.4 but with the data modified to indicate the transresistance gain (R_m) of the SenseFETs.

5.6.1 Reference SenseFET

The reference SenseFET prototype had no measurable output, as such, the only possible observation is that the reference SenseFET output was 0 V. The reference SenseFET prototype behaviour and possible failure modes are further discussed in Section 5.7.

5.6.2 Cascoded SenseFET

The basis for the analysis of the cascoded SenseFET performance is plotted in Figure 5.7.

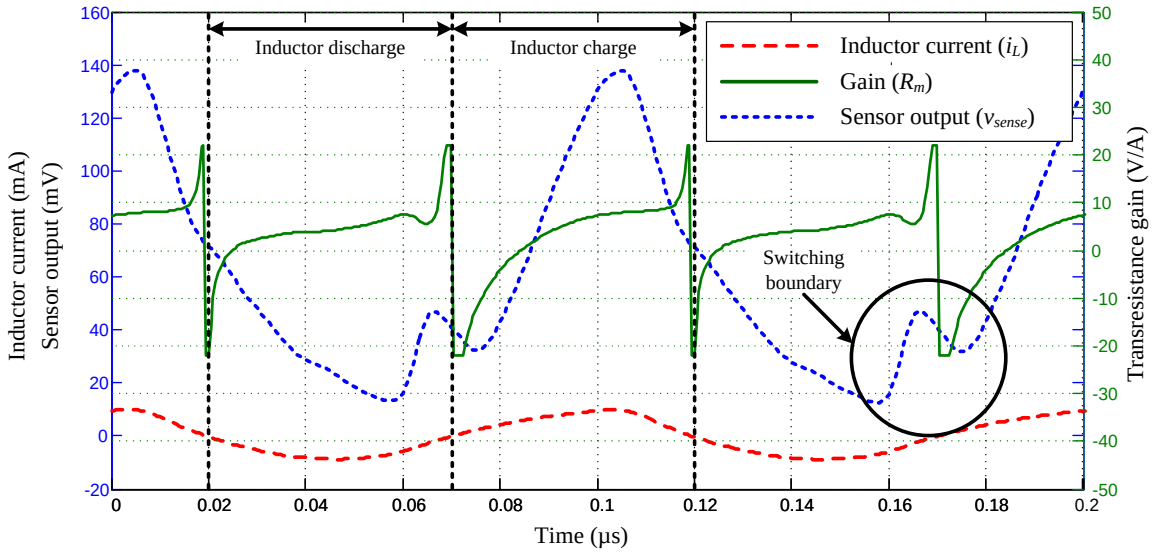

Figure 5.7. Cascode SenseFET performance over a complete switching cycle.

Figure 5.7 plots the cascoded SenseFET output (v_{SENSE}), inductor current (i_L), and the transresistance gain (R_m) of the SenseFET. v_{SENSE} and i_L are the same data plotted in Figure 5.5 and Figure 5.6. Figure 5.7 is annotated to indicate the inductor charge and discharge phase of the switching cycle. The discontinuity present in R_m at the switching boundary is also indicated. R_m is derived from application of (5.1) to v_{SENSE} and i_L. As the inductor discharges into the RC load, i_L relative to the SenseFET input decreases to 0 mA. Once the inductor transfers energy to the load, the current reverses relative to the SenseFET input.

This process of current reversal in the inductor results in the value of i_L passing through 0 mA relative to the SenseFET input. This transition introduces discontinuity into the gain characteristic at the switching boundaries present in the test circuit. The division by zero at the discontinuity is limited during the calculation of R_m. This approach allows for the plot of R_m to be readable at regions of interest.

R_m has two distinct characteristics in the respective charge and discharge phases. During the discharge phase, the SenseFET operates with a gain of 5 V/A. The gain stabilises once the SenseFET has recovered from the switching transient which is present at every switching

interval boundary. During the charge phase the achieved gain is similar to the discharge phase, 5 V/A, but the SenseFET circuit takes significantly longer to recover from the switching transient.

The behaviour of the cascoded SenseFET as shown in Figure 5.7 is discussed in detail in Section 5.7.

5.7 SENSEFET DATA INTERPRETATION AND ANALYSIS

This section presents the consideration of the results presented in preceding sections and simulation results presented in Chapter 4. The captured data and measured results are compared, and the successes and failures are discussed in detail.

5.7.1 Reference SenseFET

5.7.1.1 Measurement analysis

The reference SenseFET output was 0 V_{DC}. No variance in the output was observed and thus no meaningful measurement is possible.

5.7.1.2 Expected results from simulation

The expected cascode SenseFET gain from simulation is plotted in Figure 4.9, repeated in Figure 5.8.

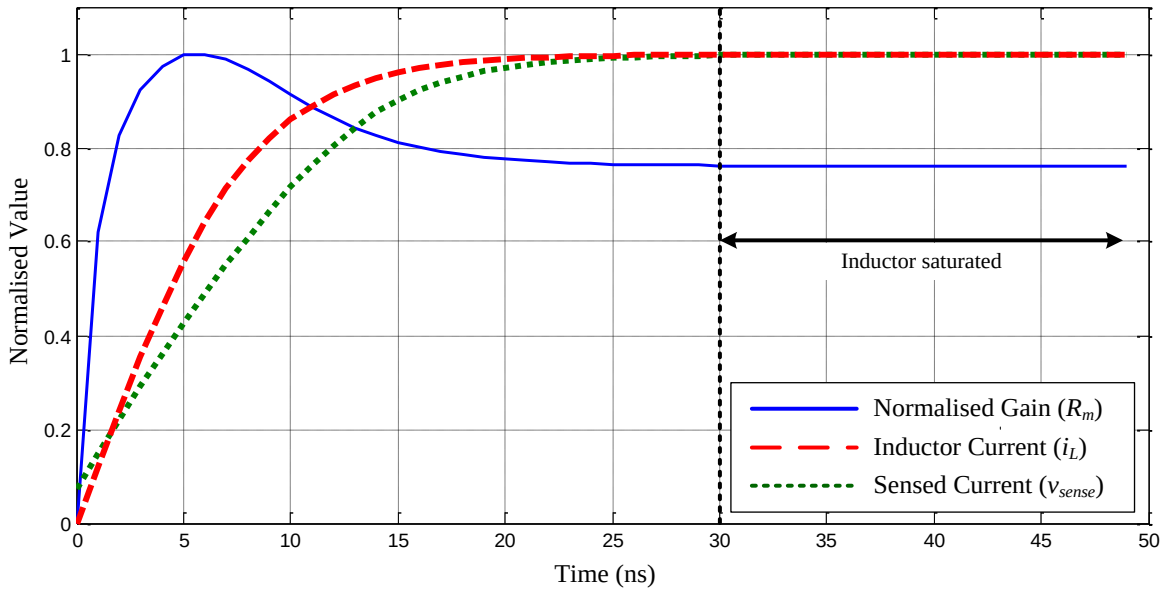

Figure 5.8. Transresistance gain, normalised inductor current, and sensed current of the reference SenseFET.

Figure 5.8 is a normalised plot of R_m, v_{SENSE}, and i_L. The plots have been normalised to emphasise the deviation of v_{SENSE} relative to i_L. During the first 15 ns of the cycle, the gain of the reference SenseFET has a distinctive non-linear behaviour

During the first 3 ns of the conversion cycle the gain is highly non-linear. This non-linearity is associated with the switching boundary of the buck-boost converter test circuit. The gain rapidly increases after 3 ns but overshoots before starting to stabilise after 15 ns.

The gain profile from 2 ns to 15 ns is strongly influenced by v_L modulating the branch currents in the reference SenseFET. The modulating behaviour is clearly expressed in (4.10) and (4.14), repeated for convenience.

$$i_{DSM_{1B}} = \frac{k_p^{`}}{2}\left(\frac{W}{L}\right)_{M_{1B}}\left(v_G - V_t - L\frac{di_L}{dt}\right)^2\left(1+\lambda\left(v_G - L\frac{di_L}{dt}\right)\right) \tag{5.3}$$

$$i_{DSM_{1B}} \cong \frac{k_p'}{2\left(1+\frac{v_G - V_t - L\frac{di_L}{dt}}{E_c L_{M_{1B}}}\right)}\left(\frac{W}{L}\right)_{M_{1B}}\left(v_G - V_t - L\frac{di_L}{dt}\right)^2 \tag{5.4}$$

Equations (5.3) and (5.4) show how the term $L\frac{di_L}{dt}$ modulates the current in branch B of the reference SenseFET through channel modulation and velocity saturation, respectively. The output of the SenseFET is defined by (4.3), restated as:

$$v_{SENSE} \approx R_{SENSE}\left(\frac{i_L}{K} - i_{DSM_{1A}}\right) \tag{5.5}$$

Equation (5.5) expresses v_{SENSE} in terms of R_{SENSE}, i_L, and K. i_{DSM1A} is ideally constant or small relative to $\frac{i_L}{K}$. The gate of M_{1A} is tied to the gate of M_{1B} and variations in the v_{GS} of M_{1B} will manifest at the gate of M_{1A}. The current in M_{1A} is given as:

$$i_{DSM_{1A}} = \frac{k_p^{`}}{2}\left(\frac{W}{L}\right)_{M_{1A}}\left(v_G - V_t - \left(L\frac{di_L}{dt} + v_A\right)\right)^2 \tag{5.6}$$

In (5.6), all parameters are relative to M_{1A}. v_A is the voltage at node A. $L\frac{di_L}{dt}$ is the voltage over the inductor and can vary from 0 V to V_{DD}. Even without including non-ideal transistor behaviour, variation of v_L will result in a variation of i_{DSM1A} in the order of tens of µA. If i_L is in the mA range and K is chosen between 100 and 1000, then the effect of i_{DSM1A} on v_{SENSE} in (5.5) is significant. Both i_{DSM1A} and $\frac{i_L}{K}$ will be in the µA range, resulting in appreciable variation in v_{SENSE}.

5.7.1.3 Possible failure modes

The prototype reference SenseFET output was 0 V_{DC} with no measurable analogue characteristics. This behaviour was present on all the manufactured prototypes, indicating a common fault to the reference SenseFET design as opposed to a manufacturing fault. The reference SenseFET design simulated correctly and the layout was successfully verified using LVS and DRC tools in the Virtuoso environment. The success of CAD based tests but prototype failure indicates a shortcoming in the simulated test environment.

The total area of the reference SenseFET is 163 μm^2, with minimum length features having at least one dimension of 120 nm. This feature scale combined with limited access to both optical and election-scanning microscope equipment has prevented inspection of the physical device at a useful resolution and fidelity. The potential failure modes are inferred from design files, observations of the prototype behaviour, and the IBM 8HP BiCMOS process documentation.

Two possible failure modes are discussed, inadequate layout and insufficient robustness to external voltages exceeding the 8HP process gate oxide breakdown voltage at the input of the SenseFET.

Potential failures caused by inadequate layout practices is considered by inspecting the layout of the reference SenseFET, as is shown in Figure 5.9.

Figure 5.9 is an annotated diagram of the layout of the reference SenseFET with two potential failure regions indicated. Region 1, as indicated in the aforementioned Figure, corresponds to the net which links M_S to M_1. Region 2 corresponds to net which links pair M_1 to M_2. The track in region 1 are minimum width for the process. The tracks in region 2, as indicated on the same Figure, are twice the minimum width for the process. Overly narrow tracks could potentially negatively affect the circuit by reducing the current density in the nets, presenting as a resistive element.

Resistive behaviour on these nets could potentially result in a voltage drop which prevents M_S, M_1, and M_2 from operating in saturation. If current density from the input at node B is too high, heat dissipated in the narrow tracks could lead to catastrophically failure of the

tracks. The cascoded SenseFET avoids this problem by having wider tracks for the equivalent nets.

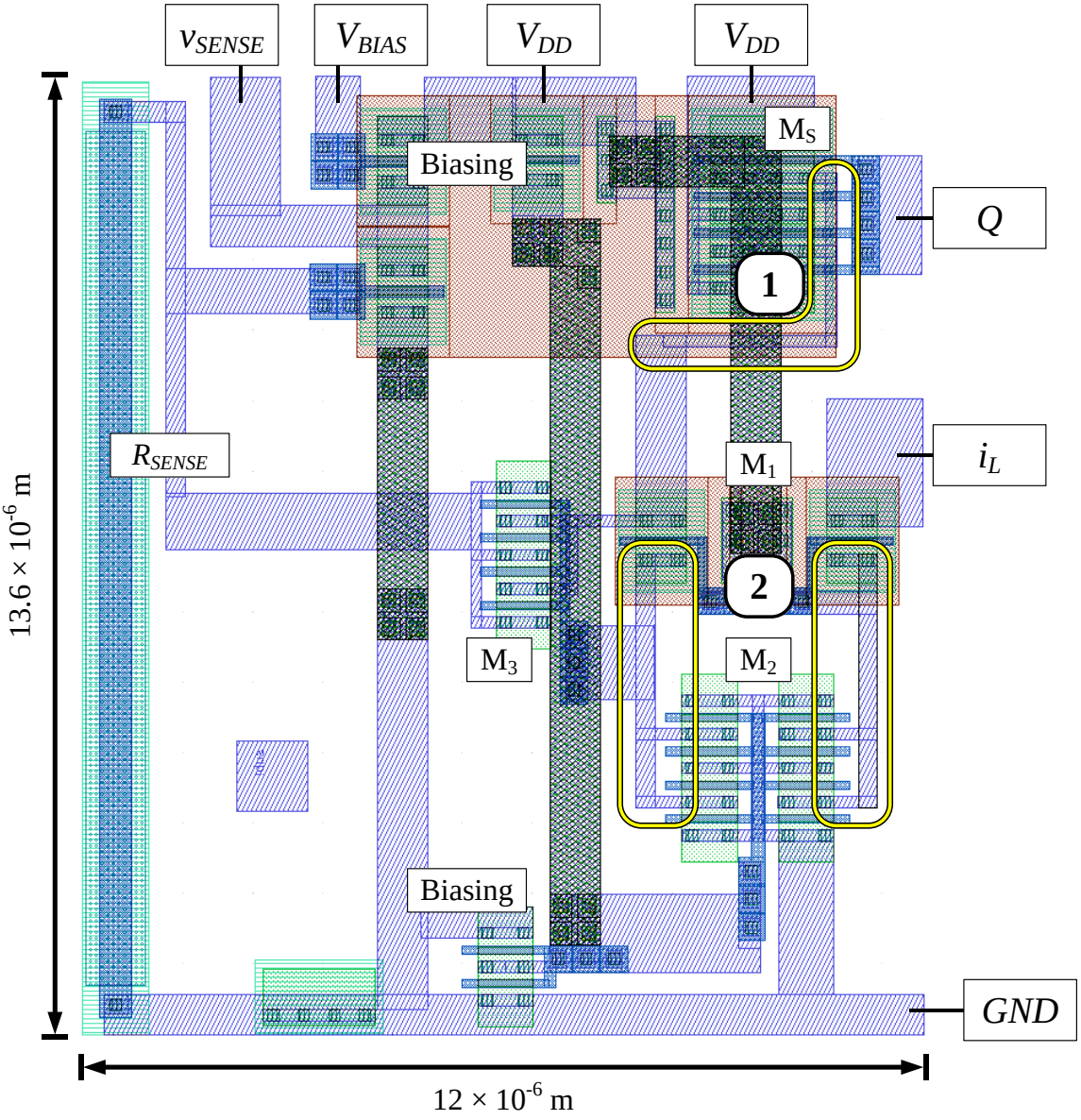

Figure 5.9. Layout of the reference SenseFET with potential layout issues indicated.

Another probable failure mode is if the voltage present at the clock input Q and the inductor terminal (Node B in Figure 4.4) exceeds the gate oxide breakdown voltage of the 8HP process. Such excessive voltage would exist at the switching boundaries during the switching cycle and both Q and v_L could potentially exceed the gate oxide breakdown voltage during the effective instantaneous change in input voltage.

5.7.2 Cascoded SenseFET

5.7.2.1 Measurement Analysis and simulation comparison

At every switching boundary, the inductor current reverses. The corresponding change in voltage over the inductor creates a negative voltage at the input of the current sensor (node B in Figure 4.10). This negative voltage drives transistor M_{1B} out of saturation into the triode region and eventually into the cut-off region. The resulting imbalance in currents between the differential pairs distorts the sensor output as shown in Figure 5.7. The sensor only resumes normal operation once the input voltage is high enough for M_{1B} to operate in saturation.

The expected cascode SenseFET gain from simulation is plotted in Figure 4.14, repeated in Figure 5.10.

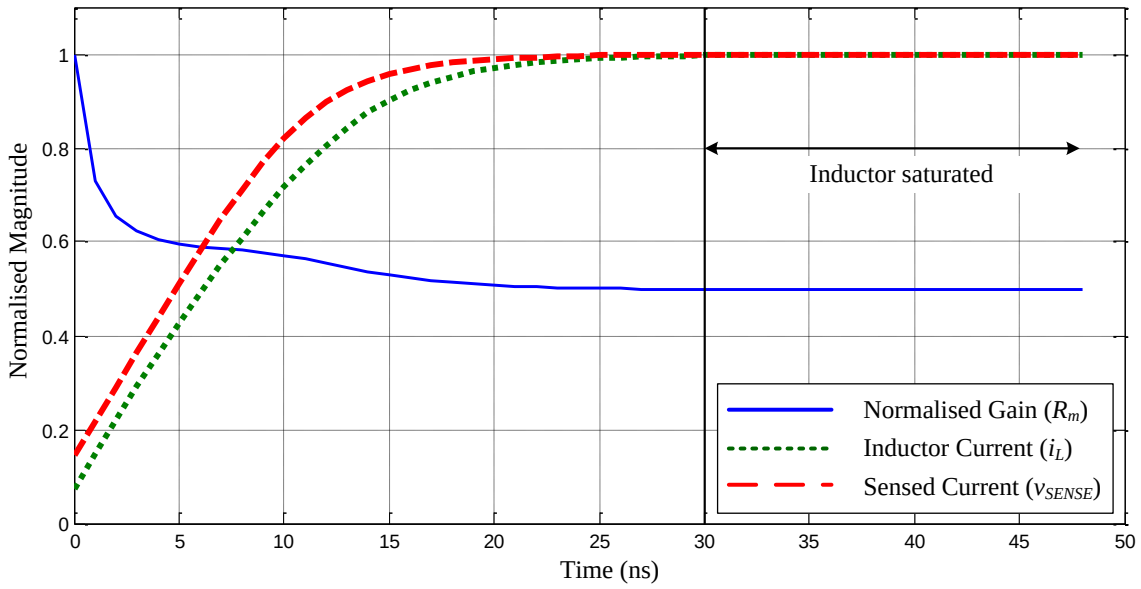

Figure 5.10. Transresistance gain (R_m), normalised inductor current, and sensed current of the cascoded SenseFET.

Figure 5.10 is a normalised plot of R_m, v_{SENSE}, and i_L. The plots have been normalised to emphasise the deviation of v_{SENSE} relative to i_L. During the first 4 ns of the cycle, the gain of the cascode SenseFET is highly non-linear. The high non-linearity is partially attributable to a discontinuity in the data at 0 ns. At 0 ns, the SenseFET output, v_{SENSE}, is non-zero. i_L at 0 ns is close to 0 mA. As i_L increases though the cycle, the normalised gain rapidly approaches 0.5. After 5 ns in the cycle, R_m varies by less than 10 % from its nominal value.

The cascoded SenseFET has two gain profiles. The gain profile during inductor discharge phase has less variation over the cycle than the gain profile during the inductor charging phase. The gain profile of the discharge phase is plotted in Figure 5.11.

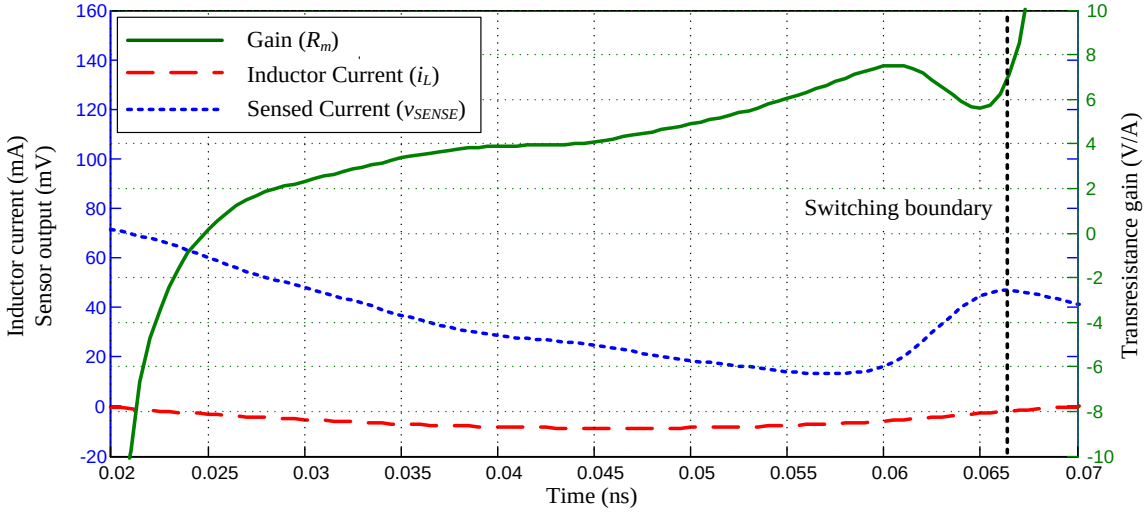

Figure 5.11. Cascoded SenseFET gain (R_m) during inductor discharge.

Figure 5.11 is a close-up plot of the cascoded SenseFET gain profile during the inductor discharge into the test circuit's RC load. From 0.03 µs to 0.055 µs the gain of the SenseFET is 4 V/A ± 2 V/A.

The gain profile of the discharge phase is plotted in Figure 5.12.

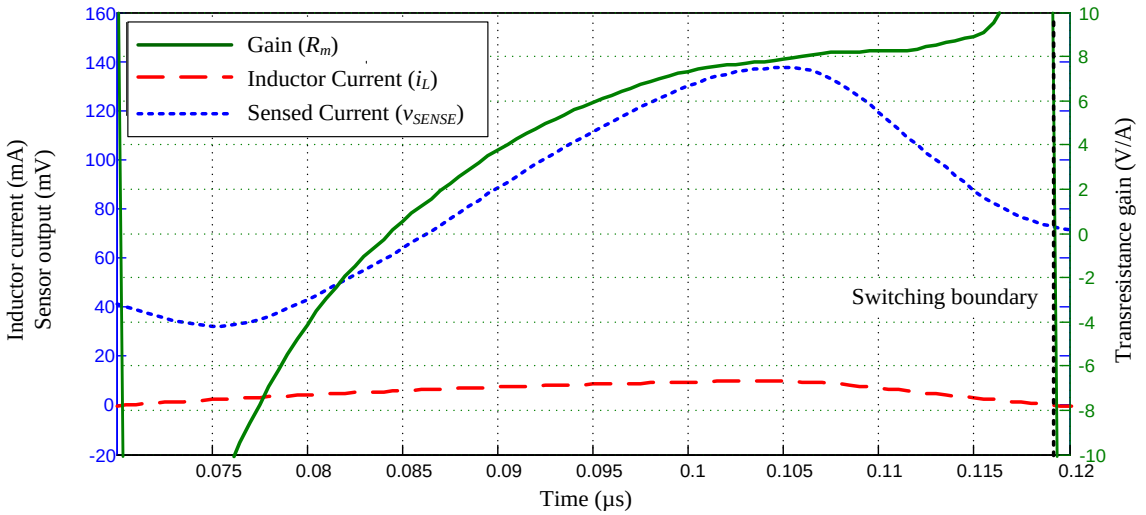

Figure 5.12. Cascoded SenseFET gain (R_m) during inductor charge.

Figure 5.12 presents a close-up plot of the cascoded SenseFET gain profile during the inductor charge phase. From 0.075 µs to 0.095 µs the gain of the SenseFET has a significant

non-linear characteristic. From 0.095 µs to 0.115 µs the gain profile stabilises to 7 V/A ± 1 V/A.

The prototype cascoded SenseFET exhibited low variance in its gain in two regions. In the discharge phase of the conversion, the gain was 4 V/A ± 2 V/A over a portion of the cycle. In the charging phase of the conversion the gain was 7 V/A ± 1 V/A. Although a linear gain characteristic was partially achieved, circuit behaviour at the switch boundaries strongly influences the overall gain profile of the SenseFET.

The prototype delivered a gain of approximately 4 V/A and 7 V/A in the discharge and charge phases respectively. The designed gain is 2 V/A. Increased gain is attributable to two circuit elements, the aspect ratio of M_S, and the interaction of M_6 and R_{SENSE}. If M_6 in Figure 4.10 develops a larger i_{DS} than designed for, the current to voltage conversion through R_{SENSE} would be larger than expected. Similarly, if the resistance of R_{SENSE} is practically larger than the simulated value, the gain would also increase.

A less likely candidate for increased gain is if M_S is smaller than designed for through process variation. A variation in the aspect ratio of M_S would result in a variation in K. M_S and M_{P1} to M_{P4} make use of fingered gates to geometrically distribute the device structure over a rectangular area to reduce the effect of process variation gradients. This technique becomes more effective at large aspect ratios, effectively reducing variations through averaging over the macro-scale of the device structure. M_S would need to be 50 % smaller to increase the gain by a factor of two. Such a large variation from repeated deviations over multiple chips is unlikely.

The expected gain linearity of the sensor over a limited range of current inputs during the switching cycle is comparative to that predicted by simulation. Comparisons can be drawn between the extent of gain deviation and the period of linearity over a switching cycle. The variation in the gain in the simulation is approximately 10 % from 5 ns to 45 ns of the 50 ns cycle, or 80 % of the total switching cycle. In the more linear region of the charging phase (0.095 µs to 0.115 µs) the gain variation is approximately 14 %. In the discharging phase, the gain varies by up to 50 %.

The gain of the sensor during the charging phase of the switching cycle does not suffer as severely as it does during the discharging cycle. The negative voltage at the sensor input is

absent, resulting in a greater range of operation when the current direction is reversed. In both instances, the gain linearity suffers as M_{1B} is driven out of saturation. Once M_{1B} is driven out of saturation and into cut-off, branch B of the SenseFET is no longer active, causing the voltage at node A to no longer able to track node B.

Both measurement phases suffer from gain deterioration, due to a lack of immunity to severe changes in voltage at the sensor input. The peak-to-peak voltage over the inductor also approached the oxide breakdown voltage of the process, which, in turn further reduced linearity of the sensor and test circuit after extended running times.

The variation of gain by 10 % over approximately 50 % of a charge or discharge cycle indicates that provided all devices in the improved SenseFET remain in the active region, an improvement in linearity is possible in comparison to the simplified design. The susceptibility of the transistors to be driven out of saturation by a significant increase in inductor voltage is a design problem which needs to be considered for future improvements.

5.7.2.2 Possible failure modes

Despite the cascoded SenseFET prototype having a measurable and meaningful output, these prototypes eventually degraded and failed over time. This time to failure was typically after several hours of continuous operation. Prototype failure was characterised by approximately five hours of operation before output degradation was noticeable. During the degradation period the v_{SENSE} output of the SenseFET would decrease in magnitude, distort, and eventually reduce to 0 V_{DC}.

The total area of the cascoded SenseFET is 218 μm^2, with minimum length features having at least one dimension of 120 nm. This feature scale combined with limited access to both optical and election-scanning microscope equipment has prevented inspection of the physical device at a useful resolution and fidelity. The potential failure modes are inferred from design files, observations of the prototype behaviour, and the IBM 8HP BiCMOS process documentation.

The cascode SenseFET layout show in Figure 4.12 makes use of significantly wider tracks in the SenseFET branches as well as a reduced biasing current in comparison to the reference design. These factors reduce the probability that these tracks would be a point of failure in the design.

As with the reference SenseFET, a possible failure mode is voltages in the circuit exceeding the gate oxide breakdown voltage at the switching boundaries. In the case of the cascoded SenseFET, this failure was more gradual, with the circuit operating normally for several hours before the output of the SenseFET started to degrade and finally failing completely.

5.8 CONCLUSION

This Chapter presents captured and measurement data of the reference and cascode SenseFETs and the analysis of this data. The measurement process was initiated through the capture of prototype data using measurement and capture equipment. The captured data was processed in MATLAB to generate plots which could be used to evaluate and measure the prototype SenseFET performance.

This presented data is considered in three stages. Truncated data with minimal processing sets are presented first. The following stage presents data which has been processed to facilitate measurement and evaluation of the SenseFET performance. In this stage observations are made and circuit behaviour is described. The final stage is an interpretation of the data. Comparison of the measured results against expectations from simulation are also made.

The cascoded SenseFET prototype showed promising results but not without ensuing difficulties. The SenseFET circuit measures the current during both the charging and discharging phases of the inductor in the buck-boost test circuit. During each phase the SenseFET output behaviour was characterised by a gain profile which was negatively affected by the switching boundaries. Once the SenseFET circuit had stabilised, it operated as predicted by simulation. The SenseFET developed a transresistance gain of 7 V/A ± 1 V/A during the inductor charging phase. During the discharging phase the SenseFET developed a gain of 4 V/A ± 2 V/A. The performance during the charging phase is significantly better than performance during the discharging phase, with only a 14 % variation in the gain, compared to 50 % during the charging phase.

Failure modes are also discussed in this Chapter. The scale of the monolithic circuits and limited access to diagnostic equipment limits failure analysis to re-analysis of the designs used and observations of prototype behaviour.
The reference SenseFET presented no variable output with only 0 V_{DC} present at the output. This behaviour is indicative of a failure, but the lack of any variance in the output makes

diagnosis of the failure type difficult. This Chapter presents several probable failure modes based on a re-interpretation of the original design. These failure modes include insufficient track width in the reference SenseFET, leading to either internal biasing driving devices into the wrong operating region or physical failure of the tracks. Voltages exceeding the gate oxide breakdown voltage of the process are also possibly responsible for failures in the reference SenseFET. These higher than expected voltages would occur at the switching boundaries, where the clock and inductor voltages rapidly change.

CHAPTER 6 CONCLUSION

6.1 CHAPTER OVERVIEW

This Chapter is the concluding chapter of this dissertation and consolidates the work presented in previous Chapters. An overview of each chapter is provided. With the exception of the introductory chapter, a reflection of each chapter is also presented with reference to the findings of the study.

6.2 OVERVIEW OF THE STUDY

6.2.1 Contextualisation

Practical distributed autonomous wireless sensor networks (WSN) are sensor networks which make use of inexpensive monolithic sensor nodes to characterise the environment in which the network is deployed. The affordability of producing the sensor nodes in the network is a determining factor for the viability of the WSN. This study examined the topology of a generalised monolithic sensor node to identify design avenues which could improve affordability [1], [2].

An effective approach to affordability is to implement sensor nodes in an established, inexpensive CMOS technology [3]. This study identified the internal current sensing circuit of the sensor node PSU as an element which could be improved for the chosen CMOS process. By improving the current sensing circuit linearity, the efficiency of the PSU could be improved, thus improving the viability of a monolithic sensor node solution for the chosen CMOS technology.

6.2.2 Hypothesis and research problems

The hypothesis for this dissertation was:

> *If integrated circuit topologies for measuring current using CMOS devices were improved to be resilient to second order effects and low voltage operation, the linearity of the measurement would improve.*

This study sought to test topological changes to a commonly used current sensing technique to improve the performance of the technique. A commonly used sensing circuit, often

referred to as a SenseFET, was used as a reference in a chosen CMOS process. This reference circuit was analysed to determine the extent to which second order process effects would degrade circuit linearity. It was found that the process characteristics of the IBM 8HP BiCMOS 130 nm process does indeed negatively affect the reference circuit. This analysis was used to develop topological changes to the SenseFET circuit which would diminish the degradation of sensor linearity.

The hypothesis was tested using both practical testing of prototypes and with detailed simulation models. In simulated testing, it was found that topological changes designed to isolate the SenseFET from second order process characteristics does improve the linearity of the measurement when compared to a standard or reference design commonly found in the literature.

Practical testing of prototypes yielded mixed results. The improved cascoded SenseFET design performed as expected over a limited range of conditions, with notable issues at the switching boundaries of the buck-boost test circuit. The reference design implementation did not produce a measurable output. The lack of a reference output resulted in no direct comparison being possible between the reference and cascoded SenseFET prototypes. The promising results from simulation suggests that the practical result is not in conflict with the hypothesis, but stems from a practical design error in the reference SenseFET layout.

The research problems based on the hypothesis were:

1. Determine the extent of the effect of second order effects on the linearity of integrated current sensing circuits.
2. How will the non-linearity be modelled using traditional analytical models? How could such models be used to gain additional insight into circuit operation and be used to derive solutions that address non-linearity? How well do these models agree with gate level simulation?
3. How robust are the solutions to process, temperature, and voltage (PVT) variations?
4. Determine if it possible to significantly improve linearity in comparison to other designs.

Problem one stemmed from the requirement to first determine the extent to which a reference current sensing circuit was affected by second order process characteristics. Problem two focussed on incorporating analytical models of second order effects into the SenseFET design equations. The extent to which these effects would influence the circuit operation was then examined. By using updated design equations in combination with empirical models and simulation, the accuracy of the updated design equation could be tested. Problem three examined how robust the designs were to process and operational variation. Finally, problem four is closely related to the hypothesis, asking if improved linearity was possible despite process characteristics.

Problem one was addressed by designing a reference SenseFET using idealised design equations and analysing simulation results. The transistors used in the design were also characterised at the operating point of interest. This characterisation showed that the classic FET i_{DS} - v_{DS} relationship was strongly influenced by second order effects. It was found that the reference SenseFET bias currents were strongly influenced by external and second order characteristics.

Problem two was addressed through the inclusion of the two dominant second order effects into the SenseFET design equations. It was found that both channel velocity saturation and channel length modulation have a distinct and marked effect on the operation and linearity of the reference SenseFET circuit. It was determined that through these mechanisms, the dynamic response of the current being measured and the inductor voltage would directly influence the circuit biasing. The compromised biasing caused the linearity of the reference SenseFET to deteriorate.

Problem three was approached by using design and layout techniques which promoted resilience towards PVT effects. Process variations were compensated for by using device geometry which promoted equalisation of process variation gradients. Circuit biasing was driven by current symmetry and not input voltage, reducing the effect of input voltage on circuit performance. Temperature compensation required the design of a robust current source for biasing. Designing such a source was beyond the scope of the hypothesis.

Through simulation of detailed empirical models and practical measurement, problem four was sufficiently addressed in a simulation environment with support from measurement. It was possible to improve the linearity of a current sensing circuit through topological changes

in the circuit. This was demonstrated clearly through simulation and to a limited extent through measurement. Measurement was hampered by design flaws which prevented comprehensive measurements of the reference SenseFET circuit.

6.2.3 Overview of relevant literature

The literature study of this dissertation considered several approaches to measuring current in the context of a DC-DC converter with an inductive element. Many of these techniques rely on measuring a characteristic of an element in series with the inductive element of the DC-DC converter. In general, the characteristic of interest is the voltage over the element as current is conducted. This voltage is measured and characterised to determine the current. These techniques were not suitable for the integrated approach in the chosen process for several reasons. These reasons include excessive chip real estate, poor scalability to low-voltage CMOS, complex active inductor characterisation, and of importance to this dissertation, susceptibility to second order process characteristics.

Techniques which made use of a resistive element were not suitable because an integrated resistor with a low enough resistance, to not dissipate excessive heat, requires a significant amount of chip real estate. An alternative technique which uses the on resistance of the DC-DC converter switches is prone to PVT variations [30]. Techniques such as those proposed by [31], [9], and [32] rely on characterisation of the inductive element. The characterisation is used to design networks which determine the current from the differential voltage over the inductor. This technique was rejected in favour of an approach which does not rely on pre-knowledge of the inductive element.

Integrated current sensing using the SenseFET [29] concept (see Figure 2.9) offered a solution which was compact, could be designed to be resilient to PVT effects, and did not require characterisation of the inductive element. The SenseFET circuit consists of two branches. The primary design challenge is to ensure that the SenseFET output branch tracks the input branch. A commonly used SenseFET configuration for achieving this is shown in [28], where an OPAMP is used to stabilise the voltages between the branches.

A disadvantage of the solutions such as that in [28] is that they require a reasonably large amount of voltage headroom to practically implement the required OPAMPs. The IBM 8HP 130 nm BiCMOS process used in this dissertation does not allow for supply voltages in the

3.3 V range. Additionally, other implementations are application specific. The literature does not yet report SenseFET circuits for low voltage, deep sub-micron process nodes.

CMOS process nodes with geometry in the deep sub-micron range are more susceptible to second order process characteristics [30], [35], and [36]. In this study, the most prevalent characteristics under consideration are described in [30]. The characteristics which were most applicable in this study were velocity saturation, channel length modulation, and low voltage operation. Velocity saturation and channel length modulation were of importance because of the significant effect these have on the transistor $i_{DS} - v_{DS}$ relationship. Velocity saturation limits i_{DS} despite increased v_{GS}. Channel length modulation provides a mechanism for the external inductor voltage to influence the biasing of the SenseFET circuit. Both channel length modulation and velocity saturation strongly affect single and differential transistor configurations in the SenseFET topology. More complex interactions such as thin gate-oxide and other field effects were taken note of but relegated to the simulation tools for analysis.

Low-voltage techniques described in [30] and [34] were used as the basis for approaching a SenseFET design in a low-voltage CMOS process. The technique that was focussed on was the use of folded cascodes, often used in low-voltage differential amplifiers, to augment the SenseFET circuit maintain branch voltage equalisation. This equalisation contributed to the linear operation of the improved SenseFET.

6.3 METHODOLOGICAL REFLECTION

6.3.1 Contextualisation

The methodology chosen for this dissertation had three distinct phases, with each phase comprised of iterative processes. The iteration in each phase was designed to realise the goals of the phase. This approach was advantageous because it emphasised design space exploration prior to focusing on hardware development.

The first phase of the methodology was designed to focus on the problem definition and literature study. This phase started with an examination of DC-DC converters in the context of WSNs. As the body of relevant literature grew, an iterative literature review was used to identify where research value was and to develop the hypothesis.

Phases two and three were similar in structure. Phase two was where design experimentation and development took place. In this phase, the goal was to use analysis and simulation to develop and test ideas. By focusing on development in a simulation environment and making use of detailed empirical models of the 8HP process, it was possible to create both a reference and improved SenseFET design before the time-consuming task of layout and preparation for manufacture. Phase two was also used to determine the requirements of the measurement setup and test parameters.

The third and final phase used processes which were complementary to that of phase two, but with an emphasis on iteration to create viable layouts and design files for the SenseFET prototypes. The simulated and software tested designs from phase two were used to create the layout geometry of the schematic designs. The created layouts were tested and verified using the process rule-sets provided by MOSIS.

6.3.2 Analysis, mathematical modelling, and characterisation

Prior to any design, circuit analysis was used to gain insight into how the reference SenseFET functions. Circuit analysis took place in phase two of methodology. An analysis of an idealised SenseFET circuit formed the basis of what the best possible expected result could be. This idealised analysis was followed by a more detailed analysis which incorporated non-ideal process effects. A comparison of the idealised and detailed analysis was used to identify and formalise which factors caused a deviation from ideal SenseFET operation. These identified factors were used to design an improved SenseFET. Analysis was used in conjunction with numerical modelling and characterisation to design the SenseFET prototypes.

Circuit analysis was limited to include the dominant contributions of velocity saturation and channel length modulation. These aspects could be clearly integrated into the classical transistor long-channel model and yielded useful mathematical results. When combined with the device characterisation, channel length modulation was identified as a key contributing factor to deviation in branch bias currents in the SenseFET. A similar approach to incorporate velocity saturation revealed that topological changes were required to linearise the reference SenseFET design. The complex process interactions were delegated to the simulation tool, with device characterisation used to incorporate these effects into the analytical model. This approach to analysis resulted in design equations which were used to design prototypes.

To use the circuit analysis results for design, device and process parameters were required. MOSIS provides 8HP process information at certain operating points which were not applicable to the design space being used. Characterisation of the empirical device models, provided by MOSIS, at the operating point of interest was successfully used to derive process parameters. These parameters were combined with circuit analysis results to facilitate SenseFET design.

The analytical equations as well as characterisation data were numerically realised in MATLAB. This modelling was done to generate a graphical representation of data and device behaviour. This approach was also used to generate useful representations of the transresistance gain profiles of the SenseFETs. The gain profiles were used to gauge the success of design choices.

6.3.3 Methodological limitations

Design constraints stemmed either from 8HP process constraints or from constraints imparted by design to limit the scope of the design space. The design space was limited to maintain focus on the hypothesis. These limitations were contributing factors in determining the methodology of this study.

Access to only the IBM 8HP 130 nm BiCMOS process limited comparative analysis with another integrated process. The limitation prevented the inclusion of comparison with an alternative process in the methodology. Additionally, the physical limitations of the process, such as the gate-oxide breakdown voltage, constrained design and testing to within the capabilities of the 8HP process.

The prototype was manufactured through the MEP[10], this program follows a strict submission and approval schedule. The scheduling of the program limited the number of prototype iterations to a single prototype over the course of this dissertation. To accommodate this the methodology emphasised thorough design in CAD, with simulation and other verification tools being used to test and verify designs. This offered flexibility in testing design ideas and iterating designs before committing to device layout

[10] The MOSIS educational program (MEP) offers students at academic institutions an avenue to prototype monolithic devices at no cost to the student.

The heavy emphasis on testing through simulation yielded functioning designs in simulation. The prototype circuits did deliver meaningful results but not without deviation from the expected results. The methodological approach used did not place enough emphasis on characterising the testing environment and layout limitations. This combined with only a single prototype, allowed for preventable failure modes to be incorporated into the reference design of the SenseFET.

The methodology focused on serial iterative approach with a reliance on simulation accuracy. Despite only a single prototyping run being possible, the simulated outcomes suggested that the prototype would function as expected. In retrospect, some uncertainty could have been reduced by layout and prototyping of design variants ("design for testability") developed throughout the design process. While this would be the approach in industry, the MPW approach is limited by the number of pads.

6.3.4 Design and prototyping

Following analysis of the basic SenseFET circuit, an iterative design process was followed. A reference SenseFET circuit was designed as well as an improved SenseFET. Comparison of the performance of the two SenseFETs was used to test the hypothesis. The design methodology included the characterisation of the 8HP process at the operating point of interest. Characterisation and design both used the AMS SPICE simulation tool in the Cadence Virtuoso software package.

Once design simulation was completed, the schematic designs were translated into a geometric device layout. The layouts were verified against the design schematics using the Assura and L-Edit tools within the Cadence package. The LVS tool in L-Edit was only used to perform a netlist comparison of the layout. Assura was used to verify that the process design rules were not violated. These checks did not provide information of the suitability of the layout choices.

The completed layouts were incorporated into the layout of a 2.5 mm × 2.5 mm die which included research projects of other students in the research group. The final layout information and packaging information was provided to MOSIS. Once MOSIS had completed manufacturing, the prototype dies were distributed to students for testing and measurement.

The methodology required that test circuits be design and implemented. The test circuits were implemented as a combination of internal test circuitry and external discrete circuits. The power transistor switching circuitry of the DC-DC converter test circuit were implemented on the die. The external reactive components which were used could not be implemented on the die, formed part of the discrete test circuit on a test PCB. The test PCB also provided power, measurement points, clock signals, and biasing.

6.3.5 Technical software

Two software packages were used throughout the study. MATLAB is a technical computational package which was used to numerically evaluate analytical work and process captured data. MATLAB scripts processed the captured data to generate graphical representations which could be used for prototype measurement and evaluation.

The Cadence Virtuoso software package is a collection tools for the design and analysis of integrated circuits. The S-Edit tool was used for schematic capture and to define simulation tests. The AMS tool was used to generate SPICE netlists from S-Edit schematics. AMS also allowed the captured schematics to be simulated using SPICE. L-Edit was used to capture and generate layouts of the SenseFET designs and internal test circuits. Finally, the Assura tool was used to verify that layouts did not violate the process design rules.

6.3.6 Measurement

Measurement and testing was performed both in simulation and in practice. SPICE simulation was used extensively during the design phase. Simulation was used to characterise the 8HP process empirical models. SPICE simulation was used to evaluate the reference and cascoded SenseFET designs.

Two sets of tests are defined in the methodology. Test 1 required the determination of the reference and cascoded SenseFET transresistance gain profiles. This test was performed in both a simulation environment and from data captured from the prototypes. This test was the primary test for generating data which could be used to test the hypothesis. Test 2 was a secondary test designed to evaluate the performance of the reference SenseFET in an integrated buck-boost converter with current-mode control.

Prototype data was captured using a multi-domain oscilloscope. This instrument was used to digitally sample and store the output of the SenseFETs as well as other circuit

characteristics. The captured data was transferred to a computing environment and processed in MATLAB.

6.4 RESULTS

6.4.1 Data interpretation and data analysis

Data captured from simulation and from measurement was used to evaluate the reference and cascoded SenseFETs.

Simulation results are presented in Chapter 4. The approach for the simulated analysis was the same for the both the reference and cascoded SenseFETs. Both SenseFETs were evaluated in terms of the branch currents and transresistance gain. Branch current symmetry was used as an indication of how well the two branches of the SenseFET track each other. A large variation in branch currents contributes to non-linearity in the gain profile of the SenseFET. The transresistance gain was evaluated to determine linearity of the SenseFET implementation. Large deviations in the transresistance gain profile of the SenseFET are associated with non-linearity. The transresistance gain directly relates the output voltage to the sampled current.

The simulated branch currents were presented in Figure 4.8 for the reference SenseFET and in Figure 4.13 for the cascoded SenseFET. The reference SenseFET branch currents varied between 0 µA and 23 µA for the first 15 ns of the switching cycle before stabilising. The cascoded SenseFET branch currents varied between 0 µA and 6 µA for the first 15 ns of the switching cycle.

The simulated normalised transresistance gain of the reference SenseFET was presented in Figure 4.9. The gain increased rapidly in the first 2 ns. Between 2 ns and 15 ns the gain overshoots the stabilised value by 20 %. After 15 ns the gain variation decreased rapidly and stabilised. The transresistance gain of the cascoded SenseFET was shown in Figure 4.14. The cascoded SenseFET gain also showed a large deviation in the first 2 ns of the cycle. For the remainder of the cycle, the cascoded SenseFET gain had a variation of only 10 % from 5 ns onwards. In both cases the distinct discrepancy in gain in the first 2 ns was caused by the switching transient in the test circuit as the DC-DC converter test circuit switched states from charge to discharge. In simulation, the cascoded SenseFET showed a distinct improvement in transresistance gain variation over the reference SenseFET circuit.

The prototype measurements focused on evaluating the transresistance gain of the reference and cascoded SenseFET circuits.

The reference SenseFET circuit did not produce any meaningful output. The lack of output was attributed to several possible factors. Insufficient track width in the layout of the reference SenseFET was isolated as the likely cause of failure in the prototype. This behaviour was noted in Test 1 and in Test 2.

The transresistance gain of the cascoded SenseFET was presented in Figure 5.7. The cascoded SenseFET had two distinct profiles for the charge and discharge phases of the power conversion cycle. These profiles were detailed in Figure 5.11 and Figure 5.12. The measured gain profiles deviated from the expected gain profile in Figure 4.14. The cascoded SenseFET gain during the converter charge phase stabilised to 7 VA ± 1 VA. The gain during the converter discharge phase stabilised to 4 V/A ± 2 V/A. In both phases the achieved gain was not achieved over the entire cycle. At the switching boundaries between each cycle, the transient response of the cascoded SenseFET and test circuit combination drove the transistors on the input branch of the SenseFET out of saturation. When the transistors in the input branch were driven out of saturation, the two branches of the SenseFET could no longer track and introduced severe non-linear behaviour into the SenseFET.

6.4.2 Discussion

The simulation results were found to strongly support the hypothesis. The two most notable observations from the cascoded SenseFET simulated result is the speed at which the transresistance gain stabilises after the switching transient and the improved gain linearity. These simulation results using device level simulation strongly motivated that the design was ready to proceed to the layout stage.

The prototype measurement data indicated that the effect of the switching transient was more prolific than that predicted by simulation. This was attributed to the simulation test bench SPICE model. The test bench SPICE model was not detailed enough when modelling the interaction of the external discrete test circuit. This resulted in optimistic simulation results when compared to the prototype measurement results.

The failure of the reference SenseFET in both the targeted transresistance gain test (Test 1) and the implementation test (Test 2) was attributed to a layout error. Despite the layout

design passing LVS, the LVS netlist comparison was not setup to consider track width and current density capacity. In an attempt to create a compact layout, minimum track widths were used in the branches of the reference SenseFET. An iteration of this design would use the layout strategy that was employed in the cascoded SenseFET. In the cascoded SenseFET, the branch tracks of the SenseFET were significantly wider, matching the width of the transistors used.

The cascoded SenseFET prototype behaved as suggested by simulation once the SenseFET had stabilised after the switching transients. The achieved transresistance gain of 4 V/A ± 2 V/A and 7 V/A ± 1 V/A, for inductor discharge and charge, was on the same order of magnitude as the designed gain of 2 VA. The deviation between the achieved and designed gain was attributed to several possible factors. These factors included the analytical model requiring refinement, particularly in determining the i_{DS} developed by M_S and M_6 in Figure 4.10. The drain-source current developed by M_S and M_6 directly influenced the transresistance gain through the current to voltage conversion through R_{SENSE}.

The partial result from measurement supports the simulation results in testing that the hypothesis is true. Simulation found that improving the resilience of the SenseFET circuit to second order process characteristics would improve the linearity of the SenseFET circuit. The prototype measurements could not directly show this in the absence of a reference measurement. The prototype measurements of the cascoded SenseFET does support that the design approached used in the development of the cascoded SenseFET would lead to a SenseFET with improved linearity.

6.5 LIMITATIONS OF THE STUDY

The lack of a full set of measurement data limits confidence in the measurement results. This was partially mitigated by evaluation of the simulation results supported by measurement results. It was found that device level simulation, using device models based on empirical data, was able to show that the cascoded SenseFET had improved linearity over the reference design from the literature. The measurement data supported the simulation data for the cascoded SenseFET, but a lack of a measurement data for the reference design limited confidence in the measured results.

The measurement data revealed that the transient response of the SenseFET and test circuit combination was more prevalent than predicted by the simulation model. The large transient

response reduced the effective input range of the SenseFET. A more detailed SPICE model of the test circuit interaction would have allowed for design changes to mitigate the transient response. Specifically, more accurate models of the external reactive components could have led to design changes to either the SenseFET or test circuits to mitigate the observed transient behaviour.

The measurement data was used to support the simulation results by isolating the different regions of operation despite the prevalent transient effects. By observing transresistance gain of the cascoded SenseFET in regions of stability, it was shown that the achieved gain is similar to that predicted by design and simulation. The observed gain was higher than designed for by a factor of 2 to 3. The increased gain was attributed to the design equations underestimating the drain-source currents driving the current to voltage conversion circuit in the SenseFET.

The study results would have benefitted from a comparative analysis of a SenseFET solution implemented in another CMOS process. This was mitigated by identifying architectural disadvantages of the reference design already presented in the literature. It was shown that the base SenseFET design was susceptible to influence from non-ideal process characteristics. The improved design approached this from a topological perspective, aiming to produce a design which mitigated the influence of these process characteristics. By generalising the solution to resolve design challenges common to this technology node, insight can be gain on how to manage SenseFET design in similar low voltage processes.

6.6 OPPORTUNITIES FOR FUTURE RESEARCH

Future iterations of this work would need to first focus on resolving the implementation problems that arose during this study. The layout of the reference SenseFET would need to be corrected for meaningful comparative analysis. The short-term failure of the test circuits would also need to be remedied. The recommendation would be for overvoltage diode protection at the input of the SenseFET circuits.

Future work would need to make use of a revised methodology, where several design variants are developed in parallel. The advantage a methodology which makes provision for parallel development branches is a reduction in turn-around time per prototype. An updated testing framework designed to allow multiple design variants to be tested simultaneously on

a single test bench would benefit a development process where only a single fabrication run is possible.

Additional improvements would be to adapt the SenseFET input to be more resilient to the transients present at the switching boundaries. By improving the transient response, the SenseFET would be able to provide useful measurement data over a longer period within the switching cycle. Ideally, an improved design would be immune to transients and provide linear gain over the entire switching cycle.

The design and simulation phase of this work made extensive use of SPICE models and simulation. Device level simulation was made possible by SPICE models based on empirical data from the 8HP process. The SPICE model of the simulation test circuit was not comprehensive enough to fully predict the behaviour experienced by the prototype SenseFETs at the switching boundaries. Future work would need to expand the scope of the simulation SPICE model to include more detailed models of external devices. A detailed, software based, WSN node model, able to generate detailed SPICE test scenarios for integration into device level hardware design, would assist in future work. The approach would make it possible to generate reliable test scenarios for future WSN node development, ultimately reducing the design iterations required

A SenseFET design which is able to mitigate the design problems discussed in this study would be suitable for integration into a compact PSU for a WSN sensor node. This would assist in research on WSN node design in low cost CMOS.

6.7 CONTRIBUTION TO THE BODY OF KNOWLEDGE

This study showed that it is possible, through topological circuit changes, to improve the linearity of a commonly used current sensing circuit. In addition to improving the linearity, it was shown this improvement could be implemented in a low-cost CMOS process. The proposed cascoded SenseFET offers improved linearity of the current reference design while remaining feasible for implementation in low-voltage CMOS. This contrasts with other solutions from the literature tabulated in Table 2.2. The implementation increases the knowledge base required to implement a complete WSN sensor node in low-cost CMOS.

Additionally, this study introduced an alternative application of folded cascodes. The common approach to branch voltage tracking in current sensing circuits was through the application of operational amplifiers or rudimentary current mirrors. As shown in this study, a rudimentary reference SenseFET design is susceptible to process characteristics in low-voltage CMOS. OPAMP implementations in low-voltage CMOS requires the design of multistage differential amplifiers, introducing unnecessary complexity. By applying the folded cascode topology to the fundamental SenseFET circuit, low-voltage process characteristics were mitigated with a compact, topologically simple solution.

This study offered a formalised approach to the engineering hardware design cycle. This approach is not unique, but allowed for a structured design methodology without limiting opportunity to test new ideas. This formalised approach is considered a strength of this study.

Finally, this study resulted in a peer-reviewed publication in Microelectronics International[11] [11]. The paper, accepted for publication in August 2016, is:

> N. Naudé and S. Sinha, "Linearized differential current sensor in low-voltage CMOS," accepted for publication to *Microelectronics International* (Emerald), Aug. 2016. (Expected publication in 2017).

[11] Microelectronics International is published quarterly by Emerald Group Publishing. The journal is peer-reviewed and listed by Thomson Reuters Web of Knowledge (formerly ISI). The journal is accessible at http://www.emeraldinsight.com/journal/mi.

REFERENCES

[1] J. Yick, B. Mukherjee and D. Ghosal, "Wireless sensor networks survey," *Computer Networks,* vol. 52, pp. 2292-2330, 2008.

[2] G. Anastasi, M. Conti, M. D. Francesco and A. Passarella, "Energy conservation in wireless sensor networks: A survey," *Ad Hoc Networks,* vol. 7, no. 3, pp. 537-568, 2009.

[3] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar and K. Bernstein, "Scaling, power, and the future of CMOS," in *IEDM,* Washington, DC, 2005.

[4] B. Sahu and G. A. Rincón-Mora, "A Low Voltage, Dynamic, Noninverting, Synchronous Buck-Boost Converter for Portable Applications," *IEEE Transactions on Power Electronics,* vol. 19, no. 2, pp. 443-452, 2004.

[5] R. Redl and N. O. Sokal, "Near-Optimum Dynamic Regulation of DC-DC Converters Using Feed-Forward of Output Current and Input Voltage with Current-Mode Control," *IEEE Transactions on Power Electronics,* vol. PE-1, no. 3, pp. 181-191, 1986.

[6] V. M. R. Bernal, S. Celma, N. Medrano and B. Calvo, "An Ultralow-Power Low-Voltage Class-AB Fully Differential OpAmp for Long-Life Autonomous Portable Equipment," *IEEE Transactions on Circuits and Systems II: Express Briefs* , vol. 59, no. 10, pp. 643-647, 2012.

[7] M. Du and H. Lee, "An Integrated Speed- and Accuracy-Enchanced CMOS Current Sensor with Dynamically Biased Shunt Feedback for Current-Mode Buck Regulators," *IEEE Transactions on Circuits and Systems - I: Regular Papers,* vol. 57, no. 10, pp. 2804-2814, 2010.

[8] C. Y. Leung, P. K. T. Mok, K. N. Leung and M. Chan, "An Integrated CMOS Current-Sensing Circuit for Low-Voltage Current-Mode Buck Regulator," *IEEE Transactions on Circuits and Systems - II: Express Briefs,* vol. 52, no. 7, pp. 394-397, 2005.

[9] H. P. Forghani-zadeh and G. A. Rincón-Mora, "An Accurate, Continuous, and Lossless Self-Learning CMOS Current-Sensing Scheme for Inductor-Based DC-DC Converters," *IEEE Transactions on Solid State Circuits,* vol. 42, no. 3, pp. 665-678, 2007.

[10] Y. Rao, W.-L. Deng and J.-K. Huang, "High-Accuracy Current Sensing Circuit with Current Compensation Technique for Buck–Boost Converter," *International Journal of Electronics*, vol. 102, no. 3, pp. 476-489, 2015.

[11] N. Naudé and S. Sinha, "Linearized differential current sensor in low-voltage CMOS," *Microelectronics International (Emerald),* to be published. (Expected publication in 2017)

[12] T. Torfs, T. Sterken, S. Brebels, J. Santana, R. van den Hoven, V. Spiering, N. Bertsch, D. Trapani and D. Zonta, "Low Power Wireless Sensor Network for Building Monitoring," *IEEE Sensors Journal*, vol. 13, no. 3, pp. 909-914, 2013.

[13] P. D. Mitcheson, E. M. Yeatman, T. C. Green, A. S. Holmes and G. K. Rao, "Energy Harvesting From Human and Machine Motion for Wireless Electronic Devices," *Proceedings of the IEEE*, vol. 96, no. 9, pp. 1457-1486, 2008.

[14] T. Torfs, V. Leonov, C. Van Hoof and B. Gyselinckx , "Body-Heat Powered Autonomous Pulse Oximeter," in *5th IEEE Conference on Sensors*, Daegu, 2006.

[15] R. J. M. Vullers, R. van Schaijk, I. Doms, C. Van Hoof and R. Mertens, "Micropower Energy Harvesting," *Solid-State Electronics*, vol. 53, pp. 684-693, 2008.

[16] S. P. Beeby, M. J. Tudor and N. M. White, "Energy Harvesting Vibration Sources for Microsystems Applications," *Measurement Science and Technology*, vol. 17, no. 12, pp. 175-195, 2006.

[17] K. B. Lee, "Urine Activated Paper Batteries for Biosystems," *Journal of Micromechanics and Microengineering*, vol. 15, no. 9, pp. 210-214, 2005.

[18] M. Brown, *Practical Switching Power Supply Design*, Elsevier, 2012.

[19] R. Sheenan and A. Hilton, "Understanding and Applying Current-Mode Control Theory," in *Power Electronics Technology Exhibition and Conference (PES07)*, Clearwater, Florida, 2007.

[20] J. H. Park, H. Kim and H. J. Kim, "A Current-Mode Non-Inverting CMOS Buck-Boost DC-DC Converter," in *31st International Telecommunications Energy Conference INTELEC*, Incheon, 2009.

[21] H.-P. Le, C.-S. Chae, K.-C. Lee, S.-W. Wang, G.-H. Cho and G.-H. Cho, "A single-inductor switching DC-DC converter with five outputs and ordered power-distributive control," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2706-2714, 2007.

[22] B. Sahu and G. A. Rincón-Mora, "High Efficiency Linear RF Power Amplifier with a Power-Tracking Dynamically Adpative Buck-Boost Supply," *IEEE Transactions on Microwave Theory and Techniques,* vol. 52, no. 1, pp. 112-120, 2004.

[23] B. Sahu and G. A. Rincón-Mora, "An Accurate, Low Voltage, CMOS Swithing Power Supply with Adaptive On-Time Pulse-Frequency Modulation (PFM) Control," *IEEE Transactions on Circuits and Systems 1: Regular Papers,* vol. 54, no. 2, pp. 312-321, 2007.

[24] Y. K. Ramadass and A. P. Chandrakasan, "Minimum Energy Tracking Loop with Embedded DC-DC Converter Enabling Ultra-Low-Voltage Operation Down to 250 mV in 65 nm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 43, no. 1, pp. 256-265, 2008.

[25] Z. Lukic, N. Rahman and A. Prodic, "Multibit ∑-Δ PWM Digital Controller IC for DC-DC converters Operating at Switching Frequencies Beyond 10 MHz," *IEEE Transactions on Power Electronics,* vol. 22, no. 5, pp. 1693-1707, 2007.

[26] Y. Lee and C. Hsu, "High Accuracy CMOS Current Sensing Curcuit for Current Mode Control Buck Converter," in *7th International Conference on Power Electronics and Drive Systems,* Bangkok, 2007.

[27] X. Tao and J. Xu, "Integrated CMOS Current-Sensing Circuit for Current-Mode Boost Converters," in *IEEE International Conferance on Industrial Technology,* Chengdu, 2008.

[28] C. F. Lee and P. K. T. Mok, "A Monolithic Current-Mode CMOS DC-DC Converter With On-Chip Current-Sensing Technique," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 1, pp. 3-14, 2004.

[29] H. Forghani-zadeh and G. A. Rincón-Mora, "Current-Sensing Techniques for DC-DC Converters," in *The 2002 45th Midwest Symposium on Circuits and Systems, MWSCAS-2002.* , Oklahoma city, 2002.

[30] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits,* 4th ed. New York: John Wiley & Sons, Inc., 2001.

[31] E. Dallago, M. Passoni and G. Sassone, "Lossless Current Sensing in Low-Voltage High-Current DC/DC Modular Supplies," *IEEE Transactions on Industrial Electronics,* vol. 47, no. 6, pp. 1249-1252, 2000.

[32] P. Midya, M. Greuel and P. Krein, "Sensorless Current Mode Control - An Observer Technique for DC-DC Converters," *IEEE Transactions on Power Electronics,* vol. 16, pp. 522-526, 2001.

[33] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*,4th ed. New York: Oxford University Press, 1998.

[34] S. S. Rajput and S. S. Jamuar, "Low Voltage Analog Circuit Design Techniques," *IEEE Circuits and Systems Magazine,* vol. 2, no. 1, pp. 24-42, 07 August 2002.

[35] M. Alioto, "Understanding DC Behavior of Subthreshold CMOS Logic Through Closed-Form Analysis," *IEEE Transactions on Circuits and Systems - I: Regular Papers,* vol. 57, no. 7, pp. 1597-1607, 2010.

[36] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur and H.-S. P. Wong, "Device Scaling Limits of Si MOSFETS and their Application Dependencies," *Proceedings of the IEEE,* vol. 89, no. 3, pp. 259-288, 2001.

[37] M. Cimino, H. Lapuyade, M. De Matos, T. Taris, Y. Deval and J.-B. Begueret, "A Robust 130 nm-CMOS Built-In Current Sensor Dedicated to RF Applications," *Journal of Electronic Sensing,* vol. 23, no. 6, pp. 593-603, 2007.

ADDENDUM A MATLAB

Script A.1 Device characterisation from process data.

```
%% ---------------------------------------------------------------------
----
% Determine NMOS VA
% -----------------
%
% this set of scripts open data from the NMOS Characteristic curves
derived
% from the 8HP models in CADENCE
% ---------------------------------------------------------------------
----
clear;
%load file
load ('calcVA_NMOS\NMOSvgsdata.mat');
figure;
hold on;
grid on;

%plot ids-vds charactersitic curve
plot(vgs100mV(:,1),vgs100mV(:,2));      %vgs = 100 mV
plot(vgs350mV(:,1),vgs350mV(:,2));      %vgs = 350 mV
plot(vgs500mV(:,1),vgs500mV(:,2));      %vgs = 500 mV
plot(vgs700mV(:,1),vgs700mV(:,2));      %vgs = 700 mV
plot(vgs900mV(:,1),vgs900mV(:,2));      %vgs = 900 mV
plot(vgs1200mV(:,1),vgs1200mV(:,2));    %vgs = 1200 mV

% extrapolate slope in saturation region to find VA
vdsi=-5:0.1:1.2;                % region to extrapolate over
interplower = 70;               % lower limit of extrapolation base
data
interhigher = length(vgs100mV); % upper limit of extrapolation base
data

idi100=interp1(vgs100mV(interplower:interhigher,1),vgs100mV(interplower
:interhigher,2),vdsi,'linear','extrap');
idi350=interp1(vgs350mV(interplower:interhigher,1),vgs350mV(interplower
:interhigher,2),vdsi,'linear','extrap');
idi500=interp1(vgs500mV(interplower:interhigher,1),vgs500mV(interplower
:interhigher,2),vdsi,'linear','extrap');
idi700=interp1(vgs700mV(interplower:interhigher,1),vgs700mV(interplower
:interhigher,2),vdsi,'linear','extrap');
idi900=interp1(vgs900mV(interplower:interhigher,1),vgs900mV(interplower
:interhigher,2),vdsi,'linear','extrap');
idi1200=interp1(vgs1200mV(interplower:interhigher,1),vgs1200mV(interplo
wer:interhigher,2),vdsi,'linear','extrap');

%plot(vdsi,idi100,'g');
%plot(vdsi,idi350,'g'); % These are not plotted. Device is off
plot(vdsi,idi500,'k');
plot(vdsi,idi700,'k');
plot(vdsi,idi900,'k');
plot(vdsi,idi1200,'k');

xlabel('Vds');
ylabel('Ids');
ylim([0e-4 3.5e-4]);
title('NMOS IDS-VDS CHARACTERISTIC CURVES FOR W/L = 6 ');
```

```
%% ------------------------------------------------------------------------
----
% Determine PMOS VA
% -----------------
%
% this set of scripts open data from the PMOS Characteristic curves
derived
% from the 8HP models in CADENCE
% ------------------------------------------------------------------------
----
%load file
load ('VA_PMOS\PMOSvgsdata.mat');
figure;
hold on;
grid on;
%plot ids-vds characteristic curves
plot(Pvgs100mV(:,1),Pvgs100mV(:,2));     %vgs = 100 mV
plot(Pvgs200mV(:,1),Pvgs200mV(:,2));     %vgs = 200 mV
plot(Pvgs400mV(:,1),Pvgs400mV(:,2));     %vgs = 400 mV
plot(Pvgs600mV(:,1),Pvgs600mV(:,2));     %vgs = 600 mV
plot(Pvgs800mV(:,1),Pvgs800mV(:,2));     %vgs = 800 mV
plot(Pvgs1000mV(:,1),Pvgs1000mV(:,2));   %vgs = 1000mV
plot(Pvgs1200mV(:,1),Pvgs1200mV(:,2));   %vgs = 1200mV

xlabel('Vds');
ylabel('Ids');
ylim([0e-4 2e-4]);
title('PMOS IDS-VDS CHARACTERISTIC CURVES FOR W/L = 6 ');

% extrapolate slope in saturation region to find VA
Pvdsi = -0.8:0.1:1;      % region to extrapolate over
Pinterplower = 1;        % lower limit of extrapolation base data
Pinterphigher = 30;      % upper limit of extrapolation base data

Pidi100 =
interp1(Pvgs100mV(Pinterplower:Pinterphigher,1),Pvgs100mV(Pinterplower:
Pinterphigher,2),Pvdsi,'linear','extrap');
plot(Pvdsi,Pidi100,'k');

Pidi200 =
interp1(Pvgs200mV(Pinterplower:Pinterphigher,1),Pvgs200mV(Pinterplower:
Pinterphigher,2),Pvdsi,'linear','extrap');
plot(Pvdsi,Pidi200,'k');

Pidi400 =
interp1(Pvgs400mV(Pinterplower:Pinterphigher,1),Pvgs400mV(Pinterplower:
Pinterphigher,2),Pvdsi,'linear','extrap');
plot(Pvdsi,Pidi400,'k');

Pidi600 =
interp1(Pvgs600mV(Pinterplower:Pinterphigher,1),Pvgs600mV(Pinterplower:
Pinterphigher,2),Pvdsi,'linear','extrap');
plot(Pvdsi,Pidi600,'k');

Pidi800 =
interp1(Pvgs800mV(Pinterplower:Pinterphigher,1),Pvgs800mV(Pinterplower:
Pinterphigher,2),Pvdsi,'linear','extrap');
plot(Pvdsi,Pidi800,'k');

Pidi1000 =
```

```
interp1(Pvgs1000mV(Pinterplower:Pinterphigher,1),Pvgs1000mV(Pinterplowe
r:Pinterphigher,2),Pvdsi,'linear','extrap');
plot(Pvdsi,Pidi1000,'k');

Pidi1200 =
interp1(Pvgs1200mV(Pinterplower:Pinterphigher,1),Pvgs1200mV(Pinterplowe
r:Pinterphigher,2),Pvdsi,'linear','extrap');
plot(Pvdsi,Pidi1200,'k');
```

Script A.2 SenseFET approximate model.

```
%% Simple Sensefet Mathematical approximation
%
% The code approximates the Simple SenseFET.
%
================================================================================
==
clear all;

% constants
L = 10e-6; %1uH
VDD = 1.2; %1.2 V
VA = 0.5; % transistor VA
K = 200; % scale factor for sensefet
kp = 50e-6; %k prime for PMOS
kn = 100e-6; % k prime for NMOS
WL1 = 6; %W/L for Transistor M1 (diode connected sensing MOS)
WL4 = 6; %W/L for Transistor M4 (diode connected sensing MOS)
WL2 = 26.6; %W/L for Transistor M2 (biasing nfet)
vt = 0.35; % threshhold voltage of mos
vbias = 0.425; %biasing voltage
RL = 1; % Inductor resistance
RSense = 1e3; % Output sesne resistor in Ohm



% inductor current is defined by
Iind = 0:0.01e-3:12e-3; % then inductor current
Tind = 0:(100e-9)/length(Iind):100e-9 - (100e-9)/length(Iind); % the
time sampling for the increase in current

%reserve mem
vl = zeros(size(Tind)); % Inductor Voltage
vd2 = zeros(size(Tind)); % Vds for bias Transistor in simple sensfet in
sensing branch

%this constant defines vds1
vds1 = (sqrt((WL2*2*(vbias-vt)^2)/WL1)+vt);

for i =1 :length(Iind)-1
    vl(i) = L*(Iind(i+1) - Iind(i))/(Tind(i+1) - Tind(i)) - RL*Iind(i);
% this evaluates L*di/dt

    vd2(i) = vl(i) - vds1;
end

% the sense curret is defined by
%Isense = Iind/K + kp*WL2*0.5*(vgs-vt)^2*(1+vds/VA);

%%
```

```
%=========================================================================
=
%   Output Voltage Vsense Approximation
% ------------------------------------
% Expressions derived for the Vsense for the simple case are
approximated
%
%=========================================================================
==

% the sensed current in terms of a voltage is given by
% Vsense = ( InductorCurrent/Kratio - K`(w/l)4*0.5*(Vdd-Ldi/dt)^2)R
% reserve mem
Vsense = zeros(size(Tind)); % Sensed Voltage
VsenseL = zeros(size(Tind)); % Sensed Voltage
VsenseM4 = zeros(size(Tind)); % Sensed Voltage

% The transistor M4's constant is:
KM4 = kp*WL4*0.5;

for i =1 :length(Iind)-1
    vl(i) = L*(Iind(i+1) - Iind(i))/(Tind(i+1) - Tind(i)) -
RL*Iind(i);% this evaluates L*di/dt
    Vsense(i) = RSense * (Iind(i)/K - KM4*(VDD-vl(i))^2);
    VsenseL(i) = RSense * Iind(i)/K;
    VsenseM4(i) = RSense * KM4*(VDD-vl(i))^2;
end

%%
%=========================================================================
=
%   Plot Results
%
%=========================================================================
=

close all;

subplot(3,1,1);
plot(Tind(1:length(Tind)-1),vl(1:length(Tind)-1),'r--');
xlabel('useconds');
ylabel('Volts');
title('First order approximation of Inductor voltage and VG of the
diode connected sensing FET');


subplot(3,1,2);
plot(Tind(1:length(Tind)-1),vd2(1:length(Tind)-1),'b:');
subplot(3,1,3);
plot(Tind(1:length(Tind)-1),Vsense(1:length(Tind)-1),'g-');
hold on;
plot(Tind(1:length(Tind)-1),VsenseL(1:length(Tind)-1),'b-.');
plot(Tind(1:length(Tind)-1),VsenseM4(1:length(Tind)-1),'r--');

%legend('Inductor','VG','Vsense');
```

Script A.3 Import and condition oscilloscope data.

```
function [filtered_data,time_index,inductor_v_data] =
import_scope_data(workbookFile, sheetName, range)
%IMPORTFILE Import numeric data from a spreadsheet
%   DATA = IMPORTFILE(FILE) reads all numeric data from the first
worksheet
%   in the Microsoft Excel spreadsheet file named FILE and returns the
%   numeric data.
%
%   DATA = IMPORTFILE(FILE,SHEET) reads from the specified worksheet.
%
%   DATA = IMPORTFILE(FILE,SHEET,RANGE) reads from the specified
worksheet
%   and from the specified RANGE. Specify RANGE using the syntax
%   'C1:C2',where C1 and C2 are opposing corners of the region.
%
%   Non-numeric cells are replaced with: 0.0
%
% Example:
%   untitled = importfile('scope_6.csv','scope_6','A1:B2002');
%
%   See also XLSREAD.

% Auto-generated by MATLAB on 2014/07/28 23:06:43

%% Input handling

% If no sheet is specified, read first sheet
if nargin == 1 || isempty(sheetName)
    sheetName = 1;
end

% If no range is specified, read all data
if nargin <= 2 || isempty(range)
    range = '';
end

%% Import the data
[~, ~, raw] = xlsread(workbookFile, sheetName, range);

%% Replace non-numeric cells with 0.0
R = cellfun(@(x) ~isnumeric(x) || isnan(x),raw); % Find non-numeric
cells
raw(R) = {0.0}; % Replace non-numeric cells

%% Create output variable
data = cell2mat(raw);

%% Strip out scope generated data set names
    %% Need to test if scope data is 2k or 1k samples. when capturing
on 2 channels the sample size per channel is reduced.
    %% If Inductor voltage data is present then it needs to be extraced
as well.
time_index = data(:,1);
signal_data = data(:,2);
data_size = size(data);

if data_size(2) > 2
    inductor_v_data = data(:,3);
else
    inductor_v_data = 0;
```

```
end

if length(time_index) > 1500
    time_index = time_index(3:2002)*1e6;
    signal_data = signal_data(3:2002)*1e3;
    inductor_v_data = inductor_v_data (3:2002)*1e3;
else
    time_index = time_index(3:1002)*1e6;
    signal_data = signal_data(3:1002)*1e3;
    inductor_v_data = inductor_v_data (3:1002)*1e3;
end

%% create Filter
windowsize = 10;
filtered_data = filter(ones(1,windowsize)/windowsize,1,signal_data);
inductor_v_data=filter(ones(1,windowsize)/windowsize,1,inductor_v_data)
;
```

Script A.4 Calculate transresistance gain from captured data.

```
function CalcGainfromFile(workbookFile, sheetName, range)
%IMPORTFILE Import numeric data from a spreadsheet
%   DATA = IMPORTFILE(FILE) reads all numeric data from the first
worksheet
%   in the Microsoft Excel spreadsheet file named FILE and returns the
%   numeric data.
%
%   DATA = IMPORTFILE(FILE,SHEET) reads from the specified worksheet.
%
%   DATA = IMPORTFILE(FILE,SHEET,RANGE) reads from the specified
worksheet
%   and from the specified RANGE. Specify RANGE using the syntax
%   'C1:C2',where C1 and C2 are opposing corners of the region.
%
%   Non-numeric cells are replaced with: 0.0
%
% Example:
%   untitled = importfile('Vsense.csv','Vsense','A2:H12082');
%
%   See also XLSREAD.

% Auto-generated by MATLAB on 2014/06/08 22:27:28

%% Input handling

% If no sheet is specified, read first sheet
if nargin == 1 || isempty(sheetName)
    sheetName = 1;
end

% If no range is specified, read all data
if nargin <= 2 || isempty(range)
    range = '';
end

%% Import the data
[~, ~, raw] = xlsread(workbookFile, sheetName, range);

%% Replace non-numeric cells with 0.0
```

```
R = cellfun(@(x) ~isnumeric(x) || isnan(x),raw); % Find non-numeric
cells
raw(R) = {0.0}; % Replace non-numeric cells

%% Create output variable
data = cell2mat(raw);

%% Extract each data vector
Transient_time = data(:,1);
Inductor_current = data(:,6);
VsenseREF = data(:,2);
VsenseCAS = data(:,4);

%% Find truncation bounds
bound_lower = 4.5505e-6;
bound_upper = 4.60e-6;

bottom = find(Transient_time >= bound_lower);
bottom_bound = bottom(1);
clear bottom; %%cleaning

top = find(Transient_time <= bound_upper);
Top_bound = top(length(top));
clear top; %%cleaning

%% Truncate data
Transient_time_trunc = Transient_time(bottom_bound:Top_bound);
Inductor_current_trunc = Inductor_current(bottom_bound:Top_bound);
VsenseREF_trunc = VsenseREF(bottom_bound:Top_bound);
VsenseCAS_trunc = VsenseCAS(bottom_bound:Top_bound);

clear Transient_time Inductor_current VsenseREF VsenseCAS; %% cleaning

%% Scaled Quantities
Time_in_us = Transient_time_trunc * 1e6;
Current_in_mA = Inductor_current_trunc * 1e3;

%% Calculate TransR gain
Ref_transresistance = VsenseREF_trunc.\Inductor_current_trunc;
CAS_transresistance = VsenseCAS_trunc.\Inductor_current_trunc;


%% Normalize data for comparative plots
Inductor_current_norm =
Inductor_current_trunc/max(Inductor_current_trunc);
VsenseREF_norm = VsenseREF_trunc/max(VsenseREF_trunc);
VsenseCAS_norm = VsenseCAS_trunc/max(VsenseCAS_trunc);



%% Clears all figures
close all;

%% plot normalized outputs vs truncated time
plot(Time_in_us,VsenseREF_norm,'g','LineWidth',2);
hold on;
plot(Time_in_us,VsenseCAS_norm,'b','LineWidth',2);
plot(Time_in_us,Inductor_current_norm,'r','LineWidth',2);
hold off;
title('Normalized outputs of VsenseREF and VsenseCAS and sensed current
```

```
in one half cycle');
xlabel('Time (us)');
ylabel('Normalized amplitude');
legend('VsenseREF','VsenseCAS','Current','Location','Best');
grid on;

%% plot Transresistance vs sense current
figure;
plot(Current_in_mA,Ref_transresistance,'g','LineWidth',2);
hold on;
plot(Current_in_mA,CAS_transresistance,'b','LineWidth',2);
hold off;
title('Transresistence vs Sensed Current');
xlabel('Sensed current (mA)');
ylabel('Transresistance gain (ohm)');
legend('Reference SensFET','Cascode SensFET','Location','Best');
grid on;
```

Script A.5 Post-processing measurement data prior to measurement.

```
function ParseData(L, sensor_data, time_data, L_voltage)
%ParseData Conditions scope data from the SenseFET prototype
%   L = Indcutor value used in uH
%   sensor_data = The captured sensor output voltage data
%   time_data = the time data that corresponds to the sensor data
%   L_voltage = the captured Voltage drop over the inductor

%% Conditioning inputs

L = L * 1e-6; % Convert uH to H
sample_rate = time_data(10) - time_data(9) % this sample rate is in us
time_index = time_data; %(1:1:length(time_data))*sample_rate;
length_time = length(time_index)

%% Integrate to get inductor current from voltage -first attempts

    % Removing DC Component
VL_dc = mean(L_voltage);
L_voltage = L_voltage - VL_dc;
    % Scale to Volts
L_voltage = L_voltage / 1000;

    % Numerically integrating Inductor voltage between each timestep.
The
    % delta between each step is used to contruct the integral of the
    % inductor voltage

IL = zeros(1,length(L_voltage));

IL = -1*cumtrapz(L_voltage)*sample_rate*1e-6;
IL = IL - mean(IL);
IL = IL/L;

%scale back to mA and mV
L_voltage = L_voltage*1000 + VL_dc;
IL = IL * 1000;
sensor_data_ac = sensor_data - mean(sensor_data);
```

```
%% plotting result of integration with sensor voltage and inductor
voltage
plot(time_index,L_voltage);
hold on;
plotyy(time_index,sensor_data,time_index,IL);

%% Determine Transresistance gain
% Calculate transresistance gain
% Discontinuity caused by values close to 0 are filtered our for
% readibility of generated graphs

transRes_1uH = zeros(1,length(time_index));

for i=1:1:length(time_index)
    transRes_1uH(i)= sensor_data_ac(i) / IL(i);
end;

transRes_1uH_mean = mean(transRes_1uH);
limit_scale = 50;

for i=1:1:length(time_index)
    if (transRes_1uH(i) > abs(limit_scale*transRes_1uH_mean)) &&
(transRes_1uH(i) > 0)
        transRes_1uH(i)= abs(limit_scale*transRes_1uH_mean);
    elseif (transRes_1uH(i) < -abs(limit_scale*transRes_1uH_mean)) &&
(transRes_1uH(i) < 0)
        transRes_1uH(i)= -abs(limit_scale*transRes_1uH_mean);
    end;
end;

figure;
%plot(time_index,transRes_1uH,'b','Linewidth',2);
plotyy(time_index,sensor_data,time_index,transRes_1uH);
%xlim([time_index(400) time_index(700)]);  %Truncates to ~ 1 switching
cycle for visibility
grid on;
title('Transresistance gain');
xlabel('Time in us');
ylabel('V/A');
hold on;
%plot(time_index,sensor_data_ac,'g','LineWidth',2);
plot(time_index,IL,'r','LineWidth',2);
```

ADDENDUM B PCB SCHEMATICS

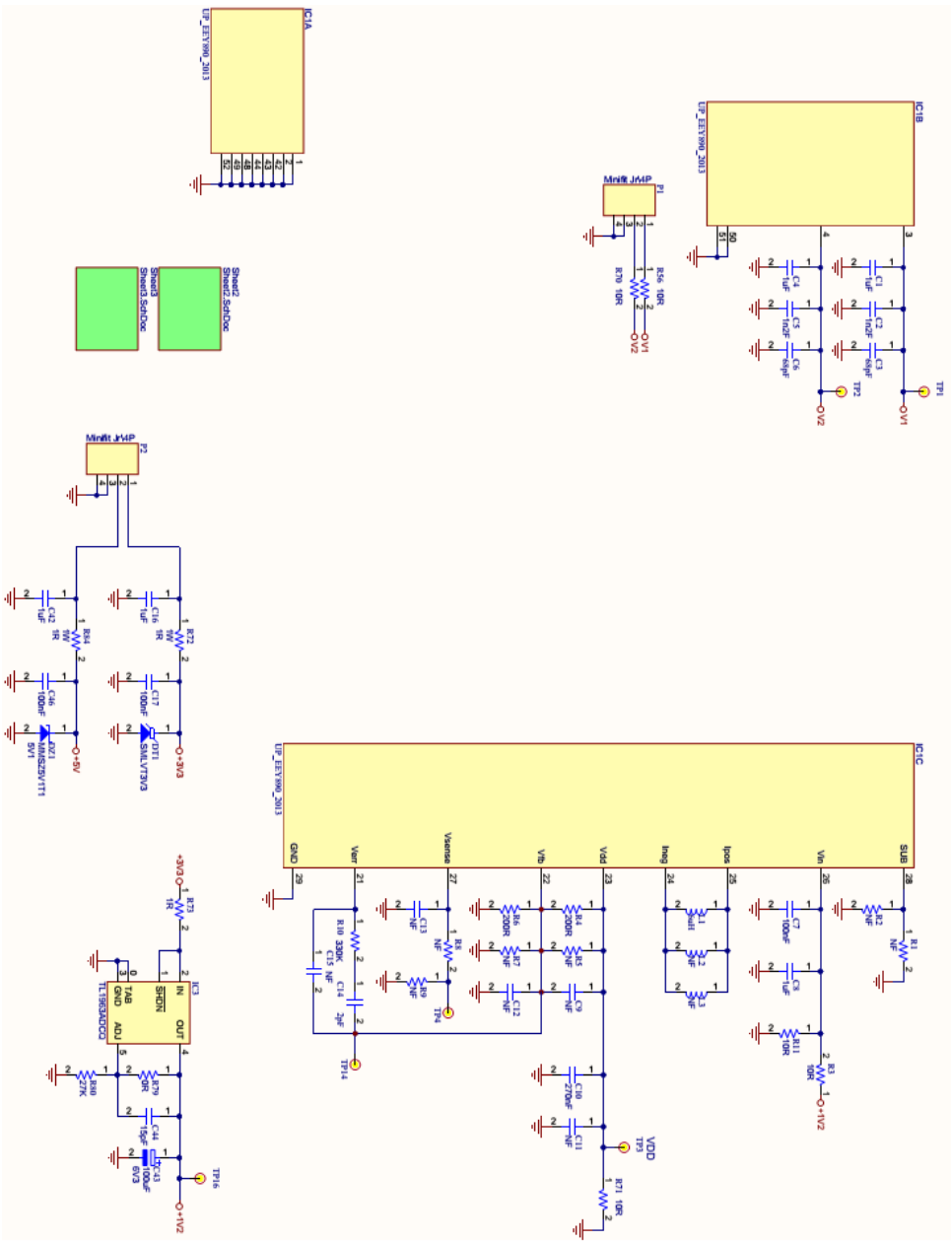

Figure B.1. Schematic page one.

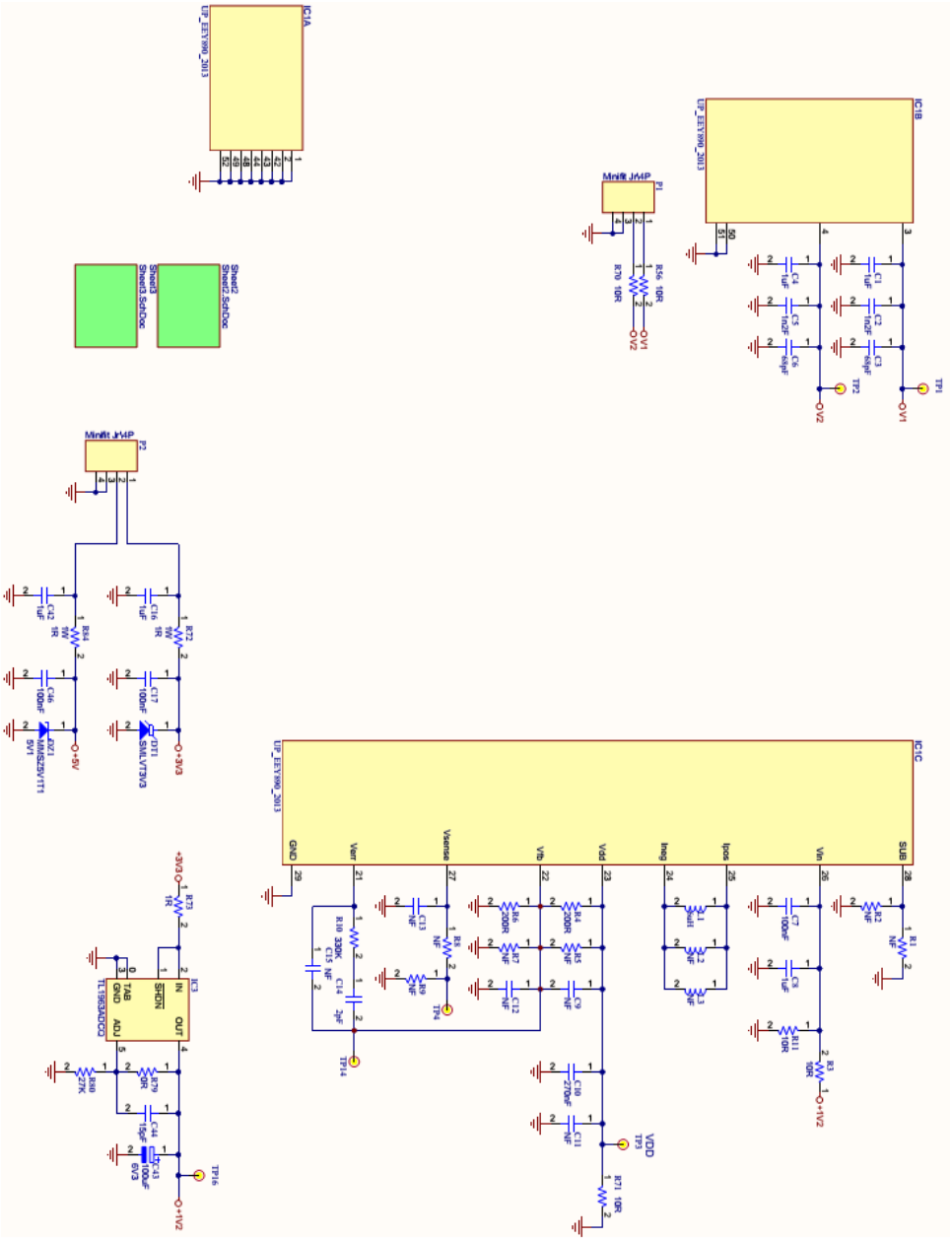

Figure B.2. Schematic page two.