Low voltage DC distribution system comprising of a small wind generator and a battery energy storage system

by

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SUMMARY

LOW VOLTAGE DC DISTRIBUTION SYSTEM COMPRISING OF A SMALL WIND GENERATOR AND A BATTERY ENERGY STORAGE SYSTEM

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Current trends in electrical power consumption indicate that there is an increase in the number of electrical appliances that consume direct current (DC) power such as computers, lighting appliances, TVs and other electronic-based apparatus. There is also a widespread adoption of distributed generators near the load centres, which are mostly DC (photovoltaic systems, battery storage systems and fuel cells), to improve the voltage profile and reduce power losses. Distribution of electric power in DC form therefore, serves to eliminate the several conversion stages common in AC distribution systems. Consequently, there is greater savings in the cost of system implementation and higher reliability due to a decreased number of converters. The growth of DC microgrids has further encouraged the harnessing of other none DC renewable energy sources such as wind which is abundant and a clean source. However, interfacing of wind energy source to a DC distribution demands a high voltage boost active rectifier and proper feedback control to handle its intermittent nature which has the potential to introduce voltage flicker in the distribution system.

This research will focus on the design of a small wind energy conversion (SWEC) system ideal for interfacing low voltage wind generator to a DC distribution system. The proposed SWECS comprises

of a three-phase diode rectifier cascaded with an interleaved tapped-coupled inductor boost DC-DC converter. This converter topology will provide very high boost voltage rectification, low input- and output-side current ripple, good input disturbance rejection and output voltage regulation. A good combination of the coupled-inductor turns ratio and duty cycle of the converter will be chosen to provide the necessary boost ratio while keeping the device blocking voltages within acceptable limits. Consequently, the proposed SWECS interface will have a small structure, simple PWM control circuitry and high efficiency.

To further address the intermittent nature of wind energy resource, a low voltage battery energy storage system (BESS) will be incorporated in the distribution system. Low voltage BESS offer the best solution in energy storage due to their low cost, mature technology and few cell failures. However, they require a high voltage gain and bidirectional power flow converter for proper operation and efficient integration to a distribution system. In this regard, the research will focus on the design of an efficient, high boost and low cost converter suitable for interfacing this low voltage BESS to the distribution system. The proposed interface comprises of a bidirectional tapped-coupled inductor boost DC-DC converter. This converter will adopt the concept of converter interleaving to enable current ripple cancellation at the converter input and output, so that the size of converter components are significantly reduced. Further reduction in inductor size will be demonstrated through application of coupled inductors, in which two-phase inductors share the same core, to provide the same effective inductance as two larger non-coupled phase inductors. A novel passive lossless snubber circuit will be employed to clamp the voltage spikes across the active switches without altering the normal operation of the converter.

LIST OF ABBREVIATIONS

AC	Alternating current
DC	Direct current
RMS	Root mean squared
DERs	Distributed energy resources
PMSG	Permanent magnet synchronous generator
VSC	Voltage-source converter
PWM	Pulse width modulation
THD	Total harmonic distortion
EMI	electromagnetic interference
MOSFET	Metal oxide semiconductor field effect transistor
PFC	Power Factor Correction
SoC	State of Charge
BESS	Battery energy storage system
SWECS	Small wind energy conversion systems
RPM	Revolution per minute
DFIG	Doubly-fed induction generator
IEEE	Institute of electrical and electronics engineer
ACMC	Average current-mode controller
CCM	Continuous conduction mode
CCS	Code Composer Studio
ZVS	Zero voltage switching
TIBC	Tapped-coupled inductor boost converter

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CHAPTER 1 INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Background and context

The current advances in the harnessing of renewable energy sources such as wind and solar have resulted in the increased application of DC systems in power distribution. DC distribution systems have numerous advantages to offer compared to conventional AC distribution systems. These include: high power transmission capability, improved reliability, simple structure, and reduced losses [1–3]. They are also able to handle the intermittent Distributed Energy Sources (DERs) owing to their simplified power flow control schemes.

In the past, electrical power was generated from centralized power plants and transmitted over long distances to the point of consumption. Any load growth necessitated either the expansion of the existing substation and transmission capacity, or the construction of new substations [4]. However, the recent trend has seen development of distributed generators near the load centres to improve the voltage profile, reduce losses and improve the system efficiency. This concept of having a cluster of loads and a host of sources operating as a unit is referred to as a microgrid [5]. Compared to an AC microgrid, a DC microgrid offers several advantages such as high efficiency, reduced number of converters and relative ease of renewable energy integration. A DC microgrid can be connected to the main AC grid or independently operated in islanded mode. In the latter mode of operation, the DC microgrid is easier to design since it is devoid of synchronization and reactive power issues that are inherent in its AC counterpart [6].

A huge portion of the future energy sources will be harnessed from renewable energy sources with the biggest portion coming from wind. The wind energy conversion system (WECS) based on a permanent magnet synchronous generator (PMSG) is the most popular technology since it does not require an extra excitation device and can adopt a direct-driven form [7–9]. However, the intermittency nature of the wind energy resource has the capacity to introduce a voltage flicker in the system. Therefore, there is need to incorporate an energy storage system to ensure proper voltage regulation in the distribution system. In addition, full harnessing of renewable energy sources (RES) requires a converting stage that can boost the often low and variable voltages from RES to the high and constant distribution system voltages [3].

1.1.2 Research gap

The ever growing demand for electrical energy coupled with the depleting reserves of fossil fuel resources have driven the uptake of renewable energy sources as an alternative source of energy. Wind is one of the most abundant renewable energy sources that can be freely tapped from nature. Wind energy conversion systems can be operated as either stand-alone systems or grid-connected systems. Majority of the previous works relating to small wind energy systems have dealt with grid-connected systems and the analysis thereof cannot be extended to stand-alone systems due to the operational differences. However, there are some few research works which have proposed converter topologies that can integrate small and low voltage wind generators to stand-alone distribution systems. One of these researches has proposed a diode rectifier with a capacitor voltage filter which has high reliability and low implementation costs. However, this topology suffers from low voltage boost ratios, poor input power factor and high levels of total harmonic distortion (THD), in generator currents which reduces the overall system efficiency. Another research has proposed a voltage source converter (VSC) which has very high input power factor and low THD. However, it has very low voltage boost ratio.

Wind energy is a highly erratic resource and can easily transfer voltage disturbances to the grid. There is need to employ a conversion interface that can extract maximum power from the wind turbines, and boost the often low and variable generator voltages to the high and constant levels required in the distribution systems. This research work will hence focus on the design of a small wind energy conversion system (SWECS) ideal for interfacing low voltage wind generator to a distribution system. The proposed SWECS will provide high boost voltage rectification, good input disturbance rejection,

and low input- and output-side voltage and current ripple. The research will further focus on regulation of voltage on the DC distribution system by introducing energy storage. Low voltage battery systems offer the best solution in energy storage due to their low cost, mature technology and few cell failures. The only challenge is in realising an effective bidirectional converter to interface them to the grid. Some research has proposed full bridge isolated DC-DC converter which provides a very high voltage boost and bidirectional power flow. However, the transformer employed in this converter topology does not only make the converter bulky, but also experiences magnetic saturation due to current flowing in it. In this research work, a simple and high voltage gain bidirectional converter will be designed to integrate the low voltage battery energy storage system to the grid.

1.2 RESEARCH OBJECTIVE AND QUESTIONS

The research questions to be addressed include:

- How to interface a small low voltage wind generator to a DC bus?
- How to realise a wind generator interface with high boost voltage rectification?
- How to implement a system that operates over a wide input voltage range while achieving output voltage regulation with optimal conversion efficiency?
- How to realise a system with good supply and load-side disturbance rejection?
- How to achieve proper energy management in a DC microgrid in the presence of intermittent wind energy?
- How to interface a low voltage battery storage system to a DC bus?
- How to realise an effective lossless snubber circuit that does not interfere with the normal operation of the interfaces?

The objective of this research is to design a low voltage DC distribution system comprising of a small low voltage wind generator and a low voltage battery storage system. The research will particularly focus on design, simulation and hardware implementation of converter interfaces which are capable of ensuring:

- A high voltage boost ratios for both the low voltage wind generator and low voltage battery storage system.
- Output voltage regulation.
- Rejection of input and load-side voltage disturbances.
- Current ripple cancellation at the converter input and output, so that the size of converter components are significantly reduced.
- Bidirectional power flow to allow for the charging and discharging of the low voltage battery storage system
- Small structure and low cost converters achieved through careful selection of the tapped-coupled inductor turns ratio and duty-cycle which effectively leads to the need for converter components with low voltage ratings.

1.3 HYPOTHESIS AND APPROACH

Small low voltage wind generators can be interfaced to a DC distribution grid using a wide input and high voltage gain active rectifier. On the other hand, energy management in the distribution system can be provided by a low voltage battery storage system interfaced to the distribution grid using a low cost and high voltage gain bidirectional boost DC-DC converter.

The following approach will be followed in this research:

- Literature study to identify previous works relating to low voltage DC microgrid incorporating wind generators and energy storage systems.

- Steady-state and dynamic analysis of a high boost voltage rectifier comprising on three-phase diode rectifier cascaded with two-phase tapped-coupled inductor DC-DC converter for low voltage wind generator integration.

- Steady-state and dynamic analysis of a high voltage gain bidirectional DC-DC converter comprising of two-phase tapped-coupled inductor boost converter for interfacing low voltage battery storage system.

- Small signal analysis of the converter interfaces to enable modelling of the systems controller.

- Software simulation of the systems to validate theoretical analysis.

- Hardware implementation of converter prototypes to provide additional validation of the systems performance.

1.4 RESEARCH GOALS

The research aims at achieving the following goals:

- Development of an electronic power processor that can achieve very high voltage boost rectification suitable for low voltage wind generator applications.

- Development of converter interfaces with good rejection of input and load-side voltage disturbances.

- Development of an electronic power processor with bidirectional power flow capability and high voltage gain for interfacing low voltage battery system to a DC bus.

- Design and development of a highly effective controller that ensures proper output voltage regulation as well as rejection of load disturbances.

- Design and development of a bidirectional passive lossless snubber that effectively clamps voltage spikes across the low voltage battery interface.

1.5 RESEARCH CONTRIBUTION

This research is geared towards the design of a robust, low cost and a high efficiency low voltage DC distribution system that incorporates a small low voltage wind generator and low voltage battery storage system. Currently, the most popular converter topology for interfacing small low voltage wind generator to a DC distribution system is a diode rectifier with an output capacitor to smooth out voltage ripples. This topology suffers from low boost ratios and injection of low order current harmonics into the generator supply. This research therefore proposes a high boost voltage rectifier comprising of a three-phase diode rectifier cascaded with an interleaved tapped-coupled inductor DC-DC converter. This interface is capable of achieving voltage boost ratios of 6 times, low total harmonic distortion of 20%, high input power factor of 0.94, and good rejection of input- and load-side disturbances.

The second contribution of this research will be in the realisation of a low voltage battery interface. Majority of the available battery interfaces employ isolated converter topologies to provide bidirectional flow of current and high voltage boost ratios. However, the transformer employed in these interfaces make them bulky and expensive. This research proposes an interleaved bidirectional tapped-coupled inductor boost converter. This interface has a high voltage gain of approximately 8 and 6 times in boost and buck-mode respectively, output voltage regulation, small structure and simple control circuitry.

Other outputs from this research will be two journal articles that have been prepared for journal publication:

- High voltage boost active rectifier interface for low voltage wind generator- *IET renewable energy*

- High voltage gain bidirectional interface for low voltage battery energy storage system- *IET renewable energy*

1.6 OVERVIEW OF STUDY

This chapter has introduced the background and context of the research work. It has identified the research gap, listed the research questions and objectives and briefly explained the approach that will be followed in this research work.

Chapter 2 presents the previous technologies identified to interface small low voltage wind generators and low voltage battery storage systems to DC distribution systems. The strengths and weakness of each solution is analysed and the chapter concludes by presenting the proposed converter interfaces to address the gaps identified.

In chapter 3, a detailed analysis of the proposed conversion systems to interface a small wind energy system and a low voltage battery to a DC distribution system are presented. The proposed SWECS comprises of a three-phase diode rectifier cascaded with an interleaved tapped-coupled inductor boost converter while the battery interface comprises of an interleaved bidirectional tapped-coupled inductor boost converter. The equivalent circuits of each individual component in the systems are presented. Small-signal transfer functions are obtained and used later to model the system controller.

Chapter 4 presents the average current mode controller design for the proposed converter interfaces. MATLAB plots and step-responses are provided to verify the operation of the proposed interface.

In chapter 5, the simulation results for the low voltage DC distribution system comprising of SWECS and low voltage BESS interfaces are presented. The converter simulations are carried out using PSIM software.

In chapter 6, the selection and sizing of magnetic components, semiconductor devices and heat sinks in the proposed conversion system interfaces are presented. This results in a hardware implementation of the system prototype.

Finally, Chapter 7 presents the practical results from the hardware implementation of the systems while Chapter 8 presents the conclusion of the research work and makes recommendations for further research.

CHAPTER 2 LITERATURE STUDY

2.1 CHAPTER OVERVIEW

In this chapter, a literature study of small wind energy conversion system (SWECS) and low voltage battery energy storage systems (BESS) are presented. The various solutions that have been advanced over the years to integrate these renewable energy sources to a distribution grid are examined. Consequently, the gaps that exist in these solutions are identified and a proposal is made to address them.

2.2 SMALL WIND ENERGY CONVERSION SYSTEM

A small wind energy conversion system consists of various components as outlined in the following sections.

2.2.1 Wind turbine

Classification of wind turbine is based on number and the manner in which the blades are mounted on the axis [10]. A three blade horizontal-axis wind turbine offers the best performance since the variations in wind speeds are distributed evenly between the rotor and drive shaft. The amount of power, P_m, that can be extracted from a small wind system is dependent on the aerodynamic characteristics of the wind turbine and the generator's rotor speed and is given by,

$$P_m = 0.5\rho \times C_p \times A \times U_W^3 \tag{2.1}$$

where ρ is the density of air (in kg/m^3), C_p is the power coefficient, A is the area swept by the wind turbine rotor (in m^2), and U_W is the wind speed (in m/s).

2.2.2 Wind turbine generator

The initial SWECS employed fixed speed operating generators such as the squirrel cage generators to extract energy from wind. These generators had reduced performance owing to their fixed speed operation at all wind velocities. The wind turbine performance also depended on the characteristics of the mechanical circuits such as pitch control time constants. Since these mechanical circuits had slow response time, wind energy variations would get transferred to the grid causing instability. It is in the backdrop of these inadequacies that has led to the recent development of variable speed operation generators such as the permanent magnet synchronous generator (PMSG) and the doubly-fed induction generator (DFIG) [11]. These generators allow wind turbines to operate at their optimum tip-speed ratio and hence provide maximum mechanical output power for a wide range of wind speed.

PMSG application in SWECS is more popular than DFIG owing to its compact design, higher efficiency and reduced losses due to the absence of rotor winding [11, 12]. The magnetic field in PMSG is generated by a permanent magnet and hence they do not require a DC supply for the excitation current. Further reduction in cost is facilitated by the elimination of a gearbox due to low rotational speed. However, because of the variable nature of output voltage and frequency, there is need to interface the PMSG to a DC distribution system using a fully controlled frequency converter consisting of a PWM rectifier and a DC-DC converter.

2.2.3 Power converter

Diode rectifier is the preferred choice of converter to interface small low voltage wind generators to DC distribution systems due to its inherent simplicity and low cost [13] . However, diode rectifiers suffer from non-linearity which makes them inject low order current harmonics into the supply leading to an increase in total harmonic distortion (THD). As a result, there is an increase in losses due to overheating, malfunction of equipment and reduced efficiency of the system [13–15]. Therefore, there is need to cascade diode rectifier with an active converter whose control can be used to shape the input line current and ensure that harmonic distortions are within the prescribed limits according to the IEEE 519 standard for a stand-alone system [16].

2.3 SWECS INTERFACE TO A DC DISTRIBUTION SYSTEM

There has been significant progress in realisation of converter topologies that can integrate low voltage wind energy systems into a DC distribution system as outlined in the following sections.

2.3.1 Voltage source converter

Voltage-source converter (VSC), shown in figure 2.1, has previously found application in the integration of wind energy to a DC bus. It offers numerous advantages such as active voltage rectification, output voltage regulation, high input power factor, and the ability to work in rectifying and regenerating mode [17]. In addition, it employs a pulse width modulation (PWM) together with closed-loop current control which allows the active shaping of the input current and hence a total harmonic distortion (THD) below 5% is achieved [18]. However, typical power device switching frequencies of between 2 and 15 kHz can cause high-order harmonics that can affect other sensitive loads or equipment connected on the grid [19]. Some VCS topology employ an LCL filter at the input to reduce this switching frequency harmonics. However, VSC still suffer from high-frequency electromagnetic interference (EMI) in frequency ranges above 150 kHz. In addition, it is not only expensive to implement a three-phase system, due to the high number of MOSFET switches required, but also a complex control system is required.

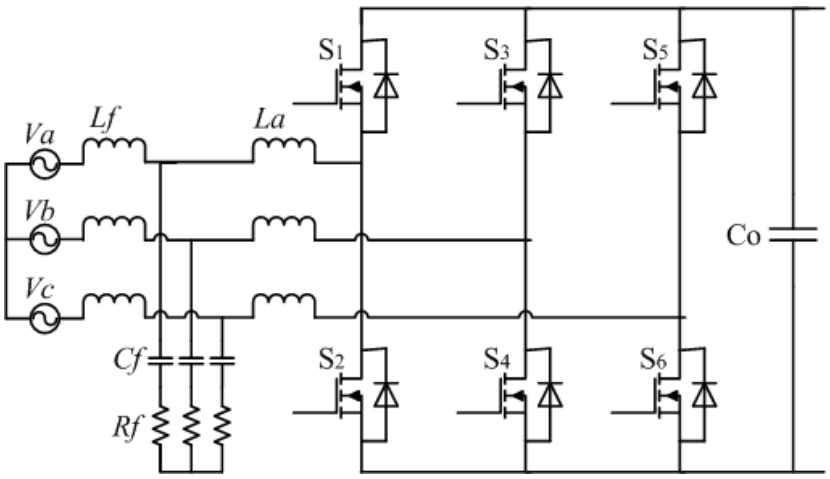

Figure 2.1: Voltage source converter

2.3.2 Diode-bridge rectifier cascaded with single-switch boost chopper

For very low-power wind systems (with rated power less than 5 kW), the most common topology for the rectifier stage is a diode-bridge followed by a conventional DC-DC boost converter for voltage gain. This topology has a simple structure, high reliability and low implementation costs [13]. However, diode rectifier does not only draw non-sinusoidal current from the utility source, but also inject current harmonics which can interfere with other electronic equipment connected on the grid [20]. This necessitates the use of Power Factor Correction (PFC) in order for the system to comply with international standards, such as IEC-1000-3-2 and IEEE-519 [16, 21]. Some converter topologies employs passive components such as capacitors and inductors to improve the power factor. Although these PFC components are effective, the size of the required inductors are large which makes them expensive and bulky. Other topologies employ the active approach by placing a boost converter between the diode rectifier and the load. The active converter regulates the output bus voltage and improves the input power factor [22]. However, it is impractical to achieve boost ratios of more than four in such topologies due to the required large duty-cycle which leads to increased switch blocking voltages and hence high cost and power losses [3].

2.3.3 Diode-bridge rectifier cascaded with double-switch boost chopper

A three phase converter cascaded with two-transistor boost chopper, shown in figure 2.2, has been proposed to address the problems associated with single switch boost converter [23]. This topology employs an LC filter at the AC side to improve the power factor. Active shaping of the input-line current is made possible by two-transistor connected at the rectifier output to lower THD and further improve on the input power factor. However, this converter topology demonstrates poor characteristics when employed in low power applications.

2.3.4 Diode rectifier cascaded with an interleaved boost chopper

A three-phase diode rectifier cascaded with an interleaved boost DC-DC converter, as shown in figure 2.3 has previously been proposed to improve input power factor, lower THD and regulate the output voltage. The interleaved concept adopted in this topology further reduces switch stress, power loss, and volume of magnetic components [24]. However, the boosting ratios of this converter topology is

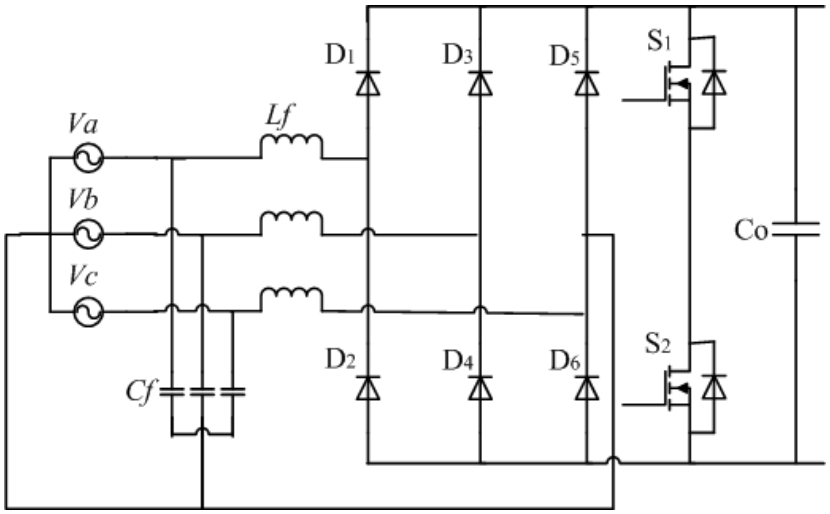

Figure 2.2: Three-phase converter cascaded with two-transistor boost chopper

limited due to the required large duty-cycles. It also suffers from high input- and load-side disturbances especially in the low-frequency region. A current compensator is needed in the PWM controller circuit to mitigate the DC current variations.

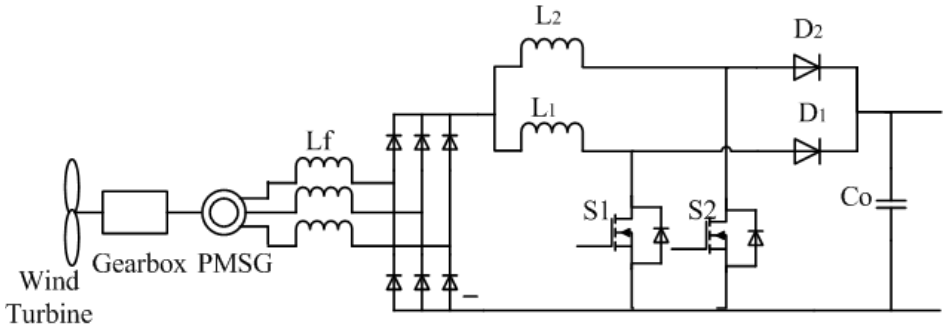

Figure 2.3: Three-phase converter cascaded with interleaved boost DC-DC converter

2.4 BATTERY ENERGY STORAGE SYSTEM

Due to the intermittent nature of wind energy resource, the SWECS power output cannot match the distribution system's demands. This variability of wind power poses a myriad of technical and economic challenges when a wind turbine is connected to a low voltage DC distribution system. There is need for integration of an efficient energy storage system to maintain the system reliability and power quality. Energy storage systems act both as an energy buffer to regulate the voltage on the distribution

grid, and a reservoir which can store excess energy produced by wind sources in off-peak periods with an aim of pumping it back to the grid during the peak periods when demand is high [25, 26].

A review of the available energy storage technologies that can be used for wind power applications has previously been made [27, 28]. These research focussed on the operating principles, main components and the most relevant characteristics of each technology. Battery storage system was found to be the most popular owing to its low cost, portability, fast response time and mature technology. However, cell balancing is critical in battery storage systems that consist of long string of cells in series. This is because individual cells in the pack are exposed to different conditions which affect their states of charge (SoC) and hence they end up with different voltage levels. As a result, the battery cells suffer from deterioration of the pack life and in worst case scenario, they can easily ignite as previously observed in Li-ion batteries [29]. However, a low voltage BESS, such as the proposed 48V, has fewer numbers of cells than a high voltage storage systems. Therefore, it experiences considerably fewer cell failures and does not demand a very expensive electrical insulation. The only challenge employing low voltage BESS is the need for a high voltage boost converter interface with a bidirectional power flow capability. A number of converter interfaces have previously been proposed as outlined in the following sections.

2.4.1 Single-phase, full-bridge bidirectional isolated DC-DC converter

Single-phase full-bridge isolated DC-DC converter, shown in figure 2.4, was first proposed to provide galvanic isolation between the input and output ports [30]. It could also provide bidirectional power flow capability, high voltage boost and high efficiency of over 97%. However, the transformer employed in this converter does not only make the converter bulky, but also experiences magnetic-flux saturation due to a DC-bias current flowing in it.

2.4.2 A hysteric controlled bidirectional DC-DC converter

A hysteric controlled bidirectional DC-DC converter, shown in figure 2.5, was proposed to address the problems associated with isolated converter in BESS applications [31]. It consists of a half-bridge insulated-gate bipolar transistor (IGBT) module with an LCL filter. The converter topology has a small structure, easy control, and high attenuation of current harmonic content which makes the converter

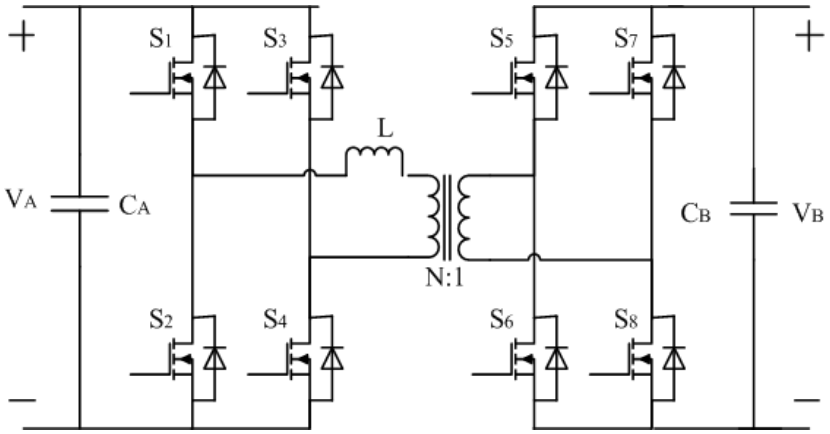

Figure 2.4: Three-phase converter cascaded with interleaved boost DC-DC converter

experience a reduced voltage drop. However, optimum design and analysis of the converter dynamics is not easy due to non-linear behaviour of the power stage and regulation loop.

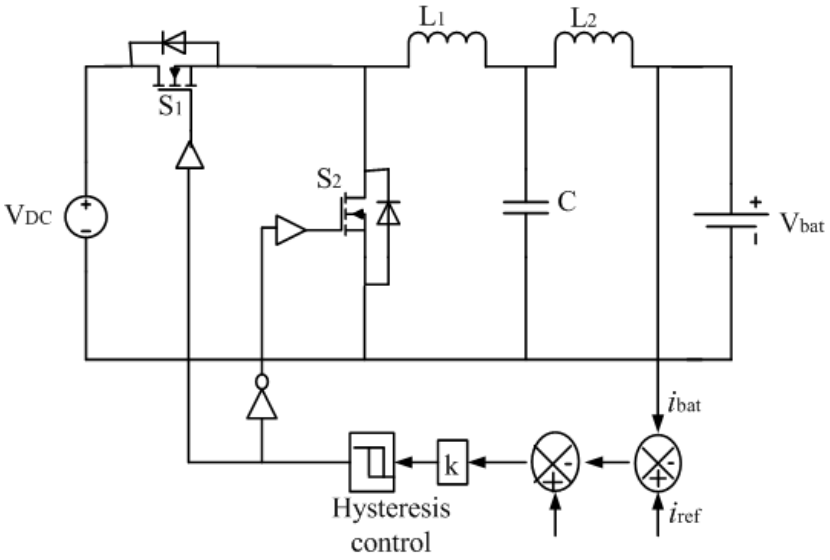

Figure 2.5: Three-phase converter cascaded with interleaved boost DC-DC converter

2.5 PROPOSED LOW VOLTAGE DC MICROGRID

This research proposes a low voltage DC microgrid comprising of a small wind energy conversion system (SWECS) and a low voltage battery storage system interface as shown in figure 2.6.

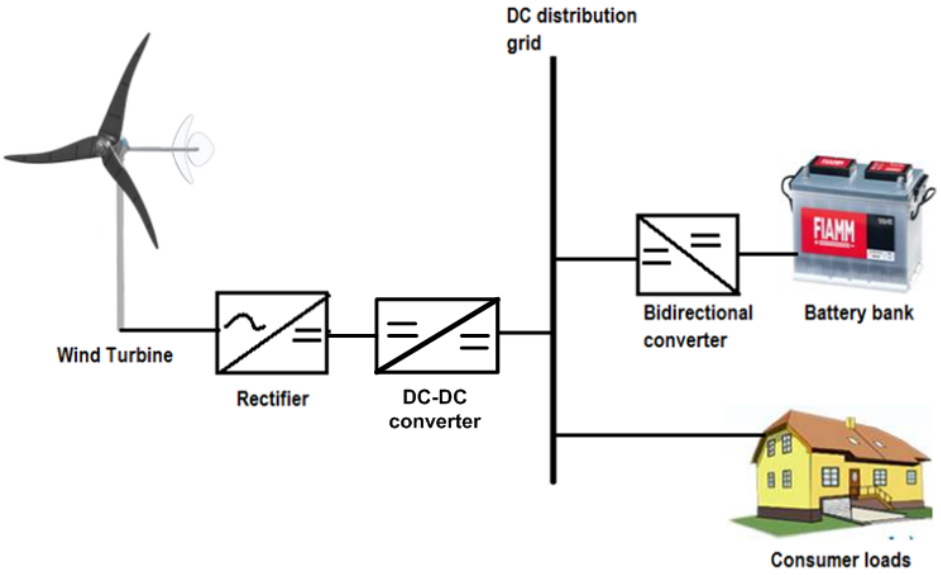

Figure 2.6: The proposed low voltage DC microgrid

2.5.1 Small wind energy conversion system

The research proposes a small wind energy conversion system (SWECS) to interface a low voltage wind generator to a DC bus. The proposed SWECS comprises of a three-phase diode rectifier cascaded with an interleaved tapped-coupled inductor boost DC-DC converter as shown in figure 2.7. A permanent magnet synchronous generator (PMSG), with variable speed operation, is used as the AC voltage source. PMSG is widely employed in small and medium power applications because of the many advantages it offers such as high efficiency, high torque density and reduced maintenance cost due to its brush-less design. On the other hand, tapped-coupled inductor DC-DC converter provides a high boosting ratio without the need for isolation. The two inductor windings N_{IN} and N_{2N} share the same core and are hence magnetically coupled. The large step-up conversion is achieved through a careful selection of the turns ratio and duty-cycle to achieve the necessary boost ratio while keeping the device blocking voltages within acceptable limits.

The proposed SWECS adopts the concept of interleaving to lower the input- and output-side voltage and current ripple [34]. Consequently, the converter is able to handle high power and operate with high reliability, and efficiency, with reduced inductor and capacitor sizes. The research further proposes an average current mode controller (ACMC) which employs two loops to control current (inner loop) and voltage (outer loop). The inner current loop is designed with a higher bandwidth and hence faster

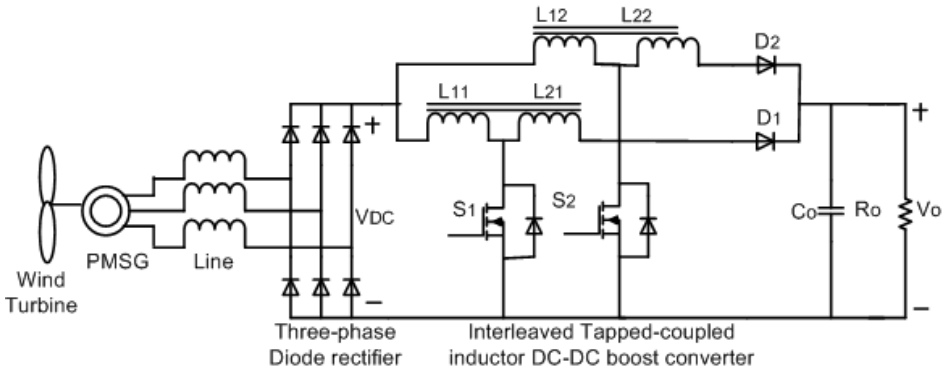

Figure 2.7: Proposed small wind energy conversion system

dynamics compared to the outer voltage loop. The resultant ACMC is able to track the input current accurately enabling less than 2% output voltage regulation. Theoretically derived characteristics of the converter topology will be validated through PSIM simulations and hardware implementation of the prototype.

2.5.2 Low voltage battery interface

This research proposes a high voltage gain bidirectional converter to interface a low voltage battery storage system to a DC bus. The proposed interface consists of a bidirectional tapped-coupled inductor boost converter. This converter interface will also adopt the concept of interleaving to enable current ripple cancellation at the converter input and output, so that the size of filter components is significantly reduced [12]. It will also employ an average current mode control to regulate the output voltage. Figure 2.8. presents the proposed converter interface.

As stated earlier, the main challenge in a converter topology based on tapped-coupled inductor is the presence of leakage inductance due to the non-ideal coupling between the primary and the secondary inductor. The leakage inductance causes high voltage stresses in the active switches, large switching losses, parasitic ringing and severe electromagnetic interference problems which degrades the converter performance. Regenerative snubber circuit offers the best solution in recycling this leakage energy, suppressing the voltage spike and providing lossless switching for the semiconductor switch. It is thus employed in this research.

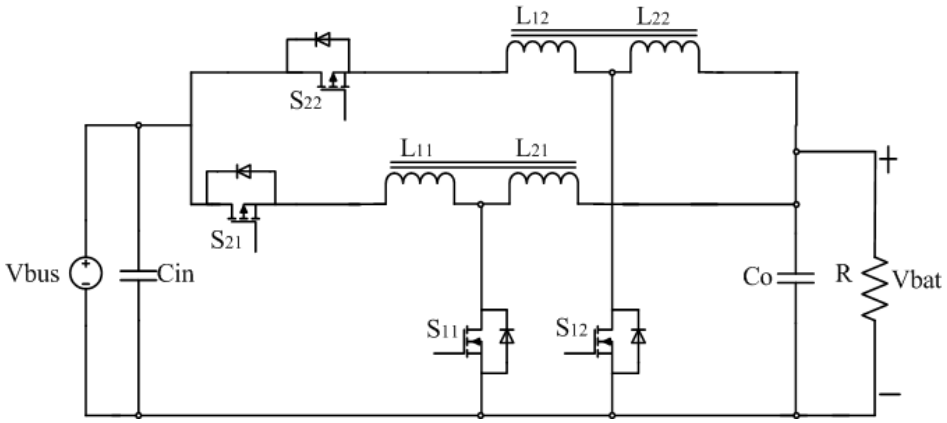

Figure 2.8: Proposed low voltage battery intertace

CHAPTER 3 PROPOSED SYSTEM THEORETICAL ANALYSIS

3.1 CHAPTER OVERVIEW

This chapter presents the performance analysis of the proposed low voltage DC microgrid comprising of a small wind energy conversion system and a low voltage battery interface.

3.2 SMALL WIND ENERGY CONVERSION SYSTEM ANALYSIS

Theoretical analysis of the proposed SWECS comprising of a three-phase diode rectifier cascaded with an interleaved tapped-coupled inductor boost DC-DC converter is presented in this section. Analysis of the converter is done for one phase, since the two phase are identical, with the system operating in the continuous conduction mode (CCM).

3.2.1 Wind turbine generator

A permanent magnet syncronous generator (PMSG) is used as the source of AC voltage. Figure 3.1 illustrates the equivalent circuit of a single-phase non-salient pole PMSG. The induced emf per phase, e_s, when it is subjected to a constant flux per permanent magnet pole, ϕ, while rotating with a speed, ω_g, in (rad/s) is given by the following expression,

$$e_s = k \times \omega_g = \frac{k \times \omega_e}{P} \tag{3.1}$$

where k is machine emf constant in (V/rpm), P is the total number of rotor pole pairs and ω_e is the electrical angular frequency of PMSG stator induced voltage.

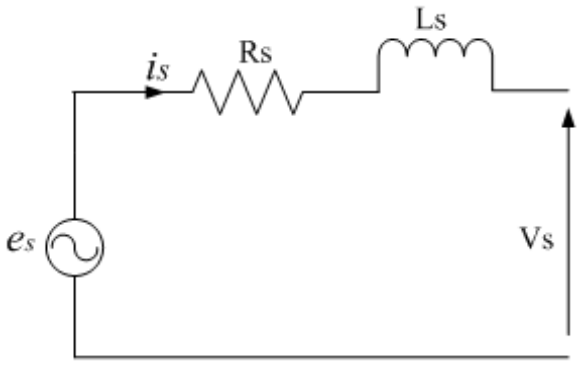

Figure 3.1: Equivalent circuit of a single-phase non-salient pole PMSG

The steady state phase terminal voltage and output power are further obtained using the following expressions

$$V_s^2 = E_s^2 - (\omega_e \times L_s \times I_s)^2 \tag{3.2}$$

$$P_g = 3V_s \times I_s = 3\sqrt{(E_s^2 - (\omega_e \times L_s \times I_s)^2)} \times I_s \tag{3.3}$$

3.2.2 Diode rectifier

A three-phase diode rectifier is used to provide voltage rectification. The relationship between the diode rectifier output voltage and the PMSG terminal voltage is given by,

$$V_{DC} = \frac{3\sqrt{3} \times V_m}{\pi} = 1.65V_m = 2.34V_{s,rms} \tag{3.4}$$

Also,

$$V_{DC} = 1.35V_{ll,rms} \tag{3.5}$$

where $V_{ll,rms}$ is the root mean square value of PMSG line-to-line voltage and $V_{s,rms}$ is the root mean square value of phase terminal voltage.

Assuming 100% voltage rectification and ignoring any power losses, then the output power from the rectifier would be equal to the output power from the PMSG.

$$P_g = P_{DC} = 3 \times V_s \times I_s = V_{DC} \times I_{DC} \tag{3.6}$$

3.2.3 Tapped-coupled inductor boost converter

Circuit components of a two-phase tapped-coupled inductor boost converter comprises of MOSFETs, S_{1N} and S_{2N}, diodes D_{1N} and D_{2N}, two sets of coupled inductor, L_{1N} and L_{2N}, output filter capacitor, C, and a load resistor R. Pulse Width Modulation (PWM) is used to control the MOSFETs by varying the gate pulse to give the desired duty ratio. The gate signal controlling S_{1N} leads the gate signal for S_{2N} by 180°. r_{L1N} and r_{L2N} are input- and output-side inductor resistances, V_{fwd} is the diode forward voltage drop and $r_{ds,on}$ is the MOSFETs channel resistance.

The dynamic analysis and component sizing can be carried out by considering only one phase of the converter since all the phases are identical. The relationship between L_{1N} and L_{2N} is determined by the turn ratio of the magnetic element,

$$\frac{L_{2N}}{L_{1N}} = \left(\frac{N_{2N}}{N_{1N}}\right)^2 = n^2 \tag{3.7}$$

where N_{1N} is the number of turns in the first inductor, L_{1N}, and N_{2N} is the number of turns in the second inductor, L_{2N}.

3.2.3.1 Tapped-coupled inductor boost converter operation

Tapped-coupled inductor boost converter operation is in such a way that either a switch or a diode is conducting at any given time.

a) **Switch is conducting** $(0 < t < \delta T_s)$

When the switch, S_{1N} is conducting, the output diode, D_{1N} is reversed biased. The equivalent circuit of the converter during this interval is shown in figure 3.2.

The voltage measured across the input-side inductor, L_{1N} is given by,

$$V_{L1N} = L_{1N}\frac{di_{L1N}}{dt} = \left(V_{in} - i_{L1N}r_{L1N} - i_{L1N}r_{ds,on}\right) \tag{3.8}$$

Due to magnetic coupling, a voltage is induced on the output-side inductor, L_{2N}, even though there is no current that flows through this inductor during this interval when the switch is conducting. This

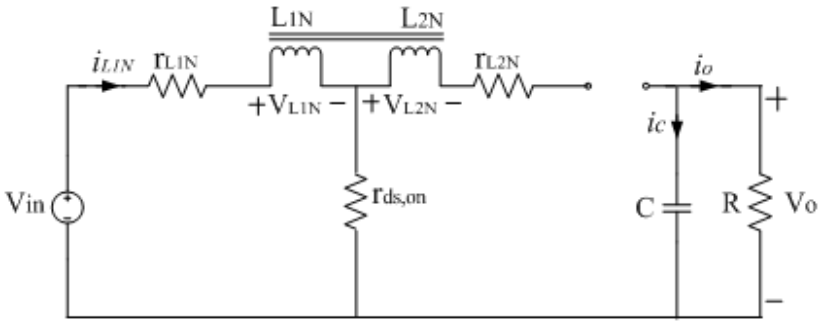

Figure 3.2: Tapped-coupled inductor equivalent circuit when the active switch is conducting

voltage is given by,

$$V_{L2N} = M\frac{di_{L1N}}{dt} = nk \times (V_{in} - i_{L1N}r_{L1N} - i_{L1N}r_{ds,on}) \tag{3.9}$$

where $M = nkL_{1N}$ is the mutual inductance and k is the coupling coefficient.

The total voltage across the two tapped-coupled inductors is given by:

$$V_L = V_{L1N} + V_{L2N} = (1 + nk) \times V_{L1N} \tag{3.10}$$

In addition, the expression for capacitor current during this interval is obtained as,

$$i_c = C\frac{dv_o}{dt} = -\frac{V_o}{R} \tag{3.11}$$

b) **Diode is conducting** ($\delta T_s < t < T_s$)

When the switch, S_{1N} is off, the diode is forward biased and hence it conducts. Figure 3.3 shows the equivalent circuit of the converter during this interval.

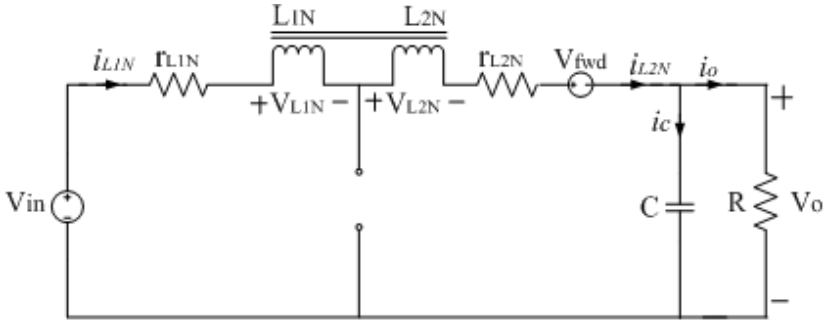

Figure 3.3: Tapped-coupled inductor equivalent circuit when the diode is conducting

The same current goes through the two coupled inductors. The energy stored in the inductors and from the input source voltage, is supplied to the output through the conducting diode. The expression of voltage across the input-side inductor, L_{1N}, is obtained as,

$$V_{L1N} = L_{1N}\frac{di_{L1N}}{dt} = \frac{1}{1+nk} \times (V_{in} - V_o - i_{L1N}(r_{L1N} + r_{L2N}) - V_{fwd}) \tag{3.12}$$

Similarly, the voltage across the output-side inductor, V_{L2N}, is given by

$$V_{L2N} = L_{2N}\frac{di_{L2N}}{dt} = \frac{nk}{1+nk} \times (V_{in} - V_o - i_{L1N}(r_{L1N} + r_{L2N}) - V_{fwd}) \tag{3.13}$$

The total voltage across the coupled inductors is obtained as,

$$V_L = V_{L1N} + V_{L2N} = (1+nk) \times V_{L1N} \tag{3.14}$$

The expression for current through the output capacitor during this interval is given as,

$$i_c = C\frac{dv_o}{dt} = i_{L1N} - \frac{V_o}{R} \tag{3.15}$$

In steady-state, the average voltage across the two coupled inductors over one switching period should be equal to zero. Hence,

$$< V_{LN} >= 0 = D \times (1+nk) \times (V_{in} - i_{L1N}r_{L1N} - i_{L1N}r_{ds,on}) + (1-D) \times (V_{in} - V_o - i_{L1N}(r_{L1N} + r_{L2N}) - V_{fwd}) \tag{3.16}$$

Similarly, the average capacitor current in one switching period is given by,

$$i_c = C\frac{dv_o}{dt} = -\frac{V_o}{R} + (1-D) \times i_{L1N} \tag{3.17}$$

The averaged equations are perturbed and separated into AC- and DC-terms. The DC-terms are then rearranged and simplified to yield expressions for nominal duty ratio.

$$D = \frac{(V_o - V_{in} + V_{fwd}) + I_{L1N}r_{eq,1}}{nkV_{in} + V_o + V_{fwd} - I_{L1N}r_{ds,on}(1+nk) - I_{L1N}r_{eq,1}(1+k+nk)} \tag{3.18}$$

where $r_{eq,1} = r_{L1N} + r_{L2N}$

The voltage transfer ratio is obtained by ignoring the parasitic components in the equation (3.18) as

$$\frac{V_o}{V_{in}} = \frac{(1+nkD)}{(1-D)} \tag{3.19}$$

From above equation, it is seen that the voltage transfer ratio of the tapped-coupled inductor boost converter depends on:

- Duty ratio, D
- Turns ratio,n
- Coupling coefficient,k

Consequently, the converter can be applied to a source with a wide-input voltage range to produce a constant output voltage by varying only the duty cycle while keeping other parameters constant. When n is equal to zero, the voltage transfer ratio, given in equation (3.19), can be reduced to that of a conventional boost converter as shown,

$$\frac{V_o}{V_{in}} = \frac{1}{(1-D)} \tag{3.20}$$

3.2.3.2 RMS voltage and current derivations

In this section, the expressions for converter input, inductor, capacitor, switch and diode rms current and voltage, are derived in order to determine the performance characteristics of the converter. The key waveforms, shown in figure 3.4, are utilised for the purpose of this exercise [35].

The input-side inductor voltage ,V_{L1N},during the switch on-state is given by,

$$V_{L1N} = \{V_{in} - i_{L1N}r_{L1N} - 2i_{L1N}r_{ds,on}\} \tag{3.21}$$

Similarly, the output-side inductor voltage, V_{L2N}, during the switch on-state is given by,

$$V_{L2N} = nk \times \{V_{in} - i_{L1N}r_{L1N} - 2i_{L1N}r_{ds,on}\} \tag{3.22}$$

The input-side inductor voltage during the switch-off state is given by

$$V_{L1N} = (\frac{1}{1+nk}) \times \{V_{in} - V_o - V_{fwd} - i_{L1N}r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\} \tag{3.23}$$

Similarly, the output-side inductor voltage during the switch-off state is given by

$$V_{L2N} = \frac{nk}{(1+nk)} \times \{V_o V_{fwd} i_{L1N}r_{ds,on} i_{L1N}(r_{L1N} + r_{L2N})\} \tag{3.24}$$

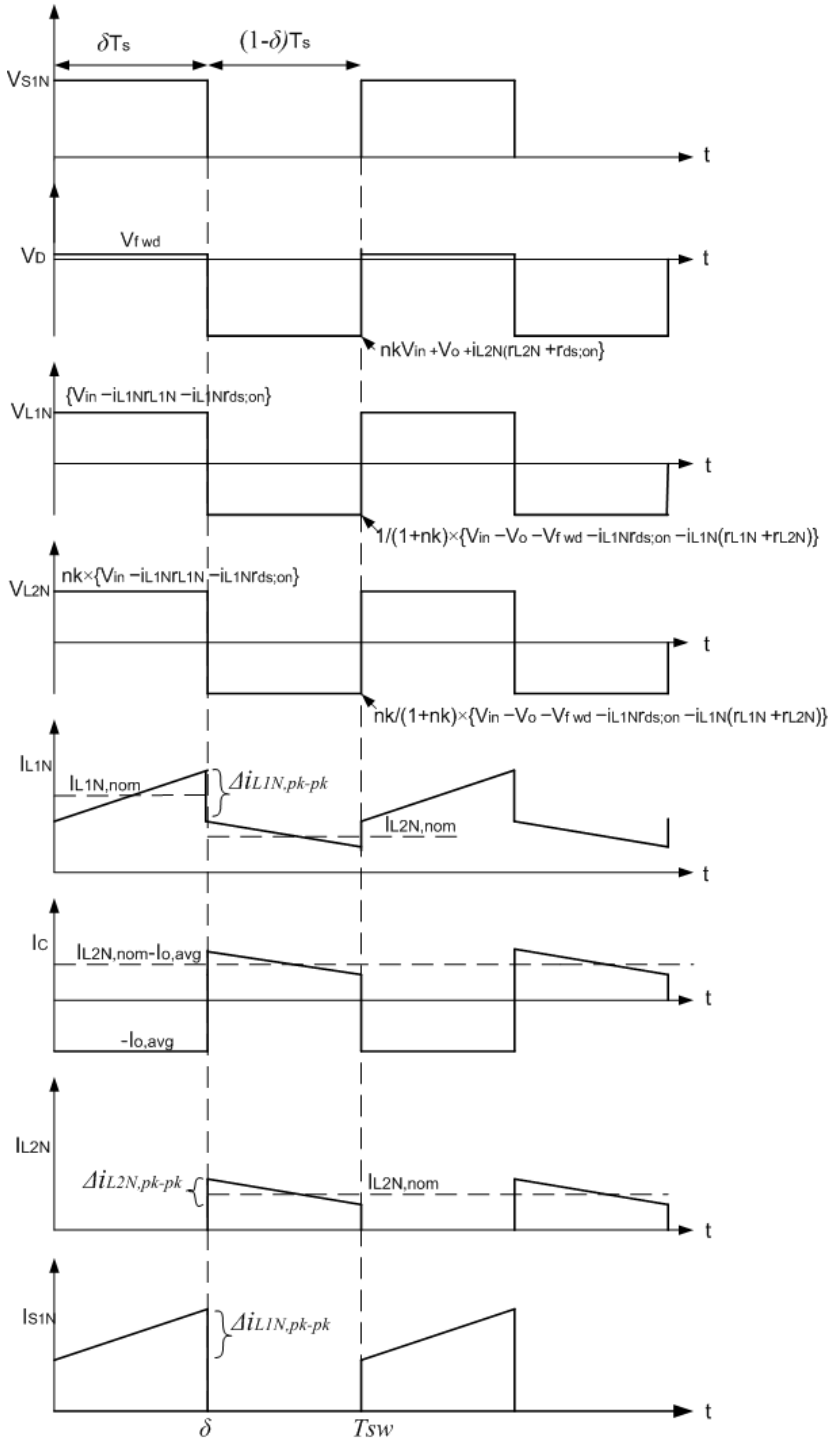

Figure 3.4: Current and voltage waveforms for the SWECS

The switch blocking voltage during its off-state is given by

$$V_s = \frac{nk\{V_{in} - i_{L1N}(r_{L1N} + r_{ds,on})\} + V_o + V_{fwd} + i_{L2N}r_{L2N}}{(1+nk)} \tag{3.25}$$

The voltage stress across the diode is given by

$$V_D = nkV_{in} + V_o + i_{L2N}(r_{L2N} + r_{ds,on}) \tag{3.26}$$

The expressions for average and nominal value of input current and output-side inductor current is obtained as,

$$I_{in,avg} = I_{L1N,avg} = I_{L1N,nom}D_2 + I_{L2N,nom}(1 - D_2) = \frac{1 + nkD}{1 - D} \times I_{o,avg} \tag{3.27}$$

But,

$$I_{L1N,nom} = (\frac{1 + nk}{1 - D}) \times I_{o,avg} \tag{3.28}$$

Hence,

$$I_{L2N,nom} = \frac{I_{o,avg}}{1 - D} \tag{3.29}$$

The current stress on the switch, S_{1N}, is given by

$$I_{s1N} = I_{in,avg} = \frac{1 + nkD}{1 - D} \times I_{o,avg} \tag{3.30}$$

The expression for current stress on the diode is obtained as

$$I_D = \frac{(1)}{(2(1 - D)} \times I_o \tag{3.31}$$

From equations (3.8) and (3.13), the expressions for inductor current ripple are obtained as

$$\Delta i_{L1N,pk-pk} = \frac{\{V_{in} - i_{L1N}r_{ds,on} - i_{L1N}r_{L1N}\}DT_{sw}}{L_{1N}} \tag{3.32}$$

$$\Delta i_{L2N,pk-pk} = \frac{nk\{V_{in} - V_o - i_{L1N}(r_{L1N} + r_{L2N}) - V_{fwd}\}(1 - D)T_{sw}}{(1 + nk)L_{2N}} \tag{3.33}$$

The expressions for input and output RMS current in a bidirectional tapped-coupled inductor operating in boost-mode are obtained from Figure 3.4 as,

$$I_{L1N,rms} = \sqrt{\{(I_{L1N,nom})^2 D[1 + \frac{1}{3}(\frac{\Delta i_{L1N,pk-pk}}{2I_{L1N,nom}})^2] + (I_{L2N,nom})^2(1 - D)[1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2I_{L2N,nom}})^2]\}} \tag{3.34}$$

$$I_{L2N,rms} = \frac{1 - D}{1 + nkD} \times I_{L1N,rms} \tag{3.35}$$

Similarly, the expressions for output diode RMS current and capacitor current are obtained as

$$I_{D,rms} = \sqrt{\{(I_{L2N,nom})^2(1 - D)[1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2I_{L2N,nom}})^2]\}} \tag{3.36}$$

$$I_{c,rms} = \sqrt{\{(I_{o,avg})^2 D + (D \times I_{L2N,nom})^2(1 - D) \times [1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2D \times I_{L2N,nom}})^2]\}} \tag{3.37}$$

The peak inductor currents are given by the following expression

$$\hat{I}_{L1N} = I_{L1N,nom} + \frac{1}{2}\Delta i_{L1N,pk-pk} \tag{3.38}$$

$$\hat{I}_{L2N} = I_{L2N,nom} + \frac{1}{2}\Delta i_{L2N,pk-pk} \tag{3.39}$$

3.2.3.3 Small signal analysis of the single-phase tapped-inductor boost converter

The small signal AC terms are obtained by adding signal variations to the averaged equations (3.16) and (3.17) while ignoring the steady-state DC terms. The second order non-linear variations are assumed to be very small and are neglected in this derivations.

$$\begin{aligned} L_{1N}\frac{d\hat{i}_{L1N}}{dt} =& D\times[(1+nk)(\hat{v}_{in}-\hat{i}_{L1N}r_{L1N}-\hat{i}_{L1N}r_{ds,on})-\hat{v}_{in}+\hat{v}_o+\hat{v}_{fwd}+\hat{i}_{L1N}(r_{L1N}+r_{L2N})] \\ &+\hat{d}[(1+nk)(V_{in}-I_{L1N}r_{L1N}-I_{L1N}r_{ds,on})-V_{in}+V_o+V_{fwd}+I_{L1N}(r_{L1N}+r_{L2N})] \\ &+[\hat{v}_{in}-\hat{v}_o-\hat{v}_{fwd}-\hat{i}_{L1N}(r_{L1N}+r_{L2N})] \end{aligned} \tag{3.40}$$

$$C\frac{d\hat{v}_o}{dt} = -\frac{\hat{v}_o}{R} + \hat{i}_{L1N}(1-D) - \hat{d}I_{L1N} \tag{3.41}$$

where the symbol $\hat{}$ represent signal variations.

In order to obtain the small signal transfer functions to facilitate the modelling of the circuit control system, the Laplace transforms of above equations are obtained.

$$\begin{aligned} s\hat{L}i_{L1N}(s) =& D\times[(1+nk)(\hat{v}_{in}(s)-\hat{i}_{L1N}(s)(r_{L1N}+r_{ds,on}))-(\hat{v}_{in}(s)-\hat{v}_o(s)-\hat{v}_{fwd}(s)] \\ &-D\times[\hat{i}_{L1N}(s)(r_{L1N}+r_{L2N}))]+\hat{d}(s)\times(1+nk)(V_{in}-I_{L1N}r_{L1N}-I_{L1N}r_{ds,on}) \\ &-\hat{d}(s)\times[V_{in}-V_o-V_{fwd}-I_{L1N}(r_{L1N}+r_{L2N})]+[\hat{v}_{in}(s)-\hat{v}_o(s)-\hat{v}_{fwd}(s)] \\ &-[\hat{i}_{L1N}(s)(r_{L1N}+r_{L2N})] \end{aligned} \tag{3.42}$$

$$sC\hat{v}_o(s) = -\frac{\hat{v}_o(s)}{R} + \hat{i}_{L1N}(s)(1-D) - \hat{d}(s)I_{L1N} \tag{3.43}$$

The open loop transfer functions are obtained from equations (3.42) and (3.43) as,

$$G_1 = \frac{\hat{v}_o(s)}{\hat{v}_{in}(s)}\Big|_{\hat{d}(s)=0} = \frac{R(1-D)(1+nkD)}{s^2L_{1N}CR + s(CRr_{eq}+L_{1N}) + R(1-D)^2 + r_{eq}} \tag{3.44}$$

$$G_2 = \frac{\hat{v}_o(s)}{\hat{d}(s)}|_{\hat{v}_{in}(s)=0} = \frac{-sL_{1N}RI_{L1N} + R(1-D)\{nk[V_{in} - I_{L1N}(r_{L1N} + r_{ds}] + V_o + V_{fwd} + I_{L1N}(r_{L2N} - r_{ds})\} - I_{L1N}Rr_{eq}}{s^2L_{1N}CR + s(CRr_{eq} + L_{1N}) + R(1-D)^2 + r_{eq}} \tag{3.45}$$

$$G_3 = \frac{\hat{i}_{L1N}(s)}{\hat{v}_{in}(s)}|_{\hat{d}(s)=0} = \frac{(sCR+1)(1+nkD)}{s^2L_{1N}CR + s(CRr_{eq} + L_{1N}) + R(1-D)^2 + r_{eq}} \tag{3.46}$$

$$G_4 = \frac{\hat{i}_{L1N}(s)}{\hat{d}(s)}|_{\hat{v}_{in}(s)=0} = \frac{(sCR+1)\{nk[V_{in} - I_{L1N}(r_{L1N} + r_{ds}] + V_o + V_{fwd} + I_{L1N}(r_{L2N} - r_{ds})\} - R(1-D)I_{L1N}}{s^2L_{1N}CR + s(CRr_{eq} + L_{1N}) + R(1-D)^2 + r_{eq}} \tag{3.47}$$

where $r_{eq} = nkD(r_{L1N} + r_{ds,on}) + (D + nkD)(r_{ds,on} - r_{L2N})$

3.3 LOW VOLTAGE BATTERY INTERFACE ANALYSIS

This section presents the performance analysis of a low voltage battery interface. The proposed interface consists of a two-phase bidirectional tapped-coupled inductor boost DC-DC converter. Analysis is done for non-ideal characteristics and with the converter operating in the continuous conduction mode (CCM). Derivation of the converter small-signal transfer functions are also presented and will later be used to model the system control.

3.3.1 Topology of the proposed battery interface

The proposed low voltage battery interface consists of MOSFETs, S_{1N} and S_{2N}, two sets of coupled inductor, L_{1N} and L_{2N}, input- and output-side filter capacitor, C_{in} and C_o and a load resistor R. r_{L1N} and r_{L2N} are input- and output-side inductor resistance respectively while $r_{ds;on}$ is the MOSFETs channel resistance. Pulse Width Modulation (PWM) is used to drive the active switches by varying the gate pulse to obtain the desired duty ratio. The gate signal controlling S_{1N} leads the gate signal for S_{2N} by 180° respectively. Dynamic analysis and component sizing is carried out by considering only one phase of the converter since all the phases are identical. The relationship between L_{1N} and L_{2N} is determined by the turn ratio of the magnetic element,

$$\frac{L_{2N}}{L_{1N}} = (\frac{N_{2N}}{N_{1N}})^2 = n^2 \tag{3.48}$$

where N_{1N} is the number of turns in the first inductor, L_{1N}, and N_{2N} is the number of turns in the second coupled inductor, L_{2N}.

3.3.1.1 Low voltage battery interface operation

The battery interface can operate in either buck- or boost-mode. Boost-mode operation represent the flow of current from the battery voltage source to the DC distribution bus. Buck-mode operation represent the flow of current from the DC distribution bus to charge the battery.

Buck-mode operation

a) **On state** ($0 \le t < \delta_2 T_s$)

The active switch, S_{2N} is turned on while S_{1N} is turned off. The tapped-coupled inductors, L_{1N} and L_{2N}, get charged. Figure 3.5 illustrate the equivalent circuit of the converter during this interval. The same current goes through the coupled inductors. The total voltage across the

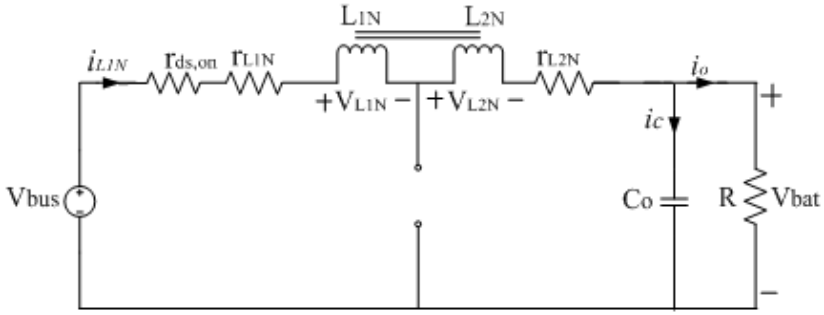

Figure 3.5: Converter operation during buck-mode on-state operation

coupled-inductors is given by,

$$V_L = V_{L1N} + V_{L2N} = V_{bus} - V_{bat} - i_{L1N} r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N}) \tag{3.49}$$

For a buck converter, the voltage ratio is given by

$$n = \frac{V_L}{V_{L2N}} = \frac{V_{L1N} + V_{L2N}}{V_{L2N}} = 1 + \frac{V_{L1N}}{V_{L2N}} \tag{3.50}$$

where n is the turns ratio .

From equation (3.49), the voltage across the output-side inductor can be expressed as,

$$V_{L2N} = L_{2N}\frac{di_{L2N}}{dt} = (\frac{1}{n}) \times \{V_{bus} - V_{bat} - i_{L1N}r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\} \quad (3.51)$$

Similarly, the output capacitor current can be expressed as

$$i_c = C_o\frac{dv_c}{dt} = i_{L1N} - \frac{V_{bat}}{R} \quad (3.52)$$

b) **Off state** ($\delta_2 T_s \le t \le T_s$)

Active switch, S_{2N}, is turned off while S_{1N} is turned on during this state. Figure 3.6 illustrate the equivalent circuit of the converter during this operation. The expression for voltage across the

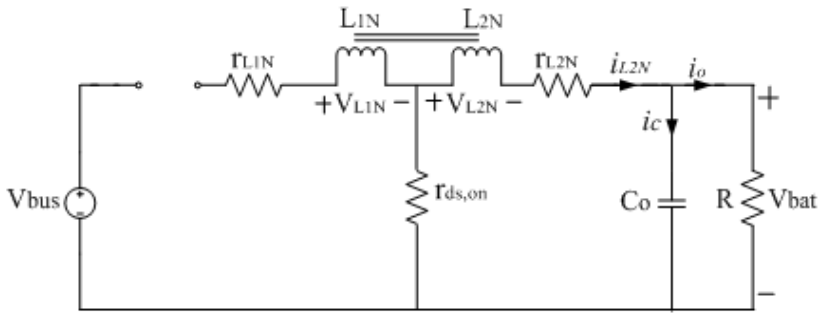

Figure 3.6: Converter operation during buck-mode off-state operation

output-side inductor is obtained as

$$V_{L2N} = L_{2N}\frac{di_{L2N}}{dt} = -\{V_{bat} + i_{L2N}(r_{ds,on} + r_{L2N})\} \quad (3.53)$$

No current flows in the primary-side inductor although, a voltage, V_{L1N} appears across it due to the coupling. This voltage is obtained as,

$$V_{L1N} = M\frac{di_{L2N}}{dt} = (1-nk)L_{2N}\frac{di_{L2N}}{dt} = (1-nk)\{V_{bat} + i_{L2N}(r_{ds,on} + r_{L2N})\} \quad (3.54)$$

Similarly, the expression for capacitor current is obtained as

$$i_c = C_o\frac{dV_c}{dt} = i_{L2N} - \frac{V_{bat}}{R} \quad (3.55)$$

Boost-mode operation

In boost-mode operation S_{1N} operates complimentary to S_{2N}.

a) **On state** ($0 \le t < \delta_1 T_s$)

The active switch, S_{1N}, is turned on while the switch, S_{2N} is turned off. The tapped-coupled inductor get charged. Figure 3.7 illustrate the equivalent circuit of the converter during this state.

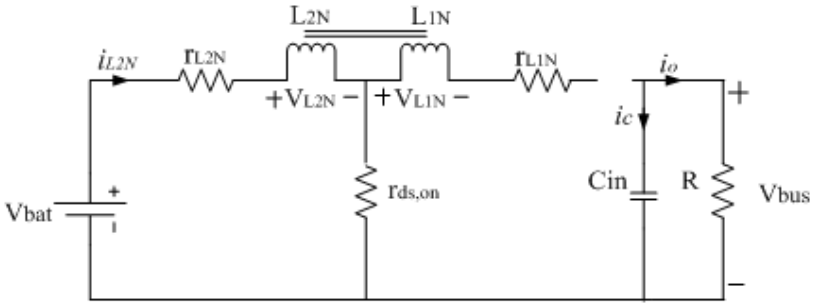

Figure 3.7: Converter operation during boost-mode on-state operation

The voltage measured across the input-side inductor, L_{2N} is given by

$$V_{L2N} = L_{2N}\frac{di_{L2N}}{dt} = \{V_{bat} - i_{L2N}r_{L2N} - i_{L2N}r_{ds,on}\} \tag{3.56}$$

Due to magnetic coupling, a voltage is induced on the output-side inductor, L_{1N}, even though there is no current that flows through this inductor during this interval. This voltage is given by,

$$V_{L1N} = M\frac{di_{L2N}}{dt} = nkL_{2N}\frac{di_{L2N}}{dt} = nk \times \{V_{bat} - i_{L2N}r_{L2N} - i_{L2N}r_{ds,on}\} \tag{3.57}$$

where $M = nk$ is the mutual inductance.

Similarly, the expression for capacitor current during this interval is obtained as

$$i_c = C_{in}\frac{dv_c}{dt} = -\frac{V_{bus}}{R} \tag{3.58}$$

b) **Off state** ($\delta_1 T_s \le t \le T_s$)

The switch S_{2N} is turned on while S_{1N} is turned off. The coupled inductors L_{2N} and L_{1N} conduct current and hence discharge their stored energy to the output. The equivalent circuit of the converter during this operation is shown in figure 3.8.

$$V_L = V_{L1N} + V_{L2N} = V_{bat} - V_{bus} - i_{L2N}r_{ds,on} - i_{L2N}(r_{L2N} + r_{L1N}) \tag{3.59}$$

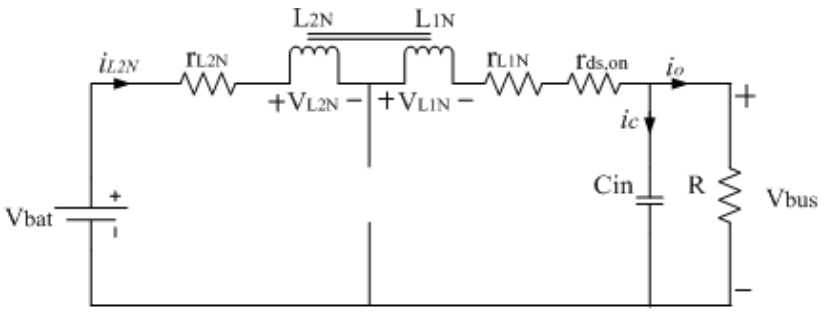

Figure 3.8: Converter operation during boost-mode off-state operation

For a boost converter, the turns ratio is defined as

$$n = \frac{V_{L1N}}{V_{L2N}} \tag{3.60}$$

Hence, the primary-side inductor voltage can be expressed as

$$V_{L2N} = L_{2N}\frac{di_{L2N}}{dt} = \left(\frac{1}{1+n}\right) \times \{V_{bat} - V_{bus} - i_{L2N}r_{ds,on} - i_{L2N}(r_{L2N} + r_{L1N})\} \tag{3.61}$$

Similarly, the expression for capacitor current during this interval is obtained as

$$i_c = C_{in}\frac{dv_c}{dt} = i_{L2N} - \frac{V_{bus}}{R} \tag{3.62}$$

3.3.1.2 Steady state analysis

In steady-state the average voltage across the coupled inductors and the average current through the output capacitor over one switching period should be equal to zero.

Buck-mode operation

The average secondary-side inductor voltage when the converter is operating in buck-mode is given by

$$\begin{aligned} < V_{LN} >= 0 = & D_2 \times \left(\frac{1}{nk}\right) \times \{V_{bus} - V_{bat} - i_{L1N}r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\} + \\ & (1 - D_2) \times -\{V_{bat} + i_{L2N}r_{ds,on} + i_{L2N}r_{L2N}\} \end{aligned} \tag{3.63}$$

Similarly, the average capacitor current in one switching period is given by

$$< I_c >= 0 = D_2 \times (I_{L1N} - I_{L2N}) + I_{L2N} - \frac{V_{bat}}{R} \tag{3.64}$$

The DC voltage transfer function when the converter is operating in buck-mode, ignoring the parasitic components, can be obtained from equation (3.63) as

$$\frac{V_{bat}}{V_{bus}} = \frac{D_2}{D_2 + nk(1 - D_2)} \tag{3.65}$$

Boost-mode operation

The average inductor voltage when the converter is operating in boost-mode is given by

$$\begin{aligned} < V_{LN} >= 0 = & D_1 \times \{V_{bat} - i_{L1N} r_{L1N} - i_{L1N} r_{ds,on}\} + (1 - D_1) \\ & (\frac{1}{1+nk}) \times \{V_{bat} - V_{bus} - i_{L1N} r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\} \end{aligned} \tag{3.66}$$

Similarly, the average capacitor current in one switching period is given by

$$< I_c >= 0 = (1 - D_1) \times I_{L1N} - \frac{V_{bus}}{R} \tag{3.67}$$

The DC voltage transfer function when the converter is operating in boost-mode, ignoring the parasitic components, can be obtained from equation (3.66) as

$$\frac{V_{bus}}{V_{bat}} = \frac{1 + nkD_1}{1 - D_1} \tag{3.68}$$

3.3.1.3 Voltage gain of a low voltage battery interface

It is observed from equation (3.63) and (3.66) that voltage gain of a low voltage battery interface depends on turns ratio, duty-cycle and coupling coefficient.

3.3.1.4 RMS voltage and current derivations

In this section, the expressions for rms input current and voltage, rms inductor current and voltage, rms output capacitor current and voltage are derived in order to determine the performance characteristics of the converter while operating in both buck and boost mode. The key waveforms, shown in figure 3.9 and 3.10, are utilised for the purpose of this exercise.

Buck-mode

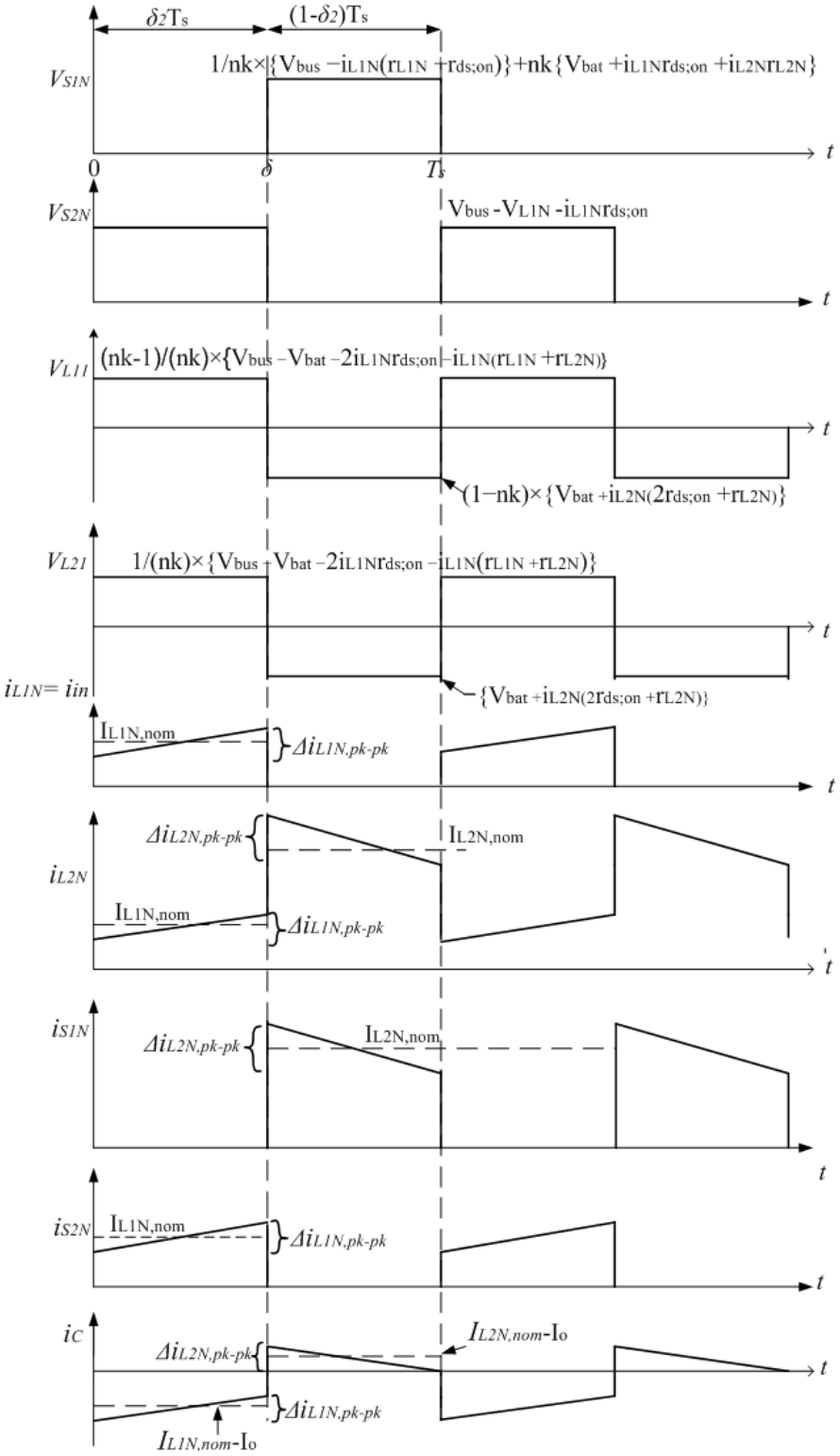

Figure 3.9: Voltage and current waveforms for the low voltage battery interface operating in buck-mode

The inductor voltage , V_{L1N}, during the on-state is given by

$$V_{L1N} = \frac{nk-1}{(nk)} \times \{V_{bus} - V_{bat} - i_{L1N} r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\} \tag{3.69}$$

Similarly, the inductor voltage, V_{L2N}, during the charging state is given by

$$V_{L2N} = \frac{1}{(nk)} \times \{V_{bus} - V_{bat} - i_{L1N} r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\} \tag{3.70}$$

The inductor voltage, V_{L1N}, during the off-state is given by

$$V_{L1N} = (1-nk) \times \{V_{bat} + i_{L2N}(r_{ds;on} + r_{L2N})\} \tag{3.71}$$

Similarly, the inductor voltage, V_{L2N}, during the off-state is given by

$$V_{L2N} = -\{V_{bat} + i_{L2N}(r_{ds;on} + r_{L2N})\} \tag{3.72}$$

The blocking voltage of switch S_{1N}, is given by

$$V_{s1N} = V_{L2N} + i_{L2N} r_{L2N} + i_{L2N} r_{ds;on} + V_{bat} \tag{3.73}$$

However, from equation (3.51),

$$V_{L2N} = (\frac{1}{n})\{V_{bus} - V_{bat} - i_{L1N} r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\} \tag{3.74}$$

Therefore,

$$V_{s1N} = \frac{\{V_{bus} - i_{L1N}(r_{L1N} + r_{ds,on})\} + n\{V_{bat} + i_{L1N} r_{ds,on} + i_{L2N} r_{L2N}\}}{(n)} \tag{3.75}$$

Similarly, the blocking voltage of switch S_{2N} is given by,

$$V_{s2N} = V_{bus} - V_{L1N} - i_{L1N} r_{ds,on} \tag{3.76}$$

From equation (3.54), this blocking voltage can be re-expressed as,

$$V_{s2N} = V_{bus} - i_{L1N} r_{ds,on} - (1-nk)\{V_{bat} + i_{L2N}(r_{ds,on} + r_{L2N})\} \tag{3.77}$$

Considering the voltage transfer ratio obtained in equation (3.65), the average input and output current is obtained as

$$I_{in,avg} = D_2 I_{L1N,nom} = \frac{D_2}{D_2 + nk(1-D_2)} \times I_o, avg \tag{3.78}$$

$$I_{o,avg} = I_{L2N,avg} = I_{L1N,nom} D_2 + I_{L2N,nom}(1-D_2) \tag{3.79}$$

From equations (3.78) and (3.79) the expressions for $I_{L1N,nom}$ and $I_{L2N,nom}$ are obtained as

$$I_{L1N,nom} = \frac{I_o, avg}{D_2 + nk(1-D_2)} \tag{3.80}$$

$$I_{L2N,nom} = \frac{nk}{D_2 + nk(1-D_2)} \times I_{o,avg} \tag{3.81}$$

The average currents through switch, S_{1N} and S_{2N}, are given by,

$$I_{sN,avg} = (1-D_2) \times I_{L2N,nom} = \frac{nk(1-D_2)}{D_2 + nk(1-D_2)} \times I_{o,avg} \tag{3.82}$$

$$I_{sN,avg} = D_2 \times I_{L1N,nom} = \frac{D_2}{D_2 + nk(1-D_2)} \times I_o \tag{3.83}$$

It can be noted that the switching current of S_{2N} is much smaller compared with that of a conventional buck converter. Hence there is reduced switching losses.

From equations (3.49) and (3.51), the expressions for inductor current ripple are obtained as

$$\Delta i_{L1N,pk-pk} = \frac{(nk-1)\{V_{bus} - V_{bat} - i_{L1N} r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\} D_2 T_{sw}}{(nk) L_{1N}} \tag{3.84}$$

$$\Delta i_{L2N,pk-pk} = \frac{\{V_{bus} - V_{bat} - i_{L1N} r_{ds,on} - i_{L1N}(r_{L1N} + r_{L2N})\} D_2 T_{sw}}{nk L_{2N}} \tag{3.85}$$

The expression for input and output RMS current are obtained from figure 3.9 as

$$I_{L2N,rms} = \sqrt{\{(I_{L1N,nom})^2 D_2 [1 + \frac{1}{3}(\frac{\Delta i_{L1N,pk-pk}}{2I_{L1N,nom}})^2] + (I_{L2N,nom})^2 (1-D_2)[1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2I_{L2N,nom}})^2]\}} \tag{3.86}$$

$$I_{L1N,rms} = I_{in,rms} = \sqrt{\{(I_{L1N,nom})^2 D_2 [1 + \frac{1}{3}(\frac{\Delta i_{L1N,pk-pk}}{2I_{L1N,nom}})^2]\}} \tag{3.87}$$

Similarly, the expression for RMS capacitor current is obtained as

$$I_{C_o,rms} = \sqrt{(I_{L1N,nom} - I_o)^2 D_2 [1 + \frac{1}{3}(\frac{\Delta i_{L1N,pk-pk}}{2(I_{L1N,nom} - I_o)})^2] + (I_{L2N,nom} - I_o)^2 (1-D_2)[1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2(I_{L2N,nom} - I_o)})^2]} \tag{3.88}$$

The expressions for RMS switch current are given by,

$$I_{sN,rms} = \sqrt{\{(I_{L2N,nom})^2 \times (1-D_2)[1+\frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2I_{L2N,nom}})^2]\}} \tag{3.89}$$

$$I_{sN,rms} = \sqrt{\{(I_{L1N,nom})^2 \times D_2[1+\frac{1}{3}(\frac{\Delta i_{L1N,pk-pk}}{2I_{L1N,nom}})^2]\}} \tag{3.90}$$

The peak inductor currents are given by the following expressions

$$\hat{I}_{L1N} = I_{L1N,nom} + \frac{1}{2}\Delta i_{L1N,pk-pk} \tag{3.91}$$

$$\hat{I}_{L2N} = I_{L2N,nom} + \frac{1}{2}\Delta i_{L2N,pk-pk} \tag{3.92}$$

Boost mode

The inductor voltage ,V_{L1N}, during the switch on-state is given by

$$V_{L1N} = nk \times \{V_{bat} - i_{L2N}r_{L2N} - i_{L2N}r_{ds,on}\} \tag{3.93}$$

Similarly, the inductor voltage ,V_{L2N}, during the switch on-state is given by

$$V_{L2N} = \{V_{bat} - i_{L2N}r_{L2N} - i_{L2N}r_{ds,on}\} \tag{3.94}$$

The inductor voltage, V_{L1N}, during the switch off-state is given by

$$V_{L1N} = (\frac{nk}{1+nk}) \times \{V_{bat} - V_{bus} - i_{L2N}r_{ds,on} - i_{L2N}(r_{L1N}+r_{L2N})\} \tag{3.95}$$

Similarly, the inductor voltage, V_{L2N}, during the switch off-state is given by

$$V_{L2N} = \frac{1}{(1+nk)} \times \{V_{bat} - V_{bus} - i_{L2N}r_{ds,on} - i_{L2N}(r_{L1N}+r_{L2N})\} \tag{3.96}$$

The voltage stress on switch, S_{1N}, is given by,

$$V_{sN} = \frac{\{V_{bus} + i_{L2N}(r_{L1N}+r_{ds,on})\} + nk\{V_{bat} - i_{L2N}r_{ds,on}\}}{(1+nk)} \tag{3.97}$$

The Voltage stress across switch S_{2N} is given by,

$$V_{sN} = V_{bus} + i_{L1N}r_{ds,on} + i_{L1N}r_{L1N} + nk\{V_{bat} - i_{L2N}(r_{L2N}+r_{ds,on})\} \tag{3.98}$$

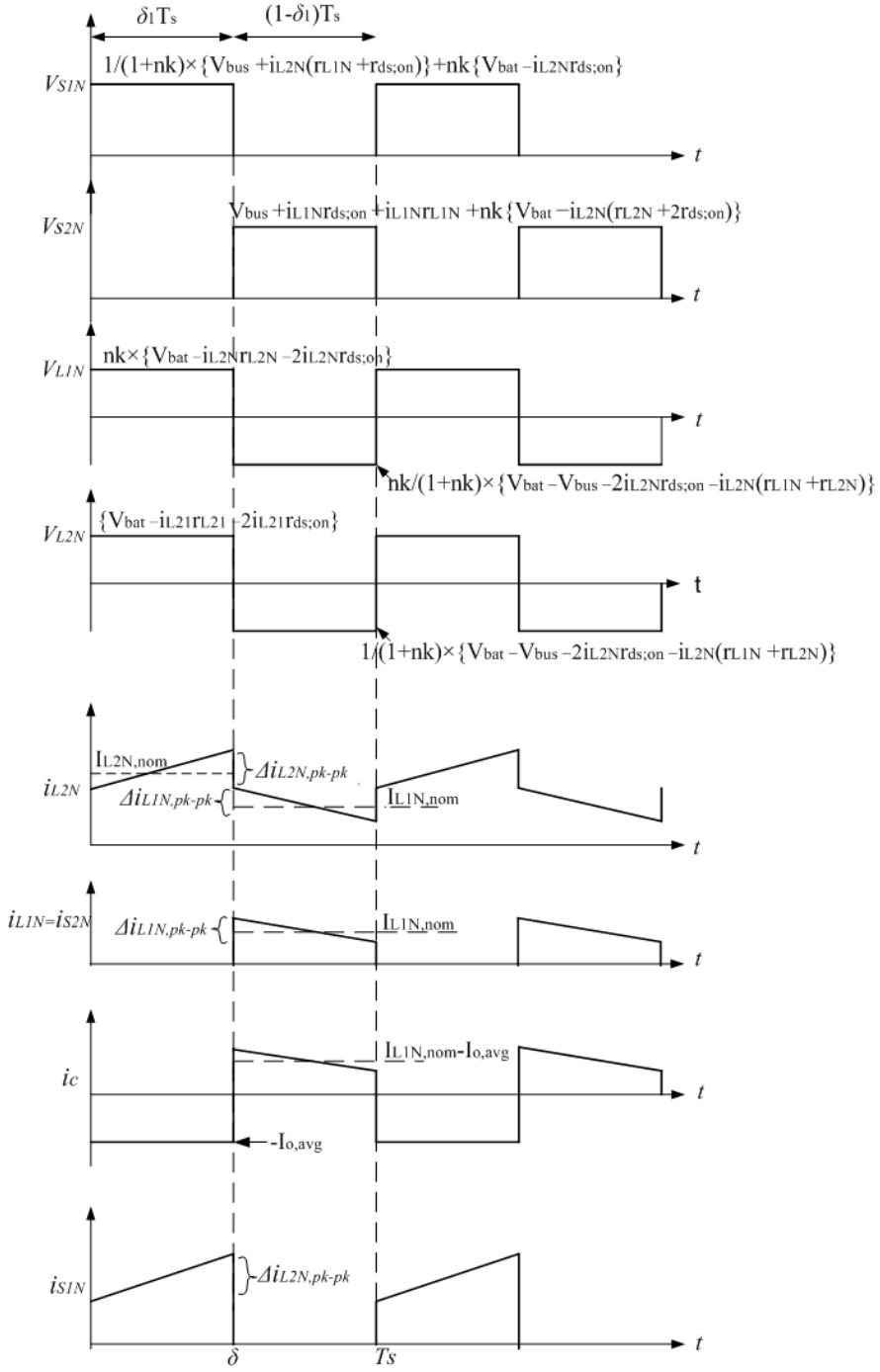

Figure 3.10: Voltage and current waveforms for a low voltage battery interface operating in boost-mode

The expressions for average and nominal value of input current and output-side inductor current are obtained from figure 3.10 as

$$I_{in,avg} = I_{L2N,avg} = I_{L2N,nom}D_1 + I_{L1N,nom}(1-D_1) = \frac{1+nkD_1}{1-D_1} \times I_{o,avg} \tag{3.99}$$

where,

$$I_{L2N,nom} = \left(\frac{1+nk}{1-D_1}\right) \times I_{o,avg} \tag{3.100}$$

and,

$$I_{L1N,nom} = \frac{I_{o,avg}}{1-D_1} \tag{3.101}$$

The average values of current through , S_{1N}, and S_{2N} are given by

$$I_{sN,avg} = \frac{D_1(1+nk)}{1-D_1} \times I_{o,avg} \tag{3.102}$$

$$I_{sN,avg} = I_{o,avg} \tag{3.103}$$

From equations (3.56) and (3.61), the expressions for inductor current ripple are obtained as

$$\Delta i_{L1N,pk-pk} = \frac{nk \times \{V_{bat} - i_{L2N} r_{ds,on} - i_{L2N} r_{L2N}\} D_1 T_{sw}}{L_{1N}} \tag{3.104}$$

$$\Delta i_{L2N,pk-pk} = \frac{nk\{V_{bat} - V_{bus} - i_{L2N} r_{ds,on} - i_{L2N}(r_{L1N} + r_{L2N})\}(1-D_1) T_{sw}}{(1+nk) L_{2N}} \tag{3.105}$$

The expressions for input and output RMS current are obtained as,

$$I_{L2N,rms} = \sqrt{\{(I_{L2N,nom})^2 D_1 [1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2I_{L2N,nom}})^2] + (I_{L1N,nom})^2 (1-D_1)[1 + \frac{1}{3}(\frac{\Delta i_{L1N,pk-pk}}{2I_{L1N,nom}})^2]\}} \tag{3.106}$$

$$I_{L1N,rms} = \sqrt{(\frac{I_{o,avg}}{1-D_1})^2 \times (1-D_1)[1 + \frac{1}{3}(\frac{\Delta i_{L1N,pk-pk}}{2(\frac{I_{o,avg}}{1-D_1})^2}]} \tag{3.107}$$

The expression for RMS capacitor current is obtained as

$$I_{cin,rms} = \sqrt{\{(I_{o,avg})^2 D_1 + (D_1 \times I_{L2N,nom})^2 (1-D_1) \times [1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2D_1 \times I_{L2N,nom}})^2]\}} \tag{3.108}$$

The expressions for RMS switch currents are given by,

$$I_{sN} = \sqrt{\{(I_{L2N,nom})^2 \times D_1 [1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2I_{L2N,nom}})^2]\}} \tag{3.109}$$

$$I_{sN,rms} = I_{L1N,rms} \tag{3.110}$$

The peak inductor currents are given by the following expressions

$$\hat{I}_{L1N} = I_{L1N,nom} + \frac{1}{2}\Delta i_{L1N,pk-pk} \tag{3.111}$$

$$\hat{I}_{L2N} = I_{L2N,nom} + \frac{1}{2}\Delta i_{L2N,pk-pk} \tag{3.112}$$

3.3.1.5 Small signal analysis of the low voltage battery interface

The small signal AC terms are obtained by adding signal variations to the averaged expressions given in (3.63) to (3.66) while ignoring the steady-state DC terms. The second order non-linear variations are assumed to be very small and are also ignored in these derivations.

Buck-mode operation

The small signal AC terms for the converter operating in buck-mode are given by

$$\begin{aligned} L_{2N}\frac{d\hat{i}_{L2N}}{dt} =& \hat{\delta}_2 \times \{\frac{1}{nk}[V_{bus} - V_{bat} - \frac{1}{nk-1}I_{L2N}(r_{ds,on} + r_{L1N} + r_{L2N})] + V_{bat} + I_{L2N}(r_{ds,on} + r_{L2N})\} \\ &+ \hat{v}_{bus} \times (\frac{D_2}{nk}) - \hat{v}_{bat} \times \{\frac{D_2 + nk - nkD_2}{nk}\} - \hat{i}_{L2N} \times \{(\frac{D_2}{nk(nk-1)})[r_{ds,on} + r_{L1N} + r_{L2N}]\} \\ &+ \hat{i}_{L2N} \times \{D_2(r_{ds,on} + r_{L2N}) - (r_{ds,on} + r_{L2N})\} \end{aligned} \tag{3.113}$$

$$C_o\frac{d\hat{v}_{bat}}{dt} = \hat{\delta}_2 \times (\frac{2-nk}{nk-1})I_{L2N} + \hat{i}_{L2N} \times \{D_2(\frac{2-nk}{nk-1}) + 1\} - \frac{\hat{v}_{bat}}{R} \tag{3.114}$$

where the symbol (^) represent signal variations.

In order to obtain the small signal transfer functions to facilitate the modelling of the circuit control system, the Laplace transform of the above equations are obtained.

$$\begin{aligned} sL\hat{i}_{L2N}(s) =& \hat{\delta}_2(s) \times \{\frac{1}{nk}[V_{bus} - V_{bat} - \frac{I_{L2N}}{nk-1}(r_{ds,on} + r_{L1N} + r_{L2N})] + V_{bat} + I_{L2N}(r_{ds,on} + r_{L2N})\} \\ &- \hat{v}_{bat}(s) \times \{\frac{D_2 + nk - nkD_2}{nk}\} + \hat{i}_{L2N}(s) \times \{(\frac{D_2}{nk(nk-1)})[r_{ds,on} + r_{L1N} + r_{L2N}]\} \\ &+ \hat{i}_{L2N}(s) \times \{D_2(r_{ds,on} + r_{L2N}) - (r_{ds,on} + r_{L2N})\} + \hat{v}_{bus}(s) \times (\frac{D_2}{nk}) \end{aligned} \tag{3.115}$$

$$sC_o\hat{v}_{bat}(s) = \hat{\delta}_2(s) \times (\frac{2-nk}{nk-1})I_{L2N} + \hat{i}_{L2N}(s) \times \{D_2(\frac{2-nk}{nk-1}) + 1\} - \frac{\hat{v}_{bat}(s)}{R} \tag{3.116}$$

The converter small-signal transfer function relating input voltage to the output voltage is obtained from equations (3.115) and (3.116) as,

$$\frac{\hat{v}_{bat}(s)}{\hat{v}_{bus}(s)}\Big|_{\hat{\delta}(s)=0} = \frac{D_2R\{D_2+nk(1-D_2)\}}{nk(nk-1)s^2L_{2N}C_oR - s\{C_oRr_{eq} - nk(nk-1)L_{2N}\} + R(D_2+nk-nkD_2)^2 - r_{eq}} \quad (3.117)$$

Similarly, the control-to-output transfer function of the converter is obtained as

$$\frac{\hat{v}_{bat}(s)}{\hat{\delta}(s)} = \frac{nk(nk-1)(2-nk)RI_{L2N}\{sL_{2N}+r_{eq}\} + (D_2+nk(1-D_2))R\{[V_{bus}-V_{bat}-I_{L1N}R_A]+nkV_{bat}+nkI_{L2N}R_B]\}}{nk(nk-1)s^2L_{2N}C_oR - s\{C_oRr_{eq} - nk(nk-1)L_{2N}\} + R(D_2+nk-nkD_2)^2 - r_{eq}} \quad (3.118)$$

The expression that relates the inductor current to input voltage is obtained as

$$\frac{\hat{i}_{L2N}(s)}{\hat{v}_{bus}(s)}\Big|_{\hat{\delta}(s)=0} = \frac{D_2(nk-1)(sC_oR+1)}{nk(nk-1)s^2L_{2N}C_oR - s\{C_oRr_{eq} - nk(nk-1)L_{2N}\} + R(D_2+nk-nkD_2)^2 - r_{eq}} \quad (3.119)$$

The control to inductor current transfer function is given by

$$\frac{\hat{i}_{L2N}(s)}{\hat{\delta}(s)} = \frac{(sC_oR+1)\{(nk-1)[V_{bus}-V_{bat}+nkV_{bat}+nkI_{L2N}(r_{ds,on}+r_{L2N})]-I_{L2N}R_A\} - R\{(D_2+nk(1-D_2))I_{L2N}\}}{nk(nk-1)s^2L_{2N}C_oR - s\{C_oRr_{eq} - nk(nk-1)L_{2N}\} + R(D_2+nk-nkD_2)^2 - r_{eq}} \quad (3.120)$$

where $R_A = r_{ds,on} + r_{L1N} + r_{L2N}$, $R_B = r_{ds,on} + r_{L2N}$, and $r_{eq} = D_2(r_{ds,on} + r_{L1N} + r_{L2N}) + nk(nk-1)\{D_2(r_{ds,on}+r_{L2N}) - r_{ds,on} - r_{L2N}\}$.

Boost-mode operation

The small signal AC terms for the converter operating in boost-mode are obtained as,

$$\begin{aligned} L_{2N}\frac{d\hat{i}_{L2N}}{dt} =& \hat{\delta}\times\{V_{bat} - I_{L2N}(r_{ds,on}+r_{L2N}) + (\frac{1}{1+nk})[V_{bus}-V_{bat}+I_{L2N}(r_{ds,on}+r_{L1N}+r_{L2N})\} \\ & - \hat{v}_{bus}\times(\frac{1-D_1}{1+nk}) + \hat{v}_{bat}\times\{\frac{1+nkD_1}{1+nk}\} - \hat{i}_{L2N}\times\{(\frac{D_1}{1+nk})[r_{ds,on}+r_{L1N}+r_{L2N}]\} \\ & - \hat{i}_{L2N}\times\{D_1(r_{L2N}+r_{ds,on})\} \end{aligned} \quad (3.121)$$

$$C_{in}\frac{d\hat{v}_{bus}}{dt} = \hat{i}_{L2N}\times(1-D_1) - \hat{\delta}I_{L2N} - \frac{\hat{v}_{bus}}{R} \quad (3.122)$$

where the symbol $\hat{(\,)}$ represent signal variations.

In order to obtain the small signal transfer functions to facilitate the modelling of the circuit control system, the Laplace transform of the above equations are obtained as,

$$\begin{aligned} sL\hat{i}_{L2N}(s) =& \hat{\delta}_1(s)\times\{V_{bat}-I_{L2N}(r_{ds,on}+r_{L2N})+(\frac{1}{1+nk})[V_{bus}-V_{bat}+I_{L2N}(r_{ds,on}+r_{L1N}+r_{L2N})\} \\ &-\hat{v}_{bus}(s)\times(\frac{1-D_1}{1+nk})+\hat{v}_{bat}(s)\times\{\frac{1+nkD_1}{1+nk}\}-\hat{i}_{L2N}(s)\times\{(\frac{D_1}{1+nk})[r_{ds,on}+r_{L1N}+r_{L2N}]\} \\ &-\hat{i}_{L2N}(s)\times\{D_1(r_{L2N}+r_{ds,on})\} \end{aligned} \tag{3.123}$$

$$sC_{in}\hat{v}_{bus}(s)=\hat{i}_{L2N}(s)\times(1-D_1)-\hat{\delta}(s)I_{L2N}-\frac{\hat{v}_{bus}(s)}{R} \tag{3.124}$$

The converter small-signal transfer function relating input voltage to the output voltage is obtained from equations (3.123) and (3.124) as,

$$\frac{\hat{v}_{bus}(s)}{\hat{v}_{bat}(s)}|_{\hat{\delta}(s)=0}=\frac{R(1-D_1)\{1+nkD_1\}}{(nk+1)s^2L_{2N}C_{in}R+s\{C_{in}Rr_{eq1}+(nk+1)L_{2N}\}+R(1-D_1)^2+r_{eq1}} \tag{3.125}$$

Similarly, the control-to-output transfer function of the converter is obtained as

$$\frac{\hat{v}_{bus}(s)}{\hat{\delta}(s)}=\frac{R(1-D_1)\{(1+nk)(V_{bat}-I_{L2N}R_Z)+V_{bus}-V_{bat}+I_{L2N}R_Y\}-I_{L2N}Rr_{eq1}-(1+nk)sL_{2N}RI_{L2N}}{(nk+1)s^2L_{2N}C_{in}R+s\{C_{in}Rr_{eq1}+(nk+1)L_{2N}\}+R(1-D_1)^2+r_{eq1}} \tag{3.126}$$

The expression that relates the inductor current to input voltage is given as

$$\frac{\hat{i}_{L2N}(s)}{\hat{v}_{bat}(s)}|_{\hat{\delta}(s)=0}=\frac{(1+nkD_1)(sC_{in}R+1)}{(nk+1)s^2L_{2N}C_{in}R+s\{C_{in}Rr_{eq1}+(nk+1)L_{2N}\}+R(1-D_1)^2+r_{eq1}} \tag{3.127}$$

The control to inductor current transfer function is given by

$$\frac{\hat{i}_{L2N}(s)}{\hat{\delta}(s)}|_{\hat{v}_{bat}(s)=0}=\frac{(sC_{in}R+1)\{(1+nk)(V_{bat}-I_{L2N}R_Z)+V_{bus}-V_{bat}+I_{L2N}R_Y\}+R(1-D_1)I_{L2N}}{(nk+1)s^2L_{2N}C_{in}R+s\{C_{in}Rr_{eq1}+(nk+1)L_{2N}\}+R(1-D_1)^2+r_{eq1}} \tag{3.128}$$

where $R_Y=r_{ds,on}+r_{L1N}+r_{L2N}$, $R_Z=r_{L2N}+r_{ds,on}$ and $r_{eq1}=D_1(r_{ds,on}+r_{L1N}+r_{L2N})+D_1(nk+1)(r_{ds,on}+r_{L2N})$

3.4 CHAPTER CONCLUSION

This chapter has presented theoretical analysis of all the components forming the low voltage DC microgrid system. Analysis was done for a non-ideal conversion system and with the DC-DC converters operating in CCM mode. Current and voltage equations and waveforms were derived and will be used later in this research to size the converter components. Small signal transfer functions were also obtained and will be used in modelling the system control.

CHAPTER 4 SYSTEM CONTROLLER DESIGN

4.1 CHAPTER OVERVIEW

The output voltage of a system is dependent on various factors such as input generator voltage, load current, duty-cycle and converter component parameters. An effective controller is needed to automatically adjust the duty-cycle so that a specified output voltage is obtained with high accuracy, regardless of input disturbances or component tolerances. This chapter presents a detailed analysis of controller design for the proposed low voltage DC microgrid.

4.2 AVERAGE CURRENT MODE CONTROLLER

Average current mode control (ACMC) is employed in this research to control the input current and output DC voltage. This controller offers excellent noise immunity and high degree of accuracy [46], [47]. It consists of an inner current control loop designed with a higher bandwidth and hence faster dynamics compared to the outer voltage control loop. The output voltage of SWECS is regulated by sensing the output voltage and comparing it with a stable reference voltage, V_{ref}. The resultant error is compensated using an appropriate compensator network before feeding it to the inner loop as reference current, I_{ref}. Figure 4.1 illustrates the block diagram of an ACMC. H_c represents the current sensor gain while H_v represent the voltage sensor gain.

The gain-bandwidth characteristic of the current-loop is tailored for optimum performance by the compensation network, G_{ci}, while the outer voltage-loop is enhanced by inclusion of the compensation network, G_{cv}. V_m represents the amplitude of the PWM saw-tooth signal while $G_1 - G_4$ represents the open-loop transfer functions of the converter.

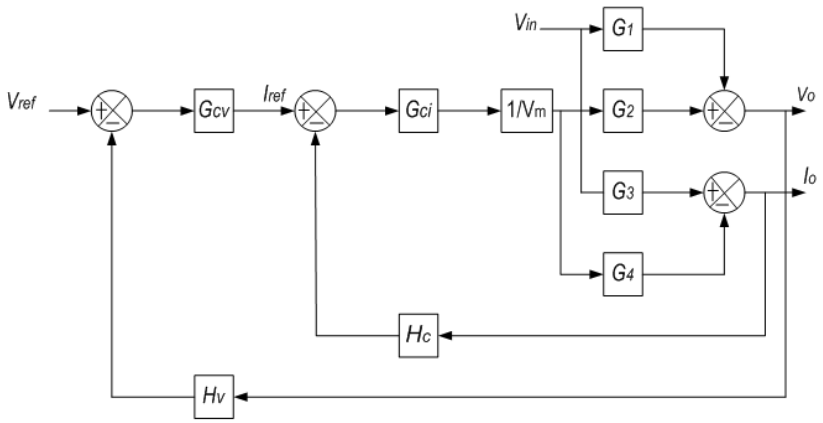

Figure 4.1: Average current mode control block diagram

4.3 SWECS CONTROLLER DESIGN

The variable voltage and frequency operation of the wind generator demands that duty-cycle of the switching converter be varied to ensure a well regulated voltage at the DC-bus. SWECS controller design will therefore, take into consideration the operation of converter in the specified range of duty-cycle in order to determine the best dynamic response.

The small signal transfer functions obtained in equations (3.44) to (3.47) are evaluated by substituting the converter specifications.

$$G_1 = \frac{\hat{v}_o(s)}{\hat{v}_{in}(s)}\Big|_{\hat{d}(s)=0} = \frac{171}{1.19\times10^{-7}s^2 - 2.05\times10^{-4}s + 29.56} \tag{4.1}$$

$$G_2 = \frac{\hat{v}_o(s)}{\hat{d}(s)}\Big|_{\hat{v}_{in}(s)=0} = \frac{-0.502s + 3.85\times10^{4}}{1.19\times10^{-7}s^2 - 2.05\times10^{-4}s + 29.56} \tag{4.2}$$

$$G_3 = \frac{\hat{i}_{L11}(s)}{\hat{v}_{in}(s)}\Big|_{\hat{d}(s)=0} = \frac{1.4\times10^{-3}s + 2.63}{1.19\times10^{-7}s^2 - 2.05\times10^{-4}s + 29.56} \tag{4.3}$$

$$G_4 = \frac{\hat{i}_{L11}(s)}{\hat{d}(s)}\Big|_{\hat{v}_{in}(s)=0} = \frac{0.305s + 1.58\times10^{3}}{1.19\times10^{-7}s^2 - 2.05\times10^{-4}s + 29.56} \tag{4.4}$$

4.3.1 Current loop design

Current loop is designed with a bandwidth of 20 kHz and a current overshoot of 25% translating to a phase-margin of 45° and a settling-time of less than 0.5ms. Open loop current gain, $T_C(S)$ is obtained from figure 4.1 as,

$$T_c(s) = \frac{H_c \times G_{ci} \times G_4}{V_m} \tag{4.5}$$

Current sensor gain, ($H_c(s)$)

For an inductor reference current, I_{ref} of 10 A, the feedback gain of the current loop, H_c is obtained as

$$H_c(s) = \frac{I_{ref}}{I_{L11}} = \frac{10A}{15.39A} = 0.65 \tag{4.6}$$

Modulator design (V_m)

The peak-to-peak value of modulating signal, V_m is chosen as $5V$.

Compensator design, $(G_{ci}(s))$

Assuming compensator transfer function, $G_{ci}(s) = 1$, the open loop current gain, $T_c(s)$, is obtained from equation (4.5) as,

$$T_c(s) = \frac{3.96 \times 10^{-2}s + 204.8}{1.19 \times 10^{-7}s^2 - 2.05 \times 10^{-4}s + 29.56} \tag{4.7}$$

The open-loop current gain bode plots are shown in figure 4.2. It is observed that the phase-margin is 90.1° at a natural crossover frequency of $52.3kHz$. The corresponding phase-margin at the $20kHz$ desired crossover frequency is 89.8°. From the step response shown in figure 4.3, the current loop has an overshoot of 5% and takes 0.25ms to settle within 2% of its final steady-state value. To slow down the current-loop, the bandwidth is reduced to the desired crossover frequency using a lag-compensator. It improves the steady-state error by increasing only the low frequency gain while leaving the system with sufficient phase-margin. The transfer function of the lag-compensator is obtained as,

$$G_{ci}(s) = \frac{3.045 \times 10^{-6}s + 0.9}{1.87 \times 10^{-5}s + 1} \tag{4.8}$$

The bode plots of the compensated current-loop transfer-function, Tci, are presented in figures 4.2. The phase-margin is 45.1° at a gain crossover frequency of 20.2kHz. It is observed from the step response, shown in figure 4.3, that the compensated system has a steady-state error of 2%, current overshoot of 24.2% and requires 0.46 ms to settle within 2% of its final value. Thus, the system meets its design specifications.

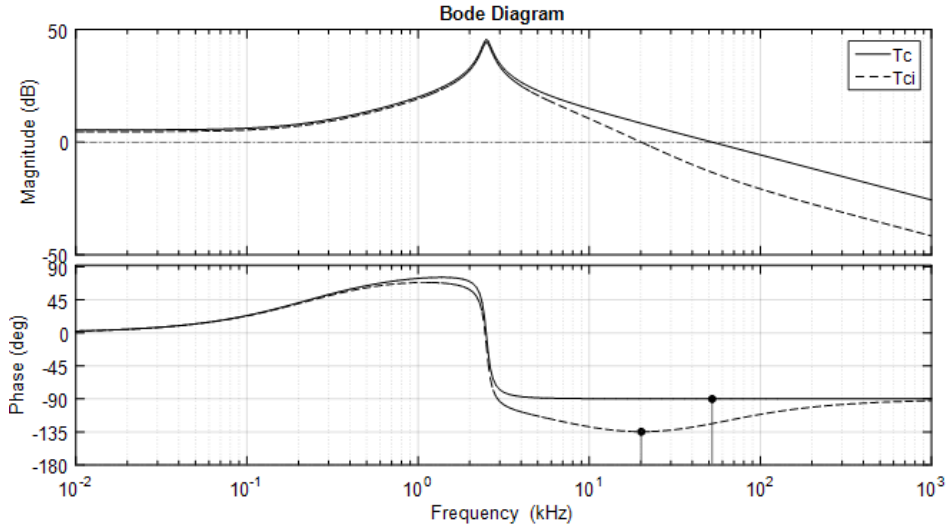

Figure 4.2: Current gain bode plots

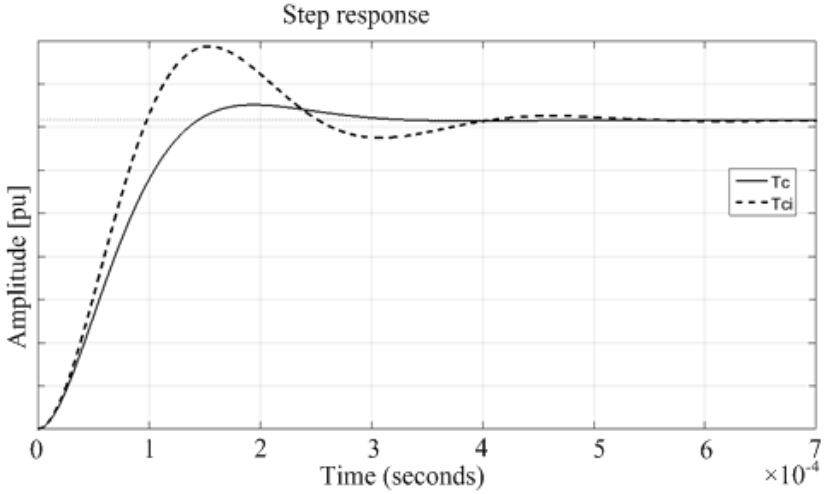

Figure 4.3: Current loop step responses

It can be seen that the gain crossover frequency and closed-loop bandwidth for the compensated system is lower than that of uncompensated system after the phase margin specification has been satisfied. Therefore, less noise and other unwanted high frequency signals are passed by the system.

4.3.2 Voltage loop design

Voltage loop is designed with a smaller bandwidth compared to that of current loop. This is because its time constant is much longer. Therefore, a voltage-loop crossover frequency equal to a quarter of the current loop crossover frequency is desirable in order to provide a good separation of operational dynamics between the two loops. In this case, a bandwidth of 5kHz and a voltage overshoot of 5% corresponding to a phase-margin and a settling-time of 65° and $2ms$, respectively, are considered. The transfer function of voltage loop is given by,

$$T_v(s) = G_{cv}G_2H_v \times \frac{1}{H_cG_4} \times \frac{T_{ci}}{1+T_{ci}} \tag{4.9}$$

Feedback voltage gain, $H_v(s)$

For a voltage reference, $V_{o,ref}$ of 10V, voltage sensor gain is obtained as,

$$H_v(s) = \frac{V_{o,ref}}{V_o} = \frac{10V}{380V} = 0.0263 \tag{4.10}$$

Compensator design, $G_{cv}(s)$

Considering a compensator transfer function, $G_{CV} = 1$, the open-loop voltage gain can be evaluated by substituting converter specifications in equation (4.9). Figure 4.4 presents the open-loop voltage gain bode plots. Phase-margin is 131° at a natural crossover frequency of $1.36kHz$. The corresponding phase-margin at the $5kHz$ desired frequency is 117°. From the step response shown in Figure 4.5, the uncompensated voltage loop has a 3.5% overshoot and a settling time of $1.65ms$. Although phase margin is good, the bandwidth is very small and hence the system might respond very slowly. A phase lead-lag compensator is proposed to increase the low frequency gain, reduce phase margin and increase system bandwidth to the specified crossover frequency. The transfer function of compensator is obtained as,

$$G_{cv}(s) = \left(\frac{1.16\times10^{-8}s^2 + 2.83\times10^{-3}s + 8.71}{1.39\times10^{-8}s^2 + 3.37\times10^{-4}s + 1}\right) \tag{4.11}$$

The compensated voltage-loop bode plots are presented in Figure 4.4. The compensated system has a phase-margin of 65° at a gain crossover frequency of $4.99kHz$. From figure 4.5, it is observed that the

system has a 4.41% voltage overshoot and takes 1.4*ms* to settle within 2% of its final value. Thus, the system meets its design specifications.

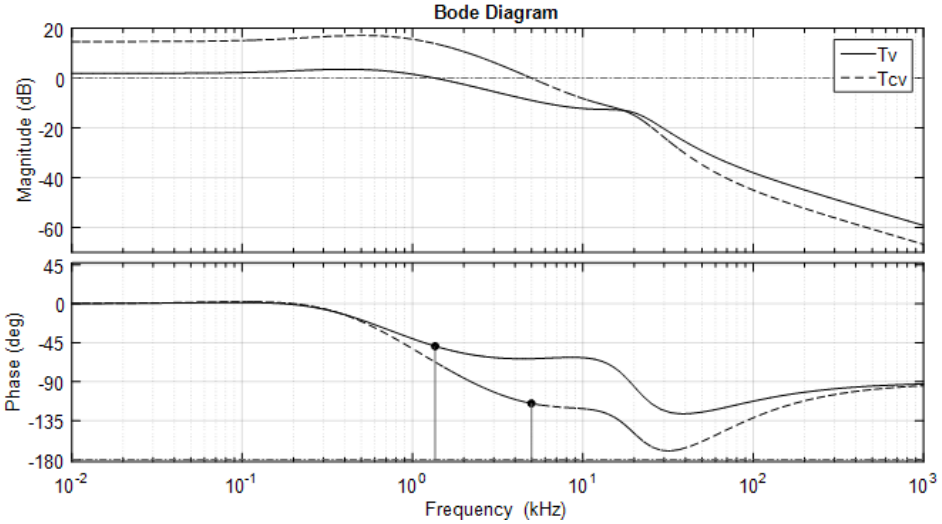

Figure 4.4: Voltage gain bode plots

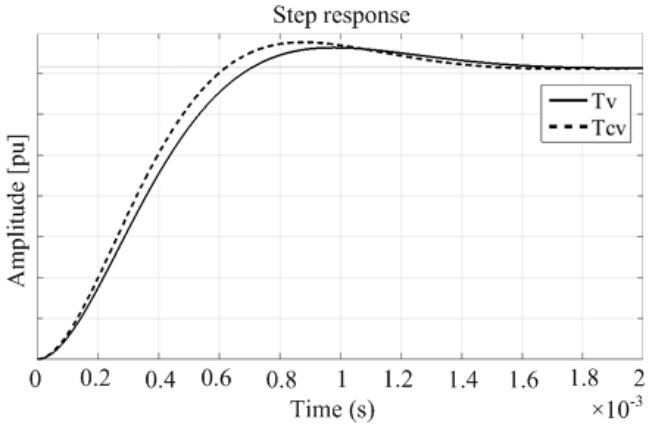

Figure 4.5: Voltage loop step response

4.4 DIGITAL CONTROL

With invention and growth of microprocessor circuitry, digital control is gaining increased popularity in control of switch-mode power converter systems. Microprocessors with a high clock speeds have emerged making it possible to implement digital controllers with a very high bandwidth. Digital signal processors (DSPs), microcontrollers and field-programmable gate arrays (FPGAs) are finding applications in motor drive controllers and high voltage and frequency converters [48], [49]. Compared to conventional analogue control, digital control offers numerous advantages such as; [50], [51],

- Reduced number of electronic devices
- Easier implementation of computational functions and sophisticated control schemes
- Reduction of electromagnetic interference levels (EMIs)
- Flexibility which makes it possible to easily modify the code for other applications
- Reduced sensitivity to noise and environmental variations

However, digital control has some limitations which include [51]:

- Word count in processor and A/D converter are finite which limits the signal resolution
- There is a sampling time delay which is caused by A/D conversion, control algorithm computation by the processor and PWM generation.
- There is restriction in computational power and control loop bandwidth

Figure 4.6 shows a block diagram of a digitally controlled DC-DC boost converter. Generally, there

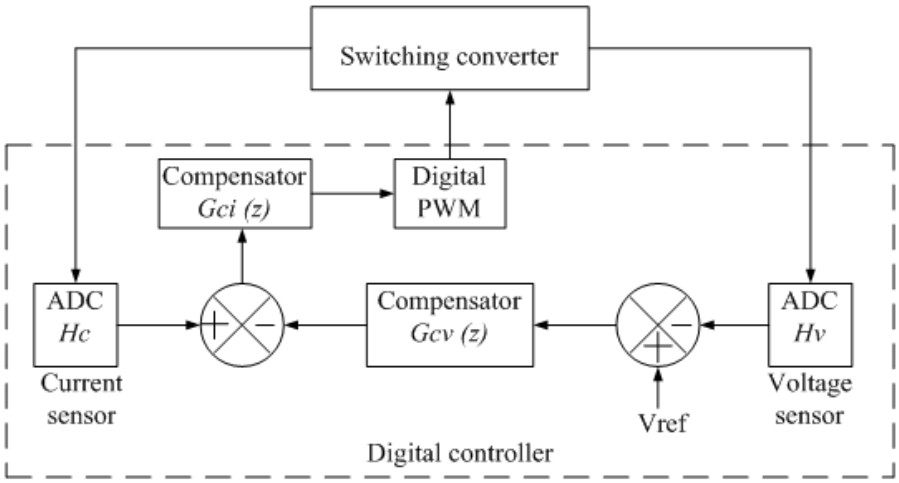

Figure 4.6: Block diagram of a digitally controlled switching converter

are two approaches that are commonly employed in design of a digital controller:

a) Digital redesign approach

b) Direct digital approach

4.4.1 Digital redesign approach

In digital redesign approach, an analogue controller is first designed in continuous s-domain and then converted into a discrete form by approximate discretization method [50], [52]. The advantage of this method is that it is easier to work in s-plane than in z-plane. However, there is a tendency of z-plane poles to get distorted during discretization process. Table 4.1 presents some common methods of dicretization.

Table 4.1: Discretization methods

Transformation method	**s-Domain**	**z-Domain**
Backward euler	s	$\frac{(1-z^{-1})}{T_s}$
Bilinear	s	$\frac{2}{T_s} \times \frac{(1-z^{-1})}{(1+z^{-1})}$
Step invariant	$G_c(s)$	$Z(\frac{1-e^{-T_s s}}{s} \times G_c(s))$
Pole/Zero match	$\frac{(s+a)}{(s+a+jb)}$	$\frac{(1-z^{-1}e^{-aT_s})}{(1-2z^{-1}e^{-aT_s}cosbT_s+z^{-2}e^{-2aT_s})}$
Matched pole/zero	e^{sT}	z

4.4.2 Direct digital approach

In direct digital approach, the converter functions in continuous s-domain are first transformed into z-domain. The controller is then designed directly in the z-domain [50], [52]. The advantage of this method is that poles and zeros of discrete compensator are located directly. However, this approach makes it difficult to visualize where to locate z-domain poles and zeroes in order to obtain a system that performs optimally. There are various methods used in direct digital approach namely; discrete-time frequency response method, root-locus method, or deadbeat method.

4.4.3 SWECS digital controller design

The average current mode control for the SWECS was implemented digitally to ease the control process, reduce number of passive components and ensure a high efficiency operation of the converter. The current compensator, $G_c(s)$, and voltage compensator, $G_v(s)$ designed in the analogue controller were converted into a discrete form using Pole/Zero Matching method [53]. This was done using Matlab algorithms for a sampling frequency, $f_s = 100kHz$.

$G_{ci}(s) = tf([3.045e-6 \;\; 0.9],[1.87e-5 \;\; 1];$
$T_s = 1e-5;$
$G_{ci}(z) = c2d(G_{ci}(s), T_s, 'matched');$

$G_{cv}(s) = tf([1.16e-8 \;\; 2.83e-3 \;\; 8.71],[1.39e-8 \;\; 3.37e-4 \;\; 1]);$
$T_s = 1e-5;$
$G_{cv}(z) = c2d(G_{cv}(s), T_s, 'matched');$

The Z-transform for the compensators were obtained as,

$$G_{ci}(z) = \frac{0.3932z - 0.02047}{z - 0.5858} \tag{4.12}$$

$$G_{cv}(z) = \frac{1.991z^2 - 2.109z + 0.1736}{z^2 - 1.778z + 0.7847} \tag{4.13}$$

The transfer functions obtained above are further converted into a difference equation for implementation in a digital controller.

$$G_{ci}(z) = \frac{D(z)}{E(z)} = \frac{0.3932 - 0.02047z^{-1}}{1 - 0.5858z^{-1}} \tag{4.14}$$

$$G_{cv}(z) = \frac{D(z)}{E(z)} = \frac{1.991 - 2.109z^{-1} + 0.1732z^{-1}z^{-2}}{1 - 1.778z^{-1} + 0.7847z^{-2}} \tag{4.15}$$

where the multiplier Z^{-1} represents a 1-cycle delay.

Thus, for current compensator

$$d(n) = 0.5858d(n-1) - d(n) + 0.3932e(n) - 0.02047e(n-1) \tag{4.16}$$

For voltage compensator,

$$d(n) = 1.778d(n-1) - d(n) - 0.7847d(n-2) + 1.991e(n) - 2.109e(n-1) + 0.1736e(n-2) \quad (4.17)$$

where d is the output of the digital compensator and e is the error current.

4.4.3.1 Digital controller implementation in PSIM

Digital controller was implemented in PSIM software to simulate the performance of the system. This was made possible through the use of z-domain simulation blocks to implement the average current mode control algorithm. Figure 4.7 present the proposed SWECS with digital controller. Voltage and current waveforms are captured and documented in the simulation results chapter.

4.4.3.2 Digital controller implementation in microcontroller

A 32-bit Piccolo microcontroller (TMS320F28027) with a processor speed of 60MHz,12-bit ADC, high resolution PWM module, and a fast interrupt response and processing was used to implement the digital controller [54]. The micro controller was coded using C language which is relatively easy to use than C++ and uses less memory as compared to the assembly language. Code Composer Studio (CCS) was used to develop the system control software and algorithms.

The selected DSP is configured to generate a PWM with a switching frequency of 100kHZ. This is done by configuring the period register (TBPRD) in up-count mode and loading it with a value of 49 which corresponds to $10\mu s$ time period of the PWM. The duty-cycle is initialised by loading a value on the compare register (CMPA). To generate a another phase shifted PWM2, the phase loading on the second PWM is enabled (TBCTL.bit.PHSEN) and loaded with a value equal to that of the first PWM1 to ensure the duty-cycle on both phases remains the same. The general purpose input and output (GPIO) are then set-up. The first PMW is initialised on EPWM1A pin, while the second PWM is initialised on EPWM2A pin.

The next step involves configuring the ADC registers of the DSP. These registers receives input from the inductor current sensor, input voltage (template) sensor and output voltage sensor, and converts these results into digital form. For proper operation of the ADC, anti-aliasing filters are added between the sensors and ADC. These filters are used to attenuate switching noise riding on the voltage and

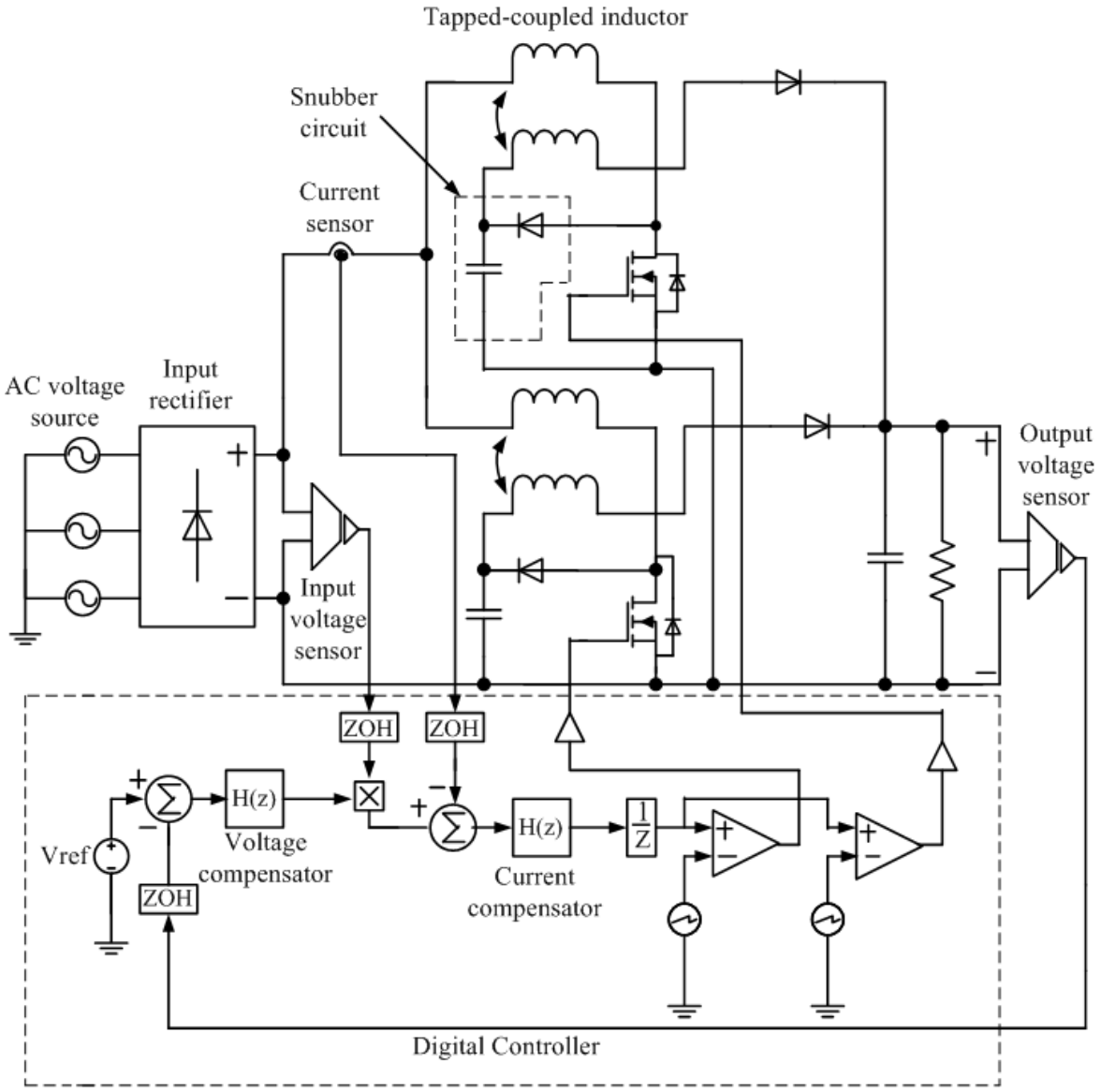

Figure 4.7: Proposed small wind energy conversion system

current signals which can degrade the performance of converter. The filtered signal is passed into the ADC for conversion and an interrupt generated to signify end of conversion. The resultant ADC value is subtracted from an initial reference value defined in the program to generate an error. This error is processed using a digital compensator algorithm already written into the code. The result is updated on CMPA for the next PWM duty-cycle which takes effect at the start of the new switching cycle. The full program code is shown in Appendix.

4.4.3.3 Sensor implementation

Implementation of the average current mode controller involves sensing the input and output voltage and current.

Voltage sensor

An LV20-P voltage transducer rated at 10mA is considered due to its high accuracy, high bandwidth and high immunity to external interference. Figure 4.8 presents the layout of the voltage sensor employed to measure the bus voltage.

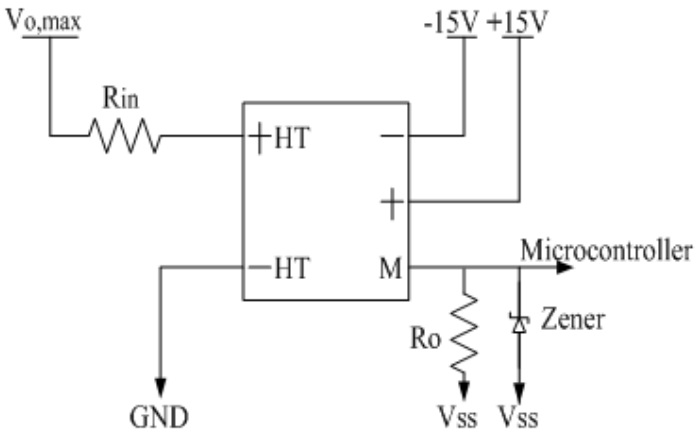

Figure 4.8: Voltage sensor

The maximum bus voltage was selected as 385V to cater for the peak-to-peak ripple. For an input current of 10mA for the sensor, the input resistor is obtained as,

$$R_{in} = \frac{V_{o,max}}{I_{in}} = \frac{385}{10 \times 10^{-3}} = 38.5k\Omega \tag{4.18}$$

The power dissipated in R_{in} is given by,

$$P_{Rin} = I_{in}{}^2 \times R_{in} = 0.01^2 \times 38.5k\Omega = 3.85W \tag{4.19}$$

Hence, a $40k\Omega$, 5W resistor was chosen.

An output voltage of 3V, which is less than the rated maximum voltage of the microprocessor ADC (3.3V), is selected for the sensor output. Consequently, the output resistor, R_o, is determined considering

the rated output current of 25mA for the sensor.

$$R_o = \frac{V_o}{I_o} = \frac{3}{0.025} = 120\Omega \tag{4.20}$$

The power dissipated in the R_o is given by,

$$P_{Ro} = I_o^2 \times R_o = 0.025^2 \times 120 = 0.075W \tag{4.21}$$

Current sensor

An LA 55-P current transducer rated at 50A was selected due to its high accuracy, wide frequency bandwidth and high immunity to external interference. Figure 4.9 presents the layout of the current sensor employed to measure the converter input current.

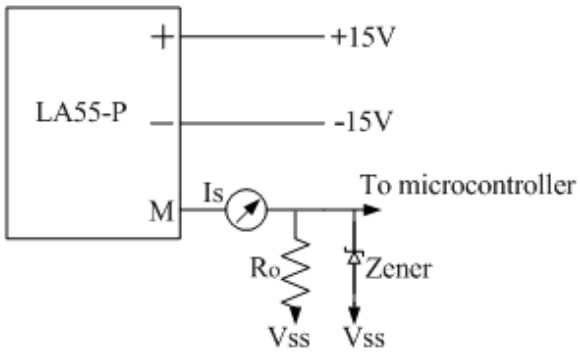

Figure 4.9: Current sensor

The cable connecting the output of the diode rectifier to the input of the interleaved DC-DC converter was wound three times around the top edge of the current sensor. The maximum current to be measured was initially determined as 15.39. Hence, the current from the measurement terminal of the sensor can be calculated as,

$$I_s = \frac{N_w I_p}{n} \tag{4.22}$$

where: N_w is the number of turns wound around the device, I_p is the maximum current passing through the cable and n is the rated conversion ratio of the sensor device.

Therefore, from equation (4.22),

$$I_s = \frac{3 \times 15.39}{1000} = 46mA \tag{4.23}$$

The value of output resistor, R_o is given by,

$$R_o = \frac{V_o}{I_s} = \frac{3}{0.046} = 65.2\Omega \tag{4.24}$$

where V_o is the voltage supplied to the ADC input of the microprocessor.

The power dissipated in the output resistor was determined as,

$$P_{Ro} = I_s^2 \times R_o = 0.138W \tag{4.25}$$

4.5 LOW VOLTAGE BATTERY INTERFACE SYSTEM CONTROL

This section presents the system control of the low voltage battery interface. Two sets of pulse width modulation (PWM) circuitries are employed to drive the pair of bidirectional switches, one set in boost-mode and the other in buck-mode operation. Closed-loop control is provided by an average current mode controller (ACMC) shown in figure 4.1. This controller employs two loops to control input current and output voltage.

4.5.1 Buck-mode controller design

Buck-mode operation of the converter corresponds to charging of the specified lead-acid battery. A three-stage charging concept is considered so that the maximum charging voltage is regulated to avoid damaging the battery cells. The first stage involves charging the battery at a constant current until the boost voltage is achieved. In the second stage, current is progressively reduced to one quarter of its maximum rating which makes the charging voltage to drop automatically to float voltage level. The final stage involves charging the battery with minimum current to compensate for losses caused by self-discharge.

Battery charging voltage ranges from 2.30V to 2.45V per cell. Thus for a 48V rated battery (with 24 cells), the charging voltage is determined as 55.2V to 60V. In addition, most manufacturers recommend selecting a maximum charging current equivalent to 25% of the battery capacity (Ampere-hours). Therefore, for the 100Ah lead-acid battery considered in this research, the maximum charging current of 25A would suffice. However, to increase the battery lifespan, a smaller charging current

of 17A is preferred which is equal to the converter output current during the converter buck-mode operation.

The small signal transfer functions of the converter operating in buck-mode is obtained from equations (3.118) to (3.121) as

$$G_{1-bu} = \frac{\hat{v}_{bat}(s)}{\hat{v}_{bus}(s)}\Big|_{\hat{d}(s)=0} = \frac{6.34}{5.3\times10^{-8}s^2 + 2.5\times10^{-3}s + 40.17} \tag{4.26}$$

$$G_{2-bu} = \frac{\hat{v}_{bat}(s)}{\hat{d}(s)}\Big|_{\hat{v}_{bus}(s)=0} = \frac{-5.88\times10^{-1}s + 3.55\times10^{4}}{5.3\times10^{-8}s^2 + 2.5\times10^{-3}s + 40.17} \tag{4.27}$$

$$G_{3-bu} = \frac{\hat{i}_{L21}(s)}{\hat{v}_{bus}(s)}\Big|_{\hat{d}(s)=0} = \frac{5.66\times10^{-5}s + 2.62}{5.3\times10^{-8}s^2 + 2.5\times10^{-3}s + 40.17} \tag{4.28}$$

$$G_{4-bu} = \frac{\hat{i}_{L21}(s)}{\hat{d}(s)}\Big|_{\hat{v}_{bus}(s)=0} = \frac{7.25\times10^{-2}s + 4.14\times10^{3}}{5.3\times10^{-8}s^2 + 2.5\times10^{-3}s + 40.17} \tag{4.29}$$

4.5.1.1 Current loop design

The current loop is designed with a bandwidth of $20kHz$ and a current overshoot of 25%, which translates to a phase-margin of 45° and a settling-time of less than $0.5ms$. The open loop current gain, $T_c(s)$ is obtained from figure 4.1 as,

$$T_c(s) = \frac{H_c \times G_{ci} \times G_4}{V_m} \tag{4.30}$$

Feedback current gain, $(H_c(s))$

Since the coupled inductor in a buck converter is on the output-side, the current sensor tracks the output current which is obtained as,

$$I_{L21,avg} = I_{o,avg} = 16.67A \tag{4.31}$$

For an inductor reference current of 10 A, the current sensor gain is obtained as

$$H_c(s) = \frac{10A}{16.67A} = 0.6 \tag{4.32}$$

Modulator design (V_m)

The peak-to-peak value of modulating signal, V_m is chosen as $5V$

Compensator design, $(G_{ci}(s))$

Assuming compensator transfer function, $(G_{ci}(s)) = 1$, the open loop current gain, $T_c(s)$, is obtained from equation (4.30) as,

$$T_c(s) = \frac{8.7 \times 10^{-3}s + 496.8}{5.3 \times 10^{-8}s^2 + 2.5 \times 10^{-3}s + 40.17} \tag{4.33}$$

The open-loop current gain bode plots are shown in figure 4.10. It is observed that uncompensated system has a phase-margin of $87.3°$ at a natural crossover frequency of $27.2kHz$. The corresponding phase-margin at the $20kHz$ desired crossover frequency is $87.1°$. From the step response shown in figure 4.11, current loop has an overshoot of 12.5% and takes $0.25ms$ to settle within 2% of its final steady-state value. To decrease system bandwidth to the desired crossover frequency, a lag compensator is proposed. It improves steady-state error by increasing only the low frequency gain while leaving the system with sufficient phase-margin. The transfer-function of lag compensator is obtained as,

$$G_{ci}(s) = \frac{5.89 \times 10^{-6}s + 1.68}{1.8 \times 10^{-5}s + 1} \tag{4.34}$$

The bode plots of the compensated current-loop transfer-function, $T_{ci}(s)$, are presented in figure 4.10.

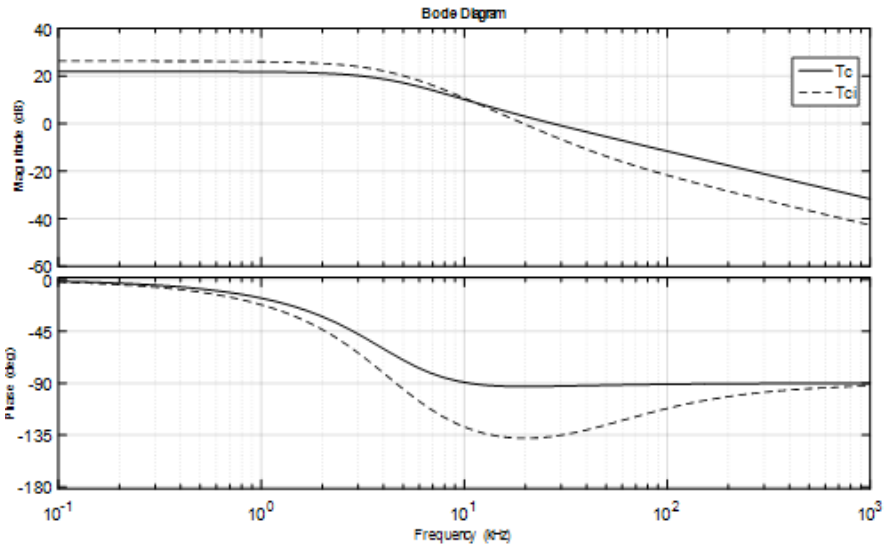

Figure 4.10: Current gain bode plots

It has a phase-margin of 44.8° at a gain crossover frequency of 20.4kHz. It is observed from the step response, shown in figure 4.11, that the compensated system has a steady-state error of 2%, current-overshoot of 23.9% and requires 0.4ms to settle within 2% of its final value. Hence the system meets design specifications. The gain crossover frequency and closed-loop bandwidth for the compensated system is lower than that of uncompensated system after phase-margin specification has been satisfied. Therefore, less noise and other unwanted high frequency signals are passed by the system.

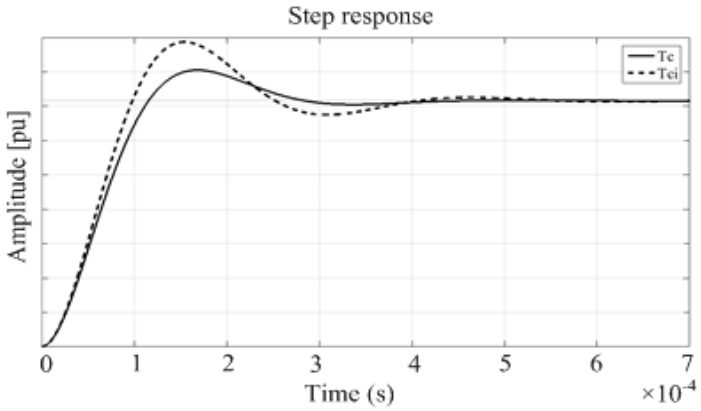

Figure 4.11: Current loop step responses

4.5.1.2 Voltage loop design

The outer voltage-loop is designed for a bandwidth of 5kHz to provide a good separation of the operational dynamics between voltage and current loops. It is also designed with an overshoot of 5% which corresponds to a phase-margin and settling-time of 65° and 2ms respectively. The open-loop voltage gain transfer-function, $T_v(s)$ is obtained from figure 4.1 as,

$$T_v(s) = G_{cv}G_2H_v \times \frac{1}{H_cG_4} \times \frac{T_{ci}}{1+T_{ci}} \tag{4.35}$$

Voltage sensor gain, $H_v(s)$

The voltage sensor gain is obtained as,

$$H_v(s) = \frac{V_{o,ref}}{V_o} = \frac{10V}{60V} = 0.167 \tag{4.36}$$

Compensator design, $G_{cv}(s)$

Considering a compensator transfer function, $G_{cv}(s) = 1$, the open-loop voltage gain can be evaluated by substituting converter specifications in equation (4.35). Figure 4.12 presents the open-loop voltage gain bode plots. Phase-margin is 69.7° at a natural crossover frequency of $37.1kHz$. The corresponding phase margin at the desired $5kHz$ crossover frequency is 170.4°. From the step response, shown in figure 4.13, voltage overshoot is 2.1% and takes $0.89ms$ to settle within 2% of its final value. A phase lag compensator is proposed to decrease system bandwidth and hence slow down the voltage-loop as compared to current-loop. The transfer-function of lag compensator is obtained as,

$$G_{cv}(s) = \left(\frac{2.55 \times 10^{-5}s + 1.5}{1.11 \times 10^{-4}s + 1}\right) \tag{4.37}$$

The bode plot of the compensated voltage-loop transfer-function, $T_{cv}(s)$, is presented in figure 4.12. Phase-margin is 65° at a gain crossover frequency of $5.01kHz$. From the step response shown in figure 4.13, the closed-loop has 3.95% voltage-overshoot and takes $1.5ms$ to settle within 2% of its final steady-state value. Thus, the system meets the desired specifications.

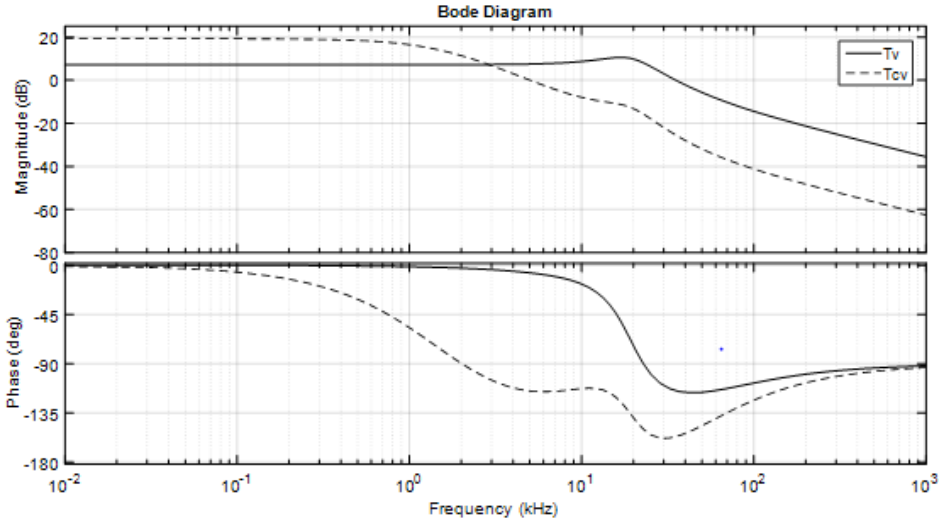

Figure 4.12: Voltage-gain bode plots

4.5.2 Boost-mode controller design

Operation of the converter in boost-mode corresponds to discharging of the battery storage system to supply the DC bus. Controller is designed to regulate output bus voltage in the presence of input voltage variations as battery charge diminishes and voltage drops below its rated value. The small

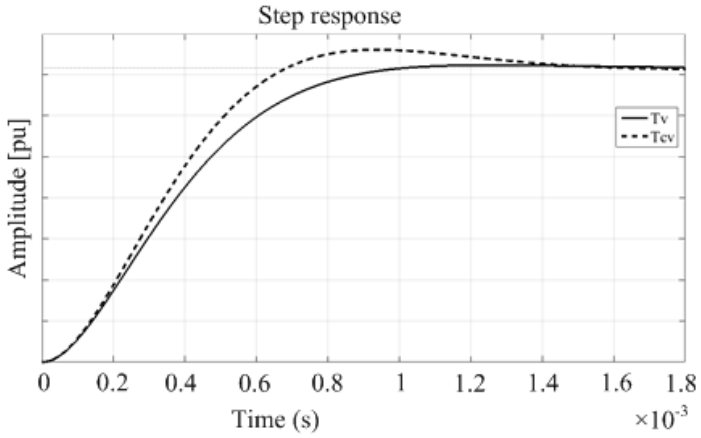

Figure 4.13: Voltage loop gain step response

signal transfer functions of the converter operating in boost-mode is obtained from equations (3.125) to (3.128) as

$$G_{1-bo} = \frac{\hat{v}_{bus}(s)}{\hat{v}_{bat}(s)}\Big|_{\hat{\delta}(s)=0} = \frac{286.6}{3.39\times10^{-7}s^2 + 8.42\times10^{-4}s + 36.54} \tag{4.38}$$

$$G_{2-bo} = \frac{\hat{v}_{bus}(s)}{\hat{d}(s)}\Big|_{\hat{v}_{bat}(s)=0} = \frac{-1.77s + 4.69\times10^{4}}{3.39\times10^{-7}s^2 + 8.42\times10^{-4}s + 36.54} \tag{4.39}$$

$$G_{3-bo} = \frac{\hat{i}_{L21}(s)}{\hat{v}_{bat}(s)}\Big|_{\hat{d}(s)=0} = \frac{2.29\times10^{-3}s + 3.97}{3.39\times10^{-7}s^2 + 8.42\times10^{-4}s + 36.54} \tag{4.40}$$

$$G_{4-bo} = \frac{\hat{i}_{L21}(s)}{\hat{d}(s)}\Big|_{\hat{v}_{bat}(s)=0} = \frac{0.386s + 2.18\times10^{3}}{3.39\times10^{-7}s^2 + 8.42\times10^{-4}s + 36.54} \tag{4.41}$$

4.5.2.1 Current loop design

The current-loop of converter operating in boost-mode can be designed with the same specifications as those listed in buck-mode operation, even though their operational dynamics are different: current overshoot of 25%, phase-margin of 45° and a settling-time of less than $0.5ms$. The open loop current gain, $T_c(s)$, is given by,

$$T_c(s) = \frac{H_c \times G_{ci} \times G_4}{V_m} \tag{4.42}$$

Current sensor gain, ($H_c(s)$)

The current sensor gain is given by,

$$H_c(s) = \frac{I_{ref}}{I_{L21}} = \frac{10A}{20.88A} = 0.479 \tag{4.43}$$

Modulator design (V_m)

The peak-to-peak value of modulating signal, V_m is chosen as $5V$

Compensator design, $(G_{ci}(s))$

Assuming the compensator transfer function, $(G_{ci}(s)) = 1$, open loop current gain, $T_c(s)$, is obtained from equation (4.42) as,

$$T_c(s) = \frac{0.037s + 208.8}{3.39 \times 10^{-7}s^2 + 8.42 \times 10^{-4}s + 36.54} \tag{4.44}$$

The open-loop current gain, bode plots are shown in figure 4.14 . Phase-margin is 88.4° at a natural crossover frequency of $17.5kHz$. The corresponding phase margin at the desired $20kHz$ crossover frequency is 88.6°. From the step response given in figure 4.15, the current loop has an overshoot of 14.5% and requires $0.35ms$ to settle to within 2% of its final value. A phase lead-lag compensator is proposed to increase bandwidth to the specified $20kHz$ and reduce phase margin to the desired 45°. The lead-lag compensator network, $G_{ci}(s)$, is derived as,

$$G_{ci}(s) = \frac{1.16 \times 10^{-8}s^2 + 7.8 \times 10^{-6}s + 2}{1.39 \times 10^{-8}s^2 + 1.61 \times 10^{-5}s + 1} \tag{4.45}$$

The bode plots of the compensated current-loop transfer-function, $T_{ci}(s)$, are presented in Figure 4.14. Phase-margin is 45.2° at a gain crossover frequency of $20.1kHz$. From figure 4.15, the system has a steady-state error of 2%, current overshoot of 21.2% and takes $0.32ms$ to settle within 2% of its final value. Thus, it meets the design specifications.

4.5.2.2 Voltage loop design

Although the operational dynamics of converter in buck and boost-mode are different, voltage loop can be designed with the same specifications, that is: bandwidth of $5kHz$, voltage overshoot of 5%, phase-margin of 65° and settling-time of less than 2 ms. The open loop voltage transfer function is

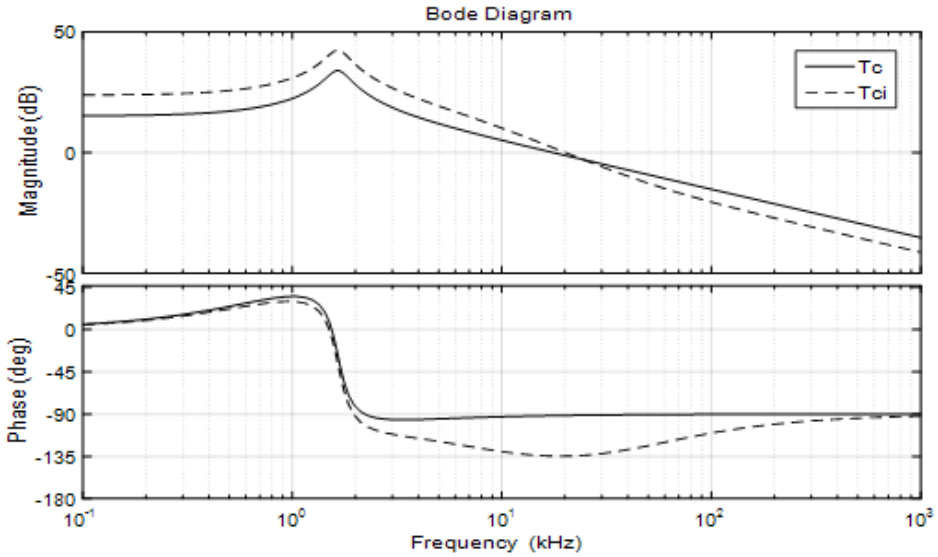

Figure 4.14: Current gain bode plots

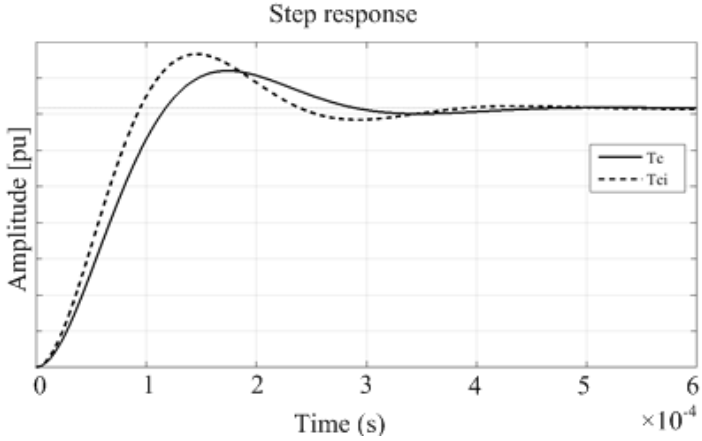

Figure 4.15: Current loop step responses

given by

$$T_v(s) = G_{cv}G_2H_v \times \frac{1}{H_cG_4} \times \frac{T_{ci}}{1+T_{ci}} \tag{4.46}$$

Feedback voltage gain, $H_v(s)$

For a voltage reference, $V_{o,ref} = 10V$, the feedback sensor gain of voltage loop is obtained as,

$$H_v(s) = \frac{10V}{380V} = 0.0263 \tag{4.47}$$

Compensator design, $G_{cv}(s)$

Considering a compensator transfer function, $G_{cv}(s) = 1$, the open-loop voltage gain is evaluated by substituting converter specifications in equation (4.46). Figure 4.16 presents the open-loop voltage-gain, Tv, bode plots. Phase-margin is 140° at a natural crossover frequency of $434Hz$. The corresponding phase-margin at the desired $5kHz$ crossover frequency is 144.5°. From the step response, shown in Figure 4.17, the uncompensated voltage loop has a 24% overshoot and a settling time of 2.5 ms. A phase lead-lag compensator is proposed to increase the low frequency gain, reduce phase margin and increase system bandwidth to the specified crossover frequency.

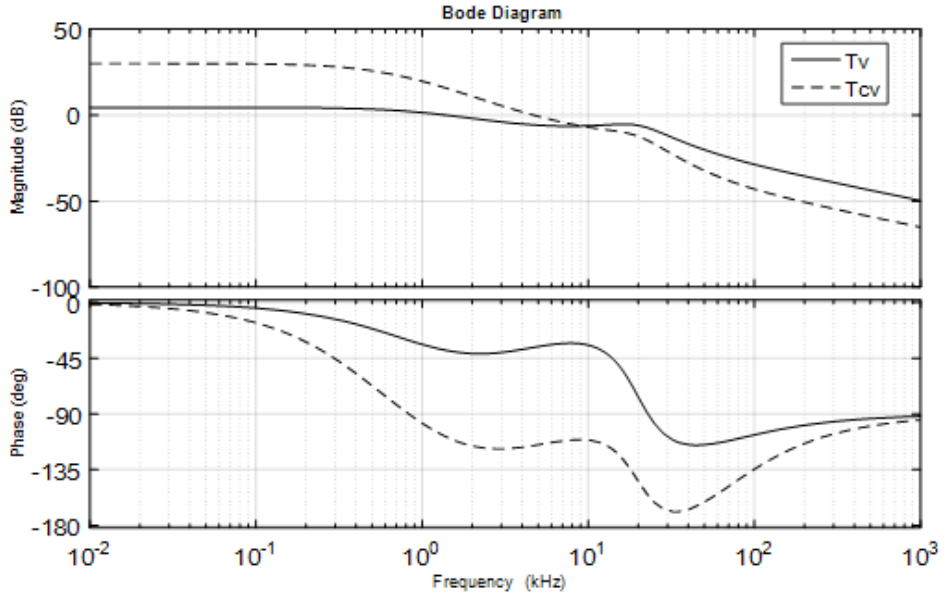

Figure 4.16: Voltage gain bode plots

The transfer function of compensator is obtained as,

$$G_{cv}(s) = \frac{1.16\times10^{-8}s^2 + 7.8\times10^{-6}s + 8.71}{1.39\times10^{-8}s^2 + 2.99\times10^{-5}s + 1} \tag{4.48}$$

The bode plots of the compensated voltage-loop transfer-function, Tcv, are presented in figure 4.16. It has a phase-margin of 65.1° at a gain crossover frequency of $5.01kHz$. From figures 4.17, the system has a steady-state error of 1.14%, voltage overshoot of 4.96%, and takes 1.5 m to settle within 2% of its final value. Thus, it meets the design specifications.

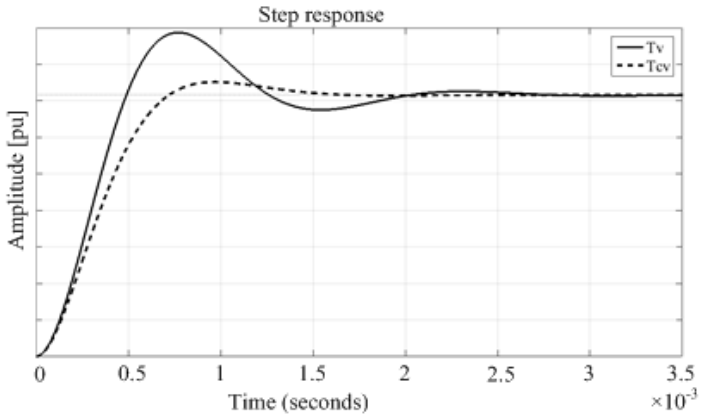

Figure 4.17: Voltage loop step response

4.5.3 Low voltage battery interface digital controller design

The analogue average current-mode controller designed in the previous section is implemented digitally to ease the control process and reduce number of passive components. The system compensator transfer functions are converted into a discrete form using Pole/Zero matching method.

4.5.3.1 Buck-mode digital implementation

Current and voltage compensator transfer functions are converted into digital format using the following matlab algorithm,

$G_{ci}(s) = tf([5.89e-6 \;\; 1.68],[1.8e-5 \;\; 1];$
$T_s = 1e-5;$
$G_{ci}(z) = c2d(G_{ci}(s), T_s, 'matched');$

$G_{cv}(s) = tf([2.55e-5 \;\; 1.5],[1.11e-4 \;\; 1];$
$T_s = 1e-5;$
$G_{cv}(z) = c2d(G_{ci}(s), T_s, 'matched');$

Z-transform of the compensators are obtained as,

$$G_{ci}(z) = \frac{0.76z - 0.04386}{z - 0.5738} \tag{4.49}$$

$$G_{cv}(z) = \frac{0.2906z - 0.1614}{z - 0.9138} \tag{4.50}$$

The transfer functions are further converted into a difference equation for implementation in a digital controller.

$$G_{ci}(z) = \frac{D(z)}{E(z)} = \frac{0.76 - 0.04386z^{-1}}{1 - 0.5738z^{-1}} \tag{4.51}$$

$$G_{cv}(z) = \frac{D(z)}{E(z)} = \frac{0.2906 - 0.1614z^{-1}}{1 - 0.9138z^{-1}} \tag{4.52}$$

Thus, for current compensator

$$d(n) = 0.5738d(n-1) - d(n) + 0.76e(n) - 0.04386e(n-1) \tag{4.53}$$

Similarly, for voltage, compensator,

$$d(n) = 0.9138d(n-1) - d(n) + 0.2906e(n) - 0.1614e(n-1) \tag{4.54}$$

where d is the output of digital compensator and e is the error current.

4.5.3.2 Boost-mode digital implementation

Current and voltage compensator transfer functions are converted into digital format using the following matlab algorithm,

$G_{ci}(s) = tf([1.16e-8 \;\; 7.8e-6 \;\; 2],[1.39e-8 \;\; 1.61e-5 \;\; 1]);$
$T_s = 1e-5;$
$G_{ci}(z) = c2d(G_{cv}(s), T_s, 'matched');$

$G_{cv}(s) = tf([1.16e-8 \;\; 7.8e-6 \;\; 8.71],[1.39e-8 \;\; 2.99e-5 \;\; 1]);$
$T_s = 1e-5;$
$G_{cv}(z) = c2d(G_{cv}(s), T_s, 'matched');$

Z-transform of the compensators are obtained as,

$$G_{ci}(z) = \frac{0.8332z^2 - 1.647z + 0.8276}{1z^2 - 1.981z + 0.9885} \tag{4.55}$$

$$G_{cv}(z) = \frac{0.8331z^2 - 1.599z + 0.8275}{1z^2 - 1.972z + 0.9787} \tag{4.56}$$

The transfer functions are further converted into a difference equation for implementation in a digital controller.

$$G_{ci}(z) = \frac{D(z)}{E(z)} = \frac{0.8332 - 1.647z^{-1} + 0.8276z^{-2}}{1 - 1.981z^{-1} + 0.9885z^{-2}} \tag{4.57}$$

$$G_{cv}(z) = \frac{D(z)}{E(z)} = \frac{0.8331 - 1.599z^{-1} + 0.8275z^{-2}}{1 - 1.972z^{-1} + 0.9787z^{-2}} \tag{4.58}$$

Thus, for current compensator

$$d(n) = 1.981d(n-1) - d(n) - 0.9885d(n-2) + 0.8332e(n) - 1.599e(n-1) + 0.8276e(n-2) \tag{4.59}$$

For voltage compensator,

$$d(n) = 1.972d(n-1) - d(n) - 0.9787d(n-2) + 0.8331e(n) - 1.599e(n-1) + 0.8275e(n-2) \tag{4.60}$$

4.5.3.3 Controller implementation in PSIM

Digital controller was implemented in PSIM software to simulate performance of the system. Figure 4.18 present the proposed low voltage battery interface with digital controller. Voltage and current waveforms for the converter components are presented in the simulation results chapter.

4.5.3.4 Controller implementation using microcontroller

The same 32-bit Piccolo micro-controller that was previously used to implement the digital control in the SWECS is also employed in this case. The DSP is set to generate a PWM with a switching frequency of 100kHz. However, the CMPA register is loaded with different values to initialise the duty-cycle of converter in buck and boost-mode. The GPIO is set to provide four PWM outputs. EPWM1A pin is set to provide a PWM signal at 180° out of phase with that of EPWM2A pin. Similarly, EPMW1B pin is set to generate a PWM signal at 180° out of phase with that of EPWM2B. Pins A and B generates a complementary PWMs output. The 12-bit ADC channels are programmed to receive analogue inputs from the current sensor, output and input voltage sensors. An anti-aliasing filter is added between the analogue signal sensors and ADC to attenuate switching noise and stray signals so that only the proper frequency content of the signal is converted. The program code is shown in Appendix B.

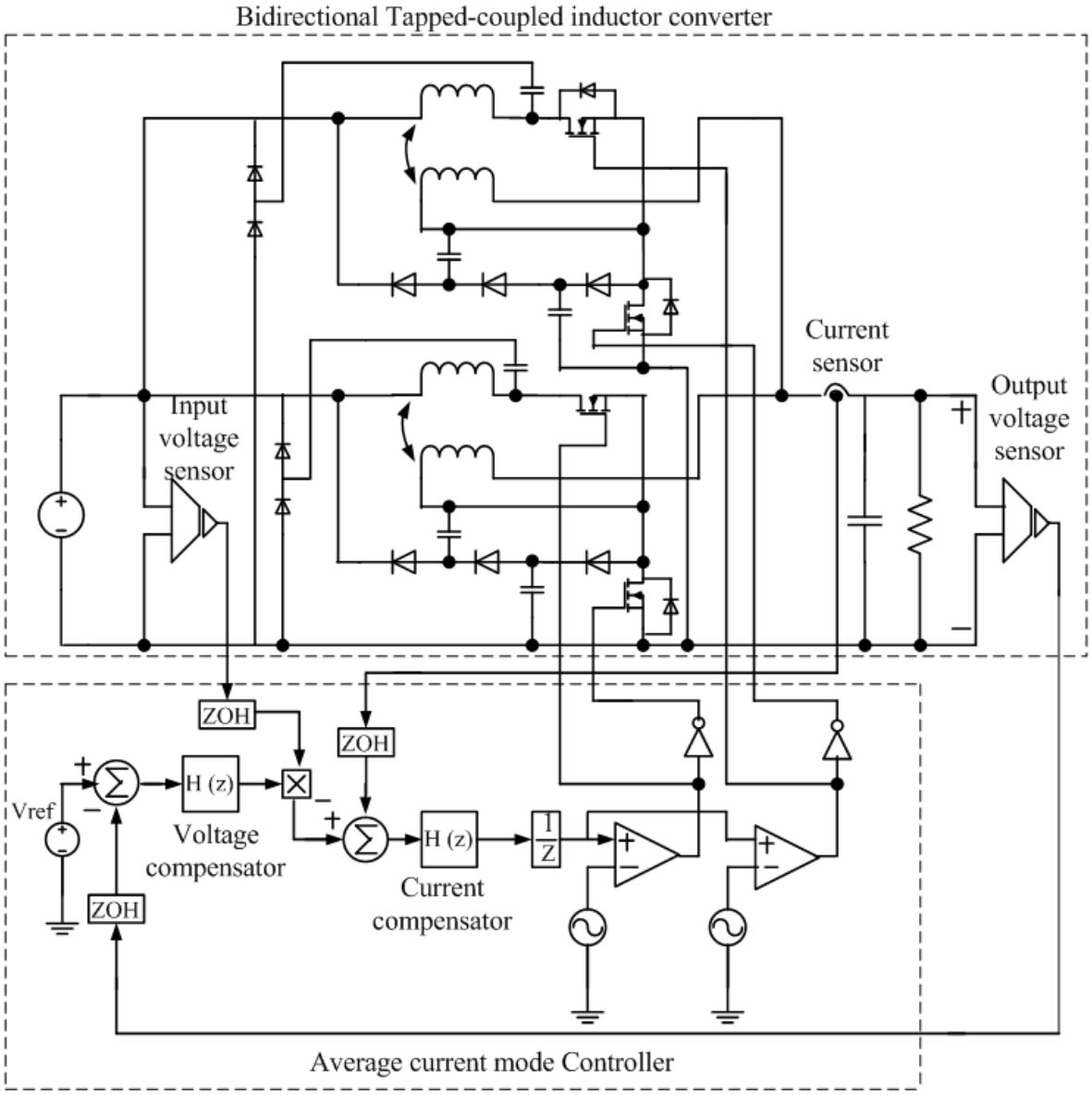

Figure 4.18: Proposed low voltage battery interface

4.5.3.5 Sensor implementation

An output current sensor and an input and output voltage sensors are required to implement the controller

Voltage sensor

An LV20-P voltage sensor, similar to the one employed in the SWECS, is used to detect the input and

output voltage in the low voltage battery interface. In buck-mode, the output sensor is tuned to measure an output voltage of 62V while in boost-mode, the sensor is tuned to measure an output voltage of 385V.

Current sensor

An LA 55-P, similar to the one that was employed in the SWECS, is used to detect current in the interface.

4.6 CHAPTER CONCLUSION

This chapter has presented the average current mode controller design of the proposed low voltage DC microgrid system. Matlab bode plots and step responses are obtained to evaluate the performance of the controller in achieving the stipulated design specifications. The controller is then converted into digital format using pole/zero matching and coded on the Piccolo micro-controller, in C++ language, using Code Composer Studio.

CHAPTER 5 SIMULATION RESULTS

5.1 CHAPTER OVERVIEW

In this chapter, the simulation results of a low voltage DC distribution system consisting of a small wind energy conversion system (SWECS) and a low voltage battery energy storage system (BESS) interface are presented. The SWECS specifications include: $V_{in,rms} = 48 - 96V$, $V_o = 380V$, 1.5% output voltage regulation, $P_o = 1000W$, $f_{sw} = 100kHz$, $L_{11} = 224\mu H$, $L_{21} = 2.02mH$, $r_{L11} = 0.029\Omega$, $C_o = 5\mu F$, $r_{L21} = 0.318\Omega$, $k = 0.99$, $n = 3$, and $r_{ds,on} = 47m\Omega$. In addition, a passive lossless snubber circuit comprising of a clamp capacitor, $C_c = 4\mu F$ and a diode is added to the converter topologies.

Low voltage battery interface specifications include: $V_{bus} = 380V$, $V_{bat} = 60V$ (while charging), and $48V$ (while discharging), $D = 0.53$ (buck-mode operation) and $D = 0.5$ (in boost-mode operation) $f_{sw} = 100kHz$, $L_{11} = 2.97mH$, $L_{21} = 84.8\mu H$, $r_{L11} = 0.73\Omega$, $C_o = 8.68\mu F$, $r_{L21} = 0.018\Omega$, $k = 0.99$, $n = 6$, $r_{ds1,on} = 82m\Omega$, $r_{ds2,on} = 1.2\Omega$. In addition, two sets of passive lossless snubber circuits were employed, one set to operate in boost mode and the other to operate in buck-mode converter operation. The boost-mode snubber comprises of two capacitors, $C_{s1} = 3nF$ and $C_{s2} = 24nF$, and three diodes while the buck-mode snubber comprises of a capacitor, $C_c = 0.47\mu F$.

5.2 SWECS SIMULATION RESULTS

The simulation of a SWECS, with the aforementioned specifications, is conducted using PSIM software. The key parameters of the converter such as output voltage and current, input rms current ripple, input peak-to-peak current, input power factor, and efficiency are plotted and their values compared with those derived from theoretical analysis.

To demonstrate the operation of the wind generator with variable speed, the SWECS is simulated with an AC input voltage of $48V_{rms}$, (which corresponds to the lowest working speed of 3m/s), and with an AC input voltage of $96V_{rms}$ (corresponding to the highest working speed of 20m/s for the specified generator). Various waveforms are obtained for converter operation that takes into account non-ideal components. The system is also subjected to a 25% step change in the input and output to simulate input voltage and load disturbances respectively.

5.2.1 Simulation waveforms for $V_{s,rms} = 48V$, and full load

Figures 5.1 (a) and (b) show the simulated waveforms for output voltage and current. The converter interface is able to achieve a high boost ratio of approximately 6 times at a moderate duty cycle of 0.55 as compared to an ideal conventional boost converter which would achieve the same voltage boost at an extremely high duty cycle of 0.83. Consequently, the proposed converter topology is suitable for interfacing a low voltage small wind generator to a DC bus.

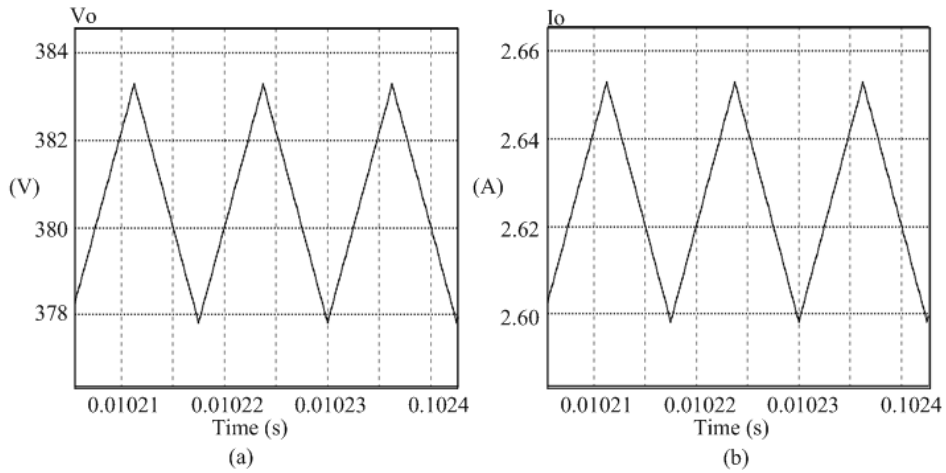

Figure 5.1: Simulated converter waveforms. (a) Output voltage and (b) Output current

Figure 5.2(a) presents the AC rectifier input current and voltage waveforms while figure 5.2(b) presents the current spectra. The first harmonic occurs at a frequency of 250Hz with a magnitude of 6A rms, the second harmonic occurs at a frequency of 550 Hz with a magnitude of 1.55A rms and the third harmonic occurs at a frequency of 650 Hz with a magnitude of 1.07A rms. The total harmonic distortion (THD) and total power factor is given by,

$$THD = \frac{1}{I_{sf}}\sqrt{\sum_{1}^{n} I_{sn}{}^{2}} \tag{5.1}$$

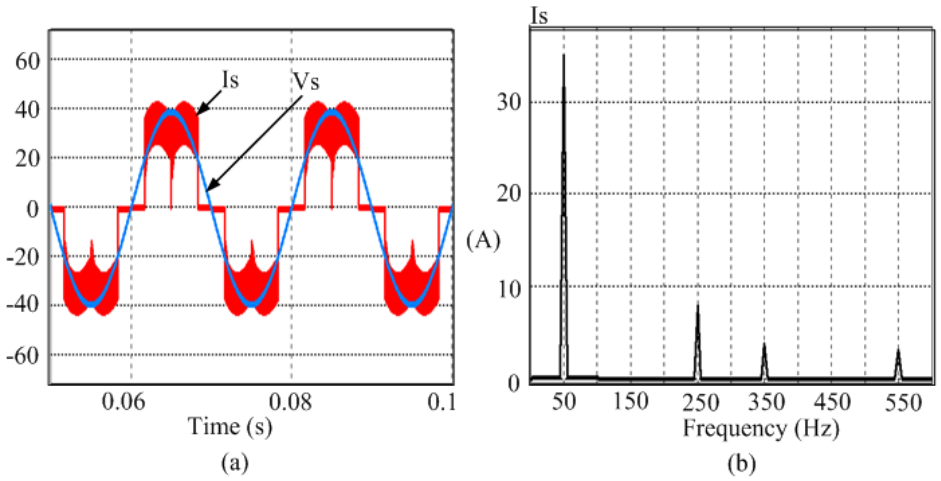

Figure 5.2: Simulated converter waveforms. (a) Input generator current and voltage (b) current frequency spectra

$$PF = \frac{DPF}{\sqrt{1+THD^2}} \tag{5.2}$$

where I_{sf} is the magnitude of the fundamental component, I_{sn} is the amplitude of the most significant current harmonics, and DPF is the displacement power factor.

From equation (5.1) and (5.2), THD is obtained as 20% while PF is obtained as 0.94. If a capacitor voltage filter was employed at the rectifier output, it has been calculated that THD would be 33.1% while PF would be 0.89. This is a clear proof that the proposed SWECS improves harmonic distortion and power factor.

Figures 5.3(a) and (b) present the input current for two phase and single-phase operation. The peak-to-peak and RMS ripple, for the two-phase converter, is 17.2A and 4.77A respectively, while that of a single-phase converter is 21.8A and 8.8A respectively. This is a clear demonstration that interleaving reduces the input current ripple.

Figures 5.4(a) and (b) present the active switch voltage with and without a snubber circuit. The applied passive lossless snubber circuit is able to clamp the voltage spikes from the initial peak of 1650V to 152.7V with no losses attributed to it. Consequently, active switches with lower voltage ratings are employed which reduces cost and power losses, hence improved efficiency of the converter.

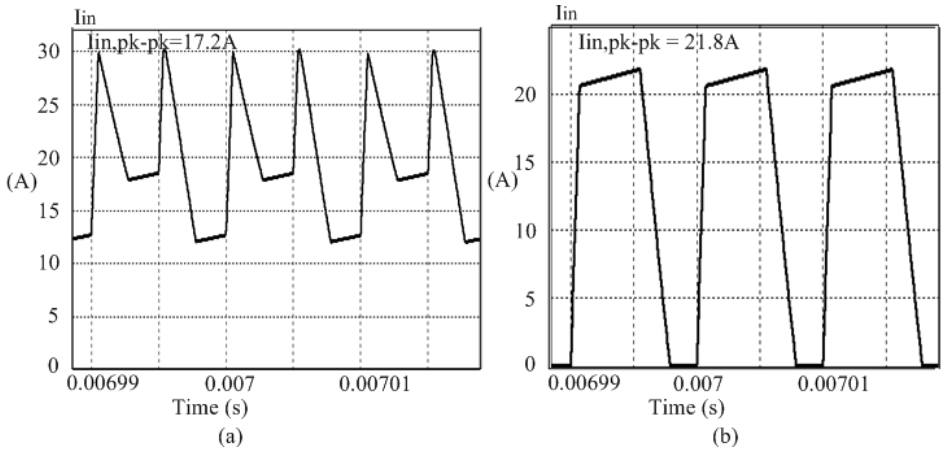

Figure 5.3: Simulated input current waveforms. (a) Two-phase operation (b) Single-phase operation

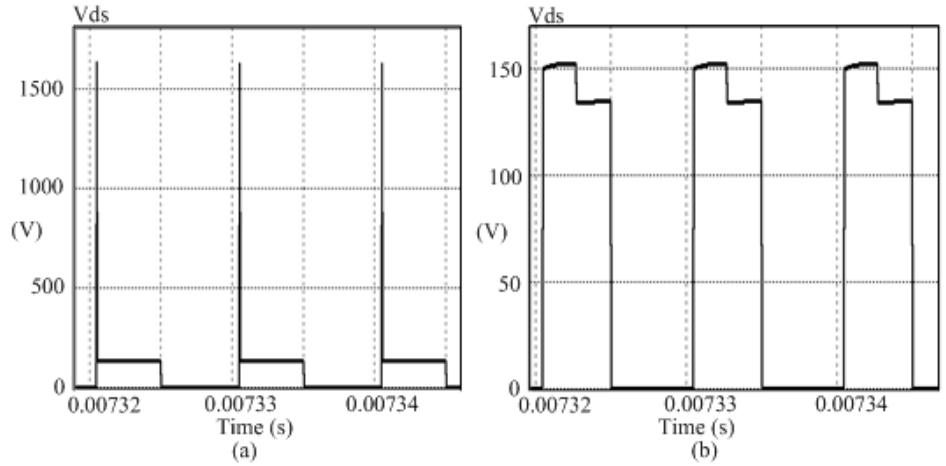

Figure 5.4: Simulated active switch voltage waveforms. (a) Without and (b) with snubber circuit

A comparison of the parameter results obtained from the simulation and those derived from theoretical analysis of the SWECS are presented in Table 5.1. It can be seen that the results are in good agreement.

5.2.2 Simulation waveforms for Vs,rms=96V and full load

A wind generator operates with a variable voltage and frequency due to variations in wind speed. To demonstrate operation of the proposed SWECS with variable input voltage, the converter is simulated with an input voltage of 96V which represents the highest generator output voltage at maximum operating speed. Figures 5.5(a) and (b) show the simulated waveforms for output voltage and current.

Table 5.1: Performance parameters for a two-phase tapped-coupled inductor boost converter

Parameter	**Analysis results**	**Simulation results**
Duty cycle	0.55	0.55
Input rms current $(I_{in,rms})$	15.61A	16.1A
Input current peak-peak $(I_{in,pk-pk})$	12.1A	12.6A
Input rms ripple current $(I_{in,rms-ripple})$	4.63A	4.77A
Capacitor rms current $(I_{c,rms})$	1.42A	1.6A
Output voltage (V_o)	380V	380.2V
Output voltage peak-peak $(V_{o,pk-pk})$	4.8V	3.8V
Average output current $(I_{o,ave})$	2.63A	2.65A
Switch rms current $(I_{ds,rms})$	17.2A	16.5A
Output diode rms current $(I_{D,rms})$	3.9A	2.5A

An average output voltage of 380V is obtained just like in the case of the converter operation with an input voltage of 48V AC. This is a demonstration of the ability of the closed loop control in regulating the output voltage and eliminating the effects of the input variations on the DC bus.

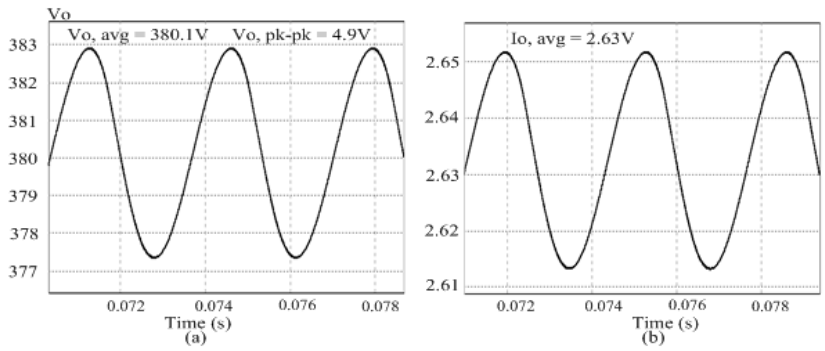

Figure 5.5: Simulated converter waveforms. (a) Output voltage and (b) Output current

5.2.3 Simulation waveforms for 25% step change in supply voltage

A wind generator is prone to disturbances due to the erratic weather conditions in which it operates. It is desirable that the converter interface is able to reject these disturbances so that they are not transferred to the grid. To demonstrate operation of the proposed SWECS with input disturbances, the converter is

simulated with a step change in supply voltage. Figure 5.6 presents simulated waveform for output voltage. It is observed that introduction of a 25% step change in supply voltage causes a 10.4% voltage undershoot. However, the normal output voltage of 380V is restored within a settling time of 1.5 ms. This means the employed controller is able to eliminate the effects of input disturbances on the output voltage.

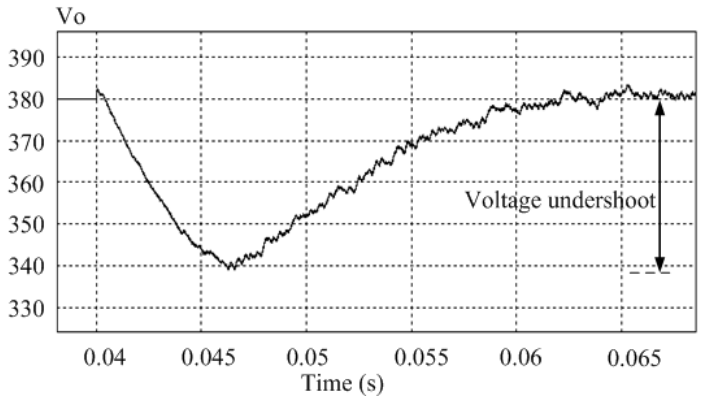

Figure 5.6: Output voltage for a 25% step change in supply voltage

5.2.4 Simulation waveforms for step change in load

The DC bus voltage is prone to variations due to changes in load. However, it is desirable that the voltage does not change much. To demonstrate operation of SWECS with load disturbances, the converter is simulated with a step change in load. Figure 5.7 presents the simulated output voltage. It is observed that introduction of a 25% decrease in load causes a 3.5% undershoot in the output voltage. The voltage oscillations settle down to a steady-state value of 377 V within a settling time of 1.5 ms. This means the controller is able to track the output voltage ensuring a voltage regulation of 0.79%.

5.2.4.1 SWECS efficiency

Efficiency is determined when the SWECS is operating at the two extreme input voltages ($V_{s,rms}$ =48 and 96V) and at different levels of output power. These levels of power are obtained by varying the output load, and hence the duty ratio, in order to maintain a constant output voltage.

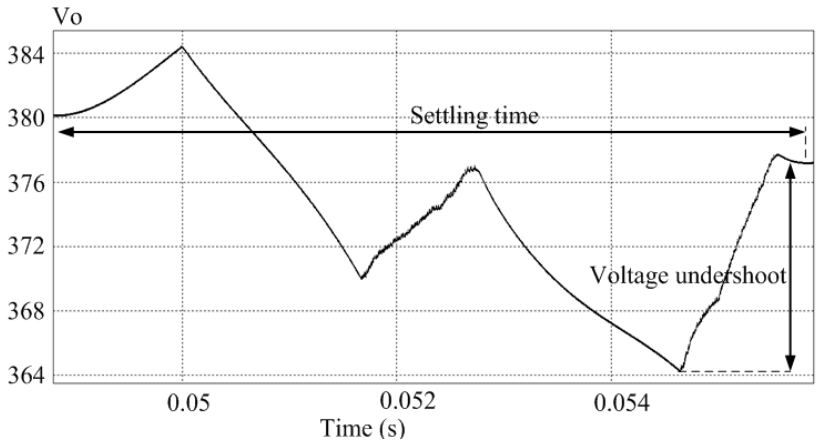

Figure 5.7: Output voltage for a 25% step change in load

Tables 5.2 and 5.3 present the converter losses at various levels of output power. At low power levels (less than 1000W), the highest losses are as a result of switching and conduction losses in the MOSFET switch which accounts for over 50% of the total converter loss. However, for power levels above 1000W, the highest losses are due to copper loss in the coupled-inductor windings which accounts for 51% of the total converter loss.

Table 5.2: Power losses in a single-phase tapped-coupled inductor boost converter with $V_{s,rms} = 48V$

Output power	**Copper loss**	**Total Switch loss**	**Diode conduction loss**	**Total loss**	**Efficiency** %
500W	6.79W	10.29W	1W	18.08W	96.38
750W	15.12W	17.92W	1.59W	34.63W	95.38
1000W	26.96W	27.39W	2.25W	56.6W	94.34
1250W	42.14W	38.66W	2.95W	83.75W	93.3
1500W	60.81W	51.65W	3.72W	116.18W	92.25

Figure 5.8 presents the efficiency-power characteristics of the converter. For operation of the converter at the two extreme input voltages, efficiency is high at low output power and decreases as the load is increased. The decrease in efficiency at high power levels is due to increase in the input rms and peak currents which causes increased converter losses. It can also be observed that efficiency is higher when the generator is operating at maximum voltage as compared to operation in low voltage. The overall efficiency of the converter can be improved by employing switching devices with lower internal resistance than the ones selected.

Table 5.3: Power losses in a single-phase tapped-coupled inductor boost converter with $V_{s,rms} = 96V$

Output power	Copper loss	Total Switch loss	Diode conduction loss	Total loss	Efficiency %
500W	3.66W	6.94W	1.49W	12.09W	97.6
750W	8.19W	11.83W	2.37W	22.39W	97.01
1000W	14.61W	16.48W	3.34W	34.43W	96.6
1250W	22.84W	21.63W	4.4W	48.87W	96.1
1500W	32.9W	27.24W	5.54W	65.58W	95.6

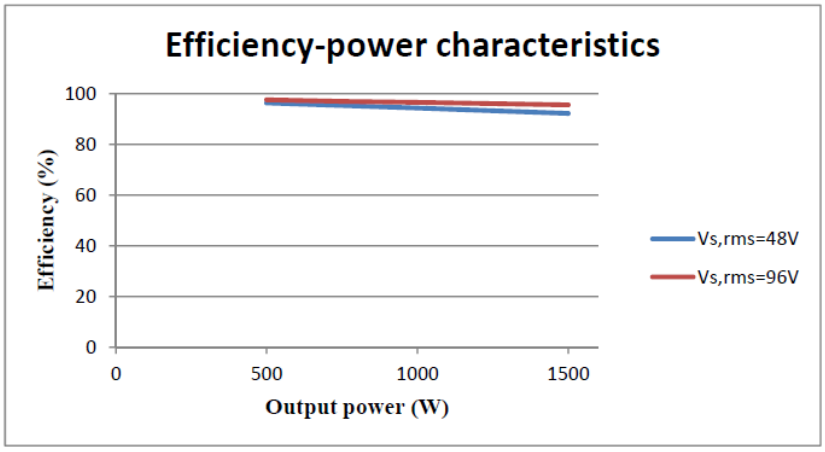

Figure 5.8: Efficiency-power characteristics of the converter

5.3 LOW VOLTAGE BATTERY INTERFACE SIMULATION RESULTS

Simulation of low voltage battery interface with the aforementioned specifications, is conducted using PSIM software. Key parameters of the interface such as output voltage and current, input rms current ripple, input peak-to-peak current, switch voltages and efficiency are plotted and their values compared with those derived from theoretical analysis. The converter is simulated in both buck and boost-mode operation to demonstrate bidirectional power flow capability. In addition, parameter waveforms are obtained for converter operation that takes into account non-ideal components. To simulate the operation of the converter with load disturbances, the system is subjected to step changes in load. Step-responses of output voltage and current are plotted.

5.3.1 Buck-mode operation

Operation of the interface in buck-mode corresponds to the charging of battery with the DC bus acting as the voltage source. Simulation waveforms are presented with a variable input voltage and output load.

5.3.1.1 Simulation waveforms for $V_{bus} = 380V$ and full load

Figures 5.9 (a) and (b) show the simulated waveforms for output voltage and current. The interface is achieves a large voltage step-down of approximately 6 times at a moderate duty cycle of 0.53 as compared to a conventional buck converter which would, ideally, achieve the same voltage gain at an extremely low duty cycle of 0.16.

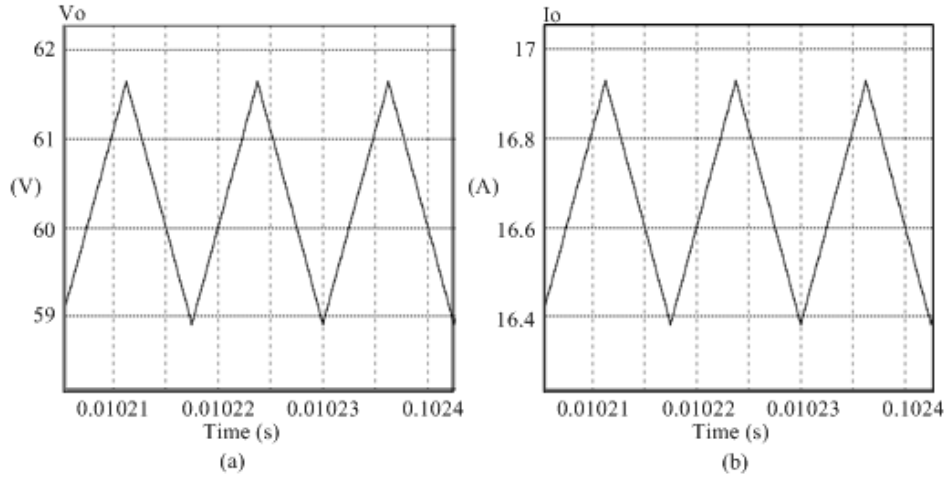

Figure 5.9: Simulated converter waveforms. (a) Output voltage and (b) Output current

Figures 5.10(a) and (b) present the input current waveforms. The peak-to-peak and RMS ripple current, in the two-phase operation, is 2.26A and 0.71A respectively, while that of single-phase operation is 4A and 2.02A respectively. This is a clear demonstration that interleaving reduces the input ripple current of the converter.

Figure 5.11(a) and (b) present the switch voltage waveforms with and without a snubber circuit. The applied passive lossless snubber circuit is able to clamp voltage spikes from the initial peak of 19000V to 1000V with no losses attributed to it.

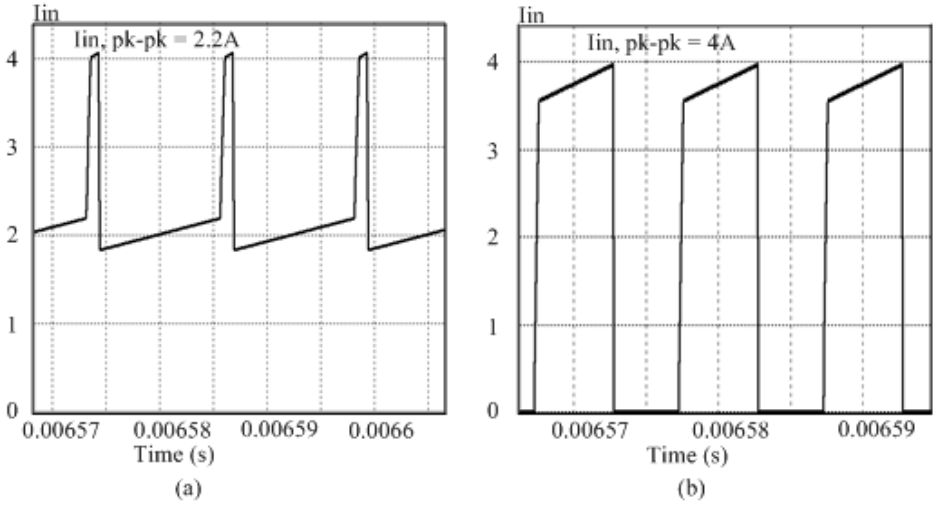

Figure 5.10: Simulated input current waveforms. (a) Two-phase and (b) single-phase operation

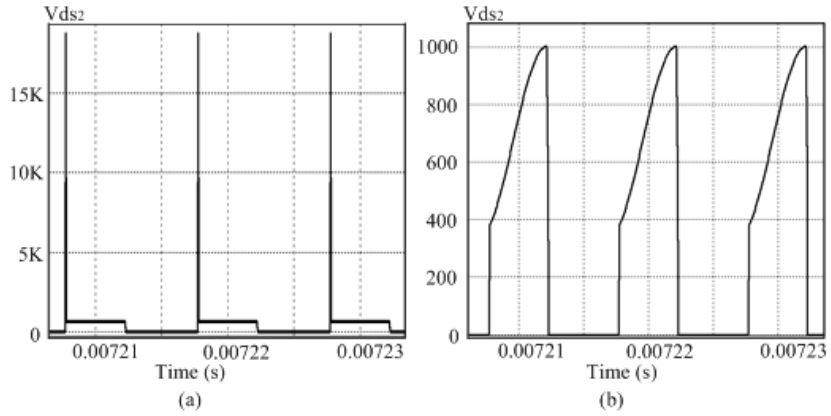

Figure 5.11: Simulated switch voltage waveforms (a) without and (b) with a snubber circuit

A comparison of parameter results obtained from simulation and those derived from theoretical analysis of the converter is presented in Table 5.4. It can be seen that the results are in good agreement with each other.

5.3.1.2 Simulation waveforms for V_{bus}= 380V and 25% step change in load

An active switch operating at 500Hz is used to introduce a step change in the output load. Figure 5.12 presents the output voltage and current waveforms. It is obserevd that introduction of a 25% decrease in load causes a 10% undershoot in the output voltage. The voltage oscillations settle down to a steady-state value of 58.4V which represents 2.7% output voltage regulation. Current transitions

Table 5.4: Performance parameters in the proposed low voltage battery interface operating in buck-mode

Parameter	**Analysis results**	**Simulation results**
Buck ratio	6.33	6.3
Input rms current $(I_{in,rms})$	2.85A	2.77A
Input rms ripple current $(I_{in,rmsripple})$	0.75A	0.76A
Input current peak-peak $(I_{in,pk-pk})$	2.2A	2.26A
Primary inductor current peak-peak $(I_{L11,pk-pk})$	2.48A	2.55A
Capacitor rms current $(I_{c,rms})$	4.3A	4.51A
Output voltage (V_o)	60V	59.5V
Average output current $(I_{o,ave})$	16.67A	16.5A

are almost instantaneous, as it is expected, and the initial current rises to 21.6A.

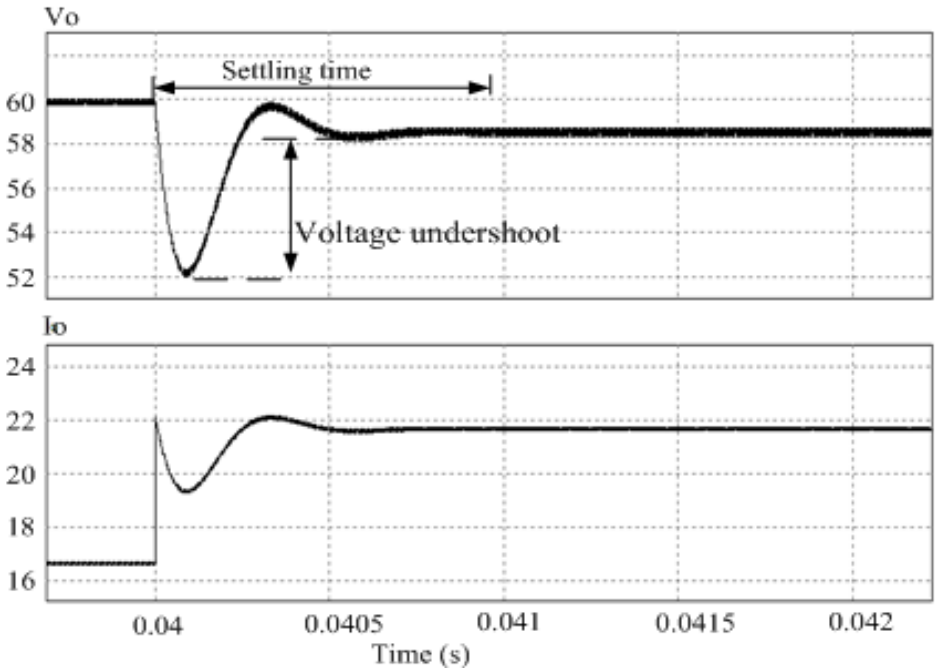

Figure 5.12: Output voltage and current waveform for 25% step change in load

5.3.1.3 Converter efficiency

The efficiency of converter interface is determined for different levels of output power. Table 5.5 presents the converter losses at the various power levels. At low power levels (less than 1000W), the highest losses are as a result of switching losses in MOSFET switches which accounts for over 50% of the total converter loss. This means that the efficiency of the converter interface can be improved by employing active switches with lower on-resistance.

Table 5.5: Power losses in a low voltage battery interface operating in buck-mode

Output power	Copper loss	Switching loss	Switch conduction loss	Total loss	Efficiency %
500W	3.26W	17.29W	5.32W	25.87W	94.8
750W	7.35W	25.1W	12.08W	44.53W	94.06
1000W	13.09W	33.03W	21.5W	67.62W	93.2
1250W	20.4W	40.83W	33.99W	95.22W	92.38
1500W	29.5W	48.7W	48.32W	126.52W	91.6

Figure 5.13 presents efficiency-power characteristics of the converter. Efficiency is high at low output power and decreases as the load is increased. The decrease in efficiency at high power levels is due to increase in the input rms and peak currents which causes increased converter losses.

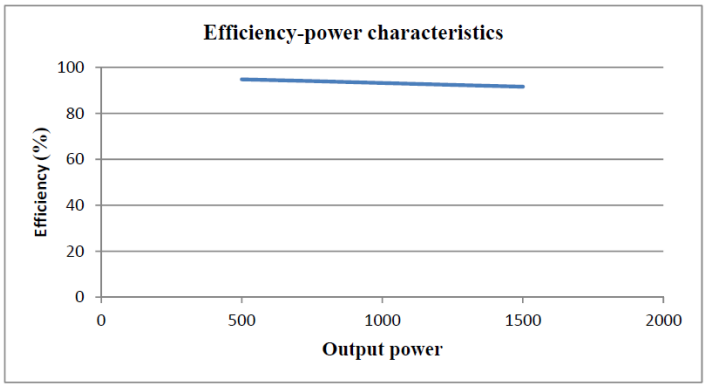

Figure 5.13: Efficiency-power characteristics of the low voltage battery interface operating in buck-mode

5.3.2 Boost-mode operation

Operation of the converter interface in boost-mode corresponds to discharging of battery to supply the DC bus. Simulation results are presented for a variable DC source as the battery charge diminishes providing voltage that is below its rated value.

5.3.2.1 Simulation waveforms for $V_{bat} = 48V$ and full load

Figures 5.14 (a) and (b) present the simulated waveforms for output voltage and current. The converter interface achieves a boost ratio of approximately 8 times at a moderate duty cycle of 0.5 as compared to a conventional boost converter which, ideally, would achieve the same voltage boost at an extremely high duty cycle of 0.87.

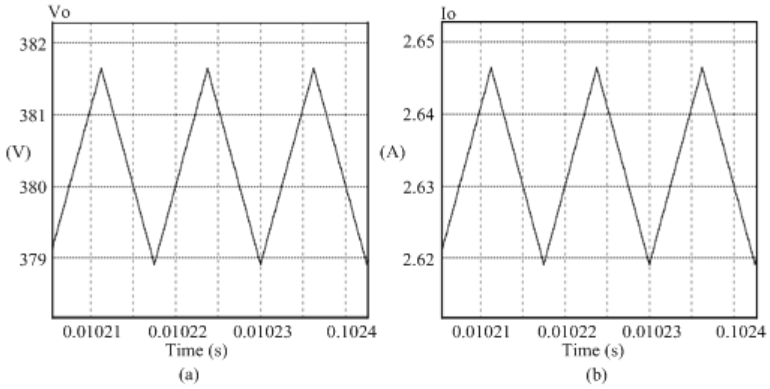

Figure 5.14: Simulated converter waveforms. (a) Output voltage and (b) Output current

Figures 5.15 (a) and (b) present the converter input current waveforms. The peak-to-peak and RMS ripple for the two-phase operation, is 17.4A and 2.97A respectively, while that of single-phase operation is 27.9A and 14.3A respectively. This is a further proof that interleaving reduces the input ripple current.

Figures 5.16 (a) and (b) present the voltage waveforms across the switch, with and without a snubber circuit. The applied passive lossless snubber circuit is able to clamp the voltage spikes from the initial peak of 1505V to 200V with no losses attributed to it.

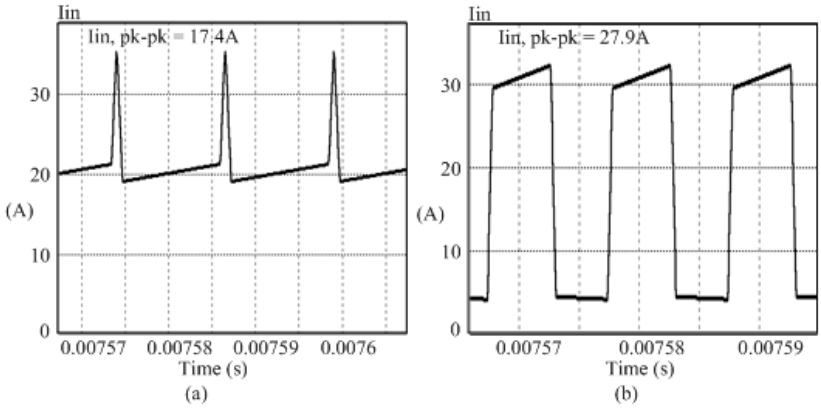

Figure 5.15: Simulated input current waveforms. (a) Two-phase and (b) single-phase converter operation

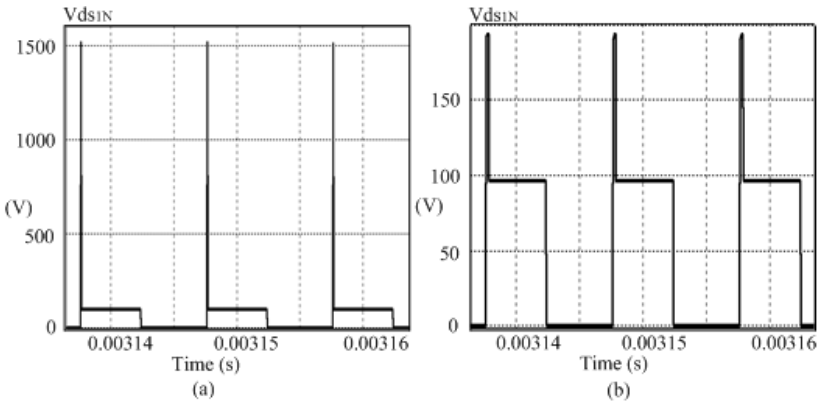

Figure 5.16: Simulated switch voltage waveforms. (a) Without and (b) with a snubber circuit

Comparison of parameter results obtained from simulation and those derived from theoretical analysis of the converter is presented in Table 5.6. There is good agreement among the results.

5.3.2.2 Simulation waveforms for $V_{bat} = 40V$ and full load

To demonstrate operation of the converter interface with a diminishing source voltage, the converter is simulated with an input voltage of 40V which represents 83% of its rated voltage. Figures 5.17(a) and (b) show the output voltage and current waveforms. An average output voltage of 380V is obtained which proves the ability of the selected controller in tracking the desired output voltage and rejecting input voltage variations.

Table 5.6: Performance parameters in the proposed low voltage battery interface operating in boost-mode

Parameter	**Analysis results**	**Simulation results**
Boost ratio	7.92	7.9
Input rms current $(I_{in,rms})$	21.8A	22.1A
Input rms ripple current $(I_{in,rmsripple})$	2.84A	2.97A
Input current peak-peak $(I_{in,pk-pk})$	17.1A	17.4A
Inductor current peak-peak $(I_{L21,pk-pk})$	18.2A	18.56A
Capacitor rms current $(I_{c,rms})$	0.4A	0.45A
Output voltage (V_o)	380V	379.9V
Average output current $(I_{o,ave})$	2.63A	2.63A

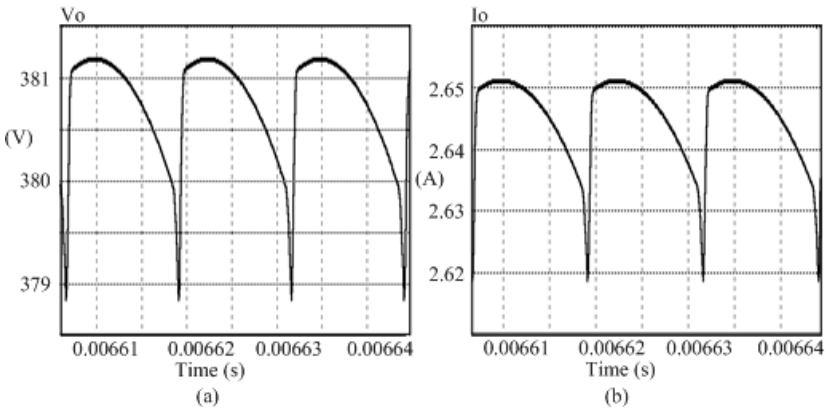

Figure 5.17: Simulated converter waveforms. (a) Output voltage and (b) current

5.3.2.3 Simulation waveforms for $V_{bat} = 48V$ and 25% step change in load

A step change in load is introduced at the output of the low voltage battery interface to simulate voltage variations on the DC bus. Figure 5.18 presents the output voltage and current waveforms. It is observed that introduction of a 25% decrease in load at the converter output causes 0.5% undershoot in the output voltage. The voltage oscillations settle down to a steady-state value of 376V which represents 1.1% output voltage regulation. Current transitions are instantaneous and the initial current rises to 2.66A.

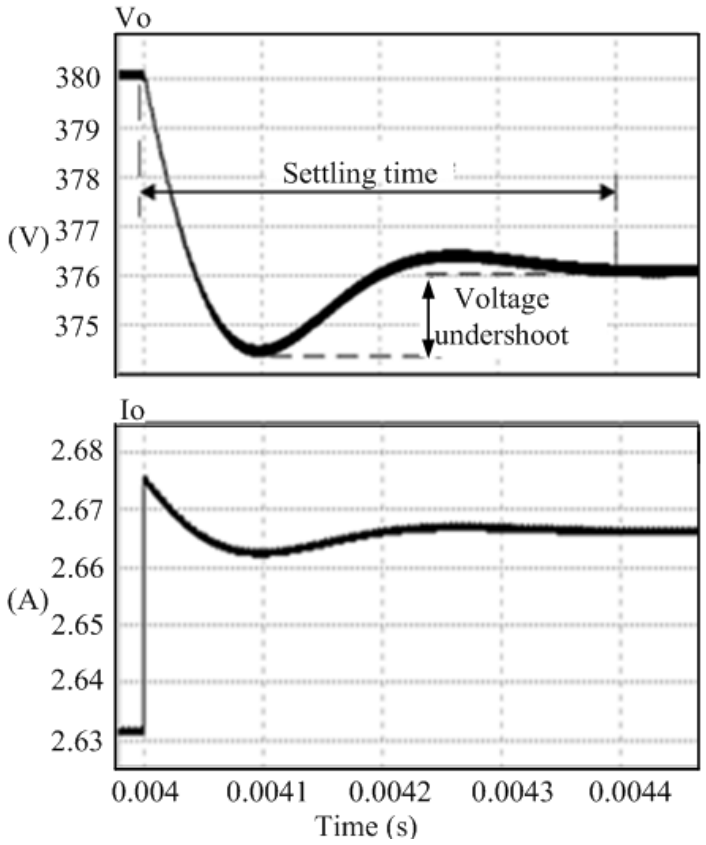

Figure 5.18: Voltage and current waveforms for a 25% step change in load

5.3.2.4 Converter efficiency

Efficiency of the converter interface is determined for different levels of output power. Table 5.7 presents the interface losses at the various levels of power.

Table 5.7: Power losses in a low voltage battery interface operating in boost-mode

Output power	Copper loss	Switching loss	Switch conduction loss	Total loss	Efficiency %
500*W*	4.39*W*	18.78*W*	7.5*W*	30.67*W*	93.9
750*W*	9.76*W*	27.3*W*	16.6*W*	53.66*W*	92.8
1000*W*	17.4*W*	35.95*W*	29.74*W*	83.09*W*	91.7
1250*W*	27.19*W*	44.6*W*	46.58*W*	118.37*W*	90.5
1500*W*	39.2*W*	53.23*W*	67.23*W*	159.66*W*	89.4

At low power levels (less than 1000W), the highest losses are as a result of switching losses in MOSFET switches which accounts for over 50% of the total converter loss. Just like in the case of buck-mode operation, efficiency of the interface can be improved by employing active switches with low on-resistance.

Figure 5.19 presents efficiency-power characteristics of the converter. Efficiency is high at low output power and decreases as the load is increased. The decrease in efficiency at high power levels is due to increase in the input rms and peak currents which causes increased converter losses.

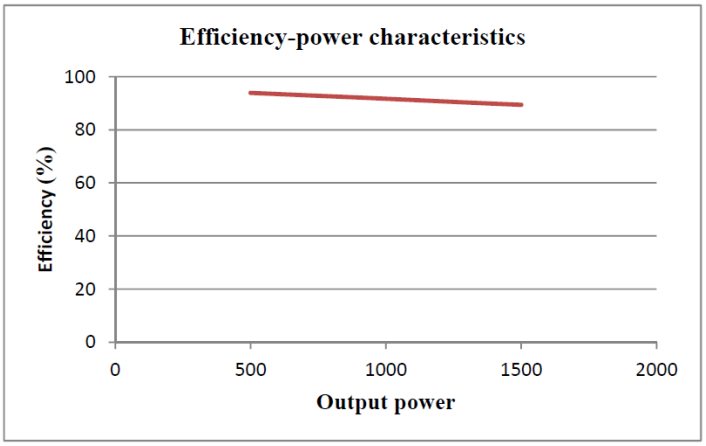

Figure 5.19: Efficiency-power characteristics of the interface in boost-mode

CHAPTER 6 SYSTEM HARDWARE DESIGN

6.1 CHAPTER OVERVIEW

In this chapter, the hardware design of the proposed low voltage DC microgrid, comprising of a small wind energy conversion system and low voltage battery interface, is presented. This design include selection and sizing of magnetic components, heat sinks and semiconductor devices.

6.2 SWEC SYSTEM SPECIFICATIONS

A 1kW prototype of the proposed SWEC interface is designed and built to confirm the hypothesis of this research. Converter output voltage is selected as 380V since it is the common voltage for DC distribution systems in data centres and telecommunication facilities.

6.2.1 Wind generator selection

An FT-1000L model of a three-phase permanent magnet synchronous generator is selected as the source voltage for the interface. This generator has the specifications shown in Table 6.1. It is observed that the output voltage varies from 48V at the lowest working speed ($3m/s$) of the generator to a maximum of 96V at the highest operational speed ($20m/s$). Hence, the duty cycle of the boost converter will have to be varied accordingly to ensure a constant output voltage.

Table 6.1: Permanent magnet synchronous generator specifications

Parameter	**Ratings**
Rated power (P_{rated})	1000W
Rated voltage (V_{rated})	48/96V
Maximum power (P_{max})	1200W
Rated wind speed ($V_{w,rated}$)	10 m/s
Start-up wind speed ($V_{w,start}$)	2.5 m/s
Working wind speed ($V_{w,working}$)	3-20 m/s
Rated rotate speed (W_r)	500 r/min

6.2.2 Diode rectifier specification

A three-phase diode rectifier is employed at the generator output to rectify the AC voltage. The rectified voltage, $V_{DC,rated}$, is given by,

$$V_{DC,rated} = 1.35 \times V_{AC} \tag{6.1}$$

where V_{AC} is the generator output voltage.

From above equation, the minimum and maximum output voltages from the diode rectifier are obtained as

$$V_{DC,rated} = 1.35 \times 48 = 65V \tag{6.2}$$

$$V_{DC,max} = 1.35 \times 96 = 130V \tag{6.3}$$

The proposed DC-DC converter is designed to boost the variable input voltage (ranging between 65V and 130V) to a constant output of 380V. A high switching frequency of 100kHz is chosen to minimise the size of converter components and ensure switching losses are minimised. In addition, a coupling coefficient, $k = 0.99$, is chosen to ensure a high voltage boost ratio.

6.2.3 Boost DC-DC converter component's selection and sizing

Hardware design of the boost DC-DC converter entail selection and sizing of active switches, tapped coupled inductors, output diodes, output capacitor, and snubber circuit components consisting of a diode and a capacitor. Sizing is only done for one phase and the results replicated to the other phase since they are identical.

6.2.3.1 Sizing of tapped-coupled inductor

The size of tapped-coupled inductor is given by,

$$L_{21} = [\frac{n(V_{in} - V_o)(1-D)T_{sw}}{(1+n)\Delta i_{L21,pk-pk}}] \tag{6.4}$$

From this equation it is seen that the size of an inductor is inversely proportional to the input current ripple. Consequently, sizing of the tapped-coupled inductor is done in such a way that minimises the input current ripple. In this research, an inductor current ripple equal to 20% of the average output current is chosen when sizing the inductor. Small ripple causes minimal core loss and ensures that the converter operates in a continuous conduction mode (CCM).

$$\Delta i_{L21,pk-pk} = 20\% \times I_o \tag{6.5}$$

From equation (3.18), it was found out that the output and input voltage are related by the following expression, assuming ideal components,

$$\frac{V_o}{V_{in}} = \frac{(1+nkD)}{(1-D)} \tag{6.6}$$

Considering the converter specifications: $V_{in} = 65 - 130V$, $V_o = 380V$, $n = 3$, $f_{sw} = 100kHz$ and $P_o = 1000W$, then the range of allowable duty cycle is obtained as,

$$D = \frac{(V_o - V_{in})}{(V_o + nkV_{in})} = 0.55, 0.33 \tag{6.7}$$

For the lowest speed operation of the wind turbine generator, a duty cycle, $D = 0.55$ will be considered. This duty cycle is also found to provide the lowest ripple in a two-phase tapped-coupled inductor boost converter. Consequently, the size of secondary-side inductor is obtained from equation (6.4) as

$$L_{21} = 2.02mH, \tag{6.8}$$

The relationship between the input- and output-side inductance is given by,

$$\frac{L_{21}}{L_{11}} = \left(\frac{N_{2N}}{N_{1N}}^2\right) = n^2 \tag{6.9}$$

where n is the turns ratio.

For $n = 3$, the primary-side inductor is obtained as,

$$L_{1N} = \frac{2.02mH}{3^2} = 224\mu H \tag{6.10}$$

The mutual inductance for a coupling coefficient, $k = 0.99$, is obtained as,

$$M = k \times \sqrt{(L_{1N} \times L_{2N})} = 666.7\mu H \tag{6.11}$$

6.2.3.2 Tapped-coupled inductor hardware design

This section outlines the procedure for hardware design of a tapped-coupled inductor so that it can meet a set of electrical and thermal specifications: $L_{1N} = 224\mu H$, $L_{2N} = 2.02mH$, $f_{sw} = 100kHz$ and $T = 100°C$.

$\hat{I}_{L1N} = 23.87A$, $I_{L1N,ave} = 15.39A$, $I_{L1N,rms} = 17.65A$, $\hat{I}_{L2N} = 6.06A$, $I_{L2N,ave} = 2.63$ and $I_{L2N,rms} = 3.02A$ are obtained from equations (3.28) to (3.39)

Step 1: Stored energy computation

Inductors are known to store energy in magnetic fields. The inductance of a coil is given by

$$L = \frac{N\phi}{i} \tag{6.12}$$

From the above equation, an expression that relates the design inputs of an inductor to the product of material parameters and geometric parameters of the core and winding is obtained [36]

$$L\hat{I}_L I_{L,rms} = k_{cu} J_{rms} \hat{B} A_w A_{core} \tag{6.13}$$

where L is inductance, $\hat{I}_L$ is peak inductor current, $I_{L,rms}$ is the rms inductor current, k_{cu} is the copper fill factor, J_{rms} is the current density, $\hat{B}$ is peak flux density, A_w is the winding area and A_{core} is the core area.

From equation (6.13), the stored energy in each of the inductor is calculated as

$$L_{1N}\hat{I}_{L1N}I_{L1N,rms} = (224\mu H)\times(23.87)\times(17.65) = 0.0945H - A^2 \tag{6.14}$$

$$L_{2N}\hat{I}_{L2N}I_{L2N,rms} = (2.02mH)\times(6.06)\times(3.02) = 0.037H - A^2 \tag{6.15}$$

Since the two inductors are coupled, the total stored energy is obtained as

$$L\hat{I}_L I_{L,rms} = 0.0945 + 0.037 = 0.132H - A^2 \tag{6.16}$$

Step 2: Core material, shape and size selection

The choice of core material is influenced by the converter operating frequency. In this research, a ferrite material is chosen for its high resistivity at the selected 100kHz switching frequency. As a result, problems of skin effect and eddy current loss are suppressed. The choice made for the shape of core is a double E-core shown in figure 6.1. This core shape has a low cost, simple assembly, excellent heat dissipation and is easier to make windings on. Combination of the core dimensions d, h, and b, is optimised by the manufacturer to ensure the lowest total volume and cost for a given rating [36].

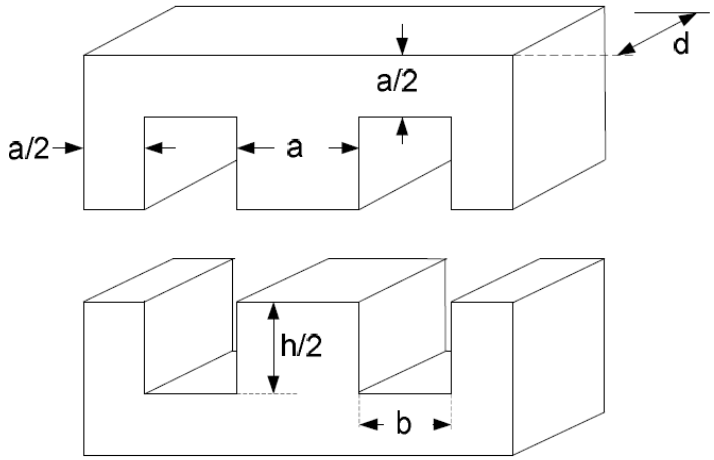

Figure 6.1: Double E-core

An N27 ferrite inductor core with a power dissipation, P_{sp} due to losses of $600kW/m^3$ at $100kHz$, flux density of $0.16T$ and operating temperature of $100°C$ was selected. Power dissipated per unit of copper winding volume is given by [36]

$$P_{sp} = k_{cu}\rho_{cu}\frac{R_{ac}}{R_{dc}}j_{rms}^2 \tag{6.17}$$

where R_{dc} is the DC resistance of the winding and R_{ac} is the AC resistance of the winding.

For a DC inductor,

$$\frac{R_{ac}}{R_{dc}} \approx 1 \tag{6.18}$$

The resistivity of copper at $100°C$ is 2.2×10^{-8}. The current density can then be obtained from equation (6.17) as

$$J_{rms} = \left(\frac{P_{sp}}{\rho \times k_{cu}}\right)^{\frac{1}{2}} = \sqrt{\frac{600kW}{2.2 \times 10^{-8} \times 0.3}} = 9.53A/mm^2 \tag{6.19}$$

An E65/32/27 core was determined to be the most suitable choice forn an inductor to satisfy the condition set above. This core has a winding area $(A_w) = 537.24mm^2$ and a core area (A_c) $529mm^2$. The peak flux density, B_{pk}, was chosen as $0.16Tesla$ which is less than the saturation flux (0.41T) of the N27 material. Consequently, the energy stored in the core can be computed as,

$$k_{cu} j_{rms} \hat{B} A_w A_{core} = 0.3 \times 9.53A/mm^2 \times 0.16 \times 537.24mm^2 \times 529mm^2 = 0.13H - A \tag{6.20}$$

This value is equal to the total stored energy obtained in equation (6.16). Hence the selected core can effectively handle the stored energy in the coupled inductors.

Step 3:Winding parameter specification

Conductor winding in the tapped-coupled inductor is made from copper because of its high conductivity and ductility which makes it easier to bend the conductors into tight windings around the magnetic core. In addition, a stranded copper conductor with a k_{cu} of 0.3 is selected because of its low eddy current loss at high frequencies. The relationship between copper conductor area and the current density is given by

$$A_{cu} = \frac{I_{rms}}{j_{rms}} \tag{6.21}$$

The conductor areas for each inductor are obtained from above equation as,

$$A_{cu1N} = \frac{17.65}{9.53} = 1.85mm^2 \tag{6.22}$$

$$A_{cu2N} = \frac{3.02}{9.53} = 0.32mm^2 \tag{6.23}$$

Step 4: Skin depth determination

Skin effect is the tendency of current carried by the copper conductor to be constricted to a relatively thin layer at the surface. It occurs when the cross-sectional dimensions of conductor used in the winding is significantly larger than the skin depth. Consequently, the effective resistance of the conductor is far larger than DC resistance since the effective cross-sectional area for current flow is small as compared to the geometric cross section of conductor. The skin depth of the copper conductor at a frequency of 100kHz is determined as,

$$\delta = \sqrt{\frac{\rho}{\pi \times \mu \times f}} = \sqrt{\frac{2.2 \times 10^{-8}}{\pi \times 100kHz \times 4\pi \times 10^{-7}}} = 0.2mm \tag{6.24}$$

Calculations have shown that if diameter of the winding conductor, $d < 2\delta$, then the consequences of skin effect can be neglected.

$$2 \times \delta = 0.4mm \tag{6.25}$$

The diameter of both the copper windings is obtained from equations (6.22) and (6.23) as $d_1 = 1.53mm$ and $d_2 = 0.635mm$. Since these diameters are greater than two times the skin depth, there is need to use stranded copper conductors so that their cross-sectional dimensions is of the order of skin depth in size. For both the primary and secondary inductors, a copper winding with a diameter of 0.41mm is chosen. This winding has a resistance of $0.169\Omega/m$ as indicated on the American Wire Gauge Data, AWG No. 27 [37]. Consequently, the number of strands in primary winding is obtained as,

$$N_{1N,strands} = \frac{A_{cu1N}}{\pi \times \delta^2} = \frac{1.85}{\pi \times 0.205^2} \approx 14 \tag{6.26}$$

Similarly, the number of strands needed in the secondary winding is obtained as,

$$N_{2N,strands} = \frac{A_{cu2N}}{\pi \times \delta^2} = \frac{0.32}{\pi \times 0.205^2} \approx 2 \tag{6.27}$$

Step 5: Air gap determination

When a coil is wound without an airgap, inductance is very large which should result in higher amount of energy storage. However, flow of current in a core that does not have an airgap is very small. Since the stored energy in an inductor is proportional to the square of current, then only a small current would flow before the core goes into saturation resulting in little energy storage. Therefore, an airgap

must be included on the centre limb of the ferrite E-core for more energy storage. The length of airgap is given by [37]

$$l_g = \frac{\mu_o \times L_{11} \times I_{avg}^2}{A_c \times B_{max}^2} \tag{6.28}$$

Therefore,

$$l_g = \frac{4\pi \times 10^{-7} \times 224 \times 10^{-6} \times 15.39^2}{529 \times 10^{-6} \times 0.16^2} = 4.9mm \tag{6.29}$$

Step 6: Number of turns determination

The selected double E-core has the following dimensions: a=20mm, b=12.1mm, d=26.4mm and h=44.4mm. Consequently, the mean length of flux is obtained from figure 6.1 as

$$l_m = 2 \times (b+h) + 2.5a = 163mm \tag{6.30}$$

The mean length of one turn, MLT, is given by,

$$MLT = 4b + 2 \times (a+d) = 141.2mm \tag{6.31}$$

The relative permeability of the selected core is $\mu_r = 2000$ at $100kHz$, $100°C$ and $0.2T$ operation. The total reluctance, R_{tot} is hence obtained as

$$R_{tot} = \frac{l_m}{\mu_r \mu_o A_c} + \frac{l_g}{\mu_o A_c} = \left(\frac{0.163}{2000 \times 4\pi \times 10^{-7} \times 529 \times 10^{-6}}\right) + \left(\frac{4.9 \times 10^{-3}}{4\pi \times 10^{-7} \times 529 \times 10^{-6}}\right) \tag{6.32}$$

$$R_{tot} = 7.49 \times 10^6 turns/wb$$

The number of turns for inductor, L_{1N} is given by,

$$N_{L1N} = \sqrt{L_{1N} \times R_{tot}} = \sqrt{224\mu \times 7.49 \times 10^6} = 40.9turns \tag{6.33}$$

The number of turns on inductor L_{1N} was chosen as 41 turns. Consequently, the number of turns on the second inductor, L_{2N} is obtained as,

$$n = \frac{N_{L2N}}{N_{L1N}} = 3 \tag{6.34}$$

$$N_{L2N} = 3 \times 41 \approx 123turns$$

Step 7: Winding resistance determination

The winding resistance is given by [37],

$$r_L = \frac{MLT \times N_L \times R_{AWG}}{N_{L,strands}} \tag{6.35}$$

From the American Wire Gauge table, copper conductor used in the inductor has a resistance, $R_{AWG} = 0.169\Omega/m$. The winding resistances are thus obtained as

$$r_{L11} = \frac{0.141 \times 41 \times 0.169}{14} = 0.07\Omega \tag{6.36}$$

$$r_{L21} = \frac{0.141 \times 123 \times 0.169}{2} = 1.5\Omega \tag{6.37}$$

6.2.3.3 Power loss in inductor windings

Power loss in the inductor winding is occasioned by conductor resistance, r_L. Therefore, in the primary inductor, L_{1N}, power loss is obtained as,

$$P_{L1N} = r_{L1N} \times {I_{L1N,avg}}^2 = 0.07 \times 15.39^2 = 16.58W \tag{6.38}$$

Similarly, the power loss in the secondary inductor, L_{2N} is obtained as,

$$P_{L2N} = r_{L2N} \times {I_{L2N,avg}}^2 = 1.5 \times 2.63^2 = 10.38W \tag{6.39}$$

The total power loss across the coupled-inductor is obtained as,

$$P_{N,tot} = P_{L1N} + P_{L2N} = 16.58W + 10.38W = 26.96W \tag{6.40}$$

6.2.3.4 Active switch selection

A MOSFET device is selected as the suitable choice of an active switch because of its ease of use in high switching frequency. It also demands a simple gate drive because its control electrode is isolated from the current conducting silicon, hence a continuous ON current is not required [38]. The size of MOSFET switch is determined by the amount of voltage that the switch can block when it is not conducting. From figure 3.3, this voltage is given by,

$$V_{ds} = \frac{V_{in}(nk + n^2) + [V_o + V_{fwd} + I_L(r_{L1} + r_{L2})](1 + nk)}{1 + 2nk + n^2} \tag{6.41}$$

From the converter specifications: $n = 3, k = 0.99, r_{L1N} = 0.07\Omega, r_{L2N} = 1.5\Omega, V_{in} = 65V, V_o = 380V P_o = 1000W$ and $f_{sw} = 100kHz$, the switch blocking voltage is obtained as,

$$V_{ds} = \frac{65(3\times0.99+3^2)+[380+1.5+15.39(0.07+1.5)](1+3\times0.99)}{1+2\times3\times0.99+3^2} = 145.15V \tag{6.42}$$

The switch RMS and peak current are obtained as,

$$I_{ds,rms} = \sqrt{[(\frac{(1+nk)I_0}{2(1-D)})^2 \times D(1+\frac{1}{3}(\frac{\Delta i_{L1,pk-pk}}{(\frac{I_o(1+nk)}{2(1-D)})})^2)]} = 17.2A \tag{6.43}$$

$$I_{ds,pk} = \frac{I_o(1+nk)}{(1-D)} + \frac{1}{2}(\frac{[V_{in}-I_{L11}(r_{ds,on}+r_{L11})]DT_{sw}}{L_{11}}) = 23.64A \tag{6.44}$$

6.2.3.5 Snubber circuit design

Leakage inductance due to imperfect coupling of the tapped-inductor causes huge voltage spikes across the switch as shown in figure 6.3(a). There is need to employ a snubber circuit in the interface. A regenerative snubber circuit offers the best solution in suppressing the switch voltage spikes since it is lossless and does not modify the original topology of the converter. It consists of clamp capacitor, C_{CN} and a diode D_{CN} as shown in figure 6.2. The leakage energy is stored in the clamp capacitor and hence the snubber limits the voltage stress of the switch to its minimum [39].

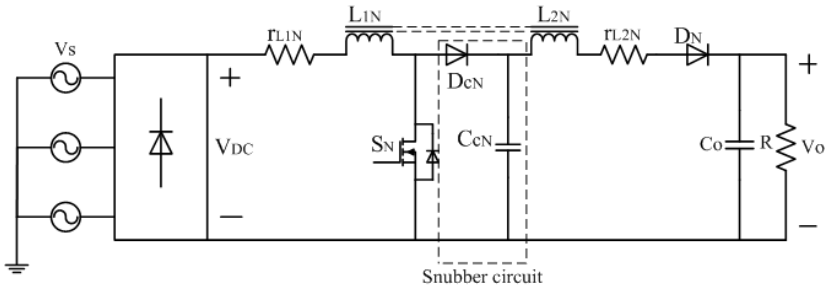

Figure 6.2: SWECS with passive lossless snubber

When the switch, S_N, is conducting, both the clamp and output diode are reverse biased and hence no current flows in the output-side inductor. Meanwhile, the coupled-inductor gets charged. When S_N, is turned off, the energy stored in leakage inductance is discharged into the clamp capacitor C_{CN}, while primary current is transferred to the secondary-side via the forward-biased diode, D_N. The magnitude of the clamp voltage, V_{CN}, is given by,

$$V_{CN} = \frac{N_{1N}V_o + N_{2N}V_{in}}{N_{1N}+N_{2N}} = \frac{30\times380+90\times65}{30+90} = 143.75V \tag{6.45}$$

The size of the clamp capacitor is obtained as,

$$C_{CN} = \frac{I_c \times D \times T_s w}{V_{c,pk-pk} \times} = \frac{1.2 \times 0.55}{0.0125 \times 143.75 \times 100kHz} = 3.67\mu F \tag{6.46}$$

Consequently, a capacitor rated at$3.67\mu F$, $300V$ is selected.

The new switch blocking voltage waveform with a passive lossless snubber circuit deployed in the converter is shown in figure 6.3(b). The voltage spike has reduced significantly from the initial peak of $1800V$ to $150V$. Consequently, an N-channel MOSFET Transistor, IRFI4229PBF, rated at $V_{dss} = 250V$,$I_{ds} = 25A$ and $r_{ds(on)} = 47m\Omega$ is selected for this application [40].

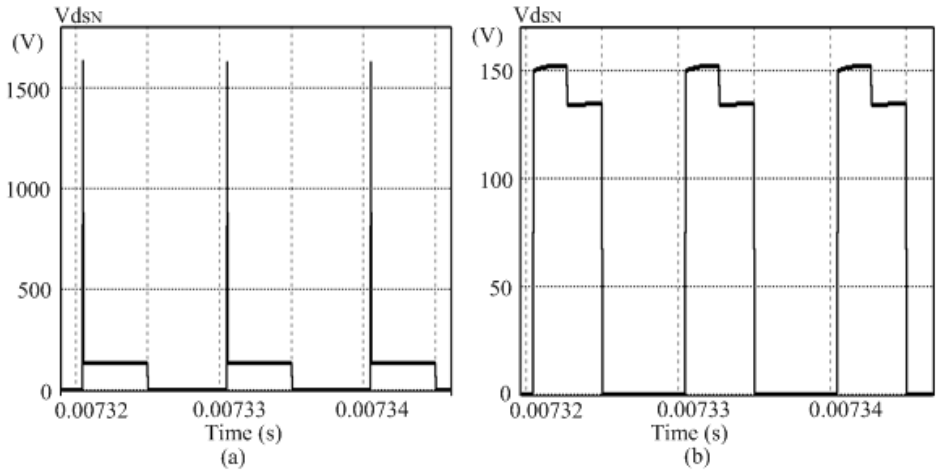

Figure 6.3: Active switch voltage waveforms (a) without and (b) with snubber circuit

6.2.3.6 Switch power losses

The total power loss in the selected MOSFET is occasioned by switching and conduction losses.

$$P_{tot} = P_{sw} + P_{cond} \tag{6.47}$$

Switching loss, P_{sw}, is given by

$$P_{sw} = 0.5 \times V_{ds} \times I_{ds,pk} \times (t_{ri} + t_{ds,on} + t_{rv} + t_{ds,off}) \times f_{sw} \tag{6.48}$$

where: $V_{ds}$is voltage blocked by the switch, I_{ds} is current passing through the switch, t_{ri} is current rise time, $t_{ds,on}$ is on-time of the switch, t_{rv} is voltage rise time and $t_{ds,off}$ is off time.

From the specifications of the power MOSFET stated on the datasheet, switching power loss is obtained as

$$P_{sw} = 0.5 \times 145.15 \times 23.64 \times 80ns \times 100kHz = 13.47W \tag{6.49}$$

Similarly, conduction loss, P_{cond}, in the switch is given by

$$P_{cond} = V_{on} \times I_{ds} \times D = (I_{ds,rms})^2 \times r_{ds,on} \tag{6.50}$$

where: $I_{ds,rms}$ is RMS current passing through the switch and $r_{ds,on}$ is on-state resistance of the switch.

From the specifications of the switch, conduction loss is obtained as

$$P_{cond} = 17.2^2 \times 0.047 = 13.9W \tag{6.51}$$

The total power loss, P_{tot} in the selected switch is obtained by summing up the switching and conduction losses.

$$P_{tot} = 13.47 + 13.9W = 27.39W \tag{6.52}$$

6.2.3.7 Thermal management

Power MOSFETs generate excessive heat when operated at high currents and frequency and hence they require thermal management to improve reliability and protect them from damage. Heat sink is one of the component that is employed in switching converters to dissipate heat to the ambient, thus cooling the switches. Sizing of heat sink is dependent on the maximum allowable junction temperature, $T_{j,max}$ of the device, ambient temperature, T_a and total power losses, P_{tot} of the MOSFET. An expression that gives the relation between these thermal parameters is given as [36],

$$R_{\theta,sa} = \frac{T_{j,max} - T_a}{P_{tot}} - (R_{\theta,jc} - R_{\theta,cs}) \tag{6.53}$$

where $R_{\theta,sa}$ is the sink-to-ambient thermal resistance, $R_{\theta,jc}$ is the junction-to-case thermal resistance and $R_{\theta,cs}$ is the case-to-sink thermal resistance.

$R_{\theta,jc}$ and $R_{\theta,cs}$ are obtained from MOSFET datasheet. Hence for the selected switch, the required size of heat sink is obtianed as

$$R_{\theta,sa} = \frac{150-70}{27.39} - (0.24+0.5) = 2.18°C/W \tag{6.54}$$

A heat sink with a thermal resistance of $2.1°C/W$ is chosen.

6.2.3.8 Output diode selection

The magnitude of voltage across the output diode when the active switch is conducting is determined in order to size the diode. Based on figure 3.2,

$$V_D = -(I_{ds}r_{ds,on} + nk(V_{in} - I_{L11}(r_{ds,on} + r_{L11})) + V_o) \tag{6.55}$$

From the converter specifications the magnitude of diode blocking voltage, V_D, is obtained as,

$$V_D = -(8.6 \times 0.047 + 3 \times 0.99(65 - 13.25(0.047 + 0.029)) + 380) = -446.9V \tag{6.56}$$

The diode RMS and peak current is given by,

$$I_{ds,rms} = \sqrt{[(\frac{I_o}{(1-D)})^2 \times (1-D)(1 + \frac{1}{3}(\frac{\Delta i_{L21,pk-pk}}{(\frac{I_o}{(1-D)})})^2)]} = 3.92A \tag{6.57}$$

$$I_{D,pk} = \frac{I_o}{(1-D)} + \frac{1}{2}(\frac{n[V_{in} - V_o - V_{fwd} - I_{L21}(r_{L11} + r_{L21})](1-D)T_{sw}}{(1+n)L_{21}}) = 6.1A \tag{6.58}$$

Considering a safety margin of 1.5, a RHRP15120 hyperfast diode with a rating of $6A$ and $1000V$ was chosen [41]. This diode has a forward voltage drop of $V_{fwd} = 1.5V$ and a forward resistance of $R_{fwd} = 150m\Omega$. It has a low stored charge and fast recovery time which minimises ringing and electrical noise in switching circuits.

6.2.3.9 Diode power losses

Conduction losses in a diode are caused by forward voltage drop, V_{fwd}, and forward resistance, R_{fwd}.

$$P_{cond} = P_{V,fwd} + P_{R,fwd} \tag{6.59}$$

Diode loss due to V_{fwd} is obtained as,

$$P_{V,fwd} = (1-D) \times V_{fwd} \times I_o = (1-0.55) \times 1.5 \times 2.63 = 1.78W \tag{6.60}$$

Diode loss due to R_{fwd} is obtained as,

$$P_{R,fwd} = (1-D) \times R_{fwd} \times {I_o}^2 = (1-0.55) \times 0.15 \times 2.63^2 = 0.47W \tag{6.61}$$

Consequently, the total conduction losses is obtained from equation (5.59) as,

$$P_{cond} = 1.78W + 0.47W = 2.25W \tag{6.62}$$

6.2.3.10 Output Capacitor

The size of output capacitor is determined by considering an output voltage ripple equal to 1.25% of the capacitor voltage. Hence,

$$C_o = \frac{I_o \times D \times T_{sw}}{\Delta V_{c,pk-pk}} = 3.05\mu F \tag{6.63}$$

Considering a safety margin of 1.25 for the capacitor voltage, a $5\mu F$, $450V$ capacitor was selected. The slightly higher voltage rating compared to the load voltage is meant to caution the capacitor against voltage overshoots following step changes in load.

6.2.3.11 Switch gate drive

The simplest way to drive the MOSFET switch gate is to utilize the output signal from PWM controller. However, the output signal from this controller is often limited to a few milliamperes of current. Since the switching time of a MOSFET is inversely proportional to the amount of current used to charge the gate, then a switch which is directly driven by such a signal would respond very slowly. Consequently, the switch suffers from high power losses and overheating which can lead to permanent damage of the circuit

A switch gate driver serves to control the switching ON and OFF of the MOSFET switch. It receives the often low-power input from a PWM controller and produces an appropriate high-current gate drive signal for the MOSFET switch. HCPL-3120 gate drive optocoupler is chosen in this research work. This gate driver has a wide voltage operating range $(15-30V)$ and switching speeds of $500ns$ [42]. Its internal construction is shown in figure 6.4.

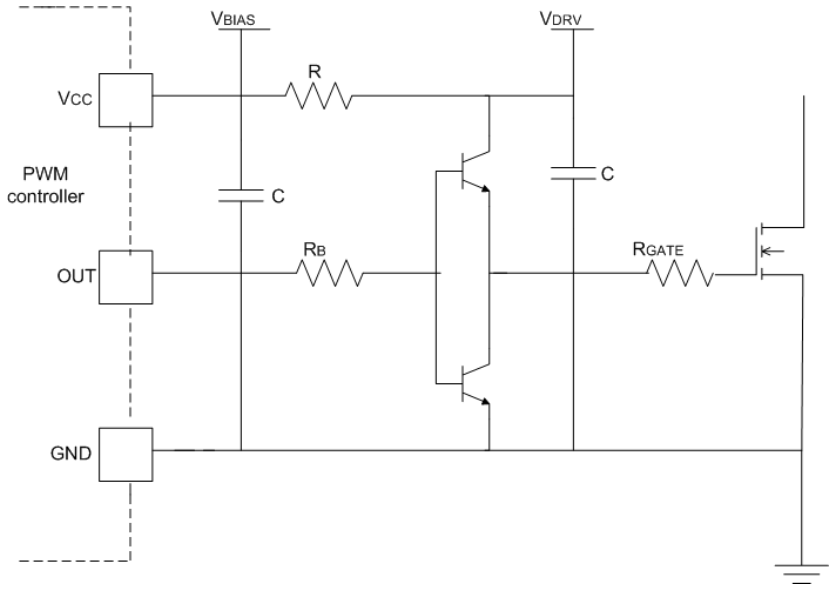

Figure 6.4: Bipolar totem-pole MOSFET driver

Sizing of the gate resistor, R_{GATE} is done in such a way that the maximum peak output current rating, $I_{OL,peak}$, of the gate driver is not exceeded.

$$R_{GATE} > \frac{V_{CC} - V_{EE} - V_{OL}}{I_{OL,peak}} \tag{6.64}$$

where: V_{OL} is the low-level output voltage of the gate driver and $I_{OL,peak}$ is the maximum peak output current.

The rated V_{OL} is obtained as 3.8V for a $I_{OL,peak}$ of 2.5A. Consequently, the size of gate drive resistor is obtained as

$$R_{GATE} > \frac{15V - 0 - 3.8V}{2.5A} = 4.48\Omega \tag{6.65}$$

6.2.4 Converter efficiency

The efficiency of the converter is given by the following expression,

$$Efficiency(\eta) = 1 - \frac{Total losses}{Output power} \tag{6.66}$$

The total converter losses comprises of MOSFET switching and conduction losses, diode conduction losses and the coupled-inductor copper losses. These losses were calculated in the previous sections and are presented in Table 6.2.

Table 6.2: Power losses in the proposed SWECS

Output power	**Copper loss**	**Total Switch loss**	**Diode conduction loss**	**Total loss**	**Efficiency** %
1000W	26.96W	27.39W	2.25W	56.6W	94.34

6.3 LOW VOLTAGE BATTERY INTERFACE HARDWARE DESIGN

A 1kW prototype of a low voltage battery interface is designed and built to confirm the hypothesis of this research. A 48V lead-acid battery is selected as the choice of energy storage owing to its low cost and and high efficiency for low power densities. It can also withstand a depth discharge of 75% and have long cyclic life of 1000-2000 cycles. Charging of the battery will be done at 60V in order to hasten the charging process.

6.3.1 Converter component's selection and sizing

The low voltage battery interface is designed to step down voltage from 380V to 60V to charge the battery. The interface also operates in boost-mode to step-up the battery voltage and feed a DC bus. A turn ratio, $n = 6$ is selected in tapped-coupled inductor to achieve large voltage gain at moderate duty-cycles. Switching frequency is chosen as 100kHz while coupling coefficient is chosen as 0.99. The components to be sized include active switches, tapped coupled inductors, output diodes and output capacitor. Since the components in each phase are identical, sizing is only done for one phase and the results replicated in the other phase.

6.3.1.1 Tapped-coupled inductor sizing

In buck-mode converter operation, the size of tapped-coupled inductor is given by,

$$L_{2N} = [\frac{(V_{bus} - V_{bat})D_1 T_{sw}}{n\Delta i_{L2N,pk-pk}}] \tag{6.67}$$

In boost-mode converter operation, the size of tapped-coupled inductor is given by,

$$L_{2N} = [\frac{V_{bat} D_2 T_{sw}}{\Delta i_{L2N,pk-pk}}] \tag{6.68}$$

An inductor current ripple equal to 20% of the average output current is considered to minimise the inductor size and to ensure that inductor current does not get discontinuous.

$$\Delta i_{L2N,pk-pk} = 20\% \times I_{o,avg} \tag{6.69}$$

For the low voltage battery interface operating in buck-mode, the input and output voltages are related by the following expression, assuming ideal components,

$$\frac{V_{bat}}{V_{bus}} = \frac{D_1}{\{D_1 + nk(1-D_1)\}} \tag{6.70}$$

Similarly, the relation between the input and output voltages for the interface operating in boost-mode is given by,

$$\frac{V_{bus}}{V_{bat}} = (\frac{1+nkD_2}{1-D_2}) \tag{6.71}$$

From equation (6.70) and (6.71), the required duty-cycles are obtained as $D_1 = 0.53$ and $D_2 = 0.5$ for buck- and boost-mode operation respectively. The size of the secondary-side inductance, L_{2N} is then obtained from equation (6.67) and (6.68) as

$$L_{2N} = 84.8\mu H, 78.3\mu H$$

However, since the same tapped-coupled inductor is employed in both buck and boost-mode operation of the interface, then an inductor of $84.8\mu H$ is employed for the worst case scenario.

The relation between the input- and output-side inductance for the interface operating in buck-mode is given by,

$$n^2 = 1 + (\frac{N_{1N}}{N_{2N}})^2 = 1 + \frac{L_{1N}}{L_{2N}} \tag{6.72}$$

Hence, the input side inductance, L_{1N}, is obtained as,

$$L_{1N} = 84.8\mu H \times 35 = 2.97mH \tag{6.73}$$

The mutual inductance for a coupling coefficient, $k = 0.99$, is obtained as,

$$M = k \times \sqrt{(L_{1N} \times L_{2N})} = 496.7\mu H \tag{6.74}$$

6.3.1.2 Magnetic design of the tapped-coupled inductor

The procedure that was previously employed in the design of tapped-coupled inductor in SWECS is also adopted in this case.

Step 1: Design inputs

The tapped-coupled inductor is designed for the following parameters: $L_{1N} = 2.97mH$, $L_{2N} = 84.8\mu H$, $I_{L1N,avg} = 2.66A$, $\hat{I}_{L1N} = 5.26A$, $I_{L1N,rms} = 3.65A$, $\hat{I}_{L2N} = 31.48A$, $I_{L2N,avg} = 16.67A$, $I_{L2N,rms} = 20.75A$, $f_{sw} = 100kHz$ and operating temperature of $T = 100°C$.

Step 2: Stored energy computation

The expression that relates design inputs of an inductor to the product of material parameters and geometric parameters of the core and winding was previously identified as

$$L\hat{I}_L I_{L,rms} = k_{cu} J_{rms} \hat{B} A_w A_{core} \tag{6.75}$$

where L is inductance, $\hat{I}_L$ is peak inductor current, $I_{L,rms}$ is the rms inductor current, k_{cu} is the copper fill factor, J_{rms} is the current density, $\hat{B}$ is peak flux density, A_w is the winding area and A_{core} is the core area.

From equation (6.75), the stored energy in each inductor is calculated as

$$L_{1N}\hat{I}_{L1N}I_{L1N,rms} = (2.97mH) \times (5.26) \times (3.65) = 0.057H - A^2 \tag{6.76}$$

$$L_{2N}\hat{I}_{L2N}I_{L2N,rms} = (84.8\mu H) \times (31.48) \times (20.75) = 0.0554H - A^2 \tag{6.77}$$

Since the two inductors are coupled, the total stored energy is obtained as

$$L\hat{I}_L I_{L,rms} = 0.057 + 0.0554 = 0.112H - A^2 \tag{6.78}$$

Step 3: Core material, shape and size selection

An E65/32/27 double E-core made of ferrite N27 material is chosen for the inductor core due to its high resistivity at high frequency. It has a maximum power dissipation, P_{sp} due to losses of $600kW/m^3$ at $100kHz$, $0.16T$ and $100°C$. From the listed core dimension: $a = 20mm$, $b = 12.1mm$, $h = 44.4mm$ and $d = 26.4mm$, the effective winding area, A_w and core area, A_{core} is obtained as,

$$A_w = b \times h = 537.24mm^2 \tag{6.79}$$

$$A_c = a \times d = 529mm^2 \tag{6.80}$$

Current density is obtained as

$$J_{rms} = \left(\frac{P_{sp}}{\rho \times k_{cu}}\right)^{\frac{1}{2}} = \sqrt{\frac{600kW}{2.2 \times 10^{-8} \times 0.3}} = 9.53A/mm^2 \tag{6.81}$$

The peak flux density, B_{pk}, is chosen as $0.16Tesla$ which is less than the saturation flux of N27 ferrite material. Hence the energy stored in the selected core is obtained as

$$k_{cu} j_{rms} \hat{B} A_w A_{core} = 0.3 \times 9.53A/mm^2 \times 0.16 \times 537.24mm^2 \times 529mm^2 = 0.13H - A \tag{6.82}$$

This value is greater than the total stored energy obtained in equation (6.78). Hence the selected core has capacity to effectively handle the stored energy in the coupled inductors.

Step 4: Winding parameter specification

Copper wire with a k_{cu} of 0.3 is chosen for the inductor winding due to its high conductivity. The relationship between copper conductor area and the current density is given by

$$A_{cu} = \frac{I_{rms}}{j_{rms}} \tag{6.83}$$

Hence the conductor area for each inductor is obtained as

$$A_{cu1N} = \frac{3.65}{9.53} = 0.383mm^2 \tag{6.84}$$

$$A_{cu2N} = \frac{20.75}{9.53} = 2.18mm^2 \tag{6.85}$$

Step 5: Skin depth determination

The skin depth of copper conductor at a frequency of 100kHz is determined as,

$$\delta = \sqrt{\frac{\rho}{\pi \times \mu \times f}} = \sqrt{\frac{2.2 \times 10^{-8}}{\pi \times 100kHz \times 4\pi \times 10^{-7}}} = 0.2mm \tag{6.86}$$

The diameter of the selected copper windings is obtained from equations (6.84) and (6.85) as $d_1 = 0.7mm$ and $d_2 = 1.67mm$. Since these diameters are greater than two times the skin depth, there is need to utilise stranded copper conductor. For both the primary- and secondary-side inductor windings, a copper wire with a diameter of 0.41mm is chosen. This winding has a resistance of $0.169\Omega/m$ as indicated on the American Wire Gauge Data, AWG No. 27 [37]. The number of strands in primary-side inductor is obtained as,

$$N_{1N,strands} = \frac{A_{cu1N}}{\pi \times \delta^2} = \frac{0.383}{\pi \times 0.205^2} \approx 3strands \tag{6.87}$$

Similarly, the number of strands in secondary-side inductor is obtained as,

$$N_{2N,strands} = \frac{A_{cu2N}}{\pi \times \delta^2} = \frac{2.18}{\pi \times 0.21^2} \approx 16strands \tag{6.88}$$

Step 6: Air gap determination

An airgap is included on the centre limb of the ferrite E-core for high energy storage of the inductor. The length of airgap is determined as

$$l_g = \frac{4\pi \times 10^{-7} \times 2.97 \times 10^{-3} \times 2.66^2}{529 \times 10^{-6} \times 0.16^2} = 1.95mm \tag{6.89}$$

Step 7: Number of turns determination

Mean length of flux for the E-core is obtained as,

$$l_m = 2 \times (b + h) + 2.5a = 163mm \tag{6.90}$$

Mean length of one turn, MLT, is obtained as,

$$MLT = 4b + 2 \times (a + d) = 141.2mm \tag{6.91}$$

The total reluctance, R_{tot}, of the core with $\mu_r = 2000$ at $100kHz$, $100°C$ and $0.16T$ operation is obtained as,

$$R_{tot} = \frac{l_m}{\mu_r \mu_o A_c} + \frac{l_g}{\mu_o A_c} = \left(\frac{0.163}{2000 \times 4\pi \times 10^{-7} \times 529 \times 10^{-6}}\right) + \left(\frac{1.95 \times 10^{-3}}{4\pi \times 10^{-7} \times 529 \times 10^{-6}}\right) \quad (6.92)$$

$$R_{tot} = 3.06 \times 10^6 turns/wb$$

The number of turns in L_{1N} is obtained as

$$N_{L1N} = \sqrt{L_{1N} \times R_{tot}} = \sqrt{2.97mH \times 2.06 \times 10^6} \approx 95turns \quad (6.93)$$

Consequently, the number of turns in L_{21} is obtained as

$$n = 1 + \frac{N_{L1N}}{N_{L2N}} = 6 \quad (6.94)$$

$$N_{L2N} = \frac{95}{5} = 19turns$$

Step 8: Winding resistance determination

The winding resistance is given by [37],

$$r_L = \frac{MLT \times N_L \times R_{AWG}}{N_{L,strands}} \quad (6.95)$$

From the American Wire Gauge table, the copper conductor used in the coupled inductor has a resistance, $R_{AWG} = 0.169\Omega/m$. Winding resistances are then obtained as,

$$r_{L1N} = \frac{0.141 \times 95 \times 0.169}{3} = 0.75\Omega \quad (6.96)$$

$$r_{L2N} = \frac{0.141 \times 19 \times 0.169}{16} = 0.028\Omega \quad (6.97)$$

6.3.1.3 Power loss in the Inductor windings

Power loss in inductor winding is occasioned by conductor resistance, r_L. For L_{1N} this power loss is obtained as,

$$P_{L1N} = r_{L1N} \times I_{L1N,avg}{}^2 = 0.75 \times 2.66^2 = 5.31W \quad (6.98)$$

Similarly, the power loss in L_{2N} is obtained as

$$P_{L21} = r_{L21} \times I_{L21,avg}{}^2 = 0.028 \times 16.67^2 = 7.78W \quad (6.99)$$

The total power loss across the coupled inductor is obtained as,

$$P_{tot} = P_{L1N} + P_{L2N} = 5.31W + 7.78W = 13.09W \tag{6.100}$$

6.3.1.4 Active switch selection

Two MOSFET switches are employed in each phase to facilitate bidirectional flow of current in the interface. The size of MOSFET switch is determined by the magnitude of voltage that the switch can block when it is not conducting.

Buck-mode operation

The voltage blocked by switch, S_{1N}, ignoring the spike due to the leakage inductance of the coupled-inductors, is given by

$$V_{ds1N} = \frac{\{V_{in} - i_{L1N}(r_{L1N} + r_{ds,on})\} + nk\{V_o + V_{fwd} + i_{L2N}r_{L2N}\}}{(nk)} \tag{6.101}$$

Similarly, the voltage blocked by switch, S_{2N}, is given by

$$V_{ds2N} = V_{in} - i_{L1N}r_{ds,on} - (1-nk)\{V_o + i_{L2N}(r_{ds,on} + r_{L2N}) + V_{fwd}\} \tag{6.102}$$

The switch rms currents are given by,

$$I_{ds1N,rms} = \sqrt{\{(I_{L2N,nom})^2 \times (1-D_2)[1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2I_{L2N,nom}})^2]\}} \tag{6.103}$$

$$I_{ds2N,rms} = \sqrt{\{(I_{L1N,nom})^2 \times D_2[1 + \frac{1}{3}(\frac{\Delta i_{L1N,pk-pk}}{2I_{L1N,nom}})^2]\}} \tag{6.104}$$

Boost-mode operation

The voltage blocked by S_{1N} is given by

$$V_{ds1N} = \frac{\{V_{bus} + i_{L2N}(r_{L1N} + r_{ds,on})\} + nk\{V_{bat} - i_{L2N}r_{ds,on}\}}{(1+nk)} \tag{6.105}$$

Similarly, the voltage blocked by S_{2N} is given by,

$$V_{ds2N} = V_{bus} + i_{L1N}r_{ds,on} + i_{L1N}r_{L1N} + nk\{V_{bat} - i_{L2N}(r_{L2N} + r_{ds,on})\} \tag{6.106}$$

The switch rms currents are given by,

$$I_{ds1N} = \sqrt{\{(I_{L2N,nom})^2 \times D_1[1 + \frac{1}{3}(\frac{\Delta i_{L2N,pk-pk}}{2I_{L2N,nom}})^2]\}} \tag{6.107}$$

$$I_{ds2N,rms} = \sqrt{(\frac{I_{o,avg}}{1-D_1})^2 \times (1-D_1)[1 + \frac{1}{3}(\frac{\Delta i_{L1N,pk-pk}}{2(\frac{I_{o,avg}}{1-D_1})^2}]} \tag{6.108}$$

Considering the converter specifications: $n = 6$, $\delta = 0.53$, $k = 0.99$, $r_{L1N} = 0.75\Omega$, $r_{L2N} = 0.028\Omega$, $V_{bus} = 380V$, $V_{bat} = 60V$, $P_o = 1000W$ and $f_{sw} = 100kHz$. Then,

In buck-mode operation: $V_{ds1N} = 123.9V$, $V_{ds2N} = 682.5V$, $I_{ds1N,rms} = 20.43A$, and $I_{ds2N,rms} = 3.65A$

In boost-mode operation: $V_{ds1N} = 106.1V$, $V_{ds2N} = 675.6V$, $I_{ds1N,rms} = 21.62A$, and $I_{ds2N,rms} = 3.51A$

Since the same switches are used in both buck and boost-mode operation, an IPP320N20N3 power MOSFET rated at $V_{dss} = 200V$, $I_{ds} = 34A$ and $r_{ds,on} = 32m\Omega$, is selected for S_{1N} while an SCT2450KEC power MOSFET rated at $V_{dss} = 1000V$, $I_{ds} = 8A$ and $r_{ds,on} = 0.61\Omega$ is chosen for S_{2N}. The switches are selected for the worst case scenario and considering a safety factor of 1.5-2.

6.3.1.5 Snubber circuit design

The leakage inductance of tapped-coupled inductor, due to imperfect coupling, causes some voltage spike across the two active switches as shown in figures 6.5. These voltage spike do not only increase the switching losses, but also have potential to destroy the MOSFET switches. There is need to employ a snubber circuit to clamp these voltage spikes.

Two sets of passive lossless snubber circuits are proposed to clamp the voltage spikes and recycle the leakage energy. These snubber circuits have previously been employed individually in a boost and buck converter topology based on tapped-coupled inductor [43], [44]. However, no study has proposed employing them in a bidirectional tapped-coupled inductor boost converter. The first set (boost-mode snubber) consists of three diodes, D_{S1N}, D_{S2N} and D_{S3N}, and two capacitors, C_{S1N} and C_{S2N}, while the

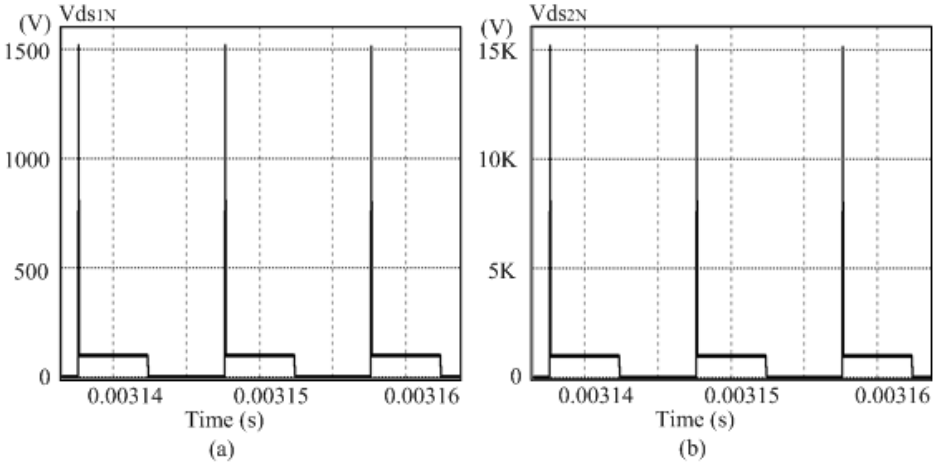

Figure 6.5: Voltage spikes across the active switches

second set (buck-mode snubber) consists of a capacitor, C_{CN} and two diodes, D_{C1N} and D_{C2N} . Figure 6.6 shows the proposed snubber circuits. These snubber circuits allow bidirectional flow of current and hence do not alter the normal function of the converter.

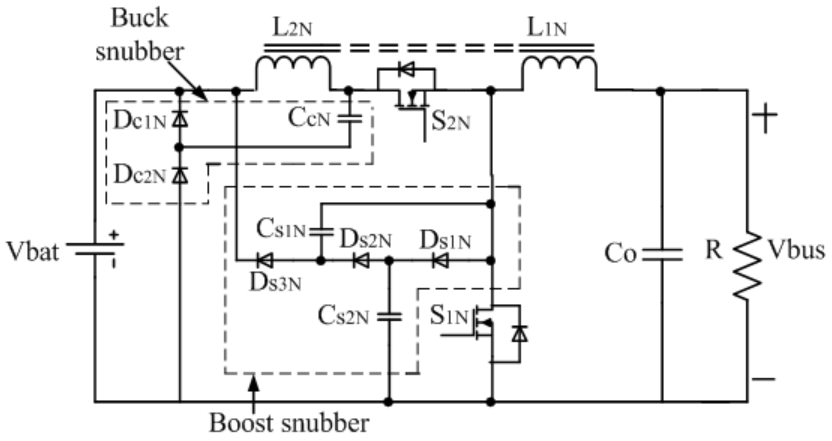

Figure 6.6: Low voltage battery interface with snubber circuit

Buck-mode snubber circuit

Buck snubber circuit operates in order to clamp the voltage spike across S_{2N} when the converter is operating in buck mode. In the first switching interval, S_{2N} is turned on allowing current to flow from the input to the output-side. The tapped-coupled inductors get charged. In the second interval, S_{2N} is turned off while S_{1N} is turned on. Leakage energy is stored in the snubber capacitor, C_{CN}, during this interval and is only released to the output, via the forward biased diode, D_{C1N}, when S_{2N} turns on in

the next cycle The magnitude of voltage across the charged snubber capacitor is given by [43],

$$V_{cs} = \frac{(V_{bus} - V_{bat})}{n} + V_{bat} = \frac{(380-60)}{6} + 60 = 113.9V \tag{6.109}$$

Consequently, the size of C_{CN} is obtained as,

$$C_{CN} = \frac{\Delta i_{L1N,pk-pk} \times T_{sw}}{8 \times \Delta V_{cs}} = \frac{0.532}{8 \times 0.0125 \times 113.9 \times 100kHz} = 0.47\mu F \tag{6.110}$$

Boost-mode snubber circuit

Boost snubber circuit operates in order to clamp voltage spikes across S_{1N} when the converter is operating in boost-mode. In the first switching interval, S_{1N} conducts while S_{2N} is off. The coupled-inductor gets charged. In the second switching interval, S_{1N} is switched off. The energy stored in the leakage inductance is discharged into the clamp capacitor, C_{S2N} via the forward biased diode D_{S1N}. This energy is further transferred to the output through the resonant capacitor, C_{S1N}, which provides additional boost capability of the converter. The value of resonant capacitor is given by [44],

$$\frac{V_{bus}}{V_{bat}} = \frac{1 + nD_2 + n\alpha(1+k)}{1 - D_2 - \alpha} \tag{6.111}$$

where: n is turns ratio, D_2 is duty-cycle and k is coupling coefficient.

$$\alpha = \frac{2C_{S1N}f_s\left(\frac{1}{1-D_2} + n\right)}{\frac{k}{1-D_2} \times \frac{I_{o,avg}}{V_{bat}} + \frac{D_2}{2L_m fs}} \tag{6.112}$$

From equation (6.111) and (6.112), $\alpha = 0.066$ while $C_{S1N} = 3nF$.

The size of clamp capacitor, C_{S2N} is obtained using the following expressions [44],

$$\frac{V_{bus}}{V_{bat}} = \frac{1 - D_2 + \frac{k^2}{n} - \frac{n(1+k)\Pi}{k} \times f_s \times \sqrt{L_k \times C_{S2N}}}{1 - D + \frac{\Pi}{k} \times f_s \times \sqrt{L_k \times C_{S2N}}} \tag{6.113}$$

From equation (6.113), $C_{S2N} = 24nF$.

6.3.1.6 Active switch power loss

Total power losses in the active switch are mainly due to switching and conduction loss.

$$P_{tot} = P_{sw} + P_{cond} \tag{6.114}$$

Switching loss, P_{sw}, is given by

$$P_{sw} = 0.5 \times V_{ds} \times I_{ds,pk} \times (t_{ri} + t_{ds,on} + t_{rv} + t_{ds,off}) \times f_{sw} \tag{6.115}$$

where: V_{ds} is the voltage blocked by the switch, I_{ds} is the current passing through the switch, t_{ri} is the current rise time, $t_{ds,on}$ is the on-time of the switch, t_{rv} is the voltage rise time and $t_{ds,off}$ is the off time.

The conduction loss, P_{cond}, is given by,

$$P_{cond} = V_{on} \times I_0 \times D = I^2_{ds,rms} \times r_{ds,on} \tag{6.116}$$

where: $I_{ds,rms}$ is the RMS current passing through the switch and $r_{ds,on}$ is the on-state resistance of the switch.

From the specifications of S_{1N}, switching loss and conduction loss is obtained from equation (6.116) and (6.117) as

$$P_{s1N,sw} = 0.5 \times 123.9 \times 31.48 \times 70ns \times 100kHz = 13.65W \tag{6.117}$$

$$P_{s1N,cond} = 20.44^2 \times 0.032 = 13.36W \tag{6.118}$$

Similarly, switching and conduction loss for S_{2N}, is obtained as

$$P_{s2N,sw} = 0.5 \times 682.5 \times 5.26 \times 108ns \times 100kHz = 19.38W \tag{6.119}$$

$$P_{s2N,cond} = 3.65^2 \times 0.61 = 8.14W \tag{6.120}$$

The total power loss, P_{tot}, in S_{1N} and S_{2N} is obtained by summing up the switching loss and conduction loss.

$$P_{s1N,tot} = 13.65 + 13.36 = 27.01W \tag{6.121}$$

$$P_{s2N,tot} = 8.14 + 19.38 = 27.52W \tag{6.122}$$

6.3.1.7 Thermal management

Thermal resistance of a heat sink is given by [36],

$$R_{\theta,sa} = \frac{T_{j,max} - T_a}{P_{tot}} - R_{\theta,jc} \tag{6.123}$$

where $R_{\theta,sa}$ is the sink-to-ambient thermal resistance and $R_{\theta,jc}$ is the junction-to-case thermal resistance obtained from the MOSFET datasheet.

The maximum junction temperature, $T_{j,max}$, in the semiconductor was chosen as 150° C while ambient temperature, T_a, was chosen as 60°C. Consequently, for S_{1N}, the thermal resistance is calculated as,

$$R_{\theta,sa} = \frac{150 - 70}{27.01} - 0.9 = 2.06^{\circ}C/W \tag{6.124}$$

A heat sink with a thermal resistance of $2^{\circ}C/W$ is chosen to dissipate the heat generated in S_{1N}. For S_{2N}, the size of heat sink is calculated as,

$$R_{\theta,sa} = \frac{150 - 70}{27.52} - 0.7 = 2.21^{\circ}C/W \tag{6.125}$$

A heat sink with a thermal resistance of $2.2^{\circ}C/W$ is chosen to dissipate the heat generated in S_{2N}.

6.3.1.8 Capacitor sizing

Two capacitors are employed in the low voltage battery interface to reduce ripple voltage. One capacitor is employed at the output (buck-mode capacitor) while the other is employed at the input (boost-mode capacitor).

Buck-mode capacitor

The output capacitor in buck-mode converter operation is given by [45],

$$C_o = \frac{I_{o,avg} \times L_{21}}{2 \times R_{bat} \times \Delta V_{bat,pk-pk}} \times \left(1 + \frac{n^2 \frac{V_{bat}}{V_{bus}}}{1 - \frac{V_{bat}}{V_{bus}}}\right) \tag{6.126}$$

where: R_{bat} is resistance of the battery during charging. The size of capacitor is obtained as $22\mu F$. Considering a safety margin of 1.5, a $22\mu F$ capacitor rated at $90V$ and $20A$ is selected.

Boost-mode capacitor

The output capacitor in a boost-mode converter operation is given by [36],

$$C_o = \frac{I_o \times D \times T_{sw}}{\Delta V_{bus,pk-pk}} = 2.5\mu F \tag{6.127}$$

Considering a safety margin of 1.25 in the capacitor voltage, a $3\mu F$, $450V$ capacitor was selected.

6.3.1.9 Switch gate drive

A HCPL-3120 similar to the one that was employed in driving the MOSFETS switches in SWECS is considered. The size of gate resistor, R_{GATE} is determined from equation as,

$$R_{GATE} > \frac{V_{CC} - V_{EE} - V_{OL}}{I_{OL,peak}} = 5.2\Omega \tag{6.128}$$

6.3.2 Converter efficiency

The MOSFET power losses as well as coupled-inductor copper losses were calculated in the previous sections. The results are summarised in Table 6.3.

Table 6.3: Power losses in a single-phase low voltage battery interface

Output power	Copper loss	Switching loss	Switch conduction loss	Total loss
$1000W$	$13.09W$	$33.03W$	$21.5W$	$67.62W$

From the calculated values in Table 6.3, efficiency of a single-phase low voltage battery interface is obtained as

$$\eta = (1 - \frac{67.62W}{1000W}) \times 100 = 93.2\% \tag{6.129}$$

6.4 CHAPTER CONCLUSION

This chapter has presented the hardware design of a 1KW low voltage DC microgrid. This design included selection and sizing of tapped-coupled inductors, capacitors, MOSFETs, heat sinks and gate drive circuits. Effective passive lossless snubber circuits were also designed to clamp the voltage spikes across the active switches due to leakage inductance.

CHAPTER 7 PRACTICAL RESULTS

7.1 CHAPTER OVERVIEW

To validate theoretical analysis and simulation results, prototypes of the proposed SWECS and low voltage battery interfaces were built and tested. This chapter presents the experimental results obtained.

7.2 SWECS PRACTICAL RESULTS

A SWECS prototype was designed for rated power of 1000W but was tested at 600W and 800W, for the two-phase and single-phase respectively, due to power constraints in the laboratory. A MOSFET IRFI4229PBF rated at V_{dss}=300V, I_{ds} = 25A with $R_{ds,on}$ = 47$m\Omega$ was chosen for S_{1N} and S_{2N}. For the output diode, a RHRP15120 hyperfast diode rated at 6A and 1000V was selected. A passive lossless snubber circuit consisting of a diode and a capacitor was employed to suppress the voltage spikes across the active switch.

To minimise leakage inductance, the coupled-inductor was wound with a split high voltage winding, half of the turns in the inside and the other half on the outside, like a sandwich. This way, a coupling coefficient of 0.99 was achieved in the inductor. The coupled-inductor series resistances are r_{L1N} = 0.07Ω and r_{L2N} = 1.5Ω. The prototype was supplied from an AC source which was rectified using a three-phase diode rectifier. Practical results are provided for both single-phase and interleaved SWECS interface. A single-phase was tested by powering only one phase of the interleaved converter. In both cases, a duty-cycle of 0.55 was maintained.

7.2.1 Single-phase SWECS interface

This section presents the simulated and practical waveforms for a single-phase SWECS interface. Input and output voltage, input AC current spectra, input DC current and capacitor current waveforms are shown.

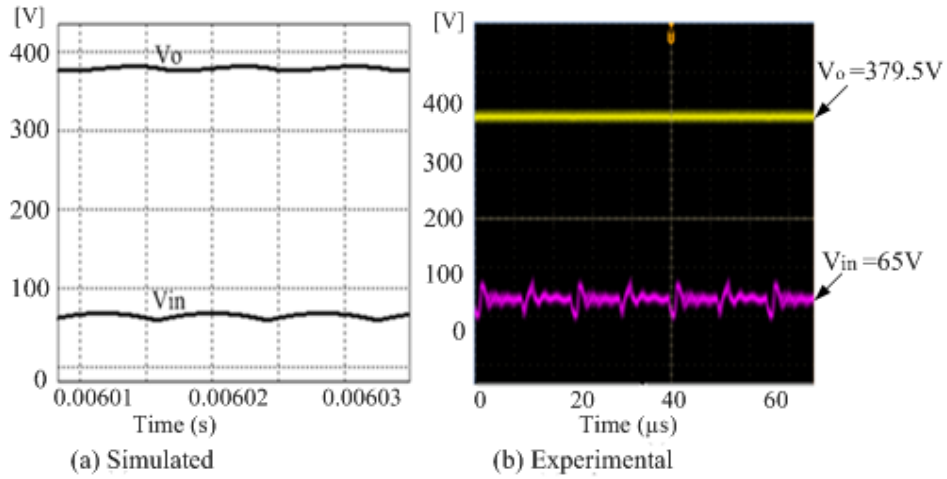

Figure 7.1: Input and output DC voltage waveforms

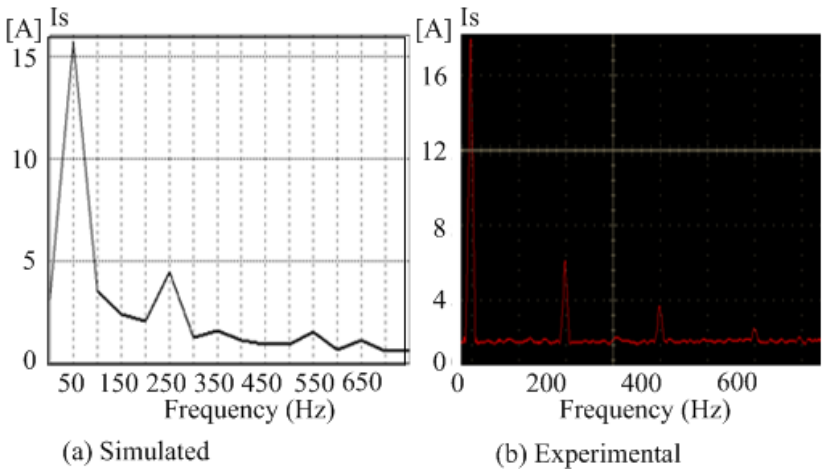

Figure 7.2: Input AC current spectra

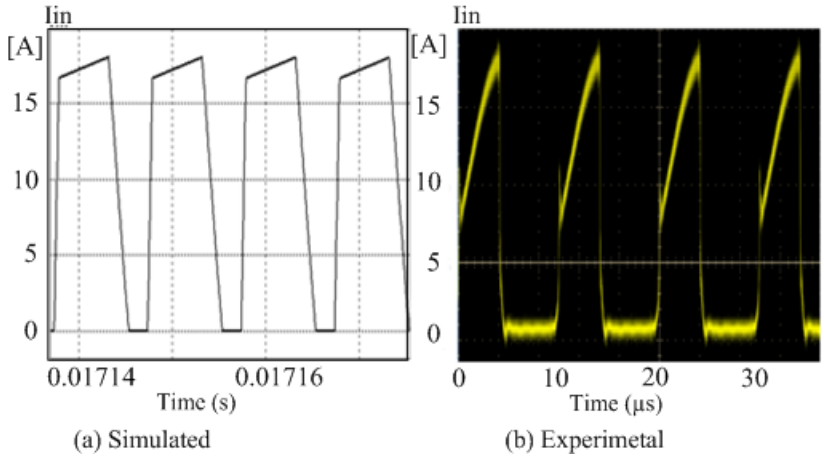

Figure 7.3: Input DC current

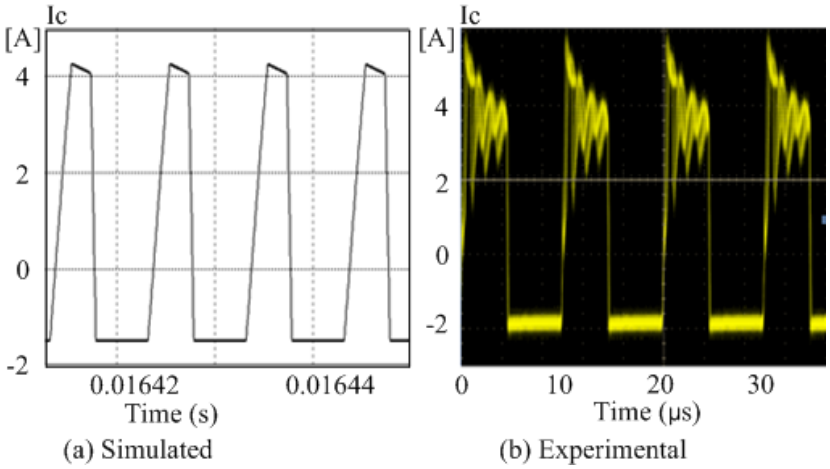

Figure 7.4: Capacitor current

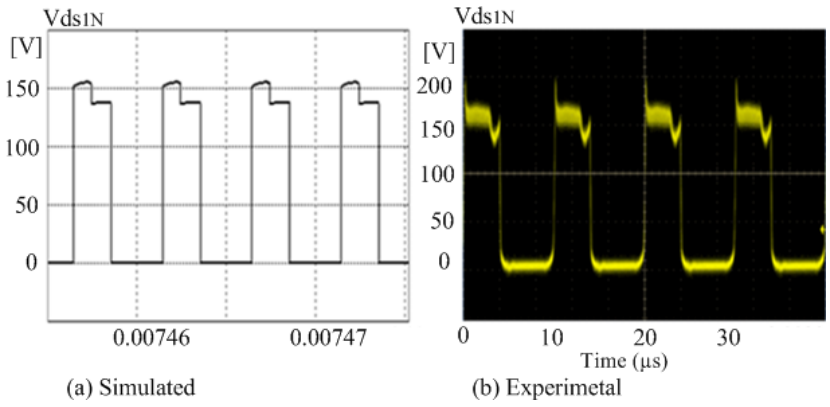

Figure 7.5: (a) Simulated and (b) experimental switch voltage waveforms

7.2.2 Two-phase SWECS interface

This section presents the simulated and practical waveforms for a two-phase SWECS interface. Input and output voltage, input AC current spectra, input DC current and capacitor current waveforms are presented.

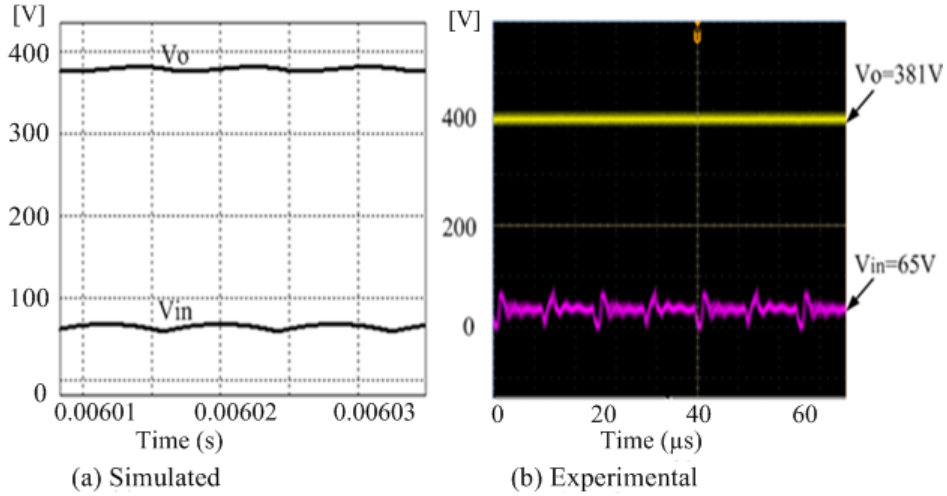

Figure 7.6: Input and output DC voltages for V_{in} = 65V

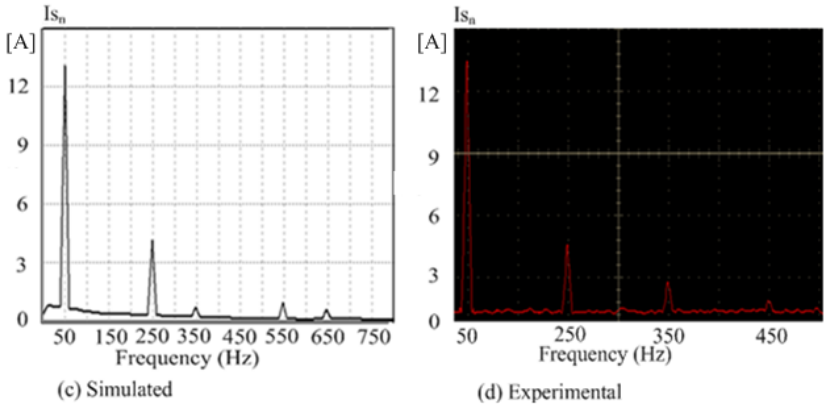

Figure 7.7: Input AC current spectra

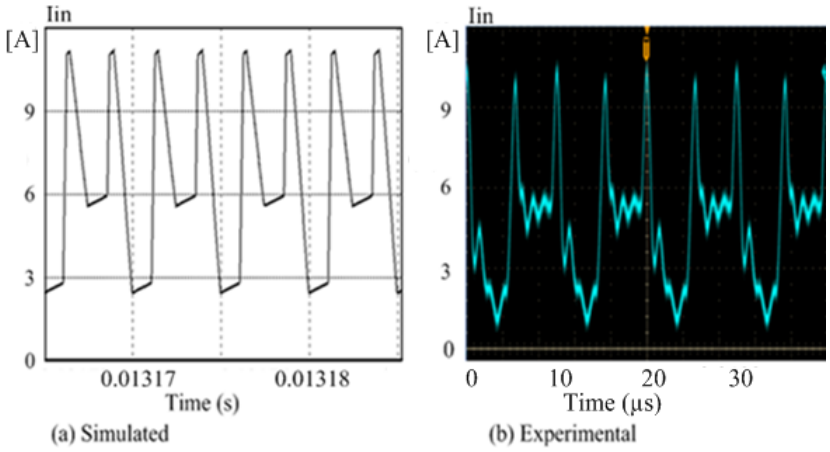

Figure 7.8: input current waveforms

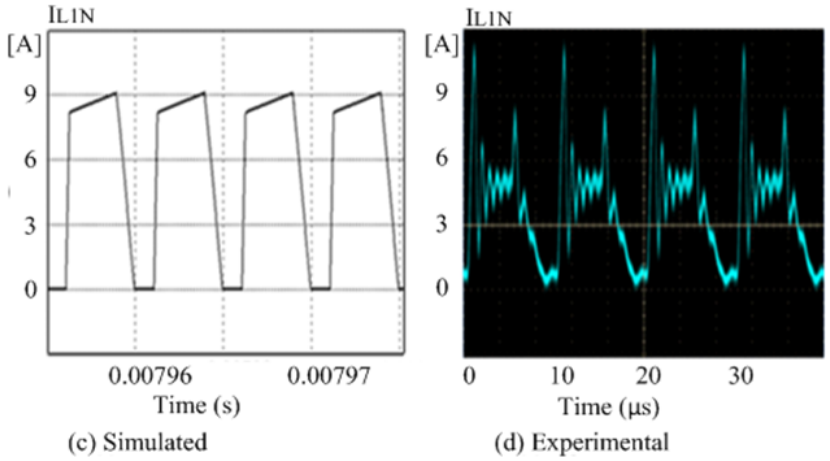

Figure 7.9: Primary inductor current waveforms

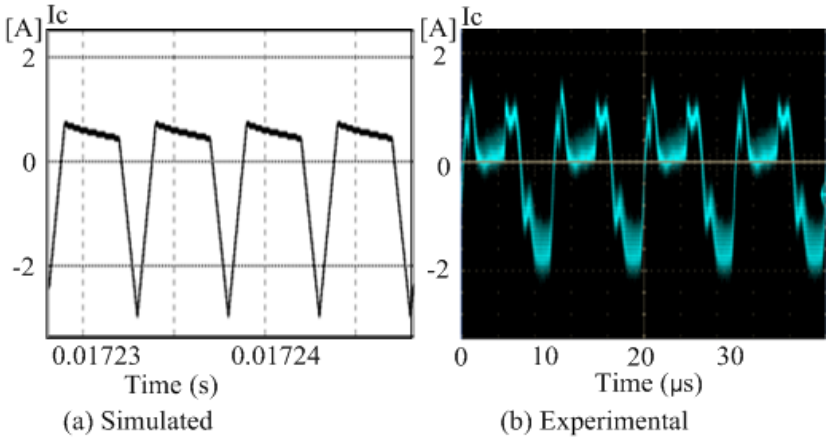

Figure 7.10: Capacitor current waveforms

7.2.3 Discussion of experimental results

From figures 7.1 and 7.6 an average output voltage of 380V is achieved from an input of 65V at a duty ratio of 0.55. This translates to a voltage boost of approximately 6 times which further confirms the high boost capabilities of the proposed active rectifier and hence its suitability in interfacing low voltage wind generator to a DC distribution grid.

Figures 7.3 and 7.8 present the input current in single-phase and two-phase operation of the SWECS. It is seen that input peak-to-peak and RMS ripple current is smaller in the two-phase operation as compared to that of single-phase operation. Similarly, it is observed from figures 7.4 and 7.10, that the output capacitor current is lower in the two-phase operation as compared to that of single-phase operation. These results are summarised in Table 7.1. They provide a clear demonstration that interleaving reduces the input and output ripple current and hence the need for smaller converter filter components.

Table 7.1: Comparison of experimental results between single-phase and two-phase SWECS operation

	V_{in}	V_o	$I_{in,rms}$	$I_{in,pk-pk}$	$I_{in,ripple,rms}$	$I_{L1N,pk-pk}$	$I_{c,rms}$
Single-phase	$65V$	$379.5V$	$11.2A$	$10.4A$	$5.16A$	$10.4A$	$2.45A$
Two-phase	$65V$	$381V$	$9.95A$	$9.1A$	$1.59A$	$10.1A$	$1.41A$

The AC input current spectra are presented in Figures 7.2 and 7.7. In single-phase SWECS operation, the first harmonic occurs at 250Hz with a magnitude of 4.45 while the second harmonic occurs at a frequency of 550Hz with magnitude of 1.53. In two-phase SWECS operation, the first harmonic occurs at a frequency of 250Hz with a magnitude of 2.5A while the second harmonic occurs at 550 Hz with a magnitude of 1.48A. THD and total input power factor, in two-phase operation, is obtained as 20% and 0.95 respectively, while in single-phase operation, it is obtained as 24% and 0.94 respectively. These results are in agreement with simulation results which is a further validation of the ability of the proposed SWECS in providing active voltage rectification with high input power factor and low THD.

Figure 7.5 shows the simulated and experimental switch voltage waveforms. The passive lossless snubber circuit employed in this circuit is able to clamp voltage spikes, due to leakage inductance, to a

maximum peak of 200V. Therefore, the required size of active switches is reduced which minimises switching losses and improves efficiency of the system

A comparison of experimental, simulated and theoretical results for the proposed SWECS are presented in Table 7.2. It is observed that there is a good agreement among the results.

Table 7.2: Comparison of experimental, simulated and analytical results

	V_{in}	V_o	$I_{in,rms}$	$I_{in,pk-pk}$	$I_{L1N,pk-pk}$	$I_{c,rms}$
Experimental	$65V$	$379.5V$	$9.95A$	$9.5A$	$10.1A$	$1.41A$
Simulation	$65V$	$381V$	$9.84A$	$8.7A$	$9A$	$1.35A$
Analysis	$65V$	$380V$	$9.8A$	$9.28A$	$9.2A$	$1.4A$

Tables 7.3 and 7.4 present efficiency results in single-phase and two-phase SWECS at different power levels. These values are in good agreement with theoretical results. For low power applications, efficiency of the single-phase interface is higher than that of two-phase interface, while at higher power levels, the vice-versa is true.

Table 7.3: Efficiency of single-phase SWECS

Power	Efficiency
400W	96%
800W	91.2%

Table 7.4: Efficiency of Two-phase SWECS

Power	Efficiency
300W	95%
600W	94.2%

7.3 LOW VOLTAGE BATTERY INTERFACE PRACTICAL RESULTS

A low voltage battery interface prototype was designed for rated power of 1000W but was tested at 500W and 750W, for the two-phase and single-phase respectively, due to power challenges in the laboratory. Two pairs of passive lossless snubber circuits were employed to suppress the voltage spikes across the active switches in buck and boost-mode operation. Just like in the case of the SWEC prototype, the coupled-inductor was wound with a split high voltage winding to improve coupling and minimise leakage inductance. Consequently, a coupling coefficient of 0.99 was achieved. The inductor series resistances are r_{L1N} = 0.75 and r_{L2N} = 0.028. The interface was tested in both buck and boost-mode operation to verify its bidirectional power flow capability. Practical results are obtained for both single-phase and two-phase BESS converter with a duty-cycle of 0.53.

7.3.1 Buck-mode operation

7.3.1.1 Single-phase interface

This section presents the simulated and practical waveforms for a single-phase battery interface operating in buck-mode. Input and output voltage, input current and capacitor current waveforms are shown.

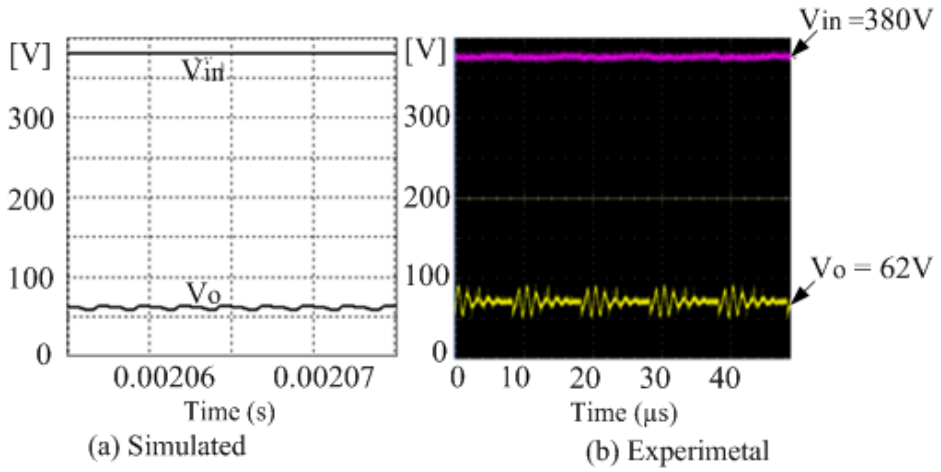

Figure 7.11: Input and output voltage waveforms

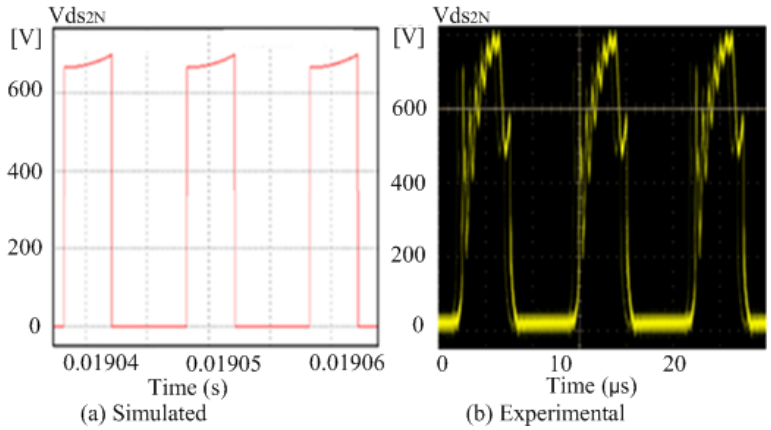

Figure 7.12: Buck switch voltage waveforms

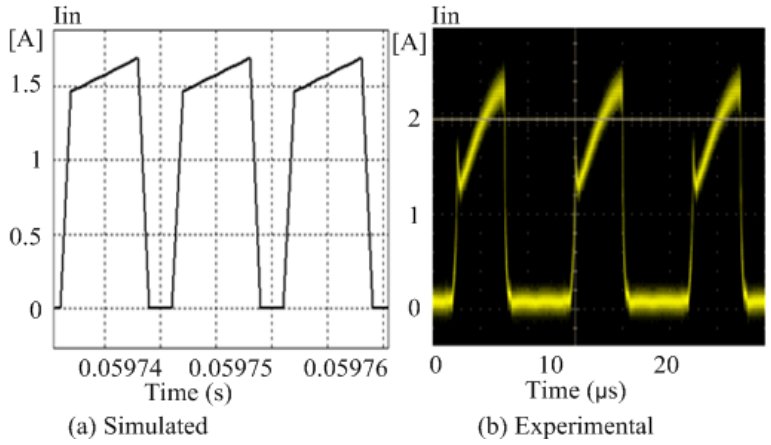

Figure 7.13: Input current waveforms

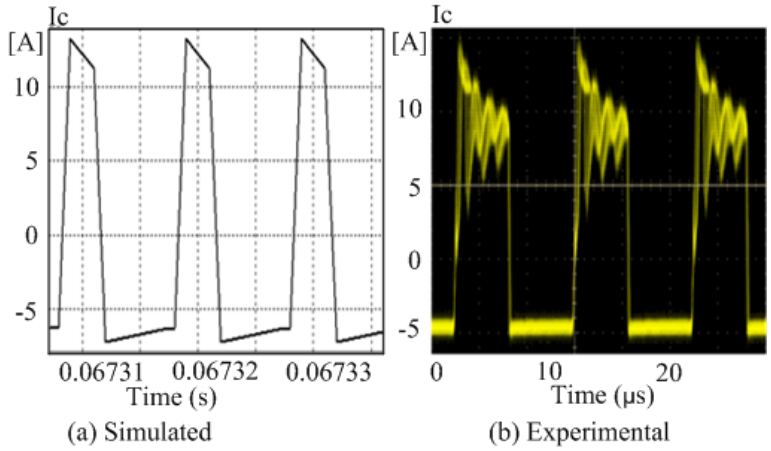

Figure 7.14: Capacitor current waveforms

7.3.1.2 Two-phase interface

This section presents the simulated and practical waveforms for a two-phase battery interface operating in buck-mode. Input and output voltage, input current and capacitor current waveforms are shown.

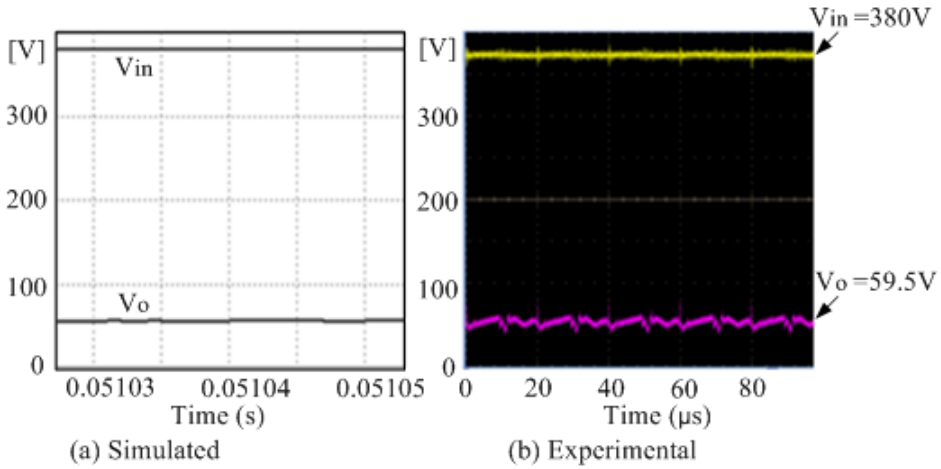

Figure 7.15: Input and output voltage waveforms

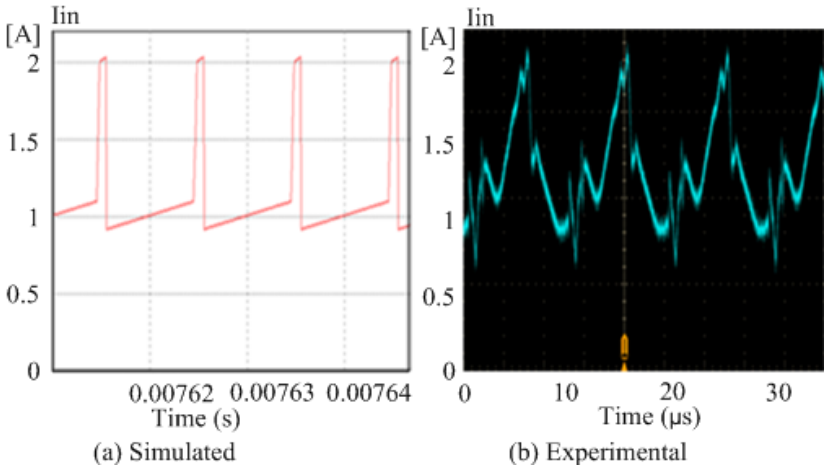

Figure 7.16: Input current waveforms

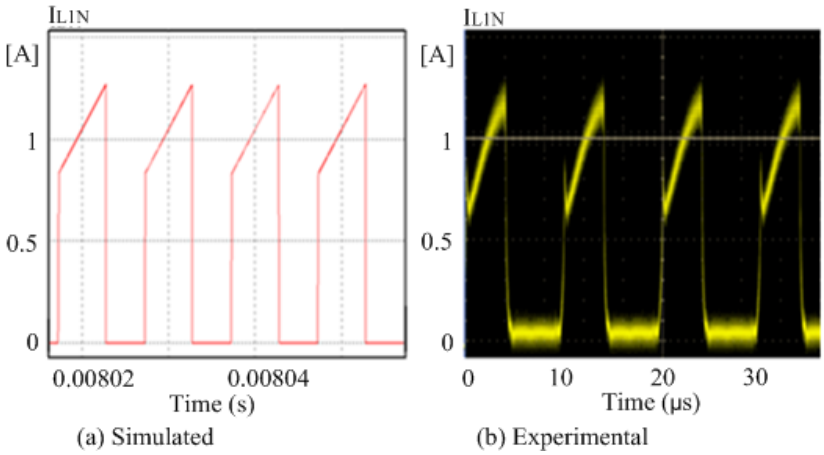

Figure 7.17: Primary inductor current waveforms

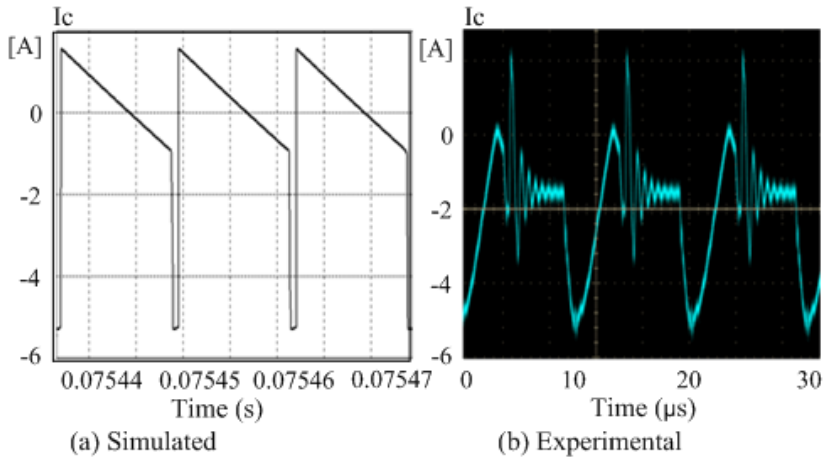

Figure 7.18: Capacitor current waveforms

7.3.1.3 Discussion of Buck-mode operation experimental results

From figures 7.11 and 7.15, an average output voltage of 61V is obtained from an input voltage of 380V. This represents a bucking ratio of approximately 6.3 which validates the large voltage step-down capability of the proposed converter interface and its suitability in interfacing low voltage battery to the distribution grid.

Figures 7.13 and 7.16 show the input current waveforms for a single-phase and two-phase operation of the proposed interface in buck-mode. It is observed that the peak-to-peak and RMS ripple current is higher in single-phase interface as compared to two-phase interface. Similarly, from the output

capacitor current waveforms shown in figures 7.13 and 7.18, the peak-to-peak and RMS ripple current is higher in single-phase interface as compared to two-phase interface. These results are summarised in Table 7.5 to validate the concept of interleaving which reduces the input and output ripple current and hence the need for smaller filter components.

Table 7.5: Comparison of experimental results between single-phase and two-phase converter interface

	V_{in}	V_o	$I_{in,rms}$	$I_{in,pk-pk}$	$I_{in,RMS,ripple}$	$I_{L1N,pk-pk}$	$I_{c,rms}$
Single-phase	380V	62V	1.65A	2.25A	1.19A	2.25A	7.1A
Two-phase	380V	61V	1.42A	1.2A	0.41A	1.3A	2.58A

Figure 7.12 presents the simulated and experimental waveforms of the buck-switch voltage. The passive lossless snubber circuit employed in the interface is able to clamp the voltage spikes from a peak of 25000V (as obtained in simulation results) to a maximum of 800V. This is a clear demonstration that application of the snubber effectively reduces the voltage ratings of the required active switch and hence a reduction in switching losses and cost.

A comparison of experimental, simulation and theoretical results for the proposed low voltage battery interface, operating in buck-mode, are presented in Table 7.6. It is observed that there is a good agreement among the results.

Table 7.6: Comparison of experimental, simulation and analytical results

	V_{in}	V_o	$I_{in,rms}$	$I_{in,pk-pk}$	$I_{L1N,pk-pk}$	$I_{c,rms}$
Experimental	380V	61V	1.42A	1.2A	1.3A	2.58A
Simulation	380V	59.5V	1.39A	1.3A	1.28A	2.35A
Analysis	380V	60V	1.43A	1.13A	1.24A	2.4A

7.3.2 Boost-mode operation

7.3.2.1 Single-phase interface

This section presents the simulated and practical waveforms for a single-phase battery interface operating in boost-mode. Input and output voltage, input current and capacitor current waveforms are

shown.

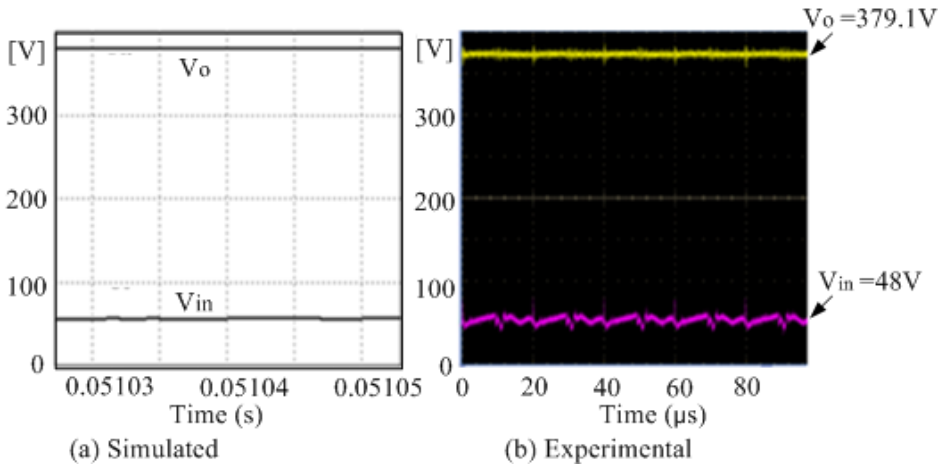

Figure 7.19: Input and output voltage waveforms

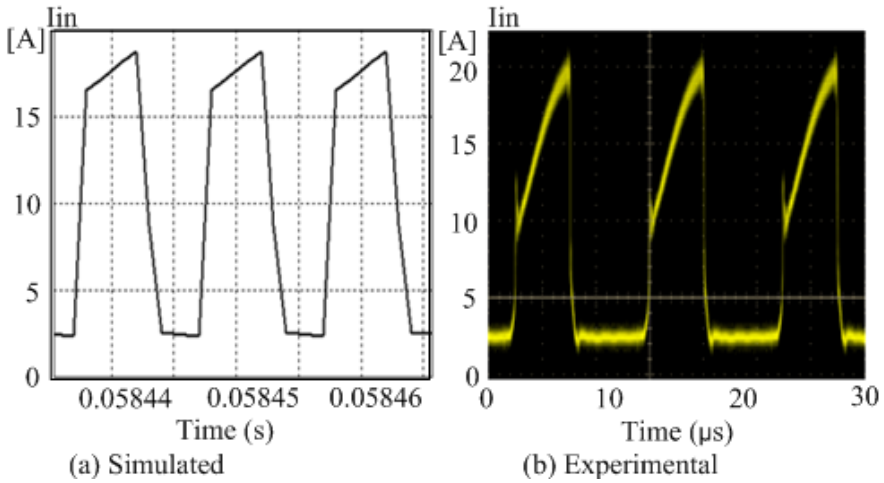

Figure 7.20: Input current waveforms

7.3.2.2 Two-phase interface

This section presents the simulated and practical waveforms for a two-phase battery interface operating in boost-mode. Input and output voltage, input current and capacitor current waveforms are shown.

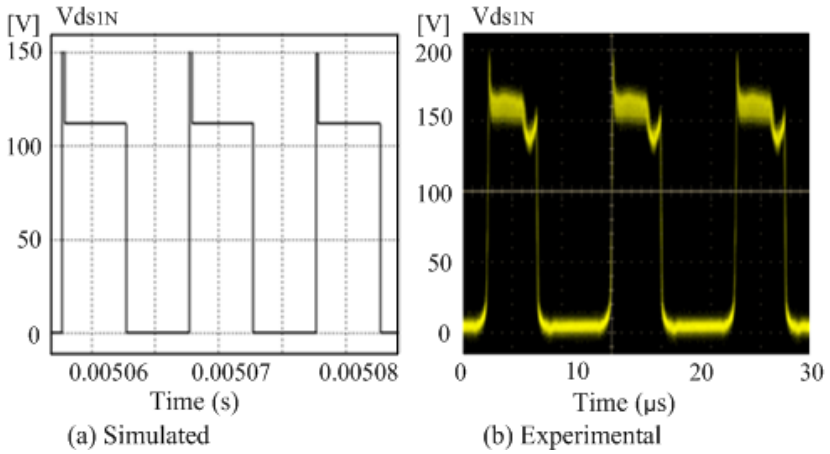

Figure 7.21: Boost switch voltage waveforms

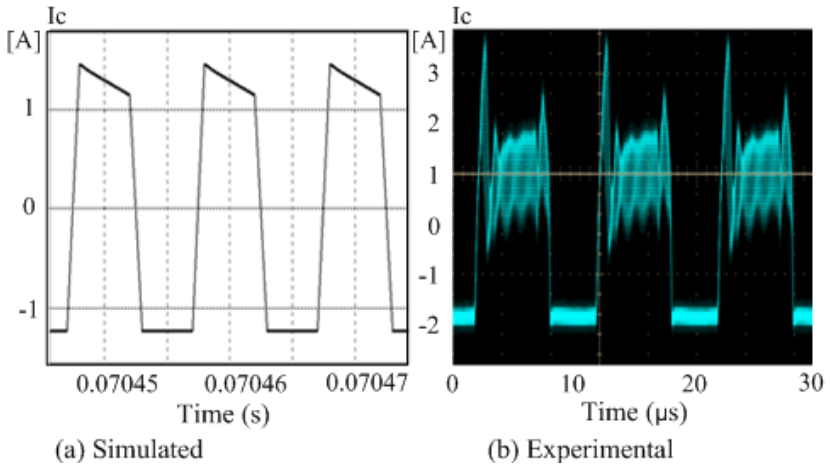

Figure 7.22: Capacitor current waveforms

7.3.2.3 Discussion of Boost-mode operation experimental results

Figures 7.19 and 7.23 present the input and output voltage waveforms for single-phase and two-phase battery interface operating in boost-mode. An average output voltage of 380V is obtained from an input of 48V which translates to a boost ratio of 7.9. Again this validates the high boosting capability of the proposed converter and its suitability in interfacing low voltage battery to a distribution grid.

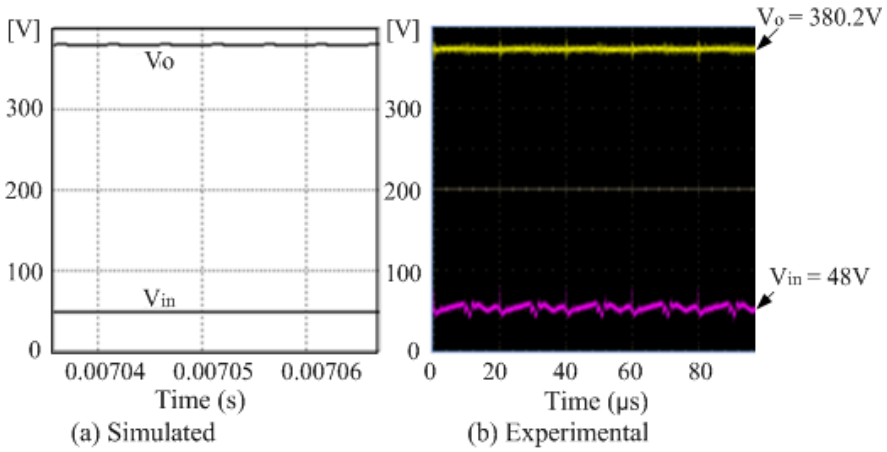

Figure 7.23: Input and output voltage waveforms

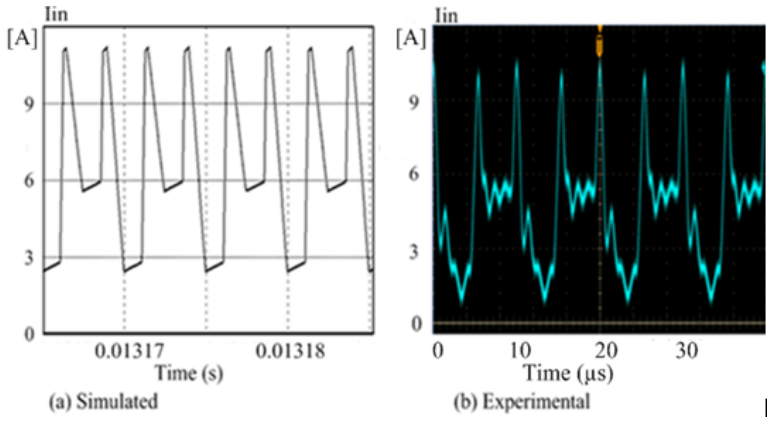

Figure 7.24: Input current waveforms

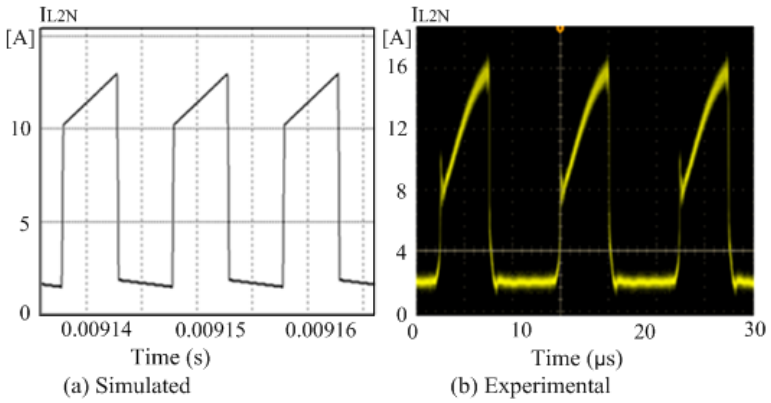

Figure 7.25: Primary inductor current waveforms

Figures 7.20 and 7.24 show the input current waveforms for a single-phase and two-phase battery

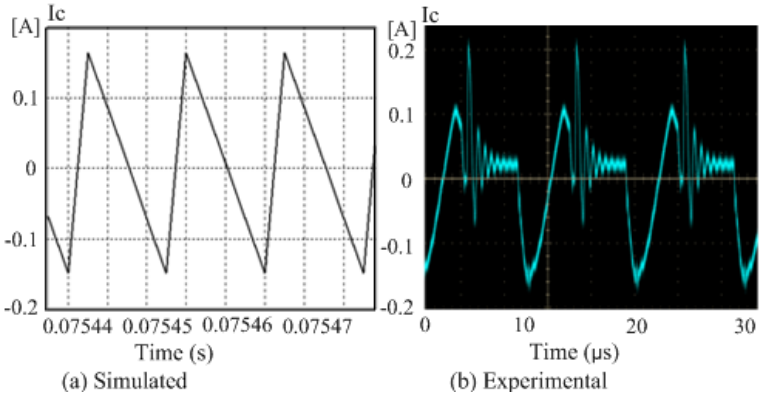

Figure 7.26: Capacitor current waveforms

interface operating in boost-mode. The peak-to-peak and RMS ripple current is smaller in two-phase converter interface as compared to single-phase. The same is observed in the output capacitor current results as shown in Figures 7.22 and 7.26 and summarised in Table 7.7.

Table 7.7: Comparison of parameter results between single-phase and two-phase converter interface

	V_{in}	V_o	$I_{in,rms}$	$I_{in,pk-pk}$	$I_{in,ripple,RMS}$	$I_{L2N,pk-pk}$	$I_{c,rms}$
Single-phase	$48V$	$379.1V$	$13.5A$	$16.5A$	$7.96A$	$16.5A$	$1.35A$
Two-phase	$48V$	$380.2V$	$10.6A$	$8.9A$	$0.92A$	$9.5A$	$0.17A$

A comparison of experimental, simulation and theoretical results for the proposed low voltage interface, operating in boost-mode, are presented in Table 7.8. It is observed that there is a good agreement among the results.

Table 7.8: Comparison of experimental, simulation and analytical results

	V_{in}	V_o	$I_{in,rms}$	$I_{in,pk-pk}$	$I_{L1N,pk-pk}$	$I_{c,rms}$
Experimental	$48V$	$380.2V$	$10.6A$	$8.9A$	$9.5A$	$0.17A$
Simulation	$48V$	$380V$	$11.1A$	$8.7A$	$9.25A$	$0.15A$
Analysis	$48V$	$380V$	$10.9A$	$8.55A$	$9.15A$	$0.16A$

7.3.3 Low voltage battery interface efficiency

Tables 7.9 and 7.10 present efficiency results for single-phase and two-phase low voltage battery interface operating in buck and boost-mode. It is observed that in both modes of operation, efficiency of the converter is high at low power levels and decreases as the operational power increases. This is in good agreement with theoretical analysis and simulation results. For low power applications, efficiency of the single-phase converter is higher than that of two-phase converter, while at higher power levels, the vice-versa is true.

Table 7.9: Single-phase converter interface efficiency

Power	Buck-mode Efficiency	Boost-mode Efficiency
400W	95.6%	95.2%
750W	93.2%	92.7%

Table 7.10: Two-phase converter interface efficiency

Power	Buck-mode Efficiency	Boost-mode efficiency
250W	95%	94%
500W	94.1%	93.1%

CHAPTER 8 CONCLUSION AND FUTURE WORK

8.1 CONCLUSION

Wind energy is the most popular source of renewable energy since it is abundant and does not pollute the environment. However, the interdependency of this resource on the prevailing weather patterns limits its full adoption. There is a high risk of transferring input voltage disturbances to the grid especially in standalone microgrids. Integration of an energy storage is necessary to regulate the bus voltage and improve reliability. This research was geared towards developing low voltage wind generator and battery storage interfaces. It sought to address issues that arise during the integration of these renewable energy sources to the distribution system. The conclusion of this dissertation is therefore, summarised in response to the research questions:

(1) How to interface a small wind generator to a DC bus?

For small wind generators, the most popular converter topology for interfacing to a distribution system is a diode rectifier with a capacitor voltage filter. However, this topology suffer from high THD in the input current and limited voltage boosting ratios. Other applications employ voltage source converters (VSCs) which have very high power factor and low THD. However, their voltage boosting capabilities are also low. This research has proposed a SWECS comprising of three-phase diode rectifier cascaded with an interleaved tapped-coupled inductor boost converter for high voltage boost ratios, low THD, and high input power factor.

Theoretical analysis, simulations and experimental results have shown that the interface has a very high boost ratio of 6 times at moderate duty-cycle of 0.55. The large step-up conversion has been achieved through careful selection of the tapped-inductor winding's turns ratio to reduce the duty-cycle

and keep the devices' blocking voltages within acceptable limits. It has been further demonstrated that interleaving reduces the input and output-side current ripple content and improves the power handling capability of the system.

(2) How to realise a wind generator interface with active voltage rectification?

Most three-phase diode rectifiers employ a capacitor voltage filter to smooth out the output DC voltage. As a result, they inject low order current harmonics into the generator supply with a THD of upto 33.1% and low power factor of 0.89. This research utilises the active switches in the interleaved tapped-coupled inductor boost converter to shape the input current and smooth-out the DC-bus voltage. Simulation and experimental results indicate that the proposed SWECS has a low THD of 20% and high total power factor of 0.94 which demonstrates its active rectification capability.

(3) How to implement a system that operates over a wide range of input voltages and achieves high conversion efficiency?

The intermittent nature of wind energy resource demands a converter interface that can operate over a wide range of input voltages while keeping the output voltage within acceptable limits. Simulation and experimental results of SWECS indicate that the operation of the interface with a variable input voltage has little effect on the output voltage due. This is due to application of an effective controller ably tracks the output voltage.

A graph showing the efficiency-power characteristics indicates that the efficiency of the converter decreases as power level increases. At 500W efficiency is 96.4% while at 1000W efficiency is 94.3%. However, in both cases the efficiency is relatively high which confirms the suitability of this interface in small wind generator applications. It has been further demonstrated experimentally that interleaving improves the efficiency of the converter at high power levels.

(4) How to achieve proper energy management in a DC micro-grid in the presence of an intermittent wind energy resource?

Integration of an efficient energy storage system offers the best solution in maintaining the reliability of a DC micro-grid in the presence of an intermittent wind energy resource. Battery cell has been used

since it is the most popular energy storage technology owing to its low cost, portability, fast response time and mature technology. Simulation results have shown that these energy storage systems can regulate the voltage on the DC micro-grid within 1.5%.

(5) How to interface a low voltage battery storage system to a DC bus?

The low voltage battery storage system is integrated to a DC-bus using a two-phase tapped-coupled inductor boost converter. This converter interface has bidirectional power flow capability allowing the charging of the low voltage battery storage system in off-peak periods and discharging of the battery when the grid voltage demand rises. Simulation and experimental results have also demonstrated that interleaving reduces the converter's input and output-side voltage and current ripple. Consequently, the size of converter inductor and capacitor are also reduced.

(6) How to realise a system with good supply and load-side disturbance rejection?

A wind generator is prone to disturbances due to the variable weather patterns in which it operates. Similarly, the DC bus is susceptible to voltage variations due to uneven loading. Therefore, there is need to employ a controller in the low voltage wind generator and battery interfaces to track the output voltage and reject these disturbances. Simulation results for the converter interfaces exposed to step changes in supply and load indicate that these interfaces are able to reject the input and load-side disturbances ensuring a voltage regulation of less than 1%.

(7) How to realise an effective lossless snubber circuit that does not interfere with the normal operation of the interfaces?

The main challenge in converter topologies employing tapped-coupled inductor is the presence of leakage inductance which causes huge voltage spikes across the active switches. Previous studies have proposed the use of passive and active snubber circuits in bidirectional converter topologies. However, there is no study that has proposed a bidirectional passive lossless snubber circuit that is employed in this low voltage battery interface. Simulation and experimental results demonstrate that this snubber circuit is effective in clamping the voltage spikes across the switches. Therefore, MOSFETs with low voltage ratings are required which minimises cost and reduces power losses.

8.2 FUTURE WORK

The blocking voltage of the output diode in the SWECS and buck-switch in the low voltage BESS interface are a function of the coupled-inductor turns ratio and duty-cycle. This has a limiting effect in high power applications of the tapped-inductor topology. Although a careful consideration of these parameters has been made in this research to keep the voltages to the lowest level possible, the voltage ratings of these devices are still quite high. There is need for further research to identify new converter configurations which takes advantage of the tapped coupled-inductor to provide very high boost ratios while keeping the device blocking voltages low.

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APPENDIX A CONVERTER PROTOTYPES

A.1 SMALL WIND ENERGY CONVERSION SYSTEM

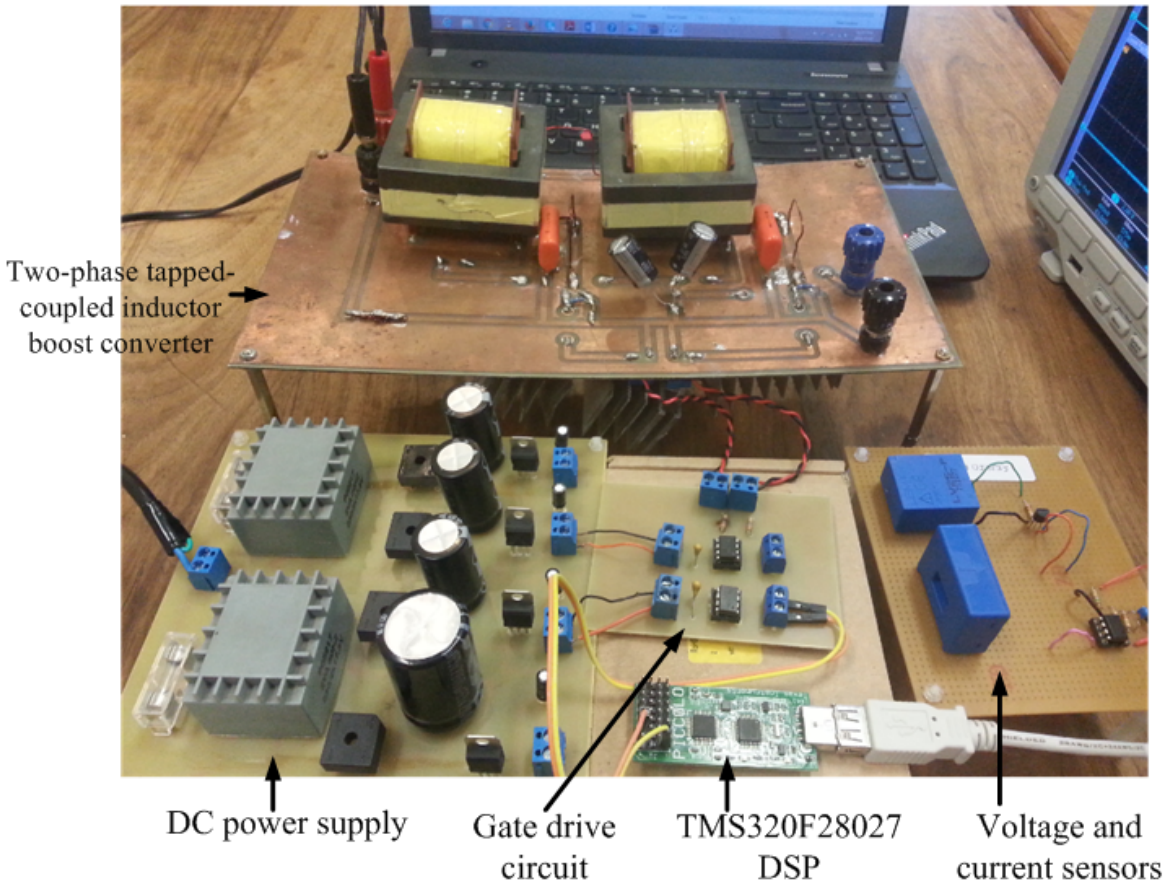

Figure A.1: Hardware implementation of small wind energy conversion system

A.2 LOW VOLTAGE BATTERY INTERFACE

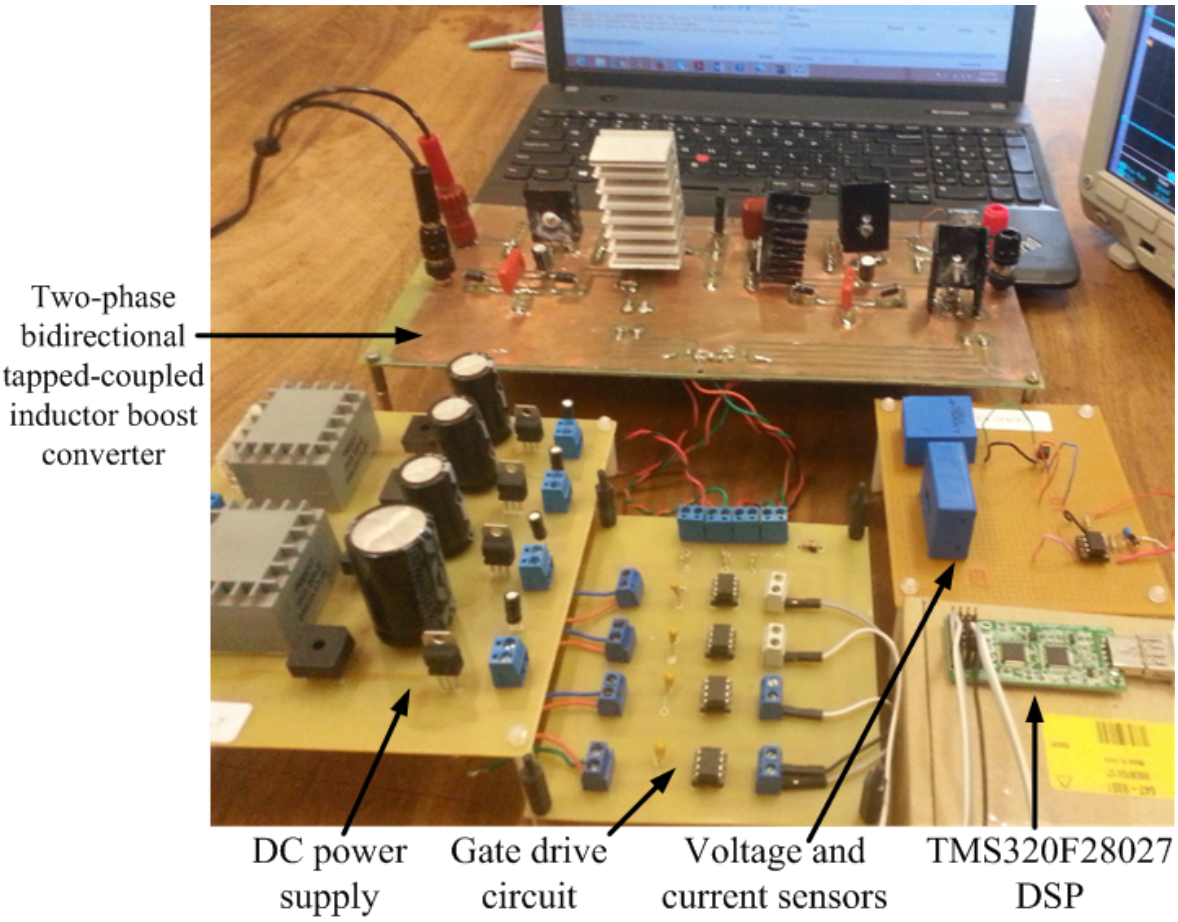

Figure A.2: Hardware implementation of low voltage battery interface

APPENDIX B DIGITAL CONTROL CODE

Diqital average current mode control implementation in the TMS320F28027 Piccolo micro-controller

```
#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File
#include "f2802x_Device.h"
#include "f2802x_common/include/clk.h"
#include "f2802x_common/include/flash.h"
#include "f2802x_common/include/gpio.h"
#include "f2802x_common/include/pll.h"
#include "f2802x_common/include/wdog.h"
#include "f2802x_common/include/IQmathLib.h"
#include "f2802x_common/include/pie.h"
#include "f2802x_common/include/adc.h"
#include "f2802x_common/include/pwr.h"
#include "f2802x_common/include/pwm.h"
#include "f2802x_common/include/timer.h"
#include "math.h"

void pwm_Init_();
 //variable definitions begin
unsigned int CMPA=0;
unsigned int CMPB=0;
unsigned int TBPRD = 49;
```

```
float vref=3.3;
float error,error1;
float a = 0.3932;
float b = -0.0205;
float g = -1;
float h = 0.5858;
float d = 5.028;
float f = -3.486;
float sum,sum1,temp,temp1,iout,c,e,an1,an2,an3;
float max = 3;
float min =0;
float max1 =15;
float min1 =1.11;
float sum2;
float i; // d(n)
float i1;//d(n-1)
float err1;//e(n-1) which is the old error
float err;//e(n)

float ic; // d(n) for the current loop
float icc1;//d(n-1) for the current loop
float errc1;//e(n-1) which is the old error for the current loop
float errc;//e(n)

//variable definitions end

void globaldisable();
void globalenable();
void ADC_INIT_Fn();
void ADC_SETUP_Fn();
void Gpio_select(void);
void InitSystem(void);
void set_duty1(int x);
```

```
void set_duty2(int y);

CLK_Handle   myClk;
FLASH_Handle myFlash;
GPIO_Handle  myGpio;
PLL_Handle   myPll;
WDOG_Handle  myWDog;
PIE_Handle   myPie;
ADC_Handle   myAdc;
PWM_Handle myPwm1;
PWM_Handle myPwm2;
PWR_Handle myPwr;
TIMER_Handle myTimer;
CPU_Handle   myCpu;

//#include "f2802x_common/include/steps.h"

uint16_t Digital_Result1 =0;
uint16_t Digital_Result2 =0;
uint16_t Digital_Result3 =0;
interrupt void adc_isr(void)
{
    //discard ADCRESULT0 as part of the workaround to the 1st sample errata for
    Digital_Result1 = ADC_readResult(myAdc, ADC_ResultNumber_0);//vout
    Digital_Result2 = ADC_readResult(myAdc, ADC_ResultNumber_1);//template
    Digital_Result3 = ADC_readResult(myAdc, ADC_ResultNumber_2);//sensed current

    an1 = Digital_Result1 * 3.3/4096; //digital to analog conversion for sensed
    an2 = Digital_Result2 * 3.3/4096; //digital to analog conversion for sensed
    an3 = Digital_Result3 * 3.3/4096; //digital to analog conversion for sensed

    //voltage loop start//
```

```
error = vref-an1 ;
  //k= a*error;
  //p= b*error;
  sum = g*i + h*i1 + b*err1 + a*error;
  //sum = k-p;
  i =sum;
  i1 = i;//d(n-1) = d(n)
  err1 = error; //e(n-1) = e(n)
  temp =sum;
  if (temp>max)
  {
   temp=max;
  }
  else if (temp<min)
  {
   temp=min;
  }
  else{
   temp=temp;
  }
  //current loop start
   //iout=temp;
   sum1 = (temp)*(an2); //sum1 is isref
   //digital result2 is the sensed input voltage
   //q= an3*9.6; // scaling factor for the sensed current
   //sensor current is 0.9607V when input current is 4.6115A, therefore (4.6
   error1 = sum1-an3*9.6; //error input to the current controller
   //c=d*error1;
    //e=f*error1;
   sum2 = g*ic + h*icc1 + f*errc1 + d*error1; //input to current controller
   //sum3 = sum2*(-1);//inverted input to the current controller for when th
   //d1=sum2;
   //d2=sum3;
```

```
        ic = sum2;
        icc1 = ic; //d(n-1) = d(n)
        errc1 = error1;
        //i think vref = max
        if (sum2>max1)
        {
        sum2=max1;
        }
        else if(sum2<min1){
        sum2=min1;
        }
        else{
        sum2=sum2;
  }
        //if (sum3>max1)
        //{
        //sum3=max1;
        //}
        //else if(sum3<min1){
        //sum3=min1;
        //}
        //else{
        //sum3=sum3;
// }


         //set_duty1(sum2);
         //set_duty2(sum3);

         CMPA = sum2;
         PWM_setCmpA(myPwm1, CMPA);
         CMPB = 125-sum2; // this ensures the 180 degrees phase shift between the
         PWM_setCmpB(myPwm1, CMPB);// Wait for ADC interrupt
```

```
    ADC_clearIntFlag(myAdc, ADC_IntNumber_1);   // Clear ADCINT1 flag reinitiali
    PIE_clearInt(myPie, PIE_GroupNumber_10);// Acknowledge interrupt to PIE
    return;
}
void main(void)
{

// myClk = CLK_init((void *)CLK_BASE_ADDR, sizeof(CLK_Obj));
   //myFlash = FLASH_init((void *)FLASH_BASE_ADDR, sizeof(FLASH_Obj));
  // myGpio = GPIO_init((void *)GPIO_BASE_ADDR, sizeof(GPIO_Obj));
   // myPll = PLL_init((void *)PLL_BASE_ADDR, sizeof(PLL_Obj));
  //myWDog = WDOG_init((void *)WDOG_BASE_ADDR, sizeof(WDOG_Obj));
//  myPie = PIE_init((void *)PIE_BASE_ADDR, sizeof(PIE_Obj));
  // myAdc = ADC_init((void *)ADC_BASE_ADDR, sizeof(ADC_Obj));
  // myPwm1 = PWM_init((void *)PWM_ePWM1_BASE_ADDR, sizeof(PWM_Obj));
   //myPwr = PWR_init((void *)PWR_BASE_ADDR, sizeof(PWR_Obj));

   myAdc = ADC_init((void *)ADC_BASE_ADDR, sizeof(ADC_Obj));
     myClk = CLK_init((void *)CLK_BASE_ADDR, sizeof(CLK_Obj));
     myCpu = CPU_init((void *)NULL, sizeof(CPU_Obj));
     myFlash = FLASH_init((void *)FLASH_BASE_ADDR, sizeof(FLASH_Obj));
     myGpio = GPIO_init((void *)GPIO_BASE_ADDR, sizeof(GPIO_Obj));
     myPie = PIE_init((void *)PIE_BASE_ADDR, sizeof(PIE_Obj));
     myPll = PLL_init((void *)PLL_BASE_ADDR, sizeof(PLL_Obj));
     myTimer = TIMER_init((void *)TIMER0_BASE_ADDR, sizeof(TIMER_Obj));
     myWDog = WDOG_init((void *)WDOG_BASE_ADDR, sizeof(WDOG_Obj));
     myPwm1 = PWM_init((void *)PWM_ePWM1_BASE_ADDR, sizeof(PWM_Obj));
     myPwm2 = PWM_init((void *)PWM_ePWM2_BASE_ADDR, sizeof(PWM_Obj));
     myPwr = PWR_init((void *)PWR_BASE_ADDR, sizeof(PWR_Obj));

     globaldisable();
     WDOG_disable(myWDog);
```

```
      CLK_enableAdcClock(myClk);
      CLK_setOscSrc(myClk, CLK_OscSrc_Internal);  //Select the internal oscillato

      PLL_setup(myPll, PLL_Multiplier_10, PLL_DivideSelect_ClkIn_by_2);  // Setup

      globalenable();
    // Disable the PIE and all interrupts
      //PIE_disable(myPie);
      //PIE_disableAllInts(myPie);
      ADC_INIT_Fn();
      ADC_SETUP_Fn();

     // Perform basic system initialization

      GPIO_setMode(myGpio, GPIO_Number_0, GPIO_0_Mode_EPWM1A);
      GPIO_setMode(myGpio, GPIO_Number_1, GPIO_1_Mode_EPWM1B);

      CLK_disableTbClockSync(myClk);
      pwm_Init_();

      CLK_enableTbClockSync(myClk);

     // If running from flash copy RAM only functions to RAM
  /*  #ifdef _FLASH
     memcpy(&RamfuncsRunStart, &RamfuncsLoadStart, (size_t)&RamfuncsLoadSize);
    #endif
  */
    // PIE_enable(myPie);
      // Register interrupt handlers in the PIE vector table
//InitSystem();
//Gpio_select();
//InitPieCtrl();
//InitPieVectTable();
```

```
//EALLOW;
//PieVectTable.ADCINT1=& adc_isr;
//IER = 1;
//EINT;
//ERTM;
    while(1)
    {
       // Digital_Result1 = ADC_readResult(myAdc, ADC_ResultNumber_0);//vout
       // Digital_Result2 = ADC_readResult(myAdc, ADC_ResultNumber_1);//template
       // Digital_Result3 = ADC_readResult(myAdc, ADC_ResultNumber_2);//sensed c

        ADC_forceConversion(myAdc, ADC_SocNumber_0);
        ADC_forceConversion(myAdc, ADC_SocNumber_1);
        ADC_forceConversion(myAdc, ADC_SocNumber_2);
   }
}
void globaldisable()
{
  // Disable the PIE and all interrupts
  PIE_disable(myPie);
  PIE_disableAllInts(myPie);
  CPU_disableGlobalInts(myCpu);
  CPU_clearIntFlags(myCpu);
}

void globalenable()
{
  PIE_enable(myPie);
  // Register interrupt handlers in the PIE vector table
  CPU_enableInt(myCpu, CPU_IntNumber_10);  // Enable CPU Interrupt 1
  CPU_enableGlobalInts(myCpu);        // Enable Global interrupt INTM
  CPU_enableDebugInt(myCpu);     // Enable Global realtime interrupt DBGM
      // Enable XINT1 in the PIE: Group 1 interrupt 4 & 5
```

```
        // Enable INT1 which is connected to WAKEINT
        PIE_enableInt(myPie, PIE_GroupNumber_1, PIE_InterruptSource_XINT_1);
    CPU_enableInt(myCpu, CPU_IntNumber_1);

        // GPIO0 is XINT1, GPIO1 is XINT2
        GPIO_setExtInt(myGpio, GPIO_Number_12, CPU_ExtIntNumber_1);

        // Configure XINT1
        PIE_setExtIntPolarity(myPie, CPU_ExtIntNumber_1, PIE_ExtIntPolarity_RisingE

        // Enable XINT1 and XINT2
        PIE_enableExtInt(myPie, CPU_ExtIntNumber_1);
}
void ADC_INIT_Fn()
{
    ADC_enableBandGap(myAdc);
    ADC_enableRefBuffers(myAdc);
    ADC_powerUp(myAdc);
    ADC_enable(myAdc);
    ADC_setVoltRefSrc(myAdc, ADC_VoltageRefSrc_Int);
}
void pwm_Init_()
{
     CLK_enablePwmClock(myClk, PWM_Number_1);
     // Setup TBCLK
     PWM_setPeriod(myPwm1, TBPRD);    // Set timer period to 100kHz
     PWM_setPhase(myPwm1, 0x0000);    // Phase is 0
     PWM_setCount(myPwm1, 0x0000);    // Clear counter
     // Set Compare values
     // Setup counter mode
     PWM_setCounterMode(myPwm1, PWM_CounterMode_UpDown); // Count up and down
     PWM_disableCounterLoad(myPwm1);                     // Disable phase loading
     PWM_setHighSpeedClkDiv(myPwm1, PWM_HspClkDiv_by_2); // Clock ratio to SYSCLK
```

```
    PWM_setClkDiv(myPwm1, PWM_ClkDiv_by_1);
    // Setup shadowing
    PWM_setShadowMode_CmpA(myPwm1, PWM_ShadowMode_Shadow);
    PWM_setLoadMode_CmpA(myPwm1, PWM_LoadMode_Zero);
    // Set actions
    PWM_setActionQual_CntUp_CmpA_PwmA(myPwm1, PWM_ActionQual_Clear);      // Set
    PWM_setActionQual_CntDown_CmpA_PwmA(myPwm1, PWM_ActionQual_Set);  // Clear P

    PWM_setActionQual_CntUp_CmpB_PwmB(myPwm1, PWM_ActionQual_Clear);      // Set
    PWM_setActionQual_CntDown_CmpB_PwmB(myPwm1, PWM_ActionQual_Set);
    //CLK_enablePwmClock(myClk, PWM_Number_2);..
    // Setup TBCLK
    //PWM_setPeriod(myPwm2, TBPRD);   // Set timer period 801 TBCLKs..
    //PWM_setPhase(myPwm2, 0x0000);   // Phase is 0
    //PWM_setCount(myPwm2, 0x0000);   // Clear counter
    // Set Compare values
    // Setup counter mode
    //PWM_setCounterMode(myPwm2, PWM_CounterMode_UpDown); // Count up and down
    //PWM_disableCounterLoad(myPwm2);                     // Disable phase loadi
    //PWM_setHighSpeedClkDiv(myPwm2, PWM_HspClkDiv_by_10); // Clock ratio to SYS
    //PWM_setClkDiv(myPwm2, PWM_ClkDiv_by_1);
    // Setup shadowing
    //PWM_setShadowMode_CmpA(myPwm2, PWM_ShadowMode_Shadow);
    //PWM_setLoadMode_CmpA(myPwm2, PWM_LoadMode_Zero);
    // Set actions
    //PWM_setActionQual_CntUp_CmpA_PwmA(myPwm2, PWM_ActionQual_Clear);      // S
    //PWM_setActionQual_CntDown_CmpA_PwmA(myPwm2, PWM_ActionQual_Set);  // Clear
}
void ADC_SETUP_Fn()
{
 PIE_registerPieIntHandler(myPie, PIE_GroupNumber_10, PIE_SubGroupNumber_1, (int
  PIE_enableAdcInt(myPie, ADC_IntNumber_1);  // Enable ADCINT1 in PIE
  //Note: Channel ADCINA1  will be double sampled to workaround the ADC 1st samp
```

```
    ADC_setIntPulseGenMode(myAdc, ADC_IntPulseGenMode_Prior);                  //ADCI
    ADC_enableInt(myAdc, ADC_IntNumber_1);                                     //Enab
    ADC_setIntMode(myAdc, ADC_IntNumber_1, ADC_IntMode_ClearFlag);             //Disa
    ADC_setIntSrc(myAdc, ADC_IntNumber_1, ADC_IntSrc_EOC0);                    //setu
    ADC_setSocChanNumber (myAdc, ADC_SocNumber_0, ADC_SocChanNumber_A4);       //set
    ADC_setSocChanNumber (myAdc, ADC_SocNumber_1, ADC_SocChanNumber_A7);       //set
    ADC_setSocChanNumber (myAdc, ADC_SocNumber_2, ADC_SocChanNumber_A3);       //set
    ADC_setSocTrigSrc(myAdc, ADC_SocNumber_0, ADC_SocTrigSrc_Sw);//set SOC0 start
    ADC_setSocTrigSrc(myAdc, ADC_SocNumber_1, ADC_SocTrigSrc_Sw);//set SOC1 start
    ADC_setSocTrigSrc(myAdc, ADC_SocNumber_2, ADC_SocTrigSrc_Sw);//set SOC2 start
    ADC_setSocSampleWindow(myAdc, ADC_SocNumber_0, ADC_SocSampleWindow_7_cycles);
    ADC_setSocSampleWindow(myAdc, ADC_SocNumber_1, ADC_SocSampleWindow_7_cycles);
    ADC_setSocSampleWindow(myAdc, ADC_SocNumber_2, ADC_SocSampleWindow_7_cycles);
}
//void set_duty1( int x)
//{
// CMPA = x;
 //PWM_setCmpA(myPwm1, CMPA);    // Set compare A value
 //return;
//}
//void set_duty2( int y)
//{
// CMPA = y;
 //PWM_setCmpA(myPwm2, CMPA);       // Set compare B value
//}
```