Linearized differential current sensor in low-voltage CMOS

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Abstract

Purpose – This work improves upon the linearity of integrated CMOS current sensors used in switch mode power supply topologies, using a low cost and low voltage (less than 1.2 V) CMOS technology node. Improved sensor accuracy contributes to efficiency in switched supplies by reducing measurement errors when it is integrated with closed-loop control.

Approach – Integrated current sensing methods were investigated and CMOS solutions were prioritized. These solutions were implemented and characterized in the desired process and shortcomings were identified. A theoretical analysis accompanied by simulated tests were used to refine improvements which were prototyped. The current sensor prototypes were fabricated and tested.

Findings – Measured and simulated results that show improved linearity in current sensor outputs are presented. Techniques borrowed from analog amplifier design can be used to improve the dynamic range and linearity of current steered CMOS pairs for measuring current. A current sensor with a gain of 5 V/A operating in a 10 MHz switch mode supply environment is demonstrated.

Originality– This article proposes an alternative approach to creating suitable bias conditions for linearity in a SenseFET topology. The proposed method is compact and architecturally simple in comparison to other techniques.

Keywords: Micro-circuit technology, Semiconductor technology

Paper Type Research paper

1. Introduction

This paper presents a current-sensing circuit for non-inverting boost-buck switched mode dc-dc converter topologies. The circuit provides measurement output without a passive element in series with the reactive components of the supply. The circuit is implemented in a low-cost 130 nm 8hp BiCMOS process from IBM using CMOS only.

In self-powered integrated systems which include digital and RF sub-systems (Arshak *et al*. 2004; Chan *et al*. 2012), efficiency is necessary in order to comply with strict power constraints (Vuller *et al*. 2009). These types of integrated systems must also typically be affordable to produce and be compact (Sahu & Rincón-Mora 2004). In integrated switched mode boost-buck power supplies with closed loop control, efficiency is determined by device characteristics and control loop design. In fully integrated systems where reactive components underperform because of parasitic factors (Lee *et al*. 2011), accurate sensing and control are required for optimal operation.

Current mode control schemes measure the input current from the external energy source into the inductor of the boost-buck converter. The measured current is a key input parameter that steers the control loop; and the quality of this measurement directly influences the overall efficiency.

Sensing of the input current is either a direct measurement using an element in series with the primary inductor (typically a resistor), or an indirect measurement of some other circuit parameter (Forghani-zadeh & Rincón-Mora 2002; Forghani-zadeh & Rincón-Mora 2007).

The presented circuit is based on the SenseFET topology which infers a measurement without a series element by sampling the input current of the inductor in the boost-buck converter during every cycle. The sampled current is converted to a voltage for input into a control loop.

This paper presents a compact design with improved performance when compared to the standard SenseFET. The base SenseFET topology is presented and analyzed in the context of the 130 nm 8hp process. Shortcomings of this design are discussed, and improvements are proposed and implemented.

Improvements to the SenseFET design focus on reducing the effect of non-ideal transistor characteristics, such as channel length modulation, velocity saturation, and other short channel effects typical of deep sub-micron processes, on circuit performance. These improvements also focus on maintaining the bias conditions under which the circuit operates. The goal of these design changes is to improve the linearity of the SenseFET design within the constraints of the 130 nm 8hp process.

2. Problem definition and methodology

2.1 Problem definition

This paper addresses the problem of poor linearity of a known current sensing technique that has been implemented in a specific CMOS process.

2.2 Methodology

The development of a new variation of the SenseFET was motivated by the outcome of a study of integrated current-measuring techniques. This study formed part of a wider investigation into improving monolithic wireless sensor nodes in wireless sensor networks.

The SenseFET makes use of a single integrated resistive component which is easily integrated and requires no reactive components. The SenseFET topology also allows for a compact design with transistor aspect ratios less than ten. SenseFET circuits are often augmented with additional circuitry to allow the SenseFET to approximate the idealized operation.

In addition to the analytical and computational characterization of SenseFET fundamentals, the methodology considered several SenseFET variations from the literature. The methods employed in the literature were used to determine which fundamental aspects of SenseFET operation in these solutions would be most influenced when implemented in a specific low voltage, deep sub-micron process. The sensing methods employed in the body of published knowledge, include among others, the use of differential amplifier circuits to improve symmetry in the basic SenseFET topology. This study isolated shortcomings in these solutions and used device level analysis and simulation to formulate an alternative which is presented in this paper. This paper thus also uses the conventional method for implementing a SenseFET presented by Du (Du and Lee 2010) but illustrates shortcomings when this SenseFET was implemented in the chosen CMOS process.

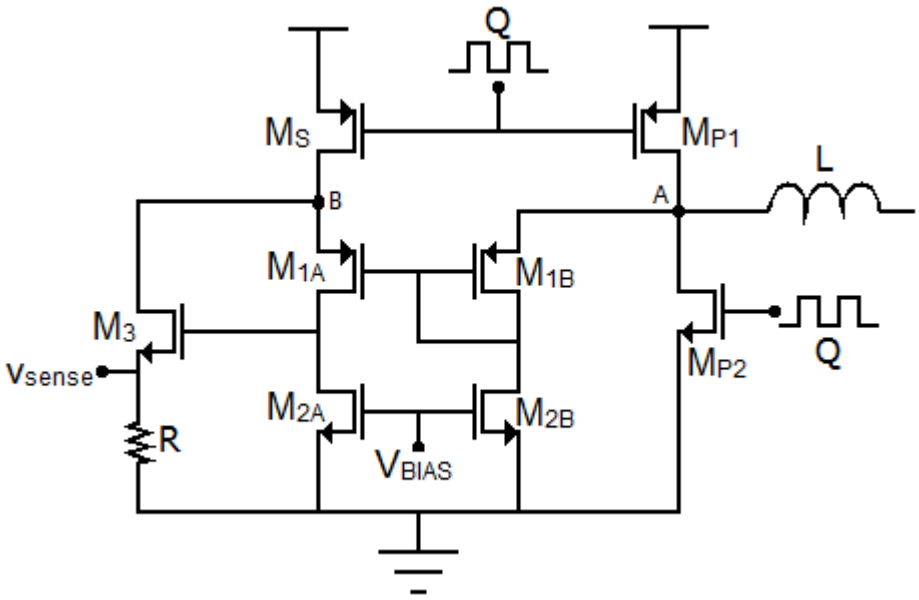
The simplified SenseFET topology was analyzed and simulated using the Virtuoso software suite from Cadence, in conjunction with process design kits from IBM for the 130 nm 8hp process. The Virtuoso software suite was also used to extract process parameters at the operating point of interest. The analysis results and process parameters were used to develop an improved variation of the SenseFET which was iterated and simulated before implementation. The designed prototype was manufactured by the MOSIS integrated fabrication service. The manufactured circuit was tested on a purpose-built, printed circuit board, which provided external test inputs, as well as reactive and passive components that were required for performance tests.

2.3 Standard sensor shortcomings

The improved sensor design is based on the operation of the simplified SenseFET in Figure 1, which samples a scaled current from inductor L on each charging cycle of the dc-dc conversion (Leung *et al*. 2005; Lee & Mok 2004). Transistor M_S has a scaled-down aspect ratio of the primary switch transistor M_{P1}. On each switching cycle M_S will provide a scaled variant of the current flowing through M_{P1}, provided that the voltage at nodes A and B is equal (Rao, Deng & Huang 2015).

The primary design choice is the aspect ratio of transistor M_S relative to power transistor M_{P1}. Both transistors are driven by the switch mode clock Q. M_S is chosen in such a way that $(W/L)_{P1} = K \cdot (W/L)_S$. Transistor pair M_1 has equal aspect ratio, with M_{1B} diode connected to force the voltage at node B to follow that of A. Matched transistor pair M_2 is for biasing.

Figure 1 Simple SenseFET implementation.



On every cycle (Q low) circuit operation is given by applying Kirchoff's current law (KCL) at nodes A and B:

$$i_{DSM_{P1}} = K i_{DSM_S} \tag{1}$$

$$i_L = i_{DSM_{P1}} - i_{DSM_{1B}} \tag{2}$$

$$i_{DSM_3} = i_{DSM_S} - i_{DSM_{1A}} \tag{3}$$

Since

$$i_{DSM_S} = \frac{i_L + i_{DSM_{1B}}}{K} \tag{4}$$

$$i_{DSM_3} = \frac{i_L}{K} + \frac{i_{DSM_{1B}}}{K} - i_{DSM_{1A}} \tag{5}$$

From Ohm's law:

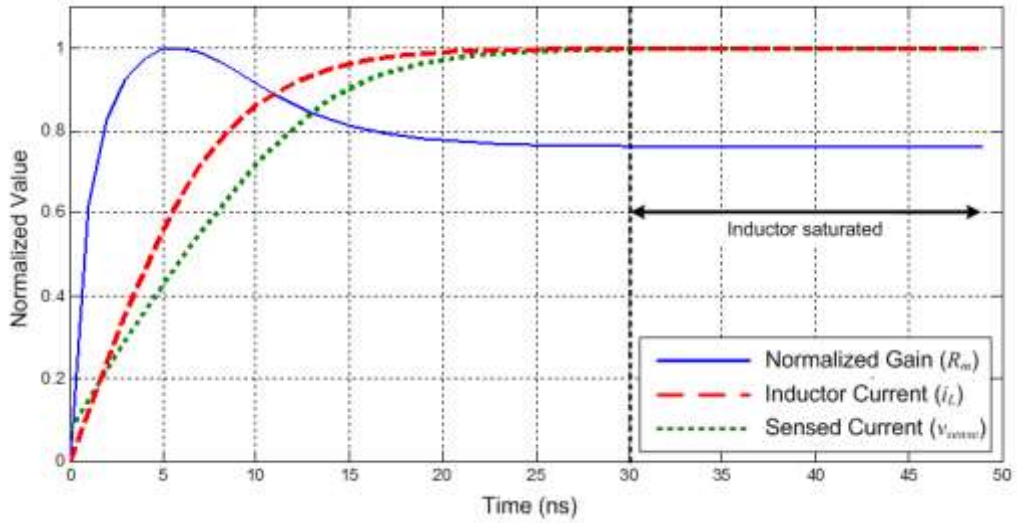
$$v_{sense} = R i_{DSM_3} \tag{6}$$

$$v_{sense} \approx R\left(\frac{i_L}{K} - i_{DSM_{1A}}\right) \tag{7}$$

If non–ideal effects are assumed to be negligible, then $i_{DSM_{1B}}/K$ becomes negligible and $i_{DSM_{1A}}$ remains constant because of bias transistor pair M_2. This yields an output v_{sense} that is directly proportional to the inductor current.

Implementing this circuit in the IBM 130 nm 8hp process yields the results shown in Figure 2. The switch mode converter and sensor was cycled at 10 MHz. V_{DD} is limited to 1.2 V by design, to prevent the gate oxide breakdown voltage being exceeded. The sensed current, actual current, and gain are normalized for the sake of comparison. The sensed and actual current for a single switching cycle are shown. These currents deviate from the simplified model derived from Figure 1 which predicts a scaled output with fixed offset. The transresistance (R_m) gain of the sensor is also shown and clearly indicates the nonlinearity of the sensor, with large deviation during the initial inductor current transient.

Figure 2 Simulated reference design performance over a 50 ns charging interval.



The non-linearity of the sensor during the initial current transient of the inductor is the source of a significant measurement error which only decreases once the inductor current approaches a steady state. The source of this non-linearity is the exclusion of non-ideal transistor effects from the simplified SenseFET design.

To improve the analysis, non-ideal device behavior is accounted for by analyzing the process characteristics within the design constraints, specifically the v_{DS}-i_{DS} relationship reveals a relatively low early voltage (V_A) with $V_A \approx 2$ V. The implication of this is that the assumption of negligible non-ideal effects is not valid, and must be included in the circuit analysis. Considering channel length modulation, re-analysis of the circuit in Figure 1 with respect to M_{1B} yields:

$$i_{DS} = \frac{k_p^{`}}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \tag{8}$$

$$\text{Since } v_{GS} = v_{DS} \text{ for } M_{1B} \text{ and } v_{SM_{1B}} = v_L \tag{9}$$

$$i_{DSM_{1B}} = \frac{k_p^{`}}{2}\left(\frac{W}{L}\right)_{M_{1B}}(v_{GS} - V_t)^2(1 + \lambda v_{GS}) \tag{10}$$

$$i_{DSM_{1B}} = \frac{k_p^{`}}{2}\left(\frac{W}{L}\right)_{M_{1B}}\left(v_G - V_t - L\frac{di_L}{dt}\right)^2\left(1 + \lambda\left(v_G - L\frac{di_L}{dt}\right)\right) \tag{11}$$

Equation (8) defines the current in M_{1B} when it operates in saturation. Non-ideal effects are approximated by $\lambda = 1/V_A$. For small λ the effect of v_{DS} on the current is small, but in this implementation $\lambda \approx 0.5$ and the second-order effects cannot be ignored. This coarse approximation, based on the 130 nm 8hp process models, aggregates the effects of channel length modulation and drain induced barrier lowering (DIBL) into a single parameter. The net effect of channel length modulation is an increase in i_{DS}. λ is inversely proportional to transistor length. If the length of the transistor is increased, then λ will decrease.

Similarly, (8) applies to M_{1A} and transistor pair M_2. Although v_{GS} of M_2 is fixed, variation of i_{DS} in each branch of the circuit results in noticeable and undesirable behavior when small-signal performance is considered.

If transistor pair M_2 is considered to be a differential pair with fixed input, then the small-signal gain is given by:

$$A_{M_2} = -gm\left(r_{oM_1} || r_{oM_2}\right) \tag{12}$$

$$\text{Where } r_o = \frac{V_A}{I_{DS}} \quad \text{and}$$

$$gm = \frac{k_n^{`}}{2}\left(\frac{W}{L}\right)_{M_{1B}}(v_{GS} - V_t)(1 + \lambda v_{DS}) \tag{13}$$

Equations (12) and (13) are both functions of V_A with (12) being a strong function of i_{DS}. This dominance manifests as an unbalanced operation of the differential pairs, as variance in i_{DS} causes the small- and large-signal parameters of the transistors to change throughout the measurement cycle.

This non-linear behavior is also significantly influenced by velocity saturation in M_{1B}. The approximate effect of velocity saturation on i_{DS} in M_{1B} is given by (Gray, *et al*. 2001):

$$i_{DSM_{1B}} \cong \frac{k'_p}{2\left(1+\frac{v_{GS}-V_t}{E_c L_{M_{1B}}}\right)}\left(\frac{W}{L}\right)_{M_{1B}}(v_{GS}-V_t)^2 \tag{14}$$

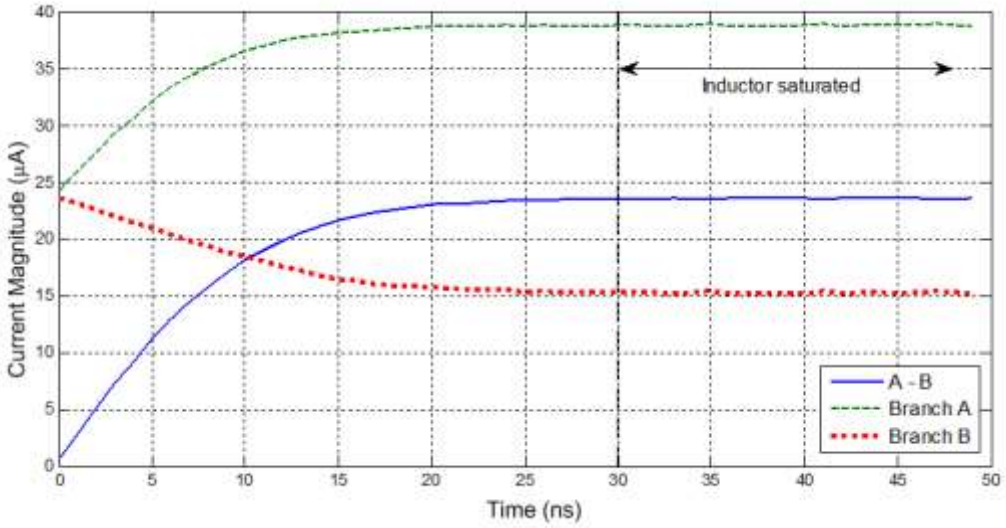
Where E_c = 1.5 × 10^6 V/m is the critical field strength at which velocity saturation becomes significant. Expanding (14) to include the effect of v_L yields:

$$i_{DSM_{1B}} \cong \frac{k'_p}{2\left(1+\frac{v_G-V_t-L\frac{di_L}{dt}}{E_c L_{M_{1B}}}\right)}\left(\frac{W}{L}\right)_{M_{1B}}\left(v_G-V_t-L\frac{di_L}{dt}\right)^2 \tag{15}$$

From (15) it can be seen that velocity saturation decreases $i_{DSM_{1B}}$ as predicted by the square-law model of (8). Equation (15) also shows that increasing $L_{M_{1B}}$ in order to reduce the product of $E_c L_{M_{1B}}$ would lead to impractical transistor lengths before the effect of velocity saturation is reduced. The dominance of velocity saturation negates any attempts to decrease channel length modulation by increasing $L_{M_{1B}}$.

Non-Ideal effects are prevalent in all the transistors in the SenseFET. The degree to which i_{DS} is affected by non-ideal characteristics is determined by influence of external stimulus on the non-ideal aspects of the transistor. The result of these non-ideal effects is seen when comparing the current in each branch during a cycle. Transistor pair M_1 behaves as a current mirror relative to pair M_2. If a large V_A is assumed, then the current in each branch should be equal in magnitude because of the shared gate voltages and high output resistance of each transistor. This is not the case and there is significant asymmetry between branches. Figure 3 shows a simulation of an asymmetric variance of branch currents.

Figure 3 Asymmetry of simple SenseFET branch currents.



3. Proposed solution

Figure 4 proposes a solution to the shortcomings of the simplified SenseFET. The circuit comprises two parts, namely the basic differential current sensing pair, and a secondary network that augments biasing transistor pair M_2. The purpose of the secondary network is to generate bias currents which are independent of variations in the inductor current i_L. By creating a robust biasing network, the voltage at nodes A and B can be made equivalent.

Transistor pairs M_3, M_4, and M_5 form a current-biasing network, where the effect of a small V_A and velocity saturation is diminished by isolating changes in the inductor voltage from the biasing network. By isolating the bias currents from external stimulus such as v_L, the variance introduced by non-ideal effects can be significantly reduced. In the circuit of Figure 1, branch bias currents are defined by pair M_1 and pair M_2. The new current-biasing network uses a topology that promotes symmetrical currents in each branch.

The advantage of the topology in Figure 4 over solutions proposed by (Du and Lee 2010) and (Lee and Hsu 2007) is that by using a folded cascode approach the topology can be implemented in processes with a maximum allowable V_{DD} of 1.2 V.

3.1 Circuit operation

Applying (8) to transistor M_{2B} of the simple sensor in Figure 1:

$$i_{DSM_{2B}} = \frac{k_n^{`}}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2\left(1 + \lambda\left(L\frac{di_L}{dt} - v_{DS1}\right)\right) \tag{16}$$

Equation (16) shows that the bias current generated by pair M_2 is susceptible to variation as v_L varies.

Applying KCL to the source of M_{2B} in Figure 4 yields:

$$i_{DSM_{3B}} = i_{DSM_{4B}} + i_{DSM_{2B}} \tag{17}$$

$$i_{DSM_{4B}} = i_{DSM_{5B}} \tag{18}$$

$$i_{DSM_{2B}} = i_{DSM_{3B}} - i_{DSM_{5B}} \tag{19}$$

Although (8) applies to transistor pair M_5, v_{DSM5} is a weak function of variations in v_L. This allows i_{DSM_5} to be controlled by a single biasing voltage, V_{BIAS2}.

Every additional transistor pair in a cascode configuration with M_1 and M_2 diminishes the effect of v_L on v_{DS} for pairs M_1 and M_2. By Kirchoff's voltage law (KVL) the sum total of v_{DS} over each cascode pair must be equal to the voltage at node A (or node B for the corresponding branch). The disadvantage of this approach is that it decreases the headroom available for v_{GS} with each additional transistor pair. The reduced headroom restricts the dynamic range of the sensor by limiting values of v_{GS} required to maintain each device in saturation.

This limitation is circumvented by using a folded cascode topology which allows for branch currents to be biased independently of v_L without limiting the headroom for v_{GS} of M_1 and M_2.

The gate voltages of transistor pairs M_4 and M_3 are both driven by v_{DSM5} with M_4 isolating M_5 from variations in v_{DSM2}. This allows the bias current in transistor pair M_2 to be set by pairs M_3, M_4, and M_5 from (16) to (19).

M_{4A} is diode connected to complement the functionality of M_1, which is to hold nodes A and B at the same voltage, by allowing each branch of the cascode to mirror the other.

The design of the improved SenseFET focuses on biasing which is independent of the inductor current being measured. The bias currents in the secondary network (M_3 – M_5) are chosen to be an order of magnitude larger than the current variance in the SenseFET (M_1, M_2, M_S). This reduces the magnitude of the variation in i_{DSM_1} caused by non-ideal device characteristics being modulated by the inductor current or voltage. The reduction in variation allows pair M_1 to hold nodes A and B at the same voltage more accurately, allowing the improved SenseFET to approach the ideal operation in (1) to (5).

Figure 4 Folded differential current sensor.

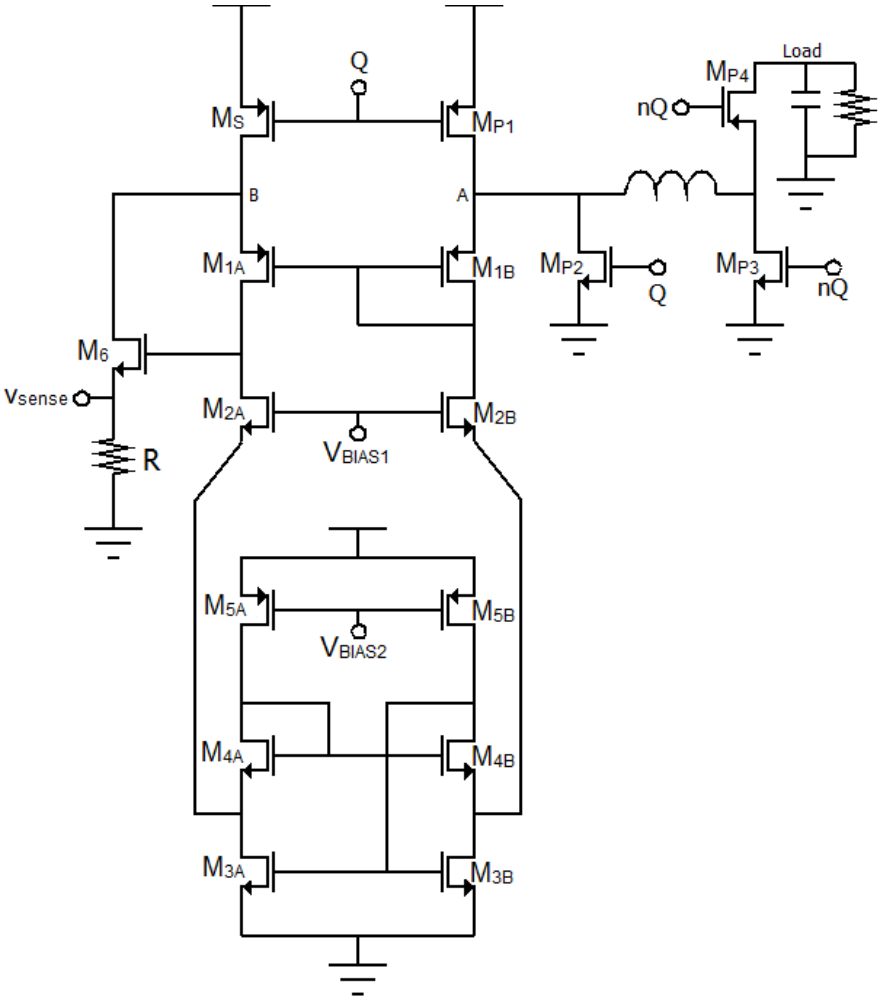


Figure 5 shows the currents in each branch of the differential sensor. Symmetry is not achieved, but a reduction in the delta between each branch is achieved.

Figure 5 Asymmetry of folded cascoded SenseFET branch currents.

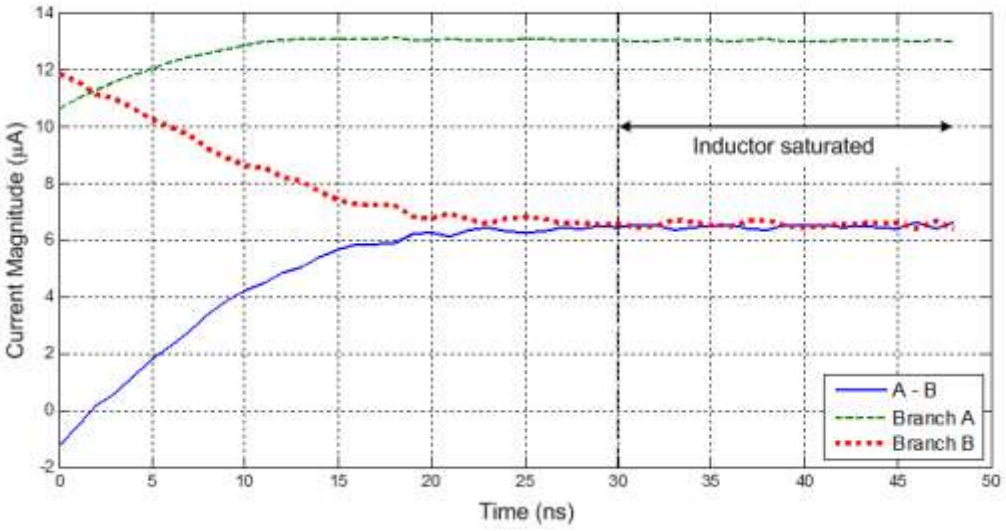
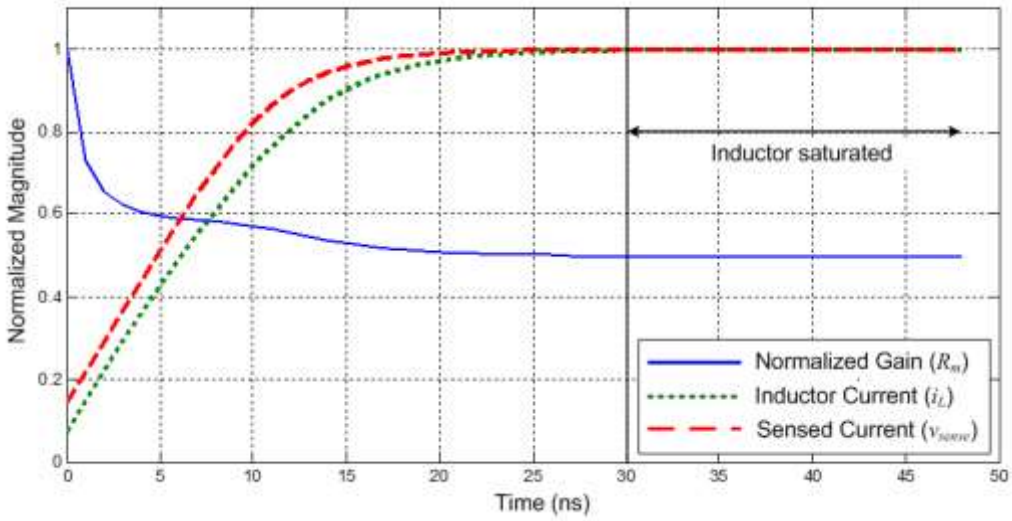


Figure 6 is a graph of the normalized R_m of the folded differential sensor. Figure 6 also shows the sensed current and actual inductor current. The peak in gain at the start of the cycle is attributed to data discontinuity at the start of the simulated cycle where the steady state inductor current is 0 A.

Figure 6 Folded differential current sensor gain performance over a single 50 ns charging cycle.



3.2 Implementation

The improved sensor was designed for implementation and prototyping in IBM's 130 nm 8hp BiCMOS process. Once the analysis and simulation of the improved SenseFET was completed, the SenseFET and test circuits were fabricated. The test circuit consisting of power transistors M_{P1} to M_{P4} were also included on the prototype silicon die. The required passive and reactive components for testing were off-chip.

3.3 Circuit design and layout

The effect of channel length modulation on each device was negated for initial designs. This effect varies significantly as a function of device operating parameters. Device aspect ratios were adjusted in the simulation phase of design.

According to (7), K is the scaling factor between transistors M_{P1} and M_S. A practical specific value of R is limited by a desire to keep the footprint of R conservative, relative to other circuit components to promote an overall compact design.

If K = 1000 then this allows for µA currents in the sensor circuit compared to the mA currents that will be measured. The mA range is derived from the maximum current that the inductor is able to conduct over the switching cycle. This current is given by (20).

$$i_{L\,Max} = \frac{v_L t}{L}\Big|_{t0}^{t1} \tag{20}$$

For a 1 µH inductor being cycled at 10 MHz this yields a maximum possible current of 600 mA with V_{DD} limited to V_{DD} = 1.2 V.

For R_m = 2, R = 2 kΩ from (7).

M_S and secondary bias transistor pair M_5 are designed such that:

$$I_{DSMS} = I_{DSM5} = 100\ \mu A \tag{21}$$

M_1 to M_4, and M_6 are chosen so that the required v_{GS} to keep the transistors in saturation is 100 mV higher than the device threshold voltage (350 mV) at a bias current of 100 µA.

Current-switching transistors M_{P1} to M_{P4} were chosen to have an aspect ratio of 4000, but after simulation there was no distinct difference in performance between aspect ratios of 1000 and 4000. Table I provides a summary of aspect ratios.

Figure 7 shows the prototyped sensor circuit layout. M_{P1} to M_{P4} are not shown. Transistors with wide aspect ratios have fingered gates and transistor pairs are grouped together. The final circuit and test circuitry were implemented on a 2.5 mm × 2.5 mm die shared with other research projects. The die is shown in Figure 8.

TABLE I Transistor aspect ratios.

Transistor	Aspect Ratio (W/L)	nm
M_{P1}, M_{P4}	1000	120000/120
M_{P2}, M_{P3}	666.6	80000/120
M_S	4	1600/400
M_1, M_2, M_3, M_4. M_6	6	720/120
M_5	8.5	1020/720

Figure 7 Cascode SenseFET layout.

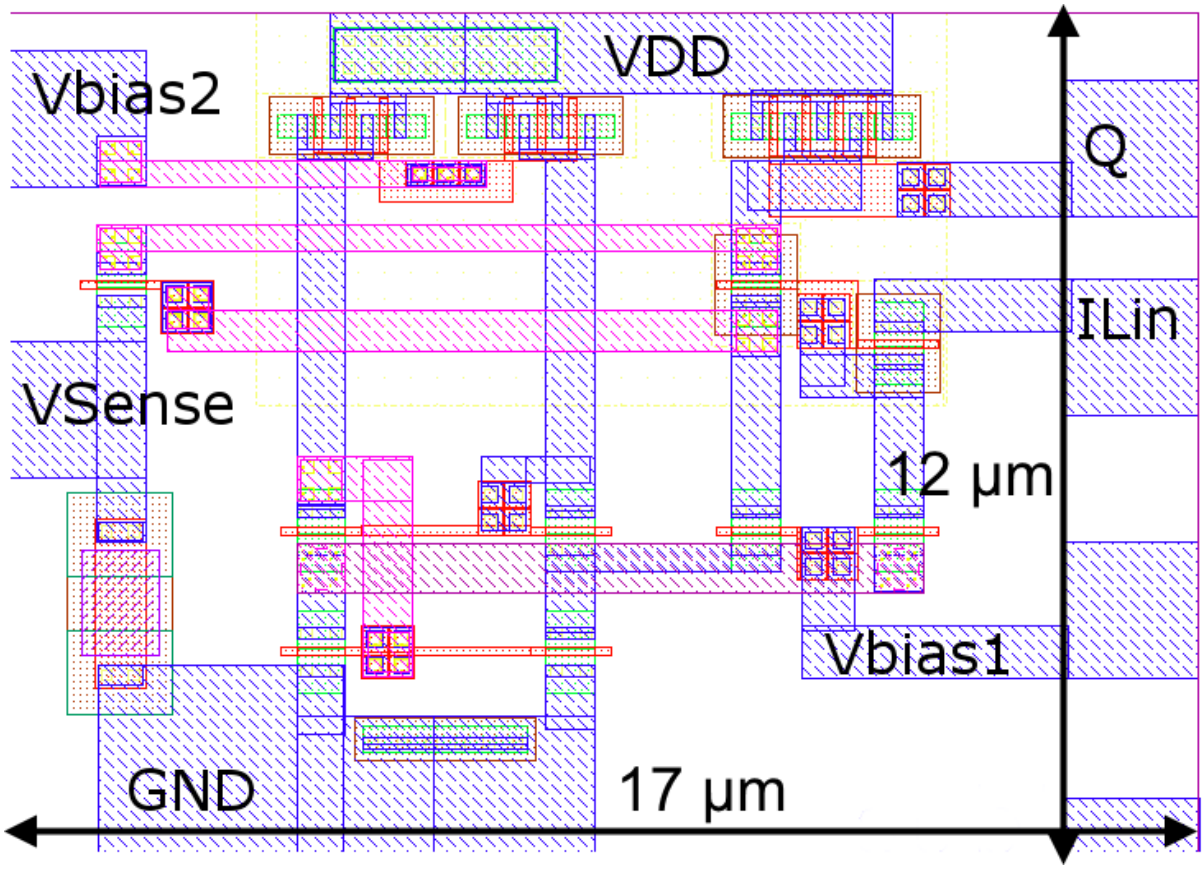
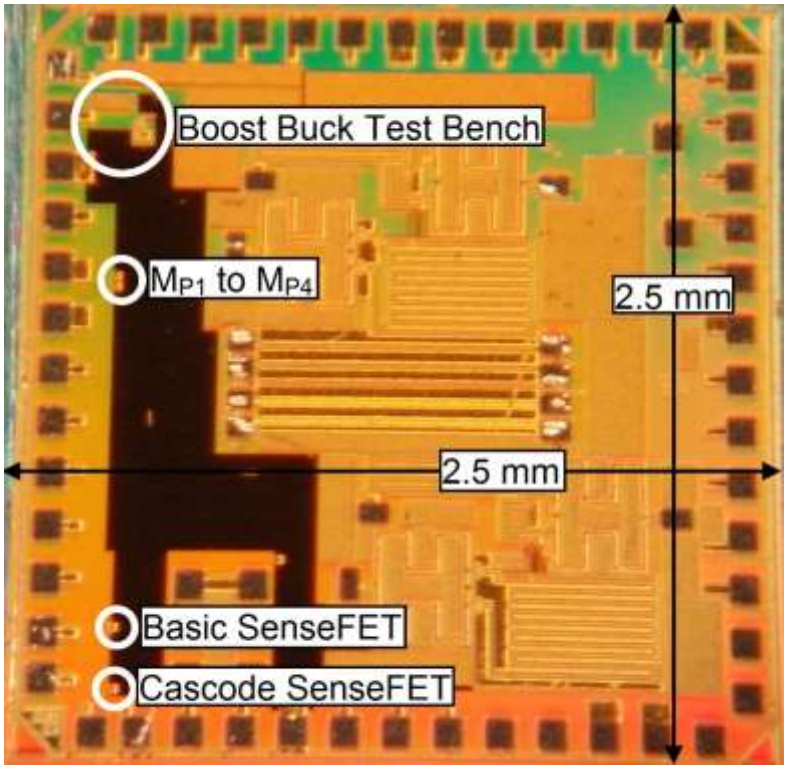


Figure 8 Optical photograph of manufactured die.



4. Results

4.1 Measurement setup

The manufactured integrated circuit (IC) containing the sensor circuit and test circuits was mounted on a test printed circuit board which exposed measurement points and provided connections for bias voltages, switching clocks, and external components in order to create the circuit of Figure 4.

4.2 Test procedure

External stimulus is summarized in Table II.

TABLE II Summary of test setup.

External Parameter	Value
V_{BIAS1}	400 mV
V_{BIAS2}	150 mV
L	L = 1 µH Q = 30 R_L = 0.5 Ω
RC Load	C = 1 µF R = 100 Ω
Q and nQ	10 MHz square wave Pk-pk: 1.2 V 50% duty cycle

v_{sense}, and the inductor voltage, v_L, were sampled and stored. Captured data were processed to extract R_m through each switching cycle. An example of captured data is shown in Figure 8.

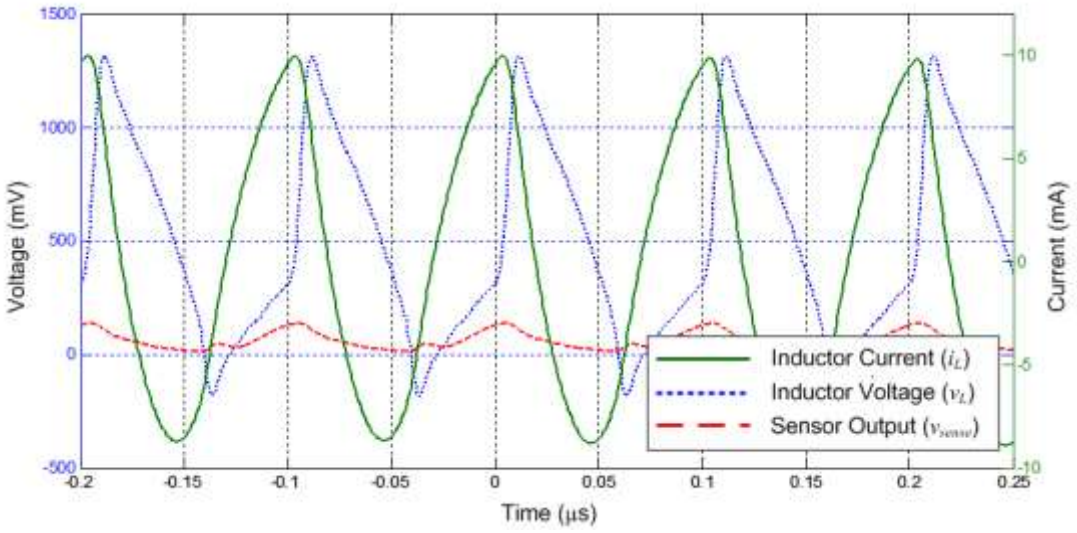
The improved SenseFET gain is simply:

$$R_m = \frac{v_{sense}}{i_L} \tag{22}$$

i_L is derived from v_L using numerical integration of the captured data. This is done by numerically evaluating (23).

$$i_L = \frac{1}{L}\int_{t0}^{t1} v(\tau)d\tau \tag{23}$$

Figure 9 Prototype sensor output and inductor voltage.



4.3 Results

Measurement results for the improved SenseFET in Figure 4 are presented in Figure 10. Three distinct traces indicate the sensor output (v_{sense}), the approximate inductor current (i_L), and transresistance gain (R_m). Discontinuities in the gain approximation occur at the charge and discharge boundary where the inductor current direction reverses. These discontinuities were limited during data processing.

The boost-buck converter in the test bench charges and discharges the inductor during each switching cycle. During the charging cycle, the inductor draws energy from V_{DD} and the RC load is unconnected. During inductor discharge, the energy stored in the inductor is transferred to the RC load. During this phase of the switching cycle the inductor current is reversed relative to the charging phase.

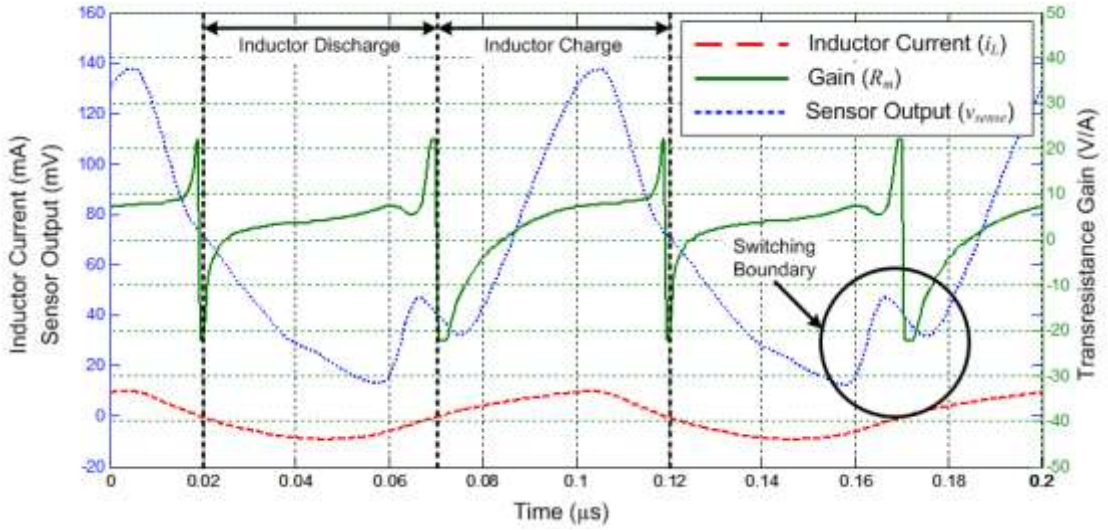
During the discharge phase the SenseFET operates with a gain of 5 V/A. The gain stabilizes once the SenseFET has recovered from the switching transient which is present at every switching interval boundary.

During the charge phase the achieved gain is similar to the discharge phase, 5 V/A, but the SenseFET circuit takes significantly longer to recover from the switching transient.

At every switching boundary, the inductor current reverses. The corresponding change in voltage over the inductor creates a negative voltage at the input of the current sensor (node A in Figure 4). This negative voltage drives transistor M_{1B} out of saturation into the triode region and eventually into the cut-off region. The resulting imbalance in currents between the differential pairs distorts the sensor output as shown in Figure 10.

The sensor only resumes normal operation once the input voltage is high enough for M_{1B} to operate in saturation.

Figure 10 Cascode SenseFET performance over a complete switching cycle.



5. Discussion and conclusion

5.1 Concessions

In order to compare the improved SenseFET to the simplified SenseFET design, both designs were implemented on the prototype die. The reference or simplified SenseFET on the prototype had no measureable output and was unfortunately non-functional. The improved SenseFET performance was therefore compared with expected outcomes from device level SPICE simulation in order to unequivocally quantify its performance in the absence of a reference.

5.2 Results analysis

The expected gain linearity of the sensor over a limited range of current inputs during the inductor charging cycle (from 0.1 to 0.115 µs in Figure 9) is comparative to that predicted by simulation in Figure 5. The gain in both cases varies by 10%.

The prototype delivered a gain of approximately 5 V/A. The designed gain is 2 V/A. The increase in gain is attributed either to M_6 in Figure 4 developing a larger i_{DS} than designed for or integrated resistor R having a higher resistance. Increased i_{DS} or increased R will result in a higher current to voltage conversion through integrated resistor R.

Beyond the 0.1 to 0.115 µs range the gain linearity deteriorates as M_{1B} is driven out of saturation.

The gain of the sensor during the discharging phase of the switching cycle does not suffer as severely as it does during the charging cycle. The negative voltage at the sensor input is absent, resulting in a greater range of operation when the current direction is reversed.

Both measurement phases suffer from gain deterioration from a lack of immunity to severe changes in voltage at the sensor input. The peak-to-peak voltage over the inductor also approached the oxide breakdown voltage of the process, which, in turn further reduced linearity of the sensor and test circuit after extended running times.

The variation in gain by 10% over approximately 50% of a charge or discharge cycle indicates that provided all devices in the improved SenseFET remain in the active region, an improvement in linearity is possible in comparison to the simplified design. The susceptibility of the transistors to be driven out of saturation by a significant increase in inductor voltage is a design problem which needs to be considered for future improvements.

5.3 Future improvements

Future development must address the significant effect of a negative input voltage at the sensor input. An additional input stage which limits the input voltage to prevent the differential pairs being driven out of saturation will be required.

The development of an improved SenseFET is motivated by the broader problem of how to improve the efficiency (and thus reduce costs) of monolithic wireless sensor network nodes. A significant requirement of such a sensor is an improvement in power conversion efficiency. An improved SenseFET can contribute to the power conversion efficiency by reducing the internal measurement error in a switched mode supply without the introduction of resistive element in series with the power inductor.

If the gain discontinuity present in the SenseFET at the switching boundaries is resolved, designers of monolithic switch mode supplies implemented in low voltage CMOS will have an accurate and fully integrated current sensing solution.

6. References

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