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Research Article

Oscillation-Based Test Applied to a Wideband CCII

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Oscillation-based testing (OBT) has been proven to be a simple, yet effective VLSI test for numerous circuit types. This paper investigates, for the first time, the application of OBT verification for second generation current conveyors (CCIIs). The OBT is formed by connecting the CCII into a simple Wien bridge oscillator and monitoring both the amplitude and frequency of oscillation. The fault detection rate, taking into account both the open and short circuit fault simulation analyses, indicates 96.34% fault coverage using a combination of amplitude and frequency output sensing in all technology corners. The only nondetected faults are short circuits between V_{DD} and V_{SS}, which can be detected using other techniques such as IDDQ testing. This method is found to be sensitive to resistor and capacitor process variation in the Wien bridge oscillator, but mitigating test steps are proposed.

1. Introduction

Despite the digital implementation of modern communication subsystems, analog front-ends and active filters are still used extensively in mixed-signal ICs. The second generation current conveyor (CCII) is an adaptable multifunction component that can be applied in a large number of analog circuits (such as active continuous time filters and all-pass networks) and has been the subject of intensive study for the last decade [1–4]. Most CCII-based circuits use only all-transistor CCIIs, resistors, and capacitors, making their use attractive compared to large on-chip inductors. Additionally, the component count of these structures is usually very low, further decreasing the area cost [1].

Given the prominent role CCIIs play in integrated systems, it would be prudent to define explicit test procedures for individual CCII elements as part of larger VLSI production testing. Due to large CMOS process tolerances as well as potential failure points, a nonintrusive testing procedure using a minimal number of input and output test vectors is necessary, especially in mass produced telecommunication systems on chip (SOC). Excellent reviews of analog IC testing can be found in [5, 6], highlighting various simulation-before-test and simulation-after-test techniques. It is, however, evident that most of these tests require multiple complex text vectors and swept DC or AC inputs. Some attempt at a formalized test of a CCII was made in [7], but the procedure is not exhaustive and the conclusions are not generally applicable. It depends significantly on the configuration used and on a very singular fault-set selection. The method requires sweeping an input voltage between a given range, making the procedure difficult to implement. As the method is analog, it is further complicated by the read-out (faulty/nonfaulty) of the produced test result.

In contrast, the oscillation-based test (OBT) technique, introduced in the early 1990s [8], is a vectorless technique that can be used either in offline testing or as the core of the so-called OBIST (Oscillation-Based Built-In-Self-Test). The principle of OBT is to convert the circuit under test (CUT) into an oscillator during the test phase by adding a feedback loop (either globally to the total CUT or locally to specific parts of it) to produce self-sustained oscillation monitored at an output. Faulty behavior is then indicated by deviation from the fault-free operation in either the frequency or the amplitude of the oscillations [9]. This method has been used extensively for operational amplifiers, filters, and data converters [8–10]. The benefit of this approach is that a single test (with a single output and no input vector) can detect multiple problems, thus reducing the number of test points and probe pads. OBT, therefore, avoids the problem of test vector generation, requires relatively simple and few measurement vectors, and generally does not require

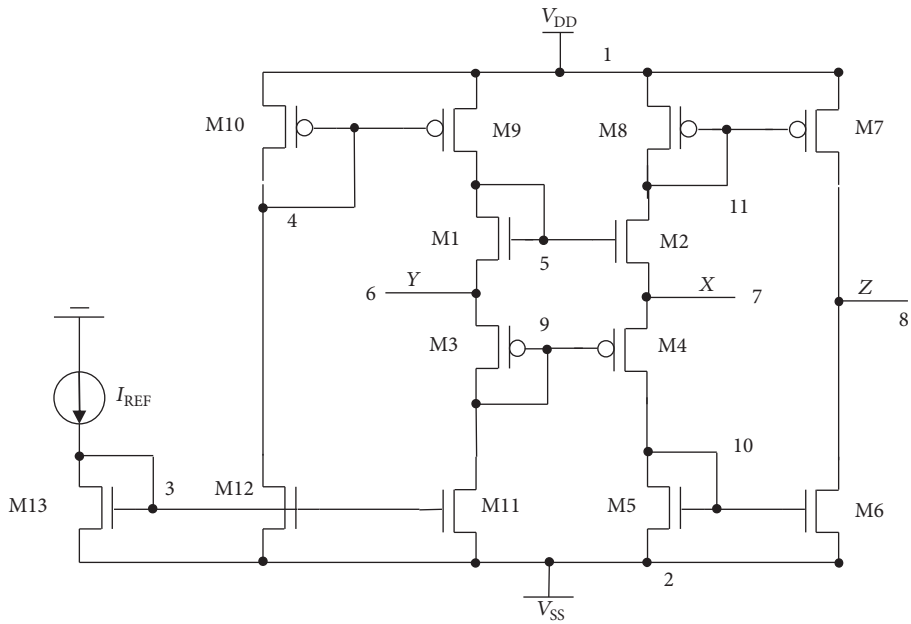

Figure 1: CCII circuit under test.

Table 1: Transistor sizing for the circuit under test.

Device name	W/L (μm)
M1, M2	14/0.35
M3, M4	37,8/0.35
Mxx PMOS	19/0.35
Mxx NMOS	7/0.35

intrusive circuit modification during the testing phase. These characteristics make OBT an appealing strategy.

In this work, we evaluate the suitability of OBT for testing CCIIs for the first time and develop a novel test procedure for CCIIs accordingly by making use of the linear characteristics in the feedback loop. The procedure is evaluated through fault simulation and fault coverage.

2. Circuit under Test

Among the numerous implementations available for CCII circuits in literature [1–4, 11] a positive Type II current conveyor is adopted and implemented in the AMS C35 0.35 μm CMOS process [12], as shown in Figure 1. The transistor sizing for the elements of Figure 1 is shown in Table 1.

In Figures 2 and 3 the output voltage as a function of frequency and its corresponding DC transfer characteristic with I_{REF} fixed to 10 μA are shown, respectively.

3. OBT Implementation

In order to perform an OBT on the circuit, the CUT must be placed into a self-sustained oscillation condition. The implementation of the OBT depends heavily on the characteristics of the system under test. The oscillator has to be designed and implemented based upon several considerations, such as the

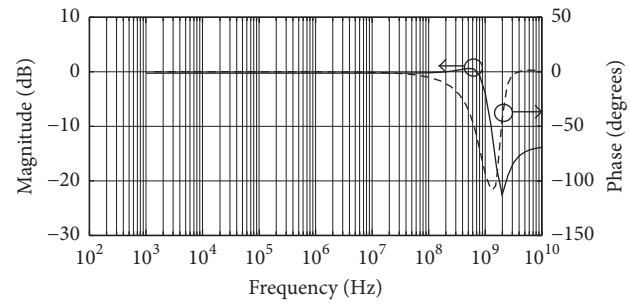

Figure 2: Output voltage and phase transfer characteristic.

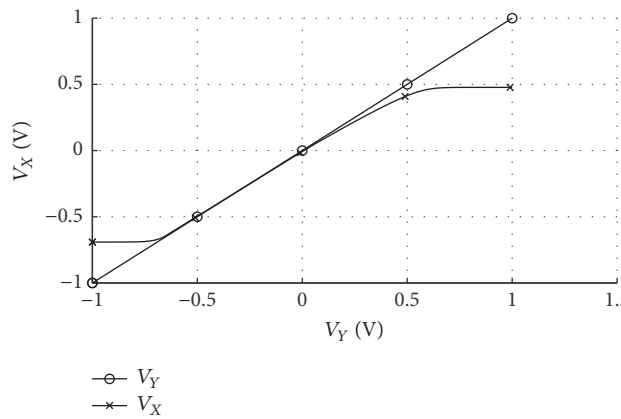

Figure 3: DC transfer characteristic.

characteristics of the system, the possibility of partitioning the CUT, the observable outputs, and the analog or digital nature of the signal. Consequently, the application of this strategy to each new class of circuits becomes a challenging

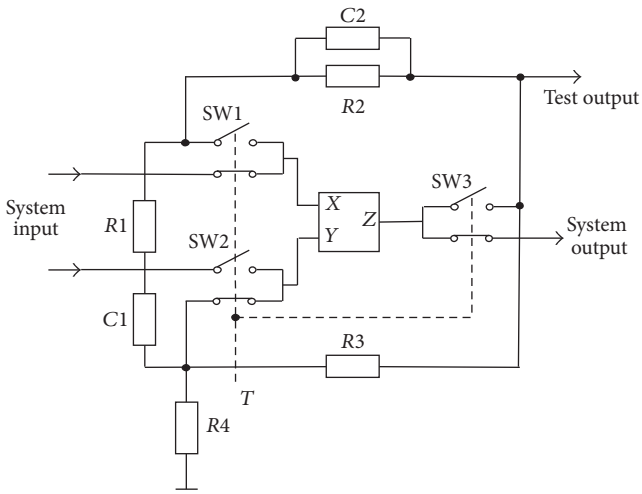

Figure 4: A voltage mode Wien bridge oscillator using a CCII+.

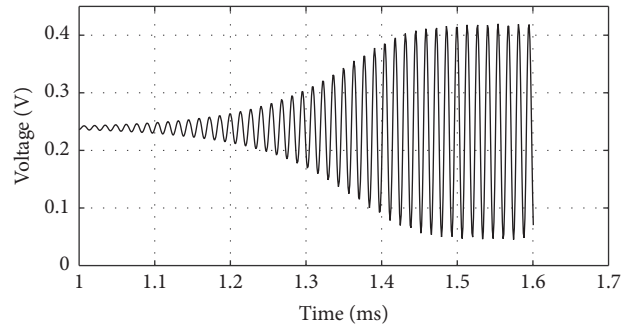

Figure 5: Oscillator output waveform of the operational (without faults) circuit.

Table 2: List of main and redundant nodes.

Reference node	Redundant nodes
1	M10_S, M9_S, M8_S, M7_S
2	M13_S, M12_S, M11_S, M5_S, M6_S
3	M13_D, M13_G, M12_G, M11_G
4	M10_D, M9_G, M10_G
5	M1_D, M1_G, M2_G
6	M1_S, M3_S
7	M2_S, M4_S
8	M7_D, M6_D
9	M3_D, M3_G, M4_G
10	M10_D, M10_G, M6_G
11	M8_D, M8_G, M7_G

task. Here, we apply the CCII as the gain element in a simple Wien bridge oscillator [13] as shown in Figure 4.

A number of additional components are required to switch the CCII into an oscillator test circuit. Since the CCII only has three terminals, this is easily accomplished by 3 pairs of switches, shown as SW1, SW2, and SW3 in Figure 4. In this way, the CUT itself is not modified to establish an oscillating output, making the OBT integration minimally invasive and, therefore, limiting the signal degradation in normal operating mode. The selection of signal path switches with adequate electrical performance is critical, as these remain connected to the CUT in both OBT and normal operating modes. The switches should be chosen to have on and off characteristics as close to the ideal (short circuits and open circuits, resp.) as possible.

In Figure 4, SW1, SW2, and SW3 are controlled by test signal T, which isolates the CUT from the rest of the circuit and connects it to the testing circuitry and test output in order to perform the test.

The resonant condition of this oscillator circuit is given by

$$s^2 C_1 C_2 R_1 R_2 + s\left[C_1 R_1 + C_2 R_2 + C_1 R_2 \frac{(R_1 - R_4)}{2R_3}\right] + 1 + \frac{R_2}{2R_3}. \quad (1)$$

For the sake of simplicity, the selections $C_1 = C_2 = C$ and $R_1 = R_2 = R_3 = R$ are made. With this simplification, the oscillation frequency can be calculated as

$$\omega_0 = \sqrt{\frac{3}{2}}\frac{1}{CR}. \quad (2)$$

Figure 5 shows the output waveform of the CCII-based oscillator with $C = 0.2\,\mu$F and $R = 10\,$kΩ. I_{REF} is kept at 10 μA as before. Under these conditions, the circuit reaches a final, stable oscillating condition within 1.5 ms at $f_0 = 75$ kHz with ±35 m V_{pp} output swing. This will be the comparison reference when simulating faults. Selecting different values of R and C do not affect the test procedure (or coverage) other than changing the nominal value of f_0.

The conventional OBT procedure is applied [14], whereby the circuit is switched into this oscillating condition and its output voltage amplitude and oscillation frequency are compared to that of the nonfaulty output in Figure 5.

4. Fault Modeling

Traditionally, the efficiency of OBT has been evaluated at a structural level by using single-catastrophic and single-deviation fault models. In this way, it is possible to use the well-known metric of fault coverage for qualifying the test.

In this work, we focus on catastrophic faults at both device and circuit level, thereby evaluating the efficiency of OBT for the faults that may cause severe failures in the circuit. Working from the schematic, an exhaustive fault list is generated, considering only catastrophic faults. This fault list includes all possible open and short circuit faults of transistors, with only the gate contact open fault omitted from analysis. The analysis is further extended to short faults at the circuit level. This extends the fault coverage to all probable faults and allows comparisons with other published results.

The CUT has 11 nodes, as numbered in Figure 1, with the schematically redundant ones listed in Table 2. The reference node and its schematically redundant subnodes are connected at the same potential, making it impossible to

Table 3: Short circuit fault results for all the five technology corners.

Tech corner	N1-N2		N4–N11		N6–N8	
	Δf (%)	ΔV_{pp} (%)	Δf (%)	ΔV_{pp} (%)	Δf (%)	ΔV_{pp} (%)
FF	2,05%	−8,69%	21,11%	185,35%	−3,42%	240,96%
FS	0,27%	39,42%	23,84%	154,12%	−3,40%	200,16%
SF	1,13%	−56,43%	16,83%	159,10%	−6,37%	211,71%
SS	−2,47%	0,71%	20,04%	129,33%	−5,69%	171,85%
TT	0,53%	−0,55%	20,94%	158,88%	−4,24%	207,59%

detect behavioral differences between them. For this reason, only the reference nodes of Table 2 (with the suffix "S," "D," or "G" in the node names referring to the source, drain, or gate, resp.) are considered for short fault simulations. In this way, we consider 527 potential short circuit faults (considering all redundant nodes) and 26 open circuit faults (considering only drain and source contacts on the transistors).

Schematically redundant subnodes are, of course, not physically redundant nodes, as the CUT may produce different outputs for open faults at different schematically redundant nodes. Therefore, for open faults, all nodes in this table are considered, excluding the gate open contact fault as is pointed out previously.

Fault simulations are carried out using SPICE, with the technology rules of AMS C35 process.

As the CUT has tuning capability through variation of IREF, parameter drift of nominal TT (Typical, Typical) conditions is usually compensated for postproduction. Under these conditions, the fault coverage for only the TT operating case would be representative of devices operating anywhere within the four corners (FF, FS, SF, and SS). However, tuning each CUT before testing could be, in some cases, excessively time consuming and thus impractical for exhaustive application. One way to avoid this time loss is simply to perform the test without tuning the circuit (though tuning or prior characterization of R and C in the OBT may be necessary, as discussed in Section 5). In order to prove the effectiveness of this idea, the test coverage is evaluated in simulation for all five cases (TT, FF, FS, SF, and SS) in Table 3, for a fixed $I_{REF} = 10\,\mu$A, using as reference for percentage calculation of the amplitude and frequency of the nonfaulty oscillation circuit with TT parameters. This is done to ensure, firstly, that circuits with acceptable parametric drift are not incorrectly detected as faulty and, secondly, that faulty circuits with acceptable parametric drift are still rejected by the OBT. Corner analysis is opted for, as opposed to Monte Carlo analysis, as it has been shown to identify more extreme variation from nominal operating conditions associated with interdie process variation than what is produced by a typical Monte Carlo analysis (which is more suited for intradie variation) [15–17].

As has been proposed in previous literature on OBT [8–10, 14] open circuit faults are modeled by a 10 MΩ resistor, while short circuit faults are modeled by a 10 Ω resistor. It is assumed here that a fault is detected when the oscillation frequency or amplitude falls outside of a tolerance band of ±5% from the nominal values simulated in the TT case. This is in keeping with the state-of-the-art in OBT techniques [14] and also allows for nonfaulty FF (which features a +2,39% increase in f_0 compared to the TT simulated case), FS (−0,34% f_0 compared to the TT), SF (+1,01%), and SS (−2,28%) circuits to pass the test.

Table 3 presents the simulation results for short circuit faults that do not result in a loss of oscillation output altogether, as was the case with all open circuit faults. It should be noted that only one fault of each schematically redundant fault set is presented. In this way, all injected faults giving a nonoscillating condition are not presented in this table, and thus the corresponding faults are considered to be detected. The open circuit faults table is not presented because all these faults are detected through complete loss of oscillation.

From Table 3, the remarkable efficiency of OBT applied to this circuit becomes evident. Of the 527 injected faults, only a few (short circuits between V_{DD} and V_{SS}) are not observable in the test. This is shown to be true, not only for the TT case, but also for all technology corners. This particular fault can, however, easily be detected with a simple IDDQ test. Furthermore, with the exception of V_{DD}-V_{SS} short circuit, all faults are detectable with amplitude measurement alone. It should be noted that some works [7] exclude from the fault list those faults that are known to be nondetectable with the methodology used. If the same principle is applied here and V_{DD}-V_{SS} short circuit faults are excluded from analysis, 100% fault coverage could be claimed. It is further noted that the oscillation outputs (f_0 and V_{pp}) of a faultless CUT are within the allowable ±5% variation under all operating corners.

5. Process Variation in R and C

In the preceding discussion, the method was shown to operate across all NMOS and PMOS corner variations of the all-transistor CUT, assuming perfect knowledge of R and C used in the attached Wien bridge oscillator. To analyse the impact of RC process variation on test coverage, a corner variation simulation of the RC components with a nominal-corner CUT is performed, with the resulting variation of f_0 and V_{pp} as shown in Figures 6 and 7.

These results indicate that a circuit operating in one of the nonnominal RC process corners would invalidate the test coverage in Table 3, as a large percentage of correctly operating circuits would produce f_0 or V_{pp} outside the ±5% variation threshold.

It is, however, evident from our preceding analysis that the OBT method is agnostic to the specific values of f_0 or V_{pp}, rather relying on known nominal values as determined by the specific RC corner. Knowledge of this corner (which may be

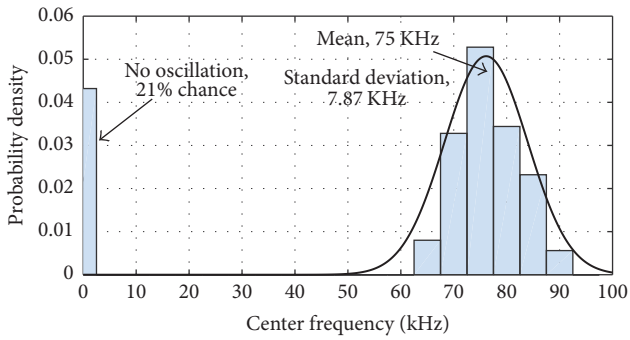

Figure 6: Center frequency variation for various process corner variations of *RC*.

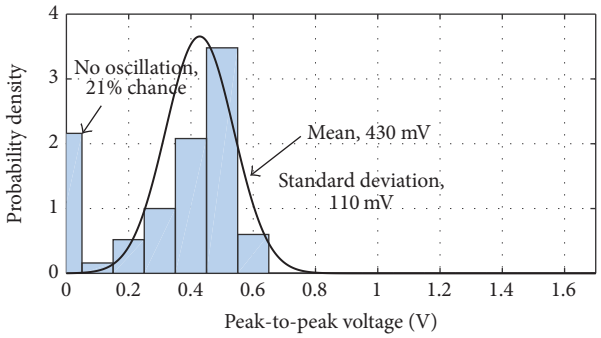

Figure 7: V_{pp} variation for various process corner variations of *RC*.

readily obtained by including probed *R* and *C* measurements, as is already commonly done in CMOS fabrication) is sufficient to recalibrate the nominal operating conditions and boundary thresholds for the OBT test.

Alternatively, *R* and *C* may be made tunable by using triode-region and varactor MOS devices, respectively. After tuning the *RC* constant to the desired value, the OBT test procedure can be carried out as described.

6. Evaluation of Short Circuit and Open Circuit Impedance Values

The state-of-the-art in OBT testing [8–10, 14] uses 10 Ω resistors to represent short circuit faults and 10 MΩ resistors to represent open circuit faults. As open and short circuits on-chip may assume a wide variety of impedance values [18], it would be prudent to analyse the effect of substituted impedance value variation on the OBT technique.

To validate these substituted impedance choices, two representative faults (one a short circuit between N6 and N8 and one an open circuit at the drain of M1) are simulated in the TT technology corner, for various resistance choices, as shown in Figures 8 and 9.

The measured outputs f_0 and V_{pp} show no variation for short circuit representations as high as 1 kΩ, two orders of magnitude higher than the selected value of 10 Ω. Similarly, the nonoscillating faulty circuit only resumes oscillation if the open circuit fault impedance is reduced to below 100 kΩ, two orders of magnitude lower than the selected value of 10 MΩ.

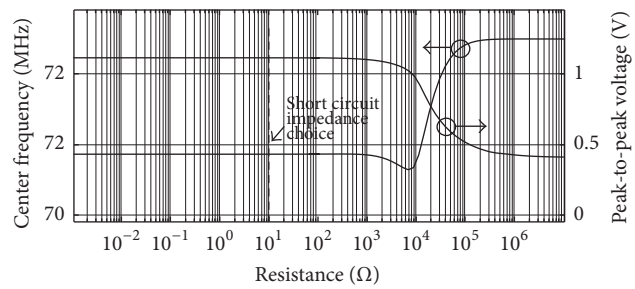

Figure 8: Center frequency and peak-to-peak variation for various choices of short fault resistances for circuit fault N6–N8.

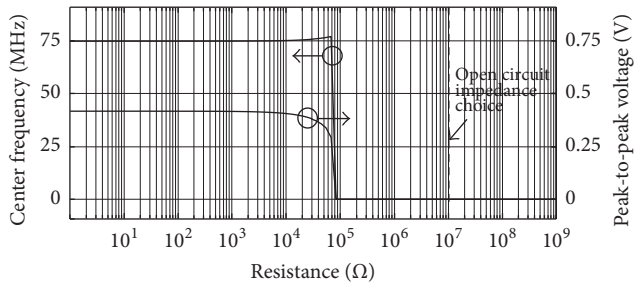

Figure 9: Center frequency and peak-to-peak variation for various choices of open fault resistances for circuit fault drain of open circuited M1.

It is clear, from these analysis, that the OBT test coverage remains valid for a wide range of actual fault impedances on-chip.

7. Conclusions

An OBT scheme has been applied to a CCII+ circuit for the first time. For evaluating OBT in this context, we adopted catastrophic fault models at both device and circuit level. The fault simulation results show 96.34% fault coverage that could be improved to achieve 100% by including additional IDDQ testing. This is consistent with other works [7] but with much easier implementation. It is also shown that OBT can correctly detect faults and pass nonfaulty circuits in all five CMOS technology corners, without the need of tuning the circuit, strongly simplifying the procedure by reducing the testing time. It is further shown that the previously applied 10 Ω and 10 MΩ impedance values to represent short circuits and open circuits are "safe" choices, with the OBT only suffering from degraded accuracy for short circuit impedances of above 1 kΩ or open circuit impedances below 100 kΩ.

The method is, however, shown to be sensitive to process variation in the values of *R* and *C* used in the Wien bridge oscillator. This can be mitigated by establishing a priori knowledge of the *R* and *C* process corners through measurement and recalibrating the nominal test values of f_0 and V_{pp} accordingly without loss of test coverage. The problem may be circumvented altogether by incorporating a tunable *RC* feedback network into the OBT circuit, though this would increase the test complexity and cost.

Future work will include comparison of the fault coverage in different CCII-based oscillators with respect to component count, fault coverage, and influence on nominal operating conditions. Replacing the sinusoidal output with a Schmitt trigger oscillator [1] will also be investigated, as this may allow for wideband fault finding using output harmonic analysis.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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References

[1] R. Senani, D. R. Bhaskar, and A. K. Singh, *Current Conveyors: Variants, Applications and Hardware Implementations*, Springer International Publishing, Berlin, Germany, 2015.

[2] N. Pandey, P. Kumar, and J. Choudhary, "Current controlled differential difference current conveyor transconductance amplifier and its application as wave active filter," *ISRN Electronics*, vol. 2013, Article ID 968749, 11 pages, 2013.

[3] A. M. Ismail and A. M. Soliman, "Wideband CMOS current conveyor," *Electronics Letters*, vol. 34, no. 25, pp. 2368-2369, 1998.

[4] S. Ben Salem, M. Fakhfakh, D. S. Masmoudi, M. Loulou, P. Loumeau, and N. Masmoudi, "A high performances CMOS CCII and high frequency applications," *Analog Integrated Circuits and Signal Processing*, vol. 49, no. 1, pp. 71–78, 2006.

[5] L. S. Milor, "A tutorial introduction to research on analog and mixed-signal circuit testing," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 10, pp. 1389–1407, 1998.

[6] A. Grochowski, D. Bhattacharya, T. R. Viswanathan, and K. Laker, "Integrated circuit testing for quality assurance in manufacturing: history, current status, and future trends," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 8, pp. 610–633, 1997.

[7] A. S. Emara, A. H. Madian, H. H. Amer, and S. H. Amer, "High coverage test for the second generation current conveyor," in *Proceeding of the IEEE International Conference on Electronics, Circuits, and Systems, (ICECS '15)*, pp. 429–432, IEEE, Egypt, 2015.

[8] K. Arabi and B. Kaminska, "Oscillation-test strategy for analog and mixed-signal integrated circuits," in *Proceedings of the 14th IEEE VLSI Test Symposium*, pp. 476–482, IEEE, Princeton, NJ, USA, 1996.

[9] K. Arabi and B. Kaminska, "Testing analog and mixed-signal integrated circuits using oscillation-test method," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, no. 7, pp. 745–753, 1997.

[10] K. Arabi and B. Kaminska, "Oscillation-test methodology for low-cost testing of active analog filters," *IEEE Transactions on Instrumentation and Measurement*, vol. 48, no. 4, pp. 798–806, 1999.

[11] U. Kač and F. Novak, "All-pass SC biquad reconfiguration scheme for oscillation based analog BIST," in *Proceedings of the 9th IEEE European Test Symposium, (ETS '04)*, pp. 133–138, IEEE, Corsica, France, 2004.

[12] S. B. Salem, A. Fakhfakh, M. Loulou, P. Loumeau, and N. Masmoudi, "A 2.5 V 0.35 μm CMOS current conveyor and high frequency high-Q band-pass filter," in *Proceedings of the 16th International Conference on Microelectronics, (ICM '04)*, pp. 328–333, Tunisia, 2004.

[13] A. Soliman and A. Elwakil, "Wien oscillators using current conveyors," *Computers & Electrical Engineering*, vol. 25, no. 1, pp. 45–55, 1999.

[14] P. Petrashin and C. Dualibe, "OBT implementation on Gm-C filters without self-tuning capability," in *Proceedings of the IEEE International Symposium of Circuits and Systems, (ISCAS '11)*, pp. 2521–2524, Rio de Janeiro, Brazil, 2011.

[15] P. I. Vaz and G. I. Wirth, "Design and comparative performance simulation of RHBD inverter cells in 180–nm CMOS," in *Proceedings of the 30th Symposium on Microelectronics Technology and Devices, (SBMicro '15)*, IEEE, Salvador, Brazil, 2015.

[16] V. M. M., R. Paily, and A. Mahanta, "A new PVT compensation technique based on current comparison for low-voltage, near sub-threshold LNA," *IEEE Transactions on Circuits and Systems. I. Regular Papers*, vol. 62, no. 12, pp. 2908–2919, 2015.

[17] S. Choi, T. Na, J. Kim, J. P. Kim, S. H. Kang, and S.-O. Jung, "Corner-aware dynamic gate voltage scheme to achieve high read yield in STT-RAM," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 9, pp. 2851–2860, 2016.

[18] M. Renovell, J. M. Gallière, F. Azaïs, and Y. Bertrand, "Modeling gate oxide short defects in CMOS minimum transistors," in *Proceedings of the 7th IEEE European Test Workshop, (ETW '02)*, pp. 15–20, IEEE, Greece, 2002.