CONDUCTED EMC MODELLING IN MODERN DC-DC POWER CONVERTERS

by

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SUMMARY

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Keywords: Conducted EMC, conducted EMI, common-mode, differential-mode, LISN, accreditation, component proximity, DC-DC conversion, components modelling, EMI modelling, LISN

Conducted Electromagnetic Compatibility (EMC) is studied. High-density high-switching frequency modern power converter conducted Electro-Magnetic Interference (EMI) for low power applications, within the automotive and handheld applications, have been analysed. The noise source and path were modelled with accurate conducted Electro Magnetic Compatibility (EMC) noise levels comparable to accredited MIL-STD-461F noise measurements (100 kHz to 10 MHz) and expanded to 100 MHz. Common-mode conducted emissions in the high frequency band (beyond 30 MHz), were shown to appear as radiated emissions. A general lumped element high frequency analyses model was developed and verified utilising different analysis packages for accuracy, affordability and ease of use. Furthermore, the common-mode and differential-mode signals were separated digitally from the recorded Line Impedance Stabilising Network (LISN) data. These separations were verified for accuracy with a wideband LINDGREN EMC high frequency current probe.

Conducted noise effects of multilevel, multiphase and synchronous converters were investigated. In addition, the effects of very high switching frequencies on noise levels are presented. In addition, the effect of combining electrically conductive and non-conductive polymer heatsinks reducing common-mode noise was investigated. This will be shown to be a viable and very effective possible solution to reduce the increased common-mode noise levels due to higher switching frequencies.

OPSOMMING

GELEIDENDE EMV MODELLERING IN MODERNE GS-GS KRAGOMSETTERS

deur

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Sleutelwoorde: Geleidende EMV, Geleidende EMS, Gemeenskaplike modus, Differensiaalmodus, Akkreditasie, Komponent Nabyheidseffekte, GS-GS Omsetters, Komponent Modellering, EMV Modellering, LISN

Geleidende Elektromagnetiese Steurings (EMS) is ontleed vir moderne draagbare kragomsetters met hoë pakkingsdigthede sowel as hoë skakelfrekwensies. Die bron van die geraas asook die voerpad is gemodelleer en die resulterende geraasvlakke is vergelykbaar met Elektromagnetiese Versoenbaarheid (EMV) opstelling soos vervat in MIL-STD-461F (100 kHz tot 10 MHz) maar die ontleding daarvan is uitgebrei tot by 100 MHz. Daar is verder bewys dat die gemeenskaplike modus bokant 30 MHz uitstraalvlakke toon. 'n Algemene hoë frekwensie stroombaan elementmodel is ontwikkel en ontleed. Die resultate van verskillende analiseringspakkette is vergelyk met die werklike metings wat betref akkuraatheid, bekostigbaarheid en gemak vir die gebruiker as kriteria. Verder is die gemeenskaplike modus- en differensiaalseine digitaal geskei van die Lynimpedansie Stabiliseeringsnetwerk (LISN) data. Die akkuraatheid van die skeidingstegniek is vergelyk met metings van 'n wyeband LINDGREN EMV hoë frekwensie stroomtaster.

Die geraaseffekte van multivlak en multifase asook gesinchroniseerde omsetters is verder ondersoek. Die gevolge van baie hoë skakelfrekwensies op geraasvlakke is ook ontleed en verduidelik. Verder is die gebruik van ‘n termies-geleide polimeer hitteput ondersoek met die oog op die vermindering van gemene modus geraas. Dit bewys dat polimeer hitteputte 'n lewensvatbare en effektiewe oplossing bied om die verhoogde gemenemodus geraasvlakke te verminder.

LIST OF ABBREVIATIONS

ABM	Analog Behavioural Model
ACEC	Advisory Committee on Electromagnetic Compatibility (International Electrotechnical Commission; Switzerland)
ANSI	American National Standards Institute
Aux.	Auxiliary
BGA	Ball Grid Array
CDN	Coupling/Decoupling Network
CE	Conducted Emissions (MIL-STD-461-F)
CEN	Comité Européen de Normalisation (French: European Committee for Standardization)
CENELEC	Comité Européen de Normalisation Électrotechnique (French: European Committee for Electrotechnical Standardisation)
CISPR	Comité International Spécial des Perturbations Radioélectriques (Special International Committee on Radio Interference; est. 1934)
CNC	Computer Numerical Control
.csv	Comma Separated Values (datafile)
Cu	Copper
CSIR	Counsel of Scientific and Industrial Research
DCB	Direct Copper Bond
DC-DC	Direct Current to Direct Current
DCE	Defence Conducted Emission (DEF STAN 59-411)
DEF STAN	Defence Standard (UK)
DIN	Deutsches Institut für Normung eV (Institute for Standardization; similar to US ANSI)
DoD	Department of Defence (USA)
DUT	Device Under Test

EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESL	Effective Series Inductance
ESR	Effective Series Resistance
ETSI	European Telecommunications Standards Institute (France)
EUT	Equipment Under Test
eV	eingetragener Verein (registered association)
FEA	Finite Element Analysis
FCC	Federal Communications Commission
FM	Frequency Modulation
GaN	Gallium Nitride
GPIB	General Purpose Interface Bus
HF	High Frequency (3 MHz to 30 MHz)
IEC	International Electrotechnical Commission (Geneva, Switzerland)
IEEE	Institute of Electrical and Electronics Engineers
IET	Industrial Engineering Technology
ISO	International Organisation for Standardisation
IT	Information Technology
ITU	International Telecommunication Union
JESTPE	Journal of Emerging and Selected Topics in Power Engineering
LED	Light Emitting Diode
LISN	Line Impedance Stabilisation Network
MathCAD	Mathematical Computer Aided Device Software Package
MATLAB	Matrix Laboratory Software Package
NATO	North Atlantic Treaty Organization

NTIA	National Telecommunications and Information Administration
PC	Private Computer
PCB	Printed Circuit Board
PDN	Passive Distribution Network
PSIM	Power Simulation Package
PWM	Pulse Width Modulation
QP	Quasi-Peak
R&S	Rohde&Schwarz
RTCA	Radio Technical Commission for Aeronautics
SiC	Silicon Carbide
SPICE	Simulation Program with Integrated Circuit Emphasis
STANAG	Standardization Agreement (for NATO)
TC	Technical Committee
.TNO	Transient Numeric Output (Spectrum Software File)
USA	United States of America
USB	Universal Serial Bus
VF	Vector Fitting
VHF	Very High Frequency (30 MHz to 300 MHz)
VG	Verteidigungs Geräte (Defense Structure)
via	Vertical Interconnected Access

LIST OF SYMBOLS

A	Waveform Amplitude [V]
A_c	Core Cross Section [m^2]
A_{cu}	Copper Area [m^2]
A_t	Tab Area [m^2]
A_v	Amplifier Gain
A_w	Wire Area [m^2]
B_{max}	Maximum Magnetic Flux Density [T]
b	PCB Trace Thickness [m]
α	Damping Coefficient
K	Cathode
C_0	Low Frequency Capacitance [F]
C_{cg}	Collector-Gate Capacitance [F]
C_{Diode}	Diode Capacitance [F]
C_{ds}	Drain-Source Capacitance [F]
C_{gd}	Gate-Drain Capacitance [F]
C_{ge}	Gate-Emitter Capacitance [F]
C_{ge}	Gate-Emitter Capacitance [F]
C_{gs}	Gate-Source Capacitance [F]
C_{H0}	Heatsink-Zero-Volt-Plane Capacitance [F]
C_{HC}	Heatsink-Chassis Capacitance [F]
C_{HD}	Heatsink-Diode Capacitance [F]
C_{HM}	Heatsink-MOSFET Capacitance [F]
C_H	Heatsink Total Capacitance [F]
C_{in}	Input Capacitance

C_{iss}	Input Transfer Capacitance [F]
C_j	Junction Capacitance [F]
C_{LEAD}	Power Lead Capacitance [F]
C_M	Miller E|ffect Capacitance [F]
C_{MD}	MOSFET-Diode Capacitance [F]
C_n	Complex Fourier Expression
C_{oss}	Output Transfer Capacitance [F]
C_{out}	Output Capacitance [F]
C_{PCB}	PCB Capacitance to Ground [F]
C_{rss}	Reverse Transfer Capacitance [F]
C_P	Parallel Capacitance [F]
C_p	Package Capacitance [F]
C_{Plate}	Parallel Plate Capacitance [F]
D	Duty Cycle [%]
D1	Component Identification: Diode
D_H	Diameter Helmholtz Coil
D_M	Density of conducted material [$g.cm^{-3}$]
d	Diameter of Wire [m]
d_i	Insulator Thickness [m]
δ	Unit Impulse Function
e	Percentage winding eddy current loss
ε_0	Permittivity of air, 8.854×10^{-12} [F/m]
ε_r	Relative Permittivity
F	Short Circuit Current Factor
f_{prf}	Parallel Resonant Frequency [Hz]

f_s	Switching Frequency [Hz]
f_{srf}	Series Resonant Frequency [Hz]
φ	Magnetic Flux [Wb]
H	Magnetic Field [A/m]
H_X	Magnetic Field in X-Direction [A/m]
h	Distance / Height [m]
h_s	Specific Heat of Conductor Material [J/gK]
θ	Angle [°]
θ_T	Temperature rise [K]
I	Current [A]
i_D	Diode Current [A]
I_{CM}	Common Mode Current [dBµA]
I_{DM}	Differential Mode Current [dBµA]
J	Winding current density in [A/m^2]
j	Complex Notation $\sqrt{-1}$
k	Heat Transfer Coefficient [W/m^2-K]
L	Inductance [H]
L1	Component Identification: Inductor
L_{0V}	Zero-volt Trace Inductance [H]
L_{ce}	Collector-Emitter Inductance [H]
L_{PCB}	PCB Trace Inductance [H]
L_d	Drain Inductance [H]
L_{Diode}	Diode Inductance [H]
L_e	Emitter Inductance [H]
L_{ESL}	Equivalent Series Inductance [H]

L_g	Gate Inductance [H]
L_{ge}	Gate-Emitter Inductance [H]
L_{GND}	Ground Lead Inductance [H]
L_{IN}	Input PCB Inductance [H]
L_{Lead}	Power Lead Inductance [H]
L_{OUT}	Output PCB Inductance [H]
L_p	Package Inductance [H]
L_s	Source Inductance [H]
L_{SK}	Source to Cathode Trace Inductance [H]
ℓ	Length [m]
ℓ_{cu}	Copper Wire Length [m]
ℓ_e	Magnetic Path Length [m]
λ	Wavelength [m]
m, n	Real Values
N	Turns
p	Arbitrary Point
p_n	n^{th} Pole
ρ	Resistivity of conducted material [Ω.m]
Q	Quality Factor
Q1	Component Identification: MOSFET
q	Heat Flux [W/m^2]
r_d	Diode Resistance[Ω]
R	Resistance [Ω]
R_{ESR}	Equivalent Series Resistance [Ω]
R_0	On Resistance[Ω]
R_g	Gate Resistance[Ω]

R_{gd}	Gate-Drain Resistance[Ω]
R_{gs}	Gate-Source Resistance[Ω]
R_H	Radius Helmholtz Coil [m]
R_{Load}	Load resistor [Ω]
R_P	Parallel Resistance [Ω]
R_S	Series Resistance [Ω]
ρ	Resistivity [Ω-m]
ρ_{cu}	Resistivity of Copper [Ω-m]
r	Radius [m]
r_n	n^{th} Residue
S	Surface Area [m^2]
S_L	Surface Area of Loop [m^2]
s	Distance [m]
s11	Return-loss Scattering Parameters
s21	Transfer Scattering Parameters
σ	Conductivity [S/m]
σ_{cu}	Conductivity of Copper [S/m]
T_S	Switching Period [s]
t_f	Fall Time [s]
t_r	Rise Time [s]
τ	On-Time [s]
u	Coil Wire Bundle Diameter [m]
μ_r	Relative Permeability
V_0	Output Voltage [V]
V_b	Battery Voltage [V]
V_{CM}	Common Mode Voltage [V]

V_D	Diode Switching Voltage [V]
V_{DM}	Differential Mode Voltage [V]
V_{IN}	Converter Input Voltage [V]
V_M	MOSFET Switching Voltage [V]
V_{OUT}	Converter Output Voltage [V]
V_P	Peak Voltage [V]
V_{PP}	Peak-to-Peak Voltage [V]
V_{OV}	Zero Line Voltage [V]
V_X	LISN Port 1 Voltage [dBµV]
V_Y	LISN Port 2 Voltage [dBµV]
w	Width [m]
ω_r	Ringing Angular Frequency [rad/s]
$\Delta\omega$	Delta Angular Frequency [rad/s]
X_C	Impedance Real [Ω]
Z_{CM}	Common-Mode Impedance [Ω]
Z_D	Diode Impedance [Ω]
Z_{DM}	Differential-Mode Impedance [Ω]
Z_C	Capacitor Impedance [Ω]
Z_L	Inductor Impedance [Ω]
Z	Impedance [Ω]
Z_0	Characteristic Impedance [Ω]
ΔZ	Delta Impedance [Ω]

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CHAPTER 1 INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Context of the problem

Electromagnetic interference (EMI) can be described as any unwanted electromagnetic energy that interferes with the operation of a device either generated by the device itself or received by other devices nearby. The electrical or electronic device or system needs to be able to operate without interfering with other systems, and must have the ability to operate as intended within a specific electromagnetic environment. We can quantify the electromagnetic noise of a device as conducted and radiated emissions from the device as well as conducted and radiated susceptibility to the device. International standards and regulations govern these levels to be within certain limits, and is a requirement to conform to in the open marketplace.

The current publications on conducted Electromagnetic compatibility (EMC) analysis mostly simplifies converter circuits and thus can achieve only accurate results below about 1 MHz, as typically seen in [1]. Better accuracies are seen with simplified noise path circuit models considering switching transient modelling [2], but accurate switching waveforms are only available when measured on the end-product. Some references use a trapezoidal waveform with simplified noise path models, but high frequency accuracy is then compromised. It will be desirable to perform conducted emission modelling and measurement up to 100 MHz. This can easily be achieved by careful design of parasitic circuit models and by the measuring equipment normally found in a power electronics laboratory, to analyse conducted emission up to the point where radiation effects starts occurring. While modelling conducted EMC with lumped element SPICE circuit analysis, spectral results are usually not presented over the entire conducted band due to inaccuracies and the difficulty to obtain. Results of only a small portion of the band are presented in [3]. In [4] a common-mode model is offered as well as high frequency impedance measurements up to 100 MHz, whereas the actual model results are fairly

accurate compared to the measurements up to 1 MHz, thereafter large discrepancies appear of more than 20- 30 dBμV. Furthermore, the predicted common-mode follows the measurement values only up to 300 kHz, thereafter fails to follow any measured result. Accurate high frequency models, up to 100 MHz are not available. The decomposition into the common- and differential-mode currents, necessary for optimal filter design, is normally done by complex analog radio frequency (RF) circuitry splitting and combining techniques, providing inaccurate results due to the handling of sensitive high frequency signals as well as impedance issues [5]. Setting up high frequency EMI current coils provides very good results, as in [6], but these instruments are not always readily available in the laboratory. Digital splitting by signal processing should be possible when simultaneous digital recordings of the LISN noise currents are made. Some equations found in literature for the decomposition in common-mode and differential-mode noise, mostly sited from an early publication in [7], provide inaccurate results. Performing accurate measurements, supplemented with first principle equation extraction, a 6 dB discrepancy was found, that highlights the need to clarify these equations. Although in [8], a current probe was used enabling the correct splitting of common- and differential-mode noise, but no comparative simulation results were presented. Furthermore, splitting the common- and differential-mode noise digitally by using the LISN, verifying the equations thereof, is not seen in literature. The measurement of conducted EMI noise with a wideband digital acquisition technique, (e.g. GHz digital Oscilloscope) and consequent signal processing as described in [9] is rarely seen. In most measurements, EMI receivers are used, and due to the dwell-time and frequency binning principle, is a very time-consuming exercise. The conducted EMC environment is in urgent need to clarify the modelling environment and provide an instinctive modelling mechanism to design for EMC, and rid itself from the ‘black art’ principle as well as trial-and-error [4] filter design.

The EMI management of a power converter should be an integral part of the converter design process. As the EMI verification is normally done when the product is at its final stage and qualification tests are underway, redesign at this stage can extend the crucial time-to-market date. For this reason proper modelling, of both EMI noise generation and propagation in power converters is of absolute importance right from the start of the design

phase. Numerical predictions of the electromagnetic behaviour prior to prototyping help reduce post prototyping electromagnetic compliance risk, costly redesigns and subsequent modifications [10]. It is thus of utmost importance to try and model the electromagnetic compatibility concurrently with the power processor design stage.

Power electronic designers are in need of an accurate and practical EMI modelling and prediction method suitable for use as a design tool [11]. The complexities of electromagnetic noise generation and propagation mechanisms make modelling prediction difficult. It depends on many variables, for example, component density, placement position, lead length, track layout, and the subsequent interaction with the environment under which the converter is to operate. An understanding of the converter behavior can assist in eliminating the EMI problems at the design stage rather than by excessive filtering. Understanding conducted EMI behavior will also substantially influence packaging density and cost as low frequency conducted noise requires large filter components. These large filter components are not only physically large but have enormous parasitics and consequently poor high frequency performance [12].

The project proposed here is to analyse and model the mechanisms of conducted electromagnetic noise originating from densely packaged components in DC-DC converters. The proposal also includes the identification of typical EMI sources, and a study of their coupling mechanisms. A case study of a selected power converter will illustrate the typical techniques for dealing with conducted noise. The study will further show how an iterative process between the theoretical and practical results will improve the accuracy and understanding of the conducted EM noise mechanisms, and in this way manage, as well as suppress EMI noise in a systematic way.

1.1.2 Research gap

The approach to conducted EMC modelling is usually to simplify the circuit so as to provide for an easier analysis method. These simplifications make it difficult to predict high frequency effects. When SPICE circuit modelling is used, the extraction of the parasitic elements does not receive the proper attention, as the switching elements do play

a large role in the conducted EMC levels [13]. Recently, in [14], equivalent parasitic model extraction by vector fitting is taken to the extreme, creating complex equivalent noise circuit models from the end-product, accurately modelled to 10 MHz. These complex equivalent circuit models seem not to relate to the functionality of the power circuit, or to the switching waveform slope information and high frequency effects that is crucial in high frequency modelling.

Power converter designers are in need of an EMC modelling and design methodology at reasonable cost. So often, power converters are designed without proper attention being given to EMC related issues. Standard recipes are normally followed during the design process, and the EMC tests are only done when the design is complete. Failing this test, modifications need to be performed and in a worst case, redesign. In a market where time and cost is of utmost importance, this is seen as a high risk. By designing for EMC at the initial design stages, optimal components can be selected, layout can be optimised and by accurate modelling and design, the accredited EMC tests can be executed with confidence

1.2 RESEARCH OBJECTIVE AND QUESTIONS

It would be useful to develop an EMC design methodology suited for the power electronics designer, knowing that through design, the applicable conducted EMC levels can be achieved. A conducted emission test bench will be designed, tested and calibrated up to at least 100 MHz, so as to see if radiated emissions start to emerge. The conducted test is a much easier test to perform in a laboratory.

Power converter designers very often see EMC design as a burden, as it can in some cases be very difficult and frustrating. Currently, the EMC modelling should form part of the converter design, so the method should be intuitive, easy to perform and provide accurate results. Questions that need to be answered are:

- Is it possible to accurately model conducted EMC without using expensive and complex EMC modelling packages?

- Is it possible to construct a LISN and consequently a test bed to be able to accurately measure conducted emissions up to 100 MHz?
- Is it possible to accurately measure conducted EMC in a development laboratory with commonly available instruments, such as a digital oscilloscope and signal generator?
- What is the accuracy in digital recording of the noise levels compared to measurement by a traditional EMC spectrum analyser?
- Can conducted emissions be split digitally by recording data from the LISN ports, into common-mode and differential-mode noise signals so as to provide inputs for optimal filter design?
- What are the effects of the required EMC measurement setup prescribed by the accreditation organisations on conducted emission; for example the power feed-line from the LISN to the power converter under test?
- What is the effect of the physical structures such as the heatsink, the enclosure, component and PCB fasteners on common-mode emissions?
- How do power components in close proximity influence conducted emissions?
- Closing the complete modelling and measurement cycle is needed. The modelling as well as measurement results in the power electronics laboratory is to be compared to accredited noise measurements. This provides confidence that the modelling as well as measurement techniques can be used in a pre-compliance test. This improves the assurance that the power unit under test will pass the accredited conducted EMC measurement qualification test performed at the final design stage before the unit can be released into the marketplace.

1.3 HYPOTHESIS AND APPROACH

A conducted EMC design philosophy will be developed and tested. The test and implementation environment will be the general power converter lab. Modelling, test and measurement techniques will be developed, up to a frequency of at least 100 MHz to be able to show radiating effects starting to emerge. The end result of this design methodology will be that if the converter design is completed, the designer will have the

confidence that the converter will adhere to the applicable EMC standard imposed on the converter.

The EMI noise source analysis will firstly consider the idealised square wave switching signal. The noise path consists of components, traces and structures. The high frequency models of these devices and structures are part of the noise path. High frequency circuit models of the passive components and circuit traces are generated and where applicable, verified with an impedance analyser or network analyser. As these expensive instruments are not readily available in a power development laboratory, a practical scheme is presented to accurately determine the high frequency impedance of components. The measurements will be verified with an impedance analyser (lower frequency) as well as a network analyser (higher frequency).

Where applicable, component and environment modelling is supplemented with finite element electromagnetic analysis. Mostly COMSOL Multiphysics will be used, but for larger structures, such as enclosure modelling, the electromagnetic analysis package FEKO will be used. This analyses the broader effects of parasitic inductance and capacitance as well as the component effects on the circuit board and the environment.

1.4 RESEARCH GOALS

Modelling and design for high frequency conducted EMC and all the aspects around it such as the noise source, the noise path and component interactions are the primary design goal. Accurate test, verification and validation should be performed. Pushing the limit of conducted EMC measurement frequencies beyond the required frequency limit so as to investigate radiated phenomena in an easier conducted EMC measurement setup.

1.5 RESEARCH CONTRIBUTION

The research goals were met. The main contributions were the accurate intuitive modelling of conducted EMC up to 100 MHz, accurate bench design and measurements, the accurate digital splitting of common-mode and differential-mode signals by means of the LISN voltages. Additional contributions included identifying a practical way of determining the

most and least susceptible side of the component as design input to a printed circuit board component placement and optimal orientation. Spinoffs achieved were a calibrated measurement technique that can be used in a development laboratory environment. Due to the noise mechanism an in-depth analysis was performed on the heatsink contributing towards common-mode noise, lowering common mode noise by using a polymer composite heatsink and the further advantages thereof, creating accurate EMC SPICE models as well as structural COMSOL FEA models applicable for a wide range of converter types. Various conducted EMC lowering techniques were tested, for example PWM jittering and slope compensation. The equations for deriving common-mode and differential-mode signals from the LISN voltage ports found in literature were not always correct. Although a simple derivation, most references to the differential-mode equation and to a lesser extent, the common-mode equation, were found not to be valid.

During the course of the EMC studies, seven conference papers were delivered and also published in conference proceedings. Three journal articles were submitted of which one has been provisionally accepted and two are undergoing revisions. These publications do provide practical solutions to the power converter designer in looking for solutions to EMC problems in converters:

I. I. Grobler and M. N. Gitau, "Common-mode noise in three-level DC-DC converters," in *Proc. IEEE AFRICON*, Nairobi, Sept. 23-25, 2009, pp. 1-6.

II. I. Grobler and M. N. Gitau, "Low cost power lead extended pre-compliance conducted EMI measurement setup and diagnostics with compact LISN," in *Proc. IEEE ECCE*, Melbourne, June 3-6, 2013, pp. 1144-1149.

III. I. Grobler and M. N. Gitau, "Characterising and modelling extended conducted electromagnetic emission," in *Proc. IEEE ECCE*, Melbourne, June 3-6, 2013, pp. 1131-1136.

IV. I. Grobler and M. N. Gitau, "Characterising and modelling extended conducted electromagnetic interference in densely packed DC-DC converter," *in Proc. IEEE ECCE*, Denver, Sept. 15-19, 2013, pp. 1676-1681.

V. I. Grobler and M. N. Gitau, "Component proximity effects in high density and high switching speed power converters," in *Proc. Energy Conversion Congress and Exposition (ECCE)*, Denver, Sept. 15-19, 2013, pp. 1251-1258.

VI. I. Grobler and M. N. Gitau, "Modelling and Measurement of High Switching Frequency Conducted EMI," in *Proc. IEEE IECON2013*, Vienna, Nov. 10-13, 2013, pp. 1029-1034.

VII. I. Grobler and M. N. Gitau, "Conducted EMC modelling for accreditation in DC-DC converters," in *Proc. IEEE IECON 2015*, Yokohama, Japan, Nov. 9-12, 2015, pp. 2329-2335.

Three journal papers have been prepared and are in review process /accepted in IET Journal of Science, Measurement & Technology:

1. SMT-2016-0188: "Modelling and Measurement of High-Frequency Conducted EMI in DC-DC Converters," reviewers comments have been incorporated and final submission was on 3 February 2017.
2. I. Grobler and M. N. Gitau, "Analysis, Modelling and Measurement of the Effects of Aluminium and Polymer Heatsinks on Conducted EMC in DC-DC Converters," *IET Science and Measurement Technology*, Online ISSN 1751-8830, Available online: 20 January 2017.
3. In preparation for re-submission: "Component Placement Effects in High Density and High Switching Speed Power Converters", that will incorporate up to 300 MHz conducted emission model and measurements with a CISPR 15 CDN.

1.6 OVERVIEW OF STUDY

The noise source and the noise path has been analysed in detail. The noise mode equations were derived and tested. A conducted EMC design method has been implemented and component as well as enclosure interaction scrutinised. The heatsink capacitances were

modelled in detail, as this is a prominent common-mode conduction path. The test bench has been designed and consistent and accurate calibrated measurements could be performed on the test devices. EMC design solutions were presented.

1.7 THESIS STRUCTURE

Chapter 2 starts off with a background and literature study on EMI noise research. Chapter 3 gives a theoretical noise generation concept. Chapter 4 deals with the noise propagation concept, component proximity effects and coupling mechanisms. Chapter 5 presents the design and simulation method for conducted EMC. Chapter 6 provides results from experimental work and Chapter 7 presents the discussion and conclusion. Chapter 8 closes down indicating suggestions for future work. Appendix A gives an EMC regulative summary, the different regulatory bodies and applicable standards.

CHAPTER 2 LITERATURE STUDY

2.1 BACKGROUND

A detailed literature review will be carried out in this chapter to establish the current status in EMI modelling. Research gaps will be identified and based on these, research goals will be determined.

2.1.1 Overview of current literature

2.1.1.1 High density packaging

The first generation converters were implemented using only discrete components [15] populated with a low component packaging density. The main switching devices and diodes were typically mounted directly onto a heatsink. The power devices were connected to one or more printed circuit boards that housed the gate drive circuitry, as well as all the protection and control circuitry. Depending on the power rating, magnetic components could also be mounted on the PCB. Larger components for higher power ratings were mounted on a separate bracket or even directly onto the heatsink.

The next power packaging technologies on the market called brick and half brick hybrids are still very popular and provide fair packaging densities at affordable costs. These are complete packaged converter structures built with discrete components that have been packed into smaller volumes than the equivalent first generation converters. This was possible due to higher switching frequencies and improved thermal management that allowed more energy to be processed with smaller components. The components are then partially or fully encapsulated into a brick-like structure. The power substrates take up the most of the volume, about 12.5%, followed by the magnetic components with about 11 %. Next the capacitors and control components with each about 3% of the total volume. It further shows that between 30% to 50% of the total volume is still not used by components in this technology [15].

To further improve packaging, power modules called Direct Copper Bonded (DCB) substrate are used to pack multiple semi-conductor power devices on a single substrate and therefore replace the old discrete power devices. It is then possible to implement the converter switching functions with a single power module with increased thermal performance. Fewer external interconnections are required due to the already made internal connections. Depending on the power rating, the magnetic components, driver, and control circuitry are normally mounted on a PCB.

2.1.1.2 Integrated electromagnetics

The new generation power converters, known as power processors, contain distributed structures or integrated Electromagnetics [12], [15]. Integrated Electromagnetics is the three dimensional integration of the functions of conduction, inductance, resistance, and capacitance in one component, namely the integrated power module. This is the electromagnetic integration of multiple passive components into a single integrated structure, also called a planar power passive module. The structure normally consists of the combination of alternative layers of conductors, dielectrics, and magnetic materials. These alternative layers realise components such as inductors, capacitors, and transformers in a series and/or parallel configuration, normally configured for a specific converter topology.

2.1.1.3 Electromagnetic environment

From the foregoing paragraphs one can conclude that in the new generation power converters, passive as well as active devices, are in closer proximity to each other now more so than ever before. This close proximity enhances parasitic capacitance and inductive coupling, creating a complex electromagnetic environment. Furthermore, switching frequencies have been dramatically increased leading to reduced passive component sizes, but also generating greater EMI levels at higher frequencies, resulting in high conducted common-mode disturbance [10]. Component parasitics, magnetic or electrostatic coupling effects can therefore not be neglected.

Currently, external to most power converters, is a modern environment consisting of sensitive electronic devices, such as communications and Information Technology. These

IT equipment are usually sensitive to electromagnetic interference levels. It is thus very important that power processors comply with the electromagnetic limits and even in some cases, that they generate less noise than proposed by the compliance authorities.

Typical power processors may have multiple converters, and although they might be synchronised, they still produce an array of broad-band EMI emissions of up to several hundred mega Hertz. The low frequency range can extend down to several Hertz and conventional methods such as shielding and typical filtering techniques do not adequately contain this noise. The space and boundary conditions necessary for the EMC design are also very complex.

The belief is that if conducted EMI can be contained by firstly, understanding the mechanism thereof, and secondly, by designing for minimum conducted emissions with this knowledge, the radiated emissions that are more difficult to analyse, could also be effectively lowered in the process [16]. The conducted EMI is considered as the source of the radiated EMI.

2.1.1.4 Modelling criteria

Due to the switching operation of power converters, enabling reduced size and weight and increased efficiency, large dv/dt and di/dt currents exist, generating unwanted noise. Placing any power product into the marketplace, it needs to adhere to stringent international EMI requirements. If a power converter does not pass the EMI qualification test, its use become limited and will be unable to enter the marketplace. Traditionally, EMI is known to many power electronics designers as a ‘black art’, implementing recipes and hope the power product will eventually pass its EMI qualification test. If not, expensive rework is performed; adding more filtering etc. and this process can be disastrous, missing deadlines and at worst, enter a re-design phase. This is why most power engineers will overdesign filters and add extra measures that might not be necessary. Designing for EMI is becoming extremely important, especially in lieu of factors even more detrimental to EMI noise, such as converters constantly evolving into better efficiencies, moving to higher frequencies and smaller packaging.

In many situations, EMI modelling is not being performed with all the required starting data. EMI models are often based on estimates and on cases where component tolerances and environment variations can be extensive. EMI modelling should be approached with the idea of bounding the problem region to reduce the uncertainty to a minimum [17].

The three basic criteria for comparing different EMI modelling methodologies can include accuracy, feasibility, and generalization [11], [18].

Both frequency and magnitude levels of the predicted EMI need to be accurate as to address the different aspects of EMI mechanisms. Most models are only accurate in the lower frequency region (below 5 MHz [11] or below 8 MHz [10]. The modern high density packaging of components introduces an increase in parasitics and creates an easier conduction path for the unwanted high frequency electromagnetic noise. It is thus very important to model these higher frequencies more accurately.

Feasibility is important as some EMI models are complicated to use, while others sacrifice accuracy to achieve simplicity. The need for less complex and practical models accessible to the power designer is becoming a valuable necessity. Generalisation is important as some models are only valid for specific applications and topologies. Even in larger converter systems or power processors, as well as in the design of different converters, a generic modelling methodology is indispensable.

2.1.2 What has been done before

From the results of reviewing the existing literature, it is obvious that conducted EMI modelling research is still not adequate and in most cases, addressing only specific topologies. Due to simplification and as a result of the techniques used, most EMI models deal only with the lower 15% of the frequency range. To incorporate the high frequency part of the conducted EMI noise, a more accurate modelling methodology is required.

In the converter design process, the EMI management tends to be included in the last step, leading to expensive rework if the EMI levels fail compliance testing. Failure of EMI management in the early design process is mostly because of lack of EMI noise source models.

The present EMI modelling research is still at the converter level. Specific topologies have specific EMI models, but in a power processor system where multiple converters are in close proximity, system level EMI is often inefficient and ineffective. This inefficiency is due to a lack of proper consideration of the appropriate interactions and inter-modulation phenomena induced by the system. This is due to the fact that a general modelling approach for the power processor system is not available and thus not implemented in the early stages of the design.

Some important EMI phenomena, such as common-mode and differential-mode noise interaction are not fully explored [12]. This type of noise interaction is not easily controlled and subsequently not suppressed by traditional EMI management. It is thus important to develop modelling technologies that take them into account.

2.1.3 EMI noise research

The objective of the conducted EMI research proposal is to understand the primary causes of EMI and how to manage and suppress EMI in a systematic, methodical yet practical manner. The basic conducted EMI modelling process includes 2 steps, namely: the EMI noise source [16] and the EMI noise propagation [10], [11]. The purpose of modelling the propagation path and noise source separately is to try to understand the EMI noise methodology. All links between the noise source and noise coupling effects are considered possible noise propagation paths. The noise paths consist of cables, wires, PCB traces, magnetic components, capacitors and their parasitics. The noise source and noise path need to be addressed simultaneously.

An important aspect of conducted EMI noise research is the verification of the simulated models. Verifying the models for accuracy needs a well-designed EMI bench to be able to take measurements of the intended noise. Unwanted noise paths, for example the DUT auxiliary power or the load interface to the test bench, has to be screened if not part of the model. Similarly for the measurement cables, it needs to terminate into 50 Ω because the LISN is a 50 Ω measurement device. The test bench needs a proper ground and care must also be taken with regards to external noise interference

Regardless of which simulation approach is taken, the key to successful EMI performance prediction is accurate noise source and path information [16], [19]. This information could also reveal the significant roles of parasitic elements combined with device switching processes in EMI.

Many EM noise simulators have not considered skin and proximity effect, non-linear characteristics, intermodulation and hysteresis. The influence of enclosures, bulky structures such as heatsinks and the effects that nuts, bolts and washers have on EMI are not considered in the present literature. Furthermore, EMC modelling on high-density packaging and power passive structures is not well researched. The PWM effects on EMI performance are also not well documented. In conclusion it seems that the requirement for further research in the above mentioned field would be of great value to the affiliated industries.

2.1.3.1 Problem and objectives

As is the case with any power converter, where current changes rapidly i.e. large di/dt and dv/dt, EM radiation will take place. This radiation needs to be limited or contained so as not to interfere with other nearby sensitive electronic equipment, by meeting internationally accepted test standards.

Most designers use the basic EMC recipes and make use of good EMC design practices when designing power processors. This design process may contain the EMI sufficiently in most cases, but poses a huge financial risk when the initial EMC qualification tests are performed for the first time on the prototyped unit. If this unit fails the initial qualification test as often happens, minor changes to the design might not solve the problem completely. This can lead to very expensive modifications, adding bulky filters or may even lead to the redesigning of a part of the converter, and extending the critical time to market deadline in a competitive marketplace.

The design goal is to develop a practical model for accurate broadband conducted EMC analysis for high density power processor packaging that could well be expanded to different structures and components. This will enable the designer to accurately predict the

EMC parameters in the early design stage and thus through the model understand the mechanisms that create EMI and solve the EMC aspects early in the design stage. The ultimate goal would be a modeling technique that would guarantee test compliance by yielding noise characteristics that are as accurate as those from an accredited test facility.

2.1.3.2 Design methodology

At this point, the proposal presents a broad research methodology. Firstly, a comprehensive literature study will be performed on the subject of conducted EMI, mathematically assessing how it relates to high density power processors and integrated power passive components. The outflow will be a model or models to do a prediction on simple packaging, verifying the accuracy of these models against practical measurements. This process will also enable a wider understanding of the mechanisms involved in EMC with regard to the close proximity of components and should lead to a substantial contribution towards more effective techniques and ideas with regards to the design of high density packaging and ultimately better EMC compliance.

2.2 ELECTROMAGNETIC INTERFERENCE ISSUES

The physical sizes of the passive energy storage elements such as transformers, inductors and capacitors in power converters decrease in size as well as in component values with an increase of the switching frequency [20].Therefore, high-density power supplies generally demand high switching frequency and fast semiconductor devices. However, the increased switching frequency, together with the increased current and voltage slew rates, dv/dt and di/dt, has negative effects on the electromagnetic compatibility (EMC) performance of the power converter.

Decreasing the EMI to acceptable levels as dictated by the applicable EMI regulatory body for the application is of utmost importance. Switch-mode power supplies were known in the past for their overwhelming electromagnetic noise interference, causing disruption to especially communication equipment such as AM/FM receivers and microprocessors. Recently, care needs to be taken to comply with the applicable regulation as power

converters are more and more utilized near sensitive radio frequency circuitry and microprocessors.

Different countries call for different EMI standards, depending on their internal regulatory bodies. The major standards are normally slightly adjusted or in some cases such as in South Africa, adopted a given standard as is. The four major bodies implementing standards are the International Electrotechnical Commission (IEC), the Federal Communications Commission (FCC) in the United States, the European Committee for Electrotechnical Standardization (CENELEC) and the European Telecommunications Standards Institute (ETSI) in European countries. Two IEC technical committees are devoted full time to EMC work, namely the TC77, who study electromagnetic compatibility between equipment, including networks, and the International Special Committee on Radio Interference (CISPR). The major output of TC77 is printed in various parts of IEC Publication 61000. CISPR publications deal with the limits and measurement of radio interference characteristics or potentially disturbing sources. CISPR publications co-exist with IEC 61000.

For military applications, a different requirement exists, explained in the DOD document MIL-STD-461F [21]. Conducted emissions are applicable down to 30 Hz for submarine applications and regulated up to 10 MHz for all equipment. Table 2.1 provides more detail pertaining the popular limits. Figure 2.1 shows a graphical representation. The MIL-STD-461F limits are standard values and guidance for relaxation of these limits is given. The basic limits are for system source voltage of lower than 28 V. Up to 115 V, a 6 dB relaxation is applicable, and for 220 V systems, 9 dB is given. Furthermore, if equipment is housed in less sensitive areas, relaxation can be negotiated.

Table 2.1 Popular conducted emission limits.

CLASS A						
	FCC Part 15		**CISPR 22**			
Frequency	**Quasi Peak**		**Quasi Peak**		**Average**	
[MHz]	**[dBµV]**	**[mV]**	**[dBµV]**	**[mV]**	**[dBµV]**	**[mV]**
0.15 – 0.45	_	_	79	9	66	2
0.45 – 0.5	60	1	79	9	66	2
0.5 – 1.705	60	1	73	4.5	60	1
1.705 - 30	69.5	3	73	4.5	60	1
CLASS B						
	FCC Part 15		**CISPR 22**			
Frequency	**Quasi Peak**		**Quasi Peak**		**Average**	
[MHz]	**[dBµV]**	**[mV]**	**[dBµV]**	**[mV]**	**[dBµV]**	**[mV]**
0.15 – 0.45	_	_	66-56.9	2.0-0.7	56-46.9	0.63-0.22
0.45 – 0.5	48	0.25	56.9-56	0.7-0.63	46.9-46	0.22-0.2
0.5 – 1.705	48	0.25	56	0.63	46	0.2
1.705 - 30	48	0.25	60	1.0	50	0.32
MIL-STD-461F						
Submarine Application			**Other Platforms**			
Frequency	**Quasi Peak**		**Frequency**	**Quasi Peak**		
[Hz]	**[dBµA]**		**[Hz]**	**[dBµV]**		
30 - 2.6 k	95 (<3 A)		10k – 500 k	94 – 60 (28 V)		
2.6 k to 10 k	95 – 76 (< 3A)		500 k – 10 M	60 (28 V)		

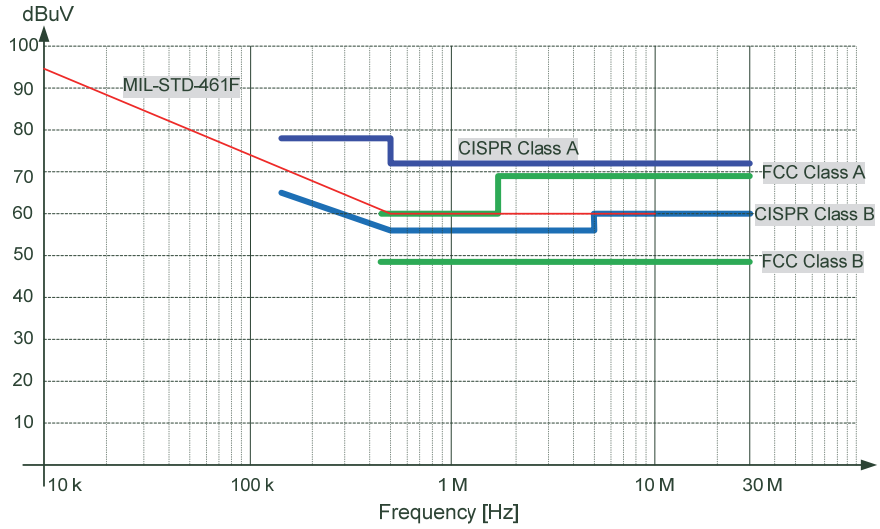


Figure 2.1. Applicable limits for conducted emissions.

The EMC bench setup as explained in MIL-STD-461E is shown in Appendix A, Figure A.3. The bench consists of a double LISN, a 2 m power feed-line suspended 50 mm above the conducting surface with wooden blocks, as well as the test equipment.

Figure 2.2 shows the conducted EMI emission path as from the noise source, a coupling path to the power source matched with a Line Impedance Stabilising Circuit (LISN). The noise source generates the EMI noise, a coupling path transfers the noise to the LISN through cables or wires. The LISN creates a standardized means to measure the EMI noise into a 50 Ω impedance and to isolate the power source noise from the converter noise.

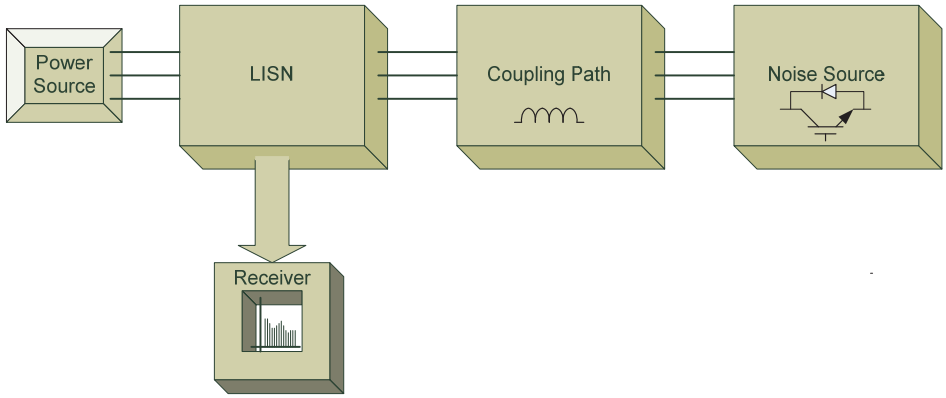


Figure 2.2. Conducted EMI emission concept.

It is worth noting that annex B of CISPR 15 [22] presents an alternative method for complying with radiated disturbances for electrical lighting and similar equipment by means of a conducted emission test ranging from 30 MHz up to 300 MHz. A specially constructed high frequency LISN, called a Coupling/Decoupling Network (CDN) is specified for this test. The test-setup recommends a power-feed length of between 10 cm and 30 cm, opposed to the MIl-STD-461F requirement of 2 m. This is a simpler test that can be performed on a test bench as opposed to having, for example, a more complex radiated test setup that requires an anechoic chamber with expensive antennas and measurement equipment.

A small 50 μH ring-core LISN [23] and earthed copper sheet bench setup, according to MIL-STD-461F specifications, was manufactured and implemented to verify the simulated data. A 2.4 GHz Tektronix oscilloscope was used to record the data, with a vertical resolution of 11 bit. MATLAB was then used as a post-processing tool analysing the recorded data and calculating the spectrum slope. The complete setup had been verified and calibrated to an accredited EMC laboratory test bench using a reference switch-mode noise generator. All spectral plots were compared to the MIL-STD-461F conducted EMC limit [21].

2.3 COMPONENT PROXIMITY EFFECTS

Advances in power semiconductor component capability allow the power density of power converters to increase. This in turn creates a complex electromagnetic environment for the components. Parasitic effects due to layout and packaging have to be addressed. Elaborate modelling of parasitic elements with for example Finite Element Analysis (FEA) software, provide good results, but can show limited insight into the problem and is very time consuming [24]. Proximity interactions between components are mainly magnetic coupling effects although capacitive coupling gains more influence at higher frequencies due to the Effective Series Inductance (ESL) value [25], [26], [27]. Placement of passive components significantly influences the Electromagnetic Interference (EMI) behaviour of the power electronic system, in particular the filter components. Modelling a switching cell with components parasitic effects and neglecting magnetic coupling may lead to differences between measured and simulation results [25]. The placement distance of components can be reduced due to effective rotation [28] or enclosing. The power filter has been extensively studied in literature, but the consequences of the coupling effect in power converters, especially relating the CM and DM noise, is not readily available.

A Helmholtz coil can be used for determining the least- and most susceptible face of a component, placing components close to each other facing their least susceptible vectors. Furthermore, the Helmholtz coil can also be used to characterise Radio Frequency (RF) inductors [29].

CHAPTER 3 MODELLING – NOISE GENERATION

3.1 NOISE CHARACTERISTICS

The fundamental noise source characteristics will be presented in this chapter, providing insight to the noise modelling environment. Ground theory publications that include the noise generation mechanisms are referred to in [30], [31], [32] and [33].

3.2 EMI NOISE MODES

Modern switch-mode converter units and motor drive systems use high speed semiconductor devices such as IGBT's and MOSFETs. The trend towards smaller packaging, higher power densities, improved performance, reduced weight and lower cost require high switching frequencies as well as higher dv/dt and di/dt for lower switching losses. The higher switching frequencies cause higher levels of interference to move into a higher frequency band than previously anticipated [31].

Two main conducted emission modes exist: the differential-mode (DM) of conduction and the common-mode (CM) of conduction as defined in Figure 3.1, the single LISN in (a), dual LISN in (b) and the DM and CM impedances in (c) and (d) respectively. Differential-mode noise is mainly caused by the current flow in the circuit, the magnetic coupling L.di/dt where L is mainly the parasitic loop inductance [34]. The DM propagation path is normally made up of the dc-link capacitors, high frequency capacitors, the bus bars or tracks, and connectors such as screw terminals.

Common-mode noise is dictated by the voltage amplitude of the switching signal [35], [36], implying the charging and discharging of parasitic capacitances, C·dv/dt, [34], [37]. The CM propagation path is made up mainly of the parasitic capacitance between the bus bars or tracks and the ground plane, and the parasitic capacitance between the switching device and the ground plane, the latter normally separated by a thin insulator .

A third component is present, called mixed mode IMM when the EUT is not connected to ground, with common-mode noise coupling through the EUT enclosure to the wires through parasitic means [38], [39], without an earth wire.

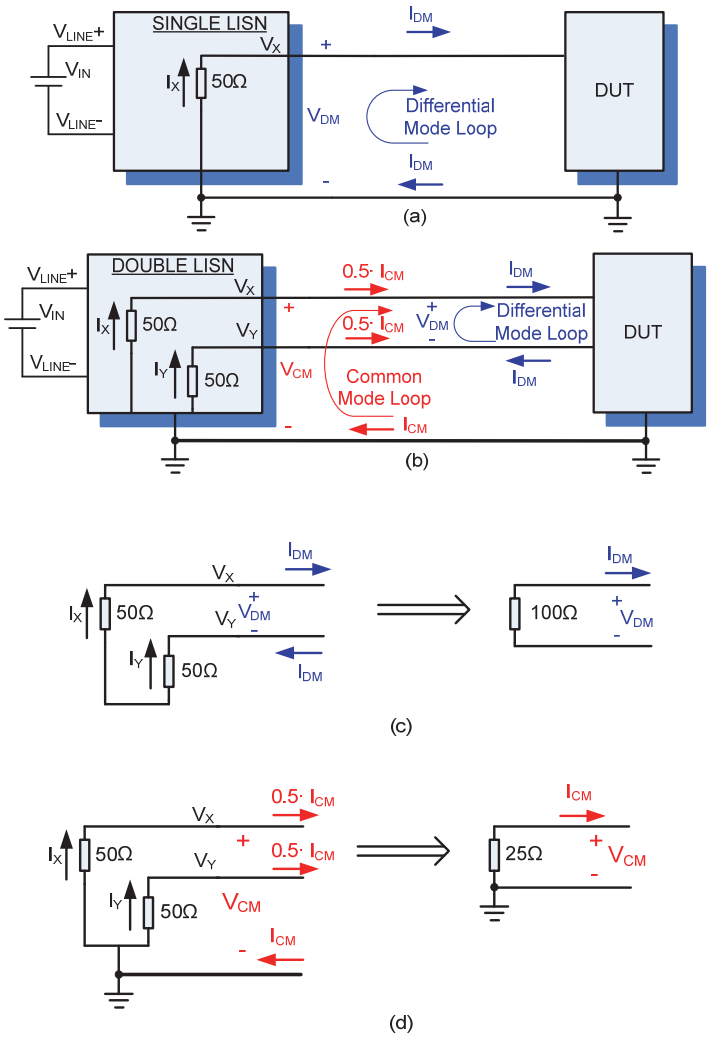


Figure 3.1. Defining conducted noise current-modes: (a) Single LISN DM, (b) dual LISN CM and DM, (c) DM LISN impedance and (d) LISN CM impedance.

Referring back to Figure 3.1 (a), it shows a single LISN measurement where a safety earth or ground return is not incorporated. Only differential-mode conducted noise is of concern and measured at port V_x. Hence the expression for differential-mode current and voltage are:

$$I_X = I_{DM} \quad , \quad V_X = V_{DM} \tag{3.1}$$

The double LISN with ground return is shown in Figure 3.1 (b). The expressions needed to separate differential and common-mode voltages will be derived from first principles using the above measurement protocol. This is necessary so as to address discrepancies relating to the equations found in the available literature. With reference to Figure 3.1 (c) an expression for differential-mode current in terms of V_X and V_Y is obtained as:

$$I_{DM} = \frac{I_X - I_Y}{2} = \frac{V_X/50 - V_Y/50}{2} \tag{3.2}$$

An expression for the differential-mode voltage is obtained in terms of V_X and V_Y as:

$$V_{DM} = 100 \cdot I_{DM} = (V_X - V_Y) \tag{3.3}$$

An expression for converting the differential-mode voltage to current is obtained with:

$$I_{DM} = \frac{V_{DM}}{100} \tag{3.4}$$

Following a similar approach, the expressions for LISN common-mode current and common-mode voltage in Figure 3.1 (d) are then obtained as:

$$I_{CM} = I_X + I_Y = V_X/50 + V_Y/50 \tag{3.5}$$

$$V_{CM} = 25 \cdot I_{CM} = \frac{V_X + V_Y}{2} \tag{3.6}$$

The conversion of common-mode voltage to current is achieved using the expression:

$$I_{CM} = \frac{V_{CM}}{25} \tag{3.7}$$

Figure 3.2 (a) and (b) shows the signal magnitudes of the common- and differential-mode noise.

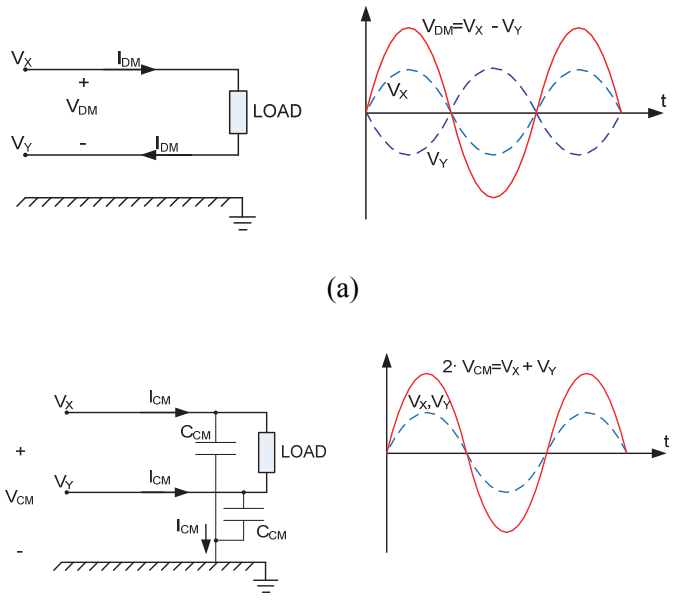


Figure 3.2. Extracting (a) differential-mode and (b) common-mode noise.

Figure 3.3 show the setups needed to measure the CM and DM signals with a high frequency LINDGREN EMC current probe [30]. Measuring the differential-mode in Figure 3.3 (a), the LISN power feed wire currents are subtracted using the EMC current probe, to yield $2I_{DM}$. Similarly, measuring common-mode in Figure 3.3 (b), the power feed-lines currents from the LISN to the DUT are added using the EMC current probe, to yield I_{CM}.

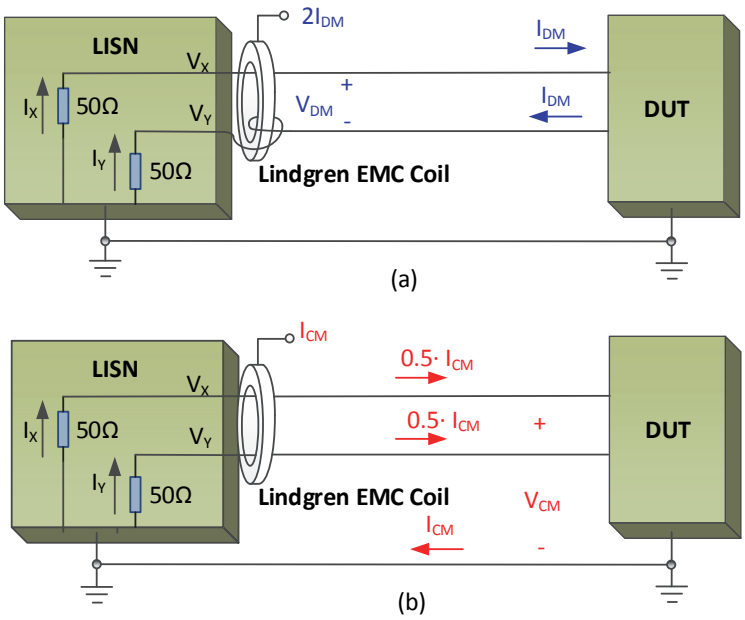


Figure 3.3. Double LISN Lindgren probe measurement: (a) Differential-mode and (b) common-mode.

Equation (3.1) – (3.7) were tested to separate noise digitally and confirmed to be correct and in agreement with those derived in [5], [40], [6]. However, expressions derived in some of the other available literature such as [20], [38], [41], [42], [43], [44], were found to give inaccurate differential-mode results due to the differential mode voltage in terms of the LISN ports being expressed as *½(Vx-Vy)*, causing a 6 dB discrepancy. In [7] the common-mode return current is defined as $2 \cdot I_{CM}$, instead of the general assumption of only I_{CM} and can also create confusion. It also seems that in general, if the derived equations can follow the backward approach, the V_{DM} signal is defined as $2 \cdot V_{DM}$ (but $1 \cdot I_{DM}$) and V_{CM} as V_{CM} $(0.5 \cdot I_{CM})$, creating confusion. As the equation to extract common mode and differential-mode noise from the LISN ports seems simple, care need to be taken to implement it correctly. The discrepancy are only detected if accurate calibrated measurements can be performed on a repetitive scale whilst comparing it to the derived expressions, and due to the nature of high frequency noise, it is very difficult to achieve.

3.3 COMMON-MODE RADIATING EFFECT

Basic electromagnetic (EM) theory shows that a current flowing around a loop generates a magnetic field (H) proportional to the area of the loop. This is of particular interest in the

case of common-mode currents. As already mentioned, common-mode currents normally form a larger loop than differential-mode currents, thus contributing to the radiated EMC, as portrayed in Figure 3.4.

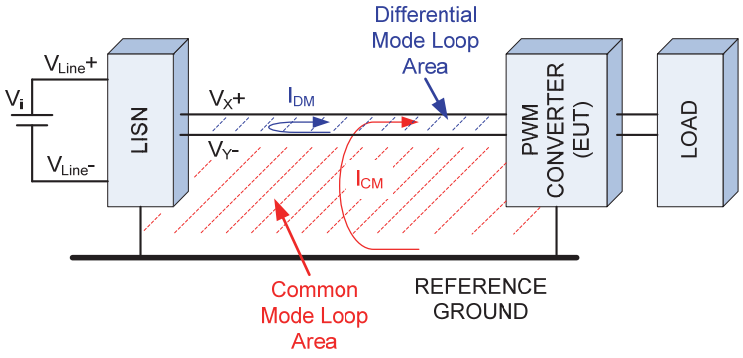


Figure 3.4. CM and DM loop areas.

The common-mode loop area can be redrawn as in Figure 3.5.

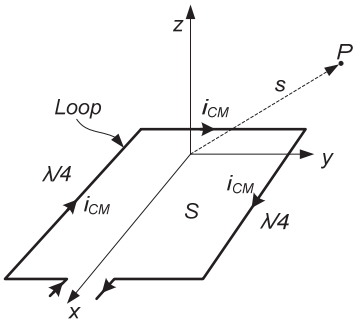


Figure 3.5. Common-mode radiation loop.

The simplified expression in (3.8) obtained referring to Figure 3.5, gives the approximate magnetic far-field at an arbitrary point, p, a distance, s, from the current loop with surface area, S.

$$H_{far} = \pi \cdot I \cdot \frac{S}{\lambda^2 \cdot s} \quad \left[A/m \right] \tag{3.8}$$

The magnetic field, H, is proportional to the surface area, a, and the current, I. Thus, an increase in a (or I) will cause an increase in the magnetic field strength at a distance s. The typical radiated emissions limit at a distance of 10 m is approximately 37 dBμV/m. If the

power feed-line is in the order of 2 m in length, positioned 50 mm from the ground plane on wooden blocks, the loop area can easily be resonant at a half wavelength, that is, at around 30 MHz, within the conducted emission band. In general, a loop current of approximately 5 μA at 30 MHz will cause the unit to fail the radiated limit at the required 10 m distance. The same order of current magnitude will cause the conducted limits to be exceeded and hence the unit to fail to comply. Thus, if the common-mode conducted emissions can be contained effectively, this will in turn have a positive effect on the radiated emissions.

3.4 THE EMI NOISE SOURCE

The power converter switching waveform is analysed, first as a square wave and then a trapezoidal wave. From this analysis, a spectral slope is drawn to determine the influence of the waveform parameters on the spectral slope, showing that higher switching frequency and faster rise – and fall-times moves the noise slope to higher frequencies, causing interference in higher frequency bands than previously anticipated.

3.4.1 Square wave expansion coefficients

The Fourier expansion coefficients of the square wave drawn in Figure 3.6 will now be determined [7]. The square wave has amplitude A, period T_S and duty cycle D. The duty cycle is defined as the on-time τ divided by the period T_S.

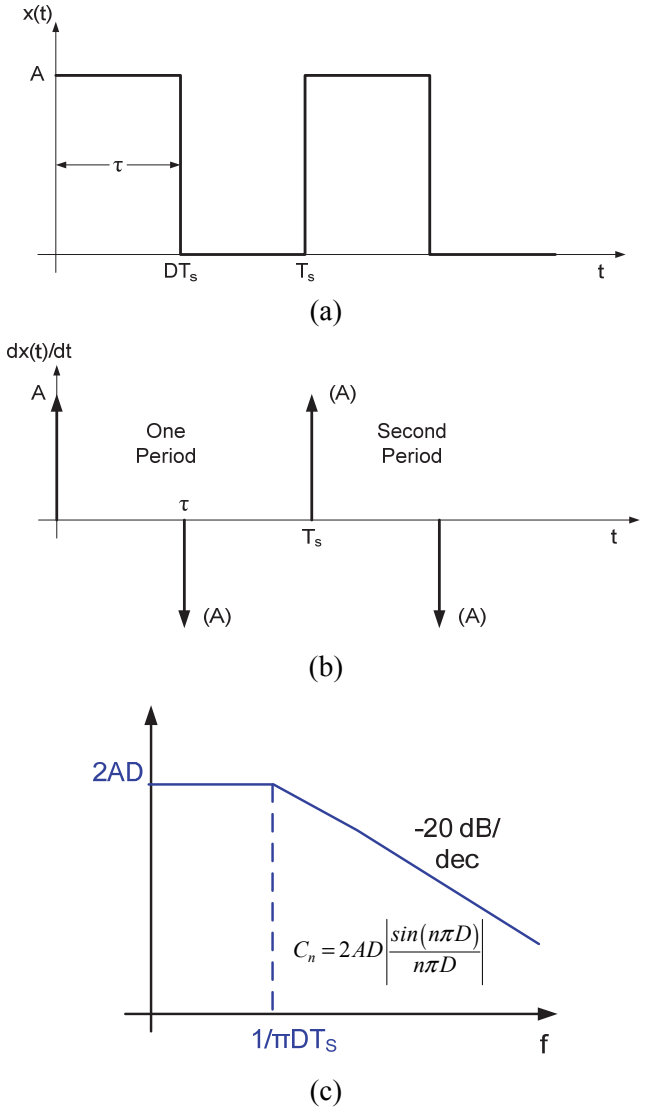


Figure 3.6. (a) Square wave defined, (b) square wave derivative and (c) spectral slope presentation.

The derivative of the square wave can be presented by a train of impulses as shown in Figure 3.6 (b). The expansion coefficients for the derivative of this function are the sums of the expansion coefficients of each pulse train component.

$$C_n = \frac{1}{(jn\omega_0)^k} C_n^{(k)} \qquad n \neq 0,\ k = 1 \tag{3.9}$$

Thus

$$C_n^{(1)} = A\frac{1}{T_S} - A\frac{1}{T_S}e^{-jn\omega_0\tau} \tag{3.10}$$

Manipulating and rearranging further gives

$$C_n^{(1)} = \frac{A}{T_S} e^{-\frac{jn\omega_0\tau}{2}} \left[e^{\frac{jn\omega_0\tau}{2}} - e^{-\frac{jn\omega_0\tau}{2}} \right]$$

$$= \frac{A}{T_S} e^{-\frac{jn\omega_0\tau}{2}} \left[2jSin(\frac{n\omega_0\tau}{2}) \right]$$

$$= jn\omega_0 A\tau/T_S \left[\frac{Sin(n\omega_0\tau/2)}{n\omega_0\tau/2} \right] e^{-jn\omega_0\tau/2} \quad (3.11)$$

From (3-9) – (3.11),

$$C_n = A\tau/T_S \left[\frac{Sin(n\omega_0\tau/2)}{n\omega_0\tau/2} \right] e^{-jn\omega_0\tau/2} \quad (3.12)$$

Replacing τ/T_S=D and multiply by two, the one sided magnitude spectrum can be expressed as:

$$C_n = 2AD \left| \frac{sin(n\pi D)}{n\pi D} \right| \quad (3.13)$$

The low frequency amplitude is dependent on the duty cycle D and the amplitude A. The first frequency cut-off is at $1/(\pi DT_S)$. Figure 3.7 shows two different scenarios, Figure 3.7 (a) and Figure 3.7 (b) with a change in the period T_S, from 50 µs to 5 µs and the duty cycle set at D=0.5. The amplitude was set at 100 V. With a decrease in the period (increase in switching frequency), the noise spectrum moves to a higher frequency. The Figure 3.7 (c) and Figure 3.7 (d) shows a spectral plot with period T_S set at 50 µs, but the duty cycle D varied from 0.9 to 0.1. The high frequency is not affected at all, but in the lower band the spectral amplitude increases for small duty cycles. It might then be advantageous to use converters operating with smaller duty cycles. For instance, the step-up (boost) converter's useful operating duty cycle is normally below 0.8 with the step-down (buck) converter's making good use of the high duty cycle, shown in Figure 3.8, and with this parameter, better suited for lower EMI.

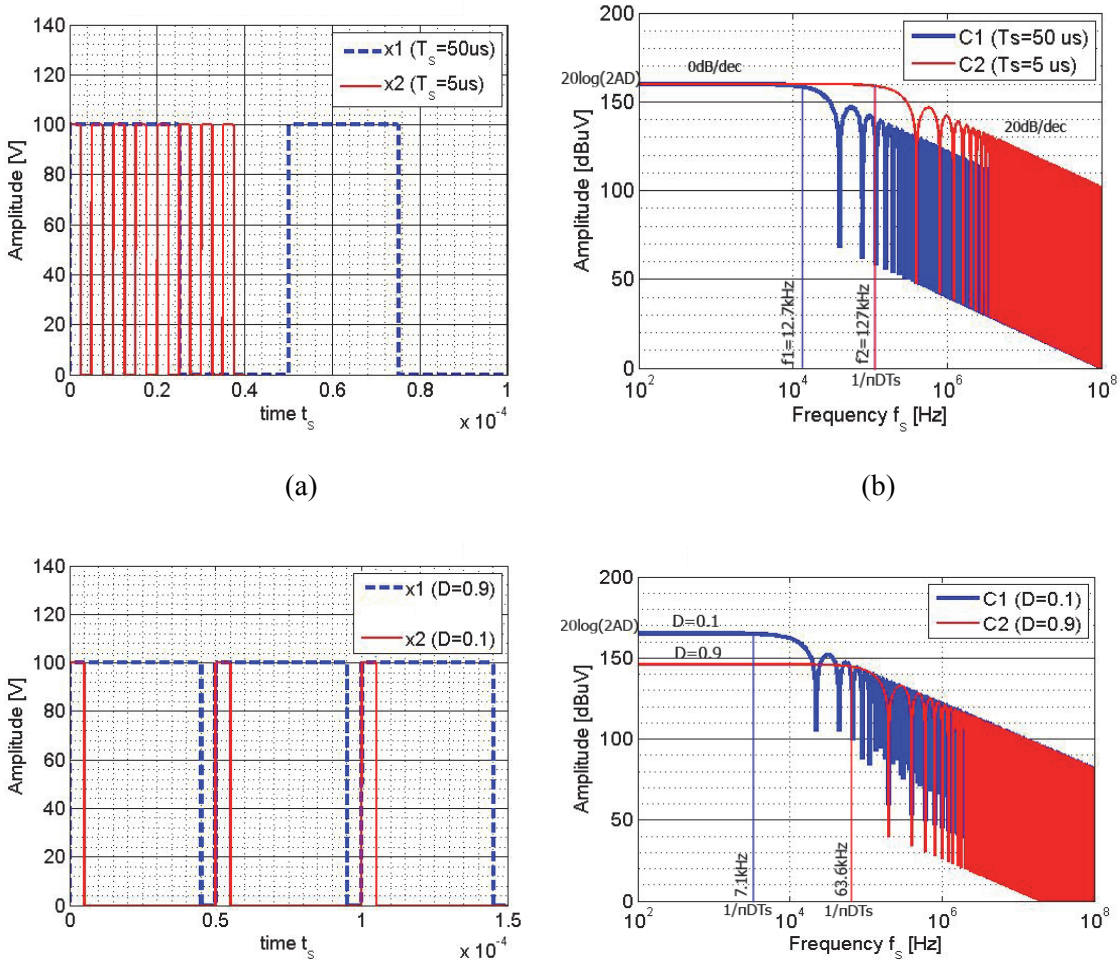


Figure 3.7. Square wave spectrum: (a) Variable period time domain, (b) variable period frequency domain, (c) variable duty cycle time domain and (d) variable duty cycle frequency domain.

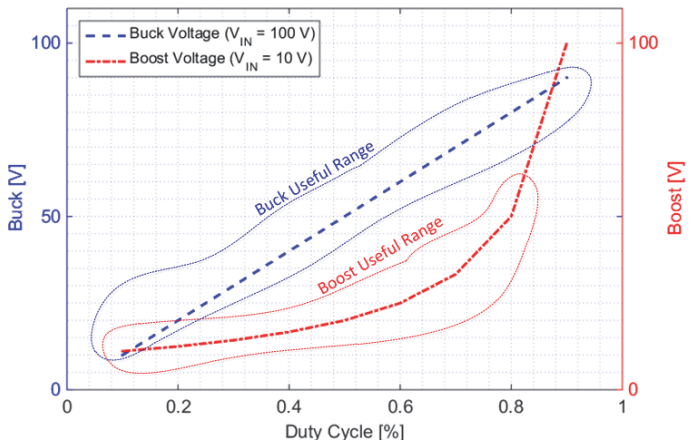


Figure 3.8. Step-up and step-down output voltage vs. duty cycle.

3.4.2 Trapezoidal wave expansion coefficients

Similarly as for the square wave, expansion coefficients for the trapezoidal wave shown in Figure 3.9 will now be calculated. The trapezoidal wave is a closer match to the practical switching waveform compared to the ideal square wave, incorporating a rise-time t_r and a fall-time t_f shown in Figure 3.9 (a). Figure 3.9 (b) and (c) show the first- and second derivative of the waveform and Figure 3.9 (d) the spectral slope.

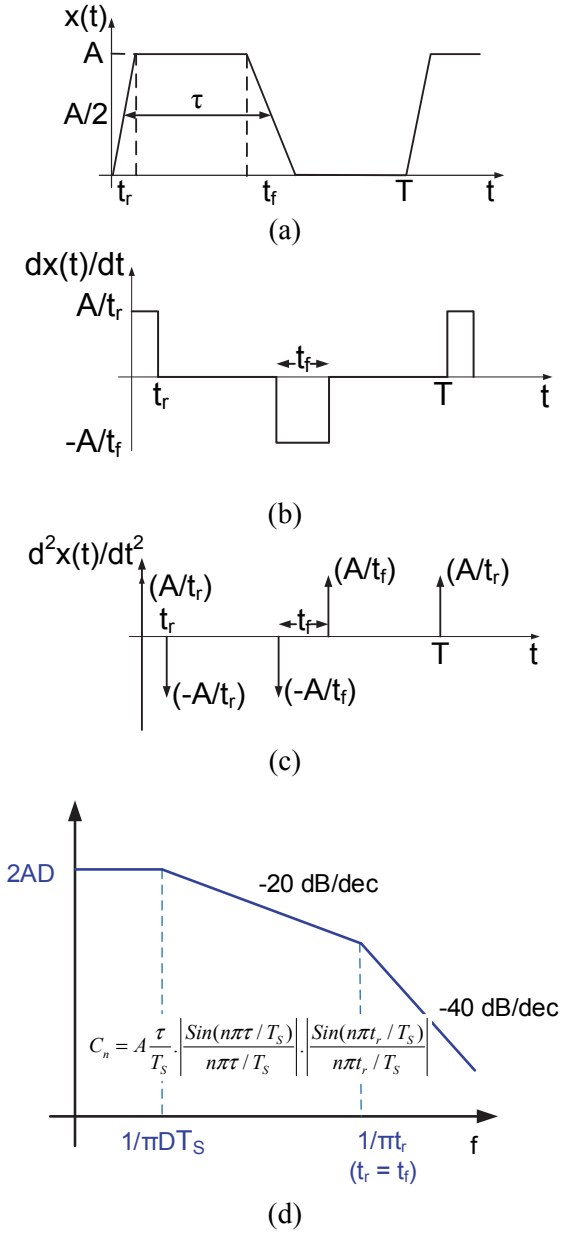


Figure 3.9. (a) Trapeziodal wave defined, (b) trapeziodal wave derivative, (c) trapeziodal wave second derivative and (d) spectral slope presentation.

The Fourier coefficient is obtained as follows [7]:

$$C_n = \frac{1}{(jn\omega_0)^k} C_n^{(k)} \qquad n \neq 0,\ k = 2 \tag{3.14}$$

thus:

$$C_n^{(2)} = \frac{1}{T}\frac{A}{t_r} - \frac{1}{T}\frac{A}{t_r} e^{-jn\omega_0 t_r} - \frac{1}{T}\frac{A}{t_f} e^{-jn\omega_0\left(\tau+\frac{t_r-t_f}{2}\right)} + \frac{1}{T}\frac{A}{t_f} e^{-jn\omega_0\left(\tau+\frac{t_r+t_f}{2}\right)}$$

$$= \frac{A}{T}\left[\frac{1}{t_r} e^{-jn\omega_0\frac{t_r}{2}}\left(e^{+jn\omega_0\frac{t_r}{2}} - e^{-jn\omega_0\frac{t_r}{2}}\right) - \frac{1}{t_f} e^{-jn\omega_0\tau}.e^{-jn\omega_0\frac{t_r}{2}}\left(e^{+jn\omega_0\frac{t_f}{2}} - e^{-jn\omega_0\frac{t_f}{2}}\right)\right]$$

$$= j\frac{A}{2\pi n}.(n\omega_0)^2 e^{-jn\omega_0(\tau+t_r)/2}\left[\frac{Sin(n\omega_0\tau_r/2)}{n\omega_0\tau_r/2}.e^{n\omega_0\tau/2} - \frac{Sin(n\omega_0\tau_f/2)}{n\omega_0\tau_f/2}.e^{n\omega_0\tau/2}\right] \tag{3.15}$$

Combining (3-14) and (3-15) gives:

$$C_n = -j\frac{A}{2\pi n}.e^{-jn\omega_0(\tau+t_r)/2}\left[\frac{Sin(n\omega_0\tau_r/2)}{n\omega_0\tau_r/2}.e^{n\omega_0\tau/2} - \frac{Sin(n\omega_0\tau_f/2)}{n\omega_0\tau_f/2}.e^{n\omega_0\tau/2}\right] \tag{3.16}$$

The special case of $t_r = t_f$ simplifies the analysis. This then gives:

$$C_n = A\frac{\tau}{T}.\frac{Sin(n\omega_0\tau/2)}{n\omega_0\tau/2}.\frac{Sin(n\omega_0\tau_r/2)}{n\omega_0\tau_r/2}.e^{-jn\omega_0(\tau+t_r)/2} \tag{3.17}$$

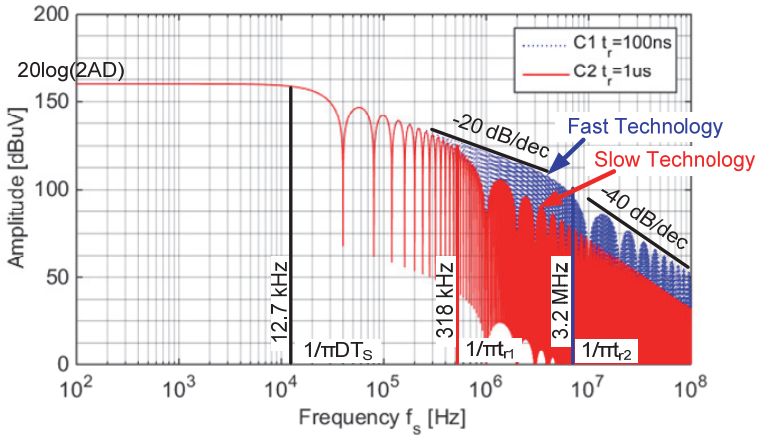
The equation for the one-sided spectrum then becomes:

$$|C_n^+| = 2.|C_n|$$

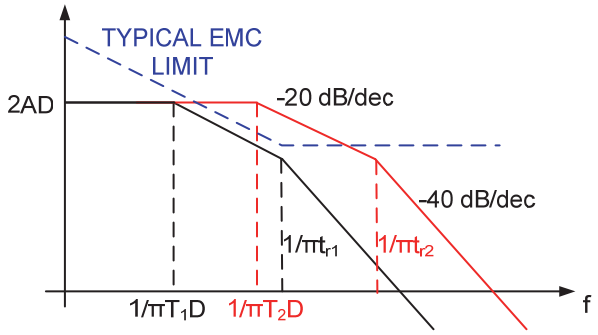
$$= 2.A\frac{\tau}{T}.\left|\frac{Sin(n\pi\tau/T)}{n\pi\tau/T}\right|.\left|\frac{Sin(n\pi t_r/T)}{n\pi t_r/T}\right|, \quad \text{for } n \neq 0 \text{ and } t_r = t_f \tag{3.18}$$

Equation (3-18) is plotted in Figure 3.10 (a), for two different rise-times t_r = 100 ns and t_r = 1 µs (note $t_r = t_f$) in order to demonstrate the effect of rise- and fall-times on noise. The amplitude of the waveform, A, is 100 V and the duty cycle D is 50%. The first cut-off is at $1/(\pi DT_s)$ and the second at $1/(\pi t_r)$, as set out in Figure 3.10 (b). Thus, a lower rise-time and slower switching device technology (previous generation) reduces the high frequency

content of the trapezoidal waveform. In modern power converters the trapezoidal switching waveform can be manipulated to lower the conducted EMI, but it will increase the switching losses and hence lower the total efficiency of the converter.



(a)

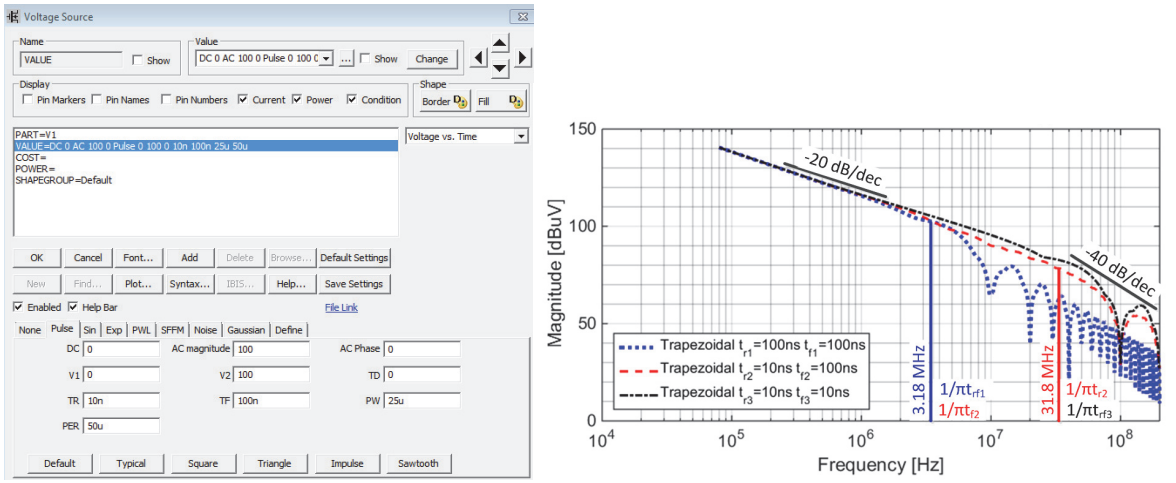


(b)

Figure 3.10. Trapezoidal wave frequency spectrum showing different rise-and fall-times (a) defined and (b) presented.

The key parameters that contribute to the high frequency spectral content of the waveform are the rise- and fall-times of the pulse. The same waveform as above can be generated in a SPICE type software package, Spectrum Software and compared to the above mathematical presentations. Utilising the SPICE simulations, more complex waveforms can be analysed with ease, for example different trapezoidal rise- and fall-times to help visualise their effect on noise.

Figure 3.11 shows a SPICE simulation of a trapezoidal waveform frequency spectrum, confirming the theory. The SPICE simulations furthermore investigate different rise- and fall-times on the trapezoidal signal spectral content. Figure 3.11 (a) shows the arbitrary SPICE trapezoidal waveform setup, with a period of 50 µs and a duty cycle of 50%, a rise-time of 10 ns and the fall-time of 100 ns. The peak-to-peak amplitude is 100 V. Figure 3.11 (b) is trapezoidal signals with a combination of rise- and fall times. Trace 1 has parameters $t_{r1} = t_{f1} = 100$ns as a reference trace. The second trace change the rise time to t_{r2} = 10 ns (same effect if fall- and rise-time swopped) and shows an increase in the spectral content above 3.18 MHz. The third trace shows $t_{r3} = t_{f3}$ = 10 ns and a further but slighter increase in noise spectral content is shown, placing the second trace with different rise- and fall-times in perspective.



(a) (b)

Figure 3.11. Trapezoidal simulation: (a) SPICE setup and (b) simulated trapezoidal plots for different rise- and fall-times.

Changing the switching frequency, while keeping the rise- and fall-times constant at 100 ns, the duty cycle at 50%, the amplitude at 100 V has the effect as shown in Figure 3.12. The increase in switching frequency increases the spectral slope amplitude, showing that the high switching speeds achieved with the present Silicon Carbide (SiC) and Gallium Nitride (GaN) devices will have a detrimental effect on the high frequency spectral amplitude.

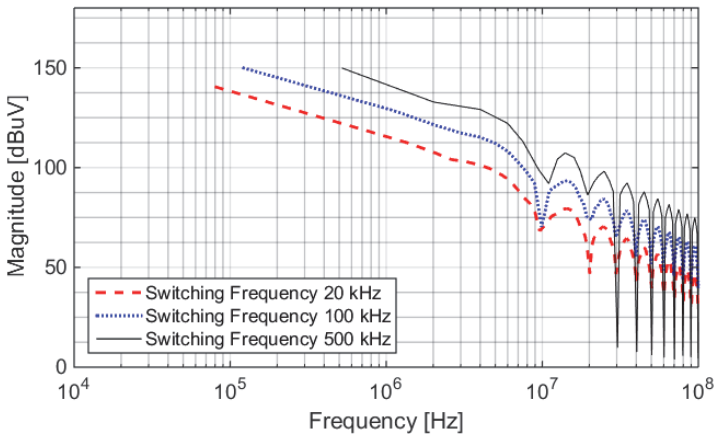
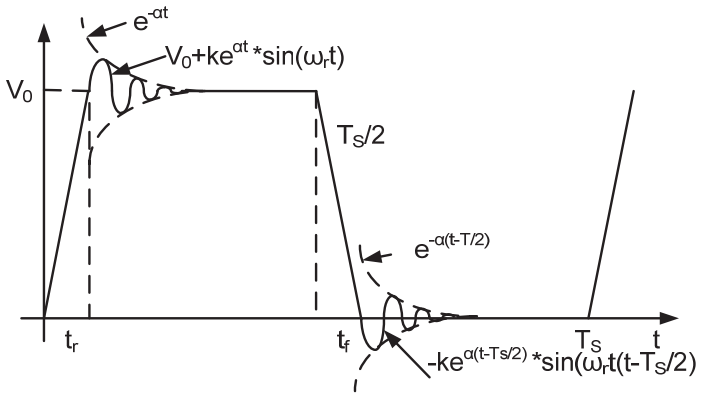


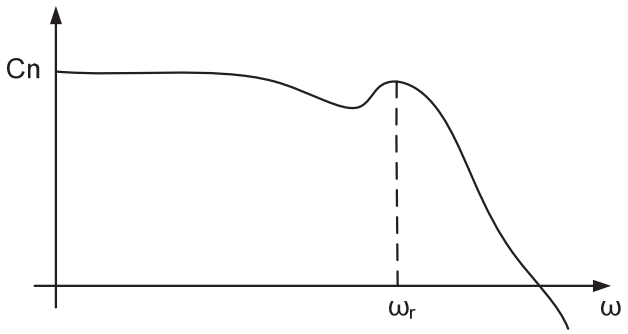
Figure 3.12. Trapezoidal waveform spectral slope variable frequency.

3.4.3 Trapezoidal wave with superimposed ringing

To further investigate an even more realistic switching signal, the ringing effect is imposed on the trapezoidal signal. The effect of a 1 MHz ringing signal as a result of parasitics is imposed on the trapezoidal signal is illustrated in Figure 3.13. It consists of the sum of 3 periodic waveforms, trapezoidal wave, damped sinusoidal at the rising slope and the same damped signal inverted and shifted ahead in time by 0.5 T_S imposed on the falling slope. A clear increase in the spectral content is visible at the ringing frequency ω_r.



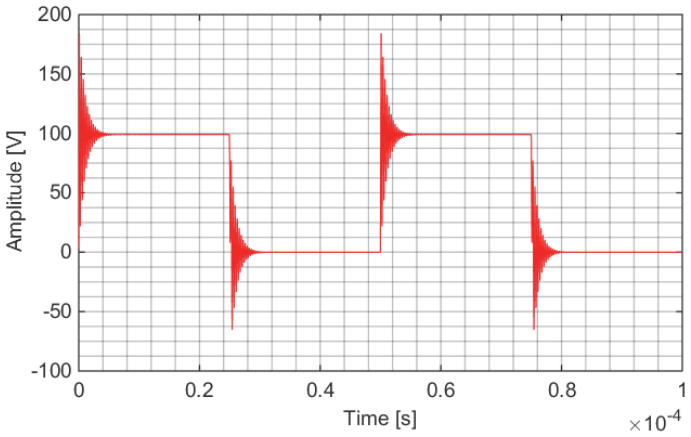
(a)



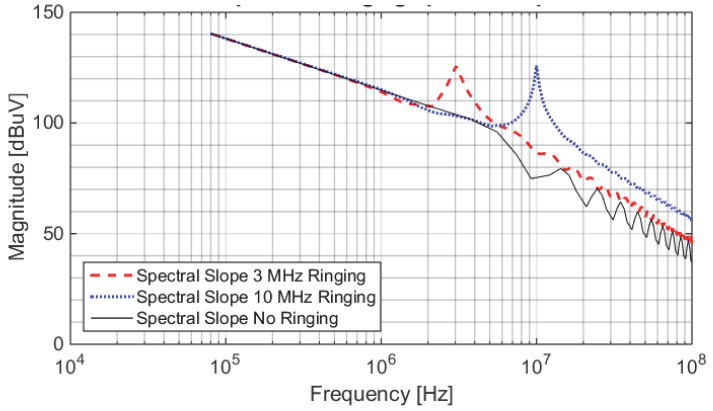
(b)

Figure 3.13. (a) Ringing effect on switching waveform and (b) frequency domain spectral content.

A SPICE generated trapezoidal ringing signal is shown in Figure 3.14 (a), representing a typical switching signal with parasitics. The rise-and fall-times are set to 100 ns, the amplitude 100 VPP, period is 50 µs and the duty cycle 50 %. The ringing frequency is a sine wave with a damping coefficient of 10^6 and frequency 3 MHz and in a second case, with the same parameters at 10 MHz, showing a clear rise in the spectral content at that frequency as well as the effect of a higher ringing frequency, raising the high frequency slope amplitude.



(a)



(b)

Figure 3.14. Ringing imposed on trapezoidal signal.

3.5 SUMMARY

The noise source switching signal was analysed in detail. First the simpler square wave and its expansion coefficients calculated showing the frequency spectrum slope amplitude effects on switching frequency as well as duty cycle. Secondly, the trapezoidal wave was introduced and analysed, showing the effects of rise- and fall times. Lastly, a ringing sinusoidal wave was superimposed on the trapezoidal wave, analysing a realistic switching wave, and the effects thereof analysed. This allowed the effects of practical simulating waveforms on noise to be investigated.

The LISN and conducted emission modes were introduced defined and calculated. The discrepancy in literature with the differential and to a lesser extent, the common mode noise equations in terms of the LISN ports was pointed out. New equations were derived from first principles and verified to be correct.

CHAPTER 4 MODELLING – NOISE PROPAGATION

4.1 INTRODUCTION

The fundamental noise path characteristics will be presented in this chapter, providing insight to the noise modelling environment.

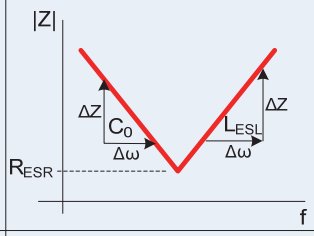
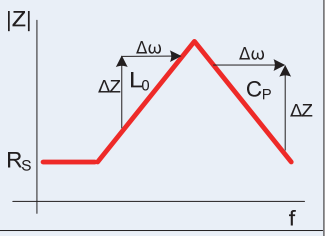
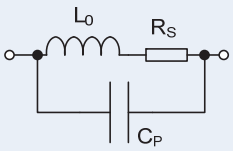
4.2 NOISE PATH MODELLING

The noise path consists of components, traces and structures. The high frequency models of these devices and structures form part of the noise path [45] and is an important aspect of noise modelling. Accurate component models form the basis of noise modelling, for the inclusion of all applicable frequency dependant effects in a typical time domain simulation. Extracting the high-frequency component models is done by measuring the impedance of such components. Three methods will be used to measure impedances of the noise path components; Vector method using an oscilloscope and signal generator calibrated to 100 MHz, the HP 4192 LF Impedance Analyser operating from 5 Hz to 13 MHz and a network analyser, the HP8753C operating from 300 kHz to 3 GHz. The first method utilises general laboratory instruments normally available in a power laboratory and is a practical inexpensive method, but very time consuming. The second method utilising the impedance analyser is quick and accurate, but only frequencies below 13 MHz can be characterised. Higher frequencies are measured with a network analyser, and the third method, provides the s-parameters of the component and need to be converted to impedance. A LABVIEW program was written to extract the s-parameter data from the network analyser's GPIB port to USB on a PC. All methods described are implemented, but the most convenient are the combination of the impedance analyser and the network analyser, covering all the frequencies of concern.

Equivalent circuit parameters are extracted from the impedance graphs and the results verified with a SPICE simulator and compared to the measured impedance. For simple

components, as portrayed in Table 4.1, the technique is well suited. From the impedance graph, the high frequency circuit parameters are extracted. When high frequency resonance occurs as well as when non-conventional impedance plots are to be extracted, a more comprehensive method is needed. An example is the vector fitting (VF) technique [46], [47], widely used for fitting a rational function for frequency domain response. The equivalent circuit for a rational function can be obtained from the measured impedance.

Table 4.1 Simple component circuit extraction.

Component	Capacitor	Inductor
Low Frequency Symbol		
Impedance Measurement		
High Frequency Equivalent Circuit		

In VF computation, the frequency domain responses are replaced with rational function approximations (4.1), fitting a ratio of two polynomials to the data [46]:

$$f(s) \approx \sum_{n=1}^{N} \frac{r_n}{j\omega - p_n} + m + j\omega n \tag{4.1}$$

The residues r_n and poles p_n are real quantities or conjugate pairs, while m and n are real values.

4.2.1 Practical complex impedance measurement – Method 1

Accurate impedance modelling and measurement of components are important when assembling an EMC model of a power converter [35], [48]. High frequency complex impedance measurement, up to 100 MHz, is more difficult to achieve. It requires much

more than to simply measure the capacitance or inductance of a component with standard laboratory instruments. Expensive measurement equipment that can perform this task exists, but the infrequent use of these instruments doesn't justify the cost. Therefore it is difficult to motivate the purchase of such instruments for the electronic laboratory. Although more tedious, simpler methods with acceptable accuracies to create conducted emission models up to 100 MHz are possible.

Practical components have a series resistance, in addition to multiple contributors to their reactance. For instance, a capacitor has an effective series inductance (ESL) that becomes dominant at high frequencies. When measuring the capacitance, it will impact on the reading, but ESL is not measured as a separate distinct component.

The impedance of a device can be calculated through complex division of the voltage and current i.e. as a ratio of voltage to current. This can be measured by applying a sinusoidal voltage to the device in series with a known resistor, and measuring the voltage across the resistor. The measurement is performed by sweeping the frequency over the band and thus providing required impedance phase and magnitude. The unknown impedance is modelled as a series circuit consisting of an unknown resistance R and an unknown reactance jX. The magnitude of the impedance is Z. The circuit for measuring the complex impedance of applicable components, traces and power feed-lines, is shown in Figure 4.1. The voltages in Figure 4.1 (a) can be portrayed as vectors, as shown in Figure 4.1 (b) where values of V_A, V_Z and φ are known. Figure 4.1 (c) shows the test setup, the signal generator on the left hand side and the oscilloscope measurement on the right.

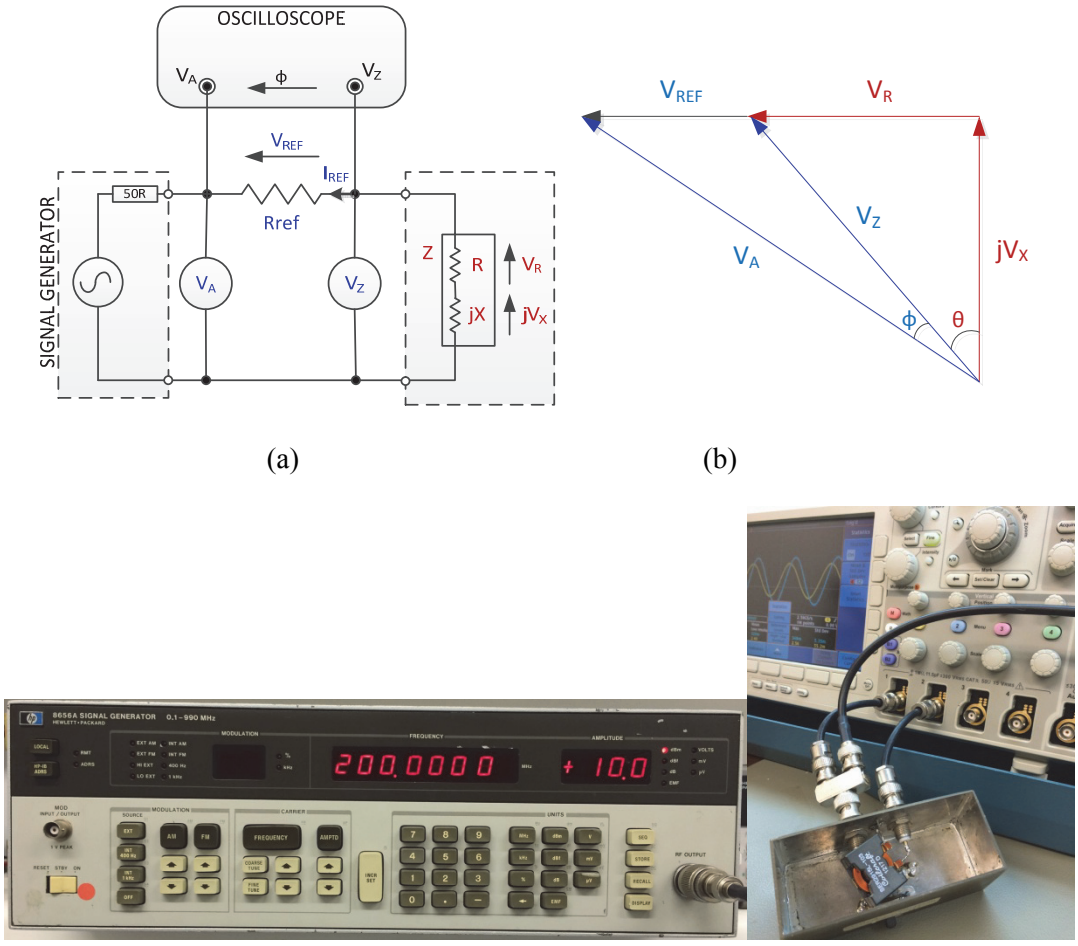


Figure 4.1. Complex impedance measurement: (a) The circuit, (b) impedance vectors and (c) the set-up with signal generator and digital oscilloscope.

The impedance Z can be easily derived:

$$Z = \frac{V_Z}{I_S} = \frac{V_Z}{V_A - V_Z} \cdot R_{ref} \tag{4.2}$$

Rewriting in polar-form and using the law of cosine to determine θ, gives rise to the following expressions

$$Z = \frac{V_Z \cdot R_{ref}}{\sqrt{V_A{}^2 - 2V_A V_Z \cdot \cos\theta + V_Z{}^2}} \tag{4.3}$$

the angle θ can be calculated as:

$$\theta = \phi - \tan^{-1}\left[\frac{-V_A \cdot \sin\phi}{V_Z - V_A \cdot \cos\phi}\right] \tag{4.4}$$

Converting back to rectangular form yields:

$$|Z| = Z \cdot \cos\theta + jZ \cdot \sin\theta \tag{4.5}$$

the resistive part, for example R_{ESR}, is obtained as:

$$R = R_{ESR} = Z \cdot \cos\theta \tag{4.6}$$

The expression for capacitance is obtained as:

$$C = \frac{1}{2\pi f Z_C \cdot \sin\theta} \tag{4.7}$$

The expression for inductance is given by:

$$L = \frac{\sin\theta}{2\pi f Z_L} \tag{4.8}$$

The method presented was used to determine analytically values of the various passive components constituting the noise path in the converter. Those include: input- and output capacitors, filter inductors, traces as well as the very important power feed-line to the converter. The power feed-line is constructed according to MIL-STD-461F, with the only difference being that it is shortened from the prescribed 2 m to 1 m, increasing the half-wavelength (λ/2) frequency from 75 MHz to 150 MHz, outside the measurement band, reducing radiating losses. This was to enable measurements of conducted emissions to be carried out more accurately up to 100 MHz.

4.2.2 The impedance analyser – Method 2

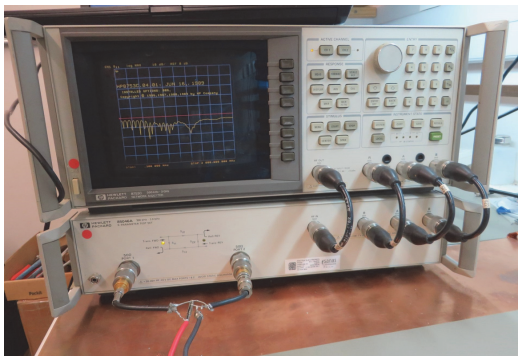
Figure 4.2 shows the HP 4192 LF Impedance Analyser, used for gain- phase measurements as well as impedance measurements (|Z|, |Y|, R, X, G, B, L, C, D, Q) from 5 Hz to 13 MHz. No equivalent circuit capability exists on this unit, but is available on newer models.

Figure 4.2. The impedance analyser HP 4192A.

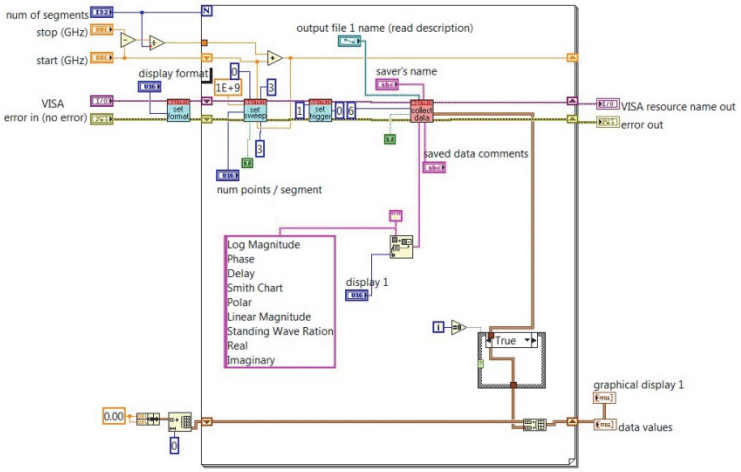
With the impedance analyser, the components are characterised from 10 kHz to 13 MHz. No external interface exist on this machine, values are written down at intervals and captured in a .csv file for further analyses and presentation.

4.2.3 The network analyser – Method 3

Figure 4.3 (a) shows the HP8753C network analyser operating from 300 kHz to 3 GHz. The conducted emission technical measurement capability is calibrated to 100 MHz, and modelling accuracy maintained to similar frequencies. For clarity as well as to get accuracies up to and around 100 MHz, some critical components are characterised up to 200 MHz. Figure 4.3 (b) gives the LABVIEW object orientated code for the GPIB to USB port. The information is captured on a PC in a .csv file format. The graphical interface is seen in Figure 4.3 (c). This new software capability on a very old and legendary machine provides it with a modern upgrade extending its useful lifespan.



(a)



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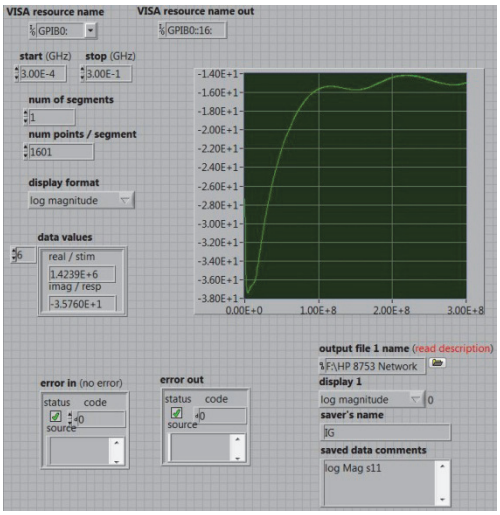


(c)

Figure 4.3. (a) The HP8753C s-parameter network analyser, (b) the LABView code and (c) the PC graphical interface output.

To convert from s-parameter to impedance, (4.9) is applied, with $Z_0 = 50\ \Omega$.

$$Z_{Line} = \frac{Z_0}{2} \cdot \frac{S_{21}}{1 - S_{21}} \tag{4.9}$$

4.2.4 Characterising the power circuit noise path

Components making up the noise path of a typical converter are characterised. The step-down as well as step-up converter in various formats, such as multi-level and multi-phase, will be modelled in the next chapter. The component models for such circuits are now modelled and verified with measurement. A typical surface mount circuit, about 30 W total power is envisaged, open loop as well as microprocessor controlled (up to 7 levels). Furthermore, incorporating large component effects, a 200 W discrete component converter will also be modelled and analysed, including the heatsink effects. The measurement bench will be incorporated in the conducted EMC models. The component models and effects described further on are based on these converter units.

4.2.5 Converter capacitor modelling

The circuit models will be for surface mount as well as radial capacitors. The applicable selection of capacitors is shown in Figure 4.4. Surface mount technology uses the SMT electrolytic capacitors and high capacitance (in the order of 100 µF) 1206 ceramic multilayer capacitors that can be paralleled to form larger capacitance values.

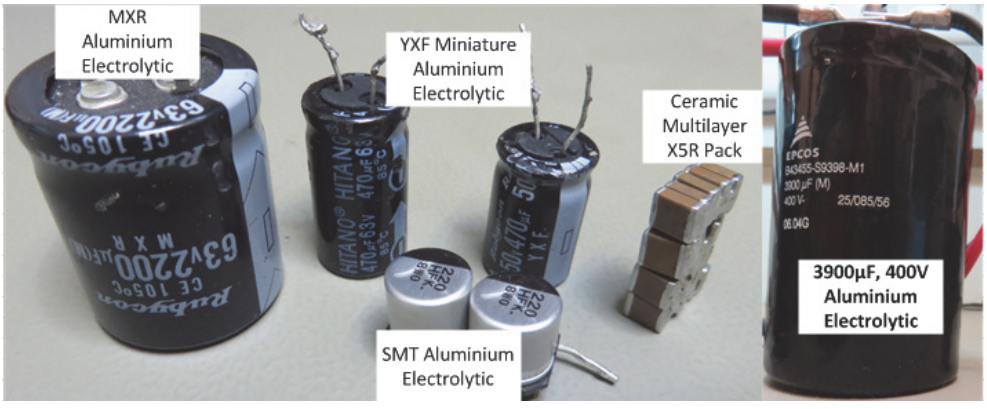


Figure 4.4. Electrolytic and ceramic capacitor selection.

Effective Series Resistance (ESR) of a capacitor depends on the dielectric loss due to the dielectric materials. The resistivity of the electrode material, the shape and number of layers determine the ESR. At higher frequencies around the resonant point, the skin- as well as proximity effects have an influence on the ESR. The Effective Series Inductance (ESL) in ceramic capacitors is largely affected by the capacitor internal electrode structure, together with the lead length of the capacitor. The ESL determines the self-resonant frequency which in smaller surface mount capacitors is generally very high.

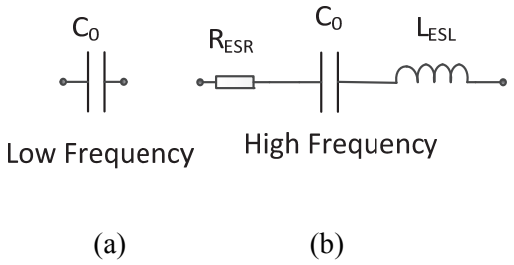


Figure 4.5. Capacitor models (a) low frequency and (b) high frequency.

An expression for the capacitor's high frequency impedance is obtained with reference to Figure 4.5 (b) as follows:

$$Z_C = Z_{L_{ESL}} + Z_{R_{ESR}} + Z_{C_0} \tag{4.10}$$

$$Z_C = R + jX = R_{ESR} + j(\omega L_{ESL} - \frac{1}{\omega C_0}) \tag{4.11}$$

$$|Z_C| = \sqrt{ZZ^*} = \sqrt{R^2 + X^2}$$

$$|Z_C| = \sqrt{\left({R_{ESR}}^2 + \left(2\pi f L_{ESL} - \frac{1}{2\pi f C_0} \right) \right)^2} \tag{4.12}$$

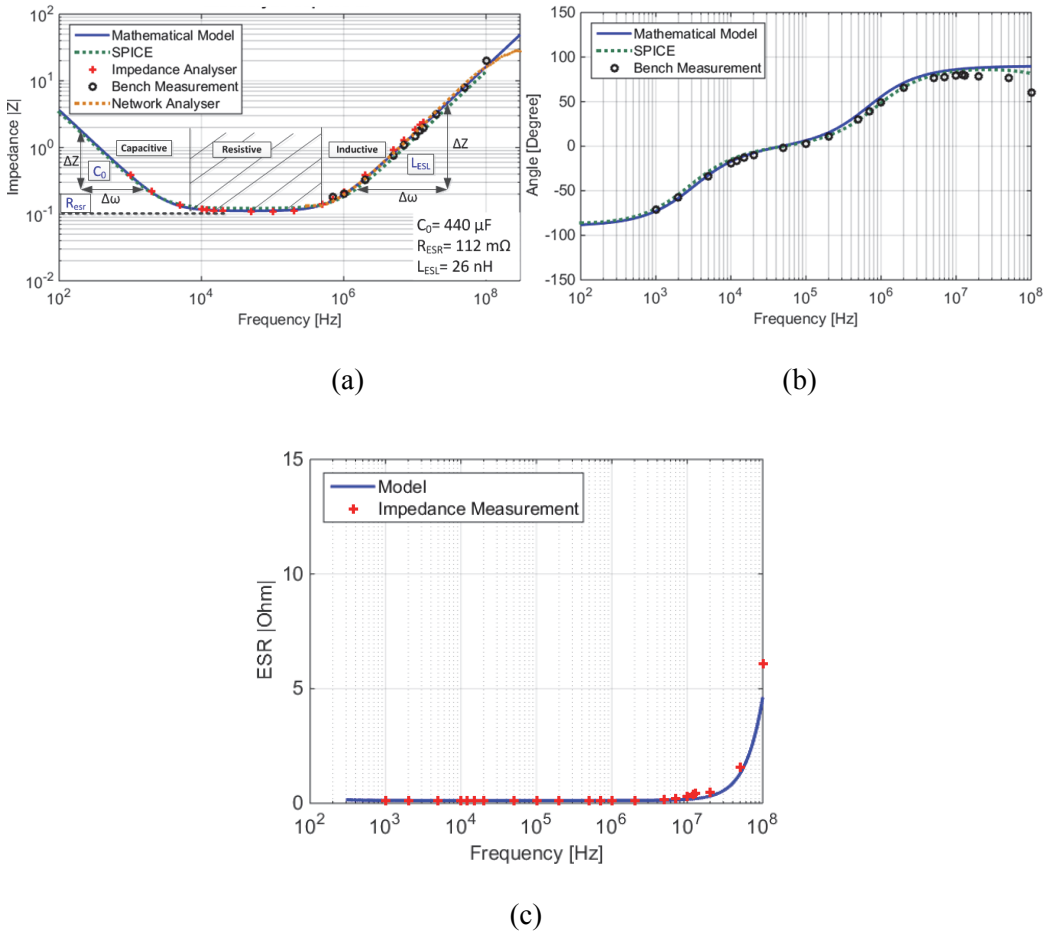
With θ being given by

$$\theta_C = \arctan \frac{X_C}{R_{ESR}} \tag{4.13}$$

If $X_C > 0$, the reactance is inductive, purely resistive if $X_C = 0$, and capacitive if $X_C < 0$. The self-resonant frequency (the series resonant frequency) of a capacitor is given by:

$$f_{srf} = \frac{1}{2\pi\sqrt{L_{ESL} C_0}} \tag{4.14}$$

The standard 3-element capacitor model [49] [50], has been verified and provides accurate results up to 100 MHz for the regular sized capacitors. Figure 4.6 (a) shows the impedance plot and (b) the phase results of a 470 µF, 63 V metal film electrolytic capacitor. Three techniques have been used to determine the impedance plot; the oscilloscope and signal generator measurements (up to 100 MHz), the impedance analyser measurements (up to 13 MHz) and the network analyser (up to 300 MHz). This model can be generalised for other capacitors utilised in the switch-mode DC-DC conversion supplies. Figure 4.6 (c) provides the high frequency ESR plot, and an increase is seen beyond 10 MHz.

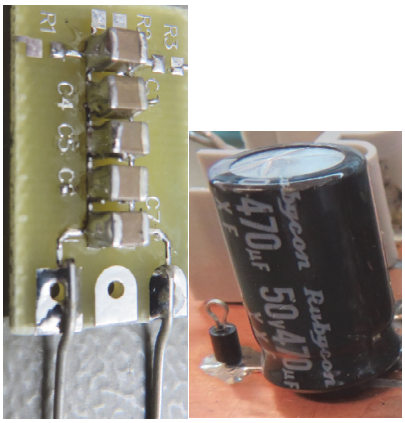


(a) (b)

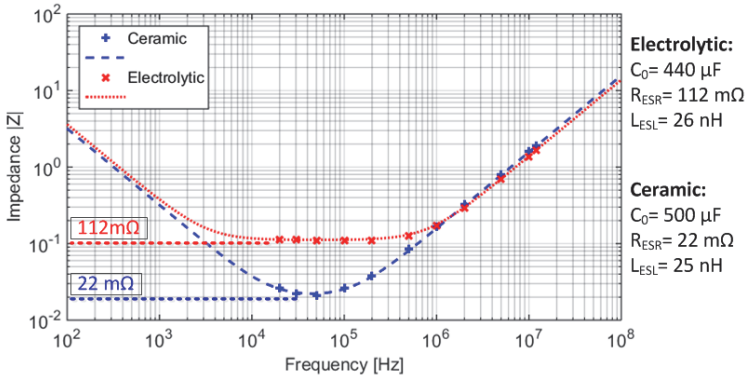
(c)

Figure 4.6. Converter capacitor model impedance verification: (a) Magnitude (b) Phase and (c) ESR.

The input capacitor to the step-down DC-DC converter is aluminium electrolytic, 470 uF and rated at 63 V. It exhibits a large ESR value, because of the high resistivity of its electrolyte material. This will be shown to be detrimental to conducted EMC levels. The ceramic capacitor uses metallic materials for its electrodes and therefore exhibits much lower ESR values than aluminium electrolytic capacitors or even tantalum capacitors and will be shown to lend to lower conducted EMI. Due to the physical construction and paralleling of the ceramic capacitors by using PCB tracks, the L_{ESL} of the two components are approximately the same.



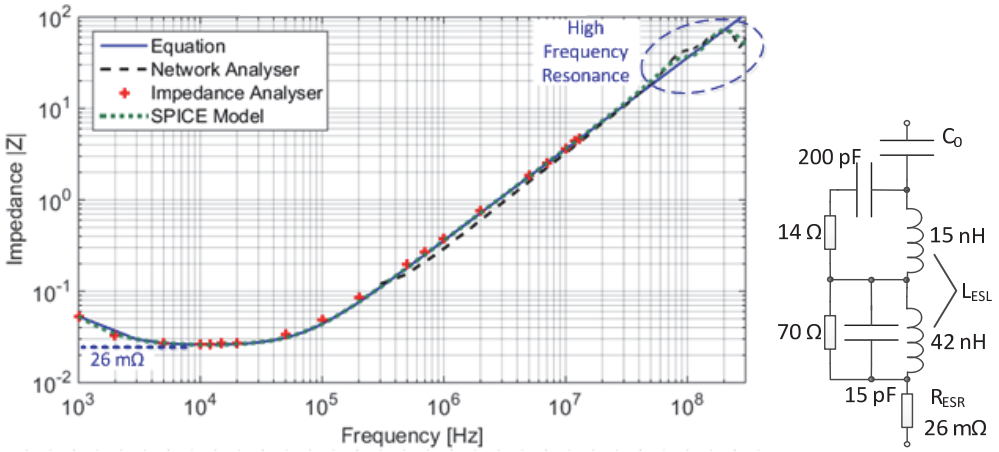
(a)



(b)

Figure 4.7. (a) Ceramic and electrolytic capacitor and (b) impedance magnitude comparison.

Larger capacitors, the 3900 µF, 400 V electrolytic as in Figure 4.4, show a slight discrepancy close to 100 MHz as seen in Figure 4.8 (a). For a better approximation, the high frequency model of the capacitor is upgraded in Figure 4.8 (b), showing C_0, L_{ESL} and R_{ESR} with added resonant loops to trace the measured impedance at 100 MHz more accurately. A higher order equivalent circuit can improve the overall performance of the model.



(a) (b)

Figure 4.8. (a) Larger capacitor high frequency effects and (b) equivalent circuit.

4.2.6 Power inductor modelling

Of all the basic passive components models, the inductor is the most difficult to realise. The inductor types to be used in the subsequent noise modelling circuits, will have a combination of surface mount, leaded as well as toriodal types, the latter comprising of two types; solid wire as well as litz wire, as shown in Figure 4.9.

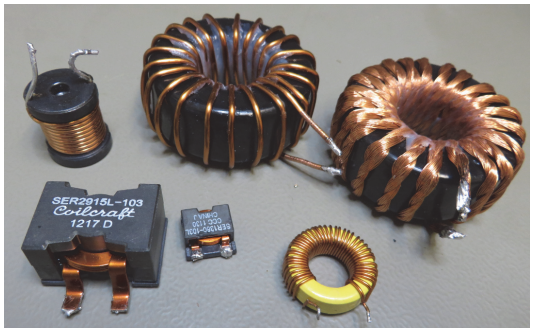
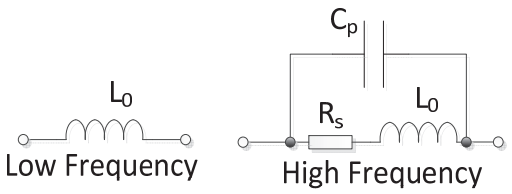


Figure 4.9. Surface mount and leaded inductor selection for modelling.

The commonly used high frequency 3-element inductor model is shown in Figure 4.10.



(a) (b)

Figure 4.10. Inductor models: (a) Low frequency and (b) high frequency (model 1).

An expression for the total high frequency inductor impedance is given by:

$$\frac{1}{Z_L} = \frac{Z_{C_P} \cdot \left(Z_{L_0} + Z_{R_S} \right)}{Z_{L_0} + Z_{R_S} + Z_{C_P}} \tag{4.15}$$

By expanding (4.15) and rearranging, impedance magnitude is obtained as:

$$|Z_L| = \sqrt{\frac{\left(\frac{L_0}{C_P}\right)^2 - \left(\frac{R_S}{\omega C_P}\right)^2}{R_S{}^2 + \left(\omega L_0 - \frac{1}{\omega C_P}\right)^2}} \tag{4.16}$$

The self-resonant frequency (parallel resonant frequency) of the inductor is given by:

$$f_{prf} = \frac{1}{2\pi\sqrt{L_0 C_P}} \tag{4.17}$$

The inductor model (model 1) shown in Figure 4.10 and expressed in (4.17) gives an infinite peak at the self-resonant frequency. If the inductor is to be used as an AC blocking component, for example, the three-element inductor model might be good enough. However, in high frequency EMC analysis applications, the generally accepted inductor model needs improvement to make it more accurate for each inductor type, especially around resonant frequency and beyond. There are three possible ways to improve the model. If one progresses to a 4- or 5-element inductor: a resistor, R_P, could be added in parallel with the capacitor as in Figure 4.11 (a) a resistor, R_{Cp}, could be added in series with the capacitor as in Figure 4.11 (b), or both R_S and R_P could be added to the model as shown in Figure 4.11 (c). However, the latter complicates model analysis even further. The

more complex 5-element model can be considered, but is usually implemented with tuned circuits where the quality factor, Q, of the inductor and the accuracy of the frequency where it occurs is of utmost importance.

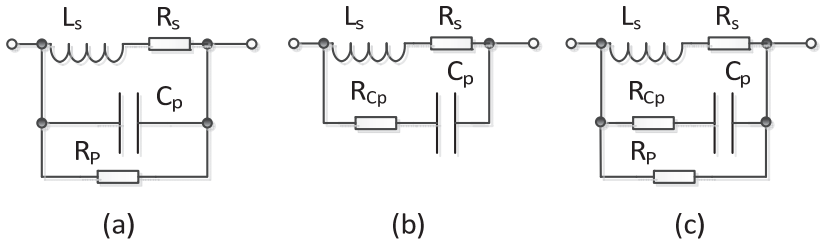


Figure 4.11. Improved 4-element inductor circuit model: (a) Model 2 adding parallel resistor, (b) model 3 adding R_{Cp} and (c) 5-element model with both R_P and R_{Cp}.

The impedance for the 4-element inductor model in Figure 4.11 (a) is given as:

$$|Z| = \sqrt{\frac{\left(\frac{L_s \cdot R_p}{C_p}\right)^2 - \left(\frac{R_s \cdot R_p}{\omega C_p}\right)^2}{\left(R_s + R_p\right)^2 + \left(\omega L_s - \frac{1}{\omega C_P}\right)^2}} \tag{4.18}$$

The impedance for the 4-element inductor model in Figure 4.11 (b) is given as:

$$|Z| = \sqrt{\frac{\left(\frac{L_s}{C_p} + \frac{R_S}{R_{cp}}\right)^2 - \left(\frac{R_s}{\omega C_p} + \omega R_{cp} L_s\right)^2}{\left(R_s + R_{cp}\right)^2 + \left(\omega L_s - \frac{1}{\omega C_P}\right)^2}} \tag{4.19}$$

The above inductor models are compared to the measured results of a flat conductor wound 10 μH inductor on an E20-core, and yield the impedance plots in Figure 4.12. Model 1 is the generalised 3-element model, showing an infinite peak at resonance. Model 2 with the added parallel resistor R_P = 1 kΩ, compared exactly to the measurement. Model 3 with the resistor R_{Cp} set at 250 Ω, added to the generalised version, with slight discrepancy at and above the resonant frequency. Model 4, the 5-element version, compares exactly to the measured results.

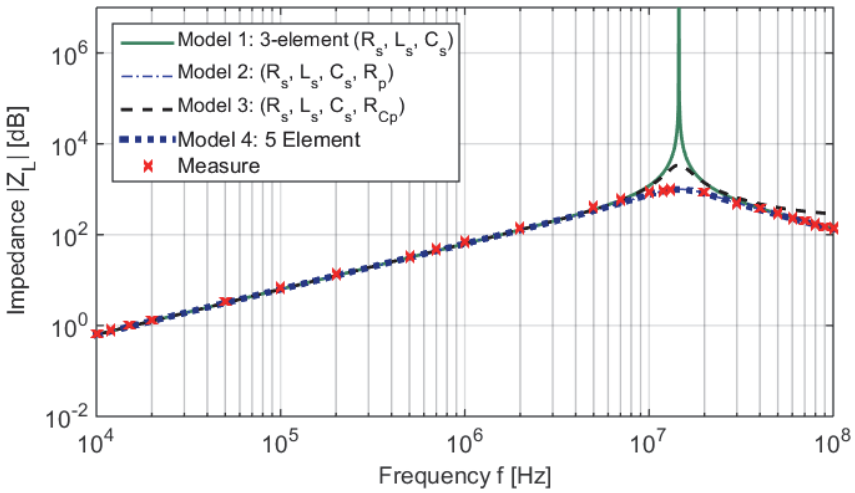


Figure 4.12. Compare inductor models to measured data.

The model in Figure 4.11 (a) (as well as the more complex model in (c)) compares accurately to the measured data up to 100 MHz. The model in (b) is shown with two values, 250 Ohm and 10 Ohm, both not providing accurate comparisons to measured data. The 5-element model gives the same accuracy as the 4-element model in (a), but due to the added complexity it will not be used. Given the above background, specific inductors, from small sizes (tens of watts) up to higher power applications (around kW) will be investigated in more detail.

4.2.6.1 Coilcraft SER2915L-103

A 10 µH inductor, the SER2915 from Coilcraft, impedance plot is shown Figure 4.13. The inductor is analysed and verified with measured results, the oscilloscope-signal generator technique, the impedance analyser as well as the network analyser for the high frequency impedance and compared to the SPICE model. The 4-element model yields an accurate representation of the impedance close to the resonant peak. Its results show very good correspondence with the measured impedance. This model can be generalised for other power inductors in the DC-DC conversion topologies.

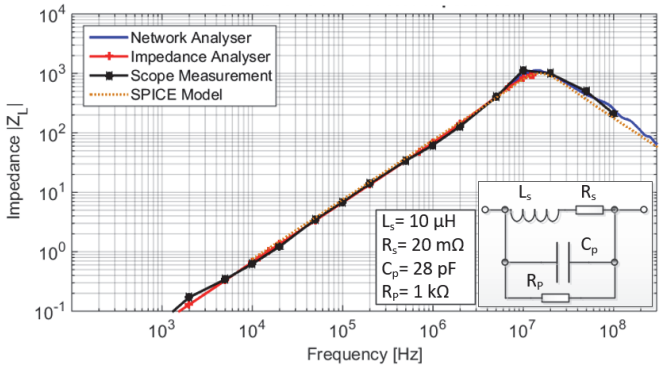
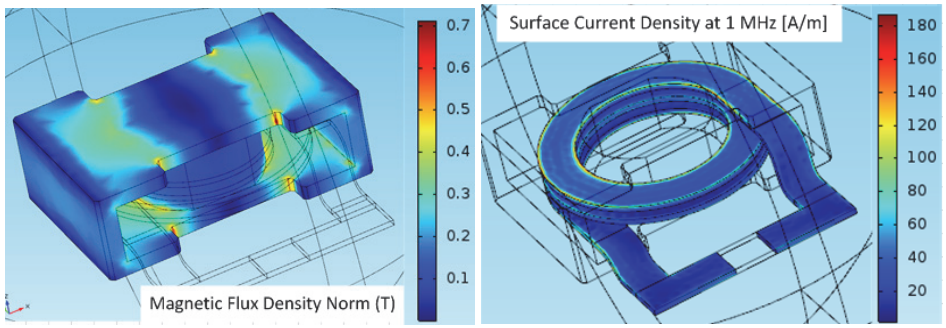


Figure 4.13. Power inductor equivalent high frequency impedance.

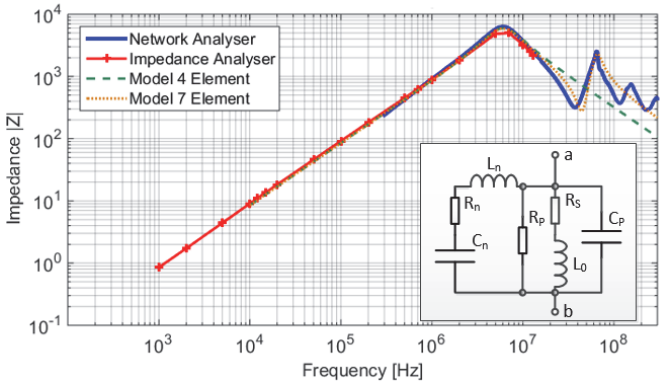
The SER2915 inductor is modelled with COMSOL Multiphysics. Due to its enclosed core design, the magnetic flux is well contained, as shown in Figure 4.14 (a). Figure 4.14 (b) shows the surface current density on the windings, initiated with a 1 A current at 1 MHz. The currents are concentrated towards the edges of the conductor.



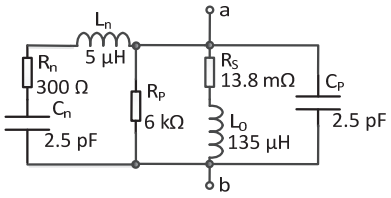
(a) (b)

Figure 4.14. COMSOL simulation of SER2915 inductor (a) flux density (a) and (b) coil current density.

The larger toroidal inductors as shown in Figure 4.9 consist of multiple resonant effects and require more complex circuitry to realise the equivalent circuit to incorporate the in-band resonant effects. The solid-wire toroidal inductor impedance shown in Figure 4.15 (a) has 22 turns, measures 135 µH, C_P = 5.3 pF and R_S = 13.8 Ω, but requires a 7-element equivalent circuit, shown in Figure 4.15 (b), to realise the impedance plot up to 100 MHz. The litz-wound toroidal inductor shown in Figure 4.16 (a) has similar parameters, except C_P = 22 pF and requires a 10-element equivalent circuit, as shown in Figure 4.16 (b), due to the increased parasitic effects of the litz wire.

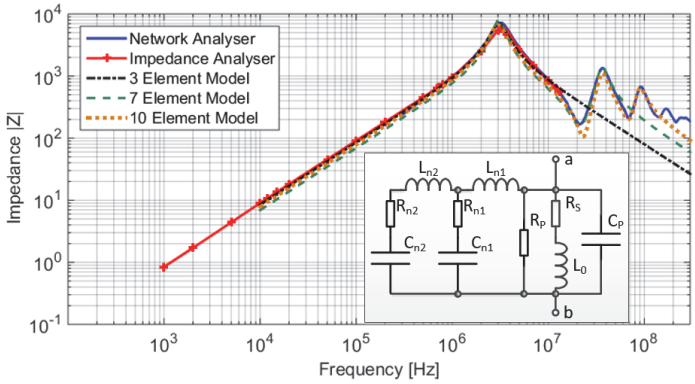


(a)

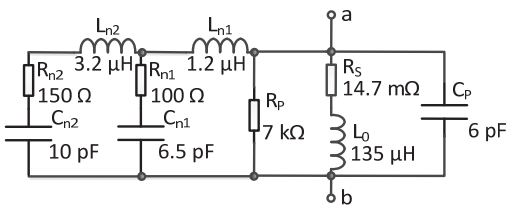


(b)

Figure 4.15. Impedance characteristics of (a) the solid-wire toroid and (b) its equivalent circuit.



(a)

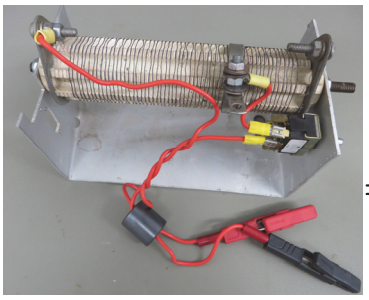


(b)

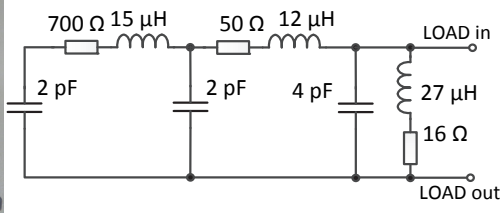
Figure 4.16. Impedance characteristics of (a) the litz-wound toroid and (b) its equivalent circuit.

4.2.7 Wirewound resistive load

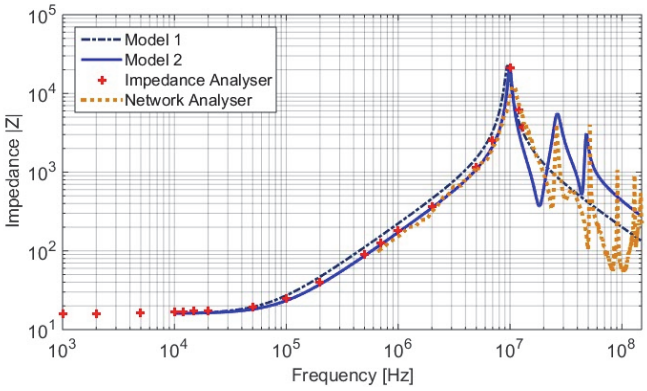
Most tests are conducted with a 200 W load as in Figure 4.17 (a), consisting of a wire wound resistor on a ceramic former. The equivalent circuit as derived from the impedance measurement is given in Figure 4.17 (b). The load is inductive, with L_L = 30 µH, the resistance is set to R_L = 15.76 Ω and the capacitance C_L is 8.5 pF. The impedance plot is provided in Figure 4.17 (c) showing the multiple resonant points beyond 20 MHz. The inductor model, Model 1, shows good correlation up to 10 MHz, thereafter it is not usable. The 9-element model Model 2, in the impedance plot, shown in Figure 4.17 (c) provides a more accurate presentation of the load impedance.



(a)



(b)



(c)

Figure 4.17. (a) 200 W test load, (b) the equivalent circuit and (c) its impedance characteristics.

4.2.8 PCB traces and wires

Stray inductance and capacitance in both power devices and PCB traces have an influence on the high frequency content during the switching transients. Quantifying these effects is

a relevant issue since they play an important role in different power loss mechanisms as well as EMI.

The self-inductance of a single wire as shown in Figure 4.18 can be given using the following well known equation, [51] and [52].

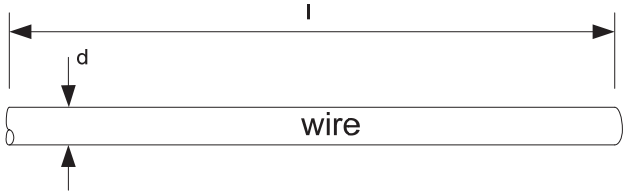


Figure 4.18. Single wire.

$$L[nH/mm] = 0.2 * \left\{ ln\left[\frac{l}{d}\right] - 3/4 \right\} \quad (4.20)$$

Figure 4.19 shows a plot of inductance versus wire length with variable diameter d. Wire diameters of 1 mm, 5 mm and 10 mm are shown. An impedance analyser was used to verify these analytical values, all measured at a reference frequency of 100 kHz.

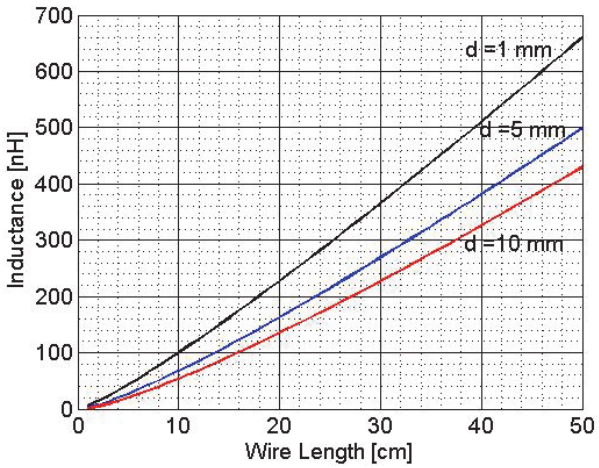


Figure 4.19. Wire Inductance.

The resistance of above wire is obtained using the following equation:

$$R = \rho_{cu} \ell / A_w$$

$$= \frac{\ell}{\sigma_{cu} A_w} \tag{4.21}$$

where ρ_{cu} is the electrical resistivity of copper, ℓ the wire length and A_w the cross section of the conductor. The inverse of the electrical resistivity ρ_{cu} is the conductivity σ_{cu}. The conductivity for copper is:

$$\sigma_{cu} = 5.81 \times 10^7 \, S/m$$

In a typical scenario, for instance a power conductor feed to a small power converter, the copper wire of diameter d=1 mm and length 0.03 m can be used, and the resistance would calculate to be:

$$R_{30cm} = \frac{\ell}{\sigma_{cu}(\pi d^2/4)}$$

$$= 6.57 m\Omega$$

Increasing the 30 cm long copper wire diameter from 1 mm to 5 mm, the high frequency impedance shows a decrease in inductance as shown in Figure 4.20.

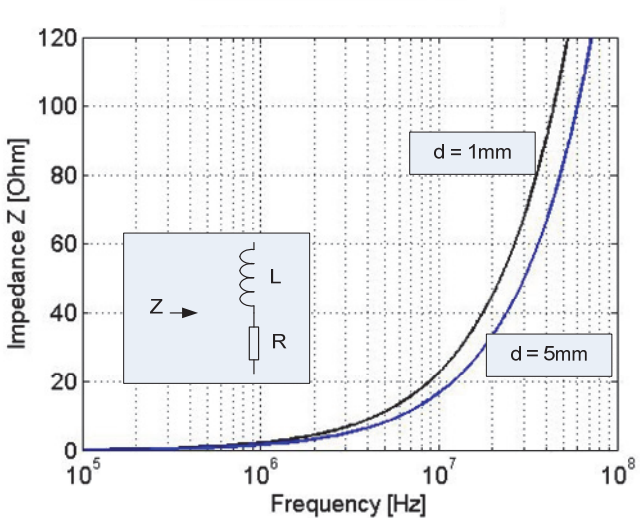


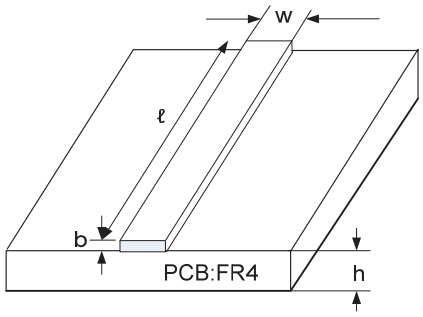
Figure 4.20. Single wire impedance with variable thickness.

Figure 4.21 (a) shows a single PCB trace with thickness *b*, width *w*, length *l* and distance *h* above a solid ground plane. For FR4 PCB material, $\mu_r = 1$ and $\varepsilon_r = 5$.

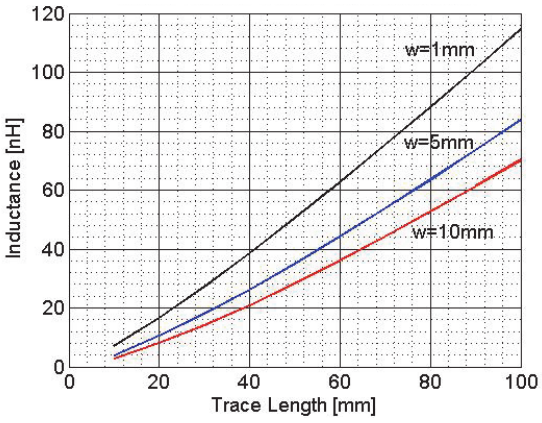
From [51] the inductance of a trace, as depicted in Figure 4.21 is given by the expression:

$$L[nH/mm] = 0.2 * \left\{ ln\left[\frac{l}{(w+b)}\right] + 1.193 + 0.224(w+b)/l \right\} \qquad (4.22)$$

Equation (4.22) is graphically presented in Figure 4.21 (b) with variable trace lengths commonly used in practice, of 10 mm, 15 mm and 20 mm. The trace thickness *b* was set at 70 µm (typical copper thickness of a power PCB) and the width *w* varied from 1 mm to 10 mm. For example, a 20 mm long trace with a set width of 5 mm, the inductance calculates to 10.5 nH.



(a)



(b)

Figure 4.21. Trace inductance for variable length *l*.

The resistance of the above trace can be calculated using (4.21). For a copper trace 1 mm wide, 10 cm long and 70 µm thick, the resistance would work out to be:

$$R_{10mm} = 24.6m\Omega$$

When current changes in one conductor and induces a voltage in another, mutual inductance occurs. The mutual inductance between two conductors or traces can cause unwanted coupling. The coupling coefficient k, with a value between 0 and 1, is a convenient way to specify the relationship between inductors.

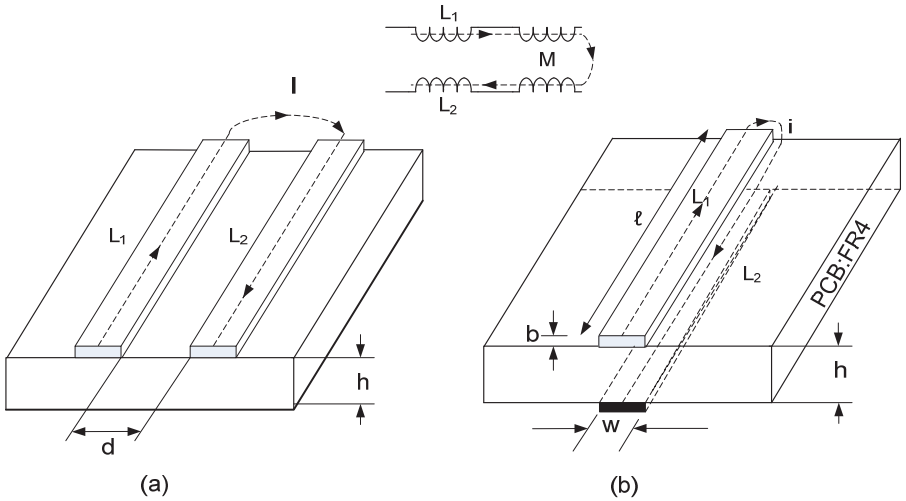


Figure 4.22. Trace mutual inductance layout.

The total inductance for the two layouts shown in Figure 4.22 is equal to:

$$L_T = L_1 + L_2 - 2 \times M \tag{4.23}$$

where L_1 and L_2 are the self-inductance of the specific conductors while M is the mutual inductance between the pair. So to minimize the total inductance of the complete current path, the mutual inductance between the conductors must be maximized. This can be achieved by placing the two conductors as close together as possible to minimize the area between them. The equation for mutual inductance for the layout in Figure 4.22 (a) is:

$$M(nH) = 200 \times l \times \ln(1 + (\frac{2h}{d})^2) \tag{4.24}$$

and thickness and width neglected for the layout in Figure 4.22 (b),

$$M(nH) = 200 \times \left[l \times \ln\left(l + \sqrt{l^2 + h^2}\right) + \sqrt{l^2 + h^2} + h\right] \tag{4.25}$$

Mutual inductance will be positive if the trace currents are in the same direction, the. If the currents are in opposite directions, the mutual inductance will be negative. Plotting these values for a strip length of 10 cm and varying the track spacing from 1 mm to 10 mm gives the mutual inductance values presented in Figure 4.23 for case (A) and case (B).

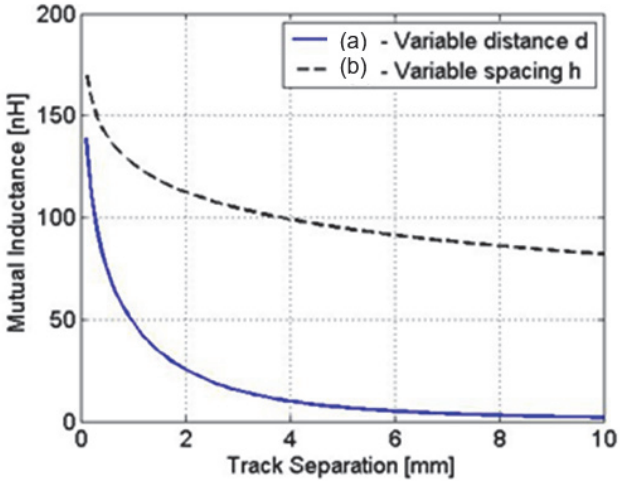


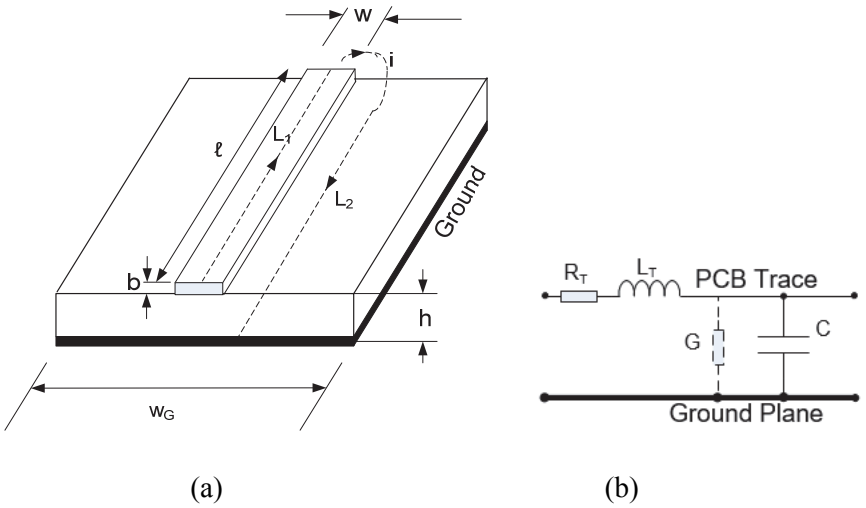
Figure 4.23. PCB trace mutual inductance for case (a) - Side by side and case (b) - Top-bottom.

Introducing a ground plane as shown in Figure 4.24 (a) and the consequent circuit model in Figure 4.24 (b), lowers the inductance of the trace substantially. The following equation can be used to calculate the inductance of the trace when a ground plane is present:

$$L_{trace} = l * \ln\left[1 + \frac{32h^2}{w^2} \times \left(1 + \sqrt{\pi \times \frac{w}{8h}}\right)\right] \tag{4.26}$$

The ground plane inductance is not affected by the PCB trace width and can be evaluated using the following expression:

$$L_{plane} = \frac{5 \times h}{w_G} \tag{4.27}$$



(a) (b)

Figure 4.24. PCB trace (a) with ground plane and (b) the equivalent PCB trace model.

Figure 4.25 shows the inductance of the trace and the ground plane separately. The trace is 10 cm long and 1 mm wide. The ground plane is 10 cm wide. In the graph, the distance h between the trace and plane are varied.

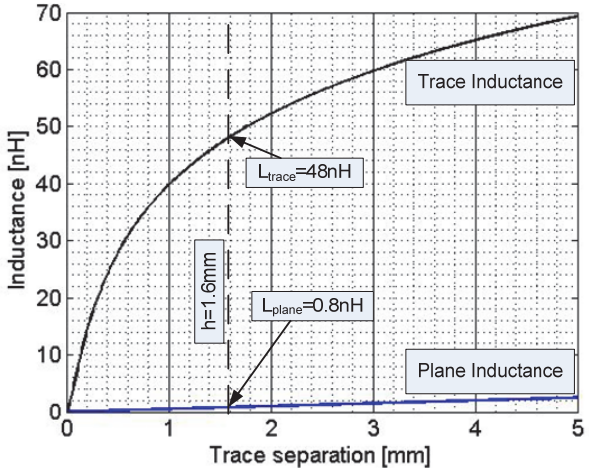


Figure 4.25. Inductance for a PCB trace and PCB plane.

For example, if the PCB thickness h is 1.6 mm, the inductance for the plane is 0.8 nH and for the PCB trace 48 nH. Note that, from Figure 4.21, a PCB trace inductance plot is given without the ground plane. Comparing with similar lengths and widths, the same trace inductance is 117 nH without the ground plane and 48 nH with a ground plane, an almost 2.5 times reduction in the trace inductance.

The PCB trace above a ground plane will have capacitance as well due to the two plate surface areas and the dielectric material separating them. The capacitance plate equation, as commonly presented in literature [53], is given by:

$$C \approx \frac{\varepsilon_r \varepsilon_0 S}{h}, S \gg h^2 \tag{4.28}$$

where ε_0 is the permeability of vacuum and equals 8.854×10^{-12} F/m, ε_r is the relative permittivity and for FR4 PCB it is about 4.8 and S is the total plate area of the trace with h the distance between the plates. This equation works well if two planes are of equal area, but will have substantial fringing effects if one plate is much larger than the other, thus giving a higher capacitance value. One such equation dealing with these effects is:

$$C(pF/in) = \frac{0.67(\varepsilon_r + 1.41)}{ln\left(\frac{5.98h}{0.8w+b}\right)} \tag{4.29}$$

In this particular instance, all dimensions are in inches. Using for example a copper trace of 1 mm wide, 10 mm long and 1.6 mm from the ground plane, the trace capacitance calculates roughly to 0.27 pF using (4.28), and when using (4.29) calculates a higher capacitance: 0.64 pF.

Making use of (4.28) and (4.29) the above equations and simulations the wire and trace characteristics can be modelled. A typical PCB trace has resistance, inductance, capacitance as well as conductance due to the dielectric material and its impedance as shown in Figure 4.26.

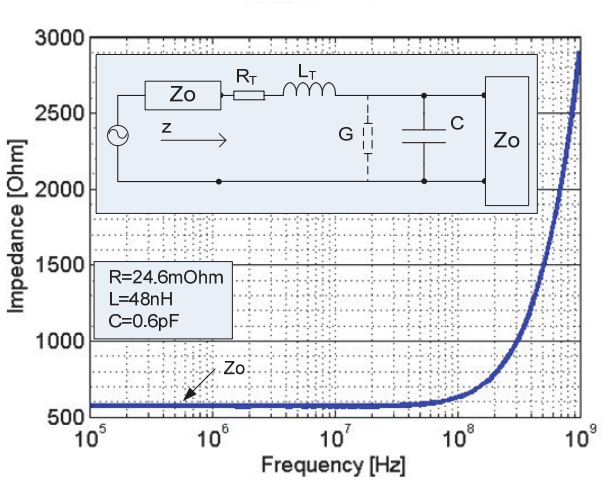


Figure 4.26. Trace impedance: RLGC transmission line.

4.2.9 PCB via inductance

Whenever there is vertical interconnected access (via) on a PCB, a parasitic inductance is formed. At a given diameter (d) the approximate inductance (L) of a via of a height (h) may be calculated as follows:

$$L_{via} \approx \frac{h}{5}\left(1 + ln\left(\frac{4h}{d}\right)\right) \quad [nH] \tag{4.30}$$

Figure 4.27 shows the via between the top-and bottom layer and applicable dimensions.

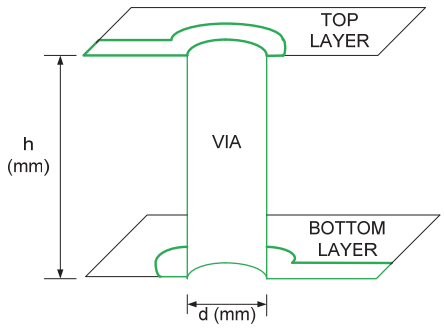


Figure 4.27. Via dimensions

As an example, a 0.4 mm diameter via through a 1.5 mm thick PCB has an inductance of 1.1 nH. Normally, in power circuits, multiple vias are used on a track to increase the

current throughput. Placing multiple vias in parallel can reduce the inductance exponentially.

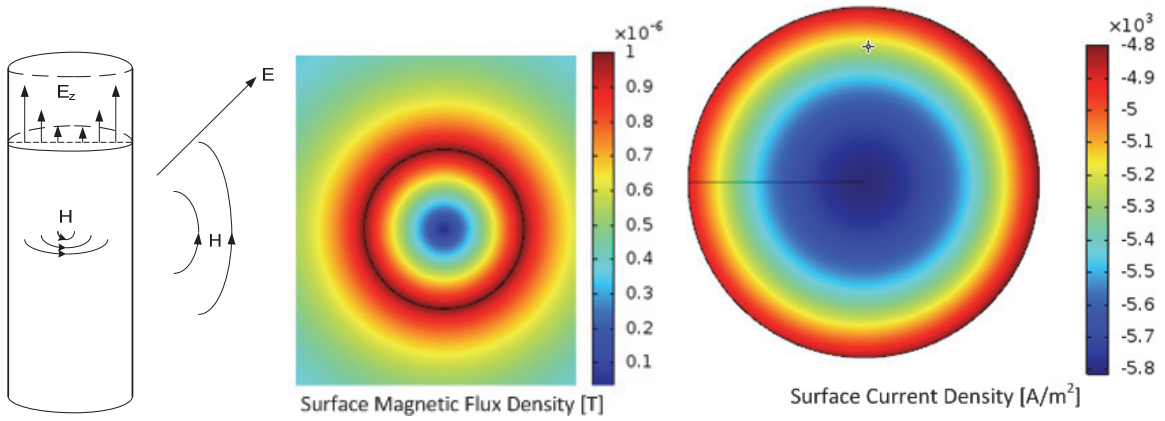
4.2.10 The skin and proximity effect

At DC and very low frequencies, current in a PCB trace or wire conductor follows the route of the lowest resistance. The low resistance path for current flowing in a PCB trace fills the volume of the trace, flowing uniformly throughout the conductor. When this current returns through the ground and /or power plane, it spreads out tending to occupy as much of the surface area of the ground planes as possible on its way back to the source.

At higher frequencies, above a few megahertz, the electromagnetic wave interacts with a conductive material; charges within the material are oscillating with the same frequency as the imposing fields, constituting an alternating electric current, with the magnitude of these alternating currents greatest at the conductor's surface. Skin effect is the tendency of an alternating electric current to distribute itself near the surface of the conductor. The decline in current density versus conductor depth is known as the skin effect.

In Figure 4.28 the conductor can be viewed as a guide for the electrical and magnetic fields around it. The current in the conductor is caused by the changing magnetic flux that penetrates into the conductor. This current opposes the magnetic field that causes it. The result is that the magnetic field decreases exponentially in strength as it penetrates the conductor. Skin effect is thus the tendency of the current in a wire to flow towards the surface of the wire more and more as the frequency of excitation is increased.

Inductors sometimes have some AC component induced on a large DC current component and the skin effect does not play a significant role. When no DC or small DC component is present with a large AC component, the skin effect plays a large role in determining the AC inductance and resistance of the conductor.



(a) (b) (c)

Figure 4.28. (a) Electric and magnetic fields around and inside circular conductor, (b) magnetic flux and (c) surface current.

The inverse of the attenuation constant α of the conductor is defined as the skin depth δ reaching a value of 1/e times the surface current density, and is defined as:

$$\delta = \frac{1}{\alpha} = \frac{1}{\sqrt{\pi f \mu_0 \sigma}} \tag{4.31}$$

The skin depth for three different materials, copper, silver and aluminium, is presented in Figure 4.29. Silver comprises of the shallowest skin depth while Aluminium portrays a deeper skin depth at the same frequency.

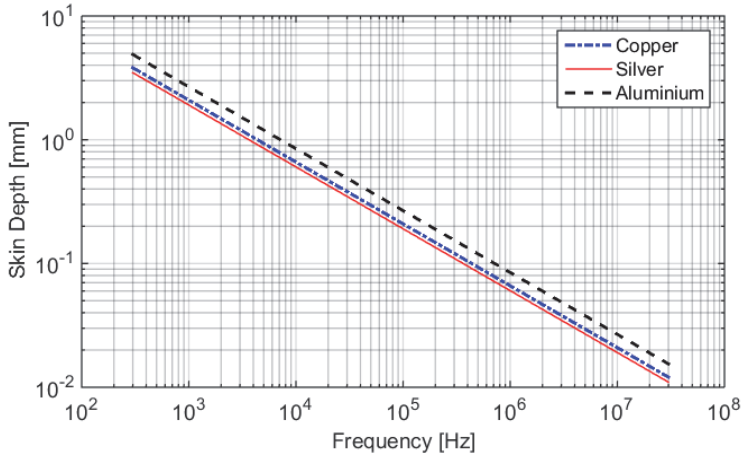


Figure 4.29. Skin depth for different materials.

Where σ is the conductivity of the material (conductivity for copper σ_{cu} = 5.8x10^7 S/m) and the permeability of air is μ_0 = 4πx10^{-7} H/m (μ_r for copper is unity).

For example, at 50 Hz, the skin depth for a round copper conductor is calculated to be 9.3 mm, and at 100 kHz it is down to 0.21 mm.

In two current carrying parallel wires, the current distribution across a cross-sectional area is not uniform. The magnetic fields from each wire affect the current flow in the other, resulting in a slightly non-uniform current distribution, which in turn increases the apparent resistance of the conductors. In parallel round wires it is called the proximity effect. The proximity effect mainly causes an increase in resistance loss. These transversal current distribution disturbances move the current off-centre from the conductor thereby reducing the effective diameter and the resultant inductance [52].

When only two conductors are in close proximity the influence of the proximity effect is relatively small compared to that of the skin effect. However, when more conductors are used, such as multi-layer windings of an inductor, or even high density layouts, it might have to be taken into account. The skin effect is more pronounced in conductors at high frequency than the proximity effect.

The frequency-dependent impedances for conductors with respect to resistance and self-inductance is discussed in [52] in the form of a numerical solution and will be expanded on further. The Bessel-Kelvin functions for frequency dependency of resistance and inductance will be taken from [54] and presented graphically with actual measurements. The frequency-dependent resistance of a wire is given by:

$$R = \frac{lR_s}{\sqrt{2}\pi\, r}\left[\frac{Ber(q)Bei'(q) - Bei(q)Ber'(q)}{\left(Ber'(q)\right)^2 + \left(Bei'(q)\right)^2}\right]$$

Where

$$R_s = \sqrt{\frac{\pi f \mu_0}{\sigma_{cu}}}, \qquad q = \sqrt{2\pi f \mu_0 \sigma_{cu}}.r \tag{4.32}$$

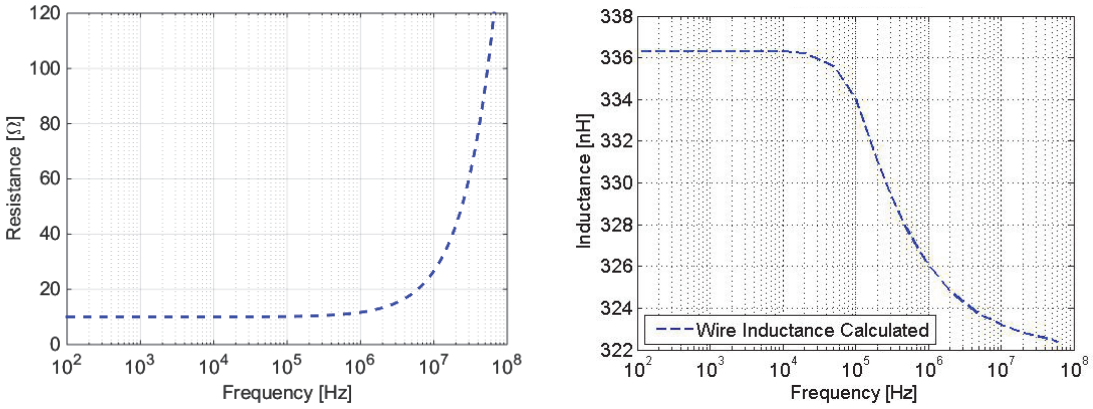
and r is the radius of the conductor, l the length of the conductor and σ_{cu} the conductivity of copper. The permeability of copper μ_0 is the same as for air. In the same manner it can be shown, from [54] that the internal inductance of the conductor with radius, r, and length, l, is equal to:

$$L_i = \frac{lR_s}{2\sqrt{2}\pi^2 f\, r}\left[\frac{Ber(q)Ber'(q)-Bei(q)Bei'(q)}{(Ber'(q))^2+(Bei'(q))^2}\right] \tag{4.33}$$

Both equation (4.32) and (4.33) are in terms of Bessel-Kelvin functions where:

$$Ber(x) + jBei(x) = J_0(j^{-1/2}\, x) \tag{4.34}$$

The self-inductance of a non-magnetic round wire at DC is given in (4-8). The frequency dependency of the total inductance can now be calculated. A 1 mm diameter solid copper wire, 30 cm long has a frequency dependent resistance and inductance due to the proximity effect as shown in Figure 4.30.



(a) (b)

Figure 4.30. (a) Frequency dependent conductor resistance and (b) inductance.

In Figure 4.30 the resistance starts increasing considerably and the inductance of a wire decreases slightly when the skin-effect starts developing at above 10 kHz.

4.2.11 Magnetic loops

A current flowing around a loop generates a magnetic field (H) proportional to the area of the loop. This is particularly of interest in common-mode currents normally forming a

larger loop area than differential-mode currents, thus contributing to the radiated EMC. Figure 4.31 shows a concept of the magnetic loop. The magnetic field equation can be expressed in two different propagation modes, the near-field and the far-field, with boundary distance *s* approximately:

$$s = \frac{\lambda}{2\pi} \tag{4.35}$$

The electrically small magnetic loop, as in our case, is where the loop area A_L is smaller than 0.1λ. The following equations show the approximate magnetic field at an arbitrary point p, a distance s from the current loop with loop surface area, S_L:

$$H_{near} = I * \frac{S_L}{4\pi s^3},\ and\ \ H_{far} = \pi * I * \frac{S_L}{\lambda^2 s}\ \ [A/m] \tag{4.36}$$

The magnetic field H is proportional to the surface area, A_L, and the current, I, Thus, an increase in A_L (or I) will cause an increase in the magnetic field strength at a distance, s.

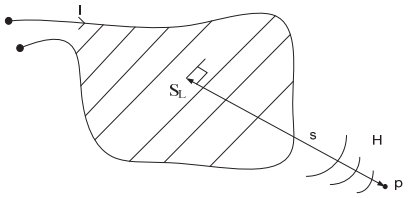


Figure 4.31. The magnetic loop.

4.2.12 Power feed-line model

The conducted emission test setup according to MIL-STD-461F is implemented. The power feed-line from the LISN to the device under test (DUT) as shown in the setup in Figure A.3 is an important component that is very often neglected in EMI analysis and will be modelled in detail. The test bench comprises of a twin power feed-line, spaced evenly 20 mm apart and elevated 50 mm above a solid copper ground plate utilising solid wood spacers. At 30 MHz, a 2 m long power feed-line is equivalent to 1/5 wavelength. At 100 MHz, this becomes 2/3 of a wavelength and an increase of radiation effects occurs. For

practical reasons, this power feed-line is halved to 1 m, to reduce the radiation effects at 100 MHz. The power feed-line parameters are defined in Figure 4.32 (a).

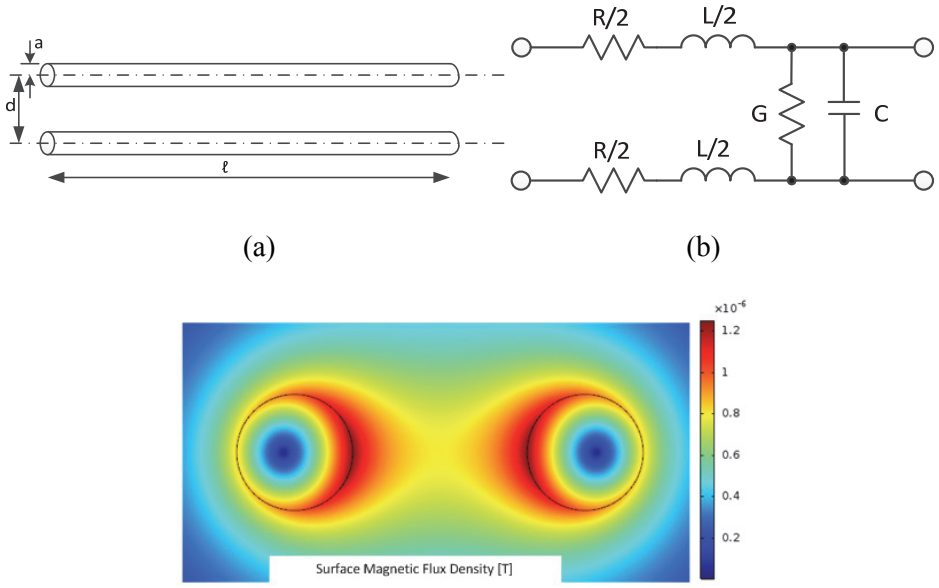


Figure 4.32. (a) Power feed-line physical dimensions, (b) simplified model and (c) magnetic flux density.

A balanced power feed-line model, referred to as the Passive Distribution Network (PDN), is shown in Figure 4.32 (b). It comprises of series surface resistance and inductance as well as shunt capacitance and electrical conductance. It is based on the distributed LC lossless lumped element equivalent circuit of the classical transmission line model [55]. The magnetic flux density model is shown in Figure 4.32 (b), demonstrating the proximity effect of a parallel line. A transmission's line characteristic impedance is represented by the general expression:

$$Z = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \tag{4.37}$$

A power feed-line that is modelled has the following parameters:

Line length, l=1 m, DC resistance with ends shorted is R_S=26 mΩ and the diameter of the copper conductor is d = 1.4 mm, which results in a radius, r = 0.7 mm. The wires are

equally spaced 20 mm apart over the entire length. The skin depth of the conductor is needed to calculate the surface resistance of the wire and is given by.

$$\delta = \sqrt{\frac{2}{2\pi f \cdot \sigma_{cu} \cdot \mu_{cu}}} \tag{4.38}$$

At 1 MHz, the skin depth is 65.8 μm. An expression for the surface resistance R for radius $r > \delta$ is then obtained as:

$$R = \frac{\mu_{cu}}{\pi} \cdot a\cosh\left(\frac{d}{2r}\right) \tag{4.39}$$

With $\mu_{cu} = 4\pi \cdot 10^{-7}$ H/m, $\sigma_{cu} = 5.84 \cdot 10^{7}$, R works out as 0.118 Ω/m at room temperature. An expression for power feed-line inductance L is obtained as:

$$L = \frac{\mu}{\pi} \cdot a\cosh\left(\frac{d}{2r}\right) \tag{4.40}$$

For the given power feed-line parameters, inductance per meter length is obtained as1.34 μH/m. An expression for power feed-line shunt capacitance is obtained as:

$$C = \frac{\pi\varepsilon}{a\cosh\left(\frac{r}{2a}\right)} \tag{4.41}$$

With permittivity of air being close to that of free-space, $\varepsilon = 8.854 \cdot 10^{-12}$ F/m, the capacitance per unit length works out as 8.3 pF/m. The electrical conductance of the power feed-line can be calculated with the following expression:

$$G = \frac{\pi\sigma_{air}}{a\cosh\left(\frac{r}{2a}\right)} \tag{4.42}$$

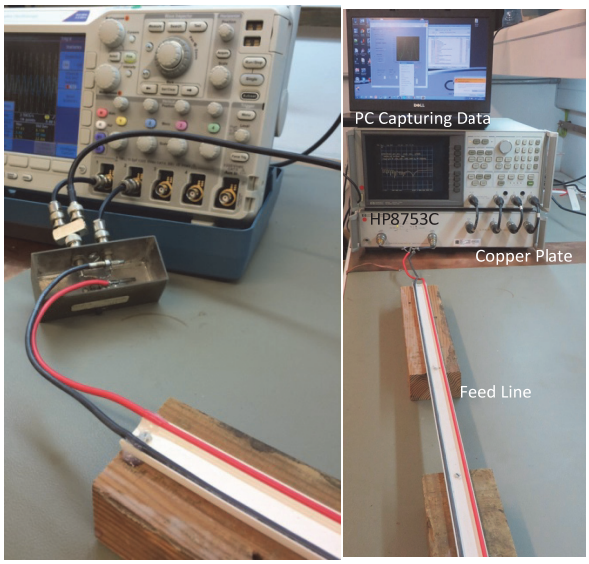
With conductivity of air $\sigma_{air} = 3 \cdot 10^{-15}$ S/m, the electrical conductance per unit length is obtained as $2.8 \cdot 10^{-15}$ S/m. If simplified to a lossless line, the expression for the characteristic impedance reduces to:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{4.43}$$

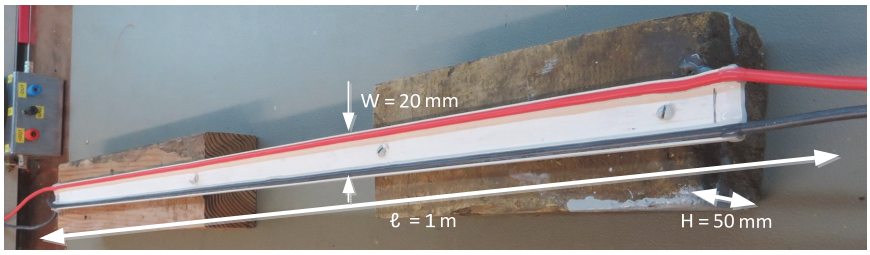
For the given power feed-line parameters, the characteristic impedance works out as Z_0=401.8 Ω.

The power feed-line is measured by using a two-part approach. The lower frequency range is measured using the impedance analyser up to 13 MHz and verified with the oscilloscope-signal generator impedance measurement technique (setup shown in Figure 4.33 (a)). For the high frequency band the power feed-line is verified with a network analyser up to 200 MHz (setup shown in Figure 4.33 (b)). The scattering parameters (S_{21}) are then converted to impedance using (4.9).

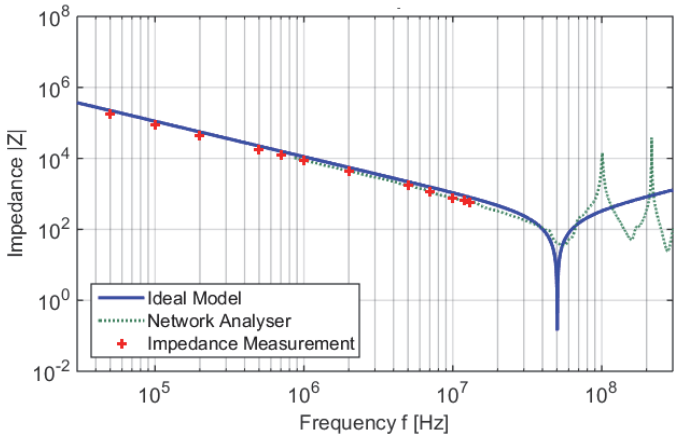
Figure 4.33 (b) shows the impedance characteristic plot of the classical high frequency model compared to measured data. Up to the resonant frequency there is very good agreement between measurements and model. However, beyond that point, the ideal model impedance is inaccurate.



(a) (b)



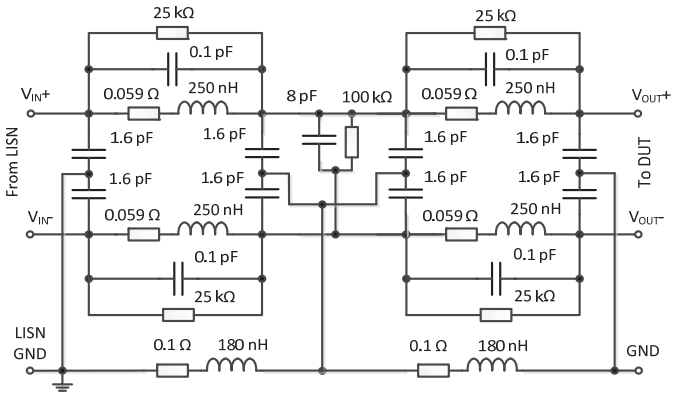
(c)



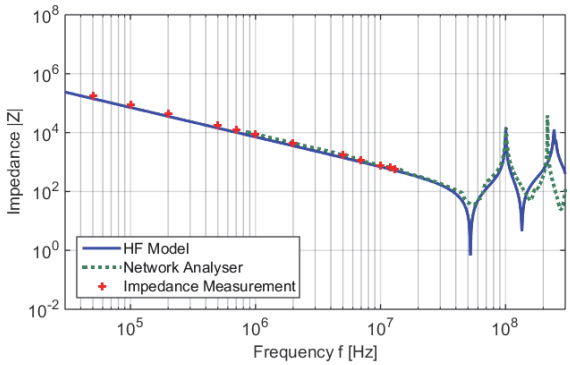
(d)

Figure 4.33. (a) Twin power feed-line (MIL-STD-461 F) scope impedance verification, (b) network analyser measurement, (c) complete line and (d) PDN Impedance.

The new SPICE power feed-line model is created in Spectrum Software as shown in Figure 4.34 (a). A two-cell distributed network is chosen. The model is constructed using the improved inductor model that is derived. The added capacitors connected to ground, simulate the power feed-line that is suspended 50 mm above a solid ground plane. Figure 4.34 (b) shows a comparison between the impedance characteristic of the new high frequency model with the measured impedance results. There is very good correspondence between the two thus verifying model accuracy [37].



(a)



(b)

Figure 4.34. (a) The power feed-line model and (b) new model impedance compared.

Due to the high frequency conducted emission measurements performed on a specific line length, some radiation losses are expected. Figure 4.35 shows s11 return transmission loss for three types of power feed configurations, having an influence on the differential-mode measurement. For the parallel line, about 0.5 dB return transmission loss at 60 MHz. Implementing a LMR400 coaxial power transmission line shows almost zero radiating loss

for the same length of power feed-line. The twisted pair line shows a larger return loss, due to the tight winding and larger inter-capacitance.

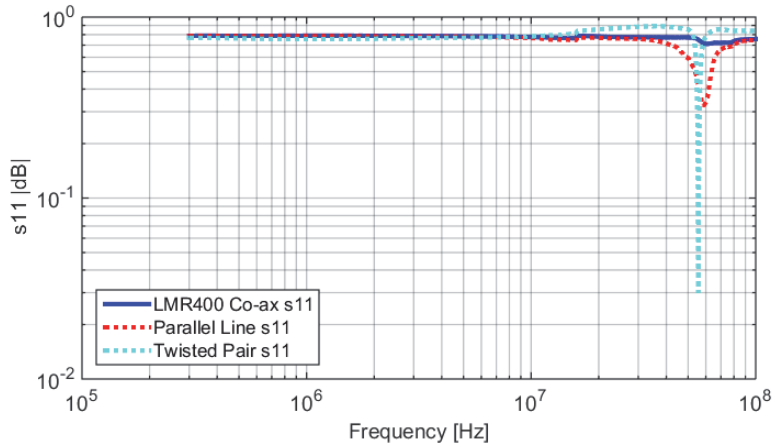


Figure 4.35. Parallel-line s11 transmission parameters compared to coaxial LMR400 power line and twisted pair.

The common-mode loop s11 transmission parameters are much more complex due to the large ground plate area as well as larger loop area, and are shown in Figure 4.36. Similar transmission loss valleys as in the differential line are noticed between 40 MHz and 60 MHz. The wider frequency band is due to the larger plate area.

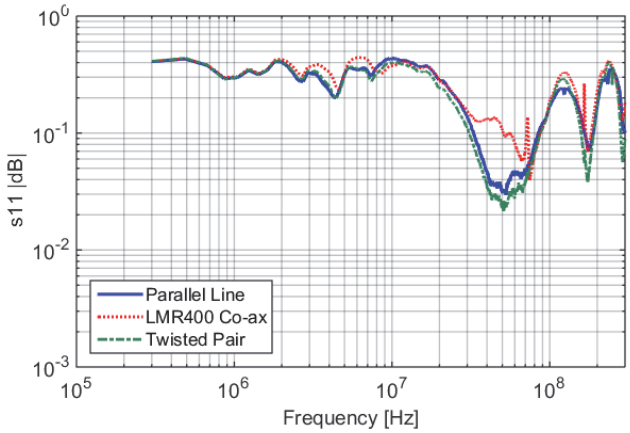
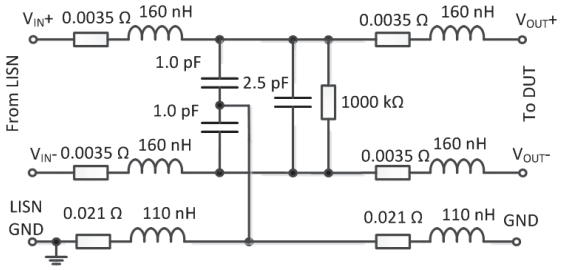


Figure 4.36. Power line-to-ground s11 transmission parameters compared to coaxial LMR400 power line and twisted pair.

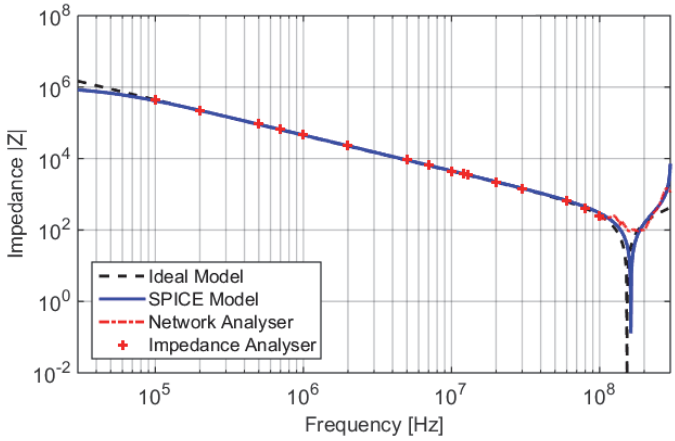
Replacing the parallel line with a coaxial feed-line will further improve the high frequency measurement accuracy, causing less radiation losses for the differential-mode measurement and to a lesser extend for the common-mode loop. Thus, for accurate high-frequency

common-mode measurements, modelling the power line from the LISN to the DUT is of utmost importance.

To completely eliminate resonant effects from the feed-line, up to 100 MHz, the optimal length is derived to be 0.3 m. In the products of concern, for example handheld power management equipment running from a mobile battery source, a shorter line is impractical, but the results provided to note the high frequency effects. Running through the same design procedure as the 1.2 m power feed-line, the simpler equivalent circuit is provided in Figure 4.37 (a), and the shorter 0.3 m power feed-line impedance in Figure 4.37 (b), showing the first resonance effect outside the 100 MHz band.



(a)



(b)

Figure 4.37. (a) Lumped element model 0.3 m power cable and (b) impedance characteristics.

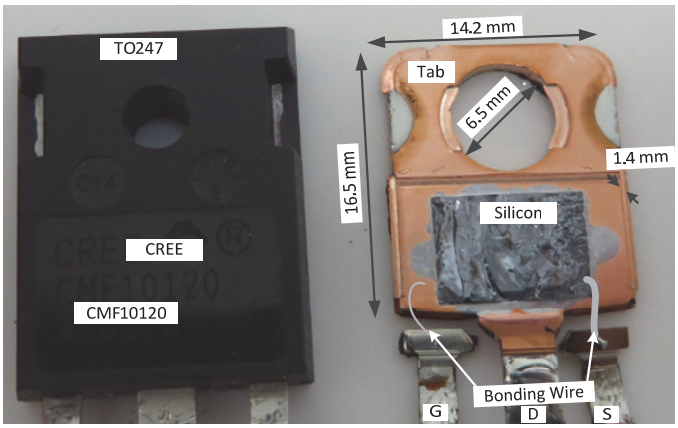
4.2.13 Active devices

In a basic DC-DC converter, the active devices are the switching transistor, either a MOSFET or IGBT, and the power diode.

4.2.13.1 MOSFET high frequency model

The high-frequency MOSFET model will be discussed in this section to understand the high frequency effects when switching at high dV/dt and dI/dt. The SMD-packages such as the DPAK and the larger D2PAK has source inductances between 1.5 nH and 7 nH with at least an added extra PCB trace inductance of 5 nH to 10 nH. Reference [56] states that the non-linear effects of the drain current rise and fall times is directly related to the package and trace parasitic inductances.

High density packaged converters are at a point where utmost care should be taken to reduce this parasitic inductance to improve the converter performance. Some low-inductance packages have been out in the marketplace, such as the BGA (Ball Grid Array) technology and the DirectFET claiming very little source inductance [57]. Figure 4.38 (a) shows the typical TO-247 MOSFET package and in (b) the skeleton view show the bonding wires attached to the silicon substrate as well as the leads, creating the parasitic inductance effects. The FlipFET (Courtesy of IR) is the modern usage for high density MOSFETS with very low parasitic inductances with the ball grid array soldering directly on the PCB, without any leads.



(a) (b)

Figure 4.38. Physical MOSFET: (a) The TO247 package CMF10120 and (b) the MOSFET skeleton with drawn-in bonding wires**.**

Combining a lumped element high frequency MOSFET model showing all the critical parameters and parasitic elements can now be drawn with the help of reference [50], [58],. The diagram is shown in Figure 4.39.

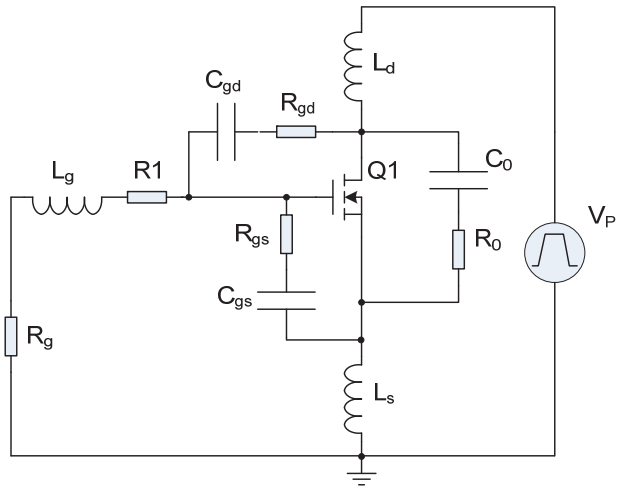


Figure 4.39. MOSFET high frequency model.

Most of the values as defined in Figure 4.39 can be found in the applicable datasheet. Values L_S and L_d can be calculated and are a function of the silicon substrate bonding wires and track parameters of the PCB. The Input Transfer Capacitance (Ciss) Output Transfer Capacitance (Coss) and Reverse Transfer Capacitance (Crss) given in the datasheet, can be calculated using the following equations:

$$C_{iss} = C_{gs} + C_{gd} \quad (C_{ds} = shorted)$$

$$C_{oss} = C_{ds} + C_{gd}$$

$$C_{rss} = C_{gd} \tag{4.44}$$

The gate-to-drain capacitance, C_{gd}, is a non-linear function of voltage and provides a feedback loop between the drain and the gate of the MOSFET. It is also called the Miller capacitance [59] and causes the switching capacitance to become greater than the sum of the static capacitances. C_{gd} can be modelled as a step value with a peak-hold function, creating multiple spectral plots. The increased input capacitance due to the Miller effect is given by:

$$C_M = C_{gd} = C(1 + A_v) \tag{4.45}$$

where A_v is the gain of the amplifier and C is the feedback capacitance.

Another aspect of noise path modelling is the capacitive coupling from the switching element to the heatsink, normally connected to ground, and responsible for the common-mode noise.

4.2.13.2 IGBT High frequency model

The IGBT high frequency model will be presented in order to predict and eventually reduce the EMI due to the IGBT high frequency characteristics. Reference [60] characterised the high frequency behaviour and validated it with experimental results. A simpler behavioural model is presented in [78]. The IGBT model accounting for the high frequency behaviour is given in Figure 4.40, a slightly modified version as from [60], adding emitter inductance and resistance.

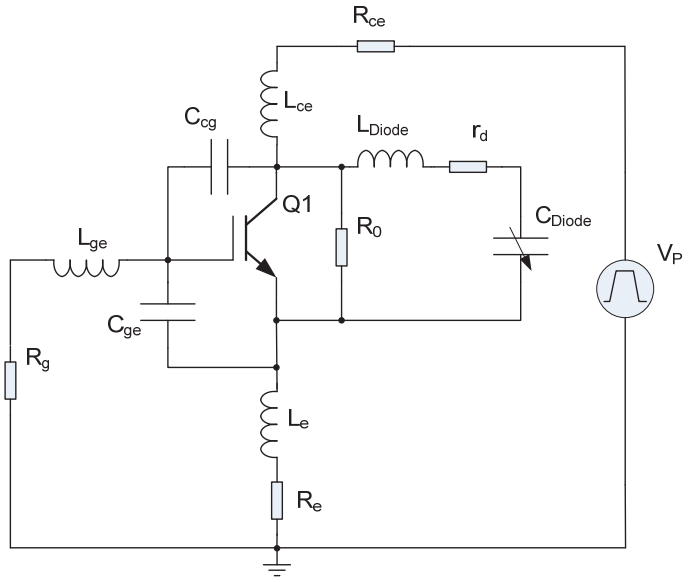
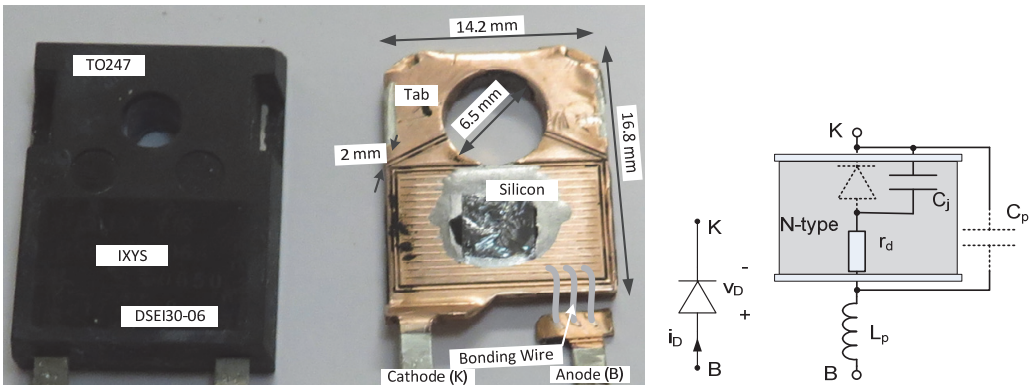


Figure 4.40. High frequency IGBT model.

4.2.13.3 Power Diode High Frequency Model

Figure 4.41 (a) shows the DSEI30-06 TO247 packaged diode that will be used frequently in EMC modelling analysis. Figure 4.41 (b) shows the skeleton view, depicting the copper tab, and the 3 parallel bonding wires. The diode equivalent circuit is presented in Figure 4.41 (c). It consists of a series resistor r_d and a charge, Q_D.



(a) (b) (c)

Figure 4.41. Physical diode (a) showing TO247 package DSEI30-06, (b) the diode skeleton with drawn-in bonding wires and (c) diode equivalent circuit**.**

C_j represents the diode depletion region capacitance and C_P is the device contact leads and pads capacitance. L_p is the inductance associated with the device package.

An expression for the diode impedance can be found with the following technique:

$$Y_{d1} = 1/r_d + j\omega C_j \tag{4.46}$$

$$Z_{d2} = Z_{d1} + r_s \tag{4.47}$$

$$Y_{d3} = Y_{d2} + j\omega C_p \tag{4.48}$$

$$Z_D = Z_{d3} + j\omega L_p \tag{4.49}$$

Manipulating (4.49) with (4.48), (4.47) and (4.46) and noting $Y = 1/Z$ gives an expression for the diode impedance:

$$Z_D = \frac{1}{\dfrac{1}{\dfrac{1}{1/r_D + j\omega C_j} + R_S} + j\omega C_P} + j\omega L_P \tag{4.50}$$

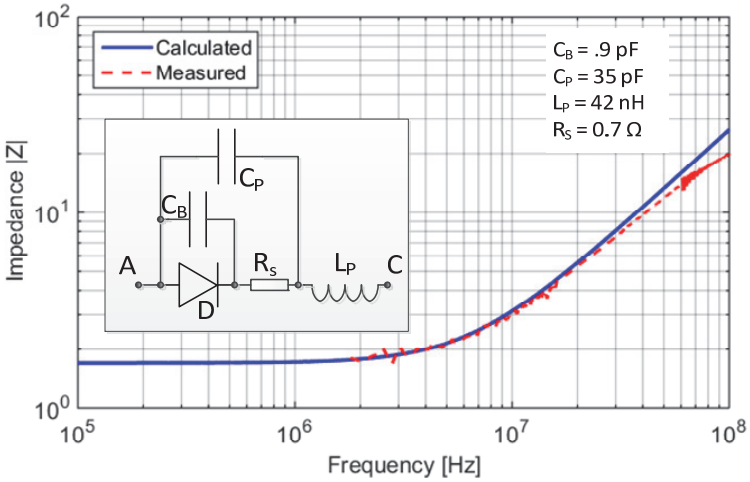


Figure 4.42. Diode DSEI30 impedance.

4.2.14 Aluminium and polymer heatsink

It is beneficial to be able to model the EMC issues concurrently with the power processor hardware as well as the thermal management design phase [61]. The parasitic couplings

between the semiconductor power devices and the heatsink are largely responsible for common-mode currents [62]. Due to the normally large physical size of the heatsink, it has a huge effect on the transmission of unwanted noise [63]. For thermal management, power semiconductor devices are in general mounted on aluminium heatsinks, but polymer (plastic) composite heatsinks are becoming popular in low-power applications.

A heat conducting plastic is a polymer composite material in which for increased heat conductivity, a high-heat conductivity filler is added [64]. The thermal conductivity of these polymers can be improved considerably by adding highly conductive fillers such as graphite, carbon fibres, ceramic, or metal particles [65], [66]. Desirable properties can be obtained that would not be achievable through the use of a single material. Thermally conductive compounds are generally not considered to be direct drop-in replacements for metals. However, they do offer a broad range of new opportunities for thermal management applications [67]. Recent improvements in the thermal conductivity of polymer composite materials have seen a thermal conductivity in the range of 20W/mK [68]. In addition to the manufacturing advantages offered by such mouldable composites, their relatively low density (around 1000 kg/m^3 opposed to 2700 kg/m^3 for aluminium) and lower coefficient of thermal expansion (7 ppm/K) can provide a significant weight reduction and improve the reliability of the converter enclosure [68], [69]. Some applications require exclusive use of polymers because of their unique physical properties: flexibility, low cost, lightweight, corrosion resistance, and ease of manufacturing [64], [70]. In most applications metals are the more appropriate materials in many applications. Where weight and expansion coefficients are a factor, they are less suitable [71]. By using polymer heatsinks, cooling rates as high as 200 W appear to be achievable [68]. Thermally conductive polymers can be broadly grouped as either electrically conductive or insulative types, with the former being used in shielding applications [66], [72].

Two examples where polymer heatsinks are used in commercial quantities are in mobile phones and motor vehicles. Designers at Apple Computer realised that they needed a heat spreader to dissipate heat from the video processor in the PowerBook computer. Due to limited space, the design of the heat spreader was only possible because the thermally conductive plastic was injection mouldable. To make a metal or ceramic part to fit into the

available space as well as meet all component clearance requirements proved impossible [72]. In the newer generation of motor vehicles polymer heatsinks in LED headlights are responsible for a 25 % reduction in headlight weight [73], contributing to the overall efficiency of the vehicle.

The heatsink capacitance and heat characteristics are numerically modelled with COMSOL Multiphysics, a finite-element analysis simulation package. The effects on common-mode noise due to grounding [62], are investigated in respect of the enclosure as well as the device fastening interactions, be it a threaded fastener (metal or nylon) or a spring clamp. The relevant conducted EMC results from this model, such as parasitic capacitances, are fed into an EMC circuit model. The application for polymer compound heatsinks is mostly in lower power applications. However, for higher power applications, SiC devices can be considered as these power semiconductor devices consist of very high junction temperature specifications [44], [69]. They have to be used with care, as too high operating temperatures can cause thermal runaway or lead to gate oxide degradation [74], [75].

The ground theory publication on the heatsink analysis is presented in [76].

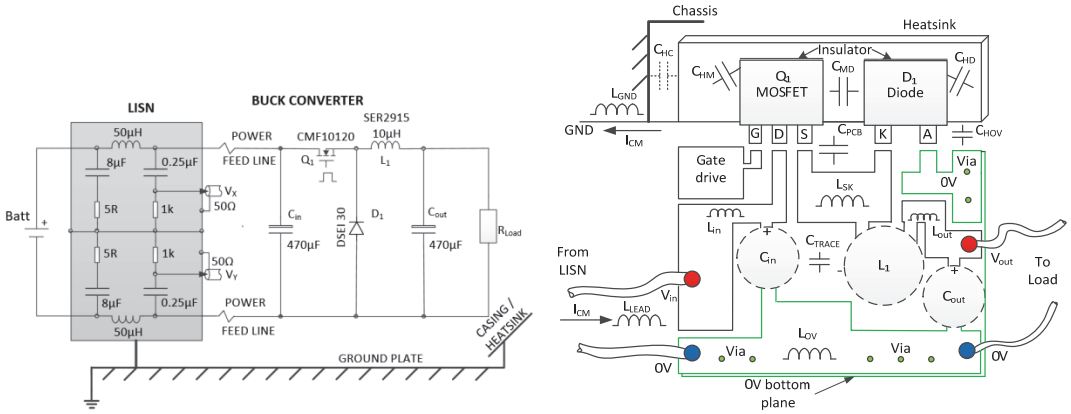
4.2.14.1 Heatsink EMC analysis – simplified model

Simplified circuit models for conducted EMC are found in the literature [42], [38] and are generally accurate enough to predict conducted noise slopes and to show general trends with accuracy within a few dB's. Although not accurate enough for certain aspects of noise modelling, particularly at high frequencies, they should be sufficient for the purpose of establishing a base line model and verifying the heatsink conducted noise effects. These effects will be demonstrated with a test circuit and simplified conducted EMC modelling, but can be extended to other converter topologies. The test circuit comprises of a step-down DC-DC converter with a heatsink, power feed-line and a LISN as shown in Figure 4.43 (a). This circuit example can be extended to other converter topologies. Two power devices are attached to the heatsink; the MOSFET and the diode. Figure 4.43 (b) shows the physical circuit layout of the sample circuit, defining the stray capacitances and the parasitic inductances. A 12 V sealed lead-acid battery suspended on a wooden block, so as

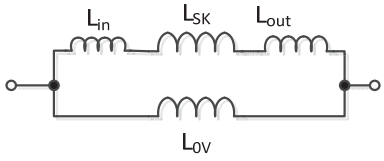
not to influence the noise path, supplies the auxiliary power for the test circuit that comprises of the MOSFET drivers and PWM controllers.

With reference to the physical layout as in Figure 4.43 (b), the converter track inductance, $L_{CIRCUIT}$, with model given in Figure 4.43 (c), is defined as the series track inductances between input and MOSFET drain (L_{IN} = 40 nH), the track between MOSFET source and L_1 (L_{SK} = 20 nH), between L_1 and R_{LOAD} (L_{OUT} = 130 nH), paralleled with the negative PCB return plane from R_{LOAD} to negative input (L_{OV} = 100 nH). This provides a measured value of 65 nH. The step-down converter circuit model consists of the capacitance from the PCB tracks to ground-plane C_{PCB} and the combined device tab capacitance to the ground-plane C_H. These models show that the DM noise is not influenced by the heatsink capacitance C_H, which however influences the CM noise signal. Consequently, to be able to accurately determine the CM noise, the total heatsink capacitance, C_H, defined as the capacitance from the device tab-pin (as close as possible to the body), through the heatsink to the ground plane, should be correctly determined.

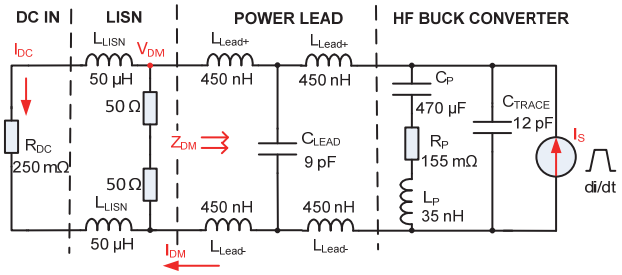
Figure 4.43 (d) and (e) shows the simplified DM and CM models respectively for the test step-down DC-DC converter [77]. They are used to discuss and analyse the conducted noise mechanisms due to the heatsink capacitance. The heatsink capacitance, C_H, is defined as the combined capacitance from the power converter devices and traces, through the heatsink to a ground connection point, creating the common-mode noise path to ground. The DM model consists of the LISN with two 50 Ω resistors in series representing the LISN impedance, the power feed-line parameters L_{LEAD} and C_{LEAD}, based on the transmission line theory, and the step-down DC-DC converter parameters, C_P, R_P and L_P representing the converter capacitor equivalent impedance. The current source, I_S, represents the trapezoidal switching waveform. Similarly, the CM model shows the LISN noise impedance as two parallel 50 Ω resistors, the power feed-line to the step-down converter represented by $L_{LEAD}/2$, C_{LEAD_G} the capacitance of the power feed-line to the ground plane as well as the ground-plane return inductance L_{GND}. The power feed-line and ground plane parameters were deducted from a series of open- and short-circuited impedance measurements.



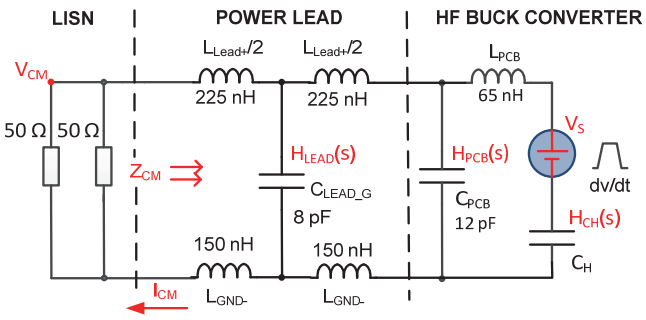
(a) (b)



(c)



(d)



(e)

Figure 4.43. (a) Step-down converter test circuit, (b) physical layout of the converter, (c) PCB inductance model and (d) DM- and (e) CM simplified models.

Referring to the equivalent DM and CM circuits in Figure 4.43 (c) and (d), the transfer-function H_{DM} of the simplified DM circuit is the ratio between the noise source I_S and the differential-mode current I_{DM}, obtained as:

$$H_{DM}(S) = \frac{I_{DM}(S)}{I_S(S)} \tag{4.51}$$

Similarly, the transfer-function for the CM circuit is given as:

$$H_{CM}(S) = \frac{V_{CM}(S)}{V_S(S)} \tag{4.52}$$

The expression for the one-sided Fourier transform of the DM LISN voltage can now be obtained as:

$$\left|V_{DM}(j\omega)\right| = \sum_{n=1}^{\infty} 2 \cdot \left|C_{nDM}\right| \cdot \delta(\omega - \omega_n) \tag{4.53}$$

The complex Fourier expression is represented by C_n, δ is the unit impulse function (Dirac-delta function) and $\omega_n = n.\omega_0$ where ω_0 is the angular switching frequency in rad/s. The coefficients C_n are computed as follows:

$$\left|C_{nDM}\right| = \frac{1}{T \cdot \sqrt{2}} \left|I_S(j\omega_n) \cdot H_{DM}(j\omega_n)\right| \tag{4.54}$$

$H_{DM}(j\omega N)$ represents the transfer-function obtained as the ratio of the equivalent current source, $I_s(s)$, to the LISN current. Similarly, an expression for the CM signals can be written as

$$\left|V_{CM}(j\omega) = \sum_{n=1}^{\infty} 2 \cdot \left|C_{nCM}\right| \cdot \delta(\omega - \omega_n)\right| \tag{4.55}$$

With:

$$\left|C_{nCM}\right| = \frac{1}{T \cdot \sqrt{2}} \left|I_S(j\omega_n) \cdot H_{CM}(j\omega_n)\right| \tag{4.56}$$

The coefficients derived in (4.54) and (4.56) are for a trapezoidal waveform. For special cases where the rise-time, t_r, and the fall-time, t_f, are equal, the expression for the trapezoidal waveform can be simplified as follows:

$$I_S(j\omega) = A\frac{\tau}{T}.\frac{Sin(n\omega_0\tau/2)}{n\omega_0\tau/2}.\frac{Sin(n\omega_0\tau_r/2)}{n\omega_0\tau_r/2}.e^{-jn\omega_0(\tau+t_r)/2} \quad (4.57)$$

Figure 4.44 (a) and (b) shows the voltage amplitudes across C_H and the CM LISN resistor respectively. The differential- and common-mode impedance is calculated and plotted for two values of C_H as shown in Figure 4.44 (c). The differential-mode impedance is seen not influenced by the heatsink capacitance. On the other hand, there is a noticeable difference in the common-mode impedance when C_H value changes from 80 pF to 20 pF. The benefit of the lower capacitance on EMC decreases at frequencies beyond 30 MHz due to other impedance branches in the circuit becoming more prominent. The common mode transfer functions defined in Figure 4.43 (d) are presented in Figure 4.44 (d). $H_{CH}(s)$ is defined as the ratio between heatsink capacitance voltage $V(C_H)$ and common mode voltage V_{CM}, $H_{PCB}(s)$ the ratio between the PCB capacitance voltage $V(C_{PCB})$ and V_{CM} and $H_{LEAD}(s)$ the ratio between the power lead capacitance voltage $V(C_{Lead})$ and V_{CM}. It shows the relevant influence these branches will have on the common mode voltage. The heatsink transfer-function is dominant in the lower frequency band, below 20 MHz. Beyond 20 MHz, the capacitance C_{PCB} becomes more prominent and at around 90 MHz, the power lead capacitance C_{LEAD} dominates. The common- and differential-mode spectrum noise plots are obtained from the models and presented in Figure 4.44 (e) and (f) respectively, against the MIL-STD-461F limit as a reference. The switching signal was modelled with a period of 10 µs (100 kHz switching frequency) and a duty cycle of 50 %. The rise- and fall-times are set to 100 ns.

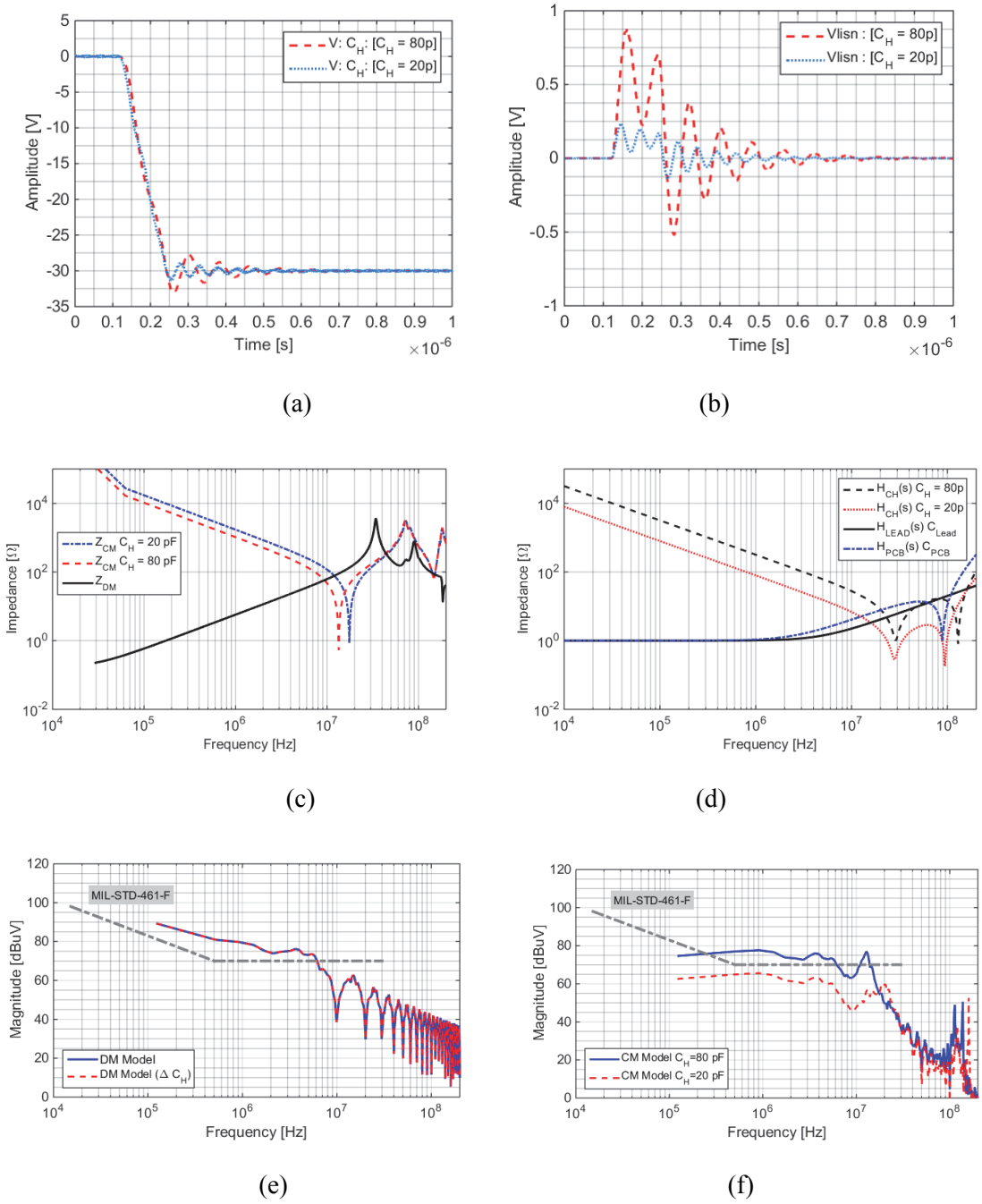


Figure 4.44. (a) Voltage over heatsink capacitance for C_H = 80pF and 20 pF, (b) CM voltage at LISN for C_H = 80pF and 20 pF, (c) DM and CM impedance for two different heatsink capacitances, (d) CM transfer-function, (e) DM spectral plot up to 200 MHz and (f) CM spectral plot for C_H = 80pF and 20 pF.

The effect of the inductance, L_{PCB} and L_{GND} on the heatsink impedance can also be determined. With lower ground- and circuit inductances, the impedance resonance moves to higher frequencies, as expected and shown in Figure 4.45.

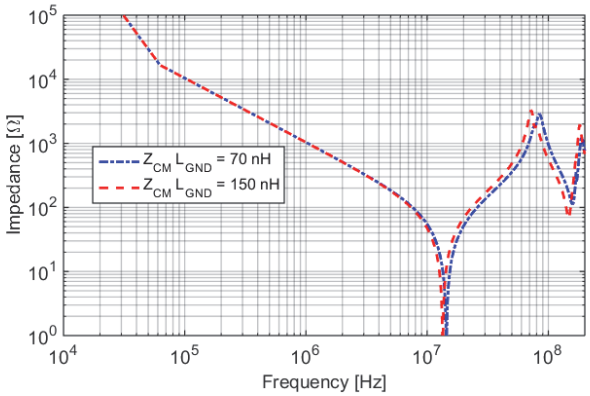
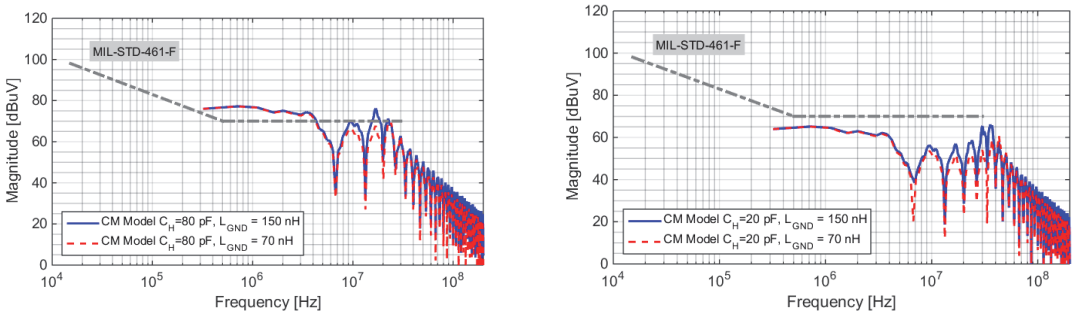


Figure 4.45. Heatsink impedance effect when inductance L_{GND} is varied.

The inductance effect L_{GND} on the common-mode noise is shown in Figure 4.46. For the proposed aluminium heatsink with C_H = 80 pF, lowering the inductance lowers the high frequency common-mode noise. Similarly with the proposed polymer heatsink, lower high frequency common-mode noise can be expected. Decreasing the heatsink capacitance lowers the lower frequency common mode noise and lowering the common mode inductance (L_{PCB} as well as L_{GND}) lowers the higher frequency common mode noise.



(a) (b)

Figure 4.46. Effect on CM noise for two values of L_{GND} (a) with C_H = 80 pF, and (b) C_H = 20 pF.

4.2.14.2 Heatsink model

The device tab capacitance-to-ground plays a very important role in both the generation and propagation of the common-mode noise. It can be estimated using the parallel-plate capacitance expression C_{Plate}, as given in (4.58)

$$C_{Plate} = \frac{\varepsilon_0 \varepsilon_r A}{d}, \tag{4.58}$$

where A is the area of the MOSFET tab and d the SILPAD insulator thickness taken as 0.152 mm, ε_0 is the permittivity of air and ε_r the permittivity of the heatsink insulator taken as 2.9 F/m. If the standard sized TO-247 metal tab (14 mm x 16 mm) data are substituted into (4.58) the capacitance C_{Plate} works out as 38.3 pF. Figure 4.47 (a) shows the physical component layout on an aluminium heatsink and Figure 4.47 (b) shows the heatsink capacitance model. The diode switching voltage is V_D and the MOSFET switching voltage V_M.

The MOSFET and diode are mounted onto the heatsink with stainless steel cheese-head threaded fasteners with a silicone insulating pad in between the devices and the heatsink as in Figure 4.47 (a). From Figure 4.47 (b), the capacitance between the MOSFET and diode is C_{MD}, from the MOSFET tab to the heatsink, capacitance is C_{HM}, and between the diode tab and heatsink it is C_{HD}. C_{H0} is the capacitance to the zero-volt plane of the PCB and C_{HC} indicates the heatsink-to-chassis capacitance. The diode switching voltage is V_D and the MOSFET switching voltage V_M. C_{HM}, and C_{HD} are the dominant capacitances coupling common-mode noise to the chassis and are considered the main common-mode noise path. There are other additional capacitances such as the PCB trace capacitances C_{HPCB} coupling to the heatsink. In this case, the heatsink is connected to the chassis, so $Z(C_{HC}) = 0$. If the heatsink is to be connected to the zero-volt line V_{0V}, C_{H0V} would have zero impedance. In this case, the heatsink capacitance to the 0 V ground plane, C_{H0} measures 0.9 pF. The capacitance C_H is all the capacitances coupled directly to the heatsink with C_{HC} short circuited and followed by L_{GND} to the earth point, and is expressed in (4.59)

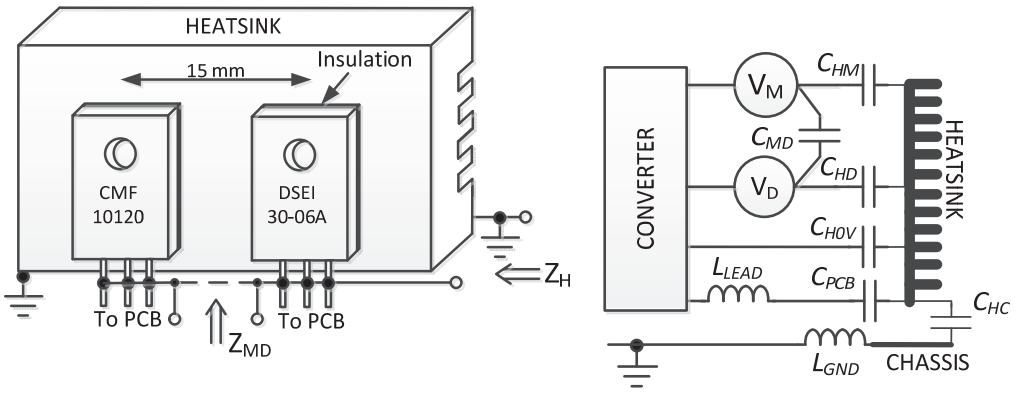
$$C_H = (C_{HM} + C_{HD}) + C_{H0V} + C_{HPCB} + \delta_{CMD}$$

where δ_{CMD} the small capacitance contribution due to the capacitance between the switching devices on the heatsink. Considering the noise path from V_D through C_{MD} to the heatsink as well as the noise path from V_M through C_{MD} to the heatsink, δ_{CMD} can be expressed as:

$$\delta_{CMD} = 2 \cdot C_{MD} \quad , \quad C_{MD} << C_{HD}, C_{HM} \tag{4.59}$$

The heatsink impedance is now expressed as:

$$Z_H = j\left(\omega\left(L_{PCB} + L_{GND}\right) - \frac{1}{\omega \cdot C_H} \right) \tag{4.60}$$



(a) (b)

Figure 4.47. Devices and heatsink models: (a) physical component layout on an aluminium heatsink, and (b) heatsink capacitance model.

The heatsink and its behaviour will be modelled with a finite element analysis tool COMSOL. FEA is a numerical method for solving partial differential equations, well suited for electromagnetic and heat transfer modelling. A COMSOL model was developed and simulations carried out to validate (4.58) as well as determining a more accurate value of heatsink capacitance. A TO-247 package is modelled on an aluminium block 0.5 cm high, 3 cm wide and 3 cm deep, shown in Figure 4.48. The metal enclosure around the model is a variable, incremented in steps from an initial size of 5 cm wide, 5 cm deep and an inside height of 2.5 cm, to final 13 cm wide, 13 cm deep and 6.5 cm high. This is done in order to model the enclosure proximity effects on the devices to the heatsink capacitance. The same enclosure is modelled in two modes: when the casing is at a floating potential and also when the casing is connected to earth. The polymer material is chosen from the library, with relative permeability $\varepsilon_r = 4$ and density of 1150 kg/m^3.

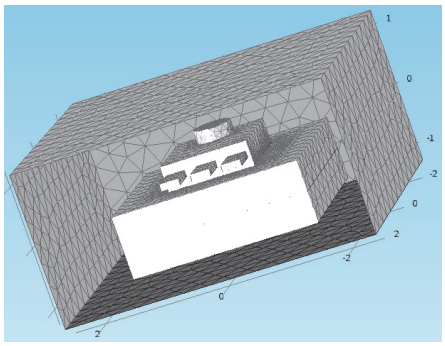


Figure 4.48. COMSOL heatsink model.

The COMSOL model graphical results showing the normalised electrical field plot in Figure 4.49 (a), illustrates the influence of the threaded fastener, with capacitor fringing fields visible in the electric field plot. Figure 4.49 (b) and (c) display the model setup showing the electric potential for aluminium and polymer heatsinks respectively at 100 V. These models are less detailed and are used to analyse different materials and compounds for comparison purposes in heatsink applications.

Figure 4.49 (d) and (e) show the capacitance plots for aluminium and polymer heatsinks respectively. In both cases they illustrate the slight differences in capacitance due to the two enclosure modes. When the enclosure is grounded, the capacitance starts off slightly higher compared to the case where the enclosure is floating. As the enclosure around the device increases in size, the heatsink capacitance converges to an average of 39.4 pF for the aluminium heatsink. This is higher than the calculated plate capacitance, C_{Plate}, of 38.3 pF. The increase is predominantly due to the fringing effects as well as the threaded fastener effects, and demonstrates the importance of including other effects on devices to ground capacitance. Moreover, it is seen that device-to-ground capacitance is also influenced by the size of the enclosure. By replacing the stainless steel threaded mounting fasteners with nylon ones, the capacitance decreases by 1.2 pF. On the other hand, securing the devices with a spring loaded metal clamp instead of stainless steel cheese-head threaded fasteners lowered the capacitance by another 0.7 pF. A further, even greater, reduction in device-heatsink-ground capacitance is achieved by introducing polymer composite material. From Figure 4.49 (e), it is seen that this causes capacitance on average to decrease from 39.4 pF to 3.8 pF for a single device.

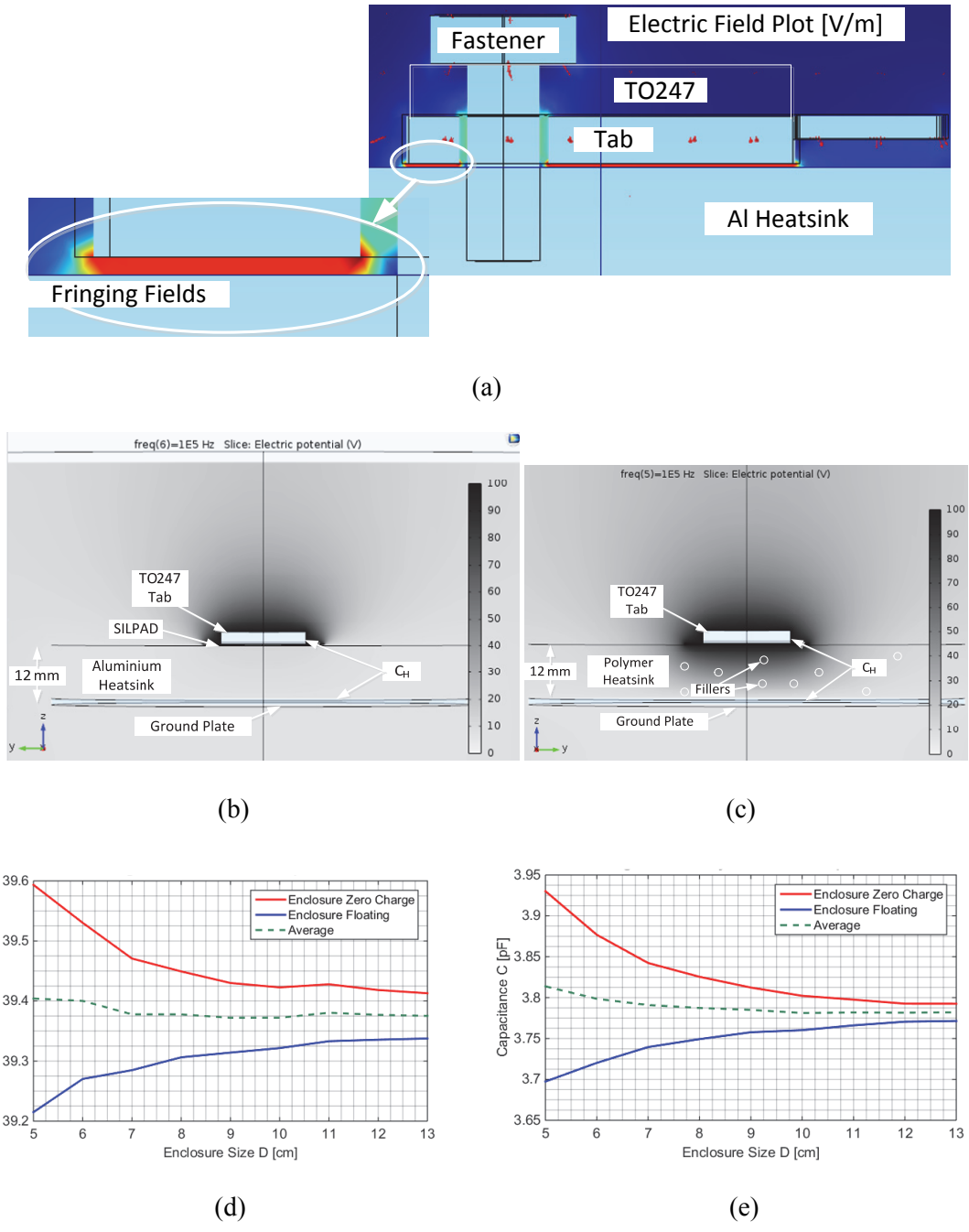
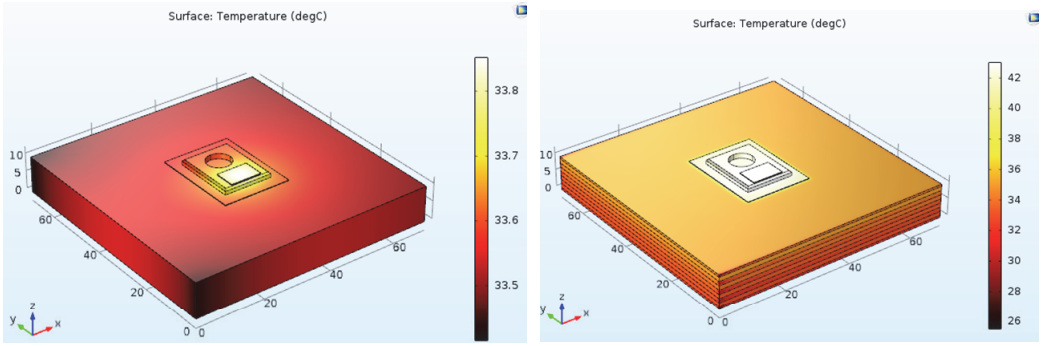


Figure 4.49. (a) Normalised modelled electric field plot, (b) aluminium and (c) polymer device capacitance model, (c) the aluminium heatsink capacitance and (e) the plain polymer heatsink capacitance.

The heat capacity of a polymer without any heat conducting fillers is very low. A filler material therefore needs to be added to increase the heat capacity. This also has the effect of increasing the capacitance. Fillers can be included in various ways, in sandwiched composite, particle composite or even fibre composite. Modelling the polymer compound

as 60 % Cu sandwich layers, increased the overall heatsink capacitance to chassis with roughly 60%, up to 6.1 pF. Figure 4.50 (a) shows the temperature distribution in an aluminium heatsink test block, 70 mm x 70 mm x 10 mm, and a TO247 device dissipating 1 W, corresponding to an output power of 50 W if switching losses are 2 %. The room temperature was set to 294 K. A SILPAD insulator of 0.15 mm separates the TO247 device from the heatsink, and has a thermal resistance of 1.3 K/W. The temperature on the die increased to 307.5 K. Replacing the aluminium heatsink with a polymer without fillers, the die temperature rose to an incredible 413 K. Adding only 25 % copper filler, reduces the die temperature to 335.4 K. With 60 % copper filler the modelled die temperature reduces even further to 316.5 K shown in Figure 4.50 (b).



(a) (b)

Figure 4.50. Temperature distribution: (a) in aluminium and (b) in Polymer with 60 % Cu filler.

The above values are determined through modelling and will be compared with measurements in a later section.

4.3 COMPONENT PROXIMITY

Component proximity effects are defined as the effect components will have on each other, thus influencing their behaviour in terms of operational processes when participating in the power conversion processes as well as its noise characteristics due to being in close proximity to each other. The influence is mostly inductive, but can be capacitive as well.

4.3.1 Enclosure effects

Power converters can achieve very high switching frequencies, in some cases within the MHz range, with the introduction of Silicon Carbide and Gallium Nitride devices. The Electromagnetic Compatibility (EMC) therefore becomes more difficult to design for, due to the more complex noise propagation coupling effects of these higher switching frequencies. Enclosure effects, Printed Circuit Board (PCB) coupling and component proximity effects start playing a vital role. For not only adding to the increase in noise levels that are of concern, but also the interference may cause erratic circuit behaviour or even failure.

The common-mode loop as found on an EMI test bench is shown in Figure 4.51. The common-mode current typically forms the larger loop-area contributing to the radiated EMC. Equation (4-36) is used to calculate the approximate magnetic field at an arbitrary point p, a distance d from the current loop with surface area, A_L. Figure 4.51 shows the larger common mode loop area, prone for radiated effects due to its larger surface area A_L.

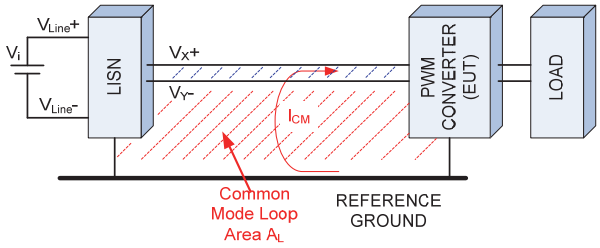


Figure 4.51. Common-mode radiation loop.

The typical limit for radiated emissions at a 10 m distance is about 37 dBµV/m. If the power feed-line is about 1 m in length, the loop area can easily be resonant at a half wavelength, thus close to 30 MHz. In general, a loop current of only 5 µA at 30 MHz will cause the unit to fail the radiated limit at 10 m distance. The same order of current will cause a failure of the conducted limits.

Capacitive coupling between components and traces can be obstructed by effective shielding. Inductive coupling or magnetic field coupling is however more complex. In any

power circuit, current loops are inevitable, causing coupling to other loops and components. The following factors summarise the coupling effects:

- A larger loop-area perpendicular to the flux will increase the induced voltage,
- A higher current frequency will increase the induced voltage,
- A higher current amplitude will increase the induced voltage.

The skin-depth is an important parameter of the wall thickness of the enclosure. For the majority of the noise frequencies of concern, the enclosure wall should be thicker than a skin-depth. The wall skin-depth is calculated using the well-known expression in (4.38). At a frequency of 100 kHz, the skin-depth for a metal enclosure is calculated to be less than 0.2 mm. Thus for an enclosure wall thicker than 0.2 mm, the noise current will flow on the outer surface of the wall and the magnetic-field will not be able to penetrate the wall.

Positioning sensitive components such as open wound inductors used in filter circuits and power converters to specific areas in an enclosure can reduce outside loop coupling effects due to power feed and load cables, common-mode loops and multiple converters in close proximity. The EM software package FEKO is used to investigate the effect of enclosing components. Simulations were performed to establish optimal component placement for a handheld power converter with a 1 m power feed-line operating in the vicinity of an HF transmitter. Simultaneously, the common-mode effect of a noisy power feed-line on the handheld converter and how to minimize the common-mode noise due to the power feed-line is also investigated.

The enclosure is typically a box-type design with non-conductive openings at the top, housing the display and interface buttons. In an ideal case, with a completely sealed conductive enclosure, no current will flow on the inside of the box due to outside magnetic noise and vice-versa.

The FEKO simulations are performed by the Method of Moments (MoM), a solution of Maxwell's integral equations in the frequency domain. The model is set up with a linear plane wave excitation, single incident wave at 30 MHz and amplitude of 1 mV/m,

converting to 60 dBμV/m. This value is the radiated emission at the power feed-line close to the conducted emission limit. The effect of an incident wave on a typical component size similar to the power inductor (25x17x12.5 mm) to be used is analysed. The optimal placement inside an enclosure of electromagnetically susceptible components such as filter inductors and power switching inductors are identified. The size of the box is 100mm x 150mm x 25mm.

Initially, a component is radiated without the enclosure, with an EM field as shown in Figure 4.52 (a). The peak current induced on the component is an expected maximum of - 108 dBA/m. This translates to about 60 dBμV/m, or 1 mV/m in air. Adding the open top enclosure as shown in Figure 4.52 (b), to the component is subjected less radiation. The peak radiation current is seen on the top rim of the enclosure. Placing the component in the middle of the enclosure it experiences about -110 dBA/m and components at the inside perimeter of the enclosure experiences slightly less, about -112 dBA/m. From Figure 4.52 (b) it is clear that the inside perimeter of this specific enclosure are the best shielded positions to place sensitive electromagnetic components, where surface currents are less than -112 dBA/m.

Raising the edges of the box from 25 mm to 50 mm as seen in Figure 4.52 (c) shows an improvement in component protection from outside fields as the components are more shielded from the currents flowing at the top of the enclosure wall. Surface currents of less than -115 dBA/m can be achieved if components are placed in the perimeter. The enclosure as proposed in Figure 4.52 (d) provides an additional 3 dB shielding effect from outside radiated fields. It is a completely sealed unit with the front open, instead of the top. The front face of the enclosure is reserved for the cable entry as well as the interactive interface, such as buttons or light indicators. The enclosure, if at all possible, should be properly earthed. Any common-mode noise injected into the signal cables will be shunted to earth. High frequency interference on power cables should be filtered and will be redirected to earth.

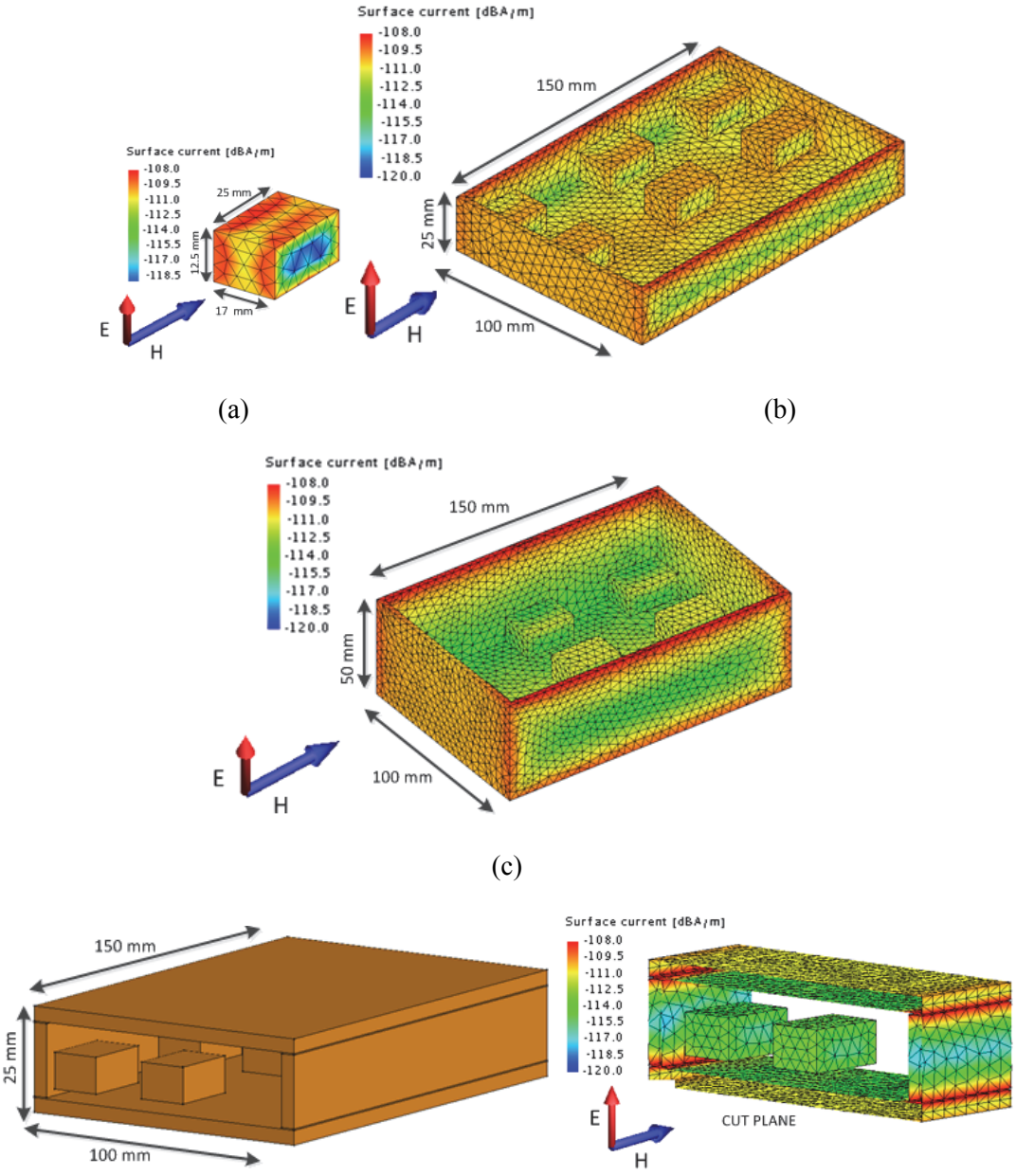
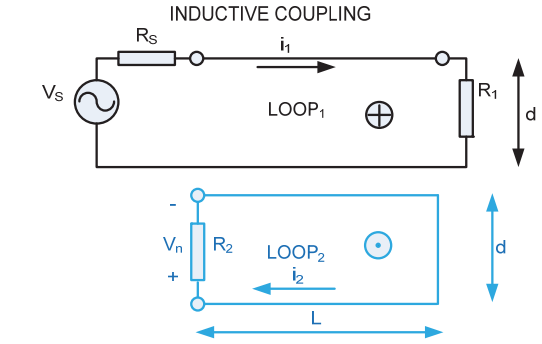


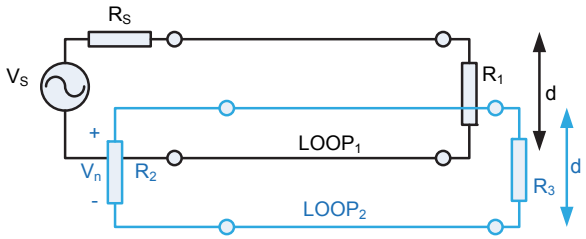
Figure 4.52. Components radiated: (a) No enclosure, (b) inside enclosure, (c) raised enclosure sidewall and (d) cut plane with lid and front open.

4.3.2 Trace coupling

Two coupling mechanisms exist, magnetic field (inductive loop) in Figure 4.53 (a) as well as electric field (capacitive) coupling in Figure 4.53 (b), between closely spaced parallel traces.



(a)



(b)

Figure 4.53. Coupling loops: (a) Magnetic and (b) electric.

The magnetic field coupling is explained as follows. Referring the inductive loop in Figure 4.53 (a), the voltage excited across R_2 due to current in Loop 1 is:

$$i_1 = \frac{V_S}{Z_{Loop1}} \tag{4.61}$$

Where

$$Z_{Loop1} = R_S + R_1 + \frac{2 \cdot L}{\sigma_{CU} \cdot A_C} + j\omega L_{self} \tag{4.62}$$

and

$$L_{self} = \frac{\int \overline{B} \cdot da}{i} = \frac{\mu_0 \cdot L}{2 \cdot \pi} \cdot \ln \left| \frac{(d-r)^2}{r^2} \right| \tag{4.63}$$

with, r, the wire radius. Using Faradays law of induction, the EMF denoted by E in Loop 2 in Figure 4.53 (b) can be found in a simpler form using relevant derived values as:

$$E = -jf\mu_0 i_1 L \ln\left[\frac{(2d-r)\cdot r}{(d+r)(d-r)}\right] \tag{4.64}$$

As can be seen from (4.65) the coupling effect is directly proportional to frequency, causing an increase in noise current due to the increase in E. In the case of capacitive coupling, the coupling capacitance is calculated by using the well-known physical expression in (4.58).

The capacitive coupling impedance is given by:

$$Z_C = \frac{1}{j\cdot 2\pi f\cdot C_{Coupling}} \tag{4.65}$$

Equation (4.66) shows yet again that with increase in frequency, the impedance decreases, with the consequence of easier noise transmission along the path.

4.3.3 Component coupling – Helmholtz Coil test bed

The Helmholtz coil is a device for producing a region of uniform magnetic field. It consists of two identical circular coils with radius R_H that are placed symmetrically along a common axis and separated by a distance D_H=R_H as shown in Figure 4.54. The two coils carry an electric field of the same magnitude and flows in the same direction, creating an uniform field in the test region.

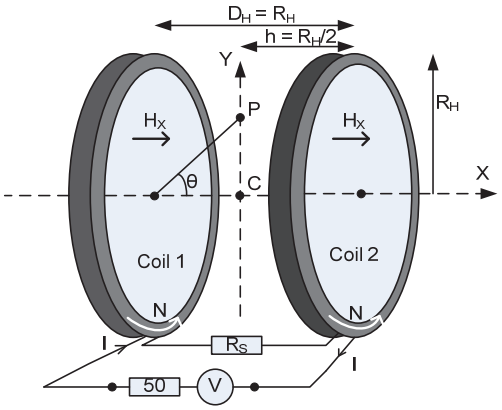


Figure 4.54. Helmholtz coil schematic.

The accuracy of the magnetic field uniformity mainly depends upon the accuracy with which the Helmholtz coil pair is constructed. Axial magnetic field strength, $H_{X,}$ in *A/m* can be calculated at any point *P* on the common axis joining the two coils using the Biot-Savart law as in (4.67).

$$H_X = \frac{N_1 I R_1^2}{2 \cdot \sqrt[3]{\left(R_1^2 + a_1^2\right)}} + \frac{N_2 I R_2^2}{2 \cdot \sqrt[3]{\left(R_2^2 + a_2^2\right)}} \tag{4.66}$$

$$H_{X,AV} = \frac{NI}{R_H \cdot \sqrt[3]{(1.25)}} \tag{4.67}$$

N and R_H are the number of turns and the separation distance between the coil pair respectively. X is the axial position of the magnetic field (in meters) and I the current flowing through the coils. At the centre position C, (4.67) can be simplified when both coil pairs have equal numbers of turns, coil diameter and radius, resulting in the average field strength in (4.68).

The wire resistance can be calculated with the well-known equation in (4.21). The Helmholtz coil series inductance L_H is calculated with the following expression using relevant derived values.

$$L_H = 2 \cdot N^2 \cdot R_H \cdot \mu_0 \left[\ln \frac{(16 \cdot R_H)}{u} - 2 \right] \tag{4.68}$$

The symbol u is the coil wire bundle diameter.

A Helmholtz coil according to MIL-STD-461-E specifications was manufactured to generate an equal B-filed to test the orientation effects of different components. The Helmholtz coil is an alternative method for testing radiated magnetic field susceptibility, if EUT size permits. The loop sensor specifications according to MIL-STD-461-E are as follows:

- Coil radius R_H = 117/2 mm
- Distance between Coils D_H = 58.5 mm
- Turns per coil, N = 37t

The average currents through the coils are 0.707 A, and the average field calculates to 0.2 mT.

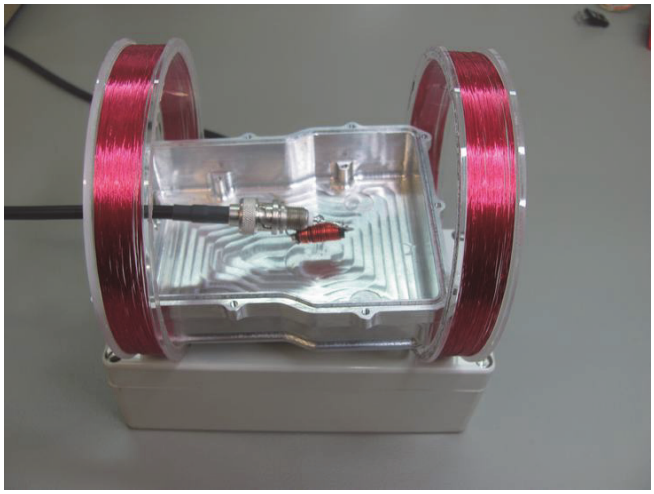


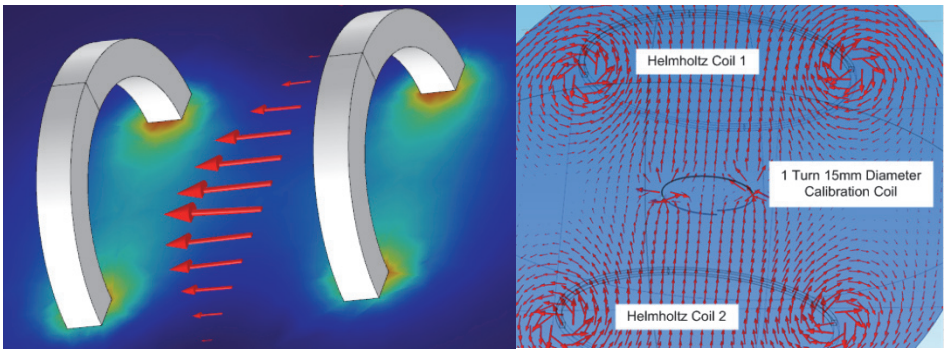
Figure 4.55. Helmholtz coil testing enclosure effects.

Due to the dimensions of this Helmholtz coil, it is usable for measurement up to 10 MHz, shown in Figure 4.57 and will not suffice in testing smaller components exhibiting higher frequency coupling effects. If higher frequencies are to be tested, a smaller sized coil need to be designed and manufactured. The Helmholtz coil shown in Figure 4.56 (a) is simulated in COMSOL, to verify the higher frequency design parameters and investigate the effect of the field on an object, in this case a single loop as in Figure 4.56 (b).

The measurement setup includes a network analyser, as depicted in Figure 4.58 (a). The component coil test bed and a test component are shown in Figure 4.58 (b). The component is rotated in the uniform electromagnetic field to determine the least and most susceptible angle. This is measured with a network analyser and recorded onto a PC through the GPIB port. The scattering parameters, S_{21} or S_{11}, converting for instance to impedance, using the following expressions:

$$Z_{IN}\,|_{Z_L=Z_0} = \frac{1+s_{11}}{1-s_{11}} \tag{4.69}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{S_{21}}{2} \tag{4.70}$$



(a) (b)

Figure 4.56. COMSOL simulation: (a) test bed and (b) calibrated object 15mm diameter loop single turn.

Three Helmholtz coils were manufactured, the MIL-STD-461 with coil diameter 117 mm, a smaller one with coil diameter 48 mm and a third and even smaller one with coil diameter 25 mm. The S_{11} parameter of these Helmholtz coil pairs, without any objects inserted in the field, is shown in Figure 4.57. This determines the maximum reliable operating frequency point. At least an order of a magnitude below the resonant point is the operating point. Beyond this frequency, the magnetic field homogeneity starts degrading [29], but it is reasonable for relative measurements up to 10 MHz.

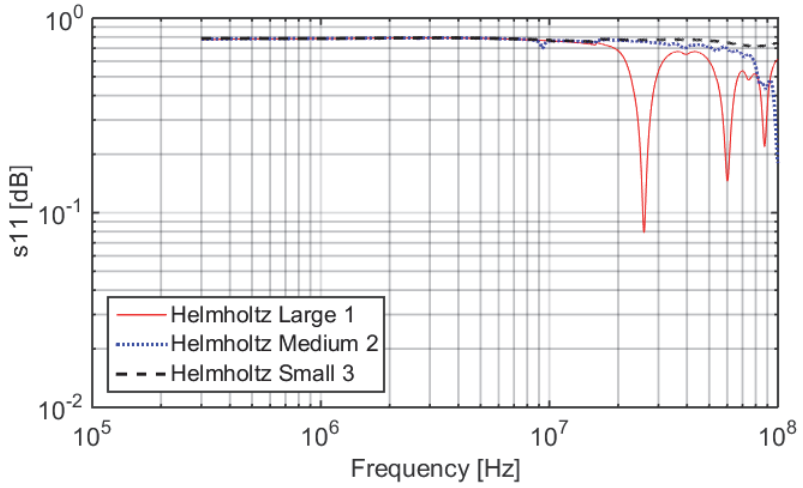
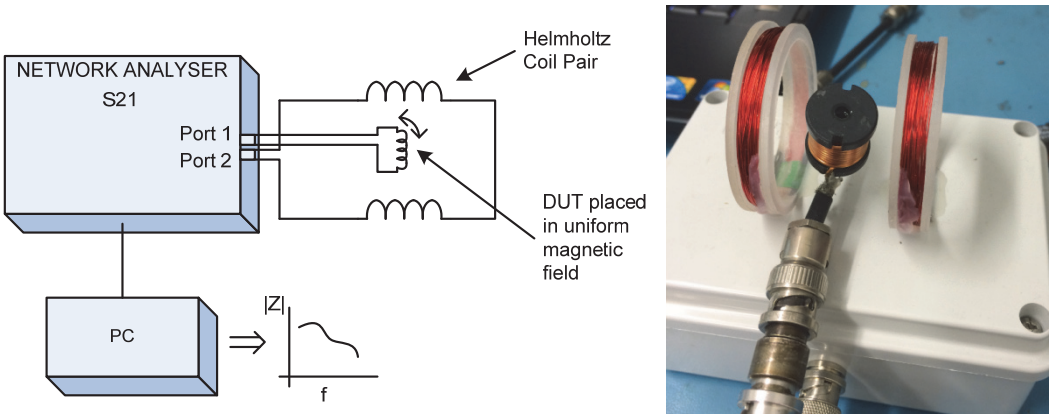


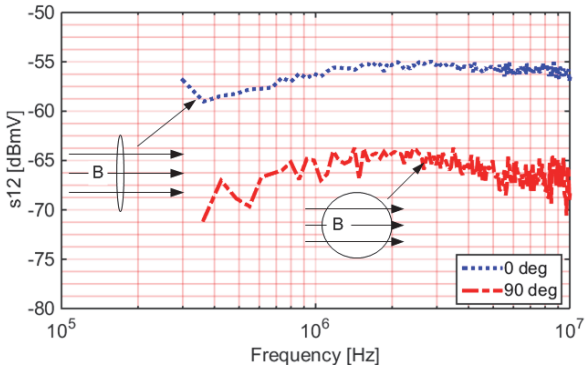
Figure 4.57. Helmholtz s11 Parameters large coil-, medium coil- and small coil-size.



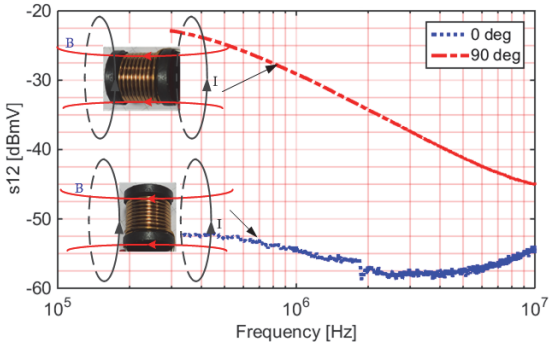
(a) (b)

Figure 4.58. (a) High frequency component orientation sensitivity test bed and (b) end product.

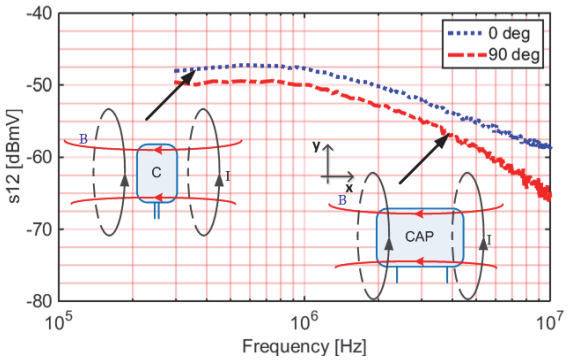
A single turn calibration test coil, 15 mm in diameter, is inserted in the field. The results in Figure 4.59 (a) show what is expected. Turning the loop so that the field cuts through an almost zero area, the coupling effect is low and the transfer scattering parameter S_{12} is obtained as -65 dBmV. When showing the maximum loop area perpendicular to the homogeneous field, it yields the maximum S_{12} value of about -55 dBmV. This clearly shows the most- and least susceptible angle of the particular component.



(a)



(b)



(c)

Figure 4.59. (a) Test loop, (b) switching inductor and (c) capacitor susceptibility.

Similar to the single loop test, passive components can be examined in this field. The components are mounted on the open end of a co-axial cable, so the mounting pins will also influence the readings, just as if mounted on a PCB. When the capacitor legs are in line with the homogeneous field, the coupling effect is at its lowest as it agrees with the field cutting through the minimum surface area.

4.4 CHAPTER SUMMARY

A practical and inexpensive method for measuring the power converter component impedances up to 100 MHz was presented. Dedicated instruments, an impedance analyser as well as a network analyser were used to verify and further analyse the component impedances in detail. Component models were derived as well as improved on to be able to accurately model components to at least 100 MHz. Accurate EMC modelling of selected key components such as the power feed-line from the LISN to the device as well as other converter noise path components, including the input- and output capacitor, power inductor as well as heatsink, was carried out.

Furthermore PCB trace effects, power lines and mutual coupling effects were analysed. Models for the switching components, MOSFETs, diodes and IGBT's equivalent circuits were derived. These will be used in the SPICE models as well as in ideal component modelling analysis software.

Proximity effects were investigated, in particular enclosure component positioning effects as well as component susceptibility effects. A Helmholtz testing technique was introduced to test component orientation sensitivity to susceptibility. This can be used to orientate components in close proximity in such a way that the least influence is exerted on adjacent components.

CHAPTER 5 DESIGN AND SIMULATION

5.1 MEASUREMENT BENCH DESIGN

Academic papers dealing with in-house conducted EMC testing [79], [80], [81], [82] were consulted. The use of a spectrum analyser is common to all. In [80], [82] a large air core inductor Line Impedance Stabilising Network (LISN) was built and verified. In [81], noise separation techniques, using complex RF circuitry or additional ETS-Lindgren current probes, not readily accessible in most power development laboratories are discussed. A shortcoming of the currently published in-house pre-compliance testing is that verification and calibration with accredited laboratories is not included. In [82] the manufactured LISNs are merely compared to a commercial LISN. Furthermore, the conducted noise levels beyond 30 MHz [33] are out of the scope of the normal EMC directive and thus not investigated. This is despite some directives for automotive requirements and also some military applications [83] being required to be tested up to 100 MHz. In modern high density high switching frequency converters (up to 1 MHz), EMI problems can occur beyond the standard measurement frequency of 30 MHz, making it necessary to test to at least up to 100 MHz. Furthermore it is mentioned in [83] that smaller ferrite-cored inductors can be used to manufacture a more compact LISN. Some negative consequences to be careful of include inductor core saturation as well as adequate core frequency response, as most mains input converters draw distorted sine-wave currents.

Performing pre-compliance tests with expensive measurement receivers and spectrum analysers consisting of pre-selectors can be costly and not viable in most cases. If these instruments are not frequently used in the laboratory, it becomes difficult to justify investing in them. Performing measurements with reasonable priced laboratory equipment, such as a digitising oscilloscope and a PC will be investigated and the results compared to compliance tests. A test bench is designed to accurately measure conducted EMC up to 100 MHz. A LISN is manufactured and tested at an accredited measurement facility. Thereafter the bench including the digital measurement technique is calibrated. This will form the basis of the experimental work.

A LISN is designed, manufactured and validated to measure power lead conducted emissions on a modified workbench. The validation is done in conjunction with an accredited Electromagnetic Compatibility (EMC) test facility. These measurements are used in the power converter design phase for diagnostic testing. A final pre-compliance test is performed in the design laboratory before visiting the accredited measurement facility. This technique will build confidence in the conducted EMC design and will eventually save time and cost in the power converter's qualification process. Basic 3-element lumped element EMC models will be created and compared to the measured results to determine if it is feasible. The ground theory publication based on this chapter was published in [23].

5.1.1 LISN design

Measurement of conducted EMI requires ambient power line noise to be isolated from that emitted by the equipment under test (EUT). This is necessary for ensuring that what is measured is from the EUT operation. The LISN is connected between the electric power source (mains or DC) and the EUT. The LISN presents defined standard impedance to the EUT power input terminals at high frequencies. Therefore, impedance variations of the power supply line are adequately isolated from the EUT. Furthermore, unwanted electromagnetic conducted interference on the power supply line is filtered out by the LISN. The LISN design should be aligned to the applicable test standard as well as the intended current carrying capability.

5.1.1.1 LISN configurations

The LISN is the standard transducer for measuring conducted emissions in most applications, although not the only way of measuring conducted emissions. Close field magnetic and electric probes can also be used in the power converter development phase. Larger diameter magnetic loop probes can also be used. In some instances voltage probes are also used for conducted measurements on power terminals, mostly because a LISN might not be appropriate, due to excessively high currents [21].

The basic configuration of the 50 µH MIL-STD-461 and ANSI LISN (also called the IEC LISN) are shown in Figure 5.1 (a) and (b) respectively. Both consist of a series 50 µH

inductor and one has an 8 μF capacitor and 5 Ω resistor to ground while the other has a 1 μF to ground on the line side. The EUT side has a 0.25 μF capacitor or 0.1 μF, and 1 kΩ resistor to ground. All measurement ports are terminated into 50 Ω. The ANSI LISN (FCC Requirement) has two models. The 150 kHz to 30 MHz and the 10 kHz to 30 MHz (also mentioned as 10 kHz to 150 kHz) shown in Figure 5.1 (c). The latter is required for the low frequency tests in CISPR 15 for electrical lighting with additional inductors and capacitors for filtering.

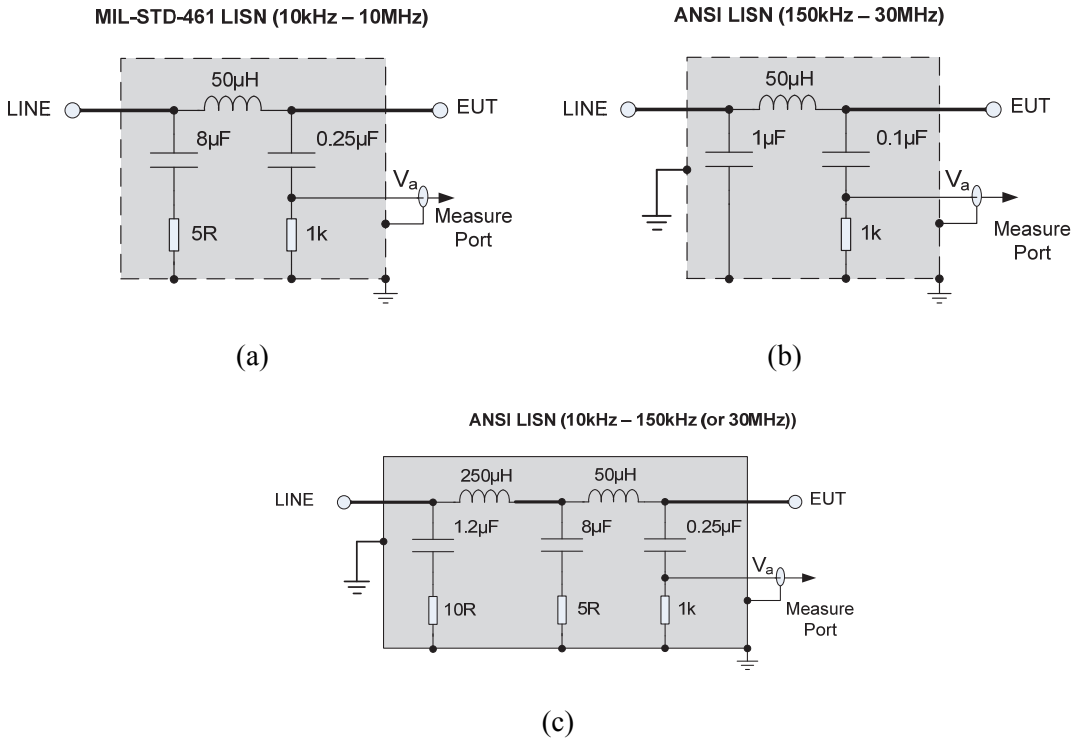


Figure 5.1. LISN configurations: (a) the MIL-STD-461 LISN, (b) the ANSI LISN 150 kHz to 30 MHz and (c) 10 kHz to 30 MHz configuration.

The impedance of the LISN is defined from the EUT port and the LINE port terminated with $0.2+j50x10^{-6}\Omega$. The configurations of Figure 5.1 have been modelled and the results displayed in Figure 5.2. The low frequency IEC LISN (10 kHz – 150 kHz) in Figure 5.1 (c), shows a slight resonance between 3 kHz to 10 kHz and this ought to be taken into consideration when measuring at lower frequencies. The MIL-STD-461 LISN shown in Figure 5.1 (a) is approximately linear at the low end due to the 5 Ω resistor added in series with the line input capacitor to quench the resonance at this point. Thus, the current

measurements such as specified in CE101 [21] from 30 Hz to 10 kHz can be correlated to the voltage measurement using the impedance plot of Figure 5.2. The characteristic impedance for all three models eventually stabilises at about 48 Ω.

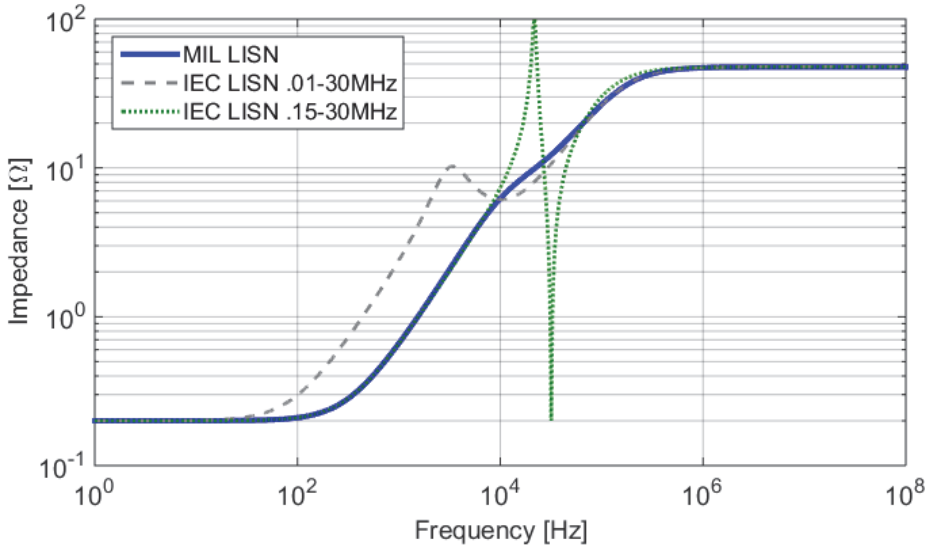


Figure 5.2. LISN impedance plot: MIL-STD-461 and ANSI LISNs.

The MI-STD-461 LISN will be manufactured to be able to measure and investigate non-compliant conducted emissions on power converters in the electronic development laboratory.

5.1.2 LISN manufacturing

An ETS-Lindgren LISN, 10 A per line, operating from 9 kHz to 30 MHz, can be purchased for around US$2500. A non-accredited self-built unit demonstrating reasonable accuracies can be manufactured for much less [79]. It can be very helpful in identifying conducted emission problems, analysing problem areas and implementing effective filters in the design stage. Manufacturing such a unit for laboratory testing will now be investigated.

A miniaturised toroidal inductor based dual MIL-STD-461 LISN was manufactured for non-compliance measurement of conducted emissions in DC-DC power converters. An attempt will be made to manufacture a LISN accurate enough and much smaller than the large air-cored wound inductor LISN's. It will be easier to carry, easier to store, and much

more convenient to use. The schematic as extracted from MIL-STD-461F is shown in Figure 5.3.

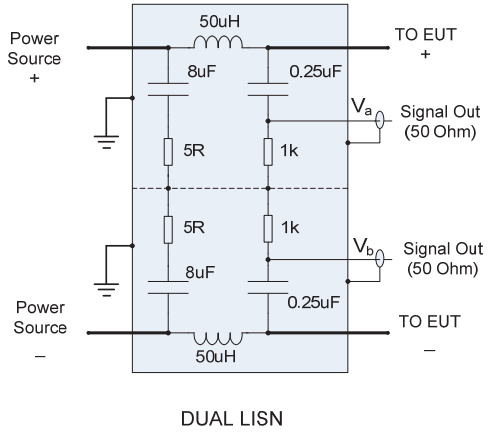


Figure 5.3. MIL-STD-461 dual LISN schematic.

Standard polypropylene film capacitors are selected and the resistors are 0.25 W carbon, 1% tolerance. The inductor was designed around a Kool Mμ distributed air gap toroidal core, part number 65AX 77548-A7. Some calculations concerning the 50 μH inductor design will be shown. The design current of the inductor will be 10 A. The winding inductance can be calculated from (5.1).

$$L = \frac{0.4 \cdot \pi \cdot \mu \cdot n^2 \cdot A_c}{l_e \cdot 10^8} \tag{5.1}$$

Where the following parameters from the datasheet are:

μ = Core Permeability (125 H/m)

N = turns

A_c = Core Cross Section (0.627 cm^2)

l_e = Magnetic Path Length (8.15 cm)

Re-arranging (5.1) and populating with the relevant values, yields N = 19.8, which is rounded-off to 20 turns.

The magnetic flux density can now be calculated.

The magnetic flux in Weber (Wb) is given as:

$$\phi = \frac{L \cdot I}{N} \tag{5.2}$$

Where L = inductance in H, I = maximum current in A and the magnetic flux density in Tesla:

$$B_{\max} = \frac{\phi}{A_e} \tag{5.3}$$

Using (5.1) and (5.3) the maximum flux density can be calculated to be 401 mT. From the datasheets this is well within the saturation limits.

Calculating the current density is more involved. One can utilise the heat calculation of copper, by using a specification from EN 60076-5 stating that the windings should be able to withstand a short circuit for at least 2 seconds. An acceptable copper heat rise value can be estimated and an acceptable wire gauge can be chosen. An acceptable continuous maximum operating current temperature rise also needs to be within acceptable temperatures. Choosing an initial copper wire current density of 5 A/mm^2 (value can be adjusted using an iterative process), the approximate heat rise within 2 s can be calculated with a simple equation based on certain assumptions. During the heat rise, parameters such as the eddy current loss, the I^{2}R loss, the specific heat value will change. By using average values, and ensuring that the temperature rise is not excessive, the following equation from [84] will be adequate:

$$\theta_T = \frac{t\left(1 + \frac{e}{100}\right) \cdot J^2 \cdot \rho \cdot F^2}{D_M \cdot h_s} \tag{5.4}$$

Where

θ_T = Temperature rise in K

e = Percentage winding eddy current loss

J = Winding current density in A/mm^2

ρ = Resistivity of conducted material (1.68x10^{-8} Ω.m)

D_M = Density of conducted material (8.9 g.cm^{-3})

h_s = specific heat of conductor material (0.385 J/gK)

F = Factor for short circuit current (multiple of rated full load current, say 5x)

Calculating a value using (5.4) gives a temperature rise of 10ºC, which is acceptable. This confirms that the initial selection of current density is acceptable.

The wire thickness is calculated from the current density, J. For a 10 A current, the copper area A_{cu} will be 2 mm^2. The copper conductor diameter is thus 1.6 mm.

Now the series resistance can be calculated. The standard equation is given as:

$$R = \frac{\rho_{cu} \cdot l_{cu}}{A_e} = \frac{l_{cu}}{\sigma_{cu} \cdot A_e} \tag{5.5}$$

Where:

R = total resistance of copper conductor

ρ_{cu} = resistivity of copper (1.7x10^{-8}Ω.m)

σ_{cu} = conductivity of copper (5.8x10^7 S/m)

l_e = copper wire length from datasheet (0.6 m)

Substituting these values into (5.5) yields a total DC resistance of 5 mΩ. The I^2R losses work out as 500 mW.

The maximum voltage drop across the LISN at full load is specified by CISPR16 to be within 5%. Using the coil DC resistance as an initial estimate, the voltage drop across the coil at 10 A is 50 mV. The wiring and connectors measured 20 mΩ, giving the total resistance as 25 mΩ. The voltage drop works out as 250 mV, and was confirmed on the test bench. At a worst case of 10 V input, the voltage drop is 2.5%, well within the specified 5%.

The inductor will be used mainly in DC-DC power converters and eddy current loss and loss due to hysteresis will be negligible. Temperature rise in a wound inductor core due to the operating current will now be considered. The temperature rise depends on the wire resistance and the current through the coil (I^2R losses), as well as the core excitation loss. The heat dissipated due to the loss depends on the total exposed surface of the wound unit. In [85], an approximate formula is provided to calculate the dissipated heat at operating current. The equation is given in (5.6).

$$TemperatureRise = \left[\frac{TotalPowerLoss}{SurfaceArea} \right]^{0.833} \tag{5.6}$$

Where:

Temperature Rise is the increased temperature from nominal i (ºC)

Total Power Loss in mW

Surface Area (cm^2) from the MAGNETICS specifications sheet, 48.0 cm^2

Substituting relevant values into (5.6) gives a total temperature increase of 7ºC.

The surface temperature increase was measured at constant full load over a period, using an infra-red instrument as displayed in Figure 5.4. The initial temperature was revealed as

22.0ºC. After about three hours on a wooden block, the temperature was measured to be 30.4ºC, an acceptable increase of 8.4ºC, slightly higher than the calculated value.

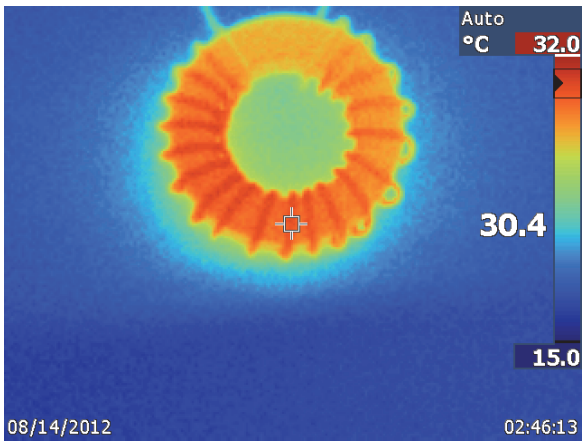


Figure 5.4. Inductor temperature rise.

The self-resonant frequency of the inductor needs to be outside the measurement band, implying as low as possible interwinding capacitance. The inductor was wound as shown in Figure 5.5. The spacing B between the windings (about 5 mm) reduces interwinding capacitance and the gap A (about 12 mm) reduces the start/finish gap capacitance. Damping resistors were placed on the windings to reduce the resonance peak, similar to the proposed damping resistors on the large air-core inductor.

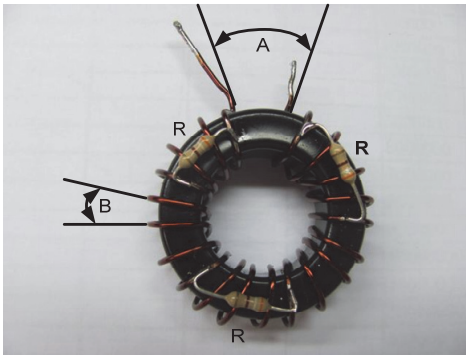


Figure 5.5. MIL-STD-461 LISN damped toroidal inductor.

Figure 5.6 shows the damped toroidal inductor impedance, an undamped version with the resonant peak at about 20 MHz, a stranded litz-wound version is also shown, with higher inter-winding capacitance and a resonant peak occurs at 10 MHz. A large inductor single layer air core version impedance is also shown for comparison.

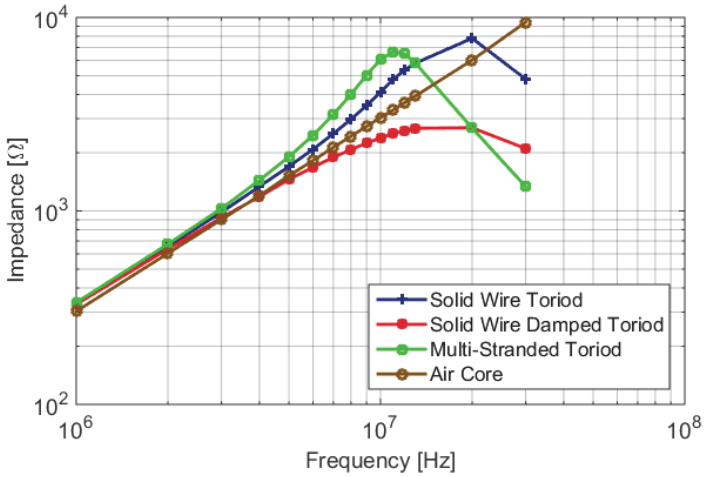
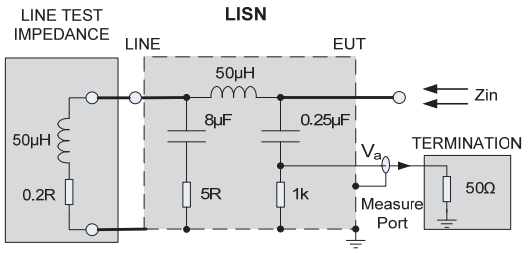


Figure 5.6. LISN 50 μH inductor type impedance.

An impedance plot, similar to Figure 5.2 was generated to measure the impedance of the constructed LISN. The measured impedance, with measurement set-up shown in Figure 5.7 (a), is similar to the simulated values shown in Figure 5.7 (b). An impedance variation of 20% tolerance is allowed by the standards. The impedance was measured with an LF Impedance Analyser, the HP4192A



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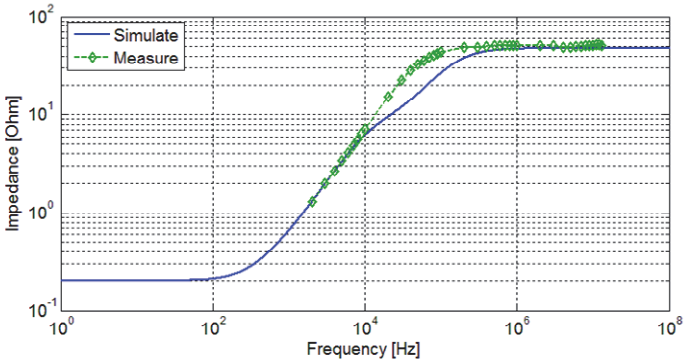
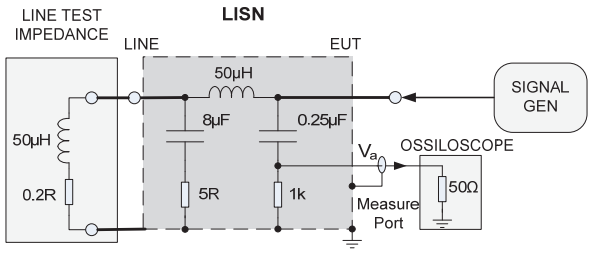


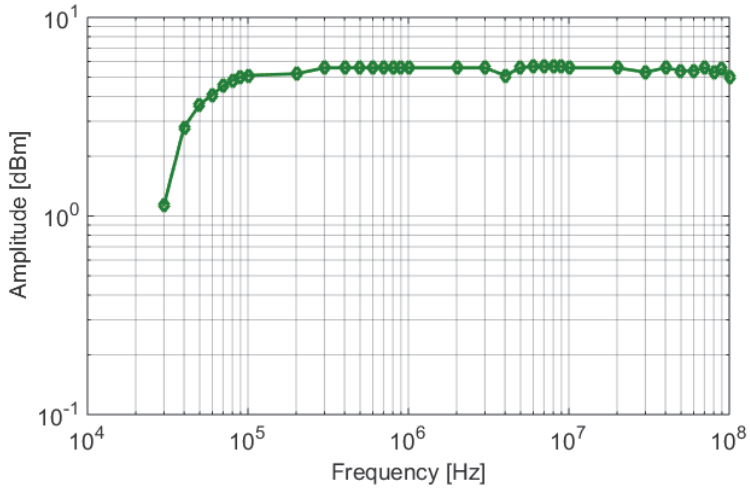
(b)

Figure 5.7. LISN impedance measurement comparison: (a) The setup and (b) the measured results.

The manufactured LISN and circuit diagram test setup is shown in Figure 5.8 (a) and was verified and the frequency response is given in Figure 5.8 (b). The LISN was terminated with the standard 50 µH/0.2 Ω circuit. The source impedance of the signal generator was 50 Ω, set to a 10 dBm output level. The MIL-LISN is able to perform measurements up to 100 MHz.



(a)



(b)

Figure 5.8. LISN frequency response: (a) the test setup and (b) measured results.

The complete LISN module is shown in Figure 5.9, its dimensions measuring 120x95x60 mm, making it easy and convenient to store, carry around and use.

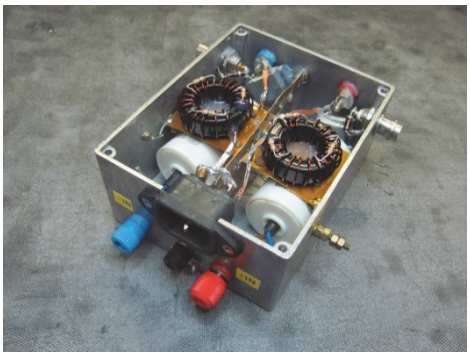


Figure 5.9. Complete LISN module.

5.2 LISN AND MEASUREMENT BENCH VALIDATION

The LISN will be validated with a circuit containing a single resistive switch and a known capacitor to earth. The conducted EMI will be predicted, measured at an accredited laboratory and verified in the LAB with the miniaturised LISN. The purpose of this will be to understand the origin of the conducted EMI noise and show a simple way of predicting the noise for future designs as well as to validate the predictions with measurements.

5.2.1 Houwteq accredited measurements

Houwteq is situated in the Western Cape province of South Africa. At this site there is a well-equipped EMC laboratory with calibrated instruments and accredited facility. The resistive switch noise source conducted EMC was measured at Houwteq with their calibrated LISN. Their LISN was afterwards replaced with our LAB prototype and the measurements repeated. These two graphs were then compared to each other. Figure 5.10 shows the measurement setup at Houwteq, comparing the large air wound inductor LISN to the compact damped toroidal inductor LISN.

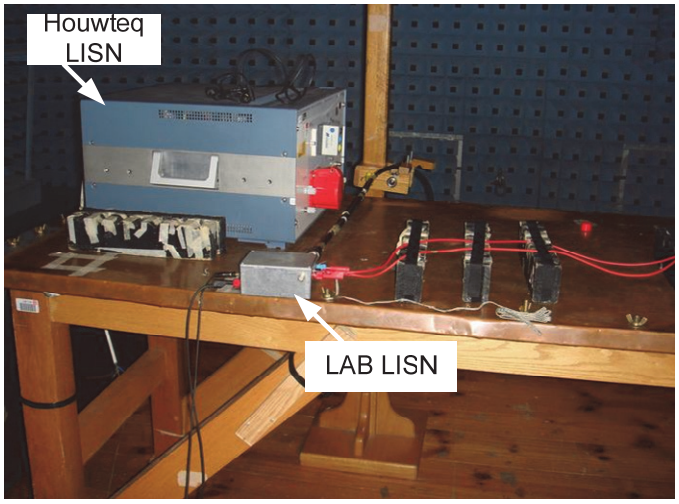
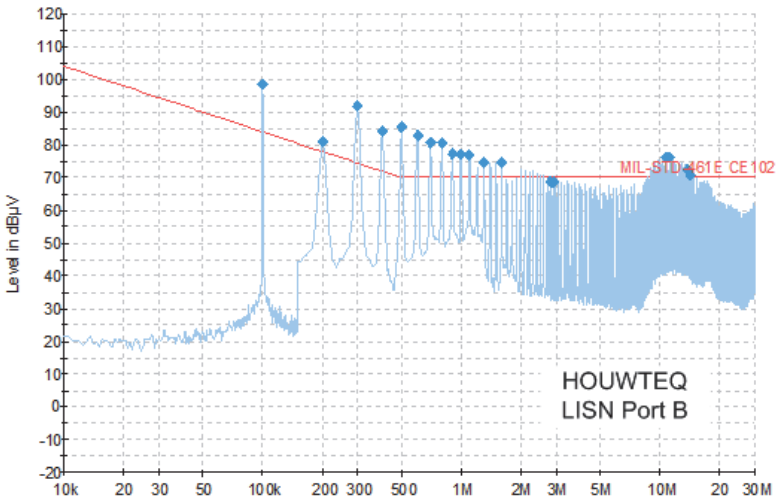


Figure 5.10. Houwteq measurement setup.

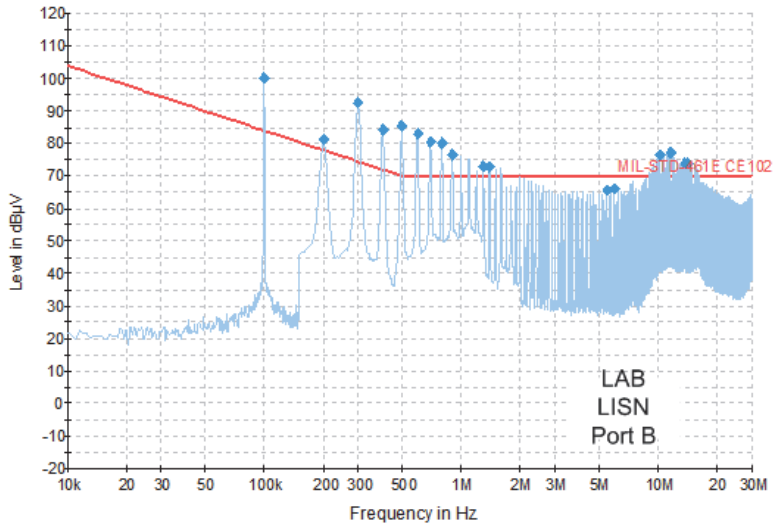
5.2.2 LISN Results

The LISN comparative conducted emissions tests were performed from 10 kHz to 30 MHz on a conductive surface utilising a resistive switch noise source. The two setups were

exactly the same with only the LISNs being swopped. Figure 5.11 (a) presents the characteristics measured with the Houwteq LISN and Figure 5.11 (b) shows the characteristics measured with the constructed laboratory LISN. Both were recorded with a calibrated R&S spectrum analyser.



(a)



(b)

Figure 5.11. LISN comparison: (a) Houwteq LISN and (b) laboratory LISN.

The LAB LISN is thus proven to be accurate enough for pre-compliance test measurements when used in a controlled environment. Small deviations can be attributed to noise fluctuations (measurement inaccuracies). These measurements need to be repeated

in a LAB environment on the workbench to be able to claim pre-compliant measurements in the development laboratory that can be used for testing during product development phase.

5.3 LAB COMPARISON

Some differences exist between the accredited facility and the laboratory measurements. The one is the anechoic chamber room properly grounded and fully screened from outside interference and inside reflections, up to tens of GHz. Conducted emissions is mostly performed at the lower frequencies, in this case below 100 MHz. The laboratory room is very well grounded, with a ground pin right outside the room and copper bar railings around the inside of the room. The walls have been plastered with chicken mesh-wire and grounded so as to create a fairly consistent EMC laboratory environment. The mains power inlet is filtered and isolated through a 10 kW mains transformer.

The accredited EMC facility records the conducted EMC with the traditional EMC spectrum analyser. In the power laboratory, a Tektronix MDO4034B oscilloscope consisting of four 11-bit analogue channels at 4 GS/s each and one frequency spectrum channel is used to record the data. MATLAB is used as a signal-processing tool for analysing the recorded data and calculating the spectral slopes [9], [86] - [89]. Due to the dwell-time in traditional spectrum analyser measurements, the time-domain measurement system yields a reduction in the measurement time [9]. The function of the dwell-time is to measure unwanted noise occurring at irregular intervals. Dwell-time can be simulated by recording multiple digital traces or even to set up an oscilloscope trigger to investigate irregular behaviour.

5.3.1 EMC measurements in the time-domain

Traditionally, superheterodyne EMC receivers are used to record the EMI spectrum. According to the EMC standards, the measurements are performed by sequentially running through the frequency band, dwelling for several seconds at each frequency bin to be measured, thus taking several hours to complete a proper scan. The time-domain EMI measurement technique is based on a broadband analogue-to-digital conversion, in this

case accomplished using the digital oscilloscope. This recorded time-based data is further processed by signal processing routines, including the Fast Fourier Transform (FFT), to provide frequency domain results. Signal processing techniques can also be used to calculate the average, RMS, peak and quasi-peak values of the EMI signals if need be [86].

The digitising bandwidth in the time-domain has to be high enough to fulfil the Nyquist criterion. In real-time systems, the data-throughput of the hardware normally limits the bandwidth, but if a post-processing method is followed such as in this case, full sampling bandwidths are utilised. In MATLAB, the function *fft(f(n),n)* computes the discrete Fourier transform of a signal. It is important to choose the data length, n, equal to a power of two, or to pad the data with zeros to equal the data length to a power of two. The fft implemented in MATLAB follows the commonly used complex exponential form:

$$F(k) = FFT\{f(n)\} \tag{5.7}$$

$$F(k) = \sum_{n=1}^{N} f(n) \cdot e^{-j2\pi nk/N}, \qquad k = 0,1,....,N-1 \tag{5.8}$$

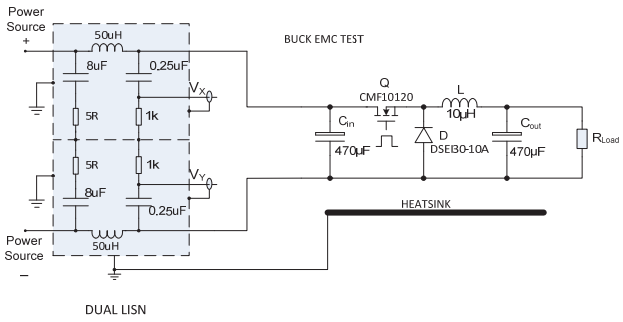
Since MATLAB does not allow zero indices, the values are shifted by one index value.

$$F(k) = \sum_{n=1}^{N} f(n) \cdot e^{-j2\pi(n-1)(k-1)/N}, \qquad k = 1,2,....,N \tag{5.9}$$

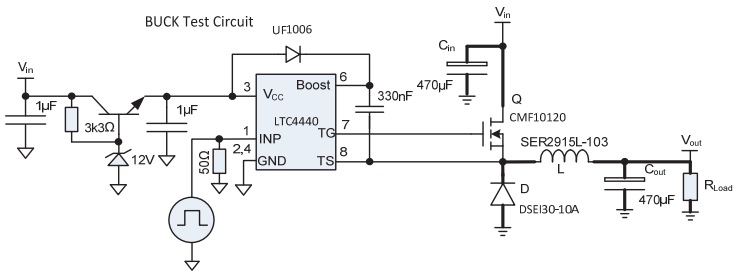
A guassian window function *w = guasswin(length(t))* is generated in MATLAB and multiplied with the signal to model the IF filter. Taking the fft in MATLAB is simply *Y = fft(signal,n).* Avoiding taking the log of zero, find all zeros by *index = find(Y==0),* and replace with a very small value, *Y(index) = 1e-17.* Further computations perform a quasi-peak value, followed by a spectral peak slope function for clear graphical presentation as only the spectral slope is of concern. The presentation output is a plot with function *semilogx*. The conducted EMC time-domain recordings and consequent FFT signal processing routine outputs are comparable to the traditional EMC spectrum analyser measurement system.

5.3.2 Step-Down DC-DC compliance comparison

The step down DC-DC converter is manufactured to compare the Houwteq accredited facility measurements to the laboratory bench measurements, thus calibrating the laboratory bench. The schematic is given in Figure 5.12 (a), incorporating the CMF10120 SiC MOSFET. The MOSFET drive circuitry is shown in Figure 5.12 (b) realised with a LTC4440 MOSFET gate driver. The oscillator is realised with a TL494 control chip. A picture of the prototype DC-DC converter is shown in Figure 5.12 (c).



(a)



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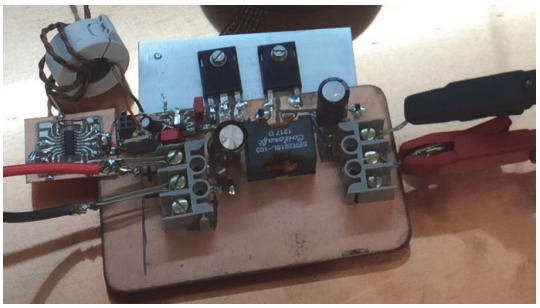
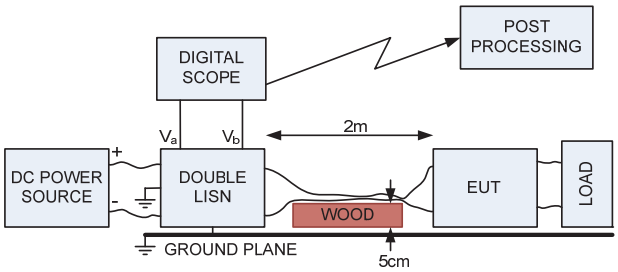


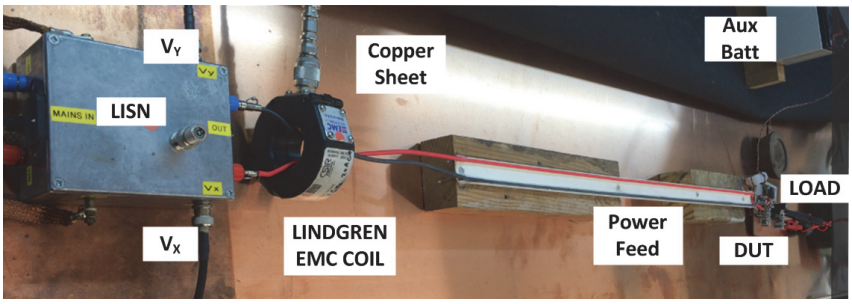
(c)

Figure 5.12. (a) Schematic of step-down converter circuit with LISN, (b) the MOSFET drive circuit and (c) the test construction.

The LAB measurement block diagram is shown in Figure 5.13 (a) and the actual setup in Figure 5.13 (b). The EUT will be the step-down DC-DC converter. The noise currents from the LISN will be recorded simultaneously with a 4 Gs/s oscilloscope and with post processing techniques that are applicable in the frequency domain. These results will be compared to the calibrated measurements. The LAB tests are processed digitally and not with a spectrum analyser. The reason is that in a power converter LAB, a spectrum analyser is normally not part of the instrumentation. A high speed digital oscilloscope can be an asset in many ways and is regarded as a preferred instrument for development. Furthermore, the post processing can be performed on a standard PC, with for example MATLAB or MathCAD. The digital; recording noise floor is presented in Figure 5.13 (c) showing a level close to 20 dBμV, showing good dynamic range up to the noise limit level.



(a)



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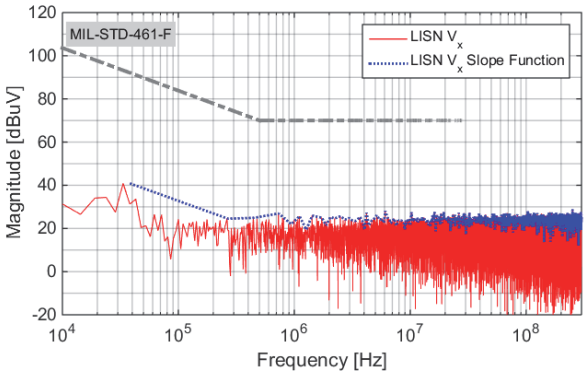
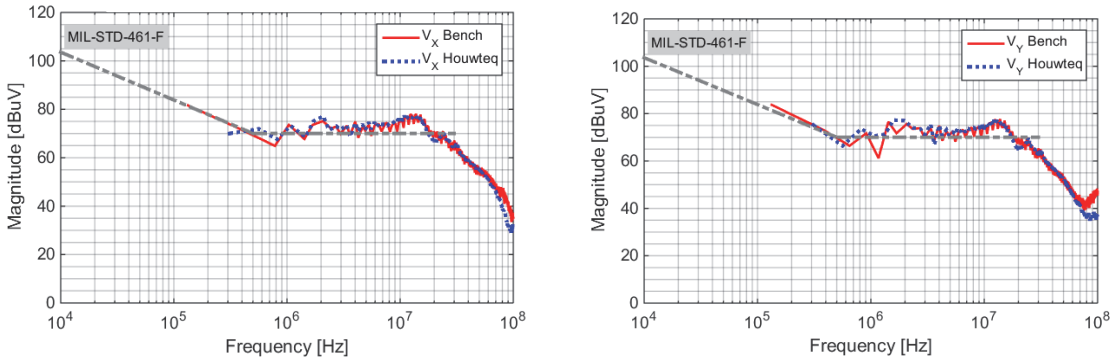


(c)

Figure 5.13. Laboratory measurement setup: (a) Block diagram, (b) construction and (c) digital recording noise floor.

Figure 5.14 (a) shows the LISN Port A output (V_X) comparison between the accredited measurement and the laboratory bench measurement. Up to 100 MHz the two characteristics compare very well. Similarly, Figure 5.14 (b) shows the LISN Port B output (V_Y) comparison. Again there is a good agreement. Above 50 MHz, the accredited measurement shows a lower value, due to the high-power dual LISN at the accredited laboratory that is specified only up to 50 MHz. The laboratory LISN on the other hand, is manufactured for up to 100 MHz [23]. A very good agreement exists between the two

measurement techniques confirming that the proposed conducted EMC pre-qualification technique is capable of yielding acceptable results.



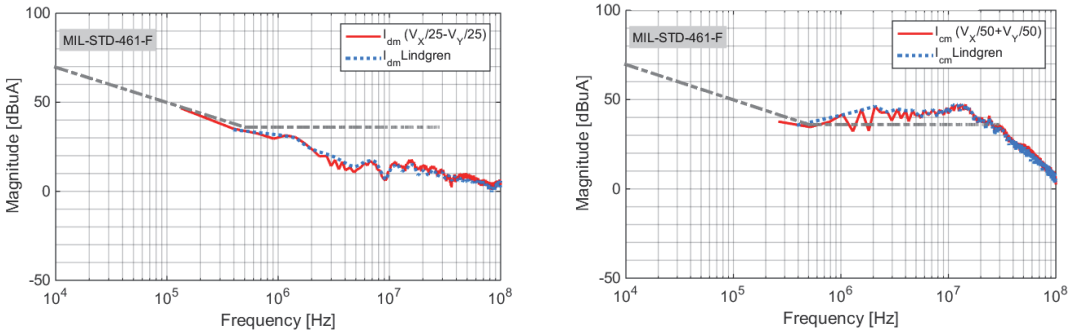
(a) (b)

Figure 5.14. (a) LAB Test Comparison Port A (V_X) and (b) LAB test comparison port B (V_Y).

The above tests were significant due to the two different measurement techniques and setups. At the accredited laboratory, a calibrated R&S spectrum analyser was used for the measurements and due to the instrument configuration, measurement traces cannot be recorded simultaneously thus the differential-mode and common-mode slopes could not be extracted.

5.4 COMMON-MODE AND DIFFERENTIAL-MODE EXTRACTION

Due to the simultaneous digital measurement of the dual LISN ports, common-mode and differential-mode can be extracted. This is done according to the calculations as described in section 3.2, and measurement setup as in Figure 3.3. The LISN port signals are recorded on channel 1 and channel 2 of the digital oscilloscope. The Lindgren EMC current probe data is recorded on the 3rd channel. The slope calculations are performed with MATLAB up to a 100 MHz. Both the differential-mode shown in Figure 5.15 (a) as well as the common-mode spectral slopes in Figure 5.15 (b) show good correlation, and thus validate the derived common-mode and differential-mode equations. This is an important contribution as it provides engineers with alternative methods to obtain common-mode and differential-mode noise signals.



(a) (b)

Figure 5.15. (a) Extracted differential-mode slope comparison and (b) extracted common-mode slope comparison.

5.5 ACCURATE HIGH FREQUENCY MODELLING

Conducted EMC noise qualification tests are normally carried out after a prototype has been designed, built and tested and the process is repeated in the event of non-compliance. The ability to determine compliance with EMI standards at the design stage is therefore desirable. This paper will present conducted EMC noise modelling and measurement techniques, yielding simulated and measurement noise results accurate enough to serve as a prequalification tests at the design and prototyping stages respectively. Accurate models of the power feed-line connecting the LISN to the DUT (converter) and the converter, including the load are developed. Predictive conducted EMC modelling is accomplished using detailed active level 3 SPICE-based models, creating a real-time circuit model consisting of a complete converter in its operational state, without the need to separate into equivalent models. Effects of the power feed-line length on EMI noise measurements are investigated as currently available literature has not dealt adequately with this issue. To detect possible radiating frequencies that might merge with the conducted noise and are detectable in the conducted emission test, results have to be accurate not just in the prescribed frequency band, but all the way up to 100 MHz. The modelling and measurements are performed using software and instruments available in a development laboratory.

A simplified EMC model was presented in section 4.2.14, analysing the heatsink interaction properties. The simplified models are ideal for investigating certain EMC

aspects, in this case the heatsink interaction. But more accurate and versatile models are needed to provide calibrated levels and high frequency effects not necessarily seen from simple models. Putting a complete model together of the converter in its test environment will be a more versatile op

The step-down sample circuit from Figure 5.12 will be used to demonstrate the modeling methodology. Based on the lumped-element models generated previously, a complete active parasitic lumped element model is created, simulating the complete power converter operation. Transient SPICE simulated output signals are stored and as before, MATLAB will perform the signal processing environment to calculate the spectral slopes. The active components such as the MOSFETS are implemented with model data gathered from datasheets for instance the SiC MOSFET [90] and free-wheel diode [91].

5.5.1 Conducted EMC modelling software

It is feasible to generate active lumped-element predictive EMC models, quantifying emissions without measurements, with readily available software, even with fairly complex converter topologies. In the literature, many attempts have been made in the past with generally not very good accuracies. In [92] the simulation tool ORCAD, a level 3 analog behavioural model (ABM), was utilised to build a flyback converter circuit with parasitic elements included, but simulations were performed only to 150 kHz. Similarly, Whole-Link was used. Recently, good accuracies have been achieved but mostly up to 30 MHz. In [44] a good predictive conducted EMC modelling method is presented, but utilising expensive Saber time analysis software not always in reach for a normal power design laboratory. The common-mode (CM) and differential-mode (DM) noise separation equations are provided but not defined, and presumed inaccurate. Furthermore, measurements are not calibrated, raising doubts about the accredited nature of the results. The important power feed-line is also not considered in detail. A high-frequency impedance modelling technique is shown in [14] with very good accuracies up to 30 MHz, based on vector modelling by impedance measurements, providing a very good analysis and complex high order models, but omits the qualification/measurement setup. Further, VHF measurement based frequency component modelling is done in [35], but providing s-

parameter results and omitting the power feed-line and LISN. A need thus exist to verify the conducted emission results for accuracy to give confidence that this converter will be accredited.

Two types of software will be investigated, PSIM, an ideal component analysis tool and Micro-Cap SPICE simulator from Spectrum Software. PSIM is easy to use and widely available in electronic power laboratories for designing power converters and its control circuitry. It also provides very fast and fairly accurate results, and quick analysis times, even with complex circuitry.

Most small-scale models can be generated with PSIM, a power simulation software package using ideal components. It is accurate and complex circuitry easy to run on this platform. The main drawback is that trapezoidal switching slope parameters are not adjustable. Furthermore, comprehensive models of the active components do not exist in PSIM and have to be created. The drawback is that it lacks the ability to model the non-linear effects of the switching components and changing the rise- and fall time slopes on the PWM is not possible. As output, a text data file gets generated from the LISN ports simulated results and MATLAB is utilised to analyse the data further, calculating CM and DM noise levels and plotting spectral slopes. Other SPICE-type packages such as Spectrum Software's Micro-Cap, were also investigated for ease of use and accuracy. The SPICE-based analysis software on the other hand, is more complex to set-up and use. It takes about 10 times longer to analyse, sometimes the complex circuitry can run into convergence problems and crucial high value resistors need to be placed at certain nodes, but once set-up, it provides very useful and accurate information. It is easy to select different component models from the build-in SPICE library, and if not available, it is recommended to set-up a new library from datasheets. It is furthermore quick to change the topology or even add multiple converters. The output is a .TNO file extracted from the simulated LISN ports; space delimited, and can easily be imported into MATLAB for further analysis.

5.5.2 Modelling process

For now, component proximity effects are not included in the model, as it pertains mostly to larger components, mostly for converters in excess of 500 W. However, in this case, due to the magnetically shielded construction of the inductor, and fairly low power conversion, the proximity effects are expected to be minimal [93]. The aim is to create a complete conducted emission model simulating accreditation measurements, building confidence in the process that the converter will pass Electromagnetic Compatibility qualification tests.

The model block diagram is given in Figure 5.16. The LISN and power feed-line model is the same for all converters, as derived in Chapter 3. The rest of the models are converter specific, such as the input- and output capacitors, the MOSFET and diode, the inductor as well as the load. In SPICE simulators, models exist for most of the switching components, but in an ideal component simulator, these models need to be created as shown in Chapter 3.

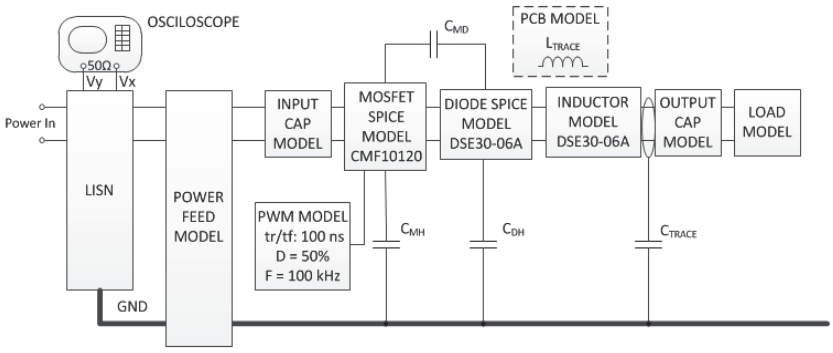
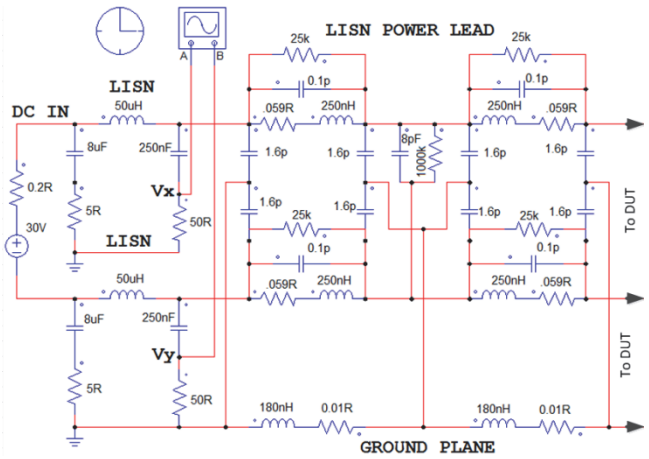


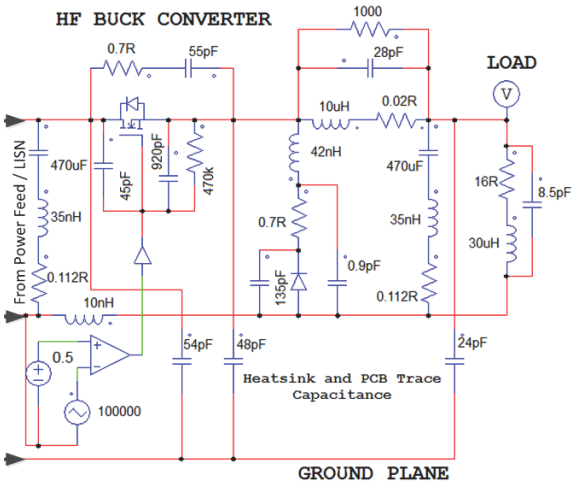
Figure 5.16. Active conductive EMC step-down DC-DC converter model block diagram.

The parasitic parameters are from the sample step-down DC-DC circuit given in chapter 3. The circuit model including the LISN and power feed-line is given in Figure 5.17 (a) and that for the step-down DC-DC converter is shown in Figure 5.17 (b). These models are a more accurate version of those used in [93]. The two parts are combined to create a model for the entire system. This is then modelled in PSIM, as it provides fast lumped element modelling times due to its ideal component solution method. The power converter switching frequency is set to 100 kHz, a duty cycle D = 0.5 and input voltage V_{in}=30V.

The wirewound load is set to 16 Ω, and has a 30 μH inductance and an 8.5 pF stray capacitance.



(a)



(b)

Figure 5.17. Equivalent PSIM circuit models: (a) LISN and power feed-line and (b) DC-DC step-down converter.

The resultant conducted EMC plots for LISN port V_X are given in Figure 5.18 referenced to MIL-STD-461F standards. They present the bench measurements, the PSIM prediction as well as a comparison to an accredited measurement. It is seen that there is very good agreement between the PSIM model prediction and the measurements for this basic step-down converter. Additionally, there is much better agreement between the PSIM and measured characteristics compared with those obtained in [93]. This is primarily due to

the more accurate models for the power feed-line and DC-DC converter implemented for the current investigation. It is further confirmation for the need to have accurate models if the predicted emissions are to be comparable to measurements. For the converter to pass accreditation, both V_x and V_y LISN ports spectral plots need to be within the limits provided by the standard.

Beyond 30 MHz more discrepancies arise, as it is in this frequency band where trace parasitics and components interaction effects will play a role, and they are not included in this model. Due to this shortcoming, slight adjustments to the model are made for better accuracies. The active components, the diode and the MOSFET, are the main cause of discrepancies. To be able to predict the magnitude lump at just over 10 MHz, the diode datasheet capacitance had to be increased from a value of 35 pF to 135 pF. This increased value is needed to compensate for the trace and proximity effects. Similarly, the MOSFET C_{GD} had to be increased from 7.5 pF to 45 pF, mostly to cater for Miller effect as well as trace effects. The low frequency discrepancy in the calibrated accredited measurement in Figure 5.18 is due to a 150 MHz peak detector attenuator that was in line to be able to accurately measure the high frequencies. However, it attenuated the measured signal below 1 MHz.

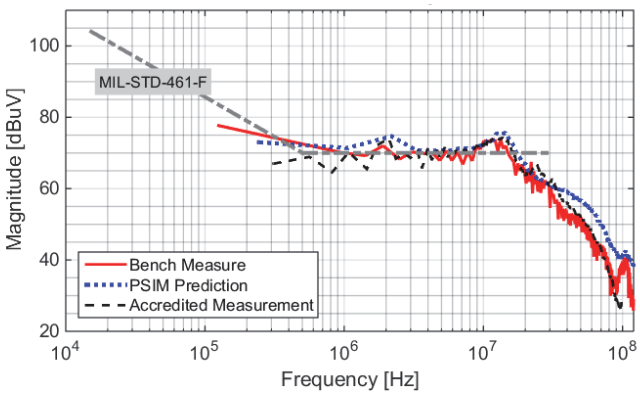


Figure 5.18. Simulated, measured and accredited LISN port signals.

In Figure 5.19 (a) the common-mode signal is compared to the MOSFET switching signal. The common-mode measurement shows that a faster dv/dt rising switching signal of 20 ns creates a larger common-mode noise signal if compared to the slower falling dv/dt of 80 ns. The CM pulse in Figure 5.19 (b) is similar to the simulation performed in [20], but the

latter excludes the high frequency oscillations. A slight switching offset can be seen, as the prototype step-down DC-DC converter switches at a slightly higher frequency at about 110 kHz, due to component tolerances. The amplitude difference is due to the slightly faster switching speed in the model. Nevertheless, there is very good correspondence between the two waveforms. Figure 5.19 (c) shows a comparison between the PSIM predictions and the actual measured on the LISN V_X port spectral plot data. Again, there is a good agreement between the simulated and the measured data curves. The oscillations at 2 MHz as well as at 10 MHz are accurately predicted. Figure 5.19 (d) shows the same prediction, but with a SPICE model. Similar accuracies are achieved, but beyond 60 MHz, the SPICE prediction seems more accurate, as noticed by the slope as well as the more accurate prediction of the CM spike at 100 MHz. The two comparison graphs shows that PSIM, an ideal component model simulation tool, adding parasitic components, can be a fast and easy first-order conducted emission simulation tool. Changing switching slopes and modelling the active components more accurately for better accuracy, a SPICE model is necessary.

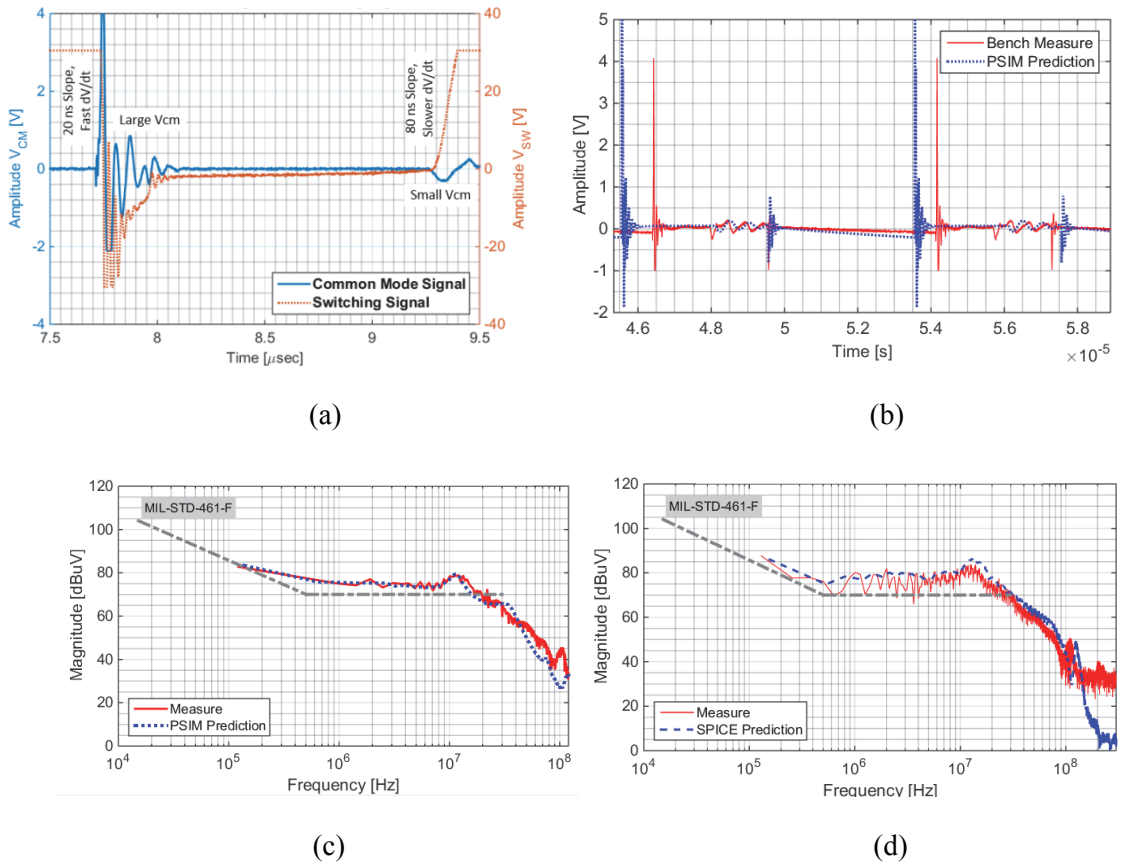
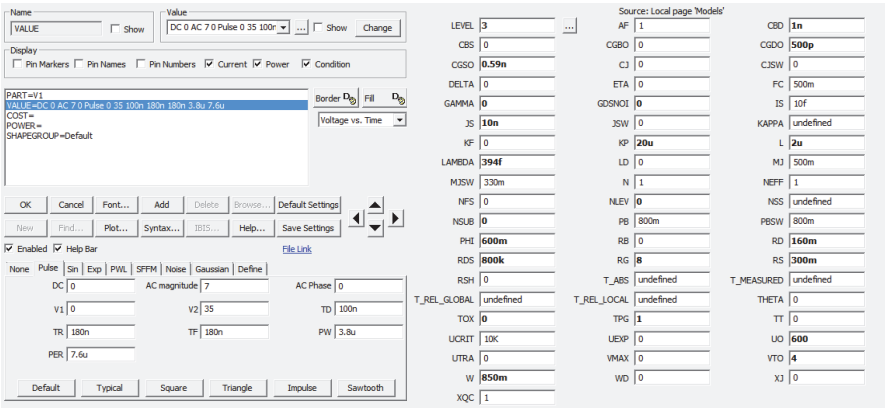
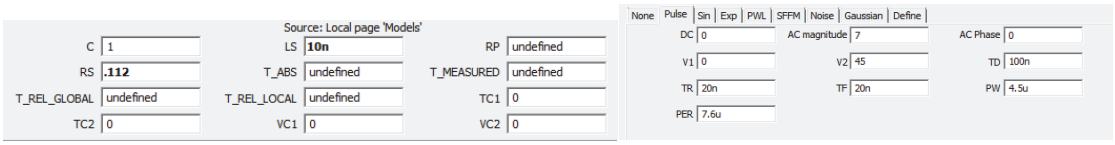


Figure 5.19. Simulated and measured common-mode signal: (a) and (b) common mode noise waveforms and (c) PSIM model V_X spectral slopes and (d) SPICE model V_X spectral slopes.

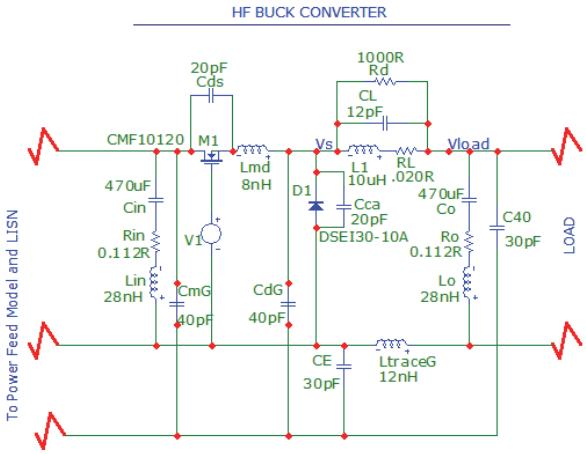
The SPICE model circuitry is the same as shown in Figure 5.17, and provides similar results, but more parameters are available. Figure 5.20 shows the SPICE signal parameter setup as well as the MOSFET level 1 SPICE parameters setup. Additional to PSIM, the SPICE parameters for the switching waveform can be modelled in detail, programming different rise- and fall-times. The detail setup of the active component parameters makes the SPICE simulator a superior tool in common mode conducted EMC analysis.



(a)



(b) (c)

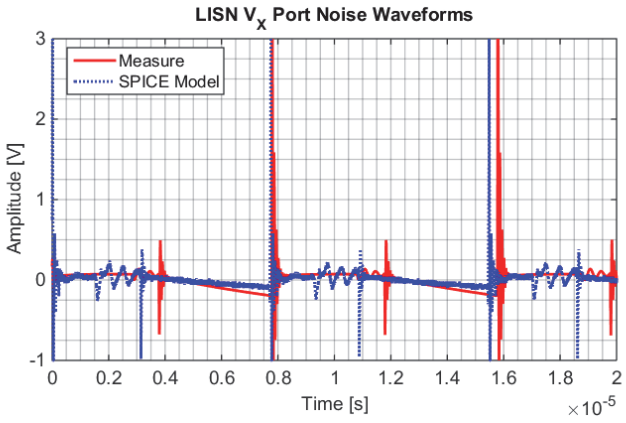


(d)

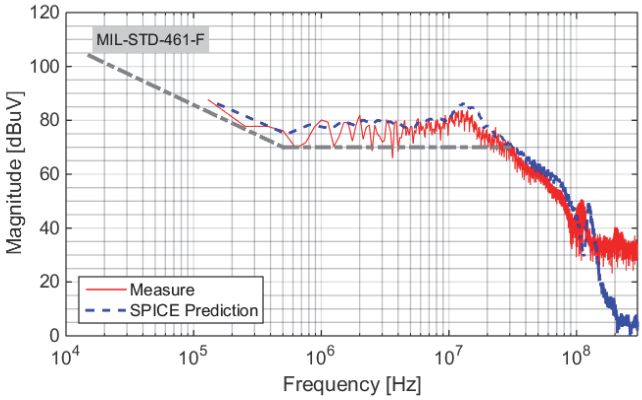
Figure 5.20. (a) Sample SPICE Signal and MOSFET parameter lists, (b) capacitor SPICE parameters, (c) PWM wave setup and (d) SPICE circuit model.

The relevant parameters for the SPICE models with regards to EMC modelling can be found in [50], also showing the effect critical parameters will have on EMC.

The V_X port results from the SPICE model given in Figure 5.21, with very good accuracies.



(a)



(b)

Figure 5.21. (a) LISN VX Port model and measurement comparison time base plot and (b) port V_X spectral slope.

5.6 CHAPTER SUMMARY

This chapter has set the basis for modelling and accurately measuring conducted EMC. A LISN was designed manufactured and calibrated up to 100 MHz. The laboratory bench, including the power feed-lines, the ground plane as well as the digital recording technique and subsequent signal processing routines were all verified against an accredited facility. A step-down DC-DC converter was analysed and a simplified model was extracted and compared to measured results. A more comprehensive, and eventually an active model was presented showing the accuracies that can be achieved up to 100 MHz. The PSIM ideal component software was utilised for this exercise, showing that an ideal component modeller can achieve acceptable results more easily and quicker. The SPICE simulator

shows slightly better accuracies, and with comprehensive component libraries and full programming is available for the switching pulse, in particular where rise- and fall times need to be adjusted. Furthermore, the SPICE model can easily be extended to multi-level DC-DC converters due to the programming freedom in the switching signal, as will be shown in a later section.

A good correlation is seen all round between predicted and measured characteristics for the step-down converter. The modelling technique developed can be extended to different converter topologies, including multi-phase, multi-level and combined converters. However during the model experimentation phase, it was found that with larger converters, above the 1 kW power level, the effect of component interaction and power traces plays a larger role due to their increased size and thus increased magnetic field vulnerability at these conducted emission frequencies and hence these effects need to be incorporated in the circuit models. As switching signals and converter complexity increases, the ideal model simulator will not be able to perform well, and a SPICE simulator needs to be utilised.

CHAPTER 6 SIMULATED AND EXPERIMENTAL WORK

6.1 MEASUREMENT PLATFORMS

Two measurement platforms were constructed to analyse conducted emission tests. The discrete step-down DC-DC converter introduced in Chapter 4 as well as a digitally controlled multi-phase surface mount converter. Similar step-up versions were also manufactured. On all units, simulation and measurements were performed.

6.2 SURFACE MOUNT TECHNOLOGIES

A surface mount multiphase step-down DC-DC converter as shown in Figure 6.1 was manufactured to investigate conducted emissions. The microprocessor can be set for single phase and multi-phase, driving the surface mount power converter.

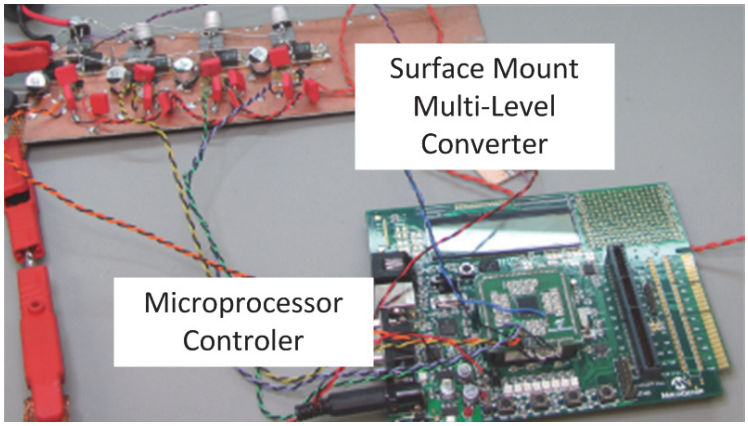
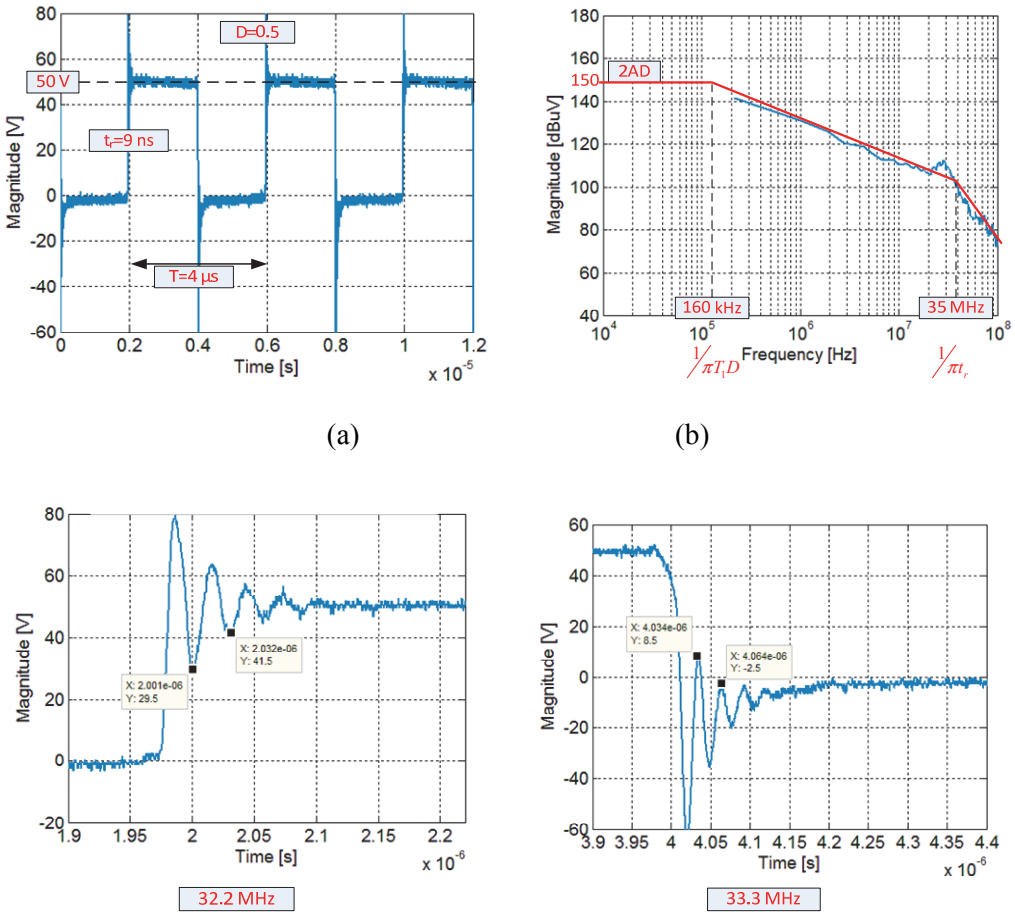


Figure 6.1. Surface mount multi-phase test converter.

The step-down DC-DC converter switching signal alone was analysed to compare the trapezoidal mathematical analysis to practical measurements. Figure 6.2 (a) shows the measured step-down DC-DC converter switching signal at 50 kHz. The duty cycle is set to D=0.5 and the rise- and fall-times about 9 ns. The ringing effect can be clearly seen emerging in the spectral plot at about 35 MHz in Figure 6.2 (b). The rise- and fall times as well as the ringing frequencies for each case are also shown in Figure 6.2 (c) and Figure 6.2 (d) respectively. This corresponds to the analysis performed in section 3.4.2.



(a) (b)

(c) (d)

Figure 6.2. (a) Trapezoidal switching signal, (b) spectral slope, (c) rise- and (d) fall-time ringing signal frequency.

The surface mount circuit is given in Figure 6.3 (a) and the EMC model in Figure 6.3 (b). This model is simulated and compared to measured results.

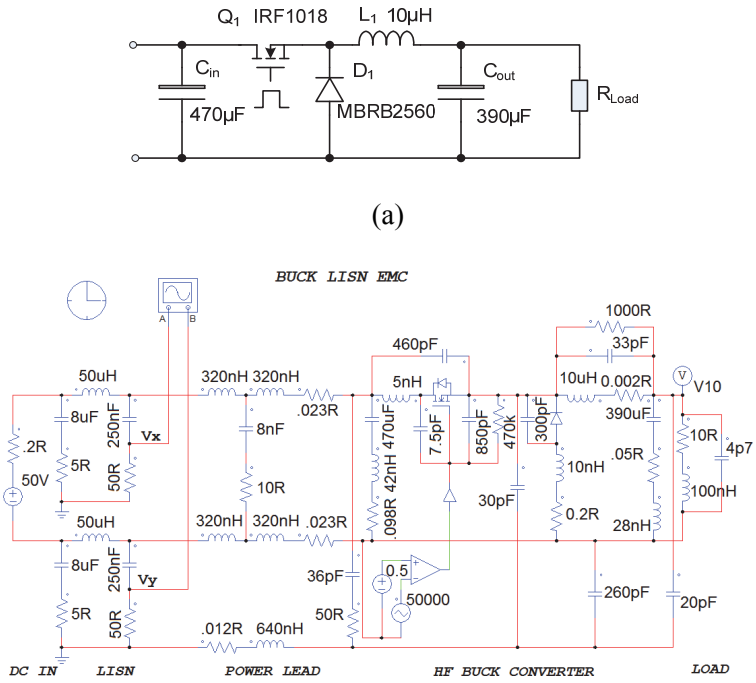


Figure 6.3. (a) Surface mount step-down DC-DC circuit and (b) PSIM EMC model.

The components were modelled as in chapter 3. A single phase step-down surface mount converter is modelled in PSIM and compared to measured results. The V_X port and the V_Y port of the LISN is shown in Figure 6.4 (a) and Figure 6.4 (b) respectively.

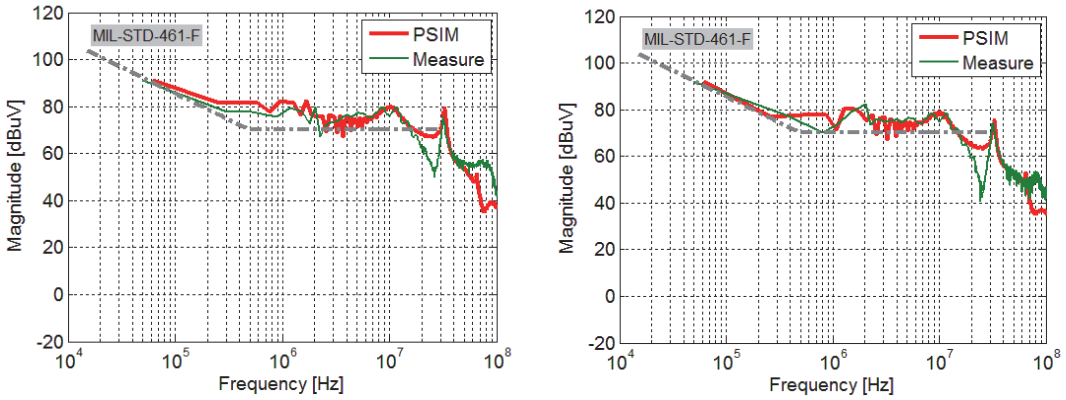


Figure 6.4. Simulated and measured V_X port (a) and V_Y port (b) signal slope.

The rising slope resonant ringing frequency at 32.2 MHz and falling slope frequency at 33.3 MHz are caused, by among others, the capacitance effect of the switching devices. The PSIM model in Figure 6.3 shows capacitances for the MOSFET switch and the freewheel diode close to each other. A similar effect of almost equal ringing frequency will occur when synchronous switching is applied and the two devices are identical. If the two synchronous devices are selected so that the switch capacitance effect is mismatched, the peak frequency is spread and thus a lower peak value can occur.

This peak at just above 30 MHz would not be visible on standard conducted EMC test as this is beyond the normal test frequency. A radiated test was performed to show that the high frequency common-mode peak, as measured with a LISN, shows up in the radiated test. The differential-mode conducted spectrum, on the contrary, had no visible effect on the radiated emissions. A handheld FSH3 Rohde&Schwarz (R&S) spectrum analyser connected to a tuned helical antenna was positioned at a 3 m distance from the LISN and converter test circuit. Substituting into (3-8) the relevant parameters and variables gives a fairly accurate prediction of the common-mode radiated frequency component magnitude prominently visible at 35 MHz. Figure 6.5 shows the radiated results together with the reference noise floor (converter switched off). The common-mode conducted resonance close to 35 MHz shows clearly in the radiated spectrum, with a peak of close to -63 dBm. The noise floor is also shown, due to the fact that the test was not performed in an anechoic chamber.

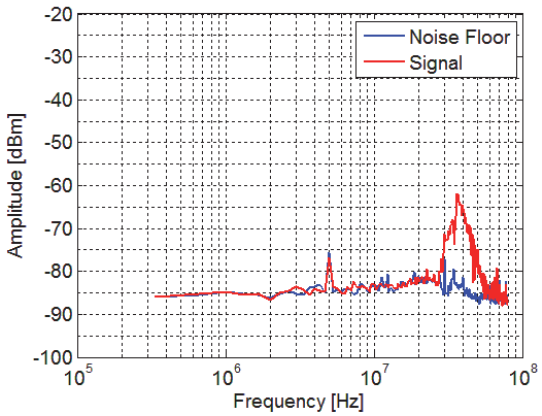


Figure 6.5. Common-mode radiation test.

6.3 COMPONENT PROXIMITY EFFECT

The component proximity effect or component interaction has a more prominent effect at higher switching frequencies or in converters with physically large components. Taking the practical component mounting positions into consideration, the least and most susceptible side of the component can be determined with the Helmholtz test bed as in section 4.3.3 and then marked appropriately. This determines component layout rotation priority. The component placement is then arranged in such a manner that the least affected directions face each other. The ground theory publication on component proximity effects are given in [93].

The discrete step-down DC-DC converter prototype was used to verify the component orientation and enclosure effects on conducted emissions. Figure 6.6 (b) shows the power component placement and the most susceptible component faces indicated by arrows. Figure 6.6 (c) shows the same circuit but with components orientated such that the most susceptible component faces are rotated away from the maximum susceptible edge. An enclosure is added to screen the power feed-line from the step-down converter components.

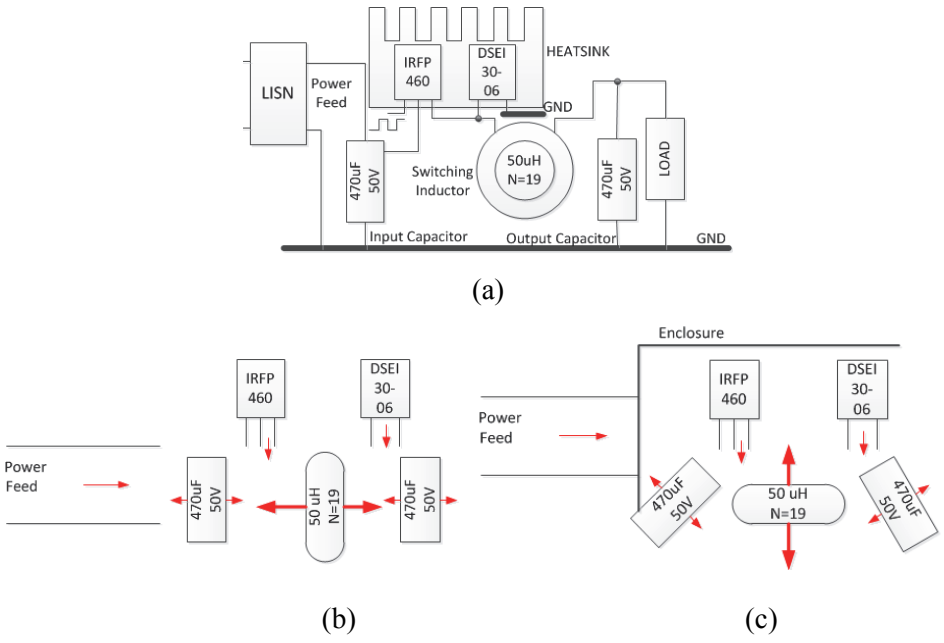
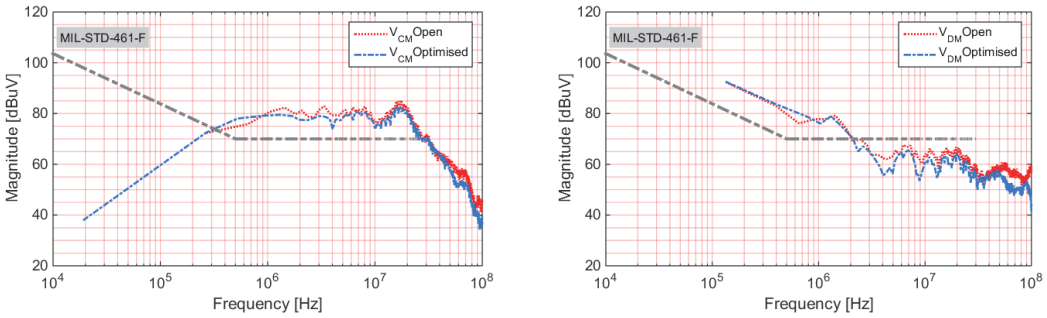


Figure 6.6. Discrete buck converter: (a) Standard component placement, (b) orientation susceptibility vectors and (c) power component placement optimised.

Figure 6.7 show the common-mode and differential-mode plot for the two different layout orientations. The standard open orientation shows a higher noise level in both common-mode and differential-mode plots. The noise level improvement seems to be more prominent at the higher frequency band as this is where component proximity starts having a noticeable effect. In general, an improvement between 3 dB and 9 dB is achieved.



(a) (b)

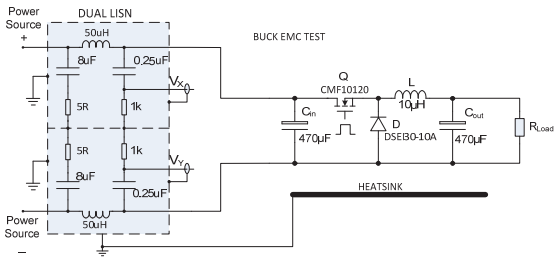
Figure 6.7. (a) CM noise signal and (b) DM noise signal.

A practical procedure has been demonstrated to verify component susceptibility to magnetic fields. The common-mode as well as differential-mode noise plots show a noise improvement of the step-down DC-DC power converter when basic coupling considerations are met.

6.4 DISCRETE POWER CONVERTER TECHNOLOGY

The discrete power converter, in this case a step-down DC-DC converter designed for 200 W, is analysed, shown in Figure 6.8 (a). A SPICE model is constructed for this circuit and it is given in Figure 6.8 (b), showing the LISN, the power line and the converter with parasitic components included. In Figure 6.8 (c) the MOSFET model level 1 SPICE parameters are given and next to it, the diode parameters. The MOSFET drive switching waveform setup is also shown in Figure 6.8 (c), with period 7.6 µs and pulse-width 4.5 µs. The transient analysis simulation SPICE module is enabled, but the circuit will go through a transient mode, until it eventually stabilises to its operational mode. This will take a few analysis cycles, about 6 or more, until the operation data is ready to be captured. The model will create a .TNO file listing time and voltage, for both the V_X port and the V_Y

port. This file is then imported into MATLAB to provide the time signals and calibrated spectral slope plots.



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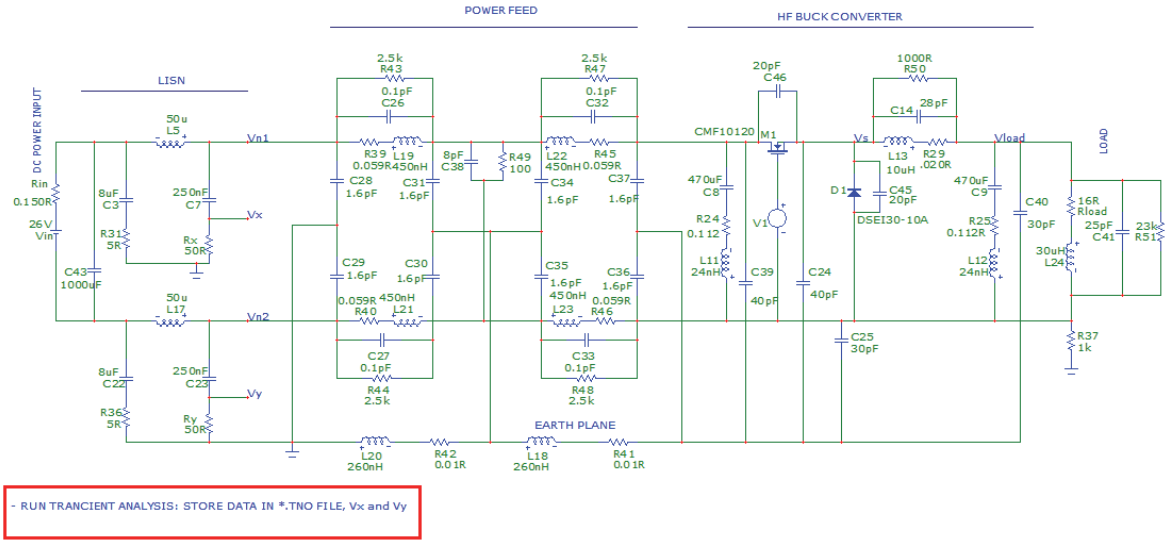

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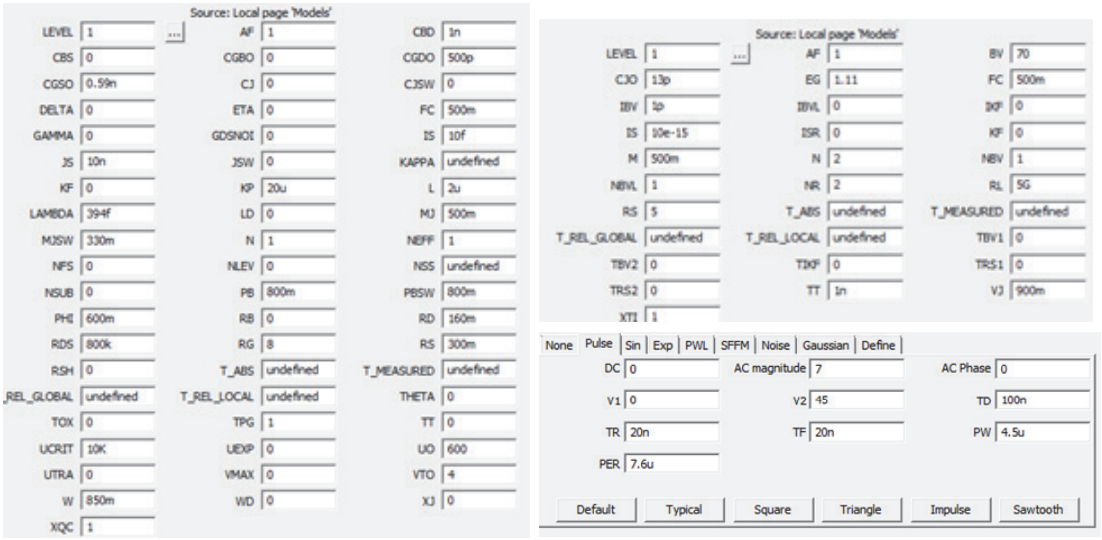
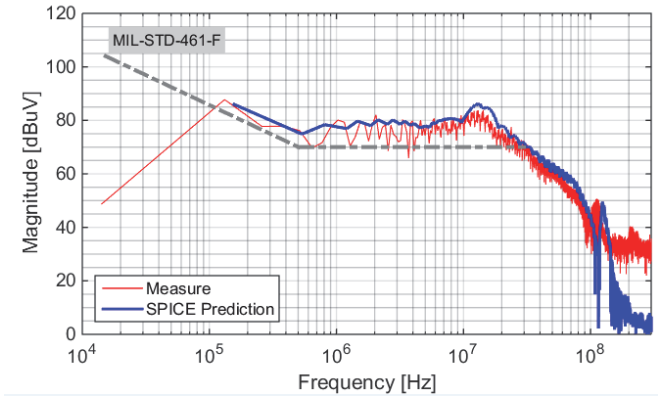


(c)

Figure 6.8. Discrete converter: (a) schematic, (b) SPICE circuit model and (c) MOSFET, diode and pulse parameter settings.

The complete result for the discrete converter and the modelling results are presented in Figure 6.9. The first plot is the V_X port in Figure 6.9 (a). The converter needs to pass this test levels for qualification. Figure 6.9 (b) and Figure 6.9 (c) show the common-mode waveform and the spectral slope measurement as well as model prediction respectively. Good accuracies are achieved. Figure 6.9 (d) and Figure 6.9 (e) shows the differential-mode signal and spectral slope measurement as well as model prediction. It is less accurate than the common-mode slope, especially at the higher frequencies. This is due to a much more complex noise transmission mechanism as with the common-mode case, with currents in the power path and coupling effects need to be dealt with in detail. Overall, accuracies are good enough for analysis purposes as well as for the purpose of optimised filter design.



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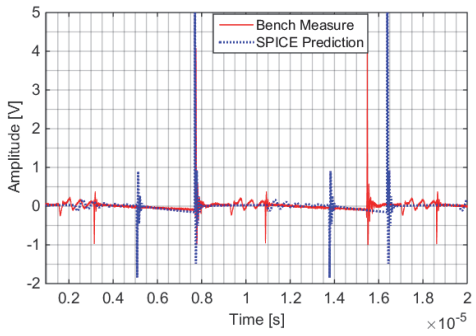

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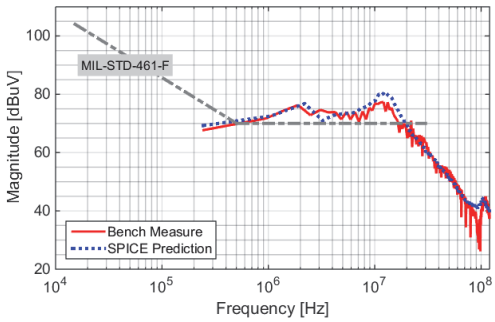

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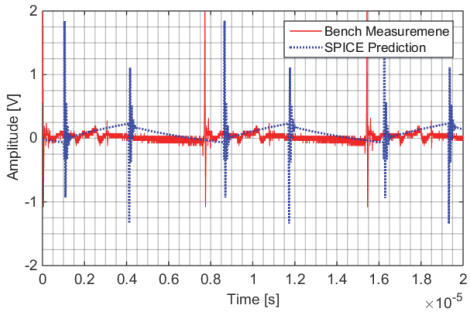

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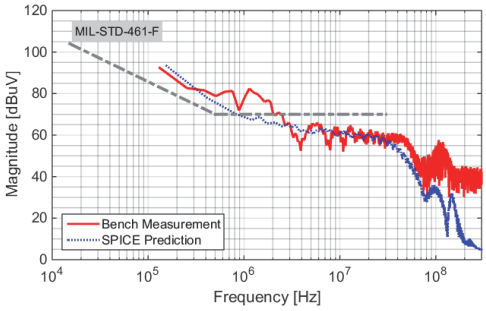


(e)

Figure 6.9. (a) V_X port noise comparison, (b) CM time signals, (c) CM spectral slope (d) DM time signal and (e) DM spectral slope.

Replacing the SER2915 coilcraft inductor with a toriodal inductor lowers the common mode conducted EMC in the upper band as shown in Figure 6.10, due to the dominant larger parasitic components in the toriodal inductor. Similarly, the resonant peak that was prominent just over 100 MHz, moved to a lower frequency, about 70 MHz.

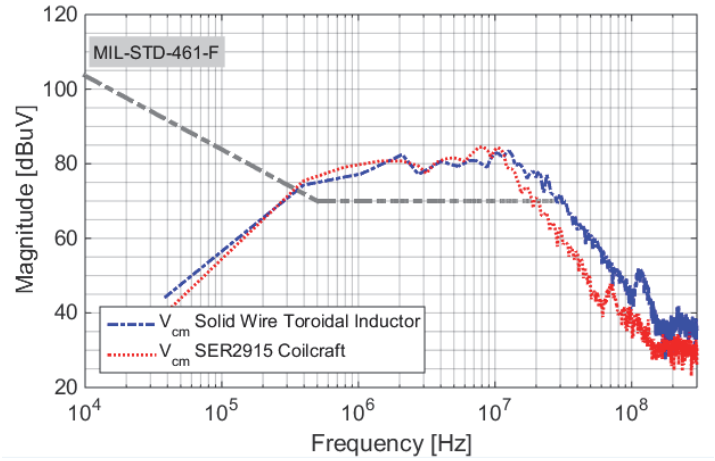


Figure 6.10. CM conducted EMC comparison: Toroidal inductor and SER2915 Coilcraft inductor.

All above tests were performed with a SiC MOSFET, the CFM10120. As this is new technology, it will be interesting to see how the noise spectrum will change when replacing the SiC switch with a standard IRFP460. It is a drop-in replacement and no other changes to the converter are made. A definite increase in common mode noise can be seen, due to the lower c_{iss} and c_{oss} values between the two switches.

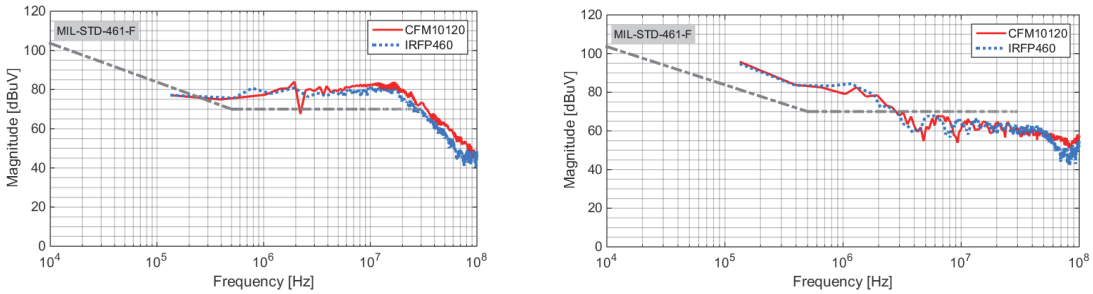


Figure 6.11. (a) CM noise slope and (b) DM noise plot for two different MOSFET technologies.

6.5 REDUCING COMMON-MODE NOISE WITH POLYMER HEATSINK

In section 4.2.14 the heatsink-to-chassis capacitance was modelled with a finite element package COMSOL. As the heatsink capacitance plays an important role in common-mode noise, it is therefore necessary to investigate it further through analysis and experimentation. The thermal image measurements are performed with a Fluke Thermal Imager, model Ti10. For more accurate temperature readings to determine thermal

conductivity, a Fluke 87 with a temperature probe is used. The impedance measurements are performed with an HP4192 LF Impedance Analyser up to 13 MHz and complimented with an HP8753 Network Analyser up to 100 MHz and beyond. Experiments will be performed on a 120 W step-down DC-DC converter tested in a MIL-STD-461F test environment

A variety of plastic heatsink materials were manufactured and tested for heat transfer properties as well as their effects on common-mode noise. Two base materials are selected, EpoxAcast 690 and F19 Urethane Resin. The filler material is fine copper particles, 80 nm to 100 nm in diameter. The variable size is to increase the packaging density of the material. The maximum percentage copper filler mass that could be achieved is 64 % for poly eurethane and 82 % for epoxy. Table 6.1 shows the mixing table for the epoxy and the polymer heatsink blocks. A similar sized aluminium heatsink, composite 6082 alloy, is used as a reference.

Table 6.1 Plastic heatsink mixing table.

Parameter	**EpoxAcast 690 Ref.**	**EpoxAcast 690 Cu Filler 82 %**	**F19 Urethane Resin Ref.**	**F19 Urethane Cu Filler 64 %**
Length [cm]	7.00	7.00	7.00	7.00
Width [cm]	5.95	5.95	5.95	5.95
Thickness [cm] (Average)	0.9	0.9	1.0	0.8
Volume [cm^3]	37.49	37.49	41.65)	33.32
Measured Mass [g]	43.25	232.35	43.65	103.92
Resin Mass [g]	41.23	41.23	43.32	36.65
Resin Density [g/cm^3]	1.10	1.10	1.04	1.04
Filler Mass [g]		191.12		67.27
Filler % (Mass)		82.25		64.73
Copper Density [g/cm3]		8.96		8.96
Mass if Solid Copper [g]		335.86		298.547

The effects of polymer heatsinks on common-mode noise are investigated using a MIL-STD-461F based measurement setup. Also not to be ignored is the important assembly procedure when tightening a device onto the heatsink. A 0.7 N-m torque setting is used on the nylon threaded fastener to guarantee consistency in all measurements carried out. Devices are mounted with a thin layer of white heat-paste. Heat transfer characteristics will

also be measured. COMSOL was used to model the heatsink capacitance (i.e. device tab to earth), the prominent cause of common mode noise in DC-DC converters. The capacitance for a single device, a TO247 package to aluminium heatsink through an insulator was measured to be 39 pF. Referring to Figure 4.47 (a), the MOSFET and diode device pair capacitances are measured and the results shown in Figure 6.12 (a). Measuring both device capacitances to ground gives 80 pF, and a small capacitance contribution between the two devices. The Stainless steel threaded fastener added 2.2 pF to the device-to-ground capacitance. The measured capacitance between the two devices is about 0.7 pF.

The high frequency test setup and impedance plot for all applicable heatsink materials are performed with the impedance analyser and network analyser combined. The test setup is shown in Figure 6.12 (b). It consists of the device, fastened with a nylon threaded fastener to the heatsink and a small ground plane acting as the reference earth. The measurement is taken between the reference earth and the shortened device legs soldered together which in turn is attached to the device tab. The heatsink to be analysed is sandwiched in between.

The results in Figure 6.12 (c) provide information about high frequency resonant effects as well as inductive effects that might occur in the measurement band. A summary of the capacitances C_H and permittivity measured are given in Table 6.2. The inductive resonant effects fall outside the 100 MHz high frequency conducted emission band. Up to 100 MHz, the heatsink impedance is capacitive, and does not need complex equivalent circuitry to model the heatsink effects. The resonant effects beyond 100 MHz are due to the short device leg length and bonding wires as well as the small ground sheet inductance. The polyurethane as well as the epoxy materials shows an increase in capacitance (permittivity) from 2.15 pF to 4.37 pF for polyurethane consisting of 65 % copper powder filler and from 2.93 pF to 7.07 pF for epoxy base material consisting of 82 % copper powder filler. This suggests that it is possible to significantly attenuate the common-mode noise (lowering the device-to-ground capacitance and hence increasing path impedance) using these thermal solutions.

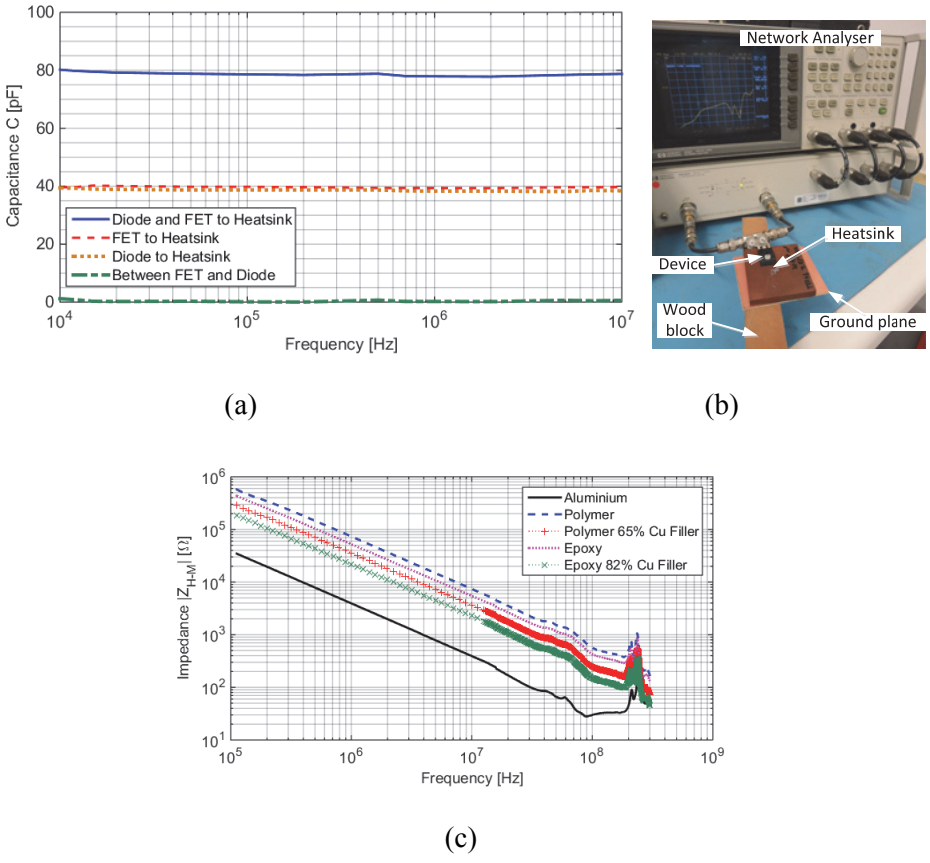


Figure 6.12. (a) Polymer heatsink capacitance, (b) the heat transfer and (c) boron polymer device heatsink test.

Figure 6.13 (a) presents the measured common-mode impedance for both the aluminium and the polymer heatsinks as measured with an impedance meter from the LISN looking towards the step-down converter, with the LISN disconnected. Up to 10 MHz polymer heatsinks show higher impedance, thereafter the impedance is roughly equal. Figure 6.13 (b) shows the V_X LISN port conducted noise spectrum from 10 kHz to 200 MHz. The V_X port noise is a combination of differential- and common-mode noise, and is obtained as:

$$V_X = \frac{V_{DM} + 2V_{CM}}{2} \tag{6.1}$$

In the case of the test step-down converter, the polymer heatsink common-mode noise advantage can be deduced from the port V_X characteristics on the dual LISN between 1 MHz and 30 MHz. Figure 6.13 (c) shows the measured differential-mode noise spectrum, and as predicted from the theory, using polymer heatsinks has no significant effect. The

common-mode noise spectrum, presented in Figure 6.13 (d) shows a good reduction in common-mode noise (10-15 dB) up to 30 MHz. As predicted, beyond 30 MHz the common-mode reduction due to heatsink capacitance to ground has almost no effect as other parasitic effects becomes more prominent. This graph is in good agreement with the theory.

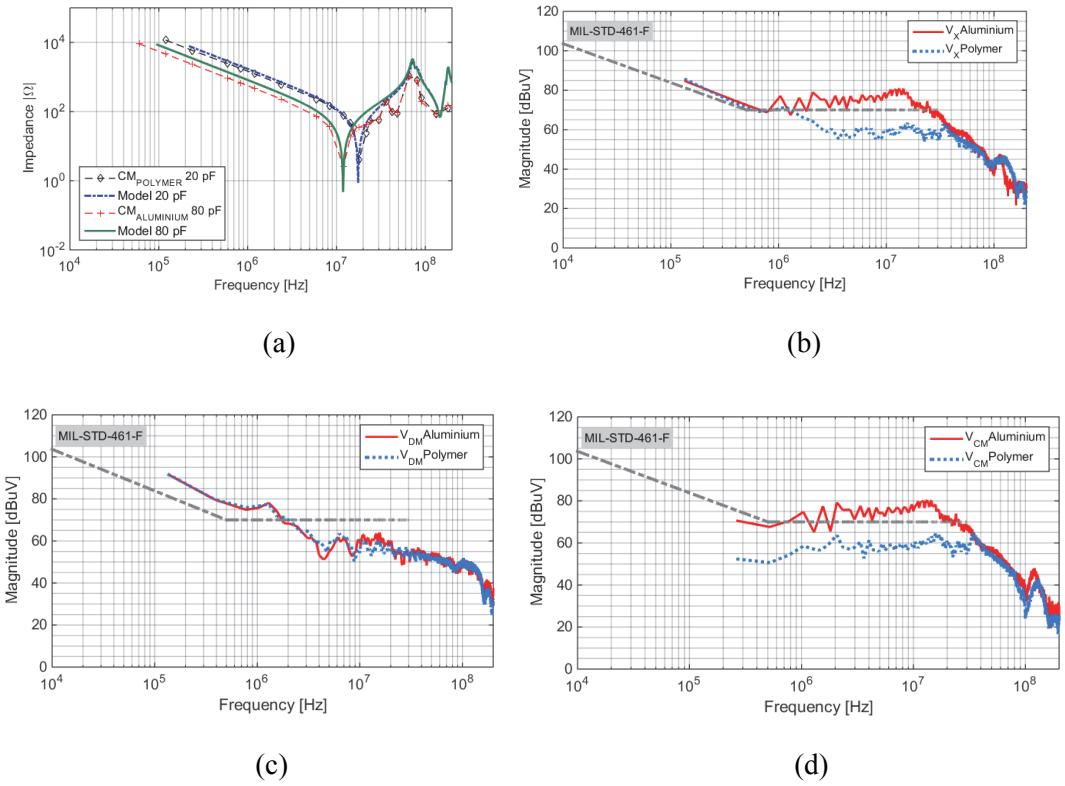


Figure 6.13. (a) CM impedance measurement compared to model, (b) polymer heatsink effect on LISN Vx port, (c) DM noise effect and (d) CM noise reduction.

Figure 6.14 (a) shows the polymer urethane temperature test sets placed on a wooden block. Each device dissipates 1 W corresponding to an output power of 50 W, if switching losses are 2%. All devices tested are mounted with nylon threaded fasteners to the heatsinks as not to influence the capacitance as well as heat distribution readings as would be the case with stainless steel threaded fasteners. The room temperature is 20 ºC and the readings are taken 1 hour after switch-on. Figure 6.14 (b) shows the infrared images of the

urethane tests. Similarly, Figure 6.14 (c) and (d) shows the epoxy test blocks and the infrared images respectively.

Table 6.2 provides a summary of the measured device tab-to-ground capacitances for different materials as well as the measured temperature difference between the ambient and device temperature, against the device dissipating just over 1 W continuously. The Poly-Urethane as well as the Epoxy materials shows an increase in capacitance (permittivity) from 2.1 pF to 4.3 pF and from 2.5 pF to 9.2 pF, when copper powder filler is added. An enhanced heat transfer capability is evident. The boron polymer shows a very good heat transfer capability, and has a fairly low capacitance. The temperature measurements were performed at an ambient temperature of 21 ºC. The results for Aluminium as well as Poly-Urethane are slightly lower than the simulated values, due to natural convection not simulated in the COMSOL model as well as the probe contact thermal resistance not incorporated. Without exception, polymers yield very low capacitances compared to aluminium. This suggests that it is possible to significantly attenuate the common-mode noise (lowering the device-to-ground capacitance and hence increasing path impedance) using these polymer thermal solutions.

The temperature measurements are performed at an ambient temperature of 20 ºC. A T0247 device dissipating 1 W is fastened to the heatsink under test with a nylon threaded fastener. The heatsink is placed on a wooden block, and natural convection takes place. After 1 hour, the temperatures for different materials were measured with an infra-red camera aimed at the top section of the device, close to the die. Table 6.2 provides a summary of the measured temperature on the device, compared to the heatsink capacitances measured previously. The aluminium heatsink has a clear advantage when the temperature increase is considered. The heat transfer coefficient is calculated with the following equation and the results presented in Table 6.2

$$k = \frac{q}{A \cdot \Delta T} \tag{6.2}$$

where k is the heat transfer coefficient [W/m^2-K], q the heat flux or amount of heat transferred [W/m^2], A the heatsink area [m^2] and ΔT the temperature differential between

ambient and the average heatsink temperature [K]. In this case, a higher value of *k* means better performance.

The temperature measurements were performed at an ambient temperature of 20 ºC. A T0247 device dissipating about 1 W is fastened to the heatsink under test with a nylon threaded fastener. The heatsink is placed on a wooden block, and natural convection takes place. After 1 hour, the temperatures for different materials were measured with an infra-red camera. The values are used to give approximate thermal conductivity values for material comparative purposes. Only the aluminium heatsink has an insulator pad. A thin layer of heatsink paste is used in all instances. Table 6.2 provides a summary of the quantitative thermal performance value compared to the heatsink capacitances as measured previously. The aluminium heatsink has a clear thermal performance advantage, but shows a poor capacitance to ground value. Three heatsink temperature readings are taken with a thermocouple and averaged [94]. Populating (6-2) with all known values and heatsink area as $5x10^3$ m^2, provides the thermal conductivity, listed in Table 6.2.

Table 6.2 Heatsink material capacitance and device temperature for single TO-247 device.

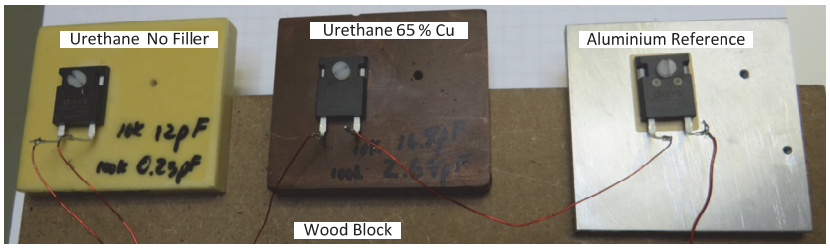
Base Material (10 mm thickness)	***TO-247 Capacitance to GND [pF]***	***Relative Permittivity [F/m]***	***Average case Temperature [K]***	***Average Heatsink Temperature [K]***	***Thermal Conductivity [W/m^2-K]***
Aluminium with silpad insulator	40.0 pF	2.9 (SILPAD)	310.8	305.5	30.6
Poly-urethane base, no filler	2.15 pF	2.7	328.8	299.0	13.1
Poly-Urethane, 65% Cu powder	4.37 pF	5.4	321.8	302.2	16.5
Epoxy base, no filler	2.93 pF	3.61	327.8	299.2	12.7
Epoxy, 82% Cu powder	7.07 pF	8.73	315.4	304.0	21.2

The downside to polymer heatsinks managing heat transfer is that due to lower thermal performance [67], higher device temperatures need to be tolerated. The thermal conductivity of aluminium was measured at 30.6 W/m^2K, close to the value as measured in [73]. The bare polyurethane and epoxy heatsinks show a thermal conductivity of 3 times

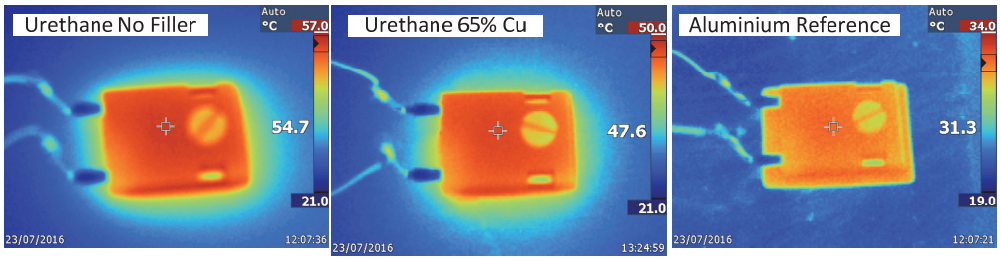
that of aluminium, but adding heat conductive filler, such as fine copper powder, reduced the heat conductivity to less than 2 times compared to aluminium. Approximately 284 K difference in temperature is observed when comparing measurements of an aluminium heatsink with those of a similar sized epoxy composite heatsink at just over 1 W device dissipation, as shown with the thermal camera in Figure 6.14 (a) - (d). This result compares well with the COMSOL model in Figure 4.50 (a) and (b), where a 60 % sandwiched copper filler model raised the die temperature to 316.5 K. Figure 6.14 (b) shows the polymer heatsink temperature effect with no filler material, raising the temperature to 327.8 K, much lower than the simulated temperature due to measurements performed on the casing instead of the die.

Extrapolating the temperature values to represent a converter delivering 120 W using the thermal conductivity readings in Table 6.2, and switching losses at 98 % with about 2x2.4 W device losses to be dissipated by the heatsink (the diode and the MOSFET), the aluminium block will have an expected device temperature of 349 K. Replacing with an epoxy block having 82 % copper powder filler, this temperature will rise to 376 K. This is still within the operating temperature of the silicon devices.

However, with higher junction-temperature devices becoming more readily available, this should not be a serious concern in the near future. For example, the SiC platform can operate at higher junction temperatures (600 K) as compared to traditional Si-based technologies [74]. In Figure 6.15 an example of a converter product employing polymer materials and utilised in a military environment is shown. It is a 60 W ruggedised IP68 solar panel switch-mode regulator encapsulated by a heat conductive injection moulded polymer, which passed the stringent MIL-STD-461F conducted emission tests as well as military shock, vibration, drop and temperature variation tests.



(a)



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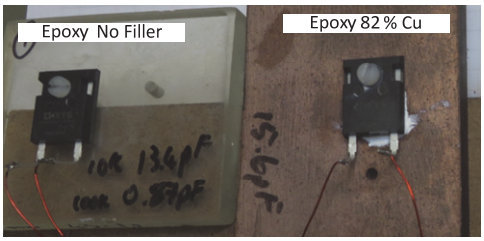
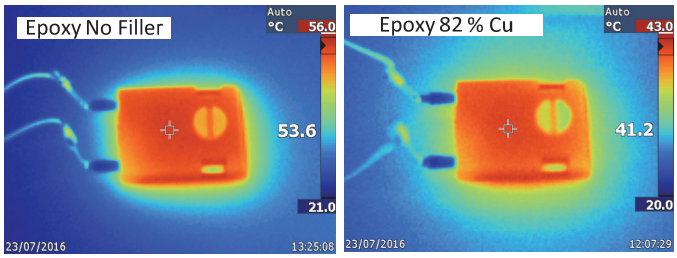


(c)



(d)

Figure 6.14. (a) Polymer urethane heatsinks and aluminium reference test, (b) urethane infrared images, (c) epoxy heatsink test and (d) infrared images.

Figure 6.15. Thermal polymer packaged product.

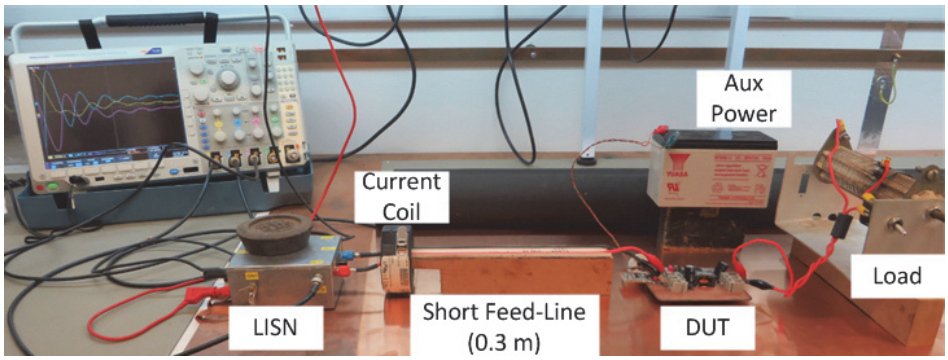
To conclude, the theoretical analysis section the EMC setup as well as common-mode and differential-mode noise was defined. A simplified EMC conducted noise model showed the noise mechanism due to heatsink capacitance and the interaction with the rest of the converter and the conducted noise setup. Transfer functions were extracted to show the dominant noise path versus frequency and showed that beyond 30 MHz the heatsink capacitance effect is no longer prominent and is surpassed by the converter power lead and the PCB impedances respectively. Thereafter the heatsink capacitance was defined, and accurately modelled, showing the effects fasteners and enclosures might have on this capacitance. Polymer materials and composites were introduced showing the capacitance advantage in common-mode noise. An interesting conclusion from modelling the heatsink capacitance and determining the effect thereof, showed that decreasing the inductances associated with the heatsink capacitances, L_{GND} and L_{PCB}, reduces the high frequency common mode noise (see Figure 4.46). The heat spreading properties are also modelled. Polyurethane and epoxy base materials as well as fine copper powder filler composites are manufactured and compared to a similar sized aluminium heatsink. The experiments validate the theory, verifying capacitances, the common-mode impedance, as well as differential and common-mode plots up to 100 MHz. Thermal measurements and the thermal conductivity of the different heatsink materials were presented.

The manufacturing advantage of polymer heatsinks is quite vast, it enables more design freedom, it is lighter, lower thermal expansion, high breakdown voltages and less expensive to manufacture compared to aluminium heatsinks. Forming aluminium heatsinks are in certain applications being machined from a solid aluminium billet with a CNC milling machine, but the polymer heatsinks require the manufacture of a once-off mould

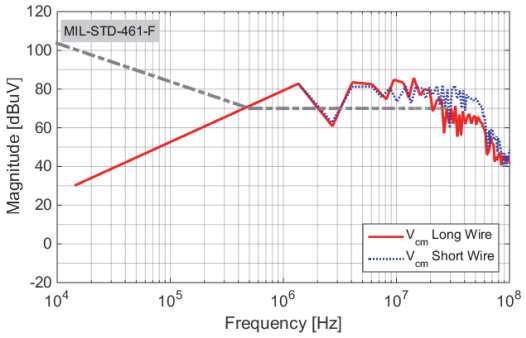
and thereafter heatsink cost turns out much lower, even for complex forms. Comparing aluminium to the polymer and epoxy thermal conductivity, it is about 3 times higher, but adding a heat conductive powder improved the thermal conductivity to less than 2 times compared to aluminium, making it viable for heatsink applications. Furthermore, careful design of the junction temperatures need to be performed, indicating that polymer heatsinks are, for the time being, more suited for lower power converters of less than 120 W. It was noted that future commercial SiC MOSFET devices might tolerate a significant high reliable operating junction temperature, making these devices possible candidates for polymer heatsink applications in transportation power electronic devices where weight as well as cost is important, although care should be taken with too high junction temperatures. It can also be considered in highly corrosive environments such as in sea water and it was shown to be well applied in robust outdoor applications.

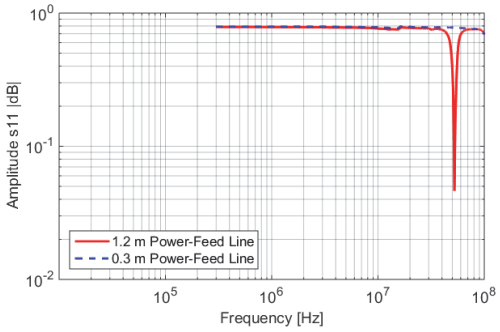
6.6 SHORTER FEED-LINE EFFECT

A shorter power feed-line can be incorporated in the measurement bench setup as shown in Figure 6.16 (a). Figure 6.16 (b) shows the result for common-mode conducted emission for two conditions, the 1.2 m power feed-line presented in the solid trace and the shorter 30 cm power feed-line. As expected, around 60 MHz, higher common-mode amplitudes are measured for the shorter power feed-line. Figure 6.16 (c) shows the power feed-line over ground plane scattering parameter reflection coefficient s11, and confirms attenuating and radiating effects occurring around 50 MHz. The power line in effect acts like a filter at that frequency, showing a lower common mode conducted signal for the 1.2 m power feed-line, but aggravating radiating effects at that frequency. Figure 6.16 (d) confirms the radiating effects on the 1.2 m power feed-line, measured at a distance of 3 m from the bench setup with an un-calibrated antenna, recorded with a Rohde&Schwarz FSH3 spectrum analyser. The 0.3 m power feed-line shows no radiating effects up to 100 MHz.



(a)





(b) (c)

Figure 6.16. (a) bench Setup with 0.3 m power feed-line, (b), shorter power feed-line CM effect and (c) scattering parameter s11.

6.7 MULTIPHASE ANALYSIS

The SPICE model in Figure 6.8 is extended to model multi-phase conversion based on the step-down DC-DC converter. The phase configuration is shown in Figure 6.17. The periods are set-up in an 8 µs duty cycles, on-time 5.4 µs and off-time 2.4 µs.

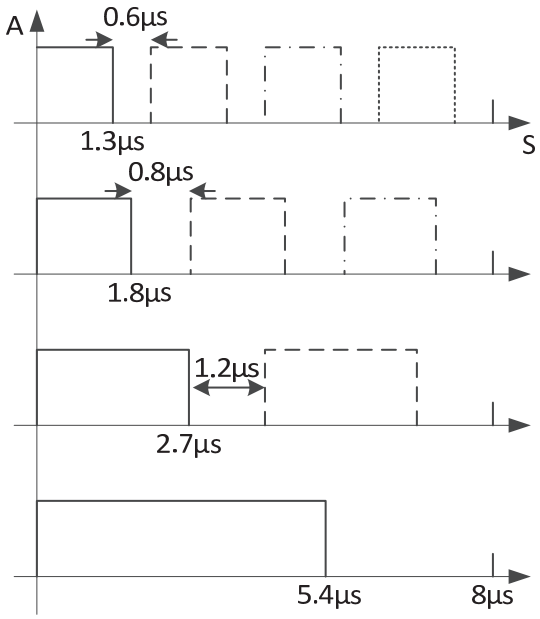
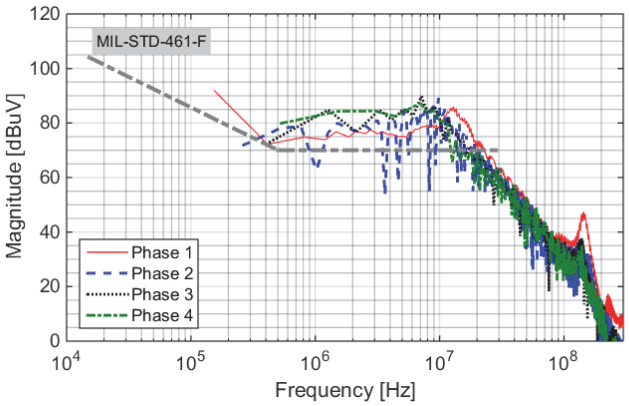
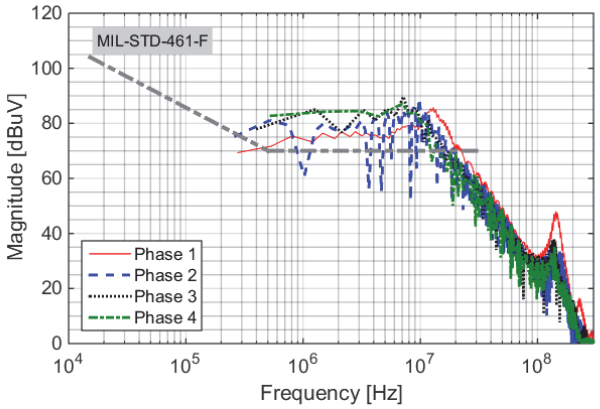


Figure 6.17. Phase configuration.

The results for the multi-phase noise plots are shown in Figure 6.18 (a), the V_X port noise, Figure 6.18 (b) the common-mode noise and Figure 6.18 (c) the differential mode noise. In all cases, the high frequency at around and over 100 MHz (un-calibrated but for reference purposes) shows a reduction in noise amplitude. The lower frequencies, below 10 MHz, show an increase in the V_X port noise as well as in common-mode noise. This is expected due to the heatsink capacitances more dominant, playing a dominant effect in that region for common-mode noise. The differential-mode noise is unaffected by the heatsink capacitance, thus showing an all-round decrease in the amplitude noise spectrum. Similarly, in [32], multi-level topologies showed a conducted emission noise reduction, also shown in the differential-mode as well as common-mode noise plots, up to 3 levels.



(a)



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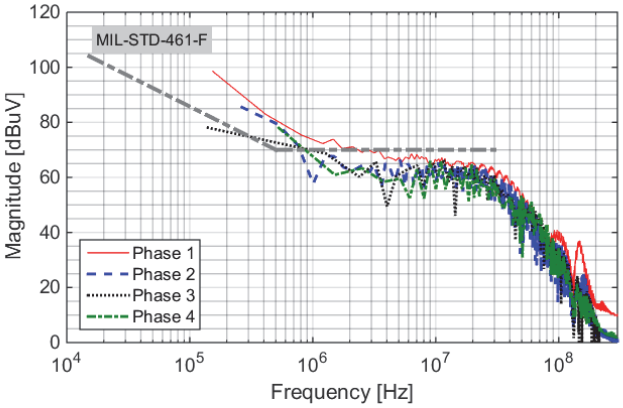

(c)

Figure 6.18. Multi-phase step-down DC-DC converter: (a) V_X port noise, (b) common-mode noise and (c) differential-mode noise.

6.8 CHAPTER SUMMARY

In this chapter highlights of experimental work carried out, was presented. The microprocessor controlled surface mount step-down converter was modelled and the results compared to measurements. The smaller components with less complex parasitic effects as compared to larger structures were modelled in PSIM and the results compared well with measured results. In this converter, a resonant peak formed just outside the official conducted emission band, and is clearly visible in the frequency extended conducted emission band. This resonance was also shown to have formed radiated effects, showing that the frequency extended conducted emission test can predict radiated problems starting to emerge. With the same circuit, a multi-phase converter was realised and it was seen that up to 3-levels an advantage in conducted emission levels is visible; thereafter no further improvement was seen.

A discrete converter was assembled testing the larger component effects. The proximity effects were investigated and a technique tested to find the susceptibility vector, the most vulnerable orientation of the component. By re-orientating the components as to have the least effect on each other, a slight improvement in conducted emissions was seen, mostly prominent at high frequencies due to the smaller parasitic values encountered.

The effect of polymer heatsinks on common-mode noise was investigated due to the marketplace starting to implement polymer heatsinks in smaller converter applications. A large reduction was seen in the lower frequency band, but at the high frequencies, the positive effect was much smaller, due to other resonant components becoming more prominent. Due to the smaller heat capacity of polymer composite heatsinks, the power limit for these converters are around 120 W.

The multi-phase converter has been analysed. It was shown that overall, the reduction in noise is only visible in the top frequency range, but lower down common mode increases. Differential mode noise shows a decrease from 1-phase to 2-phase, but 3-phases or more no reduction in spectral amplitude takes place.

CHAPTER 7 DISCUSSION AND CONCLUSION

An accurate high frequency modelling technique was developed with the aid of PowerSim as well as SPICE circuit analysis software to design for conducted EMC up to 100 MHz. The high frequency impedances of the power elements were obtained through impedance measurement and modelled as circuit elements. A combined high frequency circuit was then developed. The circuit is modelled in its active state, driving the MOSFET with the proper drive signals. The converter model operates as intended. Simulation results were compared with measured data. Active circuit models performed well on the high frequency switched circuit model and provided results comparable to the bench measurements and in turn accredited measurements. Due to the good correlation between the circuit model and the practical measurements, the model can be utilized to investigate the main contributing factors of conducted EMI as well as experimenting on different component solutions.

Measuring the common mode noise up to 100 MHz some basic high frequency noise principles need to be adhered to. The oscilloscope inputs need to be terminated to 50 Ω, and spare channels cannot be used to measure other circuit parameters, as the ground clip of the probe will create a different noise path to the oscilloscope, creating erratic measurements. Similarly, using for example a bench signal generator as input to the MOSFET gate diver, to drive the MOSFET pulses, the grounding of the signal generator cannot be the same as the measuring instrument. It needs to be isolated and if possible, long cables must be suspended as not to return noise to the bench. If the auxiliary supply of the converter under development is a bench supply, similar care needs to be taken. Even using a battery for an auxiliary supply, it is fully isolated, but it can form a good noise path to the bench, and need to be suspended as not to influence the measurement. The load is part of the test and need to be modelled and taken into account, but if the load is positioned right on top of the measurement bench it will influence the measurement. It is good practice to suspend the load on wooden blocks, moving it away from the bench, and even screening the load is advisable.

In accredited measurements, the feed cable from the LISN to the device under test is a loose cable, suspended on wooden blocks and in many cases fastened with Velcro. This created slightly different noise slopes every time a setup is performed. For high frequency conducted measurements it will be good practice to fix the power line on a wooden structure at the prescribed height from the table as well as the spacing between the wires constant at all times. This will ensure repetitive measurements and additionally, make the power feed-line easier to characterise.

The SPICE circuit simulator consists of component libraries, most of the popular MOSFETS and diodes used for power applications. Replacing the circuit model with different types and manufacturers of power components, the effect of different components on the conducted emissions can quickly be verified, even before purchasing components for the prototype circuit. Replacing the MOSFETS and running the simulation will show a vast difference in the conducted noise slopes, such as the SiC types, and will emit more high frequency noise as for example compared to the standard IRF-series silicon MOSFETS. Even selecting for example free-wheel diodes, it was seen that when the parasitic parameters compares to the applicable switching MOSFET, these two components contributes to a resonant peak. Changing to a different free-wheel diode reduces the resonant peak, and two smaller resonant peaks are visible.

A conducted EMC bench measurement setup was manufactured, utilising the manufactured high frequency LISN and a digital oscilloscope. Extracting the data from the oscilloscope, it was further analysed on a PC, in MATLAB or MathCad, to provide the spectral noise slopes as well as noise modes. This laboratory setup was calibrated and the measured noise slopes compares to calibrated accredited conducted noise measurements. Thus, this bench can be utilised as a pre-compliance test in the laboratory, ensuring that the power unit will pass the accredited conducted EMC tests. Although the bench is designed around the MIL-STD-461 standard, the same LISN and bench can be used for the CISPR test. In this case, the unit under test has to be suspended above the ground plane as not to be influenced by it. A wire ground is then used instead, returning common mode noise to the LISN. This test bench is a fixture in the laboratory and is currently used as a pre-compliance test station verifying that the power converter that has been developed will

pass the conducted EMC tests when submitted for accreditation. The test bench is also extremely handy in verifying the conducted EMC during the design phase of the product. Early in the product design, conducted EMC problems can be sorted out. This is a much easier way and cost-effective option opposed to changing a design later on should conducted EMC problems arise while the product is submitted for EMC accreditation. The calibrated EMC test bench is a well-used asset in the laboratory, and was very cost-effective to manufacture.

The digital recording of the noise measurement and the subsequent signal processing to create the calibrated conducted noise slopes was tested against the cumbersome EMC spectrum analyser measurement technique that can take several hours. Normally a quick spectrum analyser scan is performed and if possible problem areas are seen, a proper scan around that area will be performed, saving some time. The digital recording and signal processing technique is much quicker and it provides the same results. It was later seen that many publications were written on digital EMC recording and is used with great success; although the accredited EMC laboratories still use the EMC spectrum analyser technique in accordance with the standards.

On both the model and the practical experimentation, common-mode and differential-mode noises were extracted with two different techniques. One of the techniques used the LISN voltages from which the CM and DM signals were calculated. The second technique used direct measurement with a high frequency LINDGREN EMC current probe. Both techniques yielded similar results. The LINDGREN EMC current probe is a specialised measuring tool and not readily available in a power development laboratory. Extracting the common-mode and differential-mode noise from the LISN ports is convenient way to extract the noise modes for filter design applications. Normally, the noise splitting is performed by complex RF circuitry, and from literature, not very accurate. With this noise splitting technique, the set of equations describing the noise as deducted from the LISN ports, cannot be accurately verified. The widely adopted mathematical analysis method for separating the common-mode and differential-mode noise signals from the LISN ports came in for scrutiny. This was after it was found that a 6 dB magnitude difference existed between the analytical measurements obtained, mostly on the differential-mode equation.

These equations are widely accepted in the literature and the verified experimental measurements as well as with the simulated results. A set of equations to separate common-mode and differential-mode noise signals was derived from first principles and their accuracy verified. This led to analytical, simulated and experimental results being in very good agreement. In literature though, these equations are not well defined and used lightly, mostly referencing from untested sources.

It was also shown that a common-mode current of about 5 μA and greater can cause a device under test to fail the general EMC limits in both conducted and radiated scenarios. Furthermore, it was demonstrated that high frequency common-mode conducted noise shows up as radiation effects when operating at high switching frequencies due to the relatively large common-mode current loop effects. Recording conducted noise up to 100 MHz is an easier test to perform than a radiated test.

The modelling method that was developed can be extended to different converter topologies, including multi-phase, multilevel and combined converters. As the simulation results were adequately validated, one can have a high degree of confidence that the modelling and simulation process will lead to an accurate EMC design process. Moreover, the same simulation package can be used to assist in the converter design itself, taking into account the high frequency parasitic effects. At first, simulations were performed with PSIM, an ideal component simulator. Good results were achieved on simple circuits, but for more complex circuitry a SPICE simulator such as Micro-Cap, can be a very good conducted EMC simulation tool. The SPICE model for the step-down converter took some time to give accurate results, but once the setup and the link to MATLAB is setup, it worked very well. The active SPICE simulation will take a few minutes to complete, as it needs to get beyond the transient start-up before the model LISN waveforms can be recorded. Once recorded, the MATLAB program will grab the generated .TNO file and due to large files and multiple fft's to perform, will take less than a minute to present applicable graphs, the LISN V_X port, the V_Y port, common mode as well as differential mode plots in time- and frequency domains. The spectral plot can be presented as a peak-hold function, showing only the spectral slope of concern, making the spectral graphs easier to read.

Effects of multilevel, multiphase and synchronous converters on common-mode noise were also investigated. It was demonstrated that reducing common-mode noise levels can be achieved by using different techniques. Multi-level topologies showed a general conducted high frequency noise reduction up to 3 levels, mostly in differential mode. Common mode showed an increase in noise levels, due to the heatsink capacitance effect. Changing the converter topology to a multi-phase or multi-level converter to reduce conducted EMC might not be worth the while, but in all cases, the noise around and above 100 MHz decreased. If this is an important objective, then multi-phase converters can be considered if noise is the only reason.

The advantage of using electrically insulated heat conductive polymer heatsinks on common-mode currents was also investigated and very promising results obtained. It was demonstrated that the common-mode capacitance due to the switching devices can be vastly reduced by replacing aluminium with non-conductive polymer heatsinks. This has the potential of being a viable and very effective solution to reduce the increased conducted common-mode noise levels due to higher switching frequencies. Additionally, a number of manufacturing advantages are achieved as well. Surprisingly, it was shown that, at the very high end, above 50 MHz (out of the traditional conducted frequency band), the heatsink capacitance has a lesser influence on common-mode noise. Similarly, replacing stainless steel threaded fasteners that normally hold the devices onto the heatsink, with nylon fasteners reduced the common mode effect in the traditional measurement frequency band. Even replacing the fastener with a spring loaded clamp reduces the heatsink capacitance slightly.

Component proximity effects were investigated. A technique was developed, using a Helmholtz coil, so that the components susceptibility vectors can be calculated. This is rotating the component in the generated field and measuring the angle of susceptibility on the component over the frequency range. The readings are referenced to a single loop calibrator, showing the least- and most vulnerable angles of the component. Using this information, the component placement is done so as to have the least effect on each other, that is the lower values of the susceptibility vectors on the component faces each other, thus ensuring the least proximity effects. A few dB's reduction in noise were seen when

this technique was used. Similarly, when packing sensitive components in an enclosure, such as open magnetic inductors, it was shown that the most vulnerable position for such a component is in the middle of the enclosure due to outside radiation effects.

CHAPTER 8 SUGGESTION FOR FUTURE WORK

It was shown that a parasitic lumped element analytical model can provide accurate common-mode simulated results. In smaller converters and surface mount applications, the modelling technique works well. Larger discrete converters, component interaction start playing a vital role. More care is needed when modelling large scale converters (kW range).

It would be advantageous to compile a software package dedicated to conducted EMC design opposed as described in this thesis, as switching between various packages to perform certain tasks can be time consuming. Furthermore, shortcomings encountered can be addressed, for instance slope compensation on PSIM is difficult to control, but simulation times vs. complexity are very favourable. A SPICE package, such as Micro-Cap from Spectrum Software, can easily handle slope compensation and complex multi-phase converters have been modelled successfully with this software.

The conducted EMC modelling technique can be further extended to compare different topologies, even complex ones, for optimal noise levels. Component selection can easily be verified for optimum noise levels. Modelling multiple converters in a system will also be possible by adding the converters to the model, similar to the multi-phase concept.

Component proximity will remain a difficult topic, and modelling the effects with a finite element package such as COMSOL Multiphysics is time consuming, but very effective. It can be extremely useful if EMC proximity templates can be created so any power design engineer can with minimal training, properly populate power circuits effectively with minimal proximity influences.

The initial goal was to do conducted emissions up to 100 MHz. During the simulation and verification process, it was achieved. Nevertheless, it was found that modelling and measurement can be performed up to 300 MHz with the equipment and processes used.

The LISN will be the limitation, but replacing the LISN with a 300 MHz Coupling/Decoupling Network (CDN) according to the IEC61000-4-6 (as well as CISPR 15) standards, conducted emissions can be performed covering the VHF frequency band. Then, measuring conducted emissions can show radiated effects as well, as most power converters, due to relatively low frequency switching signals, do not as a rule emit large noise components beyond 300 MHz.

Future studies extending from the present baseline on conducted EMC can include the following:

- Injected EMI, emanating from external sources, propagating over mains networks or from other converter sources is an important aspect in a power network. These secondary disturbances can be seen as harmonic sources of current and voltage impacting on the primary converter. This puts a new constraint on the modern power network design where an increase number of power electronic converters in close proximity become more crucial. Study trends are focused on reducing the EMI at the source stage. This cannot be accomplished without performing formal analytical models of the network, including the converters and cables. This allows researchers to provide a better understanding of the parameter impact on the EMI noise, opposed to empirical models, which are limited to only show final results rather than revealing the EMI mechanism. Analytical models guide engineers to solve EMI problems without elaborate EMI tests. It is thus proposed to analyse the global network's EMC behaviour and contribute to reduce margin in filter design stages, with developing formal analytical models of the network, based on modelling switching impedance and harmonic sources of the converters.
- Class-D amplifiers are a widespread industrial solution. These amplifiers have a similar architecture of a buck converter but having the audio signal as reference. The switching nature of these devices allows users to increase significantly the power efficiency compared to linear audio amplifiers without reducing the audio quality. However, because of the switching behaviour, Class-D amplifiers have high levels of electromagnetic (EM) emissions which can disturb the surrounding electronics or might not comply with electromagnetic compatibility (EMC)

standards. To overcome this problem much architecture appeared in the state of the art that reduces the emissions, however, this has never been enough to remove electromagnetic interference. It is then useful to design optimal EMI filters for Class-D amplifiers. This will improve the EMI response, reducing additional power losses and to evaluate impact on the audio quality.

- It is now possible to predict the EMC compliance with Electromagnetic standards as well as accurately computing a common and differential mode conducted noise. At present, the modern car power networks supplying large quantities of electrical actuators necessitating many power converters to manage the power transfer efficiently. However using long harnesses creates new issues due to interaction between cable and converter's noise sources, and therefore the EMC study becomes more complex. Proposing an analytical model to compute common mode equivalent conducted noise sources along the network, can minimise and optimise the cable network. The model can be tested with time domain simulations and validated by experimental measurements.
- EMI modelling of power converters is crucial to develop EMI attenuation solutions. Recently, more and more modelling and mathematical analysis of electromagnetic interference sources and propagation path had allowed a better understanding of the EMI generation mechanisms. Calculation times and accuracy determine the efficiency of EMI models in the studied circuit frequency range. It is thus proposed to develop a circuit-based model for predicting the spectra of conducted interferences in a DC-DC converter in the scope of reducing calculation times of sequential simulations. The proposed new approach for high-frequency disturbance estimation can be based on the knowledge of circuit parasitic elements and semiconductor devices parameters. A good trade-off between simulation time and accuracy can be registered; making the EMC modelling process attractive for power converter designers.

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Appendix A EMC REGULATION

A.1 PURPOSE

It is important to know the noise level to design for, to be able to accurately filter the excessive noise. If a power system is cost sensitive and size matters, overdesigning for the lowest possible emission levels will increase cost and most probably size. On the other hand, failing the emission standards can be catastrophic.

Modelling for EMC in any power converter is of utmost importance and should be part of the design phase. Due to the switching operation, physical placement and structural limitations, conducted noise will be generated. Designing EMC friendly switch-mode topologies and eventually optimum sized filters to quench certain frequencies, if needed, improves the overall cost effectiveness.

A.2 BACKGROUND

The general definition for conducted emissions as stated from the IEEE EMC Society is that conducted emissions are currents that travel on circuit wiring or conductive portions of assemblies and structures. It can occur on power and/or signal wires.

This report starts with the diverse conducted emission accreditations available for the different end-users and destinations. For instance, the military specification is more stringent in certain aspects as it measures the peak disturbance opposed to the quasi peak or average disturbance for commercial accreditation. If a soldier transmit the voice command ‘don’t shoot!’ and a momentarily disturbance wipes out the ‘don’t’ the faulty message can have major consequences. On the other hand, if listening to music from the commercial FM radio and the air conditioner motor starts up causing a few tics on the radio and blobs out a word or two, it will just be a short frustration with no serious consequences. A weighted quasi-peak level for the occasional flicker noise is thus acceptable.

Conducted emissions are important as it can be easier identified and corrected compared to the more complicated path of radiated emissions [A1]. Depending on wiring length and frequency of conducted disturbance currents, it may result in radiated emissions. Paying attention to conducted emissions can eventually prevent additional compliance issues. Conducted emissions compliance testing involves the use of a Line Impedance Stabilising Network (LISN). It is the standard prescribed means of powering the device for testing and it provides a port for measuring the conducted noise levels.

The regulating bodies set forth by law requirements to regulate power devices. It is worth noting that individual companies self-impose their own set of regulations on their products and could be much more stringent than the required regulations. This is mostly seen in the automobile manufacturing environment where competition is very tight.

A.3 CONDUCTED EMC STANDARDS

A.3.1 Standards background

The EMC conducted emission standards are there to define: "the ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment". It is thus about limiting the EM pollution by defining limits to the emitted conducted power of any electrically operated piece of equipment.

The term conducted emissions refer to the mechanism that enables electromagnetic energy to be created in an electronic device and coupled to its input power cord. Regulatory agencies control the radiated emissions (not covered in this document) and conducted emissions from electronic devices.

Cables connected to a device carry unwanted transient signals and other disturbances to other devices. [A1]. The conducted emissions are measured with voltage and current measurements on the cables. Such measurement methods are standardised, for instance, for automotive appliances in CISPR25 [A2]. The voltage measurement method measures the

conducted emissions only between the power lines and a ground cable with a LISN (Line Interface Stabilisation Network), or sometimes called an Artificial Network (AN). DC converters without a safety ground (for example two-wire DC-DC supplies housed in isolated casings) use the negative (zero volt line) as the ground reference. The LISN should only be used on the high-side of the power line [A2].

All radiated and conducted emission measurement methods have different measurement sensitivities for different emission frequency ranges and different emission coupling mechanisms. This is the main reason for the application of different methods for device EMC compliance measurements.

A.3.2 Regulating bodies overview

Technical Committee 77 (TC 77) and CISPR (Special International Committee on Radio Interference) are technical commitees having responsibility for developing emission limits and measurement requirements to achieve EMC. Generally, CISPR is responsible for emissions above 9 kHz and TC 77 for emissions below 9 kHz [A3].

In South Africa, the SABS (South African Bureau of Standards) maintains the standards pertaining to EMC. The national standards have been adopted and re-designated as SANS (South African National Standard). The SANS EMC standards deal with unintentional emissions from any electrical or electronic apparatus. The technical committee within Standards South Africa that deals with EMC is TC 73, heavily influenced by the IEC and its two EMC bodies, TC 77 and CISPR. The standard for radio interference characteristics of information technology equipment is for example SANS CISPR 22 (1993).

Figure A.1 shows a diagrammatic presentation of the prominent EMI regulation bodies. The top row shows the military standards from the USA, NATO, UK and Germany. The MIL-STD-461 documents have been evolved for use by the U.S. Department of Defence. The armed forces in several other countries follow these standards, either closely or with minor variations [A1]. The international bodies concerned with EMC in the commercial market, namely ISO and IEC is shown in the left. To the right of the figure, the FCC and CENELEC are shown, applicable to the USA and Europe respectively.

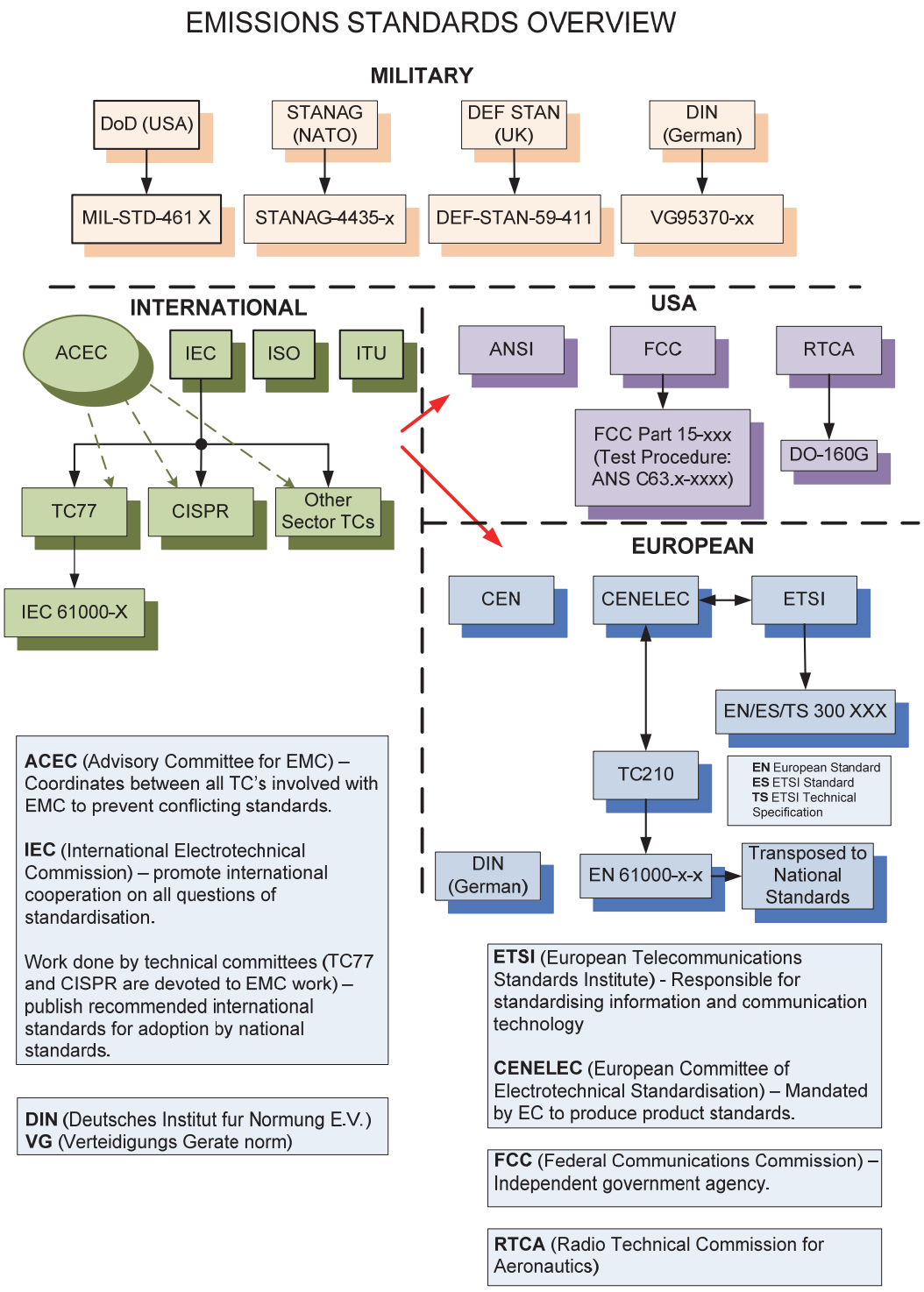

Figure A.1. Standards overview – EMC regulation bodies in context.

A.3.3 Regulating bodies summary

The ACEC is the Advisory Committee on Electromagnetic Compatibility reports and considers all aspects of the ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment. The object of ACEC is to guide and coordinate IEC (International Electrotechnical Commission) work relating to electromagnetic compatibility matters in order to ensure consistency and avoid duplication and conflict in IEC standards [A4]. The IEC prepares and publishes international standards for all electrical, electronic and related technologies [A5].

ACEC is responsible for the mandatory IEC Guide 107 which provides guidelines on drafting electromagnetic publications and through which it coordinates the EMC work of IEC's technical committees. Members of ACEC are representatives of the following TC's (Technical Committees) [A4]:

- TC77 : Electromagnetic Compatibility
- CISPR : International special committee on radio interference
- Other sector technical committees or subcommittees whose activities include EMC matters as an important part of their work.

The IEC is one of three global sister organizations that develop International Standards of the world. The other two is ISO (International Organization for Standardisation) and ITU (International Telecommunication Union) [A5], [A6], [A7]. IEC has issued four generic standards IEC 61000-6-1, 2, 3, and 4, which specify emission and immunity requirements. The generic standards list the individual test standards (generally, IEC and CISPR documents) that are applicable and the limits that apply.

The FCC (Federal Communications Commission, United States of America) regulates the interstate and international communications of the USA by radio, television, wire, satellite and cable in all 50 states, the District of Columbia and USA territories. It has responsibilities such as developing and implementing regulatory programs; processing applications for licenses and other filings; encouraging the development of innovative

services; conducting investigations and analysing complaints and is involved in public safety and homeland security. The FCC forms advice from various objective advisory committees [A8]. ANSI (American National Standards Institute) is the official U.S. representative to the ISO and IEC. It oversees the creation, promulgation and use of norms and guidelines [A9] as formed by the FCC. The FCCalso requires that testing be performed following the American National Standard Institute (ANSI) C63.4-1992 measurement procedure.

RTCA DO-160G is used by the international commercial airline industry to qualify equipment as part of Federal Aviation Administration certification of aircraft. Among commercial standards, DO-160G is the most similar to MIL-STD-461F. The test methodology addresses many issues important in MIL-STD-461F including ground planes, electrical cabling, and consistency among setups. DO-160G provides a number of different categories to which equipment can be certified depending on the type of equipment, its installation location, and the needs of the equipment and aircraft manufacturers [A3].

CEN (Comité Européen de Normalisation - French) is the overlooking body for the European Committee for Standardisation. CENELEC (European Committee for Electrotechnical Standardisation) is mandated by the European Community to produce product standards CEN and CENELEC, as European Standards Organisations, have sought to provide a comprehensive overview of the multiple standards issues [A10]. CENELEC is largely responsible for approving detailed standards, which are acceptable for demonstrating compliance with the EMC Directive. Most CENELEC approved standards are identical to or contain only minor deviations from those developed by the IEC and CISPR [A3]. Note that CEN and CENELEC do not distribute or sell standards.

ETSI (European Telecommunications Standards Institute, France) produce globally applicable standards for Information & Communications Technologies including fixed, mobile, radio, broadcast, internet, aeronautical and other areas. ETSI is recognised as an official European Standards Organisation by the European Union [A11].

Moving to the top row of Figure A.1, the most prominent military standards are shown. Military standards constitute a most comprehensive set of standards in electromagnetic

compatibility [A1]. MIL-STD-461 is the USA DoD EMC standard for defence procurement [A3] and the most widely used standard for defence products. It establishes the requirements for the control of electromagnetic interference characteristics of subsystems and equipment for applicable military requirement. The armed forces in several other countries follow this standard, either closely or with minor variations [A1].

DEF STAN 59-411 is the UK EMC standard for defence procurement, aligned to MIL-STD-461. Ministry of Defence, Def Stan 59-411 Issue 1 on Electromagnetic Compatibility (EMC) was published in January 2007 and supersedes Def Stan 59-41 and other EMC-related Def Stans [A12].

STANAG is the NATO abbreviation for Standardisation Agreement, which sets up processes, procedures, terms, and conditions for common military or technical procedures or equipment between the member countries of the alliance. Each NATO state implements STANAG within its own military. The purpose is to provide common operational and administrative procedures and logistics, so equipment can me mutually exchangeable. STANAGs also form the basis for technical interoperability between a wide variety of communication and information (CIS) systems essential for NATO and Allied operations [A14].

DIN stands for ‘Deutsches Institut für Normung’ which means ‘German Institute of Standardisation’. DIN established special standardization offices for the drawing up of defence standards (so-called Verteidigungsgerätenormen – VG Standards) [A15].

A.4 MEASUREMENT DIFFERENCES

Large military platforms, such as ships, have a large concentration of sensitive electronic devices and therefore the need for more severe EMC limits than for commercial equipment [A16]. The different test levels, test standards, frequency coverage and different detectors used in measurements will be shown in this paragraph.

A.4.1 Conducted emission frequency coverage

The main test frequency limits for DC and AC power leads, relevant to conducted emissions, is shown in Figure A.2. Deciding on the applicable standard to design for, will depend on where the product will be used. If a military product is developed, it will need to adhere to MIL-STD 461. In this instance, the conducted emission test spans from 10 kHz up to 10 MHz. If commercial equipment are manufactured in the United States and/or intended for sale in the United States, it has to be tested to FCC Part 15. Applicable frequency range for FCC is from 450 kHz up to 30 MHz. Commercial products for the European market need to comply with CISPR (EN or IEC specification), to be tested between 150 kHz and 30 MHz. Commercial avionics need to comply to the RTCA/DO-160G, spanning from 150 kHz to 152 MHz [A17].

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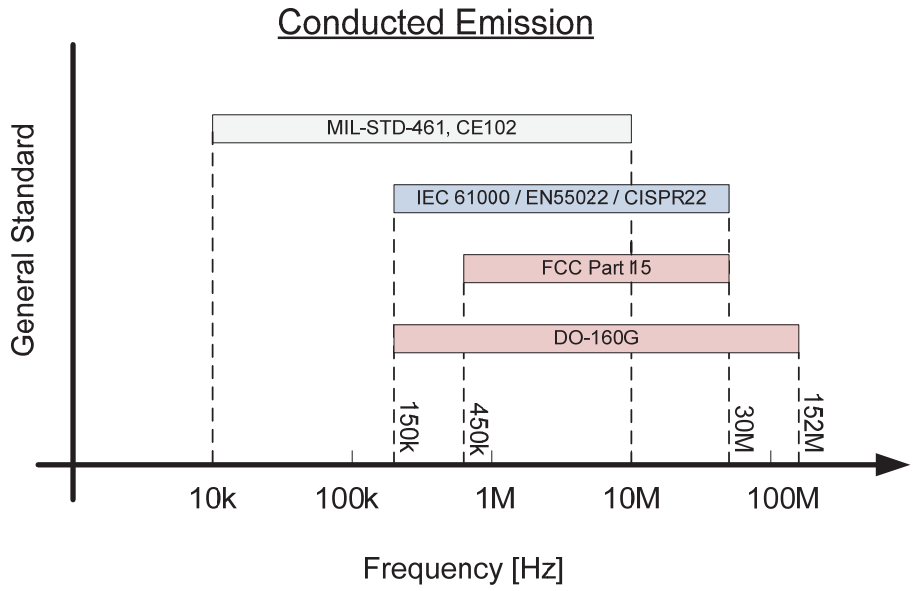

Figure A.2. Conducted emission compatibility test frequency limits.

A.4.2 Setup Differences between standards

There are basic differences in the various measurement set-ups. MIL-STD 461F calls for using the standard military environment set-up, with the test equipment placed on a solid ground plane. The presumption is that military installations are mostly mounted on a metal platform. Commercial test procedures call for mounting the test unit on a non-conductive tabletop 80 cm above the ground plane. This difference is not considered to affect measurement levels in a significant way [A16].

The MIL-STD-461 conducted EMC bench setup is shown in Figure A.3. The two LISNs (both supply lines) conditions and stabilises the power source to the equipment under test (EUT). The LISNs measure the positive line and the negative line disturbance separately. This can be recorded with a spectrum analyser.

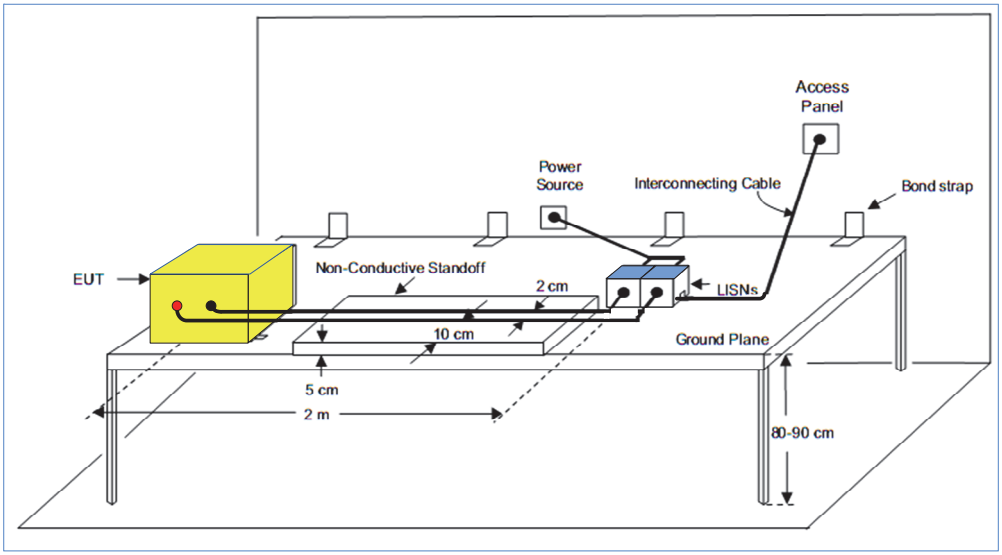

Figure A.3. Conducted EMC Setup (copied from [A13]).

CISPR 25 uses a very similar setup as in Figure A.3, except that the EUT is raised 50 mm from ground plane with a low relative permittivity support ($\varepsilon_r \leq 1.4$). CISPR 22 on the other hand, does not support a solid ground plane. The DUT has to be 700 mm above the ground plane.

The measurement bandwidth for conducted emission tests are 10 kHz for both military and commercial tests. The only difference between commercial and military bandwidth is when measurements are performed at very low frequencies, outside the normal conductive emission test frequencies. If conductive tests need to be performed between 10 kHz to about 150 kHz the measurement bandwidth is 220 Hz (commercial) and 1 kHz (military) [A3].

A detector is used to calculate a single point that represents the signal at an instant in time. EMI receivers can detect the peak, RMS (or average) value and the quasi-peak value.

The MIL-STD 461F standard calls for measurement of the conducted disturbance voltage at the LISN with a peak detector, shown in Figure A.4 (a). It indicates the highest signal level seen during the time the analyser dwells at a frequency The prevailing commercial practice, when measuring EMI from a device under test, is to measure peak values first to find problem areas that exceed or are close to the specified limits.

Quasi-peak (QP) measurements, as shown in Figure A.4 (b), which are by nature slow, are then made only on the signals that approach or exceed the limits. The QP detection is a weighted form of peak detection. QP detection is a way of quantifying the "annoyance factor" of a signal. The measured value of the QP detection is higher as the repetition rate of the measured signal increase. Thus, an impulsive signal with a given peak amplitude and a 1 kHz pulse repetition rate will have a higher quasi-peak value than a signal with the same peak amplitude but having a 10 Hz repetition rate. This signal weighting is accomplished by specific charge, discharge, and display time constants [A18]. The receiving signal $u_1(t)$ from the EMI receiver charges the capacitor C through R_1 with a time constant τ_c. If the EMI receiver signal $u_1(t)$ is lower than $u_2(t)$, the capacitor C discharges through R_2 with a time constant τ_d. For conducted EMI measurements, typically between 150 kHz and 30 MHz, the QP detector fast attack (charge) time τ_c is 1 ms and the slower decay (discharge) time τ_d is 160 ms [A19].

Figure A.4 (c) shows the average detector circuit. It applies a linear average to the incoming signal. With this detector, R1 = R2 and τ_c is 100 ms.

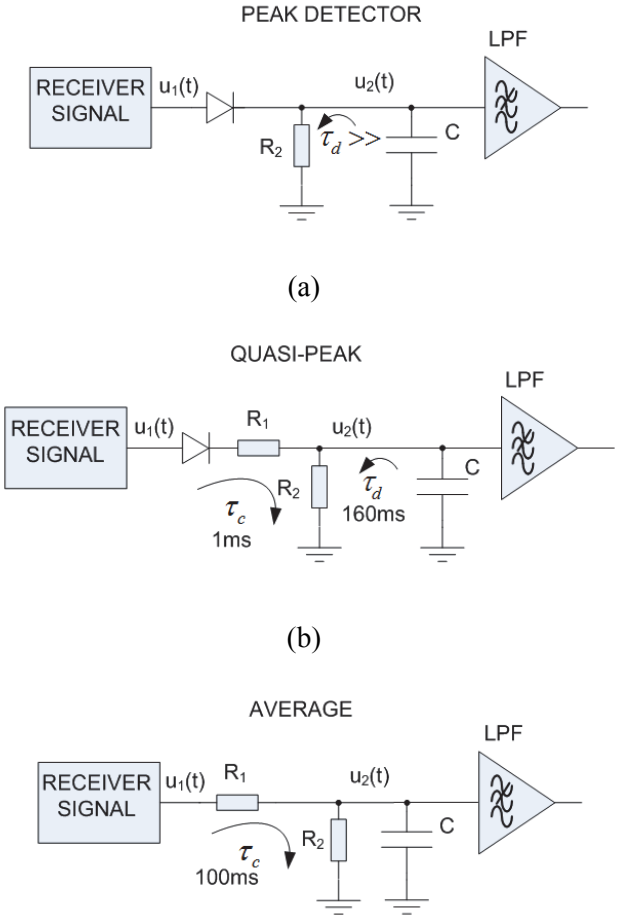

Figure A.4. Analog detectors: (a) Peak detector, (b) QP detector and (c) average detector.

The quasi-peak detector will be analysed in more detail. Figure A.5 shows a 20 ms pulse with a 100 ms frequency response combining the quasi-peak detector and the associated LPF to visualise the QP operation. The graph shows the input response (a repetitive pulse, seen in blue), the resultant quasi-peak detector response, exhibiting the fast-attack, slow-decay characteristic in red, and the combined response of the detector and the meter in black. The LPF averages the QP ripple.

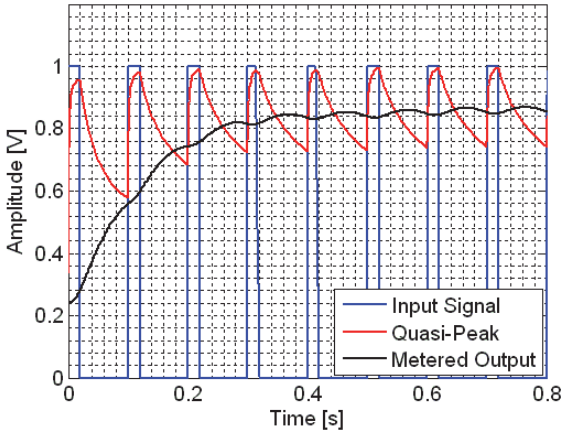

Figure A.5. QP attack and decay.

The following will show some effects when measuring noise with a QP detector. For a continuous wave, say sine wave at 100 kHz frequency, the QP detector will yield the same result as a peak detector. This is set as the reference. Signals that occur more frequently will result in a higher QP measurement than infrequent pulses. The circuit in Figure A.4 has been modelled and the analog signal response is shown in Figure A.6. A 100 kHz square wave with different duty cycles were generated as input. The dotted line shows the sine wave reference signal at 0 dB. The different duty cycles on the square wave results in different QP measurement levels. Duty cycles greater than 10% results in slightly higher values. Lower duty cycles, even down to 5% will read slightly lower values in QP, up to 1 dB, compared to peak measurements. Duty cycles in the 1% range will read almost 5 dB lower.

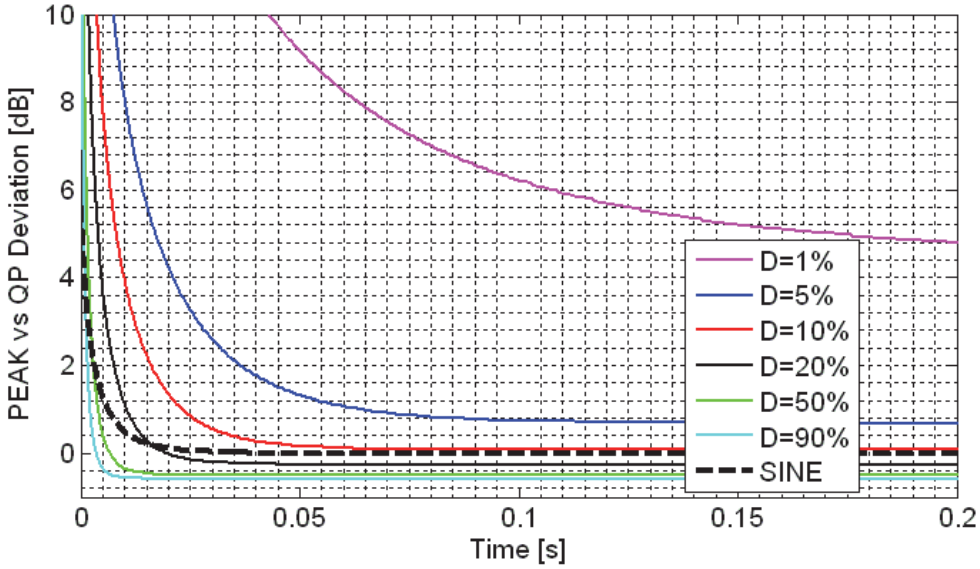

Figure A.6. QP detector analog response.

Figure A.7 shows the relationship between the duty cycle and QP loss compared to peak response at 100 kHz.

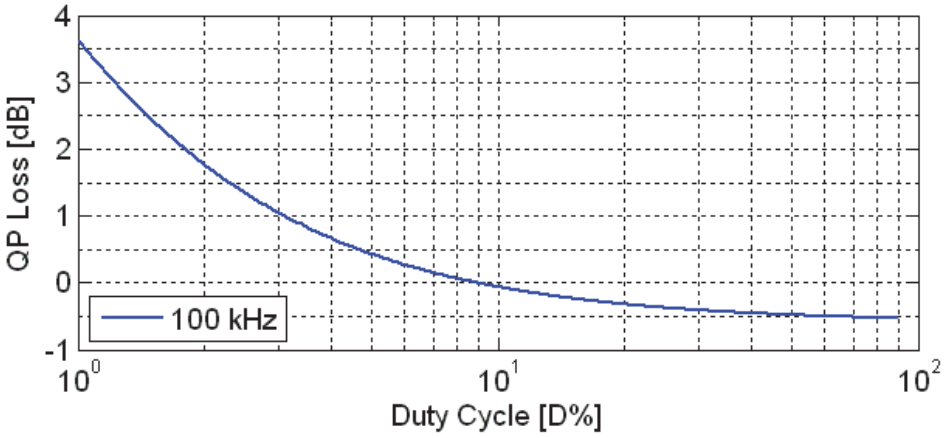

Figure A.7. QP response vs. variable duty cycle.

The peak detector measures the peak value of the signal. It can be visualised as the quasi-peak detector with a fast attack time constant and infinitely slow decay time constant.

The types of detectors vary for the test methods, but for the most part this will not cause large differences in detector signal levels [A16]. When a CISPR scan is performed, the measurement is done with a peak detector, as this is much quicker than performing a test with the QP detector. When problem areas are encountered where the set levels are not met, those frequencies are rescanned with a QP detector. Only when wideband noise characteristics are present in those bands, a lower level might be measured with the QP detector.

A.5 Conclusion

This Appendix described the background of conducted electromagnetic compliance, the bodies involved as well as the different limits, frequencies and measurement techniques to adhere to. A broad overview was covered mostly including the standards of the western world. Commercial conducted limits for Europe and the USA were provided as well as the USA DOD military specification that is widely accepted in the military field. The avionics RTCA/DO160G were also shown as this shows a very high upper frequency limit compared to other standards.

Measuring the disturbance signal with a peak detector, quasi-peak detector or average detector has to be comprehended. The quasi-peak detector is normally prescribed, but the dwell-time on the measurement frequency is very long. Normally, a peak detector is used to speed up measurements and only if possible failures occur, that portion will be re-measured with a quasi-peak detector. The relationship between these detectors are quite complex. The quasi-peak detector has been analysed and a few sample plots were presented to show its operation.

The conducted EMC test applicable for a certain product would depend on the end destination of that product. If, for instance, it is for the commercial market in Europe, the CISPR tests would be sufficient. Those limits will be the design goal for the power converter.

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