MODELLING OF A LOW PHASE NOISE RING OSCILLATOR USING SILICON GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

by

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SUMMARY

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Keywords: BiCMOS integrated circuit, feedback circuits, impulse sensitivity function, logic gates, low-noise amplifier, phase noise, ring oscillators, silicon germanium, heterojunction bipolar transistor, ultra-high frequency, voltage-controlled oscillator, wideband

In this dissertation, the phase noise performance of single-ended ring oscillators was investigated to determine their suitability in wideband, low phase noise oscillator applications. The main focus was on improving the phase noise performance of the voltage-controlled oscillator (VCO). The VCO was implemented using a custom two-stage single-ended ring oscillator configuration. The research focus was on modelling the phase noise of the VCO. This was accomplished by adapting the impulse sensitivity function for the noise sources present in the circuit. This analysis led to a closed-form phase noise expression defining the process parameters and component values. The expression was verified by way of a simulation comparison generated by SpectreRF and the process design kit supplied by metal-oxide semiconductor implementation service for the design process. A low-noise amplifier based on

a complementary metal-oxide semiconductor inverter was characterised and used to amplify the oscillator signal and transform the output impedance of the oscillator to 50 Ω.

The fabricated integrated circuit (IC) was soldered onto a printed circuit board (PCB) and measurements were conducted. It was verified that the direct current-biasing of the prototyped IC was correct, but a 17% variation was found in the passive component values. This, together with a poor ground plane choice on the IC, prohibited the device from working like the simulated version. The simulated oscillator demonstrated a phase noise performance of -80 dBc/Hz at a 1 MHz offset from the carrier. The oscillator also had a tuning range of 72% and consumed on average 4.55 mW, thus providing a VCO figure of merit of -142 dBc/Hz to -182 dBc/Hz, depending on the oscillation frequency. The size of the oscillator on the chip was 80 µm by 100 µm, occupying a total area of 0.008 mm^2. This area excluded the size of the bonding pads.

OPSOMMING

MODELLERING VAN ’N LAE FASE-RUIS KRINGOSILLATOR DEUR GEBRUIK TE MAAK VAN SILIKON-GERMANIUM HETERO-VOEGVLAK BIPOLÊRE TRANSISTORS

deur

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Sleutelwoorde: BiCMOS geïntegreerde kringbaan, fase-ruis, geïntegreerde kringbaan, hetero-voegvlak bipolêre transistor, impulssensitiwiteitsfunksie, laeruisversterker, logiese hekke, kringossillator, silikon-germanium, terugvoerkringbaan, ultra-hoë frekwensie, wyeband

Hierdie navorsing handel oor die lae fase-ruisgedrag van enkelentkringossillators om hulle geskiktheid vir aanwending in wyeband, lae fase-ruisossilators te bepaal. Die hooffokus is om die fase-ruis van ’n spanningsbeheerde ossilator (SBO) te verbeter. Die SBO is geïmplementeer deur gebruik te maak van ’n unieke twee-stadium-enkelentkringossilatorkonfigurasie. Die fase-ruis van die ossillator word in the verhandeling gemodeleer. Dit is bereik deur die impulssensitiwiteitsfunksie aan te pas vir die ruisbronne in die gekose ossillatorbaan. Hierdie analise het gelei tot ’n geslote fase-ruisvergelyking vir die kringossillator. Die vergelyking beskryf die prosesparameters en die komponentwaardes. Die vergelyking is geverifieer deur ’n simulasievergelyking wat gegenereer is deur SpectreRF en die prosesontwerppakket wat deur MOSIS uitgereik is. ’n Lae-ruisversterker wat gebaseer is op ’n CMOS-omkeerder met ’n terugvoerweerstand is gebruik om die ossillatorsein te versterk

en die uittree-impedansie van die ossillator te verander na 50 Ω. Die geïntegreerde kringbaan wat vervaardig is, is op ’n gedrukte stroombord vassoldeer en metings is geneem. Die prototipe is gemeet en die GS-spannings is geverifieer, maar ’n 17% variasie in die passiewe komponentwaardes is gevind. Die verandering in die komponentwaardes, tesame met ’n slegte keuse van ’n grondvlak, het veroorsaak dat die fisiese stroombaan nie werk nie. Die gesimuleerde ossillator het ’n fase-ruiswerksverrigting van -80 dBc/Hz by ’n 1 MHz afwyking van die draersfrekwensie af getoon. Die ossillator het ’n verstelbaarheidsvenster van 72% en 'n gemiddelde krag verkwisting van 4.55 mW. Die SBO-gevoeligheidskonstante is tussen -142 dBc/Hz en -182 dBc/Hz, afhangende van die ossilasiefrekwensie. Die silikonarea wat die ossillator in beslag neem, is 80 µm by 100 µm, wat ’n totale area van 0.008 mm^2 is, uitgesluit die grootte van die aanhegtingspunte.

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LIST OF ABBREVIATIONS

AC	Alternating current
BiCMOS	Bipolar and CMOS
BE	Base-emitter
CAD	Computer-aided design
CE	Collector-emitter
CML	Current-mode logic
CMOS	Complementary metal-oxide semiconductor
DC	Direct current
DRC	Design rules check
DUT	Device under test
F	Noise factor
FFT	Fast Fourier transform
FOM	Figure of merit
HBT	Heterojunction bipolar transistor
IC	Integrated circuit
ISF	Impulse sensitive function
LC	Inductor-capacitor
LNA	Low-noise amplifier
LO	Local oscillator
LTI	Linear time invariant
LTV	Linear time variant
LVS	Layout versus schematic
MIM	Metal-insulator-metal
MOS	Metal-oxide semiconductor

MOSIS	MOS implementation service
NDA	Non-disclosure agreement
NF	Noise figure
nMOS	Negative-channel metal-oxide semiconductor
PCB	Printed circuit board
PDK	Process design kit
PLL	Phase lock loop
pMOS	Positive-channel metal-oxide semiconductor
PSD	Power spectral density
PSS	Periodic steady state
Q-factor	Quality-factor
QFN	Quad-flat no-leads
RF	Radio frequency
SiGe	Silicon germanium
SNR	Signal-to-noise ratio
SPICE	Simulation programme with integrated circuit emphasis
VCO	Voltage-controlled oscillator

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION

1.1 CHAPTER OBJECTIVES

This chapter introduces the background of the research by considering the research question and developing an associated hypothesis. Justification is given for the research as well as the research methodology.

1.2 BACKGROUND TO THE RESEARCH

There is a continued drive to add more devices to the internet and promote communication between such devices [1]. This ever-growing trend places a huge burden on the available spectrum that can be used to accomplish such a goal. Several options are available for increasing the number of hardware devices connected to the internet. The first option is to use higher frequencies that are currently unused. This is certainly a viable option but to manufacture devices that can work at such frequencies is both complex and costly, limiting its applications to costly niche devices. Operating at these frequencies also limits the distance obtainable when sending a signal [2]. All the parasitic requirements need to be accounted for when working at these high frequencies. A second option is to multiplex several signals together on one band using either frequency or time multiplexing [3], [4]. A third option is to increase the number of available channels in the currently usable spectrum, which places more stringent requirements on the phase noise of local oscillators (LO) in devices using these spectra [1].

By improving the phase noise of the oscillator in the transmitter and receiver units, the system will observe an improvement in the dynamic range and reduce channel-spacing requirements. Improving the oscillator's phase noise is usually inversely dependent on the oscillator's bandwidth, size and power consumption. Two general groups of oscillators exist. The inductor-capacitor (LC) oscillator is most often used for its low phase noise attributes, but these oscillators require a large chip area and narrow bandwidth. The second type of oscillator used is the ring oscillator. These oscillators are much smaller in their chip area requirement, have lower power consumption, ease of implementation and have wider bandwidths, but in general have poor phase noise performance [1].

1.3 HYPOTHESIS AND RESEARCH QUESTIONS

The problem addressed in this research is:

- How can the phase noise performance of a ring oscillator be improved without sacrificing bandwidth, adding additional stages or lowering the nominal oscillation frequency?

Expanding on the primary research question, the following secondary research questions were addressed:

- How suitable are silicon germanium (SiGe) heterojunction bipolar transistor (HBT) devices for single-ended ring oscillator applications?
- How linear is the voltage-to-frequency tuning curve of a ring oscillator implemented in a SiGe HBT process?
- How will the SiGe technology affect the bandwidth of the proposed oscillator?
- Determine whether the Barkhausen's oscillator stability criteria can be adapted to include design criteria for single-ended ring oscillators.

Research has shown that SiGe HBT devices have improved $1/f$ noise qualities compared with traditional complementary metal-oxide semiconductor (CMOS) active devices when used in a differential Colpitts oscillator structure [1], [5], [6], [7]. It is this $1/f$ noise that upconverts to phase noise in the $1/f^3$ region [7].

1.4 JUSTIFICATION FOR OF THE RESEARCH

With the ever-growing number of devices that need to communicate with one another, as mentioned in section 1.2, there is merit in optimising the use of the spectrum already allocated for individual operations. One method of optimising spectrum usage is to utilise the edges of the band optimally, which correlates directly with the phase noise profile of both the carrier signal and the modulated signal.

Traditionally, optimising the phase noise of an integrated circuit (IC) oscillator is associated with the resonant LC circuit or an elaborate scheme of inverters cascaded in such a way as to produce a ring oscillator with good phase noise.

Although both of these circuits are known and used for good phase noise performance, they both suffer from large chip area requirements, narrower bandwidths and higher power consumption. Conjoined with the constantly growing number of smart devices, the functionality of these devices is continually increased and improved.

For these reasons, research activity in this field is still occurring, because there is a current need for good low phase noise oscillators with small chip area requirements, which cover a wide band of operation with minimum power consumption.

1.5 RESEARCH METHODOLOGY

The research methodology consisted of a literature study of reports on multiple voltage-controlled oscillator (VCO) configurations that have been inspected and published to date. Chapter 2 specifies the SiGe technology, as well as the single-ended ring oscillator structure. The phase noise model considered for this research is the impulse sensitive function (ISF) method performed on the linear time variant (LTV) model of the oscillator. This expression would lead to finding the major contributor of phase noise and minimising it to improve the phase noise performance.

The design, guided by the choices above, led to a two-stage single-ended ring oscillator design. Simulations were performed using the IBM8HP 130 nm process design kit (PDK). There is close correlation between the analytical phase noise model and the simulation results obtained by SpectreRF.

The final step of the design process was the layout of the designed VCO. A printed circuit board (PCB) had to be manufactured on which to place the IC. The IC was packaged in a sealed silicon quad-flat no-leads (QFN) package, which was soldered onto the PCB so that measurements could be conducted.

1.6 DELIMITATIONS AND ASSUMPTIONS

1.6.1. MOS implementation service non-disclosure agreement

A multi-project wafer run, sponsored by the metal-oxide semiconductor implementation service (MOSIS) educational programme for the process, was used to house multiple circuits from several students. The process parameters are protected by a non-disclosure agreement (NDA) for the desired manufacturing process, namely IBM's Bipolar and CMOS (BiCMOS) 130 nm process. This prohibits the extraction of exact values for most of the variables required to complete a detailed mathematical model of the ring oscillator, but a table of measurements is provided in the document [8]. Only selected model sizes have measurement results at selected frequency points. Where the size or frequency point of the model used differs from the data given, a value is derived by way of interpolation. Although this means that an exact answer cannot be obtained, it still allows the study to determine whether the outcome is valid.

1.6.2. Simulation results boundaries

For an accurate comparison between the mathematical results and the simulation results obtained, a quick look at the way radio frequency (RF) simulators operate will show their accuracy when analysing the phase noise of an oscillator. Equation (1.1) shows the equivalent phase shift $ø(t)$ that results from an arbitrary noise function $\mu(t)$.

$$\phi(t) \propto \int_{-\infty}^{t} \mu(\tau) d\tau \tag{1.1}$$

A sinusoidal signal with an alternating phase function is characterised by (1.2).

$$V(t) = A\cos[\omega_c t + \phi(t)] \tag{1.2}$$

To calculate the phase noise of the signal shown in (1.2), all RF simulators consider this signal for a short observation time, typically $ø(t) << 1$ rad [9]. To analyse a sinusoidal signal with a varying phase function and then calculate the phase noise of the signal becomes exponentially complex. For this reason, (1.2) is approximated in (1.3).

$$V(t) \approx A\cos\omega_c t + A\phi(t)\sin\omega_c t \tag{1.3}$$

The approximation step taken in (1.3) allows for the perturbation function to change from a phase element of the signal to an amplitude element of an individual signal. This approximation holds only for small *ø(t).*

In Figure 1.1, two graphs are plotted of both (1.2) and (1.3), with *ø(t)* = 0.01.

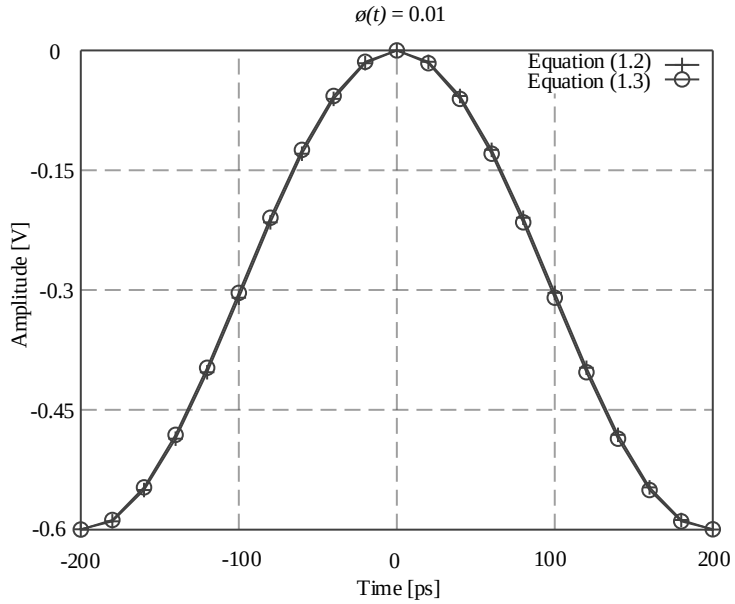

Figure 1.1. Approximations graphically shown for *ø(t)*=0.01.

For *ø(t)*=0.01 it is noticeable that the two graphs correlate with each other very closely, thus the approximation holds.

Figure 1.2 shows the plot of both (1.2) and (1.3) for *ø(t)*=0.1.

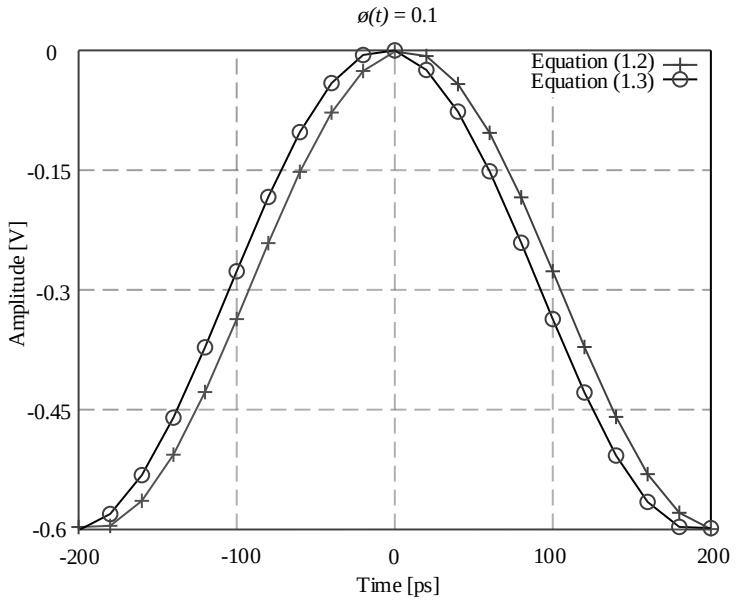

Figure 1.2. Approximations graphically shown for *ø(t)*=0.1.

In Figure 1.2 there is a correlation between the two figures, there is also a slight phase shift between the two figures, showing the assumptions made still hold for an approximation equation.

Figure 1.3 shows the plot of both (1.2) and (1.3) for *ø(t)*=1.

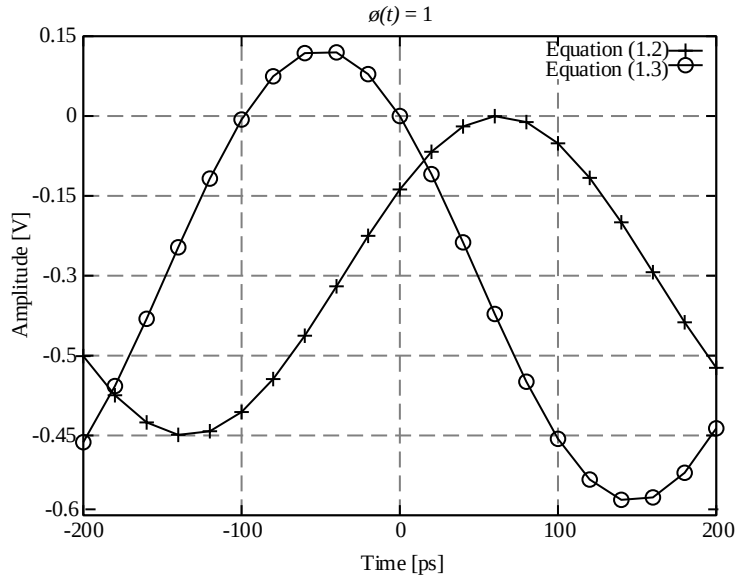

Figure 1.3. Approximations graphically shown for *ø(t)*=1.

Now it is not only the phase shift that is both present and larger, there is also an amplitude difference between the two figures, showing that the approximation no longer holds for a

$ø(t)>0.1$. It is due to this approximation that the phase noise simulation results at low offset frequencies are no longer accurate.

With the high-frequency design as well, interconnect parasitics are applicable, meaning that the tracks made in the layout process afterwards have to be characterised and imported back into the schematic to re-verify the simulation done and to ensure that the circuit is still functional. Through future research, there is, therefore, room for improving this.

1.7 CONTRIBUTION TO THE FIELD

A mathematical phase noise analysis has been done on the oscillator, resulting in an analytical expression for phase noise. The main contributing parameter of phase noise in the oscillator was found to be the base resistance thermal noise.

Further, it was shown that a two-stage single-ended ring oscillator structure is possible and practical. The proposed oscillator has a wider bandwidth when compared with other published oscillators.

Other single-ended ring oscillators were studied, but some of these were found not to conform to the Barkhausen stability criteria. This shows that the Barkhausen stability criteria do not encompass all oscillators, while it is still true that all oscillators conforming to the Barkhausen stability criteria should operate. An expansion of the Barkhausen stability criteria is proposed to include single-ended ring oscillators.

A secondary contribution of this work is the gain equation formulated for the proposed high input impedance low-noise amplifier (LNA).

1.8 PUBLICATIONS DERIVED FROM THE RESEARCH

The following peer-reviewed conference publication has resulted from this work:

S.J.L. van Niekerk and S. Sinha, “A 2.5 GHz Low Phase Noise Silicon Germanium Heterojunction Bipolar Transistor Ring Oscillator,” *Proceedings: IEEE International Semiconductor Conference*, 10-12 Oct. 2016, Sinaia, Romania.

1.9 OUTLINE OF THE DISSERTATION

Chapter 1 provides the background to the research problem and formulates the hypothesis. The research methodology is summarised and any delimitations and assumptions are presented.

Chapter 2 provides a detailed literature review outline to validate Chapters 3, 4 and 5. The requirements necessary for good oscillator design are discussed. The general classes of on-chip oscillators are described. The SiGe technology and some of its noise benefits are also briefly discussed in this chapter. A brief discussion of the NF follows, with a look at two phase noise modelling methods, namely the LTV model and the ISF model. The final topic of the literature review focusses on high impedance LNA, the NF of the LNA and the noise-to-phase noise relation of the LNA. An LNA with minimal NF and high impedance is required to measure the phase noise of the proposed oscillator, without altering or deteriorating the current phase noise.

Chapter 3 provides a detailed description of the methodology followed to complete this research, where the process and technology node used for prototyping are documented. The major components used in the design from the applicable PDK are described. The methods used to derive mathematical models for both the oscillator phase noise and the amplifier NF are described. Finally, the simulation and layout software for both the IC and PCB designs is introduced.

Chapter 4 presents the measurement set-up used to perform measurements, as well as the mathematical modelling of the ring oscillators' phase noise. The calculations of separate noise sources are done in this chapter and the individual noise sources are added together to obtain the total phase noise performance of the oscillator. The design of the oscillator is provided, as well as the expansion of the Barkhausen stability criteria, to include the stability criteria of several types of ring oscillators.

Chapter 5 provides the results obtained from the research and shows a macro-photograph of the layout and prototype circuit. The mathematical results are plotted in Octave 4.0.0 and compared with the simulation results obtained from SpectreRF. Further comparison is done with other published oscillators using a standard figure of merit (FOM) function.

Chapter 6 formally concludes the document with a summary of the research and a critical evaluation of the hypothesis in view of the results obtained.

Addendum A provides the Octave script used to plot several of the figures in Chapter 5.

Addendum B shows addition layout images of the IC.

CHAPTER 2 LITERATURE REVIEW

2.1 CHAPTER OBJECTIVES

This chapter expands on the research topics discussed in Chapter 1. It investigates the different on-chip oscillator topologies, their models, advantages and shortcomings. In addition, this chapter explores the possibility of phase noise improvements obtainable by substituting CMOS active transistors with SiGe HBTs. The passive components concerning the technology process are briefly investigated.

2.2 OSCILLATOR REQUIREMENTS

Three methods for increasing the number of wireless devices communicating with one another were discussed in section 1.2. The last method to improve spectrum utilisation is to optimise the channel width of each device. By narrowing each channel, more channels can effectively be placed in the same spectrum band. Narrowing each channel will place higher constraints on the phase noise of LO [3]. LOs will need to be lower phase noise oscillators, in an attempt to prevent channel leakage [10]. Each superheterodyne RF receiver implements frequency translation by mixing a modulated RF signal with a LO [3]. The phase noise of the frequency synthesiser degrades the integrity of the mixed-down signal, which places a limit on the selectivity of the receiver unit [9], [11].

For an oscillator to be used in many different transceivers, additional requirements need to be fulfilled. Apart from having low phase noise, it would be beneficial if one oscillator could be used in many different devices without having to develop an oscillator for each device. The IC real estate must also be kept to a minimum to allow the space to be used for other circuitry. The power consumption of the oscillator must be kept to a minimum. The oscillator must have a wide bandwidth with a linear tuning curve for tuning the oscillator in a wide bandwidth application [12]. The two major groups of oscillators discussed in this work are limited to LC oscillators and ring oscillators. The trend towards lower manufacturing cost and large-scale integration makes it desirable to implement oscillators monolithically [12].

2.3 LC OSCILLATORS

One of the two generally used oscillator structures is found in LC oscillators, which are widely considered to have superior phase noise and maximum frequency performance compared with ring oscillators for CMOS technology [13], [14], [15]. LC oscillators are realised with an on-chip capacitor and inductor tuning and resonating circuits, resulting in large chip area requirements when compared with ring oscillator structures. In addition to large surface area requirements, LC oscillators are also generally considered narrowband oscillators [13], [16]. A typical circuit schematic is shown in Figure 2.1 for an LC Colpitts oscillator.

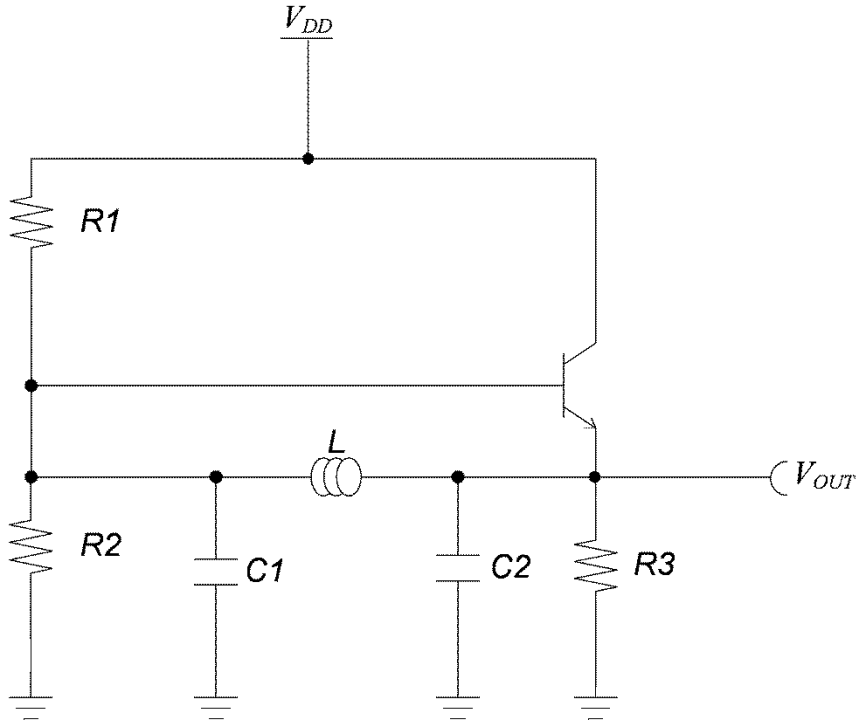

Figure 2.1. Colpitts LC oscillator.

A significant drawback of these circuits, similar to the one shown in Figure 2.1, is the required inductor and varicap (to obtain good phase noise performance, a high-*Q* typically greater than 20 is required), which places a strain on the use of low-*Q* integrated inductors [17].

2.4 RING OSCILLATORS

The second type of oscillator generally used is the ring oscillator. Unlike the LC oscillators mentioned in the previous section, ring oscillators generally consist of inverting structures cascaded in a loop in such a way as to promote oscillation in the circuit. Ring oscillators usually benefit from wider bandwidths, low power consumption, small real estate and ease of

implementation, but suffer from poor phase noise performance [13], [15], [17]. Within the ring oscillator category, two major structures also exist. The first is the differential ring oscillator and the second is the single-ended ring oscillator [12]. Although other derivatives of the ring oscillator structure also exist, such as the coupled ring oscillator, they are specific to a certain application and beyond the scope of this work [18].

Ring oscillators also have two different switching behaviours for the delay cells. The first is the non-saturated type and the second is the saturated type. For the non-saturated type, the oscillation does not swing from the rail-to-rail voltage, meaning that the CMOS devices are always in an "on" state [19]. The intuitively saturated type of ring oscillator produces a signal that has an output swing from rail-to-rail voltage.

2.4.1. Single-ended ring oscillators

A typical single-ended ring oscillator is shown in Figure 2.2 [20].

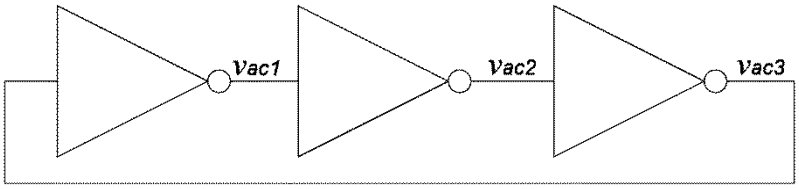

Figure 2.2. Single-ended ring oscillator structure.

For the example shown in Figure 2.2, the oscillator is constructed from three identical inverter cells. Any node after an inverter stage can be used to obtain the output signal. For applications where multiple clock signals with different phases are required, all of the output signal can be used. The phase delay between adjacent outputs is 180º plus the gate delay of the inverter circuit. A typical single-ended CMOS inverter cell has a single input and a single output port similar to the structure shown in Figure 2.3.

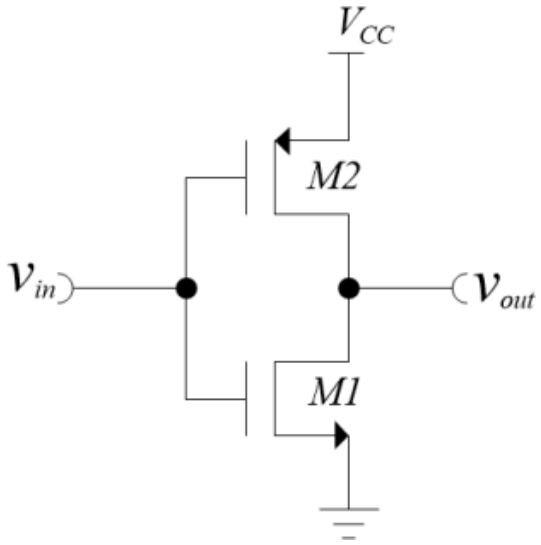

Figure 2.3. Conventional single-ended inverter cell.

Since a single stage of such an oscillator is basically an inverter, as shown in Figure 2.3, the single stages can be defined as described in the paragraphs below.

For the ring oscillator to oscillate, the voltage gain of the inverter must be larger than 1, as shown in (2.1). In addition, the phase change in the stage must be 180º, as shown in (2.2) [2].

$$A_v \geq 1 \tag{2.1}$$

$$\emptyset = 180° \tag{2.2}$$

To realise the 180º phase change, the inverters in the ring's chain need to have an uneven number of inverter cells, as shown in (2.3).

$$N_{INV} = 2n + 1 \qquad \{n\ \varepsilon\ \mathbb{N} \tag{2.3}$$

This means the single-ended ring oscillator does not conform to the Barkhausen criterion that stipulates the required conditions for proper oscillatory function. This, however, does not mean that single-ended ring oscillators do not function at all. The real reason for single-ended ring oscillators functioning is the fact that each inverter has no zero time delay between its input and its inverted output. It is this otherwise considered parasitic condition that allows the single-ended ring oscillator to function properly. To show why the inverter delay is an issue, consider the following example. For the oscillator structure shown in Figure 2.2, if v_{ac1} starts

with a zero degree phase shift, v_{ac2} will then be forced to a 360º phase shift from the start, and will force v_{ac1} to a 180º phase shift. The phase shift present at this node for the first oscillation versus the second oscillation is 180º out of phase. If the inverters did not have a delay, the structure would not oscillate and most likely force all the nodes to a voltage between V_{CC} and ground.

The maximum frequency for the single-ended ring oscillator is limited by the transient response of the positive-channel metal-oxide semiconductor (pMOS) device used in the inverter stage. The mobility of these devices, in general, is two to three times less than their negative-channel metal-oxide semiconductor (nMOS) counterparts [13]. These circuits will naturally start to oscillate at the frequency inversely proportional to the gate delay of the individual inverter stages. The natural oscillation frequency is formulated in (2.4) [20].

$$f = \frac{1}{2\tau N} \tag{2.4}$$

From (2.4) τ represents the delay time through a single inverter stage, while N denotes the number of inverter stages in a series loop. One way to improve the maximum frequency performance is to introduce negative skew delay [21].

Another consideration when using these types of oscillator structures is that the pMOS device switches more slowly for the same feature size device when compared with the nMOS. This creates several problems in terms of both devices switched “on” at the same time from low-to-high transition, allowing current pulses through both the pMOS and nMOS, creating a non-linear noise profile [21].

2.4.2. Differential ring oscillators

The differential oscillator is classically defined to have dual input and output ports on an inverter stage or a differential amplifier [17], [22]. An example is shown in Figure 2.4.

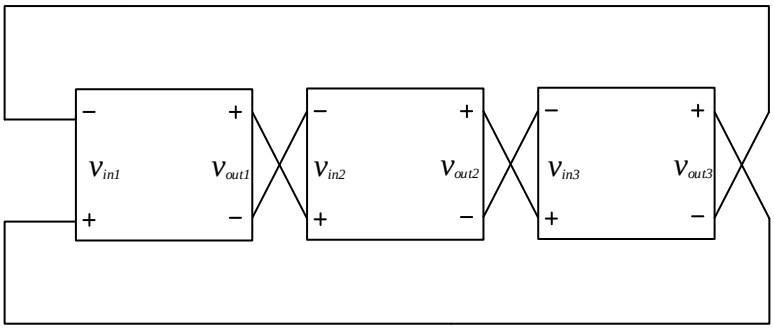

Figure 2.4. Typical differential ring oscillator structure.

The differential amplifier shown in Figure 2.4 operates with a 180º phase difference in both its input and output ports. The most common cells used for these architectures are the emitter coupled logic and the current-mode logic (CML) cells [23]. A typical CML delay cell is shown in Figure 2.5 [24], [25].

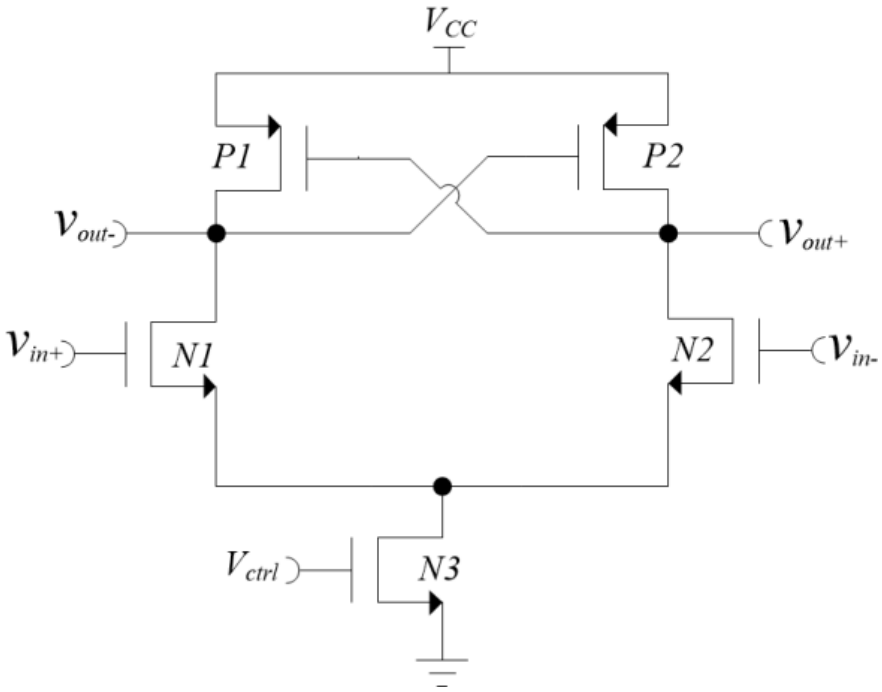

Figure 2.5. Conventional CML differential delay cell.

The differential nature of an inverter cell, as shown in Figure 2.5, used in differential ring oscillators enables these oscillators to be constructed from any number of stages, with the minimum number usually being two stages. These ring oscillators are not bounded by the *2n-1* rule shown in (2.3) [24].

2.4.3. Barkhausen stability criteria

The Barkhausen stability criteria have been used as a guideline for the fundamental conditions required in constructing an oscillating circuit. The criteria suggest two conditions to be met in order for a circuit to be a stable oscillating circuit [12]. First, the loop gain of the proposed oscillator circuit must be equal to or larger than 1, as shown in (2.5).

$$A_v \geq 1 \tag{2.5}$$

Second, the phase delay through the proposed circuit must be 0º or a multiple of 360º, as shown by (2.6).

$$\emptyset = n \times 360° \qquad \{n \, \epsilon \mathbb{N}_0 \tag{2.6}$$

These criteria set by Barkhausen are simply a unidirectional or unilateral approach taken to oscillator design. The truth is that when a circuit conforms to both criteria set out by Barkhausen, then it should theoretically oscillate, but the inverse is often not true. Not all oscillators conform to these criteria. One such example is the single-ended CMOS ring oscillator. These oscillators are usually constructed from an unequal number of inverter circuits chained together end-to-end in a circular series to form an oscillator, as shown in Figure 2.2. There is an uneven number of inverters in this circuit and the phase delay through each delay is 180°, as shown in (2.2), resulting in a 540° phase change through the ring this is not a multiple of 360°. This example shows that a major oscillator class does not conform to the Barkhausen criteria, yet the oscillators still function correctly. This shows that, as they currently stand, the Barkhausen criteria do not form a complete set of rules governing the required definitions for an oscillator to function. An expansion of the Barkhausen criteria is given in Section 4.3.

2.5 SiGe HBT NOISE PROPERTIES

This section investigates the noise properties and benefits inherent in SiGe and specifically in SiGe HBT devices. SiGe HBT devices have significantly smaller parasitic resistances, which lead to improved noise performance as well as shorter delay times [26], [27], [28]. Within the 130 nm SiGe technology node, a CML ring oscillator was shown to have a gate delay of 2.3 ps

when cryogenically cooled to 25 K [29]. This also gives the technology a higher f_{max}, making it more suitable for millimetre-wave frequencies [26].

Since the parasitic components of these devices are relatively small, allowing these high-frequency operations, it also means that the maximum voltage capability of the device decreases, reducing the dynamic range and the signal-to-noise ratio (SNR) of the circuit [27].

For SiGe HBT devices, the primary RF noise sources are the direct current (DC) base and collector currents, as well as the base resistance thermal noise [9].

SiGe is often chosen over CMOS technology for low-phase noise oscillators owing to its lower $1/f$ noise [7]. It is known that this $1/f$ characteristic of the active device upconverts to the phase noise profile in the $1/f^3$ region [1], [7].

2.5.1. Collector and base current noise

Shot noise is produced for any DC passing through any *pn* junction. This is the result of a current stream that needs to overcome a potential barrier, resulting in an uncorrelated flow of electrons [9]. For a bipolar transistor, the base majority holes flowing from the base-to-emitter node over the base-emitter (BE) junction potential field result in the base current shot noise $2qI_B$ [9]. Likewise, the current flowing through the collector-base junction has a shot noise equal to $2qI_C$ [9]. This shows that the shot noises in bipolar transistors originate from the BE junction. Other noise sources, such as the collector-emitter (CE) junction thermal noise, make a smaller contribution and can, for the most part, be omitted. Several recent studies have shown that this model can be used to model and simulate noise in SiGe HBTs accurately [9].

2.6 NOISE FIGURE

A NF is defined as the change in SNR between the input and output of a device under test (DUT) [9]. To calculate the noise factor (F), the input SNR is divided by the output SNR, as shown in (2.7) [9].

$$F = \frac{S_i/N_i}{S_o/N_o} \tag{2.7}$$

The NF is defined as the logarithmic conversion of the F, as shown in (2.8) [28].

$$NF = \log_{10} F \tag{2.8}$$

For a source termination admittance $Y_s = G_s + jB_s$, the NF can be as shown in (2.9).

$$NF = NF_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{s,opt}\right|^2 \tag{2.9}$$

Here NF_{min} refers to the minimum NF, $Y_{s,opt}$ is the optimum source admittance for the matching noise and R_n is the noise resistance.

By combining all the noise sources in a DUT into an input noise current i_{na} and an input noise voltage v_{na}, a two-port model of the noise in a DUT can be compiled. The noise parameters are functions of the power spectral densities (PSDs) of $i_{na,}v_{na}$ and $i_{na,}v_{na}^*$. The PSDs are denoted as S_{i_n}, S_{v_n} and $S_{i_n v_n^*}$, [9], as shown in (2.10) to (2.13).

$$R_n = \frac{S_{v_n}}{4kT} \tag{2.10}$$

$$G_{s,opt} = \sqrt{\frac{S_{i_n}}{S_{v_n}} - \left[\frac{\chi(S_{i_n v_n^*})}{S_{v_n}}\right]^2} \tag{2.11}$$

$$B_{s,opt} = -\frac{\chi(S_{i_n v_n^*})}{S_{v_n}} \tag{2.12}$$

$$NF_{min} = 1 + 2R_n\left(G_{s,opt} + \frac{\mathcal{R}(S_{i_n v_n^*})}{S_{v_n}}\right) \tag{2.13}$$

In equations (2.10) to (2.13) $\mathcal{R}$ and χ represent the real and imaginary parts respectively for the various factors. When the β of an HBT increases, the base current decreases for a given collector current. This relationship is shown in (2.14).

$$I_C = \beta I_B \tag{2.14}$$

The noise parameters of an ideal SiGe HBT can be deduced by determining the equivalent input noise current and voltage. For the common emitter configuration, the base current resides at the input and the collector current resides at the output, both of which have shot noise present. By using *Y*-parameters for the two-port circuit model, shown in Figure 2.6, to describe the small-signal noiseless characteristic of an HBT, (2.15) is obtained.

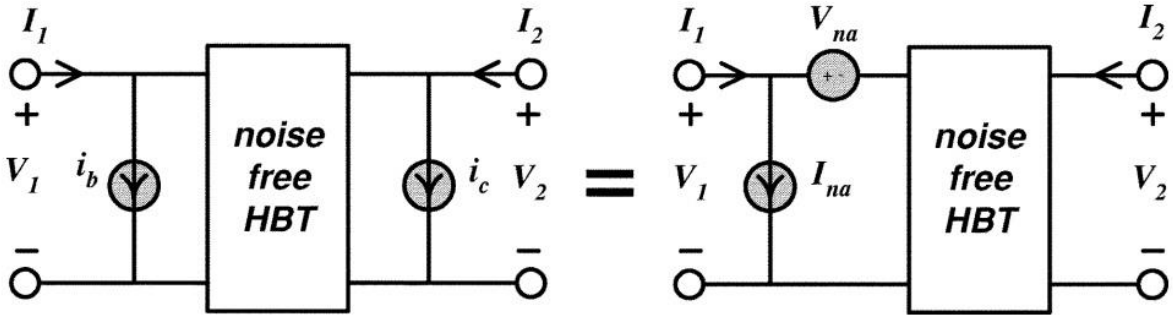

Figure 2.6. Noise source conversion. Republished with permission of IEEE, from [9]; permission conveyed through Copyright Clearance Center, Inc.

$$\begin{pmatrix} I_1 - i_b \\ I_2 - i_c \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{2.15}$$

This *Y*-parameter representation of the DUT changes when there is noise current flowing through the BE and CE junctions, namely i_b and i_c, as shown in Figure 2.6. If the current noise is referred back to the input port, a noise current I_{na} and noise voltage V_{na} are obtained. If these parameters are then used to represent the DUT in a *Y*-parameter matrix, the flow is obtained as shown in (2.16) [9].

$$\begin{pmatrix} I_1 - I_{na} \\ I_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 - V_{na} \\ V_2 \end{pmatrix} \tag{2.16}$$

The newly defined noise generators I_{na} and V_{na} can now be related back to i_b and i_c with (2.17) and (2.18).

$$V_{na} = -\frac{i_c}{Y_{21}} \tag{2.17}$$

$$I_{na} = i_b - \frac{Y_{11}}{Y_{21}} i_c = i_b - \frac{i_c}{H_{21}} \tag{2.18}$$

If an assumption is made that both current noise sources are shot noise sources, and thus independent of each other, then the PSDs, I_{na}, V_{na} and $V_{na}I_{na}^*$ are derived in (2.19) to (2.21).

$$S_{v_n} = \frac{V_{na}V_{na}^*}{\Delta f} = \frac{S_{ic}}{|Y_{21}|^2} = \frac{2qI_c}{|Y_{21}|^2} \tag{2.19}$$

$$S_{i_n} = \frac{I_{na}I_{na}^*}{\Delta f} = S_{ib} + \frac{S_{ic}}{|H_{21}|^2} = 2qI_B + \frac{2qI_c}{|H_{21}|^2} \tag{2.20}$$

$$S_{i_n v_n^*} = 2qI_c \frac{Y_{11}}{|Y_{21}|^2} \tag{2.21}$$

2.7 PHASE NOISE AND PHASE NOISE MODELS

A signal's phase noise is defined as the fluctuation in the phase and frequency of a signal over time [1]. This phenomenon is usually generated by device and channel noise contaminating the signal's purity [1]. Examples of device noise are thermal, shot and flicker noise, while substrate and supply noise are examples of channel or interference noise [1]. When considering an ideal sinusoidal oscillator, it may be expressed mathematically, as shown in (2.22).

$$v_{OUT}(t) = A\cos[\omega_0 t + \phi] \tag{2.22}$$

In (2.22), A represents the amplitude of the signal, ω_0 is the frequency and ϕ is a fixed but arbitrary phase reference. The spectrum of the signal formulated in (2.22) will thus be an impulse function located at $\pm\omega_0$. Practically, an oscillator can be expressed mathematically, as shown in (2.23).

$$v_{out}(t) = A(t)\cos f[\omega_0 t + \phi(t)] \tag{2.23}$$

In (2.23), $\phi(t)$ and $A(t)$ are functions of time, whereas f is a function with a period of 2π [1]. These fluctuations cause sidebands in the spectrum of an oscillator close to the frequency of oscillation. This phenomenon is undesirable, as it causes reciprocal mixing and degrades the

SNR in the local spectral area [17], which in turn degrades the minimum channel spacing obtainable in any given part of the frequency spectrum. The classical definition of phase noise is shown in (2.24).

$$\mathcal{L}\{\Delta\omega\} = 10\log\left(\frac{P_{offset}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right) \tag{2.24}$$

Equation (2.24) defines the phase noise of a signal as the logarithmic power percentage that a 1 Hz band at the offset $\Delta\omega$ from the carrier has compared with the power present at the centre of the carrier, as shown in Figure 2.7.

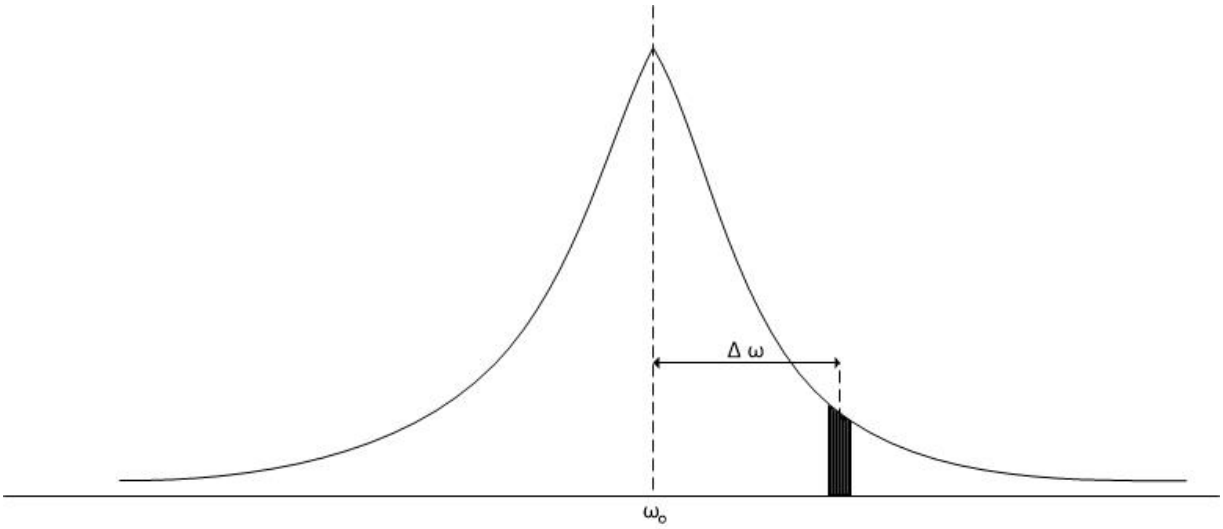

Figure 2.7. Phase noise definition at Δω offset.

Figure 2.7 shows the energy in the 1 Hz band at $\Delta\omega$ offset frequency to the carrier frequency ω_0.

Several mathematical models exist for calculating the phase of an oscillator. For this study the ISF method will be used. A quick look will also be taken at Leeson's LTI model, but other methods, such as quantifying the jitter in the oscillator by using information theory quantifiers, will not be considered [31].

2.7.1. Leeson's LTI model

The first approximation model for phase noise in an oscillator was presented by Leeson in 1966 and is constructed by taking a linear time invariant (LTI) approach to an otherwise non-linear time variant system [32], [33]. The phase noise model proposed by Leeson considers

only the phase noise contribution due to the losses from the tank circuit. Additional noise sources, which in most cases are the major contributors, such as the phase noise contribution from the active devices, are not considered in this model [7], hence it is not suitable for determining the improvement of phase noise contribution from a SiGe active device.

A second reason not to use this model is that since all oscillators are periodically time-varying systems, these characteristics need to be taken into account when constructing a model for the oscillator's phase noise. It is for this reason that LTI models are not suitable for use when analysing the phase noise profile of any oscillator and give an estimate only of the phase noise performance [5]. Although this model is limited in its prediction ability of absolute phase noise figures, it still provides valuable insight into the factors contributing to phase noise. The composite expression proposed by Leeson is shown in (2.25) [32].

$$S_{\emptyset}\{\omega_m\} = S_{\Delta\emptyset}\left(1 + \left[\frac{\omega_0}{2Q\omega_n}\right]^2\right) \tag{2.25}$$

Since this model for phase noise calculation is outdated and an improved alternative [6] is available, it was not considered further for this study.

2.7.2. Impulse sensitive function

To analyse the phase noise profile of the two-stage ring oscillator, the ISF theory, originally developed in [1] and later expanded on by [5] and [6], will be used. This method suggests that each noise source can be considered individually and then added together to get the cumulative effect. This method relies on injecting a current pulse in series with a known noise source, such as the base resistance thermal noise or the collector current shot noise, and then monitoring the output variation when such a pulse is presented. The common equation used for calculating the ISF is shown in (2.26) [5], [6].

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{\Gamma_{ns,rms}^2}{q_{max}^2}.\frac{\overline{i_{ns}^2}/\Delta f}{2\Delta\omega^2}\right] \tag{2.26}$$

To solve (2.26), an in-depth look into each variable must be taken. The maximum charge across the capacitor on the node of interest is denoted by q_{max}. This refers to the total capacitance on the base node, which includes the parasitic capacitance of the active device on this node. The track connecting the two stages is negligibly small, thus the capacitance formed between this track and the ground plane will be negligibly small.

$$q_{max} = AC_{max} \tag{2.27}$$

In (2.27), A represents the maximum voltage swing across the capacitance on the node when injecting a current impulse and C_{max} represents the maximum capacitance on the node of interest. Next, two variables are considered simultaneously, namely i^2_{ns} and Δf. The result of dividing the first variable by the second variable is the PSD of the Gaussian noise generated by the noise source of interest, as shown in (2.28).

$$\frac{\overline{i_{ns}^2}}{\Delta f} = \frac{4k_B T}{ns} \tag{2.28}$$

In (2.28), k_B refers to Boltzmann's constant (1.38×10^{-23} J/K) and T refers to the temperature of operation in Kelvin.

The final closed-form expression was derived in [6] for a SiGe HBT device used in a Colpitts oscillator configuration, as shown in (2.29).

$$\Gamma_{ns,rms}^2 = \Gamma_{ns}^2 \cdot \frac{B_1(2a_x)}{B_0(a_x)B_1(a_x)} \tag{2.29}$$

In (2.29), Γ_{ns} denotes the ISF of the noise source considered as defined by [1]. The ISF function for a single-ended LC oscillator was defined as a sinusoidal signal, while the ISF function for the single-ended ring oscillator will be similar. $B_0(a_x)$ is a modified Bessel function of the first kind of order zero, while $B_1(a_x)$ *and* $B_1(2a_x)$ are all modified Bessel functions of the first kind of order one. The equation for a_x is shown in (2.30) [6].

$$a_x = \frac{A_x}{V_T} \tag{2.30}$$

In (2.30), V_T denotes the thermal voltage of the transistor and A_x denotes the maximum voltage swing of the oscillator. Equation (2.29) can be solved by making use of the modified Bessel function of the first kind [5], [6], as shown in (2.31).

$$B_m(y) = \frac{1}{\pi}\int_0^{\pi} e^{ycost}\cos(mt)\,dt \tag{2.31}$$

In (2.31), m denotes the order of the Bessel function. For the case where m = 0, the Bessel function is of the first kind. This means the cosine part of (2.31) is reduced to one leaving an exponential term. The resultant term is then removed from (2.30) leaving the expression as shown in (2.32).

$$I_B = I_S e^{\frac{V_{BE}}{V_T}} \cdot B_0\left(\frac{A_e}{V_T}\right) = I_S e^{\frac{V_{BE}}{V_T}} \cdot B_0(a_e) \tag{2.32}$$

All the variables have been solved for (2.29) and can now be substituted into (2.26) and the result is shown in (2.33).

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T I_B r_b}{2(A_x C_{\max})^2 \Delta\omega^2 N^2 V_T R_L} \cdot \frac{B_1(2a_x)}{B_0(a_x)B_1(a_x)}\right] \tag{2.33}$$

This process needs to be completed for each noise source in the oscillator, and the total phase noise performance of the oscillator is calculated by adding all of these noise source contributions together, resulting in a total phase noise per frequency offset figure. Since this method of calculating phase noise enables one to consider all the noise sources in a circuit, it is more favourable to calculate the phase noise more accurately, thus making it the most favourable method to use for calculating the phase noise.

2.8 LNA CONSIDERATION

Considering the Friis noise equation shown in (2.34) [34], it is noticeable that the total F value in an RF sequence is highly dependent on the noise factor of the first element in the chain. The noise factor of the subsequent RF block is scaled by the gain of the preceding RF blocks [9]. To minimise the noise factor of any given RF sequence, there is a huge incentive to make the first block one with a very low noise factor and a large gain, as shown in (2.34).

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{2.34}$$

For this reason, there needs to be an LNA or low noise block following the oscillator, which ensures that the phase noise degradation of the oscillator is contained to the oscillator and the amplifier, minimising the influence of any circuit using the oscillator signal.

2.8.1. CMOS inverter with feedback resistor

The CMOS inverter is one of the foundational building blocks used in CMOS circuitry, as shown in Figure 2.3. Not only is it used to invert a digital signal, but it is often also used as a building block in a larger hierarchy of circuitry to obtain a complex function. A second advantage of the inverter is its ease of implementation and small chip area requirement.

One method of amplifying a signal with the use of a CMOS inverter is to place a resistor between the input and output terminals of the inverter, thereby giving it negative feedback, as shown in Figure 2.8.

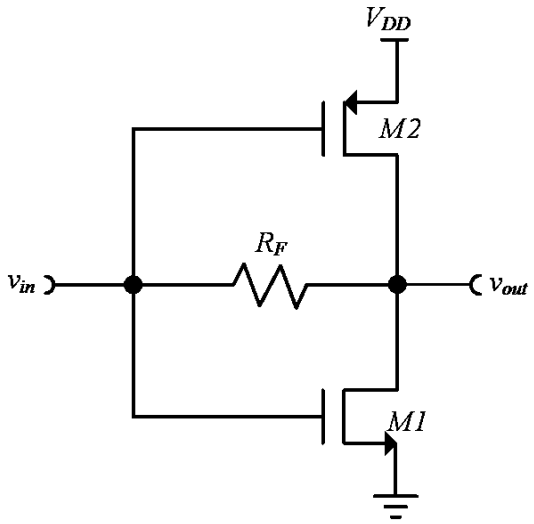

Figure 2.8. Inverter amplifier/limiter circuit.

Although the technique shown in Figure 2.8 is known to amplify [35], the true analogue gain of such an amplifier with a feedback resistor has not been published, nor has its influence on phase noise; a mathematical model for the gain of the amplifier shown in Figure 2.8 is deduced in Section 4.5. This is mainly because of a high gain value that this circuit exhibits, allowing most of its applications to be limiter circuits or digitiser circuits. Since space and the number of active devices are of concern, it is required that the feasibility of using such a device to amplify an LO without adding significant phase noise to the signal be determined. A second requirement is to have high input impedance, which is matched with the oscillator output. In [35], the three states of the CMOS inverter are discussed, as shown in Figure 2.9.

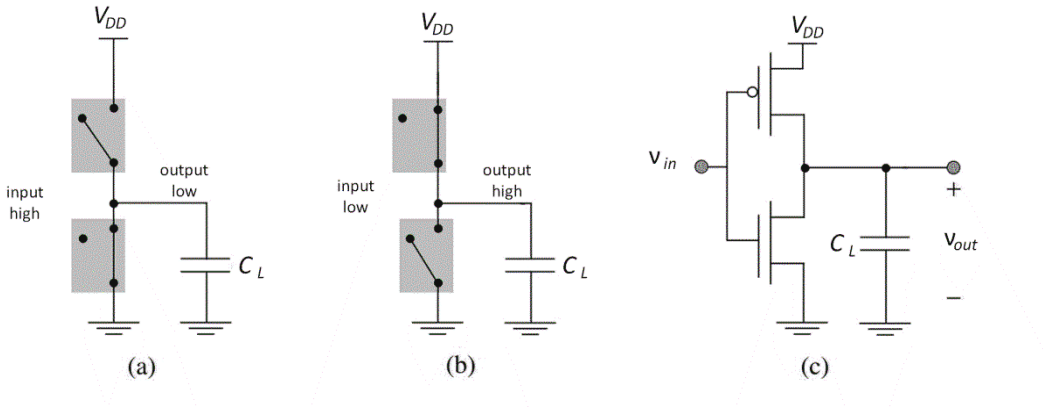

Figure 2.9. Modes of operation in a CMOS inverter.

(a) High input. (b) Low input. (c) Inverter circuit. Adapted from [35], with permission.

For the first state shown in Figure 2.9, the input of the inverter is given a digital high condition, meaning the nMOS is active while the pMOS is operating in shutdown mode, as

shown in Figure 2.9 (a). For the second state, a digital low condition is introduced to the input of the inverter, as shown in Figure 2.9 (b). This activates the pMOS device, while the nMOS device operates in shutdown mode. From the previous two conditions, it is easy to see why the circuit functions as an inverter of the input signal. The third state of operation occurs when both devices are in a linear region, i.e. the transition between a low and a high output or vice versa. During this time, there is a momentary period where a path is open for current to run between the power supply and the ground terminal through both active devices. This third state exhibits a very large gain profile [35].

The transfer curve of the inverter is shown in Figure 2.10, as well as the current-voltage transfer curve of both the pMOS and nMOS devices.

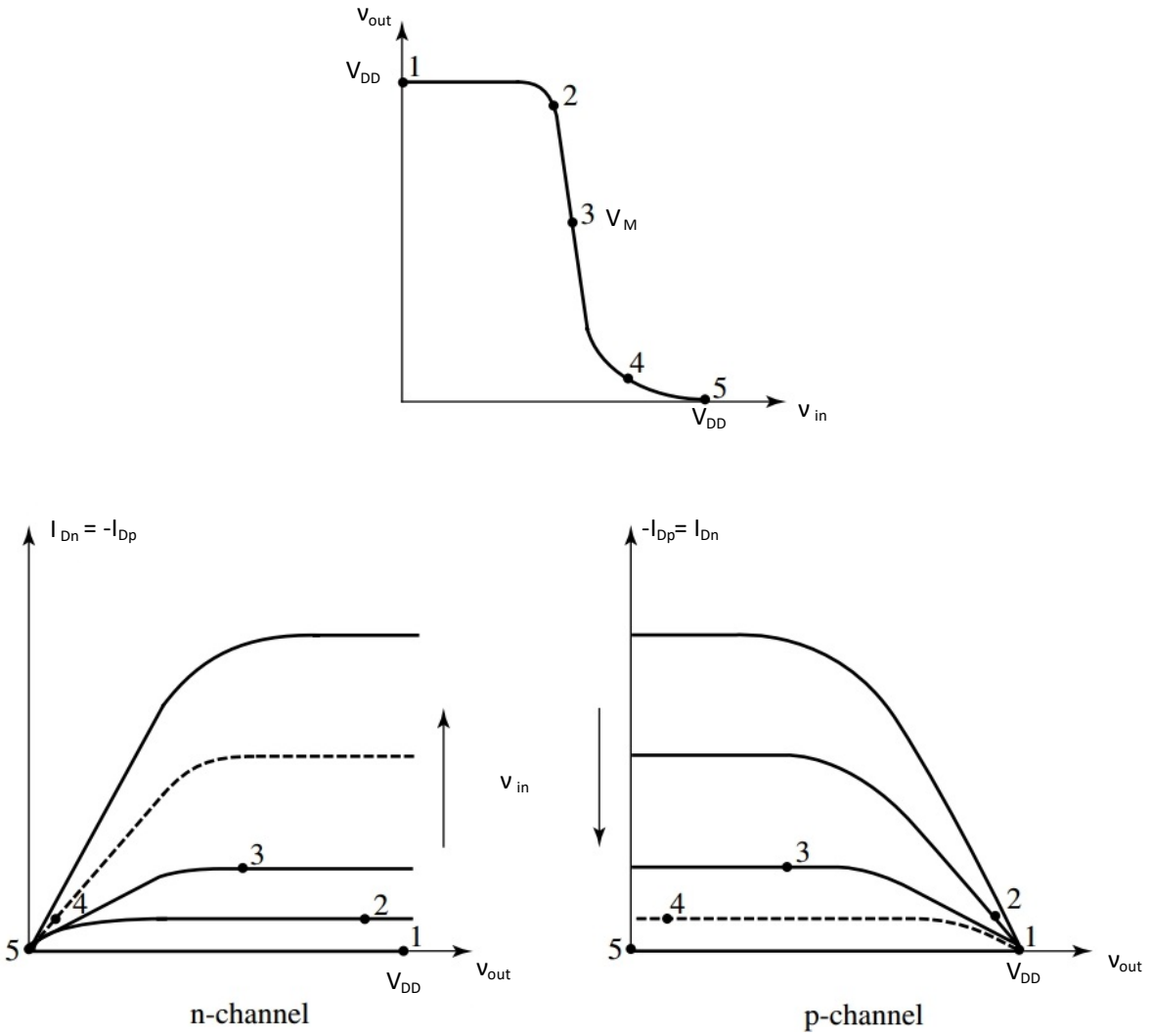

Figure 2.10. Inverter transfer curves. Adapted from [32], with permission.

By combining the two transfer curves of the nMOS and pMOS devices, the transition from high to low, as shown in Figure 2.10, is notable in that the incline of the curve between the high and low transition is not infinite, hence there is a time delay between the input signal, which is at a minimum value, and the output signal reaching the maximum value. This is shown in the first figure in Figure 2.10.

To calculate the propagation delay of the inverter, a definition is given of the time required to change from 10% of the bottom voltage value to 90% of the highest voltage value. The average between the rise (t_{PLH}) and fall (t_{PHL}) times in this window gives the averaged delay, as shown in (2.35).

$$t_p = \frac{t_{PHL} + t_{PLH}}{2} \tag{2.35}$$

A second parameter that is also important for inverter operation is the threshold voltage V_M where both the input and output voltages are equal [35] . When assuming that both devices are operating in the constant-current region, the following two equations are valid for the currents through each device. Equation (2.36) refers to the drain current of the nMOS device and (2.37) refers to the drain current of the pMOS device. For the work in this dissertation, device lengths of the biasing network exceeded the minimum feature size of the technology node, so the effect of velocity saturation was therefore not applicable. Quasi-ballistic transport will most likely not occur [17], hence long channel MOS device equations are used for the amplifier design.

$$I_{Dn} = \left(\frac{W}{2L}\right)_n \mu_n C_{ox}(V_M - V_{Tn})^2(1 + \lambda_n V_M) \tag{2.36}$$

$$-I_{Dp} = \left(\frac{W}{2L}\right)_p \mu_p C_{ox}\left(V_{DD} - V_M - V_{Tp}\right)^2\left(1 + \lambda_p(V_{DD} - V_M)\right) \tag{2.37}$$

Substituting the two variables shown in (2.38) and (2.39) into (2.36) and (2.37). Since I_{Dn} and I_{Dp} are equal, it can be deduced that (2.36) and (2.37) are equal to each other, resulting in (2.40) [35]. Here V_M is defined as the point where the input and output voltages are equal, a voltage midpoint.

$$k_n = \left(\frac{W}{L}\right)_n \mu_n C_{ox} \tag{2.38}$$

$$k_p = \left(\frac{W}{L}\right)_p \mu_p C_{ox} \tag{2.39}$$

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}\left(V_{DD} + V_{Tp}\right)}{1 + \sqrt{\frac{k_p}{k_n}}} \tag{2.40}$$

To find the gain of the inverter when the input voltage is equal to V_M, the small-signal model of both MOS transistors are used, as shown in Figure 2.11 [32].

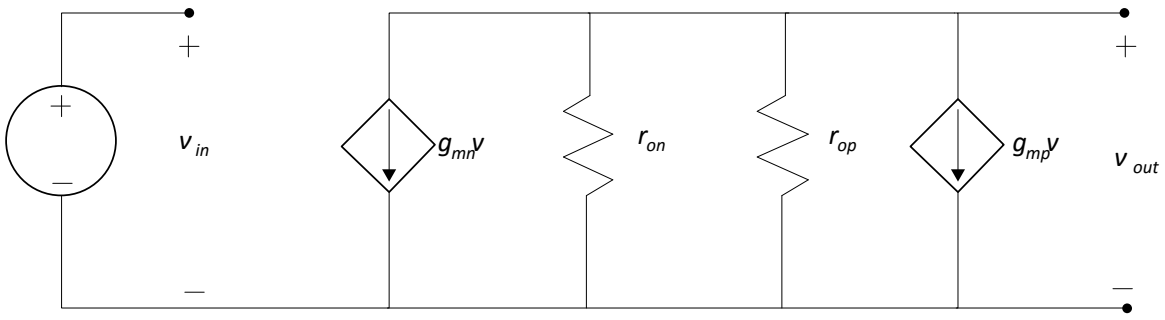

Figure 2.11. CMOS inverter small-signal model.

Figure 2.11 shows the small-signal model for a CMOS inverter, used to determine the small signal gain of the inverter.

The transconductance and the output resistance of the nMOS and pMOS devices at this operating point are shown in (2.41), (2.42), (2.43) and (2.44) respectively [35].

$$g_{mn} = k_n(V_M - V_{Tn}) \tag{2.41}$$

$$r_{on} = 1/(\lambda_n I_{Dn}) \tag{2.42}$$

$$g_{mp} = k_p\left(V_{DD} - V_M + V_{Tp}\right) \tag{2.43}$$

$$r_{op} = 1/(\lambda_p I_{Dp}) \tag{2.44}$$

The gain of the inverter is then considered the relation that the output voltage has to the input voltage, and is shown in (2.45) [35].

$$A_v = -(g_{mn} + g_{mp})(r_{on}||r_{op}) \tag{2.45}$$

For the gain formula as shown in (2.45), it should be noted that an assumption was made that the transition curve between the output high and low value of the inverter is a linear line, with no exponential curve.

2.9 NOISE-TO-PHASE NOISE RELATION

The noise-to-phase noise relation of the amplifier is also an important concept to consider. Since the LNA sequentially follows the oscillator in the ring, the degradation of the phase noise caused by the LNA must be considered. According to [36], the phase noise of the oscillator signal is degraded exactly by the NF of the RF sequence following it, as shown in (2.46) to (2.48).

$$\mathcal{L}_{\phi}[dBc/Hz] = SNR_{OUT}(dBc) \tag{2.46}$$

$$SNR_{OUT}(dBc) = -177\ dBm - P_{IN}(dBm) + NF_{DUT}(dB) \tag{2.47}$$

$$NF_{DUT} = SNR_{OUT} - SNR_{IN} \tag{2.48}$$

2.10 OSCILLATOR BANDWIDTH

The bandwidth of an oscillator is application-dependent, with some applications requiring a narrowband oscillator, whereas other applications require a wider-band oscillator able to tune over several hundred MHz or a couple of GHz. The oscillator tuning bandwidth is calculated in (2.49), where f_{max} is the maximum oscillation frequency, f_{min} is the minimum oscillation frequency and f_c is the centre oscillation frequency. This then gives a tuneable bandwidth, denoted by $f_{bw.}$

$$f_{bw} = ((f_{max} - f_{min})/(f_c)) * 100\% \tag{2.49}$$

CHAPTER 3 RESEARCH METHODOLOGY

3.1 CHAPTER OBJECTIVES

In this chapter, the research methodology used in this research is discussed. For this method, the research hypothesis, mathematical modelling, computer-aided design (CAD) and the IC fabrication process are discussed. A comparison between the modelling and the final IC prototype model has been used to validate the hypothesis. The mathematical models, CAD software and measurement set-up of the final prototype are discussed in this section.

3.2 RESEARCH METHODOLOGY

The research methodology followed in this research is presented graphically in Figure 3.1.

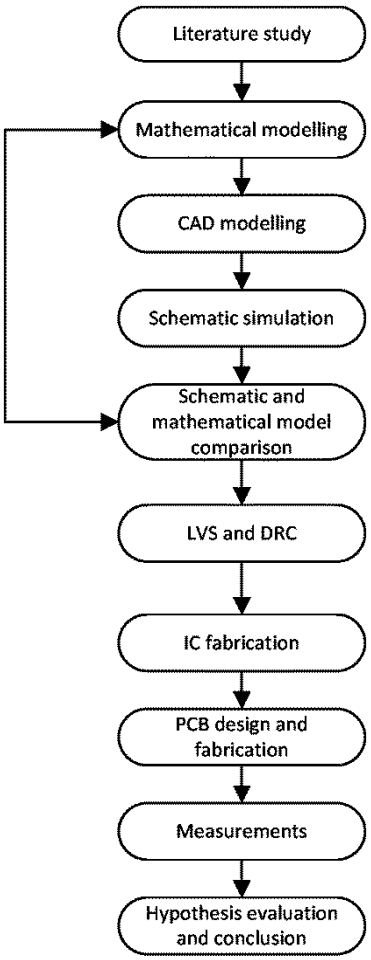

Figure 3.1. Research methodology.

The research methodology process started with a literature study, presented in Chapter 2. The fundamental theories of single-ended and double-ended ring oscillators were discussed. The background to NFs, phase noise, phase noise analysis methods and challenges relating to this work was also presented in this chapter.

Mathematical modelling and manual analysis were sufficient for first-level design and testing of both the oscillator circuit and the phase noise of the said circuit.

CAD tools were used for a two-step design verification. The first step was to compare the schematic simulations with the mathematical results, repeating these steps until correlation was achieved between the mathematical model and the simulation results. The literature review, simulations and mathematical model yielded predictions of the expected results of the prototypes. The second step involved the layout design and simulations. A layout versus schematic (LVS) software package was used to compare the schematic and layout designs. A design rules check (DRC) was done to verify no infringement on the design rules.

The design was then sent to a production house for fabrication. The resulting prototypes then served as a practical measurement platform to verify the simulation results. A PCB was designed to house the prototyped IC as well as the external biasing components. Measurements were taken of the prototyped IC housed on the PCB. The hypothesis was then validated based on the literature study, mathematical models and simulation results.

3.3 IC PROCESSES

For prototyping a circuit that implements the low phase noise oscillator, the 130 nm SiGe BiCMOS from IBM, namely the IBM8HP process, was used. Although the technology node available for student prototyping is not the smallest technology node available, it still allows for a good platform to test the hypothesis made in this research, as a relative measurement is added with a standard three-stage single-ended CMOS ring oscillator. Since the $1/f$ noise profile of the active device upconverts to the $1/f^3$ part of the oscillator's phase noise profile [7]; the SiGe HBT transistors were chosen over the CMOS devices because of their superior $1/f$ noise profile. Apart from being a BiCMOS process, it also houses five metal layers

available for interconnection. The bottom three layers are copper, while the top two layers are aluminium. The 130 nm process has an f_T of 200 GHz [8], [37], [38].

3.3.1. SiGe HBT characteristics

The high f_T device in the IBM8HP process has single-stripe emitter npn models (npn_inh) that support only geometries with a c-b-e-b-c layout [38]. While the emitter length can be varied from 0.52 µm up to 12 µm [36]. The emitters of these transistors are made from polysilicon while it also has a non-self-aligned extrinsic base [36]. The open base CE breakdown voltage of the transistor is a variable that limits the maximum voltage swing allowable [37]. Table 3.1 reflects the HBT used in the ring oscillators device characteristics.

Table 3.1 IBM8HP process NPN device characteristics.

Device parameters	Emitter dimensions L = 0.54 - 12 µm W = 0.12 µm
extrinsic r_e (Ω)	38 – 1.5
extrinsic r_b (Ω)	236 – 13
intrinsic r_b (Ω)	125 – 5
extrinsic r_c (Ω)	51 – 4
intrinsic r_c (Ω)	198 – 6
BE intrinsic cap (fF)	0.7 – 18
BE oxide cap (fF)	0.8 – 18
BC extrinsic cap (fF)	0.1 – 1.4
BC intrinsic cap (fF)	0.5 – 9
BC oxide cap (fF)	1 – 9
CS intrinsic cap (fF)	0.08 – 0.6
peak f_T I_C (mA)	0.8 – 17

Because of the NDA, exact values for the chosen model are not published in this dissertation. The values shown in Table 3.1 are from a variable table given in the PDK reference guide [38].

3.3.2. Inductors

Spiral inductors of 0.15–35 nH are available in the IBM8HP technology. Although no inductors are used in this ring oscillator design, they are usually present in other alternatives for low phase noise oscillators. One inductor, depending on the value, is several times the size of the complete oscillator circuit proposed in this work.

3.3.3. Capacitors

The IBM8HP technology provides fixed capacitance metal-insulator-metal (MIM) as well as several variable capacitance devices. For this design, only DC-blocking capacitors, as well as a kick-start capacitor, are used in the circuit. These capacitors are realised by making use of MIM capacitors which are single MIM capacitors with a nitride dielectric layer between two alumina plates. From Addendum B, it is easy to see that most of the space requirement goes towards housing the capacitors. It would thus be sensible to reduce the number of capacitors used in a design if the space requirement is very important. The model includes both the wiring parasitic resistance and capacitance values [7].

3.3.4. Resistors

Several types of resistors are available in the IBM8HP process, which include the diffusion resistor (*NS* diffusion), polysilicon (*RR* poly), metal plate resistor (*KQ BEOL*) and a second polysilicon resistor (*P+* poly). Here the poly-resistors have the highest sheet resistances and the diffusion resistor has the lowest sheet resistance value. For this design, the resistors are only required to be able to handle the current, not to have significant stray capacitances.

3.4 LNA MATHEMATICAL MODELLING

The LNA definition and modelling are beyond the scope of this research. The gain of a CMOS inverter amplifier with resistor feedback is, however, considered and modelled in this work using existing inverter mathematics as well as superposition to determine the closed loop gain of the amplifier when the feedback resistor is introduced.

3.5 PHASE NOISE MATHEMATICAL MODELLING

Leeson’s LTI phase noise model uses a full explanation of the up-conversion of device flicker noise to oscillator phase noise, near the oscillating frequency [32]. For this study, the ISF

method was used to evaluate the effect of various noise sources on the oscillator phase noise. Using this method of up-converting individual noise sources to oscillator phase noise provides greater insight into the design of the said oscillator. This enables a designer to optimise the oscillator for optimum phase noise by striving to minimise the major sources contributing to phase noise. A detailed mathematical phase noise analysis is given in section 4.4 for a two-stage single-ended SiGe HBT based ring oscillator. The mathematical model was analysed in Octave using the code provided in Addendum A. The simulation results were used for comparison with the CAD software simulation results.

3.6 SCHEMATIC DESIGNS AND SIMULATIONS

Virtuoso Schematic and Layout Editor from Cadence Design Systems were used for the schematic and layout design entries respectively. Assura was used for DRC and LVS verification. It is a software package integrated into the Cadence Virtuoso software suite.

The mathematical model derived for the phase noise of the oscillator needs to be verified against a simulation result. For this study, SpectreRF from Cadence Design Systems was used as a simulation programme with integrated circuit emphasis (SPICE) based simulator. With SpectreRF, the steady-state solution can be performed on the oscillator circuit. From the steady-state simulation option, the periodic steady state (PSS) was used to determine the oscillation frequency and the steady-state response of the oscillator [39]. This steady-state response could then be used to perform a phase noise analysis of the circuit [39]. The steady-state analysis is very useful for simulating time-invariant circuits.

These circuits do not have a linear time response for a given input, but rather a non-linear time-varying response for a no/constant given input signal. Oscillators fall into this category, as the output is constantly changing without giving a constant input to the oscillator, namely the bias and tuning voltages. The transient phase of the PSS is generated by monitoring two predefined nodes on this circuit. The PSS analysis is separated into two phases, namely the initial transient phase and the shooting phase. The simulator starts and restarts the simulation several times and each time a comparison is done between the two different simulation stages. When a correlation is obtained between these two stages, the steady-state analysis has been completed. SpectreRF thus computes the periodic steady state of an oscillator with the use of

PSS analysis. After the PSS analysis, the simulator linearises the circuit to obtain a time-varying linear system and then the simulator proceeds to calculate the noise power density.

3.7 PCB DESIGN AND LAYOUT

The wafer housing the IC was packaged in an 8 mm × 8 mm QFN package. Many vendors successfully use the QFN package in the sub-20 GHz range with input reflections better than -18 dB. This gives a good indication that the packaging method will have a minimal influence on the IC's connection to the biasing circuit on the PCB. To house this IC, a PCB was manufactured on a 0.2 mm Rogers laminate board with ENIG finishing. The schematic and layout design was done in Altium Designer 11. A photograph of the PCB is shown in Figure 3.2**,** with the biasing circuit and connectors.

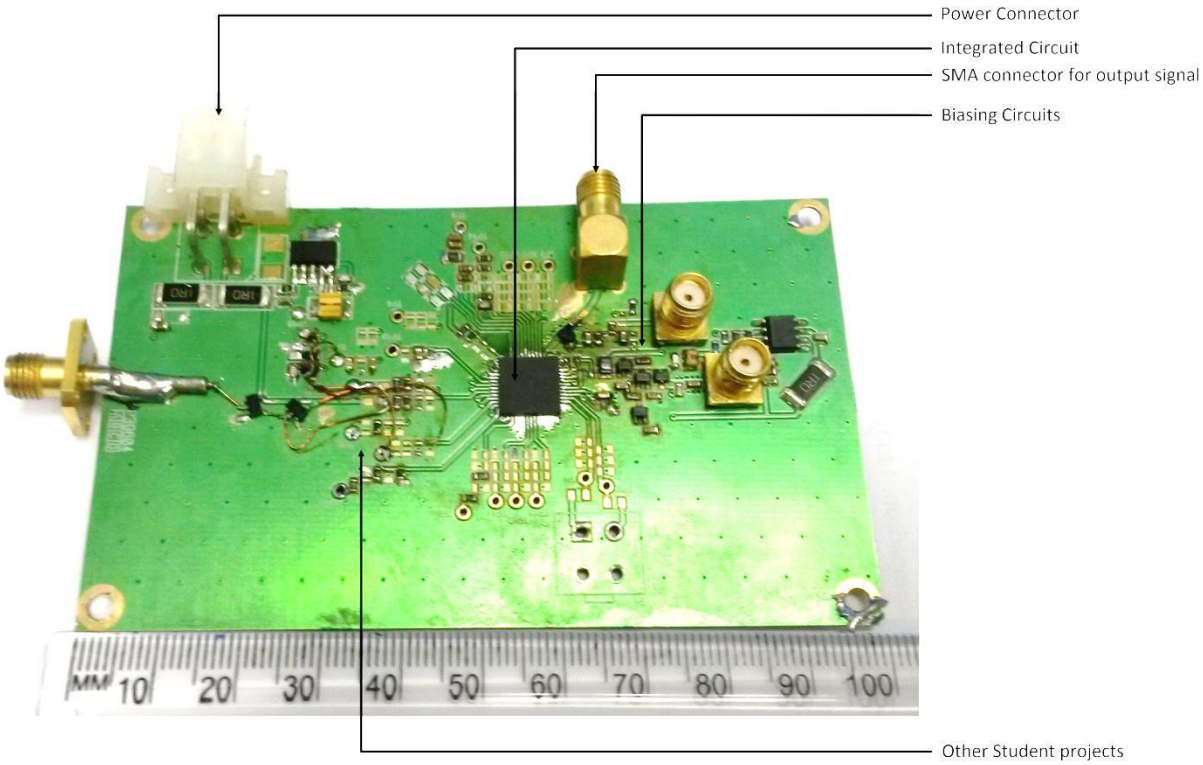

Figure 3.2. PCB with prototyped IC and biasing circuit.

A biasing circuit and a footprint housing the IC were required on the PCB, as well as an RF connector to feed the oscillator's output to a spectrum analyser. The black arrows in the photograph show the individual parts required for this project. The other components or non-fit components form part of other students' projects that were part of the multi-project wafer. These include filters, amplifiers, switch-mode power supplies and transistor measurements.

3.8 MEASUREMENTS SET-UP

Since the oscillator is packaged in a QFN package, no wafer probing is required. The measurement set-up is shown in Figure 3.3.

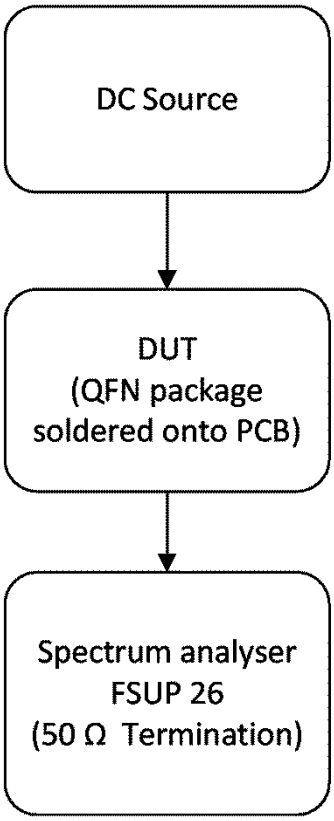

Figure 3.3. Measurement set-up block diagram.

A variable DC source is required to vary the DC bias voltage. Since the bias pin doubles as a frequency tuning pin, varying the bias voltage changes the oscillation frequency. The output of the oscillator is then connected to the input of a spectrum analyser that is able to measure phase noise via a 50 Ω coaxial cable.

Figure 3.4 shows the physical measurement setup used to test and verify the oscillator design.

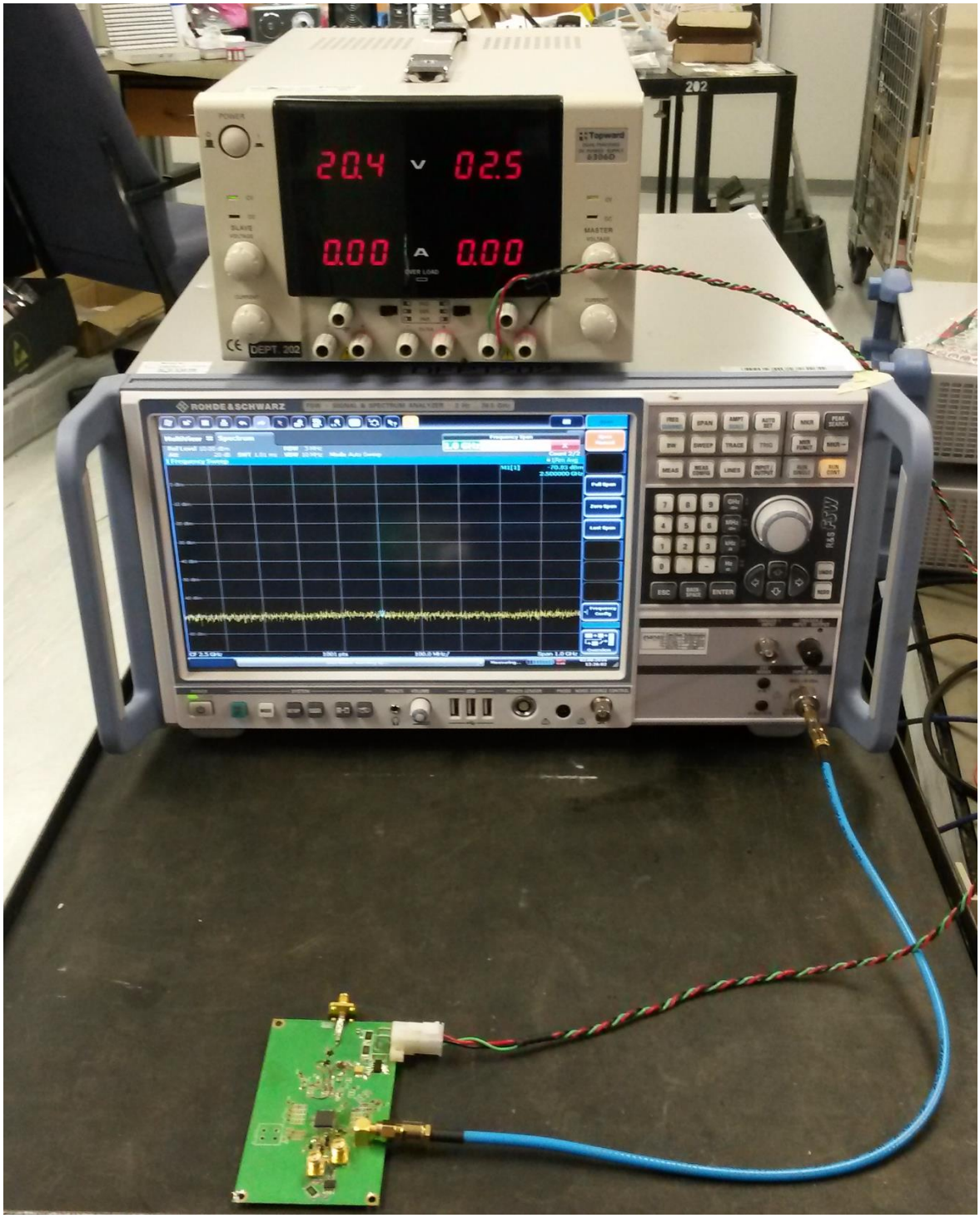

Figure 3.4. Physical measurement setup

A two-channel 30 V/3 A laboratory DC power supply from Topward was used for the DC source, the model number being 6306D. This is shown in Figure 3.4.

The signal spectrum analyser used to do the measurement is a Rohde and Schwarz signal spectrum analyser model number FSW26. The spectrum analyser has an internal cross-correlation path that cancels out any internally generated noise. This means the noise floor of the instrument is well below the phase noise floor of the oscillator.

3.8.1. Verification of fabricated IC

The design of the oscillator, discussed in Chapter 4 was done to enable further measurements and also to enable validation of the phase noise. The following devices were fabricated:

- a two-stage single-ended ring oscillator with LNA, and
- a two-stage single-ended ring oscillator with high impedance output.

Tests done on the prototyped oscillator included:

- testing the phase noise of the oscillator at the centre and edges of the band at 10 kHz and 1 MHz offset frequency,
- testing the power consumption of the oscillator,
- sweeping the oscillator over a wide band, to determine the tuning curve of the oscillator, and
- plotting the tuning curve over the frequency band to determine the linearity of the curve.

The tests and experimental procedure for the single-ended ring oscillator are shown in Table 3.2.

Table 3.2 Test and experimental procedures of a two-stage, single-ended HBT ring oscillator.

Objective	Procedure	Acceptance criteria
1) Phase noise test: To determine the phase noise of the oscillator at 10 kHz and 1 MHz offset frequencies from the carrier at the centre frequency of the band.	The oscillator was biased to oscillate in the middle of the band. The LNA version of the oscillator was connected to the signal source analyser and the phase noise was measured.	The device had to exhibit similar phase noise figures to the simulation and calculated values, and had to show improvement in the phase noise produced by the test circuit and/or other published circuits. The phase noise was tested at a 10 kHz offset and a 1 MHz offset to compare it with other published works.
2) Bandwidth test: To test the operational bandwidth of the oscillator.	The tuning voltage was varied while the oscillator was connected to a spectrum analyser. It was noted when the oscillator stopped functioning and the voltages and frequencies were recorded.	The device had to show wideband tuning ability, with operation in the 2 to 3 GHz region. The frequency had to change by varying the biasing voltage between 2 V and 4 V. The obtainable bandwidth was also compared with other published oscillators.
3) Power consumption test: To measure the power consumption of the oscillator over the whole band of operation.	The oscillator was biased without the LNA to function at the lower, mid- and upper frequency points. The current drawn by the oscillator was measured with a multimeter and the voltage was measured as well. The power was then computed.	The power consumption was calculated into the FOM and a good FOM indicated that the oscillator produced good phase noise figures for the power efficiency.
4) Output RF power test: To measure the output RF power of the oscillator LNA combination.	The oscillator was biased with the LNA to function in the middle of the band. After allowing the measurement to settle on the spectrum analyser, the peak power of the oscillating signal was measured.	The output power of the oscillator had to be higher than -10 dBm to be useful. The power was also factored into the FOM equation and a comparison with another oscillator provided a good indication of its functioning.

The experimental procedures presented in Table 3.2 provide detailed objectives for each test and the evaluation criteria used. The fabricated IC was placed on a PCB, which enabled integration with an external power supply and the measurement equipment. The oscillator's phase noise, bandwidth and power consumption were measured. The mid-band phase noise measurement determines the optimum phase noise performance that can be achieved.

3.9 TECHNICAL SPECIFICATIONS

For the hypothesis to be verified, a set of specifications needed to be deduced. The process for obtaining these specifications is shown in Figure 3.5.

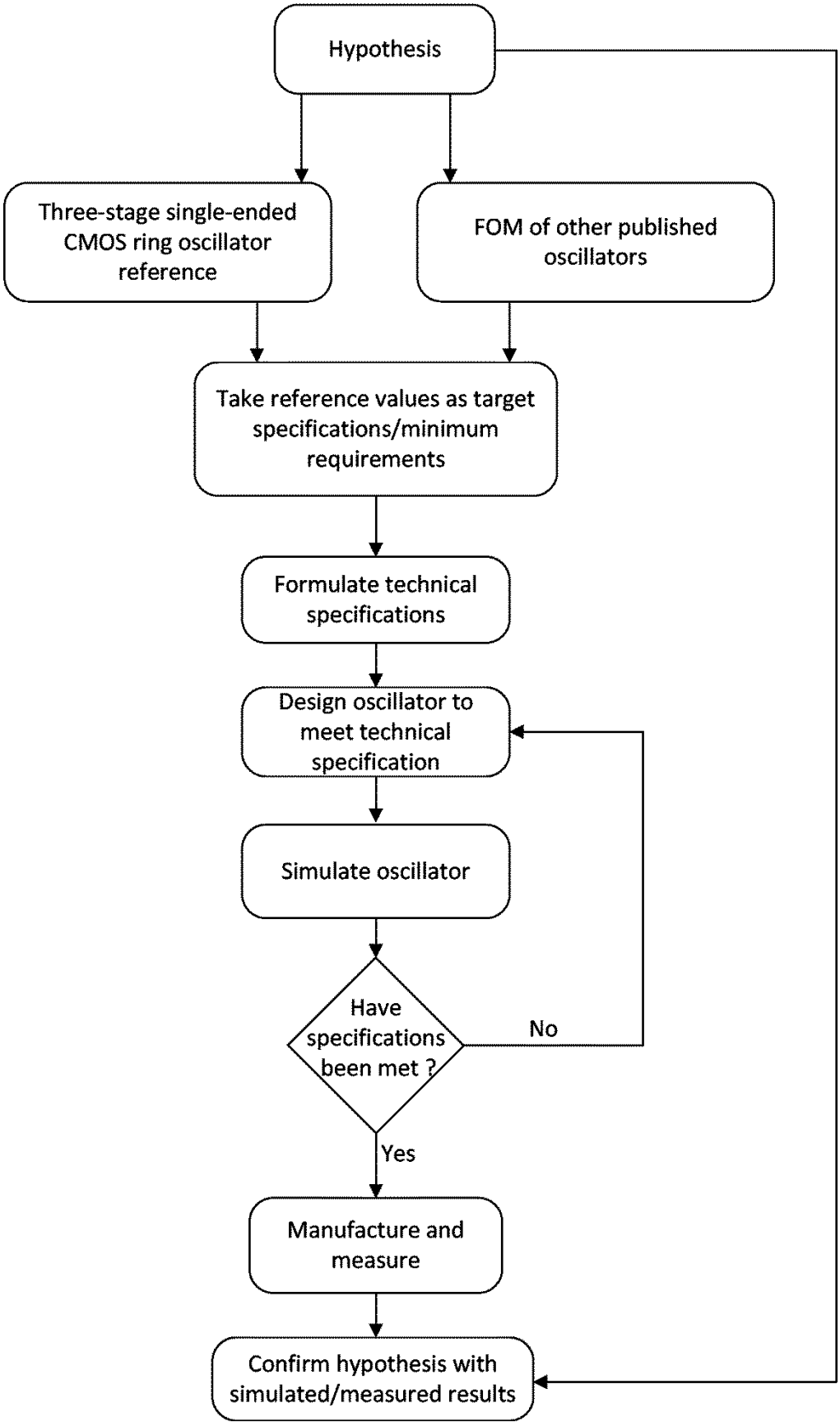

Figure 3.5. Technical specifications flow diagram.

The process started by considering the hypothesis. For this study, the main focus is the phase noise improvement obtained when using a SiGe HBT device in a single-ended ring oscillator structure. By then obtaining the phase noise measurement of a standard CMOS three-stage ring oscillator from the same technology node, a minimum requirement specification is obtained for the phase noise. A second control is done by obtaining the FOM of different oscillator structures in different technology nodes and different frequencies. By combining these two sets of specifications, a target specification is formulated for the oscillator design. The oscillator is then designed according to these specifications. Once the oscillator design has been completed, the specifications are verified by way of simulation. If the specifications have not been met, a redesign is done to improve on the unmet specifications. If the specifications have been met, the design goes on to the prototyping phase. The manufactured prototype is then measured and compared with the simulation results. If these results are comparable, the hypothesis will be verified and the study completed.

CHAPTER 4 MATHEMATICAL MODELLING AND SIMULATIONS

4.1 CHAPTER OBJECTIVES

The research study provided in Chapter 2 showed two major oscillator groups, namely the LC oscillator and the ring oscillator groups. It was shown in the referenced text [17], [26] that ring oscillators are an attractive technology solution, but they suffer from low phase noise performance. The topology selection for this study was not based on choosing the oscillator structure with the best phase noise performance, but rather by focussing on the ring oscillator structure and seeing whether its phase noise performance could be improved, since all other attributes of a ring oscillator improved its usefulness.

A detailed mathematical analysis of the two-stage single-ended ring oscillator is compiled in this chapter. For this work, the method used was to identify the major noise contributor in a classic CMOS ring oscillator and to seek an alternative. Since most CMOS ring oscillators are constructed purely from active pMOS and nMOS devices, it is safe to say these devices are inherently high-noise devices. An improved choice on the CMOS device would naturally be a device with lower device noise inherent in it – a device such as the SiGe HBT being a good choice.

It was decided that the best circuit layout for this research would be a single-ended ring oscillator with a minimum number of inverter stages. Classically, the minimum number of stages in a ring oscillator would be defined by (2.3), which shows that the minimum number of inverter stages required will be three. Since HBTs will be used to construct the ring oscillator, the general rule for minimum inverter stages set in (2.3) will be tested.

The delimitations and assumptions made in this section are discussed in section 1.6.

4.2 BARKHAUSEN STABILITY CRITERIA EXPANSION

If one were to consider the phase conditions of a single-ended ring oscillator stipulated in (2.2) and (2.3), it is easy to note that there is a contradiction between the Barkhausen stability

criteria and the operability of single-ended ring oscillators. In the majority of the cases a single-ended ring oscillator is constructed from an uneven number of inverter stages in series, as shown in Figure 2.2. This means the phase delay through these oscillators is a multiple of 180° and not a multiple of Barkhausen's prescribed 360°. An expansion of the Barkhausen stability criteria is thus proposed to account for the functionality of the single-ended ring oscillators. Equation (4.1) shows the proposed phase condition for the expanded Barkhausen stability criteria.

$$\emptyset = \begin{cases} n \times 360°, & for\ general\ oscillators \\ n \times 180°, & for\ ring\ oscillators \end{cases} \{n \in \mathbb{N}_0 \tag{4.1}$$

4.3 SINGLE-ENDED RING OSCILLATOR DESIGN

Since the main focus of this research is the single-ended ring oscillator, a ring oscillator with two inverter stages is suggested, as shown in Figure 4.1 (a).

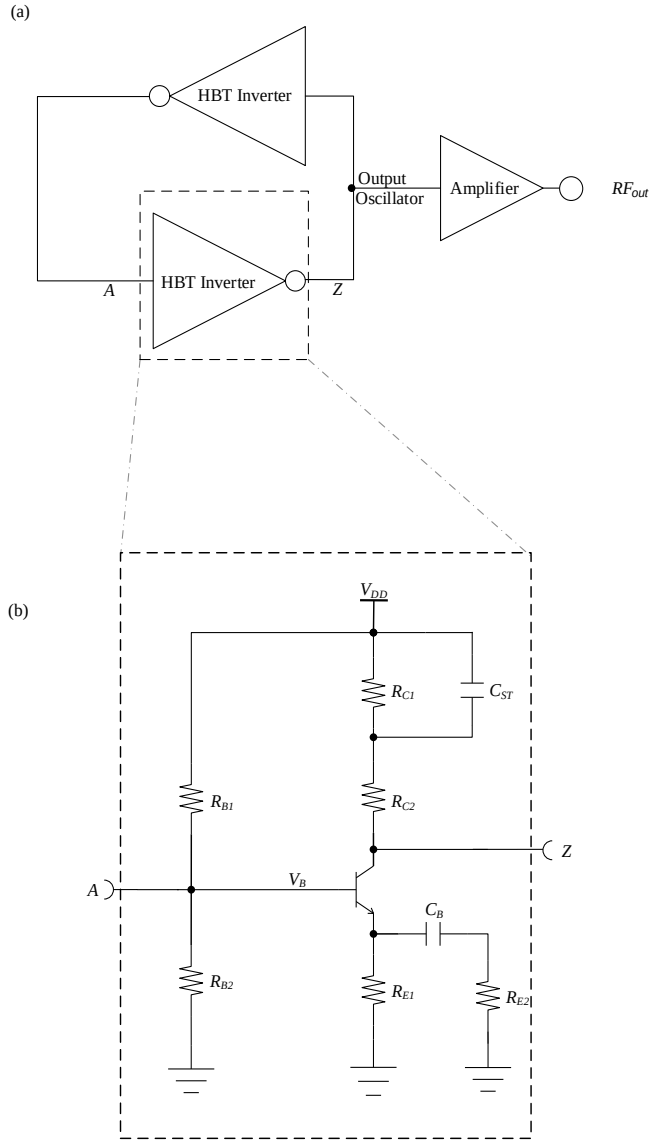

Figure 4.1. Two-stage ring oscillator.

(a) Two-stage ring oscillator structure. (b) HBT based inverter cell.

The inverter cells will be constructed from a single NPN type HBT device, as shown in Figure 4.1 (b). The passive devices surrounding the active device are used to bias the transistor in the forward-active mode. Equation (4.2) shows the base bias voltage circuit.

$$V_B = V_{DD}\left(\frac{R_{B2}//(B+1)(R_{E1} \parallel r_O)}{R_{B1} + R_{B2}//(B+1)(R_{E1} \parallel r_O)}\right) \tag{4.2}$$

Resistor R_{E1} is used to bias the emitter current of the transistor, as shown in (4.3), while both R_{E1} and R_{E2} are used in parallel to set the alternating current (AC) gain of the circuit. Both R_{E1} and R_{E2} are used to set the gain of the inverter. C_{ST} is used as an oscillator start-up mechanism

by delaying the charging time of the collector nodes at start-up for one of the inverter stages. This results in a transient between the output of this stage and the input of the second stage. The transient results in the circuit's start-up.

$$I_E = V_E \times R_{E1} \tag{4.3}$$

Assuming collector AC voltage is sinusoidal with amplitude A_e, the signal can be defined by an arbitrary initial phase constant, as shown in (4.4).

$$v_c(\theta) = A_e \cos(\emptyset) \tag{4.4}$$

If V_{BE} is defined as the DC voltage across the BE junction of the transistor, then the collector current is as shown in (4.5).

$$I_c(\theta) = I_s e^{\frac{V_{BE} - A_e \cos(\theta)}{V_T}} \tag{4.5}$$

In (4.5), I_S denotes the saturation current of the HBT, while the thermal voltage V_T can be calculated as shown in (4.6) and q denotes the electron charge constant.

$$V_T = \frac{k_B T}{q} \tag{4.6}$$

The transistor bias current, which should is also I_E is shown in (4.7) [6].

$$I_B = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_c(\theta) d\theta = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_S e^{\frac{V_{BE} + A_e \cos(\theta)}{V_T}} d\theta \tag{4.7}$$

Since the chosen oscillator topology is constructed from only two inverter stages, the circuit can settle to a non-oscillating state, since this structure is not inherently unbalanced like a three-stage CMOS ring oscillator. Since the oscillator is basically a high impedance circuit, another method that could also have been chosen is a kick-start method where a pulse is inserted into one of the inverter circuits. Ideally, an oscillator must start on its own. This

means there needs to be enough noise, in the band of interest, at the output fed back into the input of the oscillator. The oscillator should then amplify this noise and the output should be fed back into the oscillator, continually amplifying the signal until the amplitude limit of the amplifying part is reached. However, since this requirement is contrary to the low phase noise requirement, alternate ways of starting up the oscillator are used. The transient is calculated to correlate with the desired oscillation frequency, as shown in (4.8).

$$f_{ST} = \frac{1}{2\pi R_{C1} C_{ST}} \tag{4.8}$$

The amplifier is biased to work as a CE class-A gain stage, which allows for minimum distortion of the signal integrity while sacrificing the efficiency of the amplifier.

4.4 PHASE NOISE ANALYSIS

The three phase noise contributing noise sources in the SiGe HBT are the base current shot noise ($\overline{i_b^2}$), the base resistance thermal noise ($\overline{i_{r_b}^2}$) and the collector current shot noise ($\overline{i_c^2}$) [6], as shown in Figure 4.2.

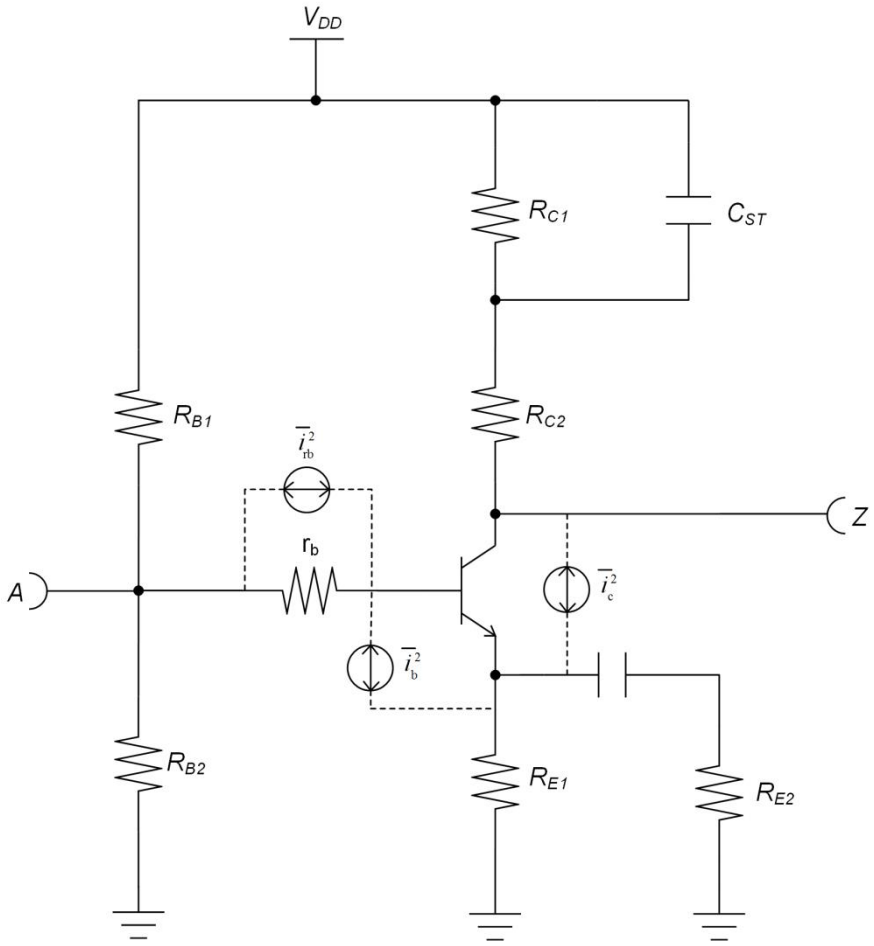

Figure 4.2. Active device noise sources.

The closed-form expression of the ISF is used to calculate each of these noise sources individually. This method works by injecting a current impulse in parallel to each of the noise sources and analysing the resultant impulse. Of these three noise sources, the base current shot noise will be disregarded, as its contribution to the phase noise is minimal [6].

4.4.1. Base resistance thermal noise contribution

In the case of the bipolar transistor, the major contributor to phase noise is the base resistance thermal noise [6]. Equation (2.26) for the base resistance thermal noise needs to be calculated, as shown in (4.9) [40]. The equations and variables for the ISF theory have been discussed in section 2.7.2; in this section only the parts that vary from the original theory are discussed.

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{\Gamma_{r_b,rms}^2}{q_{max}^2}.\frac{\overline{i_{r_b}^2}/\Delta f}{2\Delta\omega^2}\right] \tag{4.9}$$

To solve (4.9), the variables need to be calculated, as shown in section 2.7.2. Equation (4.10) shows how to calculate q_{max} [40].

$$q_{max} = A_c C_{max} \tag{4.10}$$

In (4.10), A_c represents the maximum voltage swing across the capacitance on the node when injecting a current impulse parallel to the base resistance r_b and C_{max} represents the maximum capacitance on the base node.

Next, the variables, namely i^2_{rb} and Δf, are considered simultaneously. The result of dividing the first variable by the second variable is the PSD of the Gaussian noise generated by the base resistance, as shown by (4.11) [40].

$$\frac{\overline{i_{r_b}^2}}{\Delta f} = \frac{4k_B T}{r_b} \tag{4.11}$$

The equivalent base resistance, or r_b, for one of the inverter stages is considered next. According to Table 29 [8], the values can be interpolated to obtain the base resistance for an HBT of a given size. The base resistance is defined by (4.12) [40].

$$r_b = R_C // R_{B1} // R_{B2} // (r_{be} + r_{bi}) // (\beta + 1)(R_{E1} // R_{E2}) \tag{4.12}$$

From (4.12), the base resistance is seen to consist of several individual impedance values. In (4.12), R_C represents the collector resistor of the previous inverter stage; the collector resistance of the previous stage's HBT is deemed large enough not to contribute to the base resistance, hence it is omitted from (4.12). Further, R_{B1} and R_{B2} are the base biasing resistors of the inverter stage, while r_{be} and r_{bi} are the intrinsic and extrinsic resistance values of the HBT, as given by the data columns in Table 29 [8].

The final closed-form expression was derived in [6] for a SiGe HBT used in a Colpitts oscillator configuration. Application of the same methodology for the given ring oscillator is given in (4.13) [40].

$$\Gamma_{r_b,rms}^2 = \frac{r_b^2 I_B}{4N^2 V_T R_L} \cdot \frac{B_1(2a_b)}{B_0(a_b)B_1(a_b)} \tag{4.13}$$

In (4.13), *N* denotes the number of noise sources; for a single-ended ring oscillator this will be one [6]. R_L is the load resistance on the collector node of the inverter, while I_B refers to the bias current flowing into the base node, as shown in (4.7). V_T refers to the thermal voltage of the HBT. All the variables have been solved for (4.13) and can now be substituted into (4.9), with the result shown in (4.14) [40].

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T I_B r_b}{2(A_c C_{\max})^2 \Delta\omega^2 N^2 V_T R_L} \cdot \frac{B_1(2a_b)}{B_0(a_b)B_1(a_b)}\right] \tag{4.14}$$

4.4.2. Collector current shot noise

The result of considering the collector current shot noise is shown in Figure 4.2. As for the case of base resistance, the thermal noise is shown in (4.9) and the ISF is shown in (4.15).

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{\Gamma_{i_c,rms}^2}{q_{max}^2} \cdot \frac{\overline{i_c^2}/\Delta f}{2\Delta\omega^2}\right] \tag{4.15}$$

In the case of a cyclo-stationary noise source such as $\overline{i_c^2}$, the ISF associated with $\overline{i_c^2}$ is replaced by an effective ISF, as shown in (4.16) [5], [6], [40].

$$\Gamma_{i_c,eff}(\theta) = \Gamma_{i_c}(\theta) \cdot \alpha_{i_c}(\theta) \tag{4.16}$$

In (4.16), the noise power dependence on θ is accounted for by including $\alpha_{i_c}(\theta)$. The expression for $\Gamma_{i_c}(\theta)$ was derived in [5] and is shown in (4.17) [40].

$$\Gamma_{i_c}(\theta) = \Gamma_{R_T}(\theta) = \frac{\sin\theta}{N} \tag{4.17}$$

The expression for $\overline{i_c^2}$ is given in [6] and shown in (4.18).

$$\overline{i_c^2} = 2qI_c(\theta)\Delta f \tag{4.18}$$

By combining (4.5), (4.16) and (4.18), the following can be derived:

$$\frac{\overline{i_c^2}}{\Delta f} = 2q\, I_s e^{\frac{V_{BE} - A_c\cos(\theta)}{V_T}} \equiv \frac{\overline{i_c'^2}}{\Delta f} \cdot \alpha_{i_c}^2(\theta) \tag{4.19}$$

Further, substituting (4.19) with the thermal voltage in (4.6) and the Bessel functions of the base emitter voltage in (4.21) will result in (4.22) [40].

$$a_c = \frac{A_c}{V_T} \tag{4.20}$$

$$V_{BE} = \ln\left(\frac{I_B}{I_S \cdot B_0(a_c)}\right) V_T \tag{4.21}$$

$$\frac{\overline{i_c'^2}}{\Delta f} = 2q\, I_s e^{\frac{V_{BE}}{V_T}} = 2q\frac{I_B}{B_0(a_c)} = \frac{2k_bT}{V_T}\frac{I_B}{B_0(a_c)} \tag{4.22}$$

It is also shown in [6] that (4.23) is true.

$$\alpha_{i_c}(\theta) \equiv \sqrt{e^{a_c\cos\theta}} \tag{4.23}$$

With these variables calculated, it is possible to calculate the effective ISF associated with the collector current shot noise, as shown in (4.24).

$$\Gamma_{i_c,eff}(\theta) = \Gamma_{i_c}(\theta) \cdot \alpha_{i_c}(\theta) = \frac{\sin\theta}{N}\sqrt{e^{a_c\cos\theta}} \tag{4.24}$$

Integrating (4.24) over one oscillation period and dividing it by 2π will give the root mean square of the collector current shot noise ISF, as shown in (4.25) [40].

$$\Gamma_{i_c,eff,rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} \Gamma_{i_c,eff}^2(\theta)d\theta = \frac{1}{2\pi}\cdot\frac{(1-n)^2}{N^2}\int_0^{2\pi} \sin^2(\theta)\, e^{a_c\cos(\theta)}d\theta \tag{4.25}$$

The trigonometric identity provided in (4.26) means that (4.25) will be changed to (4.27) [41].

$$2\sin^2\theta = 1 - \cos(2\theta) \tag{4.26}$$

$$\Gamma^2_{i_c,eff,rms} = \frac{1}{4\pi}\cdot\frac{1}{N^2}\cdot\left[\int_0^{2\pi} e^{a_c\cos(\theta)}d\theta - \int_0^{2\pi} e^{a_c\cos(\theta)}\cos(2\theta)\,d\theta\right] \tag{4.27}$$

In (4.27), the first term results in a constant value while the second term can be resolved by making use of the Bessel functions. By substituting the first integral with $B_0(x)$ and the second integral with $B_2(x)$ the Bessel identity shown in (4.28) is used to solve the equation.

$$B_0(x) - B_2(x) = \frac{2}{x}B_1(x) \tag{4.28}$$

This reduces (4.27) to (4.29) [40].

$$\Gamma^2_{i_c,eff,rms} = \frac{1}{2N^2}[B_0(a_c) - B_2(a_c)] = \frac{1}{N^2}\cdot\frac{1}{a_c}B_1(a_c) \tag{4.29}$$

Multiplying (4.29) by $\overline{i_c'^2}$ results in (4.30) [40].

$$\Gamma^2_{i_c,eff,rms}\cdot\overline{i_c'^2} = \frac{1}{N^2}\cdot\frac{2k_BT}{V_T}\cdot\frac{I_B}{a_c}\cdot\frac{B_1(a_c)}{B_0(a_c)} = \frac{1}{N^2}\cdot\frac{k_BT}{R_T} \tag{4.30}$$

Substituting the numerator in (4.15) with (4.30) produces the phase noise contribution of the collector current shot noise, as shown in (4.31).

$$\mathcal{L}_{i_c}(\Delta\omega) = 10\log\left[\frac{k_BT}{2NR_TC^2A_c^2\Delta\omega^2}\right] \tag{4.31}$$

4.4.3. Total phase noise calculation

To reduce the formula for total phase noise, $1/f^2$ exhibited by the two-stage SiGe HBT ring oscillator can be obtained by adding (4.14) and (4.31) together, which results in (4.32).

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T I_B r_b}{2(A_b C_{\max})^2 \Delta\omega^2 N^2 V_T R_L} \cdot \frac{B_1(2a_b)}{B_0(a_b)B_1(a_b)}\right] + 10\log\left[\frac{k_B T}{2NR_T C^2 A_c^2 \Delta\omega^2}\right] \quad (4.32)$$

To simplify the log expression shown in (4.32), the log simplification rule can be used to change the summation of two log terms to a single log term where the log expressions are multiplied together, as shown in (4.33) [41].

$$\log_x y + \log_x z = \log_x yz \quad (4.33)$$

Using the logarithmic rule shown in (4.33) and applying it to (4.32) results in (4.34) [40].

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T I_B r_b}{2(A_b C_{\max})^2 \Delta\omega^2 N^2 V_T R_L} \cdot \frac{B_1(2a_b)}{B_0(a_b)B_1(a_b)} \cdot \frac{k_B T}{2NR_T C^2 A_c^2 \Delta\omega^2}\right] \quad (4.34)$$

4.4.4. Optimising the oscillator design for maximum phase noise performance

Unlike the Colpitts oscillator, the phase noise can be optimised by inspecting the closed-form ISF. The phase noise will be optimised by minimising base resistance and the bias current, while at the same time maximising the voltage swing on the output node and the load resistance. Conceptually, it is possible to see the most optimised structure for good phase noise performance, but the dependence these variables share with one other makes it difficult to optimise one variable without degrading another. A compromise had to be found between the variables to optimise the phase noise.

4.5 LOW NOISE AMPLIFIER

In section 2.8.1, the open loop gain of the CMOS inverter was described. Now consider the closed loop gain of the CMOS inverter amplifier with a feedback resistor. To calculate the closed loop gain, the superposition method is incorporated [42]. First, consider the transient equations of Figure 4.3 when v_{out} is connected to ground to calculate the input voltage of the inverter.

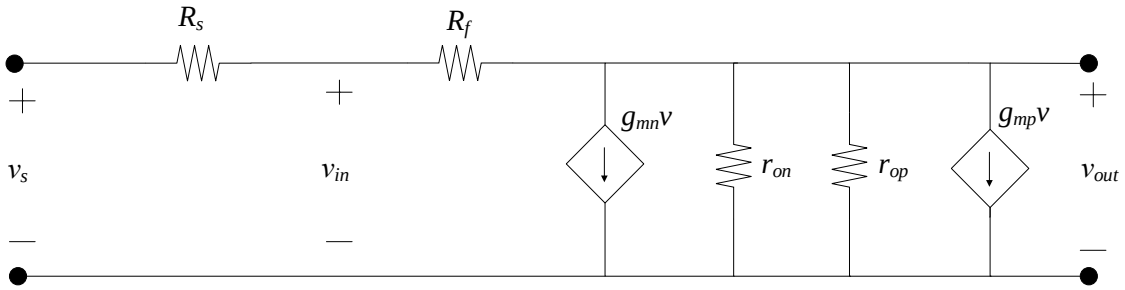

Figure 4.3. Small-signal model for CMOS inverter with feedback resistor.

Equation (4.35) is used to calculate the input voltage of the inverter. By considering Kirchhoff's voltage law for Figure 4.3, one obtains the input voltage in its relation to the output and source voltage [42].

$$v_{in} = \left(\frac{R_f}{R_f + R_s}\right) v_s + \left(\frac{R_s}{R_s + R_f}\right) v_{out} \tag{4.35}$$

Substituting the open loop gain in (2.45) into (4.35) results in (4.36).

$$A_{vc} = \frac{v_{out}}{v_S} = \left(\frac{\frac{A_{vo}R_f}{R_f + R_s}}{1 - \frac{A_{vo}R_S}{R_f + R_S}}\right) \tag{4.36}$$

The second stage of the amplifier consists of a SiGe HBT based Darlington pair, as depicted in Figure 4.4.

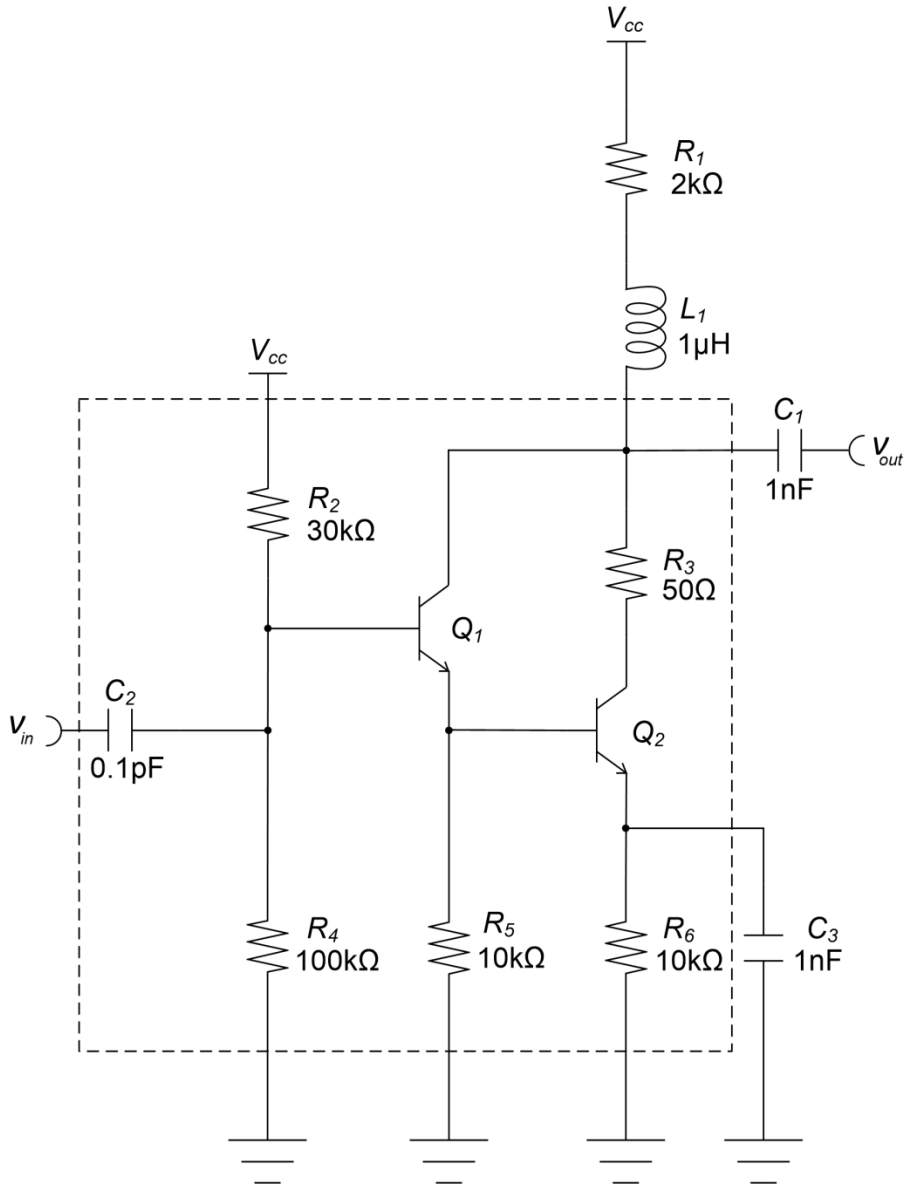

Figure 4.4. Second amplifier stage.

The primary requirement of this stage is to have high input impedance with a 50 Ω matched output impedance. The focus on current gain is higher than on voltage gain, since the first stage of the amplifier has amplified the signal into the desired area of operation. The small-signal model of the second amplifier stage is shown in Figure 4.5.

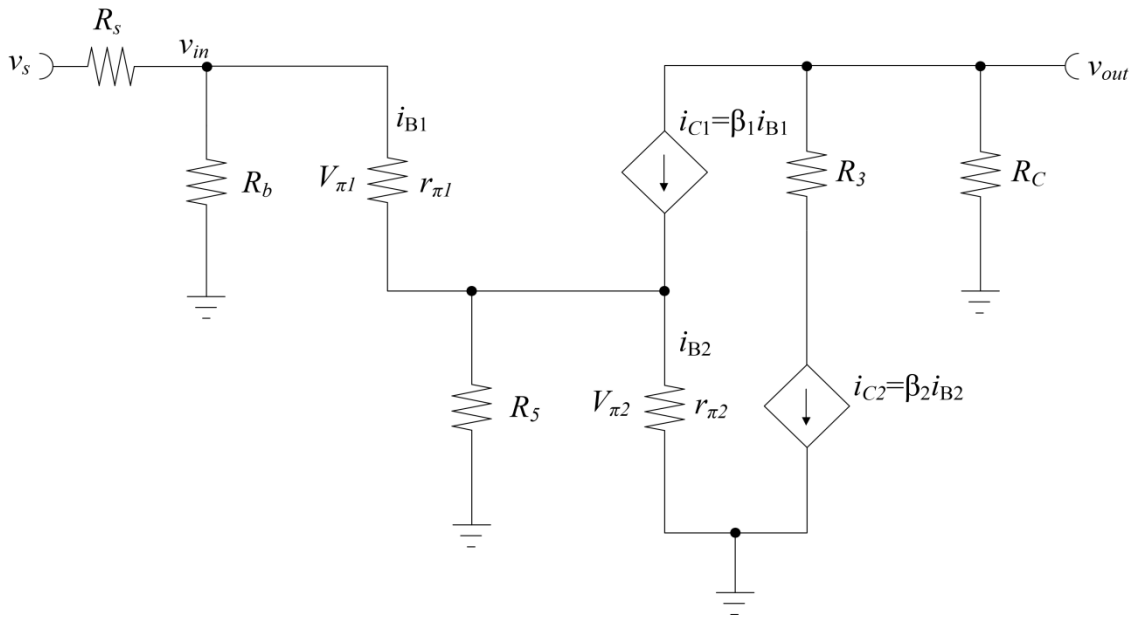

Figure 4.5. Second stage amplifier small-signal model.

The current gain equation of this stage can be easily calculated, as shown in (4.37).

$$i_{c2} = \beta_1 \beta_2 i_{b1} \tag{4.37}$$

Considering the output voltage swing over a 50 Ω load, the voltage is expected to drop slightly, but ultimately there must be a power gain, as shown in (4.38) to (4.40).

$$v_{out} = 50\beta_1 \beta_2 i_{b1} \tag{4.38}$$

$$v_{in} = i_{b1} R_{btot} \tag{4.39}$$

$$A_i = \frac{R_L i_{c2} \beta_1 \beta_2}{R_{btot}} \tag{4.40}$$

The second amplifier stage has a current amplification factor of 20 dB when loaded with a 50 Ω load, while the voltage amplitude drops by a factor of 26 dB. This means that the second stage does not have any power gain, but forms an impedance transformation buffer. This amplifier transforms from a high impedance input amplifier to a low impedance output amplifier, whereby only the current is amplified.

CHAPTER 5 RESULTS

5.1 CHAPTER OBJECTIVES

This chapter discusses the results obtained from this research. Simulations are shown for different parts of the oscillator. Photographs of both the layout and the manufactured IC are shown. The transient analysis, AC analysis and phase noise analysis results are provided here. Furthermore, a comparison is made with other published oscillators.

5.2 PROTOTYPED CIRCUIT

The circuit was prototyped with the 130 nm BiCMOS8HP process. Figure 5.1 shows two images. Figure 5.1 (a) shows an image of the layout in Cadence.

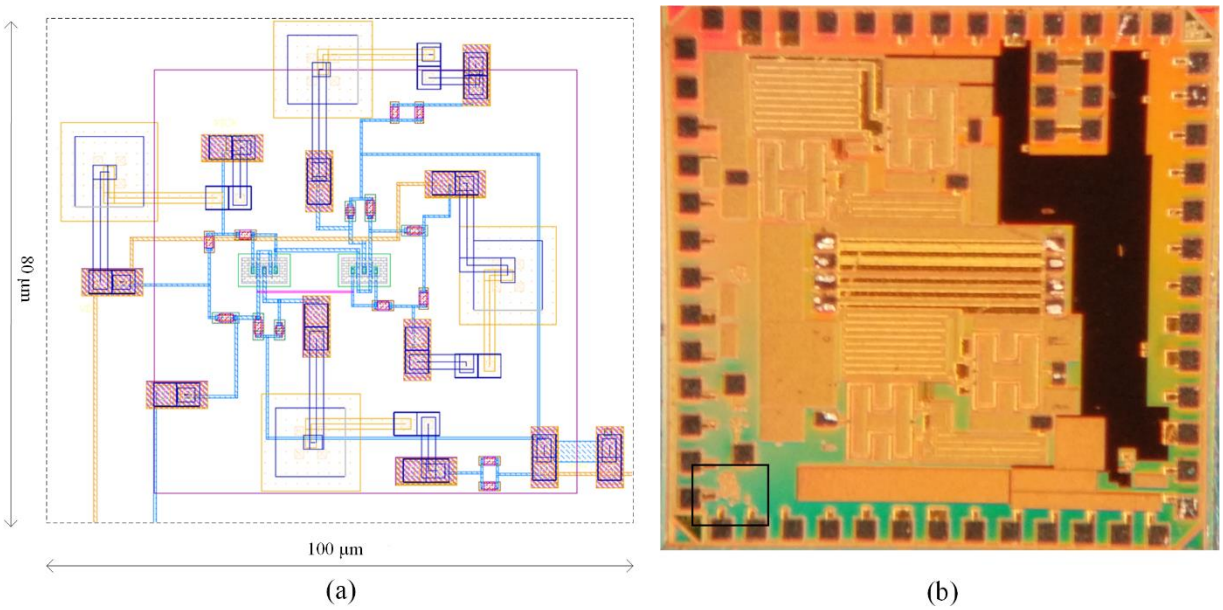

Figure 5.1. Circuit layout and photograph.
(a) Cadence layout image. (b) Photograph of prototyped integrated circuit.

The reader will note that the layout area is very small when compared with other oscillators with equal FOM. This shows that the total size of the oscillator is less than 0.008 mm^2. Figure 5.1 (b) shows a macro-photograph of the final prototyped circuit. The IC houses several different circuits and the small black frame in the bottom left corner shows both the oscillator circuit and the LNA circuit used for amplification and impedance transformation. Additional images of the layout are presented in Addendum B. The prototyped circuit did not function as the simulations did. As seen in Figure 5.1 (a), the traces connecting the individual components

are very thin. These traces include the ground connections. Since multiple MIM caps were used, the top metal layers of the process were used for MIM caps. When using both these smaller ground interconnects, an additional inductance value is seen at all the ground nodes indicated on the schematic and the real ground. Second, the process varied by -17% from the simulated values. These two issues seem to be the main reasons why the circuit did not function as the simulation did. By introducing a proper ground plane on one of the metal layers and leaving a cut-out for the MIM caps where they need to be, a better ground connection could be made. Second, the design can be made more immune to component variation and tolerances.

5.3 OSCILLATOR SIMULATION RESULTS

Simulations were conducted with SpectreRF in the Cadence environment, where all the SPICE models used for the parts in the constructed circuit were taken from the BiCMOS8HP library of parts. The parts used externally to the final IC are simulated with perfect parts where primarily capacitors and resistors are used for DC-blocking and resistors are used for biasing the circuit.

5.3.1. Transient analysis

A time domain analysis was done on the oscillator over a period of 10 ns and the results are shown in Figure 5.2.

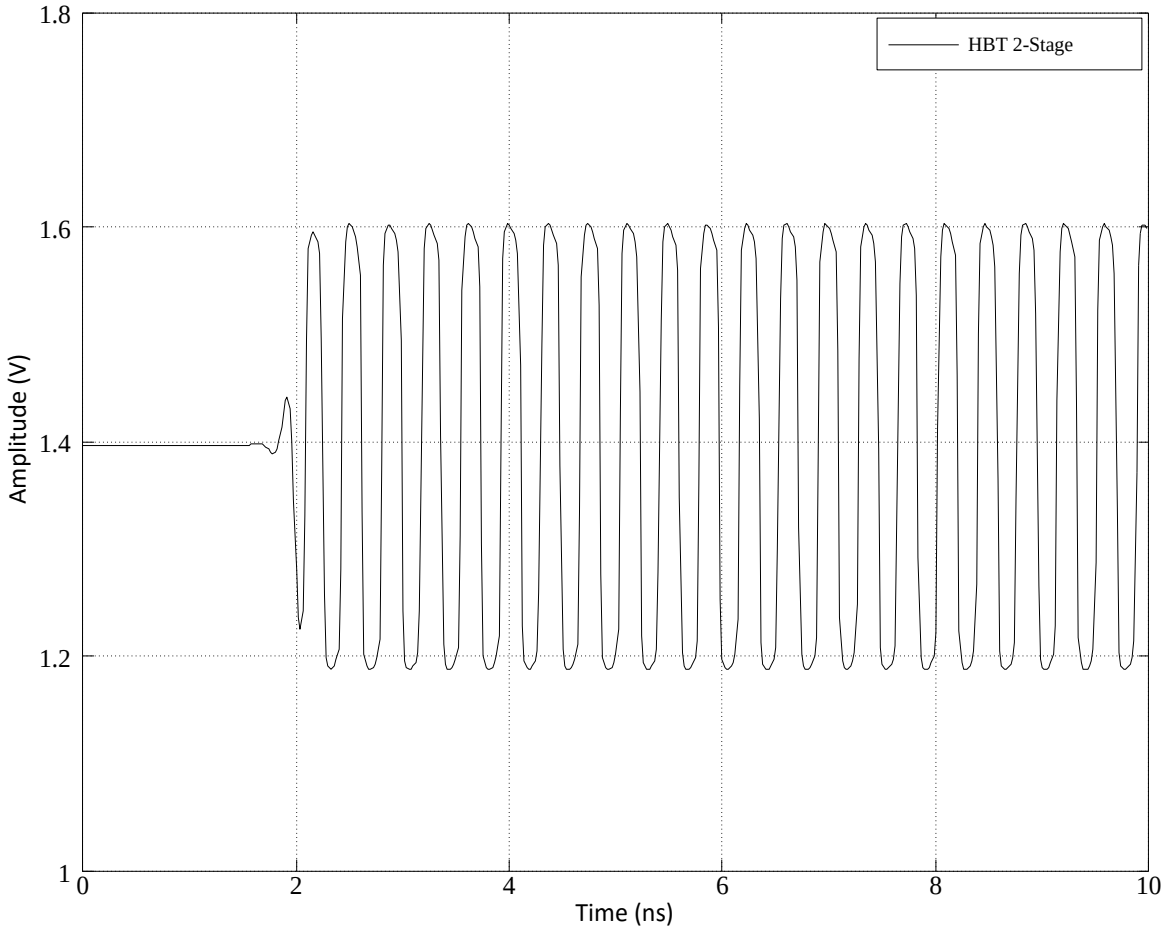

Figure 5.2. Oscillator time domain simulation results.

Figure 5.2 shows the start-up cycle of the oscillator. Start-up happens within the first 2.5 ns from the power being switched on. The first 1.8 ns, while the kick capacitor is charging up the oscillator, remains on a constant output voltage. Once the differential voltage is large enough between the input and output of the first inverter stage, the second inverter stage inverts the output of the first stage, thus triggering a continuous oscillating circuit. A second time domain figure is shown that is measured after the oscillator has started up and with a DC-blocking capacitor, as shown in Figure 5.3.

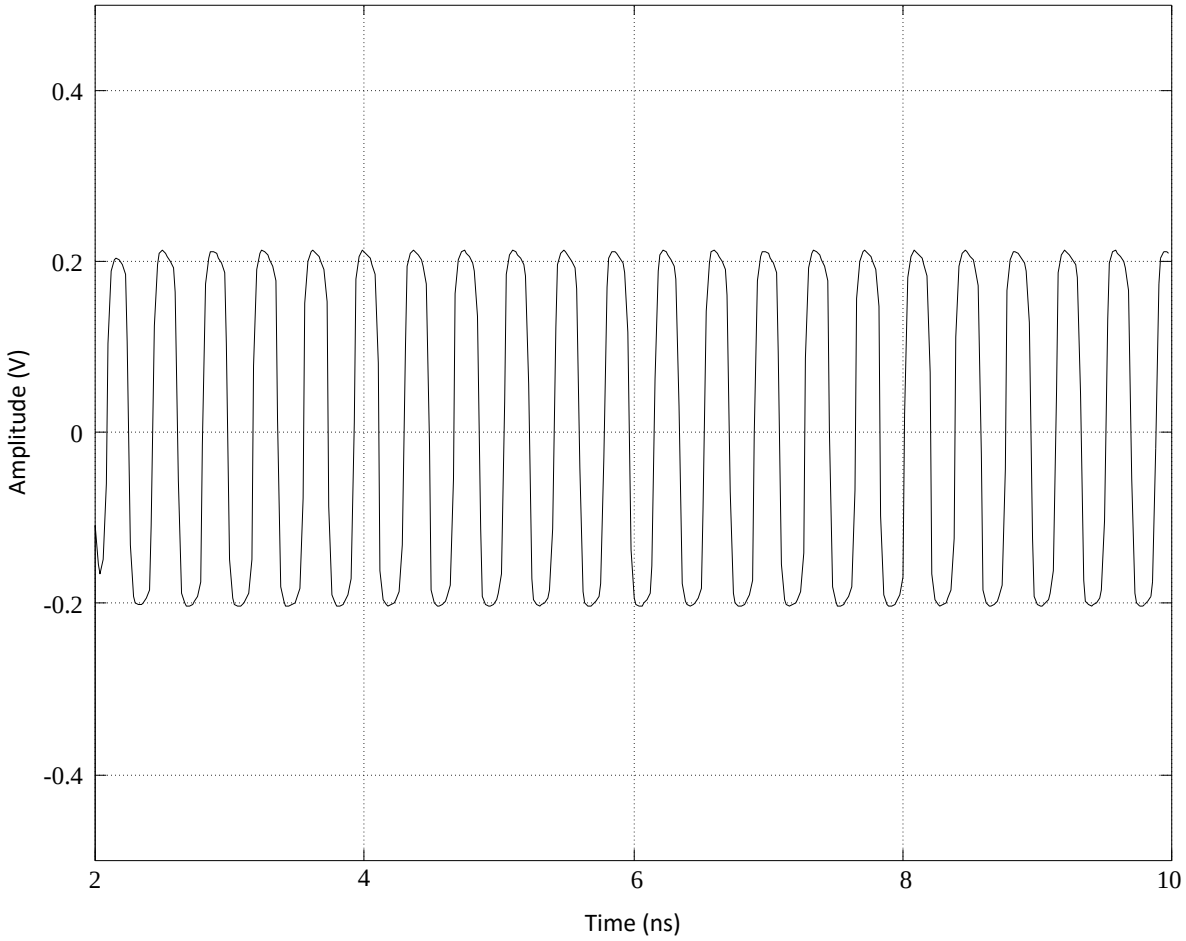

Figure 5.3. Oscillator time domain simulation after DC-blocking capacitor.

The DC is removed from the signal for both measurement purposes and doing a fast Fourier transform (FFT) on an AC-only signal.

By analysing the time domain signal as shown in Figure 5.2, it is shown that the oscillator, once started, reaches its maximum amplitude within three oscillation cycles, indicating that the gain for individual stages is more than sufficient to maintain the oscillation. Second, by looking at the waveform itself in Figure 5.2, it looks as if the HBT goes into compression at the 1.2 V mark, resulting in a rounder wave at the bottom of the waveform. This is expected from theory, since this is the point where the transistors start to saturate and approximate a 0 V CE voltage. Since the impedances on the collector node and emitter node are of similar value, this voltage is expected to be half of the supply voltage. This phenomenon will produce spurs in the frequency domain; although they are expected to be present, they are also expected to be multiples of the base oscillation frequency. These spurs fall well outside the band of operation, and would otherwise be filtered out easily for real world applications. These can also be seen in section 5.3.2. From Figure 5.2 one can also estimate the oscillation frequency. By looking at

the waveform between 4 and 5 ns, it is seen that the wave completes close to 2.5 oscillation cycles in 1 ns of time. Dividing the number of oscillations over the time taken by the oscillations shows the oscillation frequency. For the case of Figure 5.2, the oscillation frequency of 2.5 GHz is obtained. Although just an estimation, it shows that the frequency of oscillation is close to the desired frequency. The steady-state analysis conducted in Cadence also resolves the circuit to oscillate at 2.5 GHz.

5.3.2. AC analysis

To consider the frequency domain of the oscillator, an FFT is done in Octave on the data of Figure 5.3. The DC biasing has been removed from this simulation, as there is a DC-blocking capacitor at the output of the oscillator, removing any DC component still present on the signal. The AC simulation result is shown in Figure 5.4.

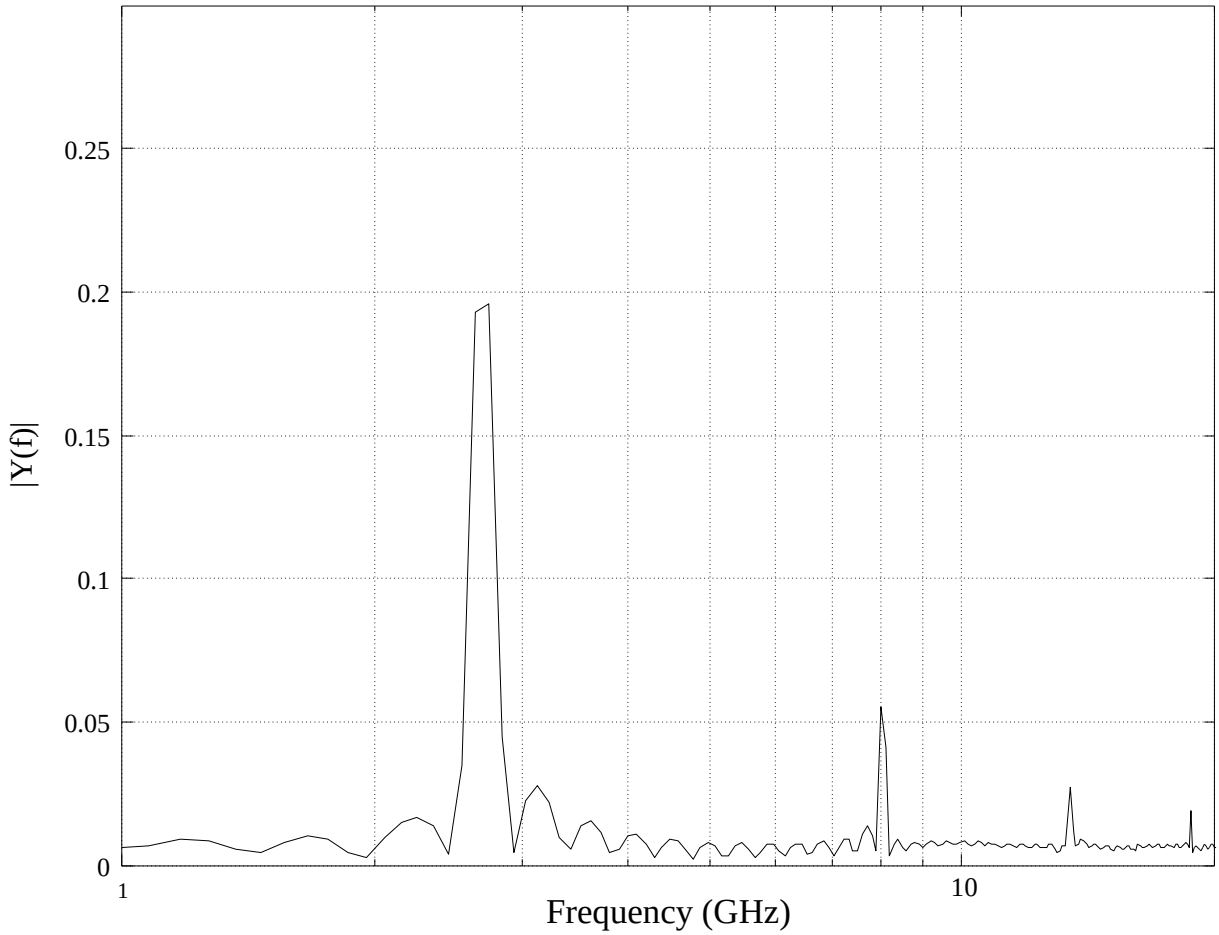

Figure 5.4. Oscillator AC simulation results.

From Figure 5.4, one will observe that the main oscillation frequency is close to the 2.5 GHz frequency of oscillation, which correlates with the estimation done in section 5.3.1.

The bandwidth of the oscillator was determined with the simulation. Adjusting the bias voltage of the oscillator, denoted by V_{DD} in Figure 4.1 (b), changes the oscillation frequency. This oscillator has a wide tuning range, with the average K_v being 730 MHz/V. The tuning curve of the oscillator is shown in Figure 5.5.

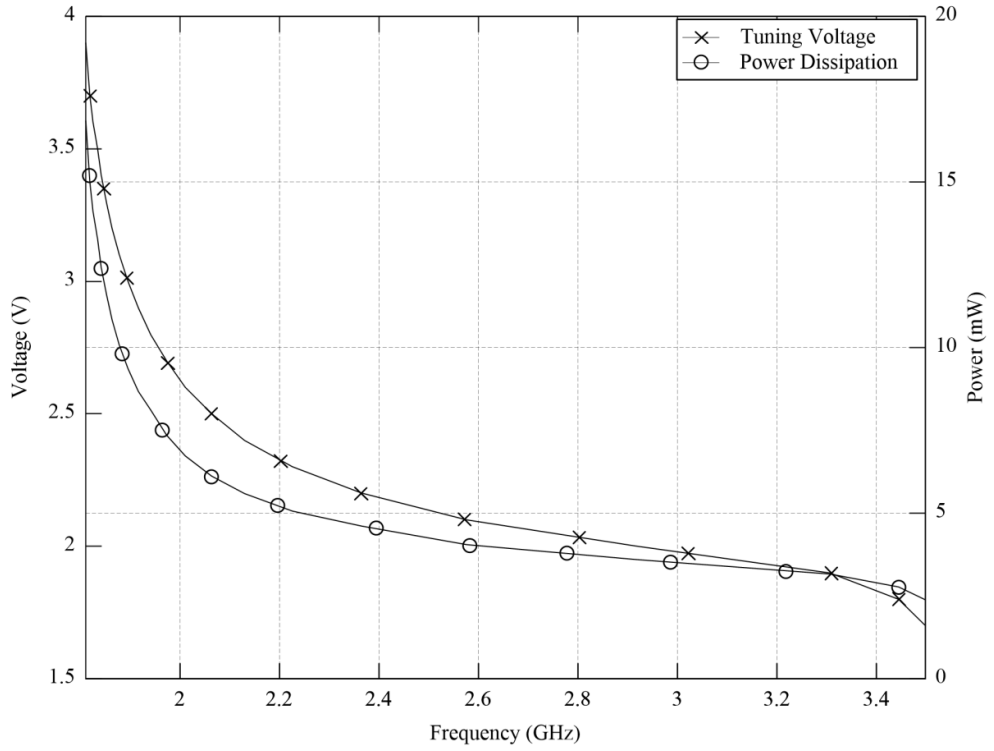

Figure 5.5. Power/K_v vs Frequency plot.

The tuning curve shows a 72% tuning bandwidth, which is comparable with other CMOS ring oscillator [24] . The high linearity of the tuning curve in the 2 to 3 GHz band is beneficial to good wideband phase noise performance when locking the VCO with a phase lock loop (PLL) [3]. This means there is no need to vary the loop filter or charge pump current in the PLL dynamically with frequency variation [43]. To vary the frequency of the oscillator, the V_{DD} of both inverter stages shown in Figure 4.1 (a) needs to be varied, as shown in Figure 5.5.

This method of frequency tuning has a direct impact on the power consumed by the oscillator. The power consumption of the oscillator is plotted on a separate curve in Figure 5.5.

5.3.3. Phase noise analysis

Running the phase noise analysis with SpectreRF in the Cadence environment with the noise setting on maximum produces the phase noise results shown in Figure 5.6.

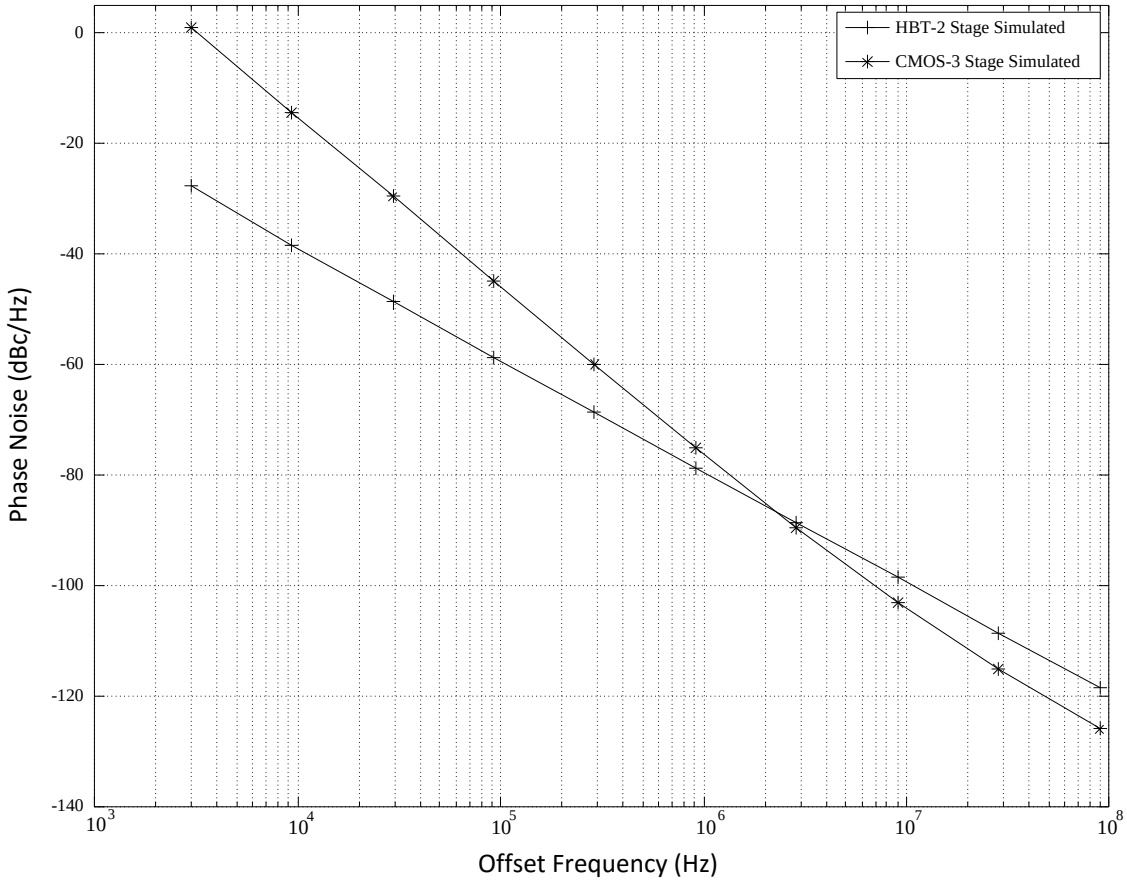

Figure 5.6. HBT and CMOS ring oscillator phase noise comparison.

The first step is to compare the simulated phase noise of the two-stage single-ended HBT ring oscillator with the simulated phase noise of the three-stage single-ended CMOS ring oscillator. From Figure 5.6, it is seen that the SiGe ring oscillator does have a major phase noise advantage over the CMOS oscillator at low offset frequencies. Since the CMOS oscillator has a higher quality-factor (Q-factor), it has a steeper gradient on its phase noise profile. This means that at offset frequencies higher than 2.5 MHz, the CMOS oscillator produces better phase noise performance. A logical extrapolation to be made here is that if a two-stage single-ended ring oscillator was realisable here the phase noise gradient would follow the same curvature. A higher number of HBT inverters could also have been used for the SiGe-based oscillator, but this would reduce both the oscillation frequency, (2.4), and the bandwidth. An in-depth phase noise FOM comparison is done in section 5.3.4.

Second, the phase noise simulated in SpectreRF for the SiGe HBT oscillator is compared with the mathematical equations for the phase noise as derived in section 4.4.3. The results are shown in Figure 5.7.

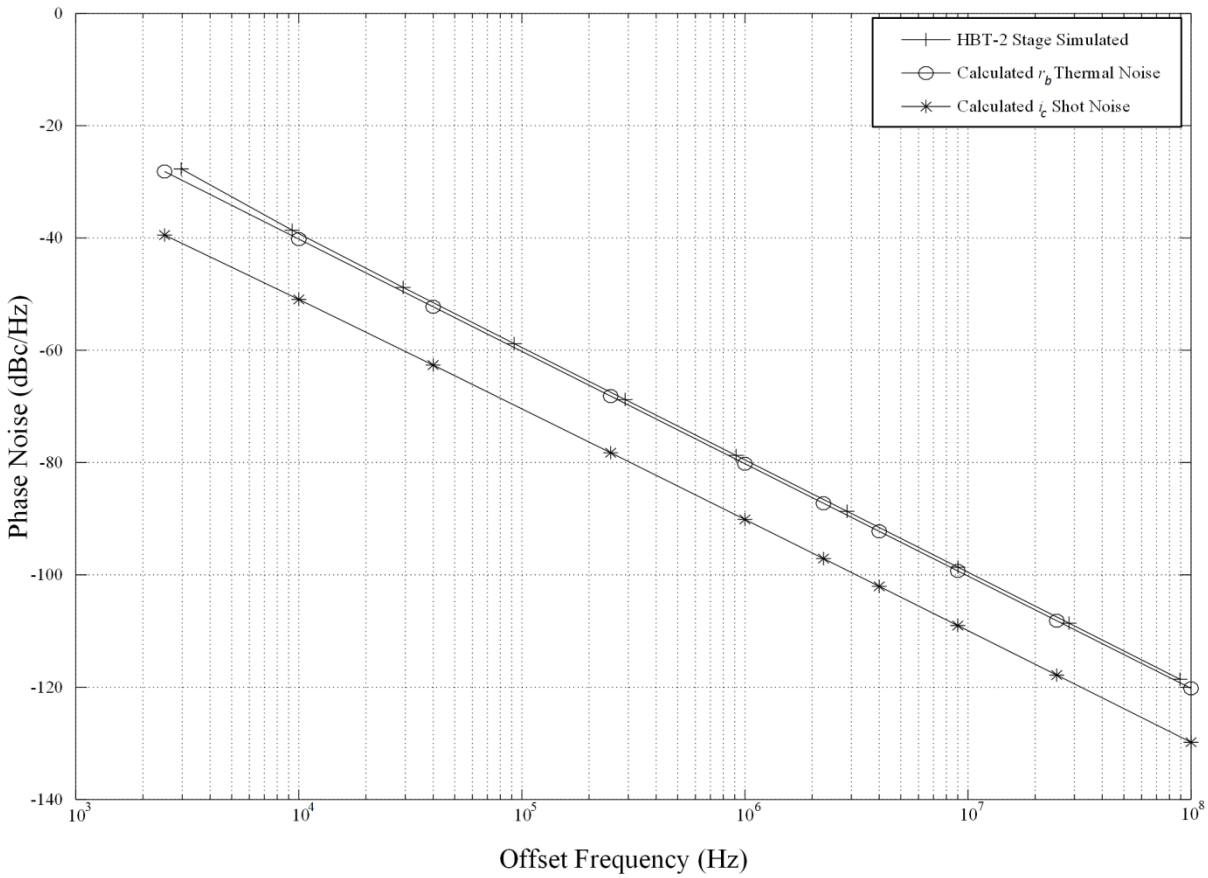

Figure 5.7. Calculated phase noise sources vs simulated phase noise.

Figure 5.7 shows that most of the phase noise is caused by the carrier density fluctuations in the base resistance, which correlates with other findings [32], [44]. This result correlates with the results obtained in [24]. The ISF method for obtaining the over phase noise value at an offset frequency is to add the different phase noise contributions together, as explained in section 2.7.2 [5]. By adding the two-phase noise results together, a total phase noise profile is obtained and compared with the simulated phase noise result shown in Figure 5.8.

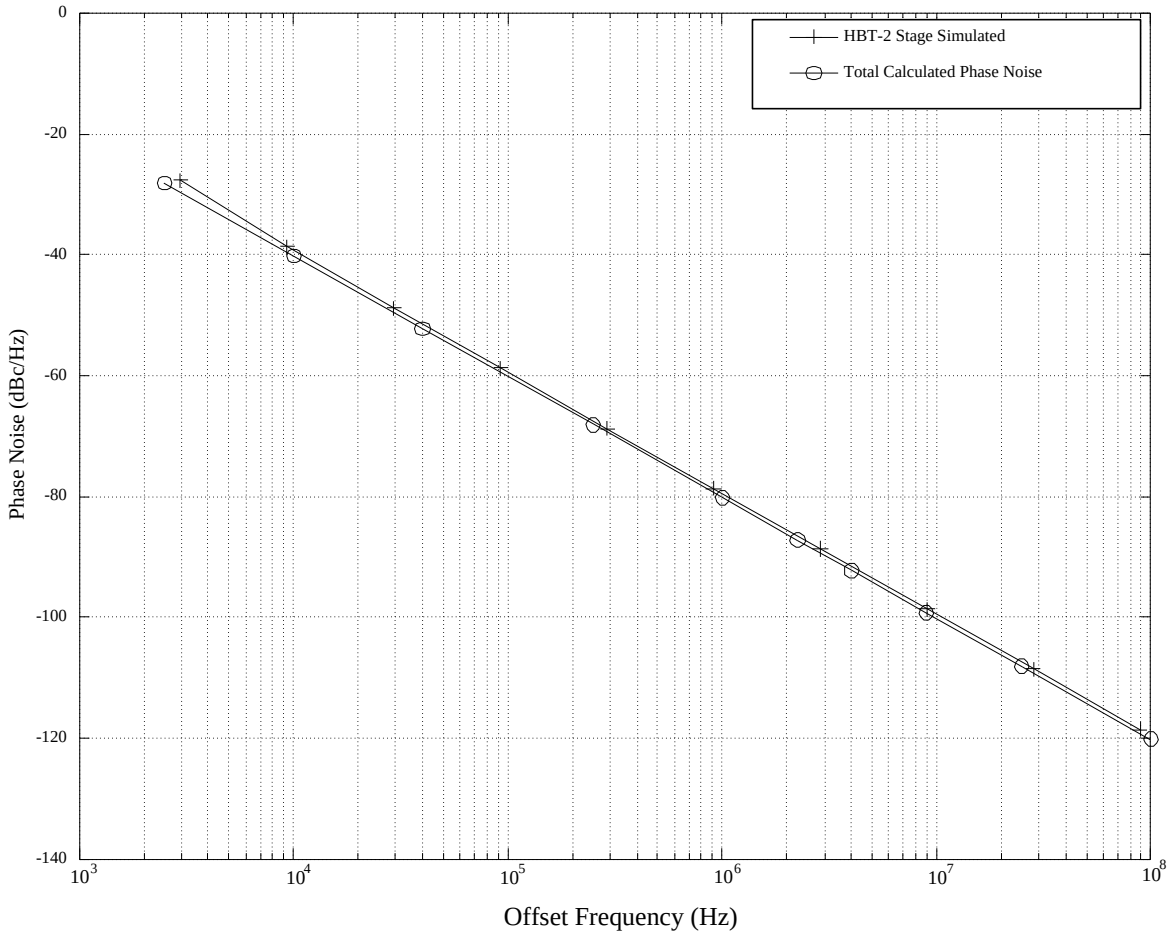

Figure 5.8. Total calculated phase noise vs simulated phase noise.

It should be noted from Figure 5.8 that the mathematical model, which included only the major noise sources, produces a phase noise result that is within 1 dB of the simulated phase noise of the circuit. This indicates any assumptions made concerning disregarding other noise sources are thus validated. These noise sources include the base-current shot noise and the bias resistor's thermal noise shown in Figure 4.1.

5.3.4. Phase noise comparison with other references

Since most oscillators are constructed differently and oscillate at different frequencies, a direct comparison between oscillator parameters was done [20]. A widely used method for testing the quality of an oscillator is the FOM [13], [20], [45]. The FOMs for both HBT and CMOS ring oscillators were calculated with (5.1). The results are shown in Table 5.1 and compared with the results obtained by other oscillators.

$$\text{FOM} = \mathcal{L}(f_{off}) - 20\log\frac{f_{osc}}{f_{off}} + 10\log\frac{P_{DC}}{1\ mW} \tag{5.1}$$

Table 5.1 Oscillator comparison.

Ref.	Process	Freq. (GHz)	Tuning range	Topology	Output power (dBm)	Power consumption (mW)	Phase noise (dBc/Hz)	Phase noise offset (MHz)	FOM (dBc/ Hz)
[5]	Not provided	10	Not provided	Perovskite differential CMOS ring	18.4	28.4	-106.41	1	-171.9
[7]	IBM BiCMOS SiGe 130 nm	52.8	13%	Colpitts oscillator	Not provided	140	-98.9	1	-171.9
[13]	AMS 350 nm	4.4 (simulated)	4.5%	Three-stage single-ended ring with RC differentia-tor	Not provided	12.5	-98	1	-158
[24]	UMC CMOS 130 nm	5.65	139.4	Two-stage differential CMOS ring	Not provided	5	-88.4	1	-156.5
[46]	CMOS 130 nm	2.2	16.8%	Cross-coupled LC VCO	-5.8 to -9.6	51.6	-104.7 to -108.83	1	-154.4 to -158.6
[45]	BiCMOS SiGe 130 nm	0.8–13.4 (simulated)	177%	Quadrature VCO+ one stage XOR	-45 to -30	13.98–15.52	-100 to -91.5	10	-127 to -142
[47]	TSMC CMOS 180 nm	10.875–11.1	2%	Cross-coupled differential CMOS LC VCO	-10.5	15	-120.42	1	-189
This work	BiCMOS SiGe 130 nm	2.5–3.8 (simulated)	43%	Three-stage CMOS ring	0	1.2–1.8	-76 to 0	0.01–1	-109 to -145
This work [40]	IBM BiCMOS SiGe 130 nm	1.8–3.5 (simulated)	72%	Two-stage HBT single-ended ring	-5	3.3–5.8	-80 to -14	0.01–1	-142 to -182

For the FOM the output power of the oscillator is calculated as the power equivalent for a 50 Ω load. The FOM is very good for the HBT based oscillator at low offset frequencies, while the FOMs of both oscillators at higher offset frequencies are more comparable. This can be attributed to the Q-factor of both oscillators. Since the CMOS ring oscillator is constructed from an additional inverter stage, it has a higher Q-factor, resulting in the steeper gradient observed in the phase noise slope, as shown in Figure 5.6. Consequently, the CMOS ring oscillator will operate in a narrower band than the HBT oscillator. When one analyses (5.1), it is observed that this FOM is biased towards narrowband oscillators with good phase noise figures at low offset frequencies to the carrier with low power requirements. Other parameters, such as linearity, bandwidth and real estate are not factored into this calculation. However, if only the phase noise performance is considered, the HBT ring oscillator proves to be a superior phase noise device, considering its lower flicker noise properties. The improvement in phase noise comes at the expense of higher power consumption, which in turn degrades the FOM of the oscillator.

5.4 OSCILLATOR MEASUREMENT RESULTS

Physical measurements were conducted on the prototyped circuit. The oscillator did not function as the simulated circuit. This can be attributed to two factors not considered during the circuit simulation. The ground nodes on the circuit were connected in a star pattern, rather than using a solid ground plane. This choice was mostly attributed to the MIM caps consuming most of the top layers usually considered for a ground plane. The star configuration consequently has an inductance effect on all the ground nodes. Secondly, the process variation was not correctly accounted for. The process run yielded a -17% deviation from the desired values this was not correctly accounted for when designing the circuit. Both these points contributed to the deviation between the simulated circuit's response and the physical measurement. By doing an analysis on the layout and considering the process, deviations could yield comparable result. A picture of the spectrum measuring the oscillator is shown in Figure 5.9.

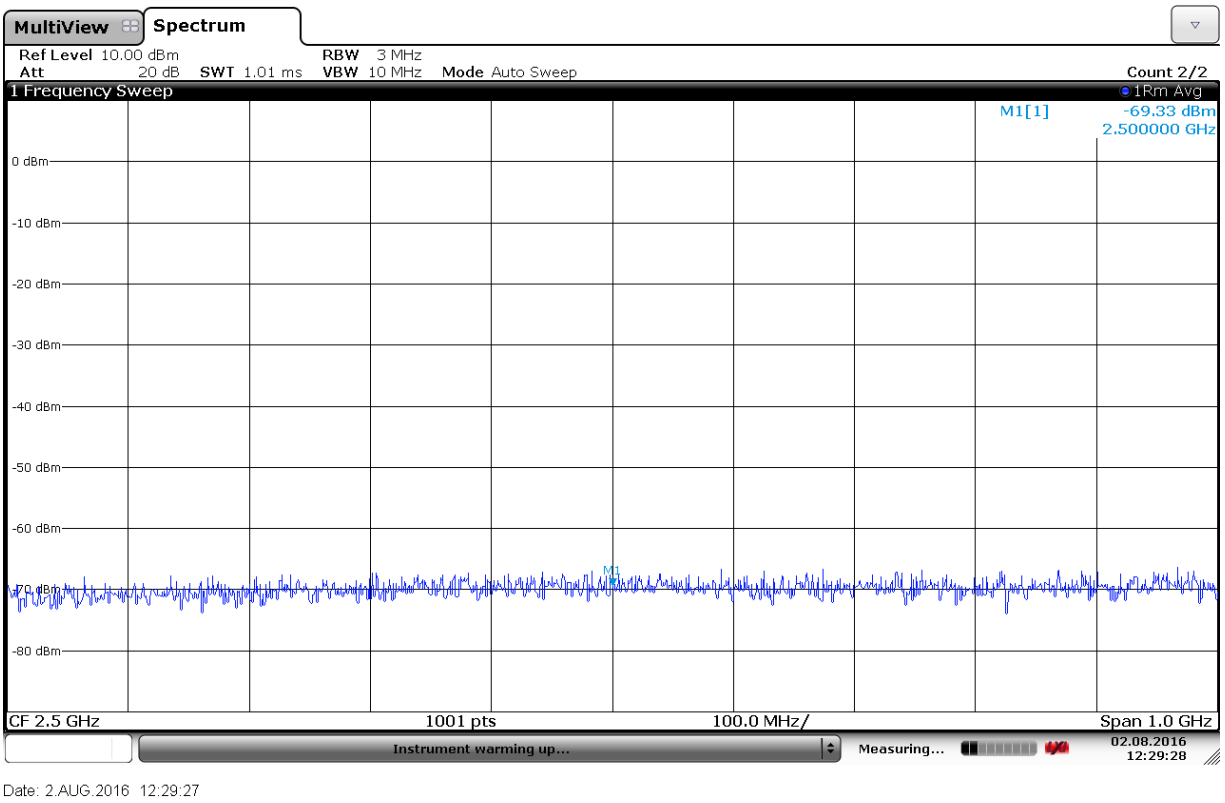

Figure 5.9. Spectrograph of oscillator output.

The spectrum analyser was set to a centre frequency of 2.5 GHz with a bandwidth of 1 GHz, the resolution bandwidth was set to 3 MHz and the video bandwidth to 10 MHz. The spectrograph shows no signal present in the oscillator's bandwidth of operation. A zerospan measurement was also taken and shown in Figure 5.10.

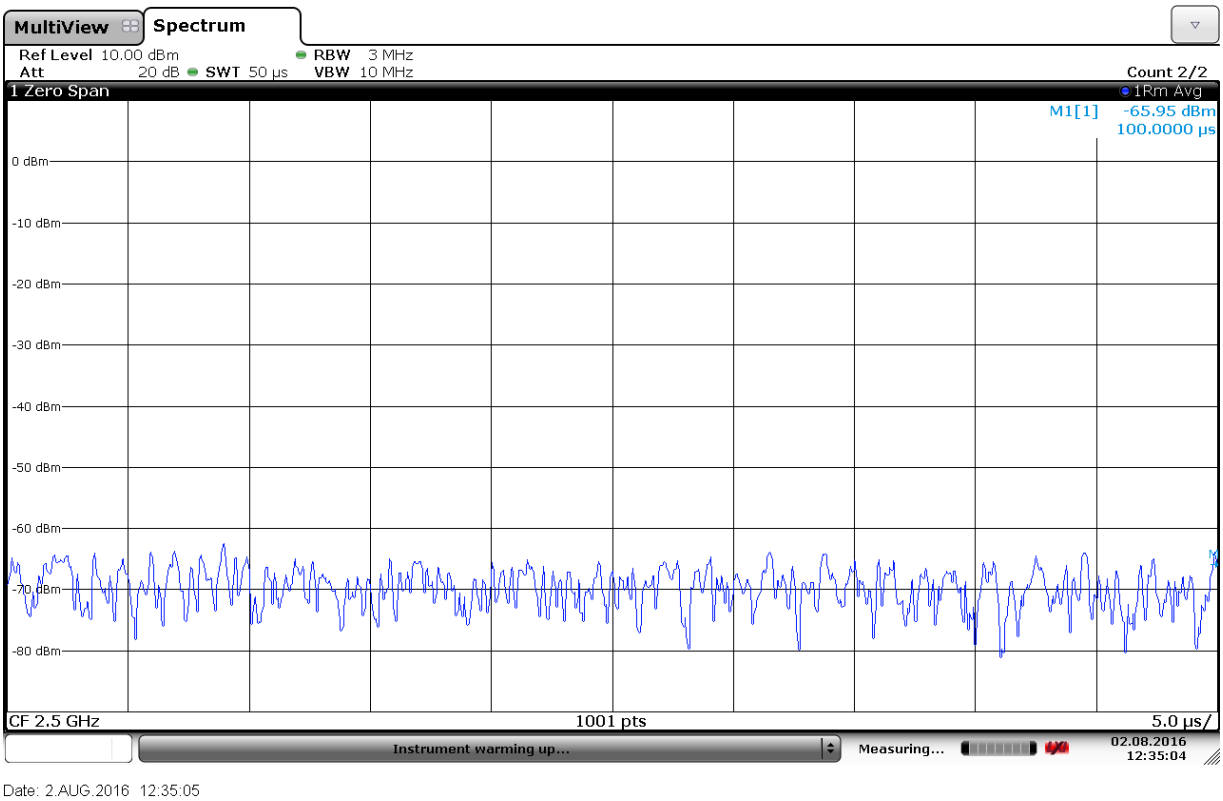

Figure 5.10. Zerospan measurement at 2.5 GHz of oscillator output.

The oscillator as tuned through the whole band of operation and a trigger is set up to show any pulses larger than -50 dBm. From both Figure 5.9 and Figure 5.10, it is noticeable that the oscillator is not working.

5.5 LNA SIMULATION RESULTS

This section presents the simulation results of the LNA used in conjunction with the oscillator. The AC voltage gain curve of the LNA is shown in Figure 5.11.

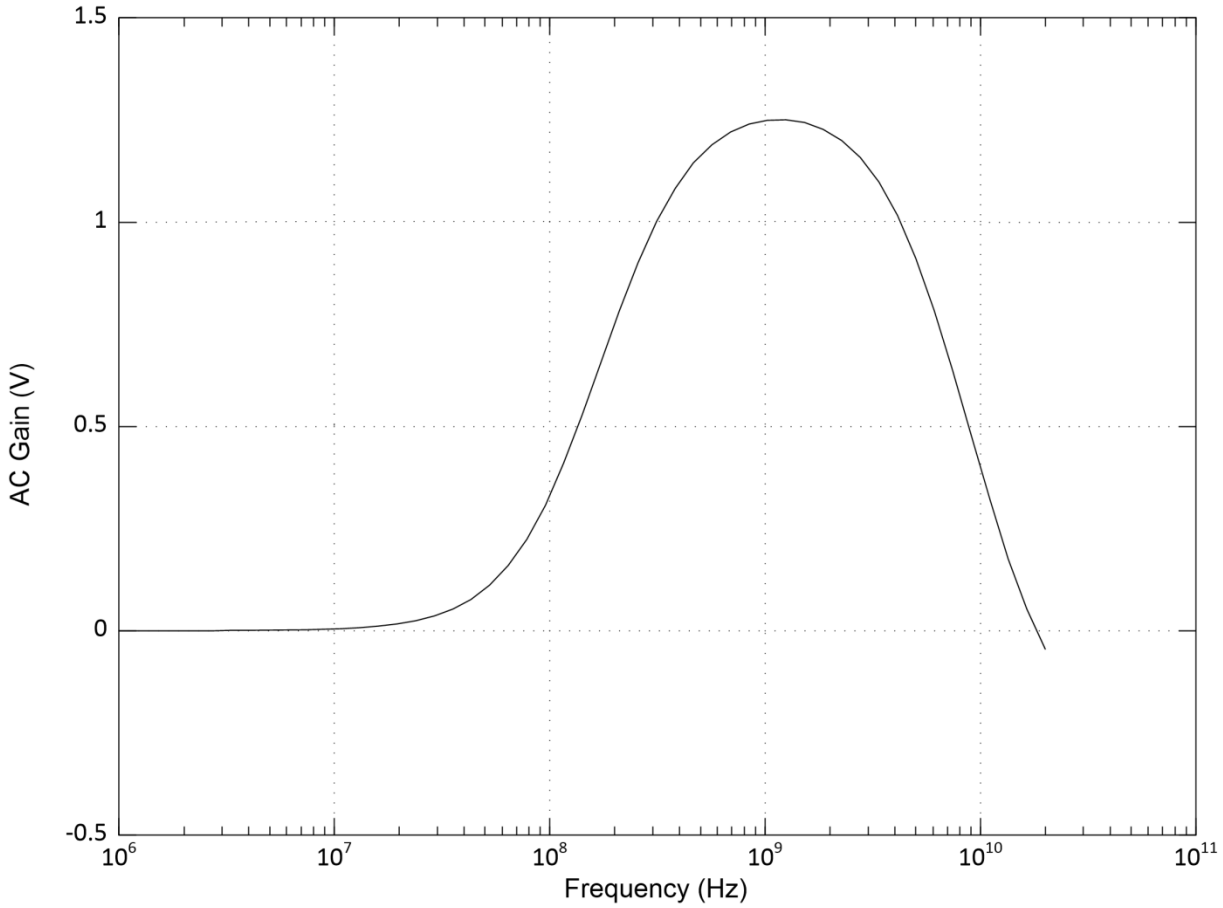

Figure 5.11. Amplifier AC voltage gain curve.

The AC voltage gain curve shown in Figure 5.11 is obtained when a 250 mV signal is introduced into the first stage of the amplifier. The maximum gain of the amplifier is obtained between 400 MHz and 3 GHz with a bandpass filter effect to suppress out-of-band harmonics. The upper cut-off frequency was chosen as 3 GHz since the second and third harmonic of the signal needed to be suppressed.

The AC power gain curve of the LNA is shown in Figure 5.12.

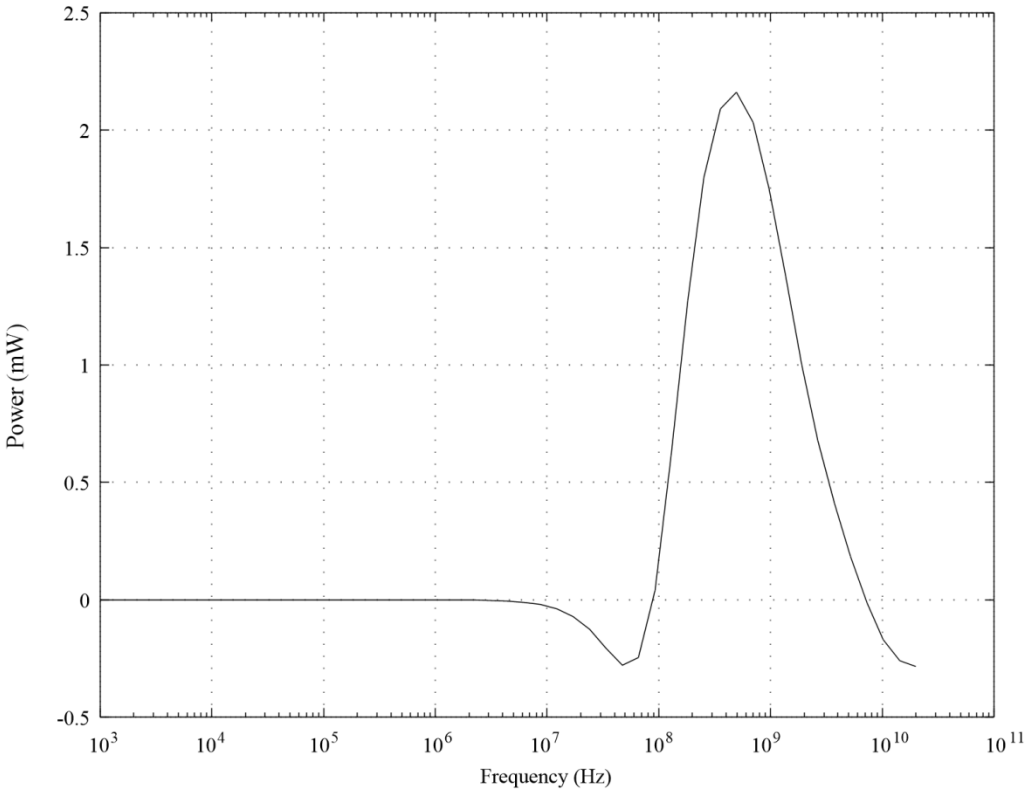

Figure 5.12. Amplifier AC power gain curve.

The power gain of the LNA shown in Figure 5.12 shows the maximum power gain of the LNA to be below 1 GHz. The power gain of the LNA in the region of interest is still positive. The reader should note the two different functions of the two different stages in the LNA, and why they were combined. The first stage of the LNA was used for amplifying the signal of the oscillator with a minimal NF. This allows for the oscillator output to be amplified with minimal degradation to the phase noise of the signal. The gain of the first stage also minimises the phase noise degradation imposed by following stages in the RF chain. The second stage of the amplifier acts as a current amplifier and impedance transformer. By transforming the impedance of the first amplifier stage from a high impedance to 50 Ω and amplifying the current, the second stage enables the output of the oscillator to be directly measured with a spectrum analyser, or to be used in conjunction with a PLL synthesiser with a 50 Ω characteristic impedance. The optimal power gain of both stages is lower than 1 GHz. This was not the optimal design choice, but to enable sufficient current supply from the power transistors, a frequency limit was imposed by the parasitic capacitances on the device.

CHAPTER 6 CONCLUSION

6.1 CHAPTER OBJECTIVES

The conclusion to the research conducted in this dissertation is summarised in this chapter and a critical analysis of the research hypothesis is presented, including scope delimitations and assumptions and proposals for future work.

6.2 INTRODUCTION

In Chapter 1, the research problem was introduced, as well as background given to the problem, explaining how improving the phase noise of a single-ended ring oscillator would be beneficial. Current findings and knowledge found in published literature were discussed in Chapter 2. The solution to the research problem was developed from this platform. In Chapter 3, the methodology followed in this research was discussed, which included a discussion of the IBM8HP PDK used for this research, as well as the guidelines used for realising a mathematical model for this work and the final verification method. In Chapter 4, a mathematical model was derived for the phase noise of the two-stage ring oscillator using a derivative of the closed-form ISF method. An expansion on the Barkhausen criteria was also given in Chapter 4 to include oscillation criteria of general odd-numbered CMOS inverter stages. The simulation and mathematical results are provided in Chapter 5 and compared with other recently published results.

6.3 CRITICAL EVALUATION OF HYPOTHESIS

For this research, it was hypothesised that using a SiGe HBT device in a single-ended ring oscillator structure will improve the phase noise of the ring oscillator. It was also hypothesised that the ISF method could be adapted for the oscillator structure in question, and a mathematical model was formulated to represent the oscillator's phase noise. This helped in optimising the phase noise of the oscillator. The resultant mathematical model was used, with parameters supplied by [8], and plotted in Octave. This result was then compared with a numerical simulation result, obtained in SpectreRF, and shown to be quite comparable. The results obtained by these authors also showed the base resistance thermal noise to be the major phase noise contributing to the noise source. The optimum value for the base resistance was

used to obtain maximum phase noise performance. Essentially, this was found to be the minimum base resistance value.

In addition, the FOM of this oscillator was calculated and compared with other measured and simulated oscillators. The FOM showed that the oscillator has very good overall performance when attributes such as phase noise, bandwidth and power consumption are factored in. It was also mentioned that the FOM does not factor in any of the oscillator's attributes, such as the chip area requirement, the number of required pins and the tuning linearity over the band.

A 2.5 GHz two-stage low phase noise ring oscillator was fabricated using the IBM8HP 130 nm SiGe BiCMOS process. The fabricated VCO was biased and measured. The device was found to deviate -17% from the optimal bias value, which resulted in the circuit not oscillating. It was hypothesised that the phase noise of a single-ended ring oscillator was dependent on the NF of the active device used in the loop. Equation (4.34) shows that the total phase noise of the oscillator is highly dependent on both the SiGe HBT device's base resistance thermal noise and the collector current shot noise, thus showing that the hypothesis still holds.

6.4 SUGGESTIONS FOR FUTURE WORK

Suggestions for future work derived from this research are offered below. By using a newer technology node, the researcher will obtain even better results with improved process parameters. By reducing the feature size of the active device, the parasitic resistance will be reduced and channel lengths will be shortened, allowing for lower noise active devices. The expansion of the Barkhausen oscillator stability criteria can be tested and investigated on a wider range of oscillators. Since it was found that the base resistance thermal noise is the major contributor to phase noise, a low impedance oscillator is also suggested for future research.

For closer operational performance between the simulation results and the physical operation of the oscillator, additional steps in the modelling process need to be taken. Firstly, the layout needs to be extracted and imported back into the schematic simulator. In this way the parasitic added by the interconnection traces can be accurately modelled and compensated for. Only

once this circuit layout has been simulated can a prototyped be made and expected to follow the simulation results closely.

Additional focus can also be placed on the phase noise performance between the centre and edge of the tuning bandwidth, and how the Q-factor of the oscillator affects the phase noise performance.

Focus in this study was also placed on the phase noise of a single-ended HBT based ring oscillator compared to a classic CMOS ring oscillator. It is suggested that the $1/f$ noise profiles of these two active devices be considered and compared in depth in future, in addition to taking a closer look at the $1/f$ upconversion from both devices to the $1/f^3$ phase noise.

REFERENCES

[1] A. Hajimiri and T.H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, February 1998.

[2] D.M. Pozar, *Microwave engineering*, 3rd ed., B. Zobrist, Ed. New York, United States of America: Wiley, 2005.

[3] J.G. Proakis and M. Salehi, *Communication systems engineering*, 2nd ed., M.J. Horton, Ed. New Jersey, United States of America: Prentice Hall, 2002.

[4] J.G. Proakis, *Digital communication*, 4th ed., W. Sephen, Ed. New Jursey, United States of America: McGrawHill, 2001.

[5] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[6] A. Fard and P. Andreani, "An analysis of $1/f^2$ phase noise in bipolar Colpitts oscillators (with a digression on bipolar differential-pair LC oscillators)," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 374–384, February 2007.

[7] G. Deepa, "SiGe based multiple-phase VCO operating for mm-wave," University of Pretoria, Pretoria, PhD Thesis 2013.

[8] MOSIS Department CL4V, *BiCMOS-8HP model reference guide*.: MOSIS, 2010, vol. 1.1.2.0.

[9] G. Niu, "Noise in SiGe HBT RF technology: physics, modeling, and circuit implications," *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1583–1597, September 2005.

[10] W. Loh, S. Yegnanarayanan, R.J. Ram, and P.W. Juodawlkis, "Unified theory of oscillator phase noise I:," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 6, pp. 2371–2381, June 2013.

[11] L. Dai and R. Harjani, "Design of low-phase-noise CMOS ring oscillators," *IEEE Transactions on Circuits and Systems*, vol. 49, no. 5, pp. 328–338, May 2002.

[12] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, March 1996.

[13] A.E. Mourabit, G-N. Lu, P. Pittet, Y. Birjali, F. Lahjomri, and M. Zhang, "A new method to enhance frequency operation of CMOS ring oscillators," *International Journal of*

Electronics, vol. 99, no. 3, pp. 351–360, November 2011.

[14] Y.A. Eken and J.P. Uyemura, "A 5.9-GHz voltage-controlled ring oscillator in 0.18-um CMOS," *IEEE Journal of Solid State Circuits*, vol. 39, no. 1, pp. 230–233, January 2004.

[15] T. Miyazaki, M. Hashimoto, and H. Onodera, "A performance comparison of PLLs for clock generation using ring oscillator VCO and LC oscillator in a digital CMOS process," in *Design Automation Conference*, Yohohama, 2004, pp. 545–546.

[16] F. Brandonisio and M.P. Kennedy, "Comparison of ring and LC oscillator-based ILFDs in terms of phase noise, locking range, power consumption and quality factor," in *Research in Microelectronics and Electronics*, Cork, 2009, pp. 292–295.

[17] B. Razavi, *RF microelectronics*, 1st ed.,T.S. Rappaport, Ed. New Jursey, United States of America: Prentice Hall, 1998.

[18] B. Mesgarzadeh and A. Alvandpour, "A wide-tuning range 1.8 GHz quadrature VCO utilizing coupled ring oscillators," in *IEEE Proceedings on Circuits and Systems*, Island of Kos, 2006, pp. 5143–5146.

[19] C-H. Park and B. Kim, "A low-noise, 900-MHz VCO in 0.6-um CMOS," *IEEE Journal of Solid State Circuits*, vol. 34, no. 5, pp. 586–591, June 1999.

[20] C. Zhang and J. Zhou, "A 2.4GHz low power low phase noise ring VCO," in *Anti-Counterfeiting, Security and Identification (ASID)*, Taipei, 2012, pp. 1–4.

[21] S-J. Lee, B. Kim, and K. Lee, "A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 2, pp. 289–291, February 1997.

[22] C. Sánchez-Azqueta, F. Aznar, and S. Celma, "A 0.18 um CMOS ring VCO for clock and data recovery applications," *Microelectronics Reliability*, vol. 51, no. 12, pp. 2351–2356, June 2011.

[23] M. Alioto and G. Palumbo, "Highly accurate and simple models for CML and ECL gates," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 18, no. 9, pp. 1369–1375, September 1999.

[24] B. Fahs, W.Y. Ali-Ahmad, and P. Gamand, "A two-stage ring oscillator in 0.13-um CMOS for UWB impulse radio," *IEEE Transactions of Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1074–1082, May 2009.

[25] S-L. Jang, Y-C. Lin, W-C. Lai, and C-W. Hsue and M-H. Juang, "A class-C quadrature VCO using the varactor coupling technique," *Microwave and Optical Technololgy Letters*, vol. 58, no. 8, pp. 1961-1965, August 2016.

[26] B. Jagannathan, M. Meghelli, A.V. Rylyakov, R.A. Groves, A.K. Chinthakindi, C.M. Schanbel, D.A. Ahlgren, G.G. Freeman, K.J. Stein, and S. Subbanna, "A 4.2-ps ECL ring-oscillator in a 285-GHz f_{max} SiGe technology," *IEEE Electron Device Letters*, vol. 23, no. 9, pp. 541–543, September 2002.

[27] D.L. Harame, D.C. Ahlgren, D.D. Coolbaugh, and J.S. Dunn, "Current status and future trends of SiGe BiCMOS technology," *IEEE Transactions on Electron Devices*, vol. 48, no. 11, pp. 2575–2594, November 2001.

[28] A. Fox, B. Heinemann, H. Rucker, R. Barth, G.G. Fischer, C. Wipf, S. Marschmeyer, K. Aufinger, J. Bock, S. Boguth, H. Knapp, R. Lachner, W. Liebl, D. Manger, T.F. Meister, A. Pribil and J. Wursthorn, "Advanced hetrojunction bipolar transistor for half-THz SiGe BiCMOS technology," *IEEE Electron Device Letters*, vol. 36, no. 7, pp. 642-644, July 2015.

[29] J. Yuan, K.A. Moen, J.D. Cressler, H. Rücker, B. Heinemann and W. Winkler, "SiGe HBT CML ring oscillator with 2.3-ps gate delay at cryogenic temperatures," *IEEE Transactions on Electron Devices*, vol. 57, no. 5, pp. 1183–1187, May 2010.

[30] E.G. Ioannidis, S. Haendler, C.A. Dimitriadis, and G. Ghibaudo, "Characterization and modeling of low frequency noise in CMOS inverters," *Solid-State Electronics*, vol. 81, pp. 151–156, March 2013.

[31] M. Antonelli, L.D. Micco, and H.A. Larrondo, "Measuring the jitter of ring oscillators by means of information theory quantifiers," *Commun Nonlinear Sci Numer Simulat*, vol. 43, pp. 139-150, February 2017.

[32] D.B. Leeson, "A simple model of feedback oscillator noise spectrum," *IEEE Proceedings*, vol. 54, no. 2, pp. 329–330, February 1966.

[33] T.H. Lee, "Oscillator phase noise: a tutorial," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 326–336, March 2000.

[34] H.T. Friis, "Noise figures of radio receivers," *Proceedings of the IRE*, vol. 32, no. 7, pp. 419–422, July 1944.

[35] B.H. Calhoun, *Design Principles for Digital CMOS Integrated Circuits*, 1st ed., R.T.

Howe, Ed. Viginia, United States of America: NTS Press, 2012.

[36] L. Dickstein, “Introduction to phase noise in signal generators,” Giga-tronics, San-Ramos, White paper 2012.

[37] IBM Microelectronics, *BiCMOS8HP design manual*, July 2007.

[38] IBM Microelectronics, *BiCMOS8HP model reference guide*, July 2007.

[39] Cadence, *SpectreRF user guide*, Cadence design systems, 2003.

[40] S.J.L. van Niekerk and S. Sinha, "A 2.5 GHz low phase noise silicon germanium heterojunction bipolar transistor ring oscillator," *Proceedings: IEEE international semiconductor conference*, 10-12 Oct. 2016, Sinaia, Romania.

[41] J. Steward, *Calculus early transcendentals*, 5th ed., B. Pirtle, Ed. Belmont, United States of America: Thomson, 2003.

[42] C.K. Alexander and M.N.O. Sadiku, *Fundamentals of electric circuits*, 2nd ed., C. Paulson, Ed. Cleveland, United States of America: McGraw-Hill, 2004.

[43] A.A. Ahmad, M. Pichan, and A. Abrishamifar, "A new simple structure PLL for both single and three phase appiclations," *Electrical Power and Energy Systems*, vol. 74, no. 1, pp. 118-125, January 2016.

[44] G. Deepa and S. Sinha, “Phase noise analysis for a mm-wave VCO configuration,” *Microwave and Optical Technology Letters*, vol. 55, no. 2, pp. 290–295, May 2012.

[45] Y. Lin and D.E. Kotecki, “A 0.8-13.4GHz combined voltage-controlled oscillator with and exclusive-OR in 130nm SiGe BiCMOS,” in *Electronics, Circuits, and Systems (ICECS)*, Athens, 2010, pp. 426–429.

[46] S.M.M. Hassan, M.A. Ismail, N.E. Farid, N.F.I. Muhammad, and A.I.A. Rahim, “A dual-band voltage-controlled oscillator in 0.13 μm CMOS technology”, *Microelectronics International*, vol. 29 no. 3 pp. 153-162, March 2012.

[47] M-L. Yeh, Y-C. Lin, and W-H. Chang, “An 11 GHz low-phase-noise voltage-controller oscillator”, *Microelectronics International*, vol. 29 no. 2, pp. 90-95, February 2012.

ADDENDUM A OCTAVE CODE FOR ISF MODELLING

The following script was used in Octave 4.0.0 to calculate the phase noise of the suggested ring oscillator. The script plots three figures. The first plots the simulated phase noise of the two-stage HBT ring oscillator and compares it to the simulated phase noise of the three-stage CMOS ring oscillator. The second figure plots the two individual phase noise results of the base resistance thermal noise and the collector current shot noise separately, as well as the total simulated phase noise for comparison. Lastly, the total phase noise of the oscillator produced by the mathematical model is then plotted and compared with the simulated phase noise profile for easy comparison.

```
clear;

kb  = 1.38068*10^-23;          % Boltzmann constant
T = 300;                       % This is at room temperature (300 K)
Rb = 860;                      % Base resistance, calculated on page
N = 1;                         % 1 = single-ended oscillator (4.13)
Rl = 860;                      % Load resistance seen by one inverter stage
Ib = 1e-6;                     % Base Current in amps
q = 1.60217657e-19;            % Electron charge constant
Vbe = 0.5;                     % Base emitter voltage
Ae = 0.3;                      % Amplitude of oscillator signal
Is = 1e-20;
Ctot = 100*10^-15;             % Total capacitance at base
Vswing = 0.6;                  % voltage swing of oscillator

%-------------------------------------------------------------%
%   Base resistance thermal noise phase noise component      %
%-------------------------------------------------------------%

qmax = Ctot*Vswing;
ac = qmax/(kb*T);

Vt = (kb*T)/q;
ae = Ae/Vt;
Ib = Is*(10^(Vbe/Vt))*besselj(0,ae);
```

```
Gamma_rms_sqr_rb=((Rb^2*Ib)/(4*N^2*Vt*Rl))*((besselj(1,2*ae))/(besselj(0,ae
)* besselj(1,ae)));


i_c2_DelF = (4*kb*T)/Rb;

Constant = (Gamma_rms_sqr_rb*i_c2_DelF)/(qmax*qmax);

for count = 1:1000
     F(count) = 100*count^2;
     Calc_PN_temp(count)= 10*log10(Constant/(2*(2*pi*F(count))^2));
endfor


F_rb(1) = F(5);
Calc_PN_rb(1) = Calc_PN_temp(5);
F_rb(2) = F(10);
Calc_PN_rb(2) = Calc_PN_temp(10);
F_rb(3) = F(20);
Calc_PN_rb(3) = Calc_PN_temp(20);
F_rb(4) = F(50);
Calc_PN_rb(4) = Calc_PN_temp(50);
F_rb(5) = F(100);
Calc_PN_rb(5) = Calc_PN_temp(100);
F_rb(6) = F(150);
Calc_PN_rb(6) = Calc_PN_temp(150);
F_rb(7) = F(200);
Calc_PN_rb(7) = Calc_PN_temp(200);
F_rb(8) = F(300);
Calc_PN_rb(8) = Calc_PN_temp(300);
F_rb(9) = F(500);
Calc_PN_rb(9) = Calc_PN_temp(500);
F_rb(10) = F(1000);
Calc_PN_rb(10) = Calc_PN_temp(1000);

%-----------------------------------------------------------------%
%      Collector current shot noise phase noise component       %
%-----------------------------------------------------------------%

i_c2_DelF = (2*kb*T*Ib)/(Vt*besselj(0,ae));
```

```
Gamma_rms_sqr_ic =  (1/((N^2)*ae))*besselj(1,ae);
Constant = i_c2_DelF*Gamma_rms_sqr_ic/(qmax*qmax);

for count = 1:1000
     F(count) = 100*count^2;
     Calc_PN_temp(count)= 10*log10(Constant/(2*(2*pi*F(count))^2));
endfor

F_ic(1) = F(5);
Calc_PN_ic(1) = Calc_PN_temp(5);
F_ic(2) = F(10);
Calc_PN_ic(2) = Calc_PN_temp(10);
F_ic(3) = F(20);
Calc_PN_ic(3) = Calc_PN_temp(20);
F_ic(4) = F(50);
Calc_PN_ic(4) = Calc_PN_temp(50);
F_ic(5) = F(100);
Calc_PN_ic(5) = Calc_PN_temp(100);
F_ic(6) = F(150);
Calc_PN_ic(6) = Calc_PN_temp(150);
F_ic(7) = F(200);
Calc_PN_ic(7) = Calc_PN_temp(200);
F_ic(8) = F(300);
Calc_PN_ic(8) = Calc_PN_temp(300);
F_ic(9) = F(500);
Calc_PN_ic(9) = Calc_PN_temp(500);
F_ic(10) = F(1000);
Calc_PN_ic(10) = Calc_PN_temp(1000);

Calc_PN_ic = -1.*abs(Calc_PN_ic);

%-------------------------------------------------------------------%
%                 Total calculated phase noise                      %
%-------------------------------------------------------------------%

F_tot(1) = F(5);
Calc_PN_tot(1) = log10(10^(Calc_PN_rb(1))+10^(Calc_PN_ic(1)));
F_tot(2) = F(10);
Calc_PN_tot(2) = log10(10^(Calc_PN_rb(2))+10^(Calc_PN_ic(2)));
F_tot(3) = F(20);
```

```
Calc_PN_tot(3) = log10(10^(Calc_PN_rb(3))+10^(Calc_PN_ic(3)));
F_tot(4) = F(50);
Calc_PN_tot(4) = log10(10^(Calc_PN_rb(4))+10^(Calc_PN_ic(4)));
F_tot(5) = F(100);
Calc_PN_tot(5) = log10(10^(Calc_PN_rb(5))+10^(Calc_PN_ic(5)));
F_tot(6) = F(150);
Calc_PN_tot(6) = log10(10^(Calc_PN_rb(6))+10^(Calc_PN_ic(6)));
F_tot(7) = F(200);
Calc_PN_tot(7) = log10(10^(Calc_PN_rb(7))+10^(Calc_PN_ic(7)));
F_tot(8) = F(300);
Calc_PN_tot(8) = log10(10^(Calc_PN_rb(8))+10^(Calc_PN_ic(8)));
F_tot(9) = F(500);
Calc_PN_tot(9) = log10(10^(Calc_PN_rb(9))+10^(Calc_PN_ic(9)));
F_tot(10) = F(1000);
Calc_PN_tot(10) = log10(10^(Calc_PN_rb(10))+10^(Calc_PN_ic(10)));


%-----------------------------------------------------------------%
%                       Plotting figures                          %
%-----------------------------------------------------------------%

PNSim = dlmread("PNSim.csv",",");
CMOSPNSim = dlmread("CMOSPNSim.csv",",");
CMOS5SPNSim = dlmread("CMOS5SPNSim.csv",",");

size(PNSim);
size(CMOSPNSim);
size(CMOS5SPNSim);

t = PNSim(:,1);

yHBT = PNSim(:,2);
yCMOS = CMOSPNSim(:,2);
yCMOS5S = CMOS5SPNSim(:,2);

figure(1)
clf
grid on;
semilogx(t(1:20:end),yHBT(1:20:end),'-+110;HBT-2 Stage Simulated;');
hold on;
```

```
semilogx(t(1:20:end),yCMOS(1:20:end),"-*110;CMOS-3 Stage Simulated;" );

axis([1E3,1E8,-140,5]);
grid on;

saveas(gcf, "PN_Sim_Comparison.svg","svg")

figure(2)
clf
grid on;
semilogx(t(1:20:end),yHBT(1:20:end),'-+110;HBT-2 Stage Simulated;');
hold on;
semilogx(F_rb(1:end),Calc_PN_rb(1:end),"-o110;Calculated     Rb     Thermal
Noise;");
hold on;
semilogx(F_ic(1:end),Calc_PN_ic(1:end),"-*110;Calculated  Ic  Shot  Noise;");

%axis([1000,100000000,-150,10]);
grid on;

saveas(gcf, "Calculated_vs_Simulated_PN.svg","svg")

figure(3)
clf
grid on;
semilogx(t(1:20:end),yHBT(1:20:end),'-+110;HBT-2 Stage Simulated;');
hold on;
semilogx(F_tot(1:end),Calc_PN_tot(1:end),"-o110;Total    Calculated    Phase
Noise;");
%axis([1000,100000000,-150,10]);
grid on;

saveas(gcf, "PN_Total.svg","svg")
```

ADDENDUM B CIRCUIT LAYOUTS

The layout schematics used for the fabricated devices are presented in this Addendum. The two-stage single-ended ring oscillator and the high impedance LNA were integrated as both single and separate circuits, allowing measurements of both systems separately was well as conjoined.

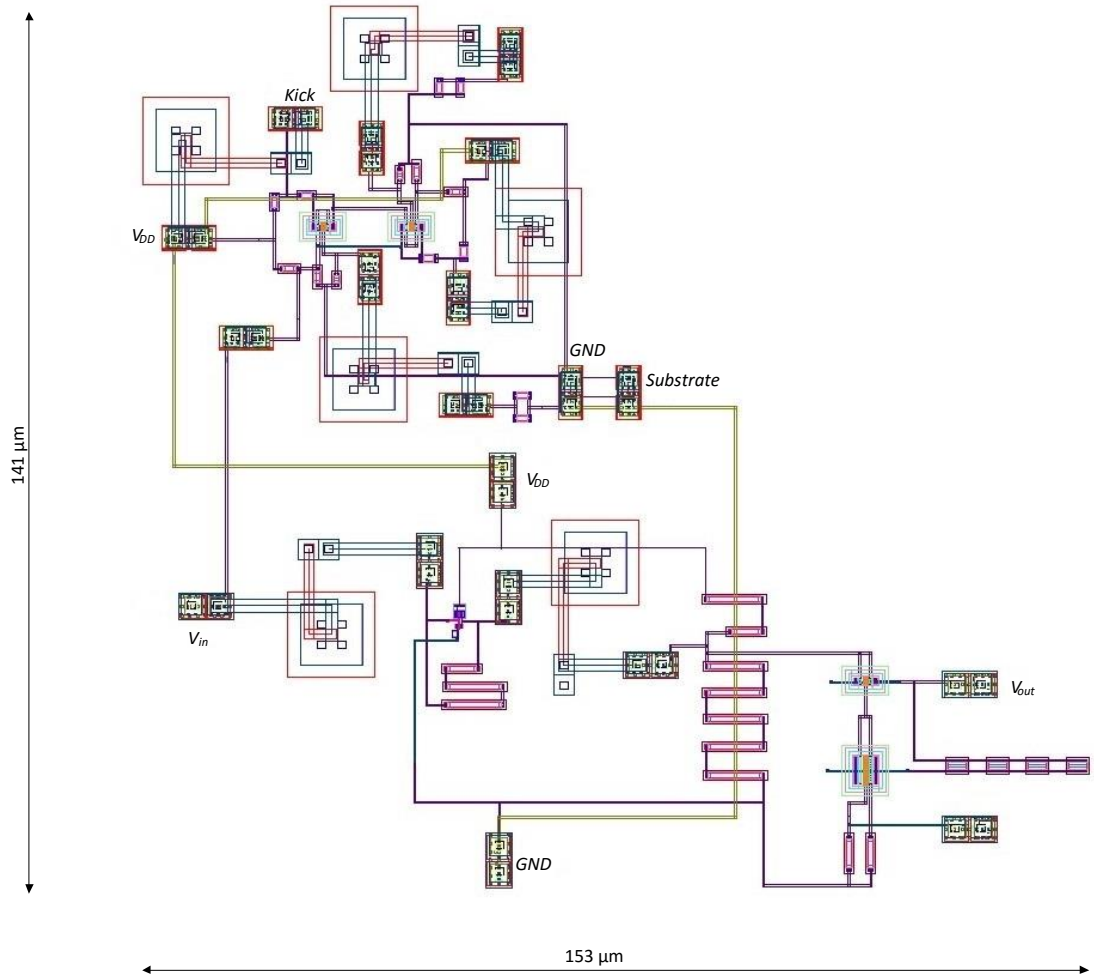

Figure B1. Single-ended ring oscillator and high impedance amplifier.

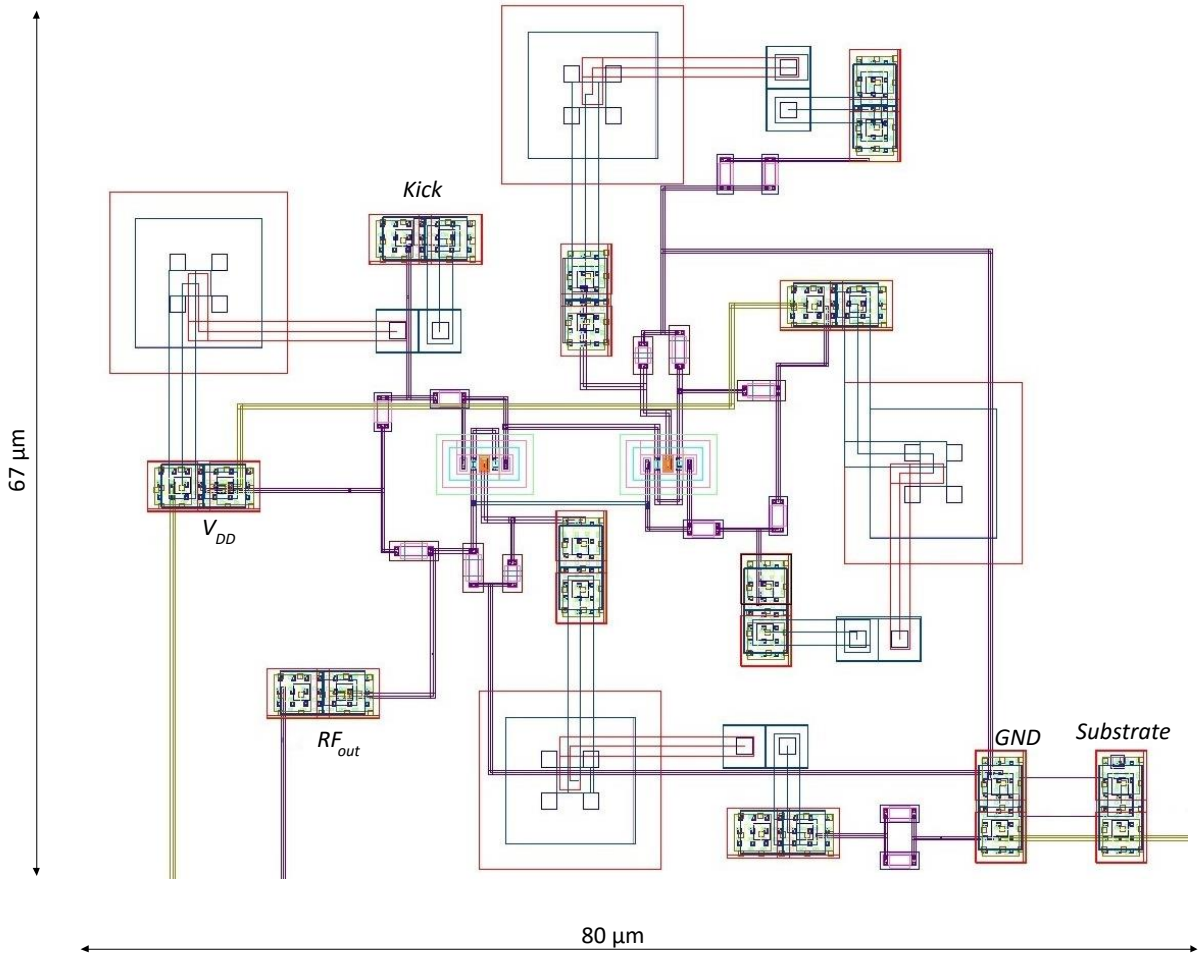

Figure B2. Two-stage SiGe HBT ring oscillator.

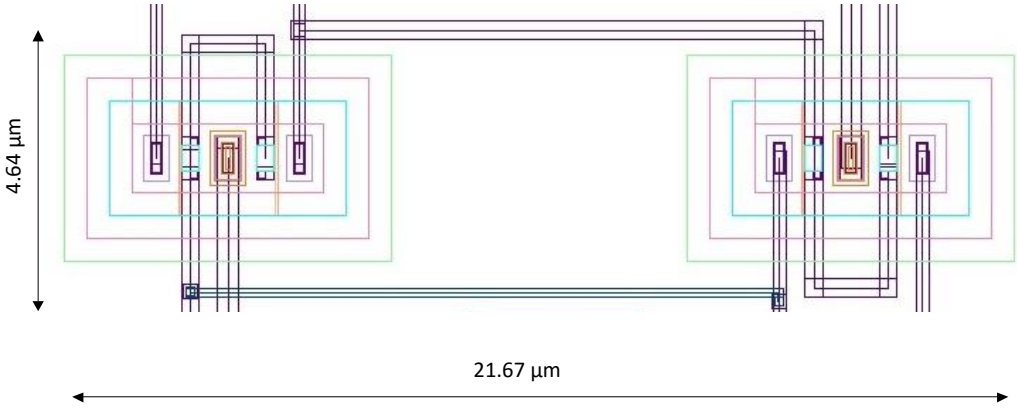

Figure B3. Two SiGe HBT in ring layout.

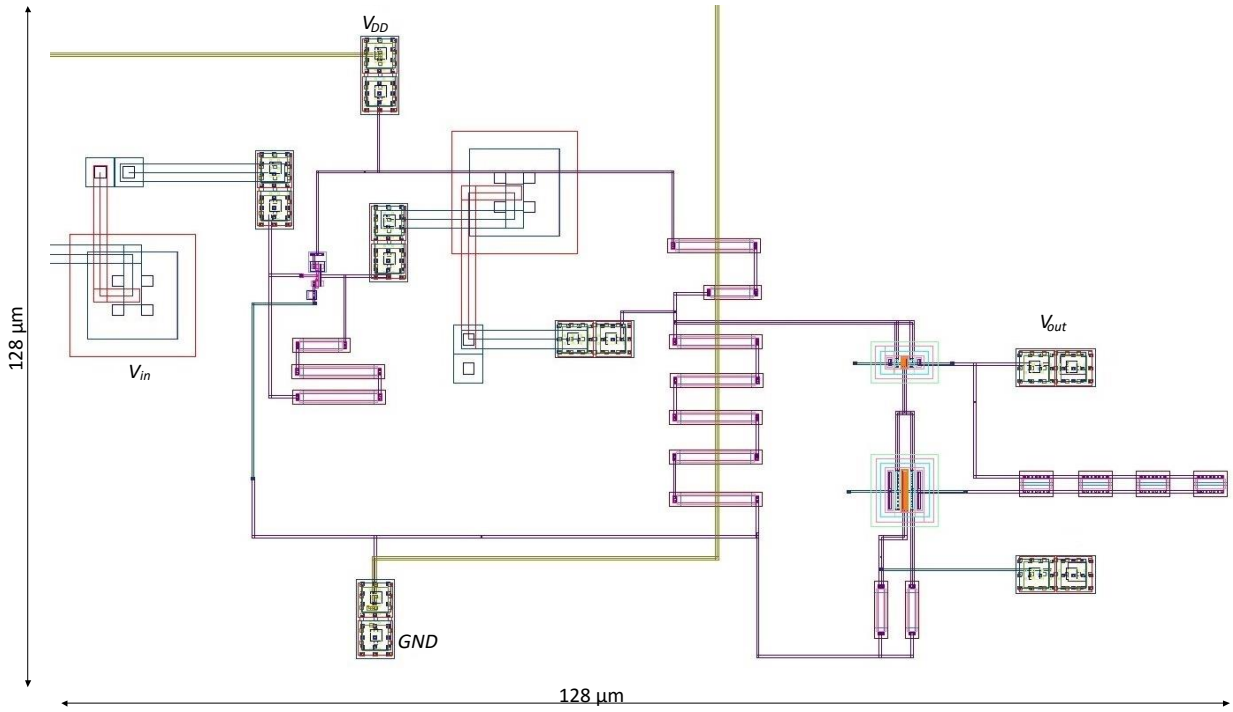

Figure B4. High impedance LNA layout.