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# HIGH BANDWIDTH CHERRY HOOPER FLASH ADC IN 0.13 µm SIGE BICMOS

by

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Submitted in partial fulfilment of the requirements for the degree

**Master of Engineering (Microelectronic Engineering)**

in the

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# SUMMARY

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Keywords: Analogue-digital conversion, effective number of bits (ENOB), differential amplifier, millimetre wave (mm-wave) integrated circuits, heterojunction bipolar transistor (HBT)

There exists a need to be able to acquire high data speed over a wide bandwidth. This requires the use of an analogue-to-digital converter (ADC) capable of achieving wide input bandwidth. With the 60 GHz unlicensed band, which has 7 GHz of usable bandwidth, the effective resolution bandwidth of an ADC must be at least 7 GHz. Parallel architectures, such as the flash ADC, are used to obtain fast sampling speeds and are suitable for systems where a wide bandwidth is required. The input bandwidth is reduced as the bit size is increased due to the large parasitic capacitance present at the input of the ADC. The 0.13 µm IBM 8HP SiGe BiCMOS process provides high speed heterojunction bipolar transistors (HBTs) with cut-off frequencies ($f_T$) up to 200 GHz providing possible operation in the mm-wave region. Amongst other advantages, HBTs have good noise performance characteristics and are discussed in the dissertation.

The focus of the research is to reduce the effect of the parasitic input capacitance of a flash ADC, whilst still maintaining ADC performance at low-GHz range frequencies. In order to improve the input bandwidth a common collector input tree is proposed. The Cherry Hooper differential amplifier is proposed to function as the ADC comparator. The input tree separates the parasitic input capacitances of each comparator thereby reducing the high parasitic input capacitance and improving the bandwidth of the ADC. The Cherry Hooper

amplifier can be used as a transimpedance amplifier for mm-wave signals. By connecting the Cherry Hopper amplifier in a differential pair configuration, a comparator can be realised for use in an ADC. The input tree in combination with the Cherry Hooper amplifier could provide high bandwidth and maintain ADC performance at low-GHz frequencies for use in the 60 GHz mm-wave bandwidth frequency. This led to the hypothesis of this research.

Cadence Virtuoso results are presented in this dissertation to support the derived hypothesis. AC simulation results show a gain of approximately 6 dB with a bandwidth up to 30 GHz for a two-bit ADC. Time domain simulation results show digital outputs within the 10/90% range of the 440 mV single ended output swing, up to 5 GHz. A two-bit ADC is also prototyped within the 0.13 μm 8HP IBM SiGe process in order to affirm the hypothesis. Measurement printed circuit boards (PCBs) were designed and developed to measure various characteristics of the ADC, such as the integral non-linearity (INL) and differential non-linearity (DNL), to determine the effective number of bits (ENOB) and hence the figure of merit (FOM). Measurement results showed INL and DNL results up to 0.33 least significant bits (LSBs), an effective resolution bandwidth (ERBW) up to 2 GHz and an ENOB up to 1.18. Reduction in bandwidth of the implemented system was due to high inductive test leads. The increase in inductance at the test leads lead to oscillations on the comparator outputs and reduced the voltage standing wave ratio. These measured results were confirmed in post layout simulations.

# OPSOMMING

## HOË BANDWYDTE CHERRY HOOPER BLITS ADO IN 0.13 µm SIGE BICMOS

deur

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Sleutelwoorde: Analoog-digitale omskakeling, effektiewe hoeveelheid bisse (ENOB), syfer van meriete (FOM), differensiaalversterker, millimeter golf (mm-golf), parallelle argitektuur, logiese stroombane, heterovoegvlak-bipolêre transistor (HBT), silikon germanium (SiGe), BiCMOS geïntegreerde stroombane

Daar bestaan ŉ behoefte om hoë spoed data oor ŉ hoë bandwydte te verkry en dus word ŉ analoog-na-digitale-omsetter (ADO) benodig wat hierdie bandwydte kan handhaaf. Die ongelisensieerde 60 GHz band, wat oor 7 GHz bruikbare bandwydte beskik, benodig dus ŉ ADO met ŉ effektiewe resolusie bandwydte van ten minste 7 GHz. ŉ Parallelle argitektuur, soos die blits ADO, word gebruik om vinnige monsterspoed te bereik en is gevolglik geskik vir stelsels waar wye bandwydte benodig word. Die insetbandwydte word verminder soos die biswydte verhoog word weens die teenwoordigheid van die groot parasitiese kapasitansie by die inset van die ADO. Die 0.13 µm IBM 8HP SiGe BiCMOS proses maak voorsiening vir hoëspoed heterovoegvlak-bipolêre transistors (HBTs) met afsnyfrekwensies ($f_T$) tot by 200 GHz, wat dit in staat stel om in die mm-golf gebied te funksioneer. ŉ Verdere voordeel is dat HBTs oor goeie ruis werkverrigtingseienskappe beskik, soos wat verder in hierdie verhandeling bespreek word.

Die fokus van die navorsing is om die effek van hoë inset parasitiese kapasitansie van ŉ blits ADO te verminder, terwyl ADO funksionaliteit by lae GHz bestek frekwensies gehandhaaf word. ŉ Gemene kollektor insetvertakking word voorgestel om die inset-bandwydte te verbeter. Verder word ŉ Cherry Hooper differensiële versterker voorgestel

om die ADO vergelyker se funksie te verrig. Die insetvertakking skei die inset parasitiese kapasitansie van elke vergelyker. Sodoende verminder dit die totale inset parasitiese kapasitansie van die ADO en verhoog terselfdertyd die ADO bandwydte. Die Cherry Hooper differensiële versterker kan as ŉ transimpedansie versterker gebruik word vir mm-golf seine en kan dus as ŉ geskikte vergelyker gebruik word in ŉ ADO. Die insetvertakking, in kombinasie met die Cherry Hooper versterker, kan moontlik ŉ hoë bandwydte voorsien en ADO werkverrigting by lae GHz frekwensies handhaaf vir gebruik in die 60 GHz mm-golf bandwydte. Dit het aanleiding gegee tot die navorsingshipotese.

Cadence Virtuoso resultate word in hierdie verhandeling aangebied om die afgeleide hipotese te versterk. Kleinsein simulasieresultate toon ŉ wins van 6 dB met ŉ bandwydte tot en met 30 GHz vir ŉ twee-bis ADO. Tydgebied simulasieresultate toon digitale uitsette binne die 10/90% bestek van die 440 mV enkeluitset tot en met 'n bandwydte van 5 GHz. ŉ Twee-bis ADO prototipe is met die 0.13 µm 8HP IBM SiGe proses ontwerp en vervaardig om die hipotese te bevestig. Toetsstroombaanborde is ontwerp en vervaardig om verskeie ADO eienskappe, soos bv. die integraal nielineariteit (INL) en die differensiële nielineariteit (DNL) te meet om die effektiewe aantal bisse (ENOB) en merietesyfer (FOM) te bepaal. Die gemete resultate toon INL en DNL syfers van 0.33 van die mins beduidende bis (LSB), ŉ effektiewe resolusie bandwydte (ERBW) van 2 GHz en ŉ ENOB van 1.18. Die vermindering in bandwydte was as gevolg van ŉ hoër induktansie op die toetspunte. Dit gee aanleiding tot dramatiese ossillasie van die vergelykeruitsette en ŉ verswakte staandegolf-verhouding. Na-uitleg simulasies is uitgevoer om die gemete resultate te bevestig.

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studentships towards young students who want to continue with their postgraduate studies.

## LIST OF ABBREVIATIONS

| | |
|---|---|
| **ADC** | Analogue-to-digital converter |
| **ADE** | Analog Design Environment |
| **BER** | Bit error rate |
| **BiCMOS** | Bipolar complementary metal-oxide-semiconductor |
| **BJT** | Bipolar junction transistor |
| **CAD** | Computer aided design |
| **CBEBC** | Collector-base-emitter-base-collector |
| **CC** | Common collector |
| **CE** | Common emitter |
| **C-H** | Cherry Hooper |
| **CMOS** | Complementary metal-oxide-semiconductor |
| **CSIR** | Council for Scientific and Industrial Research |
| **DAC** | Digital to analogue converter |
| **DNL** | Differential non-linearity |
| **DPSS** | Defence, peace, safety and security |
| **DRC** | Design rule checks |
| **DSP** | Digital signal processor |
| **DUT** | Device under test |
| **ECL** | Emitter coupled logic |
| **ENOB** | Effective number of bits |
| **FFT** | Fast Fourier transform |
| **FOM** | Figure of merit |
| **HBT** | Heterojunction Bipolar Transistor |
| **HICUM** | High current model |
| **IC** | Integrated circuit |
| **INL** | Integral non-linearity |

| | |
|---|---|
| **InP** | Indium Phosphide |
| **KCL** | Kirchhoff's Current Law |
| **KVL** | Kirchhoff's Voltage Law |
| **LSB** | Least significant bit |
| **LVS** | Layout versus schematic |
| **MEP** | MOSIS Education Programme |
| **MOS** | Metal-oxide-semiconductor |
| **MOSFET** | MOS Field Effect Transistor |
| **MOSIS** | MOS implementation system |
| **MPW** | Multi-project wafer |
| **MSB** | Most significant bit |
| **NAD** | Noise and distortion ratio |
| **PCB** | Printed circuit board |
| **PDK** | Process design kit |
| **RF** | Radio Frequency |
| **SFDR** | Spurious free dynamic range |
| **SGP** | SPICE Gummel-Poon |
| **SINAD** | Signal to noise and distortion ratio |
| **SNR** | Signal to noise ratio |
| **SPICE** | Simulation Program with Integrated Circuit Emphasis |
| **S/H** | Sample and hold |
| **TDR** | Time Domain Reflectometry |
| **THA** | Track and hold amplifier |
| **THD** | Total harmonic distortion |
| **VBIC** | Vertical Bipolar Inter-company |
| **VSWR** | Voltage standing wave ratio |
| **XOR** | Exclusive-or |

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# CHAPTER 1 INTRODUCTION

## 1.1 BACKGROUND TO THE RESEARCH

The 60 GHz unlicensed band is being utilised for high speed wireless networks with data rates in the gigabit range. In order to successfully make use of these high speed signals in a digital system, a high speed analogue-to-digital converter (ADC) is required. A high speed ADC can further be of use in software defined radios, digital oscilloscopes, radar applications and satellite communication systems.

Various ADC architectures exist and the flash architecture obtains the highest sampling speeds. Unfortunately flash ADCs consume the most power due to the high comparator count needed. Flash ADCs thus tend to have lower resolution than other ADC architectures. Time interleaving has been used to improve ADC sampling speeds, but is more susceptible to clock jitter, phase skew and component mismatches. By using time interleaving, slower sampling ADCs can be employed to obtain high sampling speeds. This, however, involves increased power dissipation and increased complexity in order to obtain sampling speeds comparable with flash ADCs.

The ADC resolution, bandwidth and clock jitter all play a role in the effective number of bits (ENOB) the ADC can produce. Therefore, the performance of an ADC does not only rely on the architecture used to obtain a high sampling speed. Due to the skin effect, the design of high speed circuits becomes more complex as the current flows in the outer surface of the conductor increasing the resistance at high frequencies. The resulting deviations may, amongst others, cause an increase or decrease in comparator gain. This change in gain could reduce the slew rate of the comparator or cause the comparator to become unstable. Another important factor of high speed ADCs is the substrate type in the manufacturing process as well as the transition frequency ($f_T$) and maximum frequency ($f_{max}$) of the transistors used in the process. Higher $f_T$ and $f_{max}$ values increase transistor regeneration times, which increase achievable switching speeds. Modern SiGe processes have achieved high $f_T$ and $f_{max}$ values for their heterojunction bipolar transistors (HBTs). With further technology scaling in SiGe HBTs, higher $f_T$ and $f_{max}$ values can be expected and may result in higher bandwidth performance with the same power consumption as

previous technologies [1]. The bipolar complementary metal-oxide-semiconductor (BiCMOS) design provides the advantages of both bipolar and metal-oxide-semiconductor (MOS) transistors to achieve high $f_T$ and $f_{max}$ values and reduced power consumption. Additional benefits of SiGe HBTs over traditional Si bipolar junction transistors (BJTs) also include higher current densities improving the current gain ($\beta$) of the transistor, lower base resistance and favourable temperature effects allowing SiGe HBTs to be operable at cryogenic temperatures [2, 3]. With the high $f_T$ and $f_{max}$ values, high $\beta$ and low base resistance better noise performance can be expected from SiGe HBTs when compared to its Si BJT counterparts. SiGe HBTs also exhibits excellent linearity in both small signal and large signal radio frequency (RF) circuits [3, 4].

In order for high speed digital systems to properly make use of mm-wave signals, a need exists for high speed ADCs, which are able to accurately sample these high speed signals. Factors such as the ADC architecture, error sources and the technology used to fabricate such ADCs have to be investigated in order to develop an appropriate high speed ADC.

## 1.2 RESEARCH PROBLEM AND HYPOTHESIS

The problem addressed in this research is the limitation of available input bandwidth for high speed ADCs. Due to ADC architectures, jitter and technology capabilities, the available bandwidth of an ADC is limited. Different ADC architectures exist and each poses a trade-off on bandwidth, power consumption, resolution and sampling speeds. The effect of jitter is severe at high frequencies and alters the sampling clock of the ADC, causing incorrect sampling times and erroneous outputs. Other aspects include, but are not limited to, the integrated circuit layout plan and circuit design techniques.

Utilizing the 0.13 µm SiGe BiCMOS technology node may improve ADC performance since the available transistors have high $f_T$ and $f_{max}$ values that improve switching times allowing operation at high speeds. The $f_T$ and $f_{max}$ values are related to the internal parasitic capacitances of the transistors. Decreasing these parasitic capacitances leads to an increase in $f_T$ and $f_{max}$. The decrease in parasitic capacitances may improve the available bandwidth for transistors. The parasitic capacitances internal to the HBTs are, however, fixed to the

chosen manufacturing process, driving the need to employ modern SiGe technology nodes. The basic building block of the ADC is a differential amplifier configured as a comparator. The reduction in parasitic capacitances, provided in modern processes, thereby improves the available bandwidth obtainable by the differential configuration. The reduction in parasitic capacitances also reduces the time delays found in the clock circuitry. With higher time constants within the clock circuitry, the switching time of the clock circuit is delayed and in turn increases the system jitter.

The research will accordingly focus on input bandwidth improvement methods in order to determine their effectiveness for input signals in the low-GHz frequency range. The Cherry Hooper (C-H) amplifiers are commonly used in high speed optical systems for their high gain and large bandwidth. The research will determine the performance of the C-H amplifier when connected as a comparator for use in an ADC. Therefore the hypothesis can be stated as the following:

> *If input networks are capable of improved bandwidth and the Cherry Hooper amplifier provides high speed comparator performance, a high speed ADC may be feasible within the 0.13 µm SiGe BiCMOS technology node.*

## 1.3 JUSTIFICATION OF THE RESEARCH

Analogue to digital conversion is required for any digital system that monitors or uses signals from the analogue domain. As systems have advanced, the need for higher sampling ADCs has become an apparent necessity. In software defined radios and radar applications a large input bandwidth is needed to sample high speed signals without requiring mixing of these signals into intermediate frequency ranges. This eliminates the components needed to mix the signals, which may corrupt or distort the information encapsulated in the signal. The sampling rate also increases with an increase in bandwidth due to the Nyquist criterion. The increase in signal and sampling frequency leads to needed improvements in circuit designs and improvements in technology nodes. As a result the 0.13 µm SiGe BiCMOS technology node was chosen as the prototype platform.

## 1.4 METHODOLOGY

In order to validate the hypothesis a literature study was undertaken on ADC architectures to determine a suitable architecture for high speed operation. Research was also conducted on comparators and methods used to improve the input bandwidth of an ADC. The SiGe BiCMOS technology node was investigated in order to determine the suitability of the technology node for high frequency operation. Simulations were subsequently performed in software packages optimised for integrated circuits (ICs) within the SiGe BiCMOS technology node in order to strengthen the hypothesis. To further validate the hypothesis a prototype was developed for measurement purposes. Hardware test platforms were developed to accommodate measurement equipment and perform measurements on the prototype IC.

## 1.5 OUTLINE OF THE DISSERTATION

The report is organised as follows:

- Chapter 1: Introduction

  This chapter introduces the research problem and hypothesis. A short summary of the justification of the research and research methodology is given.
- Chapter 2: Literature review

  This chapter describes the body of knowledge relevant to the research conducted. The chapter is divided into six main sections namely: ADC characteristics, ADC architectures, Input bandwidth improvements, Jitter, SiGe-Based BiCMOS processes and HBTs and Current high speed ADCs. This is done in order to give a short background on ADC characteristics and provide the reader with insight on the formulation of the research questions.
- Chapter 3: Research methodology

  This chapter provides a detailed description of the methodology used to complete the research project. Software, simulators and the prototyping process are discussed and the justification thereof is provided.
- Chapter 4: Mathematical design and simulations

The chapter provides the circuit designs for the prototype circuit. This consists of the comparator design as well as the input circuit and current source designs. The chapter concludes with the combined circuits in order to create an ADC. The simulation results for the circuits are discussed in this chapter. Simulation results are provided for each separate part of the ADC as well as for the entire ADC. Simulation results showing the improvement in ADC performance are also provided in support of the hypothesis.

- Chapter 5: Layout, fabrication and measurement results

  This chapter describes the layout of the circuits simulated in Chapter 4. Methods used in an attempt to properly prototype the simulated circuits are also provided in this chapter. The final layout micrographs are also provided. The prototype chip was funded by the MOSIS education programme (MEP) and was therefore a multi-project wafer (MPW). The chapter also includes the results obtained by measuring the prototype ADC. The measurement results aim to strengthen the hypothesis.
- Chapter 6: Conclusion

  The research is concluded in this chapter and the results obtained are discussed with suggestions for possible future work.

## 1.6 LIMITATIONS OF THE SCOPE OF THE RESEARCH

The scope of this research is limited to the bandwidth improvement for ADCs. ADC architectures, input circuits and high speed comparators need to be investigated in order to improve the available bandwidth of an ADC. Jitter causes the sampling instants to vary and does not directly influence available input bandwidth. Therefore, the reduction of jitter falls outside the scope of this research.

## 1.7 RESEARCH CONTRIBUTION

An ADC with a common collector (CC) input tree and C-H comparators were proposed, evaluated and tested using the 0.13 μm SiGe BiCMOS technology node. The use of input networks to reduce the effect of cumulative input capacitance from the comparators is not unique in itself, but the use of CC stages for performing this task is novel according to the

knowledge of the author. The prototype ADC was measured and characterised according to the IEEE 1241 ADC test methods. The IEEE slow ramp wave and a digital to analogue (DAC) variant test methodology were applied to obtain static performance metrics. The sine wave fit test methodology, described in the IEEE standard, was applied to obtain dynamic performance metrics. A detailed list of the contributions to the body of knowledge is provided here.

- Simulation results show a bandwidth improvement when using the CC tree as input stage for the comparators when compared to a standard C-H architecture.
- The C-H comparator shows high speed operation with an AC bandwidth greater than 10 GHz and time response allowing favourable results of up to 5 GHz.
- Dynamic measurement results showed an ENOB of 1.18 over a bandwidth of 0 - 2 GHz for the prototype two-bit flash ADC. Static measurement results showed maximum integral non-linearity (INL) and differential non-linearity (DNL) errors of 0.33 LSB.
- Power consumption of 180 mW for a two-bit ADC without integrated clocking was established. The prototype ADC occupied 1.75 mm × 1.155 mm die area with active circuits utilising 550 µm × 300 µm of the enclosed area.
- The effectiveness of the HBT devices within the 0.13 µm SiGe BiCMOS technology node was demonstrated through simulations and measurement results.

The following peer reviewed journal article has been submitted and was accepted for publication:

- N. Faure and S. Sinha, "High-speed Cherry Hooper Flash Analog-to-Digital Converter," *Microelectronics International*, vol. TBD, no. TBD, pp. TBD,

The research questions, mathematical design and initial simulation results were presented in December 2011 and November 2012 at the CSIR Radar and EW knowledge base event.

## 1.8 CONCLUSION

This chapter provided the foundation for the research and presented the formulation of the hypothesis. The research methodology, dissertation outline, limitations and research contributions were provided. Chapter 2 provides background to ADC fundamentals and technology advantages. Chapter 3 details the methodology used throughout the research

and Chapter 4 provides the mathematical design to support the hypothesis. Chapter 5 provides the prototype layout and measurement results of the research. Chapter 6 concludes the research through the critical evaluation of the hypothesis and presents suggestions for possible future work.

# CHAPTER 2 LITERATURE REVIEW

## 2.1 INTRODUCTION

With the advances in semiconductor technology it is now possible to develop high speed wireless transceivers in the millimetre-wave range [5]. ADC circuits need to advance in order to improve digital high speed systems [6]. The most common ADC architectures are multistep ADCs, parallel ADCs, integrating ADCs, DAC-based ADCs and oversampling ADCs [7, 8]. Important characteristics common to all ADC architectures are their resolution, sampling speed and quantisation error. The resolution of an ADC determines the accuracy at which the ADC is able to present an analogue input value in a digital format. A higher resolution results in a more accurate digital output word. ADCs produce outputs periodically and this is referred to as the sampling speed. When an ADC determines the value of an input signal, a probability exists to make an error in the range of ±½ least significant bit (LSB). This error is known as the quantisation error and can be improved by increasing the resolution of the ADC.

An HBT is a transistor fabricated from two materials such as silicon (Si) and germanium (Ge). A SiGe HBT has higher $f_{max}$ and $f_T$ than normal silicon bipolar junction transistors (BJTs) due to the increased mobility of germanium used in the base of the transistor [9]. This is advantageous in high speed systems since the transistors are able to perform adequately at higher frequencies. A BiCMOS integrated circuit makes use of both bipolar and complementary metal-oxide-semiconductor (CMOS) devices in one chip. This is done in order to make use of the strengths of both bipolar and metal-oxide-semiconductor (MOS) technologies.

## 2.2 ADC CHARACTERISTICS

This chapter provides background on ADC characteristics used to describe ADC performance.

### 2.2.1 ADC fundamentals

The analogue part of an ADC may consist of track and hold amplifier (THA) circuits, comparators, integrators and DACs. A THA is also sometimes referred to as a sample and hold (S/H) circuit. The digital part of an ADC consists of logic gates and latches. The composition of the ADC depends on the ADC architecture. THA circuits are used to hold an input signal at a constant level to provide enough time for the ADC to sample the input signal. The THA also limits the maximum performance characteristics of the ADC since the ADC is only able to sample signals as quickly as the THA is able to capture them. As mentioned earlier, an ADCs purpose is to convert an analogue signal into a binary word. This can be explained as follows. An ADC forms a ratio between a DC reference voltage ($V_{REF}$) and the input voltage ($v_{in}$) and then rounds the result to the nearest binary word ($D_o$) [7],

$$D_o = rnd\left(\frac{v_{IN}}{V_{REF}} 2^n\right), \tag{2.1}$$

where $n$ is the resolution of the ADC. The steps at which an ADC digitises a signal is called the quantisation level,

$$q = \frac{V_{REF}}{2^n} = LSB. \tag{2.2}$$

The maximum quantisation error an ideal ADC can produce is $\frac{1}{2}q$. The quantisation error resembles a sawtooth wave and knowing this information the rms quantisation error may be expressed mathematically as follows,

$$E_q = \frac{V_{REF}}{2^n\sqrt{12}}, \tag{2.3}$$

with $n$ the resolution and $E_q$ the rms quantisation noise [8]. Since the quantisation error is known, the signal to noise ratio (SNR) can be computed. The maximum quantisation error is ½ LSB and the SNR is found to be,

$$SNR_{max} = 6.02n + 1.76\ dB, \tag{2.4}$$

with $n$ the ADC resolution [8]. As (2.3) and (2.4) show, the resolution of an ADC plays an important role in noise tolerance in an ADC. An increase of 1 bit resolution halves the quantisation error and increases the SNR by 6.02 dB.

### 2.2.2 ADC performance characteristics

The quantisation error is common in all ADCs and is reduced when the ADC resolution is increased. Other ADC characteristics that influence ADC performance are discussed in this section. Figure 2.1 shows an ideal code transition scheme for a three-bit ADC with priority encoding. Each output code is separated by $q$ showing an ADC output code gain of 1 and maximum quantisation error of ½$q$. In Figure 2.2 possible error sources in an actual ADC output are plotted against an ideal ADC output.

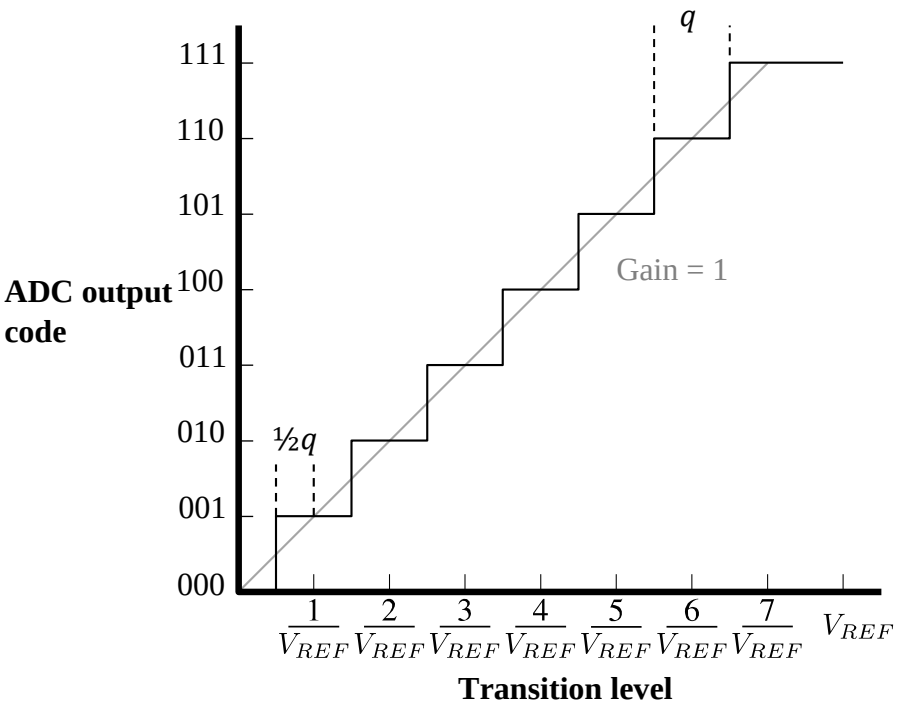


**Figure 2.1.** Ideal three-bit flash ADC output code

#### 2.2.2.1 Offset error

The offset error is caused by a voltage offset in the comparator which is used to compare the input signal with the reference voltage. Therefore the value between the ½ LSB and first actual binary code transition may differ from ideal conditions. In Figure 2.2 the offset error would result in the ADC never producing a 000 code output.

### 2.2.2.2 Gain error

Due to the possible offset, INL and DNL errors, the first and last transition code may deviate from the ideal. An ideal gain of an ADC is 1 as shown in Figure 2.1 and an actual ADCs transfer slope may differ as shown in Figure 2.2. This difference in output slope is the ADC gain error.

### 2.2.2.3 Linearity errors

Two linearity errors are common to ADCs namely INL and DNL.

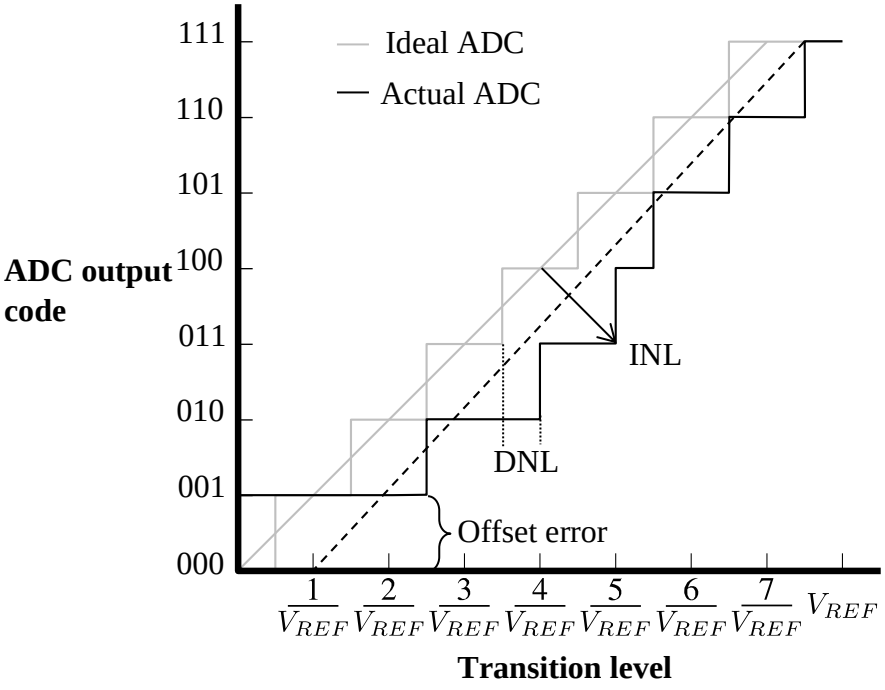


**Figure 2.2.** ADC error sources

The INL error is the deviation in transition values from the ideal transition values when the gain and offset errors have been removed. Linearity errors are caused by the devices used to fabricate the ADC. The DNL error is the deviation from the ideal code transition width, which is 1 LSB. The straight line INL can be determined using,

$$\text{INL} = \frac{V(k)-V(0)}{q} - k,\ 0 < k < 2^n - 1 \tag{2.5}$$

and the DNL can be determined using,

$$\text{DNL} = \frac{V(k+1)-V(k)}{q} - 1,\ 0 < k < 2^n - 2. \tag{2.6}$$

In (2.5) and (2.6) *V(k)* is the voltage transition level for code word *k*.

#### 2.2.2.4 Distortion

ADC distortion can be caused by INL, DNL, limitations in a preceding THA circuit, self-generated by the ADC and by voltage variable capacitance found in the converter active circuits. The resulting distortion causes a reduction in ENOB of the ADC.

#### 2.2.2.5 Spurious components

Spurious components are unwanted spectral lines which are caused by interference sources such as digital system clocks, non-ideal ADC performance or power line sources.

#### 2.2.2.6 Aperture jitter

Aperture jitter refers to time jitter in the clocks or sampling circuits in the ADC. The influence of clock jitter on the timing accuracy of an ADC can become severe at high frequencies [7, 10].

#### 2.2.2.7 Metastability

The metastable state occurs when a comparator's output is neither a logic high nor a logic low. Metastable errors are more likely to occur in high speed circuits since they have less time to regenerate to a proper output value, or are not geared for driving the load fast enough.

#### 2.2.2.8 Aliasing

To successfully sample an input signal, the sampling frequency must be at least twice the bandwidth of the input signal. This is called the Nyquist rate. If the sampling frequency is below this rate, aliasing will occur and an incorrect signal will be reconstructed. Anti-aliasing filters are sometimes incorporated before ADCs to reduce the effect of aliasing.

#### 2.2.2.9 SINAD, ENOB and FOM

The signal to noise and distortion ratio (SINAD) is used to describe the SNR of an ADC with the addition of distortion in the system. SINAD may be calculated from the residuals

after performing a sine-wave fit on the ADC output data, or by analysing the frequency contents of the output data [11]. The SINAD is used to determine the ENOB of an ADC. The ENOB value attempts to capture the ADC resolution with the addition of noise and distortion into one number. The ENOB can be calculated from [8],

$$ENOB = \frac{SINAD-1.76}{6.02}. \quad (2.7)$$

Therefore, when an *n*-bit ADC is designed, the ENOB can provide a good approximation of the performance level of the ADC. For example, a 10-bit ADC with an ENOB of 9 operates as an ideal 9-bit ADC. Therefore noise and distortion need to be kept to a minimum in order to maximise the SINAD. Another important aspect of an ADC is its power performance. The power figure of merit (FOM) is commonly used to compare different ADC approaches [12, 13, 14],

$$FOM = \frac{P}{2^{ENOB} F_{S-NYQ}}, \quad (2.8)$$

where $P$ is the power consumption and $F_{S\text{-}NYQ}$ is the resolution bandwidth (or in certain cases, the sampling rate). A good ADC must strive to have a low FOM since a low FOM relates to high ENOB, high $F_{S\text{-}NYQ}$ and low power consumption. Even though the FOM is used to show the performance quality of an ADC, it is not equal for all ADC architectures [12]. Certain ADC architectures are influenced by their input and output loads whereas others are not. There are thus some power dissipation effects which are not included in this FOM.

## 2.3 ADC ARCHITECTURES

This section will describe the various architectures available for ADCs and their various attributes.

### 2.3.1 Multistep ADCs

A multistep ADC consists of various building blocks, such as smaller ADCs and DACs, and converts the input in a series of steps. Multistep ADCs require a THA circuit to capture the input signal and hold it constant until the conversion steps are complete. Multistep ADCs have a relatively high resolution (12-bit) with moderate sampling speeds

(1-100 MHz) [7]. Multistep ADCs usually require fewer components than parallel ADCs with the same performance. With fewer components the circuit has the potential to be more power efficient, have less input capacitance and be less complex. The drawback is that THAs are required which may reduce the maximum bandwidth of the ADC.

### 2.3.2 Integrating ADCs

Integrating ADCs have high resolution (20 bits and higher) and very good linearity and almost no DNL error. An integrating ADC converts the input signal into a linear function of time and thereafter to a binary word. Integrating ADCs have good AC noise rejection, since the noise components which fall on multiples of its clock are averaged to zero [8]. The major drawback of integrating ADCs is that the resolution of the integrating ADC is inversely related to its sampling speed. An integrating ADC can therefore not have a high resolution with a high sampling speed. These types of ADCs are generally used for the accurate measurement of slowly varying signals, such as audio signals.

### 2.3.3 DAC-based ADCs

In a DAC-based ADC the input signal is compared to an output signal of a DAC. The input of the DAC is driven by a counter and it increments its value at the clock period. When the DAC output reaches the input value of the comparator, the comparator signals the counter to stop incrementing. The value on the DAC input is therefore the converted analogue value. The resolution of this ADC is therefore dependant on the DAC used. DACs are not as complex as ADCs and can have relatively high resolutions (16 bit). The drawbacks of DAC-based ADCs are their conversion times. The time it takes for the counter to reach the full scale input is $2^n - 1$ clock periods, with $n$ being the ADC resolution.

### 2.3.4 Oversampling ADCs

Oversampling, or sigma-delta ($\Sigma$-$\Delta$), ADCs make use of oversampling to reduce anti-alias filter requirements and reduce quantisation noise. Oversampling occurs when the

sampling rate is higher than the Nyquist rate. Oversampling ADCs have an SNR provided by [8],

$$SNR_{max} = 6.02(n + 0.5m) + 1.76\ dB\ , \quad (2.9)$$

with an oversampling ratio of $2^m$. This shows a half bit improvement for every octave of oversampling. The modulator is made up of a 1-bit ADC, 1-bit DAC and an integrator used to integrate the difference between the input signal and the DAC output. A digital filter/decimator is needed at the output of the ADC to suppress both spectral components and noise above the Nyquist rate and to revert the data rate back to the normal sampling rate. Oversampling ADCs are very linear and a THA circuit is unnecessary as an integrator is used. Even though a low bit ADC is used (1-2 bits), the ENOB of the oversampling ADC is larger than one bit [15].

### 2.3.5 Interleaved ADCs

When it seems that the maximum speed has been achieved with a certain ADC architecture, time interleaving can be used to create a higher speed ADC. By driving four similar ADCs with the same input signal, but with their clocks separated by 90°, creates an aggregate sample rate of four times the ADC's sample rate [7]. The increased effective sampling speed comes at the cost of introducing additional error sources. Mismatches between ADCs, particularly gain and offset errors, will cause spurious components in the signal. Offset and gain errors can be calibrated out of interleaved systems [13]. Another major problem with interleaved ADCs is inaccurate phasing of the clocks that interleave the ADCs. This can cause spurious components in the signal or cause the signal shape or timing to change. Phase errors can also be calibrated out if they occur [13]. Careful design is therefore needed for the clock distribution in interleaved ADCs to prevent frequent clock recalibration.

### 2.3.6 Parallel ADCs

Parallel ADCs, most commonly known as flash converters, are high speed converters. They consist of various comparators in parallel and complete a conversion in one step [16]. Comparators and logic gates can be clocked at very high frequencies and therefore flash

ADCs are able to sample input signals at very high speeds (1 GHz and higher) [7]. The drawback of flash converters is the complexity and power consumption of the ADC. The number of comparators needed in a flash ADC is $2^n - 1$ with $n$ the resolution of the ADC. Therefore, a 12-bit flash ADC requires 4095 comparators, which increases the power consumption dramatically. This increase in component count also increases the input capacitance of the ADC, which degrades ADC performance at high speeds. Due to the component count restrictions, flash ADCs usually have a low to moderate resolution (4-10 bits) [7]. To improve the static and dynamic performance of an ADC, the comparators should have identical performance characteristics. This becomes increasingly difficult with large comparator counts where all the devices should be matched [17]. This becomes practically impossible when considering standard process variations. As a result, parallel ADCs are often utilised for very high speed conversion with minimal resolution (1-4 bits). As a result of the unprecedented achievable input bandwidth, flash based ADCs are pursued in this research.

## 2.4 INPUT BANDWIDTH IMPROVEMENTS

### 2.4.1 Inductive peaking

Inductive peaking has been used to improve the bandwidth of amplifiers. An inductor is added in a series or shunt configuration of the amplifier. The inductor resonates with the parasitic capacitances charging each capacitor one at a time, improving the switching rate of each capacitor [18]. This extends the amplifier bandwidth, but the time needed to charge the parasitic capacitance introduces a delay within the system. Figure 2.3 shows an example of shunt inductive peaking in an amplifier circuit.

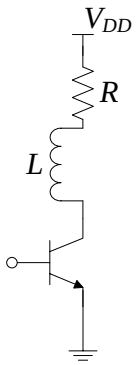


**Figure 2.3.** Shunt inductive peaking

In Figure 2.3 the inductor will resonate with the parasitic capacitance at the output of the common emitter configuration thus extending the bandwidth of the system. Active and passive methods have been used in literature to create an inductor. With small inductor values, active devices have been used and have obtained better performance than their passive counterparts [18]. When the inductor value increases, the die size of active devices also increase. This causes an increase in parasitic capacitances in the active devices which cause input bandwidth reduction. There is therefore a limit to when an active device can be used for inductive peaking. In contrast, passive inductors require significant real estate in the back-end-of-line stack to implement, achieving only moderate Q-values.

### 2.4.2 Input networks

With a high comparator count of a flash ADC, a high amount of parasitic capacitance is present in each comparator input. This reduces the amount of bandwidth the circuit is capable of utilising. Active input matching has been used to match the transmission line to a smaller input capacitance, improving the input bandwidth. Special care should be taken to properly match an input line to the high amount of parasitic capacitance of an ADC [14]. Figure 2.4 shows a simplified input network utilising a modified common-collector (CC) transistor configuration [14].

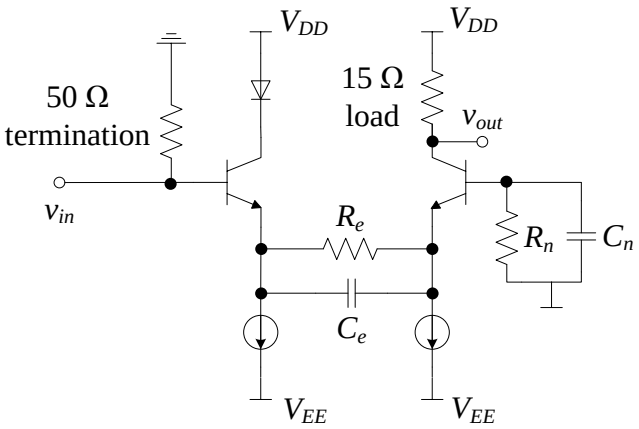


**Figure 2.4.** Active input matching network. Adapted from [14], with permission © IEEE 2009

The 50 Ω input transmission line is fed into the 50 Ω termination and input stage. The input stage amplifies the input signal with a gain of approximate unity to an output load of 15 Ω at the input of the comparators. The large parasitic capacitance generated by the high

amount of comparators is therefore terminated with a smaller resistance, increasing the frequency of the dominant poles. This type of input bandwidth improvement also limits the total amount of bandwidth and capacitive degeneration was implemented, with the addition of $C_e$, to maximise the bandwidth of the input stage. The configuration in Figure 2.4 used two different power sources as well, with positive ($V_{DD}$ = 1.2) and negative ($V_{EE}$ = -3.2) voltages, which increase the power consumption and complexity of the circuit. The standard CC transistor configuration is a widely used input circuit since it has a theoretical bandwidth close to the $f_T$ of the transistor. The parasitic capacitance at the input of the following stage sees the output resistance of the CC stage, which is very small ($\approx r_e$). The normal CC configuration therefore provides a high input bandwidth when used as an input stage. The CC input stage, however, still requires a 50 Ω input resistor for maximum power transfer from an external 50 Ω source.

## 2.5 COMPARATORS

Comparators are used to compare two voltage levels with each other. This is done by using a differential amplifier as shown in Figure 2.5.

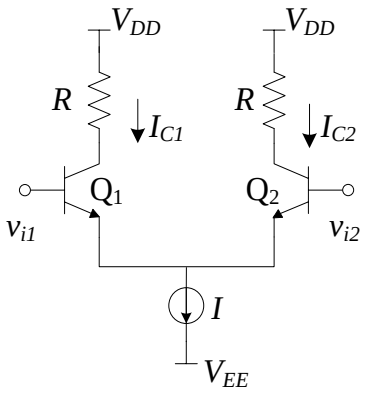


**Figure 2.5.** Differential amplifier

In Figure 2.5, when the differential amplifier is used as a comparator, an analogue input is fed into port $v_{i1}$ of the differential pair whereas port $v_{i2}$ is connected to a reference voltage. When the input voltage becomes higher than the reference voltage, the input transistor switches ‘on’ whereas the reference transistor switches ‘off’. When the input voltage drops below the reference voltage, the differential pairs revert to the input transistor being ‘off’ and the reference transistor in the ‘on’ state. This effect is illustrated in Figure 2.6 where

the collector currents, $I_{c1}$ and $I_{c2}$, of a differential pair are shown for a difference in differential input voltage. In Figure 2.6, $V_T$ (=kT/q) is the thermal voltage of the transistor which is approximately 26 mV at room temperature and $V_{id}$ is the voltage difference between the inputs of both transistors. $I_{TAIL}$ is the bias current at the emitter of both transistors with $\alpha_F$ the ratio between the collector and emitter current. When analysing differential pairs, normal amplifier analysis is used and the input is either regarded as completely differential or common. Inductive peaking can be used to improve the bandwidth of a comparator, single-ended and differential. Other methods, such as the cascode of transistors, have been used to improve the bandwidth of a differential amplifier.

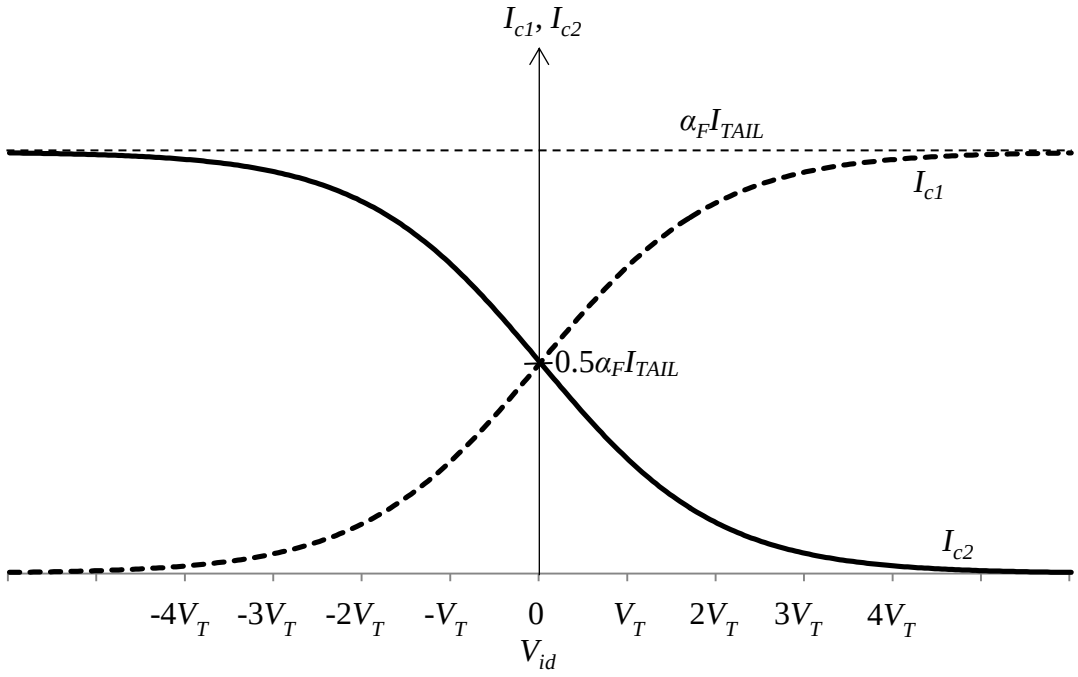


**Figure 2.6.** Collector currents as a function of differential input voltage. Taken from [9], with permission

The C-H amplifier has been developed and achieves high bandwidth and has been used in broadband applications [19]. Figure 2.7 shows a C-H amplifier configuration. In Figure 2.7 $R_f$ supplies a feedback current from the output voltage $v_o$. It is favourable that $R_f$ is large enough to minimise the amount of feedback from the output since it reduces the voltage at node A. The advantages of this configuration are that the resistance at nodes A and $v_o$ is very small. Since there are parasitic capacitances at both point A and $v_o$, the smaller resistances seen at each node result in high frequency poles. The C-H amplifier can be modified and used in differential pairs such as the one depicted in Figure 2.8. In the circuit of Figure 2.8 the feedback is implemented with a common emitter (CE) stage and the

addition of resistance $R_2$ provides a larger DC voltage output [20]. By increasing $R_f$ the gain can be increased considerably, but the bandwidth decreases.

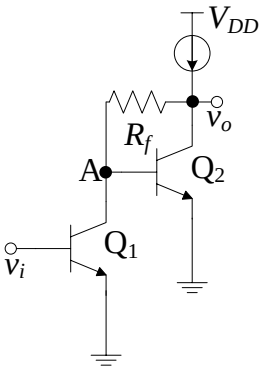


**Figure 2.7.** Single-ended C-H amplifier configuration. Adapted from [19], with permission

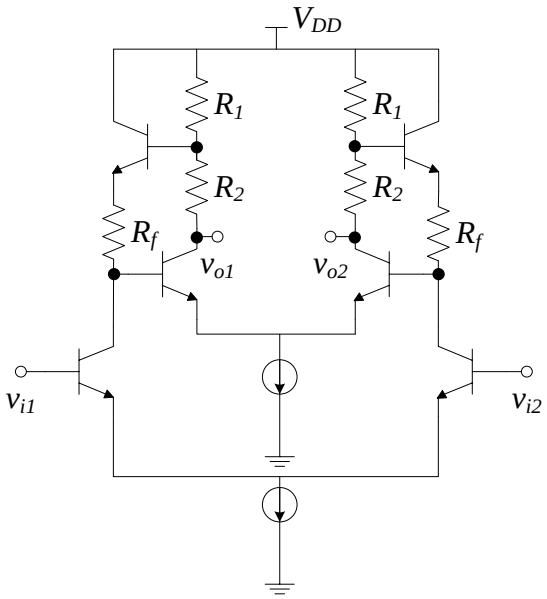


**Figure 2.8.** Variant of the C-H amplifier in a differential pair. Adapted from [20], with permission © IEEE 2004

By increasing $R_1$ the bandwidth improves by a small amount whereas the gain decreases considerably. For the values where $R_2$ is within $0 < R_2/R_1 < 2.5$, the gain is increased without adversely affecting the bandwidth [20**,** 21]. The C-H amplifier configuration therefore shows high speed capabilities with some trade-offs for 3 degrees of freedom (gain, bandwidth and output voltage swing).

## 2.6 JITTER

If proper care is not taken in the distribution of clock trees and floor planning, the clock signal can be affected by skew and cause incorrect sampling times in the ADC. Incorrect output values will therefore be given as shown in Figure 2.9. The output will therefore be distorted and not useable. [10] and [12] show that in order to improve sampling speeds, clock jitter must be kept to a minimum.

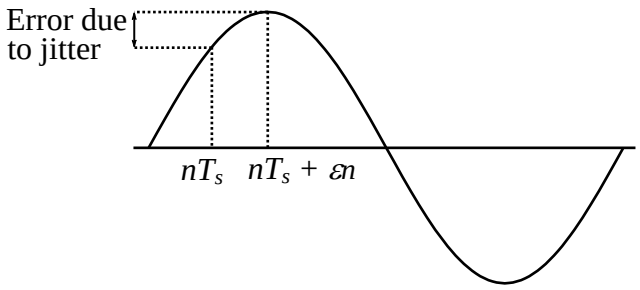


**Figure 2.9.** Error due to jitter. Taken from [22], with permission © IEEE 1999

Shown in Figure 2.9 is an input signal with $nT_s$ the $n^{th}$ sampling time of the system. The error introduced through jitter at the $n^{th}$ sampling time is $\varepsilon n$. The actual sampling time is then the sampling instant with the error added through jitter, $nT_s + \varepsilon n$, causing an erroneous result. The most common methods to remove the effect of jitter are careful floor planning, clean clock sources and THA circuits.

### 2.6.1 THA circuits

A THA circuit holds the input value constant for enough time to enable the ADC to sample the correct value (each ADC having a finite acquisition time). The effect of jitter is therefore accounted for since the input is held constant for a certain period of time. The same value will therefore be sampled by the ADC. Figure 2.10 shows an example of a typical THA circuit. In Figure 2.10 the input value is fed into an amplifier with the output to a switch. When the hold command is inactive, the capacitor, $C_H$, charges to the input value from the input amplifier. $C_H$ holds the value when the hold command is active and the value is transmitted to the ADC via the output amplifier. A separate circuit is sometimes used to drive the switch and is shown in Figure 2.10 as a switch driver. THA circuits also suffer from jitter and gain errors. In addition, THA circuits suffer from signal

droop in the capacitor used to hold the input value. This droop is important for small capacitance values where a fast switching time is needed [8].

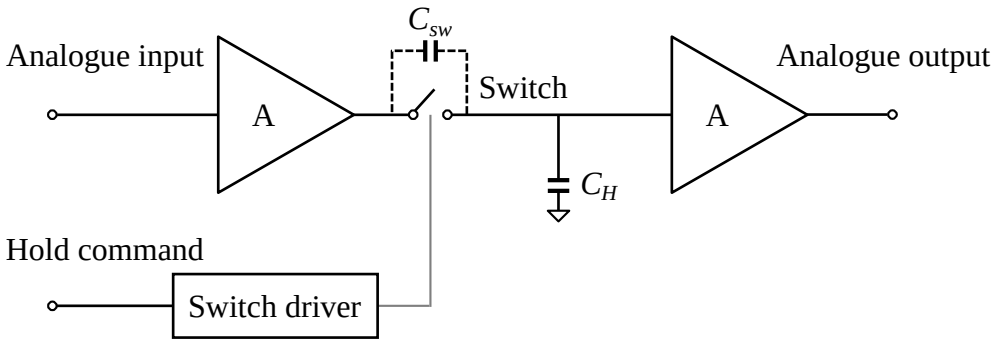


**Figure 2.10.** Typical THA circuit. Adapted from [23], with permission

Signal feed-through may also occur in the hold mode of the THA. This feed-through is caused by the parasitic capacitance, $C_{sw}$, of the switch used in the circuit. Small AC voltages are therefore able to couple from the hold capacitor to the input stage. Since a THA also has its own range of errors, it may degrade ADC performance even if the ADC is working properly.

## 2.7 SiGe-BASED BICMOS PROCESSES AND HBTS

### 2.7.1 SiGe-based BiCMOS process

As mentioned previously, in a BiCMOS process, devices from both bipolar and CMOS families are used in one chip. CMOS based ADCs typically use less power per conversion step than bipolar based ADCs. Therefore in a BiCMOS chip, the advantages of both technologies can be leveraged to design a high performance device. Several disadvantages exist in a SiGe-based BiCMOS process [24]. The collector current in HBT devices are approximately 1 mA, to achieve maximum $f_T$, and the base emitter voltage ($V_{BE}$) approaches 0.9 V [24]. This requires higher power supply voltages and can lead to higher power dissipation. The substrate is also conductive and may decrease the SINAD since part of the signal is conducted in the substrate itself. Higher speed HBTs can be developed in other materials such as Indium Phosphide (InP). HBTs developed in InP have $f_T$/ $f_{max}$ values over 400 GHz [24**,** 25]. The disadvantage with InP is the manufacturing process. InP is a difficult and expensive material to work with and this results in a more complex

manufacturing process when compared to SiGe manufacturing. SiGe has the advantage of high yield, low cost and large integration potential, whereas InP suffers from high cost and limited integration [25]. Technology nodes have been specifically developed in order to improve circuits within the mm-wave region [26, 27]. Modifications within the SiGe BiCMOS node in [26] have been performed to improve breakdown voltages of the HBTs and maintain high $f_T$/ $f_{max}$ values up to 150 GHz. Other improvements have been made at a higher cost for $f_T$ and $f_{max}$ values, reducing them to a lower 50/130 GHz, but obtained a very high breakdown voltage, in the region of 3.7 V compared to 1.7 V for devices with higher $f_T$/ $f_{max}$ values [27]. This improvement in breakdown voltage can provide flexibility where a $f_T$/ $f_{max}$ value higher than 200 GHz is not required.

### 2.7.2 HBTs

HBTs have higher $f_T$ and $f_{max}$ values than ordinary BJTs. HBTs are therefore more favoured in high speed circuits. In a SiGe HBT the *n*-type region is made from Si whereas the *p*-type region, base of the *npn* transistor, is made from Ge or a SiGe compound. The junction between these regions forms a heterojunction [9], hence the name HBT. The operation of an HBT is similar to the BJT, but improved models are developed for HBTs since they operate at much higher frequencies. Figure 2.11 shows the high frequency model for BJT devices.

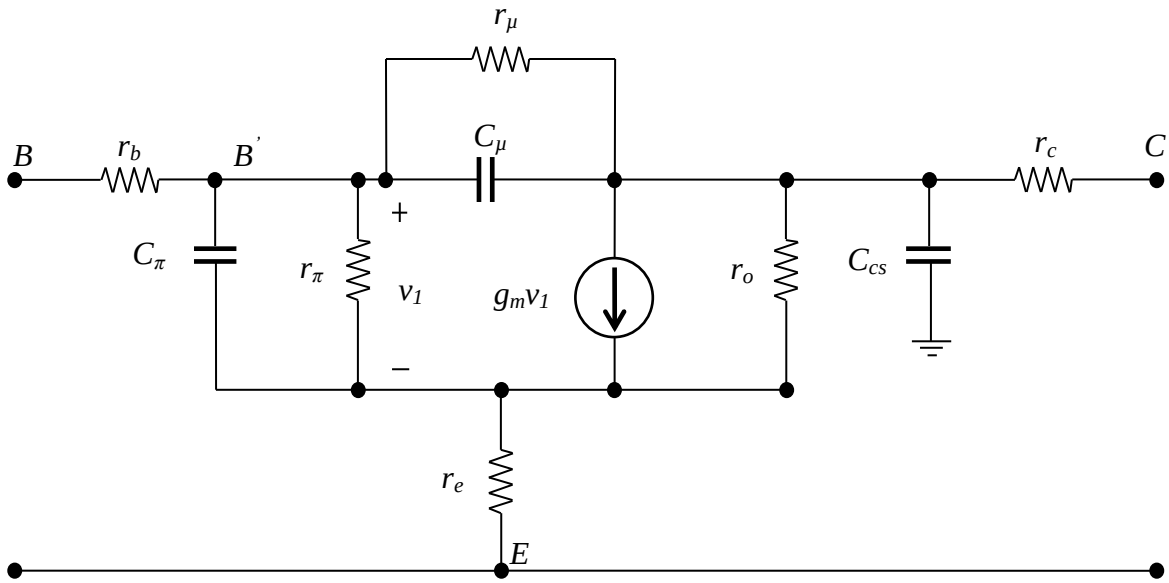


**Figure 2.11.** High frequency model of the BJT. Adopted from [9], with permission

In Figure 2.11, $r_\mu$ represents the increase $\Delta V_{CE}$ in $V_{CE}$ that causes a reduction $\Delta I_B$ in $I_B$. The capacitances $C_\mu$, $C_{CS}$ and $C_\pi$ are all intrinsic parasitic capacitances. It is important to note that the capacitance $C_{CS}$ presents capacitive coupling to the process substrate. This becomes increasingly important at mm-wave frequencies. The resistive parasitic elements are $r_b$, $r_c$ and $r_e$ and are caused by the finite resistance of the material at the base (*B*), collector (*C*) and emitter (*E*), also shown in Figure 2.11.

In a homojunction BJT, the emitter doping is selected to be much greater than the base doping to get emitter injection efficiency close to unity. Therefore the base region is relatively lightly doped whereas the emitter is heavily doped. To increase the $f_T$ of the transistor, the base width can be reduced. If the base doping remains constant, to keep the emitter injection efficiency constant, the base resistance ($r_b$) increases with the decrease in base width. This in turn decreases the speed of the transistor since $r_b$ forms a time constant with the base capacitance. A trade-off therefore exists between $f_T$ and $r_b$ and both limit the speed which can be obtained in practice [9]. In HBTs, Ge is added to the base of the transistor. Si has a higher band gap than Ge. Therefore the effective band gap in the base is reduced. The relatively higher band gap in the emitter can be used to increase the potential barrier to holes that can be injected from the base back to the emitter. This results in an increase in base doping and a decrease in emitter doping. By increasing the base doping, $r_b$ can be held constant whilst the base width is decreased and therefore a higher $f_T$ can be obtained. The reduction in the emitter doping causes $C_{je}$ to reduce, which reduces the effective transit time, since $C_\pi = C_{je} + C_b$, and therefore $f_T$ increases. Another advantage is that the base-collector depletion region, in the base, is reduced when the transistor is operated in the forward active region resulting in an increase of the early voltage ($V_A$).

Since the BJT and HBT operate similarly (they only differ through the addition of Ge into the doping levels), the same model can be used for hand analysis, hand design and approximate two port modelling to determine the performance of a SiGe HBT [3]. When more accurate simulations are to be performed on HBTs, the model in Figure 2.11 becomes inadequate and more complex models have been derived for more accurate modelling, e.g. a more complex model for noise simulation and results up to 40 GHz have been performed [28]. Further improvements on high frequency HBT models have been made and are used in simulators. Various simulators make use of the SPICE Gummel-Poon (SGP) model

which has been used for a long time to simulate bipolar devices [29]. The SGP model does not account for various effects and is not accurate enough for modern transistors [29, 30]. This has led to the development of other models, such as the Vertical Bipolar Inter-Company (VBIC) model and high current model (HICUM). Several deficiencies exist in the SGP model [29] where the VBIC and HICUM models have accounted for deficiencies such as the early effect, quasi-saturation, substrate parasitic, avalanche multiplication and self-heating [30]. Software packages used to simulate circuits within the 0.13 µm SiGe BiCMOS node make use of the VBIC model for a more accurate prediction of circuit behaviour. Due to the complexity of the model, hand analysis is not an option and computer aided design (CAD) is used to verify circuit operation with more accurate results.

## 2.8 CURRENT HIGH SPEED ADC CIRCUITS

Various ADCs have been developed for use in high speed circuits. The most common architecture used is the flash architecture. As stated in Section 2.3.2, flash ADCs are the fastest ADCs, but suffer from high power consumption and low resolution. It is therefore difficult to design a high speed flash ADC and have a low FOM. Table 2.1 shows various high speed ADCs available with their most important characteristics and the impact factor of the journals they appear in. From the data in Table 2.1 it is clear that a trade-off in ADC design exists. When comparing the SiGe BiCMOS ADCs [14, 31], it is clear that the power consumption, sampling speed, bandwidth and ENOB have a close relationship. Their FOMs are nearly equal, but they differ greatly in their bandwidths. There is a small difference in ENOB as well. In [31] more attention was given to the clock and data distribution. The clock and data distribution is each performed by a tree of linear buffers. These trees drive the comparators thereby dividing the large capacitance of the comparator bank into the tree of buffers. The input capacitance of the tree is smaller than that of the comparator bank and enables the use of a high gain front-end amplifier with high bandwidth. The same type of tree is used for clock distribution enabling a clock of 35 GHz to be distributed between the comparators. This combination enables the ADC to sample inputs at 35 GS/s with a bandwidth of 8 GHz. The need for a THA circuit is also unnecessary and [31] shows that a THA drastically decreases the ENOB at higher frequencies. The ADC presented in [14] implements comparators with exclusive-or (XOR) gates to minimise power consumption. In normal ADCs the XOR gates are not

implemented into the comparators, but rather used after the comparators. This design method reduces the component count in the ADC therefore reducing the power consumption. The ADCs in [32] and [33] make use of CMOS technologies. It is clear that the process technology used for ADC fabrication makes a large difference in the ADC performance.

**Table 2.1.** Various ADC performance specifications

| | [14] | [31] | [32] | [33] | This work |
|---|---|---|---|---|---|
| Architecture | Dual-Nyquist flash | Flash | Successive-approximation | Sigma-Delta | Flash |
| Technology | 0.13 µm SiGe BiCMOS | 0.18 µm SiGe BiCMOS | 65 nm CMOS | 90 nm CMOS | 0.13 µm SiGe BiCMOS |
| Bits | 5 | 4 | 6 | 8 | 2 |
| ENOB | 4 | 3.7 | 3.9 | 7.1 | 1.18 |
| Sampling speed | 20-35 GS/s | 35 GS/s | 40 GS/s | 1 GS/s | N/A[3] |
| Bandwidth | > 20 GHz | 8 GHz | 18 GHz | 62.5 MHz | > 5 GHz (Simulated) 2 GHz (Measured) |
| Power dissipation | 4.8 W | 4.5 W | 1.5 W | 10.8 mW | 178 mW |
| FOM | ~11 pJ/sample | ~9.9 pJ/sample[1] | 3 pJ/sample | 78 pJ/sample[2] | ~39 pJ/sample |
| Journal impact factor | 3.106 | 3.106 | *Conference* | 0.694 | 0.659 |

1. FOM was calculated using (2.8) with P = 4.5 W, ENOB = 3.7 and $F_{S\text{-}NYQ}$ = 35 GS/s. FOM was not calculated in [31].
2. FOM was calculated using (2.8) with P = 10.8 mW, ENOB = 7.1 and $F_{S\text{-}NYQ}$ = 1 GS/s. FOM was not calculated in [33].
3. A front-end S/H circuit was used with a sampling rate of up to 4 GS/s

The CMOS devices have lower FOM than the BiCMOS ADCs due to the decreased power consumption in MOS devices. The ADC in [32] makes use of a successive approximation architecture, which is a form of multistep architecture, and achieves a faster sampling speed than both SiGe BiCMOS ADCs. The power consumption in [32] is much lower than the SiGe BiCMOS ADCs and contributes to its lower FOM. The sigma-delta ADC in [33]

has a high resolution, good power consumption, great FOM with a relatively high sampling speed, but a low bandwidth. The sigma-delta converter in [32] is therefore suitable for high speed applications with low bandwidth requirements. The low FOM in the CMOS devices accounts primarily for the lower power consumption of CMOS devices.

## 2.9 CONCLUSION

With the increase in speed and bandwidth requirements in modern communication systems, an ADC becomes the limiting factor in circuit design [34]. ADCs have been used extensively and various architectures have been developed to enhance ADC performance. High speed ADCs need to be developed in order for high speed digital systems to operate adequately. The available input bandwidth may pose a limit for high speed ADCs and cause a reduction in ENOB at high frequencies. Inductive peaking and input matching techniques have been used to improve input bandwidths in ADCs sampling up to 40 GS/s. THA circuits have been used to remove the effect of jitter, but have caused ADC performance degradation in certain architectures [31]. Comparator characteristics are also an important part of an ADC. The C-H differential amplifier configuration has been used for limiting amplifiers, high speed optical links, high speed DACs, as well as input/output buffers for high speed THAs and as variable gain amplifiers for wideband circuits in the mm-wave area [19, 20, 35, 36, 37, 38]. The selection of technology is an important aspect when an ADC is being prototyped for proper testing. Each technology has its own advantages and disadvantages. The SiGe BiCMOS process shows promise for high speed circuits with the HBTs having inherent high $f_T$ and $f_{max}$ frequencies. The SiGe process is also cost-effective compared to an exotic process such as InP, it is scalable and has low clock jitter [14]. The next chapter will describe the methodology used in the research process.

# CHAPTER 3 METHODOLOGY

## 3.1 INTRODUCTION

This chapter describes the outline of the methodology followed in the research in order to test the hypothesis. This includes information on the modelling, simulation tools, layout tools, technology node and measurement equipment used to verify the hypothesis.

## 3.2 JUSTIFICATION OF THE METHODOLOGY

Various ADCs have been designed, tested and described in literature. Simulations provide a prediction of practical circuit performance and the process design kits (PDKs) used in these simulators are updated for new technology nodes. These PDKs incorporate advanced device models, such as the VBIC and HICUM models, described in Section 2.7.2, to predict circuit performance. Simulation software, utilising the newest models for devices, therefore gives a good estimate of circuit performance. In order to strengthen the hypothesis a prototype is needed for measurements. Using IC design for high speed system prototypes is favoured due to the lessened parasitics and reduced skin effect. A PCB design is also necessary to properly test and bias the circuit. Wire bonding was used to connect the prototype to the test board in order to accommodate the measurement equipment for testing the prototype.

## 3.3 OUTLINE OF THE METHODOLOGY

The following list contains the research procedures followed in the design of the ADC to test the hypothesis.

- *Theoretical background* – Several ADC architectures exist and a literature study was performed in order to select an appropriate architecture for the research. An investigation of comparator and input circuitry was necessary in order to improve ADC bandwidth. From the information obtained in literature a hypothesis was formulated.

- *Mathematical design* – The mathematical design of the ADC is done in order to investigate the suitability and implement the proposed design. This consists of comparator, input network and current source circuit design.
- *Software aided design* – Simulation tools, such as Cadence Spectre Analog Design Environment (ADE), are used to simulate and optimise the ADC. The results are compared to expected results.
- *Low level design* – The ADC is prototyped within the 0.13 µm 8HP IBM SiGe BiCMOS process. This consists of the layout design which is done in Cadence Virtuoso Layout XL.

The outline of the methodology is illustrated in Figure 3.1.

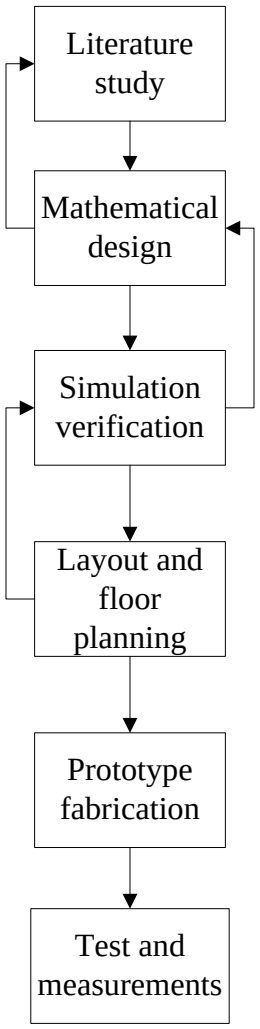


**Figure 3.1.** Outline of the methodology to test the hypothesis

Figure 3.1 shows that the methodology is performed in a recursive fashion. The research starts by performing a literature study to identify a research gap and formulating a hypothesis. Thereafter a mathematical design must be developed in order to test the

hypothesis. Insights gained in the mathematical design will require the literature to be revisited in order to develop a solution. After completion of the mathematical design, the design needs to be verified in a software simulator with PDKs for the technology node prototype. Simulations may show that the results are not acceptable and the previous steps may have to be revisited in order to resolve any problems. Circuit layout and floor planning can be completed after the mathematical design and simulations have been correlated. Due to the physical layout of the circuit, different input and output wire lengths are needed for each comparator section. Additional transmission line components used within the layout are added to the circuit in order to resimulate circuit performance. This may lead to the redesign of the circuit or referencing of literature in order to solve errors. The prototype is fabricated after the layout has been completed and the post-layout simulations are acceptable. Standard ADC characterisation techniques are studied in order to properly measure and characterise the device under test (DUT). Measurements are made in order to find a correlation between the practical operation of the design and theoretical observations in order to validate the hypothesis.

## 3.4 MATHEMATICAL DESIGN

Using information gathered from literature and circuit design, it is possible to determine the performance of the ADC with the IBM 8HP process. These results are verified using software simulators with more accurate device modelling. A favourable characteristic of the 0.13 µm 8HP SiGe BiCMOS node is the high $f_T$ facilitating higher bandwidth of the differential amplifiers. The HBTs in the 0.13 µm 8HP node therefore provide high gain at higher $f_T$ and $f_{max}$ values than their normal BJT counterparts.

## 3.5 MODELLING, SIMULATION AND LAYOUT DESIGN

The modelling and simulation of the design was done in the Cadence Virtuoso design package from Cadence Design Systems[1]. Cadence Design Systems has been chosen for electronic simulation since the Cadence company has plenty experience in the field of

[1] Cadence is a company focusing on electronic design automation (EDA) to improve system design in electronics, www.cadence.com.

electronic design and the software suite is one of the premier packages available for microelectronic design. The IBM 8HP models for the components used in fabrication are integrated into the Cadence environment, providing more accurate simulation results for the IBM 8HP process. The VBIC model is used for the HBTs in the process and a brief description of the VBIC model was given in Section 2.7.2. Cadence Layout XL was used to perform the layout of the ADC and Assura was used to perform design rule checks (DRCs) and layout versus schematic (LVS) checks. Spectre, a simulation tool in Cadence Virtuoso, was used to simulate and verify ADC operation and compare inputs with outputs.

## 3.6 MEASUREMENT PROCEDURE AND ADC CHARACTERISATION

### 3.6.1 Test setup

The measurement setup overview is shown in Figure 3.2. The dotted lines were optional and not present in all tests. Filters are added between the sine-wave generators and test devices in order to remove unwanted signal components. Digital and analogue oscilloscopes are used in order to capture high speed signals from the DUT. The data are transferred to a PC in order to be analysed using computer software.

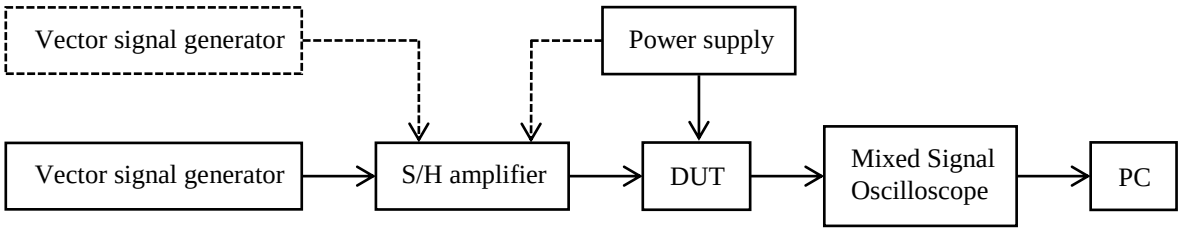


**Figure 3.2.** Measurement setup overview

A PCB design is required in order to properly bias the DUT as well as to connect the inputs and outputs to the signal generator and measurement equipment. The measurement setup and required connections are shown in Figure 3.3. The DUT is the prototype chip containing both a two-bit ADC and a single comparator. Wire bonding is used to connect the chip to the PCB. The ADC receives a single input from the signal generator, with the inputs of the comparators connected to reference voltages. An on-chip voltage resistor ladder is used to generate each comparator's reference voltage and $V_{REF}$ is used as the

biasing voltage for the ladder. The LSB voltage reference resistor is placed off-chip in order to measure the LSB voltage if $V_{REF}$ is present.

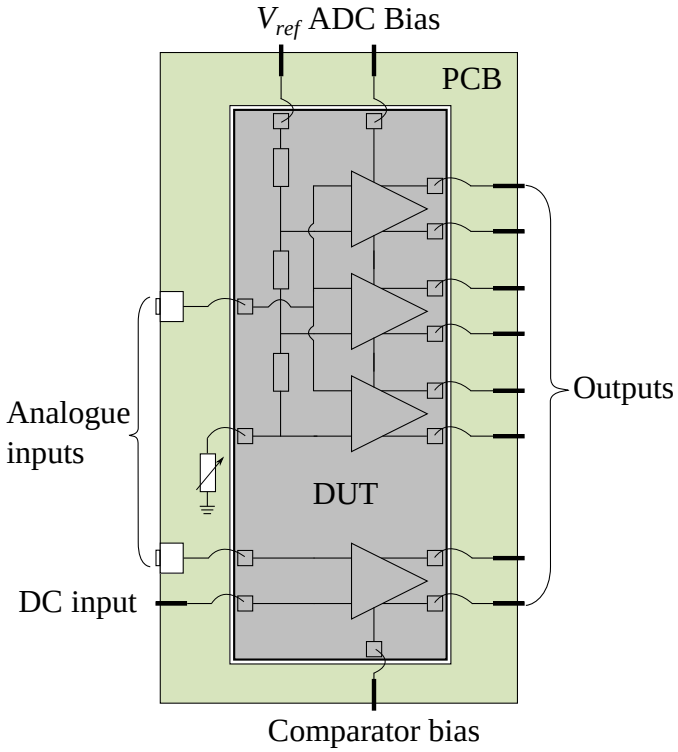


**Figure 3.3.** Measurement setup of DUT

A single comparator is also prototyped to test its individual performance. This is done in order to measure a single comparator if the two-bit ADC is faulty.

### 3.6.2 Measurement equipment

A Tektronix TDS7404B oscilloscope and a Tektronix MSO5104B mixed signal oscilloscope was determined suitable to capture the ADC outputs. The TDS7404B has an analogue bandwidth up to 4 GHz whereas the MSO5104 has an analogue bandwidth of 1 GHz. The MSO5104 has a digital bus with a bandwidth of up to 500 MHz. The TDS7404B is therefore used to measure analogue inputs larger than 1 GHz and the MSO5104B is used to measure digital outputs and clock frequencies up to 500 MHz and 1 GHz respectively.

### 3.6.3 ADC characterisation

Static and dynamic performance tests must be used for an ADC. A popular method for static tests is the histogram testing methodology and feedback DAC methodology [11]. In a histogram test the converter code transition levels are not measured directly, but rather through statistical analysis of converter activity [39]. Since the input stimulus is known, an expected amount of output code transitions can be computed for a select number of periods statistically relevant to the input signal. Ramp and sine-wave signals can be used for such tests, as shown in Figure 3.4. Also shown in Figure 3.4 are the code transition counts.

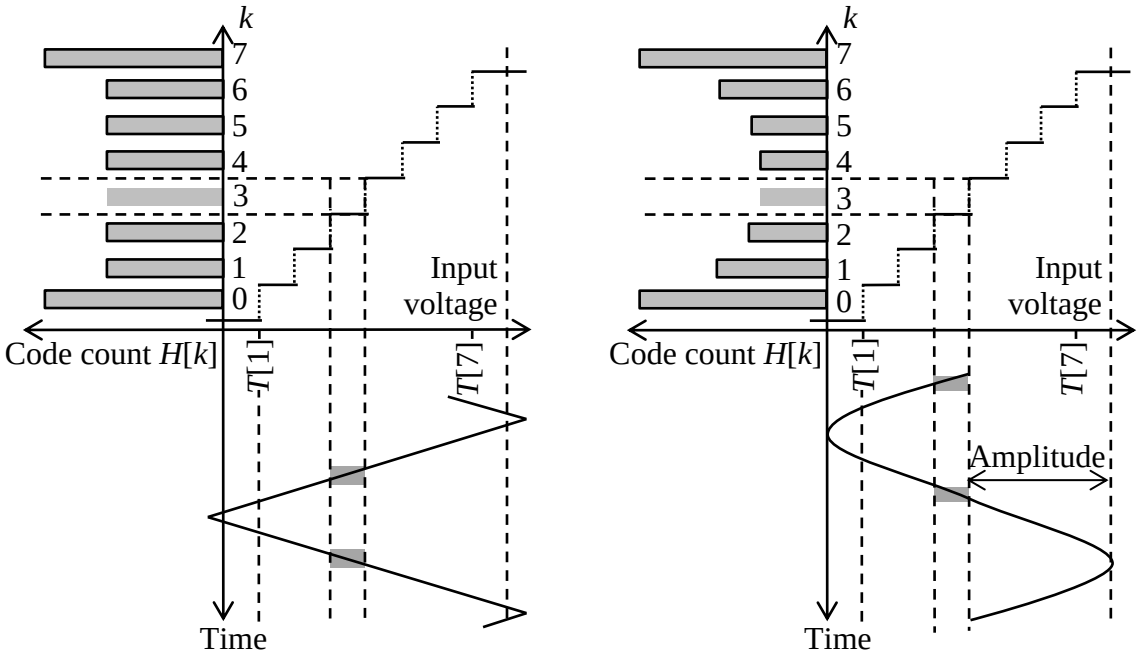


**Figure 3.4.** Ramp and sine-wave histogram testing. Taken from [39], with permission

In the feedback DAC testing methodology the ADC input is connected to a DAC output and the ADC output is connected to a word comparator. The word comparator compares the ADC output to a list of known ADC outputs. If the output doesn't match a known value, the word comparator increases the DAC output until the ADC output changes. In this manner the ADC transition voltages can be determined. Using the transition levels, the INL and DNL of the ADC can be computed. In order to test the dynamic performance of an ADC, various records of data are captured. Using the methods in [11] the noise and distortion (NAD), SINAD, total harmonic distortion (THD) and spurious free dynamic range (SFDR) can be computed from sine wave fit data and fast Fourier transform (FFT) results.

## 3.7 CONCLUSION

This chapter described the methodology used to test the hypothesis. An outline of the methodology was given with information and justification of the simulation tools used in the design of the ADC and ADC subsections. The measurement equipment was described along with their specifications that make them suitable for measuring the DUT.

# CHAPTER 4 MATHEMATICAL DESIGN AND SIMULATIONS

## 4.1 INTRODUCTION

In order to test the hypothesis, an ADC circuit needs to be designed to determine the performance of the proposed configuration in the hypothesis. This section describes the comparator design and input circuit design for the comparator circuit as well as the entire ADC design. The core of an ADC is a comparator circuit since it is used to determine the voltage levels at the input. A two-bit ADC was designed to investigate ADC performance using the designed comparators within the IBM 8HP process. A voltage supply, $V_{EE}$, of -3.3 V was selected and emitter coupled logic (ECL) was used in the comparator design.

## 4.2 INPUT CIRCUIT

### 4.2.1 Analysis and mathematical design of ADC input circuit

In order to separate the comparator input capacitances, a two stage CC tree was used for the input circuit of the ADC, as shown in Figure 4.1.

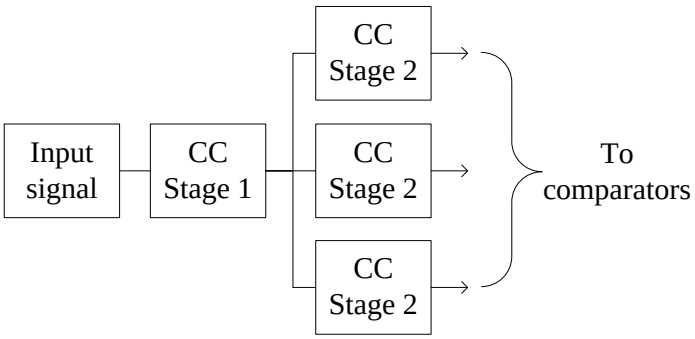


**Figure 4.1.** Input circuit tree

The CC tree was chosen since it has a low output impedance and high bandwidth. Figure 4.2 shows a CC stage with its small-signal equivalent model, where the resistance was replaced with complex impedance. In Figure 4.2 $R_S$ is the signal generator source resistance, $Z_\pi$ is the impedance formed by $r_\pi$ and $C_\pi$. $Z_O$ is the load resistance connected to the emitter of the transistor. The parasitic capacitance $C_\mu$ was ignored since it is small

compared to $C_\pi$ and $r_o$ was assumed to be very large. Additionally, the CC stage has unity gain; hence the Miller-effect does not increase the effective $C_\mu$ seen at the base of the transistor.

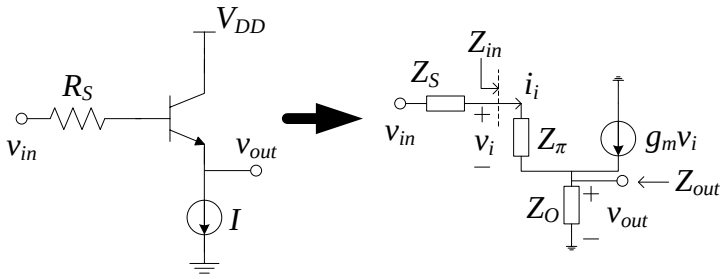


**Figure 4.2.** CC stage with small signal equivalent model

Using Figure 4.2 the important characteristics of the configuration can be determined and are shown in Table 4.1 [9].

**Table 4.1.** CC characteristic equations

| | | |
|---|---|---|
| Transfer function | $\frac{v_{out}}{v_{in}} = \frac{g_m R_O + \frac{R_O}{r_\pi}}{1 + g_m R_O + \frac{R_S + R_O}{r_\pi}} \left(\frac{1 - \frac{s}{z_1}}{1 - \frac{s}{p_1}}\right)$ | (4.1) |
| Input resistance | $R_{in} \simeq r_\pi + (\beta_0 + 1) R_O$ | (4.2) |
| Output resistance | $R_{out} \simeq \frac{1}{g_m} + \frac{R_S}{\beta_0 + 1}$ | (4.3) |
| Dominant pole | $p_1 = \frac{1}{C_\pi (r_\pi \parallel \frac{R_S + R_O}{1 + g_m R_O})}$ | (4.4) |
| Dominant zero | $z_1 = \frac{g_m + \frac{1}{r_\pi}}{C_\pi}$ | (4.5) |

Figure 4.3 shows the first CC stage used in the design. In Figure 4.3 $R_S$ is the source resistance of the signal generator and therefore 50 Ω.

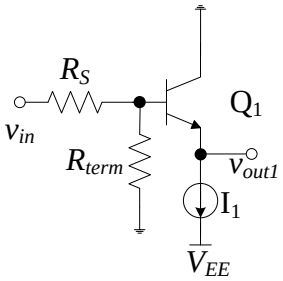


**Figure 4.3.** Input CC stage

Resistance $R_{term}$ is the termination resistance to minimise reflections and therefore also 50 Ω. Resistance $R_{term}$ adds a small parasitic capacitance to the input and reduces $R_S$ in (4.1)-(4.5) to $R_S \parallel R_{term}$. Throughout the design 3 µm emitter sized HBTs were used due to the high $f_T$ they are capable of achieving. A current of $I_1$ = 1 mA was used for the CC stage in Figure 4.3 to reduce the power consumption. The HBT at this chosen quiescent point has an approximate $f_T$ of 110 GHz. The CC stage has a bandwidth close to the device $f_T$ and 110 GHz was deemed acceptable as its cut-off frequency is much larger than the comparator cut-off.

The current source design used high breakdown HBTs. Using the model guide supplied by IBM, the approximate early voltage ($V_A$) was estimated and the output resistance was calculated. The input device parameters were calculated based on estimating the $\beta_0$ from the IBM PDK datasheets and using basic transistor equations from Table 4.1. The low frequency gain, pole and output resistance were determined and are shown in Table 4.2. Table 4.2 shows that the CC stage has a large bandwidth with values from the IBM 8HP process. If, however, the total input resistance value is close to or larger than $R_O$ the pole will decrease reducing the available bandwidth.

**Table 4.2.** First CC stage performance characteristics

| | |
|---|---|
| Low frequency gain | 0.975 V/V |
| Dominant pole | 90.65 GHz |
| Output resistance ($R_{o1}$) | 26 Ω |

The second CC stage is shown in Figure 4.4. A current of $I_2$ = 2 mA was used in the second stage to improve the bandwidth and reduce the output resistance even further. In Figure 4.4 the diode connected HBT is placed at the collector of transistor $Q_3$ to prevent $Q_3$ from having a higher than breakdown voltage ($BV_{ceo}$) over the collector-emitter terminals. As the voltage over the current source transistor changed, $V_A$ also changed. Figure 4.5 shows the complete input CC tree with biasing currents, terminations and output resistances.

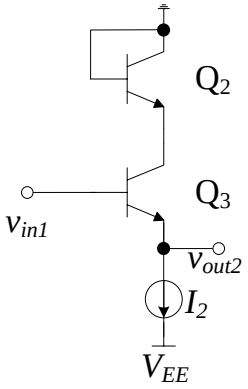


**Figure 4.4.** Second CC stage

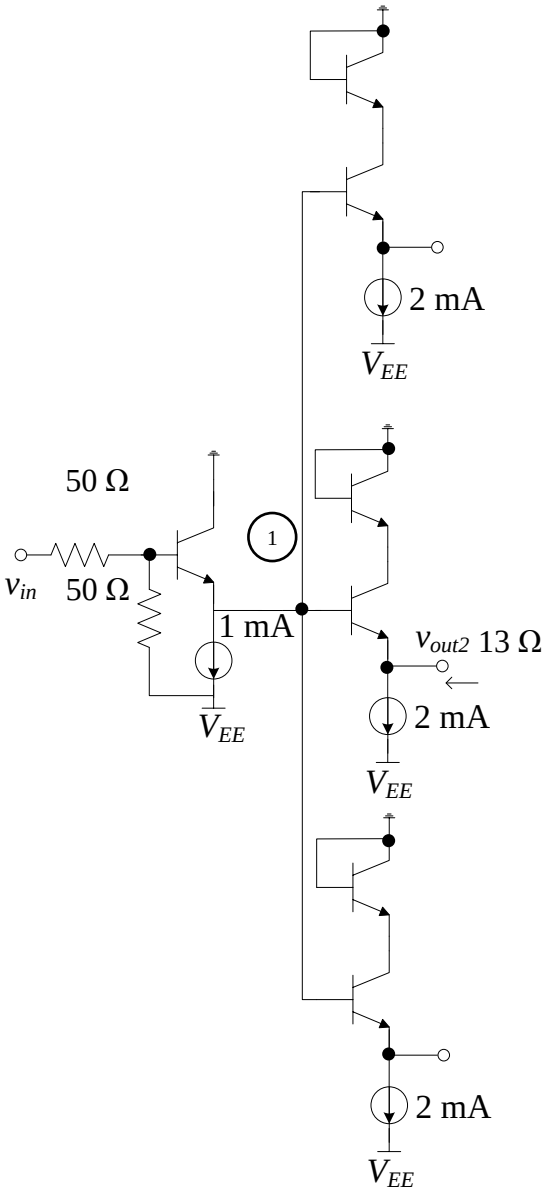


**Figure 4.5.** Complete input circuit diagram

The output resistance of the current source in this stage was recalculated using the new values. The same parameters were calculated for the second CC stage and are shown in Table 4.3. The total resistance seen at point 1 in Figure 4.5 is equal to the parallel combination between the input resistances of the second stage and output resistance of the first CC stage. The resistance at point 1 is therefore approximately $R_{o1}$.

**Table 4.3.** Second CC stage performance characteristics

| | |
|---|---|
| Low frequency gain, α | 0.99 |
| Dominant pole | 180.6 GHz |
| Output resistance ($R_{o2}$) | 13.09 Ω |

The total parasitic capacitance at point 1 is the sum of the input capacitances of the second CC stage as well as the substrate capacitance from the first CC stage. The time constant at point 1 is therefore approximately, $\tau_1 = R_{o1}(3\times C_\pi + C_{sub1})$. Therefore the input capacitances from the subsequent comparators are not present and these large capacitances cannot contribute to the time constant of the input stage. The source and termination resistances are shown as the two 50 Ω resistances and the bias currents are also shown for each CC stage. The total gain of the input circuit to each output is,

$$\frac{v_{out2}}{v_{in}} = \frac{v_{out1}}{v_{in}} \times \frac{v_{out2}}{v_{in1}} = 0.975 \times 0.99 \backsimeq 0.975. \tag{4.6}$$

The input circuit therefore has a close to unity gain and high bandwidth which is required for the input stage. Since the Miller effect does not play a role in the CC stage (gain~1), the total input capacitance of the parallel CC stage is lower than that of an amplifier stage. The CC stage placement was selected in order to separate comparator stages from each other and maintain low time constants at the parasitic capacitances present in the input network. Current sources were designed to bias the CC stages and are described in Section 4.4.

### 4.2.2 Simulation

Due to the on-chip 50 Ω termination the input signal is halved. Figure 4.6 shows the AC response of the input CC tree. An input voltage signal of 1 V was used for AC simulation purposes and the results in Figure 4.6 show the output voltage being halved (-6.04 dB ~ 500 mV) and therefore a close to unity gain is observed. A -3 dB bandwidth of 111 GHz is also shown in Figure 4.6. The result obtained in Figure 4.6 was expected since the only

function of the input network is to have a large bandwidth with close to unity gain. A larger bandwidth is observed when compared to the mathematical analysis and is due to the approximations used for the mathematical analysis.

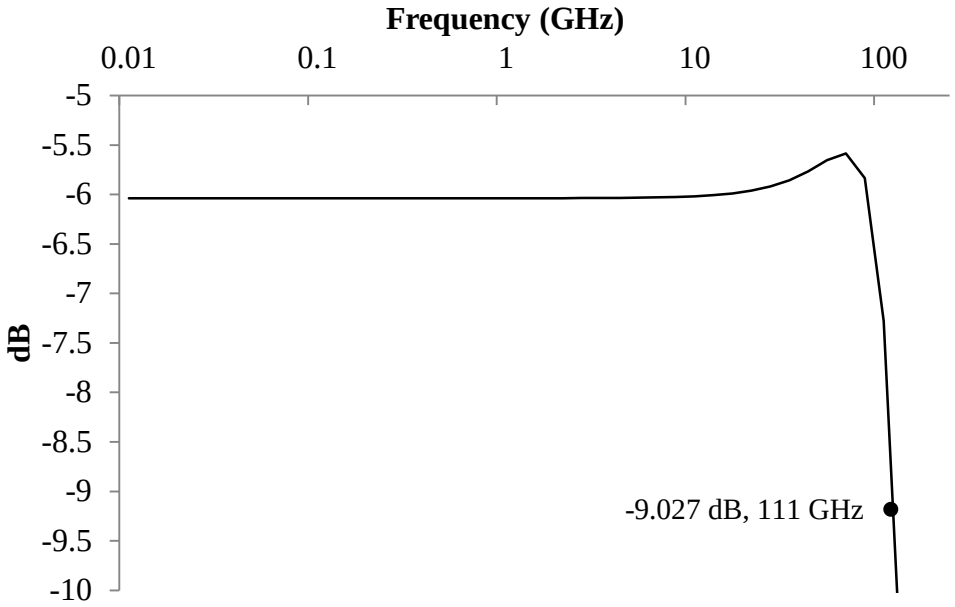


**Figure 4.6.** AC response of CC input tree

## 4.3 COMPARATOR

### 4.3.1 Analysis and mathematical design of ADC comparator

As briefly mentioned in Section 2.5, the comparator circuit is a differential amplifier. The C-H differential amplifier was chosen due to its high frequency of operation. The configuration in Figure 4.7 was used and was adopted from [20]. In Figure 4.7 $I_{CORE}$ and $I_{OUTER}$ represent the bias currents. For the comparator setup $v_{in}$ is the analogue input and $V_{REF}$ is the DC reference voltage (from reference ladder). The performance of the C-H amplifier in [20] was tested using a 47 GHz $f_T$ SiGe process. Equations given in [20] were used to determine the bandwidth and approximate overshoot for different resistance values. The amount of overshoot and bandwidth is given by [20],

$$Q = \left[\frac{g_{m5}C_1C_L(R_1+R_2)(R_Fg_{m5}+r_eg_{m5}+1)(R_1g_{m3}+r_eg_{m3}+1)}{(r_eg_{m3}+1)(R_Fg_{m5}C_1+C_1r_eg_{m5}+C_1+C_Lg_{m5}R_1+C_Lg_{m5}R_2)^2}\right]^{1/2}, \quad (4.7)$$

$$\omega_0 = \left[\frac{R_1+{g_{m3}}^{-1}+r_e}{C_1C_L({g_{m3}}^{-1}+r_e)(R_1+R_2)(R_F+r_e+{g_{m5}}^{-1})}\right]^{1/2}, \quad (4.8)$$

where $C_L$ is the load impedance which was converted to a single capacitance value.

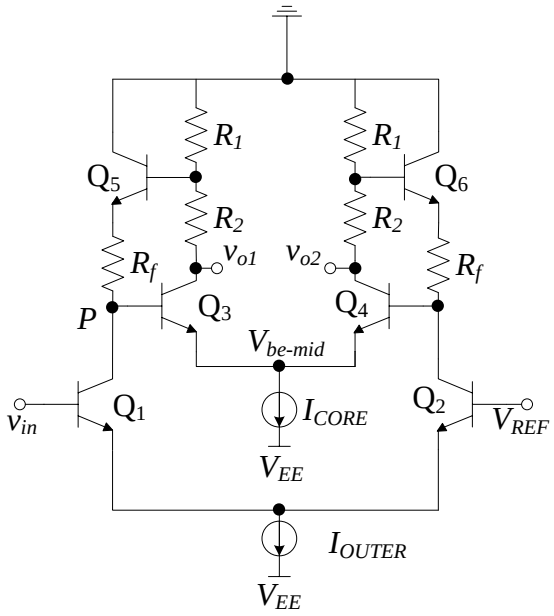


**Figure 4.7.** C-H amplifier. Adopted from [20], with permission © IEEE 2004

$C_1$ is the total parasitic capacitance resulting from $Q_1$ and $Q_3$ and is shown as node $P$ in Figure 4.7. The value of $C_1$ is given by [20],

$$C_1 = C_{\pi 3} + \left(1 - A_1^{-1}\right)C_{\mu 1} + C_{sub1} + C_{\mu 3}(1 - A_2). \tag{4.9}$$

The values of $A_1$ and $A_2$ are the gains across $Q_1$ and $Q_3$ respectively and are added to $C_1$ due to the Miller effect [20],

$$A_1 \cong \frac{(g_{m3}^{-1} + r_e)(R_f + r_e + g_{m5}^{-1})}{(g_{m1}^{-1} + r_e)(g_{m3}^{-1} + r_e + R_1)}, \tag{4.10}$$

$$A_2 \cong \frac{R_1 + R_2}{(g_{m3}^{-1} + r_e)}. \tag{4.11}$$

In order to compute the approximate $C_\pi$ and $C_\mu$ value the following well-known equation was used,

$$\omega_T = \frac{g_m}{C_\mu + C_\pi}. \tag{4.12}$$

with $\omega_T$ specified at the chosen quiescent point. The $C_{sub}$ capacitance is the capacitance from the transistor to the substrate and difficult to calculate precisely. The value for $C_{CS}$ and parasitic resistance, $r_e$, were estimated from the IBM 8HP PDK for use in the design equations. A collector current value of 4 mA ($I_{CORE}$) was used for transistors $Q_3$ and $Q_4$ to improve their switching speeds. Transistors $Q_1$, $Q_2$, $Q_5$ and $Q_6$ were biased at a lower current ($I_{OUTER}$) to reduce power consumption, but still provide high frequency bandwidth for the comparator. To achieve a high bandwidth for the C-H amplifier it is not necessary

to bias all transistors at their optimal $f_T$ current. Increasing $I_{OUTER}$ also increases the overshoot value, Q, and was therefore chosen low enough for less power consumption, but high enough for acceptable overshoot. Since the current in $Q_1$ and $Q_5$ are approximately equal, each transistor's transconductance is shown in Table 4.4.

**Table 4.4.** Transconductance of $Q_1(Q_2)$, $Q_3(Q_4)$ and $Q_5(Q_6)$

| | |
|---|---|
| $g_{m1} \approx g_{m2}$ | 153.85 mS |
| $g_{m3} \approx g_{m4}$ | 67.31 mS |
| $g_{m5} \approx g_{m6}$ | 67.31 mS |

The C-H differential stage (using equivalent half-circuit analysis) was re-evaluated from first principles and using Matlab the results were calculated. For the feedback network in a C-H amplifier a voltage is sensed at the output and a current is returned at the input. Therefore the feedback network is series-shunt and *h*-parameters were used to determine the transfer function from input to output. Figure 4.8 shows the half circuit of the C-H amplifier with the feedback network identified. Diode connected HBTs were placed at the collector terminals of $Q_1$ and $Q_3$. This was done in order to prevent the collector-emitter voltages exceeding the breakdown voltage.

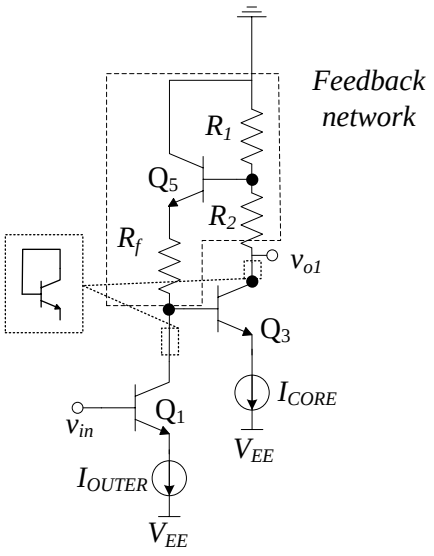


**Figure 4.8.** C-H half circuit

Figure 4.9 shows the feedback circuit removed from the rest of the circuit to determine the *h*-parameters. $R_1$, $R_2$ and $R_f$ are the same resistances as in Figure 4.7 and Figure 4.8. Using the small signal equivalent circuit the *h*-parameters were derived as,

$$h_{11f} = R_f + \frac{z_\pi + R_1||R_2}{\beta+1}, \tag{4.13}$$

$$h_{22f} = \frac{1}{R_1+R_2}, \tag{4.14}$$

$$h_{12f} = \frac{R_1}{R_1+R_2}, \tag{4.15}$$

with $z_\pi = r_\pi || \frac{1}{sC_\mu}$. Shown in Figure 4.9 are the voltage and current sources, $v_1$ and $i_2$ respectively, which are used to determine the *h*-parameters of the feedback network.

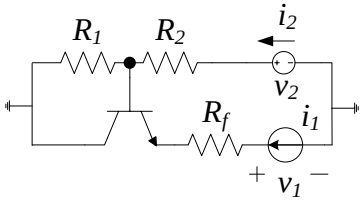


**Figure 4.9.** Feedback circuit for *h*-parameters

Using the *h*-parameters the open loop gain can be calculated as follows,

$$A_0 = \frac{v_{o2}}{v_{in}} \approx \frac{g_{m1}g_{m3}{h_{22}}^{-1}z_1z_2Z_1}{(z_1+r_{e1}(\beta))(z_2+R_S+\beta r_{e2})}, \tag{4.16}$$

with,

$$Z_1 = h_{11}||(z_2 + r_{e2}), \tag{4.17}$$

and $z_1$ and $z_2$ being the parallel impedance of $r_\pi$ and $C_\pi$ of each transistor. Table 4.5 shows the closed loop gain and cut-off frequency of the C-H amplifier using the equations provided from (4.7)-(4.17) with $R_1 = R_2 = 55$ ohm and $R_f = 150$ ohm.

**Table 4.5.** C-H amplifier gain and cut-off frequency

| | |
|---|---|
| Gain | 5.9 dB, 1.97 V/V |
| Cut-off frequency | 187 Grad/s, 29.76 GHz |

From the results in Table 4.5 it is clear that the C-H amplifier is capable of high bandwidth operation with an AC response of up to 29 GHz, although at moderate gain. The low gain causes a slow slew rate which is undesirable in an ADC. An additional gain stage can be implemented in order to improve the slew rate of the C-H amplifier [20].

### 4.3.2 Simulation

The C-H amplifier was simulated to determine its performance characteristics for high speed input signals using the IBM 8HP technology node. Figure 4.10 shows the AC response of the circuit with an AC signal input of 1 V. Ideal current sources were used since the goal of this simulation was to simulate ideal circuit performance. From Figure 4.10 the low frequency gain and -3 dB bandwidth is observed to be 6.8 dB and 28.81 GHz respectively. These results deviate slightly from the mathematical analysis with the low frequency gain being approximately 1 dB higher and cut-off frequency 0.9 GHz lower. At a somewhat higher frequency the simulated results show a gain closer to mathematical results with a deviation of 0.15 dB. The deviation from simulation results are the result of not taking into account all the parasitic effects in the mathematical analysis since it would increase computation time, with only a small margin of improvement.

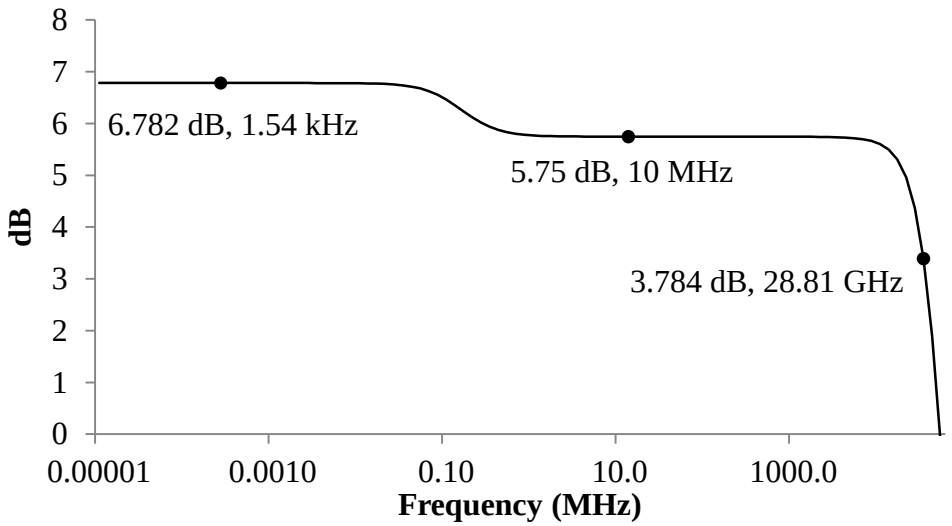


**Figure 4.10.** AC response of C-H differential amplifier

Since the ADC is supposed to switch at high frequencies it should have low rise and fall times. The rise and fall time effectively limits the speed of the ADC since it will switch at a low rate if the rise and fall times are high. The theoretical limit for the rise time of an amplifier is $\frac{0.34}{BW}$, with $BW$ the bandwidth of the system. Using the bandwidth result in Figure 4.10 gives a minimum rise time of approximately 12 ps. The rise and fall times were simulated using different input waves at different frequencies. In order to determine the instantaneous rise and fall times of the comparator, an input step response was simulated with a rise time of 1 ps.

Figure 4.11 shows the input block wave and output wave of the comparator. The input block wave was plotted with an offset to clearly show when the input switches. The rise and fall time (10-90%) of the C-H amplifier was 12 ps and 14 ps and is shown in Figure 4.11. The instantaneous response therefore shows a quick switching time and the circuit does not oscillate as a result from the over- and under-shoot, as observed in Figure 4.11. Figure 4.12 shows the output time response for an input sine wave at 1 GHz for both outputs of the comparator, V+ and V-. The rise and fall times are also shown in Figure 4.12. The rise and fall times are slower since the input rate of change is slower for a 1 GHz sine wave than that for the block wave input.

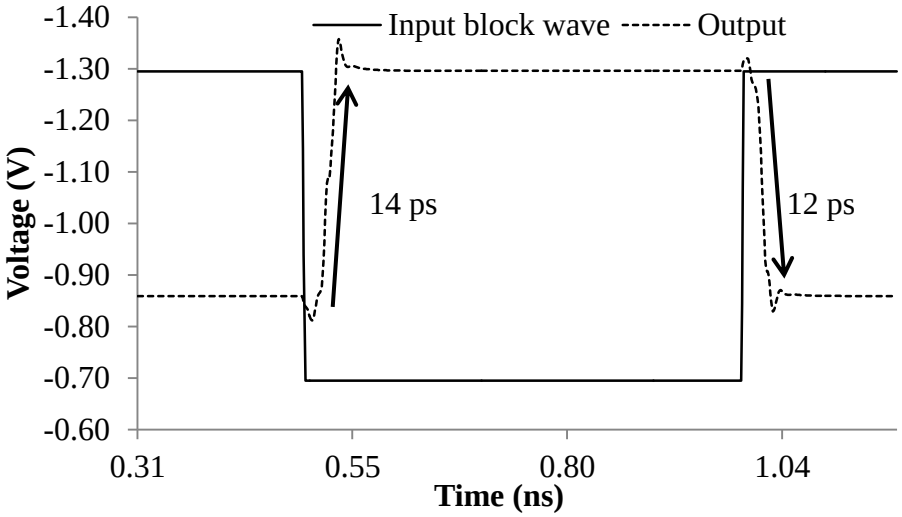


**Figure 4.11.** Output waveform with input step waveform

The rise and fall times can be improved by increasing the gain of the ADC which in turn results in a lower bandwidth.

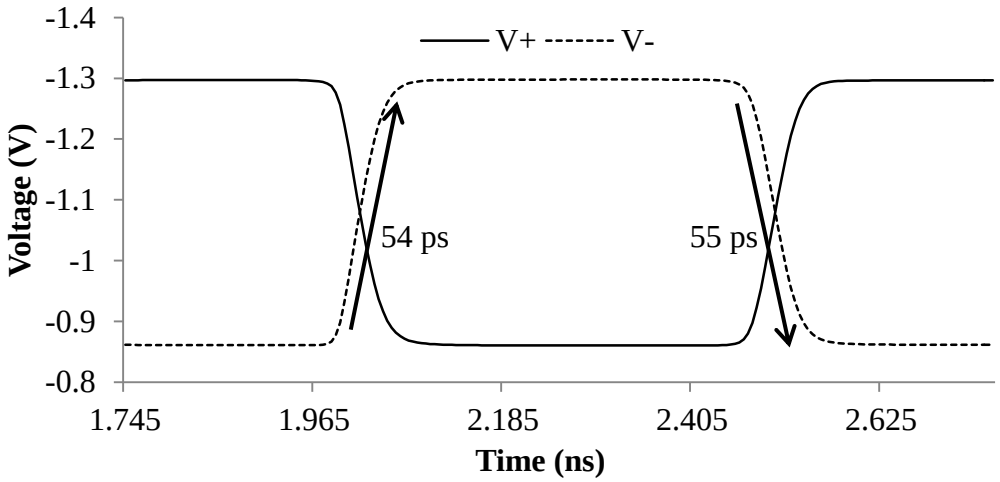


**Figure 4.12.** Output waveform for 1 GHz sine-wave input

Figure 4.13 shows a time response output for an input sine wave of 5 GHz and its rise and fall times are also provided in Figure 4.13. The rise and fall times for an input sine wave of 5 GHz closely match the instantaneous rise and fall times as simulated with a block wave input. From Figure 4.12 and Figure 4.13 it is clear that the C-H amplifier is capable of fast switching inputs when it is driven with high frequency input signals which coincide with the eye diagrams simulated in [20] with Q < 1. The output block waveforms are clearly distinguishable with minimal distortion.

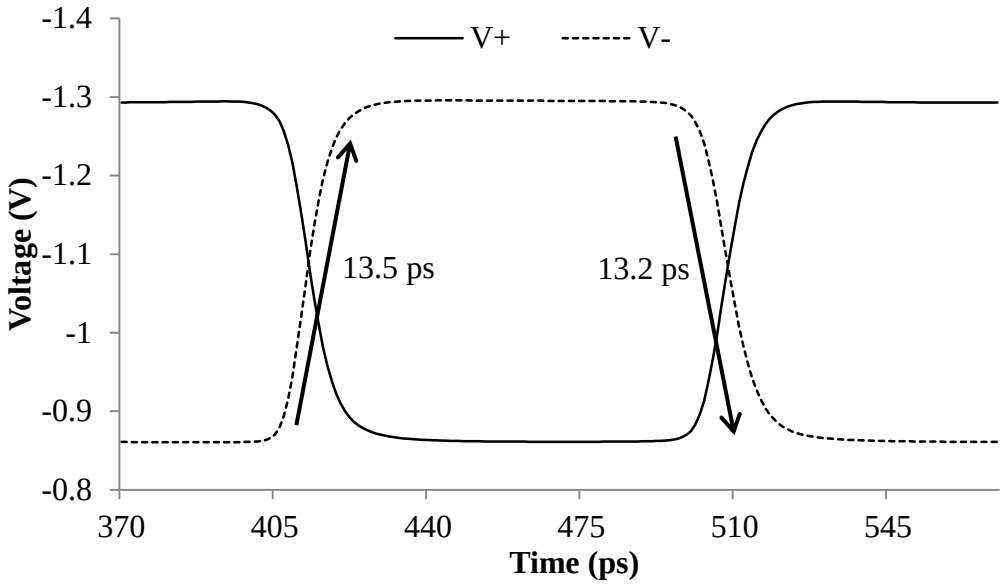


**Figure 4.13.** Output waveform for 5 GHz input sine wave

## 4.4 CURRENT SOURCES

Simple current mirrors were used for the input and output CC stages. Figure 4.14 shows the current mirror configuration for the input tree stage. A bias current, $I_{MIR}$, of 1 mA was used and $R_{bias}$ was computed to be 750 Ω. The devices in Figure 4.14 with $m$ = 2, mirrored $I_{MIR}$ twice therefore producing 2 mA for the second CC stage. The two diode connected transistors in Figure 4.14 were used to reduce the voltage headroom (reduction by 2 × $V_{BE}$) leading to a smaller $R_{bias}$ value, reducing the amount of space needed in the layout. Due to the $V_{BE}$ voltage drops from input to the comparator different current sources were used for the comparator. In order to closely mirror the tail current for the comparator stages, the operating point for the current source transistors should be the same.

Figure 4.15 shows the modified current mirror for the outer channel of the comparator to obtain closer operating points for $Q_1$ and $Q_2$. In the modified current source shown in Figure 4.15, $R_{Vce}$ is added to make $V_{CE}$ of $Q_1$ and $Q_2$ similar.

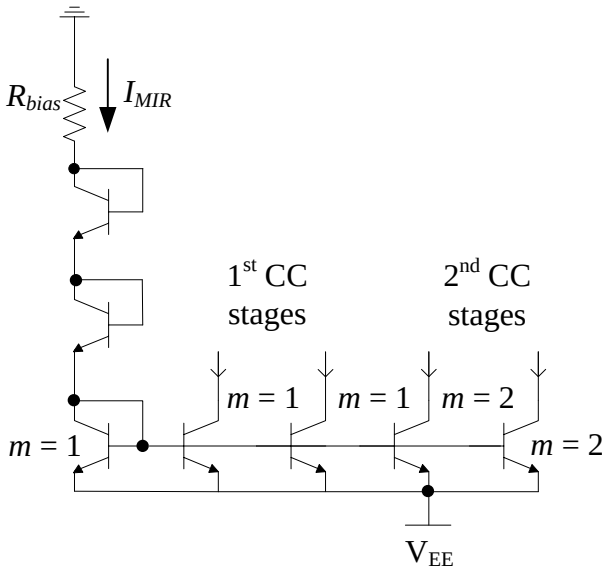


**Figure 4.14**. Current mirror configuration

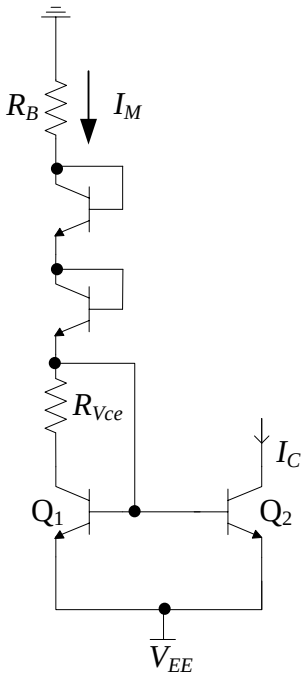


**Figure 4.15.** Modified current mirror

A bias current, $I_M$, for $I_{OUTER}$ was desired and $R_B$ was calculated to generate this bias current. In order to use fewer components in the design, a different current source was used for the inner channel of the comparator and is shown in Figure 4.16. In Figure 4.16 the bias current is generated through the $V_{BE1}$ voltage of $Q_1$. $V_{BE1}$ remains constant if the current ($I_E$), temperature and supply voltages remain constant. Since $R_D$ is fixed and connected to

the power supply rail, current $I_E$ can be controlled and held constant. In this manner a constant output current, $I_C$, can be achieved. An output current, $I_C$, of 4 mA was required for the inner channel of the comparator and $R_{bias1}$ was computed to achieve this. The only purpose of $R_D$ in Figure 4.16 is to supply a constant base current for $Q_2$.

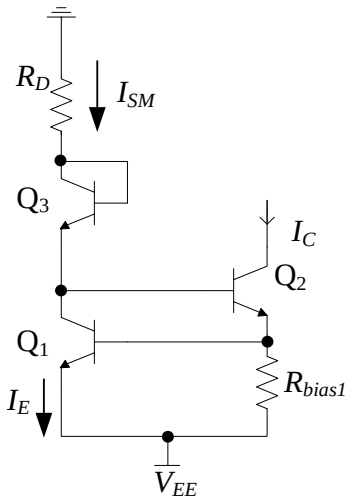


**Figure 4.16.** Base-emitter referenced current source

A current, $I_{SM}$, of 0.85 mA was selected and $R_D$ was computed subsequently. Table 4.6 shows the values obtained for the resistors used in the current sources.

**Table 4.6.** Resistor values for current sources

| | |
|---|---|
| $R_{bias}$ | 750 Ω |
| $R_B$ | 400 Ω |
| $R_{Vce}$ | 171 Ω |
| $R_D$ | 750 Ω |
| $R_{bias1}$ | 220 Ω |

The resistance values in Table 4.6 are relatively small and can be easily prototyped on chip without occupying a large area when using the *OPPRES* resistor. The *OPPRES* has a higher tolerance ratio than *KQRES* but generates less heat in comparison. Methods used to improve the tolerance of the resistor were implemented and explained in Section 5.2.

## 4.5 TWO-BIT FLASH ADC

For an *n*-bit flash ADC, $2^n - 1$ comparators are needed. Three comparators are therefore required for a two-bit flash ADC. The two-bit ADC configuration is shown in Figure 4.17.

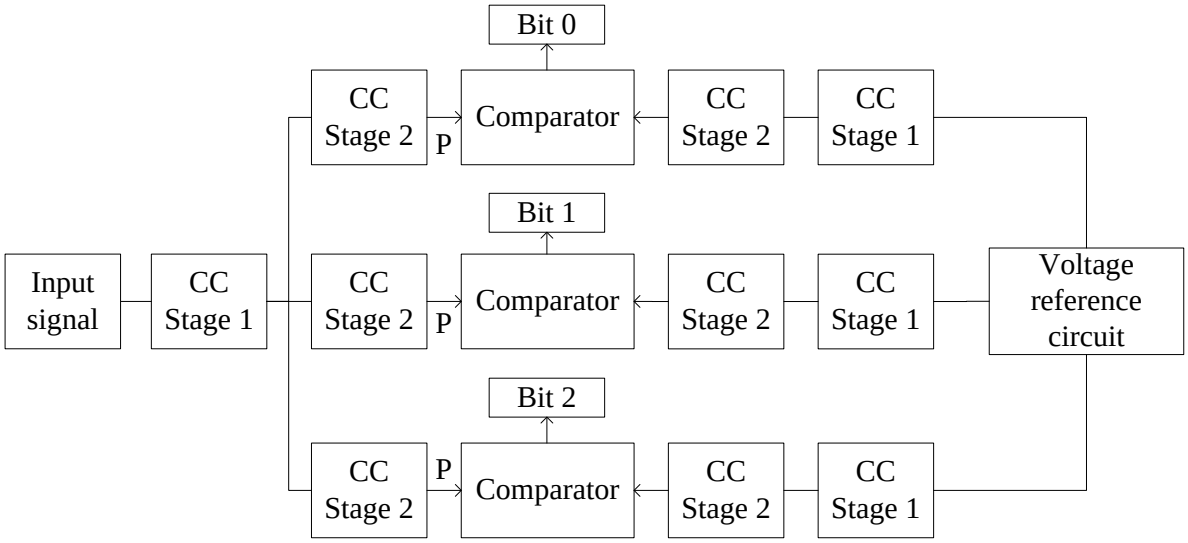


**Figure 4.17.** Two-bit flash ADC configuration

A CC stage is placed before each comparator as shown in Figure 4.17. In Figure 4.17 the input signal is wired into the first CC stage. The first CC stage terminates to 50 Ω at the input as discussed in Section 4.2. The first CC stage is then connected to the second stage as depicted in Figure 4.5. The second CC stage outputs are each connected to its own comparator input. Each bit voltage generated by the voltage reference circuit is connected to a CC tree identical to the CC tree at the ADC input. This was done in an attempt to keep both sides of the comparator in symmetry and have the same bias voltages for the input transistors of the comparator, however, at the cost of increased power consumption. A drawback of using a CC stage before each comparator is that more power is consumed by the circuit since each 2nd CC stage consumes 6.6 mW. Therefore, for a two-bit ADC an additional 19.8 mW is consumed by the circuit to achieve a wider bandwidth.

The voltage reference circuit is a simple resistor ladder, as shown in Figure 4.18, to produce the reference voltages. Each bit (Bit 0, Bit 1 and Bit 2 in Figure 4.18) is separated by one LSB. Output pads were made available for all of the comparator outputs in order to perform single ended or differential output measurements on each comparator output. Figure 4.19 shows the circuit diagram for one comparator, in the two-bit ADC, indicating

the inputs of the ADC. The resistance, $R_{ladder}$ and $R_{bit}$, will be different for each comparator as shown in Figure 4.18.

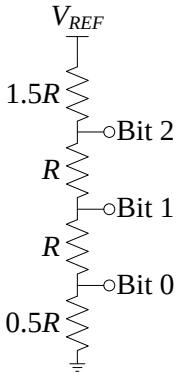


**Figure 4.18.** Voltage reference circuit

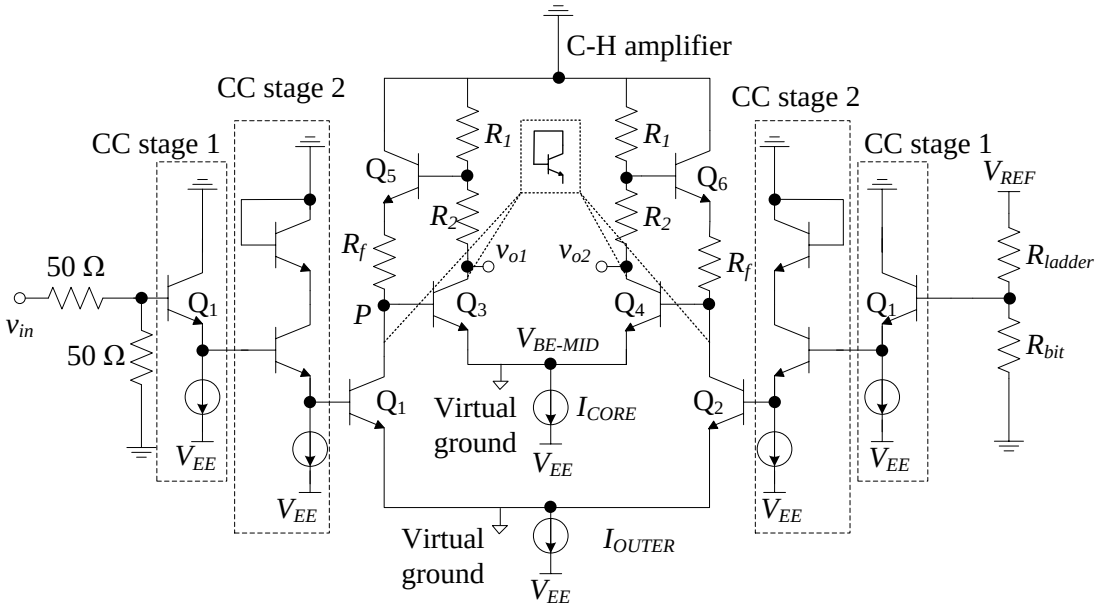


**Figure 4.19.** Single comparator output circuit diagram

### 4.5.1 Two-bit flash ADC with CC tree

Figure 4.20 shows an AC response for one comparator output. Figure 4.20 shows a high bandwidth of > 20 GHz with a gain of approximately 5 dB. This result was anticipated since the input tree had a very large bandwidth and close to unity gain, which would minimally affect the bandwidth and gain of the comparator stage. A reduction in gain is observed since the input tree has a close to unity gain, although not exactly one. Input

loading effects as well as the designed current sources also reduce the gain with the additional parasitic resistances and finite output resistance.

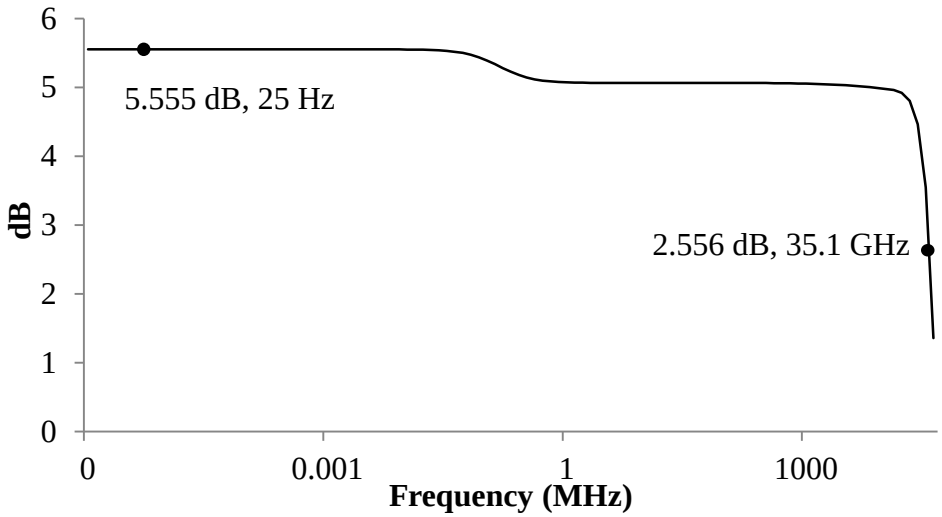


**Figure 4.20.** AC response for two-bit flash ADC

In first order calculations an infinite output resistance was assumed for the current sources resulting in the difference between simulation and mathematical analysis. A time response simulation was performed using a sine input wave at 1 GHz and 5 GHz to validate circuit performance when the CC tree and comparator is connected. The time response for an input signal with frequency of 1 GHz is shown in Figure 4.21.

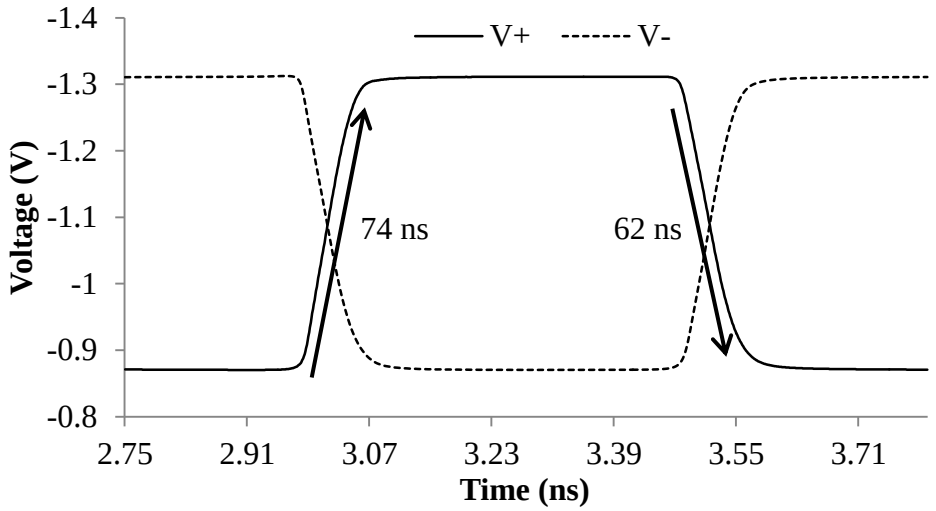


**Figure 4.21.** Time response output for two-bit ADC with input sine wave of 1 GHz

Comparing Figure 4.21 with Figure 4.12 shows that the figures are almost the same with each representing digital outputs. The slew rate of the combined circuit decreased showing a slower output response. Figure 4.22 shows the output waveforms for an input signal with a frequency of 5 GHz. In Figure 4.22 a small amount of oscillation is present with very

little overshoot in both output waves and a small decrease in slew rate for the inverting output of the comparator. The small amount of ripple and overshoot observed is a result from the response of the input tree, which has an inductive effect at high frequencies and prone to cause oscillations [9].

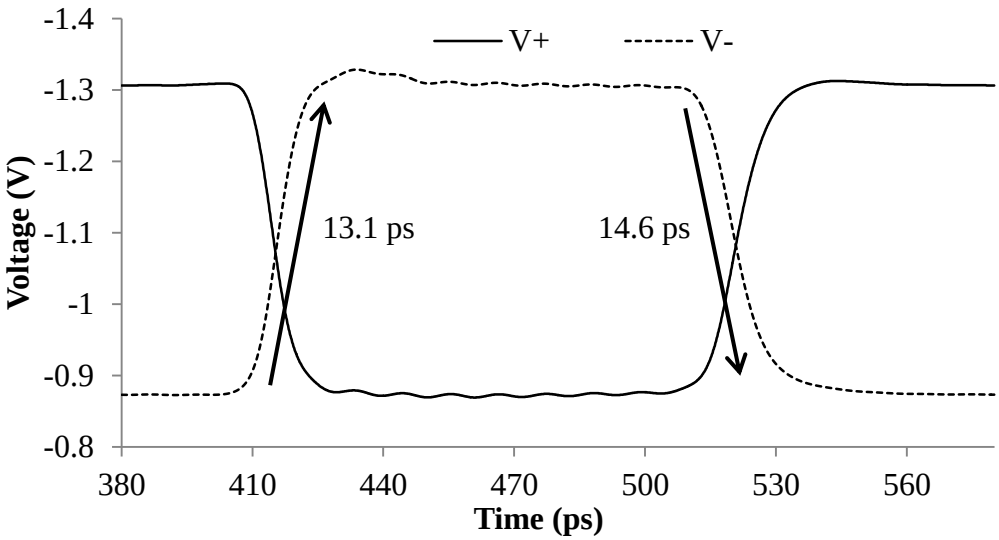


**Figure 4.22.** Time response output for two-bit ADC with input sine wave of 5 GHz

From the results in Figure 4.21 and Figure 4.22 it is clear that the addition of the CC tree does not affect the comparator function, making it suitable for use in an ADC. In order to test the two-bit ADC functionality a simulation setup was performed with an input signal, an offset voltage of -0.6 V and amplitude of 0.6 V with a frequency of 1 GHz. This provides a full scale input voltage range of 1.2 V and verifies the circuit configuration for ADC use. A reference voltage of 0.6 V was used since the input voltage is halved before the input transistor. The reference voltages for lowest to highest comparators were set to 75 mV, 225 mV and 375 mV respectively, as would be expected in a two-bit ADC configuration with a voltage reference of 600 mV.

Figure 4.23 shows the single ended output of all 3 comparators. Signal “Bit 0” is the comparator with the lowest reference voltage and “Bit 2” has the highest voltage reference value. The outputs in Figure 4.23 are as expected with the LSB comparator being in the ‘on’ (voltage level of -0.9 V) state for most of the duration when compared to the most significant bit (MSB). Since the LSB voltage is fairly small, the LSB will switch to the ‘off’ state for a very short duration. The bit values between each of the comparators are constant and can be seen in Figure 4.23 where the outputs switch at a constant rate after

each other. The CC tree and C-H configuration therefore shows effective two-bit ADC performance.

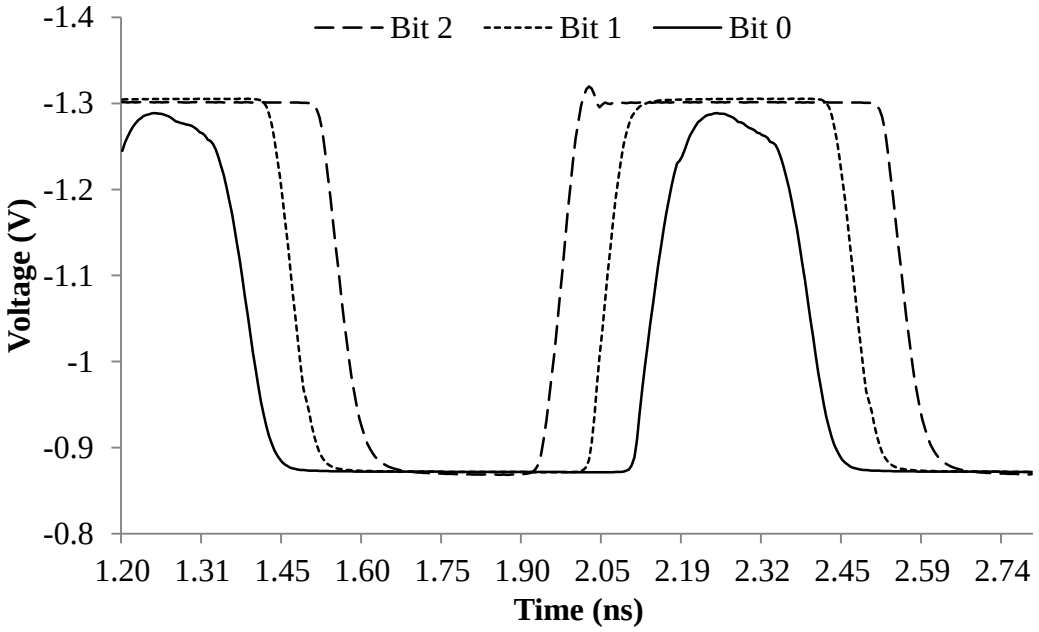


**Figure 4.23.** Single ended output waveforms for each ADC comparator output

### 4.5.2 Two-bit flash ADC without CC tree

In order to determine the effectiveness of the CC input tree, simulations were performed when the CC tree was not used, but rather where all the comparators are directly connected to each other. Figure 4.24 shows the circuit design for the two-bit flash ADC without the CC tree. When comparing Figure 4.24 with Figure 4.17 it is seen that the reference circuit is connected in the same manner to the CC stages and comparators. For simulation purposes a capacitance of 1 pF was added in front of each comparator, indicated by node P, as shown in Figure 4.17 and Figure 4.24. This was done to clearly show the difference between the different configurations. Figure 4.25 shows the AC response of the circuit set up as in Figure 4.17 and Figure 4.24.

The same amount of gain is achieved with both circuits, but the circuit with the CC tree shows an improved bandwidth up to three times that of the circuit excluding the CC tree. From Figure 4.25 it is also seen that a reduction in gain for the system is observed for

increased cumulative input capacitance. Therefore, if a large number of comparators exist (increased input capacitance), the circuit gain will decrease and reduce switching speeds.

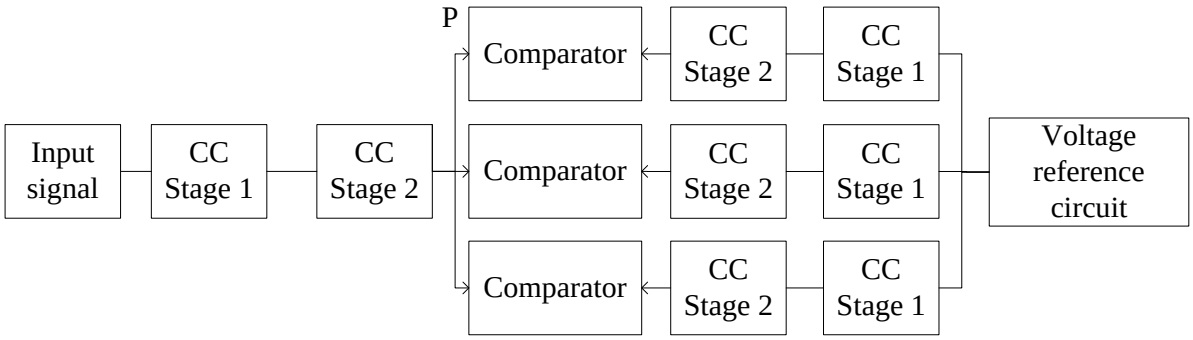


**Figure 4.24.** Two-bit ADC configuration without proposed CC tree at the input

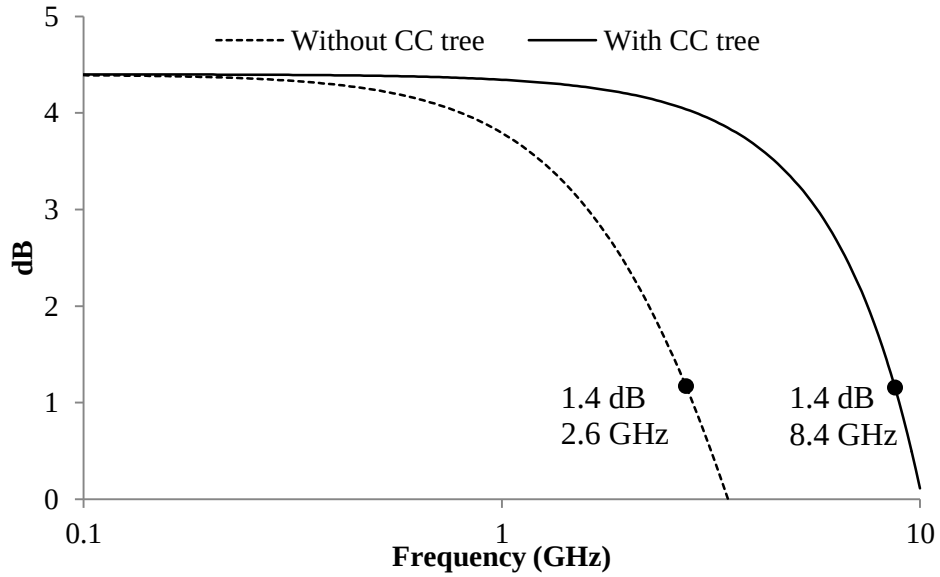


**Figure 4.25.** AC response showing comparison between ADC including CC tree and excluding CC tree

### 4.5.3 Two-bit flash ADC post layout simulations

Layout was completed using the Cadence Layout suite which has the 8 HP IBM PDKs included. The IBM PDKs include transmission lines as well as bends and were used in the layout of the circuit. These components were added to the schematic view and AC as well as time-response simulations were performed to determine circuit performance after layout was completed. Figure 4.26 shows the AC response of the circuit after layout components

were included. A small amount of gain reduction is present with a large reduction in bandwidth when comparing Figure 4.20 with Figure 4.26.

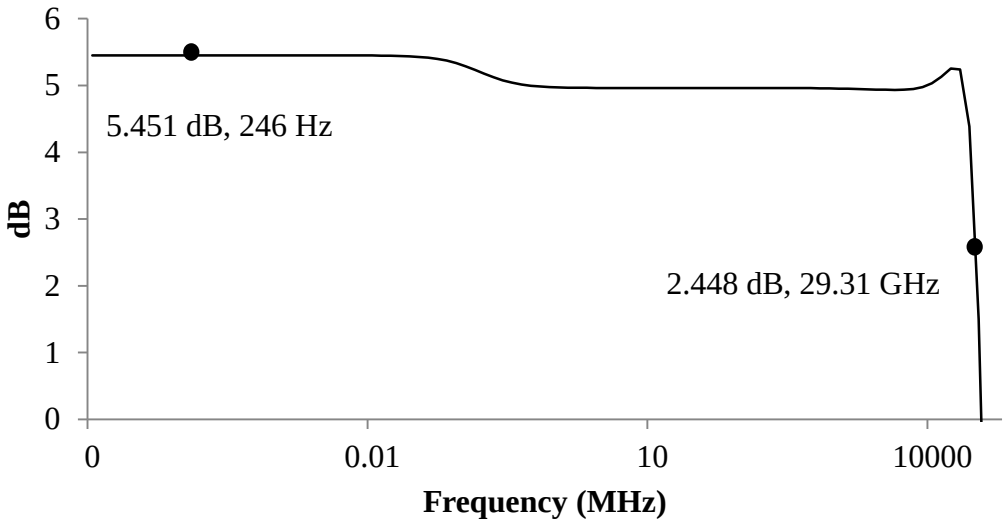


**Figure 4.26.** AC response of two-bit ADC post layout

These changes result from the addition of inductance in the input and output transmission lines of the circuit. Figure 4.27 and Figure 4.28 shows the time response for an input sine wave of 1 GHz and 5 GHz respectively.

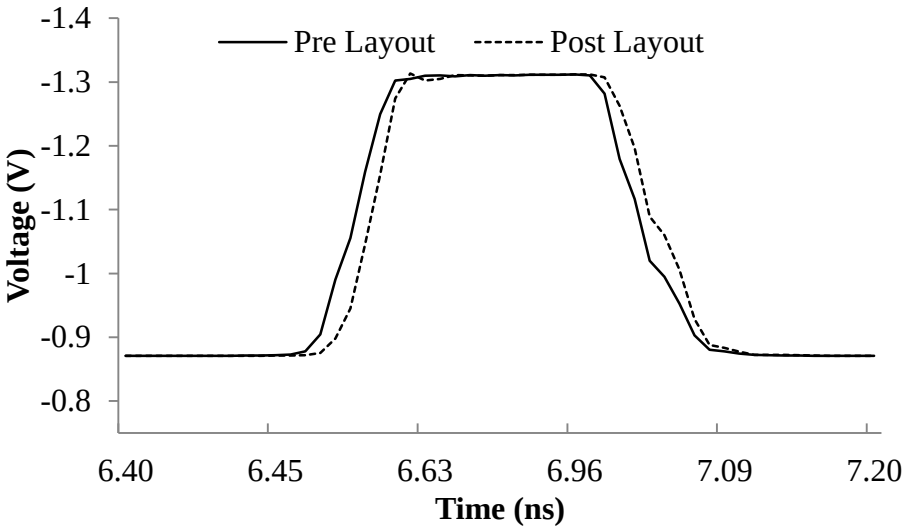


**Figure 4.27.** Single bit output waveform for 1 GHz sine-wave input

Figure 4.27 and Figure 4.28 also show the output before layout was completed for ease of comparison. From Figure 4.27 it is clear that after layout, the circuit still behaves normally at an input signal of 1 GHz. Small delays are present and are due to the added inductances. When an input signal of 5 GHz is used, the output waveform becomes distorted with oscillations and propagation delay which can be seen in Figure 4.28. This results from the fact that the effect of an inductance becomes higher as the frequency increases and the

addition of transmission lines at the input shows this effect. Even though the oscillations occur, the output is still within the 10/90% rise and fall time boundary of the output. Group delay simulations where performed for the two-bit ADC.

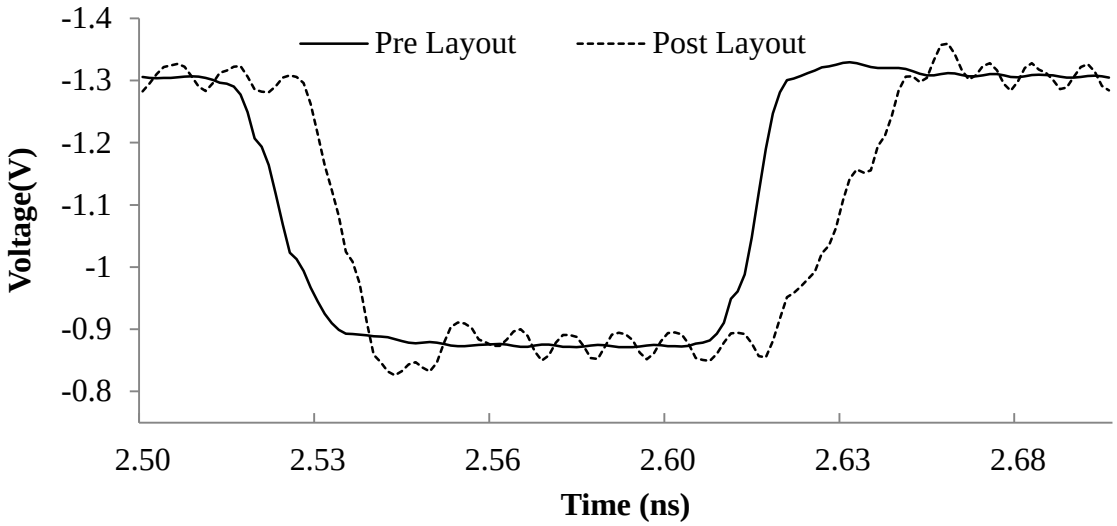


**Figure 4.28.** Output waveform for 5 GHz sine-wave input post layout

Figure 4.29 shows the group delays through each comparator output. Small deviations exist (close to 9 ps) between comparator outputs at low frequencies and converge for higher frequencies. This is acceptable since a delay of 1 ps at low frequencies will not affect the timing of the comparator outputs. The group delay simulation was repeated, but resistors $R_1$, $R_2$ and $R_f$ were selected to deviate from ideal. The resistors for the MSB comparator had an increased value of 20% from the ideal, whereas the LSB comparator resistors had a decreased value of 20% from the ideal.

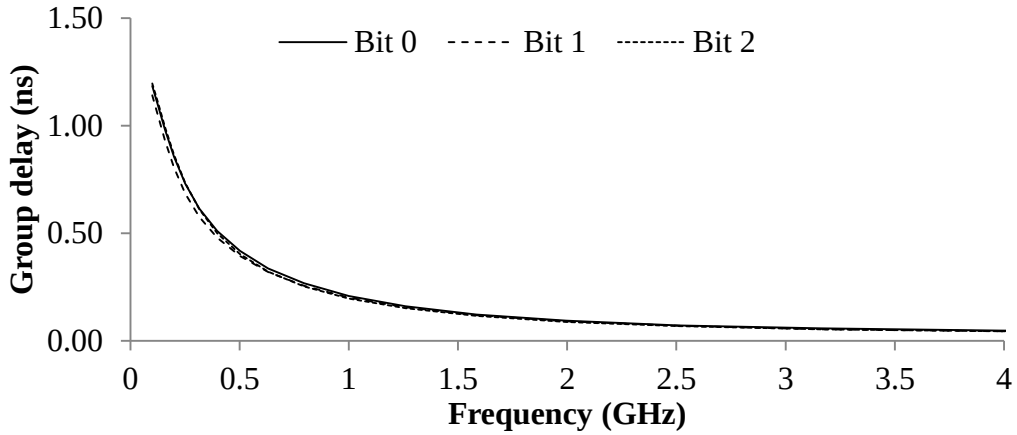


**Figure 4.29.** Group delay simulation for ideal two-bit ADC

The 2nd bit comparator values where unaltered. Figure 4.30 shows the simulated results for variations between each comparator. From Figure 4.30 it is clear that even a small deviation in resistor values will affect the group delay between comparator channels.

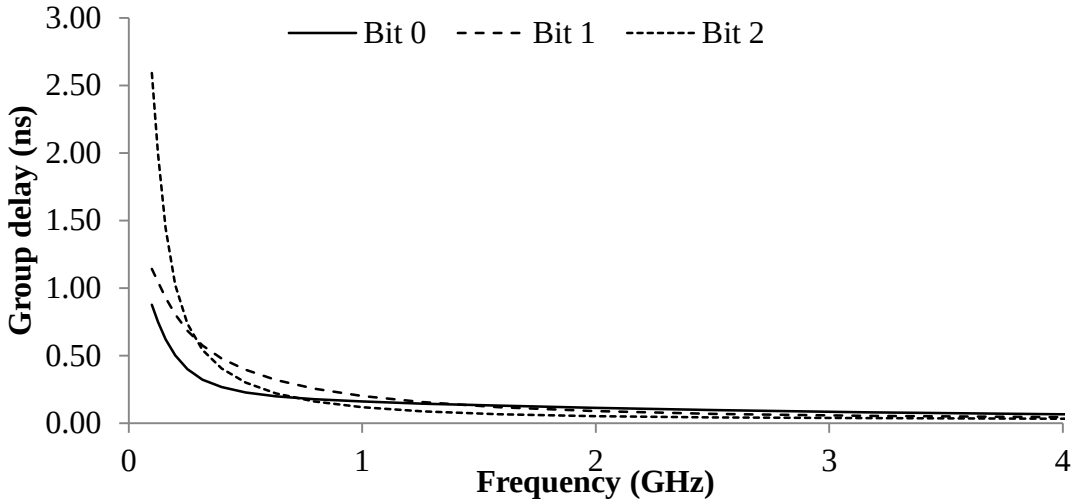


**Figure 4.30.** Simulated group delay for variations in MSB and LSB comparator

## 4.6 CONCLUSION

This chapter detailed the two-bit flash ADC design and simulation for testing the hypothesis. Detailed designs of each subsystem and current sources were provided. Simulation results were provided for input signals up to 5 GHz verifying the design results. The bandwidth of the CC tree was shown to be proficiently high up to 90 GHz. Using the parameters of the 0.13 μm 8HP SiGe BiCMOS technology node results show a wide bandwidth of up to 25 GHz for the C-H amplifier. Time domain results show low rise and fall times for high speed input signals making the comparator configuration adequate for high speed input signals and therefore high input bandwidth. The design using the CC tree and C-H amplifier in combination showed wider bandwidth (up to three times) results for ADC operations, thus supporting the hypothesis. Due to the relatively large voltage overhead required with the C-H architecture, MOSFET devices were not used. MOSFET terminal breakdown voltages are lower than HBT devices and the reliability of these devices would be compromised in the selected technology node.

# CHAPTER 5 LAYOUT, FABRICATION AND MEASUREMENT RESULTS

## 5.1 INTRODUCTION

This section describes the layout steps followed for the design of the prototype to be tested. Two separate circuits were prototyped, a two-bit ADC and a single comparator. Since the prototype chip was part of a multi-project wafer (MPW), it was decided to prototype a smaller bit size ADC since higher bit size ADCs use excessive silicon real estate.

## 5.2 LAYOUT TECHNIQUES

If matching components vary, the differential circuit may become unbalanced and cause erroneous switching, which in turn causes ADC linearity errors. Component variations result from the fabrication process and an ideal component value cannot be guaranteed. Matching HBTs were therefore placed in close proximity and inline in order for the processing gradient to be the same, aiming for an equal variation in HBTs. Variations in the transistors will then be close to equal thereby keeping the symmetry within the differential configuration. The same method was used for the HBTs within the current sources, but since the HBTs in the current sources operated at DC levels, the HBTs were placed closer together when compared to the differential pairs. In areas where there were an uneven number of transistors, dummy transistors were placed in an attempt to keep the gradient equal.

The IBM 8HP run has 5 available metal layers namely M1, M2, MQ, LY and AM with M1 being the lowest level layer and AM the top layer metal. Each metal layer has its own maximum current density and therefore minimum line width. Process variations may cause the line width to be less than the minimum and therefore the line width was increased in order to prevent any wires from failing under stress. A safety margin of 2 mA was used when calculating the minimum line width for each layer. The HBT configuration used was the collector-base-emitter-base-collector (CBEBC) configuration shown in Figure 5.1. Also shown in Figure 5.1 is an example of the metal wires connecting the transistor with

the pattern lines indicating the direction of current flow and solid lines the minimum line width (W) for each wire.

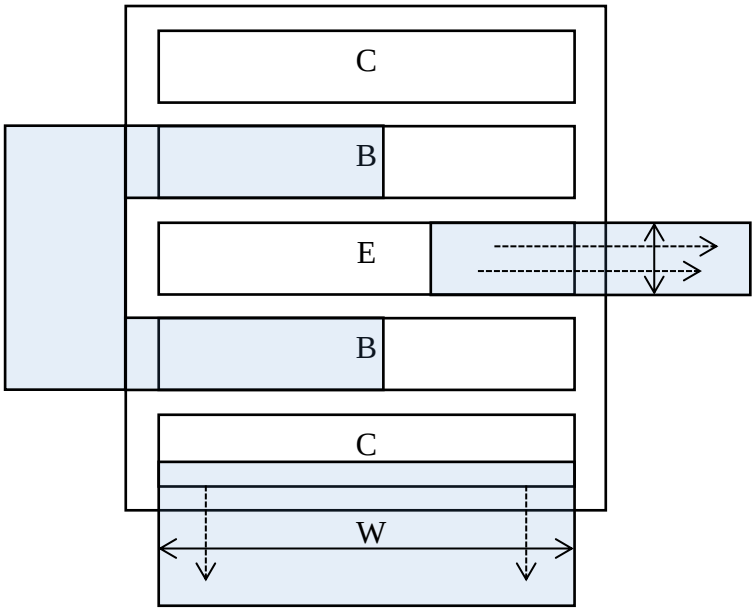


**Figure 5.1.** CBEBC HBT configuration with metals connected to a collector and emitter

In order to realise resistance values as close as possible to designed values, the resistors were split into two smaller values or/and *KQRES* resistors that have smaller tolerance values, were used. A resistor was split up and connected in series with an added dummy resistor as shown in Figure 5.2. A dummy resistor, which is the same value as *R*/2, is added in order to improve the accuracy of the *R*/2 resistance and therefore the total resistance, *R*. Due to process variations the combination of two smaller series resistors with a dummy resistor provides a more accurate total resistance than a single resistor.

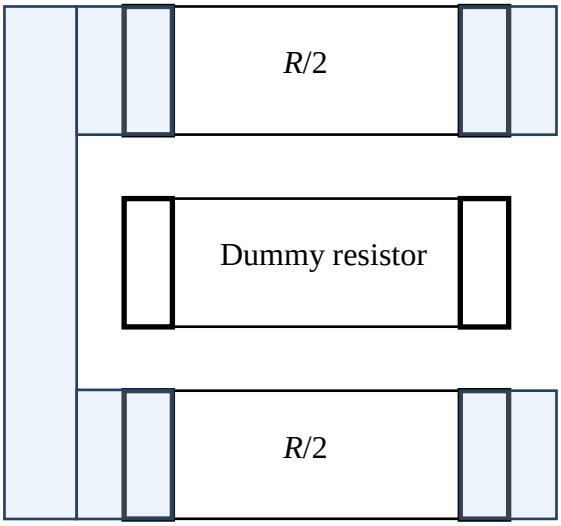


**Figure 5.2.** Resistor placement for better accuracy

Figure 5.2 also shows the metal lines used to connect the *R*/2 resistances with the dummy resistance being left unconnected. The *KQRES* resistor was used in the comparator and voltage reference circuit since it has lower tolerance and parasitic values than the other available resistors in the process. For lengthy interconnects the AM layer was used. This was done as the AM layer has the least resistance and provides transmission lines which have models that can be used in simulation to test the circuit functionality. After DRC and LVS checks were completed, the chip was sent for prototyping.

## 5.3 TWO-BIT ADC

The two-bit ADC layout was developed from the design and simulations in Section 4.5. The layout also made use of the techniques described in Section 5.2. Figure 5.3 shows the comparator core for the ADC.

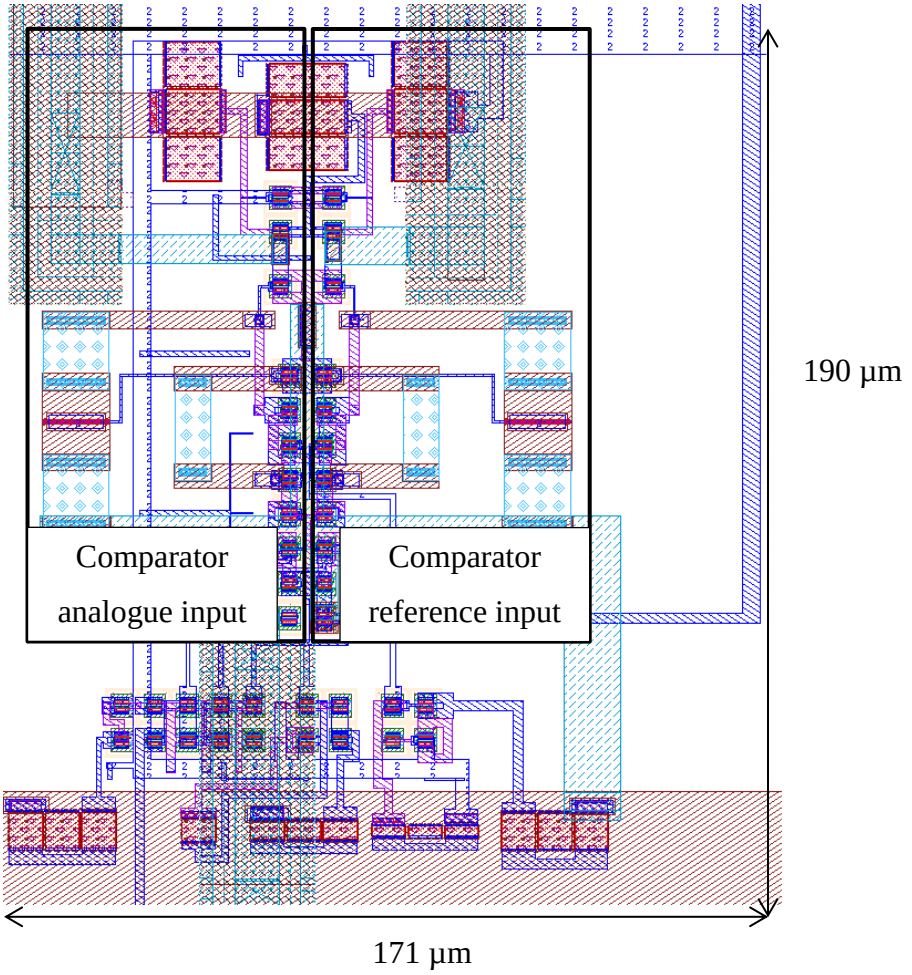


**Figure 5.3.** ADC comparator

It can be seen in Figure 5.3 that the comparator sides mirror each other and this was done to try and achieve symmetry. The *KQRES* resistors can be seen in the middle of Figure 5.3 and were placed further away from each other and the transistors. The specific placement of the *KQRES* resistors was to reduce the effect of the heat that each *KQRES* resistor generates on the rest of the circuit. The two small rows of blocks are the transistors used for the current mirrors. They were placed in close proximity to improve matching and hence distribute the currents evenly for the entire circuit. Large line widths can also be identified for areas where large amounts of current were required to reduce the effect of electron migration.

Figure 5.4 shows the voltage reference circuit for the ADC and shows how the resistors were split up and connected in series for improved matching. Minimum distances were used between resistors and shown in Figure 5.4 are the branches towards the MSB and middle bit voltage reference inputs of the ADC. The relatively small footprint, 52 × 73 µm, of the voltage reference circuit is also shown in Figure 5.4.

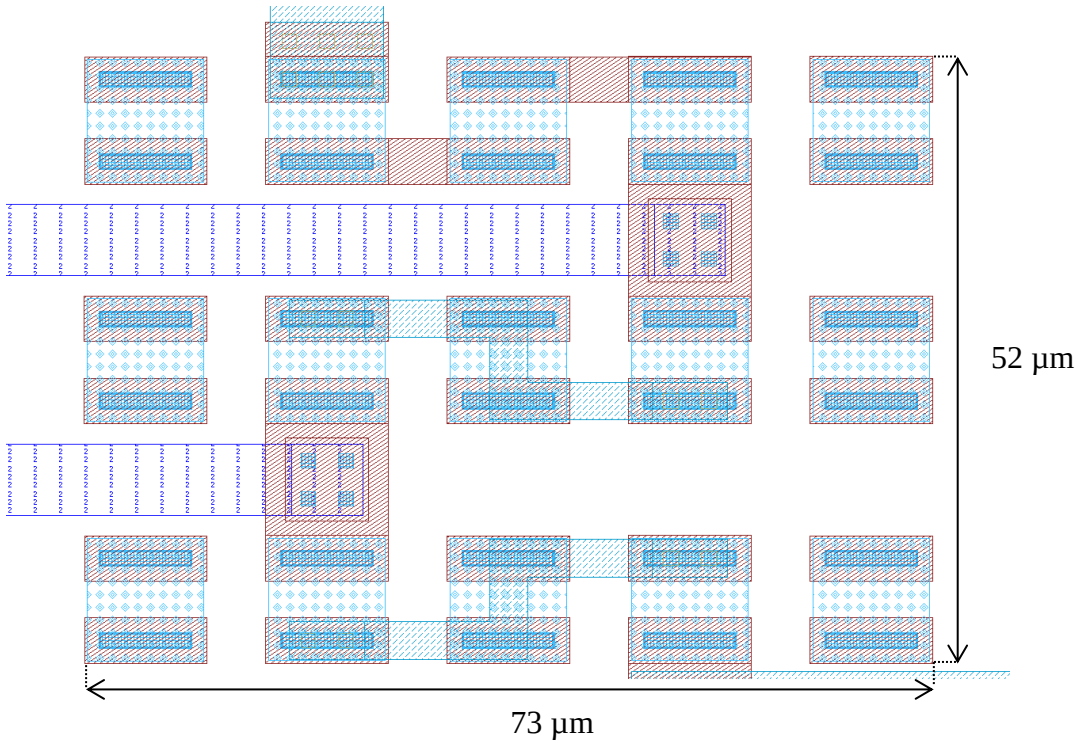


**Figure 5.4.** Voltage resistor reference ladder

Figure 5.5 shows the entire two-bit ADC with transmission lines connecting the bond pads to the inputs and outputs of the circuits.

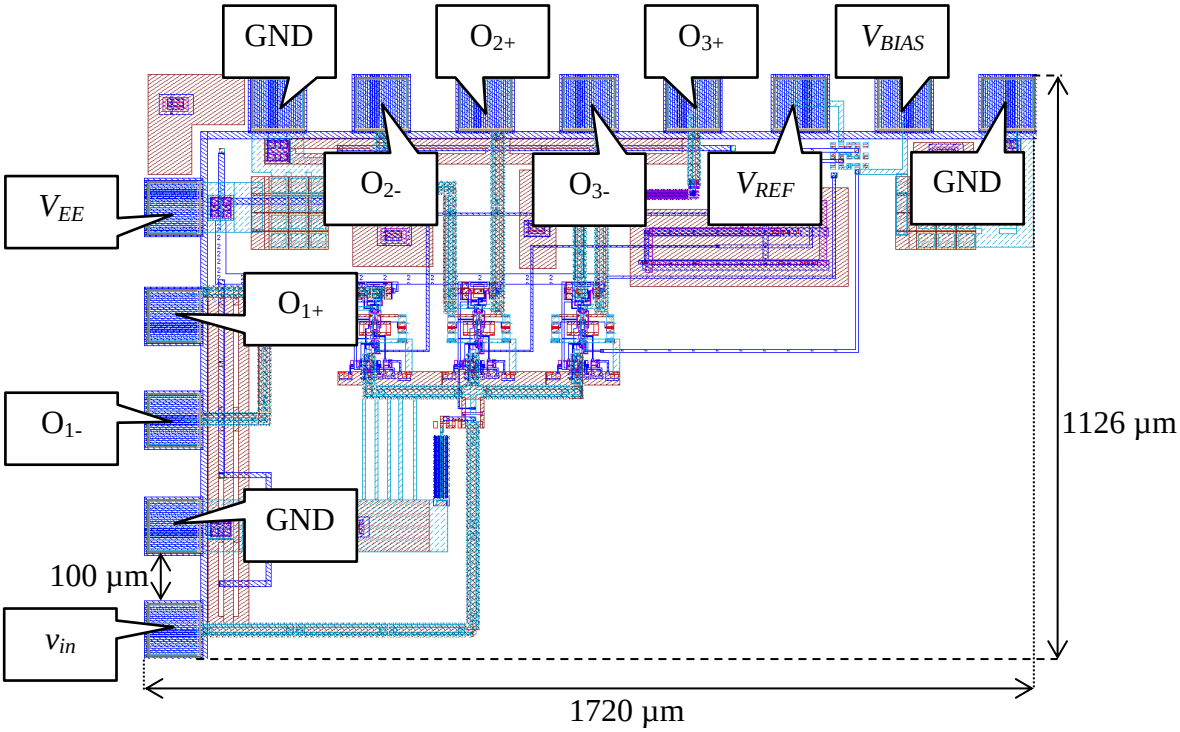


**Figure 5.5.** Full ADC layout

Decoupling capacitors are also located at the top left and top right sections for the supply and reference voltages. The bond pad listing is as follows.

- Three ground pads, GND.
- One voltage supply pad, $V_{EE}$.
- Six output pads designated by $O_{x-}$ and $O_{x+}$ indicating the inverting and non-inverting outputs of each comparator.
- Reference ladder voltage, $V_{REF}$.
- Reference ladder bias resistance, $V_{BIAS}$.

Due to the pad and comparator placement, the transmission line lengths for each output were not identical. The comparator placements were adjusted in order to provide one output transmission line of equal length for all comparators. External bias resistors were needed for the voltage reference in order to measure the LSB voltage and add a large decoupling capacitor to the reference ladder. The three identical parts in the middle of Figure 5.5 are the comparator designs from Figure 5.3. The full ADC layout footprint size of approximately 1126 × 1720 µm and a pad separation distance of 100 µm are shown in Figure 5.5. The large placement between pads was selected to reduce crosstalk between

lines and provide enough space for the wire bonds used to connect the chip to the measurement PCB. The voltage reference circuit of Figure 5.4 can be seen just below the $V_{REF}$ pad of Figure 5.5.

## 5.4 SINGLE COMPARATOR

Figure 5.6 shows the full circuit diagram for the single comparator. For the single comparator both inputs are connected to bond pads in order to measure the outputs for known inputs at both ends. One current source is also connected to a bond pad in order to adjust the current in the comparator to measure the effect on the response of the comparator. The same transistor placement was used for the single comparator when compared to the comparators in the two-bit ADC. Wide lines were also used for the high current parts of the single comparator.

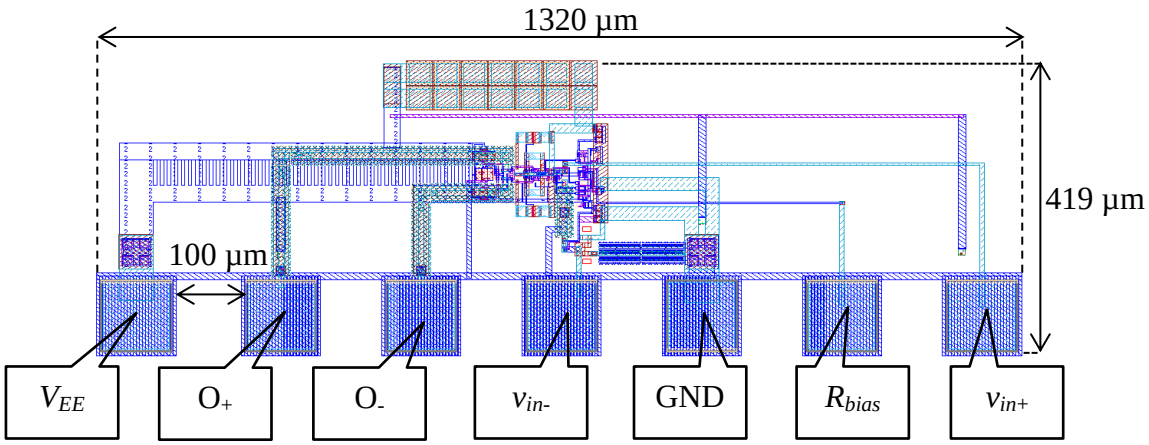


**Figure 5.6.** Single comparator layout

The bond pad listing for the single comparator is as follows:

- A single voltage supply pad, $V_{EE}$.
- Two pads for the differential outputs, $O_+$ and $O_-$.
- Two pads for each input, $v_{in+}$ and $v_{in-}$.
- A single ground pad, GND.
- A pad to connect a bias resistor to adjust the bias current of the outer core of the comparator, $R_{bias}$.

A short line distance was used for the single comparator with the pad placement very close to the input of the CC tree. This was done in order to reduce the amount of inductance at the input which would reduce the bandwidth of the system.

## 5.5 MEASUREMENT RESULTS

The measurement setup described in Section 3.6 was used to measure the two-bit ADC. Three test circuits were designed for measurements. One circuit was used for static testing and two circuits were used for AC tests. For the static test circuit, coupling capacitors were excluded from the input and output channels. The coupling capacitors were removed as the DC voltages will not be measurable if coupling capacitors are present. For the AC measurement PCBs, coupling capacitors and bias tees were used in order to properly measure the ADC characteristics. The coupling capacitors were added to prevent the oscilloscope impedance from affecting the biasing of the output stages. Bias tees were used at the input to add an offset voltage to the input signal and capacitively couple the input signal to the ADC. The bandwidth of the bias tee was 10 MHz to 20 GHz. The HMC760LC4B wideband DC-4 GS/s S/H amplifier from Hittite was used to create a clocked ADC and the clocked outputs were also measured [40]. For all tests the input sinusoid waves were between 90% and 100% of the full scale range as specified in [11].

### 5.5.1 Two-bit ADC

All possible ADC output codes and corresponding voltage levels (in terms of LSB) are shown in Table 5.1 for an ideal two-bit ADC.

**Table 5.1.** ADC output code words

| Code word | Voltage level |
|---|---|
| 000 | 0 |
| 001 | 0.5 LSB |
| 011 | 1.5 LSB |
| 111 | 2.5 LSB |

This was used for the data processing of the ADC output records. Since the comparators are not all identical, erroneous output codes may occur. The data processed within Matlab used error correction and counted each erroneous result to get a bit error rate (BER) for a specific sample set of measured data. Table 5.2 shows the error correcting scheme used within Matlab. For this correcting scheme the MSB is used to determine the output code and it is assumed that the other bits have not settled at the specific time when the measurement was made.

**Table 5.2.** Error correction for ADC outputs

| Erroneous code word | Corrected code word |
|---|---|
| 010 | 011 |
| 100 | 111 |
| 101 | 111 |
| 110 | 111 |

#### 5.5.1.1 Static test

Figure 5.7 and Figure 5.8 show the DNL and INL of the measured ADC, respectively. The INL and DNL errors were computed using (2.5) and (2.6) after the code transition levels were measured.

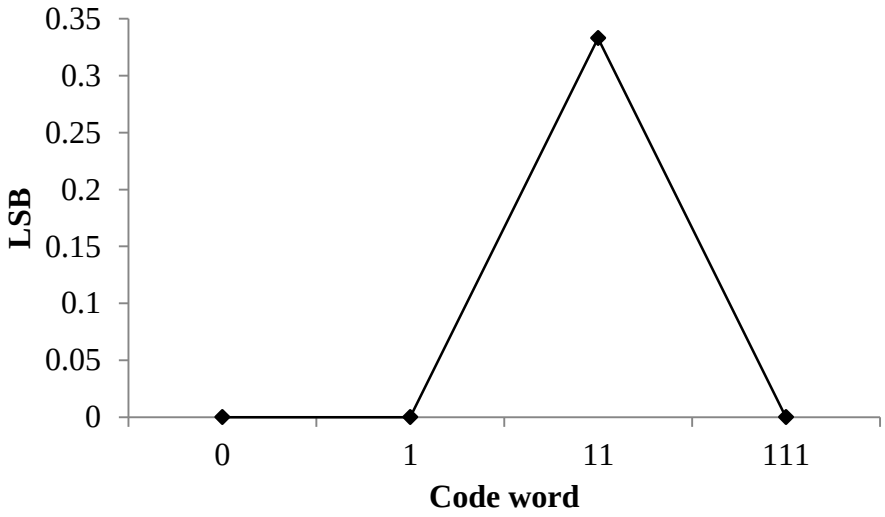


**Figure 5.7.** Measured DNL of the two-bit ADC

A ramp signal of 1 MHz was used for a slow varying test signal in order to measure the transition levels of the ADC. Since all the outputs can at the same time be measured with the MSO5104, a manual test was also performed. A power supply was connected to the

ADC input and adjusted until the ADC outputs started to 'jump' between adjacent output code words. The voltage was then recorded as the transition level for a specific code word. This process was repeated for all output code words. Both methods produced the same results for the INL and DNL of the system.

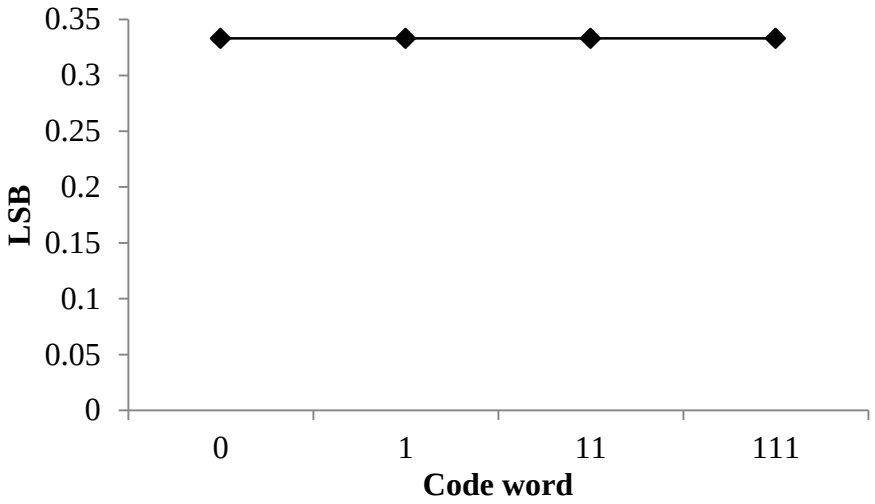


**Figure 5.8.** Measured INL of the two-bit ADC

#### 5.5.1.2 Dynamic tests

In order to determine the ENOB, SFDR, SINAD and FOM, various data records were taken at different frequencies. Best fit sine-wave curve fitting was performed as described in [11]. Using the best fit sine-wave data the SINAD was calculated and the corresponding ENOB was determined using (2.7). Figure 5.9 shows the measured ENOB for a set of test frequencies. An S/H circuit was used as depicted in Figure 3.2. Sampling rates of 250 MS/s and 1 GS/s were used in order to sample above the Nyquist rate for the various input frequencies. The input test frequency range was limited to 500 MHz as the measurement equipment was band limited to 500 MHz.

Figure 5.10 shows the measured ENOB for the ADC without an S/H circuit. An analogue oscilloscope with high bandwidth was used to measure the ADC outputs. The analogue outputs were then analysed in Matlab and converted into digital data with the same threshold value used in the digital oscilloscope. The digital data was then used to compute the ENOB. Both Figure 5.9 and Figure 5.10 show an ENOB value close to 1. This result

stems from the error correction scheme utilised and the static errors for the ADC. Since the second to last code word of the ADC has a large error, its transition value is closer to the final code word.

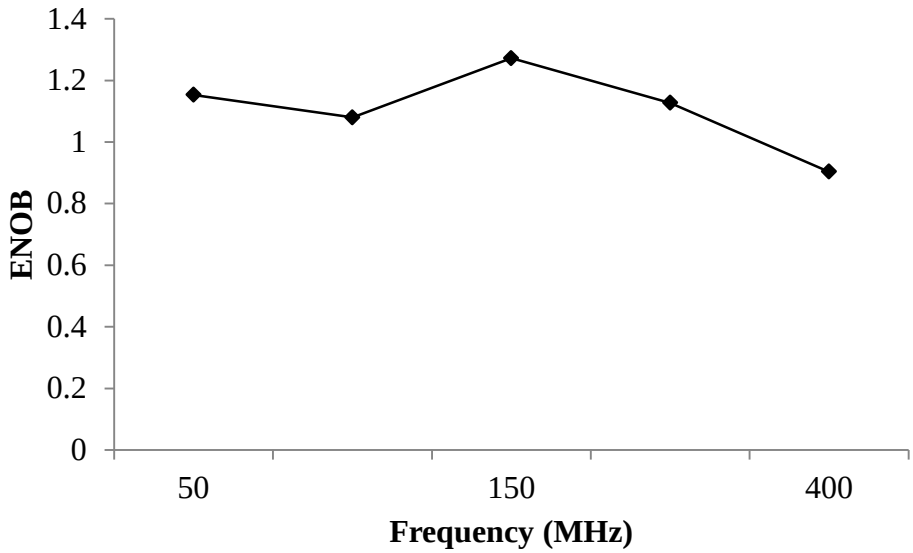


**Figure 5.9**. ENOB with S/H circuit sampling

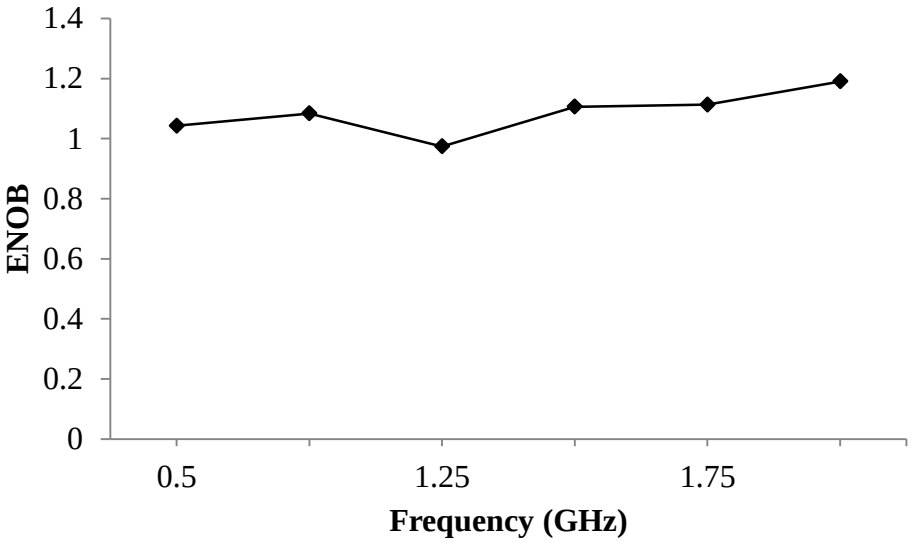


**Figure 5.10**. ENOB of free running ADC

The second to last and last code word therefore switch closely together and the effective number of transition levels decrease by 1. Figure 5.11 shows the BER for the ADC at the different frequencies at which the ENOB was calculated. Even though the ENOB is close to 1, the BER shows that the ADC outputs often switch to invalid output words as the input frequency increases. Viewing the output signals in the time domain reveals some of the dynamic error sources for the prototype ADC. Figure 5.12 shows a time domain

measurement of the ADC outputs for an input sinusoid frequency of 1.75 GHz. As can be seen in Figure 5.12 the outputs switch at different times indicating different group delays through each comparator. The output code words are therefore invalid at specific time intervals. This delay between all the outputs causes an increase in the BER and reduces the ENOB.

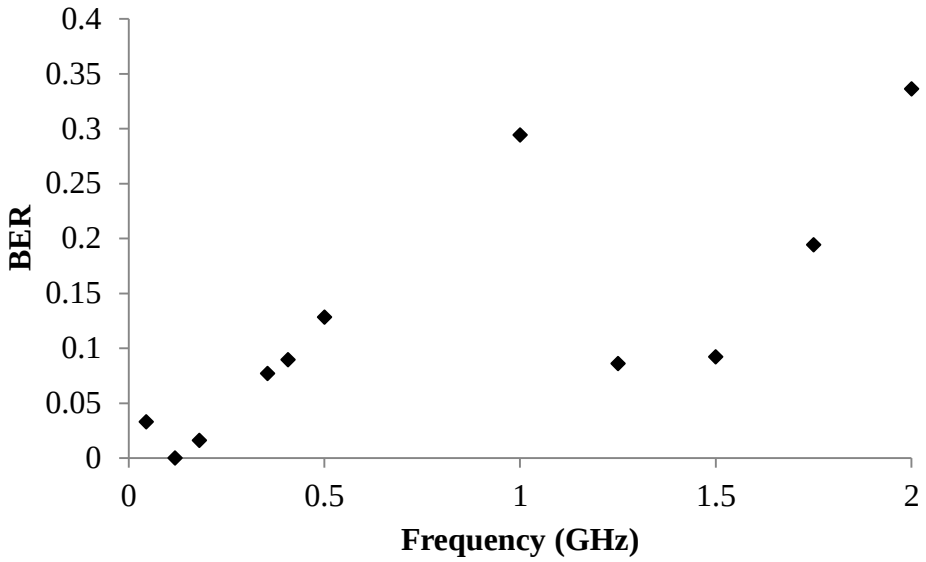


**Figure 5.11.** BER for ADC outputs

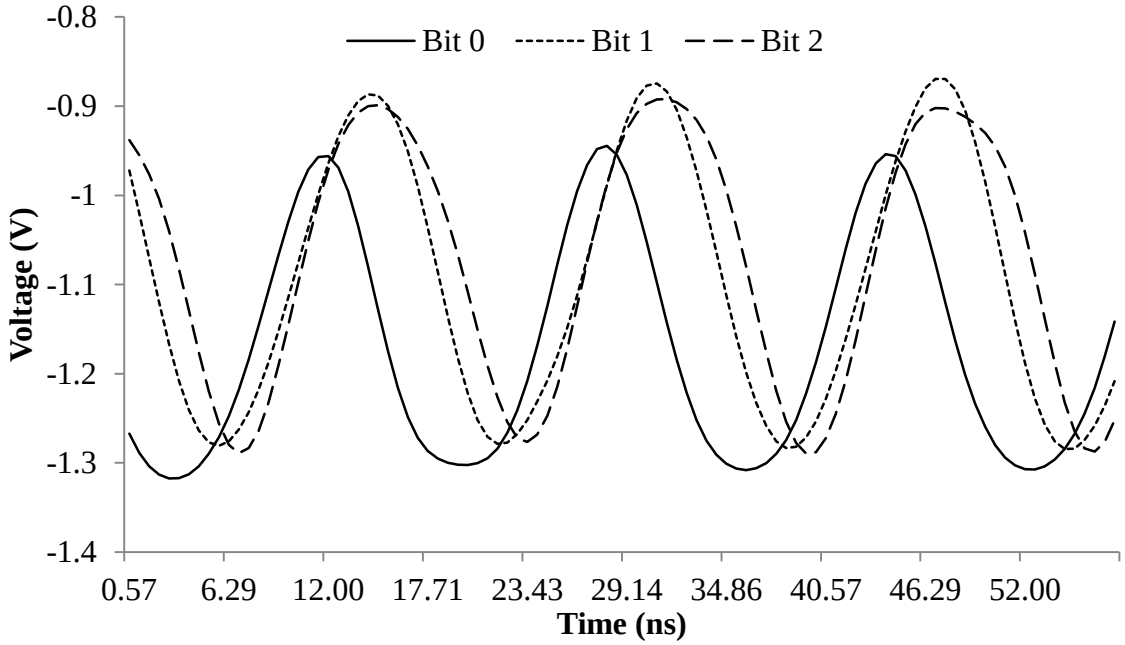


**Figure 5.12.** ADC outputs for an input sinusoid frequency of 1.75 GHz

In Figure 5.13 the ADC outputs from Figure 5.12 where manually scaled in time, by a small amount, to indicate the switching ratio between each output. Comparing Figure 4.23 with Figure 5.13 a resemblance can be seen in the switching performance of the ADC, with

the LSB comparator switching before the other outputs. The INL and DNL errors can also be seen on the edges of the outputs in Figure 5.13. It is clear that the group delays in each comparator reduces the performance of the ADC even further.

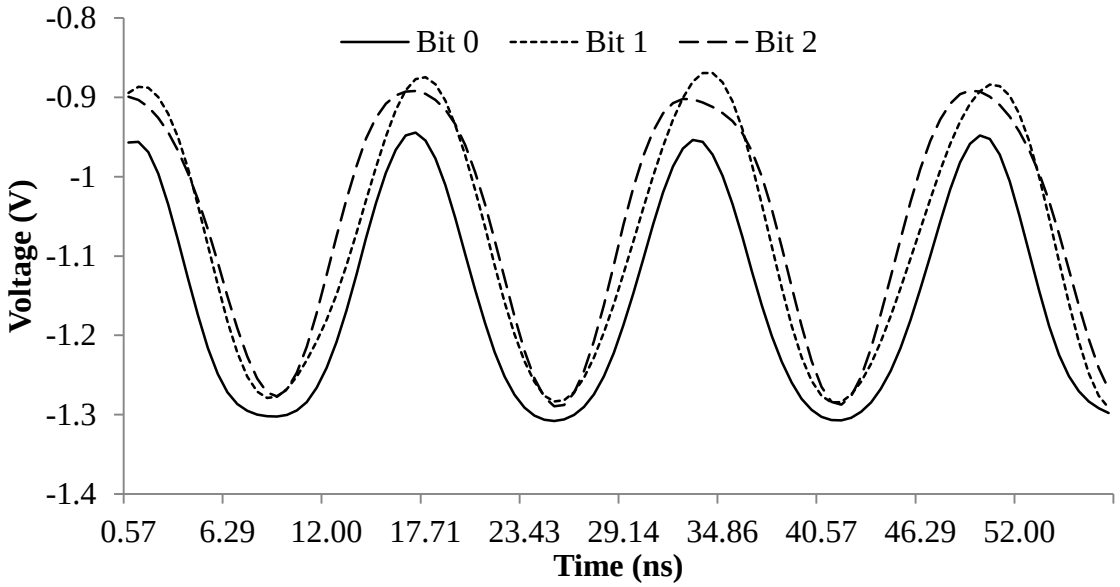


**Figure 5.13.** Adjusted ADC outputs for an input sinusoid frequency of 1.75 GHz

Frequency domain results provide useful information regarding the spectral content of the ADC output signals and can be used to determine the SINAD, SFDR and thereby the resulting ENOB. In order to reduce the amount of spectral leakage in the FFT outputs, coherent sampling was required. The ratio to perform coherent sampling is given as follows,

$$f_i = \frac{J}{M} f_s, \tag{5.1}$$

with $f_i$ the input frequency, $f_s$ the sampling frequency, $J$ an integer relatively prime to $M$ and with $M$ the record length [11]. A record length is a sequential set of samples acquired by an ADC. For a recommended set of chosen values for $M$ and $J$ to be relatively prime, at a specific input frequency, $M$ should be a power of 2 and $J$ must be an odd integer [11].

Figure 5.14 shows a Blackman windowed FFT result for a 45 MHz input sinusoid wave signal at a sampling rate of 1024 MS/s. $J$ and $M$ were selected to be 45 and $2^{10}$ respectively. The sampling clock was connected to the S/H amplifier from Hittite and measured while records were taken. From Figure 5.14 the SFDR is 8.285 dB and the DC offset is clearly visible. Figure 5.15 shows the FFT output for a 2 GHz input sinusoid signal. A Blackman window was also used when the FFT was performed on the output

data. From Figure 5.15 the SFDR reduced to 6.23 dB and more harmonic components are present in the output showing a reduced ADC performance.

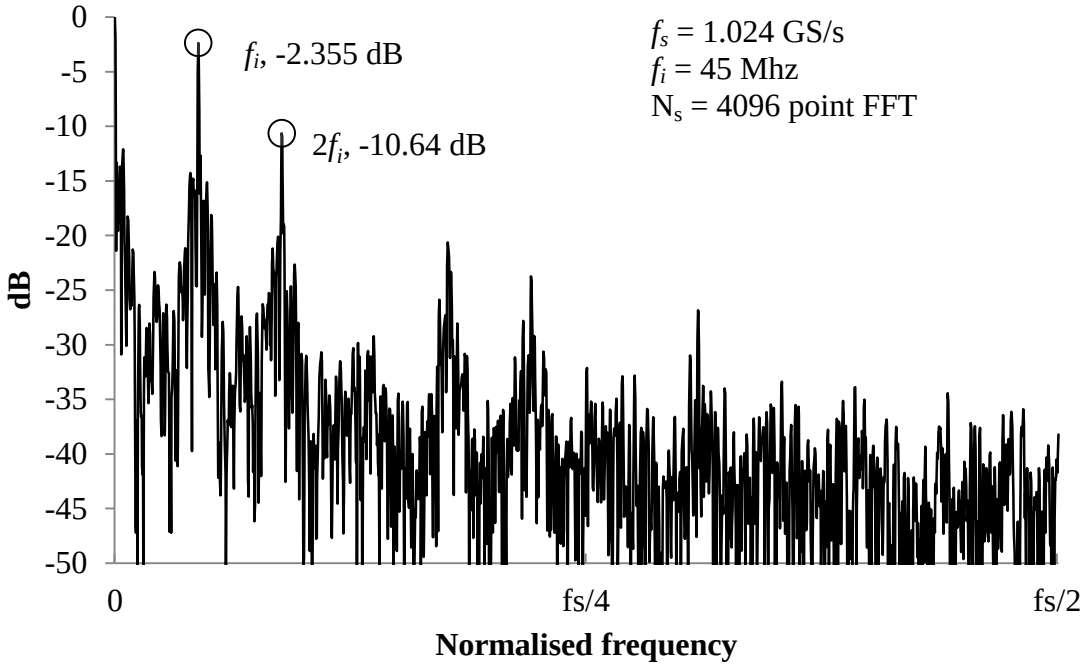


**Figure 5.14.** FFT of 45 MHz input signal

At an operating frequency of 2 GHz the output signal amplitudes reached the -3dB bandwidth level and diminished at higher frequencies. The ERBW was therefore DC - 2 GHz.

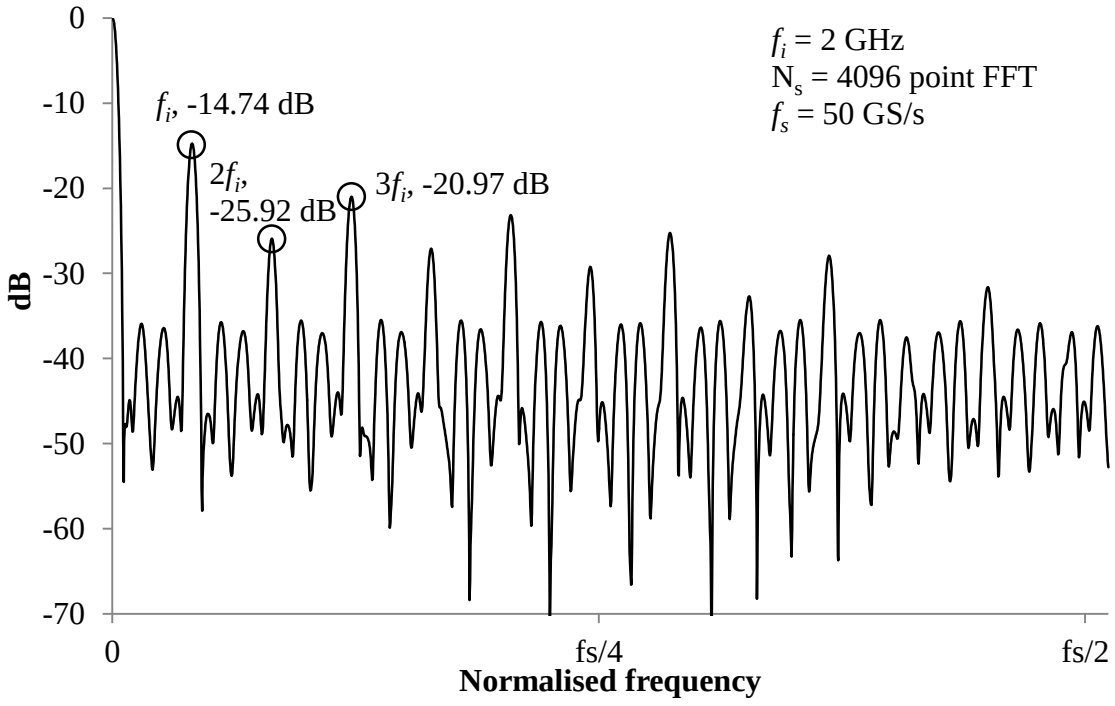


**Figure 5.15.** FFT of 2 GHz input signal

### 5.5.2 C-H amplifier as a comparator

Table 5.3 provides a summary of various high performance comparators in relation to the current C-H design, with an added input tree. The CMOS comparator in [41] trumps the comparator in this work with all the specifications except bandwidth. The comparator presented in [42] shows better power consumption and gain, but occupies a larger chip area and has a reduced bandwidth. The comparators in [43] and [44] have improved gain performance and a smaller active area than the current C-H design, but has a smaller bandwidth and output swing. In order to achieve a similar output swing while maintaining a constant gain, adjustments must be made to $R_1$, $R_2$, $R_f$ and $I_{CORE}$. From (4.8) and (4.16) reducing $R_1$, $R_2$ and $I_{CORE}$ reduces the gain of the circuit. $R_f$ must hence be increased to maintain a constant gain, which in turn reduces the bandwidth of the comparator. This effect was simulated and presented in Table 5.3, clearly indicating a decreased bandwidth and power consumption.

**Table 5.3.** C-H comparator comparison to state of the art comparators

| | [41] | [42] | [43] | [44] | This work | This work[1] |
|---|---|---|---|---|---|---|
| Technology | 0.5 µm CMOS | 0.13 µm SiGe | 0.18 µm SiGe | 200 GHz SiGe | 0.13 µm SiGe | 0.13 µm SiGe |
| Supply | 5 | -3.3 V | 3.3 V | 3.5 V | -3.3 V | -3.3 V |
| Power consumption | 5.65 µW | 48 mW | 28 mW | 405 mW | 87 mW | 78 mW |
| Gain | 29.54 dB | 42 dB | 40 dB | 11 dB | 5.6 dB | 5.84 dB |
| Bandwidth | 33 MHz | 3.3 GHz | 22 GHz | 18 GHz | 29 GHz[1] | 12.6 GHz |
| Input offset | 50.57 µV | +/- 5 mV | N/A | < 16.7 mV | 17 mV | N/A |
| Output swing | 5 V | 100 mV | ~ 10 mV | ~ 40 mV | 400 mV | 100 mV |
| Active area ($mm^2$) | 0.064 | 1.9 | 0.0053 | 0.0226 | 0.027 | N/A |

1. Simulated values.

It must be noted that the comparators in Table 5.3 are latched comparators and the current C-H design does not include clocking circuitry. Including clocking circuity will increase power consumption and the active area occupied by the C-H comparator.

### 5.5.3 Measurement board results

In order to determine the effect of the measurement PCB parasitics, time domain reflectometry (TDR) measurements were performed on the measurement PCB. The Tektronix 80E04 TDR sampling module was use with the Tektronix DSA8300 sampling oscilloscope in order to perform TDR measurements. Both have analogue bandwidth support up to 20 GHz. Figure 5.16 shows the connection between the TDR module and the measurement PCB.

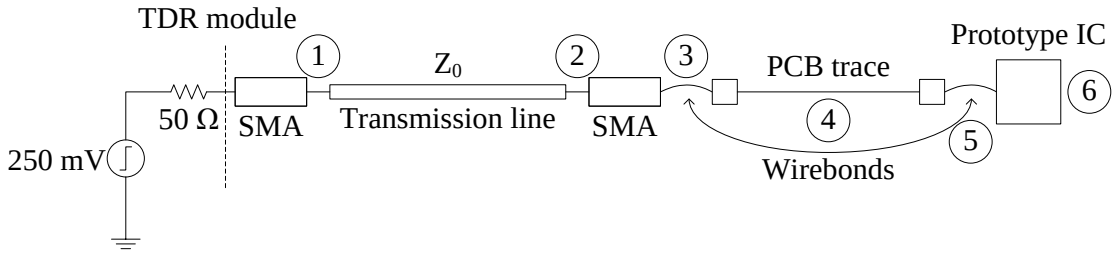


**Figure 5.16.** TDR module setup

As indicated in Figure 5.16 the TDR module uses a 250 mV step wave in order to measure the reflections in the DUT. As the step voltage travels along the test line a reflection occurs at each discontinuity. The reflected wave is compared to the incident 250 mV signal and a reflection coefficient (ρ) is calculated at the source. The discontinuities in Figure 5.16 are illustrated as impedances in Figure 5.17. Each impedance ($Z_x$) reflects a part of the signal and is convoluted with any discontinuities back to the source.

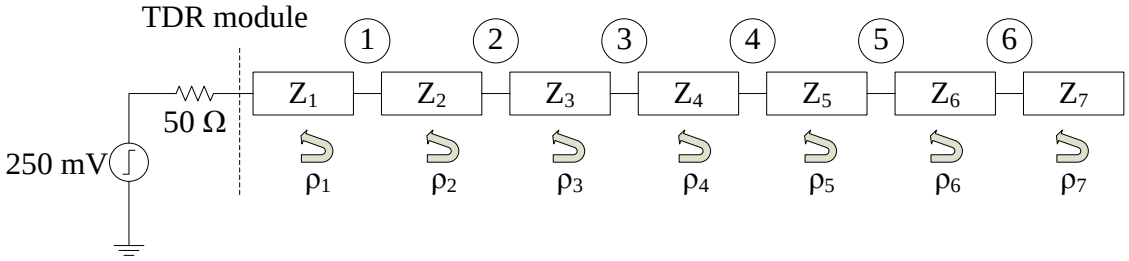


**Figure 5.17.** TDR reflections

Figure 5.18 shows the measured TDR response for the ADC input. $Z_1$ shows the discontinuity observed from the 8.5” SMA cable used to connect the DUT to the TDR module. $Z_2$ is the transmission line impedance of the SMA cable and has almost zero reflection since it is closely matched to 50 Ω. $Z_3$ has a similar response as $Z_1$ and indicates the discontinuity reflected from the SMA connector on the measurement board. $Z_4$ to $Z_6$ are due to the wire bond and PCB trace connections to the prototype ADC. $Z_7$ is the final reflection coefficient resulting from the input termination of the prototype ADC. From

Figure 5.18 the reflection coefficient is close to 0.08 which indicates an input impedance close to 60 Ω.

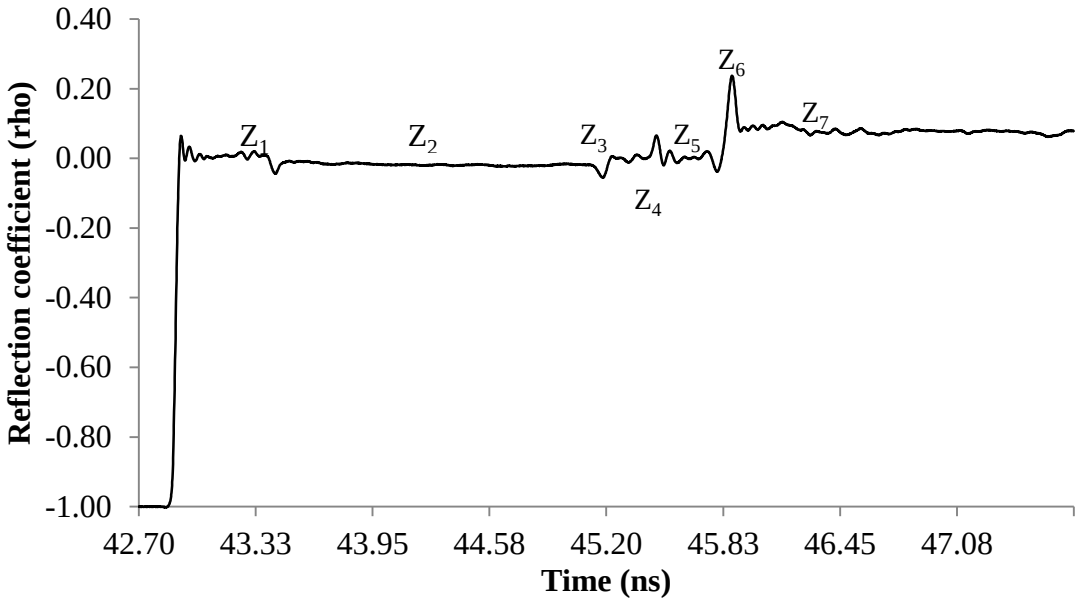


**Figure 5.18.** Input TDR result

Figure 5.19 shows the TDR results for each ADC output for the AC coupled measurement PCB.

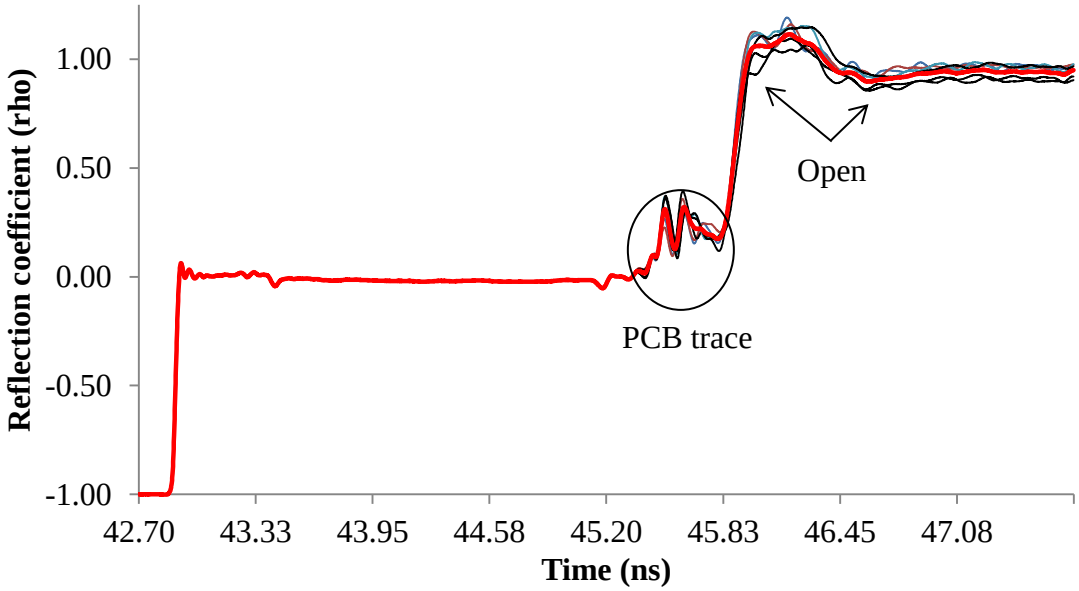


**Figure 5.19.** TDR output result

The impedance connection is the same as for the ADC input except for $Z_4$. $Z_4$ is split up into a wire bond and 100 pF series capacitor for the AC coupled measurement PCB. This was done in order to properly match the ADC outputs to 50 Ω terminations. The ADC was switched off when the TDR measurement was made; hence $Z_7$ would be seen as an open

circuit. As would be expected in Figure 5.19, the reflected response for the TDR module and SMA cable are the same for all measurements. The expected PCB trace measurement should indicate a series of inductor-capacitor-inductor responses. This results from the wire bond connection to the series capacitor. The capacitor is connected to the PCB trace and wire bonded to the prototype ADC. For an inductive discontinuity the TDR response is a peak reflected wave. For a capacitive discontinuity the TDR response is a reduced reflected wave. This result is evident from Figure 5.19 where the PCB trace is indicated. Parasitic inductance and capacitance on the PCB reduces the measured performance of the ADC. The added inductance at the input and output terminals reduces the available ADC bandwidth. The added parasitics also reduce the input and output load match to 50 Ω. This results in a voltage standing wave ratio (VSWR) higher than 1:1. Using inductor values of 1 nH per 1 mm of bond wire length, and estimating a bond wire length of 1 mm per bond wire, the ADC performance was resimulated. The VSWR result is shown in Figure 5.20.

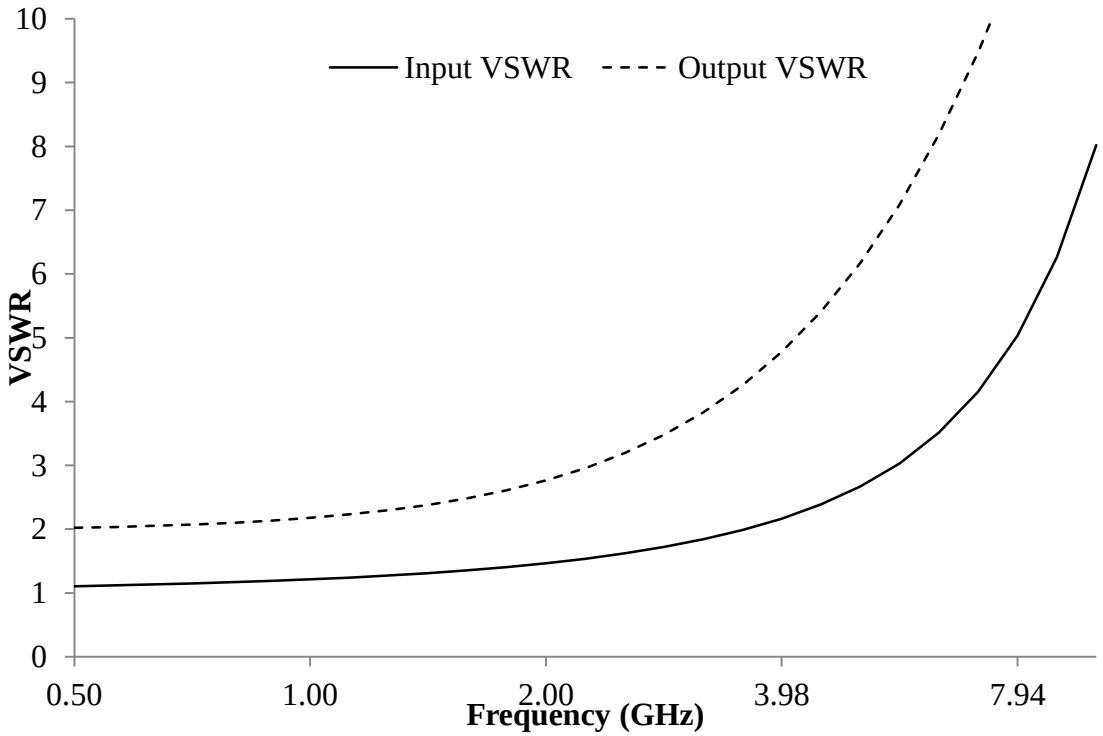


**Figure 5.20.** Simulated VSWR

From the VSWR result it is clear that the power transfer from the ADC to the measuring equipment degrades drastically from 2 GHz and higher. At a frequency of 2 GHz the VSWR ratio for the output is 1:2.76. The input match is better over the frequency range with a VSWR ratio of 1:1.4 at 2 GHz. In Figure 5.21 AC simulation results are shown for the case where the wire bond inductance was taken into account. At low frequencies both results show the same gain. The -3 dB cut-off value for the wire bond simulation is close to

7 GHz. This shows a reduction of 4 times in the bandwidth due to the addition of wire bond inductance. Including the PCB trace inductance will degrade performance results even further.

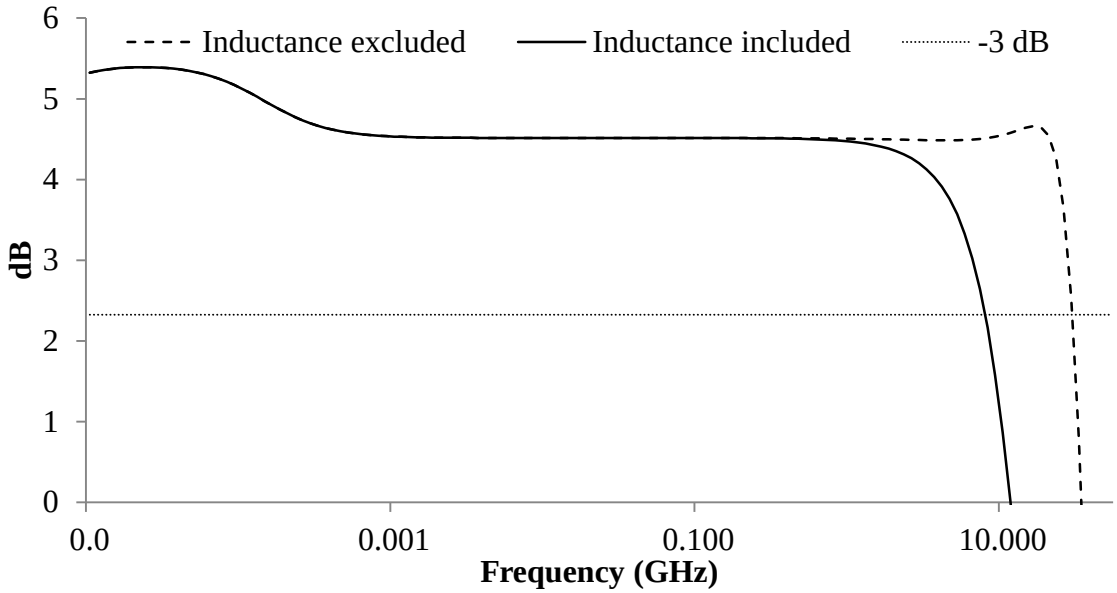


**Figure 5.21.** AC simulation results with included inductance

## 5.6 CONCLUSION

This chapter presented the layout of the prototype ADC and the comparator used to test the hypothesis. Measurement results were also presented showing static and dynamic ADC performance. Various layout techniques were given to successfully implement the design for proper measurements. Larger line widths can easily be seen in the final layouts of the two-bit ADC as well as the single comparator to reduce the effect of electromigration. Resistor placement for improved matching can easily be identified for the reference voltage generation. Transistor connections were not shown explicitly since they differ depending on their placement, but adhere to the electromigration rules. In the final chip design fill patterns were added to some parts of the design in order to comply with the pattern density rules required by the fabrication facility. Measurement results show an ENOB close to 1.1 for input frequencies up to 2 GHz. Group delays between comparators increase the BER and reduce the ENOB for the prototype ADC. This is due to variations between each comparator stage and output leads to the test equipment.

# CHAPTER 6 CONCLUSION

## 6.1 INTRODUCTION

The research was aimed at improving the available input bandwidth of a high speed ADC. Chapter 2 provided the literature study as a foundation for the hypothesis. Chapter 3 discussed the methodology used throughout the research to validate the hypothesis. Chapters 4 and 5 presented the simulation and measurement results used to evaluate the hypothesis and draw a conclusion from the results. This final chapter describes the conclusion of the work as well as possible future work.

## 6.2 CRITICAL EVALUATION OF THE HYPOTHESIS

The improvement of flash ADC input bandwidth was proved using the methods and results provided in Chapters 3, 4 and 5. Various methods have been investigated in order to improve ADC input bandwidth [45, 46, 47], but to the author's knowledge the combination of CC input trees with the C-H converter is novel. The proposed ADC does have its strengths and weaknesses. These are provided in the following list.

- Even though the proposed ADC has a wide bandwidth it has a relatively low gain. This causes a slow slew rate and therefore requires a large difference in input voltages before the outputs are fully switched.
- The CC input tree successfully improves the bandwidth of the system, but increases the power consumption. This is the result of the bias currents needed for the input circuit as well as the increased supply voltage due to the $V_{BE}$ increases from the input to the comparator. The additional components also increase the footprint size of the ADC.
- The C-H amplifier requires a relatively high voltage supply and in conjunction with the common collector input tree increased the minimum power supply voltage to 3.3 V. This is a high voltage supply for the 0.13 µm IBM 8HP process and MOS field effect transistors (MOSFETs) cannot be used within the design.
- The breakdown voltages for the HBTs are low and to prevent transistor breakdown, diode connected transistors were used in the input tree as well as the comparator.

These additional devices add to the parasitic capacitances of the circuit and slightly reduce the overall performance.

- The C-H amplifier configuration successfully switched between (10/90%) logic states for input signals of up to 5 GHz in simulation. In measurements the -3dB bandwidth was measured at 2 GHz before the outputs diminished. The reduced bandwidth is caused by the added parasitic components of the measurement PCBs.

Table 6.1 compares high speed ADC measurement results from literature with this work. The FOM for this work is higher than the other high speed ADCs. This is due to the increased voltage headroom required by this design, the low ENOB as well as the limited bandwidth of the system.

**Table 6.1.** Comparison of state of the art flash ADC measurements

| | This work | [48] | [49] | [50] |
|---|---|---|---|---|
| **Technology** | SiGe | SiGe | SiGe | CMOS 65 nm |
| **ERBW** | 2 GHz | 20 GHz | 7 GHz | 7 GHz |
| **Bits** | 2 | 6 | 5 | 6 |
| **ENOB @ ERBW** | 1.18 | 3.7 | 4.5 | 5 |
| **FOM** | 39 pJ/sample | 3.9 pJ/sample | 9.54 pJ/sample | 259 fJ/sample |

## 6.3 LIMITATIONS AND ASSUMPTIONS

No sampling was incorporated in the formulation of the hypothesis. Sampling is usually used in an ADC and can be seen as a necessity. Flip-flops and THA circuits can be used to hold the input value constant and provide sampling intervals for an ADC. The comparator design can also be modified to incorporate sampling within the design itself. Both methods are viable sampling tools, but may suffer from jitter and affect ADC performance, which could provide inaccurate results when evaluating the hypothesis.

The hypothesis was focused on improving the available input bandwidth of an ADC with the use of the C-H amplifier as comparator. Sampling methods were therefore excluded from the design phase.

## 6.4 FUTURE WORK AND IMPROVEMENTS

The following list details possible future work and improvements.

- To improve the switching rate, inductive peaking can be used and the best area for placement within the comparator design can be investigated. An additional gain stage can also be utilised to improve the output switch rate, but may reduce circuit performance.
- To improve measurement and testing methods, a DAC can be implemented on chip thereby reducing the number of bond pads and wire bonds used to test the system. This can potentially reduce the amount of inductance and capacitance present at the outputs, providing more accurate results. In addition, wideband input and output matching networks can be implemented for improved measurement results. Grey coding can also be implemented in order to reduce the number of data lines required to test the ADC as well as the number of output pads required.
- Clocking and jitter performance can be investigated in order to determine the effect it will have on the current CC tree and C-H design. This can possibly be accomplished by removing the diode connected transistors and replacing them with clocked transistors thus making use of the real estate area they occupy.
- A higher bit number is more useful in design applications since it reduces the quantisation error and hence improves the SNR of the system. A stand-alone two-bit flash ADC therefore might not be very useful.
- In applications where only a one- or two-bit quantiser is required, such as in $\Sigma$-$\Delta$ ADCs, the appropriateness of this design can be investigated.
- Recent improvements in SiGe technologies have shown improvements on pnp devices [51]. At higher currents the pnp structures show better gain performance and linearity characteristics than their npn counterpart. By utilizing these pnp devices within the ADC design the gain can be improved while maintaining high speed performance.
- The group delay through each comparator reduced the ENOB of the system at high frequencies. Methods to maintain equal group delays through each channel can be investigated in order to improve the ENOB at higher operating frequencies. Providing high input and output bandwidth impedance matching techniques might improve the measured ENOB as well.

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