Electrical characterisation of silicides and process induced defects in silicon

By

Helga Tariro Danga

Submitted in partial fulfilment of the requirements for the degree

Magister Scientiae (Physics)

in the Faculty of Natural and Agricultural Science

Department of Physics

University of Pretoria

Pretoria

Supervisor: Dr. M. Diale

Co-supervisor: Prof F.D. Auret

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Metal deposition on Si has effects that may be detrimental to device operation such as diffusion, Fermi level pinning and silicide formation. Silicide formation is dependent on type of metal and temperature at which particular silicide is formed. Different defects have been observed during metallisation of Si to form electrical contact. The electrical characterisation of platinum silicides and palladium silicides were investigated using current-voltage and capacitance voltage measurements. Defects introduced were characterised by deep level transient spectroscopy (DLTS) and Laplace DLTS (L-DLTS) while silicidation process was monitored by Rutherford backscattering spectroscopy (RBS). The Rutherford utilities manipulation program (RUMP) and Genplot program were used to analyse the data from RBS.

The electron beam deposition process was used to fabricate Pt Schottky contacts onto n-Si (111). Subsequently these contacts were annealed at temperatures varying from 50°C to 600°C for ten minutes at each temperature. The forward *I-V* characteristics show that the diodes were stable at lower voltages and suffer series resistance effects at voltages higher than 0.5 V. The reverse *I-V* curves shows increasing leakage current with increasing annealing temperature. At lower annealing temperatures, the reverse leakage current is constant at about 10^{-9} A. The ideality factor increased from 1.02 to 2.61 while the barrier height decreased from 0.80 to 0.70 eV as the annealing temperature increased. DLTS revealed that electron beam deposition introduced defects which were identified as the E-centre (VP centre), the A-centre (VO centre),

the interstitial carbon (C_i) and the interstitial carbon-substitutional carbon (C_iC_s) pair. Isochronal annealing at 10 minutes intervals revealed that the E-centre vanishes between 125 and 175°C annealing while the concentration of the A-centre increased in this range. The A-centre annealed out above 350°C and after 400°C, all the electron beam induced defects were all removed.

Palladium Schottky contacts were fabricated on epitaxially grown n-Si (111) by resistive deposition. Current-voltage (*I-V*), capacitance- voltage (*C-V*) measurement techniques were used to characterise the as deposited and annealed Pd/n-Si Schottky contacts. These contacts were annealed at temperatures ranging from 200°C to 700°C, in steps of 100°C for ten minutes each temperature. The ideality factor increased from 1.2 for as deposited to 1.6 after annealing at 700°C while the Schottky barrier height (SBH) decreased from 0.69 to 0.64 eV as the annealing temperature increased. In this study, silicides seem to form at 300°C where the ideality factor is at its lowest value and SBH begins to lower. The Rutherford backscattering Spectroscopy (RBS) technique was used to verify temperatures at which Pd_2Si was formed. The results obtained suggest that the Pd_2Si silicide phase begins to form at 200°C and at 300°C it is completely formed.

The defects introduced in epitaxially grown p-type silicon (Si) during electron beam exposure were electrically characterised using deep level transient spectroscopy (DLTS) and high resolution Laplace-DLTS. In this process, Si samples were first exposed to the conditions of electron beam deposition (EBD) without metal deposition. This is called electron beam exposure (EBE). After 50 minutes of EBE, aluminium (Al) and nickel (Ni) Schottky contacts were fabricated using the resistive deposition method. For the Al contacts, the defect level H(0.33) was identified as the interstitial carbon (C_i) related defect. The defect level observed using the Ni contacts had an activation energy of H(0.55). This defect has an activation energy similar to that of the I-defect. DLTS depth profiling revealed that H(0.33) and H(0.55) could be detected up to a depth of 1.2μm and 0.8μm respectively. We found that exposing the samples to EBD conditions without metal deposition introduced a different group of defects which are not introduced by the EBD method.

Investigation of defects introduced when epitaxially grown Si was irradiated by making use of a 5.4MeV americium 241 (Am241) foil radioactive source with a fluence rate of 7×10^6 cm^{-2} s^{-1} at room temperature. Deep level transient spectroscopy and Laplace-DLTS measurements were used to investigate the electronic properties of the defects introduced. After

exposure to alpha-particles with a fluence of 5.1×10^{10} cm^{-2}, the energy levels of the hole traps measured were: H(0.16), H(0.33) and H(0.52). H(0.33) was identified as the interstitial carbon (C_i) related defect. It was a result of induced damage and could only be explained by the presence of donor-like traps. H(0.52) was a boron-related defect. The identity of (0.16) was not clear.

Declaration

I, Helga Tariro Danga declare that this dissertation, which I hereby submit for the degree of Magister Scientiae (MSc) in Physics at the University of Pretoria is my own work and has not been submitted by me for a degree at this or any other tertiary institution.

Signature…… Date……..

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Contents

Chapter 1

Introduction

Silicon (Si) is the second most abundant element on earth. It occurs in the form of a compound, most often as the oxide (silica) or as a silicate. These compounds form a wide variety of rocks and minerals. The common mineral quartz is a form of silica. Silica was considered to be an element until late in the 18th century. It was correctly proposed to be an oxide by Lavoisier in 1787 [1].

In the second half of the twentieth century, one of the most important uses for Si was its ability to conduct electricity in a controlled manner relative to how many impurities or dopants (boron, phosphorus, arsenic, antimony, etc.) are placed into its crystal structure. Simply put across, the more dopant in the crystal lattice of Si the more it will conduct electricity. In theory pure monocrystalline Si will not conduct electricity very well at all, the beauty of Si is that it can be made to take on dopants precisely and after this doping it will normally remain stable under many adverse conditions. Thus making the Si wafer an ideal surface for the construction of today's and tomorrow's most advanced semiconductor devices. In recent years, Silicon is the most commonly used material for internal cavity fold mirrors and external beam delivery mirrors. The selection is mainly due to its low cost, thermal stability, and good durability.

The interest in metal silicides is because of their technological application as ohmic contacts, metal gates, Schottky contacts, and interconnects, all which possess reliable and stable characteristics. These features have been considered for solar cell fabrication since silicides can be prepared by techniques suitable for mass production. The annealing processes involved occur at moderate temperatures for a short space of time, therefore, there is low energy consumption.

Defects in crystal can either be beneficial or a nuisance to the electrical properties of semiconductors. Some structural defects are unavoidable whereas others are process-dependent so they can be controlled to a certain extent.The radiation of semiconductors targets the understanding of the structure of defects introduced during irradiation. While the main aim of the EBE technique is to see if electron beam deposition (EBD) induced defects can be introduced in a controlled manner [2].

The aim of this work is to investigate the effect that certain critical fabrication processes have on device performance. In chapter 2 the general theory of semiconductors is laid out. Chapter 3 deals with the theory of silicon as a semiconductor and gives the overview of silicides formation and defects in Si. Chapter 4 discusses the experimental techniques employed in this work. In chapter 5 all the results in this study are discussed. Chapter 6 consists of the conclusions of the study and suggestions for future work.

Chapter 2

Semiconductor Theory

2.1 Introduction

Semiconductors are solid state materials having electrical conductivities intermediate between those of metals and those of insulators. Their electrical conductivity can be varied by altering temperature and impurity content. It is because of these variations of electrical properties that make semiconductors ideal for use in electronic devices making them a good medium for the control of electrical current. They get their characteristic conductivity from their small band gap. Having a band gap prevents short circuits since the electrons aren't continuously in the conduction band. Semiconductors are classified by the fully occupied valence band and unoccupied conduction band. With the small band gap in between these two bands, it takes a certain amount of energy to excite the electrons from the valence to conduction band. Thus it follows that the higher the temperature, the more conductive the solid will be. At high temperatures its conductivity approaches that of a metal, and at low temperatures it acts as an insulator [3].

2.1.1 General properties of semiconductors

Electrical characterisation of semiconductors is achieved by having the knowledge of their basic properties. In a semiconductor, electrical conduction is made possible by charge carriers. These can be electrons in the conduction band or holes in the valence band. The concentration of electrons and holes can be controlled by the amounts of impurities which are intentionally introduced into a semiconductor.

2.1.2 Energy and band structure

Complete energy band diagrams of semiconductors are quite complex. The detailed energy band diagram of silicon is shown in Figure 2-1. The energy is plotted as a function of the wavenumber, k, along the main crystallographic directions in the crystal since the band diagram depends on the direction in the crystal. The energy band diagrams contain multiple completely-filled and completely-empty bands. For any semiconductor there is a forbidden energy range in which allowed states cannot exist. Energy regions or energy bands are permitted above and below this energy gap. The upper bands are called the conduction bands; the lower bands, the

valence bands. The separation between the energy of the lowest conduction band and that of the highest valence band is called the bandgap or energy gap E_g, which is one of the most important parameters in semiconductor physics. In this figure the bottom of the conduction band is designated E_C and the top of the valence band E_V.Within the bands, the electron energy is conventionally defined to be positive when measured upward from $E_C$and the hole energy is positive when measured downward from E_V.

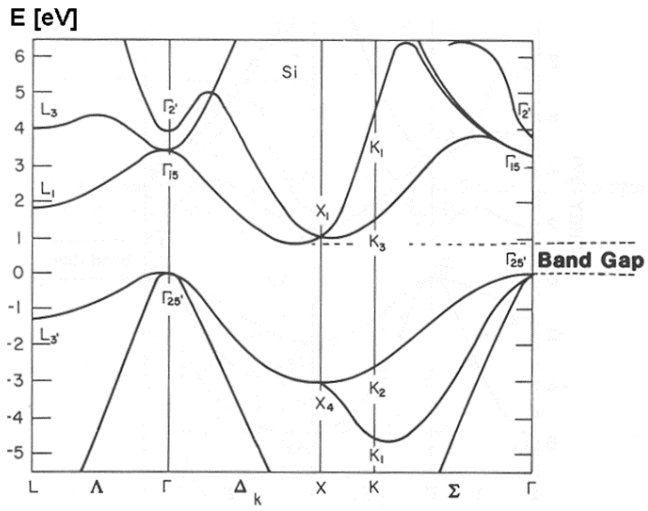

Figure 2-1: Energy band structure of Si.

Fortunately, we can simplify the energy band diagram since only the electrons in the highest almost-filled band and the lowest almost-empty band dominate the behaviour of the semiconductor.

2.2 Occupancy of states in the valence band and conduction band

When electrically characterising semiconductors, it is essential to know the response of electrons to an applied electric field. For an intrinsic semiconductor, there are just enough electrons to fill all the states in the valance band [3]. In order to obtain a semiconductor material that is useful for device fabrication, it is necessary to dope the material with specific impurity atoms. In general, adding group V elements to semiconductor materials in group IV for example produces extra electrons within the material yielding an n-type semiconductor material. Similarly, adding group III elements to the material produces a p-type semiconductor [3]. This is because only three bonds are complete, resulting in holes.

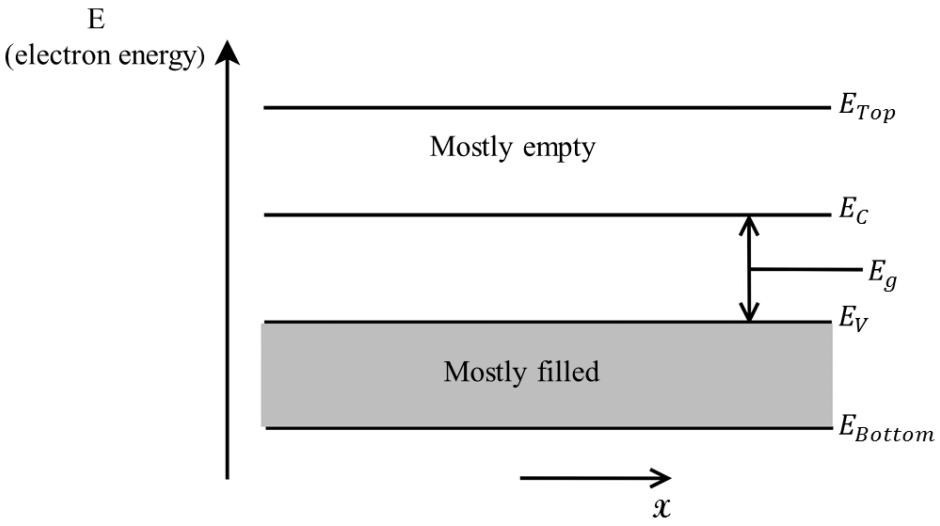

Figure 2-2: Schematic diagram of the energy band model shown on a plot of allowed electron energy states, E as a function of position x redrawn from [3].

The total number of electrons in the conduction band of a semiconductor material is given by:

$$n = \int_{E_C}^{E_{Top}} N(E)\,F(E)dE \qquad 2.1$$

Where $E_{Top}$the energy at the top of the conduction is band and E_C is the energy at the bottom of the conduction band. $N(E)$ is the density of states in the conduction band and $F(E)$ is the probability that a state is occupied. $N(E)$ can be approximated by the density near the bottom of the conduction band using:

$$N(E) = M_c \frac{\sqrt{2}}{\pi^2}\frac{(E - E_C)^{1/2}}{\hbar^3}(m_{de})^{3/2} \qquad 2.2$$

Where M_c is the number of equivalent minima in the conduction band,h is the reduced Planks constant and $m_{de}$is the density of state effective mass for electrons [3].

The Fermi-Dirac distribution function $F(E)$ is given by

$$F(E) = \frac{1}{1 + exp\left(\frac{E - E_F}{kT}\right)} \qquad 2.3$$

Where k is Boltzmann's constant, $T$is the absolute temperature and E_F is the Fremi energy which can be obtained from the charge neutrality condition:

$$n + N_A^- = N_D^+ + p \qquad 2.4$$

Where n is the electron density in the conduction band, N_A^- is the ionised acceptor concentration, N_D^+ is the ionised donor concentration and p is the hole density in the valence band. The number of ionised donors N_D^+ is given by

$$N_D^+ = N_D \left[1 - \frac{1}{1 + \frac{1}{g} exp\left(\frac{E_D - E_F}{kT}\right)} \right] \qquad 2.5$$

where g is the ground-state degeneracy of the donor impurity level. When acceptor impurities are added to the semiconductor material a similar expression can be written for the charge neutrality condition. The concentration of the acceptor impurity is given by N_A.

The integral, equation 2.1, can be evaluated to give

$$n = N_C \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{E_F - E_C}{kT}\right) \qquad 2.6$$

Where N_C is the effective density of states in the conduction band and is given by

$$N_C \equiv 2\left(\frac{2\pi m_{de} kT}{h^2}\right)^{3/2} M_c \qquad 2.7$$

and $F_{1/2}(\eta_f)$ is from the Fermi-Dirac integral. Changing variables with $\eta \equiv (E - E_C)/kT$ and $\eta_F \equiv (E_F - E_C)/kT$ it is given by

$$\begin{aligned} F_{1/2}\left(\frac{E_F - E_C}{kT}\right) &\equiv F_{1/2}(\eta_F) \\ &= \int_{E_C}^{\infty} \frac{[(E - E_C)/kT]^{1/2}}{1 + exp[(E - E_F)/kT]} \frac{dE}{kT} \\ &= \int_0^{\infty} \frac{\eta^{1/2}}{1 + exp(\eta - \eta_F)} d\eta \end{aligned} \qquad 2.8$$

Consider that for $\eta_F < -1$, the integral can be approximated by an exponential function. At $\eta_F = 0$ when the Fermi level coincides with the bandedge, the integral has a value of approximately 0.6 such that $n \approx 0.7N_C$.

2.2.1 Degenerate semiconductors

For degenerate doping levels the carrier concentrations are near or beyond the effective density of states (N_C or N_V), the value of Fermi-Dirac integral has to be used instead of the simplified Boltzmann statistics. For $\eta_F > -1$, the integral has weaker dependence on the carrier concentration. Note that also the Fermi levels are outside the energy gap. A useful estimate of the Fermi level as a function of carrier concentration is given by,

$$E_F - E_C \approx kT\left[ln\left(\frac{n}{N_C}\right) + 2^{-3}/_2\left(\frac{n}{N_C}\right)\right] \qquad 2.9$$

for n-type semiconductor and

$$E_V - E_C \approx kT\left[ln\left(\frac{p}{N_V}\right) + 2^{-3}/_2\left(\frac{p}{N_V}\right)\right] \qquad 2.10$$

for p-type semiconductor.

2.2.2 Non-degenerate semiconductors

In the case of non-degenerate semiconductors, the doping concentrations are smaller than N_c and the Fermi levels are more than several kT below E_C, the Fermi-Dirac integral approaches

$$F_{1/2}\left(\frac{E_F - E_C}{kT}\right) = \frac{\sqrt{\pi}}{2} exp\left(-\frac{E_C - E_F}{kT}\right) \qquad 2.11$$

The Boltzmann statistics case, for the Fermi level several kT below E_C in non-degenerate semiconductors, the integral approaches $\sqrt{\pi}e^{\eta_f/2}$ and equation 2.6 becomes

$$n = N_C exp\left(-\frac{E_C - E_F}{kT}\right) \qquad 2.12$$

Similarly for hole density near the top of the valence band, we obtain:

$$p = N_V \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{E_V - E_F}{kT}\right) \quad 2.13$$

Where N_V is the effective density of states in the valence band and is given by

$$N_V \equiv 2\left(\frac{2\pi m_{dh} kT}{h^2}\right)^{3/2} \quad 2.14$$

Where under non-degenerate conditions we obtain

$$p = N_V exp\left(-\frac{E_F - E_V}{kT}\right) \quad 2.15$$

2.3 Electrical properties of semiconductors

For one to electrically characterise semiconductor materials, the following properties are of interest: donor density N_D, acceptor densityN_A, resistivityρ, mobility μ and carrier lifetime τ.

The total resistivity is a sum of two contributions:

$$\rho = \rho_o + \rho_i \quad 2.16$$

Where ρ_o is due to scattering by impurities and ρ_i is a result of electrons being scattered by phonons. Mobility measures the ease with which electrons move under the influence of an electric field. If the effective density N_D of the donors and the resistivity ρ are known, then mobility can be calculated from:

$$\sigma = {}^{1}/_{\rho} = q\mu N_D \quad 2.17$$

Similarly for holes we obtain

$$\sigma = {}^{1}/_{\rho} = q\mu N_A \quad 2.18$$

Where σ is the conductivity and q is the electronic charge [3].

2.3.1 Intrinsic Semiconductor

A crystal structure which contains negligible amounts of impurities and also in which no atoms are displaced from their lattice sites is called an intrinsic semiconductor [4]. In such a material,

there are no charge carriers at absolute zero since the valence band is completely filled with electrons and the conduction band is empty. At higher temperatures electrons are thermally excited across the band gap to the conduction band. Each electron that is excided into the conduction band leaves a hole in the valence band as a result, the number of electrons and holes should be equal [4].

2.3.2 The Fermi level

The Fermi level of an intrinsic semiconductor is found very close to the middle of the band-gap. When impurities are introduced into the material, the Fermi level must adjust itself to maintain charge neutrality. For an intrinsic semiconductor the number of electrons in E_C is equal to the number of holes in E_V.

Recall: $n = N_C exp\left(\frac{-E_F - E_C}{kT}\right)$ and $p = N_V exp\left(\frac{-E_V - E_F}{kT}\right)$

$$n = p$$

gives

$$N_C exp\left(\frac{E_F - E_C}{kT}\right) = N_V exp\left(\frac{E_V - E_F}{kT}\right) \qquad 2.19$$

Dividing both sides of the equation by N_C yields

$$exp\left(\frac{2E_F - E_C - E_V}{kT}\right) = \frac{N_V}{N_C} \qquad 2.20$$

Applying the natural logarithm to both sides gives

$$\frac{2E_F - E_C - E_V}{kT} = ln\left(\frac{N_V}{N_C}\right) \qquad 2.21$$

Solving for E_F

$$2E_F - E_C - E_V = kTln\left(\frac{N_V}{N_C}\right) \qquad 2.23$$

$$2E_F = kTln\left(\frac{N_V}{N_C}\right) + E_C + E_V \qquad 2.24$$

$$E_F = \frac{E_C + E_V}{2} + kTln\left(\frac{N_V}{N_C}\right) \qquad 2.25$$

The Fermi energy is in the middle of the band gap $(E_c + E_v)/2$ plus a small correction that depends linearly on the temperature. The correction term is small at room temperature since $E_g \sim 1eV$ while $kT \sim 0.025\ eV$ [3].

2.3.3 Extrinsic semiconductor

When a semiconductor is doped with impurities to the extent that the equilibrium carrier concentration of electrons and holes are different from the intrinsic carrier concentration, the material is said to be extrinsic [3]. It is possible to create carriers in semiconductors by introducing impurities into the crystal so that has predominance of either holes or electrons. When impurities are added to a perfect crystal additional levels are created within the band gap. An energy level created by an impurity near the conduction band is called a donor level and an energy level introduced close to the valence band is called an acceptor level.

2.4 Defects in semiconductors

During semiconductor-processing defects are introduced. These defects modify the electronic structure of the semiconductor material [3]. The defects can be classified into two groups: shallow levels and deep levels. Shallow levels are located near the conduction band for donors and for acceptors, near the valance band. Deep levels are those defects located deeper in the bandgap than the dopant levels [3]. Deep levels are desirable in some applications for example, in fast switching devices where recombination centres are exploited since they quickly remove minority carriers, thereby enhancing the switching speed of the device increasing its efficiency as a result. Deep level defects can also be an inconvenience if they are present in semiconductors that are used for photovoltaic applications since they reduce the solar cell's efficiency by allowing created electron-hole to recombine. Generally, the periodicity of the crystal is disturbed and local deformation in the crystal is introduced resulting in new energy levels which are often found in the forbidden bandgap [3].

2.4.1 Impurities and defects

The presence of small amounts of impurities in a semiconductor drastically influences its electronic properties. There are two types of impurities found in semiconductors. The first type is as a result of dopant impurities which have shallow levels close to the conduction band or valence band and are responsible for conduction [5]. Dopant elements found on the right side of the host atom in the periodic table are referred to as donors because they have more unpaired electrons than the host atoms. They give rise to n-type semiconductors. Elements to the left of the periodic table are called acceptors because they accept electrons from the host atom in order for them to fulfil the bonding requirements. These atoms give rise p-type semiconductors.

The second type impurities are found further from the band edges and are usually referred to as traps, recombination centres, generation centres or deep level defects [6]. An electron trap can be defined as a defect for which the electron capture is larger than the hole capture rate. In contrast, a recombination centre is defined as a defect for which both the electron and hole capture rates are large and comparable in magnitude [7].

Defects can be defined in terms of majority or minority carrier traps in terms of their thermal emission properties. A defect where the rate of thermal emission of majority carrier is larger than that of a minority carrier is known as a majority carrier trap. A minority carrier trap has its rate of thermal emission larger than that of the majority carrier and is known as a minority carrier trap [7].

2.4.2 Types of defects

In a perfect crystal, all host atoms are located on their proper lattice sites and the crystal contains neither impurities nor structural imperfections. The band diagram for such a crystal consists of the conduction and valence band with no energy levels within the band gap as shown schematically in Figure 2-3(a). A real crystal is not like that. It contains structural imperfections as well as foreign impurities. The foreign impurities consist of intentionally introduced dopant atoms and unintentionally introduced impurity atoms as well as structural imperfections that are generated during crystal growth and during device processing.

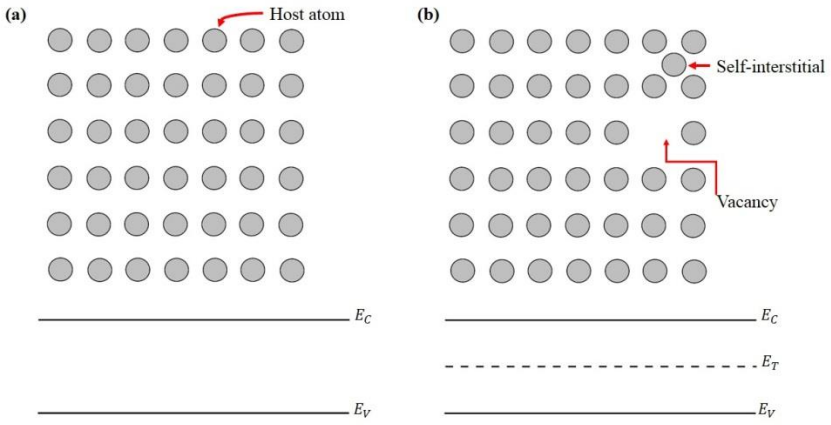

Figure 2-3: Schematic diagram of a silicon crystal lattice and the corresponding energy band diagrams (a) without, and (b) with vacancies and self-interstitials [8].

Some structural defects are unavoidable while others are process-dependent. In principle it is possible to eliminate all foreign impurities and most structural defects. Thermodynamic considerations, however, demand a certain concentration of self-interstitials and vacancies as shown in Figure 2-3 (b). In other words the perfect crystal of figure 2-3 (a) is thermodynamically impossible to achieve. Self-interstitials are atoms of the host lattice (silicon atoms in a silicon crystal) displaced from their normal substitutional sites to interstitial sites.

Thermodynamics tells us that the free energy of a crystal depends on its internal energy, E, entropy, S, temperature, T, pressure, p, and volume, V. A reduction in self- interstitials and vacancies reduces the crystal's internal energy because the crystal takes on a more ordered structure. However, the entropy of a more ordered crystal is higher than that of a disordered crystal. The free energy, G, sometimes called the Gibbs free energy, is given by

$$G = U - TS + pV \qquad 2.26$$

Aside from the pV product, the free energy is proportional to the difference between the internal energy, U and TS - a term proportional to the entropy. The pV term in this discussion is not considered. The equilibrium state of the crystal corresponds to a minimum in the free energy which requires a certain amount of disorder. Recall that entropy is a measure of disorder. That is to say, the most favourable free energy state of the crystal is a compromise between crystal perfection and disorder. A single crystal is largely a perfect crystal, but contains a certain

concentration of self-interstitials and vacancies to satisfy the "minimum free energy" standard [8]. Besides vacancies and self-interstitials, there are other defects as shown in table 2-1.

Table 2-1: Examples of crystalline defects

Type of Defect	Examples
Point or Zero-Dimensional Defects	Vacancy
	Interstitial (self and foreign interstitials)
	Frenkel
	Extrinsic Defects
Line or One-Dimensional Defects	Straight dislocations (edge or screw)
	Dislocation Loops
Area or Two-Dimensional Defects	Stacking Faults
	Twin planes
	Grain boundaries
Volume or There-Dimensional Defects	Precipitates
	Impurity clusters
	Voids

Grain boundaries and twin planes are not found in single crystal Czochralski or float-zone grown Si. All other defects can be and usually are encountered in a processed device [8].

Various types of defects are shown schematically in figure 2-4. The grey circles represent the host atoms (e.g., silicon). The defects are: (a) foreign interstitial, (b) foreign substitutional, (c) vacancy, (d) self-interstitial, (e) stacking fault, (f) edge dislocation and (g) precipitate [5].

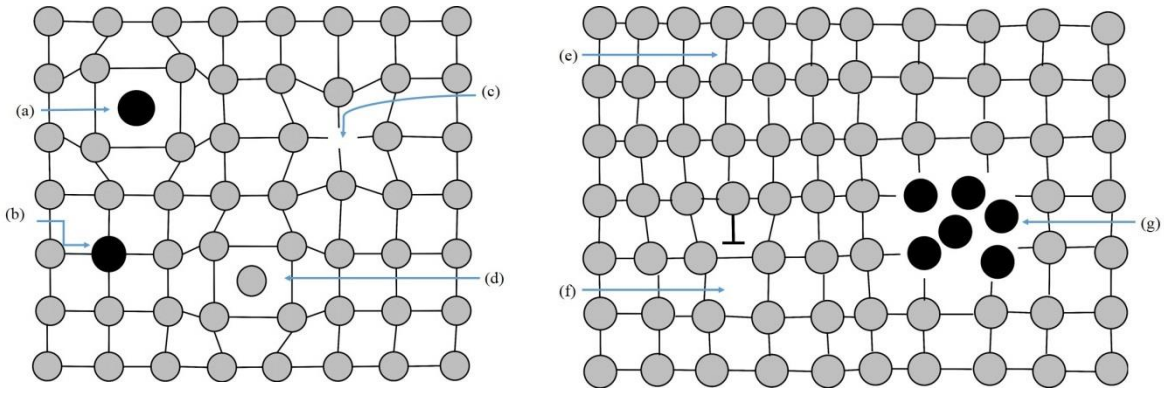

Figure2-4: Schematic representation of defects in semiconductors redrawn from ref [5].

2.4.3 Point defects in semiconductors

Point defects in elemental semiconductors can be divided into three groups:

a) **Vacancies** occur when an atom is missing from a regular lattice site.

b) **Interstitials** are formed when an atom occupies the space between regular lattice sites. The interstitial atom can be of the same atomic species as the lattice or it can be an impurity atom.

c) **Substitutional impurity.** This is when a foreign atom replaces a native atom in the lattice [9].

d) **Frenkel Pair** is a vacancy and an interstitial defect. This occurs when an atom vacates its original position in the lattice and occupies an interstitial position in the crystal [10].

Figure 2-5 represents the above mentioned defects.

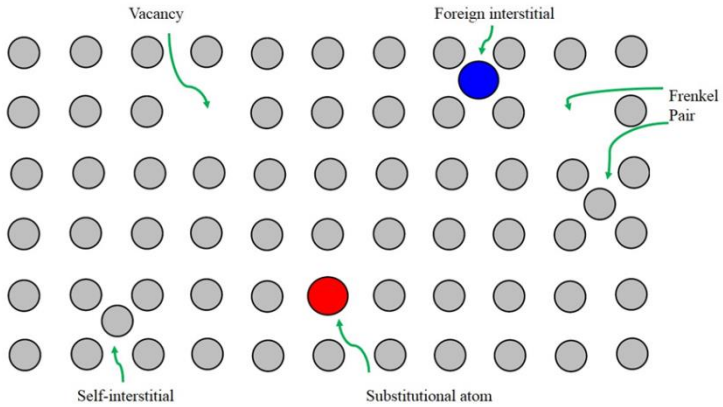

Figure 2-5: Common point defects in semiconductors. Substitutional and interstitial defects involve a separate ion, whereas self-interstitials are due to an original atom [10].

2.4.4 Capture and emission by electronic defect states

The fabrication and development of efficient semiconductors requires sufficient knowledge of the identity, nature and properties of the deep levels that are native and those which are induced in the semiconductor. Depending on the application of the semiconductor, defects can be detrimental to device operation or they may enhance the operation of the device. Defects with deep states in the forbidden energy gap or band gap (E_g) are usually referred to as traps, recombination centres, generation centres or deep level defects [7]. Taking into consideration an electron state at the energy of the trap (E_T) below the conduction band (E_C) and with a concentration of N_T. The rates of emission of an electron to E_C and a hole to the valance band (E_V) are denoted by e_n and e_n, respectively. The rate of capture of an electron from E_C or a hole from E_V is c_n and c_p respectively,taking into consideration an electron state at an energy E_T below E_C and with a concentration of N_T. The rates of emission of an electron to E_C and a hole to E_V are denoted by e_n and e_n, respectively. The rate of capture of an electron from E_C or a hole from E_V is c_n and c_p respectively.

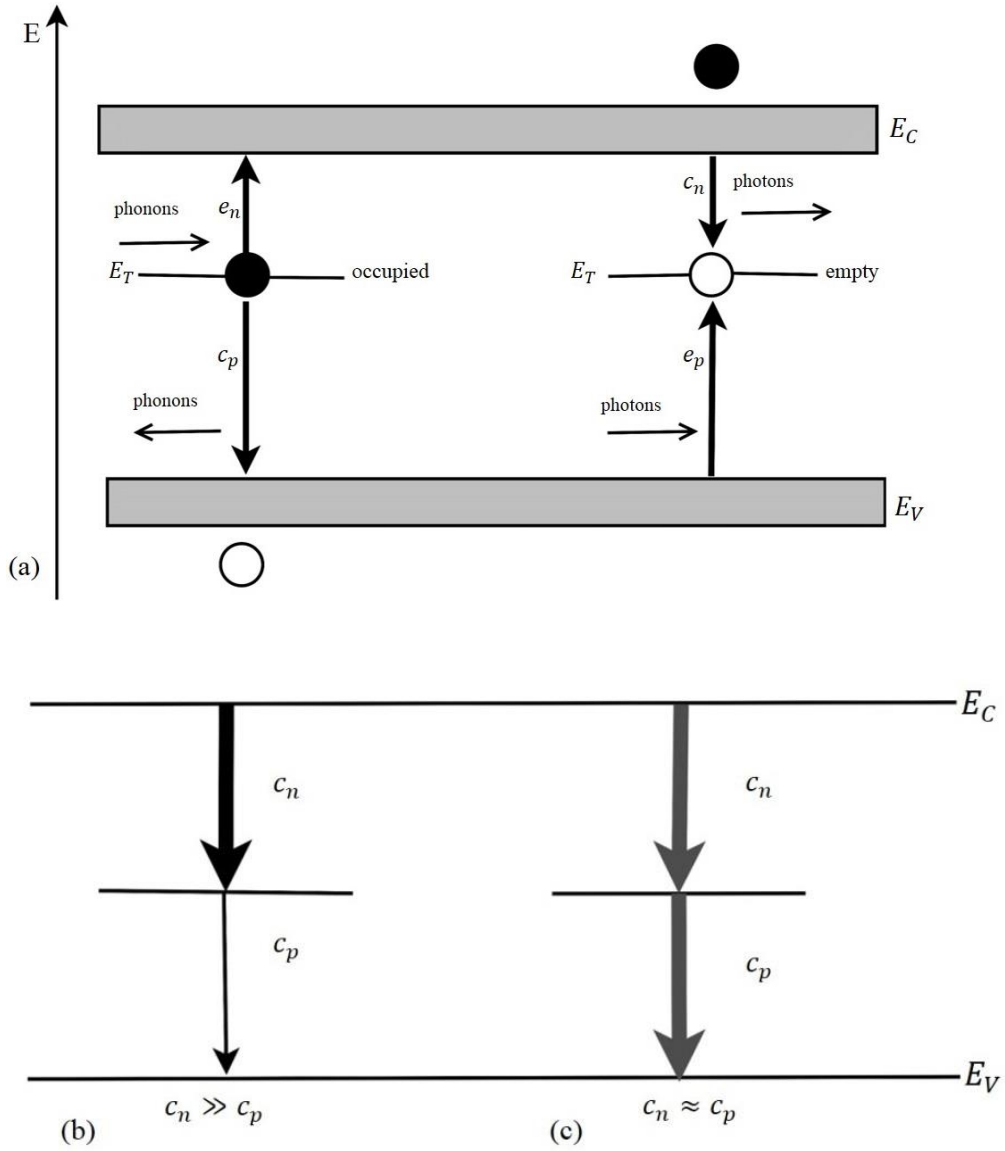

Figure 2-6: (a) a schematic illustration of thermal emission and capture rates at deep levels, (b) the electron trap, (c) a recombination centre redrawn from refs [7, 11].

According to the Shockley-Read model [12], the capture-cross section, σ_n, for electron capture is related to the electron capture rate, c_n,by the expression

$$c_n = \sigma_n \langle V_n \rangle n \qquad 2.27$$

Where $\langle V_n \rangle$= average thermal velocity of free electrons and is given by

$$\langle V_n \rangle = \sqrt{3kT/m^*} \qquad 2.28$$

with m* as the effective mass for electrons (holes), T as the absolute temperature, and k as Boltzmann's constant.

Traps are further characterised as majority or minority carrier traps. The thermal emission rate,e_n, of carriers from traps is proportional to a Boltzmann factor, $exp(-\Delta E/kT)$ and for traps which emit electrons to the conduction band, e_n can be expressed as follows:

$$e_n = \frac{\sigma_n \langle V_n \rangle N_C}{g}\ exp\left[\frac{-\Delta E}{kT}\right] \qquad 2.29$$

Where: $\Delta E = E_C - E_T$

E_C and E_T= energies of the conduction band trap respectively

N_C= effective density of states in the conduction band

g = degeneracy of the defect level

T = absolute temperature

It must be noted that analogous expressions hold for holes.

The quantity $\langle V_n \rangle N_c$ varies as T^2 this means that if e_n can be measured as a function of temperature, an Arrhenius plot of $^{e_n}/_{T^2}$ against $^{1000}/_{T}$ must produce a straight line whose slope will yield ΔE and the intercept (at $1000/T = 0$) will give σ_n. The electron and hole capture cross- sections, σ_n and σ_p are generally temperature dependant. In the case of deep level defects, this is often the result of carrier capture by multiphonon emission through lattice relaxation [13]; in which case the capture cross-section, σ has the form:

$$\sigma = \sigma_\infty \exp\left[\frac{-\Delta E_\sigma}{kT}\right] \qquad 2.30$$

Where ΔE_σ= thermal activation energy of the capture cross-section

A more general expression for the thermal emission rate of electrons to the conduction band:

$$e_n = \frac{\sigma_n \langle V_n \rangle N_C}{g}\, exp\left[-\frac{(\Delta E + \Delta E_\sigma)}{kT}\right] \qquad 2.31$$

The thermal activation energy for emission of an electron to the conduction band, $\Delta E_a = \Delta E + \Delta E_\sigma$, determined from an Arrhenius plot, has two components: the energy difference between the trap level and the bottom of the conduction band, ΔE, and the thermal activation energy of the capture cross-section, ΔE_σ. The activation energy for thermal emission is the most frequently used parameter to characterise a deep level. Nevertheless, the parameter ΔE in equations 2.29 and 2.31 is the Gibbs free energy:

$$\Delta E = E_V - E_T \equiv \Delta H - T\Delta S \qquad 2.32$$

Where ΔH and ΔS are the changes in enthalpy and entropy due to the change in the charge state of the level. Combining equations 2.29 and 2.32 gives:

$$e_n = \frac{\sigma_n \langle V_n \rangle N_C}{g} exp\left[\frac{\Delta S}{k}\right] exp\left[\frac{\Delta H}{kT}\right] \qquad 2.33$$

From equation 2.33 the slope of the Arrhenius plot gives the enthalpy of the deep level, not the free energy which can only be determined from optical measurements [7]. Looking at equation 2.33 it is observed that the activation energy obtained from the slope of an Arrhenius plot is equal to the free energy obtained at $T = 0\ K$. This is generally the same as free energy at the measurement temperature, due to the temperature dependence of the energy gap. For temperatures greater than absolute zero, that being the case, the energy position of the trap can be determined precisely when the temperature dependence is known [14].

2.5 Metal-semiconductor contacts

Metal-semiconductor contacts were intensively studied during the 1960s and 1970s. This was greatly encouraged by their importance in semiconductor technology, both as rectifying elements and as low resistance contacts [15]. These contacts are also important in direct current and microwave applications and as intricate parts of other semiconductor devices. Specifically, they have been used as photodetectors, solar cells, as the gate electrode of the MESFET, just to mention a few. Most importantly, the metal contact on heavily doped semiconductor forms an ohmic contact that is required for every semiconductor device in order to pass current in and out of the device [3].

2.5.1 The depletion region

When a metal is brought into close contact with a semiconductor, the conduction and the valence bands of the semiconductor are brought into a definite energy relationship with the Fermi level in the metal. In the n-type semiconductor of figure 2-9 depletion region W is formed near the junction. The positive charge due to uncompensated donor ions within W matches the negative charge on the metal.

Within the depletion region, electrons and holes are in transit from one side of the junction to the other. Some electrons diffuse from semiconductor to metal , and some are swept by the electric field from metal to semiconductor (and conversely for holes); there are, however, very few carriers within the depletion region at any given time, since the electric field serves to sweep out carriers which have wandered into W. To a good approximation, we can consider the space charge within the transition region as due only to the uncompensated donor and acceptor ions. The assumption of carrier depletion within W and perfect neutrality outside W is known as the depletion approximation. The charge density $\rho(x)$ in the depletion region where there are no electrons in the conduction band is given by qN_D. Given that the depletion width is given by W_D, $\rho\ (x)$ in the semiconductor can be written as:

$$\rho(x) = \begin{cases} qN_D \text{ if } x \leq W_D \\ 0 \text{ if } x > W_D \end{cases} \qquad 2.34$$

where N_D is the dopant density and q is the electronic charge [3].

An electric field is created by the charge separation and it results in a potential difference across the metal-semiconductor junction. Solving Poisson's equation and applying the necessary boundary conditions can determine the shape of the band edge profiles. These boundary conditions are obtained from:

(a) the barrier height
(b) the electric field (given that it is considered to be zero within the bulk of the semiconductor).

Taking x to be zero at the interface, the boundary conditions can be written as $V(0) = Vd$ and $E(\infty) = 0$. The solution to the Poisson's equation can be written in one- dimension as

$$\frac{d^2V}{dx^2} = \frac{1}{\varepsilon_s}\rho(x) \qquad 2.35$$

where $\rho(x)$ is the total charge density in the semiconductor at a depth x and ε_s is the semiconductor permittivity. Now if $\rho(x)$ includes the effects from the valence band, conduction band, ionized donors and acceptors, the resulting equation becomes more complicated and would then require the numerical methods to solve it. Making use of the depletion width approximation, integrating equation 2.35 twice and using the boundary conditions will give W as

$$W = \sqrt{\frac{2\varepsilon_s V_d}{qN_d}} \qquad 2.36$$

Under externally applied bias,V_a, the expression for the depletion region is

$$W = \sqrt{\frac{2\varepsilon_s}{qN_D}}\left(V_{bi} - V_a\frac{kT}{q}\right) \qquad 2.37$$

The electric field in the semiconductor is given by

$$E(x) = -\frac{qN_D}{\varepsilon_s}(W - x) \qquad 2.38$$

Integrating equation 2.32, can obtain the electrostatic potential given by

$$V(x) = -\frac{qN_D}{\varepsilon_s}\left(Wx - \frac{1}{2}x^2\right) \qquad 2.39$$

The space charge per unit area of the semiconductor is given by:

$$Q_{sc} = qN_D W = \sqrt{2\varepsilon_s qN_D\left(V_{bi} - V_a - \frac{kT}{q}\right)} \qquad 2.40$$

If this is the amount by which the charge within the depletion region width W changes as a result of a dc bias, this means that a small signal capacitance is given by

$$C = \frac{|\partial Q_{sc}|}{\partial V_a} = \sqrt{\frac{\varepsilon_s qN_D}{2\left(V_{bi} - V_a - \frac{kT}{q}\right)}} = \frac{\varepsilon_s A}{W} \qquad 2.41$$

Equation 2.41 can be written as follows

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - V_a - \frac{kT}{q}\right)}{\varepsilon_s A^2 qN_D} \qquad 2.42$$

Plotting $\frac{1}{C^2}$ versus V_a yields a straight line from which N_D, the doping density, can be calculated from the gradient provided N_D is constant throughout the depletion region. The built-in-voltage V_{bi} is obtained from the voltage intercept [3]. Figure 2-7 shows a plot of $\frac{1}{C^2}$ against V_a

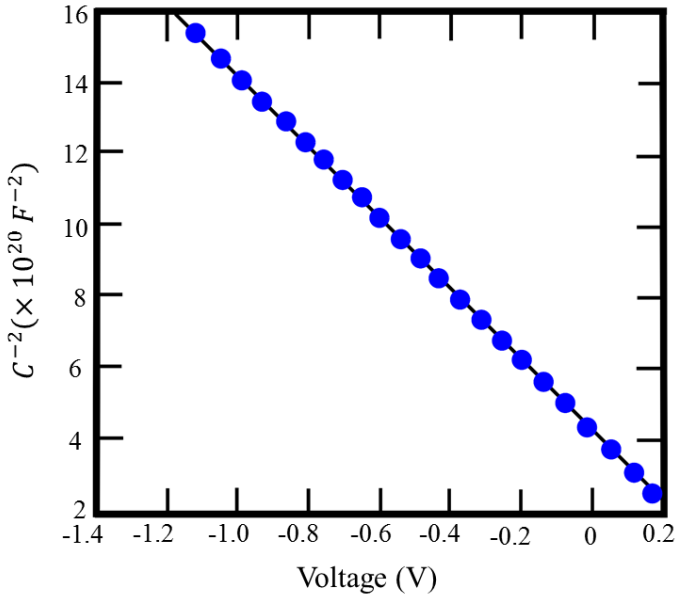

Figure 2-7: The graph of $1/C^2$ against V from which N_D, the doping density, can be calculated from the gradient provided N_D is constant throughout the depletion region. The built-in-voltage V_{bi} is obtained from the voltage intercept.

2.5.2 Barrier height formation

When metal makes contact with a semiconductor, a barrier is formed at the metal-semiconductor interface. This barrier is responsible for controlling the current conduction as well as its capacitance behaviour. When negative charges are brought near the metal surface, positive (image) charges are induced in the metal. When this image force is combined with an applied electric field, the effective work function is somewhat reduced. Such barrier lowering is called the Schottky effect. Although the Schottky effect is only a part of the explanation of metal-semiconductor contacts, rectifying contacts are generally referred to Schottky barrier diodes.

When a metal with work function $q\phi_m$ comes into contact with a semiconductor having a work function $q\phi_s$, charge transfer occurs until the Fermi levels align at equilibrium (figure 2-8). If for example, when $\phi_m > \phi_s$, the semiconductor Fermi level is initially higher than that of the metal before contact is made. To align the two Fermi levels, the electrostatic potential of the semiconductor must be raised (meaning the electron energies must be lowered) relative to that of the metal. In the n-type semiconductor a depletion region W is formed near the junction (figure 2-8). The positive charge due to uncompensated donor ions within W matches the negative charge on the metal.

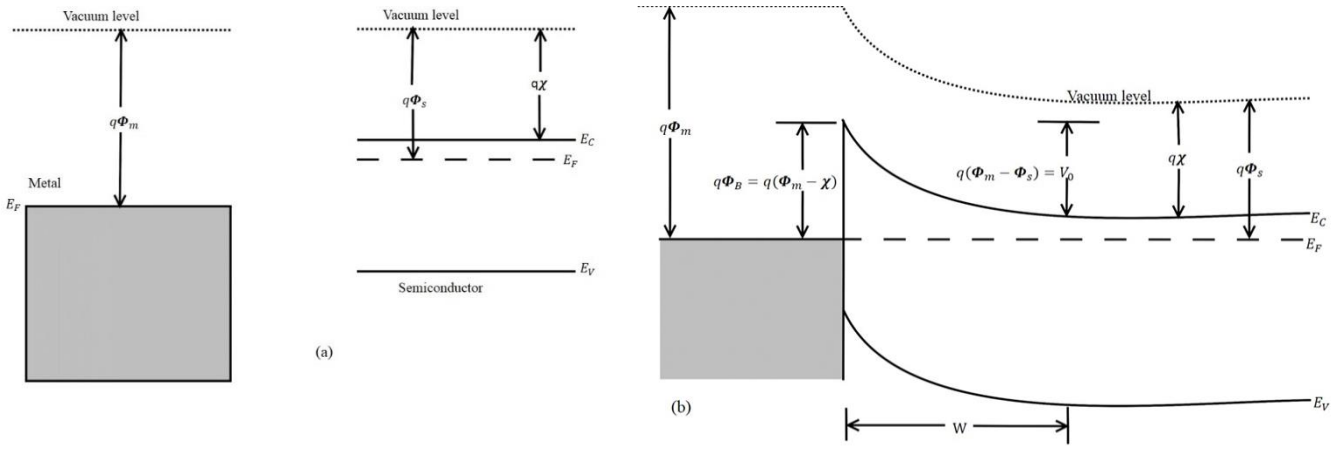

Figure 2-8: (a) band diagrams for the metal and the semiconductor before coming into contact, (b) equilibrium band diagram for the metal-semiconductor junction redrawn from [4].

The equilibrium contact potential V_o, which prevents further net electron diffusion from the semiconductor conduction band into the metal, is the difference in work function potentials $\phi_m - \phi_s$. The potential barrier height ϕ_B for electron injection from the metal into the semiconductor conduction band is $\phi_m - \chi$ where χ (called the electron affinity) is measured from the vacuum level to the semiconductor conduction band edge. The equilibrium potential difference V_o can be decreased or increased by the application of either forward or reverse-bias voltage.

Figure 2-9 illustrates a Schottky barrier on a p-type semiconductor, with $\phi_m < \phi_s$. In this case aligning the Fermi levels at equilibrium requires a positive charge on the metal side and a negative charge on the semiconductor side of the junction. The negative charge is accommodated by a depletion region W in which ionized acceptors (N_a^-) are left uncompensated by holes. The potential barrier V_o retarding hole diffusion from the semiconductor to the metal is $\phi_s - \phi_m$, and as before this barrier can be raised or lowered by the application of voltage across the junction.

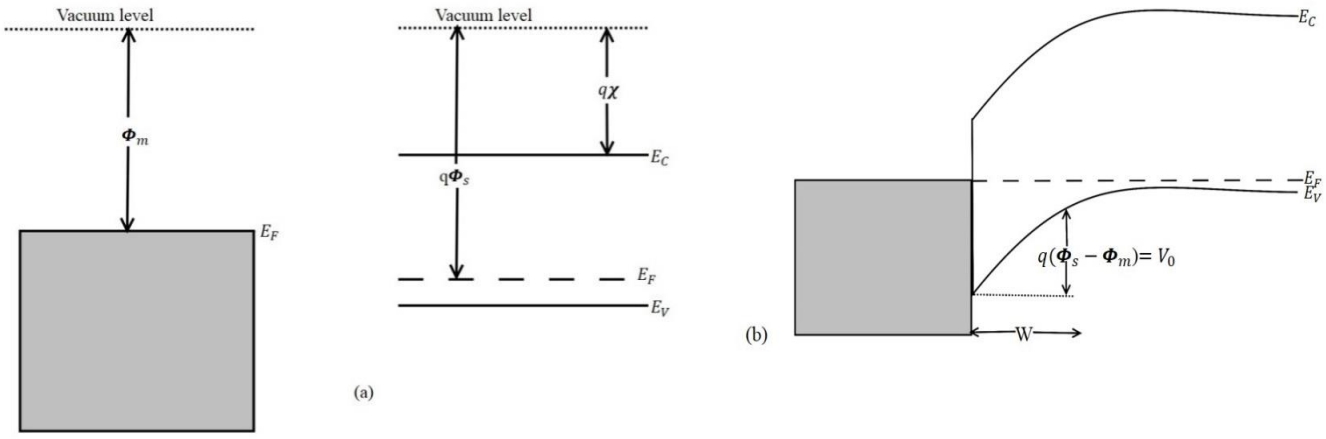

Figure 2-9: Schottky barrier between a p-type semiconductor and a metal having a smaller work function: (a) band diagrams before contact; (b) band diagram for the junction at equilibrium [4].

2.5.3 Rectifying contacts

When a forward-bias voltage V is applied to the Schottky barrier shown in figure 2-10 (a), the contact potential is reduced from V_o to $V_o - V$. As a result, electrons in the semiconductor conduction band can diffuse across the depletion region to the metal. This gives rise to a forward current (metal to semiconductor) through the junction. Conversely, a reverse bias increases the barrier to $V_o + V_r$, and electron flow from semiconductor to metal becomes negligible. In either case flow of electrons from the metal to the semiconductor is retarded by the barrier $\phi_m - \chi$ .The resulting diode equation is

$$I = I_o\left(exp\left({}^{qV}/_{kT}\right) - 1\right) \qquad 2.43$$

One important feature that can be predicted is that the saturation current should depend upon the size of the barrier ϕ_B for electron injection from the metal into the semiconductor. This barrier (which is $\phi_m - \chi$ for the ideal case shown in figure 2-10 (b)) is unaffected by the bias voltage. We expect the probability of an electron in the metal overcoming this barrier to be given by a Boltzmann factor.

$$I \propto exp\left({}^{-q\phi_B}/_{kT}\right) \qquad 2.44$$

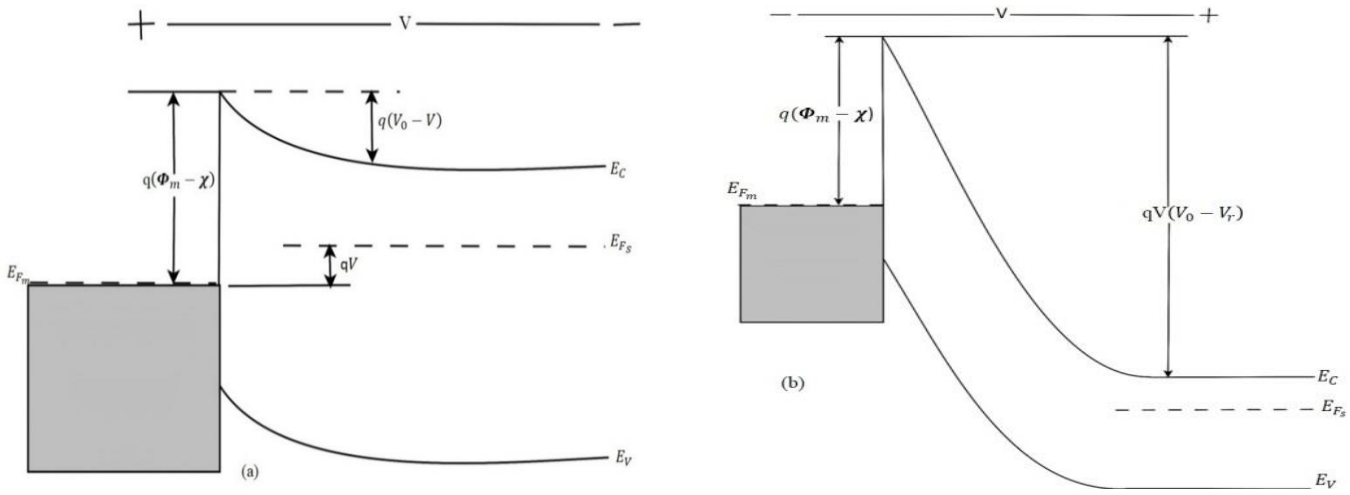

Figure 2-10: Effects of forward and reverse bias on the metal-semiconductor junction (a) forward bias ;(b) reverse bias [4].

The diode equation 2.45 applies also to the metal-p-type semiconductor junction of figure 2-9. In this case forward voltage is defined with the semiconductor biased positively with respect to the metal. Forward current increases as this voltage lowers the potential barrier to $V_o - V$ and holes flow from the semiconductor to the metal. Of course, a reverse voltage increases the barrier for hole flow and the current becomes negligible. In both of these cases the Schottky barrier diode is rectifying, with easy current flow in the forward direction and little current in the reverse direction. We also note that the forward current in each case is due to the injection of majority carriers from the semiconductor into the metal. The absence of minority carrier injection and the associated storage delay time is an important feature of Schottky barrier diodes. Although some minority carrier injection occurs at high current levels, these are essentially majority carrier devices. Their high-frequency properties and switching speed are therefore generally better than typical p-n junctions. In the early days of semiconductor technology, rectifying contacts were made simply by pressing a wire against the surface of the semiconductor. In modern devices, however, the metal-semiconductor contact is made by depositing an appropriate metal film on a clean semiconductor surface and defining the contact pattern photolithographically. Schottky barrier devices are particularly well suited for use in densely packed integrated circuits, because a few photolithographic masking steps are required [4].

2.5.4 Ohmic contacts

In many cases it is desired to have an ohmic metal-semiconductor contact, having a linear current-voltage characteristic in both biasing directions. For example, the surface of a typical

integrated circuit is a maze of p and n regions, which must be contacted and interconnected. It is important that such contacts be ohmic, with minimal resistance and no tendency to rectify signals. Ideal metal-semiconductor contacts are ohmic when the charge induced in the semiconductor in aligning the Fermi levels is provided by majority carriers (figure 2-11). For example, in the case where $\phi_m < \phi_s$ (n-type) case of figure 2-11 (a), the Fermi levels are aligned at equilibrium by transferring electrons from the metal to the. This raises the semiconductor electron energies (lowers the electrostatic potential) relative to the metal at equilibrium. In this case the barrier to electron flow between the metal and the semiconductor is small and easily overcome by a small voltage. Similarly, the case $\phi_m > \phi_s$ (p-type) results in easy hole flow across the junction (figure. 2-11 (b)). Unlike the rectifying contacts discussed previously, no depletion region occurs in the semiconductor in these cases since the electrostatic potential difference required aligning the Fermi levels at equilibrium calls for accumulation of majority carriers in the semiconductor. A practical method for forming ohmic contacts is by doping the semiconductor heavily in the contact region. Thus if a barrier exists at the interface, the depletion width is small enough to allow carriers to tunnel through the barrier. For example, gold (Au) containing a small percentage of antimony (Sb) can be alloyed to n-type Si, forming a n^+ layer at the semiconductor surface and an excellent ohmic contact. Similarly, p-type material requires a p^+ surface layer in contact with the metal. In the case of aluminium (Al) on p-type Si, the metal contact also provides the acceptor dopant. Thus the required p^+ surface layer is formed during a brief heat treatment of the contact after the Al is deposited [4].

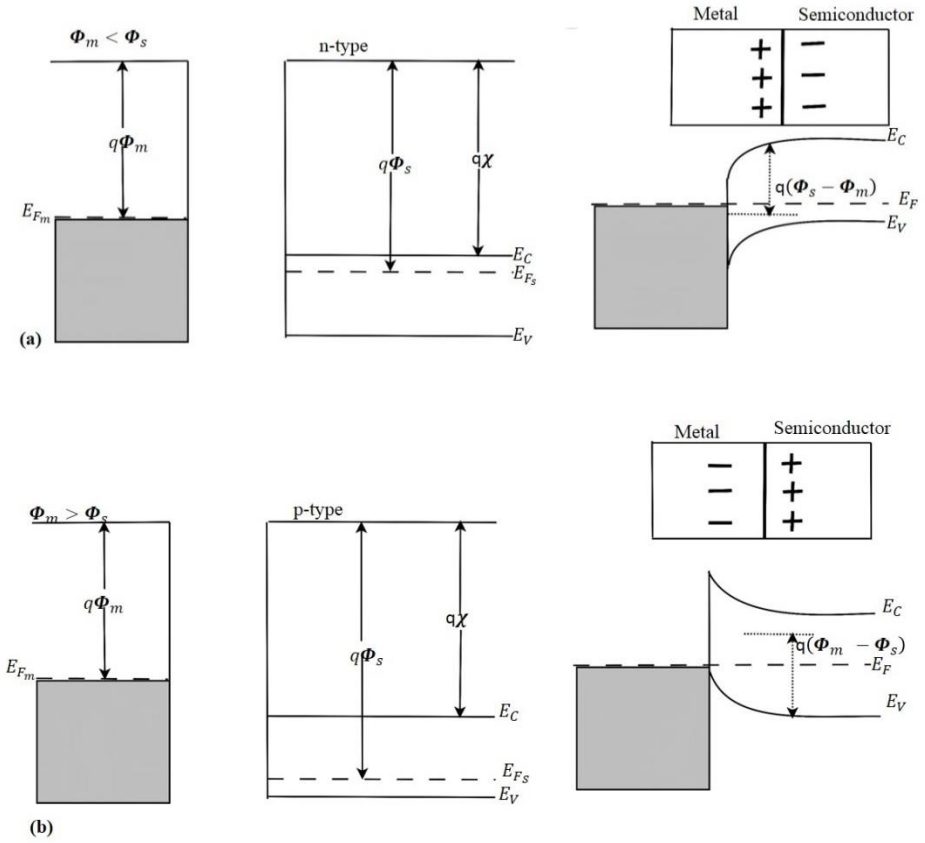

Figure 2-11:Ohmic contacts: (a) n-type semiconductor, and the equilibrium band diagram for the junction; (b) p-type semiconductor, and the junction at equilibrium redrawn from [4].

2.5.5 Current-voltage characteristics

The current-voltage technique is a good method of evaluating the quality of a Schottky diode by determining the reverse and forward current that flows through the device under different biasing conditions. This allows the deduction of the current carrying mechanisms that dominate within the device. Parameters which include ideality factor, barrier height and series resistance can also be obtained from *I-V* measurements.

2.5.6 Capacitance-voltage characteristics

Capacitance–voltage characterisation is a method for describing distinctively semiconductor materials and devices. The applied voltage is varied, and the capacitance is measured and plotted as a function of voltage. The technique uses a metal–semiconductor junction or a p–n junction to create a depletion region which is empty of conducting electrons and holes, but may contain ionized donors and electrically active defects or traps. The depletion region with its ionized charges inside behaves like a capacitor. By varying the voltage applied to the junction it is possible to vary the depletion width. The dependence of the depletion width upon the

applied voltage provides information on the semiconductor's internal characteristics, such as its doping profile and electrically active defect densities [16].

2.5.7 The ideal Schottky diode

Current transport mechanisms

The current transport in metal-semiconductor contacts is due mainly to majority carriers, in contrast to p-n junctions where the minority carriers are responsible. The various ways in which electrons can be transported across a metal-semiconductor junction under forward bias are listed as follows:

(a)**Thermionic emission.** Electrons are discharged over the barrier. There is low probability of direct tunnelling. This is valid for low doping ($N_D \leq 10^{17} cm^{-3}$)

(b) **Thermionic-field emission.** Electrons use thermal energy to tunnel through the thin barrier in the upper end of the conduction band. This applies for intermediate doping ($10^{17} cm^{-3} \leq N_D \leq 10^{18} cm^{-3}$)

(c**) Field emission.** Direct tunnelling occurs since the depletion region is very narrow. This mechanism applies for heavy doping ($N_D \geq 10^{18} cm^{-3}$) ; the contact is almost ohmic.

(d) **Leakage current.** This mechanism occurs as a result of a high probability of defect-assisted tunnelling and simple conduction. Occurs in poor material/interface quality; dislocations

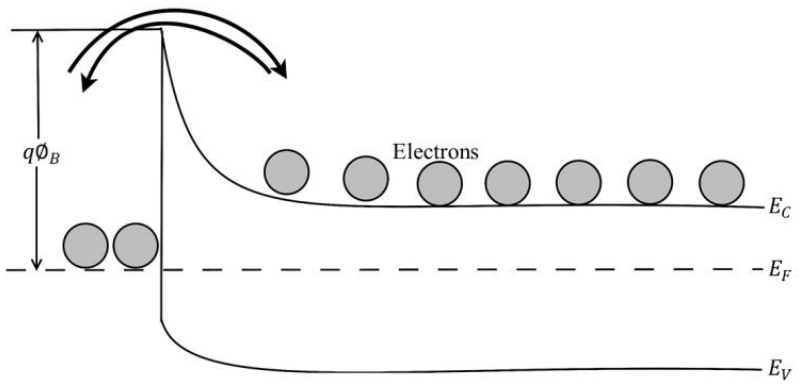

Figure 2-12: a sketch depicting Thermionic Emission.

Thermionic Emission

This process is dominant for Schottky diodes with moderately doped semiconductors (e.g., Si with $N_D \leq 10^{17}$ cm^{-3}) operated at moderate temperatures (e.g., 300 K) [3]. The emission of

electrons from the semiconductor over the potential barrier into the metal is controlled by two processes. Firstly, electrons are transported from inside the semiconductor to the interface by drift and diffusion in the electric field of the barrier and secondly, at the interface, their emission into the metal is determined by the rate of transfer of electrons across the border between the semiconductor and the metal [15]. For common high-mobility semiconductors (e.g., Si and GaAs) the transport can be adequately described by this thermionic-emission theory [3].

By analysing the diffusion and thermionic emission currents it is revealed that they can be written in the following form:

$$\mathrm{I} = I_0 exp\left(\frac{qV}{nkT}\right)\left[1 - exp\left(\frac{-qV}{kT}\right)\right] \qquad 2.45$$

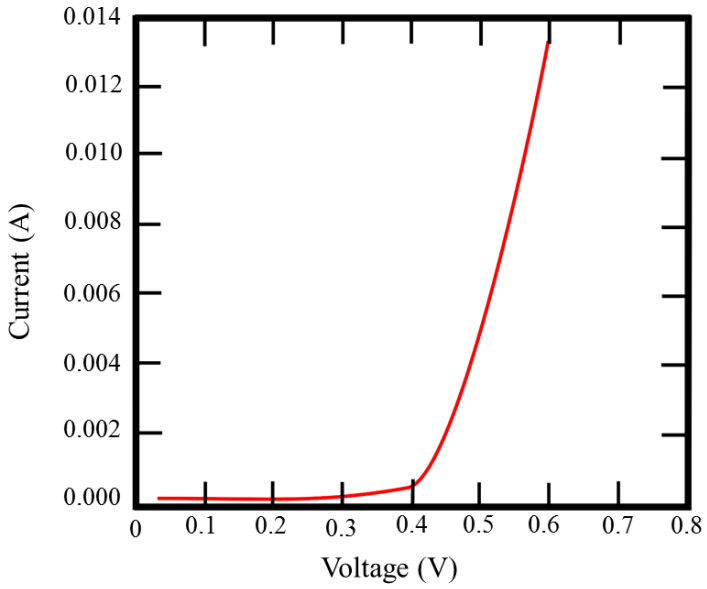

Figure 2-13: A graph showing the linear Current -Voltage characteristics for an ideal diode.

Where I_0 is the saturation current which is given by:

$$I_0 = AA^*T^2 exp\left(\frac{-q\phi_B}{kT}\right) \qquad 2.46$$

Substituting for I_0 into equation 2.45 gives

$$I = AA^*T^2 exp\left(\frac{-q\phi_B}{kT}\right) exp\left(\frac{qV}{nkT}\right)\left[1 - exp\left(\frac{-qV}{kT}\right)\right] \quad 2.47$$

Applying natural log to both sides yields

$$\ln(I) = ln(I_0) + \frac{qV}{nkT} + ln\left[1 - exp\left(\frac{-qV}{kT}\right)\right] \quad 2.48$$

If $V \gg kT/q$ (strong bias conditions), then $V/(kT/q)$ is large and $exp(-qV/kT)$ tends to zero and $ln[1 - exp(-qV/kT)] \sim ln(1) = 0$, then $ln(I) = ln(I_0) + qV/kT$

$$ln(I) = ln(I_0) + \frac{qV}{nkT} \quad 2.49$$

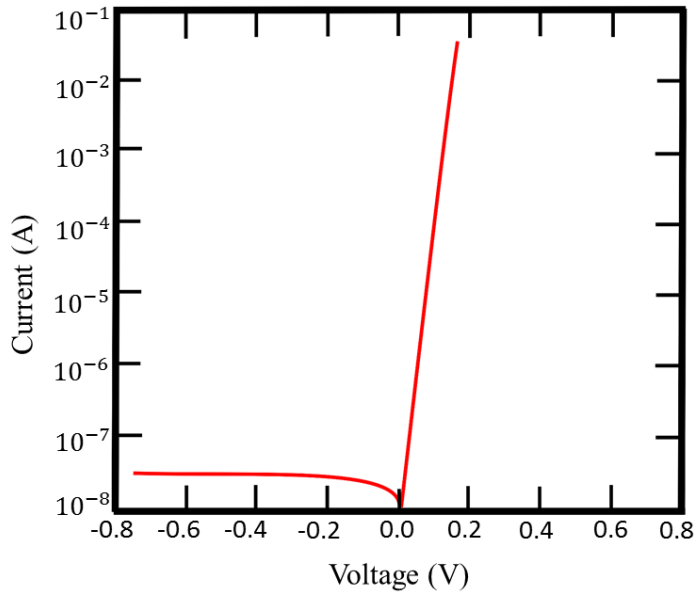

Figure 2-14: A graph of ln (I) against V for an ideal diode.

The slope of ln (I) against V gives the ideality factor n.

The intercept is ln (I_0).

Recall from equation 2.46:$I_0 = AA^*T^2 exp\left(\frac{-q\phi_B}{kT}\right)$ applying the natural log to both sides yields:

$$ln(I_0) = ln(AA^*T^2) - \frac{q\phi_B}{kT} \qquad 2.50$$

The parameter (n) in the diode current-voltage relationship; approaches 1 when carrier diffusion dominates current flow; approaches 2 when recombination current dominates.

2.5.8 The non-ideal Schottky diode

The discussion so far focused on the ideal space charge regions. However, real Schottky diodes exhibit wire resistances and non-ideal contacts [11]. In the following section the equivalent circuit of a non-ideal Schottky diode is given and the resulting current-voltage characteristics discussed.

The diagram shown in figure 2-15 is an equivalent circuit for a real Schottky diode. The series resistance R_S originates from the resistance of the wires connecting the device with the power supply and from the resistance of semiconductor bulk, which is a result of electron concentration and mobility and is strongly temperature dependent. Correspondingly, leakage currents due to imperfect metal contacts which lower the parallel resistance R_P were neglected in the ideal diode where R_P is infinitely high. If the capacitance of the Schottky diode is determined from phase shift and amplitude of the sinusoidal current driven by an AC voltage applied to the diode, it will appear to be temperature and frequency dependent [11].

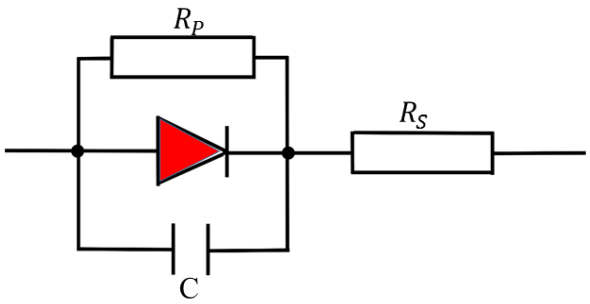

Figure 2-15: A sketch showing an equivalent circuit for a real Schottky diode redrawn from ref [11].

The graph in figure 2-16 shows the *I-V* characteristics of an ideal and a real diode. It can be seen that the ideal diode displays linear variation in the forward bias region, it is not affected by series resistance and there is low leakage current so parallel resistance is infinitely high. In the case of the real Schottky diode, the forward bias voltage is affected by series resistance to

the extent that the graph begins to plateau at about 0.3V and leakage current is high resulting in the lowering of the parallel resistance.

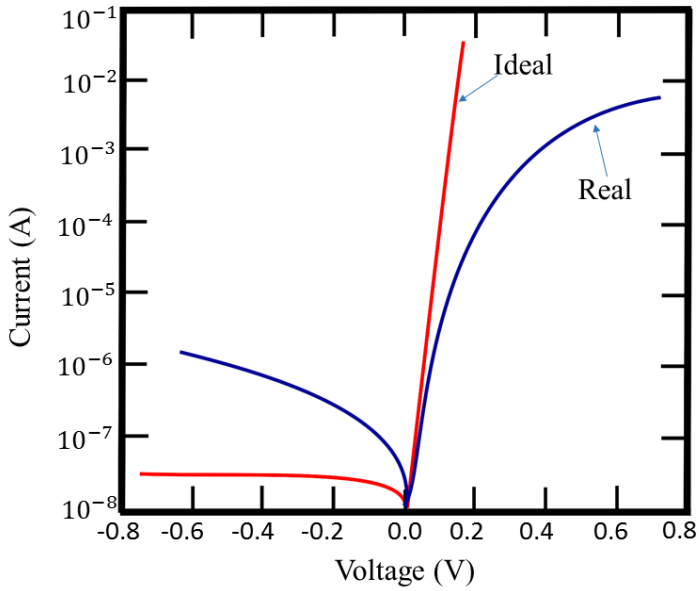

Figure 2-16: A semi-logarithmic I-V graph comparing an ideal Schottky with a non-ideal (real) Schottky.

The semiconductor surface contains surface states due to incomplete covalent bonds and other effects, which can lead to charges at the metal-semiconductor interface. Furthermore, the contact is seldom an atomically sharp discontinuity between the semiconductor crystal and the metal. There is typically a thin interfacial layer, which is neither semiconductor nor metal. For example, Si crystals are covered by a thin (10-20Å) oxide layer even after etching or cleaving in atmospheric conditions. Therefore, deposition of a metal on such a Si surface leaves a glassy interfacial layer at the junction. Although electrons can tunnel through this thin layer, it does affect the barrier to current transport through the junction. Because of surface states, the interfacial layer, microscopic clusters of metal-semiconductor phases, and other effects, it is difficult to fabricate junctions with barriers near the ideal values predicted from the work functions of the two isolated materials. Therefore, measured barrier heights are used in device design. In compound semiconductors the interfacial layer introduces states in the semiconductor band gap that pin the Fermi level at a fixed position, regardless of the metal used [4].

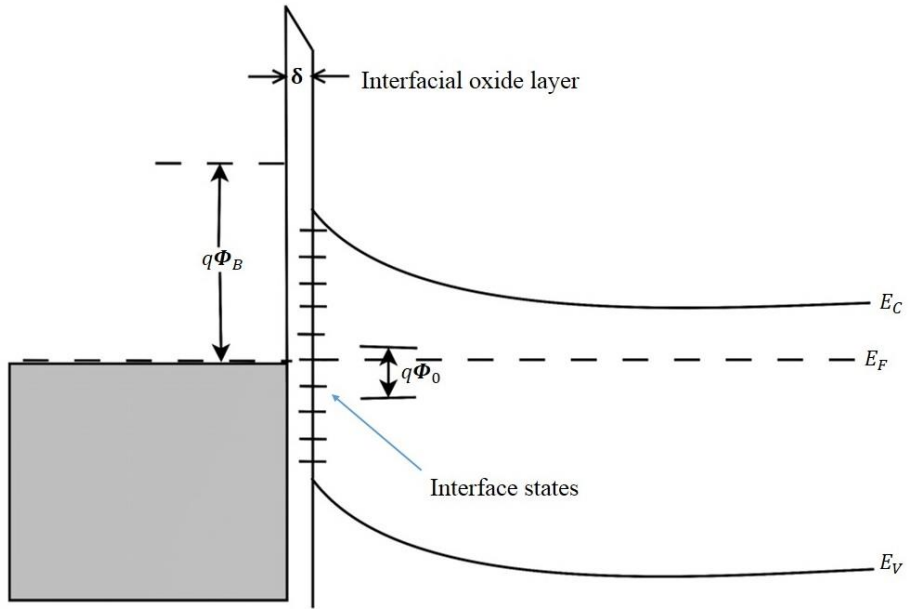

Figure 2-17: Energy band diagram in the presence of interface states.E_F shifts down relative to E_C at the interface and previously filled traps are emptied [4, 17].

For Si, good Schottky barriers are formed by various metals, such as gold (Au), palladium (Pd) or platinum (Pt). In the case of Pt, heat treatment results in a platinum silicide layer, which provides a reliable Schottky barrier with ϕ_B approximately 0.85 V on n-type Si. A full treatment of Schottky barrier diodes results in a forward current equation of the form

$$I = ABT^2 exp\left(^{-q\phi_B/kT}/_{nkT}\right) \qquad 2.51$$

where B is a constant containing parameters of the junction properties and n is a number between 1 and 2, similar to the ideality factor in equation 2.42 but arising from different reasons. The mathematics of this derivation is similar to that of thermionic emission, and the factor B corresponds to an effective Richardson constant in the thermionic problem [4].

Chapter 3

Silicon as a Semiconductor

3.1 Introduction

Si is the most widely used material in semiconductor devices. Its combination of low raw material cost, relatively simple processing, and a useful temperature range make it the best compromise among the various competing materials. Silicon used in semiconductor device manufacturing is fabricated into boules that are large in diameter to allow the production of wafers with a diameter of 30cm [3, 18, 19].

3.2 Crystallography

The atoms in crystalline materials are arranged in a periodic pattern. This pattern can be visualized as a number of parallelepipeds with atoms at the corners. These parallelepipeds, or unit cells, repeat themselves throughout the structure. There are seven different crystal systems; some of these have variants with extra atoms between the corner atoms so that 14 different atomic structures are possible [20]. Cubic crystals are characterized by unit cells with three equal lengths along three mutually perpendicular axes. The unit cell of a cubic crystal is described by the lattice constant, a, which is the length of a side of the cube.

Si, like other group IV insulators and semiconductors including diamond and germanium crystallizes in the diamond cubic lattice structure. Each Si atom has four bonds, one to each of its four nearest neighbours. This lattice structure can be constructed from two interpenetrating face-centred cubic lattices displaced from each other along the body diagonal by a distance equal to one-fourth of its length. Group III-V compounds and some II-VI compounds crystallize in a similar arrangement, called the zinc-blende lattice where two atom types form two interpenetrating face-centred cubic lattices.

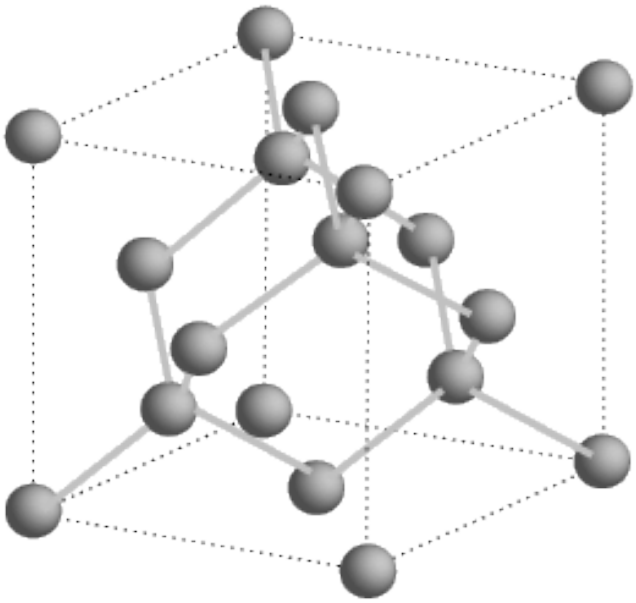

Figure 3-1: diamond crystal structure showing the tetrahedral arrangement of the Si atoms.

3.3 Silicon growth methods

The raw material for Si crystal is silicon dioxide (SiO_2). SiO_2 is reacted with C in the form of coke in an arc furnace at very high temperatures (approximately1800°C) to reduce SiO_2 to Si and CO. This forms metallurgical grade Si (MGS) which has impurities such as Fe, Al and heavy metals at levels of several hundred to several thousand parts per million (ppm). The MGS is refined further to yield semiconductor-grade or electronic- grade Si (EGS), in which the levels of impurities are reduced to parts per billion (ppb). This involves reacting the MGS with dry HC1 according to the following reaction to form trichlorosilane, $SiHCl_3$, which is a liquid with a boiling point of 32°C. By using fractional distillation pure $SiHCl_3$ can be separated from the impurities (for example $FeCl_3$). $SiHCl_3$ is then converted to highly pure EGS by reaction with H_2. Next, the high purity but still polycrystalline EGS is converted to single-crystal Si ingots or boules. This is generally done by a process commonly called the Czochralski method [4].

3.3.1 The Czochralski method

All Silicon wafers are grown from the Czochralski (CZ) method. This is achieved by melting polysilicon which is held just below 1417°C, and a single seed crystal is dipped in the melt and it starts the growth. The pull rate, melt temperature and rotation rate control the growth of the crystal. CZ crystal growth produces structurally perfect Si single crystals which are cut into wafers and polished. Starting wafers contain only dopants, and trace amounts of contaminants

Oxygen and Carbon in measurable quantities. Dopants can also be incorporated during crystal growth.

An alternative process is the Float Zone (FZ) process which can be used for refining or single crystal growth. In the float zone process, dopants and other impurities are rejected by the re-growing silicon crystal. Impurities tend to stay in the liquid and refining can be accomplished [4].

3.3.2 Epitaxial growth

One of the most important and versatile methods for growing crystals for device applications is the growth of a thin crystal layer on a wafer of a compatible crystal. The substrate crystal may be a wafer of the same material as the grown layer or a different material with a similar lattice structure. In this process the substrate serves as the seed crystal onto which the new crystalline material grows. The growing crystal layer maintains the crystal structure and orientation of the substrate. The technique of growing an oriented single-crystal layer on a substrate wafer is called epitaxial growth, or epitaxy. Epitaxial growth can be performed at temperatures considerably below the melting point of the substrate crystal. A variety of methods are used to provide the appropriate atoms to the surface of the growing layer. These methods include chemical vapour deposition (CVD), growth from a melt [liquid-phase epitaxy (LPE)] and evaporation of the elements in a vacuum [molecular beam epitaxy (MBE)]. With this wide range of epitaxial growth techniques, it is possible to grow a variety of crystals for device applications, having properties specifically designed for the electronic or optoelectronic device being made [4].

3.3.3 Oxygen contamination in silicon

Oxygen is the most important impurity found in Si. It is incorporated in silicon during the CZ growth process as a result of disintegration of the quartz crucible in which the molten silicon is contained. The oxygen is typically at a level of about $10^{18}/cm^3$. With time it has become possible to use a magnetic field during CZ growth to control thermal convection currents in the melt. This slows down the transport of oxygen from the crucible walls to the growing Si interface and reduces the oxygen concentration in the resulting crystal. Oxygen is always present at concentrations of approximately $5\times 10^{17} - 10^{18} cm^{-3}$in CZ Si. The oxygen can affect processes used in wafer fabrication such as impurity diffusion [4].

3.3.4 Carbon contamination in silicon

Carbon is normally present in CZ grown Si crystals at concentrations on the order of $10^{16}/cm^3$.The carbon comes from the graphite components in the crystal pulling machine. The melt contains Si and moderate concentrations of oxygen. This results in the formation of SiO that evaporates from the melt surface. Generally, the ambient in the crystal puller is Argon flowing at reduced pressure, and the SiO can be transported in the gas phase to the graphite crucible and other support fixtures. SiO reacts with graphite (carbon) to produce CO that again transports through the gas phase back to the melt. From the melt, the carbon is incorporated into the growing crystal [4].

3.4 Band structure of silicon

A Si atom has 14 electrons; these are distributed two each in the 1s and 2s states, six in 2p states and three each in the 3s and 3p states. When Si atoms are brought together to form a crystal, the discrete levels are broadened into bands so that all the electrons originally in a given energy state have energies slightly different from each other. Since there are so many atoms per unit volume, these bands may be regarded as continuous. In the crystal, the 3s and 3p states intermingle to form two bands separated by a large energy gap without energy states. There are four quantum states per atom in the lower band, called the valence band (E_V) and four quantum states in the upper band called the conduction band (E_C). The gap between these two bands is called the forbidden energy gap or simply, the band gap (E_g) [8].

As mentioned previously, each atomic site in Si is surrounded by four nearest neighbour sites which are found at points of a tetrahedron. The chemical bonds in Si are formed between nearest neighbours, each atom contributing one electron. As a result, each atom is surrounded by eight electrons, four of its own and one from each of its four neighbours. A configuration like this, which is similar to that of a noble gas, is very stable chemically. All of the available electrons have places in the valence bonds and none are free to move in the lattice unless some energy is applied to break the bond. For an electron to move, it must gain enough energy to be raised across the forbidden energy gap to an energy state in the conduction band. The energy required may be supplied from a photon of energy equal to or greater than the forbidden energy gap (a process known as photoconductivity) or thermal energy if the temperature is adequately high. As a result, electrons which leave the broken bonds go into the conduction band states and are free to move throughout the crystal lattice [8].

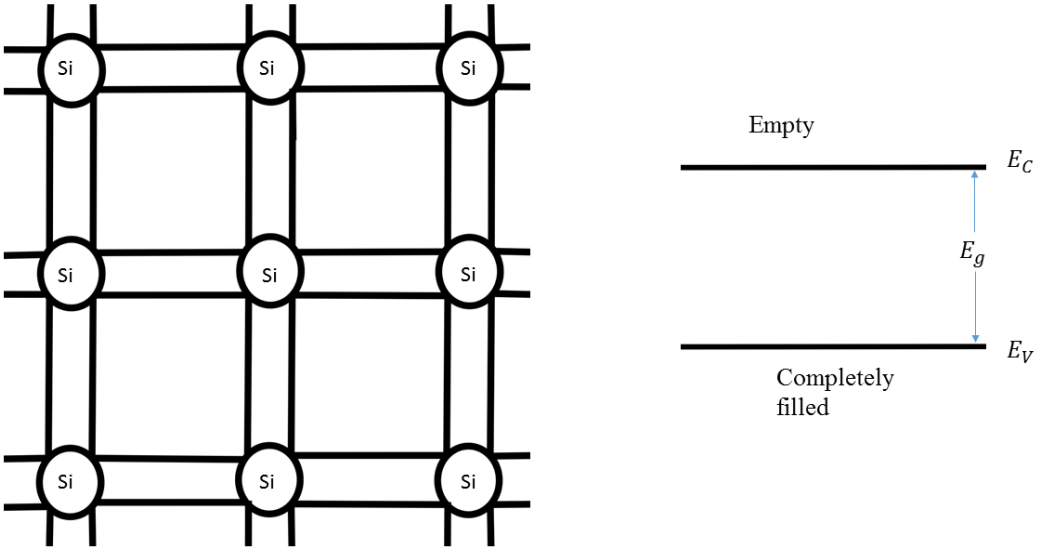

Figure 3-2: The energy band model of Si redrawn from ref [21].

The value of the band gap of silicon at room temperature and under normal pressure is 1.12eV [3].

3.4.1 Doping in silicon

Doping in semiconductor terminology is the addition of controlled amounts of specific impurity atoms with the intention of increasing either electron or hole concentration. Adding dopants in controlled quantities to semiconductor materials takes place routinely in the fabrication of almost all semiconductor devices. Frequently used dopants in silicon are listed in table 3-1.

Table 3-1: Common Si dopants. The elements written in red being the most frequently used dopants.

Donors (Group V elements: electron-increasing dopants)	Acceptors (Group III elements: hole-increasing dopants)
Phosphorous (P)	Boron (B)
Arsenic (As)	Gallium (Ga)
Antimony Sb)	Indium (In)
	Aluminium (Al)

Up to now, pure Si without impurities or defects has been considered, and it has been assumed that each lattice site is occupied by one and only one Si atom. Suppose now that a phosphorus atom is substituted for a Si atom as shown in figure 3-3.

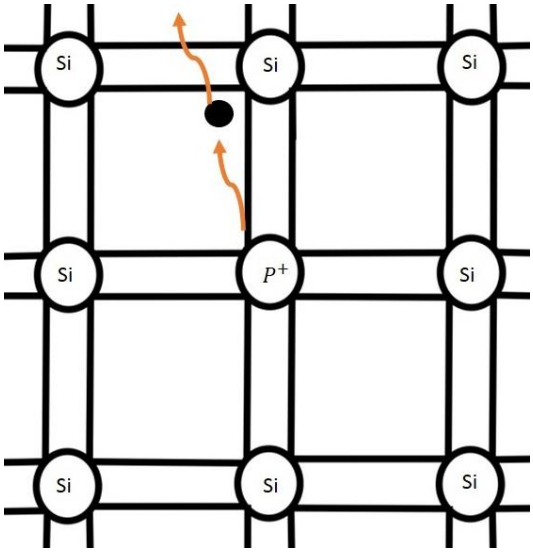

Figure 3-3: Visualisation of donor action of Phosphorus using the bonding model redrawn from ref [21].

Phosphorus is in the fifth column of the periodic table and has five valence electrons. Four of these electrons contribute to the valence bonds in the same way as the four valence electrons of the replaced Si atom. The fifth electron is not a part of the valence bond structure. It is attached to the phosphorus atom only by the electrostatic attraction of the positive charge of the nucleus. The energy required to release this electron is much smaller than that required to break a valence bond. Because one of its electrons can easily be released to move about in the crystal, phosphorus is known as a donor impurity. In an energy band diagram, the phosphorus atom is represented by an energy level in the forbidden gap very close to the bottom of the conduction band. The energy difference between this level and the bottom of the conduction band is the energy required to free the electron from the phosphorus atom; this energy is known as the donor activation energy. Because mobile electrons have a negative charge, Si containing phosphorus or another group V impurity is called n-type [8].

If a Si atom is replaced by a boron atom, or another atom from column 3 of the periodic table, the impurity atom contributes only three valence electrons. These three electrons form valence bonds with three of the neighbouring silicon atoms. In the fourth bond there is a missing electron, or hole. An electron from a neighbouring bond may move into this hole with very little spending of energy, leaving a hole behind, as shown in Figure 3-4.

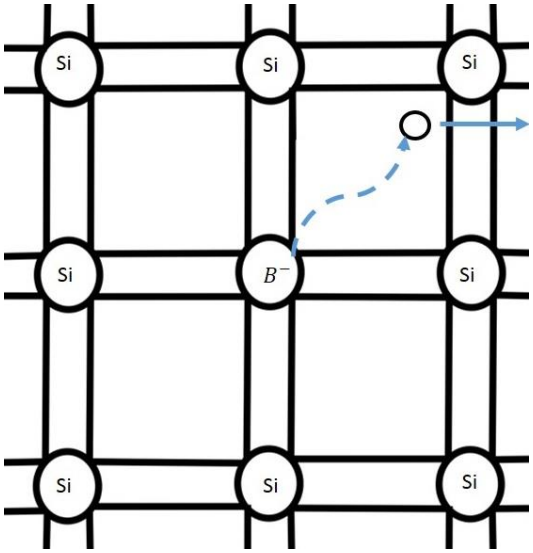

Figure 3-4:Visualisation of acceptor action of Boron using the bonding model redrawn from ref [21].

3.5 Silicides

Metal silicides as intermetallic compounds between metals and Si have been used as electrical contacts in Si integrated circuits (SIC) since the beginning of the 20th century. This is due to their low electrical resistivities, good thermal stability and compatibility with Si processing technology. These properties have made them good materials for use in electronics, photovoltaics and thermoelectrics [22, 23]. An example with important implications in nowadays microelectronic industry is the reaction between an ultrathin metal layer and Si to form low-resistive materials to be used as metal gates [24].

3.5.1 Silicide formation overview

The interface between a transition metal and silicon is highly reactive. Freeouf *et al* and Ho *et al* found that palladium reacts spontaneously with Si upon deposition to form a Pd_2Si-like compound at room temperature with the thickness of palladium being about 10-15Å [25]. The formation of silicides can be divided into two fundamental metal reaction methods. The first method relies on the reaction between an elemental metal film and underlying Si (i.e. the diffusion couple reaction). This method is discussed in this work. The second method involves the (simultaneous) co-deposition of metal and Si atoms and is frequently achieved by co-sputtering the two elements. This approach results in a layer covering the complete surface of

a wafer (a 'blanket' deposition) which must be subsequently patterned for use [22]. This method is not discussed in this work.

To form a silicide by the diffusion couple method, the metal (M) is first deposited on a Si wafer. The substrate is then annealed to promote diffusion of one or both of the atomic species across the metal/Si interface. In most cases, a thin film of silicide is, in such a way, formed at the interface. Further annealing leads to a thickening of this interfacial silicide which ultimately consumes the complete metal layer. The growth process can be characterized by recording the thickness of the formed interfacial silicide at a particular annealing temperature and time. In this work the Rutherford Backscattering technique was used to monitor the growth of the silicide layer. By noting the thickness of silicide formed as a function of the annealing time, conclusions were drawn from the results obtained.

3.5.2 Growth kinetics of silicides

Kinetic data are crucial for a basic understanding of interfacial reactions between metal thin films and silicon. Most silicides are formed at a temperature far lower than the eutectic temperature. The growth is often diffusion controlled or interface-reaction controlled. The thickness of the silicide is proportional to the square root of time t and t, respectively. The presence of contaminating or doping impurities was found to influence the growth rate [26]. Cross-section transmission electron microscopy (XTEM) has been demonstrated to provide direct and accurate kinetic data, such as the sequence of phase formation, the dependence of the phase growth, and morphology of phase and interface structure in the growth of silicides on silicon [27].

In the silicide formation, metal atoms diffuse across the metal/silicide interface, Si atoms diffuse across the silicide/silicon interface, or both. In order to determine the dominant diffusing species, it is common to introduce an inert marker. In thin film reactions, the markers are usually tens of nanometres in size and should not influence the growth kinetics of silicide formation. Ideally, the markers should be inert and remain immobile as the diffusing species streams by. An additional constraint is that the marker should be located in the silicide layer to avoid possible influence due to the presence of the interface [28].

From the marker experiments, it was revealed for metal-rich silicides such as M_2Si, the dominant diffusing species are mostly metal atoms. On the other hand, in the formation of monosilicide and disilicide, silicon atoms are generally the dominant diffusing species. However, there are exceptions [26].

3.5.3 Palladium silicides

The use of palladium silicides in Si device technology in the 1970s provided a boost in the investigation of crystallography, electrical properties and growth kinetics of thin film Pd_2Si on bulk Si substrates. The phase structures of PtSi, Pd_2Si, Pd_3Si, Pd_4Si and Pd_5Si have been studied in considerable detail [29]. Over the years, most investigators have come to the conclusion that Pd_2Si is the primary phase formed during the palladium-silicon reaction. Pd_2Si is thermally stable compared to the other phases and this was found to be dependent on the annealing ambient [30].

Table 3-2: the information on formation temperature and temperature range of the Pd_2Si phase.

Substrate	Formation Temperature Range (°C)	Time Range (minutes)	Reference
Si (111)	150-175	0-800	[31]
Si (111) Phosphorus doped $(\mathbf{4.5 \times 10^{14} cm^{-3}})$	200-250	0-300	[32]
Si (111) Arsenic doped $(\mathbf{5 \times 10^{20} cm^{-3}})$	200-250	0-300	[32]
Si (111)	190-300	0-140	[33]

3.5.4 Platinum silicides

The platinum-silicide system was one of the first silicides mentioned in the application of Schottky barrier diodes. It is ideal for illustrating silicide formation due to its high barrier height [34]. Pt-Si intermixed layers can present distinct types of composition: PtSi, Pt_2Si and Pt_3Si but only the first two are stable. Studies have shown that platinum silicidation is a two-step process. In the first reaction Pt diffuses into Si to form the intermediate compound Pt_2Si and in the second reaction Si diffuses into Pt_2Si to form a stable PtSi layer. These two reactions occur sequentially [35].

Table 3-3: the information on formation temperature and temperature range of the Pt_2Si phase.

Substrate	Formation temperature range (°C)	Time range (minutes)	Reference
Si	200-600°C	0-10	[34]
p-type Si(100)	100-300°C	0-2	[35]

3.6 Defects in silicon

The study of defects in any material must include the understanding of the properties of the intrinsic vacancy and interstitial. On the basis of thermodynamic evidence, such defects will be present in all crystals once they have solidified and a primary requirement is to determine their equilibrium concentrations as a function of temperature. It is known that the defects are extremely mobile in silicon and they are lost to sinks on cooling, so that quenching experiments are not very valuable in determining concentrations [36].

There are two primary native defects in Si; the lattice vacancy and the Si interstitial. Each defect is present in thermodynamic equilibrium at any specific temperature limit T, its concentration being proportional to $\exp(-W/kT)$, where W is its formation energy. At high temperatures, consequently, each provides a mechanism for normal thermally activated diffusion of the substitutional host and impurity atoms. In addition, non-equilibrium conditions produced during device processing such as metallisation and ion implantation damage can serve to provide a temporary release of these defects, which, in turn, can cause anomalous transient enhanced diffusion phenomena [37].

Furthermore , these defects, whether isolated or compounded with other defects or impurities, represent a disruption of the normal bonding structure of the lattice, and therefore can introduce electrically active levels into the forbidden gap. They therefore directly affect the electrical properties of the material. This also means that the defects can take on several charge states, each potentially with a different structural arrangement in the lattice, different diffusional properties, different interactions with other defects, etc. Determining, therefore, their electronic and physical properties, and the relationship of these to their local structural arrangements in the lattice, is essential to understanding their role in silicon device technology [37].

3.6.1 Primary Defects

There are two main groups of semiconductor defects; point defects and extended defects. Point defects are not extended in space in any dimension and this means that the disturbance of the lattice is localised about a lattice site and involves only a few nearest neighbours. There are two kinds of point defects of interest in semiconductor crystals, these are: intrinsic (e.g. vacancies and self-interstitials) and extrinsic point defects (e.g. impurity atoms occupying substitutional or interstitial lattice sites). Extended defects are extended in nature (for example, grain boundaries, dislocations and stacking faults) [10]. This work focuses more on the point defects.

The vacancy defect

If an atom is removed from its regular lattice position, the empty lattice is called a vacancy defect (V). The vacancy in some semiconductors (e.g. in Si) can have up to five charge states: V^{++} ,V^{+},V^{0},V^{-} and V^{--} (which represent the number of electrons occupying the dangling bonds) [38]. When a vacancy is formed, four bonds are broken in the diamond crystal structure as shown if figure 3-5. The broken bonds can form new bonds depending on the charge state of the vacancy. This causes small inward and outward displacement of neighbouring atoms, which either maintains or transforms the crystal's local symmetry [10].

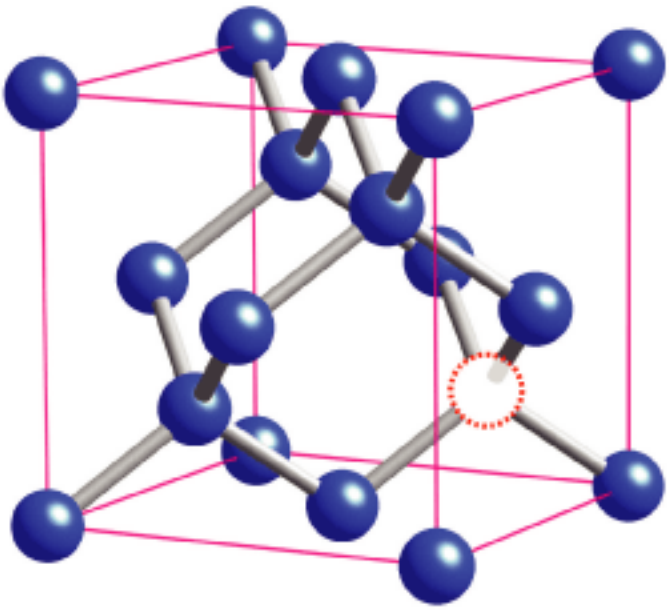

Figure 3-5: the vacancy defect in a diamond structure of a Si crystal.

Interstitial defect

An interstitial defect is caused by an atom occupying a site in the crystal structure which is not its regular position as shown in figure 3-6. It can be an atom of the same species as those in the lattice (self-interstitial) or of a different species (interstitial impurity).The energy of formation of an interstitial defect is higher than that of the vacancy. The introduction of an interstitial results in a large lattice stain due to the relaxation and distortion of the lattice surrounding it [10].

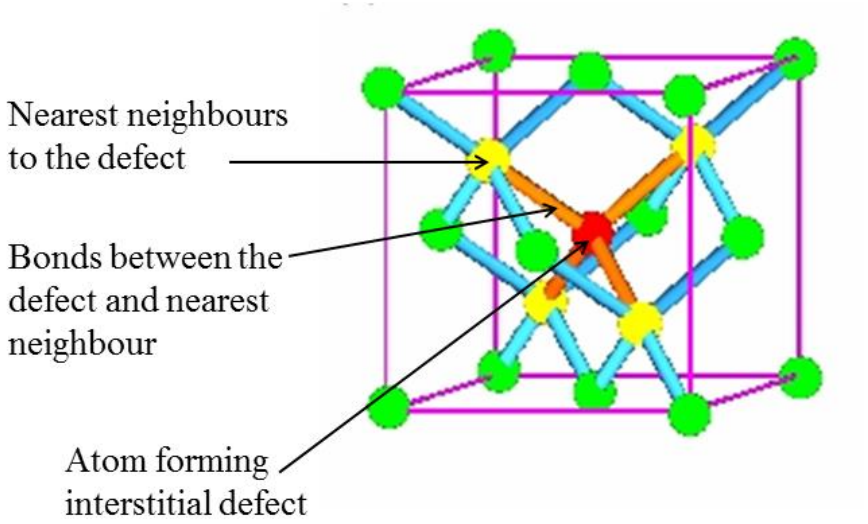

Figure 3-6:The self-interstitial defect in silicon [39].

If an atom leaves its site in the lattice (thereby creating a vacancy) and then moves to the surface of the crystal, then it becomes a 'Schottky' defect. On the other hand, an atom that vacates its position in the lattice and transfers to an interstitial position in the crystal is known as a 'Frenkel' defect. The formation of a Frenkel defect therefore produces two defects within the lattice - a vacancy and the interstitial defect this is also known as a Frenkel pair.

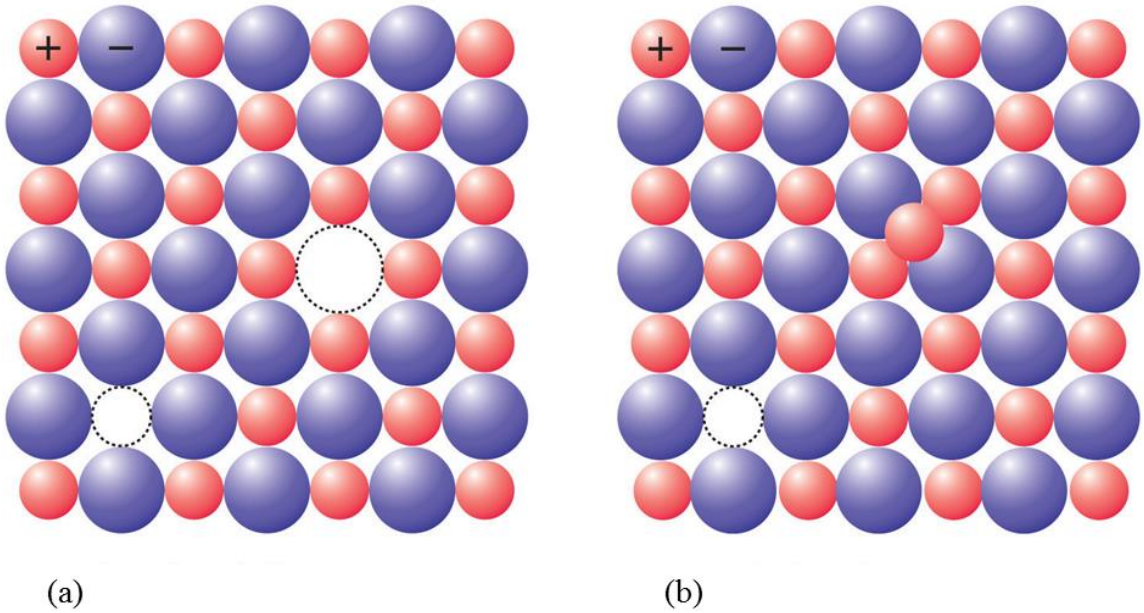

Figure 3-7: The(a) Schottky defect and (b) the Frenkel defect.

3.6.2 Secondary defects

The isolated lattice vacancy (V) and self- interstitial (I) are primary defects produced after high-energy particle irradiation in semiconductors. The primary defects are mobile at low temperatures for example in Si, the vacancy becomes mobile above 150K and 4.2K for the interstitial [40]. The V and I which survive recombination of simple defects can diffuse into the semiconductor and interact with other intrinsic and extrinsic defects resulting in the formation of complex room temperature stable defects. In Si when a vacancy becomes mobile, it can be trapped by an oxygen atom to form a complex, V-O (A-centre) or a doping impurity like phosphorus P, to form the complex V-P (E-centre), or by another vacancy to form a divacancy [10].

The E-centre

The defect known as the E-centre is described as a vacancy trapped next to a substitutional donor atom. The E-centre can be formed as a primary defect or when the impurity atom captures a mobile vacancy [41]. Taking into consideration the E-centre in phosphorous doped Si, in the neutral charge state two of the three Si atoms surrounding the vacancy pull together to form an electron pair leaving an unpaired electron in the orbital of the third Si atom, while two electrons with antiparallel spins are accommodated by the phosphorous atom. When the Fermi level is above the E-centre an extra electron is accepted and becomes negatively charged, PV^-. The formation of E-centre in Si removes two electrons in the conduction band by converting a positively charged P donor atom to a negatively charged V-P centre. The

formation of the E-centre is regarded as an intermediate step in dopant diffusion in both Si and Ge [10, 42].

The A-centre

The A-centre (V-O) can be regarded as a vacancy trapped next to an oxygen atom in an interstitial position. Similar to the E-centre, the A-centre can be formed as a primary defect or when an oxygen impurity traps a mobile vacancy. The A- centre competes for vacancies the E-centre and its concentration is dependent on the relative O impurity concentration in the sample. The A-centre has also been found to be an efficient recombination centre and therefore can be used to control minority carrier lifetimes in Si for fast switching device application [10, 43].

Table 3-3: shows well-known complexes in silicon, and an overview of the levels they induce in the band gap.

Defect	$\mathbf{E_T(eV)}$	$\boldsymbol{\sigma_a(cm^2)}$	**Reference**
$\mathbf{V}\ (=/-)$	+0.23	7.00×10^{-16}	[38]
$\mathbf{V}\ (-/\mathbf{0})$	-0.42	2.10×10^{-15}	[38]
$\mathbf{V}\ (\mathbf{0}/+)$	+0.20	8.00×10^{-16}	[38]
VO	-0.17	1.44×10^{-14}	[38]
$\mathbf{C_i}(-/\mathbf{0})$	-0.11	5.9×10^{-15}	[38]
$\mathbf{C_i}\ (\mathbf{0}/+)$	+0.27	1.11×10^{-15}	[38]
$\mathbf{C_iO_i}(+/\mathbf{0})$	+0.36	3.5×10^{-15}	[44]
$\mathbf{C_iO_i^*}(+/\mathbf{0})$	+0.34	4.2×10^{-15}	[44]
$\mathbf{C_iC_s}(-/\mathbf{0})$	-0.17	1.44×10^{-14}	[38, 45]
$\mathbf{C_iC_s}(+/\mathbf{0})$	+0.09	5.26×10^{-14}	[38, 45]
$\mathbf{C_iC_s}(-/\mathbf{0})$	-0.11	3.00×10^{-15}	[38, 45]
$\mathbf{B_i}(\mathbf{0}/+)$	-0.13		[45]
$\mathbf{B_i}(-/\mathbf{0})$	-0.45		[45]
$\mathbf{B_iO_i}$	-0.26		[45]
$\mathbf{B_iC_s}$	+0.29		[45]
$\mathbf{B_iB_s}$	+0.30		[45]
VP	-0.44		[45]

3.6.3 Radiation-induced defects in silicon

The irradiation of semiconductors has been studied for many years with the target of understanding the structure of defects introduced during irradiation and the effects of radiation-induced defects on semiconductor properties. These studies have assisted in the development of semiconductor materials [6].

During irradiation or ion implantation of Si, large amounts of Frenkel pairs (vacancy-interstitial pairs) are generated. These simple point defects are not stable at room temperature and they quickly either annihilate or develop into more stable point defect complexes [46].During and after implantation, oxygen complexes like the A-centre may be formed. The interstitial-carbon-interstitial-oxygen pair (C_iO_i) is also formed when interstitial oxygen O_i captures an interstitial carbon C_i which in turn is generated when implantation-induced interstitials react with the substitutional carbon C_s [45, 47-50].

When dopant atoms like phosphorous or boron build defect complexes, they no longer function as dopants. For example, in n-type Si, where group five elements (donors) are known to trap mono-vacancies and form what are known as the E-centres [51, 52]. In p-type Si the typical acceptor (substitutional boron B_s) is immobile at room temperature and has a shallow level just above the valance band edge. Then again, implantation may introduce boron related defects with deeper levels for example, the interstitial boron(B_i) , boron impurity pairs or boron interstitial clusters [53-56].

Chapter 4

Experimental Techniques

4.1 Introduction

In this chapter the experimental techniques used for sample preparation, contact fabrication, electrical characterisation, composition and surface analysis are described. The Schottky contact electrical characterization methods include: current-voltage *(I-V)*, capacitance-voltage *(C-V)* and deep level transient spectroscopy (DLTS). Compositional and surface analysis were carried out using Rutherford backscattering spectroscopy (RBS) and scanning electron microscopy (SEM) respectively.

4.2 Sample preparation

Before metallisation, Si is cut and cleaned using a chemical cleaning process to remove organic materials such as oils, waxes and fingerprints, ionic substances such as sodium and potassium, and trace metals [8]. Immediately after cleaning metallization follows to prevent further oxidation of the silicon surface.

4.2.1 Silicon wafer cleaning procedure

The cleaning steps were used sequentially as follows:

(1) A three step degrease for the removal of dust particles and grease using:

- Trichloroethylene (TCE)
- Isopropanol
- Methanol

Samples were placed in an ultrasonic bath for 5 minutes for each degreasing step.

(2) The samples were then etched in dilute 40% Hydrofluoric acid (HF) for 1 minute. This is done to remove the native oxide SiO_2.

(3) The samples were then blow dried using Nitrogen gas.

4.2.2 Ohmic contact fabrication

Immediately after the chemical cleaning procedure, ohmic contacts were fabricated on n-type material. This was done by resistively depositing a 100nm thick layer of Au-Sb (4% Sb) on the back surface of the sample after evacuating the chamber to 2×10^{-5} milibar. The ohmic contact was then annealed at 370°C for 10 minutes in Argon gas. This annealing step helps to optimise the ohmic contact by lowering the barrier height hence reducing its resistivity [57]. The resistive deposition system is shown in figure 4-1. In this technique, a current flows through the crucible containing the metal to be deposited until the metal reaches its melting point. The metal then evaporates and deposits on the sample mounted above the crucible. The deposition rate is monitored by a crystal monitor and controlled by adjusting the current until the desired deposition rate is reached. The resistive deposition method is used for metals with low melting points that is, below 1600°C. Metals which can be deposited using this method include gold, aluminium, palladium, nickel and silver.

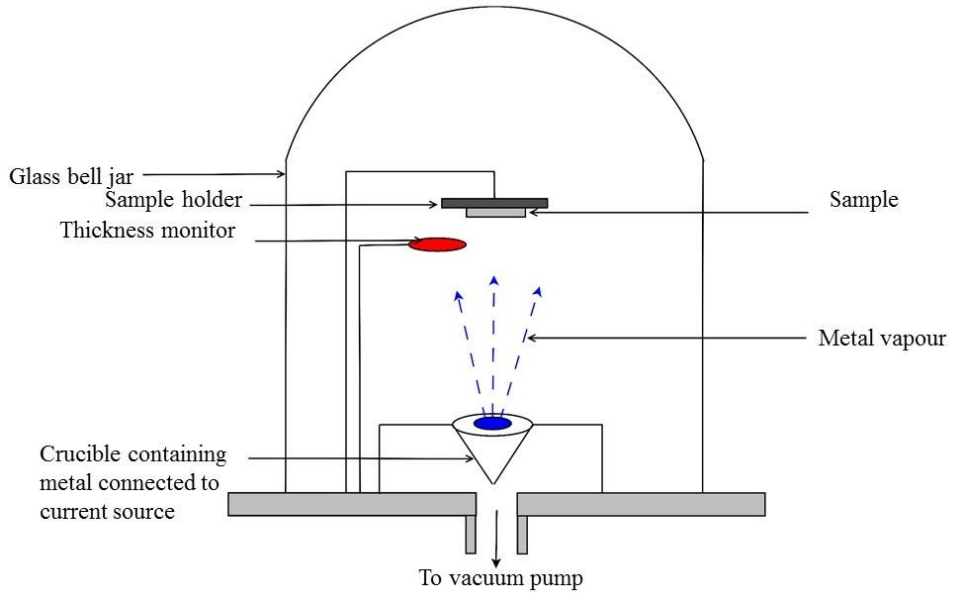

Figure 4-1: Schematic of the resistive deposition system set up at the University of Pretoria.

For p-type material, indium-gallium eutectic was used as the ohmic contact. This was achieved by painting the back of the sample using the eutectic.

4.2.3 Schottky contact fabrication

Schottky contacts with a thickness of 100nm were fabricated on Si wafers by evaporating Palladium on the polished side through a mask with circular holes 0.60 mm in diameter. The contacts were deposited using electron beam deposition. In this technique a hot filament discharges electrons which are then accelerated by electric and magnetic fields, onto the crucible containing the metal to be deposited. As a result, the metal melts and evaporates and deposits onto the sample. The deposition rate is controlled by the filament current. The EBD system can be used to deposit any metal but it may introduce defects on or below the surface of the sample on which the contacts are made. After metallisation the sample electrical characterisation techniques are carried out on it.

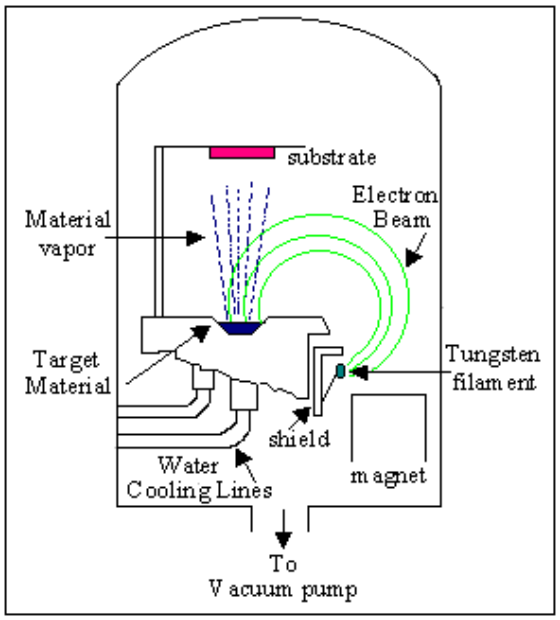

Figure 4-2: A schematic diagram of the electron beam deposition system.

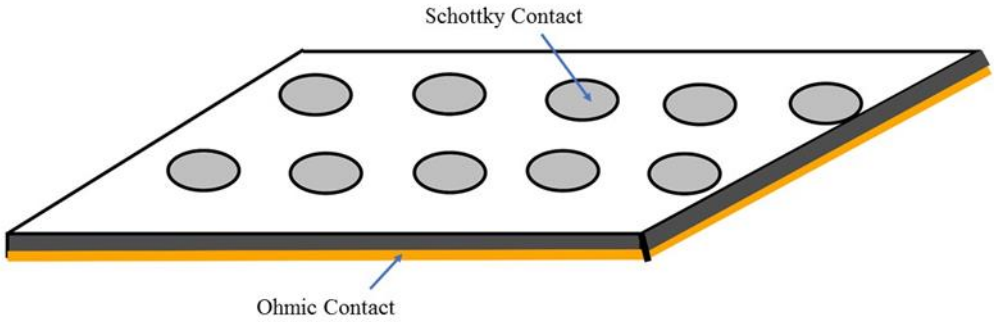

Figure 4-3: A schematic diagram showing Schottky and ohmic contacts on Si.

4.2.4 Sample irradiation

Contacts fabricated on the p-type Si samples were irradiated with alpha particles using the Americium241 foil at room temperature. Alpha particle irradiation was achieved by making use of a 5.4 MeV Am-241 radioactive source with a fluence rate of $7 \times 10^{6}\text{cm}^{-2}$. The sample was irradiated for 30 minutes at first. The fluence was $6.4 \times 10^{9}\text{cm}^{-2}$. *I-V C-V* measurements and DLTS were done after each irradiation.

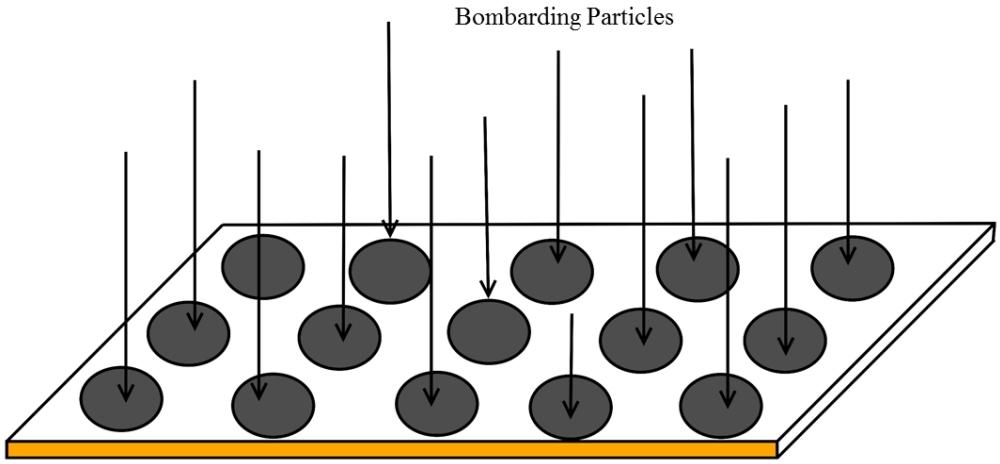

Figure 4-4: A diagram showing alpha-particle radiation on a silicon sample.

4.2.5 Electron beam exposure (EBE)

The main aim of developing the EBE technique was to see if EBD induced defects can be introduced in a controlled way. Excessive exposure (time and beam current) would reduce the usefulness of diodes for further study thus putting a limit on how much damage could be introduced. Energetic particles that cause EBD damage are present during EBE but interact directly with the semiconductor whereas during EBD this interaction mostly occurs via the metal used as a contact [58].

Vacuum pumping was carried out by a dry pump in series with a turbo molecular pump and to lower the H_2 concentration. Tungsten (W) was evaporated in the chamber with the sample rotated away from the evaporation source. While the pre-deposition vacuum was typically 5×10^{-7} mbar, this soon went up to approximately 3×10^{-6} mbar during the evaporation. As the vacuum conditions vary greatly during EBD, forming gas H15 with a composition of N_2:H_2 of 85%:15% by volume was also used to raise the pressure in the vacuum chamber to 10^{-4}mbar and kept constant during processing of select samples. EBE of samples and EBD of contacts were fabricated using a 10 kV source (MDC model e-Vap 10CVS) with the samples positioned 50cm above the crucible [2].

During EBE, without metal deposition, the samples were exposed for 50 minutes; while the beam heated a tungsten source using a beam current of 100 mA, this current being insufficient to evaporate tungsten, thus exposing the samples to EB conditions comparable to those experienced during deposition. Gold and nickel diodes were used for all the other samples prepared for this study as it can be evaporated resistively, a process that is known to not introduce defects in concentrations measurable by deep level transient spectroscopy (DLTS) [2].

4.3 Electrical characterisation techniques

Current-voltage *(I-V)* and capacitance-voltage *(C-V)* measurements were conducted on the samples to monitor the quality and electrical characteristics of the diodes while annealing of the samples was carried out. Deep level transient spectroscopy (DLTS) was used to characterise the defects in the semiconductor band gap after annealing, irradiation and electron beam exposure.

4.3.1 Current-voltage measurement set-up

The *(I-V)* measurement technique is ideal for checking the quality of the Schottky contacts on each sample after preparation. Measuring the current that flows through the contact under forward and reverse bias conditions enables the deduction of whether a contact is a good rectifier or it is ohmic. The properties of diodes that are extracted from (*I-V*) measurements are; series resistanceR_s, ideality factor *n*, reverse leakage current I_R(measured at -1V reverse bias) and barrier height Φ_B. These diode properties determine whether the sample can be used for DLTS measurements. A good diode suitable for DLTS measurements should have a high barrier height, low leakage current (less than 10^{-4}A) and a low series resistance (less than 200Ω) [10]. The (*I-V*) characteristics were measured using an HP 4140B pA meter/DC voltage source with a current limit of 10^{-14}A.

4.3.2 Capacitance-voltage measurement set-up

The (*C-V*) technique is used to deduce important parameters of the contact which include; the barrier height, built-in-voltage, and free carrier concentration. The (*C-V*) characteristics of the contacts are determined using an HP 4192A LF impedance analyser. The (*I-V*) and (*C-V*) contacts were carried out in the dark. A schematic diagram of the (*I-V*) and (*C-V*) measurement set up is shown in figure 4-5.

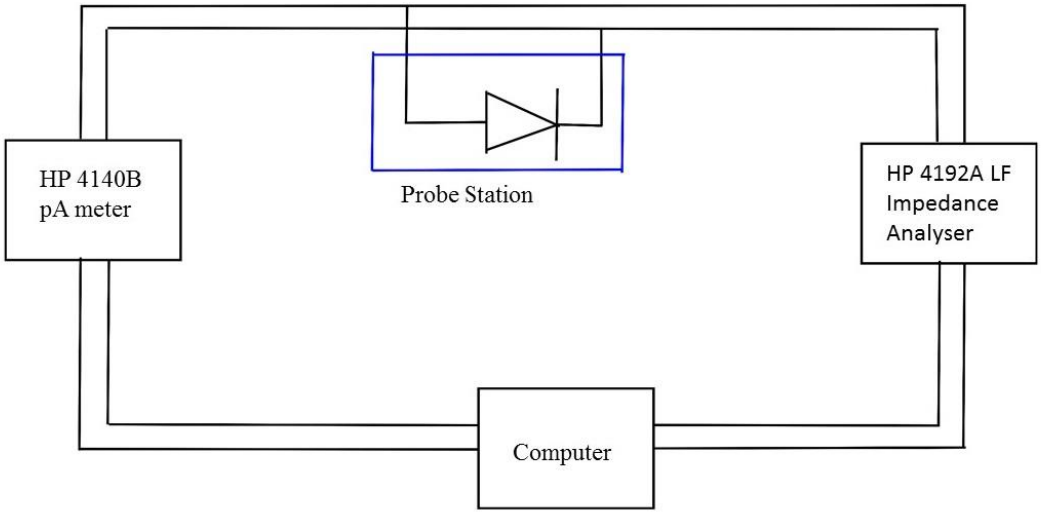

Figure 4-5: A block diagram of (I-V) and (C-V) station set up at the University of Pretoria.

4.3.3 Deep level transient spectroscopy concepts and measurement set-up

Introduction

Deep level transient spectroscopy (DLTS) is a unique and powerful tool used for the study of electrically active point defects in semiconductor materials. DLTS measures the electrical effects of defect states in the depletion region of a p-n junction or a metal-semiconductor junction [59, 60]. In DLTS a defect is observed by monitoring the effect of emission of a carrier from a deep level to the corresponding band edge in the depletion region of a reversed biased semiconductor junction. A lattice defect, such as a vacancy, interstitial, or a dislocation; or an impurity, either substitutional or interstitial; or a complex of these simple defects in the semiconductor material introduces an electronic energy state into the band gap of the semiconductor. Intentionally processed dopants produce shallow states within the energy gap and control the majority carrier concentration in the material. The deep states measured in this spectroscopy are those whose energy levels fall deeper in the bandgap than the dopant levels. The deep levels in silicon produce a spectral peak within the temperature range of 40 to 350 K for typical DLTS measurements systems .In n-type samples, the observed defects will emit electrons to the conduction band and will lie above the middle of the gap [59].

4.3.4 Deep level transient spectroscopy (DLTS)

By making use of DLTS, defects in semiconductors are analysed by probing the space charge region which exists in both a p-n junction and a Schottky barrier. The width, W, of the depletion region of a SBD or p-n junction varies with applied voltage according to:

$$W = \sqrt{\frac{2\varepsilon(V_{bi} + V)}{qN}} \qquad 4.1$$

Where $\varepsilon =$ dielectric constant of the depleted semiconductor

$V_{bi} =$ built-in-voltage of the junction

$V =$ externally applied voltage

$q =$ charge on the electron

$N =$ density of ionised impurities due to the dopants and other imperfections.

The junction capacitance due to the depletion layer is:

$$C = \frac{\varepsilon A}{W} = A\sqrt{\frac{q\varepsilon N}{2(V_{bi} + V)}} \qquad 4.2$$

Where A= area of the junction.

From equations 4.1 and 4.2 it can be seen that if N changes in the depletion region, W and C will also change, and so junction capacitance is a direct measure of the total charge. If the concentration of electrons or holes trapped at deep levels is changed by the thermal or optical emission of carriers to the conduction or valence bands, this change can be monitored by measuring the variation in junction capacitance at constant applied voltage. The variation in the temperature dependant variation of N forms the basis of capacitance-based DLTS [7, 61] The processes of carrier capture and emission are shown in figure 4-6 for a Schottky barrier diode having an electron trap in the upper half of the bandgap. In equilibrium, when a defect level is below the Fermi level, it is filled with electrons, whereas it is empty when above the Fermi level.

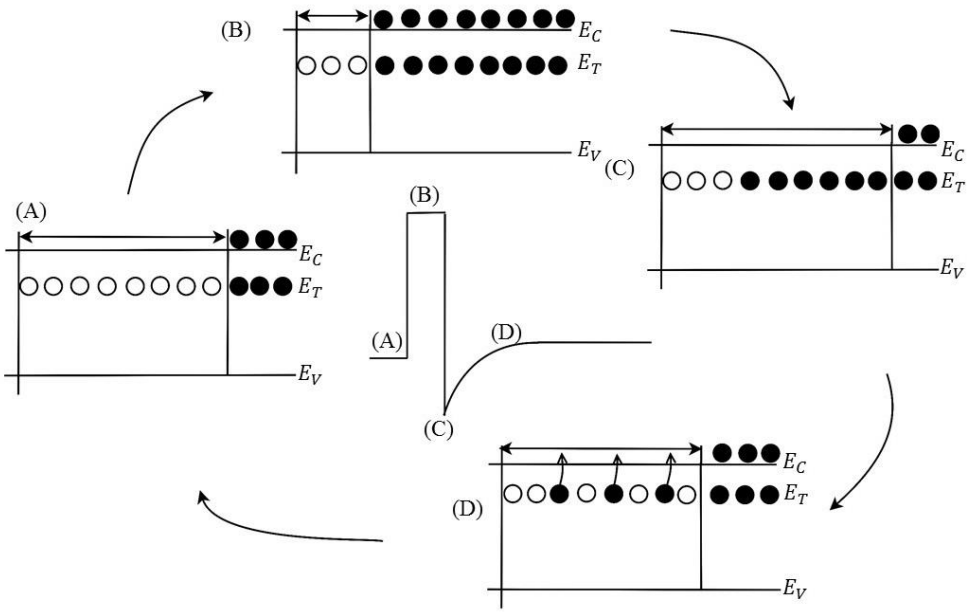

Figure 4-6: The variation of the depletion region width and capacitance after the application of a voltage bias and filling pulse sequence for an electron trap in an n-type semiconductor [10].

Before applying a reverse voltage, the traps in the depletion region above the Fermi level are empty as shown in (A). Reducing the applied voltage to $V - V_P$ reduces the width of the depletion region, allowing electrons to be trapped as deep levels, as depicted in (B). Electron capture into an initially empty trap is given by

$$N(t) = N_T[1 - exp(-c_n t)] \qquad 4.3$$

Where $N_T =$ trap density

and $c_n =$ capture rate.

Part (C) shows the point when the voltage is returned to is steady-state value, V, where the filled traps lie within the depletion region. When electrons are emitted into the conduction band by the traps, where they are immediately swept away by the junction electrical field, this is observed as a majority carrier capacitance transient as shown in (D).

Using the experimental approach, the electron emission can be determined from the time dependence capacitance transient. The density of the occupied traps at time t after removing the pulse is:

$$N(t) = N_T exp(-e_n t) \qquad 4.4$$

Where e_n is the thermal emission and N_T is the trap concentration. From equations 3.4 and 3.12 it can be shown that change in trap population gives rise to a corresponding diode capacitance which is dependent on time. Furthermore, if $N_T \ll N_D$, it can be expressed as:

$$C(t) = C_O - \Delta C_O exp(-e_n t) \qquad 4.5$$

Where $C_O$the equilibrium is reverse bias capacitance and ΔC_O is the change in capacitance after the immediate removal of the filling pulse.

The method for obtaining the energy level, E_T and capture cross-section σ_n, of a defect is to extract e_n from the transient $C(t)$, in equation 3.13 at several temperatures and the use equation 3.4 to obtain E_T and σ_n REF

4.3.5 The concepts of DLTS

DLTS is a highly sensitive capacitance technique with good transient response. It is a technique that is capable of clarifying different traps from each other. DLTS is also capable of setting an emission rate window which the measurement apparatus responds to when it sees a transient whose rate falls within its window. While temperature scanning takes place, taking into consideration that the thermal emission process is strongly temperature dependant, the peak positions of observed spectra shift to higher positions for higher emission rates and lower positions for lower emission rates thereby allowing a distinct determination of those positions by using the rate window thermal scans. DLTS uses the boxcar method for accurate determination of the emission rate window and signal averaging, therefore improving the signal to noise ratio [60]. Figure 4-6 shows how the double boxcar method works.

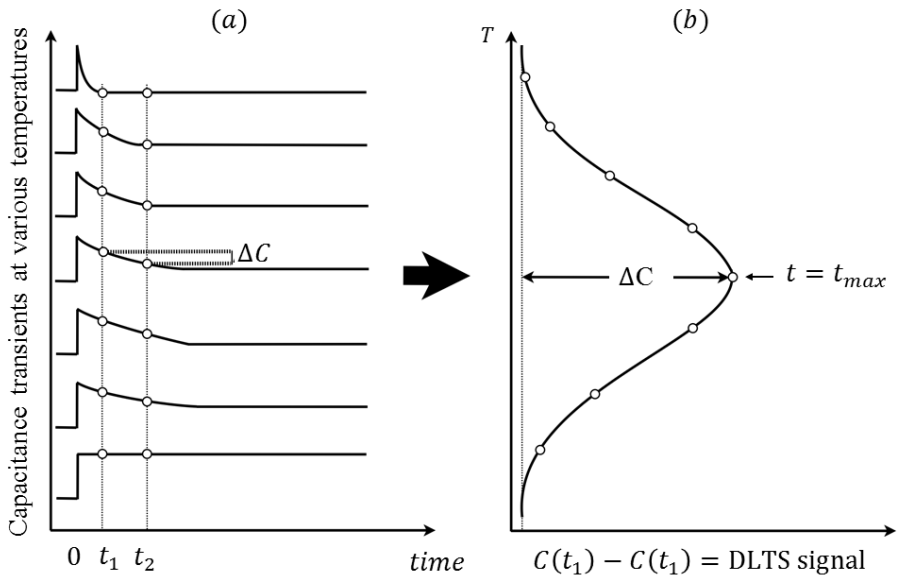

Figure 4-7: A schematic diagram showing (a) the change in the shape of the DLTS transient with increasing temperature and (b) the DLTS signal obtained from the transients as a function of sample temperature.

The transient figures shown in figure 4-7 (a) are fed through the double boxcar with pre-set times, t_1 and t_2. The average difference between the capacitances at t_1, C(t_1) and at t_2,C(t_2) are plotted as a function if temperature as shown in figure 4-7(b). The rate window for the thermal scan is determined by t_1 and t_2. The peak is formed when the decay constant $\boldsymbol{\tau}$ falls within the order of $t_2 - t_1$. The value of $\boldsymbol{\tau}$ at the maximum of the $C(t_2) - C(t_1)$ vs T for a particular trap, τ_{max} can be related to the gate positions t_1 and t_2. This is achieved by normalising the DLTS signal in figure 4-6 to define S(T) given by

$$S(T) = [C(t_1) - C(t_2)]/\Delta C(0) \qquad 4.6$$

Where ΔC(0) is the capacitance due to the pulse change at t = 0. Now for exponential transients,

$$S(T) = \left[exp\left(-t_1/\tau\right)\right] - \left[exp\left(-t_2/\tau\right)\right] \qquad 4.7$$

which can also be written as

$$S(T) = exp\left(-t_2/\tau\right)\left[1 - exp(-\Delta t/\tau)\right] \qquad 4.8$$

where $\Delta t = t_2 - t_1$. Therefore the relationship between τ_{max}, t_1 and t_2 can be obtained by differentiating S(T) with respect to τ and equating the result to zero:

$$\tau_{max} = \frac{t_1 - t_2}{ln\left(\frac{t_1}{t_2}\right)} \qquad 4.9$$

Therefore the emission rates of the peak of DLTS signal can be obtained accurately. Carrying out a thermal scan using many different rate windows enables one to identify the peak positions and the temperature at which they occur. This information can be used to calculate the activation enthalpy and the apparent capture cross-section [16].

4.3.6 Laplace-DLTS

Deep level transient spectroscopy has been a valuable tool in characterising electrically active deep level states in semiconductors since its invention in the 70s by Lang. Unfortunately, this technique has limitations as far as its emission rate resolution is concerned. The lock-in-amplifier or the double boxcar filter used in DLTS shows good sensitivity but poor time constant resolution. It is because of this poor time constant resolution that makes DLTS unsuitable for separating closely spaced transients and therefore its inability to study defect fine structure.

Dobaczewski *et al* [62] developed an improved a high resolution version of DLTS in 1990. They called it Laplace-DLTS (LDLTS). LDLTS uses a regularised inverse Laplace transform instead of the boxcar analysis. This results in an order of magnitude improvement in emission rate resolution in the studies of the thermal emission of carriers from deep states. Consequently, LDLTS can separate closely spaced transients when a number of defects with similar emission characteristics are present. LDLTS can also probe very narrow regions of the semiconductor and study selectively the active regions of devices.

4.3.7 The concepts of Laplace-DLTS

In DLTS there are two main classes of transient processing methods, analog and digital signal processing. Analog signal processing is a real-time process which involves extracting the capacitance transients as the temperature is ramped. The digital signal processing involves digitalising the transient output of the capacitance meter, normally done with a sample held at a fixed temperature and averaging many of these digitalised transients to reduce noise. If the transient is digitalised then it is easier to apply signal processing tasks, even complex ones. The concept of digitalising capacitance at a constant temperature and extracting the time constant is the basis of high resolution L-DLTS.

Within the context of DLTS using digitised transients, various schemes have been published and various degrees of success reported. Among the range of approaches that are of importance is the method of moments technique as used by Ikossi-Anastasiou and Roenker [63] Nolte and Haller [64]used an approximation the Gaver-Stehfest algorithm to effect a Laplace transform although achieving a substantial increase in resolution found the approach to be unstable in the presence of experimental noise levels. Eiche *et al.* [65] use Tikhonov regularization to separate the constituent exponentials in a photo-induced current transient spectroscopy signal with an approach very similar to that which has been adopted for the work described in this work.

In order to give a quantitative description of the non-exponential nature observed in the capacitance transients, one assumes that they are characterized by a spectrum of emission rates [66]

$$f(t) = \int_0^\infty F(s)\, e^{-st} ds \qquad 4.10$$

where $f(t)$ is the recorded transient and $F(s)$ is the spectral density function. Equation 4.10 gives a mathematical Laplace transform of the true spectra of the emission rates. To get the real spectra of the emission rates, an algorithm is made use of that performs an inverse Laplace transform of the function $f(t)$. As a result, a spectrum of delta-like peaks is expected to be obtained for multi-, mono-exponential transients or a broad spectrum with no fine structure for continuous distribution [66].

In the experimental demonstration of the Laplace DLTS system, three different software procedures are used for the numerical calculations. All of them are based on the Tikhonov regularization method. However, they differ in the way the criteria for finding the regularization parameters are defined. The first one, (CONTIN) is in the public domain and has been obtained from a software library and modified in order to integrate it with our system [67]. The outline code of the second one (FTIKREG) is distributed by the same library but it has been substantially modified by the original authors for operation within our LDLTS system [67]. The last one, (FLOG) has been specifically developed for the system. The parallel use of three different software packages substantially increases the level of confidence in the spectra obtained [68]. Additionally, for preliminary data analysis a discrete (multiex- ponential) deconvolution method can be used. This method is based on a simple integration procedure [69].

4.3.8 Deep level transient spectroscopy measurement set-up

The set-up of the DLTS and Laplace-DLTS system used in this work consists of the following:

(a) A cryostat, which the sample to be characterised is mounted on. A closed cycle cryostat is used in the cooling from high to low temperatures. A heater is located at the tip of the cryostat which raises the temperature from low to high values. The temperature of the cryostat is controlled by a Lakeshore 340 temperature controller which is used in the range 40 K to 350 K in this study.

(b) A Boonton 7200 capacitance meter with 100 mV, 1 MHz ac voltage signal used to monitor the thermal emission of carriers after excitation by a pulse generator.

(c) A Laplace card with an internal pulse generator for producing the appropriate quiescent reverse bias voltage and pulses. The Laplace card also contains software used for data collection and has a processing system which analyses and averages transients before the spectra is displayed for both conventional and Laplace- DLTS. The Laplace card was also used to record the capacitance-temperature (CT) scans.

(d) A HP 33120 15 MHz waveform external generator, which produced the desired quiescent bias and filling pulse in measurements that required shorter filling pulse widths.

Conventional and Laplace-DLTS sample excitation parameters are set up using the Laplace program. In the conventional-DLTS mode the capacitance meter measures the capacitance transient after excitation. The transients are then processed by the Laplace card. Ramping up or down the temperature using a particular rate window, a DLTS spectrum is displayed on the computer.

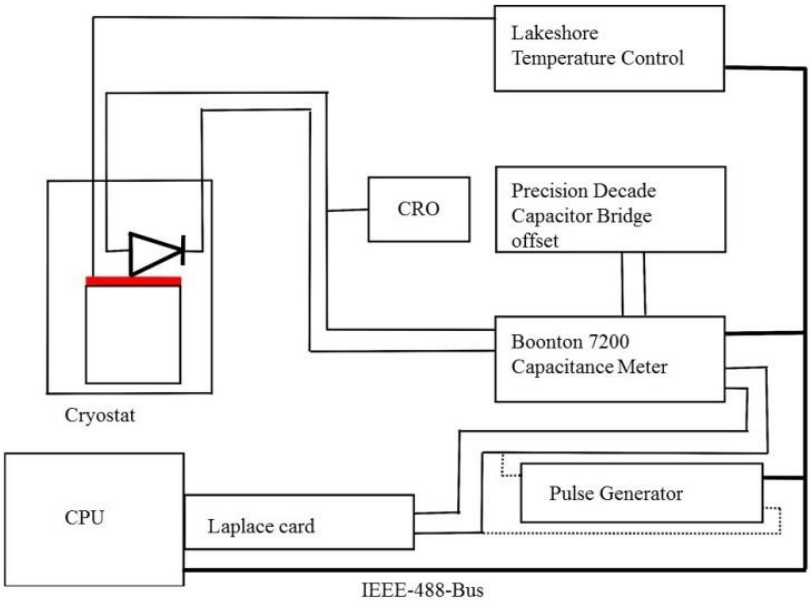

Figure 4-8: A block diagram of DLTS set up at the University of Pretoria.

4.4 Sample Annealing

Annealing a crystal can sometimes help reduce defects in semiconductors and in some cases introduce them. The purpose of the annealing is three-fold. Firstly, to achieve epitaxial growth or oxidation, heating is necessary to obtain the required chemical reaction at the surface. Secondly, it is to increase the diffusion coefficient of some defect so that it has sufficient mobility to migrate the required distance during the time of the treatment. Thirdly, following irradiation of samples by high-energy particles which leads to the displacement of atoms from lattice sites, it is usually necessary that the damage should subsequently be removed. It is not so much a matter of making primary defects more mobile, but of allowing metastable configurations involving perhaps clusters of vacancies to dissociate and annihilate with interstitials which may be clustered elsewhere in the crystal [36].

The samples were annealed in a Lindenberg Hevi-duty furnace. A gas cylinder was connected to the furnace so that it provided the required ambient, in this work argon was used. A thermocouple placed in the furnace just below the sample was used to monitor the annealing temperature. Argon was supplied at a constant rate of 2.0L/min for the whole annealing period. Figure 4-9 shows the set-up of the furnace.

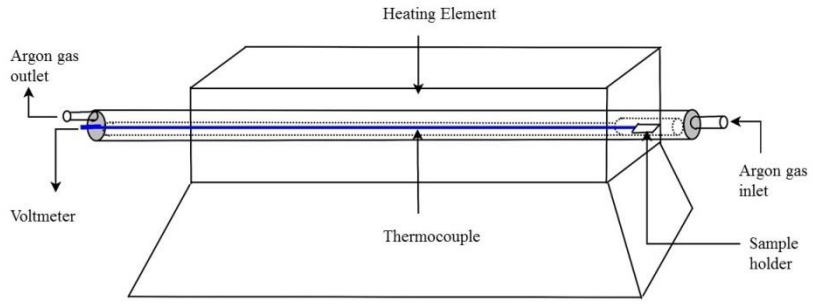

Figure 4-9: A sketch of the annealing furnace used in this study at the University of Pretoria.

4.5 Rutherford Back Scattering

Rutherford Backscattering Spectrometry (RBS) is an ion scattering technique used for determining the thickness and composition of thin films (< 4000 Å).

Areas that have been lately explored are the use of backscattering technique in composition determination of new superconductor oxides; analysis of lattice mismatched epitaxial layers, and as a probe of thin film morphology and surface clustering [70].

During the collision, energy is transferred from the incident particle to the target specimen atoms; the change in energy of the scattered particle depends on the masses of incoming and target atoms. For an incident particle of mass M_1, the energy is E_0while the mass of the target atom is M_2. After the collision, the residual energy E of the particle scattered at angle Φ can be expressed as:

$$E = k^2 E_0 \qquad 4.5$$

Where k is the kinematic scattering factor, which is actually the energy ratio of the particle before and after the collision. Since k depends on the masses of the incident particle and target atom and the scattering angle, the energy of the scattered particle is also determined by these three parameters.

$$k = \frac{\left(M_1 cos\Phi + \sqrt{(M_2^2 + M_1^2 sin^2\Phi)}\right)}{M_1 + M_2} \qquad 4.6$$

During an RBS analysis, high-energy (MeV) He^{2+}ions (i.e. alpha particles) directed onto the sample and the backscattered particles are detected by the detector-analysis system which measures the energies of the particles. During the collision, energy is transferred from the incident particle to the target specimen atoms; the change in energy of the scattered particle depends on the masses of incoming and target atoms. In this study RBS was used to investigate the temperature at which the Pd_2Si silicide phase was formed.

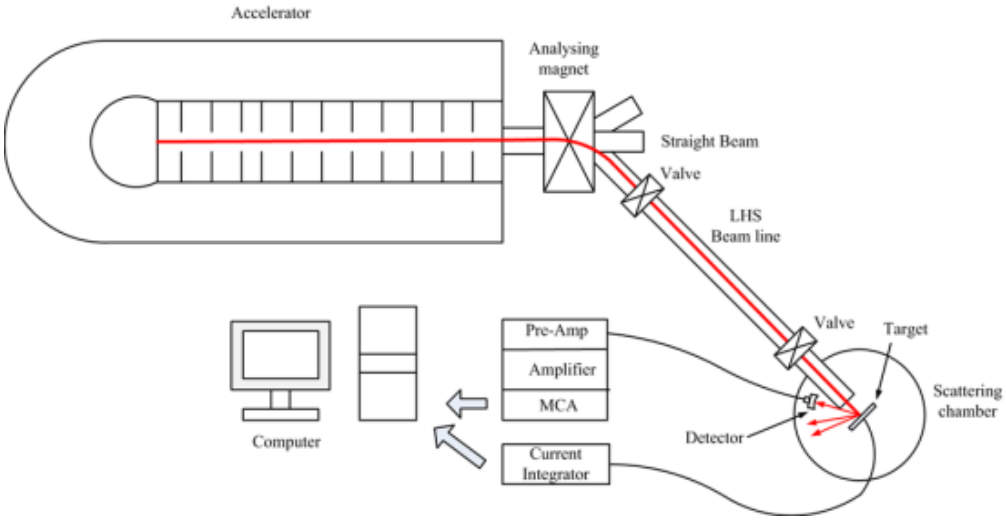

Figure 4-10: A schematic diagram of the Rutherford backscattering spectroscopy set up at the University of Pretoria [71].

4.6 Scanning Electron Microscopy

The scanning electron microscope (SEM) uses a focused beam of high-energy electrons to generate a variety of signals at the surface of solid specimens. The signals that derive from electron-sample interactions reveal information about the sample including external morphology, chemical composition and crystalline structure and orientation of materials making up the sample. In most applications, data are collected over a selected area of the surface of the sample, and a 2-dimensional image is generated that displays spatial variations in these properties [72].

A source which is the electron-gun, provides a stable electron beam with adjustable energy and is accelerated down the column. The beam passes through a series of lenses (condenser and objective) which act to control the diameter of the beam as well as to focus the beam on the

specimen. When focused on the specimen, the electron beam stimulates the emission of electrons. An area of beam-specimen interaction generates several types of signals that can be detected and processed to produce an image or spectra [72].

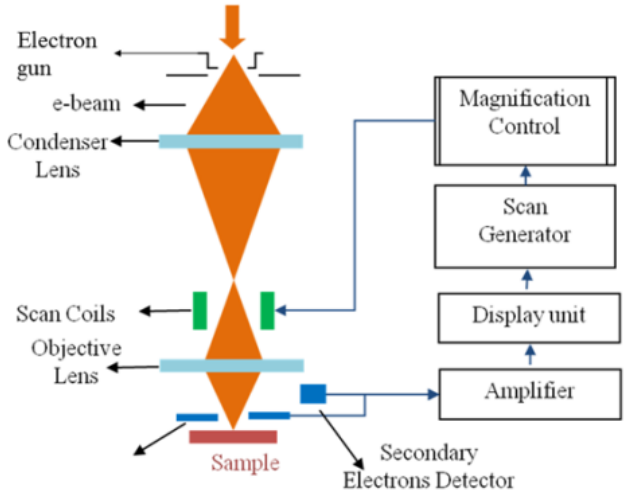

Figure 4-11: A schematic diagram of the Scanning Electron Microscope.

When an incident electron beam interacts with a sample, the incident electrons undergo two types of scattering; elastic and inelastic scattering. These interactions result in a number of signal events. For example backscattering of electrons, secondary electrons, X-rays just to mention a few. In this work only backscattered and secondary electrons will be discussed.

Backscattered electrons are a result of elastic collisions between incoming incident electron beam and a target atom. They consist of high energy electrons that are reflected or backscattered out of the target sample. The number of backscattered electrons generated depends on the atomic number of the target. For example, an element with a higher atomic number will backscatter more electrons and as a result appear brighter than an element with a lower atomic number. The backscattering imaging mode is useful when relative atomic density information together with topographical information is required [73].

Inelastic collisions between incident electrons and the target give rise to secondary electrons. Secondary electrons have less energy compared to that of back scattered electrons. The signals from the secondary electrons are used to study the topography of a sample.

Chapter 5

Results and discussion

5.1 Characterisation of Silicides

5.1.1 Introduction

The aim of studying silicide formation was stimulated by the expectation of device applications of silicides in the late 1970s and early 1980s [26]. Metal silicides have been fascinating materials owing to their technological application as ohmic contacts, Schottky contacts and interconnects. Palladium (Pd) silicide is potentially attractive from the viewpoint of contact materials for shallow junctions because Pd forms a metal- rich silicide, Pd_2Si which remains stable up to 700°C after forming at low temperatures [74-76]. It has been shown recently that silicide thin films can be formed by rapid thermal annealing (RTA). Titanium disilicide, for example, has been obtained after short-time processing of thin titanium layers deposited by electron gun evaporation or magnetron sputtering over single crystal or polycrystalline silicon. The reaction between Ti and Si was completed after a few seconds of heating. The quality of the silicide was demonstrated by its low resistivity (14 mΩ.cm) [77]. In this section, the results obtained from *I-V* measurements, *C-V* measurements, RBS and SEM will be discussed.

5.2 Experimental Procedure

In order to investigate the annealing behaviour of Pd and Ti Schottky contacts, epitaxially grown, 13 µm thick, phosphorus doped Si, with free carrier concentration of $3.55 \times 10^{15}\ cm^{-3}$, grown on an n^{++} Si substrate and boron doped Si with a free carrier concentration of $1.48 \times 10^{15} cm^{-3}$ grown on a p^{+} substrate respectively, were used for our investigation. Before metallization, samples were first degreased in trichloroethylene (TCE), isopropanol (ISO) and methanol for 5 minutes each followed by dipping into 40% HF for 60 seconds. Immediately thereafter, the samples were loaded into the electron beam deposition (EBD) system that was pumped down to a pressure below 10^{-6} mbar. Eight Pd Schottky contacts of 0.6 mm diameter and 100 nm thicknesses were deposited. Samples for silicide studies were deposited without the mask onto cleaned Si. Vacuum just before evaporation was

3×10^{-6} mbar which increased to 3×10^{-5}mbar during deposition. After contact formation, *I-V* and *C-V* measurements were performed to assess the quality of the diodes and to determine the free carrier density of Si after electron beam exposure. *I-V* and *C-V* measurements were repeated after every annealing cycle in Ar gas, for ten minutes from 200°C to 700°C in steps of 100°C. RBS was carried out on the samples covered with metal on the whole surface for each annealing cycle, using the same temperature range and annealing times as that of the Schottky contacts.

5.3 Results and discussion

n-type material

Figure 5-1 shows the semilog forward and reverse bias *I-V* characteristics of the Schottky barrier diodes (SBD) for the as-deposited samples and after annealing in the temperature range between 200°C and 700°C. The forward *I-V* characteristics of the Schottky diodes from 0 - 0.3V are deduced from the thermionic emission current-transport model [3]. The graphs for the forward *I-V* characteristics of the diodes were linear at lower voltages and suffer the effects series resistance at voltages higher than 0.3 V. The effects of surface states and leakage current may also have affected the linearity of the *I-V* graphs [78]. Figure 5-2 shows the plot of series resistance as a function of annealing temperature. The graph shows a general increase in series resistance with increase in annealing temperature. The value of series resistance increases from 32 Ω for the as-deposited sample to 242 Ω after annealing at 700°C.

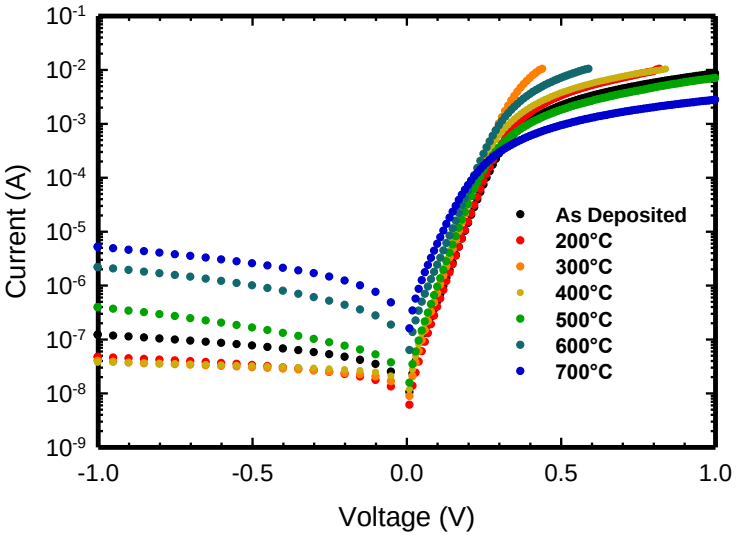

Figure 5-1: The forward and reverse I-V characteristics of a Schottky contact after isochronal thermal annealing for 10 minutes from temperatures ranging from 200°C to 700°C.

Figure 5-3 shows the SBH and the ideality factor as a function of annealing temperature. The SBH decreased from 0.69 eV to 0.64 eV, while the corresponding ideality factor increased from 1.2 to 1.6 as the annealing temperature increased. The change is due to the effects of interface states, series resistance, leakage current and non-uniform distribution of interfacial charges is responsible for the decrease in the values for the SBH and the increase in ideality factor. This is in agreement with Sahin *et al*. These researchers concentrated on *I-V* and *C-V* measurements at a frequency range between 0.3-2MHz [79].

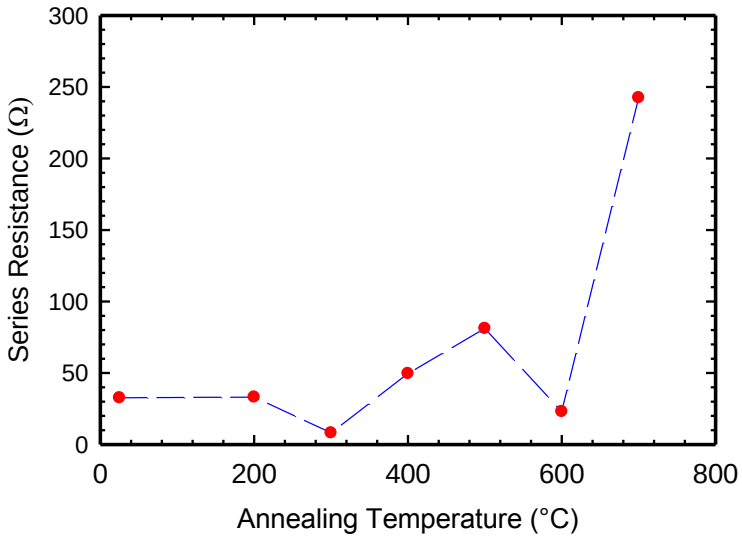

Figure 5-2: A plot of series resistance as a function of annealing temperature.

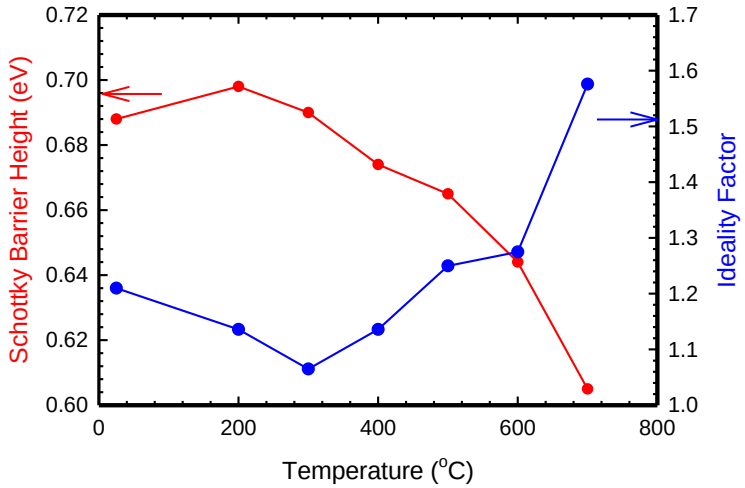

Figure 5-3: The graph of Schottky barrier height and ideality factor as a function of temperature for Pd/n-Si (111) Schottky contacts.

Using equation 2.47 and the intercept of the straight line fit of the semilog-forward bias *I-V* graph, the value of the effective Schottky barrier height (SBH) was determined. Figure 5-4 shows the graph of Schottky barrier height (SBH) and reverse leakage current at -1V as a function of annealing temperature. The as deposited sample had a reverse leakage current of 1.20×10^{-7} A at -1V measured at room temperature. As the annealing temperature increased to 700°C, the reverse current increased approximately by one order of magnitude to 5.10×10^{-6}A. The increase in reverse leakage current with increase in annealing temperature is due to a decrease in the depletion layer width. As a result of annealing, changes in the current transport mechanism across the interface took place. Conventional thermionic emission converted into tunnelling [80]. The SBH drops significantly to a value of 0.64eV after annealing at 600°C while the reverse leakage current at -1V reaches a value of 2.10×10^{-6}A. The results obtained at 600°C could be due to interfacial reactions at the metal-semiconductor interface due to the increase in annealing temperature. The presence of a thin insulating layer between the metal and semiconductor may be factor to consider. Another cause may have been inhomogeneities of the thickness and composition of the metal layer [81].

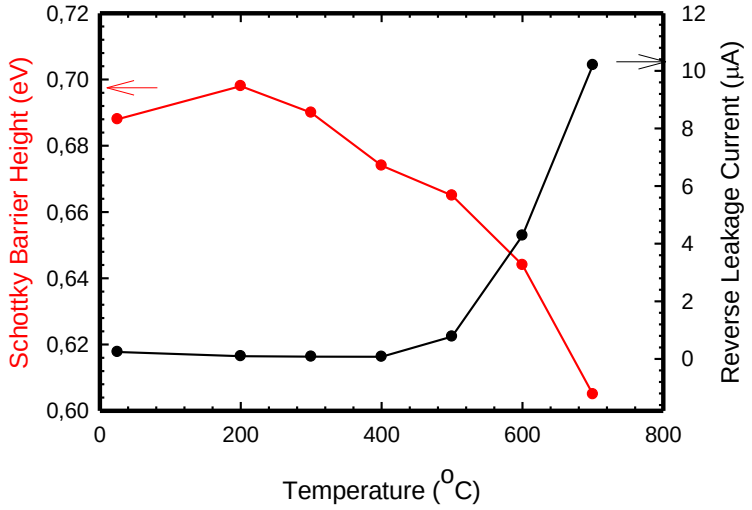

Figure 5-4: The plot of Schottky barrier height and reverse leakage current at -1V as a function of temperature for Pd/n-Si (111) Schottky contacts.

Figure 5-5 displays the plot of C^{-2} against V at 1 MHz under reverse bias for Pd/n-Si (111) Schottky diodes at different annealing temperatures. The graph obtained is linear which shows that the carrier concentration is constant, a parameter determined from the slope of the $C^{-2} - V$ graph [82].

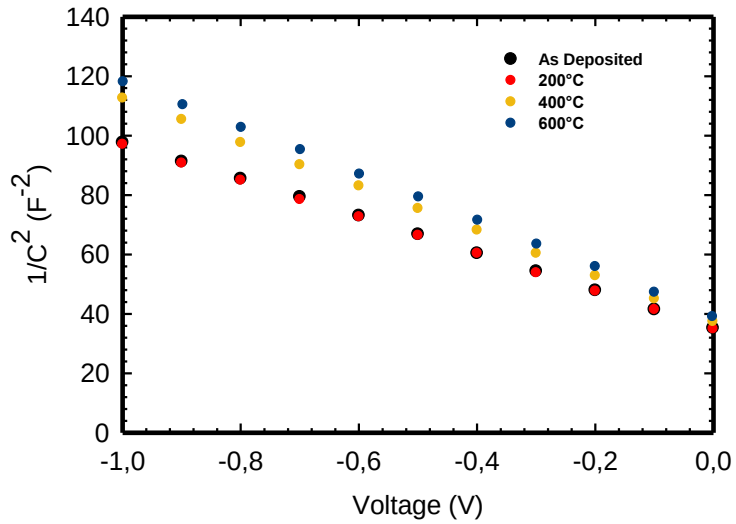

Figure 5-5: The C^{-2}-V characteristics of a Pd/n-Si (111) Schottky contacts at a frequency of 1.0MHz after isochronal annealing for 10 minutes at different annealing temperatures: as-deposited, 200°C, 400°C and 600°C, measured at room temperature.

Figure 5-6 shows the plot of the net doping density at different annealing temperatures. The carrier concentration decreases sharply with increasing temperature from 200°C to 400°C.

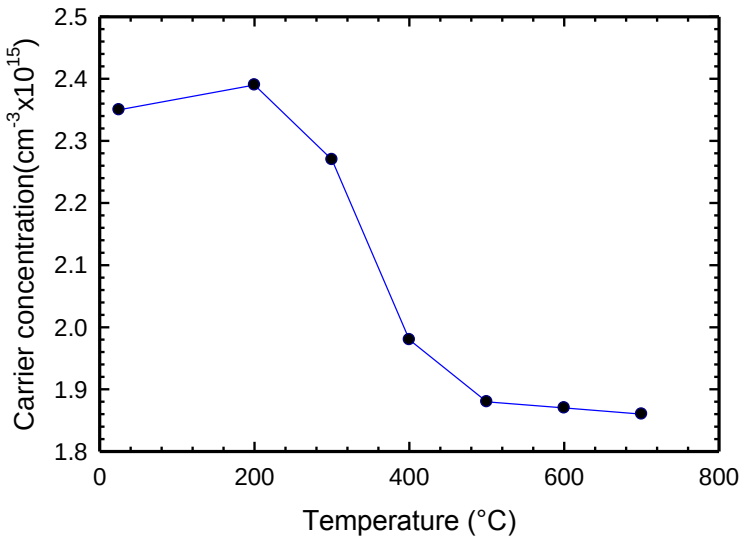

Figure 5-6: The plot of carrier concentration as a function of annealing temperature.

The parameters obtained from fitting the linear part of the *I-V* curves shown in figure 5-1 are displayed in table 5-1. There is a general increase of reverse leakage current with increase of annealing temperature. There is a sharp increase at 600°C. There is a general decrease in both *I-V* and *C-V* Schottky barrier heights (SBH). The *C-V* SBH was found to be 0.82 eV before annealing while the *I-V* barrier height was 0.69 eV. Due to different nature of measurements techniques, SBH obtained by *I-V* and *C-V* are not the same [74]. The discrepancy between them could also be attributed to interface states, quantum mechanical tunnelling and lateral distribution of barrier height inhomogeneities [81, 83].

As the annealing temperature increased from 200°C to 400°C, the *C-V* Schottky barrier values were 0.83eV and. 0.77eV respectively. A decrease in barrier height could be due to the presence of interface states at the metal-semiconductor junction [30, 84].The leakage current also decreases between 200°C and 400°C from 0.05 to 4.0×10^{-8}A. At 300°C the leakage current is at 3.0×10^{-8}A. This may be attributed to the presence of Pd_2Si which forms between these temperatures mentioned above [22].

Table 5-1: Reverse leakage current, SBHs, ideality factor, series resistance and net doping density as a function of temperature.

Annealing Temperature (°C)	Leakage Current at -1V (μA)	*I-V* SBH (eV)	*C-V* SBH (eV)	Ideality Factor, n	R_s (Ω)	N_d ($\times 10^{15}$ cm^{-3})
as-deposited	0.12	0.69	0.82	1.2	32	3.55
200	0.05	0.70	0.83	1.1	33	2.39
300	0.03	0.69	0.79	1.1	8	2.27
400	0.04	0.67	0.77	1.1	49	1.98
500	0.04	0.67	0.78	1.3	81	1.88
600	2.10	0.64	0.77	1.3	23	1.87
700	5.10	0.60	0.78	1.6	242	1.86

RBS was conducted to determine the structure of the compound formed at the metal-semiconductor interface in this study. In silicide formation, the transport mechanism has often been found to be a combination of simple diffusion processes [3]. From the RBS spectra shown in figure 5-7, Si diffused towards the surface while Pd diffused into the bulk. The arrows indicate the surface channel numbers of Pd and Si which are 448 and 298 respectively. At 200°C, there is a step forming on the Pd low energy edge of the palladium peak. The ratio of the heights of the Pd step and Si step at 250°C suggests that the silicide phase formed is Pd_2Si. Diale *et al* did a comparative study of cobalt/silicon (Co/Si) and chromium/silicon (Cr/Si) inter-diffusion by introducing tantalum (Ta) thin layers within the Co layers. This was done so that the Ta layers acted as inert markers. The interdiffusion of Si and Co occurred at 390°C. RBS results from their study suggested that the ratio of the heights of the Co step to the Si step [85]. At 400°C, Si has diffused to the surface and Pd has completely reacted with Si to form Pd_2Si as suggested by the RBS spectra in figure 5-7.

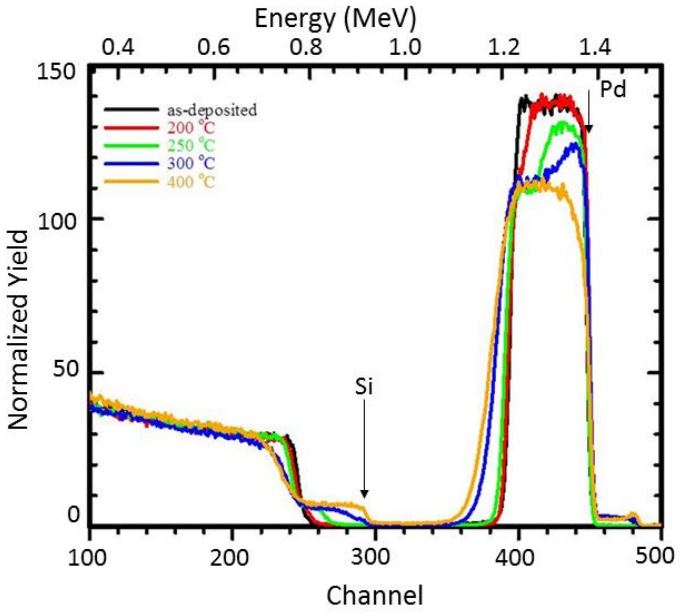

Figure 5-7: The RBS spectra of 1.6MeV He^+ ions for Pd/n-Si sample as a function of annealing temperature.

Wei *et al* found out that Pd_2Si is the first and only phase detected in the temperature range 310°-460°C after subjecting the sample to rapid thermal annealing. The temperature at which Pd_2Si started to form was 320°C [86]. Levy *et al* reported that Pd_2Si layers were formed at 400°C after being annealed for a few seconds using rapid thermal annealing [87]. From both TEM and XRD analysis, J.F Chen and L.J Chen observed that Palladium was found to coexist with epitaxial Pd_2Si in as-deposited and 200°C annealed samples. Pd_2Si is the only silicide phase present in samples annealed between 300-800°C. The Pd_2Si/ (lll) Si interfaces are rather smooth over long distances. In samples annealed at 800°C, Pd_2Si was observed to be epitaxially related to the silicon substrate [88]. In this study, at 300°C the Pd_2Si phase may have been influencing the electrical characteristics of the Pd Schottky contacts. From table 5-1, the values of reverse leakage current and series resistance were at their lowest values, 0.03μA and 8.1Ω respectively, at 300°C.

Scanning electron microscopy was carried out on the Pd/n-Si as-deposited sample and samples annealed at different temperatures each for 10 minutes. Figure 5-8 shows the morphological changes as annealing temperature was increased. Surface roughness increases with increase of annealing temperature and at 600°C, the Pd deposited on the surface of the silicon substrate shows signs of agglomeration but this does not seem to affect the rectifying properties of the Pd/n-Si contact as indicated by figure 5-1. This could be due to the thermal stability of the Pd contact on the n-Si (111) substrate. Suryana *et al* reported agglomeration of Pd_2Si at 550°C

after depositing two layers of Pd each 10 nm thick, with a Ti intermediate layer. These samples were annealed at temperatures between 300°C-600°C using the rapid thermal annealing method in a nitrogen ambient [84].

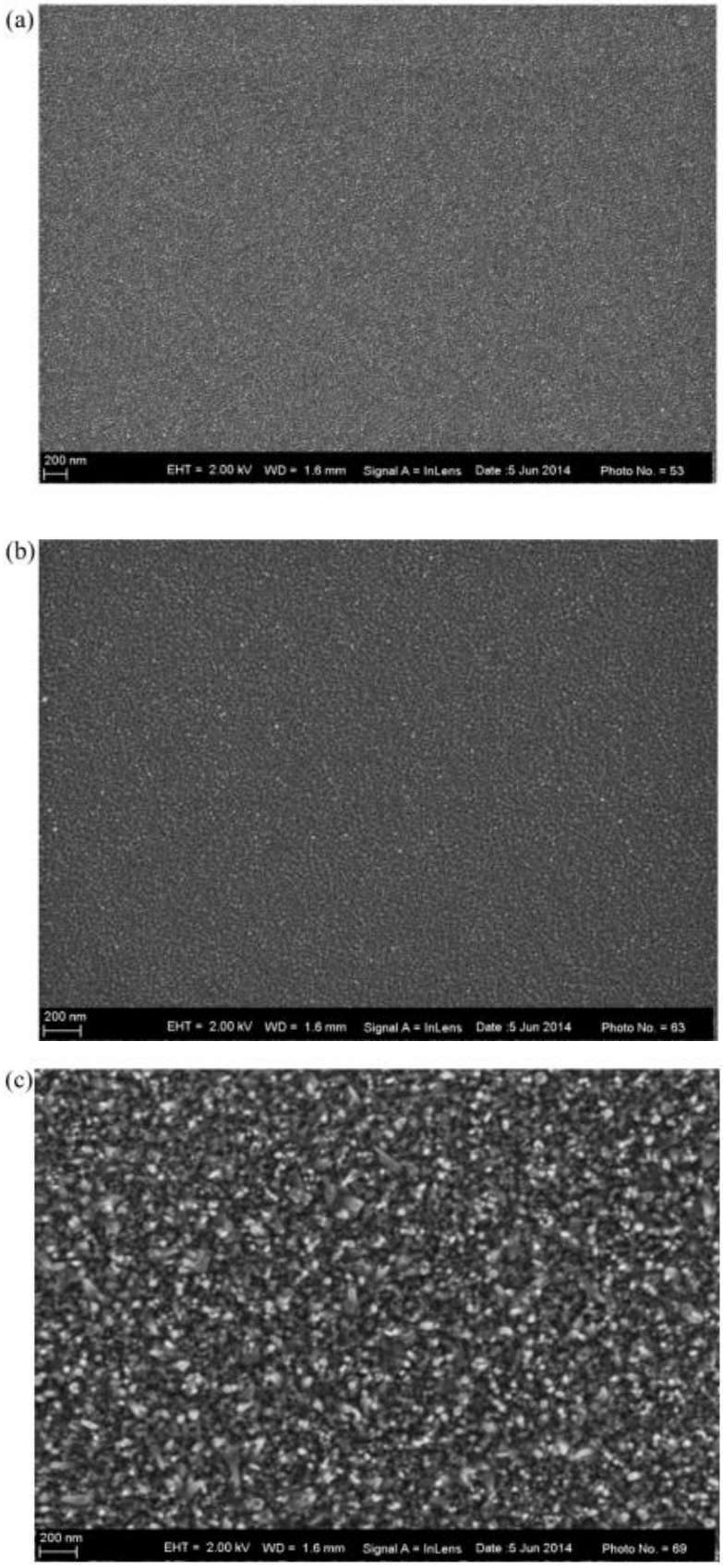

Figure 5-8: SEM images of (a) the as-deposited Pd/n-Si sample and samples annealed at (b) 250°C and (c) 600°C each for 10 minutes.

An article by Diale *et al* reports on Pt Schottky barrier diodes fabricated onto n-Si(100) using electron beam deposition [85]. The behaviour of the Schottky barrier diodes (SBD) was investigated under various annealing conditions. The variation of SBH and ideality factor with annealing temperature was attributed to interfacial reactions of Pt and n-Si(100) and the subsequent formation of platinum silicides. Pt_2Si formed at temperatures between 210°C and 280°C with ideality factor increasing to 1.16 and SBH decreasing to 0.77 eV. At 300°C, $PtSi$ has formed increasing the ideality factor to 1.83 while the SBH decreased to 0.70 eV.

p-type material

A similar study was conducted on epitaxially grown p-type Si <111> material using titanium (Ti). Figure 5-9 shows the semilogarithmic forward and reverse bias *I-V* characteristics of Ti contacts fabricated on p-Si and annealed in the temperature range 100°C-500°C. The graphs of the forward characteristics of the diodes annealed up to a temperature of 300°C were linear at voltages lower than 0.3V. At 400°C the curves become less linear this could have been as a result of the formation of an oxide of titanium at the metal-semiconductor interface. G.P. Burns formed titanium dioxide films on Si substrates at temperatures ranging 450°C- 800°C using rapid thermal oxidation [89].

The reverse leakage current increased with increasing annealing temperature, from 3.8 μA to 8.5 μA. At about 300°C, the Schottky barrier height dropped to 0.55eV while the reverse leakage current at -1 V reaches a value of about 6.5μA. Figure 5-13 shows the plot of the net doping density at different annealing temperatures. The carrier concentration increases with increasing annealing temperature from 100°C to 500°C. The *C-V* SBH was found to be 0.57 eV before annealing while the *I-V* barrier height was 0.53 eV. Due to different nature of measurements techniques, SBH obtained by *I-V* and *C-V* are not the same [74]. In this study the *C-V* barrier exhibited a general trend compared to the *I-V* barrier height which showed no clear trend. This could be as a result of inhomogeneity in (or over the surface of) the metal-semiconductor interface. Figure 5-11 shows the SBH and the ideality factor as a function of annealing temperature. The Schottky barrier height (SBH) deduced from the thermionic emission current model, increased from 0.53 eV to 0.56 eV, while the corresponding ideality factor increased from 1.2 to 1.8 as the annealing temperature increased.

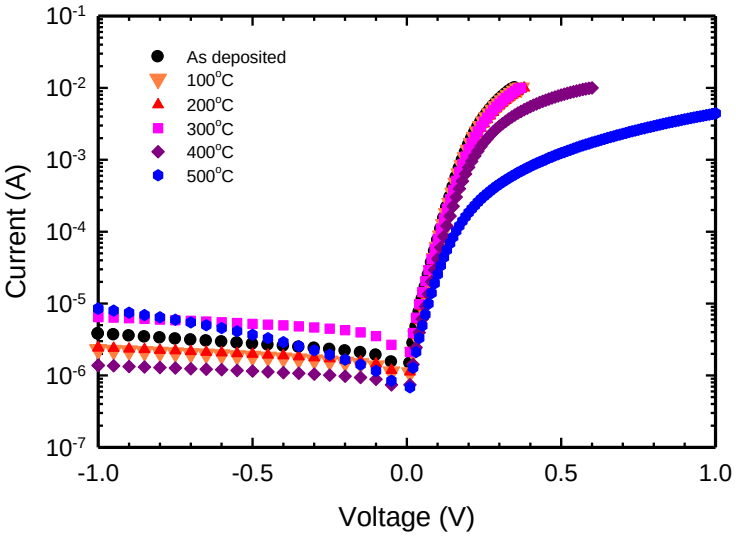

Figure 5-9: The forward and reverse I-V characteristics of a Schottky contact after isochronal thermal annealing for 10 minutes at temperatures ranging from 100°C to 500°C.

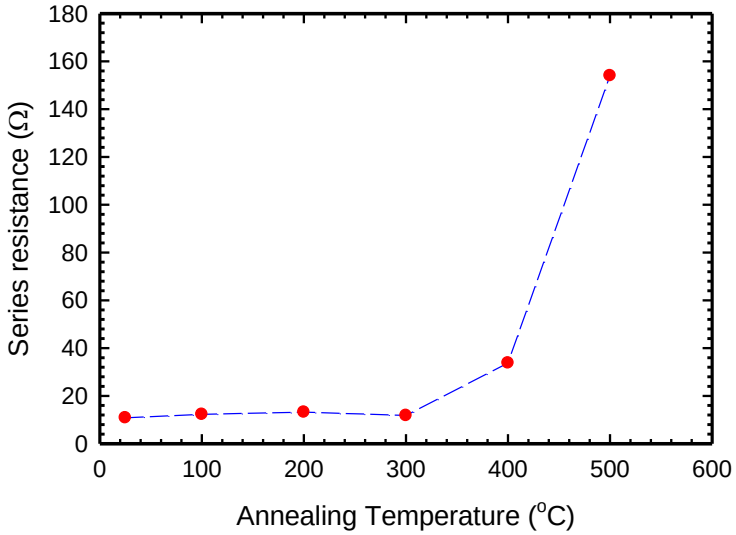

Figure 5-10: A plot of series resistance as a function of annealing temperature for Ti/p-Si (111) Schottky contacts.

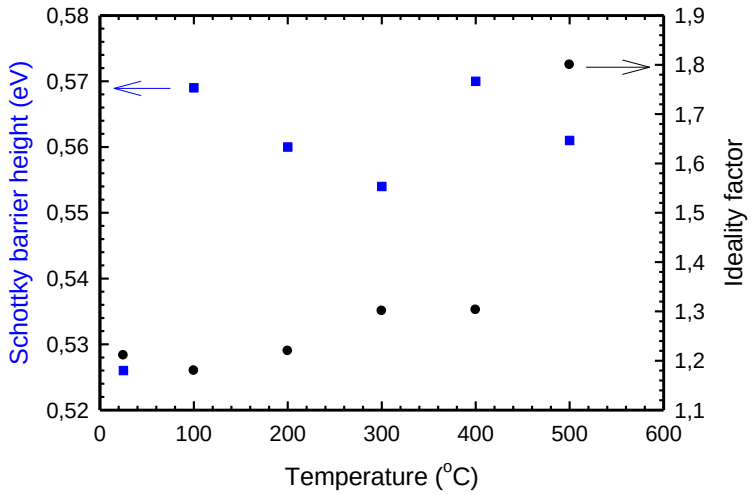

Figure 5-11: The graph of Schottky barrier height and ideality factor as a function of temperature for Ti/p-Si (111) Schottky contacts.

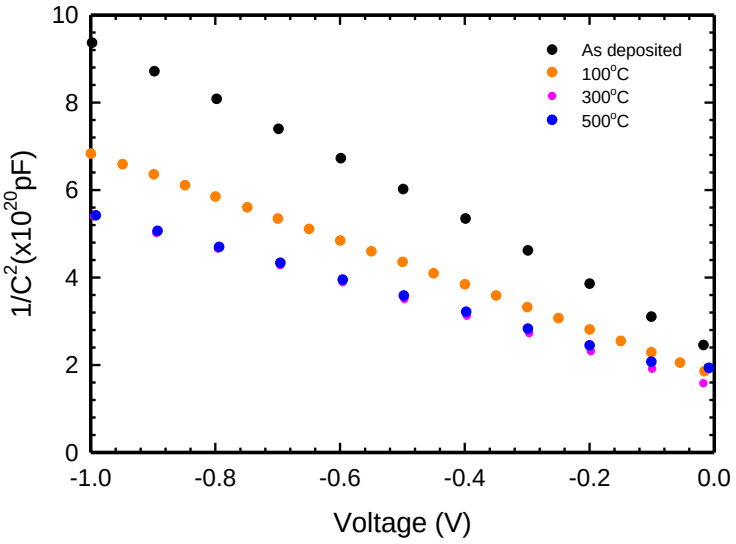

Figure 5-12: The C^{-2}-V characteristics of a Ti/p-Si (111) Schottky contacts at a frequency of 1.0MHz after isochronal annealing for 10 minutes at different annealing temperatures: as-deposited, 100°C, 300°C and 500°C measured at room temperature.

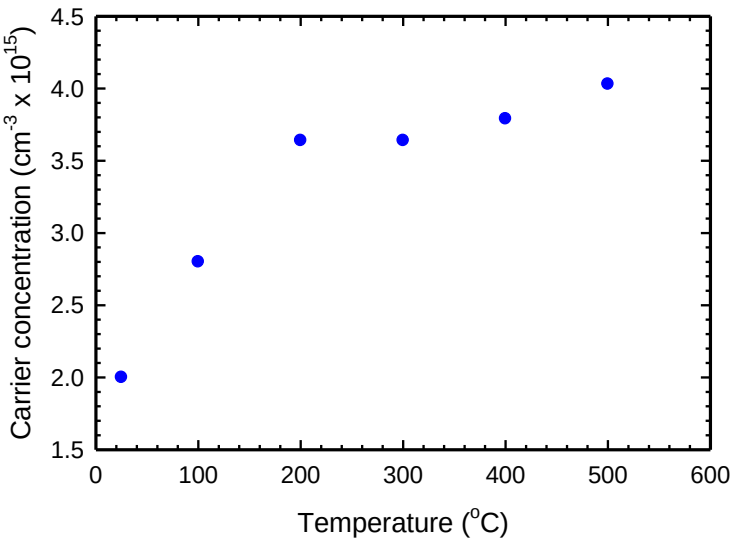

Figure 5-13: The plot of carrier concentration as a function of annealing temperature for Ti/p-Si (111) Schottky contacts.

Table 5-2: Reverse leakage current, SBHs, ideality factor, series resistance and net doping density as a function of temperature

Annealing Temperature (°C)	**Leakage Current at -1V (μA)**	***I-V* SBH (eV)**	***C-V* SBH (eV)**	**Ideality Factor, n**	**R_s (Ω)**	**N_d ($\times 10^{15}$ cm^{-3})**
as-deposited	3.8	0.53	0.57	1.2	10	2.40
100	2.3	0.57	0.58	1.2	12	2.80
200	2.4	0.57	0.61	1.2	13	3.64
300	6.5	0.55	0.61	1.3	11	3.64
400	1.4	0.57	0.66	1.3	33	3.79
500	8.5	0.56	0.73	1.8	154	4.03

The study seems to suggest that silicide formation in n-type material occurs at lower annealing temperatures than in p-type material. The Ti contacts on p-type Si degraded at a lower temperature than the Pd contacts on n-type material. In p-type material, SBH increased from 0.53 eV to 0.56 eV whereas in n-type material, the SBH decreased from 0.69 eV to 0.60 eV. From table 5-1 and table 5-2 showed that all the other parameters had the same general trend.

Thermal stability studies of platinum Schottky contacts on n- Si (111) and the defects introduced during fabrication and annealing processes.

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Abstract. The electron beam deposition process was used to fabricate Pt Schottky contacts onto n-Si (111). Subsequently these contacts were annealed at temperatures varying from 50°C to 600°C for ten minutes at each temperature. The forward *I-V* characteristics show that the diodes were stable at lower voltages and suffer series resistance effects at voltages higher than 0.5 V. The reverse *I-V* curves shows increasing leakage current with increasing annealing temperature. At lower annealing temperatures, the reverse leakage current is constant at about 10^{-9} A. The ideality factor increased from 1.02 to 2.61 while the barrier height decreased from 0.80 to 0.70 eV as the annealing temperature increased. DLTS revealed that electron beam deposition introduced defects which were identified as the E-centre (VP centre), the A-centre (VO centre), the interstitial carbon (C_i) and the interstitial carbon-substitutional carbon (C_iC_s) pair. Isochronal annealing at 10 minutes intervals revealed that the E-centre vanishes between 125 and 175°C annealing while the concentration of the A-centre increased in this range. The A-centre annealed out above 350°C and after 400°C, all the electron beam induced defects were all removed.

1. Introduction

Metal silicides have been used as electrical conductors in silicon integrated circuits (SIC) since the beginning of the 20th century due to electrical properties such as low resistivities, easy fabrication and general stability in most processing techniques [1]. The resistivities of transition metal silicides are comparable with those of metals and metal-alloys, making this group of silicides good electrical conductors. Applications of metal-silicides have focused on Schottky barrier and ohmic contacts, gate and interconnection metal and as epitaxial conductor in heterostructures. Silicides with high melting points are attractive to use in high temperature device fabrication and operating environments [2]. In the fabrication of silicides, metals are deposited according to their melting points in different metallization systems. In particular, the electron-beam deposition (EBD) is used to deposit metals with high melting points, with an added advantage of uniform deposition rates. The EBD process, like many other metallization processes, introduces defects at and close to the metal-semiconductor interface, which has adverse effects on the device performance [3]. The defects responsible for the alteration of the barrier height of the metal contacts are those formed when energetic particles reach the semiconductor surface, creating damage in the lattice. In Si-based devices, defects created by proton and electron radiation increase the switching speed of the devices [4]. For high open circuit voltage Si photovoltaic devices, defect degradation in electrical properties of the device has been reported [5]. Defects introduced during EBD of metals on Si grown by Czochralski and float zone methods have previously been reported, where the E-centre (VP) and the A-centre (VO) appeared as dominant [6]. A defect similar to a divicancy was also observed [7]. The difference between the observed defects in reference [6] and [7] may be attributed to different EBD

systems used, different vacuum conditions as well as the use of Si with different concentrations of impurities such as C and O In this work, Pt Schottky contacts on n-Si (111) were fabricated and electrical properties of the contacts were investigated. We also report on the electronic properties of defects introduced during metal deposition and the effects of annealing on the defects.

2. Experimental Procedure

We have used epitaxially grown, 12 μm thick, Si doped with P to a level of 3.5×10^{15} cm^{-3} grown on a n^{++}Si substrate for our investigation. Before metallization, samples were first degreased in trichloroethylene (TCE), isopropanol (ISO) and methanol for 5 minutes each followed by dipping into HF for 60 seconds. Immediately thereafter, the samples were loaded into the EBD vacuum system that was pumped down overnight to a pressure below 10^{-6} mbar. Pt Schottky contacts 0.6 mm in diameter and of various thicknesses were deposited in an EBD vacuum system through a mechanical mask. Typically, eight Schottky Pt contacts were fabricated onto piece of 3 mm x 5mm Si. A Varian 10 KW electron gun (model 989-1118) vacuum evaporation system was used for metallization of Pt. The vacuum before evaporation was 10^{-6} mbar and this would increase to 10^{-5} mbar during deposition. After contact formation, current-voltage (*I-V*) and capacitance-voltage(*C-V*) measurements were performed to assess the quality of the diodes and to determine the free carrier density of Si. It was found that the free carrier density of the EPI Si was 3.5×10^{15} cm^{-3}. *I-V* and *C-V* measurements were repeated after every annealing cycle in Ar gas, for ten minutes from 50°C to 600°C in steps of 50°C. The diodes were irradiated with electrons from a Sr-90 source with a dose of up to 1×10^{15} cm^{-2}. Conventional DLTS was used to study defects introduced during the metallization and irradiation processes. High resolution Laplace DLTS was used to separate the conventional DLTS signals of defects with closely spaced energy levels. The signatures of the defects for electron traps, E_γ and their apparent cross-section σ_a were determined from Arrhenius plots of $\ln(T^2/e)$ versus $1000/T$, where e is the electron emission rate and T is the measurement temperature.

3. Results and Discussion

I-V characteristics of the diodes presented here are deduced from the thermionic emission current-transport model [1]. Figure 1 shows the semilog forward and reverse bias I-V characteristics of the samples in the annealing temperature range 100°C to 600°C. The forward I-V characteristics of the diodes annealed at temperatures up to 100°C show that the diodes were stable at lower voltages and suffer the series resistance effects at voltages higher than 0.5V. Series resistance increases sharply as the annealing temperature increases. Diodes annealed at temperatures higher than 250 °C suffer series resistance at voltages lower than 0.3 V. Figure 2 shows the graph of SBH and reverse leakage current at -1V as a function of annealing temperature. The reverse leakage current increased with increasing annealing temperature, from 9.4×10^{-4} μA to 7.0×10^{-2} μA. Throughout the annealing process the reverse leakage current at -1V remains in the same order of magnitude of μA. At about 300°C, the Schottky barrier height drops significantly while the reverse leakage current at -1V reaches its highest value.

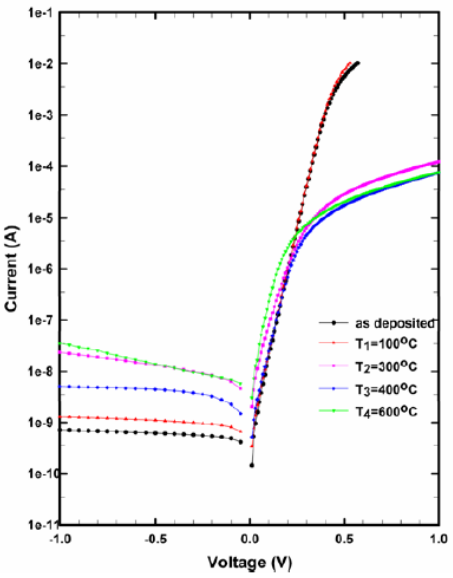

Figure 1: The I-V characteristics of SBD of Pt/n-Si(111) after isochronal thermal treatment at different annealing temperatures

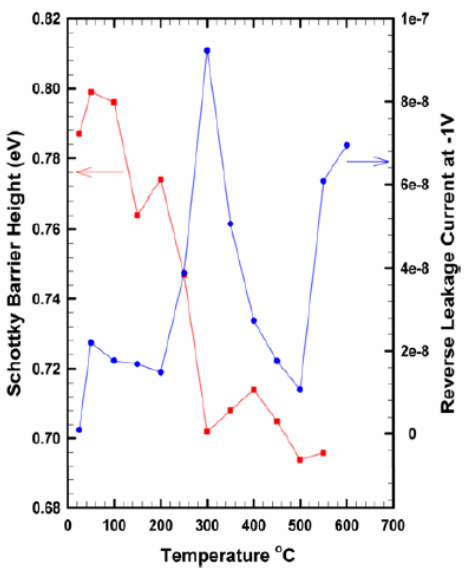

Figure 2: SBH and reverse leakage current at -1V factor as a function of temperature

Figure 3 shows the plots of Pt/n-Si Schottky barrier reverse biased C^{-2}-V characteristics at 1.0 MHz for different annealing temperatures. The plots of C^{-2} as a function of reverse bias voltage are near linear, indicating the formation of Schottky diode and constant non-compensated ionized donor concentration [8]. The SBH of the C^{-2}-V plots were found to be 0.88 eV before annealing while the I-V barrier height was 0.80 eV. Due to different nature of measurements techniques, SBH obtained by I-V and C-V are not the same [1]. Figure 4 shows the SBH and the ideality factor as a function of annealing temperature. The Schottky barrier height (SBH) deduced from the thermionic emission current model, decreased from 0.80eV to 0.70 eV, while the corresponding ideality factor increased from 1.02 to 2.61 as the annealing temperature increased. At temperatures between 240°C and 260 °C there appears a clear transition for the diodes where the ideality factor, SBH and the reverse leakage current at -1V changes.

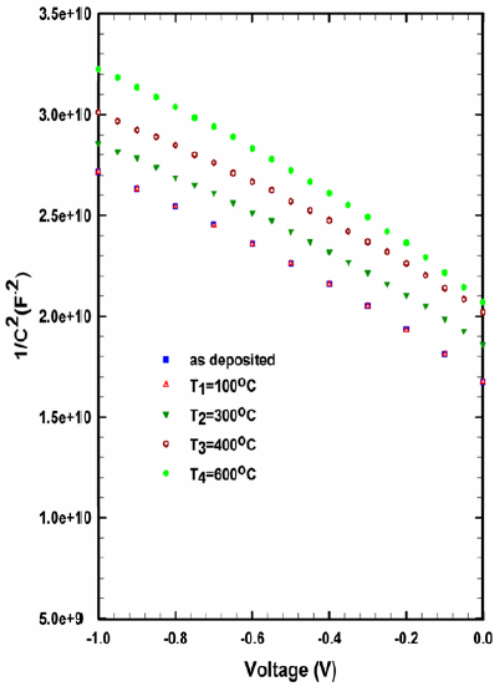

Figure 3: The C-V characteristics of SBD of Pt/n-Si(111) after isochronal thermal treatment at different annealing temperatures

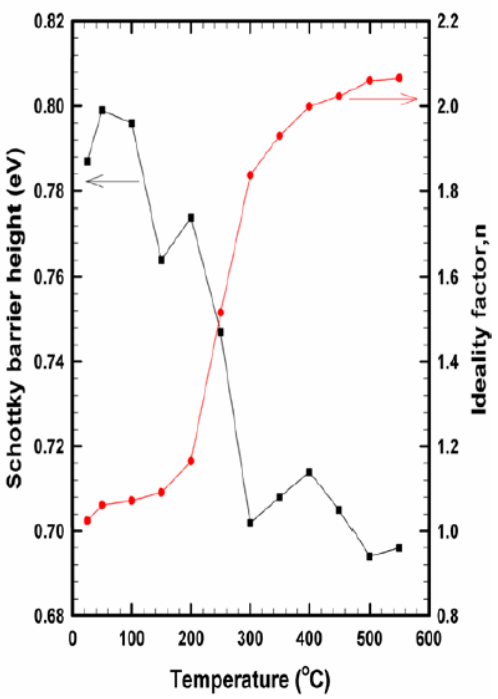

Figure 4: SBH and ideality factor as a function of temperature

We suggest that there is significant reaction between Si and Pt to form a Pt-Si intermix (25°C to 200°C), Pt_2Si (210°C to 280°C) and PtSi (280°C and 350°C). The changes in both SBH and ideality factor coincides with these three regions of Pt-silicidation: between 25°C to 200°C, 200°C to 300°C and 300°C and 550°C, as shown in Fig 4. It has been reported that Pt-Si starts forming at room temperature because of Pt atoms attaching themselves to Si atoms via the Si dangling bonds [10]. In addition, Larrieu et al has reported on the Pt-Pt_2Si-PtSi reaction chain completed within 2 minutes in the temperature range 300°C, 400°C and 500°C [11]. Furthermore, platinum silicides compounds are reported to grow sequentially as the temperature increases. Pt_2Si phase grows between the 210°C and 280°C due to the diffusion of Pt atoms into bulk Si, a process that continues until all the Pt is depleted from the surface [10]. PtSi forms between 300°C and 350°C, starting from the interface between Pt_2Si and Si, by in-diffusion of Si atoms into Pt_2Si lattice. This process is very rapid and comes to completion in about 2 minutes at 350°C [12]. In this work, the diode characteristics show that there Pt on Si formed a rectifying metal contact where the diodes characteristics followed a known pattern where SBH decreases with increasing temperature and the ideality factor increases with increasing temperature. The SBH, ideality factor and reverse leakage current at temperatures between 240°C and 260°C shows that there is a transition of the metal contacts, where Pt_2Si formed. The ideality factor is lowest at temperature range 50°C to 200°C and increases sharply from 200°C to 300°C, and then stabilizes after 300°C, further evidence due to different phase of silicide. The reserve leakage current

is lowest at lower annealing temperatures, but increases immediately with increasing temperature. We have found that Pt_2Si is a more stable compound for metal contacts for devices operating at lower temperatures while PtSi is suitable for devices operating at higher temperatures. In the case of solar cells which are exposed to radiation where temperatures fluctuate, a further study of PtSi as contact will be investigated.

Since we will be comparing the defects introduced during electron beam deposition (EBD) with those introduced by high energy (MeV) electrons, we first discuss the latter defects in n-type Si. High energy electron irradiation of Si introduces single vacancies and self interstitials that are mobile at room temperature [13]. These defects are created when the atoms are displaced by elastic scattering of the high-energy electrons. If a mobile interstitial moves next to a substitutional carbon (C_s) in the Si lattice, it may replace C_s to create C_i, which is also mobile at room temperature [14]. The DLTS spectrum that we record after room temperature irradiation will therefore contain the products that form when vacancies, interstitials and C_i form when reacting with each other (V_2, C_iC_s,) and with impurities in the lattice (VP, VO, C_iP_s) [15].

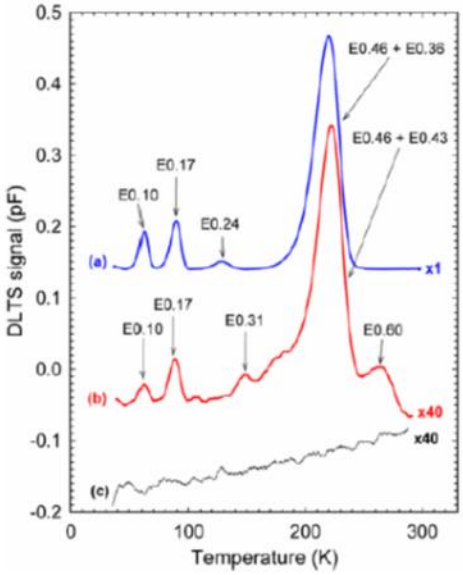

Figure 5: DLTS spectra of EPI n-Si: (a) Irradiated with MeV electrons; (b) Pt Schottky diode deposited by EBD, (c) control spectrum of resistively deposited Schottky diode.

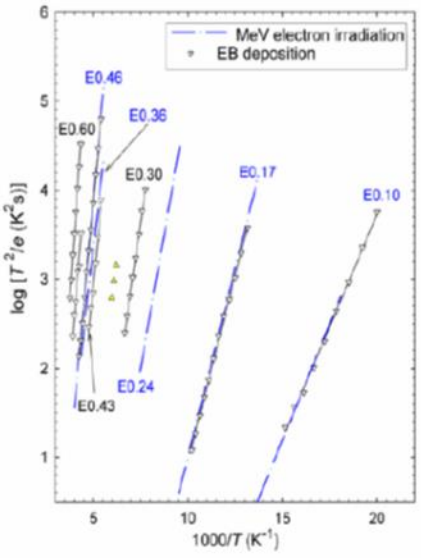

Figure 6: Arrhenius plots for defects introduced by: MeV electron irradiated n-Si (blue dot-dash line); and electron beam deposition (down triangles).

Curve (a) in Fig. 5 is the DLTS spectrum of MeV electron irradiated EPI n-Si recorded directly after irradiation with a fluence of 10^{15} e^- cm^{-2}. It contains at least four DLTS peaks. From the Arrhenius plots where the signatures of these defects were determined (Fig. 6), these peaks are identified as E0.10 (C_i), E0.17 (superposition of A-center (VO) and C_iC_s), E0.24 ($V_2^{=/-}$) and the superposition of E0.46 + E0.36 [13]. Here the E0.46 and E0.36 contributions to the peak at 220 K were determined by high resolution Laplace DLTS measurements. E0.46 is the VP or E-centre, while E0.36 has a similar signature as one of the metastable components of the C_iP_s centre [17]. The concentration ratio of VP to E0.36 is about 5:2. The VP + E0.36 peak also contains a small contribution due to the $V^{-/0}$ but this is too small to be distinguished from the two main peaks (VP and E0.36).

The DLTS spectrum recorded from Pt Schottky contacts that were fabricated by EBD, without any intentional shielding, is shown in curve (b) of Fig. 5. The similarities between some of the defects introduced by EBD and by MeV electron irradiation are evident. Both processes introduce E0.10 (C_i), E0.17 (VO + C_iC_s) and E0.46 (VP) [13 – 17]. This correspondence is confirmed by the Arrhenius plots in Fig. 6. From the Laplace DLTS spectra it was found that EBD does not introduce the E0.36 defect, but instead a defect peak E0.43 of which the DLTS peak also overlaps with that of the E0.46 (VP) peak. From the spectra in Fig. 5 it is also evident that EBD introduces at least two other defects not seen after MeV electron irradiation: E0.30 (similar, but not the same, signature as VOH [19]) and a defect E0.60. This latter defect consists of two closely spaced levels (see the Arrhenius plots in Fig. 6). This defect was also not observed in all EBD samples. It is also noteworthy that no divacancies ($V_2^{=/-}$) in measurable concentrations could be detected in samples prepared by EBD. Previously, a defect with very similar properties to $V_2^{=/-}$ was reported to be introduced after EBD of metal contacts on CZ Si [5].

4. Conclusions

Pt Schottky barrier diodes were fabricated onto n-Si(100) using electron beam deposition. The behaviour of the Schottky barrier diodes (SBD) was investigated under various annealing conditions. The variation of SBH and ideality factor with annealing temperature can be attributed to interfacial reactions of Pt and n-Si(100) and the subsequent formation of platinum silicides. The electrical properties of the Pt Schottky barrier diodes revealed the as deposited ideality factor of 1.02 and SBH of 0.80 eV. Pt_2Si was formed at temperatures between 210°C and 280°C with ideality factor increasing to 1.16 and SBH decreasing to 0.77 eV. At 300°C, PtSi has formed increasing the ideality factor to 1.83 while the SBH decreased to 0.70 eV. DLTS revealed that electron beam deposition introduced defects which were identified as the E-centre (VP centre), the A-centre (VO centre), the interstitial carbon (C_i) and the interstitial carbon-substitutional carbon (C_iC_s) pair.

Acknowledgements

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5.4 Defect Studies

5.4.1 Introduction

In this section, results obtained from the electrical characterisation of alpha-particle irradiation and electron beam exposure (EBE) of p-type and n-type Si samples is discussed. Irradiation experiments were carried out on p-type silicon. Aluminium (Al), nickel(Ni) and titanium (Ti) contacts were fabricated on the p-type material.

5.4.2 Alpha particle irradiation

Al and Ti contacts fabricated on the p-type Silicon samples were irradiated with alpha particles using the americium 241 foil at room temperature. Alpha particle irradiation was achieved by making use of a 5.4 MeV Am-241 radioactive source with a fluence rate of $7 \times 10^{6}\text{cm}^{-2}$. The aluminium and titanium samples were irradiated for 30 minutes at first, the fluence was $1.3 \times 10^{10}\text{cm}^{-2}$. *I-V* measurements, *C-V* measurements and DLTS were done after each irradiation.

5.4.3 The Current-Voltage Characteristics of Aluminium Schottky Contacts

The *I-V* characteristics of the Al Schottky contacts prior to and after α-particle irradiation are shown in figure 5-8. The as deposited sample produces a linear forward *I-V* curve. At this point the thermionic emission model can be used to explain the transport mechanism at the metal-semiconductor interface. The forward *I-V* curves obtained after irradiation deviate from linearity as the time of exposure to irradiation of the sample increases. The results obtained maybe due to defects produced by irradiation which may lead to generation recombination current therefore the non-linear curves at low voltages. The ideality factor increases tremendously from 1.36 to 5.68. This value is very large and illustrates that there could be the contribution of generation recombination current.

Barrier height is modified as the irradiation fluence increases. The *C-V* SBH increases with increasing radiation fluence as shown in table 5-2. The SBH increases for p-type Si due to damage [90]. The reverse leakage current, measured at -1V, increases from $1.44 \times 10^{-8}\text{A}$ before irradiation to $7.2 \times 10^{-5}\text{A}$ after irradiation with an influence of $5.1 \times 10^{-10}\text{cm}^{-2}$. The increase in the reverse leakage current can be associated with defect formation where introduced recombination centres are responsible for the increase in leakage current. This could also be a consequence of interface states present at the metal-semiconductor interface or a non-uniform thin oxide layer at the interface.

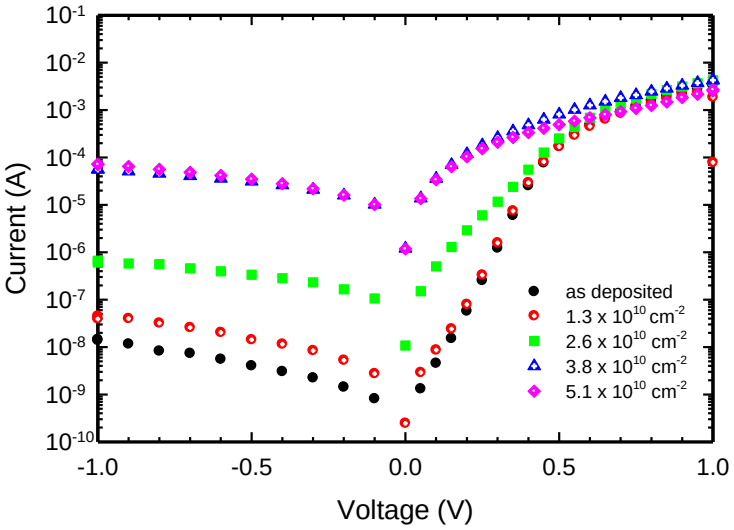

Figure5-14: Semilogarithmic plot for forward and reverse I-V characteristics for the Al/p-Si contacts before and after α-particle irradiation up to a fluence of $5.1 \times 10^{10} cm^{-2}$.

Before irradiation the value obtained was $2.4 \times 10^{15}\text{cm}^{-3}$. As the irradiation fluence increased, the free carrier density decreased at a fluence of $1.3 \times 10^{10} cm^{-2}$ to $2.3 \times 10^{15}\text{cm}^{-3}$. It remained at this value for the consequent two fluences then it decreases to $2.2 \times 10^{15}\text{cm}^{-3}$ at a fluence of $5.1 \times 10^{10}\text{cm}^{-2}$.

Table 5-3: Parameters obtained from *I-V* and *C-V* measurements as the irradiation fluence was increased.

Fluence $(\mathbf{cm^{-2}})$	n	I-V SBH (eV)	C-V SBH (eV)	I_R at -1V (A)	Free carrier density $(\mathbf{cm^{-3}})$
0	1.36	0.81	1.25	1.4×10^{-8}	2.4×10^{15}
$\mathbf{1.3 \times 10^{10}}$	1.43	0.79	1.20	3.9×10^{-8}	2.3×10^{15}
$\mathbf{2.6 \times 10^{10}}$	2.55	0.64	1.24	6.7×10^{-7}	2.3×10^{15}
$\mathbf{3.8 \times 10^{10}}$	4.30	0.52	1.32	5.6×10^{-5}	2.3×10^{15}
$\mathbf{5.1 \times 10^{10}}$	5.68	0.51	1.30	7.2×10^{-5}	2.2×10^{15}

5.4.4 DLTS Results

DLTS was conducted on the Al/p-Si as deposited and irradiated samples in the temperature range 30-300 K. A reverse bias of -2V was maintained while a filling pulse of 0.3V was applied with a pulse width of 2 ms. The DLTS spectra obtained are shown in figure 5-10. Three energy levels were introduced by α-particle irradiation. Figure 5-11 illustrates the Arrhenius plots obtained from L-DLTS. These hole traps were: H(0.16), H(0.33) and H(0.52). H(0.33) has been identified as the interstitial carbon (C_i) related defect [90]. It is a result of induced damage and can only be explained by the presence of donor-like traps [90]. The capture cross-section was calculated to be 1.6×10^{-19} cm^2 from the Arrhenius plot shown in figure 5-11. Auret *et al.* observed a defect in p-type silicon with the same activation energy in samples that had been fabricated with titanium contacts using the resistive deposition method [91]. Defects with similar activation energies have been identified in literature. They are all related to the residual carbon impurity which has been reported to form complexes directly with radiation-produced primary defects or with secondary defects induced by radiation damage [92, 93]. These defects include the interstitial-carbon-interstitial-oxygen $(C_i - O_i)$ complex (C(3) centre) [92], the carbon-oxygen-vacancy complex (the K centre) [94, 95] and the interstitial-substitutional-carbon complex $(C_s - C_i)$ [93, 96, 97]. In their study, Asghar *et al.* observe that the 0.35 eV defect annealed at approximately 400°C in agreement with the literature of similar defect levels E_V+0.38 and E_V+0.33 [94, 95]. These reports suggest that this level originates from the carbon-oxygen-vacancy $(C - O - V)$ complex. However, studies by Song *et al.*[98] strongly suggest this defect to be associated with $C_i - O_i$ complex. This deep level would be expected to strongly depend on the material and sample since unintentional carbon and oxygen contamination could vary with the material as well as device processing.

H(0.52) may have been an EBD process induced defect and it is boron impurity related [99]. It is not clear what the identity of H(0.16) is.

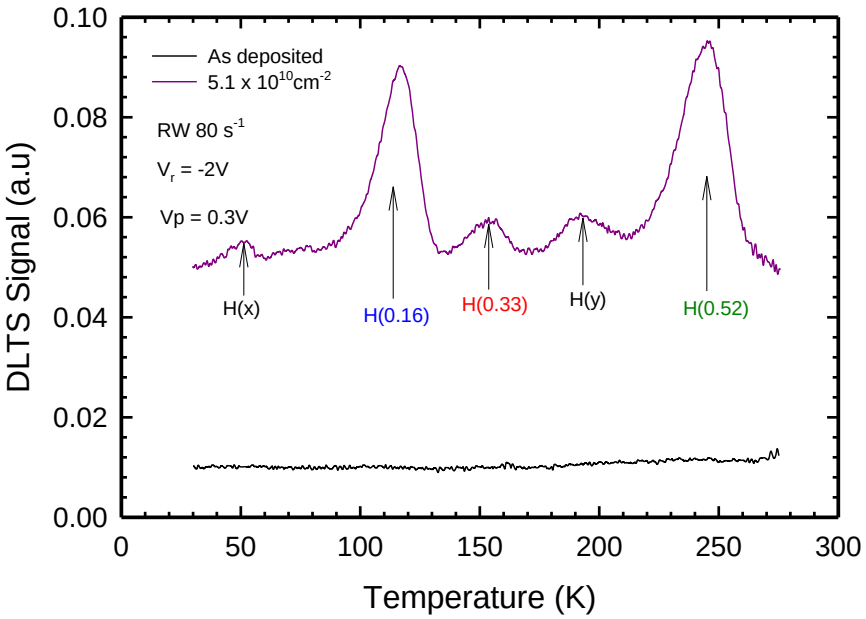

Figure 5-15:DLTS spectrum illustrating the as deposited sample and defects obtained after alpha particle irradiation at a fluence of $5.1 \times 10^{10}\text{cm}^{-2}$ *on Al/p-Si.*

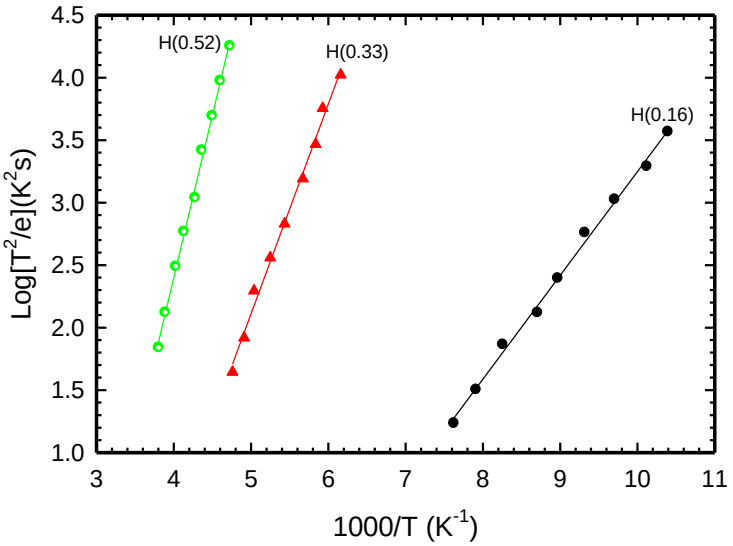

Figure 5-16: Arrhenius plots obtained using the L-DLTS technique on Al/p-Si.

5.4.5 The Current-Voltage Characteristics of Titanium Schottky Contacts

The *I-V* characteristics of the Ti Schottky contacts prior to and after α-particle irradiation are shown in figure 5-11. The as deposited sample produces a linear forward *I-V* curve. At this point the thermionic emission model can be used to explain the transport mechanism at the metal-semiconductor interface. The two curves obtained from the first two fluences suggest that the sample was resistant to the α-particle radiation exposure. The SBH increases slightly from the as deposited to a fluence of $5.1 \times 10^{10}\text{cm}^{-2}$. Here the SBH increased from 0.80 eV to 0.83 eV. The forward *I-V* curves deviate from linearity as the time of exposure to irradiation of the sample was increased to a fluence of $2.1 \times 10^{11}\text{cm}^{-2}$, that is exposure for 8 hours. After this fluence the SBH did increase significantly to 1.6 eV. The results obtained maybe due to defects produced by irradiation which may lead to generation recombination current therefore the non-linear curve at low voltages.

The reverse leakage current of the Ti Schottky diodes increased slightly between the as deposited and the fluence of $2.6 \times 10^{10}\text{cm}^{-2}$. The leakage current increases between the fluence of 0 and $2.6 \times 10^{10}\text{cm}^{-2}$ in general, there is a small increase in the value of leakage current from 9.7×10^{-7}A to 1.2×10^{-6}A. The effects of irradiation did not seem to affect the reverse leakage current of the Ti Schottky contacts significantly.

Table 5-4: Parameters obtained from *I-V* and *C-V* measurements on α-particle irradiation on the Ti contacts.

Fluence (cm^{-2})	n	*C-V* SBH (eV)	I_R at -1V (A)	Free carrier density (cm^{-3})
0	1.58	0.80	9.7×10^{-7}	2.3×10^{15}
$\mathbf{2.6 \times 10^{10}}$	1.21	0.81	9.9×10^{-7}	2.3×10^{15}
$\mathbf{5.1 \times 10^{10}}$	1.24	0.83	1.2×10^{-6}	2.2×10^{15}
$\mathbf{2.0 \times 10^{11}}$	1.72	1.57	1.2×10^{-6}	2.2×10^{15}

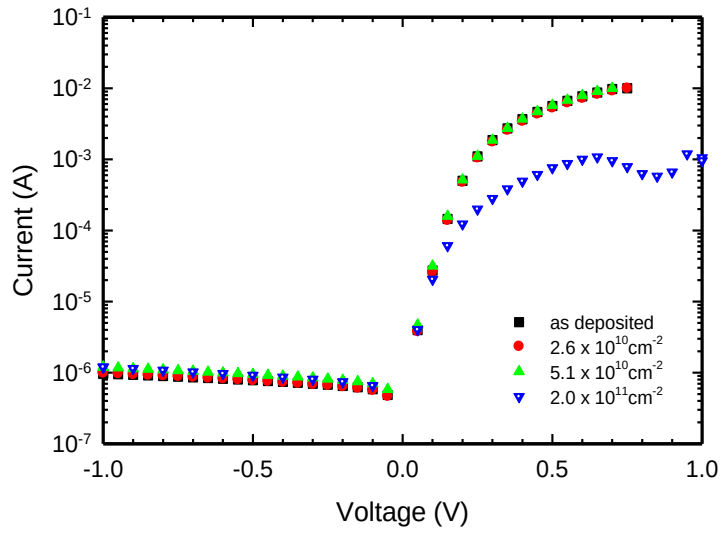

Figure5-17: Semilogarithmic plot for forward and reverse I-V characteristics for the Ti/p-Si contacts before and after α-particle irradiation up to a fluence of $2.0 \times 10^{11} cm^{-2}$.

5.4.6 DLTS Results

Figure 5-18 shows the DLTS spectra obtained before and after α-particle irradiation. The spectra illustrate that there is an increase in defect peak intensity for all defect levels identified in this experiment. After exposure to α-particles with a fluence of $1.3 \times 10^{10} \mathrm{cm}^{-2}$ only the defect H(0.19) is measured. Its concentration increases as the irradiation fluence increases. The intensity of the other defect levels namely: H(0.10) , H(0.42) and H(0.58) start to appear at a fluence of $2.6 \times 10^{10} \mathrm{cm}^{-2}$ and $5.1 \times 10^{10} \mathrm{cm}^{-2}$ respectively. H(0.58) seems to be a EBD process induced defect and it is boron impurity related [99].

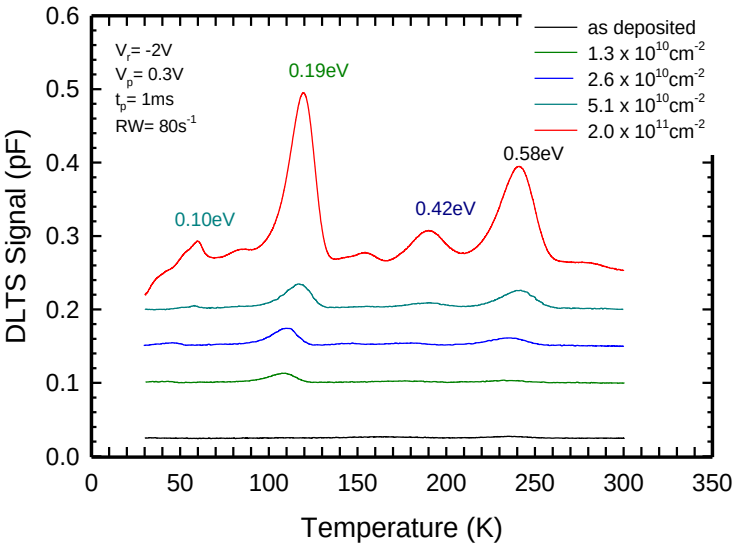

Figure 5-18:DLTS spectra obtained after Ti/p-Si was exposed to alpha particle irradiation.

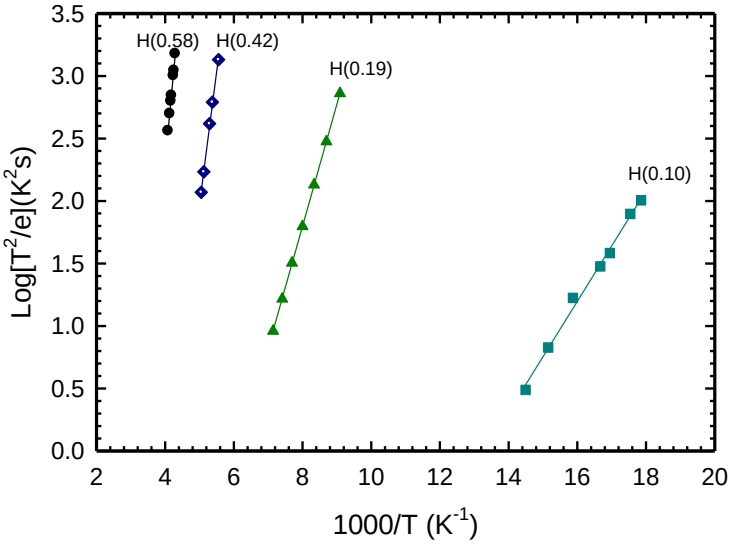

Figure 5-19: *Arrhenius plots obtained using the L-DLTS technique on Ti/p-Si contacts.*

5.5 Electron Beam Exposure

Vacuum pumping was carried out by a dry pump in series with a turbo molecular pump and to lower the H_2 concentration. Tungsten (W) was evaporated in the chamber with the sample rotated away from the evaporation source. While the pre-deposition vacuum was typically 5×10^{-7} mbar, this soon went up to approximately 3×10^{-6} mbar during the evaporation. As

the vacuum conditions vary greatly during EBD, forming gas H15 with a composition of N_2:H_2 of 85%:15% by volume was also used to raise the pressure in the vacuum chamber to 10^{-4}mbar and kept constant during processing of select samples. EBE of samples and EBD of contacts were made using a 10kV source (MDC model e-Vap 10CVS) with the samples positioned 50cm above the crucible. Ni diodes were used for all the samples prepared for this study as this metal can be evaporated resistively, a process that is known to not introduce defects in concentrations measurable by deep level transient spectroscopy (DLTS) [100]. A control sample was prepared where aluminium (Al) contacts were resistively deposited on the p-type epitaxial material without using the EBE technique. A sample with Al contacts irradiated with alpha-particles at a fluence of 5.1×10^{-10} cm^{-2} was also used in this study for comparison.

5.5.1 p-type Silicon Results

In the EBE experiment only one defect level was detected. The only defect level observed has an activation energy of 0.546eV with a capture cross-section of $6.6 \times 10^{-14}cm^2$. This defect had an activation energy similar to the I-defect. Pintilie *et al* observed a similar energy 0.545eV with a capture cross-section $1.7 \times 10^{-15}cm^2$ and $9.0 \times 10^{-14}cm^2$ after exposing their samples to high irradiation fluences. The defect level was detected using thermally stimulated current (TSC) [101]. The H(0.55) defect is aligned to the defect H(0.52) as shown in figure 5-16. This defect was introduced by alpha-particle irradiation. It had an apparent capture cross-section of $1.7 \times 10^{-14}cm^2$ and it temperature peak was at 246°C. Nyamhere et al. measured a defect they referred to as HB4, a defect having an apparent cross-section of 1.3×10^{-13} cm^2. It had an activation enthalpy of 0.54eV and its peak temperature was at 240°C. This peak temperature was similar to that of H(0.55), which lay at 242°C. HB4 was attributed to interstitial boron-substitutional boron-hydrogen (B_i-B_s-H) complex [99, 102-104].

For Ni contacts fabricated using EBD, spectrum (d) in figure 5-15, we observed the defect level H(0.59). This defect had a similar activation enthalpy and apparent capture cross-section as that of HB5, a defect observed by Nyamhere *et al.* [99]. In their study of EBD processed induced defects and their annealing behaviour, it was proposed that the breakup of the 0.54 eV defect level was responsible for the introduction of the 0.59eV level. This defect was boron related [99].

From the spectrum shown in figure 5-15 (b), for the alpha-particle irradiated Al contacts, the hole traps observed were: H(0.16), H(0.33) and H(0.52).The defect level H(0.33) was identified as the interstitial carbon (C_i) related defect. It was a result of induced damage and could only be explained by the presence of donor-like traps [90].

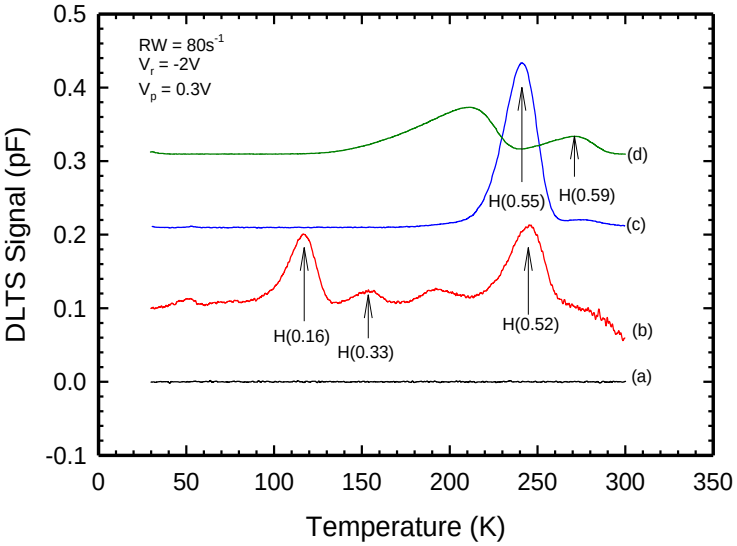

Figure 5-20: DLTS spectra for (a) is a control spectrum measured from Al Schottky diodes fabricated using resistive deposition, (b) α-particle irradiated Al Schottky diodes , (c) Ni Schottky diodes fabricated after EBE and (d) Ni Schottky diodes fabricated using the EBD method.

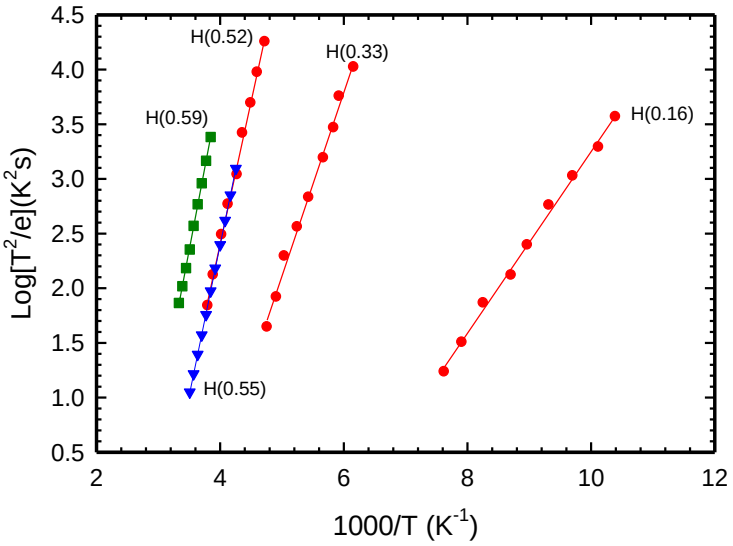

Figure 5-21: Arrhenius plots obtained after: samples exposed to electron beam conditions (EBE) thereafter Ni Schottky diodes fabricated (down triangles); α-particle irradiated Al Schottky diodes (circles) and Ni Schottky contacts fabricated using the EBD method (squares).

5.5.2 Depth Profiling

The aim of depth profiling was to find the defect concentration as a function of depth for individual defects. Fixed bias-variable pulse Laplace-DLTS depth profiling [105, 106] was used to measure the depth distribution of the defects investigated in this study. For the defect level H(0.55), Laplace-DLTS was used to investigate its depth profile. Temperature was kept constant at 250 K. The measurements were first done at a reverse bias of -2 V while varying the filling pulse. The experiment was repeated for larger values of reverse bias down to -5V while varying the filling pulse. Figure 5-17 illustrates the results obtained. As we probe deeper into the bulk away from the junction, it can be seen that the H(0.55) defect concentration is still visible even at a depth of 1.6 μm from the junction. This implies that the damage caused by EBE extends to a significant depth into the bulk.

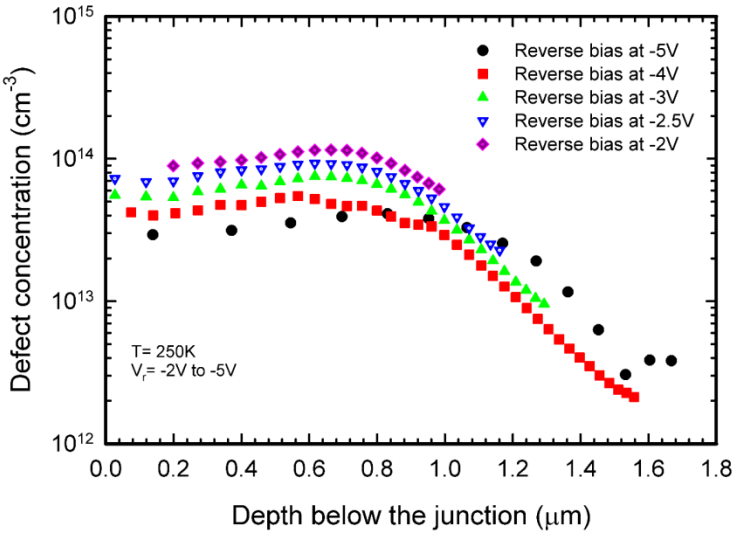

Figure 5-22: Depth profile of the H(0.55) defect detected on EBE Ni/p-Si contacts at different reverse bias conditions.

A comparison study was conducted for the three techniques. For each defect, the temperature was kept constant, the reverse bias of -2V was maintained while varying the filling pulse. Figure 5-18 illustrates the results obtained. Depth profiling of the defects showed that as we probed deeper into the bulk away from the junction, the H(0.55) defect decreased from $1 \times 10^{14}\text{cm}^{-3}$at the metal-semiconductor interface to $6 \times 10^{13}\ \text{cm}^{-3}$about 0.8$\mu$m below the interface. The defect level H(0.59) introduced by EBD, decreased from $2 \times 10^{14}\ \text{cm}^{-3}$at the interface to about $5 \times 10^{13}\ \text{cm}^{-3}$at 0.4$\mu$m below the junction. In the case of the defect level H(0.52), the defect concentration showed a decrease from $4 \times 10^{13}\ \text{cm}^{-3}$at the junction to $1 \times 10^{13}\ \text{cm}^{-3}$ at approximately 0.8μm below the junction. This implies that the damage caused by EBE extends deeper into the material compared to EBD. This is because during EBD, the metal deposited shields the semiconductor material from the energetic particles which would otherwise penetrate deeper into the material.

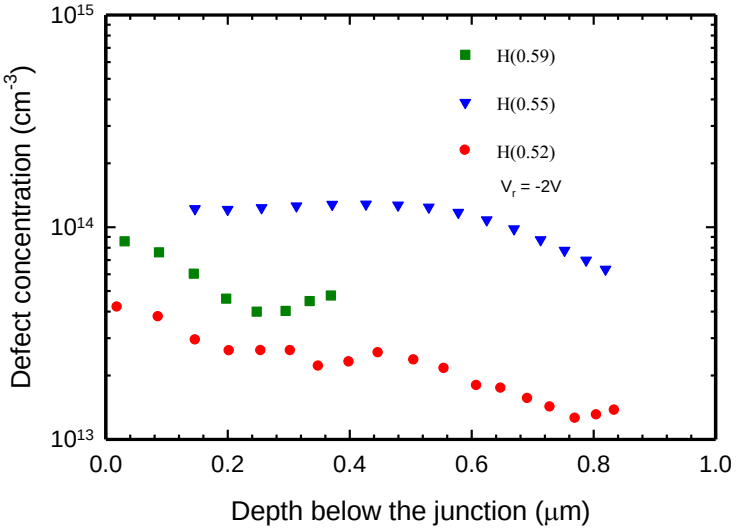

Figure 5-23: Depth concentration profiles of H(0.59) a defects introduced by EBD,H(0.55) is a defect introduced during EBE and H(0.52) is a defect level introduced by α-particle irradiation.

5.5.3 n-type Silicon

The DLTS spectrum of the defects induced by electron beam exposure (EBE) is shown in figure 5-18. The defect energy levels were calculated from the Arrhenius plots in figure 5-19.

Table 5-5: Parameters obtained from Arrhenius plots calculations and the DLTS spectrum using a rate window of $80s^{-1}$.

$E_T(eV)$ L-DLTS	$\sigma_a cm^2$	T^a_{peak}	Defect structure	References
E(0.11)	1.6×10^{-15}	64	$C_iC_s(-/0)B$	[45]
E(0.17)	5.7×10^{-15}	92	$C_iC_s(-/0)A$	[45]
E(0.21)	3.4×10^{-14}	105	?	[96, 107]
E(0.41)	8.2×10^{-13}	175	$V_2^{(-/0)}$	[108, 109]
E(0.45)	3.9×10^{-15}	225	VP (E centre)	[45]
E(0.47)	9.4×10^{-15}	260	?	
E(0.44)	5.5×10^{-18}	292	?	[45]

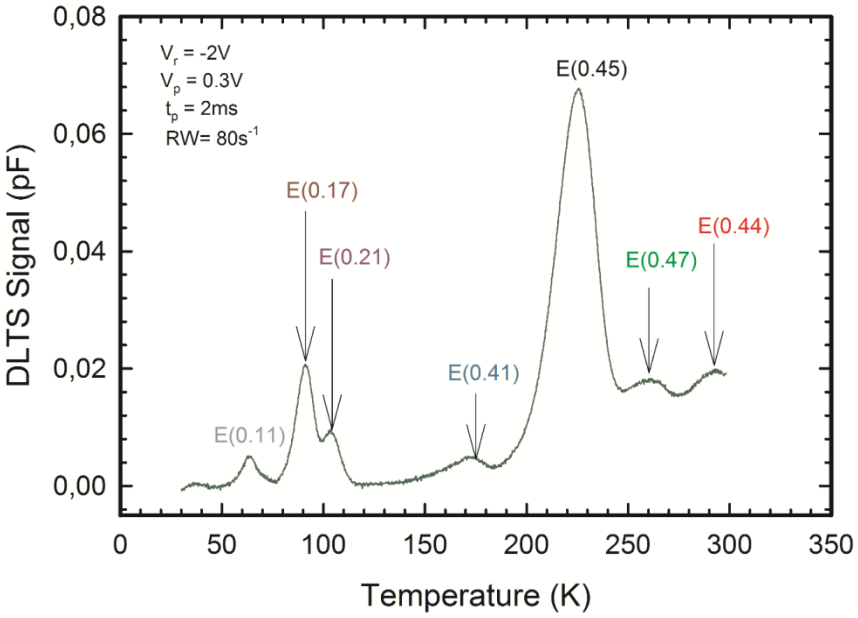

Figure 5-24: DLTS spectrum obtained from EBE Au/n-Si contacts.

L-DLTS was used to identify defects in n-type silicon introduced as a result of electron beam exposure. The defect levels E(0.11) and E(0.17) seem to be associated with the carbon interstitial- substitutional pair C_iC_s. The C_iC_s-defect is a bistable defect with amphoteric character in both defect configurations. The transition from configuration A to B and vice versa is possible by a simple bond switching transformation [98] . A defect level E(0.21) was observed. Asghar *et al* also measured and calculated E(0.21) but the defects structure is not clear [107]. Kimberling linked it to the emission of a hole by a positively charged state of the divacancy but this is debatable [96]. E(0.41) and E(0.45) were also observed and these were associated with a divacancy and a boron interstitial respectively. E(0.47) was observed but its structure is not yet known. Finally, the level E(0.44) was not established.

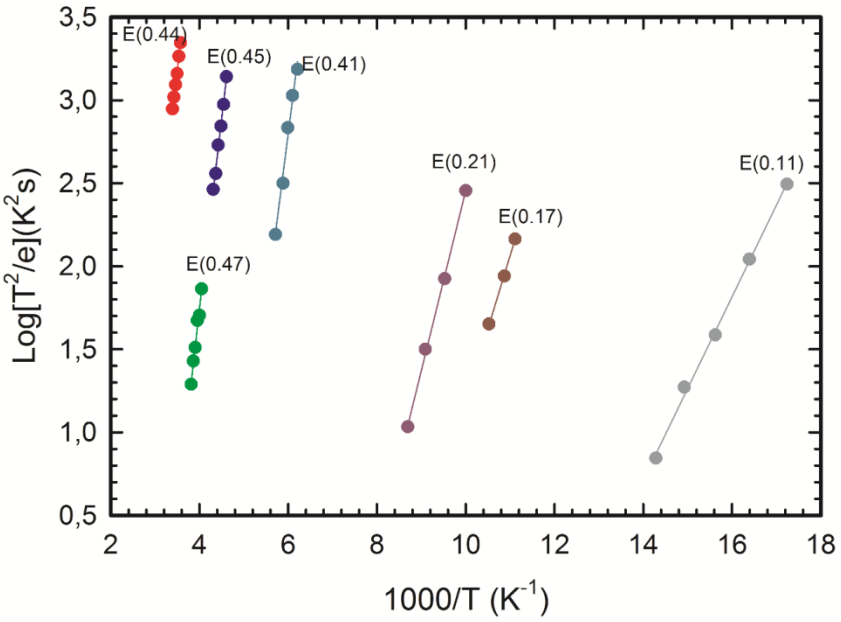

Figure 5-25: Arrhenius plots of EBE Au/n-Si contacts.

From this study we deduced that more defects are detected in n-type material than in p-type material when the EBE method is used. EBE induced defects seemed to extend deeper into the substrate than the defects introduced by EBD.

Chapter 6

Conclusions and future work

This dissertation contains work covered on silicides and defects induced by alpha-particle irradiation and electron beam deposition. Conclusions specific to each experiment are summarised in this chapter.

Silicide Characterisation

Pd and Ti Schottky barrier diodes were fabricated onto n-Si (111) and p-Si (111) respectively, using electron beam deposition. For the n-type material, the behaviour of the Schottky barrier diodes (SBD) was investigated using annealing temperatures from 200°C to 700°C. The variation of SBH and ideality factor with annealing temperature can be attributed to interfacial reactions of Pd and n-Si (111) and the subsequent formation of palladium silicides. The electrical properties of the Pd Schottky barrier diodes revealed the as deposited ideality factor of 1.2 and SBH of 0.69 eV. The wPd_2Si phase was formed at a temperature of 300°C with ideality factor increasing to 1.6 and SBH decreasing to 0.64 eV. The RBS results suggest that Pd_2Si is the most stable silicide phase. The RBS reveals that silicide formation begins to occur at 250°C. The SEM images illustrate that surface roughness increases with increase in annealing temperature.

For p-type material, the reverse leakage current increased with increasing annealing temperature, from 3.77 μA to 8.53 μA. At about 300°C, the Schottky barrier height dropped to 0.55eV while the reverse leakage current at -1 V reached a value of about $6.5 \times 10^{-6}\mu$A. The carrier concentration increased within the temperature range 100°C to 500°C. The *C-V* SBH was found to be 0.57 eV before annealing while the *I-V* barrier height was 0.53 eV. We proposed that at 400°C a titanium silicide may have been formed.

The study seemed to suggest that silicide formation on n-type material occurred at lower annealing temperatures than on p-type material. The Ti contacts on p-type Si degraded at a lower temperature than the Pd contacts on n-type material. Further work must be undertaken to explain these results.

Alpha Irradiation Experiments

The *I-V* characteristics illustrate that the Al contacts' rectification properties deteriorated as the irradiation fluence increased. The as deposited sample showed linear forward *I-V* characteristics with the leakage current at $1.4 \times 10^{-8} A$. The value of the reverse leakage current increases to $7.2 \times 10^{-5} A$ while the forward log *I-V* graphs lost their linearity as the irradiation fluence increases. The DLTS results reveal that three defects were measured. These were hole traps comprising of the defect levels H(0.16), H(0.33), and H(0.52). H(0.33) has been identified as the interstitial carbon (C_i) related defect. It is a result of induced damage and can only be explained by the presence of donor-like traps. It seems that H(0.52) is an EBD process induced defect and it is boron impurity related. The identity of H(0.16) is not clear.

In the case of the Ti Schottky contacts, the as deposited sample produced a linear forward log *I-V* graph. At this point the thermionic emission model can be used to explain the transport mechanism at the metal-semiconductor interface. The two curves obtained from the first two fluences suggest that the sample was resistant to the α-particle radiation exposure. The effects of irradiation do not seem to affect the reverse leakage current of the Ti Schottky contacts significantly. The spectra illustrate that there was an increase in defect peak intensity for all defect levels identified in this experiment. After exposure to α-particles for 30 minutes the only defect measured was H(0.19). Its concentration increased as the irradiation fluence increased. The intensity of the other defect levels namely: H(0.10), H(0.42) and H(0.58) started to appear after exposure for 60 minutes and 120 minutes respectively. H(0.58) seems to be an EBD process induced defect and it is boron impurity related.

Electron Beam Exposure Experiments

In this experiment, n-type and p-type Silicon were exposed to electron beam evaporation conditions without metallisation. For the p-type material, only one defect level was measured. This defect had an activation energy of 0.546eV with a capture cross-section of $6.6 \times 10^{-14} cm^2$. The depth profiling revealed that the H(0.55) defect concentration was still visible even at a depth of 1.6μm from the junction. In comparison to the EBD induced defect H(0.59) seems to extended to a depth of 0.4μm from the junction whereas H(0.55) extended to a depth

of about 0.8μm taking the measurement at -2 V reverse bias. This implies that the damage caused by EBE extends deeper into the substrate than the damage caused by EBD.

In n-type silicon the defect levels E(0.11) and E(0.17) seemed to be associated with the carbon interstitial- substitutional pair C_iC_s . The C_iC_s -defect is a bistable defect with amphoteric character in both defect configurations. A defect level E(0.21) was observed. Asghar *et al* also measured and calculated E(0.21) but the defects structure is not clear . Kimberling et al linked it to the emission of a hole by a positively charged state of the divacancy but this is debatable. E(0.41) and E(0.45) were also observed and the wee associated with a divacancy and a boron interstitial respectively. E(0.47) was observed but its structure is not yet known. Finally, the level E(0.44) is associated with the “E centre”.

From this study we deduced that more defects are detected in n-type material than in p-type material

Future work

Surface and structural characterisation techniques for the study of silicides must be conducted to obtain more conclusive results. Techniques such as XRD and TEM should be employed.

For EBE, other metals should be used as contacts particularly on the p-type silicon.

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