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A novel, flexible Pcell-driven design flow for mm-wave on-chip passives

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***Abstract*—On-chip EM modeling at mm-wave frequencies requires design methods that incorporate the layout and verification macros of IC EDA tools with parameterized EM CAD. We propose a novel, flexible design flow for 3D EM modeling of BEOL structures that allows for parameterized design of BEOL structures using Pcell elements as seed, thereby reducing the time required to generate the full simulation model in EM CAD. The method is illustrated by the co-design of a 94 GHz directional coupler.**

Keywords— Computer aided design; Design automation; millimeter wave integrated circuits; simulation

I. INTRODUCTION

Millimeter wave frequencies have received significant interest as band of choice for future 5G communication networks [1]. A key enabling technology in large scale roll-out is the single-chip transceiver, which requires the integration of numerous passives (eg. couplers and filters) in the back-end-of-line (BEOL) of semiconductor process [2]. To reduce the number of prototyping iterations, these devices need to be modeled and simulated as accurately as possible, making full-wave electromagnetic (EM) simulation imperative [3]. Commercial EM solvers are provided with a computer aided design (CAD) front-end for design capture, and allow the designer to enter the design in a mode most conducive to the type of structure. For planar EM structures, a top-down 2D planar geometry editor is often provided, whereas complex 3D structures require a 3D solids modeling interface.

Another imperative in on-chip passives design is the integration of dedicated integrated circuit (IC) electronic design automation (EDA). The incorporation of IC EDA in on-chip passives ensures verification of foundry layout design rules [4] though integrated design rule checking (DRC). This also gives the designer access to the parameterized cell (Pcell) [5], which is a chip layout macro used to generate artwork for common pre-defined and modelled devices in the semiconductor foundry's process design kit (PDK) [6][5][7].

This need for EM-circuit co-simulation is addressed in the design flow presented in [8], but the proposed solution is limited to verification of the electromagnetic properties of an IC layout generated in an IC EDA tool. Although this is an important step, the design of complex mm-wave passives on-chip requires the use of 3D EM simulation as a *design tool* (similar to what is achieved in the 3D solids modeling interface of an EM CAD package) as opposed to a *verification tool*.

Although some commercial tools already provide a unified interface for both EM CAD and IC EDA (such as Keysight ADS, or the background scripting between Cadence Virtuoso and Ansys HFSS) it is advantageous to have a design flow where this interaction is not required. Herein lies the power of our novel method: that, given a common geometric data interchange format, any two unrelated EM CAD and IC EDA tools may be used.

In this paper, we will first motivate the use of the Pcell as the seed of the design flow, and then state the criteria for using Pcell generated geometry in EM CAD. Based on these criteria, we will propose a novel design flow that incorporates parameterization, and demonstrate it in a practical example. In all cases, Cadence Virtuoso is used as IC EDA tool, with Ansys HFSS for EM CAD

II. THE PCELL AS THE CORE OF THE DESIGN FLOW

The reasons for using the Pcell to create EM CAD layouts are numerous, of which the following are most important:

A. Design rule checks

Layout design rules, as they relate to EM passives on-chip, are rules of minimum and maximum geometric measures for back-end metallization, and are designed to present a compromise between component size, performance, and die yield [4]. Typical design rules include minimum distance between conductors, minimum and maximum width of a conductor, minimum and maximum metallization density across the die, and numerous others.

In a top-end CMOS or BiCMOS process, the multitude of metals and process mask layers lead to rule sets of *several hundred pages*. It is, therefore, unlikely that the BEOL passives designer can keep these rules in mind when capturing data in a 3D EM CAD interface. However, Pcells are programmed to adhere to process design rules, making manual verification unnecessary.

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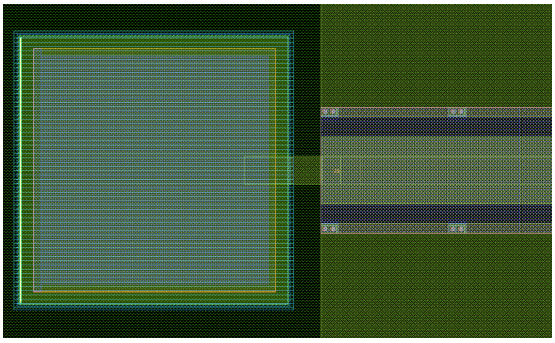

Fig. 1. Layout generated by combining the Pcells for a probe pad and a shielded 50Ω transmission line using IBM 8HP PDK.

B. *Automatic generation of standard geometries*

The 3D EM CAD interface requires the designer to create all required geometry (including the capture of dimensions for layer thicknesses and elevations) from scratch. Although most of the 2D geometry will be unique to that design, there are geometries that are often repeated between designs. These include via stacks to connect different layers, probe pads, transmission lines, shielding, and others, as shown in Fig. 1. Using a Pcell to generate these geometries enables the designer to automatically generate large and intricate sections of geometry using only a few input parameters.

C. *Automated geometry alteration to ensure design rule adherance*

One of the most useful functionalities in Pcells is that it can alter an input geometry to approximate that of the designer's input, but that adheres to the process design rules. A typical example is shown in Fig. 2, where the designer's input of an angled line is approximated by a staircase geometry which meets the design rule requiring only horizontal or vertical edges on metal layers. Also visible are the holes generated in the designed wide metal fill areas, to meet the design rules of maximum metallization width and maximum metallization density. Generating these geometries by hand in an 3D EM CAD environment is time-consuming, and is best achieved by generating the Pcell geometry in IC EAD layout and exporting it to EM CAD.

III. Requirements for expanding on the Pcell-based layout in EM CAD

Although the Pcells generated in IC EDA is fast and convenient to use, it still has to integrate into a 3D EM simulation. This is easily achieved, that the following criteria hold:

A. *Common description of geometric data*

To transfer the Pcell generated geometry to EM CAD, a common description of the geometry is required. The industry standard for transferring IC layout data is GDSII, and is easily imported in most modern EM CAD packages.

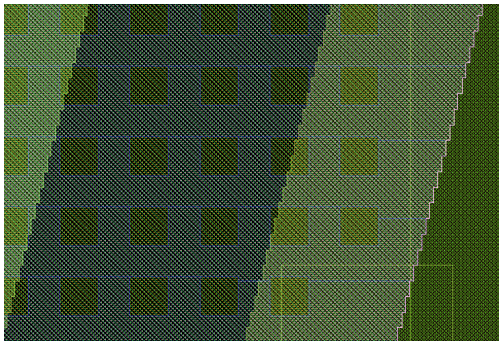

Fig. 2. IC EAD layout showing automatically generated holes and staircase geometries using IBM 8HP PDK.

Apart from the GDSII data itself, the EM CAD data import also requires a GDSII layer map. This layer map should match the layer numbers in the GDSII file to, in the minimum, elevation, thickness, and designation of metal layers (as is done in the Ansys HFSS *.tech* file. This method of import generates static ACIS solids in the 3D EM CAD environment. It also requires that dielectrics and air boxes are drawn in the EM CAD interface, and that all metal and dielectric material properties be assigned per solid.

A preferred import method preserves not only the metal geometry, but also the material properties of both metal and dielectric layers, as well as advanced parameters such as metal edge taper and surface roughness. In the case of HFSS, this is accomplished though a custom formatted XML file, the template of which is readily available.

B. *Post-generation parameterization*

Although using Pcells in an IC EDA tool to generate EM CAD data is fast, the parameterization is lost as soon as the artwork is transferred out of the IC EDA tool to an EM CAD tool, leaving the EM CAD geometry static. In modern EM CAD, it is commonplace to parameterize model geometry, as it allows for tuning and optimization of dimensions based on the numerical EM solver results.

Two modes of parameterization are possible, depending on the type of EM CAD interface used. In the case where the design data is imported in a 3D solids modeling interface, the geometry may be parameterized by applying variable translation / rotation to solids, and variable offset to faces. In case of a 2.5D planar layout environment, the properties of imported shapes and polylines may be edited directly, which means fixed geometric values can easily be edited out and replaced by variables.

C. *Addition of excitation*

Finally, it must be possible to add some form of excitation to the structure once it has been imported and parameterized. In the case of 2D layout editing, only simple lumped / terminal ports may be available. In the case of a 3D solids modeling environment, any number of complex excitations (waveguide

ports, incident farfield, nearfield source) may be applied to the model, which is the main advantage of using 3D solids editing over 2.5D layout editing in EM CAD for BEOL structures. The 3D editing environment also allows for more explicit control over boundary conditions, as well as the inclusion of packaging and other interfering structures.

IV. Proposed Design Flow

Given the ability import, parameterize, and excite Pcell-generated geometry in an EM CAD environment, we can propose the novel design flow in Fig. 3.

As with all EM CAD, initial geometry is first generated through theoretical calculation of geometry based on idealized analytical solutions. Examples of these would be the length of line required to create a half-wavelength resonator, or the line separation to achieve a required coupling value between two lines. Next, appropriate Pcells are used in the IC EDA software to generate the geometry, at which time an initial DRC is conducted. The geometry is then altered and the DRC iterated until all design rules are adhered to, at which time the initial GDSII artwork may be exported by the IC EDA tool.

Depending on the design context, the GDSII file may be imported (using the appropriate layer map interpretation) either in a planar layout or 3D solids modeling EM CAD interface, after which the simulation model is prepared. In the case of 2.5D layout, this only involves adding port excitation and parameterization, whereas 3D solids modeling additional modeling steps as discussed in Section III. After simulation and tuning / optimization to achieve the desired electrical response, the S-parameters may now be exported from the EM CAD tool and re-imported into the IC EDA tool for co-simulation with other PDK elements in a circuit solver.

Once satisfactory co-simulation results are obtained, the parameter changes applied in the EM CAD environment now need to be applied *manually* to the PCells in the IC layout tool by entering new geometric parameter values, since re-importing the GDSII from the EM CAD to IC EDA tools would again lead to static geometry. A final DRC is then conducted, at which the final EM artwork is either confirmed to be design rule compliant or areas of non-compliant geometry are pointed out. These areas, if any, may then be altered in the EM CAD, re-simulated, and then re-checked by DRC, until a final camera-ready GDSII stream is sent for fabrication.

V. Design Example: Quarter-Wave Coupled Line Coupler

As an example of the design flow, we will demonstrate a coupled line coupler as shown in Fig. 4. The coupler's desired response is -15 dB coupling at 94 GHz in a 50 Ohm environment, implemented in microstrip on IBM 8HP between metal layers AM and MQ. Using the Pcells *singlewire*, *coupledwires* and *bend*, an initial circuit simulation in IC EDA (Fig. 4) indicates that the desired response (Fig. 8) is achieved with the initial values of l = 400 µm, w = 18 µm, and s = 14 µm. A layout is then generated, DRC passed, and the layout exported to GDSII. Since no 3D excitation is required, the layout is imported in EM CAD using an appropriate 2.5D stack-up template, and excitation ports applied (Fig. 6).

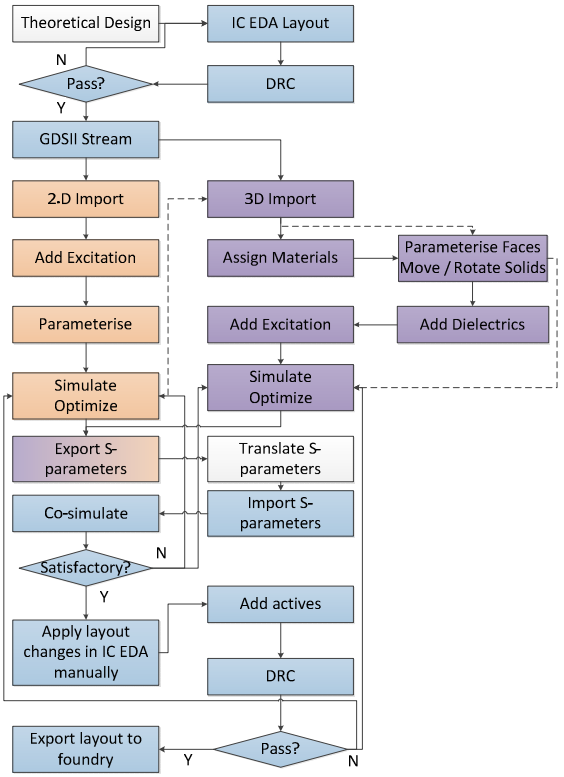

Fig. 3. Proposed IC EDS / EM CAD co-simulation design flow.

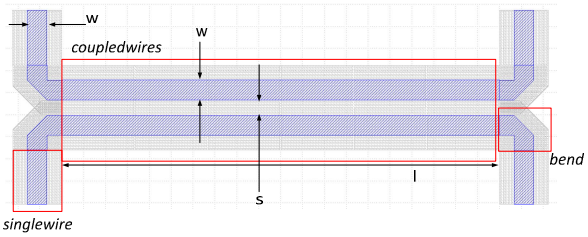

Fig. 4. Layout of quarter-wave coupled line coupler, with constituent Pcells indicated.

The initial 3D EM response (Fig. 8) indicates maximum coupling at 94 GHz and a matched input, but only -15.25 dB of coupling is achieved. This necessitates parameterization of the coupling s distance by variable delta, applied to all geometry in the lower coupled line (Fig. 7).

A subsequent EM parametric sweep of *delta* indicates that the required -15 dB coupling is achieved by reducing s to 13.64 µm, a change that can now be updated in the IC EDA layout by entering a different value in the Pcell properties dialog box. Finally, the second DRC is run and passed, after which the artwork is ready for export to the foundry.

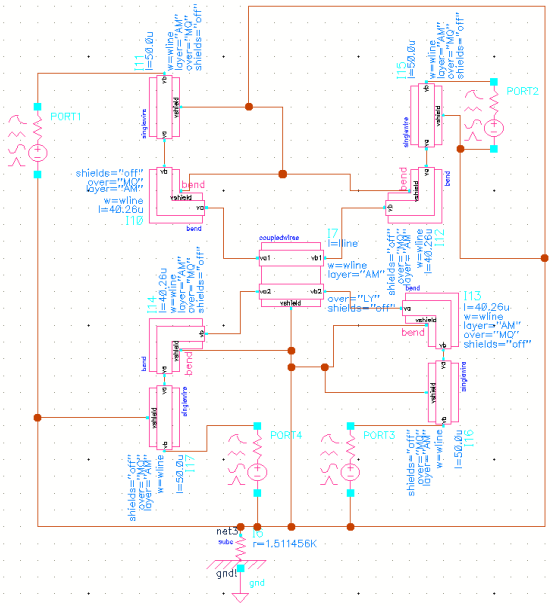

Fig. 5. Circuit simulation using Pcell elements.

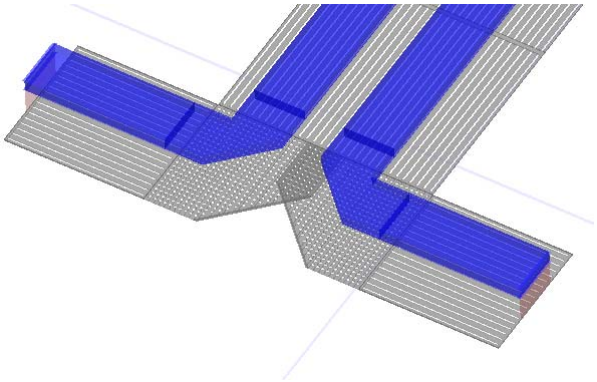

Fig. 6. Imported EM CAD model.

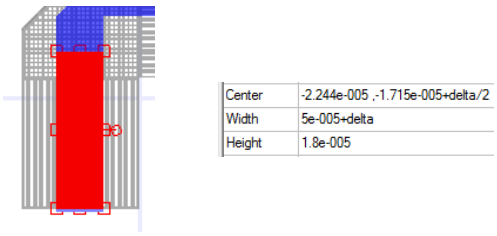

Fig. 7. Layout polygon (left) and properties dialog box (right) indicating parameterized dimensions.

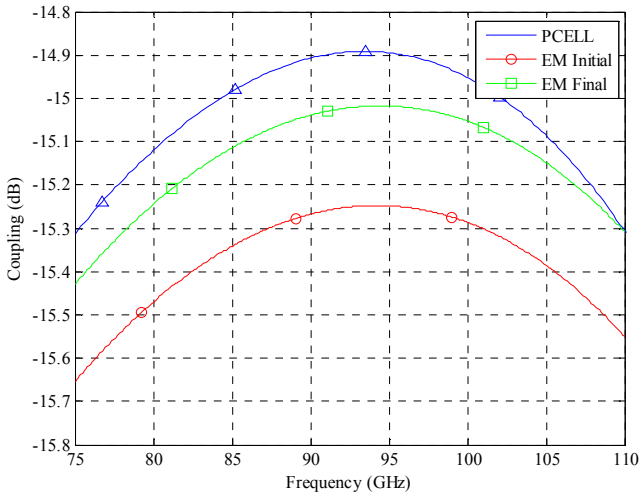

Fig. 8. Coupling response at different simulation stages

VI. Conclusion

We have proposed a novel, flexible design flow for 3D EM modeling of BEOL structures using the strengths of both IC EDA and 3D EM CAD tools. The method allows for parameterized design of BEOL structures using Pcell elements as seed, thereby reducing the time required to generate the full simulation model in EM CAD. The method requires no background scripting; only the GDSII streamed layout data and knowledge of the process parameters. The method is demonstrated using a 94 GHz quarter-wave directional coupler as example, with the increased accuracy demonstrated.

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