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AN ON-CHIP POST-PRODUCTION TUNABLE GROUP DELAY EQUALISER

Abstract — A design method for distributed element on-chip post-production tunable group delay equalising networks is presented. It is shown that a number of adjustable Darlington C-sections can be used to equalise the group delay of an arbitrary network. The C-sections are implemented in an IBM 0.13 µm BiCMOS process as complementary microstrip slotline-stub all-pass structures and modified to provide post-production tunability. The group delay ripple of a theoretical second-order Butterworth bandpass filter, cascaded with the synthesised all-pass network, is reduced by 43% as proof of concept.

Introduction

The Square Kilometre Array (SKA) radio telescope Phase II system is expected to generate and process 15 Tbits/s of data in real time [1]. Signal distortions, caused by a non-flat group delay with frequency of any of the RF front-end components on the low noise receiver block (LNB), are commonly corrected for in digital post-processing [1]. With the volume of data throughput required for the SKA and other big data problems, such digital post-correction is undesirable [2]. A preferred solution is to post-distort the group delay of the preceding channel by means of an analogue equalisation network that is cascaded in the receiver chain, thereby producing a channel with a net flat group delay [2] without altering the magnitude transmission response. The functionality of this solution can be extended on significantly by making the equalisation network post-production tunable [3], thus enabling the use of the same hardware to correct for varying delay properties of the receiver chain.

Early examples of quasi-arbitrary continuous group delay functions realised with analogue all-pass networks are generally limited to particular applications, taking the form of design tables and graphs [4]. Although numerical algorithms can be used [2], [5], analytical techniques (as is presented in [4]) are less numerically expensive and therefore, preferred. The method in [4] allows for the synthesis of a group delay equalisation network for almost any arbitrary group delay ripple to within a specified error, with an optimal number of all-pass sections[1].

Cascaded all-pass C-sections, realised in soft-substrate microstrip technology [2], [4], [6], have been shown to exhibit quasi-arbitrary group delay functions, without affecting the transmission channel's magnitude response appreciably [2] and are thus suitable to realise the equalising all-pass networks

[1] Exact restrictions could not be accurately determined.

generated by means of the aforementioned techniques. C-sections implemented using microstrip stubs with complementary slotlines [6] exhibit large operational bandwidths (up to 20 GHz) and can be implemented at X-band frequencies. Frequency agility has, however, never been demonstrated in this topology.

Furthermore, all-pass group delay equalising networks have not been demonstrated on-chip in the filter literature to date. Monolithic microwave integrated circuit devices have become attractive solutions in applications such as the SKA project requiring minimal device dimensions, low costs of mass production, low operating power requirements, system on-chip solutions integrating entire microwave systems on a single die and simple post-production integration [7].

In this work the complementary slotline-stub C-section is implemented on-chip in the IBM 0.13 µm SiGe BiCMOS technology node and modified/improved to realise a post-production tunable eighth order group delay equalising all-pass network in the X-band frequency range. The all-pass network is generated using Hellerstein's analytical algorithm [4] and a design procedure for a tunable on-chip complementary slotline-stub C-section group delay equaliser is formalised. The all-pass equaliser is demonstrated by reducing the ripple of a second order Butterworth bandpass filter (BPF). Final results are derived from full-wave 3D electromagnetic (EM) simulations using the CST Microwave Studio software package.

Synthesis procedure

The objective of minimising the existing group delay ripple of the LNB can be expressed mathematically as:

$$\max_{\text{rippple}}\left\{GD_{filter}(f)+GD_{equal}(f)\right\} \le GD_{ripple,\max} \cap \max_{\text{rippple}}\left\{\left|H_{filter}.H_{equal}\right|\right\} \le \left|H\right|_{ripple,\max} \quad (1.1),$$

where the existing group delay curve is $GD_{filter}(f)$ and the equalising group delay is expressed by $GD_{equal}(f)$. H represents the total system transfer function.

To realize a programmable group delay equalisation network, the response of the preceding receiver chain is characterized a priori, and the extracted S-parameters are used as numerical input to Hellerstein's algorithm [4] to calculate the poles/zeros of the equalisation network required to minimise the net group delay ripple. These pole/zero values are then related to C-section coupling values *k* and phase lengths *l* by:

$$\begin{aligned}
&\text{Poles: } s_p = \frac{1}{2l\sqrt{\mu\varepsilon}}.\left[\ln\left|\frac{\sqrt{1+k}-\sqrt{1-k}}{\sqrt{1+k}+\sqrt{1-k}}\right| + j\pi(1+2\,\mathrm{n})\right] \\
&\text{Zeros: } s_z = \frac{1}{2l\sqrt{\mu\varepsilon}}.\left[-\ln\left|\frac{\sqrt{1+k}-\sqrt{1-k}}{\sqrt{1+k}+\sqrt{1-k}}\right| + j\pi(1+2\,\mathrm{n})\right] \text{ with } \begin{matrix} n \in \square \\ k \in (0:1) \end{matrix}
\end{aligned} \quad (1.2).$$

The *l* and *k* values generated in this way are expressed as C-section line lengths with even- and odd-mode characteristic impedances [8] (for the purpose of circuit simulations) which are cascaded with the original LNB S-parameters.

To demonstrate the method, a second-order Butterworth BPF is used as input to the synthesis, and its group delay response equalised with a fourth-order (two coupled line sections) equalisation network (Figure 1), producing the results in Figure 2. The equalisation network reduces the group delay variation of the original filter by 71% over the passband of 8 – 14.5 GHz.

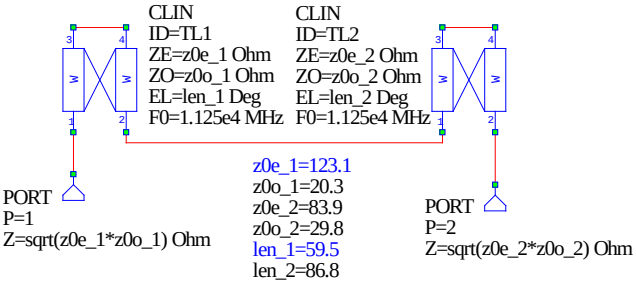

Figure 1. Fourth-order all-pass delay equaliser simulated in AWR Microwave Office.

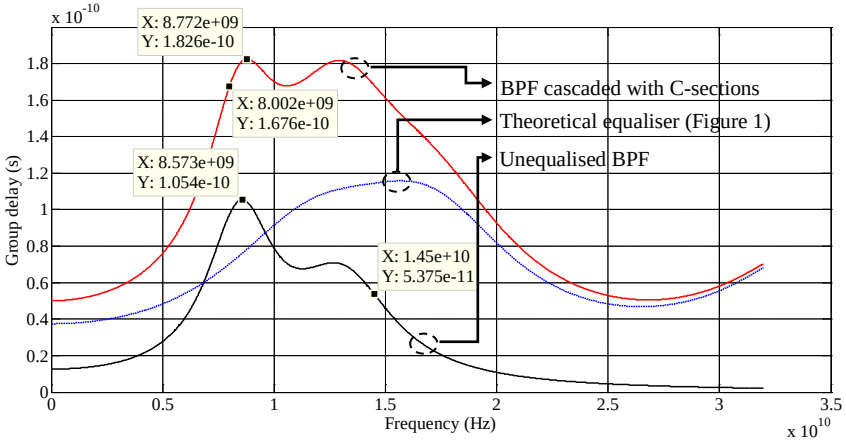

Figure 2. Second-order Butterworth BPF equalised by a fourth-order all-pass network.

Implementation on-chip

The previously calculated values of *k* and *l*, as produced by the synthesis method, are readily related to the complementary slotline-stub [6] width (*w*) and length (*d*) dimensions respectively for hardware implementation. The *w*- and *d*-parameters of both the slotline and stub structures in Figure 3 are assumed identical for the design procedure of this paper. In order to improve insertion and return losses these parameters are fine-tuned separately for the slotline and the stub in EM simulation during final design optimisation [6].

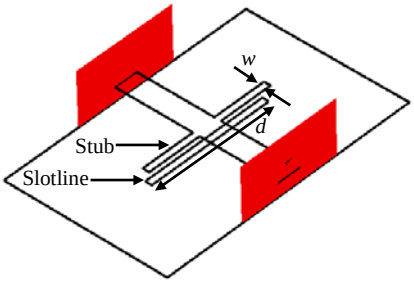

Figure 3. C-section implemented using the complementary microstrip slotline-stub structure [6].

Each theoretical C-section developed in synthesis can now be implemented physically in a cascaded complementary microstrip slotline-stub geometry, as shown in Figure 3 [6] and in Figure 4. The effective stub and slotline lengths can be made adjustable by adding bridging CMOS switches (Figure 5), to change the short-circuit point. Variation in *k* is achieved by varying the stub and slotline widths, but since it is not possible to change the manufactured width post-production, network agility is achieved in discrete steps by cascading a variety of complementary slotline-stubs (all representing different *k* values) and including/excluding slotline-stubs from the network as necessary. The required *k*-value slotline-stubs are included by selecting an appropriate slotline-stub length with the switches, whilst the slotline-stubs not required by the network are bypassed by enabling all slotline and disabling all complementary stub switches (effectively reducing the slotline-stub length to 0).

This geometry may be implemented on-chip as shown in Figure 4, where the microstrip signal track is implemented in the top aluminium layer AM, whilst the slots are cut from a solid ground plane on the lowest copper layer M1.

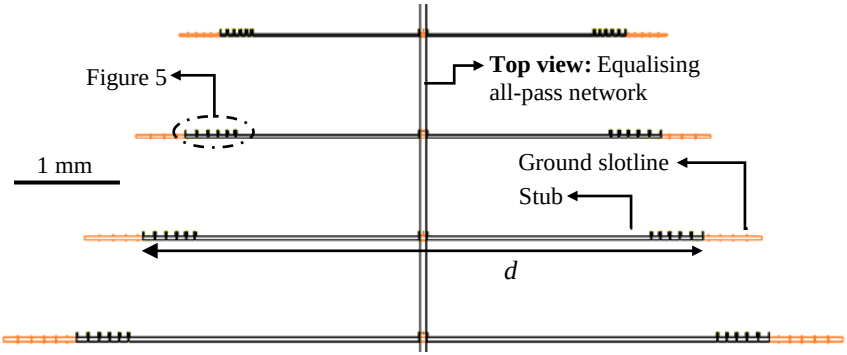

Figure 4. X-band on-chip post-production tunable group delay equaliser.

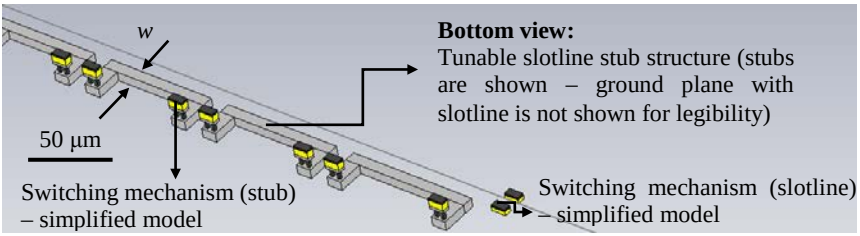

Figure 5. X-band on-chip post-production tunable group delay equaliser.

The *k* value of a slotline-stub is adjusted in simulation by width (*w* in Figure 5) [6] while the effective length (determined by the number of switch-connected lines and corresponding short-circuited slotline switches) is set by *d*. These discrete adjustments lead to the tuning grid in Figure 6. These values of p-p group delay (*GD*) and centre frequency (f_o) may now be related back to the synthesised all-pass poles/zeros [2]. Consequently, each theoretically synthesised all-pass section may now be implemented in hardware by the selection of slotline-stub width and discrete switched slotline-stub length that best approximates the theoretically required *GD* and f_o values of the C-section.

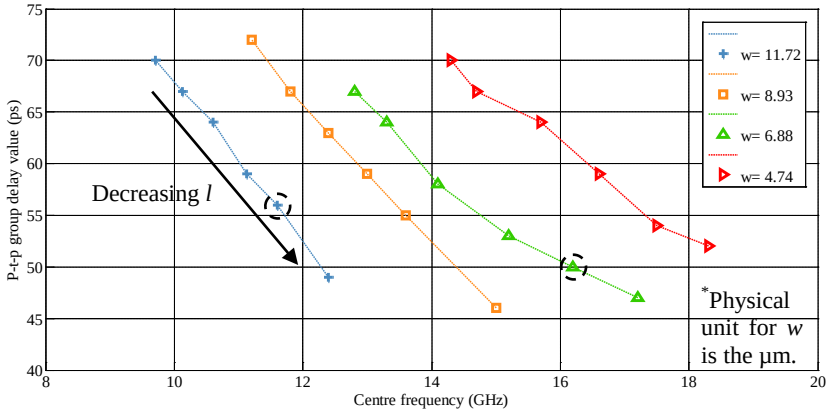

Figure 6. Tuning grid of the delay equaliser with tuned locations indicated resulting in a fourth-order equaliser for a second-order Butterworth BPF.

Simulation results

An eighth-order (four cascaded stubs) network is implemented in CST Microwave Studio on the IBM 8HP process with complementary slotline-stub widths (*w*) 11.72 µm, 8.93 µm, 6.88 µm, 4.74 µm and 6 discrete switched lengths (*d*) for each slotline-stub width ranging from 2.97 mm to 6.03 mm. This network is applied in the equalisation of the previously shown second-order Butterworth filter in Figure 2, with a fourth-order synthesis producing 11.63 GHz, 17.02 GHz and 46.42 ps, 60.5 ps as optimal f_o and *GD* values respectively. The best discrete switched approximations for these are 11.6 GHz,

16.2 GHz and 56 ps, 50 ps with the slotline-stubs of width 4.74 µm and 8.93 µm bypassed to reduce insertion loss.

The full-wave EM simulation results of the final cascaded system are presented in Figure 7 and Figure 8. The group delay ripple in the band 7.37 – 14.2 GHz for the original unequalised BPF is 46.79 ps. Over the narrower band 8.17 – 14.2 GHz the group delay ripple is initially 46.79 ps. After cascading the BPF with the delay equaliser the new ripple over the resulting passband is 49.9 ps. The delay ripple over the narrower bandwidth is 26.9 ps. Thus a group delay ripple improvement of 43% is achieved over the slightly narrower bandwidth, as illustrated in Figure 7.

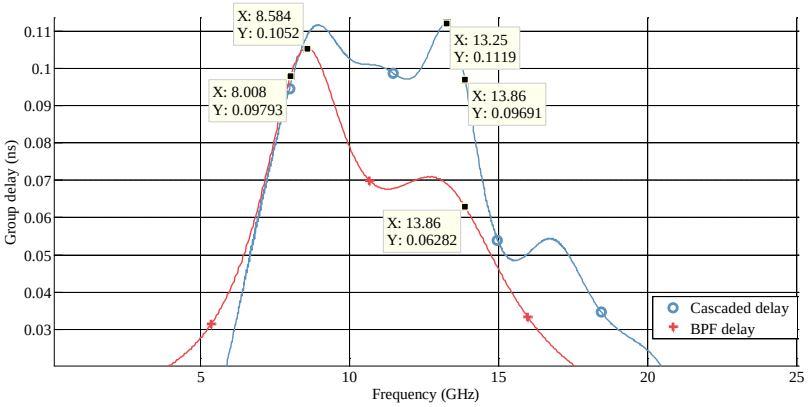

Figure 7. Equalisation of the group delay ripple of a second-order Butterworth BPF with a fourth-order all-pass network – group delay response.

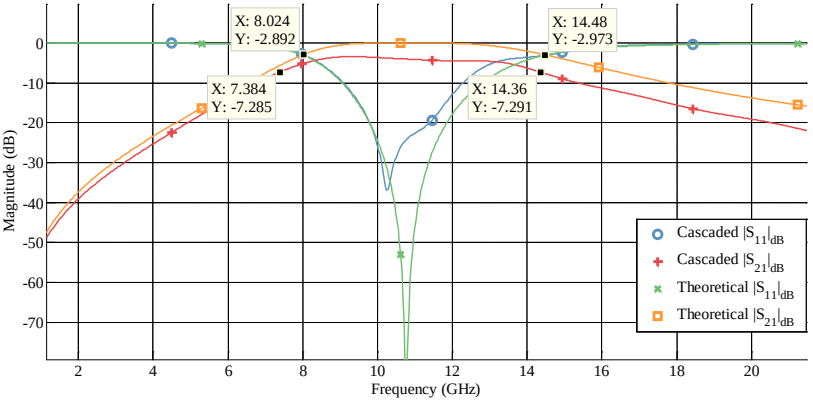

Figure 8. Equalisation of the group delay ripple of a second-order Butterworth BPF with a fourth-order all-pass network – magnitude response.

As a trade-off for delay ripple improvement the magnitude response is degraded as shown in Figure 8. The resulting -3 dB cut-off points are shown with the effective passband frequency of 7.37 – 14.2 GHz and a ripple magnitude increase of 1.3 dB.

Conclusion

A distributed element X-band on-chip post-production tunable group delay equaliser has been presented. Hellerstein's method for the synthesis of all-pass delay equalisers has been applied to bandpass signals for the first time. A design approach based on Hellerstein's algorithm has been developed for an agile C-section complementary slotline-stub on-chip delay equaliser. The equaliser's order is tunable from second- to eighth-order with a centre frequency tunability ranging from 9 to 19 GHz and a peak-to-peak (p-p) group delay basis function tunable from 45 to 60 ps. The group delay ripple of a theoretical second-order Butterworth BPF is reduced by 43% with the equaliser tuned in a fourth-order configuration as proof of concept.

Acknowledgments

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References

1. Manley J. *et al.* // IEEE 2012 International Conference on Electromagnetics in Advanced Applications. 2012. V. P. 462-465.

2. Gupta S. *et al.* // IEEE Transactions on Microwave Theory and Techniques. 2010. V. 58. P. 2392-2407.

3. Gupta S. *et al.* // IEEE Antennas and Propagation Society International Symposium. 2007. V. P. 5523-5526.

4. Hellerstein S. // IRE Transactions on Circuit Theory. 1961. V. 8. P. 215-222.

5. Ziska P. *et al.* // Proceeding of the Thirty-Eighth Southeastern Symposium on System Theory. 2006. V. P. 483-487.

6. Mandal M. *et al.* // IEEE Microwave and Wireless Components Letters. 2012. V. 22. P. 388-390.

7. Mbuko O. *et al.* // IEEE 2006 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. 2006. V. P. 163-165.

8. Pozar D.M. // Microwave Engineering, 4th edition, Amherst, USA: John Wiley & Sons Publishing. 2012. V. P. 347-359.