A Frequency Agile Switched Delay Line Slow-wave BiCMOS Filter

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Abstract—**A mm-wave BiCMOS back-end metallization switched delay line frequency agile filter is presented. Miniaturization of the delay lines is achieved by using slow-wave propagation modes on shielded CPWs, with a standard BiCMOS process transistors used as on-chip switching elements. A first-order filter is presented, with simulation results indicating one transmission band at 40.4 GHz of 22.8 % relative bandwidth and insertion loss of –12.25 dB, with the other transmission band at 47.55 GHz with a 23.79 % relative bandwidth and insertion loss of –13.66 dB. Both bands feature below -15 dB input reflection loss. The paper further establishes the potential for shielded CPW transmission lines for the design of complex passive devices on the back-end metallization of various semiconductor technologies.**

Keywords—millimeter wave integrated circuits; BiCMOS integrated circuits; Silicon on insulator technology; passive circuits; microstrip filters; integrated circuit modeling.

I. INTRODUCTION

The utilisation of Bipolar Complementary Metal-Oxide Semiconductor (BiCMOS) for radio frequency (RF) applications is increasing. This is due to the cost effective high volume production capabilities, established by manufacturers of digital integrated circuits. By using the back-end metallised layers for RF designs it is now possible to produce a complete system-on-chip (SOC) on a single die, containing both digital and analogue subsystems. This integration level reduces both size and cost, and increases reliability [1]. Millimetre-wave transceiver technology has achieved a rapid development boost due to the standardisation of the 45 GHz band by the IEEE802.11aj. The mm-wave band can allow for a data rate up to 1.6 Gb/s per 2.16 GHz channel band [2]. This proliferation of standards in the mm-wave domain creates a need for transceivers that can simultaneously handle multiple standards and frequency bands [3]. To this end, the ability to achieve frequency agile filtering needs to be developed for transceivers in the mm-wave band [3]. Passive filter designs [4] are preferred due to their stability, wide operating voltage regions, cost and linearity in comparison to active filters. However, lumped network filters with high quality (Q-) factors are difficult to realise at mm-wave frequencies since the associated wavelengths are comparable to that of the actual dimensions of the circuit elements. This has driven the need for research into on-chip filter implementations where the wavelengths associated with the lumped elements are no longer comparable with the dimensions of a typical on-chip circuit equivalent.

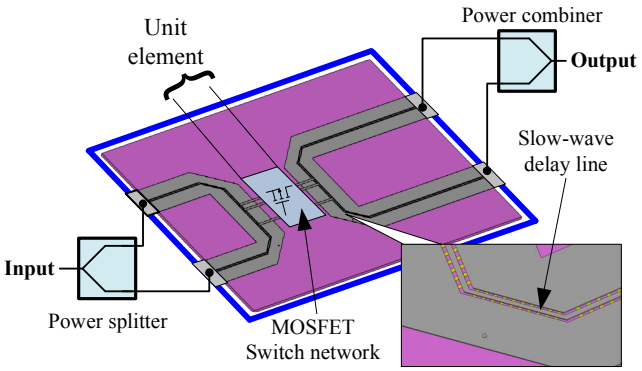

FIGURE 1. BICMOS SDL SLOW-WAVE FILTER.

Switched delay line (SDL) based filters [5], [6], can be utilised without forfeiting a large amount of linearity and loss. The filter topology makes use of in-phase and out-of-phase combination of two switchable unequal phase length propagation paths to tune the centre frequency and passbands, unlike other filter designs which configure my means of tuning the centre frequency of the coupled resonators [6]. This paper demonstrates the viability of these structures on BiCMOS back-end metallisation.

II. DEVICE OPERATION

A. SDL filter operation

An SDL resonator [5] is shown in Figure 2. The structure consists of a -3 dB in-phase power splitter, delay line structure and multi-pole switch. The input signal is divided by means of a power splitter between two delay line structures. The parallel lines impose different time delays upon the incident wave at a selected point, where the signal is tapped off the delay line by an engaged switch. θ_1 and θ_2 represent the phase of the respective delay lines. The transmission response of the SDL resonator is determined by the phase relationship between the delay lines at the point where the line are tapped [5]. Therefore by toggling the respective multi-pole switch to the appropriate location, in-phase combination will be achieved at a specific frequency, and the centre frequency of the filter may be selected.

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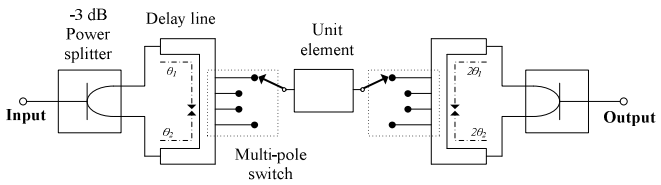

FIGURE 2. QUASI-ELLIPTIC SDL FILTER WITH UNIT ELEMENT [5].

As in [5], a quarter wave unit element (UE) is introduced between the two reversely cascaded delay line resonators, realising a quasi-elliptic filter, in order to improve the bandwidth and stopband rejection. Varying the impedance of the UE controls the filter bandwidth and stop-band rejection, whilst the switching elements control the centre frequency.

B. Slow-wave transmission lines

The slow-wave mode occurs where the Si substrate acts neither like a dielectric nor a conductor. A strong interfacial polarisation occurs and gradually grows [7] as a result of the SiO_2 thickness being much less than the Si thickness. This results in the magnetic (H-) fields penetrating the substrate while the electric (E-) fields do not and are confined in the SiO_2 layer. As a result of the separation of the E- and H-fields the propagation velocity slows down and hence a slow wave is realised. Figure 3 illustrates the field distribution of a microstrip exhibiting slow-wave propagation properties.

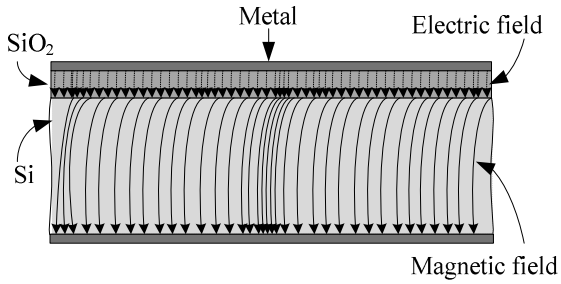

FIGURE 3. ELECTRIC AND MAGNETIC FIELDS WITHIN A MICROSTRIP ON SI SUBSTRATE.

The slow-wave mechanism is enhanced by introducing floating shielding structures in order to suppress substrate loss [8] .This is done by means of shielded co-planar waveguides (CPWs). Figure 4 shows a CPW implemented in a BiCMOS process with 7 metallization layers. The mutual coupling between the signal and ground conductor results in equal but opposite currents on the transmission line and the floating shield strips. The characteristic inductance of the transmission line depends on this mutual coupling. If the shield strips are placed on the lowest metal layer (metal 1), there is negative coupling between the signal, ground conductor and shield strips. This causes the per-unit length inductance to be lower than that of the standard CPW, as well as increasing the per-unit length capacitance. An increase in the capacitance results in a larger RC time constant and hence a larger delay.

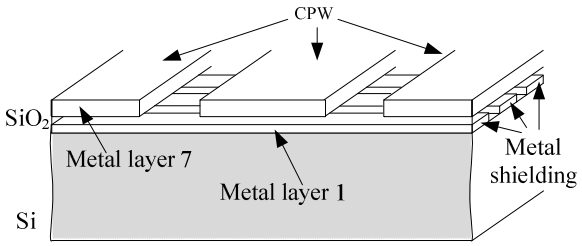

FIGURE 4. SLOW-WAVE CPW WITH METAL SHIELDING.

Due to the longer time delay per unit length, slow-wave mode transmission lines are used as delay lines on-chip as a reduced length alternative to conventional transmission topology. The propagation mode demonstrates low dispersivity, low loss with good signal integrity with delays up to 30 times slower than the speed of light in a vacuum [9] and is identified as a viable method to realise on-chip delay lines. Design guidelines for on-chip slow-wave structures are presented in [10] and conclude that the slow-wave effect is dependent on the SiO_2 thickness and dimensions relating to the planar transmission lines and floating metal strips. The design guidelines and measurements from [10] indicate that slow-wave designs implemented in CMOS technologies have low levels of loss and dispersion at mm-wave frequencies.

TABLE I. SLOW-WAVE TECHNOLOGY

Ref.	Slow-wave mechanism	Attenuation (dB/mm)	*Q*-factor
[10]	Floating metal strips	0.50 at 60 GHz	30 – 50 at 60 GHz
[11]	Floating metal strips	0.63 at 20 GHz	27 at 20 GHz
[12]	Floating metal strips on M1	0.15 at 60 GHz	38 at 60 GHz
[13]	Floating metal strips	0.52 at 40 GHz	20 at 40 GHz

The switched delay line structure is attained by connecting different SiGe FET source terminals to points along the UE, with the drain of each transistor connected to the same embedded UE line and the gate voltages used as binary switch control as shown in Figure 5. The different points on the delay line provide various phase delays which are fed into the UE.

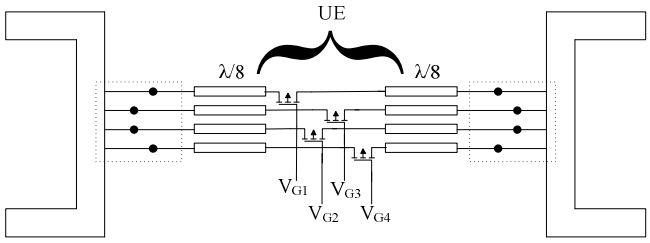

FIGURE 5. SWITCHING OF DELAY LINES.

III. Synthesis and Circuit Simulation

A 1st order quasi-elliptic delay line filter is synthesised by the method provided in [5]. The first filter band is designed to have a centre frequency of 40 GHz and a transmission bandwidth of 30 % which results in a phase delay of 25.71° at 40 GHz. The second band is designed for a centre frequency of 45 GHz and a bandwidth of 25 % which results in a phase delay of 19.2° at 45 GHz. The ripple and bandwidth of the filter can be tuned by means of varying the UE impedance. For a bandwidth of 30 % of the centre frequency of 45 GHz the normalised UE impedance can be expressed as:

$$\frac{0.3\pi}{4}Z^2 - Z + \frac{0.3\pi}{4} = 0 \qquad (1)$$
$$Z = 3.99;\ Z = 0.25$$

A normalised UE impedance of 3.99 is then selected and inserted and used to obtain the stopband ripple level:

$$|S_{21}|_{\max[\mathrm{dB}]} = 10\log\left[\left(\frac{2Z}{Z^2+1}\right)^2\right] \qquad (2)$$
$$= -6.59 \ \mathrm{dB}$$

The transfer functions of the synthesised filters for the two respective bands, for a normalised UE impedance of 3.99, are shown in Figure 6, with a ripple level of -11.35 dB.

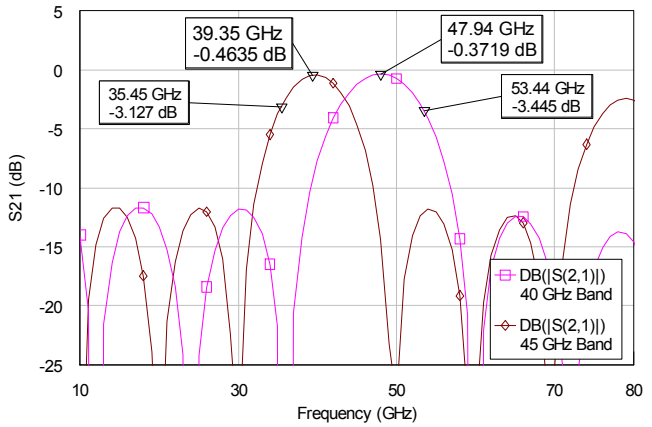

Figure 6. Circuit simulation of SDL Filter.

IV. Full-wave Simulation

After a circuit synthesis has been concluded, the required values of impedance and delay are implemented on the IBM 8HP process by means of full-wave simulation in CST Microwave Studio using the time domain solver. A CPW transmission line is designed with a strip width of 16 µm and a spacing of 11 µm to achieve a characteristic impedance of 49.85 Ω. The slow-wave delay is calculated to have a length of 823 µm in order to obtain a phase delay difference of 25.71° at 40 GHz for the single SDL resonator structure. The resonators (Figure 7) are joined by means of a quarter-wave UE of length 668.64 µm.

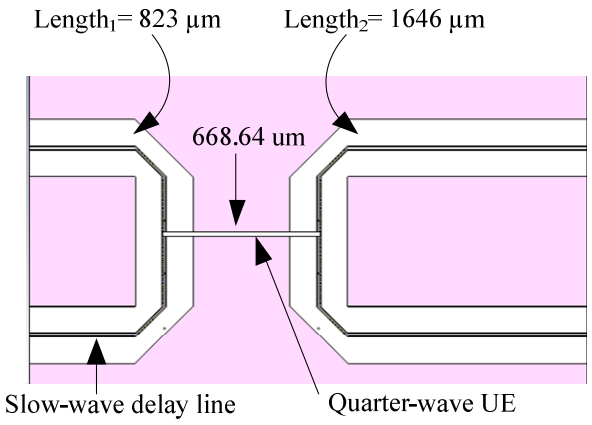

Figure 7. CST model of SDL filter.

The delay line is realised by placing floating copper strips of width 12 µm and 25 µm separation on the bottom metallization layer. The bottom metal layer is selected since it is the thinnest of the metal layers measuring only 0.3 µm. The thin nature of the strips is chosen to mitigate the effects of induced eddy current on the surface of the conductor [12]. The conducting CPW is placed on the second highest metallization layer (aluminium), and not the top layer. This choice was made to introduce a uniform dielectric around the CPW, and not an air dielectric, further reducing dispersion. It also provides more routing flexibility, since the top metallization layer may now be used to connect the various sub-circuit elements without having to introduce discontinuities in the lower shielding structure.

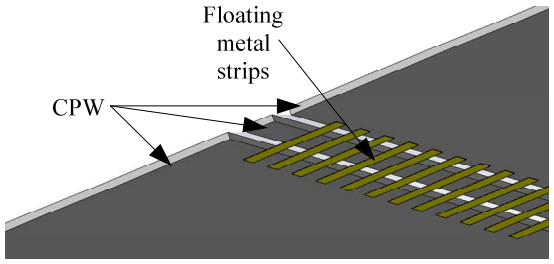

Figure 8. Floating metal strips underneath CPW, as viewed from substrate (below).

The phase of the SDL resonator is simulated in CST Microwave Office and has a linear response in the band of interest around 45 GHz as seen in Figure 9. By placing the CPW in a homogeneous dielectric the design near-TEM characteristics with a larger propagation delay and better signal integrity. It can be seen that the response is linear throughout the frequency band with a simulated phase delay of -29.021° at 45 GHz.

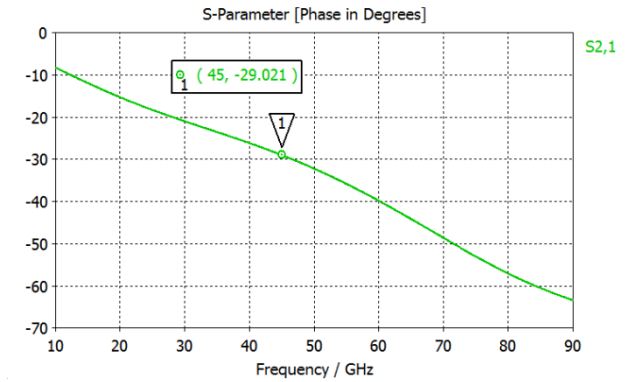

FIGURE 9. EM SIMULATION OF THE PHASE OF SDL RESONATOR.

The group delay of the stand-alone slow-wave structure is shown in Figure 10. It can be seen that the group delay varies by only 8.854 ps for the frequency band of interest. This results in a delay flatness of 191.1 fs/GHz across the band of interest. The phase delay of -29.021° will therefore not drastically vary as a result of frequency changes.

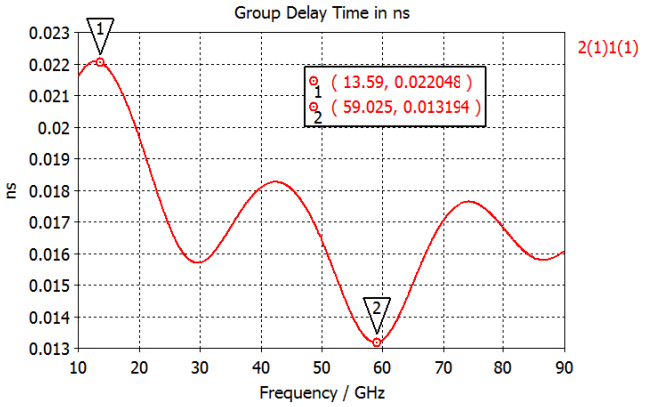

FIGURE 10. EM SIMULATION OF THE GROUP DELAY OF SDL RESONATOR.

The time delay of a two switch configuration in Figure 11 is shown in Figure 12.

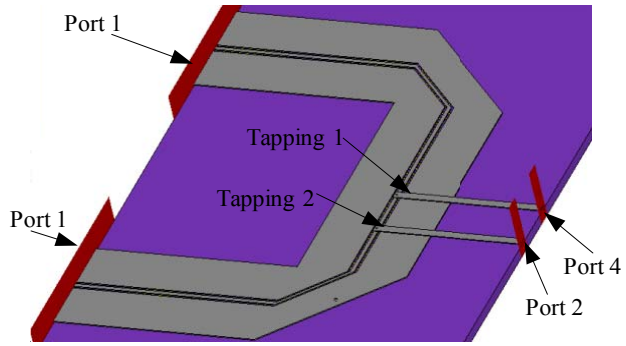

FIGURE 11. TAPPING CONFIGURATION.

It can be seen from Figure 12 that for an equal tapping length (tapping 1) the delay of the two respective delay lines (td_{41} and td_{43}) differ by 1 ps as compared to the (td_{21} and td_{23}) where the difference in delay of the unequal tapping length of tapping 2 is 8 ps. This indicates that for an unequal tapping length a large phase delay can be achieve which is attributed to the slow-wave mechanism.

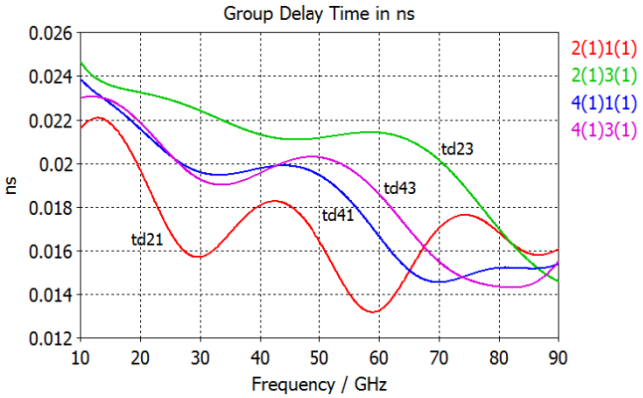

FIGURE 12. EM SIMULATION OF THE GROUP DELAY OF DELAY LINES.

A second three-port SDL resonator is designed in CST using the geometry and characteristics as described above. The second structure has a length of 1646 µm and therefore a corresponding phase delay of -61.23° at 45 GHz. A quarter wave microstrip routed on metal layer 7 is used to join the two respective SDL resonators. Each resonator is initially tapped in the centre of its length by means of the UE. The SDL resonators and UE are imported into AWR Microwave office as described by Figure 13.

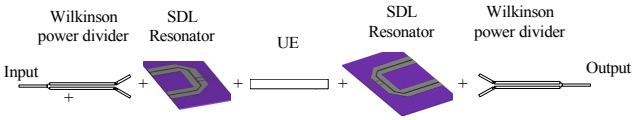

FIGURE 13. SDL SIMULATION STRATEGY.

Pre-defined -3 dB Wilkinson power splitters will used from the fabrication foundry in prototyping and are considered ideal for simulation purposes. As shown in Figure 14, the EM simulation of the filter has a centre frequency of 40.4 GHz and a bandwidth of 22.8 % with an insertion loss of -12.25 dB.

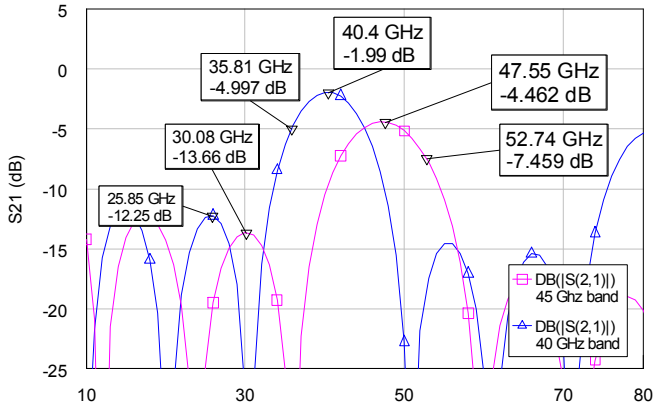

FIGURE 14. EM S_{21} SIMULATION OF THE SDL FILTER FOR TWO UE TAPPINGS.

For the second tapping point each resonator is tapped at 3/8ths of its respective length. This results in an unequal phase relation of each delay line and as a result an increase in the

centre frequency and decrease in the bandwidth of the filter. This strategy is used to emulate the switching of the MOSFET devices to control different phase paths. As shown in Figure 14, the second filter network has a centre frequency of 47.55 GHz and a bandwidth of 23.79 %. The insertion loss of the filter is –13.66 dB.

V. CONCLUSION

The synthesis and full-wave simulation of an SDL filter based on a CMOS slow-wave CPW is presented. This paper demonstrates the suitability of this frequency agile filtering topology for on-chip implementation. It can be noted that frequency agile filters reaching mm-wave operating frequencies on back-end IC metallisation require efficient modelling and simulation.

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