SPURIOUS FREE DYNAMIC RANGE ENHANCEMENT OF HIGH-SPEED INTEGRATED DIGITAL-TO-ANALOGUE CONVERTERS USING BiCMOS TECHNOLOGY

by

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SUMMARY

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Keywords: Digital-analogue conversion, BiCMOS integrated circuits, dynamic range, analogue-digital integrated circuits, mixed analogue digital integrated circuits, wideband.

High-speed digital to analogue converters (DAC), which are optimised for large bandwidth signal synthesis applications, are a fundamental building block and enabling technology in industrial instrumentation, military, communication and medical applications. The spurious free dynamic range (SFDR) is a key specification of high-speed DACs, as unwanted spurious signals generated by the DAC degrades the performance and effectiveness of wideband systems. The focus of this work is to enhance the SFDR performance of high-speed DACs.

As bandwidth requirements increase, meeting the desired SFDR performance is further complicated by the increase in dynamic non-linearity. The most widely used architecture in high-speed applications is the current-steering DAC fabricated on CMOS technology. The current source finite output impedance, switch distortion and clock feedthrough are the greatest contributors to dynamic non-linearity and are difficult to improve with the use of MOS devices alone. This research proposes the use of BiCMOS technology that offers high performance, using heterojunction bipolar transistors (HBT) that, when combined with MOS devices, are able to improve on the linearity of the current-steering DAC and hence improve the SFDR.

A design methodology is introduced based on BiCMOS fabrication technology to improve SFDR performance and places emphasis on the constraints of modern fabrication processes. A six-bit current-steering application-specific integrated circuit DAC is designed based on the proposed design methodology, which optimises the SFDR performance of high-speed binary weighted architectures by lowering current switch distortion and reducing the clock feedthrough effect to verify the hypothesis experimentally.

A novel current source cell is implemented that comprises HBT current switches, negative channel metal-oxide semiconductor (NMOS) cascode and NMOS current source to overcome distortion by specifically enhancing the SFDR for high-speed DACs. A switch driver and low-voltage differential signalling receiver to achieve high-speed DAC performance and their influence on the SFDR performance are designed and discussed.

The DAC is implemented using the International Business Machines Corporation (IBM) 8HP silicon germanium (SiGe) BiCMOS 130 nm technology. The DAC achieves a better than 21.96 dBc SFDR across the Nyquist band for a sampling rate of 500 MS/s with a core size of 0.1 mm^2 and dissipates just 4 mW compared to other BiCMOS DACs that achieve similar SFDR performance with higher output voltages, resulting in much larger power dissipation.

OPSOMMING

VALS VRY DINAMIESE-OMVANG-VERSTERKING VAN HOËSPOED-GEÏNTEGREERDE DIGITAAL-TOT-ANALOOGOMSETTERS DEUR VAN BiCMOS-TEGNOLOGIE GEBRUIK TE MAAK

deur

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Sleutelwoorde: Digitaal-analoog-omskakeling, BiCMOS geïntegreerde stroombane, dinamiese reikwydte, analoog-digitale geïntegreerde stroombane, gemengde analoog-digitale geïntegreerde stroombane, breëband.

Hoëspoed digitaal-tot-analoogomsetters (DAO) wat vir groot bandwydteseinsintese-toepassings geoptimeer is, is ’n fundamentele bousteen en magtigingtegnologie in industriële instrumentasie, militêre, kommunikasie- en mediese toepassings. Die vals vry dinamiese reikwydte (VVDR) is ’n sleutelspesifikasie vir hoëspoed-DAOs, aangesien ongewenste vals seine wat deur die DAO gegenereer word, die werkverrigting en effektiwiteit van wyebandstelsels verlaag. Die fokus van hierdie werk is die verbetering van die VVDR-werkverrigting van hoëspoed-DAOs.

Soos bandwydtevereistes vermeerder, word die bereiking van die gewenste VVDR-werkverrigting verder gekompliseer deur die verhoging in dinamiese nie-liniariteit. Die mees algemeen gebruikte argitektuur in hoëspoedtoepassings is die stroombaanstuur-DAO wat volgens CMOS-tegnologie vervaardig word. Die stroombron- eindige uitsetimpedansie, skakeldistorsie en klokdeurvoer maak die grootste bydrae tot nie-liniariteit en is moeilik om te verbeter deur slegs MOS-toestelle te gebruik. Hierdie navorsing stel die gebruik van BicMOS-tegnologie voor, wat hoë werkverrigting bied deur die gebruik van heterovoegvlak- bipolêre transistors (HBT) wat, in kombinasie met MOS-

toestelle, in staat is om die lineariteit van die stroomstuur-DAO te verbeter en sodoende die VVDR te verbeter.

ʼn Ontwerpmetodologie gebaseer op BicMos-fabriseringtegnologie word aangebied om VVDR-werkverrigting te verbeter; dit benadruk die beperkings van modern vervaardigingprosesse. ʼn Ses-bis stroomstuur toepassing spesifiek geïntegreerde stroombaan DAO is ontwerp gebaseer op die voorgestelde ontwerpmetodologie, wat die VVDR-werkverrigting van die hoëspoed- binêre beswaarde argitekture optimeer deur die stroomskakelaardistorsie te verlaag en die klokdeurvoereffek te verminder om die hipotese eksperimenteel te bevestig.

ʼn Nuwe stroombronsel word geïmplementeer wat bestaan uit heterovoegvlak- bipolêre transistorstroombaanskakelaars, ʼn negatiewekanaal-metaaloksiedhalfgeleier- (NMOS) kaskode en NMOS-stroombron om distorsie uit te skakel deur spesifiek die VVDR vir hoëspoed-DAOs te verbeter. ʼn Skakelaardrywer en laespanning- differensiaalseining-ontvanger om hoëspoed-DAO-werkverrigting te bereik en hulle invloed op die VVDR se werkverrigting word ontwerp en bespreek.

Die DAC word geïmplementeer deur gebruik te maak van International Business Machines Corporation (IBM) 8HP silikon germanium (SiGe) BiCMOS 130 nm-tegnologie. Die DAO bereik ʼn VVDR van meer as 21.96 dBc dwarsoor die Nyquist-band vir ʼn steekproeftempo van 500 MS/s met ʼn kerntempo van 0.1 mm^2 en dissipeer slegs 4 mW vergeleke met ander BiCMOS DAOs wat soortgelyke VVDR-werkverrigting bereik met hoër uitsetspanning, wat ʼn veel groter kragdissipasie tot gevolg het.

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LIST OF ABBREVIATIONS

ASIC	Application-specific integrated circuit
AWD	Analog waveform display
BiCMOS	Bipolar complementary metal oxide semiconductor
CBE	Collector-base-emitter
CBEBC	Collector-base-emitter-base-collector
CMOS	Complementary metal oxide semiconductor
CSIR	Council for Scientific and Industrial Research
DAC	Digital-to-analogue converter
DEM	Dynamic element matching
DNL	Differential non-linearity
DRC	Design rule check
EW	Electronic warfare
FET	Field effect transistor
FMC	FPGA mezzanine card
FOM	Figures of merit
FPGA	Field programmable gate array
HBT	Heterojunction bipolar transistor
HIT-Kit	High performance interface toolkit
IBM	International Business Machines Corporation
IC	Integrated circuit
INL	Integral non-linearity
IO	Input output
LSB	Least significant bit
LVDS	Low voltage differential signalling
LVS	Layout versus schematic
MEP	MOSIS Educational Programme
MIM	Metal insulator metal
MOS	Metal oxide semiconductor
MPW	Multi-project wafer
MSB	Most significant bit
NMOS	Negative channel metal oxide semiconductor
OSS	Open simulation system

PDK	Process design kit
PCB	Printed circuit board
QFN	Quad flat no-lead
RF	Radio frequency
RTZ	Return to zero
SFDR	Spurious free dynamic range
SiGe	Silicon germanium
SMA	Sub-miniature A
SNR	Signal-to-noise ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
SRD	Swing-reduced driver

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CHAPTER 1: INTRODUCTION

1.1 BACKGROUND TO THE RESEARCH

The spurious free dynamic range (SFDR) of high-speed digital-to-analogue converters (DACs) is a key specification in a variety of applications such as electronic warfare (EW), wideband communications and software-defined radio. Unwanted spurious signals generated by the DAC can degrade the bit error rate of wideband communication systems and the effectiveness of wideband EW systems [1], [2].

Meeting the desired spurious performance of sampled signals close to the Nyquist rate will become more stringent owing to the trade-off that exists between the SFDR and sampling rate [3]. The degradation of the spurious performance can be attributed to static and dynamic non-linearity [1], [4]. Static non-linearity arises from the mismatch between transistors, while dynamic non-linearity is attributed to switching characteristics and finite output impedance of the current source cells [1]. The dynamic non-linearity worsens as the sampling rate increases and is usually the limiting factor in achieving good SFDR in high-speed DACs [1]. SFDR enhancement techniques have mainly attempted to improve static linearity and are inadequate at high sampling rates.

The most widely used architecture in high-speed applications is the current-steering DAC fabricated using complementary metal oxide semiconductor (CMOS) technology [3]. The current source finite output impedance, switch distortion and clock feedthrough are the greatest contributors to dynamic non-linearity and are difficult to improve with the use of metal-oxide-semiconductor (MOS) devices alone [3]. BiCMOS technology offers high-speed and high-gain heterojunction bipolar transistors (HBT) that, when combined with MOS devices, are able to improve on the linearity of the current-steering DAC and hence improve the SFDR.

1.2 RESEARCH PROBLEM AND HYPOTHESIS

Virtually all high-speed DACs are based on the current-steering approach. The current source cell comprising a current source and a switch to steer the current is the origin of clock feedthrough and finite output impedance, which degrades the SFDR severely.

Traditionally CMOS-only technology has been used to implement the current source cell using solely MOS devices. The research will attempt to evaluate the following hypothesis:

If a BiCMOS DAC achieves a lower distortion, higher output impedance and reduction of the clock feedthrough effect, then the SFDR will be improved in comparison to a CMOS-only DAC.

In undertaking the research to test the hypothesis, various further research questions arose. The following research questions will be addressed in this research:

- How can a BiCMOS implementation of a high-speed DAC improve the SFDR across the Nyquist band?
- How can current source cells in such a BiCMOS process simultaneously achieve a lower distortion, higher output impedance and reduction of the clock feedthrough effect?
- What is the best design approach, architecture and weighting of the current source cells to enhance the SFDR and still maintain good metrics in sampling rate, area and power dissipation?

1.3 JUSTIFICATION FOR THE RESEARCH

The spurious performance of high-speed DACs is of importance in radar, wideband communications and software-defined radio applications. Radars with wideband receivers are capable of distinguishing a false target EW transmission from a real target by analysing the generated spurious signals. Enhancing the SFDR at high frequencies will improve the DAC spectral fidelity, enabling traditional analogue functionality to be implemented in the digital domain, which is the premise of software-defined radio.

Because of dynamic nonlinearity the SFDR will worsen, as higher bandwidth systems require higher sampling rates. Implementations in use today have focused on SFDR enhancement of CMOS processes, at lower sampling rates where the static non-linearity dominates, as noted in Table 1.1. The published SFDR of some of the techniques in the literature has been measured at input frequencies lower than the Nyquist rate. These techniques do not suppress the dynamic non-linearity at high sampling rates and high input frequencies, leading to poor SFDR. A summary of published research on current-steering DACs is presented in Table 1.1.

Table 1.1: Summary of published current-steering DACs related to this research.

	Process Technology	SFDR (dB)	Input Frequency (MHz)	Sampling Rate	INL (LSB)	DNL (LSB)	Resolution (bits)	Area (mm^2)	Journal Impact Factor
[3]	0.35 µm CMOS	65	589	1.2 GS/s	0.6	0.6	10	1.97	-
[4]	0.35 µm CMOS	68	10	250 MS/s	0.90	0.20	12	0.08	0.401
[5]	130 nm CMOS	40	150	300 MS/s	3.00	1.00	12	0.26	2.303
[6]	0.35 µm CMOS	60	10	100 MS/s	0.20	0.10	10	1.33	2.303
[7]	65 nm CMOS	60	550	1.6 GS/s	0.51	0.31	12	0.31	3.106
[8]	130 nm BiCMOS	38	469	5 GS/s	-	-	10	-	3.106
[9]	90 nm CMOS	74	0.98	153 MS/s	0.6	0.6	12	0.13	0.872
[10]	0.25 um BiCMOS	28	6170	20.5 GS/s	-	-	6	3.24	-
[11]	65 nm CMOS	40	5	1.4 GS/s	0.11	0.18	6	-	-
[12]	0.35 µm CMOS	61	500	1 GS/s	0.2	0.14	10	-	3.106
[13]	0.25 µm BiCMOS	-	3850	30 GS/s	0.49	0.57	4	1.8	-
[14]	0.18 µm BiCMOS	-	-	10 GS/s	0.8	0.5	5	1.5	-
[15]	0.25 µm BiCMOS	30.1	5900	13.4 GS/s	-	-	6	0.9	2.943
This work	130 nm BiCMOS	21.96	250	500 MS/s	0.38	0.21	6	0.1	0.924

From Table 1.1, it is seen that CMOS fabrication technology is still the dominant fabrication process for high speed DACs. Research on high-speed BiCMOS DACs is limited, and often achieves SFDR performance by using large power supply voltages at the output stage and suffers from very high power dissipation and area. Many of the projects using BiCMOS fabrication technology have not considered the static and dynamic linearity performance of the DAC. This work is based on BiCMOS fabrication technology, but will place the constraint of matching the output analogue stage power supply voltage to the internal digital logic voltage, thus maintaining low power dissipation. This constraint is pertinent in applications where the DAC is implemented as part of a larger system on chip.

In addition, from a system perspective, most high-speed DAC outputs in communication, radar and EW applications are connected to traditional analogue circuits comprising mixers, amplifiers and filters. BiCMOS technology is more suitable for the implementation of these analogue functions than CMOS-only technology, which is dominant in the digital domain.

The IBM 8HP technology is a SiGe 0.13 µm BiCMOS fabrication process that offers high-performance HBTs with a unity gain frequency (f_t) of over 200 GHz and forward current gain (β) of over 600. The collector of the HBT is heavily doped in order to achieve a high unity gain frequency. As a result of this heavy doping, the breakdown voltage of the transistor is lowered. In the IBM 8HP process, a breakdown voltage of 1.77 V is expected. The breakdown voltage poses a constraint on the current-switching transistors, but can be increased depending on the transistor bias and base resistance. This BiCMOS technology combines metal oxide field effect transistors (MOSFETs) and HBT, which offer better gain, noise, frequency and linearity characteristics. These factors have a direct and indirect relation to the spurious performance and can improve the SFDR that is attainable with CMOS-only technology.

1.4 METHODOLOGY

The hypothesis that SiGe BiCMOS technology can improve the SFDR is investigated. The effects of clock feedthrough, switch distortion and finite current source output impedance are identified as the factors contributing to SFDR degradation and the reduction of these effects is investigated through theoretical study. The central element, namely the current source cell, is discussed in detail. A design methodology for modern high-speed DACs is introduced. An additional switch driver and input and bias circuits are designed and discussed.

The resulting circuit-level implementation is verified through simulations in the Cadence Virtuoso software package using the 0.13µm SiGe IBM BiCMOS 8HP, high-performance interface toolkit (HIT-Kit). The resulting simulations provide first-order estimates of the achievable SFDR. In addition, theoretical and simulation analysis on the sub-system level of the current source cell provides insight into SFDR enhancement techniques.

The layout of the prototype integrated circuit (IC) was detailed and factors affecting SFDR were discussed. The prototype IC was fabricated as part of a multi-project wafer (MPW) fabrication run. A printed circuit board (PCB) was designed and manufactured to serve as a test bench for the prototype IC. The prototype IC was packaged and tested using a field programmable gate array (FPGA) to generate the input digital data. Time and frequency domain measurements were performed to characterise the prototype IC and comparisons to the state-of-the-art were made.

1.5 RESEARCH CONTRIBUTION

The research aimed to improve the SFDR that is attainable in high-speed DACs by using BiCMOS technology. BiCMOS technology allows for the inclusion of HBTs, which offer superior gain, linearity and noise performance in the analogue sections, while MOS transistors may still be used in the digital section because of superior power dissipation and input impedance. A novel current source cell was implemented that comprised of HBT current switches, NMOS cascode and NMOS current source to overcome distortion by specifically enhancing the SFDR for high-speed DACs.

A systematic design methodology was introduced for the design of BiCMOS high-speed binary weighted DACs. The design approach also factors in short-channel effects and low voltage supply headroom constraints of modern fabrication processes. Quantitative results reveal the improvement in linearity and clock feedthrough distortion attainable with BiCMOS technology.

A combination of novel design techniques in the literature on switch drivers and input differential amplifiers is combined with this work to ensure that the entire DAC can operate at a high sampling rate. The resulting spurious performance in combination with metrics of power, sampling rate and area makes it possible to compare this work holistically to other work in the literature and demonstrates that this work compares favourably to the state-of-the-art.

To experimentally verify the hypothesis, a 6 bit DAC was implemented using the IBM 8HP SiGe BiCMOS 130 nm technology. The DAC achieved a better than 21.96 dBc SFDR across the Nyquist band for a sampling rate of 500 MS/s with a core size of 0.1 mm^2 and dissipates just 4 mW compared to other BiCMOS DACs that achieve similar SFDR performance with higher output voltages, resulting in much larger power dissipation.

The research targeted the current-steering DAC used in virtually all high-speed DACs, making the results easily extendable and useful. It is projected that this research will become increasingly significant as higher bandwidth systems are required, owing to the advantage of BiCMOS in high-frequency applications. A peer reviewed journal article resulted from this research and contributed to the current body of knowledge is summarized in the section 1.8.

1.6 OUTLINE OF THE DISSERTATION

The dissertation is organised as follows:

□ Chapter 1: Introduction

The chapter introduces the research problem and presents a hypothesis to address the research problem. The methodology describing how the research will be conducted provides a clear means to validate the hypothesis. The research conducted is placed in context and the contribution of the research to the body of existing knowledge is clarified.

□ Chapter 2: Literature review

The chapter advances the body of knowledge incorporated within the research that is conducted. The phenomena leading to the degradation of SFDR in high-speed digital-to-analogue converters are discussed. Specific methods to improve the SFDR are presented. The broadly defined research field is narrowed down to arrive at specific research questions.

□ Chapter 3: Research methodology

The chapter elaborates on the research methodology followed to test the hypothesis under question. The process and the corresponding models are detailed and their incorporation into the tool chain is described. Justification and limitations to the methodology are also presented and discussed. The theoretical, simulation and fabrication procedures are discussed. The measurement setup and implemented IC verification using experimental testing are also presented in this chapter.

□ Chapter 4: Mathematical and systems design

The chapter describes the mathematical and system design from a theoretical and practical perspective. All DAC circuit details from theory to practice are considered. General architecture considerations are first explored, followed by linearity matching requirements. The design of the current source cell, switch driver and LVDS receivers are covered in depth. Lastly, the complete DAC circuit design is presented.

□ Chapter 5: Layout and fabrication

The layout of the DAC to verify the hypothesis of this work experimentally is detailed in this chapter. The layout of each sub-circuit is detailed, which includes the layout of the current source cell, current source cell matrix, switch driver, LVDS receiver and bias circuits. These cells are combined to form the top-level layout. Various layout-specific considerations are detailed, including the packaging, bonding and fill requirements.

□ Chapter 6: Results

The DAC measurement setup and results are presented in this chapter. Static and dynamic, time and frequency domain measurements are presented. The complete DAC specifications allow for comparisons to other work based on accepted figures of merit (FOM). A discussion of the measurements concludes the chapter.

□ Chapter 7: Conclusion and future work

The chapter brings the dissertation to an end with the conclusions and critical evaluation of the research hypothesis. The limitations of and assumptions about the current research are discussed. Suggestions for future work and improvements conclude this chapter.

1.7 DELIMITATIONS OF THE SCOPE OF THE RESEARCH

The scope of the research is limited to enhancing SFDR in current-steering DAC architectures due to dynamic non-linearity. The sampling rate of the experimental DAC is limited to the availability of high-speed digital inputs for the fabrication process. However, the custom-designed high-speed digital inputs presented in this work were adequate for the purposes of this research.

As this design was combined with three other designs on a single die, there was a limitation on the availability of certain resources, such as die area and input pads, limiting this work to a six-bit DAC. The design methodology presented is independent of the DAC resolution and could be scaled to any high-speed binary weighted current-steering DAC.

This work does not implement or rely on any pre-processing or post-processing of the digital or analogue signals, such as adding noise to the system to reduce the spurious components. It is based on the traditional concept of a DAC, as these techniques cannot circumvent or abstract away the fundamental DAC characteristics.

1.8 PUBLICATION FROM THIS RESEARCH

The research that has been presented in this work has been formulated as an academic journal research paper and submitted to Elsevier Microelectronics Journal, which is a peer-reviewed journal. The paper was reviewed by the journal and accepted for publication by the journal editor. The journal is listed by the Thomson Reuters Web of Knowledge as:

- R. Reddy and S. Sinha, "A 6-bit, 500-MS/s current-steering DAC in SiGe BiCMOS technology and considerations for SFDR performance."

A comment from the journal is presented below:

"Paper is well-written, clear and sound, and the design method and procedure will be valuable reference for researchers to design current-steering DAC with better SFDR and low power."

1.9 CONCLUSION

This chapter introduced the research problem and hypothesis. The background to the research problem places the research in context. The organisation of the dissertation was outlined to introduce the path to be followed through the dissertation. Chapter 2 follows with a detailed literature review of the body of knowledge, followed by Chapter 3, which outlines the methods of research, simulation and experimental validation of the hypothesis. Chapter 4 contains the mathematical verification, system level design and the design considerations used in this research. Chapter 5 presents the layout of the prototype IC. Chapter 6 presents the simulation and experimental results and compares the work to the state-of-the-art. Chapter 7 concludes the research and provides a critical evaluation of the work presented, as well as suggestions for future research leading from this study.

CHAPTER 2: LITERATURE REVIEW

2.1 INTRODUCTION

The SFDR of high-speed DACs is a key specification in a variety of applications and is degraded by static and dynamic non-linearity [1], [4]. Static non-linearity arises from the mismatch between transistors, while dynamic non-linearity is attributed to switching and the finite output impedance of the current sources [1]. Dynamic non-linearity worsens as the operating frequency increases and is usually the limiting factor in achieving good SFDR in high-speed DACs [1].

The static performance, namely the integral non-linearity (INL) and differential non-linearity (DNL), can be further divided into systematic and random errors. Systematic errors are attributed to process, temperature and voltage variations, which can be compensated for by the layout of the current source matrix and inclusion of dummy current sources. Random errors are caused by transistor mismatch and are reduced by increasing the area of the current sources [4], [16]. Good static performance is necessary but not sufficient to achieve improved SFDR.

Measures of the dynamic performance are glitch energy, settling time and SFDR. The main factors that limit the SFDR are current source finite output impedance, clock feedthrough, propagation delay differences and imperfect synchronisation of the switches [5], [17].

An overview of the realisation of high-speed DAC architectures is presented. Several methods that have been used to improve the spurious performance in current-steering DACs are discussed, leading to recommendations to enhance SFDR in future work.

2.2 THE CURRENT-STEERING ARCHITECTURE

Current-steering DACs are preferred in applications where high-speed converters are required because of their high speed, low power consumption, small layout area and compatibility with CMOS processes. Both current sink and source designs are collectively referred to as current-steering DACs in the literature. In current-steering converters,

current is steered to the output from an array of current sources, based on an input digital word. This technique is referred to as flash conversion [4], [18], [6], [17].

The current sources may be unary or binary weighted. The unary weighted DAC employs a thermometer decoder to control each of the current sources individually. A unary weighted implementation employs one current source per quantisation level. As each current source carries the same weight; the matching requirements are relaxed. The unary weighted DAC exhibits an improved glitch energy and DNL, but increases the layout area and design complexity as the number of thermometer coded bits increase [3].

The binary weighted implementation employs one current source per bit and each current source has a value of twice the previous current source. Binary DACs occupy a smaller layout area and are easier to implement, as the current sources are directly controlled by the input word. However, the DNL, mismatch and glitch energy are degraded owing to the stringent matching requirements and input-dependent non-linearity [4], [2]. The integral INL is independent of the coding [2].

A combination of the two selection methods is often used and is referred to as segmented coding. Thermometer coding is usually used on the most significant bits (MSB), where the accuracy and reduced glitch energy are needed most. Binary weighted current sources are used on least significant bits (LSB) where the accuracy is not as critical and a reduction in the layout area is achieved [6]. The number of thermometer to binary coded bits is referred to as the segmentation ratio [2].

The effect of the segmentation ratio on performance has been well analysed for obtaining minimum area, good static performance and low distortion [2]. Varying the segmentation ratio alone cannot improve the SFDR any further without degrading other specifications. The techniques discussed aim to improve the SFDR beyond that of an optimally segmented DAC. They are directed towards the current-steering architecture because of its almost exclusive use in high-speed applications.

A block diagram of a representative eight-bit, segmented current-steering DAC is shown in Figure 2.1.

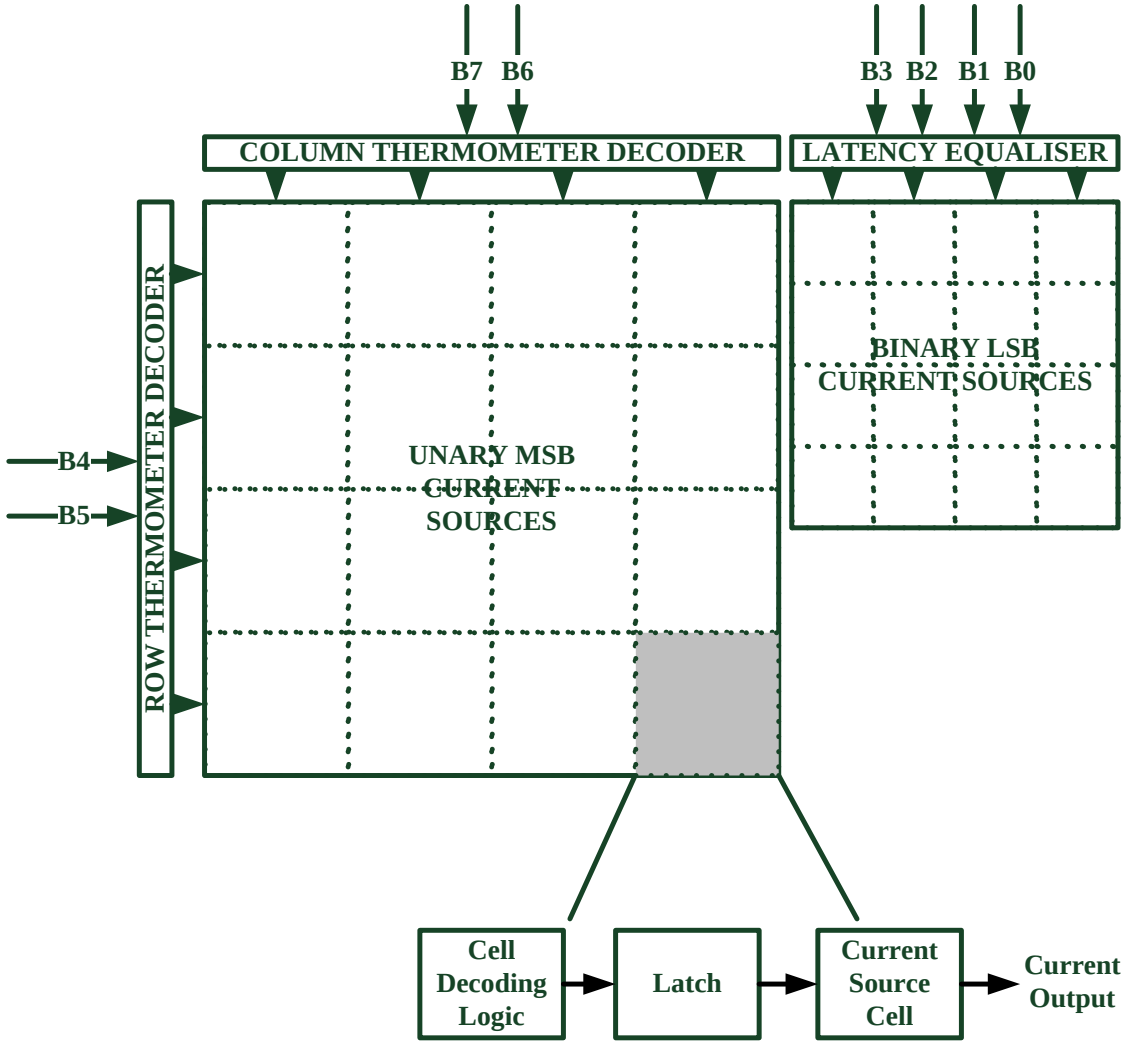


Figure 2.1: Functional block diagram of a representative eight-bit DAC with 50% segmentation ratio.

In Figure 2.1, a portion of the input digital word is passed through a thermometer decoder to control the unary weighted current source array. The remaining portion of the input digital word is passed through a delay circuit to synchronise it with the thermometer decoder and is used to control the binary weighted current source array directly. A latch is used to synchronise the input data and limit glitch energy. The current switches finally steer the generated current to one of the differential outputs [3].

2.3 FINITE OUTPUT IMPEDANCE AND MISMATCH OF THE CURRENT SOURCE CELL

The finite output impedance of the current source cell is a source of systematic error that affects the DAC linearity directly. As the input digital word changes, the number of current

sources connected to the output changes and different impedances are seen at the output. The total effective load impedance and hence the output voltage become signal-dependent, leading to non-linearity [8], [16]. In [5]. It is predicted that the non-linearity due to finite output impedance will worsen as the fabrication technology miniaturises owing to the lowering of the transistor transconductance. A reference current source cell is shown in Figure 2.2.

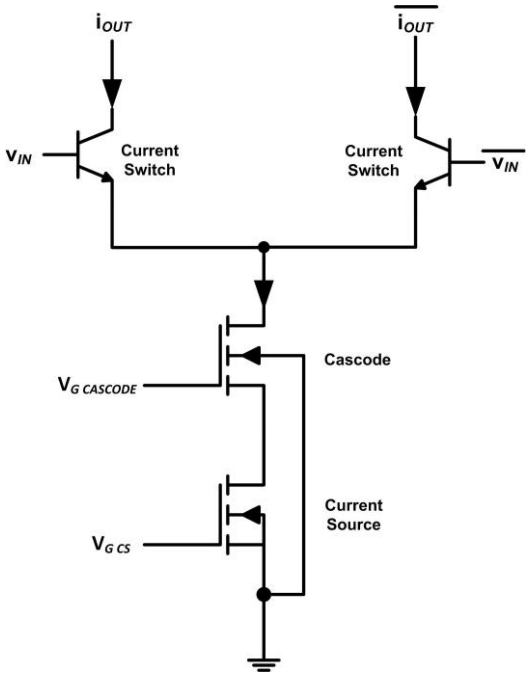


Figure 2.2: Typical reference source cell with cascode transistor.

In Figure 2.2, the current source is steered via the differential switch transistors to the DAC output or to a dummy output based on the input word. The cascode transistor is often used to increase the output impedance [4], [9].

Attempting to increase the output impedance directly does not yield a significant increase in SFDR, as shown in [17]. A local feedback loop was created around the cascode transistor with a folded cascode amplifier, which achieved only 40 dB of SFDR at an input frequency of 150 MHz.

A more successful approach followed in [8], representing an attempt to minimise that portion of the output impedance that is switching, termed the *switching impedance* [8]. Additional smaller current sources were added to ensure that the switch transistors were never switched off fully. This reduced the parasitic capacitance observed at the DAC

output. This technique reduced the effective switching capacitance, achieving an SFDR of 60 dB at an input frequency of 550 MHz on a 12-bit DAC operated at a sampling rate of 1.6 GS/s.

The aforementioned techniques used a pure CMOS process, unlike the 0.13 µm SiGe BiCMOS technology in [19]. A bipolar transistor was selected for the cascode transistor, as it has higher maximum gain, while a MOS transistor was chosen for the current source because it has higher output resistance and lower overdrive voltage. The 5 GS/s, BiCMOS current source cell was able to demonstrate a clear advantage in terms of achievable sampling rate.

The results, however, are not directly extendable to wideband applications, as the application was a narrowband radar receiver. The analysis of spurious performance in narrowband applications excludes the worst case spurious components that may reside several hundreds of megahertz away from the carrier frequency.

2.4 IMPERFECT SYNCHRONISATION OF SWITCHES

Mismatch between components and different propagation delays between logic paths result in distortion and glitches at the outputs of the decoder [1], [20]. Synchronised signals are ideally required to drive the switches, which can be achieved by using latches placed between the decoder and current source cells to minimise the timing skew between input digital data [18]. This technique is not effective at high sampling rates, as the clock that controls the latch degrades owing to worsening jitter, resulting in poorer SFDR [3]. In [5], it is predicted that the cell-dependent delay differences due to timing skew between the input digital data will become easier to meet because of the miniaturisation of the process technology, resulting in a smaller layout area.

The crossing points of the control signals need to ensure that at least one of the switches that compose the current-steering pair is on. In [9], this is achieved by varying the aspect ratio of the transistors. Furthermore, the delay differences between the LSB and MSB cells were compensated for by placing delays to the LSB cells. Experimental results for this highly optimised latch structure were obtained from a 10-bit, 100 MS/s DAC, which demonstrated an SFDR of 66 dB. The measurement was performed at an input frequency of 2 MHz and would degrade as the input frequency approached the Nyquist rate. Well-

designed latch structures are required but are insufficient to meet wideband SFDR requirements.

2.5 SWITCH CLOCK FEEDTHROUGH

Switches are used to steer current to the DAC output based on an input digital word. Clock or signal feedthrough is the term for switching noise that couples to the drain of the switch transistor via the gate-drain capacitance [9]. Clock feedthrough causes drain voltage variation and hence current variation, resulting in the degradation of SFDR.

The glitch induced by the clock feedthrough is proportional to the input signal step, regardless of the coding strategy [21]. A swing-reduced driver (SRD) is a circuit technique designed to limit the swing of the controlling signal of the switches to minimise the fluctuation of the drain voltage. A swing reduction in [18] from 3.3 V to 400 mV was able to achieve a 12-bit DAC with an SFDR of 67.6 dB at an input frequency of 10 MHz.

Attempts have also been made to cancel instead of minimise the clock feedthrough by adding dummy transistors to produce an opposite voltage spike [9]. The success of these techniques is difficult to measure in practice.

The 10 bit DAC in [9] obtained an SFDR of 60 dB at 100 MS/s for input frequencies of up to 10 MHz. An effective swing reduction can be achieved by lowering the minimum differential input voltage to enable a transistor in the switch pair to carry all the current [22]. This was achieved via source degeneration but was only verified at low input frequencies under 1 MHz.

2.6 SUB-DAC TOPOLOGY

A sub-DAC or hybrid DAC topology employs smaller DACs to act on portions of the input bits. For example, a segmented DAC architecture can be considered to consist of two sub-DACs.

Sub-DAC topologies have recently been used to reduce the area, number of control signals and switches required. In [18], a 12-bit DAC was realised by employing four identically sized thermometer-coded sub-DACs of four bits. The current output generated at the output of each sub-DAC is connected through scaled resistors to provide the necessary scaling. This type of architecture exhibits better matching properties and a significantly

reduced area. In [22], a similar sub-DAC topology was used, which also resulted in a significantly reduced area.

The variation of the segmentation ratio and the effect on the performance metrics in current-steering DACs have been well investigated, among others in [2] and [23]. However, the use of sub-DAC topologies such as in [22] and the effect on the SFDR have not been derived. These alternative architectures have already shown a reduction of area and simplicity in design and may enhance SFDR.

2.7 CONCLUSION

A review of the body of knowledge on high-speed DACs has been presented. Virtually all high-speed DACs are based on the current-steering architecture. Improving the frequency performance of high-speed DACs focuses on various elements of the current-steering architecture. The various derivatives of current-steering DACs and the trade-offs of each have been discussed. Unary, binary and segmented DACs are used extensively to realise high-speed DACs.

The research and literature on the key elements of current-steering DACs was presented. The finite output impedance, imperfect synchronisation of switches and clock feedthrough are primary considerations to improved SFDR. The existing techniques and methods to improve SFDR have been presented. From this review, a research gap emerges in the use and impact of BiCMOS technology on the DAC architecture, current source cell circuit and ultimately the effect on SFDR performance.

CHAPTER 3: RESEARCH METHODOLOGY

3.1 INTRODUCTION

The research methodology followed to test the hypothesis under question is detailed in this chapter. The experimental DAC IC is implemented in IBM 8HP technology, which is a SiGe 0.13 µm BiCMOS fabrication process. The process and the corresponding models are detailed and their incorporation into the tool chain is described.

The effects of clock feedthrough, switch distortion and finite current source output impedance have been identified as the factors contributing to SFDR degradation and the reduction of these effects will be investigated via theoretical study.

The resulting circuit level implementation is verified and optimised through simulations in the Cadence Virtuoso software package using the 0.13 µm SiGe IBM BiCMOS 8HP process design kit (PDK). The resulting simulations provide first-order estimates of the achievable SFDR. The Cadence Virtuoso software package comprises various features, which are used at all stages of the research, and is described in further detail in this chapter.

The layout of the prototype IC is detailed and factors affecting SFDR are discussed. The prototype IC was fabricated as part of an MPW fabrication run. The supporting peripherals required to test the prototype IC are presented.

The prototype IC was packaged in a quad flat no-lead (QFN) package and mounted on a PCB. An FPGA is used to generate the input digital data. A spectrum analyser and digital oscilloscope are used to measure the frequency and time domain performance respectively. The measurement setup forms a critical aspect of the research, as it will influence the measured SFDR. The measurement and equipment requirements are further specified in this chapter.

3.2 MANUFACTURING PROCESS

The IBM 8HP technology is a SiGe 0.13 µm BiCMOS fabrication process that offers high performance HBT with a unity gain frequency (f_t) of over 200 GHz and forward current gain (β) of over 600. The collector of the HBT transistors is heavily doped in order to

achieve a high unity gain frequency. The IBM 8HP process is IBM's fourth generation SiGe foundry technology [24]. The IBM 8HP process is a speciality foundry designed for high-performance radio frequency (RF) applications. The HBT switches offer a significant advantage in current steering DACs to realise the switch transistors and achieve a higher sampling rate in comparison to a CMOS only process.

As a result of the heavy collector doping, the breakdown voltage of the transistor is lowered. In the IBM 8HP process, a breakdown voltage of 1.77 V is expected. The breakdown voltage poses a constraint on the current-switching transistors but can be increased depending on the transistor bias and base resistance, which are of relevance to the output stage of the DAC.

BiCMOS technology combines MOSFETs and HBTs that offer improved gain, noise, frequency and linearity characteristics. These factors have a direct and indirect relation to the spurious performance and can improve the SFDR that is attainable with CMOS-only technology.

The IBM 8HP process offers up to seven metal layers. For MPW runs, all of the metal layers are supported. The supply voltages are 1.2 V or 1.5 V for the core and 2.5 V for input/output (IO) pads. The process is well suited to applications that require analogue and digital sections to be merged onto a single IC. The isolation between these sections is achieved via 6 µm deep trench isolation minimising perimeter capacitance from collector to substrate.

The addition of germanium to the transistor base results in lower band-gap energy, resulting in improved transistor speed, current gain and Early voltage [25], [26]. This increased speed or lowering of the base transit time results in unity gain frequencies of over 200 GHz.

The Early voltage is inversely proportional to the output impedance of the transistor. When the HBT is used as the switching transistor, the increased Early voltage directly improves the SFDR. Both the Early voltage and base transit time are directly linked to the distortion and final DAC SFDR performance. The HBT also allows the DAC to operate at higher sampling rates.

The SiGe HBT switches can be realised in two configurations, namely collector-base-emitter (CBE) or collector-base-emitter-base-collector (CBEBC). The CBEBC configuration offers better frequency performance at the expense of area. The simplified typical BiCMOS process cross-section is shown in Figure 3.1.

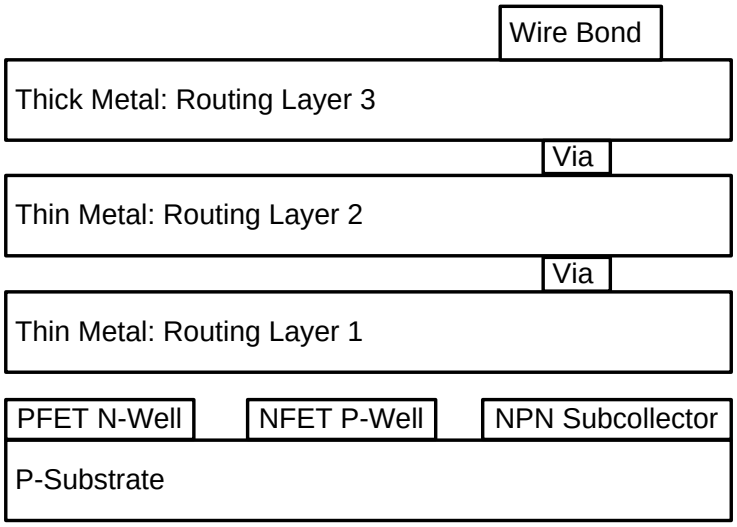


Figure 3.1: Simplified process cross-section for typical BiCMOS process.

In Figure 3.1, a typical process cross section of a BiCMOS process is shown that consists of a P-type substrate. NMOS and PMOS transistors can be created using a P-Well and N-Well respectively. The IBM 8HP process offers two different NPN transistors. The first is a high-performance model that is able to obtain a unity gain frequency of 200 GHz at a low breakdown voltage of 1.8 V. This model is of key interest in this work because of its high unity gain frequency and high forward current gain. The second model offers a high breakdown voltage of 3.5 V at the expense of speed and is of less importance in this work. The PDK supports a Vertical Bipolar Inter-Company NPN model, which accounts for many higher order effects such as weak avalanche, quasi-saturation region modelling and self-heating [24].

There are also two different field effect transistor (FET) models. The 2.2 nm thin FET is used for internal logic and operates at 1.2 V or 1.5 V. The thin FET is used extensively for all digital decoding circuitry. The 5.2 nm thick FET is used for IO functionality and operates at 2.5 V. The PDK uses version 4 of the Berkeley short-channel IGFET model (BSIM4) as a foundation for FET modelling.

Modern fabrication processes such as the IBM 8HP process have shrunk the FET channel length significantly to the extent that second order short-channel effects are pronounced. The minimum channel length in this process is 130 nm. The short-channel effects arise from phenomena known as, drain-induced barrier lowering (DIBL), mobility reduction and interdependence of threshold voltage on transistor dimensions and gate voltage.

In the classic MOS transistor models, the V_{TH} is independent of the drain voltage. DIBL is a short-channel effect that arises from the proximity of the drain to the channel so that a high drain voltage can turn on the transistor prematurely. At sub-micron process nodes, the influence of the drain potential on the channel region can have a serious impact on the performance of sub-micron MOS transistors. The drain current is controlled not only by the gate voltage, but also by the drain voltage.

There are also thin and thick decoupling capacitors and a single nitride metal-insulator-metal capacitor. There are diffusion, polysilicon and Tantalum Nitride resistors, which are selected based on the desired resistance.

Other devices that are supported are:

- triple-well NFET,
- NMOS transistor,
- hyper-abrupt junction varactors,
- forward bias diode,
- programmable electronic fuse,
- high density and/or high Q series and parallel spiral inductors,
- transmission line and distributed passive RF elements and
- wire bond and solder bump (C4) terminals.

Access to the IBM 8HP process is provided by the MOSIS integrated circuit fabrication service. MOSIS provides an MPW service to prototype scholarly research for prototype and low-volume fabrication. Multiple designs are concatenated onto a single die to provide access to a state-of-the-art fabrication service that would otherwise be too costly for scholarly research in which once-off designs are tested.

3.3 COMPUTER AIDED DESIGN ENVIRONMENT

The Cadence Virtuoso Custom Design Platform is an electronic design automation tool produced by Cadence Design Systems that supports all stages of IC design and verification. The environment is fabrication technology independent and supports multiple fabrication processes via a foundry-specific PDK.

The Cadence Virtuoso Custom Design Platform caters for digital, analogue and mixed signal design flows in a single integrated design environment. The design flow supports high-level and low-level design techniques such as full custom, standard cells, gate array, structured design and cell libraries.

The PDK contains all the manufacturing related parameters, including design rules and characterised models that are needed to ensure that it will be possible to manufacture a design according to the original design intent. The device models are Silicon calibrated, ensuring the manufactured performance closely matches simulation results. These device models are linked directly to the Virtuoso environment. The design process and corresponding tools are shown in Figure 3.2.

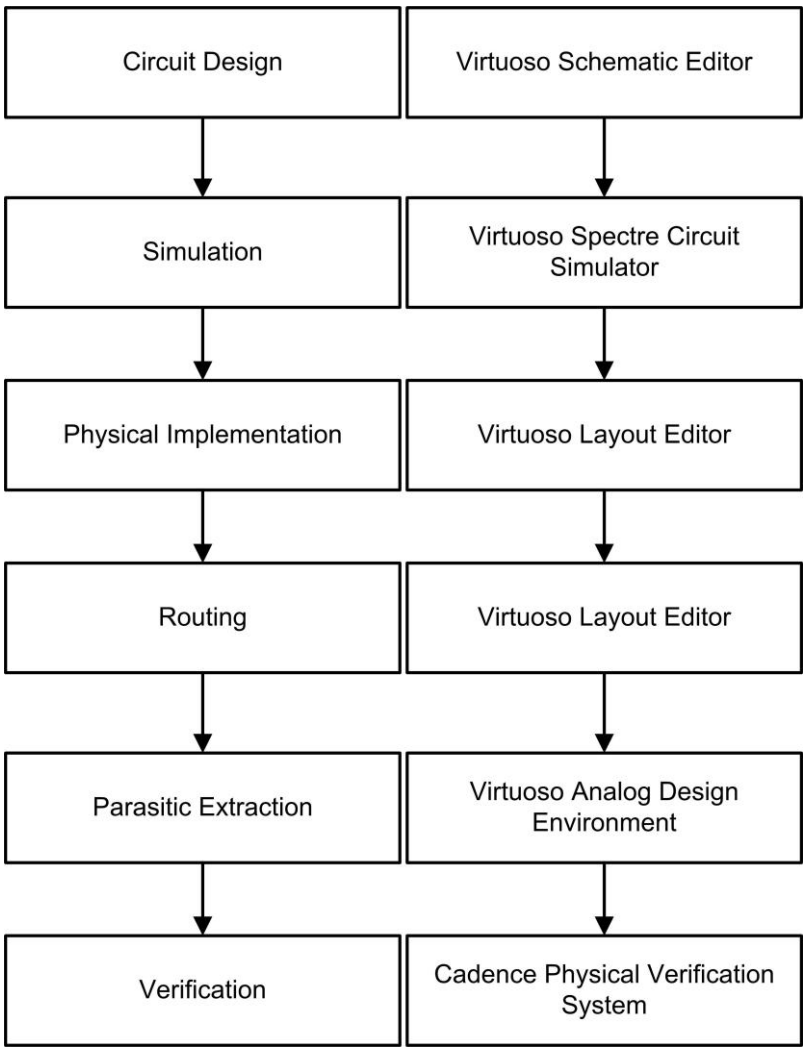


Figure 3.2: Tool support for the different aspects of circuit design.

In Figure 3.2, the Virtuoso Schematic Editor was used for design entry of analogue and digital circuits. It supports hierarchical schematic design. Different cell views may be created to view a circuit in different forms such as symbol, schematic or layout. The Virtuoso Schematic Editor also performs design checking. The tool then outputs a net-list that may be used for simulation and layout.

The Virtuoso Schematic Editor provides an open simulation system net-list generator for various simulators to be invoked. The Virtuoso Spectre Circuit Simulator was used for enhanced Simulation Program with Integrated Circuit Emphasis (SPICE) type simulations. The Virtuoso Spectre Circuit Simulator may be directly invoked from the Virtuoso Schematic Editor. An Analog Waveform Display (AWD) tool is coupled to the simulator to allow for the viewing of waveforms. The Virtuoso Layout Editor was used to create the layout for fabrication. The Virtuoso environment also performs design rules check (DRC) and layout versus schematic (LVS) tests. The DRC and LVS checks form part of the

Virtuoso Physical Verification System. Finally the Virtuoso Analog Design environment can also perform parasitic extraction and post-layout simulation that will take into account the layout parasitic elements.

Cadence Virtuoso Layout Suite, which is a component of the Cadence Virtuoso package, is the design software used to create the custom IC layout that provides the capability to create complete physical layouts. The close coupling of Cadence Virtuoso Schematic Editor and Cadence Virtuoso Layout Suite allows design closure with a quicker turnaround time by automating DRC and LVS checks.

Cadence Virtuoso Layout Suite allows for the creation of cell views in the layout, which allows the designer to create the layout once and re-use it across the design. This is identical to the methodology used in Cadence Virtuoso Schematic Editor and allows the layout hierarchy to match the circuit schematic.

3.4 INTEGRATED CIRCUIT PACKAGING

Physical connections to the external world are required in order to test the DAC IC. The DAC IC was packaged in QFN packaging. The alternate method using on-wafer probing was not suitable for this design. On-wafer probing is preferable when possible, as it directly stimulates and probes signals on the die, thus eliminating bonding wire and packaging parasitics. On the DAC digital interface, on-wafer stimulus of the input data bus and clock signals was not possible with the instrumentation available.

Twenty-one pads were used. Twelve were used for the input differential data and an additional two pads carried the clock signals. The DAC has two outputs and the remaining pads were used for power signals. A 64-pin QFN package was used, as the design formed part of an MPW run. A bonding diagram of the die and QFN package is shown in Appendix D.

Following the analysis in [27], the bandwidth for the package may be estimated. The bandwidth for signals travelling from the pin to the die is estimated. This corresponds to the input digital pins, which have a higher bandwidth requirement than that of the analogue output pins. The lumped circuit model parameters for the bond wire are estimated from [28] for a diameter of 1 mil and a wire length of 5 mm and are:

$$
\begin{aligned}
L_{wirebond} &= 5.8\ nH \\
C_{wirebond} &= 242\ fF \\
R_{lead} &= 257\ m\Omega \\
L_{lead} &= 2.06\ fH \\
C_{lead} &= 500\ pF
\end{aligned}
\tag{3.1}
$$

The bond wire is modelled by passive parasitic elements. The circuit to estimate the bandwidth of a QFN pin used for a digital input is shown in Figure 3.3.

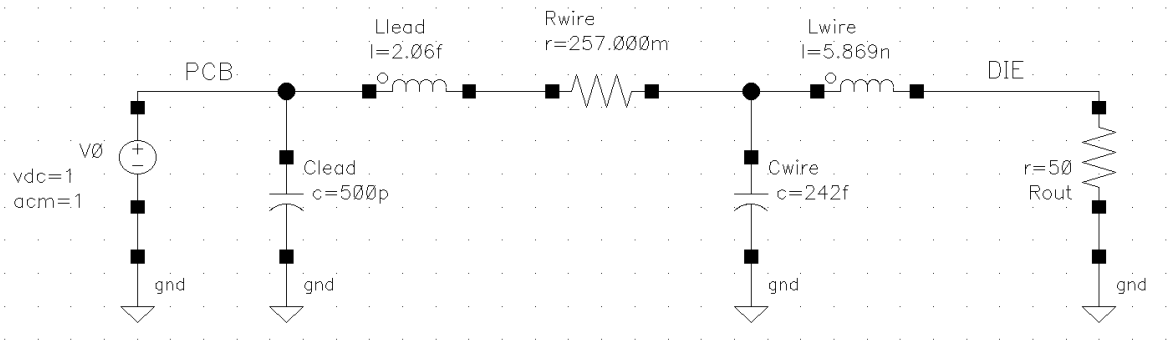


Figure 3.3: Lumped lead and wire bond parasitic RLC parameters for QFN input.

The bond wire modelled in Figure 3.3 will influence the maximum sampling rate at which the DAC can be operated. In order to estimate the effect of the bond wire, an AC analysis was performed on the circuit and the resulting frequency response is shown in Figure 3.4.

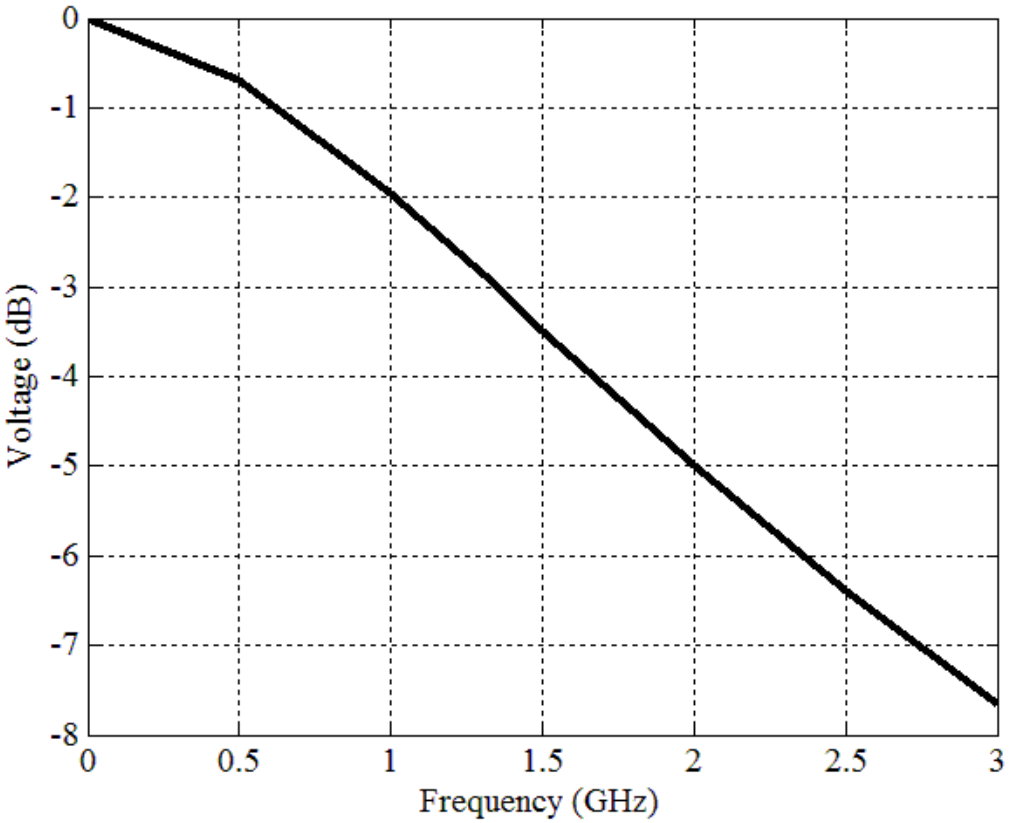


Figure 3.4: Bode plot estimating the frequency response of a QFN package.

The bandwidth of a QFN pin is estimated to be 1.3 GHz shown in Figure 3.4. This is adequate for the purposes of this research, as the digital inputs are clocked at a maximum of 500 MS/s. The packaging does impose a restriction on the DAC to operate at higher frequencies. However, even in commercial applications operating above 1 GS/s, de-multiplexing is used to distribute the digital data across multiple digital inputs.

3.5 PRINTED CIRCUIT BOARD

In order to evaluate the hypothesis under question experimentally, a PCB was designed and manufactured. The PCB incorporated the DAC IC and the surrounding circuitry. A high-level block diagram of the PCB is shown in Figure 3.5.

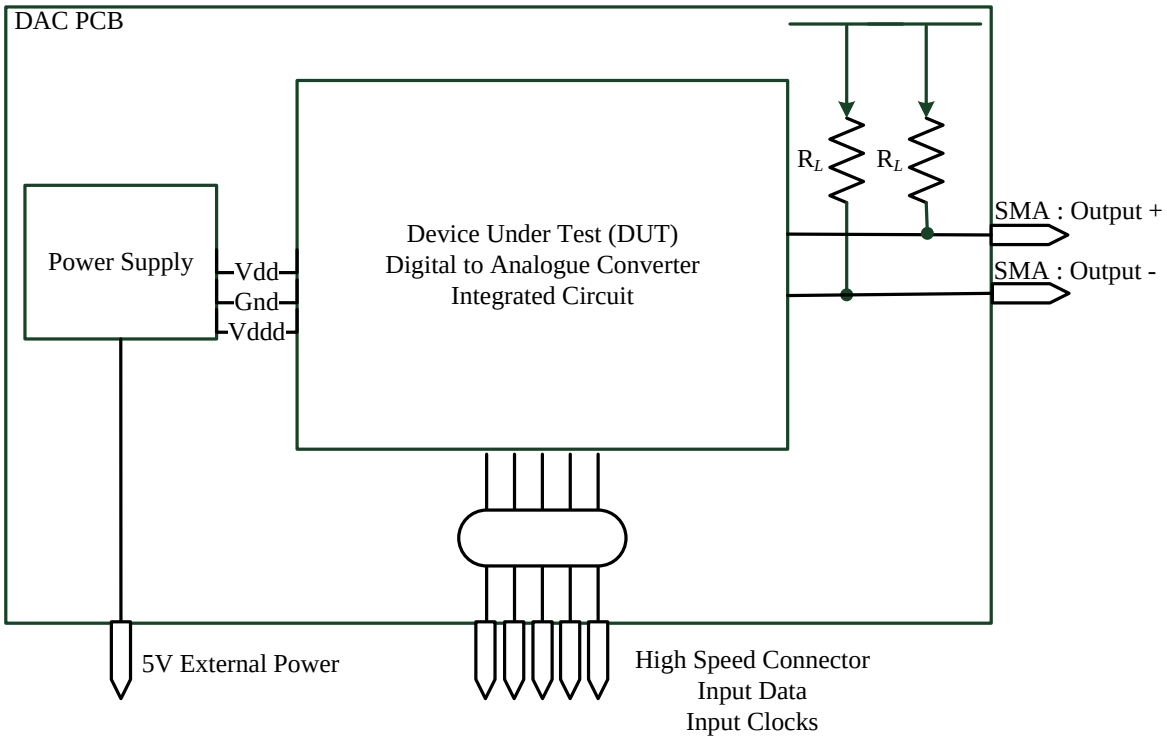


Figure 3.5: High-level PCB block diagram.

As shown in Figure 3.5, provision for power was made available via a header, which will allow an external power supply to power the setup. The output of the DAC was fed to a Sub-Miniature-A (SMA) connector and an on-board test point. The SMA connector is a 50 Ω treaded connector. This setup allowed the measurement equipment to measure the time and frequency domain specification.

The input to the DAC IC was supplied from an FPGA that resides on existing Council for Scientific and Industrial Research (CSIR) hardware modules. A high-speed connector allows the FPGA to drive the DAC with data and a clock. The full PCB schematic and layout are detailed in Appendix A.

3.6 MEASUREMENT EQUIPMENT

In order to measure time-domain specifications accurately, a wideband, fast settling time oscilloscope was required. The required oscilloscope bandwidth may be calculated based on the rise and fall time of the DAC output [29]. The oscilloscope bandwidth is ideally two to three times greater than the signal bandwidth to characterise the second and third harmonics. The following equation may be used to estimate the minimum required oscilloscope bandwidth:

$$\begin{aligned} &Minimum\ Oscilloscope\ Bandwidth \\ &= 3 \times \frac{0.35}{t_r} \\ &= 3\ \frac{0.35}{400\ ps} \\ &= 2.625\ GHz \end{aligned} \tag{3.2}$$

The parameter t_r represents the rise time of the signal and is estimated to be 400 ps based on the characteristics for a Xilinx Virtex 4 FPGA specification [30]. A Tektronix DSA 71254 digital oscilloscope and digital signal analyser will be used for time domain measurements. The instrument is available at the CSIR and is shown in Figure 3.6. The oscilloscope meets the bandwidth requirements with 12.5 GHz of analogue bandwidth at a sampling rate of 50 GS/s. Four channels are available that cater for the measurement of the DAC true and complementary outputs simultaneously.

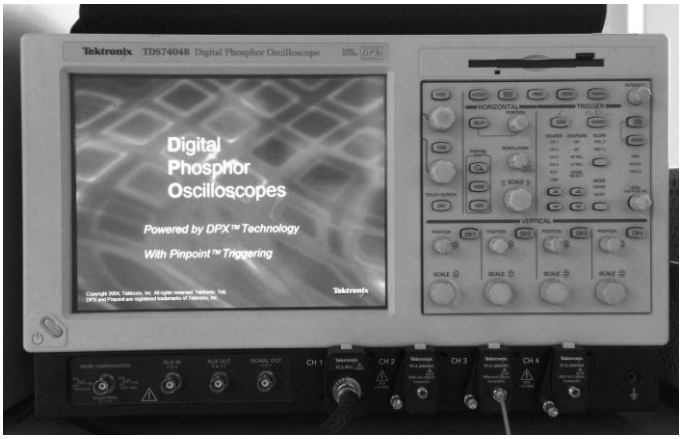


Figure 3.6: Tektronix DSA 71254 digital oscilloscope and digital signal analyser.

The oscilloscope in Figure 3.6 also has built-in logic analyser functions to characterise logic circuit performance with correlated analogue and digital signal views. The logic analyser is able to provide timing resolutions of 80 ps, which are adequate for this nvestigation. The input sensitivity may be used at a 10 mV/division scale resulting in a full-scale amplitude of 100 mV. It will be necessary to ensure that the DAC IC design has sufficient voltage swing to utilise the oscilloscope dynamic range fully. In addition to bandwidth requirements, the sensitivity of the scope should be sufficient to measure the desired error band.

An Agilent E4440A PSA Spectrum Analyser covering a frequency range from 3 Hz to 26.5 GHz will be used for the frequency domain measurements. The instrument is available at the CSIR and is shown in Figure 3.7.

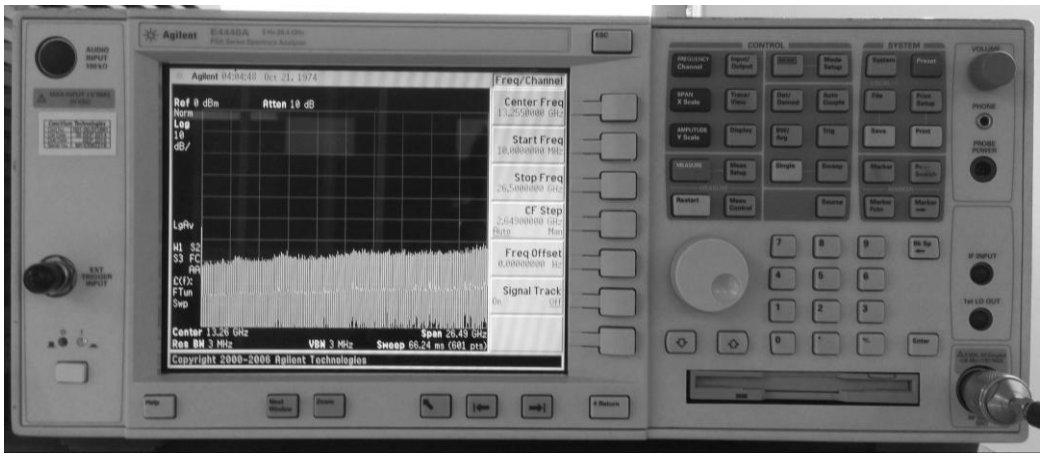


Figure 3.7: Agilent E4440A PSA Spectrum Analyser.

The spectrum analyser in Figure 3.7 can measure the amplitude with an accuracy of 0.2 dB across the resolution bandwidth range. The second and third harmonic inter-modulation distortion is typically better than -80 dBc, which will not influence the SFDR measurement. In addition, the instrument is terminated with a 50 Ω load and can connect directly to the DAC output.

3.7 MEASUREMENT SETUP

The DAC IC to verify the hypothesis experimentally was measured in order to compare simulated to real world performance. The complete measurement configuration is shown in Figure 3.8.

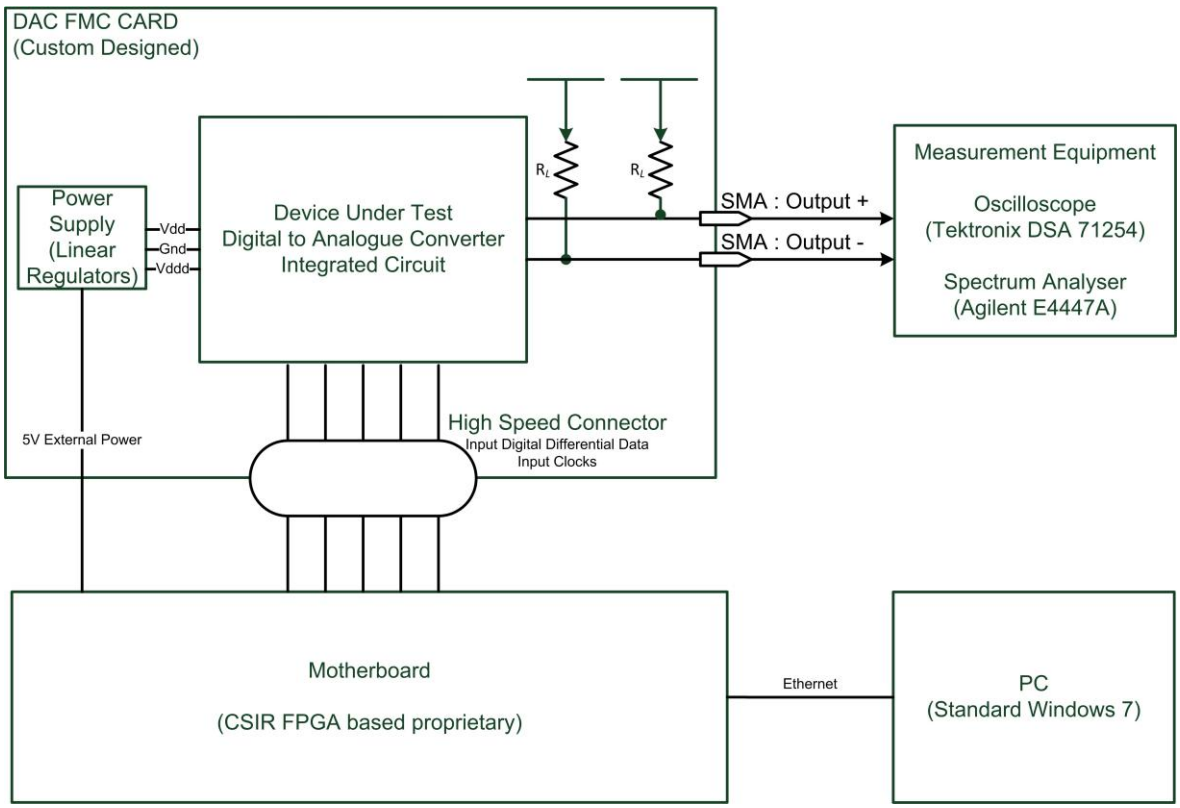


Figure 3.8: Measurement setup.

The measurement setup in Figure 3.8 was required to measure static and dynamic parameters of the DAC. In order to characterise the DAC performance adequately, the sampling rate had to be varied. Both time and frequency domain measurements were performed.

Of the static parameters, the INL and DNL were measured to ensure that the DAC exhibited monotonic behaviour. Static performance was necessary but not sufficient to enhance the DAC SFDR. For both measurements, the DAC input was changed across all quantisation levels and the corresponding output voltage measured using a digital oscilloscope. The dynamic performance of the DAC was evaluated by measuring the SFDR and signal-to-noise ratio (SNR) in the frequency domain. The DAC was stimulated with pure sine wave digital data at various frequencies.

3.8 CONCLUSION

The research methodology followed in this research was presented. The tools and technologies used to verify the hypothesis experimentally were discussed.

The SiGe process technology has various device structures and models available, including MOS and HBT transistors. The available models in the process technology are incorporated via the PDK into the Cadence Virtuoso Custom Platform.

The Cadence Virtuoso Custom Platform caters for all the necessary tools to design, simulate and manufacture an IC. The Virtuoso environment will be used for schematic entry, simulation, layout and verification.

The measurement setup forms a critical portion of the experimental verification of the hypothesis. The measurement setup and the measurement equipment have been specified in order to minimise their effect on the SFDR. A wide-band oscilloscope and spectrum analyser will be needed to characterise the DAC performance. High-level PCB requirements were discussed, completing the measurement setup requirements.

CHAPTER 4: MATHEMATICAL AND SYSTEMS DESIGN

4.1 INTRODUCTION

The mathematical and system design of the DAC is considered in this chapter from a theoretical and practical perspective. The primary functions that need to be performed by the DAC circuits are current generation, current-steering and control of current-steering, in addition to secondary functions such as biasing and high-speed digital inputs. General architecture considerations are first explored, followed by linearity matching requirements.

The matching of the current sources determines the static linearity of the DAC, which is a prerequisite to good SFDR performance. The matching requirements for DNL and INL lead to the design of the current source transistor. A systematic iterative procedure is introduced to design the current source. Based on the predicted output impedance, an additional cascode transistor is introduced and designed to increase the output impedance and SFDR. The HBT current switches are also designed, which concludes the current source cell design.

A switch driver circuit is introduced that functions as a signal-conditioning circuit to synchronise incoming digital signals to the clock. The switch driver incorporates a SRD that reduces the amplitude swing to minimise the clock feedthrough effect. An LVDS receiver circuit is designed to enable the DAC to accept high-speed digital data to test at higher sampling rates. Lastly, the complete DAC circuit design is presented.

4.2 ARCHITECTURE SELECTION

The primary functions of the DAC are current generation, current-steering and control of the current-steering. The secondary functions of the DAC are signal conditioning, biasing and high-speed digital inputs. The application, speed and area specifications of the DAC determine the optimal weighting of the current source cells, which are unary or binary weighted.

The circuit configuration for the current source cell is shown in Figure 4.1. The current source cell comprises a current source, cascode and switching transistors.

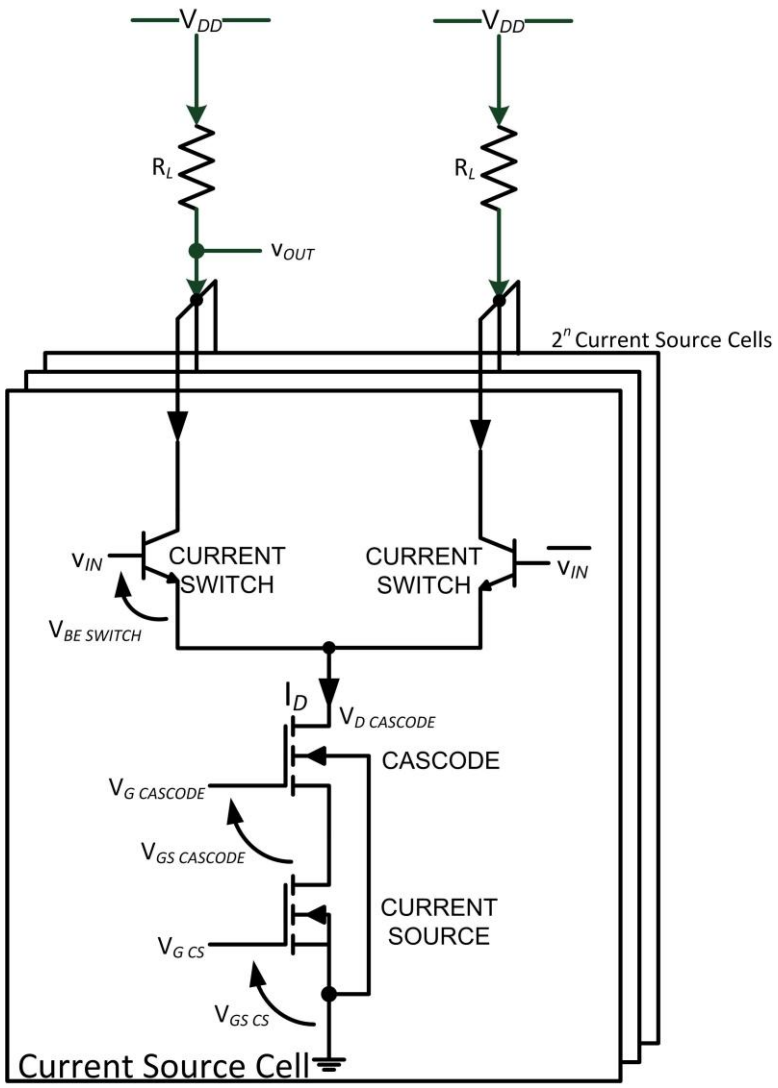


Figure 4.1: Current source cell.

The input word controls the number of current source cells shown in Figure 4.1 that are connected to the DAC output. The unary weighted DAC uses a thermometer decoder to control each of the current sources individually, relaxing matching requirements and lowering the glitch energy at the expense of increased area and design complexity. In a binary weighted DAC, the current sources are directly controlled from the DAC input, resulting in a smaller area, decreased design complexity and more importantly, increased speed. These benefits come at the expense of inferior DNL and glitch energy owing to the stringent matching requirements and input-dependent non-linearity.

While a thermometer-decoded unary weighted DAC will achieve better linearity and reduce glitch energy, a binary weighted implementation is selected as the architecture for improved speed. The binary weighted DAC also exhibits a lower complexity and power

dissipation because a thermometer decoder and an additional retiming stage can be omitted and is often selected when very high sampling rates are required.

The selection of the number of bits places a finite restriction on the DAC's dynamic range owing to the amplitude quantisation effect. The quantisation effect degrades the SNR that may be approximated by (4.1) [31]:

$$\frac{S}{N} = 6.02\,n + 1.76\,dB \tag{4.1}$$

The converter's second harmonic component is a function of the output impedance of the unit current source cells and is considered in Section 4.6. The amplitude quantisation also introduces a third harmonic component that is given by the equation (4.2) [31]:

$$A_3 = 2^{-n\frac{3}{2}} \tag{4.2}$$

Table 4.1 shows the approximated SNR and third harmonic distortion for various resolution DACs, which impose a theoretical limit on SFDR performance.

Table 4.1: Theoretical limits to SFDR performance.

Number of bits (n)	Signal to noise ratio (SNR)	Third Harmonic
4	25.84 dB	36.12 dB
5	31.86 dB	45.15 dB
6	37.88 dB	54.18 dB
7	43.90 dB	63.21 dB
8	49.92 dB	72.25 dB
10	61.96 dB	90.31 dB
12	74.00 dB	108.37 dB
14	86.04 dB	126.43 dB
16	98.08 dB	144.49 dB

Ideally, a higher number of bits will lead to better SNR as shown in Table 4.1. However, for every bit increase, the required current source cell matrix area will double. In addition to this, the matching requirements, which are discussed further in subsequent sections, become more stringent. To meet the random matching requirements, the area occupied by a single current source cell also doubles [32]. The total layout area hence increases by a

factor of four per bit increase. The layout and decoding complexity also become more difficult with a higher resolution.

The number of I/O pins increases for every bit increase as well. As this design is an MPW, the chip area and I/Os are shared across multiple designs; the number of I/Os in total is limited to 16 per design if shared equally. As two of the other designs in the MPW use on-chip wafer probing, the I/O constraint is relaxed to allow for 21 I/O pads for this design. This limit stems from two constraints.

The I/O pad and bonding wire rules are the first constraint [24]. These rules are summarised below:

- The bonding wires must not exceed an angle greater than 45 degrees.
- The number of pads on a side must not exceed the number of bonding fingers along the cavity edge of a package by more than two.
- The pads must be placed along the chip edge in accordance with spacing rules. It is recommended that the pads be distributed evenly among all sides of the device.
- Bonding wires must not pass over any active circuitry.

The second is the layout of the IC, which is such that each design in the MPW occupies a quadrant, illustrated in Figure 4.2. Hence a quarter of the chip periphery is allocated to each design.

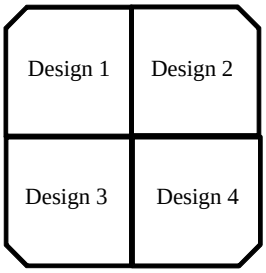


Figure 4.2: Multi-project wafer layout.

An alternate layout, such as dividing the die into four rectangles that run horizontally from edge to edge, would potentially be able to accommodate more I/O pads in the designs that occupy the top and bottom positions. However, owing to various considerations stemming from a consolidated view of all the designs in the MPW, it was decided to adopt the layout template of Figure 4.2.

The layout, bonding wire and pad constraints limit this design to six bits because of the availability of a maximum of 21 I/O pads. A resolution of six bits is chosen, which places a limit of approximately 37.88 dB on the SNR. The limitation of six bits resolution is adequate for testing the key SFDR principle proposed in this dissertation.

4.3 MATCHING REQUIREMENTS FOR DIFFERENTIAL NON-LINEARITY

The DNL is the worst case deviation from an ideal LSB step between two subsequent output codes and is of particular importance when generating small signals. A monotonic DAC meets the criterion that for each subsequent digital input code, the output analogue value increases. The DAC design must be constrained to guarantee the desired monotonic behaviour.

In all practical DACs, the quantisation steps have limited accuracy because of a mismatch between design elements such as transistors. The DNL specification is architecture-dependent [31]. In a binary weighted converter, the maximum DNL must be less than twice the maximum INL [31]. In order to guarantee monotonic behaviour for a binary weighted converter, the following relationship must be satisfied [31]:

$$\mathrm{DNL} < 2 * INL = 2 * 0.5\ LSB = 1\ LSB\ . \tag{4.3}$$

However, the DNL specification is usually specified to be more stringent:

$$\mathrm{DNL} < 0.5\ LSB. \tag{4.4}$$

The DNL specification together with the INL will impose a requirement on the matching accuracy. While every transition of the input digital word will need to satisfy this requirement, the most stringent matching requirement is architecture-dependent.

For a binary weighted converter, the midscale transition is the most stringent. For an *N*-bit binary weighted converter, the midscale transition is between word (2^{N-1}) and ($2^{N-1} - 1$). At this transition, ($2^{N-1} - 1$) current sources must match within 0.5 LSB of (2^{N-1}) unrelated current sources. The current sources are assumed to exhibit an approximately normal distribution according to the central limit theorem.

A good approximation for the DNL is the standard deviation of current for a single increase in the quantisation level, which is represented by $\sigma(\Delta I)$.

The DNL is calculated at the worst case scenario, which occurs at the DAC mid-scale transition:

$$\sigma^2(\Delta I) = \sigma^2(2^{N-1}I - (2^{N-1} - 1)I)$$
$$\frac{\sigma(\Delta I)}{I} < 0.063 \; or \; 6.3\% \tag{4.5}$$

The result is that the standard deviation for each current source must be within 6.3 % to meet the DNL specification. The INL specification will add an additional constraint on the standard deviation. The more stringent of the INL and DNL constraint will be used to derive matching parameters.

4.4 MATCHING REQUIREMENTS FOR INTEGRAL NON-LINEARITY

The INL is the worst case deviation of the actual DAC output from an ideal DAC output across all quantisation levels. The INL determines the overall DAC linearity and is important for large signals [31]. In order to guarantee monotonic behaviour, the following relationship must be satisfied:

$$INL < 0.5 \; LSB \tag{4.6}$$

The matching is influenced by the process gradient of the manufacturing process. The INL yield is the percentage of manufactured DACs that meet the INL linearity specification. The INL yield was introduced to compute the standard deviation of a unit current source quantitatively to meet INL specifications [33]. In order to characterise the INL yield statistically, Monte Carlo simulations are typically required. Monte Carlo simulations are processor-intensive, time-consuming and do not provide the designer with insight into the trade-offs required to improve the INL yield [33].

A more insightful yet accurate method resulting in parametric expressions was introduced in [33] and will be followed to derive the matching requirements to meet the INL specification. The problem may be approached in two ways. The first is to specify the required INL and then derive the minimum required current-matching accuracy and INL

yield. The alternative and more useful approach, which is to specify the required INL yield and then derive the minimum required current matching-accuracy, is followed.

Following the approach in [33], the standard deviation for a unit current source cell is:

$$\sigma < \frac{A}{\sqrt{2^N}} Z(Y) \tag{4.7}$$

The parameter *A* represents the INL specification in the units of LSB, which is 0.5 for this design. The parameter *N* represents the number of bits resolution of the DAC. The INL yield requirement determines *Z(Y)*, which is well tabulated in the literature and is derived via Monte Carlo simulations. From [33], Figure 4.3 plots *Z(Y)* against INL yield.

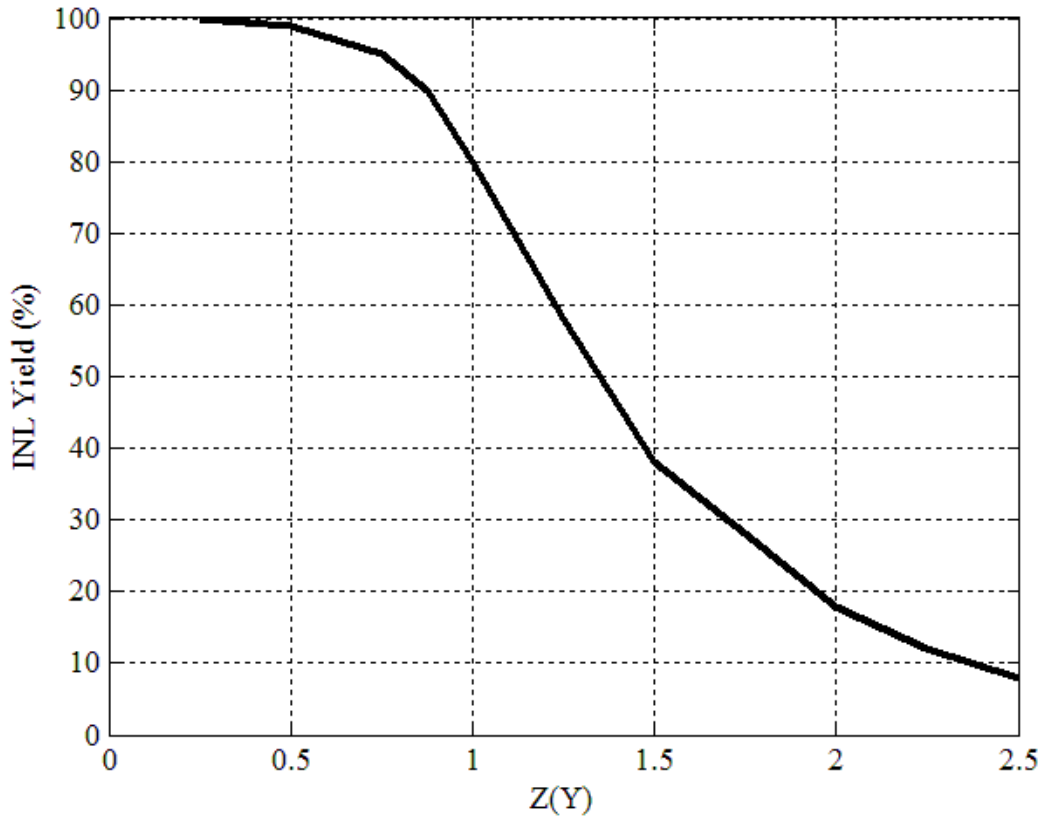


Figure 4.3: Tabulated INL yield [33].

The INL matching requirement results in a required standard deviation of each current source cell to be within 3.12 % from Figure 4.3. The INL matching requirements are more

stringent than the DNL matching requirements for this design and will be used to design the current sources.

4.5 CURRENT SOURCE TRANSISTOR DESIGN

4.5.1 Design Methodology

The current source transistor design is a central element in a current-steering DAC. The matching requirements for INL and DNL are required to be met to ensure monotonic behaviour and static performance. The INL and DNL matching requirements require that the standard deviation of a unit current source be within 3.12 % and 6.3 % respectively. The INL is the more stringent requirement in this design.

Based on the Pelegrom model, for a given technology the relative standard deviation of a current source is determined by its overdrive voltage and gate area [33]. Three degrees of freedom are available to achieve the required matching, namely the current source width, length and overdrive voltage.

The available voltage headroom, which is determined by the output voltage swing and voltage drop over the switch transistors, places a constraint on the overdrive voltage. Ideally, the overdrive voltage would be made as large as possible to achieve the required current with minimal transistor area. However, the matching constraints require the transistor width and length to be made as large as possible to increase the gate area. Hence one has conflicting constraints and a trade-off between matching, output voltage swing and transistor area must be made.

In this particular design, the IBM 8HP technology, which is a 130 nm SiGe BiCMOS process, imposes very low voltage headroom at 1.2 V. Unlike designs in the 1990s and early 2000s, voltage headroom has become the most stringent constraint and will be prioritised over matching constraints. The output impedance is 50 Ω and for a 100 mV output full-scale voltage swing results in a total output current of:

$$i_{TOTAL} = \frac{v_{TOTAL}}{R} = \frac{100\ mV}{50\ \Omega} = 2\ mA \tag{4.8}$$

Each unit current source supplies 31.25 µA of current:

$$i_{UNIT} = \frac{i_{TOTALTotal}}{2^N} = \frac{2\ mA}{2^6} = 31.25\ \mu A \tag{4.9}$$

At this point in the design, it is useful to consider how the output of the DAC is coupled to the measuring devices. Many commercially available DACs recommended coupling the DAC output via a transformer. The benefits of transformer coupling are differential to single-ended conversion and potentially better dynamic performance. Transformer coupling is also used when the application requires the ability to set the common-mode voltage and for impedance matching. In addition the common-mode noise that contributes to even harmonics is rejected.

At this point, the choice between transformer or direct coupling only affects the output impedance of the DAC output. When transformer-coupled, the output impedance is 25 Ω and the voltage swing is halved. The design can support both direct and transformer coupling.

Because of the available voltage headroom, a MOSFET is the only practical choice for the current source transistor. As the performance and matching of the NMOS are better than those of its positive-channel metal-oxide semiconductor (PMOS) counterpart, a current sink design is selected. The current source transistor would ideally produce a constant current independent of the voltage across it, which is closely represented by a MOSFET biased in the constant-current region. The drain current for a saturated FET is expressed as:

$$i_D = u_n C_{OX} \frac{W}{L} (v_{GS} - V_{TN})^2 \tag{4.10}$$

The transistor dimensions play an important role in meeting the matching requirements. The variation in threshold voltage and current gain determines the transistor matching. The analysis of MOS matching models in [31] derives two matching models based on the current density of the transistor. For small current densities, the threshold voltage matching primarily determines the current matching represented by:

$$\frac{\Delta I_D}{I_D} = \frac{2}{V_{gs} - V_{th}} \frac{A_{Vth} t_{ox}}{\sqrt{WL}} \tag{4.11}$$

and for large current densities, the slope mismatch primarily determines the current matching represented by:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta\beta}{\beta}\frac{1}{\sqrt{WL}} \tag{4.12}$$

Overall, the small and large current density mismatch equation may be combined to form a single equation.

$$\frac{\Delta I_D}{I_D} = \left(\frac{\Delta\beta}{\beta} + \frac{2\Delta V_{th}}{V_{gs}-V_{th}}\right)\frac{1}{\sqrt{WL}} \tag{4.13}$$

A higher transistor gate area improves matching. There are two conflicting constraints on the overdrive voltage [34]. The first is that the overdrive voltage is made larger in order to minimise the transistor dimensions and thus the overall area. The second is that the overdrive voltage is limited by the amount of available voltage headroom determined by the output voltage swing, drain-to-source voltage of cascode, and collector-to-emitter voltage of the switch transistors.

Based on the design manual for the process [35], for identical devices with the same orientation separated by less than 200 µm, the mismatch in the device current at the final wafer test has been characterised. Adjacent MOSFET devices are modelled as in the by a combination of threshold voltage and mobility mismatch terms that varies in proportion to the inverse root of the area product. The mismatch terms have been statistically characterised for this process and are represented in equations (4.14), (4.15) and (4.16).

The overall current mismatch:

$$\sigma\left(\frac{\Delta I_{ds}}{I_{ds}}\right) = \sqrt{\sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \sigma^2\left(\frac{2\Delta V_{th}}{V_{gs}-V_{th}}\right)} \tag{4.14}$$

The mobility mismatch:

$$\Delta\beta = \frac{K_\beta}{\sqrt{(W - K_{\beta W})NF(L - K_{\beta L})}} \tag{4.15}$$

The threshold voltage mismatch:

$$\Delta Vth = \frac{K_V}{\sqrt{(W - K_{VTW})NF(L - K_{VTL})}} \tag{4.16}$$

To summarise, from the matching requirements, the following observations are made:

1. A higher overdrive voltage improves matching.
2. A higher gate area product improves matching.

However, there are constraints on these parameters:

1. The overdrive voltage is limited by voltage headroom.
2. The gate area is limited by the overall layout area.

There are also further factors affecting the calculation in sub-micron technology. The short-channel second-order effects complicate the design process. There is no closed form solution to this design procedure in this case and in general DAC design. In order to address modern fabrication processes, the design procedure in Figure 4.4 is proposed.

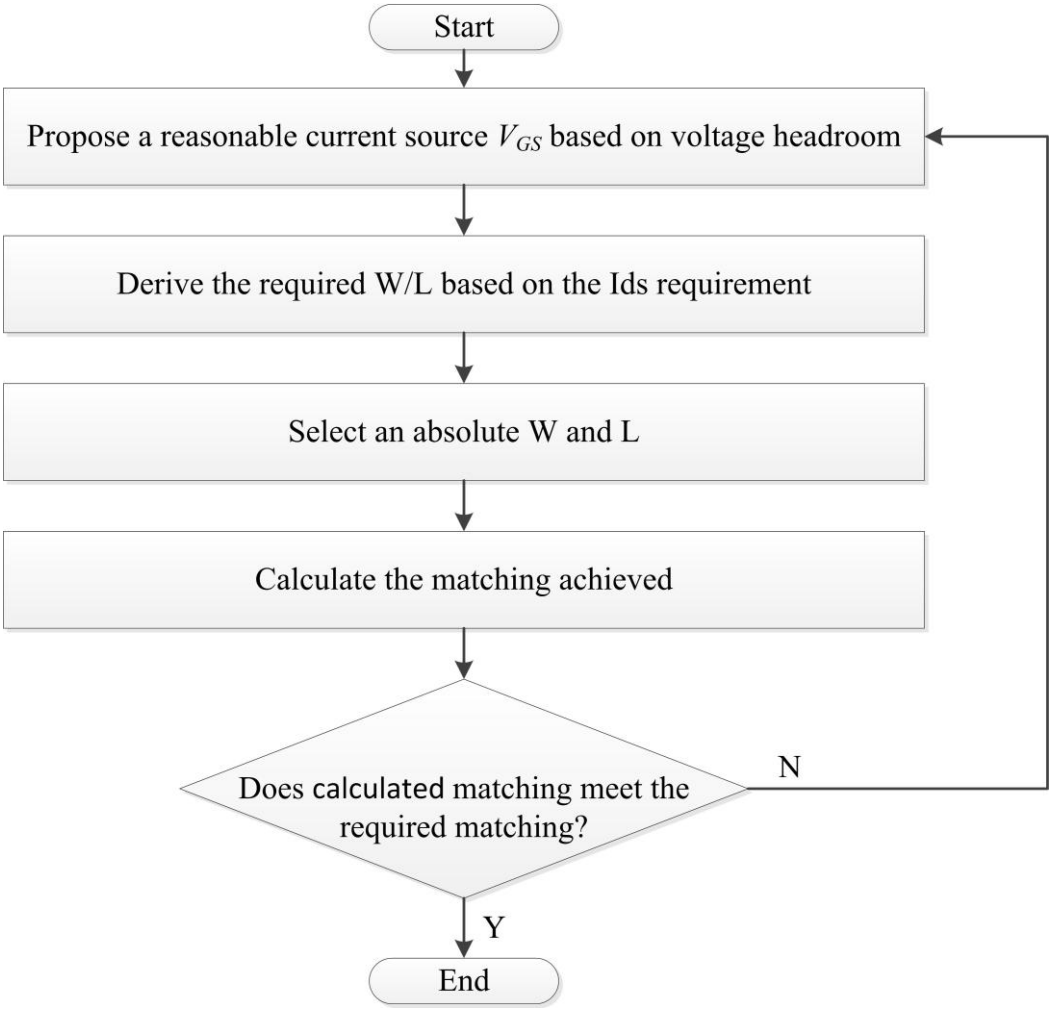


Figure 4.4: Design procedure for design of current source cell.

Various techniques and approaches have been proposed in the literature. Many of these techniques are based on older processes in which the voltage headroom is not the tightest constraint. The design procedure detailed in the Figure 4.4 begins with addressing the voltage headroom, then deriving the transistor dimensions and finally closing the loop by considering the matching constraints and iterating if required. The design procedure is elaborated further in Chapter 4.5.2 to Chapter 4.5.4.

4.5.2 Current Source Threshold Voltage

From the design manual for the IBM 8HP process [35], the threshold voltage to bias an NMOS into the constant-current region is 0.355 V. The power supply voltage, V_{DD}, in this design is 1.2 V. The output voltage swing, v_{out}, is 100 mV. This leaves a total of 1.1 V to be used by the current source, current switch transistors and possibly a cascode transistor. The $V_{GS\ CS}$ is chosen to be approximately equal to the classical threshold voltage at 350 mV, as the voltage headroom is severely limited.

In order to bias the NMOS current source into the constant-current region, usually the $V_{GS\ CS}$ should be made greater than the V_{TH}. In this design, however, the $V_{GS\ CS} \approx V_{TH}$. The reason for this stems from the second-order effect, DIBL, which modifies the classical equations for MOS transistors. The classical V_{TH} will be lowered by the DIBL effect aiding the voltage headroom requirements. For device-modelling purposes, DIBL can be accounted for by a V_{TH} reduction depending on the drain voltage.

An exact calculation of the DIBL effect cannot be made at this step as the drain voltage of the current source transistor has to be known. One may, however, make an estimate of the DIBL effect based on certain assumptions.

Firstly, assume that a cascode transistor will be added to increase the output impedance. The total voltage over the current source and cascode transistors will be the supply voltage minus the voltage across the base-emitter or gate-source junction of the switch transistor, depending on whether an HBT or NMOS is used. The IBM 8HP process was selected for the ability to use HBT transistors to switch current as detailed in Section 3.2. The base emitter voltage is 0.725 V for a HBT NPN transistor. The total voltage across the drain of the cascode transistor to ground is:

$$V_{D\ cascode} = V_{DD} - V_{BE\ Switch} = 1.2 - 0.726 = 0.474 \tag{4.17}$$

The next assumption is that the drain-to-source voltage of the current source and that of the cascode are equal, which will be realised later in this design, resulting in a $V_{DS\ CS}$ of 0.236 V. Based on these assumptions, the effect of DIBL on the current source V_{TH} may be estimated:

$$\text{DIBL} = \frac{\Delta V_{TH}}{\Delta V_{DS}}$$

Reference point, V_{TH} = 0.355 V at V_{DS} = 1.2 V [35]

Hence as V_{DS} = 0.25 V

$$0.073 = \frac{0.355 - V_{TH|VDS=0.25}}{1.2 - 0.25}$$

$$V_{TH|VDS=0.25} = 284.65\ mV \tag{4.18}$$

The various assumptions made in the DIBL effect estimation are verified or designed to be true later in the design. The DIBL effect reduces the V_{TH} by 70 mV, assisting in meeting the voltage headroom requirements marginally.

4.5.3 Transistor Aspect Ratio and Dimensions

One may now calculate the transistor dimensions to achieve the required current per unit current source.

$$I_D = kn\frac{W}{L}(V_{GS}-V_{th})^2 \tag{4.19}$$

$$\frac{W}{L} \cong 5$$

Absolute values of the current source dimensions may now be selected. The process transconductance, *kn* is approximately 1.43 mS at the operating region. In digital designs, the transistor area is minimised in order to integrate more transistors on the die. However in analogue and mixed signal design, the gate density is not the primary concern. It has already been established that a higher gate area improves matching, which is the primary reason to avoid minimum dimension transistors.

The secondary reason to avoid minimum dimension transistors is that second-order short-channel effects are more pronounced at channel lengths below 1 µm. At shorter channel lengths, the effect of channel length modulation will reduce the output impedance and therefore the SFDR. If a shorter channel length is selected, the channel length modulation effect must be accounted for. While the design approach does factor in the DIBL due to the short-channel, a design that is not highly constrained in area will still benefit from a larger channel in terms of matching and hence spectral fidelity. The selection of the transistor drawn length is chosen to be 2 µm to minimize the short-channel effects and increase the gate area for matching purposes. This leaves the drawn width at 10 µm.

4.5.4 Current Source Matching

The current matching for a unit current source may now be calculated, closing the loop of parameters for the current source transistor, using the mismatch (4.13). The overall device

mismatch is calculated to be 0.921 %, satisfying the matching requirements of static linearity. A matching analysis is detailed below to verify the matching calculations.

A corner simulation would allow the designer to verify the design functionality at the global process boundaries. In the DAC current source cell matrix, the effect of the local process mismatch primarily determines the SFDR performance. As the DAC design is primarily an analogue design, a Monte Carlo analysis is a more useful tool, as a corner simulation would only provide insight into the global process variations, but a Monte Carlo simulation allows for variance of local and global process parameters.

Monte Carlo statistical simulations provide the best approximation of the circuit performance variation over the manufacturing process window. Multiple simulations are run to vary the temperature and process parameters within the expected distribution. Statistical simulations can also explore the effects of mismatch between like devices within a chip.

In the specific case of the IBM device models, parameters are provided with statistical distributions that represent long-term process variation during manufacturing using separate distributions to describe global and mismatch variations. The global variations apply to device performance over the total manufacturing process window. Mismatch distributions, typically much smaller, generate different device parameters for each device instance in a single Monte Carlo iteration. The mismatch variations are typical variations and not worst case ones, so as not to over-constrain the design and assume good layout practices. The layout needs to ensure that device performance is not degraded. For instance, devices for which matching is critical should be placed in close proximity on the chip.

As a fundamental process parameter is varied, it will influence all devices that physically depend on that parameter. The simulations are created such that independent distributions are used for physical parameters, assuring proper correlations between various devices are preserved through the use of those parameters in the model equations. A script to perform the Monte Carlo simulation is attached in Appendix D and an example of the current distribution is shown in Figure. 4.5.

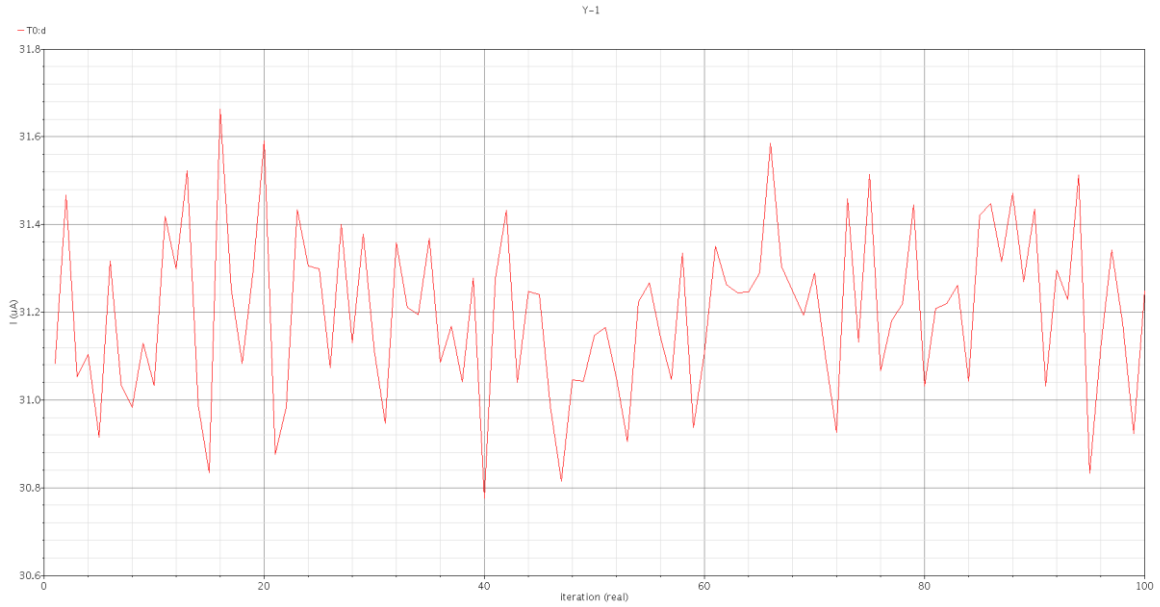


Figure 4.5: Monte Carlo simulation output current.

The current distribution from simulation run to run is shown in Figure 4.5. The Monte Carlo analysis predicts a device mismatch variance of 0.6 %, which is better than the calculated mismatch. The design procedure that was introduced provides a systematic methodology to address current source matching in modern fabrication processes.

4.6 CASCODE TRANSISTOR DESIGN

An ideal current source has infinite output impedance. This is derived from the requirement of an ideal current source to maintain a constant current independent of the voltage across it. In practice, all physically realisable current sources at present have a finite internal resistance. Most modern high-speed DACs are designed for a 50 Ω load. This deterministic load and required SFDR will determine whether the current source output impedance is adequate.

Finite output impedance of DAC current sources leads to distortion. Depending on the digital input code, more or fewer current sources are connected to the left and right output nodes. Along with that, more or fewer output impedances are connected in parallel with the load impedance. This means that the total effective load impedance becomes signal-dependent. Since the output voltage is a simple multiplication of the current and the output impedance, signal-dependent load impedance leads to distortion. This produces third-order harmonic distortion [8].

Equation (4.20) is used to predict the effect of the finite output impedance of the SFDR [7], [19] and [32].

$$SFDR = 20log\left(\frac{R_{OUT}}{R_L}\right) - 6.02(N-2) \tag{4.20}$$

R_{OUT} is the total output resistance of the current source cell, while R_L is the load resistance. The single transistor current source has an output resistance of 44 kΩ. Without any additional transistors in the current source design, the SFDR is limited to 34 dB. An alternate estimation of SFDR is presented in [12] and [36]. Q represents the estimated SFDR, and N is the number of current sources. The result also shows the SFDR is limited to 34 dB with the current output impedance.

$$Zreq = \frac{NR_L}{4Q} \tag{4.21}$$

Both methods for SFDR estimation are in agreement. In order to obtain an SFDR of 50 dB, for example, the required output impedance would be greater than 253 kΩ. The output impedance also affects the static linearity of the DAC; this is shown in [16] and [32] according to:

$$INL = \frac{I_{unit}\,R_L{}^2N^2}{4R_{Imp}} \tag{4.22}$$

However, the dynamic requirements are more stringent, hence the static case is not pursued further. As stated above, an ideal current source should produce a constant current independent of the voltage across it. In the current source transistor, this is a constant current independent of V_{DS}. The current through the current source transistor changes for varying V_{DS} in response to channel length modulation. The slope of the I_D-$V_{DS,}$ which is equivalent to the output impedance, is not completely flat but rather 44 kΩ, which negatively affects the DAC linearity and hence SFDR as expected.

In order to increase the output impedance, a cascode current source is used. The drawback of this approach is that more of the voltage headroom is required in a voltage-constrained design. With the addition of an active load, the output impedance is increased. The cascode transistor may either be a common-source NMOS or common-base HBT. Both have a

multiplier effect on the output impedance of the current source. The common-gate NMOS Cascode configuration is shown in Figure 4.6.

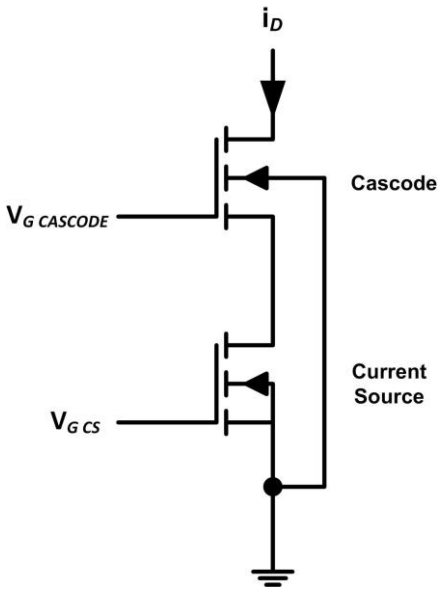


Figure 4.6: Cascode configuration.

The cascode transistors shown in Figure 4.6 should be biased in the constant-current region [12]. The total allowable voltage for the cascode and current source transistors is 0.5 V. This is due to the current switch transistors, which consume half of the available voltage headroom. This leaves a remainder of 0.25 V for the cascode transistor.

An HBT exhibits higher transconductance in comparison to an NMOS, which results in a higher achievable output impedance. If the HBT is selected, the HBT base voltage of the cascode transistor would be approximately 0.95 V. In order to keep this transistor in the saturation region, an HBT collector voltage of at least 0.95 V is required, which cannot be handled within the available voltage headroom.

An NMOS would, however, be able to operate within the constant-current region with a gate overdrive voltage of greater than 0.25 V. The gate voltage would need to be greater than 0.5 V in order to keep the cascode NMOS in the constant-current region. Selecting a $V_{GS\ CASCODE}$ of 0.35 V; similar to the current source transistor, results in a gate voltage, $V_{G\ CASCODE}$ of 0.6 V. The analytically predicted SFDR with the inclusion of the cascode transistor is 56.5 dB because of the increase in output impedance to 560 kΩ.

This answers one of the major research questions on how to address finite output impedance. The general observation that stems from the above analysis is that in modern fabrication processes, the tendency to lower supply voltages places a severe limitation on the use of BiCMOS HBTs to be used as a cascode transistor due to its higher transconductance. One of main areas in the DAC design that could benefit from BiCMOS over traditional CMOS does not benefit at all because of the voltage headroom.

4.7 CURRENT SWITCH DESIGN

Most modern high-speed DACs with resolutions of fewer than eight bits operate on the principle of current-steering [37]. Based on the input word, current is steered to either the positive or negative output. This allows the DAC to be used either as a single-ended or differential-ended voltage or current-based driver. The current-steering as opposed to switching of current improves performance.

The input of the current switches is effectively the point where the analogue and digital portions of the DAC interface. The switching core and the switches are separated from the current sources to avoid coupling between the digital signals and the analogue signals. The current switches are designed with HBTs owing to the switching speed. The device biasing needs to ensure that the transistors always operate within the forward active region to avoid distortion. The current source cell is shown in Figure 4.7.

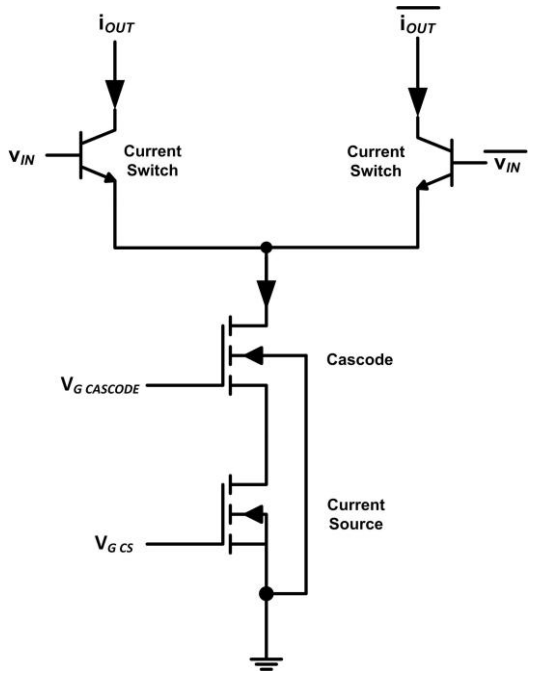


Figure 4.7: Current source cell.

If the input voltage in the current source cell in Figure 4.7, v_{IN} is selected to equal V_{DD}, the emitter voltage of the switching transistors is 450 mV. The emitter voltage of the switch transistors is v_{BE} below the switch-on voltage, i.e. the voltage at the base required to turn the transistor on.

$$v_{E\ SWITCH} = v_{IN} - v_{BE\ SWITCH} = 1.2\ V - 0.726\ V = 450\ mV \tag{4.23}$$

The worst case conditions within which the device needs to operate in the forward active region occur when all the current sources are simultaneously on or off. In this case, the collector voltage of the switch transistor may fall to 1.1 V.

$$v_C = V_{DD} - i_{OUT}\, R_{Out} = 1.2\ V - 2\ mA\ x\ 50\ \Omega = 1.1\ V \tag{4.24}$$

The current switch transistors will operate within the forward active region even in the worst case condition, as the saturation voltage is 0.2 V.

$$v_{CE\ SAT} \cong 0.2\ V \tag{4.25}$$

The performance of the HBT-based current switch design is compared to a typical NMOS-based current switch. Two functionally equivalent circuits were created, as shown in Figure 4.8.

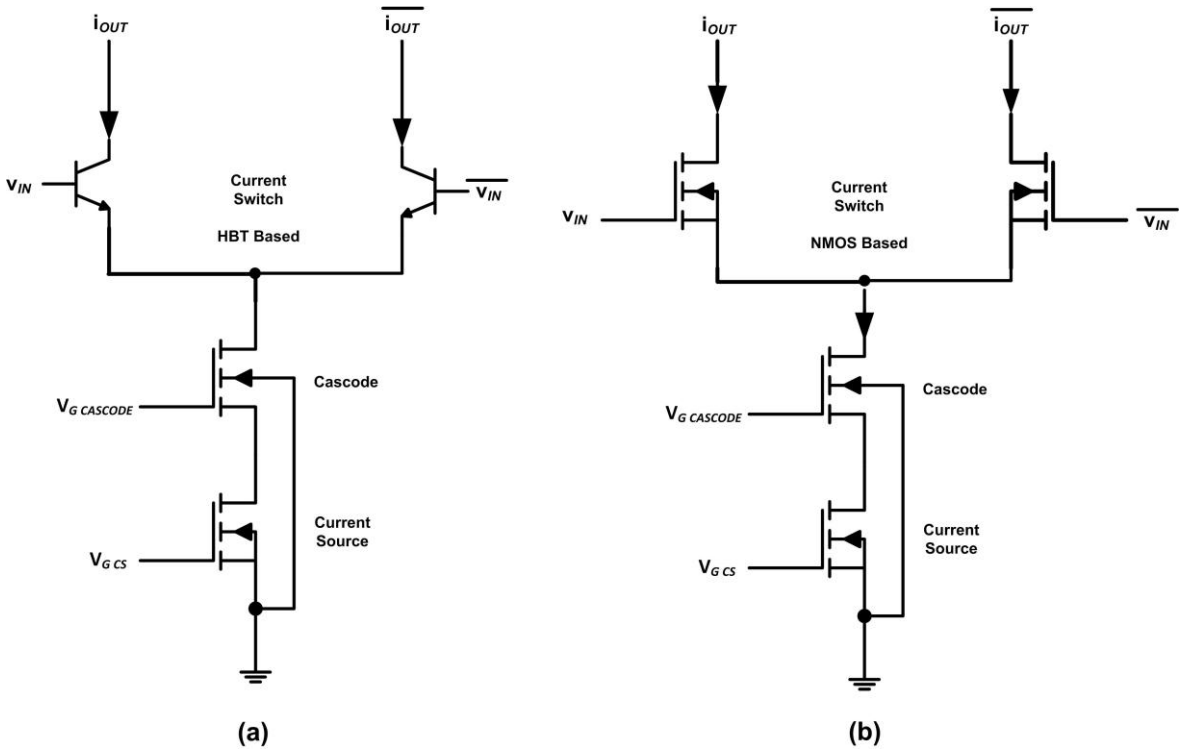


Figure 4.8: (a) HBT-based current switch and **(b)** CMOS NMOS-based current switch.

The first is the BiCMOS current switch in Figure 4.8 (a), as used in this design. The second is an equivalent CMOS version using NMOS as the current switch transistors in place of the HBT switches shown in Figure 4.8 (b).

A transient simulation is run with a square wave stimulus on the HBT and NMOS-based current switch circuit configurations. The voltage output of the HBT-based current switch and NMOS-based current switch is shown in Figure 4.9, illustrating the clock feedthrough effect.

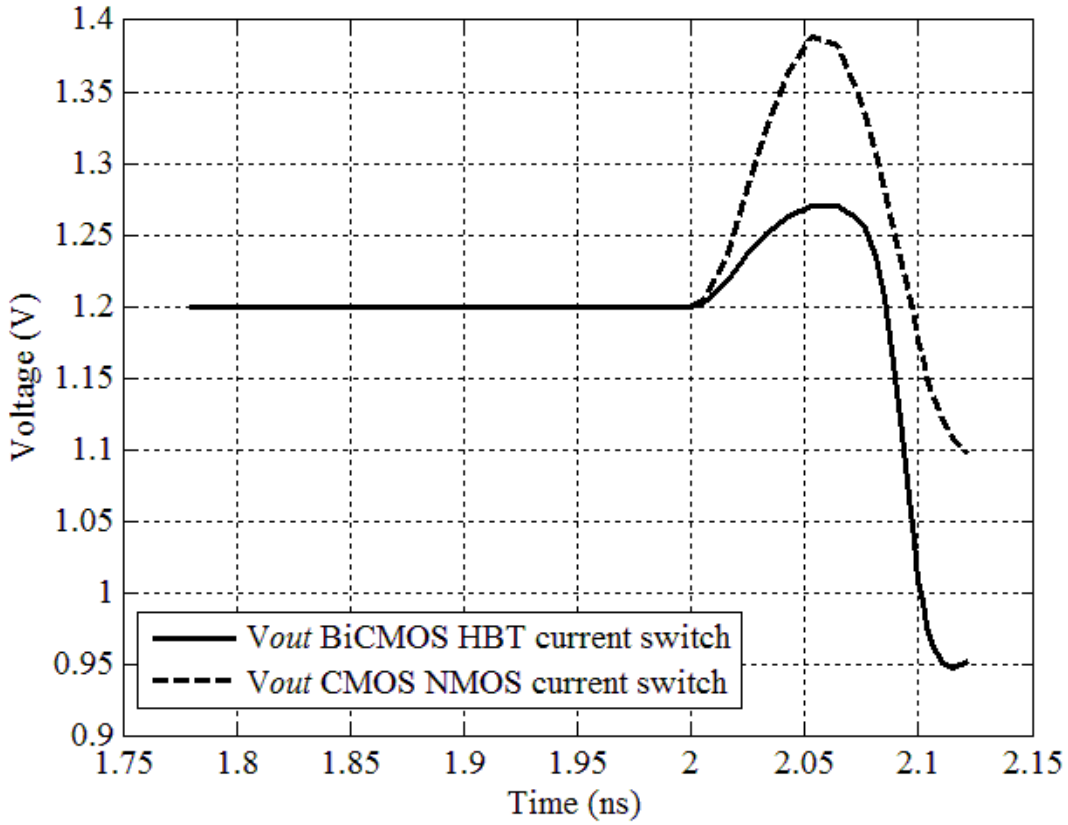


Figure 4.9: Transient response of BiCMOS HBT-based current switch (solid) and CMOS NMOS-based current switch (dash).

In order to quantify this effect, the area between the actual voltage and ideal voltage curves in Figure 4.9 may be used. Table 4.2 summarises the total clock feedthrough distortion simulation results.

Table 4.2: Clock feedthrough distortion measurements.

Current switch implementation	**Clock feedthrough distortion**
BiCMOS using HBT current switch	~ 3.75 pV-s
CMOS-only using NMOS current switch	~ 8.65 pV-s

From Table 4.2, the HBT-based current switch transient response is closer to the ideal response in comparison to the NMOS current switch as the total clock feedthrough distortion is over 65% lower. Another important aspect of the current switch design is the voltage variation at the drain of the current source transistors, which is also the variation at the emitter or source of the HBT or NMOS respectively. This is shown in Figure 4.10.

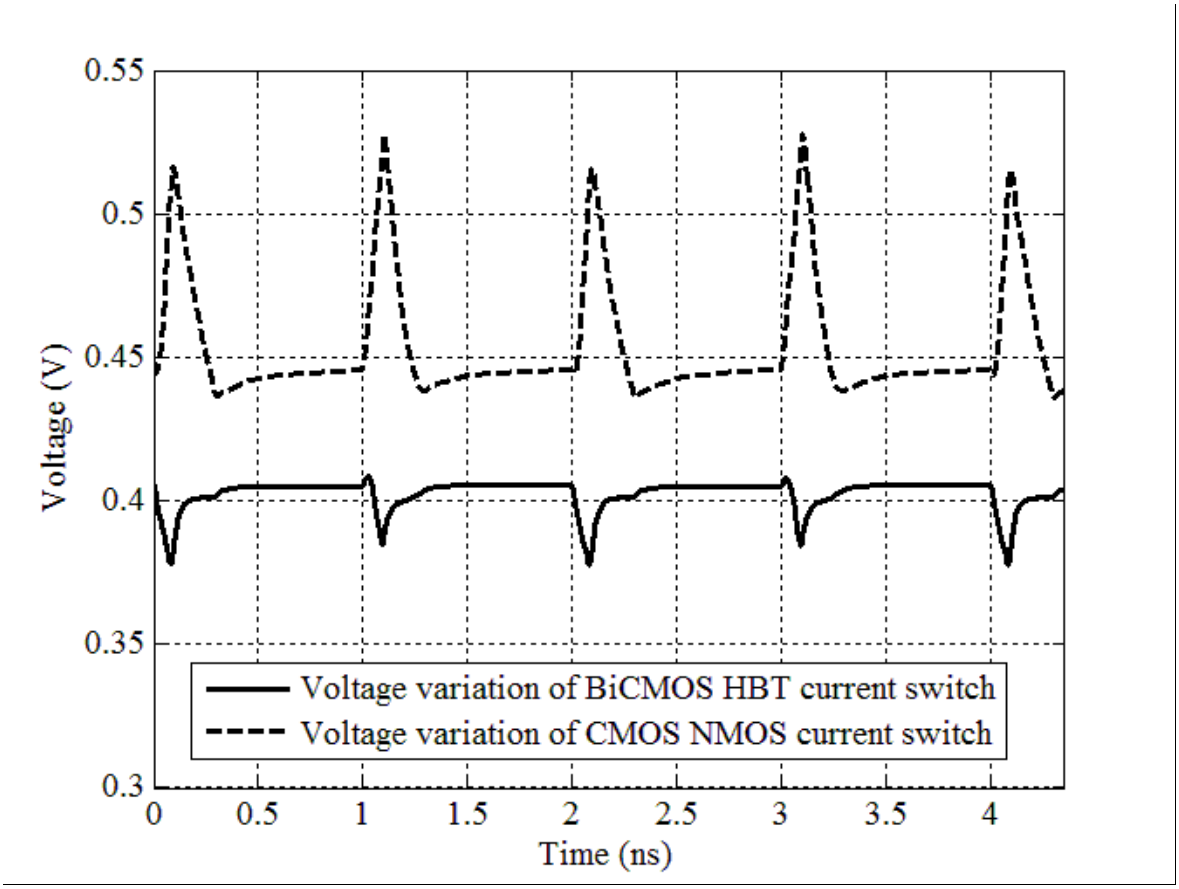


Figure 4.10: Voltage variation of the drain of the current source transistors in BiCMOS HBT-based current switch (solid) and CMOS NMOS current switch (dash) illustrating clock feedthrough distortion.

Distortion is improved in the BiCMOS current cell as the v_{BE} is more constant than v_{GS} in CMOS-only implementations. This implies less voltage variation at the drain of the current source transistors, resulting in improved distortion.

Clock feedthrough distortion is improved in the BiCMOS HBT-based current cell when there is less voltage variation at the drain of the current source transistors, as shown in Figure 4.10. The BiCMOS HBT-based current source cell improves performance in comparison to a CMOS-only current source cell, as the clock feedthrough distortion is improved for a BiCMOS HBT-based implementation.

This answers one of the fundamental research questions of this work, namely that the performance of a BiCMOS current source cell improves performance in comparison to a CMOS-only current source cell. Clock feedthrough effects and distortion are lowered in a BiCMOS implementation.

4.8 SWITCH DRIVER

The signals that drive the current switches are crucial to the dynamic linearity of the DAC. The outputs of the LVDS receiver are not suitable to drive the current switches directly owing to mismatch in components and differences between logic paths, which result in distortion and glitches. Timing glitches and coupling of the clock signals through the current switches create dynamic non-linearity and degrade the DAC SFDR. Consequently, identical and synchronised signals are required to drive the switches.

The switch driver circuit functions are to synchronise the control signals of the current switches to the clock and control the voltage swing of the control signals to minimise the clock feedthrough effect. A switch driver was designed to transfer the full-scale control signals from the LVDS receiver and derive signals that swing in a limited range to drive the current switches. The switch driver comprises a latch and an SRD shown in Figure 4.11.

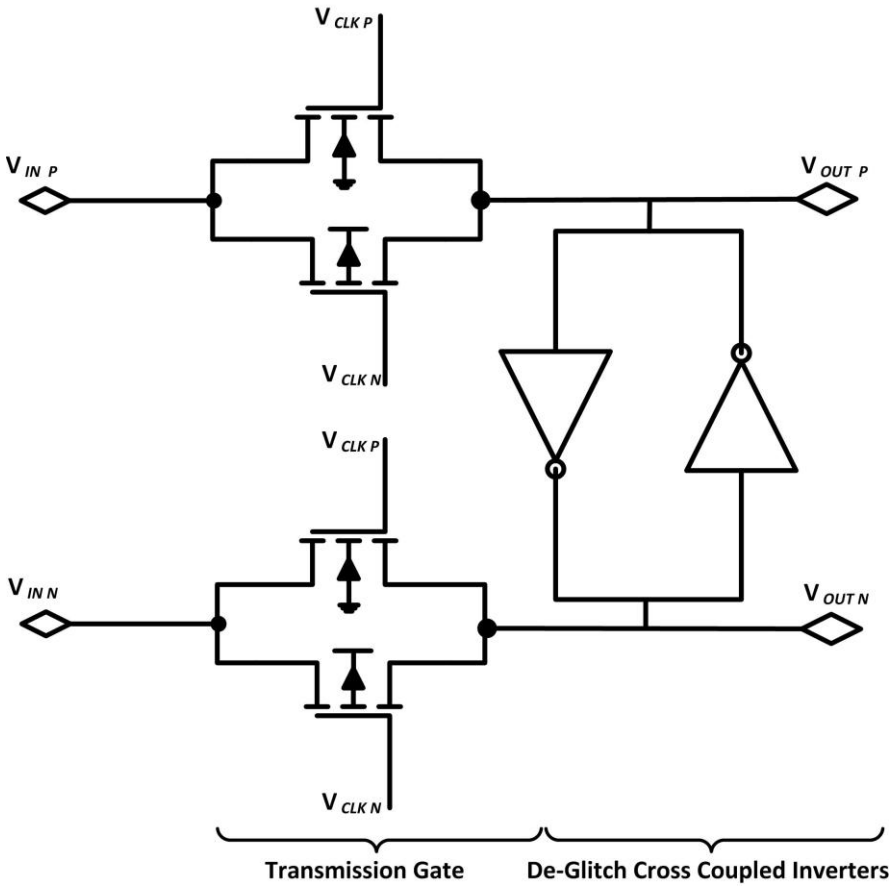


Figure 4.11: CMOS latch circuit.

Two design approaches are used for the CMOS latch design in the literature. Traditionally, current mode logic drivers are often used to obtain maximum possible clock speed. Regular CMOS logic has been used to obtain the steepest transitions and shortest clock-to-Q delay [12]. The basic concept of the latch circuit is shown in Figure 4.11, which consists of a transmission gate followed by de-glitch cross-coupled inverters.

The de-glitch cross-coupled inverters form a bistable storage cell. The transmission gate controls access to the cross-coupled inverters based on the inputs and clock signal. The CMOS latch design is based on [12], as it creates the steepest transition and shortest delay in comparison to common-mode logic latches and uses fewer transistors.

The latch minimises timing skew by synchronising the differential control signals with the clock signal. The de-glitch circuit aligns the crossing point of the input differential signal to suppress glitches. Inherently, this circuit has a low crossing of the $V_{OUT\ P}$ and $V_{OUT\ N}$ signals.

As in all dynamic latches, the data are stored on the gate capacitance of the inverter and the charge is switched in or out with the transmission gate. The complementary transmission gate ensures that the storage gate is always strongly driven. The operation of the latch is very simple: when $V_{CLK\ P}$ is low, the transmission gate is off and the output is determined by the storage node, when $V_{CLK\ P}$ is high the transmission gate is on and inverter output follows the input. Thus, the latch is transparent when the transmission gate is closed.

The SRD design is based on [18] and drives the current switches with decreased voltage swing signals to reduce the clock feedthrough effect. The SRD design maintains the voltage swing in the desired range without seriously compromising the area. The SRD design is shown in Figure 4.12.

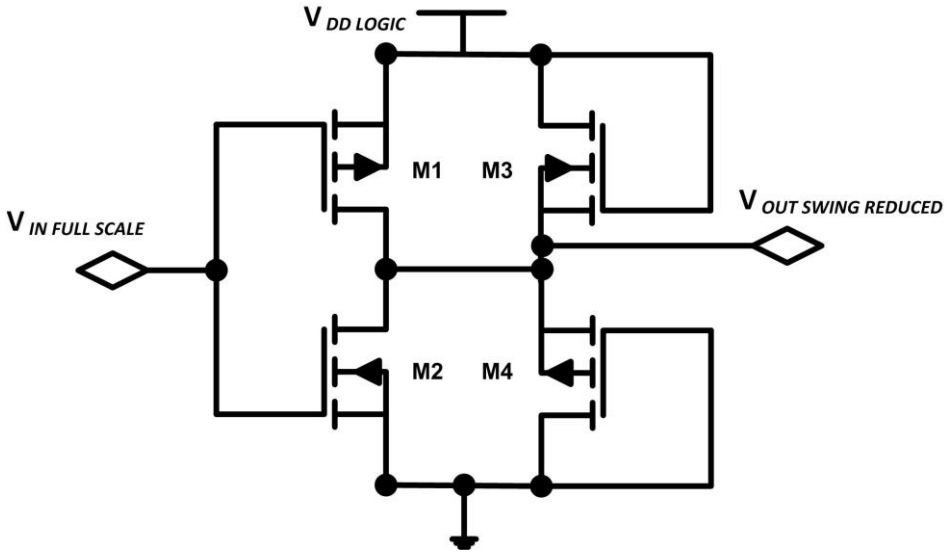


Figure 4.12: Swing reduced Driver Circuit.

Generally and in this design shown in Figure 4.12, the input signal to the SRD is varying from the ground to the supply voltage level. If these signals are used directly, switching speed is limited, power dissipation is increased and clock feedthrough distortion is increased. The input voltage is applied to the inverter pair M1 and M2 and an inverted swing-reduced output is maintained by M3 NMOS and M4 PMOS diode-connected transistors.

When the input represents a logic level high, the transistors M2 and M3 are on, while M1 and M4 remain off. When the input represents a logic level low, the transistors M2 and M3 are off while M1 and M4 remain on. By weighting the transistors M3 and M4 appropriately, the output level swing can be controlled. For this design, the procedure in [18] is followed to obtain output signals that swing from 0.55 V to 1.1 V to minimise the clock feedthrough effect. The complete switch driver circuit is shown in Figure 4.13.

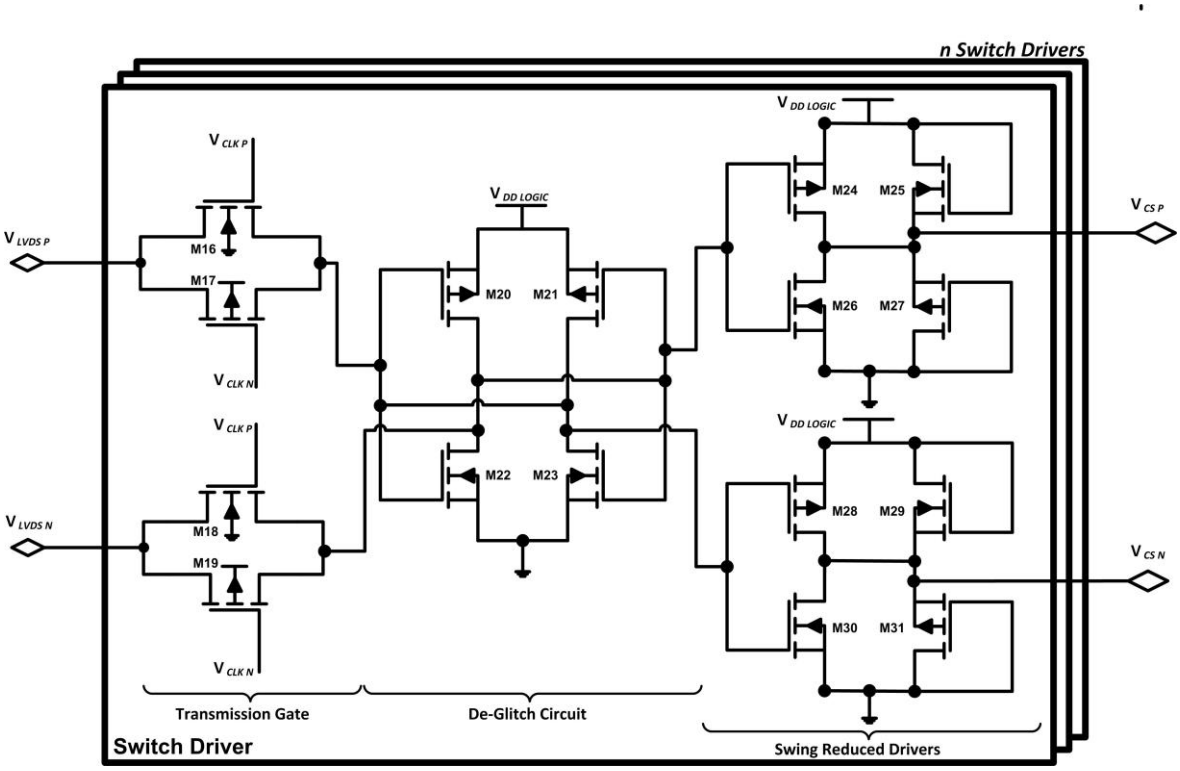


Figure 4.13: Complete Switch Driver Circuit.

In Figure 4.13, the complete switch driver circuit combines the CMOS latch and SRD circuits and transfers full-scale unsynchronised control signals from the LVDS receiver to swing-reduced synchronised control signals to control the switching of the current source cells.

4.9 INPUT LVDS RECEIVER

To enable the DAC to operate at high sampling rates, an LVDS input stage was designed. Generally LVDS pads with the full receiver circuit are available on most digital fabrication technologies. This type of technology is commercially available via third party suppliers but was not available for scholarly work. The fabrication of the IC was sponsored by the MOSIS Educational Programme in which LVDS pads does not form a part of the standard libraries for the fabrication process.

Communication on the external digital signals is done through differential signalling, which is less susceptible to noise. Two balanced signals are transmitted on the lines in opposite directions. The electromagnetic fields are radiated in opposite directions, resulting in common-mode rejection. The LVDS receiver design is based upon [7], [38] and [39]; it

consists of a differential amplifier followed by a level shifter and inverter buffer, shown in Figure 4.14.

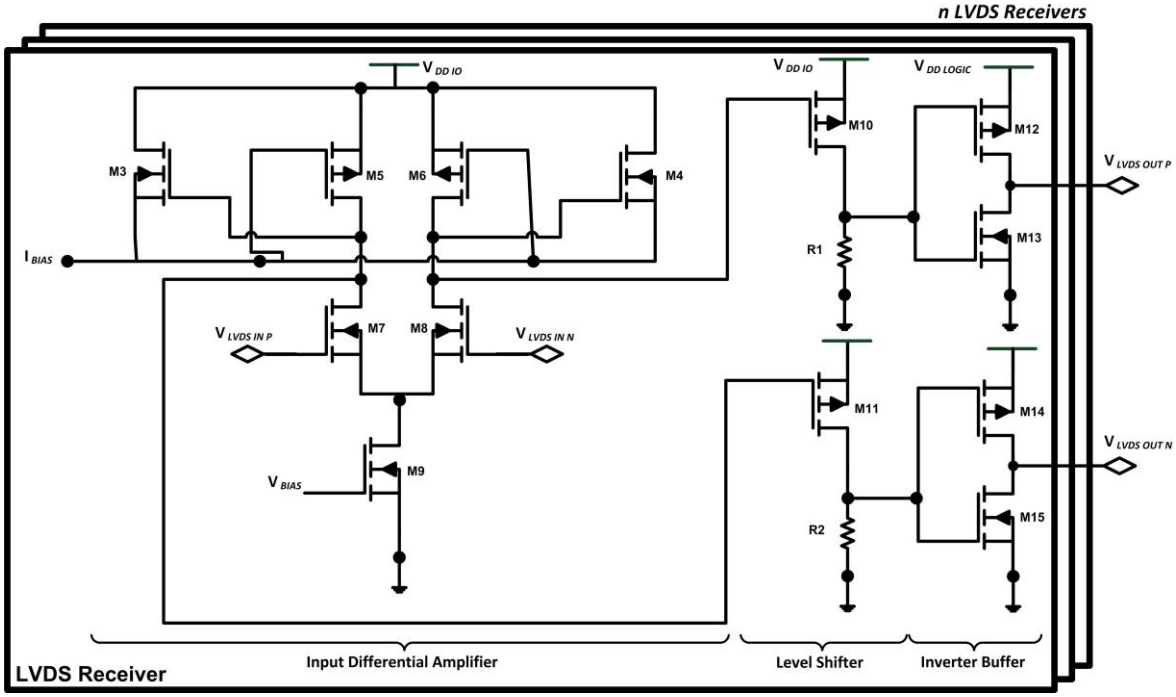


Figure 4.14: Complete LVDS Receiver Circuit.

In Figure 4.14, the LVDS circuit transfers the signals from the I/O signal voltage to the internal digital logic voltage. Transistors M3 – M8 form a Schmitt trigger that detects the input differential voltage with a hysteresis of around 25 mV to 50 mV. The outputs of the Schmitt trigger are converted to full-scale voltage swings with a level shifter and inverter buffer.

On-chip termination of the LVDS signals was used to reduce reflections on the high-speed inputs. Each LVDS differential pair requires a termination resistor in order to generate the differential output voltage and create a current loop of 2.5 mA to 4.5 mA. As the LVDS operates at sub-nanosecond range, proper termination prevents reflections and improves signal integrity.

The LVDS signals have a voltage swing range from 250 mV to 450 mV, with 350 mV being typical with the common-mode centre voltage of 1.2 V. As the voltage swing is very low, it requires less time to rise and fall, which achieves a higher operating frequency. Low power consumption and low current also result from the low voltage swing.

4.10 COMPLETE DIGITAL-TO-ANALOGUE CONVERTER

The full six-bit DAC is constructed using the current source cell, switch driver, LVDS receiver and bias circuits. Each circuit is built as a cell and reused across the design. The design uses 64 current source cells, one for each quantisation level. These current sources are arranged as a matrix to facilitate the layout.

Circuits to generate bias voltages and currents for the current source cells and LVDS receiver are designed. The bias circuit for the current source cell generates the bias voltage reference for the current source and cascode transistors. These circuits are shown in Figure 4.15.

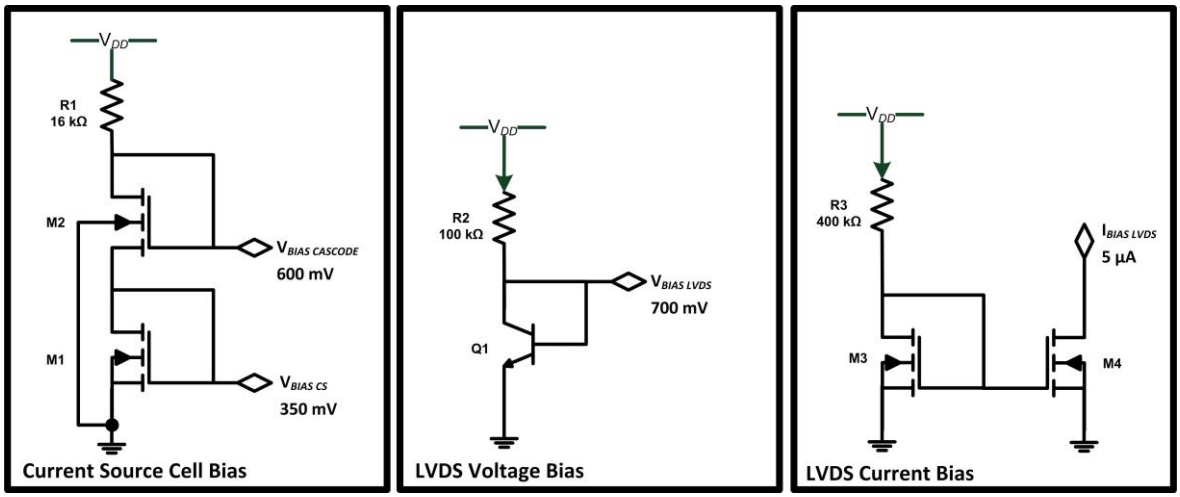
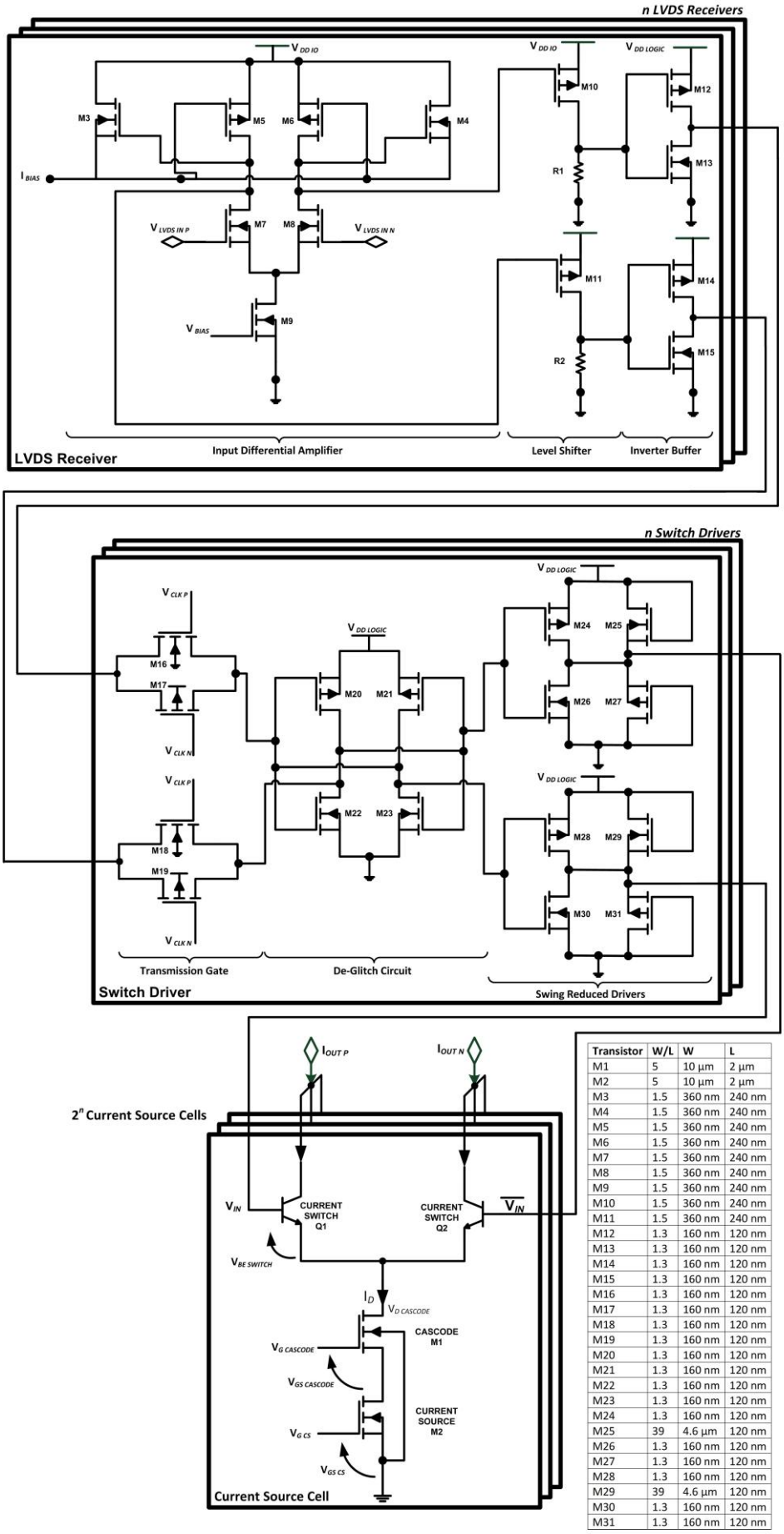


Figure 4.15: DAC bias circuits.

In Figure 4.15, the voltage references are generated with diode-connected NMOS transistors. The LVDS receiver bias circuit generates the bias current for the Schmitt trigger using a current mirror structure and a bias voltage reference for the tail transistor of the Schmitt trigger using a diode-connected NMOS.

The full DAC design is shown in Figure 4.16. The transistors' sizes are annotated on this diagram together with the multiple reuse of cells.



Transistor	W/L	W	L
M1	5	10 µm	2 µm
M2	5	10 µm	2 µm
M3	1.5	360 nm	240 nm
M4	1.5	360 nm	240 nm
M5	1.5	360 nm	240 nm
M6	1.5	360 nm	240 nm
M7	1.5	360 nm	240 nm
M8	1.5	360 nm	240 nm
M9	1.5	360 nm	240 nm
M10	1.5	360 nm	240 nm
M11	1.5	360 nm	240 nm
M12	1.3	160 nm	120 nm
M13	1.3	160 nm	120 nm
M14	1.3	160 nm	120 nm
M15	1.3	160 nm	120 nm
M16	1.3	160 nm	120 nm
M17	1.3	160 nm	120 nm
M18	1.3	160 nm	120 nm
M19	1.3	160 nm	120 nm
M20	1.3	160 nm	120 nm
M21	1.3	160 nm	120 nm
M22	1.3	160 nm	120 nm
M23	1.3	160 nm	120 nm
M24	1.3	160 nm	120 nm
M25	39	4.6 µm	120 nm
M26	1.3	160 nm	120 nm
M27	1.3	160 nm	120 nm
M28	1.3	160 nm	120 nm
M29	39	4.6 µm	120 nm
M30	1.3	160 nm	120 nm
M31	1.3	160 nm	120 nm

Figure 4.16: Complete DAC.

In Figure 4.16, each bit of the DAC requires an LVDS receiver and switch driver cell. The control signals propagate through these cells from the external LVDS signals through to full-scale control signals and then reduced-swing control signals. The digital control signals control a number of current source cells depending on which bit is represented.

4.11 CONCLUSION

The mathematical and system design of the DAC was presented in this chapter from a theoretical and practical perspective. All of the DAC primary and secondary functions were presented and a design methodology for high-speed binary weighted DACs in modern fabrication processes was presented.

General architecture considerations were first explored, followed by linearity matching requirements. The design of the current source cell, switch driver and LVDS receivers was covered in depth. Lastly, the complete DAC circuit design was presented.

The hypothesis of this work was discussed in detail and it was shown from a theoretical perspective that a BiCMOS DAC achieves a lower distortion and reduction of the clock feedthrough effect, thus enhancing the SFDR. Insight into a number of research questions was gained, including the best architecture and weighting of the current source cells and the optimal design approach for BiCMOS high-speed DACs fabricated using modern processes.

CHAPTER 5: LAYOUT AND FABRICATION

5.1 INTRODUCTION

The layout of the DAC to experimentally verify a BiCMOS DAC that achieves a lower distortion and reduction of the clock feedthrough effect leading to improved SFDR is detailed. A full custom layout methodology is followed as used in traditional analogue application-specific integrated circuit (ASIC) design flow. The DAC layout may also be approached from an ASIC digital design flow perspective using automated layout methodologies in which synthesis, routing and placing of transistors may be done from hardware design descriptions. While the non-recurring engineering cost is lower with a digital design flow, the DAC performance is generally worse. A custom IC layout is used most often in DAC design industry, literature and this work.

Many of the sub-circuits in the DAC design are used multiple times. This is especially useful for the current source cell matrix that consists of many recurring current source cells and is handled by the Virtuoso tools described in Chapter 3.4. The layout of each sub-circuit is detailed, including the layout of the current source cell, current source cell matrix, switch driver, LVDS receiver and bias circuits. These cells are combined to form the top-level layout. Various layout-specific considerations are detailed, including the packaging, bonding and fill requirements.

The layout of an integrated circuit cannot purely be approached from a top-down or bottom-up methodology. Various considerations at the highest level of the hierarchy influence layout decisions at the lowest level, making the optimal design methodology iterative. Power, clock and data routing, together with space and orientation aspects, must be considered during the layout of each sub-circuit. The layout of each circuit is presented in a bottom-up methodology and considerations from higher levels of the hierarchy are also detailed.

5.2 PROCESS CONSIDERATIONS

The layout of the DAC is first considered from a top-down methodology and layout considerations of the fabrication technology are detailed. Routing layers, device and

transistor orientations, interconnects and I/O pads must be decided upon before the layout is drawn.

Ideally ground and power pads should be distributed liberally to ensure minimal ground bounce, lower inductive noise coupling and better heat dissipation. As highlighted in section 4.2, I/O pads were limited by the perimeter available in an MPW design. For this design, 21 I/O pads were fitted on the DAC portion of the total IC in order to satisfy all the bonding wire design rules. Of this total, 12 pads were used for input data, two pads for the input clock and two pads for the output signal. This left five pads for the power signals, of which two pads were used for ground, two pads for 1.2 V power and one pad for 2.5 V power.

The IBM 8HP process provides a maximum of seven levels of global metal routing, which includes four layers of thin copper, one thick copper layer and two layers of aluminium. For ease of routing, each power net is assigned its own layer. Ground is assigned metal 3 and 1.2 V power is assigned metal 4. By assigning the power and ground signals on layers and using a grid to distribute these signals, the return current path was minimised. Each layer has associated design rules constraining width, fill and dimension requirements. The metal 1 and metal layers are dedicated for internal cell routing on a sub-circuit level. The thick metal layer is used to route interconnections between cells/sub-circuits for clock and data signals in this design. The two highest aluminium layers are used for I/O pad interconnections and routing of interconnections between cells/sub-circuits in areas of dense routing.

5.3 CURRENT SOURCE CELL

The current source cell is the critical sub-circuit in the overall DAC layout. The current source cell forms a building block of the current source cell matrix. The layout of the current source cell is designed to facilitate easy use in matrix structures, which has an impact on the routing of power, ground, and data nets.

Nets that are common to current source cells, such as power, switch inputs and current outputs, are routed vertically or horizontally fully across the layout from edge to edge. This method allows the layout of a single cell to be re-used efficiently to form a matrix with minimal effort by placing multiple cells adjacent to each other. The layout is designed such

that cells belonging to the same bit of the DAC are stacked horizontally while cells belonging to different bits are stacked vertically.

To achieve this stacking, all power and input nets are routed horizontally. The output nets, namely the positive and negative current outputs, are routed vertically. An annotated layout of the current source cell is shown in Figure 5.1.

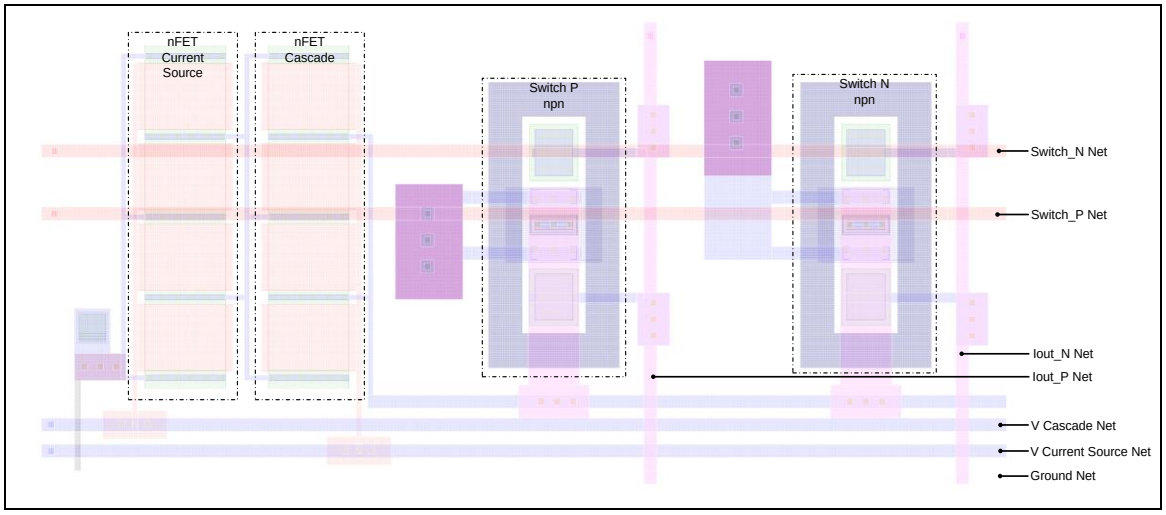


Figure 5.1: Annotated layout of current source cell, 30 µm by 14 µm.

The switch, current source and cascade transistors are outlined in Figure 5.1. All subsequent layouts in this chapter will outline the transistors in a similar manner. All HBT's are realised in the CBEBC configuration. The NMOS current source and cascade transistors are realised as folded four-finger transistors to achieve lower terminal capacitances, faster speed and a more compact area at the expense of greater circuit variations.

All HBTs and FETs in the design make similar configuration trade-offs in the layout but are not detailed explicitly. In general, all FETs are realised in the folded configuration and all bipolar transistors are realised in the CBEBC configuration unless otherwise stated.

The drawn layout dimensions of the current source cell are 30 µm by 14 µm. This layout is compact and could fit over 2000 current source cells into an area of 1 mm^2.

5.4 SWITCH DRIVER

The layout of the switch driver uses largely the same methodology as the rest of the sub-circuits, with the exception of the layout of the transmission gate. The layout of the switch driver is shown in Figure 5.2.

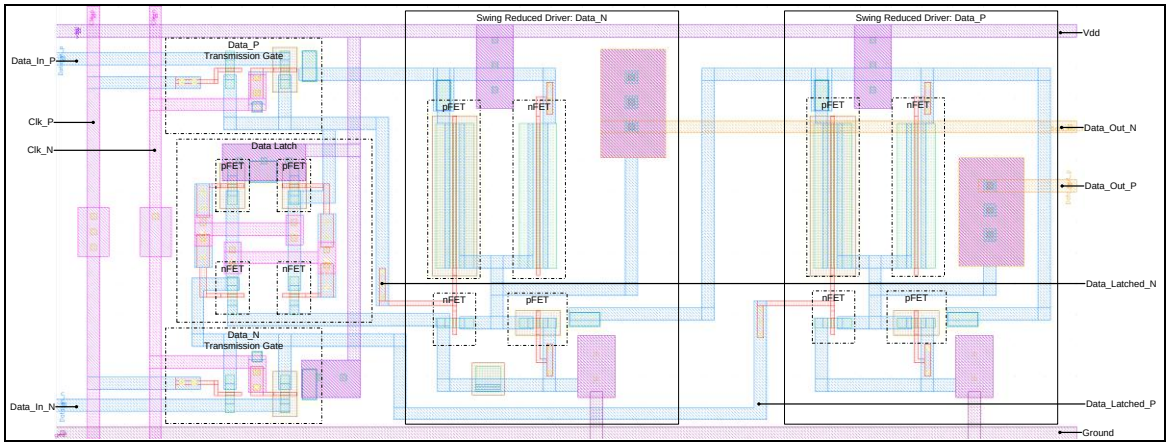


Figure 5.2: Annotated layout of switch driver, 33 µm by 14 µm.

In Figure 5.2, most of the transistor logic in the design consists of NMOS and PMOS devices with sources tied to ground or power respectively. The transmission gate is unique in that the source and drain are tied to data inputs and outputs while the gates are tied to clocks. The NMOS and PMOS share common data input and output. This leads to the switch driver requiring dense routing.

In order to design an efficient overall DAC layout, it is desirable to match the height of the switch driver to the current source cell. This places a requirement to design a switch driver with a height of 14 µm.

The height restriction combined with unique requirement of the transmission gates requires six metal layers to route. The overall dimensions of the switch driver are a 33 µm by 14 µm. This is approximately the same area as the current source cell but uses 16 as opposed to four transistors and is achieved by placing the transistors very densely and routing.

5.5 LVDS RECEIVER

The LVDS receiver is essentially the I/O pad for the data and clock inputs of the DAC. In order to comply with the LVDS specification, 2.5 V-tolerant transistors are required. Thick

oxide FETs natively handle 2.5 V consistent with the LVDS specification. The layout of the LVDS receiver is shown in Figure 5.3.

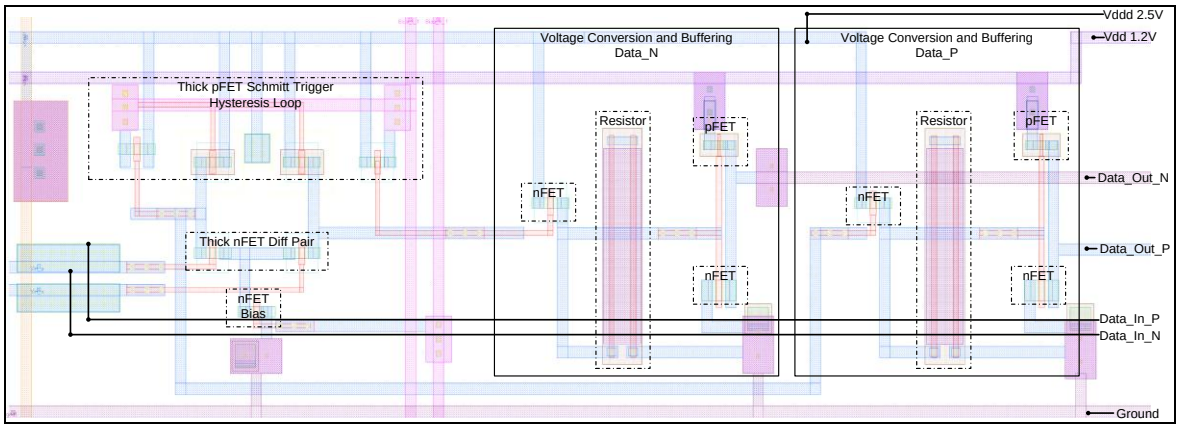


Figure 5.3: Annotated layout of LVDS receiver cell, 55.4 µm by 14 µm.

As mentioned in the design of the LVDS receiver, native LVDS pads were not available in the I/O pad library for this process. Third-party LVDS pads and layouts were available but were not used because of cost factors. The essential elements of an LVDS receiver consisting of differential buffering, triggering and voltage conversion were catered for in this LVDS implementation shown in Figure 5.3.

It is desirable to match the height of the current source cell to the switch driver and current source cell. This allows the circuits to be interconnected by merely placing the layouts adjacent to each other, promoting a compact layout. The drawn layout dimensions of the LVDS receiver are a 55.4 µm by 14 µm.

5.6 BIAS CIRCUITS

The bias circuits for the current source cells and LVDS receiver are the only layouts that use passive devices; resistors in this case. The layouts of the bias circuits are shown in Figure. 5.4 and Figure. 5.5.

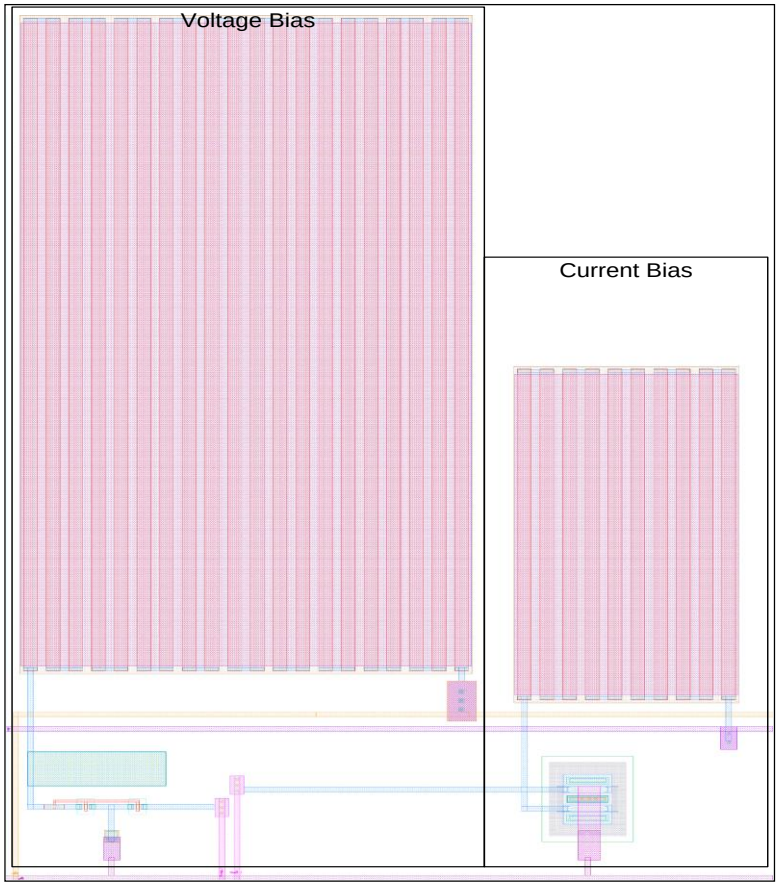


Figure 5.4: Annotated layout of LVDS receiver bias, 55 µm by 76 µm.

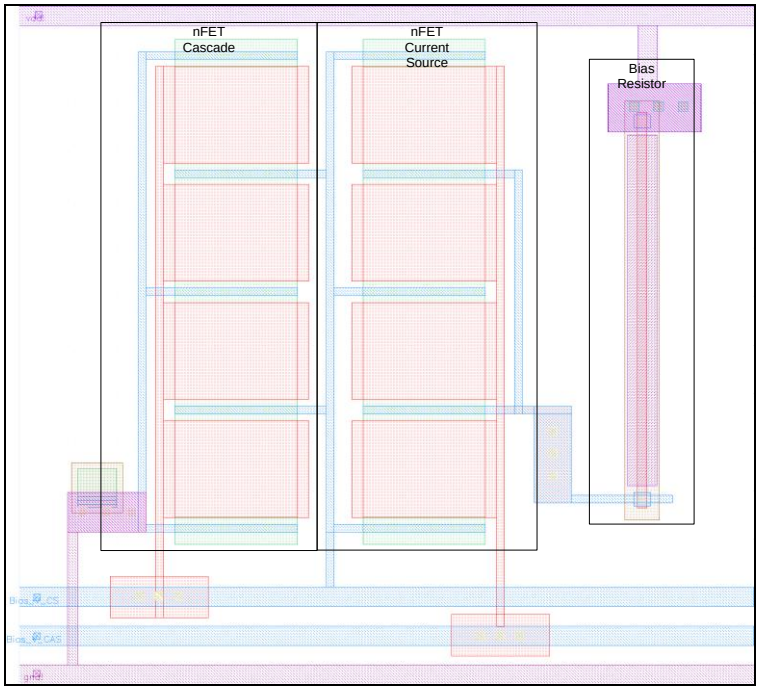


Figure 5.5: Annotated layout of current source cell bias cell, 15 µm by 14 µm.

The drawn layout dimensions of the LVDS receiver bias circuit in Figure 5.4 are a 55 µm by 76 µm. The drawn layout dimensions of the current source cell bias circuit in Figure 5.5 are a 15 µm by 14 µm.

5.7 CURRENT SOURCE CELL MATRIX

The current source cell matrix for a six-bit binary weighted DAC consists of a current source bias circuit and 63 current source cells. The design and layout of the current source cell makes the layout of the current source cell matrix relatively easy, as layouts of single cells are simply placed adjacent to one another to build up the matrix. The annotated layout is shown in Figure 5.6.

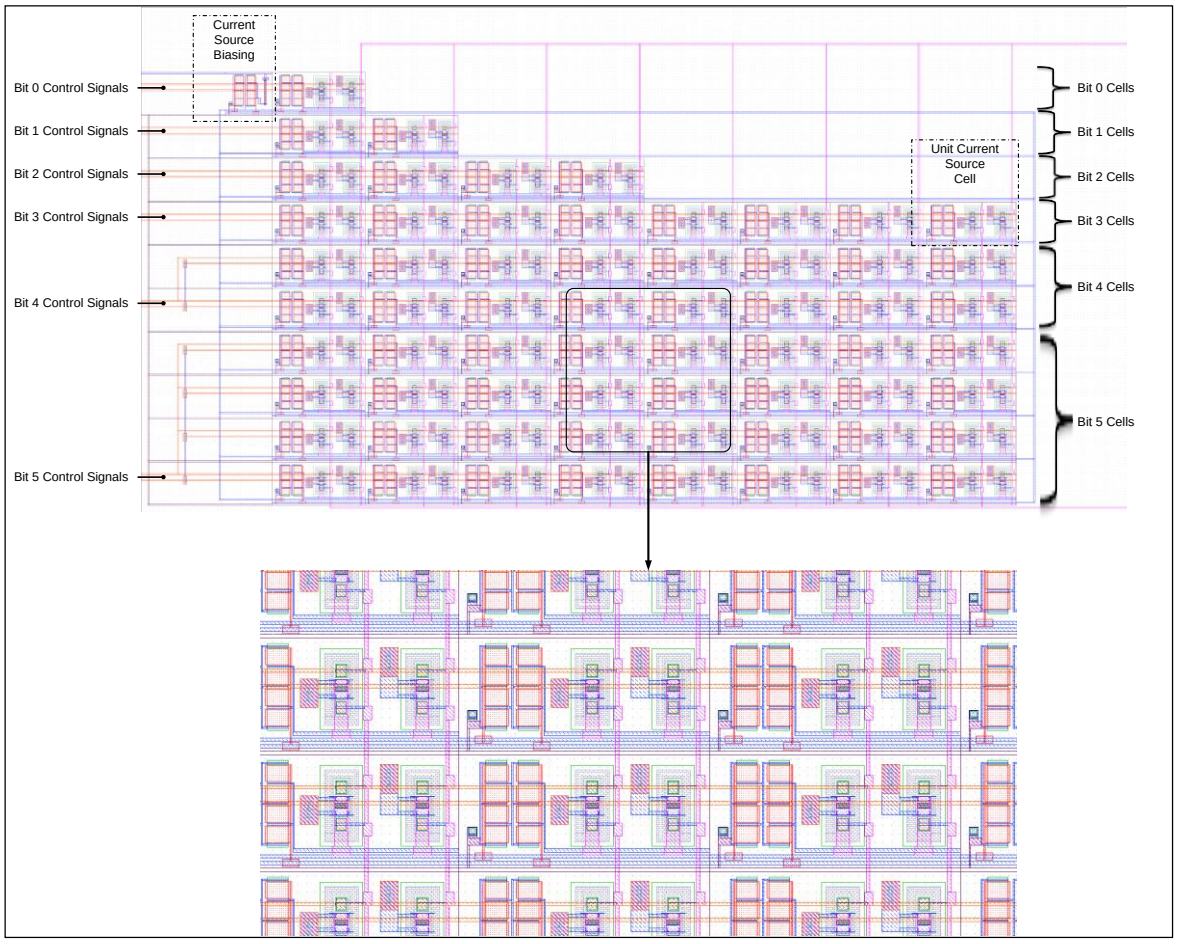


Figure 5.6: Annotated layout of current source cell matrix, 300 µm by 150 µm.

The layout of a single current source cell is stacked to form the matrix shown in Figure 5.6. Each bit in the DAC has a pair of control signals that switch a group of current source

cells. Multiple routing layers are necessary to achieve a compact current source cell matrix. The drawn layout dimensions of the current source cell matrix are a 300 µm by 150 µm.

5.8 COMPLETE LAYOUT AND FABRICATION

The entire DAC layout is achieved by combining the layout of the sub-circuits detailed. The Cadence Virtuoso Layout tool supports hierarchical layouts, which facilitates a drag-and-drop approach from sub-circuit layouts to the overall layout. The complete DAC layout is shown in Figure 5.7.

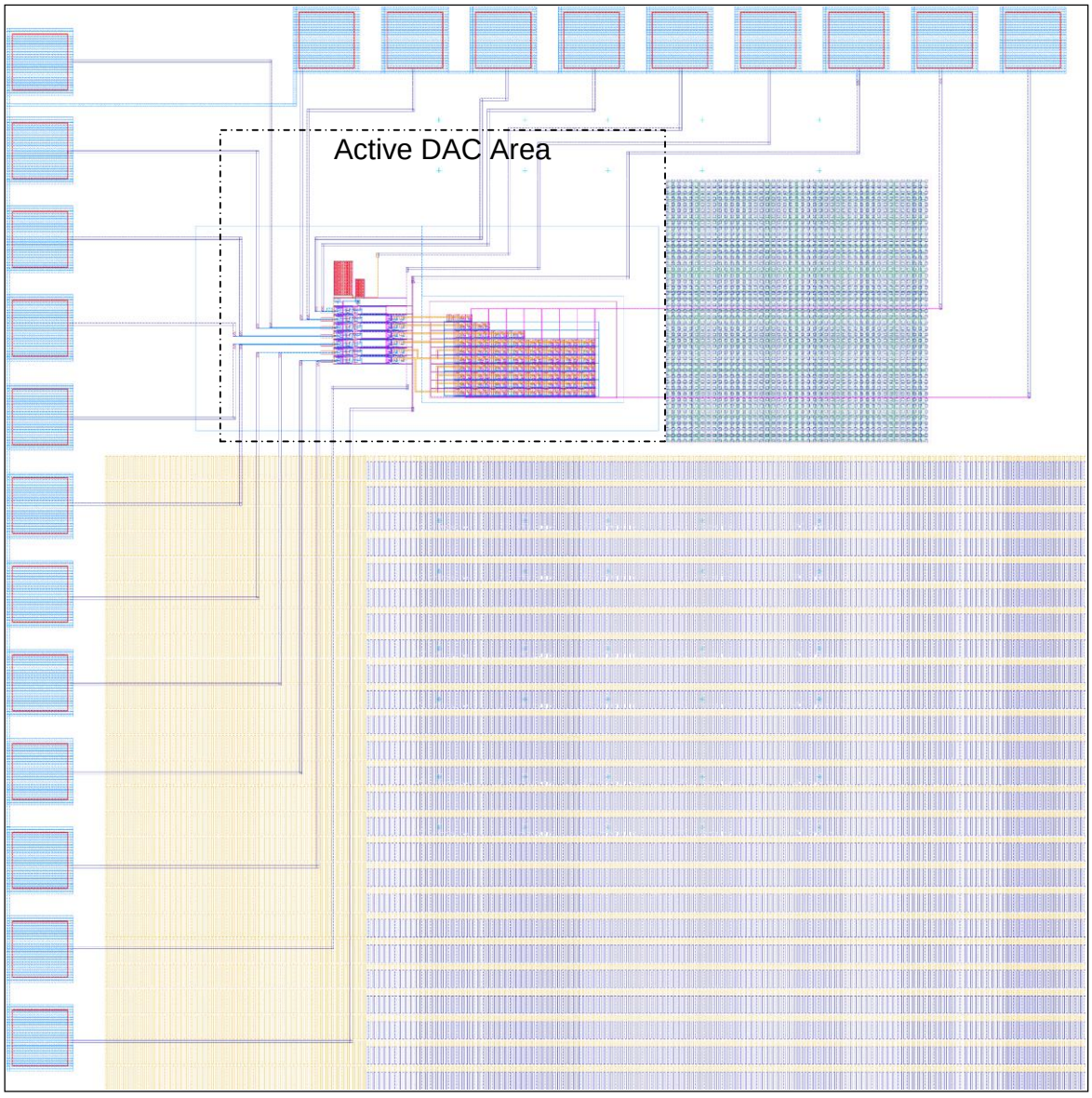


Figure 5.7: Annotated layout of complete DAC, 500 µm by 200 µm.

The DAC layout shown in Figure 5.7 was combined with three other designs to form the layout used for submission for fabrication. A fabrication consideration not highlighted up

to now is the fill requirements for each layer. A fill specification is a fabrication requirement for each metal layer to have a minimum coverage. There are local and global fill requirements that are satisfied by adding dummy cells. A custom dummy cell was used in this design to meet the local and global fill requirements.

The overall layout area is 2 mm by 2 mm, which includes the dummy fill cells. The active DAC area is significantly smaller and is approximately 500 µm by 200 µm or 0.1 mm^2.

The completed layout was fabricated via the MEP through IBM foundries. A micrograph of the unpackaged die is shown in Figure 5.8.

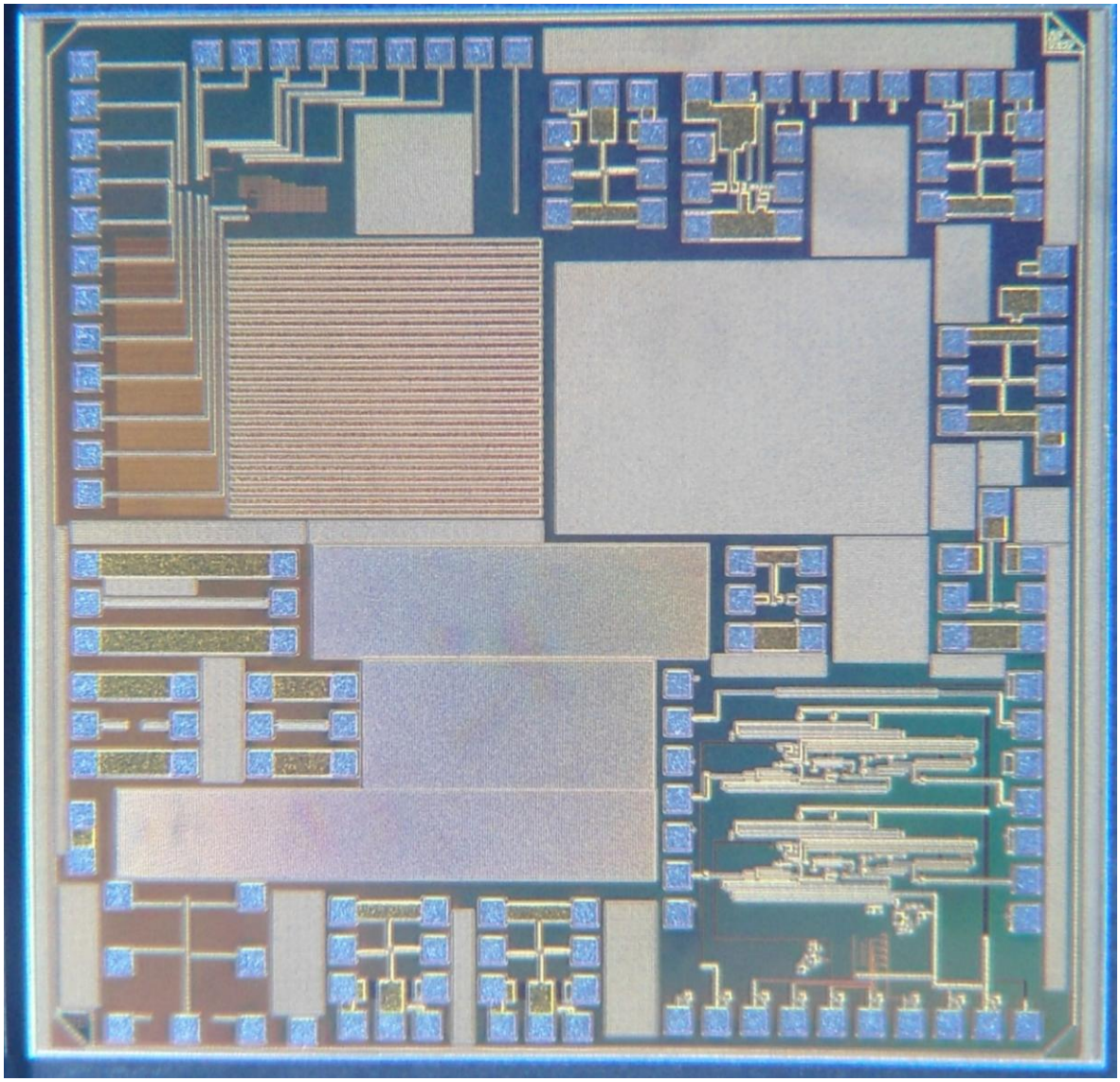


Figure 5.8: Micrograph of complete MPW run integrated circuit with DAC in the upper left quadrant, 4236 µm by 4082 µm .

The die shown in Figure 5.8 was then packaged in a QFN package. A tray of the packaged parts is shown in Figure 5.9. This was the best possible packaging option in terms of frequency performance, as ball grid array packaging was not available.

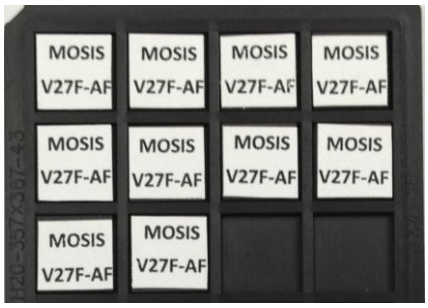


Figure 5.9: Tray of fabricated DAC parts, 6900 µm by 6900 µm.

The packaging shown in Figure 5.9 uses full epoxy bonding to seal the lid. The QFN package is adequate for this DAC design, but ideally a ball grid array package would be used. The packaging options offered to MPW designs, however, do not make provision for ball grid arrays. Ten packaged parts were received. The dimensions of the packaged parts are 6900 µm by 6900 µm.

5.9 PRINTED CIRCUIT BOARD

A printed circuit board was also designed and fabricated. The design was implemented in Altium Designer, a popular PCB design and layout tool. The completed unpopulated PCB is shown in Figure 5.10.

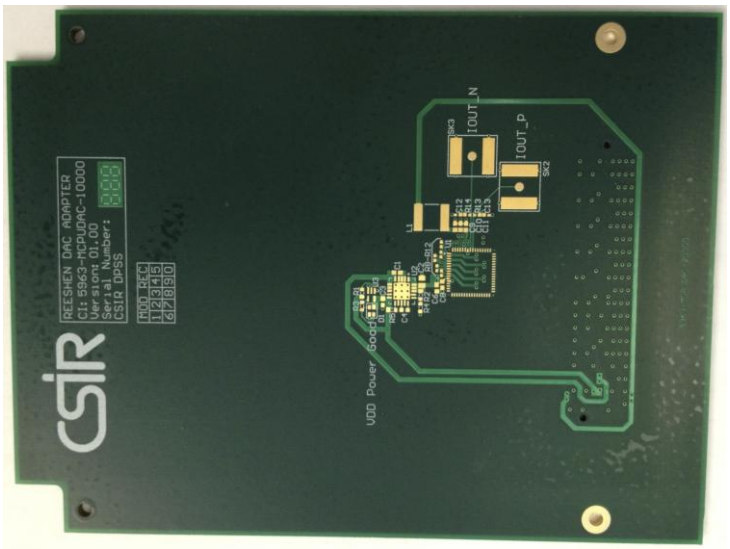


Figure 5.10: DAC PCB. Prototyping of the PCB was funded via the CSIR.

The PCB in Figure 5.10 conforms to the FPGA mezzanine card (FMC) form factor and supplies power and signal interconnections to the DAC. All of the DAC signals are routed through the FMC high-speed connector, which connects to a motherboard. For this design, the DAC FMC card is connected to a processor motherboard supplied by the CSIR. The processor motherboard drives the FMC signals with high-speed LVDS signals from an FPGA as detailed in Chapter 3.7. Further details on the PCB design, schematic and layout are given in appendices A and B.

5.10 CONCLUSION

The layout process and implementation have been detailed. The process and fabrication considerations in the DAC layout have been highlighted and their effect on the design has been explained. The dimensions of the different sub-circuits and their effect on the overall layout area have been detailed. In general, the smallest area achievable on a single circuit layout would not result in the most compact DAC if interconnections are not considered. The fabricated DAC integrated circuit and PCB have also been detailed. The layout of the DAC is a critical aspect of the testing of the hypothesis to ensure that the signal integrity and SFDR that are achieved in the experimental verification match the simulated results.

CHAPTER 6: EXPERIMENTAL RESULTS

6.1 INTRODUCTION

The DAC measurement setup and results are presented in this chapter. The measurement setup consists of the DAC, PCBs and measurement equipment used to perform time and frequency domain measurements. The DAC measurements of static linearity, namely the INL and DNL, are presented, followed by the dynamic linearity SFDR measurements. The complete DAC specifications allow for comparisons to other works based on accepted FOM. A discussion of the measurements concludes this chapter.

6.2 MEASUREMENT SETUP

In order to characterise the DAC, time and frequency domain measurements are required. The DAC IC is mounted on an FPGA FMC card that supplies the DAC with power and signal interconnects. The DAC FMC card is connected to a motherboard supplied by the CSIR. The motherboard carries an FPGA that drives the DAC digital LVDS input signals.

A number of design considerations are needed on the PCBs to ensure that the DAC performance is not degraded. Of specific concern are the length matching of the DAC LVDS signals and isolated power supply regulators from the main processor board. The length matching of tracks ensures that the digital signals arrive at the DAC with minimum timing differences. Timing differences at the DAC input can induce further glitches within the DAC, leading to poorer SFDR performance. The processor motherboard contains various switching components that generate noise. The use of isolated power supply regulators on the DAC FMC board allows the noise from the motherboard to be isolated from the DAC IC.

6.3 MEASUREMENT RESULTS

The prototyped DAC is packaged in a QFN package and mounted on a PCB. The PCB conforms to the FMC form factor and supplies power and signal interconnections to the DAC. For this design, the DAC FMC card is connected to a processor motherboard. The processor motherboard drives the FMC connections with high-speed LVDS signals from

an FPGA. The processor motherboard is 233 mm by 160 mm and the DAC FMC card is 140 mm by 105 mm. Both boards are routed with multiple routing layers with dedicated layers for power and ground to ensure signal integrity. Both the motherboard and FMC slot into a standard rack that allows for power and signal interconnections over a backplane. The processor motherboard and DAC FMC card setup are shown in Figure 6.1.

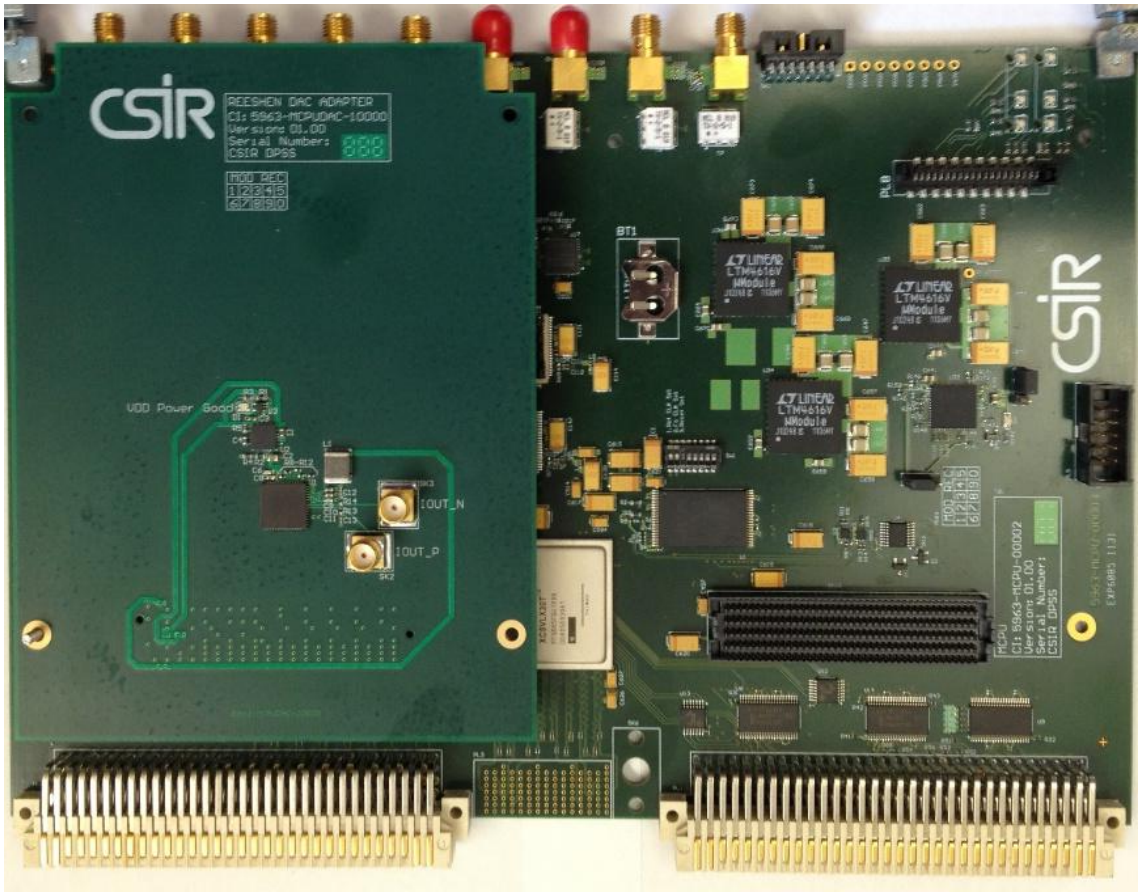


Figure 6.1: Processor motherboard with FMC mezzanine card mounted.

A Tektronix DSA 71254 digital phosphor oscilloscope and Agilent E4447A PSA spectrum analyser were used to perform the time and frequency domain measurements respectively to test the setup in Figure 6.1. The static linearity measurements, namely the DNL and INL, are shown in Figure 6.2 and Figure 6.3 respectively.

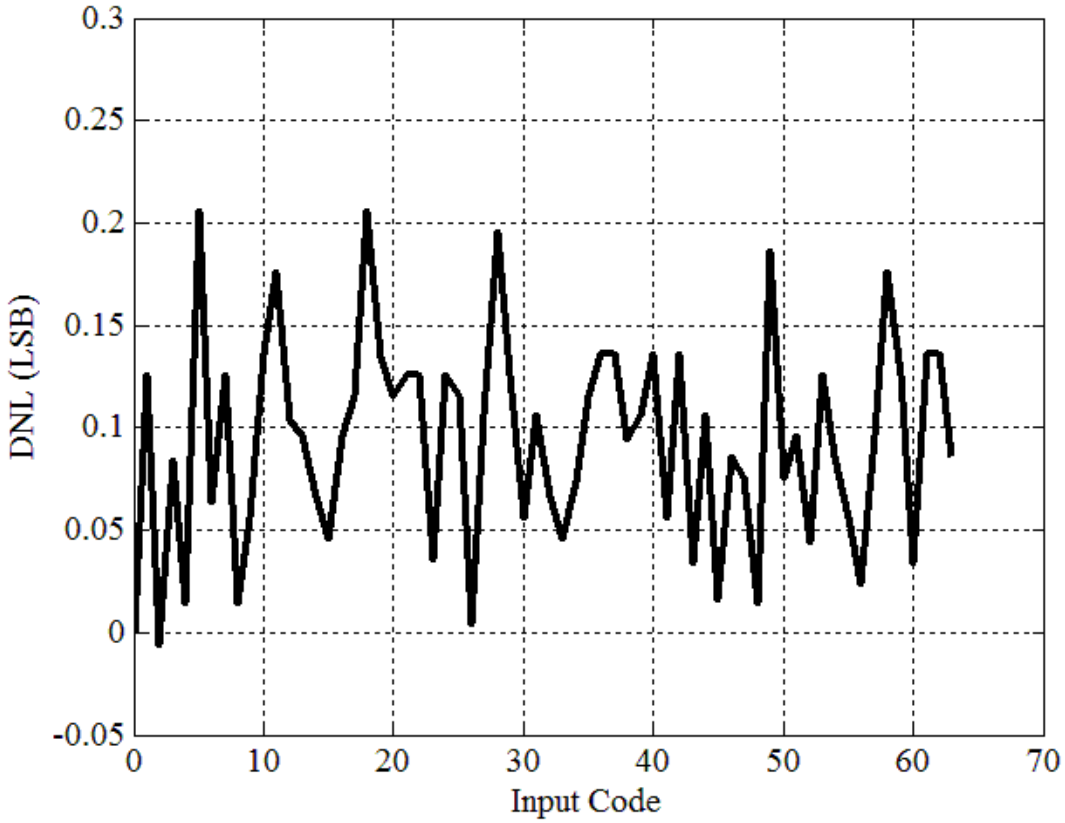


Figure 6.2: DNL of the DAC measured using Tektronix oscilloscope.

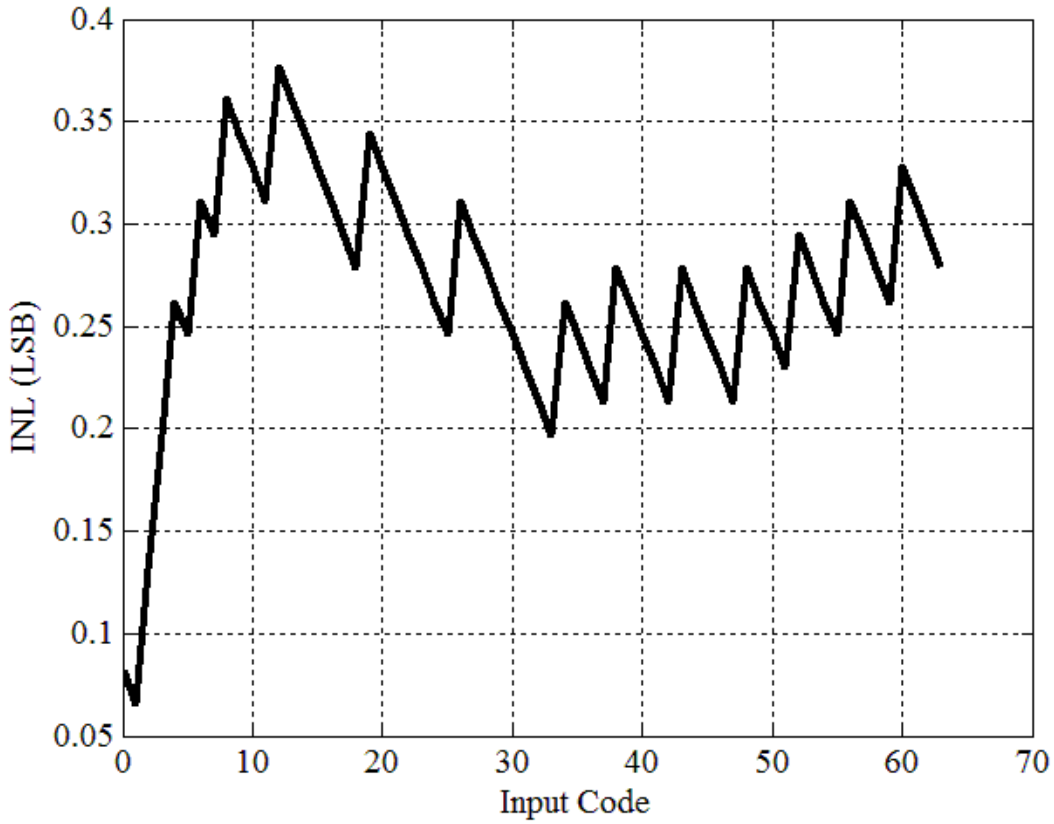


Figure 6.3: INL of the DAC measured using Tektronix oscilloscope.

The DAC is monotonic, as the INL and DNL measurements satisfy the constraints for monotonicity and matching goals shown in Figure 6.2 and Figure 6.3. Neither INL nor DNL exceeds 0.5 LSB, which guarantees monotonic behaviour and the matching requirements detailed in Chapter 4.4. In addition to achieving monotonicity, the INL and DNL reflect the accuracy of the DAC. Having achieved satisfactory static linearity results, the dynamic linearity measurements will be addressed, bearing in mind that good static performance is necessary but not sufficient for good SFDR performance.

The DAC transient behaviour was simulated for an input digital word toggling from the minimum to maximum values to verify the strict timing requirements that could result in timing errors and degrade the SFDR. Simulation results for pertinent signals in the digital chain are presented that are not possible to measure in the packaged DAC IC. The LVDS receiver output for the clock which is the fastest signal is shown in Figure 6.4.

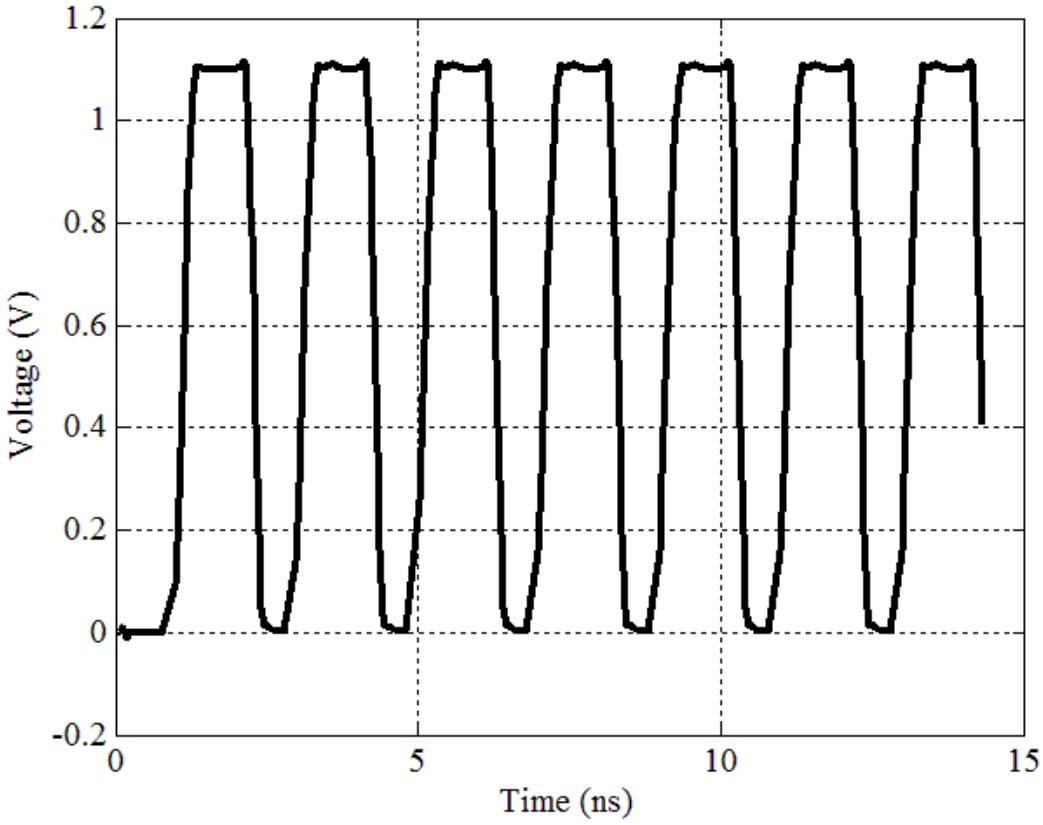


Figure 6.4: LVDS receiver output.

The LVDS receiver output for the 500 MHz clock signal is shown in Figure 6.4. Each of the LVDS receiver outputs are completely independent from each other. The receiver

circuits are identical for the different digital bits hence any timing differences that exist are resultant from routing differences across the bits. In this design, length matching was extensively employed minimising timing differences. The LVDS receiver outputs are fed through the switch driver circuit for signal conditioning. The outputs of the switch driver is shown in Figure 6.5.

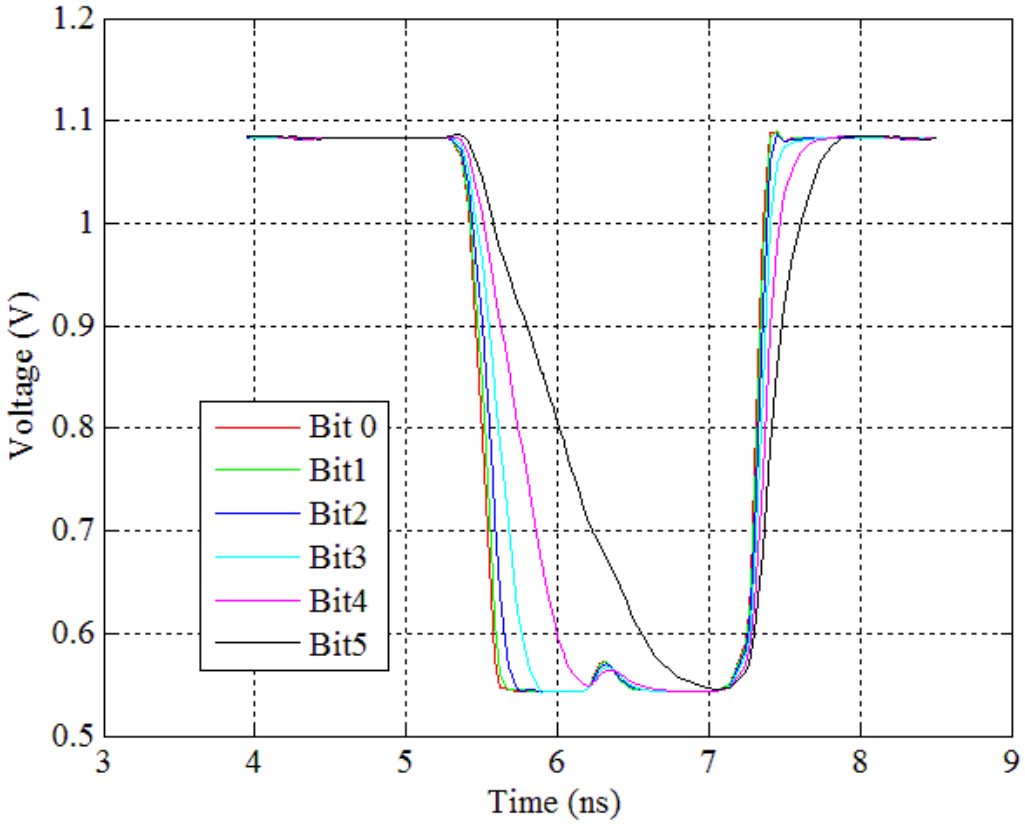


Figure 6.5: Switch driver outputs.

It should be noted from Figure 6.5 that voltage levels have now been level shifted by the swing reduced driver. The six digital paths per bit are superimposed in Figure 6.5 to compare the delays through the digital paths. Any timing glitches present in the signal have also been removed by the de-glitch circuit. The signals are also synchronized to the DAC clock ensuring well synchronized control signals. In Figure 6.5, it is noted that the control signals transition at the same time, however the rise and fall time of each bit gets progressively slower for higher weighted bits primarily due to the number of current sources driven by each switch driver. The time domain DAC output is shown in Figure 6.6 for a 100 MHz sine wave.

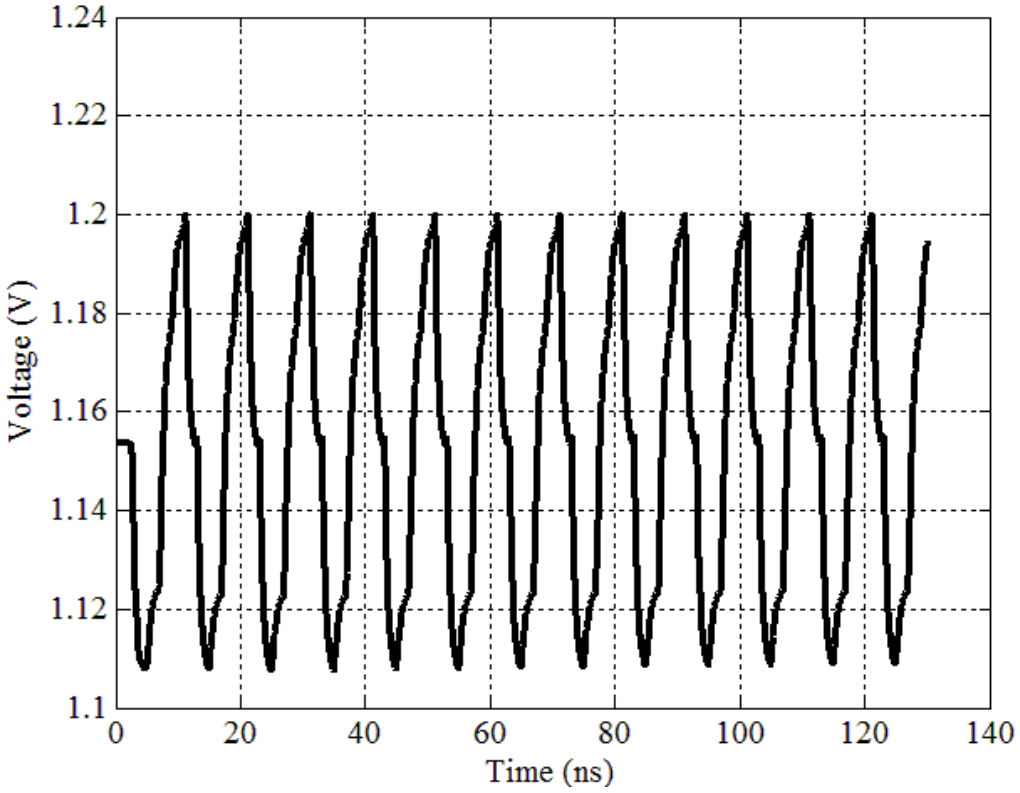


Figure 6.6: Time domain DAC output signal for a 100 MHz sine wave.

The DAC output time domain behaviour shown in Figure 6.6 exhibits no noticeably timing errors. The DAC output spectrum for a 100 MHz sine wave input signal is shown in Figure 6.7.

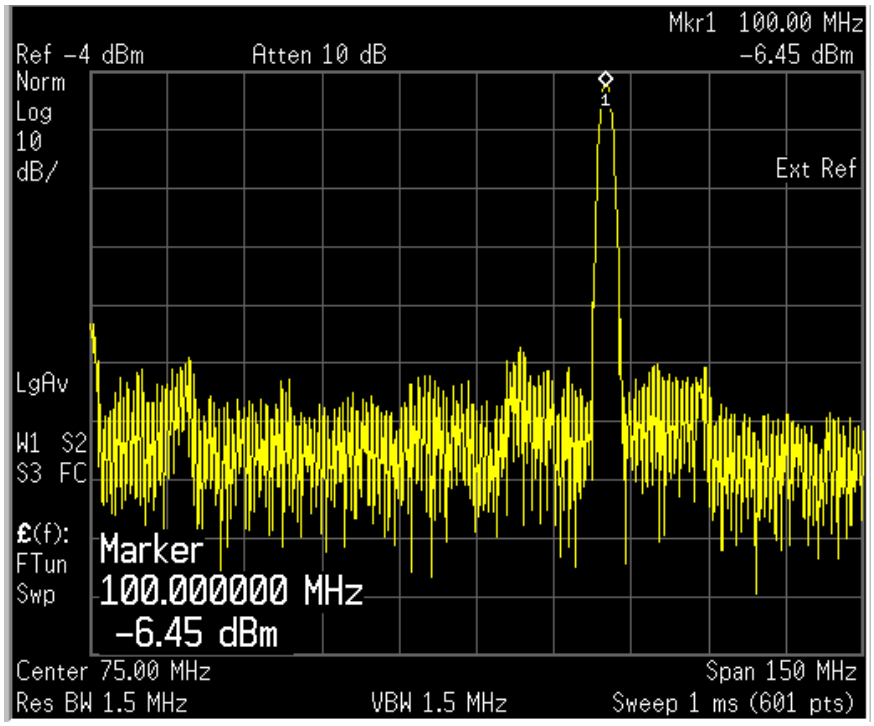
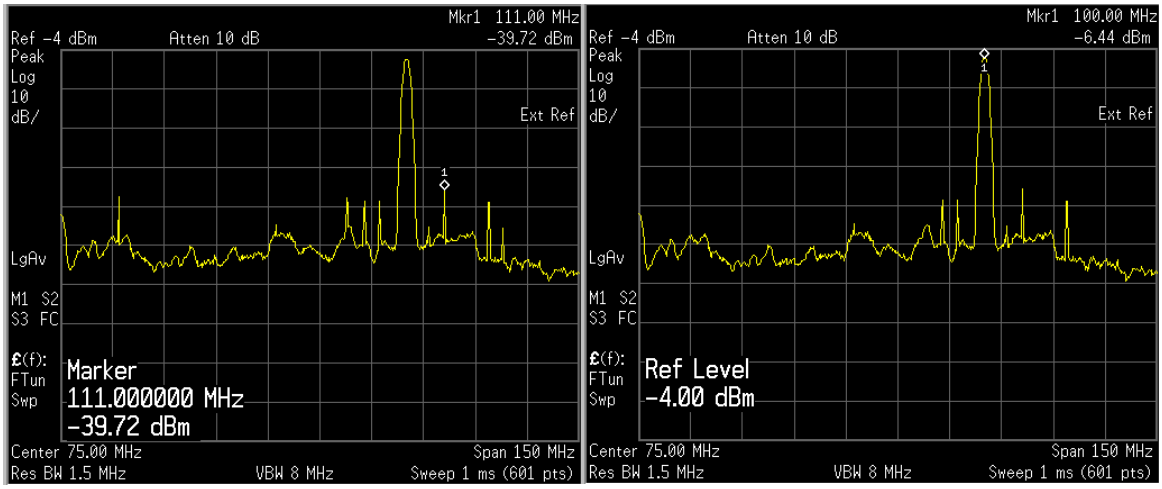


Figure 6.7: DAC output spectrum for a 100 MHz sine wave input signal.

In order to measure the SFDR performance shown in Figure 6.7, the DAC spectrum measurement is set to maximum hold. In this mode, the maximum energy in a measurement bin is displayed. This allows for the accurate measurement of the SFDR performance, as infrequent glitches are also captured. The ratio of the largest unwanted signal to the signal of interest commonly termed the carrier is the SFDR. An example of the SFDR measurement at 100 MHz input frequency is shown in Figure 6.8.



(a) (b)

Figure 6.8: DAC SFDR measurement with (a) DAC spectrum maximum held with marker on largest unwanted signal and (b) DAC spectrum with marker maximum held with marker on wanted 100 MHz signal

In the maximum held measurements in Figure 6.8, the amplitudes of the carrier and largest unwanted signal may now easily calculate the DAC SFDR. This procedure is repeated for multiple frequencies to form the SFDR over frequency measurements.

For each frequency, computer software generates the raw DAC values against time. This information is sent to the FPGA on the processor motherboard and is stored in memory. The FPGA on the processor motherboard drives the DAC LVDS signals and could institute slight delays to each LVDS line to compensate for routing differences or to shift the sampling clock relative to the data.

The SNR is approximately 42 dB, which corresponds to the predicted value from quantisation noise estimates. The simulated and measured SFDR as a function of input frequency is shown in Figure 6.9.

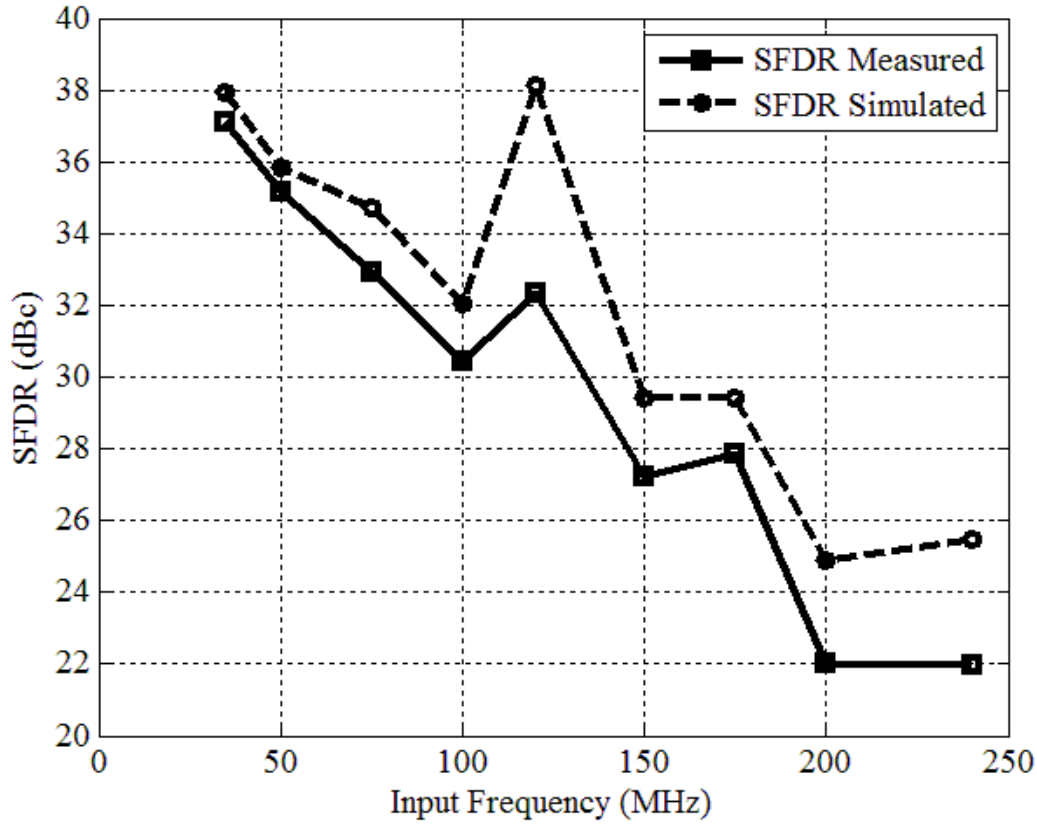


Figure 6.9: Simulated and measured SFDR of the DAC measured using an Agilent spectrum analyser.

As expected, the SFDR worsens as the input frequency increases and is at a worst case of 21.96 dBc with an input frequency of 240 MHz shown in Figure 6.9. The measured results follow the trend of the simulated results generally, but are 2 to 3 dB worse in all measurements. This may be attributed to the chip packaging, bonding wire, PCB signal integrity and crosstalk effects.

In [8] and [40], the SFDR at high frequencies was shown to mainly depend on the output switching capacitance. The design methodology presented in this work did not account for the switching capacitance of the current switches. The capacitor charge and discharge is dependent on the input digital word and output voltage of the DAC. The charge variation is given by [40]:

$$\frac{\Delta Q}{\Delta t} = V_{diff}\frac{\Delta C_{out}}{\Delta t} + C_{out}\frac{\Delta V_{diff}}{\Delta t} \tag{6.1}$$

In [40], an updated SFDR equation that accounts for the switching capacitance was derived. The resulting SFDR equation is given as:

$$SFDR = \frac{10}{N\ R_L C_{sw} w_s} \tag{6.2}$$

In [41], the parasitic output capacitance leading to finite output impedance is addressed with the use of a return-to-zero (RTZ) scheme. RTZ methods insert a zero differential output between two adjacent signals to allow the output transition to be independent of the previous signal. The RTZ technique is suitable for communication applications but not for Radar applications.

In [41], it is described that the Cascode configuration traditionally used to increase output impedance also created parasitic capacitance due to large transistors used for lower mismatch. Hence the addition of a Cascode in this work still limits the high-frequency output impedance and is a possible explanation for the degradation of SFDR performance at close to the Nyquist rate. The analysis to derive the SFDR with the addition of a Cascode transistor in this work is valid only at lower sampling rates and should be updated with the methods presented in [40] and [41].

In addition, at higher frequencies the limits of the LVDS receivers are also reached. At high sampling rates, multiplexing of the digital inputs is used. Recently in [42], the importance of on-chip test inputs is demonstrated. A digital front end design-for-test is integrated on-chip to facilitate the testing at high sampling rates. This eliminates the need for high speed LVDS inputs and multiplexed inputs which can degrade the SFDR and limit the overall achievable sampling rate.

The use of input buffers and latches was replaced with variable delay buffers with a compact layout to compensate for the delay difference among different bits in [42]. The more traditional approach in this work achieved a glitch energy of 3.75 pVs while the variable delay buffers achieved an even lower glitch energy of 1.36 pVs.

The power dissipation and area of the DAC core of this work are very low at less than 4 mW and 0.1 mm^2 respectively. The specifications of the fabricated DAC are documented in Table 6.1.

Table 6.1: DAC Specifications.

Specification	**Value**
Technology	IBM 8HP
Process	130 nm SiGe BiCMOS
Total Area	4 mm^2
Active Area	0.1 mm^2
Sampling Frequency	500 MS/s
Power Dissipation (Core)	3.97 mW
Resolution	6 bits
INL	0.38 LSB
DNL	0.21 LSB
SFDR (worst case)	21.96 dBc

6.4 CONCLUSION

The DAC design is often a trade-off between different performance aspects. The relative importance of the metrics is determined by the needs of its application. For instance, a DAC in a battery-powered device may place a priority on power dissipation. This work placed emphasis on SFDR performance at high frequencies.

In order to compare them to different DAC designs, the FOMs in [7] are used. The first FOM is:

$$FOM_1 = \frac{Power}{2^N . Sample\ Rate} \tag{6.3}$$

The FOM_1 is often used, as it is simple and the information required is often published. However, FOM_1 does not account for SFDR performance and hence an additional FOM that accounts for resolution, power and frequency domain performance is used:

$$FOM_2 = \frac{2^N \ .\ f_{sig}|@SFDR = 6(N-1)}{POWER} \tag{6.4}$$

The FOM_2 is more appropriate for this work and high-speed DACs. It accounts for the linearity of the device over the Nyquist frequency. The parameter f_{sig} is the input signal frequency where the SFDR has dropped 1 bit or 6 dB in comparison with the quantisation limited dynamic range. The FOMs for this work and other projects are tabulated in Table 6.2.

Table 6.2: Comparison with other DACs published.

	This work	**[7]**	**[12]**	**[13]**	**[14]**	**[15]**
Technology	130 nm BiCMOS	130 nm CMOS	0.35 µm CMOS	0.25 µm BiCMOS	0.18 µm BiCMOS	0.25 µm BiCMOS
Sampling	500 MS/s	3 GS/s	1 GS/S	30 GS/s	10 GS/s	13.4 GS/s
Core Area	0.1 mm^2	0.2 mm^2	-	1.8 mm^2	1.5 mm^2	0.9 mm^2
Resolution	6 bit	6 bit	10 bit	4 bit	5 bit	6 bit
Power Dissipation	3.97 mW	29 mW	110 mW	455 mW	10.2 mW	1050 mW
Frequency (SFDR = 6N-1)	170 MHz	1.5 GHz	-	-	-	6 GHz
FOM_1	0.125 pJ	0.15 pJ	0.11 pJ	0.95 pJ	0.031 pJ	1.22 pJ
FOM_2	2.72 GHz/ mW	3.3 GHz/ mW	4.7 GHz/ mW	-	-	0.36 GHz/ mW

This work compares favourably in FOM_1 because of the extremely low power dissipation. Many designs that make use of SiGe technology achieve the frequency performance by using large external power supply voltages at the DAC output at the expense of power.

In the FOM_2, this work is not the best but does achieve good results. This can be attributed to a lower sampling rate when compared to other work, which can be achieved with LVDS receivers with deserialisation. This type of technology is commercially available but was not available for this scholarly work. Nevertheless, the sampling rates were still adequate for the purposes of this work.

The power and area of the DAC presented in this work is the lowest of any in the comparison, partially because of the process technology but also because of the compact

layout, smaller transistor sizes and binary weighted architecture. The low power and area are particularly suitable for a system-on-chip requiring a DAC. The DAC in this work is able to achieve better SFDR performance than 5 effective number of bits up to approximately 130 MHz. The SFDR performance degrades for input frequencies above 170 MHz. Possible explanations for the SFDR performance at high frequencies include output capacitance effects and limitations of the LVDS receivers are discussed.

CHAPTER 7: CONCLUSION

7.1 INTRODUCTION

A design approach to high-speed binary weighted DACs was synthesised. It takes into account voltage headroom and short-channel effects that are present in modern fabrication processes. A BiCMOS six-bit binary coded DAC was designed and implemented in IBM 8HP SiGe 130 nm process technology and was shown to have a SFDR of 21.96 dB at the Nyquist input frequency and a sampling rate of 500 MS/s.

BiCMOS technology is shown to have advantages in the design of high-speed DACs in the area of the clock feedthrough effect in the current switches. However, in a number of design areas such as the current source cell, the voltage headroom available in modern fabrication processes favours the use of NMOS transistors as opposed to HBTs.

The use of BiCMOS technology in high-speed DAC design theoretically offers higher performance over CMOS-only technology but in practice, system considerations such as area and voltage headroom limit its use to specific areas in the DAC architecture.

7.2 LIMITATIONS AND ASSUMPTIONS

SFDR performance can be thought of as an emergent property of DACs that arises out of many metrics and is influenced by various factors. For instance, to achieve good SFDR, both dynamic linearity and static linearity must be considered. Even if a DAC meets static linearity goals, it does not guarantee good SFDR performance; other aspects such as power supply integrity also can degrade the SFDR.

The SFDR calculations in this work focussed on the identified dominant dynamic linearity phenomena of finite output impedance, clock feedthrough and distortion. In [40], it is shown that SFDR at high sampling rates has a further dynamic non-linearity created by the switching transistors capacitance.

One of the key assumptions of this work is that all other aspects that affect SFDR performance besides the dynamic linearity phenomena of finite output impedance, clock feedthrough and distortion are sufficient for the testing of the hypothesis.

In the SFDR measurements, this assumption holds true for most of the frequency spectrum except near the Nyquist sampling rates in which the limits of the LVDS receivers are reached. Typically the LVDS receiver component is a standard cell (intellectual property block) that is purchased by many commercial entities. This work being a student design, it was impossible to use commercially available LVDS standard cells in view of the costs involved.

Another limitation of the work is the constraint of available I/Os, limiting the research to six-bit DACs. The constraint on resolution placed a finite limit on the achievable SFDR owing to the quantisation effect. Ideally the architecture of the DAC and area available to the DAC core could achieve eight bits of resolution at the expense of increasing the area by a factor of around 16. This would potentially result in a better SFDR spectrum due to resolution increase and an increased number of current source cells to supply more current. Another important limitation stemming from the constraint of available I/O is that the number of power and ground pads was limited. Ideally ground and power pads should be distributed and interleaved between data lines to reduce coupling of noise.

7.3 FUTURE WORK AND IMPROVEMENTS

The following list of future work and improvements are suggested:

- A study into a timing-compensated DAC. Each bit of the DAC controls a different number of current source cells and has independent routing. This creates timing differences between the different bits, leading to degradation of the SFDR. A possible solution to this phenomenon is to use the ability of the device driving the DAC input to fine-tune the delays between the different DAC input bits. This can be achieved with current FPGA technology. A system to measure the timing differences dynamically and then compensate for such timing differences is suggested as a further research project.

- A study into signal-processing techniques within the digital domain to improve SFDR is suggested. The combination of BiCMOS fabrication processes with signal-processing techniques such as dithering is an unexplored sphere. The addition of intentional noise to cancel out non-linearity effects poses a research challenge.

- A study into the effect of output capacitance on the design methodology presented is suggested. The output capacitance was shown recently to be a dominant dynamic non-linearity at high sampling rates.

A major limitation of the DAC is the digital interface as the sampling rate gets higher. This work made use of high-speed LVDS serial links. On the ADC technology, modern ultra-high speed standards have begun to appear commercially, such as the JESD204 for ADC data converter serial interface standard. This interface enables the use of higher speed data links to reduce the number of links required and thus reduces board complexity. A similar study into optimal interfaces to the DACs is proposed.

7.4 CRITICAL EVALUATION OF THE HYPOTHESIS

The hypothesis of this work proposed that SFDR performance of high-speed DACs can be improved if distortion and clock feedthrough can be reduced and the output impedance can be increased with the use of BiCMOS technology. The design architecture allowed for the improvement of two of the three dynamic linearity-degrading phenomena. The clock feedthrough and distortion were lowered over traditional designs but the output impedance was the same compared to traditional CMOS design.

The DAC design compares well in typical FOMs to other works in the literature. The inclusion of the HBT current switches over the NMOS current switches improves distortion and clock feedthrough. The following aspects of the work are highlighted:

- A BiCMOS implementation of a high-speed DAC was shown to enhance the SFDR across the Nyquist band by improving two of the three main influencing factors in the current-steering architecture.

- A novel current source cell is implemented in a BiCMOS process that comprises HBT current switches, an NMOS cascode and NMOS current source cell to overcome distortion by specifically enhancing the SFDR for high-speed DACs by lowering current switch distortion and reducing the clock feedthrough effect.

- A systematic design approach was synthesised resulting in a binary weighted DAC that was shown to maintain good metrics in sampling rate, area and power dissipation.

- A six-bit current-steering DAC was designed to experimentally verify the hypothesis along with the required supporting circuits.

- The DAC is implemented using SiGe BiCMOS 130 nm technology and achieves a better than 21.96 dBc SFDR across the Nyquist band for a sampling rate of 500 MS/s with a core size of 0.1 mm^2 and dissipates 4 mW compared to other BiCMOS DACs that achieve similar SFDR performance with higher output voltages, resulting in much larger power dissipation.

The research questions and hypothesis of this work addressed SFDR performance across the Nyquist band in high speed DACs by using a BiCMOS implementation. It was shown that the advantages of BiCMOS process in the current source cells results in a lower distortion and reduction of the clock feedthrough effect.

A higher output impedance would have further enhanced the SFDR but was shown to be similar to the output impedance in a CMOS only process primarily due to the low voltage headroom in modern fabrication processes. A systematic and iterative design approach to achieve an optimal SFDR while still maintaining a good sampling rate, area and power dissipation was derived and demonstrated to design a six-bit DAC that verifies the hypothesis experimentally. The design approach differs from existing literature in that constraints in modern fabrication processes are prioritised while still satisfying the traditional matching constraints.

REFERENCES

[1] G. Chandra and A. Seedher, "On the spectral tones in a digital-analog converter due to mismatch and flicker noise", *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 7, pp. 619-623, Jul. 2008.

[2] C-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2", *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948-1958, Dec. 1998.

[3] I. Benamrane and Y. Savaria, "Design techniques for high speed current-steering DACs", *IEEE North-East Workshop on Circuits and Systems*, Montreal, pp. 1485-1488, 5-8 Aug. 2007.

[4] P. Aliparast and N. Nasirzadeh, "Very high-speed and high-accuracy current-steering CMOS D/A converter using a novel 3-D decoder", *Analog Integrated Circuits and Signal Processing*, vol. 60, no. 3, pp. 195-204, Sept. 2009.

[5] T. Chen and G. G. E. Gielen, "The analysis and improvement of a current-steering DAC's dynamic SFDR—II: The output-dependent delay differences", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 2, pp. 268-279, Feb. 2007.

[6] D. Marche and Y. Savaria, "An improved switch compensation technique for inverted R-2R ladder DACs", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 6, pp. 1115-1124, Jun. 2009.

[7] X. Wu, P. Palmers, and M. S. J. Steyaert, "A 130 nm CMOS 6-bit full Nyquist 3 GS/s DAC", *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2396-2403, Nov. 2008.

[8] C-H. Lin, F. M. L. Van der Goes, J. R. Westra, J. Mulder, Y. Lin, E. Arslan, E. Ayranci, X. Liu, and K. Bult, "A 12 bit 2.9 GS/s DAC with IM3 ≪ -60 dBc beyond 1 GHz in 65 nm CMOS", *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3285-3293, Dec. 2009.

[9] Z. Y. Cui, J. H. Choi, Y. S. Kim, S. H. Kim, and N. S. Kim, "Application of a low-glitch current cell in 10-bit CMOS current-steering DAC", *Microelectronics International*, vol. 26, no. 3, pp. 35-40, Jul. 2009.

[10] M. Khafaji, H. Gustat and C. Scheytt, "A 6 bit linear binary RF DAC in 0.25 µm SiGe BiCMOS for communication systems", *IEEE MTT-S International Microwave Symposium*, Anaheim, pp. 916-919, 23-28 May 2010.

[11] Y. D. Jeon, J. K. Kwon, Y. G. Kwon and S. H. Lee, "A 6b 1.4 GS/s 11.9 mW 0.11 mm^2 64 nm CMOS DAC with a 2-D INL bounded switching scheme", *IEEE SoC Design Conf*, Seoul, pp. 198-200, 22-23 Nov. 2010.

[12] A. Van Der Bosch, M. A. F. Borremans, M. Steyaert, and W. Sansen, "A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter", *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 315-324, Mar. 2001.

[13] S. Haider and H. Gustat, "A 30 GS/s 4-bit binary weighted DAC in SiGe BiCMOS technology", *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Boston, pp. 46-49, 30 Sept. - 2 Oct. 2007.

[14] J. I. Jamp, J. Deng, and L. E. Larson, "A 10GS/s 5-bit ultra-low power DAC for spectral encoded ultra-wideband transmitters", *Radio Frequency Integrated Circuits (RFIC) Symposium*, Honolulu, pp. 31-24, 3-5 June 2007.

[15] M. Khafaji, H. Gustat, B. Sedighi, F. Ellinger, and J. C. Scheytt, "A 6-bit fully binary digital-to-analog converter in 0.25-µm SiGe BiCMOS for optical communications," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 9, pp. 2254–2264, Sep. 2011.

[16] T. Chen and G. G. E. Gielen, "The analysis and improvement of a current-steering DACs dynamic SFDR—I: The cell-dependent delay differences", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 1, pp. 3-15, Jan. 2006.

[17] J. Moon, M. Song, S. Shin, K. Moon, and B. Park, "Design of a laminated current cell relocation 12-bit CMOS D/A converter with a high output impedance

technique and a merged switching logic", *Analog Integrated Circuits and Signal Processing*, vol. 63, no. 3, pp. 407-414, Jun. 2010.

[18] I. Myderrizi and A. Zeki, "A 12-bit 0.35 µm CMOS area optimized current-steering hybrid DAC", *Analog Integrated Circuits and Signal Processing*, vol. 65, no. 1, pp. 67-75, Oct. 2010.

[19] X. Geng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "24-Bit 5.0 GHz direct digital synthesizer RFIC with direct digital modulations in 0.13 µm SiGe BiCMOS technology", *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 944-954, May 2010.

[20] A. Fornasari, F. Borghetti, P. Malcovati, and F. Maloberti, "A second-order ∑Δ multi-bit RD modulator with on-line calibration and digital correction of the digital-to-analog converter mismatches", *Analog Integrated Circuits and Signal Processing*, vol. 62, no. 2, pp. 193-204, Feb. 2010.

[21] M. Shen, J. Tsai, and P. Huang, "Random swapping dynamic element matching technique for glitch energy minimization in current-Steering DAC", *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 5, pp. 369-373, May 2010.

[22] D. Seo and H. Gene, "A low-spurious low-power 12-bit 160-MS/s DAC in 90-nm CMOS for baseband wireless transmitter", *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 486-495, Mar. 2007.

[23] J . Bastos, A. M. Marques, M. S. J. Steyaert, and W. Sansen , "A 12-bit intrinsic accuracy high-speed CMOS DAC", *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1959-1969, Dec. 1998.

[24] IBM Foundry and Manufacturing Services Education, BiCMOS8HP Design Kit and Technology Training manual, San Jose: Cadence Design Systems, 18 July 2009.

[25] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y.-C. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors—Part I: Materials, physics and circuits," *IEEE Trans. Electron Devices*, pp. 469–482, Mar. 1995.

[26] J. D. Cressler, "SiGe HBT technology: A new contender for Si-based RF and microwave circuit applications," *IEEE Trans. Microwave Theory Tech*, vol. 46, pp. 572–589, May 1998.

[27] Freescale Semiconductor. "Application Note 1902: Quat Flat No-Lead", Available at: http://cache.freescale.com/files/analog/doc/app_note/AN1902.pdf. Oct. 2014 [Accessed Dec. 24, 2014].

[28] MOSIS. "MOSIS packaging and assembly", Available at: http://www.mosis.com/Technical/Packaging/pkg-intro.html#wire, [Accessed June. 14, 2014].

[29] W. Kester. "Analog devices tutorial: Evaluating high speed DAC performance", Available at: http://www.analog.com/static/imported-files/tutorials/MT-013.pdf, Aug, 2008, [Accessed June. 20, 2014].

[30] Xilinx. "Virtex-4 FPGA data sheet: DC and switching characteristics", Available at: http://www.xilinx.com/support/documentation/data_sheets/ds302.pdf , Sep. 2009 [Accessed June. 28, 2014].

[31] M. Steyaert, J. H. Huijsing and A. Van Roermund, "Introduction to high-speed digital-to-analog converter design" in *Analog Circuit Design : Scalable Analog Circuit Design, High-Speed D/A Convertors, RF Power Amplifiers*, The Netherlands, Kluwer Academic Publishers, 2002, ch. 2, sec. 1, pp. 115-150.

[32] M. Steyaert, J. H. Huijsing and A. Van Roermund, "Solving static and dynamic performance limitations for high speed D/A converters", in *Analog Circuit Design : Scalable Analog Circuit Design, High-Speed D/A Convertors, RF Power Amplifiers*, The Netherlands, Kluwer Academic Publishers, 2002, ch. 2, sec. 4, pp. 189-210.

[33] Y. Cong and R. L. Geiger, "Formulation of INL and DNL yield estimation in current-steering D/A converters", *IEEE Symposium on Circuits and Systems*, Scottsdale, vol. 3, pp. 149-152, 26-29 May 2002.

[34] M. Steyaert, J. H. Huijsing and A. Van Roermund, "Design considerations for a retargetable 12b 200 MHz CMOS current-steering DAC" in *Analog Circuit Design: Scalable Analog Circuit Design, High-Speed D/A Convertors, RF Power Amplifiers*, The Netherlands, Kluwer Academic Publishers, 2002, ch. 2, sec. 2, pp. 151-170.

[35] IBM Foundry and Manufacturing Services Education, BiCMOS8HP Model Reference Guide, San Jose: Cadence Design Systems, 22 Sept. 2009.

[36] A. Van Der Bosch, M. Steyaert, and W. Sansen, "SFDR-bandwidth limitations for high speed high resolution current-steering CMOS D/A converters", *Proc. IEEE Int. Conf. Electronics, Circuits and Systems*, Pafos, vol. 3, pp. 1193 -1196, 5-8 Sep. 1999.

[37] R. S. Gaddam, K. S. Lee, and C. K. Kwon, "A 10-bit dual plate sampling DAC with capacitor reuse on-chip reference voltage generator", *Microelectronics Journal*, vol. 44, no. 6, pp. 511-518, Jun. 2013.

[38] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O interface for Gb/s-per-pin operation in 0.35-µm CMOS", *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 706-711, Apr. 2001.

[39] P. Wijetunga, "A 10.0Gb/s all-active LVDS receiver in 0.18 µm CMOS technology", *IEICE Electronics Express*, vol. 3, no. 10, pp. 216-220, May. 2006.

[40] M. Khafaji, C. Scheytt, U. Jörges, D. Micusik and F. Ellinger, "SFDR considerations for current steering high-speed digital to analog converters", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Portland, pp. 1-4, 30 Sep. 2012.

[41] W. Lin, H. Huang and T. Kuo, "A 12-bit 40 nm DAC achieving SFDR > 70dB at 1.6 GS/s and IMD < -61 dB at 2.8 GS/s with DEMDRZ technique", *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 708 -717, Mar. 2014.

[42] G. I. Radulov, P. J. Quinn and A. H. M. van Roermund, "A 28-nm CMOS 7-GS/s 6-bit DAC With DfT Clock and Memory Reaching >50 dB Up to 1 GHz", *IEEE Trans. VLSI Syst*, To be published, Sep. 2014.

APPENDIX A: PRINTED CIRCUIT BOARD SCHEMATICS

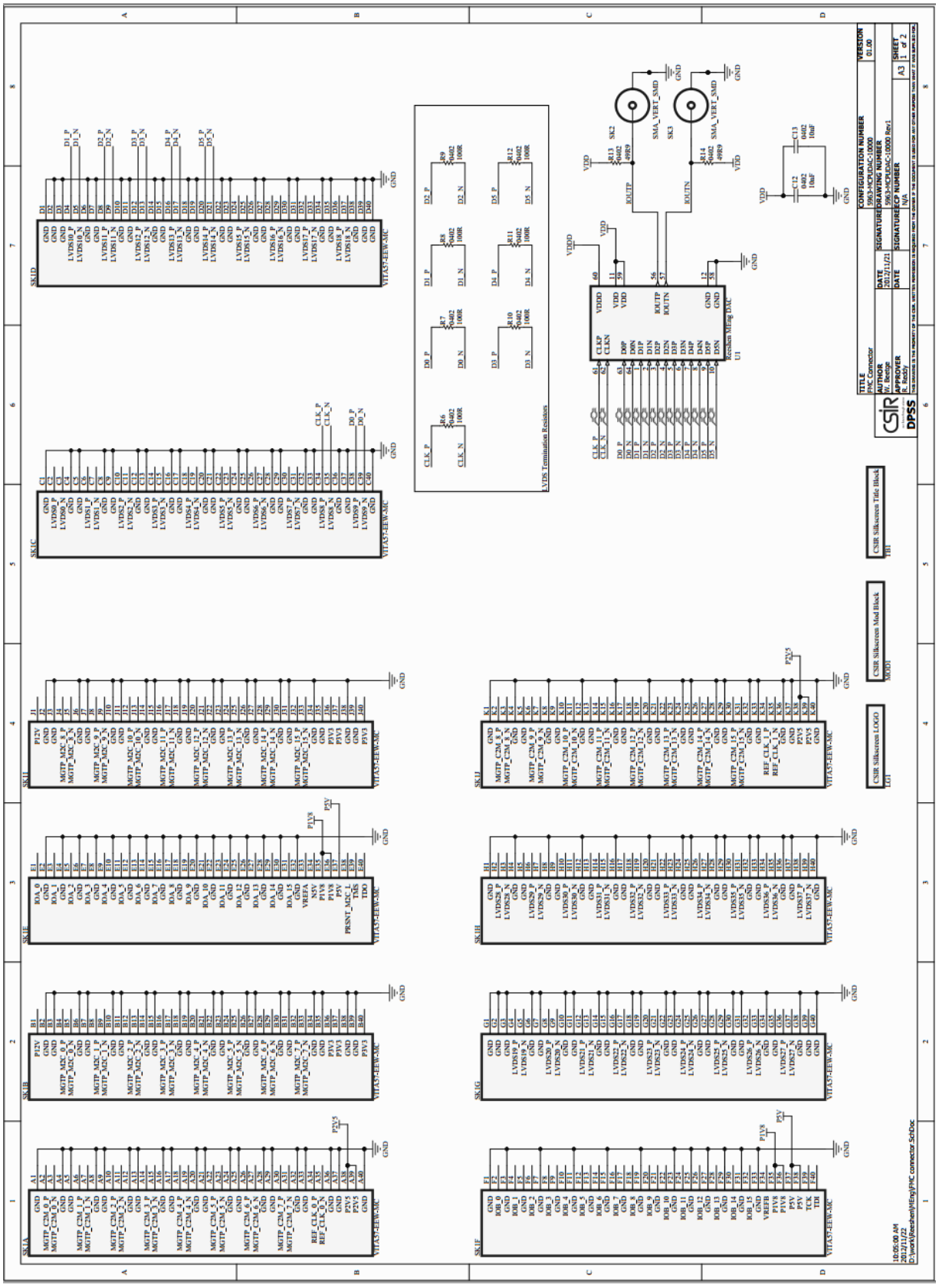


Fig. A.1. DAC FMC PCB Schematic 1.

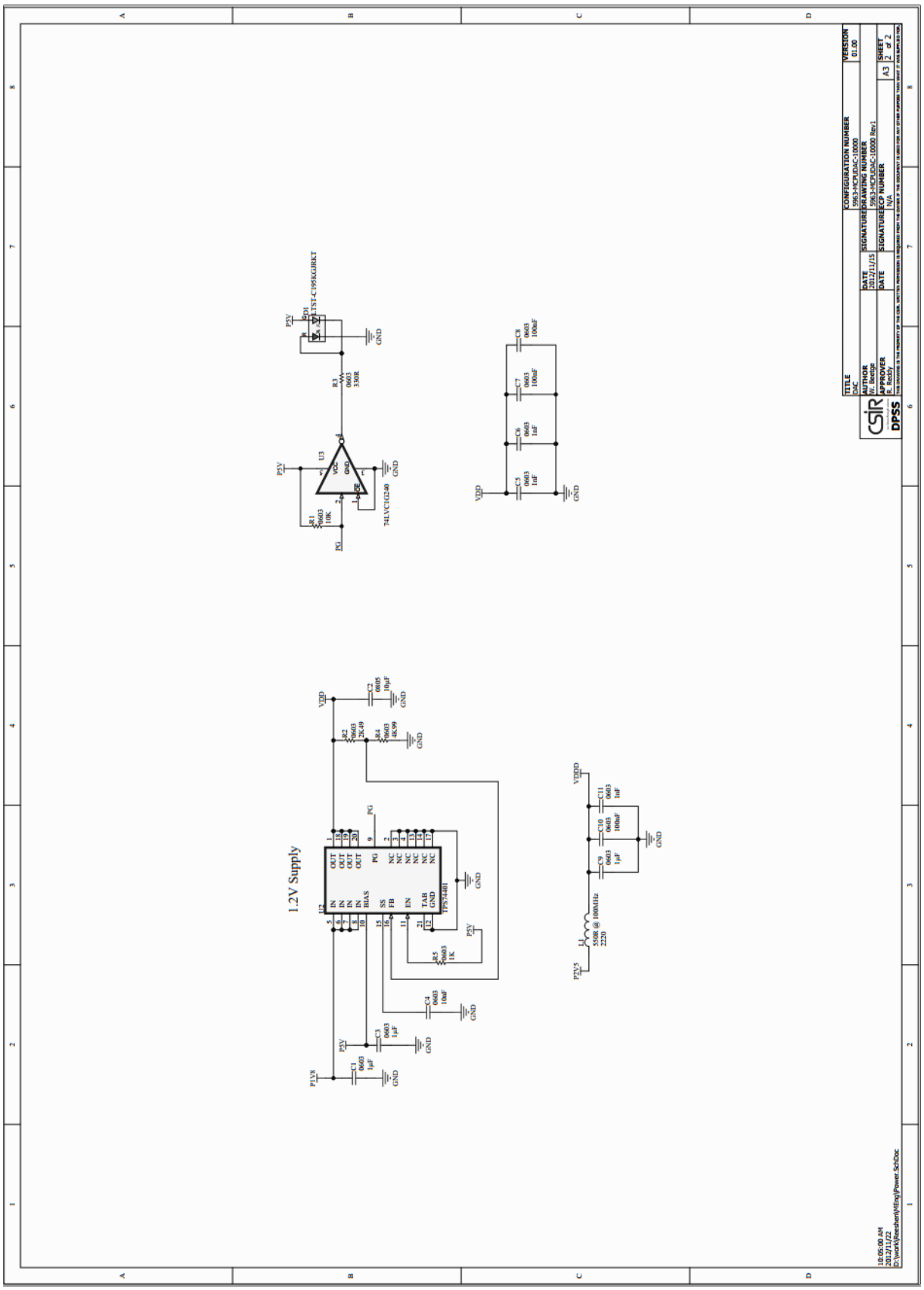


Fig. A.2. DAC FMC PCB Schematic 2.

APPENDIX B: PRINTED CIRCUIT BOARD LAYOUT AND BILL OF MATERIALS

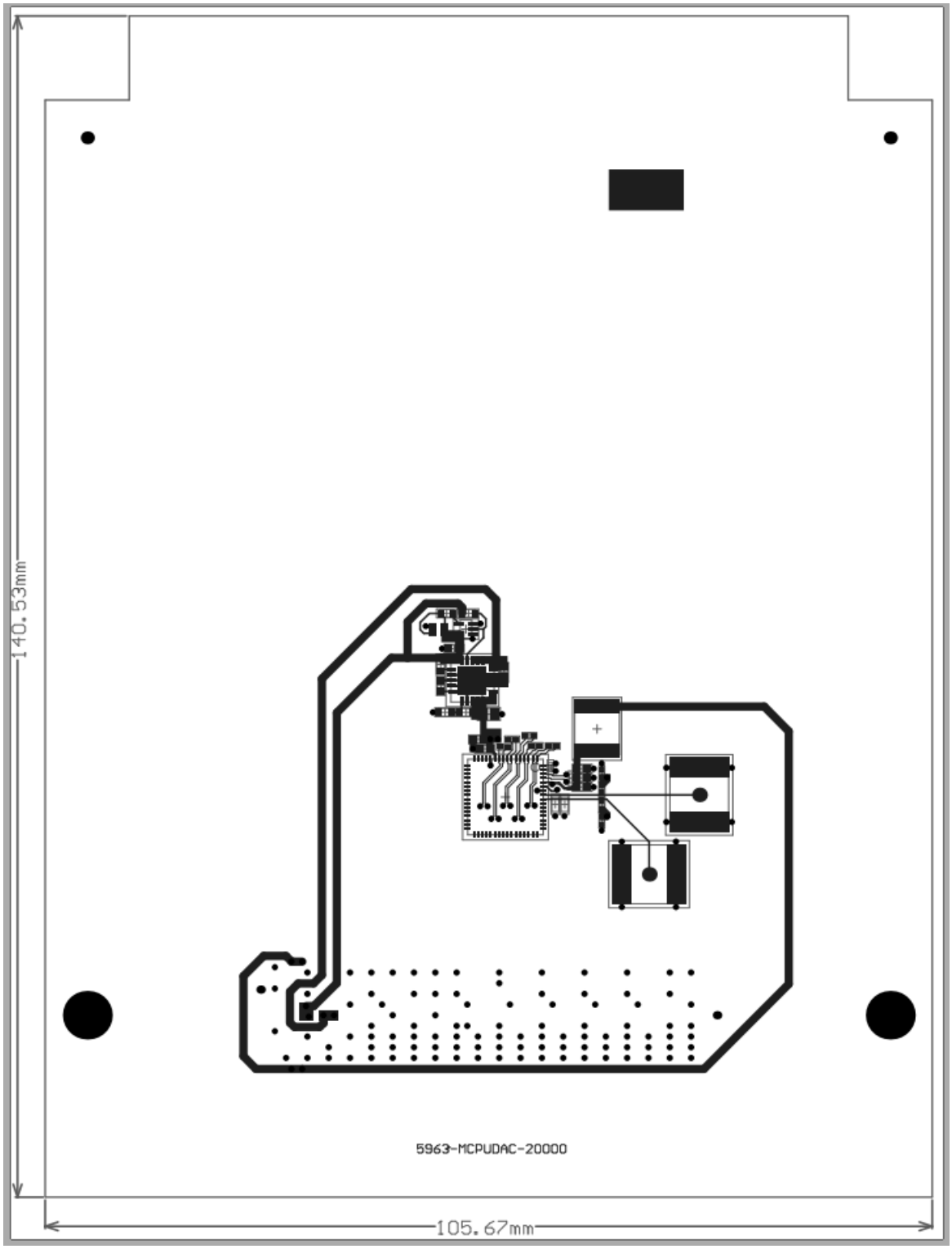
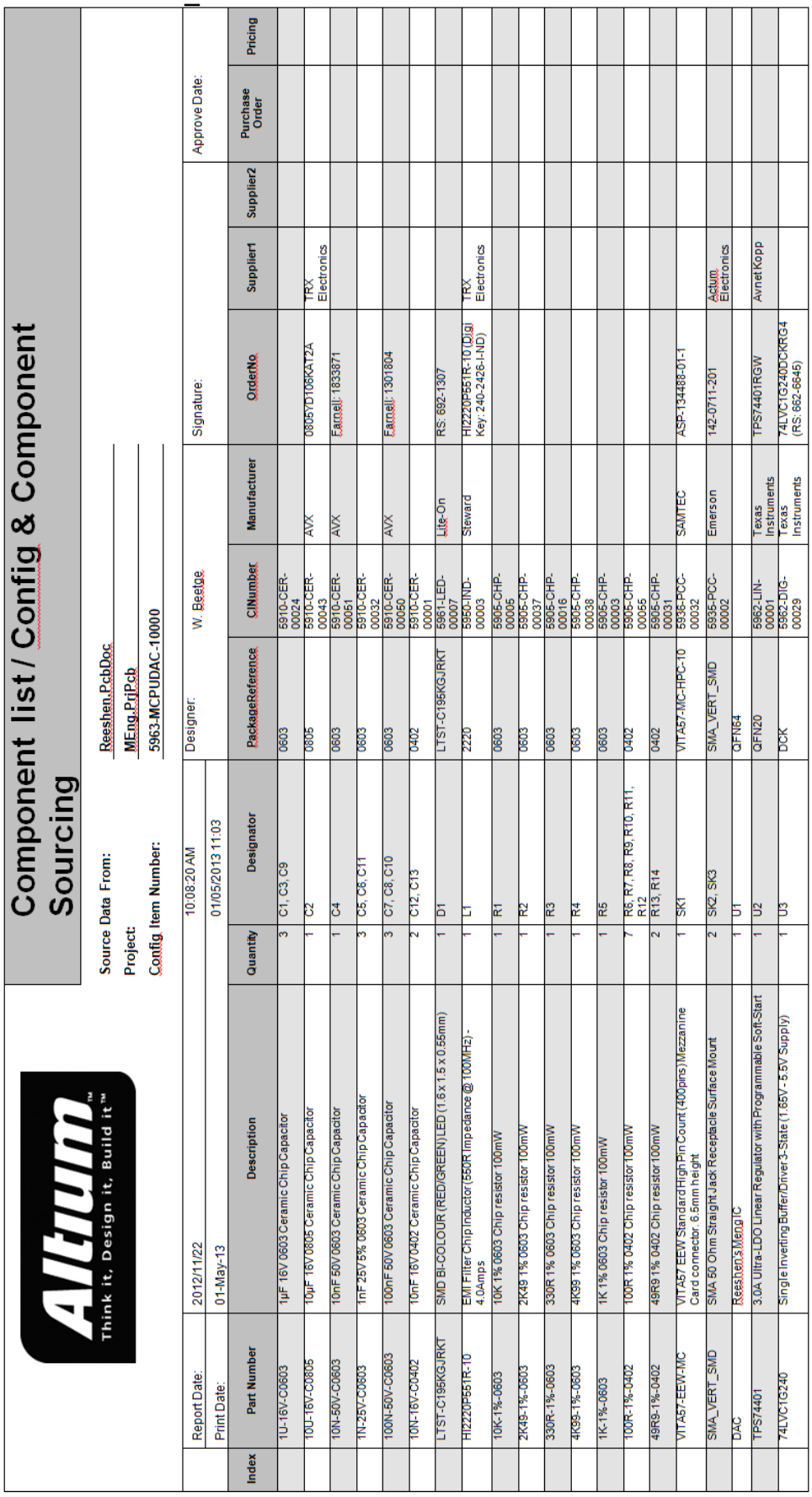


Fig. B.1. DAC FMC PCB Layout with top view shown.



Component list / Config & Component Sourcing

Source Data From: Reeshen.PcbDoc
Project: MEng.PrjPcb
Config Item Number: 5963-MCPUDAC-10000

Designer: W. Beetge
Signature:
Approve Date:

Report Date: 2012/11/22 10:08:20 AM
Print Date: 01-May-13 01/05/2013 11:03

Index	Part Number	Description	Quantity	Designator	PackageReference	CINumber	Manufacturer	OrderNo	Supplier1	Supplier2	Purchase Order	Pricing
	1U-16V-C0603	1uF 16V 0603 Ceramic Chip Capacitor	3	C1, C3, C9	0603	5910-CER-00024						
	10U-16V-C0805	10uF 16V 0805 Ceramic Chip Capacitor	1	C2	0805	5910-CER-00043	AVX	0805YD106KAT2A	TRX Electronics			
	10N-50V-C0603	10nF 50V 0603 Ceramic Chip Capacitor	1	C4	0603	5910-CER-00061	AVX	Farnell: 1833871				
	1N-25V-C0603	1nF 25V 5% 0603 Ceramic Chip Capacitor	3	C5, C6, C11	0603	5910-CER-00032						
	100N-50V-C0603	100nF 50V 0603 Ceramic Chip Capacitor	3	C7, C8, C10	0603	5910-CER-00050	AVX	Farnell: 1301804				
	10N-16V-C0402	10nF 16V 0402 Ceramic Chip Capacitor	2	C12, C13	0402	5910-CER-00001						
	LTST-C195KGJRKT	SMD BI-COLOUR (RED/GREEN) LED (1.6 x 1.5 x 0.55mm)	1	D1	LTST-C195KGJRKT	5961-LED-00007	Lite-On	RS: 692-1307				
	HI2220P561R-10	EMI Filter Chip Inductor (560R Impedance @ 100MHz) - 4.0Amps	1	L1	2220	5950-IND-00003	Steward	HI2220P561R-10 (Digi Key: 240-2426-1-ND)	TRX Electronics			
	10K-1%-0603	10K 1% 0603 Chip resistor 100mW	1	R1	0603	5905-CHP-00006						
	2K49-1%-0603	2K49 1% 0603 Chip resistor 100mW	1	R2	0603	5905-CHP-00037						
	330R-1%-0603	330R 1% 0603 Chip resistor 100mW	1	R3	0603	5905-CHP-00016						
	4K99-1%-0603	4K99 1% 0603 Chip resistor 100mW	1	R4	0603	5905-CHP-00038						
	1K-1%-0603	1K 1% 0603 Chip resistor 100mW	1	R5	0603	5905-CHP-00003						
	100R-1%-0402	100R 1% 0402 Chip resistor 100mW	7	R6, R7, R8, R9, R10, R11, R12	0402	5905-CHP-00055						
	49R9-1%-0402	49R9 1% 0402 Chip resistor 100mW	2	R13, R14	0402	5905-CHP-00031						
	VITA57-EEW-MC	VITA57 EEW Standard High Pin Count (400pins) Mezzanine Card connector. 6.5mm height	1	SK1	VITA57-MC-HPC-10	5936-PCC-00001	SAMTEC	ASP-134488-01-1				
	SMA_VERT_SMD	SMA 50 Ohm Straight Jack Receptacle Surface Mount	2	SK2, SK3	SMA_VERT_SMD	5935-PCC-00002	Emerson	142-0711-201	Actum Electronics			
	DAC	Reeshen's Mengl C	1	U1	QFN64							
	TPS74401	3.0A Ultra-LDO Linear Regulator with Programmable Soft-Start	1	U2	QFN20	5962-LIN-00001	Texas Instruments	TPS74401RGW	Avnet Kopp			
	74LVC1G240	Single Inverting Buffer/Driver 3-State (1.65V - 5.5V Supply)	1	U3	DCK	5962-DIG-00029	Texas Instruments	74LVC1G240DCKRG4 (RS: 662-6845)				

Fig. B.2. DAC FMC PCB Bill of materials

APPENDIX C: SCRIPT FOR MONTE CARLO SIMULATIONS

```
Netlist
// Library name: DAC
// Cell name: cmos_cs
// View name: schematic
T0 (net010 net11 0 0) nfet l=2u w=10u ad=5.251p as=5.251p pd=20.965u \
        ps=20.965u nf=1 ngcon=1 m=1 nrd=0.0442 nrs=0.0442 psti=1 pam1=0p \
        pam2=0p rf_rsub=1 dtemp=0
V1 (net11 0) vsource dc=350.0m type=dc
V0 (vdd! 0) vsource dc=1.2 type=dc
R0 (vdd! net010) resistor r=30.4K
```

```
Sim
// Spectre Analyses and Output Options Statements
```

```
// Output Options
  simOptions options
  //+       reltol = 1.00000000E-03
  //+       vabstol = 1.00000000E-06
  //+       iabstol = 1.00000000E-12
  //+       temp = 27
  //+       save = allpub
  //+       currents = selected
```

```
// Analyses
```

```
  //dc analysis
  dc1  dc  oppoint=logfile homotopy=all
```

```
  //dc mistmatch analysis
  //oprobe(mismatch at the output defined by this)
  //porti(Current through this point is output)
  //dcmm1  dcmatch   oprobe=T0 porti=1 version=1
```

```
  //montecarlo analysis
  mc1  montecarlo numruns=100 variations=mismatch savefamilyplots=yes{
    //child analysis
    dc2  dc  oppoint=logfile homotopy=all
  }
```

```
  // tran1 tran stop=1 errpreset=moderate
```

```
//Saves
  save T0:currents
```

```
Design in extremely sensitive to process variation!
```

```
Ids: 25 to 35 uA (process + mismatch variation)
Mean: 30.66e-6
Stddev: 3.309e-6
Result: 10.7% Terrible!!!!
```

```
Ids: 30.8 to 31.5 uA (mismatch variation)
Mean: 31.2e-6
Stddev: 188.6e-9
Result: 0.6% Nice!
```

APPENDIX D: BONDING DIAGRAM

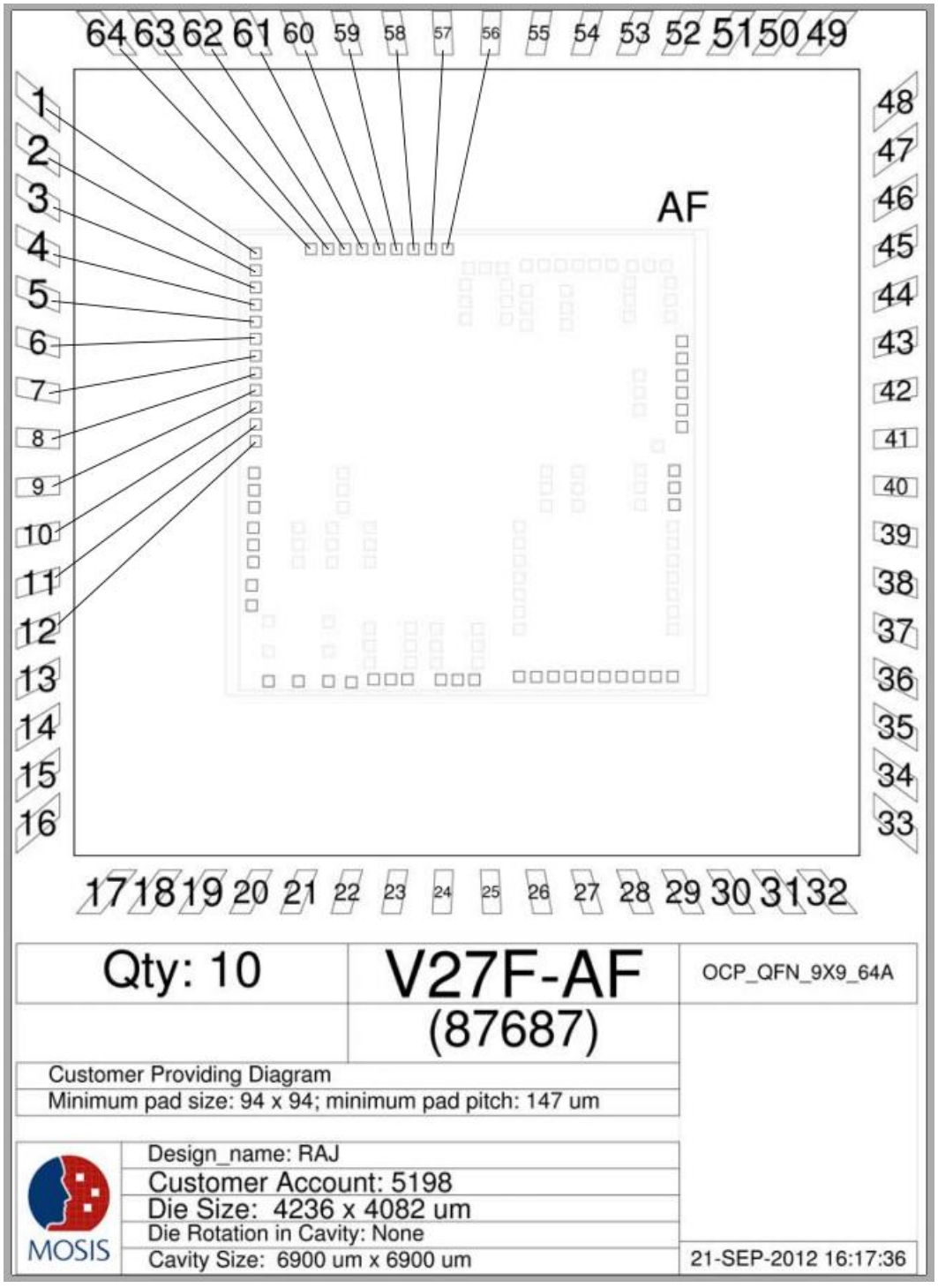


Fig. D.1. Bonding diagram of DAC IC for MPW run.