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DIE ONTWERP, SIMULASIE EN REALISERING VAN 'n MASKER-PROGRAMMEERBARE I^2L PLM

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Ja, Geed

deur

D.F. Frost

Voorgelê ter vervulling van die vereistes vir die graad

M.Sc. (Ing.) (Elektronies)

in die

Fakulteit van Ingenieurswese

Universiteit van Pretoria

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Die ontwerp, simulasie en realisering van 'n masker-programmeerbare I^2L PLM

deur

D.F. Frost

Leier : Prof. P. Rademeyer

Departement Elektroniese Ingenieurswese

M.Sc. (Ing.) (Elektronies)

Samevatting

'n Programmeerbare logiese matriks (PLM) wat gebruik maak van geïn=tegreerde injeksielogika (I^2L) is plaaslik ontwerp en vervaardig met behulp van 'n aangepaste standaard-bipolêre proses. Hierdie verhan=deling beskryf die ontwikkeling van dié element asook die proses wat gebruik is om dit te vervaardig.

Die konsep van die ontoegewyde stroombaan word bespreek en vergelyk met ander metodes van stroombaan-realisering in terme van ekonomiese fak=tore, met spesifieke verwysing na die Suid-Afrikaanse situasie. Verskil=lende tegnologieë word beskou en die redes vir die keuse van I^2L word uiteengesit. Statiese en dinamiese modelle van die I^2L-hek is ontwikkel en deeglik ondersoek op teoretiese en eksperimentele vlak met behulp van twee doelgemaakte geïntegreerde stroombane. Hieruit word toepaslike uit=legreëls en prosesspesifikasies bepaal. Hierdie inligting is gebruik om 'n PLM met 16 ingange, agt uitgange en 80 produk-terme te ontwerp en te vervaardig. Hierdie stroombaan is in staat tot 1 MHz-werking,

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met 'n drywingsverkwisting van 44 mW. Elf skywe is geprosesseer en 'n statistiese analise van die opbrengs is gemaak met behulp van 'n rekenaarprogram. Hierdie analise dui op 'n dominante opbrengs-verminderende meganisme in die produksietoleransie in epitaksiale dikte. Voorstelle om die ontwerp en prosessering te verbeter is gemaak op grond van die resultate behaal.

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The design, simulation and realization of a mask programmable I^2L PLA

by

D.F. Frost

Leader : Prof. P. Rademeyer

Department of Electronic Engineering

M.Sc. (Eng.) (Electronic)

Synopsis

A programmable logic array (PLA) using integrated injection logic (I^2L) has been designed and manufactured locally, using a modified version of a standard bipolar process. This thesis describes the development of this device and also of the process used to manufac= ture it.

The uncommitted integrated circuit concept is examined and com= pared with other methods of circuit realization in terms of economic factors, with particular reference to the South African situation. Various technologies are examined and the reasons for choosing I^2L clearly stated. Static and dynamic models of the I^2L gate are developed and thoroughly investigated, both theoretically and experimentally by means of two special-purpose integrated circuits. From this investi= gation, suitable layout rules and process specifications are deter= mined. These are used to design and manufacture a PLA with 16 inputs, 8 outputs and 80 product terms. This circuit is capable of 1 MHz operation at a power consumption of 44 mW. Eleven wafers were produced

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and a statistical analysis of yield was made by means of a com= puter program. This indicates a dominant yield reducing mechanism in the production tolerance in epitaxial layer thickness. Sugges= tions for improving the design and processing of the circuit are made on the basis of the results obtained.

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10. Mrs S. Wittstock of the IC production facility for producing the three circuits described in this report and carrying out the necessary processing experiments.
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CHAPTER 1

1. INTRODUCTION AND STATEMENT OF OBJECTIVES

The study arose from the need for a locally-produced uncommitted digital integrated circuit. Such a circuit would complement the existing UC1 circuit which is oriented more towards analog appli= cations. It would be used to replace random logic circuits built with large numbers of SSI devices, in cases where the additional flexibility and sophistication of a microprocessor was not war= ranted. Electrically, the specification was for a device optimized for low-speed, low-power applications. A maximum clock frequency of 1 MHz was specified, with power consumption kept to a minimum. Full TTL compatability was also required.

The first objective was to decide on the precise form which the circuit should take (Chapter 3). It was originally envisaged that the device would be designed using integrated injection logic gates designed by other researchers of the National Electrical Engineering Research Institute[10]. This soon proved technically not feasible and the second objective was then to analyse all other process-compatible structures which could conceivably be used (Chapter 4). This showed that an improved version of I^2L with specific charac= teristics was required. The third and fourth objectives were re= spectively the development of such structures from basic principles, and the design of the final circuit using these devices (Chapter 5). Interface circuits were also required.

The fifth and final goal was to produce a limited number of samples and evaluate their performance, both electrically and in

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CHAPTER 2

2. THE MICROELECTRONICS INDUSTRY IN SOUTH AFRICA

This thesis describes the development of a general-purpose digital IC intended for production by the South African microelectronics indus= try. A brief review of the history, present state of development and future prospects of this industry is therefore pertinent, and forms the subject of this chapter. The role that the PLA is intended to play within the South African electronics industry will be described in Chap= ter 3.

2.1 Historical Developments

The early development of each of the 3 important microelectronic technologies will be described in turn.

2.1.1 Thin-film microcircuits

Briefly, thin-film technology consists in the construction of a circuit by the deposition of layers of conductive, resis= tive or dielectric material on a glass or ceramic substrate whereby conductors, resistors or capacitors are respectively formed. The materials are deposited by means of evaporation or R.F. sputtering in a vacuum chamber. A layer is deposited over the whole substrate surface and then selectively etched to produce the required pattern for component formation. Low-value inductors may be produced by means of conductor spirals. All other components, such as transistors, monolithic integra= ted circuits and high-value resistors, conductors and capacitors, may be added discretely by soldering them into position on the substrate. Thin-film circuits generally have areas of several cm^2. The main applications lie in the field of high-frequency

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devices with close tolerances, such as microwave cir= cuits (e.g. amplifiers, filters, directional couplers) and surface acoustic wave devices. Thin-film circuits were the first to be produced in South Africa when in 1965 the Council for Scientific and Industrial Research (CSIR) began work in this field[1]. The first all-South African microcircuit was produced in 1967. Today the CSIR still produces thin-film circuits using the evaporation technique. The Electrical En= gineering Department of the Rand Afrikaans University has con= ducted research in this field since 1971, using R.F. sput= tering techniques. (Sputtering equipment is fully automated).

2.1.2 Thick-film microcircuits

In thick-film technology components are formed by printing on a substrate with special-purpose inks by means of the silk screen printing process. Conductors, resistors and capacitors may be formed in this way, and additional components mounted as in the case of thin-film circuits. After printing the sub= strates are baked in a furnace to harden the printed layers. Thick-film circuits are more suitable for mass-production than thin-film circuits but cannot be as accurately manufactured and are best suited to low-frequency applications. Thick-film research has been conducted at the University of Pretoria (UP) since 1971[1]. Several hybrid circuits have been produced, such as a diode matrix for example.

2.1.3 Monolithic integrated circuits

Monolithic integrated circuit technology is the most mass-pro= duction orientated of all technologies. This is so because of

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the high capital outlay for a monolithic process and the low unit cost of devices produced (primarily determined by testing and packaging costs). Thus the total unit cost will fall rapidly with increasing production. Whereas thin- and thick-film technologies consist in depositing layers on a surface, monolithic circuits are produced by the formation of regions within a solid crystal of semiconductor material, usually silicon. The process may involve some or all of the following steps: epitaxial growth, deposition of dopants, diffusion, oxide growth, etching, and deposition of conductive or resistive materials. Dimensions are much smaller than in the case of the other technologies, and therefore packing den= sity is much higher. The small dimensions imply the need for much more accurate mask-making, with the result that more so= phisticated equipment such as pattern generators and electron-beam writing apparatus may be used. The epitaxial growth and diffusion steps require epitaxial reactors and diffusion furnaces with very accurate temperature control. Automatic test equipment is necessary to rapidly test the large volume of ICs produced. Because of these factors the capital invest= ment required to begin production is high (e.g. the production facility of the CSIR has a capacity of 100 wafers per week[1] (approximately 30 000 units) and represents an investment of approximately R1,5 M). For this reason, monolithic technology has been a comparative late-comer in South Africa, where the domestic market is small. In 1973 the first wholly South African integrated circuit was produced by the CSIR. Since then, both the CSIR and UP have conducted research and development in this

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field, the former concentrating on bipolar technology and the latter on MOS devices. The CSIR has produced some devices for industry and for military applications, and in 1975 it began producing UC1, a so-called 'uncom= mitted' integrated circuit. This device contains several components, e.g. resistors, pnp and npn transistors, power transistors and small capacitors, which may be connec= ted to form the required circuit. This personalization process takes place in the final mask stage of aluminium etching. Thus only one mask step is required to personalize the circuit - all other steps being standard. This is an effective way of reducing the high unit cost of small volume production in a developing country such as South Africa.

2.2 The State of Microelectronics in South Africa today

The present state of research, development and production in the field of microelectronics in South Africa will now be reviewed. The activities of each of the relevant institutions will be described in turn.

2.2.1 The University of Pretoria

The Department of Electronic Engineering of the University of Pretoria is active in both monolithic and film technology, and has created an interdisciplinary Institute for Micro= structures, in conjunction with the Department of Physics. The main interest lies in the field of MOS and related technologies, i.e. charge-coupled devices (CCDs) and surface-acoustic-wave devices (SAWs). A p-channel MOS technology has been success= fully implemented in small-scale integration (SSI) and medium-scale integration (MSI) devices for research purposes. Two

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types of metal oxide semiconductor (MOS) technology are being developed; one where the gate electrode is formed by Al deposition and another where it is formed by a polycrystalline silicon (polysilicon) deposition. A n-MOS process involving two polysilicon deposition steps is also under development. Surface type CCDs, suitable for image processing applications such as delay lines and transversal filters, are being developed. An analysis is being made of the high-frequency properties of p-MOS tran= sistors for use in distributed R-C filters. While most of the research work undertaken is concerned with MOS devices, bipolar diode matrices have also been developed and the tech= nology exists to manufacture bipolar transistors, both pnp and npn. In the field of processing technology, the growth of epitaxial silicon and polysilicon layers is being investi= gated. The Department has some powerful measuring equipment at its disposal, such as a scanning electron microscope, trans= mission electron microscope and an Auger spectroscope with which diffusion profiling is done, using the back-scattering technique. An electron-beam writing apparatus has recently been acquired, with which sub-micron line-width MOS structures are being developed for use in RAMs, ROMs and SAW devices. This is an important development as packing density is ulti= mately limited by the resolution obtainable with masks pro= duced by conventional photolithographic processes. The reso= lution is limited by the wavelength of the light used (about 0,7 μm). The use of electrons to produce the mask, or to di= rectly expose the photo-resist on the silicon surface, enables

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much smaller structures to be made. The Department has been active for some time in the field of thick-film research and development (R and D). This is applied R and D, and several circuits have been de= veloped for industry. Some research into thin-film technology is also being conducted.

2.2.2 The Council for Scientific and Industrial Research

The National Electrical Engineering Research Institute of the CSIR has purchased a proprietary bipolar process (the Plessey Process 1) for use in its production faci= lity. This is a general-purpose process suitable for bi= polar analog or digital circuits. A number of circuits for industry, including both 'dedicated' designs and de= signs based on the UC1 concept, are currently under deve= lopment. The CSIR is also offering a UC1 Designer's Kit to industry. This kit consists of a circuit designer's handbook[8], and a number of breadboard components as well as sheets of rubylith on which the Al mask may be designed, and is intended to help engineers with no microelectronics experience to design their own ICs using the components of UC1. This system can help the user to minimize the design costs involved in producing ICs in small quantities. In addition to the production facility, equipment exists for producing circuits for research purposes. There is a definite need for separate processing of research and production circuits, as the former often require special non-standard

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processing which disrupts the flow of a production line using a standard process. The result of such dis=ruptions is reduced yield and increased turn-around time on production circuits. At present research is being conducted in the following areas:

1. I^2L technology: A bipolar process optimized for I^2L production has been developed. Further research is being conducted into optimizing the process for high yield.
2. Charge-coupled devices and MOS transistors.
3. The development of an improved bipolar process for use in the production facility.

The CSIR is able to design and produce microstrip elements in thin-film technology[4]. Circuits which have been produced include filters, directional couplers and amplifiers. Computer programs have been developed to enable microstrip devices to be designed quickly. Apart from pro=cessing and testing equipment, some sophisticated mask-making apparatus is available. A computer-aided design system (CALMA) is available for designing monolithic or film micro=circuits and printed circuit boards quickly and efficiently. The output from the CALMA system is stored on magnetic tape and used to program an Electromask pattern generator and step-and-re=peat camera which produces the final masks on glass plates. This system is capable of producing masks of a very high quality (greatly superior to the rubylith cut-and-peel methods used previously).

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2.2.3 The Rand Afrikaans University

The light current section of the Department of Electri= cal Engineering at the Rand Afrikaans University is at present conducting the following research projects in the field of microelectronics.

1. Investigation of tantalum thin-film technology. A wide-band amplifier has been made using this technique.
2. The design of ultrasonic compression and decom= pression filters. (Surface acoustic wave devices).
3. The realization of field effect transistors in Gallium Arsenide (GaAs) technology.
4. The design and construction of a deep channel charge-coupled device (CCD).
5. The design and construction of high efficiency solar cells in silicon technology. With the increasing shortage of energy sources the use of solar power can be expected to increase, especially in countries with favourable climates, such as South Africa.
6. The design of a power switch. A conventional SCR (silicon controlled rectifier) suffers from the dis= advantage that it cannot be turned off, other than by interrupting the primary (anode) current. The power switch may be turned on or off by the application of currents to either of two gate electrodes, making it a much more easily controllable device than an SCR. Prototypes capable of handling 50 A at 300 V have been produced.

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7. Improvement of I^2L performance by means of ion implantation in an I^2L transistor produced with a standard bipolar process the concentration gradient in the base is not optimized for a high upward gain. The gain may therefore be improved if this profile is modified by means of ion implantation, at the expense of one extra non-standard process step.

The activities of this Department thus cover a variety of technologies, and the emphasis is on the development of special structures and processes.

2.2.4 Other Universities

Because of the high costs involved in producing micro= circuits, relatively few electrical engineering depart= ments are prepared to undertake research in this field. Apart from the two universities already mentioned, a li= mited amount of research is being undertaken at the fol= lowing universities.

1. University of Natal: Ultra-high vacuum studies are being made of clean metal-insulator-semiconductor (MIS) surfaces.
2. University of Stellenbosch: Research and development into thick-film hybrid microcircuits and thin-film cir= cuits for microwave frequencies.

2.2.5 Siemens SA

This company, while not actually producing microcircuits in South Africa, does conduct the operations of wafer scribing, breaking, bonding, encapsulation and testing locally. Wafers are imported form the parent company in the

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Federal German Republic. Encapsulation facilities are also available to local producers of ICs. Encapsulation is by means of plastic injection moulding.

2.3 Overview

To summarize, the following points are worth enumerating.

2.3.1 The South African microelectronics industry is still a young one (12 years old).

2.3.2 Until recently emphasis was placed on research rather than on the development of devices suitable for production, as fa= cilities for large-scale production were simply not available.

2.3.3 Microelectronics is a mass-production orientated industry. This is particularly true of monolithic technology. A high capital outlay is necessary to begin production and this must be recouped from sales over a period of time. The larger the volume produced, the smaller the unit price need be to achieve this. Production volumes of the major producers in the highly industrialized countries are enormous and a South African indus= try producing solely for the domestic market would not be able to produce large-volume components (e.g. TTL components, opera= tional amplifiers, microprocessors) at competitive prices, as long as imported items are freely available. For this reason a local microelectronics industry should be geared firstly to the production of specialized, made-to-order circuits for in= dustry which would not otherwise be available. Because of the small-volume production, the unit cost would be high, but con= ceivably cheaper than a discrete component solution. The pro= duction facility of the CSIR, which is also of strategic

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importance (see 2.3.5), is intended to provide such a service to industry on a non-profit-making basis.

2.3.4 Microelectronics is an interdisciplinary science requiring a nucleus of highly trained technologists and a larger quan= tity of skilled and semi-skilled labour. Acquiring staff with the necessary training and expertise locally may be difficult and importation of skilled know-how the only alter= native. However, there are strong arguments in favour of introducing advanced technologies into South Africa, either by importing skilled technologists or (preferably) by de= veloping local expertise. Already the two universities which are actively engaged in microelectronics research have built up a considerable amount of know-how of most aspects of the technology (see 2.2.1 and 2.2.3) and can play a vital role in the training of technologists for the future[6].

2.3.5 It has been estimated[7] that the South African electronics industry is currently worth about R1 billion per annum, and is growing at a rate of 20% per annum. Microelectronic compo= nents must account for a considerable part of this total, and are thus of considerable strategic importance to the country (particularly in the context of military equipment). At pre= sent South Africa is almost entirely dependent on overseas sup= plies for its microelectronic component requirements. Seen against this background it seems not only desirable but imperative that South Africa develop a greater measure of self-sufficiency in the production of microelectronic components.

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CHAPTER 3

3. THE CONCEPT OF THE UNCOMMITTED INTEGRATED CIRCUIT

In the preceding chapter the concept of the uncommitted integrated cir= cuit was introduced and its ability to cut the cost of small volume IC production was mentioned. The uncommitted circuit in its various forms will now be examined in detail, with particular reference to the South African context.

3.1 Advantages and Disadvantages of Uncommitted Circuits

Fig. 3.1[10] shows the flow chart of a typical bipolar process (Plessey Process 1). This is a 23-step process and typical steps include cleaning, oxide growth, photo-engraving, deposition and diffusion of impurities, epitaxial growth and aluminium deposition. Masks are required to de= fine the following regions by means of photo-engraving.

1. Buried n+ layer for collectors.
2. P+ isolation region.
3. P base regions.
4. N+ emitter regions.
5. Contact windows.
6. Contact pattern.
7. Passivation.

The cost of mask design and manufacture is a constant overhead, which must be shared amongst the total number of circuits produced. The larger the volume, the smaller its effect on the per circuit cost. Furthermore, large volume production ensures that the maximum possi= ble number of wafers is processed at one time. Processing is complex and expensive and an IC production line is most efficient when it has a full, constant work load.

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FLOW DIAGRAM OF THE STANDARD BIPOLAR PROCESS

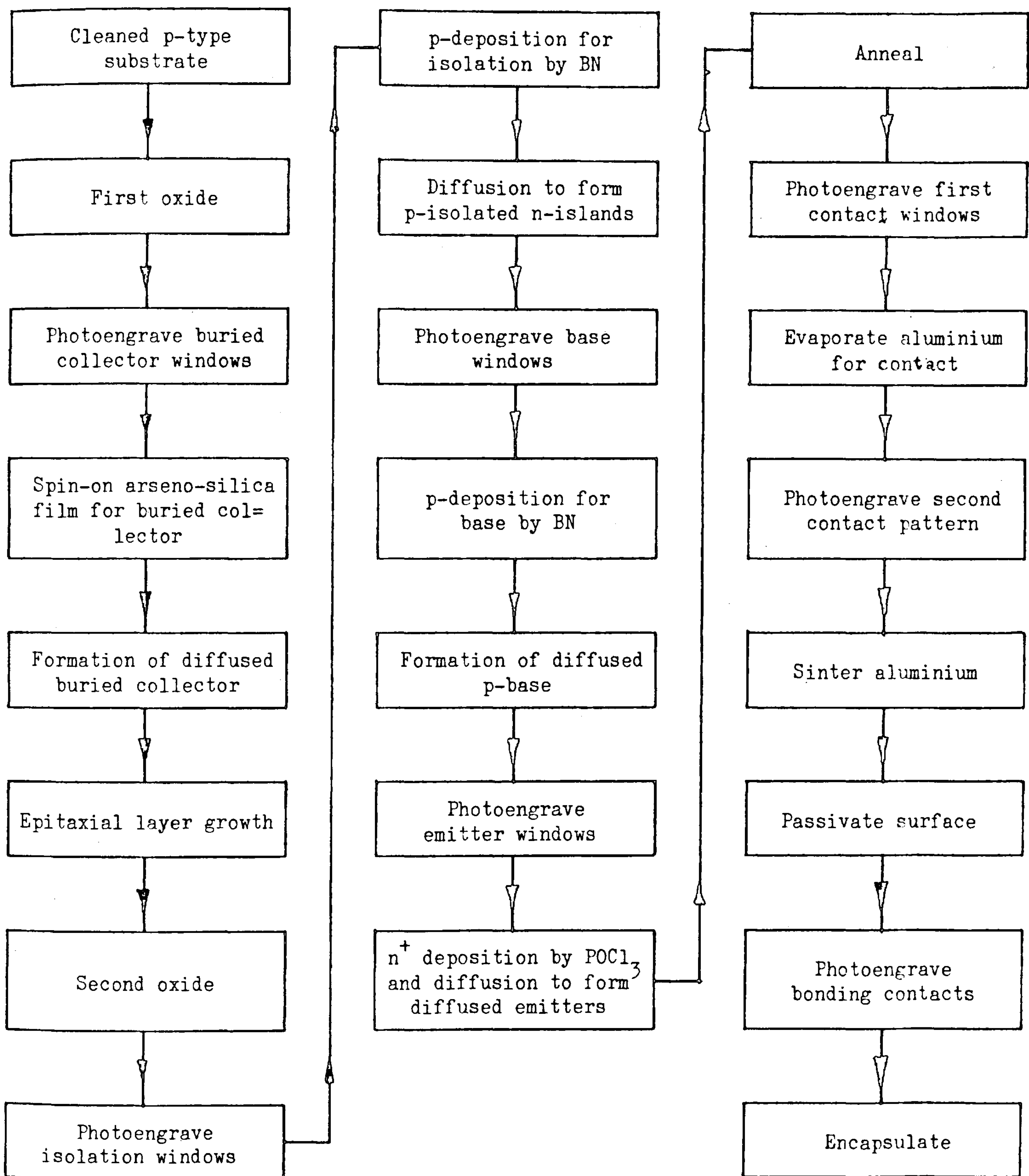

Fig. 3.1

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In the light of these remarks the uncommitted circuit (UC) has the following advantages over single-purpose 'dedicated' designs.

1. The component layout is designed once only and so six of the seven masks are standard for a number of different circuits (the exception being the contact pattern mask). Thus the bulk of the mask design and production costs are shared amongst a larger volume of circuits.
2. Eighteen of the twenty-three steps in the process may be completed in advance and the wafers stored until needed. They are then cleaned and the contact pattern mask is used to etch the aluminium. After passivation they are tested, scribed and encapsulated, and are then ready for use. Thus a factory may produce circuits at a more constant tempo than that determined solely by immediate needs. The turn-around time for a design is also greatly reduced.
3. Because designing a circuit with a UC consists only in designing the contact pattern for interconnecting compo= nents, relatively inexperienced engineers can design inte= grated circuits for their own needs. This involves the client in the design process, which can lead to a more sa= tisfactory final product and will further reduce design costs.
4. In a low-volume environment such as South Africa the UC approach places 'custom' integrated circuits within the reach of a wider range of potential users.

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The CSIR has exploited the UC approach by means of the UC1 Designer's Kit (see Chapter 2). The philosophy behind the Kit is to enable electrical engineers with no IC design experience to design their own circuits with a minimum of assistance. A de= scription of IC design techniques is given in the Designer's Hand= book[8] and several components are supplied so that circuits may be tested and debugged before the mask is laid out.

3.2 Uncommitted Digital Integrated Circuits

A major disadvantage of the UC approach is the poor usage of silicon 'real estate', i.e. only a small number of the components available are used in a particular design. In the case of analog circuits a trade-off exists between the variety of components supplied on a UC and the area usage. If a wide range of components is supplied, a wider range of circuits may be implemented, but these will need to be simpler, as fewer components of a given type will be available. Many components will remain unused. On the other hand, a small range of components means higher packing densities for certain types of cir= cuits. This relationship does not really hold for digital circuits, where the basic functional unit is not a component (resistor, capa= citor or transistor) but a gate of some sort. Thus, in the case of a digital UC only a limited range of components need to be provided (those needed to produce the gate). Although various types of gates are possible, the logic equations governing the circuit can always be rewritten in a suitable form for implementation with the gates avai= lable. It would appear, therefore, that the basic form of uncommitted

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circuits intended exclusively for digital applications would dif= fer somewhat from that of UCs intended primarily for implementing analog functions. Furthermore, attempts to produce complex digital circuits by means of the latter would result in low packing densities and poor component usage. This thesis describes the development of an uncommitted digital circuit, suitable for production by the CSIR's production facility, using Process 1. This is intended to supplement the analog-orientated UC1 circuit already in use.

3.3 Alternative Methods of Realizing Digital Circuits

Digital UCs represent only one of several methods of implementing di= gital functions. Ultimately, the method chosen will depend on a num= ber of factors such as cost, complexity, packing density, reliability, flexibility, power consumption and speed. A circuit may be construc= ted using one or a combination of the following methods.

1. Random logic using standard SSI and MSI circuits

   Traditionally digital circuits have been designed in this way and it still remains the most popular single method[11]. Circuits are normally implemented in transistor-transistor logic (TTL) or comple= mentary metal-oxide semiconductor (CMOS) technology. Other logic families such as diode-transistor logic (DTL), Schottky TTL and low-power TTL are also used. A large number of functional blocks are available today, such as gates (of various types), flip-flops, resistors, counters, dividers, arithmetic logic units, display drivers and interface circuits. This wide range of modules enables the designer to construct digital circuits quickly, using off-the-shelf components. Components are mounted on a printed circuit board or wire-wrap board. The method suffers from several disadvantages

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when compared to more highly integrated forms of logic. Firstly, the cost per gate is high, especially for SSI de= vices. For example, a TTL quad 2-input NAND gate (SN 7400) currently costs about 20c, or 5c/gate. A 2-input gate has a 4-line truth table which, if implemented by means of a ROM, would require 4 bits of storage. The current price of a 8-kilo= bit PROM is about R45, or 0,56c/bit. Thus, to implement the quad 2-input gate would require 4 x 4 = 16 bits, costing 16 x 0,56 = 9c. A PLA solution would be considerably cheaper (see section 3.3 (3)). The reason for this high cost per unit is the cost of bonding and packaging. Each SSI device requires a 14- or 16-pin package, while an entire 8k PROM can be fitted into a 24-pin package. A random logic solution is even more expensive than this example shows - to the basic cost of devices must be added the cost of printed circuit or wire-wrap boards, edge connectors, IC sockets and assembly and wiring costs. The finished product is bulky and potentially less reliable than an integrated component because of the large number of soldered or wrapped connections. In short, random logic is today only cost effective for relatively simple cir= cuits produced in small quantities (less than 10 units). An excep= tion to this rule is when random logic has superior electrical cha= racteristics to the LSI alternatives. For example, the high-speed logic families such as emitter coupled logic (ECL), TTL and Schottky TTL are capable of speeds unattainable by most LSI circuits. The li= miting factor here is the chip-dissipation which restricts the ope= rating power of a circuit, and therefore its speed.

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2. Microprocessors

As the price of processor and memory chips continues to fall, this becomes an increasingly attractive method of implementing larger digital systems. Digital circuits may be divided into two classes, namely combinational and sequential. The former are characterized by the fact that their present-state outputs are de= pendent only on the present-state inputs. In the case of the latter, previous inputs also determine the present state outputs; that is, the circuit contains some form of memory element such as a register or latch. The applications of combinational and se= quential circuits are not distinct; in fact it is possible to implement <u>any</u> digital function either combinationally or sequen= tially. Consider the following example (see Fig. 3.2): the equa= tion

$$Q = \overline{\overline{I_1} I_2 I_3}$$

must be implemented. The truth table and combinational solution are shown in Fig. 3.2(a). Note that there are eight possible com= binations of inputs and outputs, or states. Consider the case where the input variable $I_1 I_2 I_3$ may only assume one of three values: 001, 010 and 011, and only in that sequence. There are now only three states of interest, and each can only be reached from a certain previous state. The state diagram and sequential realization are shown in Fig. 3.2(b). In this simple example the combinational so= lution is obviously cheaper, but this is not always the case. When a large number of inputs are involved but only a few states are permissible, then the sequential solution will be the best

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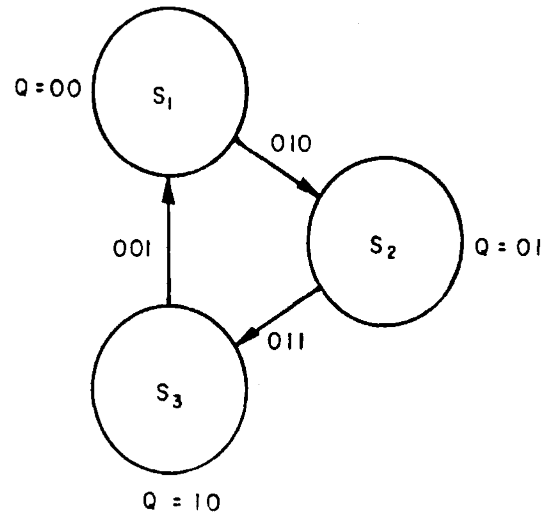
$$Q = \overline{\overline{I_1 . I_2} . I_3}$$



I_1	I_2	I_3	Q
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	0	1	1

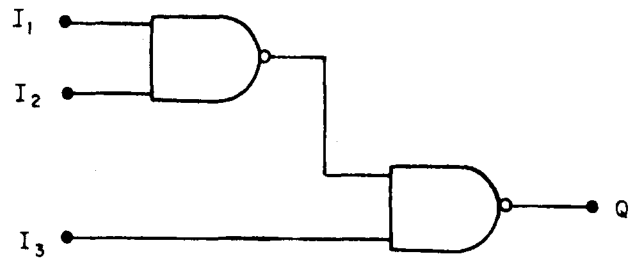


Fig.3.2(a) Combinational realization

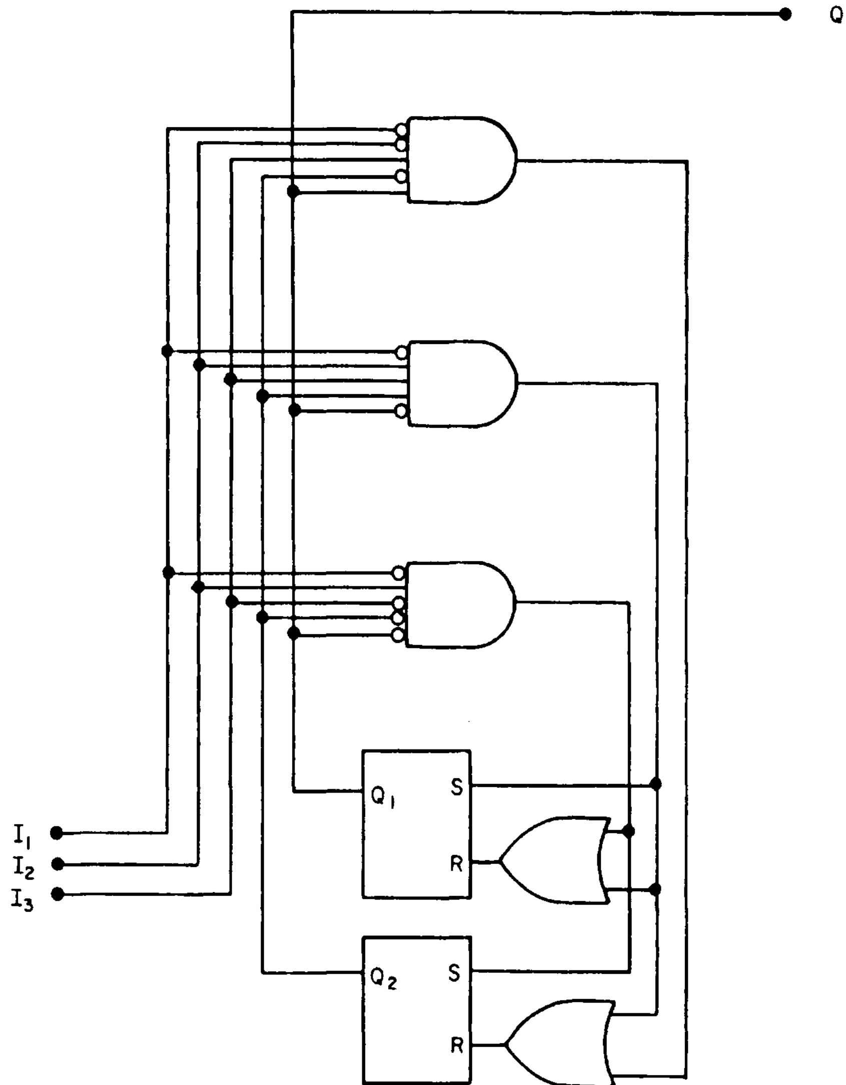


Fig.3.2(b) Sequential realization

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choice. This is analogous to the case of adding two numbers together. It is far simpler to remember the algorithm for ad=ding any two numbers (which describes the sequence of operations necessary) than to attempt to remember the sums of all possible combinations of two random numbers. A microprocessor is a se=quential machine in which the algorithm (equivalent to the state diagram) is defined by a software program. It may therefore be described as a highly modifiable sequential circuit, which can be used for tasks of a wide range of complexities. It is diffi=cult to define the level of complexity at which a microprocessor begins to out-perform a more combinational circuit (such as would be realized with random logic), but the following factors are per=tinent.

(a) Microprocessors have an advantage in applications where flexibility is important (the program is easier to alter than a P.C. board would be).

(b) The cost of a microprocessor system is largely inde=pendent of the complexity of the program it has to im=plement, within the limitations of its memory capacity. Thus it can be expanded at little extra cost.

(c) On the other hand, a microprocessor system can still represent a considerable capital outlay if it includes peripherals and a lot of software (e.g. assemblers, editors).

(d) Programming expertise must be acquired. This is less of a problem if a number of processor systems are de=veloped together as this overhead can be written off pro=portionally amongst them.

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(e) Because of their sequential nature, micropropro= cessors tend to be slow. Typical cycle times are of the order of 0,5 μs.

It would appear from the foregoing that microprocessors are probably still too expensive or too slow for many simpler circuits and subsystems, and will probably remain so for some time to come. To use a microprocessor as a code converter, for example, would represent a tremendous technological overkill. However, to im= plement such a device in random logic might also be undesirable, for reasons already discussed. Assuming that no standard LSI part is available which suits the application, one must think in terms of some form of 'custom' circuit.

3. Customized Integrated Circuits

There are three possibilities:

(a) A 'dedicated' integrated circuit

The merits and demerits of dedicated ICs have already been discussed. They generally offer the most elegant solution to a problem, with optimized components and good layout. For reasons discussed they are only economical in large vo= lumes. Hill and Peterson[12] analyse the cost of producing a custom integrated circuit in the following manner: a part of the design, layout and maskmaking costs may be considered independent of the complexity of the circuit produced and will be represented by a constant A_c. The remainder of the costs may be considered proportional to the number of gates g in the circuit, so that the total design cost is:

$$\phi_d = A_c + B_c g. \qquad 3.1$$

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The values of A_c and B_c depend on the particu= lar economic situation. The per unit production costs are considered to follow a similar law, and are given by

$$\phi_p = C_c + D_c g. \qquad 3.2$$

The total cost of producing p circuits is

$$\phi_{tc} = \phi_p + \phi_d = A_c + B_c g + p\,(C_c + D_c g)$$

and the per unit cost is

$$\phi_{tc}/p = (A_c + B_c g)/p + C_c + D_c g. \qquad 3.3$$

Equation 3.3 is valid for a standard MSI or LSI part as well as for a custom circuit. Thus the ratio be= tween the per unit price of a custom component and a standard component of the same complexity is:

$$R = \frac{\phi_{tc}\, p_s}{p_c\, \phi_{ts}} = \{(A_c + B_c g)/p_c + C_c + D_c g\}/\{(A_s + B_s g)/p_s + C_s + D_s g\} \qquad 3.4$$

For a standard component p_s is usually suffi= ciently large for 3.4 to be reduced to

$$R = \{(A_c + B_c g)/p_c + C_c + D_c g\}/\{(C_s + D_s g\} \qquad 3.5$$

As p_c tends to infinity, so R tends toward $(C_c + D_c g)/(C_s + D_s g)$. This term will generally be

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greater than unity because per unit production costs are larger for small volumes. Thus the custom circuit will always be more expensive than an equivalent standard component. However, if the standard component cannot perform the function fully, external gates may be necessary. The standard MSI or LSI circuit plus gates form a 'hybrid' solution, with a per unit cost of

$$\emptyset_{ts}/p_s = C_s + D_s g + \emptyset_w + \emptyset_g$$

where $\emptyset_w$ and $\emptyset_g$ are respectively the per unit costs of wiring and of the gates needed ($\emptyset_w$ can easily be greater than $\emptyset_g$). Equation 3.5 now becomes

$$R = \{(A_c + B_c g)/p_c + C_c + D_c g\}/\{C_s + D_s g + \emptyset_w + \emptyset_g\}$$

The break-point occurs when R = 1, or

$$(A_c + B_c g)/p_c + C_c + D_c g = C_s + D_s g + \emptyset_w + \emptyset_g$$

$$\therefore p_c = (A_c + B_c g)/\{(C_s + D_s g) - (C_c + D_c g) + \emptyset_w + \emptyset_g\}$$

$$= (A_c + B_c g)/\{(\emptyset_w + \emptyset_g) - (C_c + D_c g - (C_s + D_s g))\} \qquad 3.6$$

It is desirable that the break-point occurs at a low value of p_c (see Fig. 3.3). This will be the case when the extra costs accruing from the gating network are

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much larger than the difference in production costs between the custom and the standard circuits. The values of the various cost parameters must be determined for each design in order to calculate the break-point. However, it has been estimated[11] in the U.S.A. that custom circuits are cost-effec= tive in quantities greater than 2 000, or 20 to 50 wafers. In South Africa the CSIR has the capability to produce such devices to order.

(b) A gate array

Several manufacturers are today producing devices of this type. A gate array is a digital UC containing a large number of uncommitted logic gates of a certain type. As in the case of UC1 the device is personalized by means of the aluminium contact pattern mask. By in= terconnecting the gates to form flip-flops and registers, it is also possible to realize sequential circuits. A typical example of a gate array is the Uncommitted Logic Array (ULA) offered by Ferranti[13]. Collector diffusion isolation (CDI) technology is used and the ULA consists of 187 3-input NOR gates in a 11 x 17 array (see Fig. 3.4(b)). Although all the components needed for a gate are grouped into a cell, they are not interconnected. This enables those components (4 resistors and 3 npn transistors) to be used individually to realize simple analog circuits. In CDI technology a deep n+ isolation

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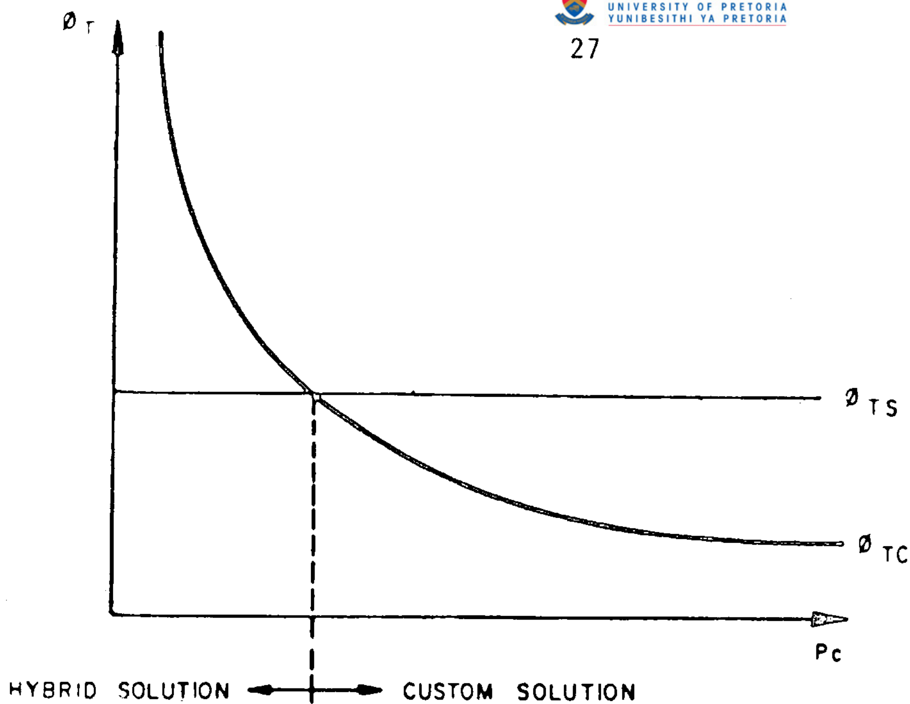

Fig.3.3 Hybrid solution/custom solution breakpoint

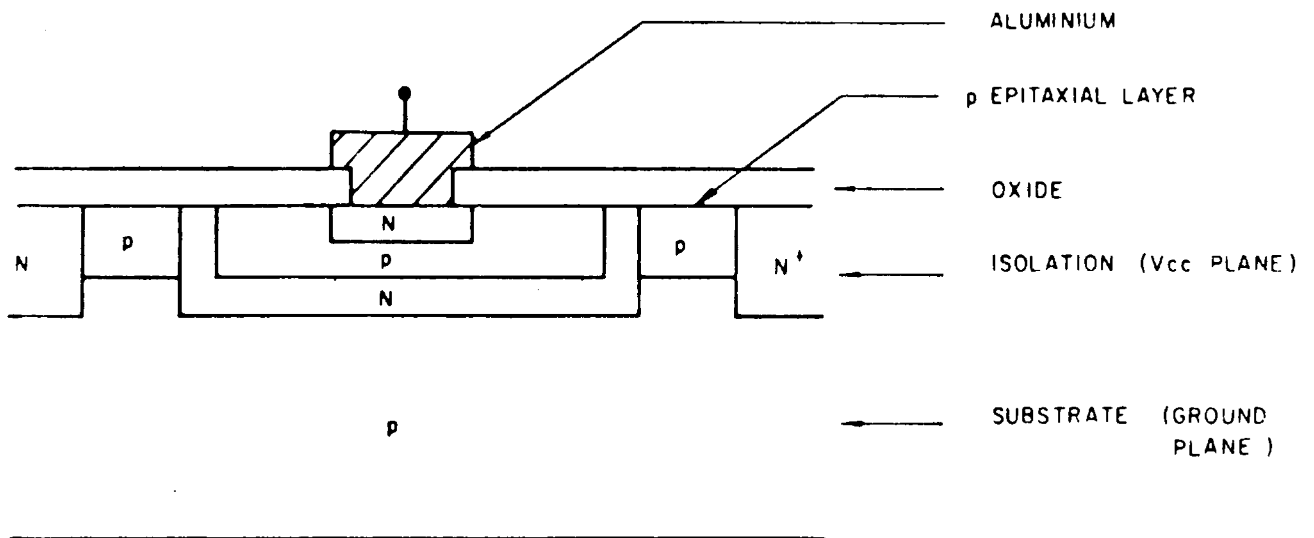

Fig.3.4(a) CDI structure

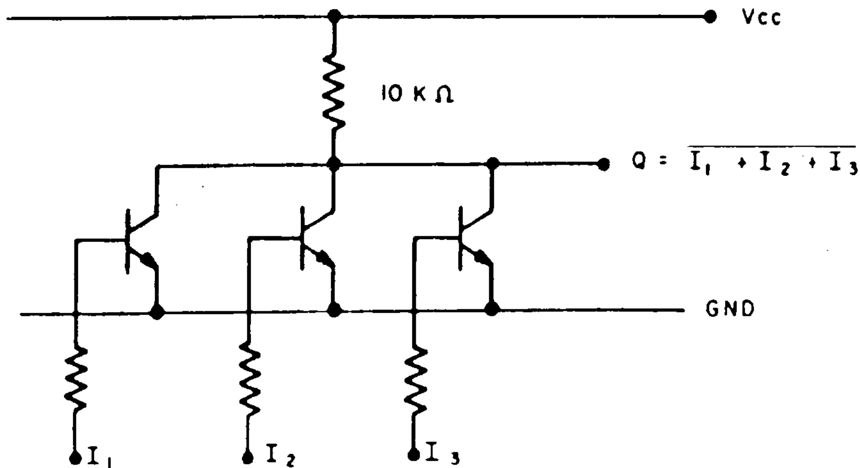

Fig.3.4(b) 3-input NOR gate

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diffusion serves as a V_{cc} grid to carry the positive supply voltage all over the chip. The p-substrate forms a ground plane (see Fig. 3.4(a)). This fact makes the interconnection problem somewhat simpler. This is particularly important in a non-optimized lay= out. Other similar products are the XR400 Master Chip[14] from Exar Integrated Systems, Inc., and the SWAP (Stewart-Warner Array Programming[15]) system from Stewart-Warner, Inc., both of which use I^2L technology. The former contains an array of 256 quad-output I^2L gates and 16 special-purpose I^2L gates. Npn and pnp transistors and resistors are also supplied for the for= mation of interface circuits or simple analog circuits. An I^2L design kit (similar to the UC1 Designer's Kit) is available. Typical development costs for initial pro= totypes of \$3 500 to \$5 000 are quoted. The latter con= tains 208 gates (SWAP 16) or 408 gates (SWAP 24). I^2L transistors with high breakdown voltages are available for interface circuits. Development costs are \$1 800 to \$4 500 and production circuits in quantities of around 10 000 cost about \$1,50 each.

I^2L has much to recommend it for digital arrays. The inherently high packing density (of the order of 100 gates/mm^2) enables LSI circuits to be produced even in the non-optimal layouts of uncommitted arrays. The buried n+ layer forms a common ground for all cells and the injector rail a diffused

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power supply connection which can pass under logic interconnections on the surface (however, these cross-overs should be minimized). Thus, like CDI, the inter=connection problem is reduced to the design of the logic interconnections.

International Microcircuits, Inc., offer a CMOS gate array under the trade name of Master MOS[16]. It consists of an array of 254 p-channel and 254 n-channel MOS transis=tors and some special-purpose MOS transistors for interface circuits. Capable of running at supply voltages up to 15 V, it has similar performance to SSI and MSI CMOS circuits and, in fact, designs may be breadboarded using CMOS gates.

Despite the obvious interest in gate arrays they will always suffer from the following disadvantages.

(a) Provision must be made for all possible inter=connections, many of which will not be needed in a particular design.

(b) Special-purpose components (such as high-speed gates or low-power gates) may not be available.

(c) The component layout is not optimized for the design which is being implemented.

The poor usage of area resulting from (a) and (c) imply that the gate array area will need to be larger for a specific design than would be required by an equivalent dedicated design, resulting in a lower yield for the gate-array solution.

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(c) Programmable arrays

This class of circuits includes the following.

Read-Only Memories (ROMs)

Read-Only Memories were originally developed for permanent program storage functions in computers. With the trend towards microprogrammed machines they are finding widespread applica= tion in this field. However, their use as a substitute for combinational logic networks is also on the increase and has been well-documented in the literature. This application of ROMs may be understood by considering a sum-of-products reali= sation of a function of m-inputs and n-outputs. This is a com= pletely general case, as any combinational circuit may be trans= lated into this form. Consider the most 'complex' case, where every one of the 2^m-products of the m-inputs is required and every one of the output sums contains all 2^m-product terms. This is illustrated in Fig. 3.5 for the case m = 3, n = 2. The most 'complex' case actually yields a trivial solution, namely $Q_o = Q_1 = 1$. However, all practical circuits will be simpler than this, in the sense that they may be realized merely by omitting to connect the unwanted product terms to the output OR-gates. The first logic level of AND-gates is in reality nothing more than a m- to 2^m-decoder, and can be made standard for any circuit with m-inputs. The programmable interconnections and the second logic level (OR-gates) can be implemented by means of a matrix of programmable decoupled cross-points. This matrix forms the major part of a ROM.

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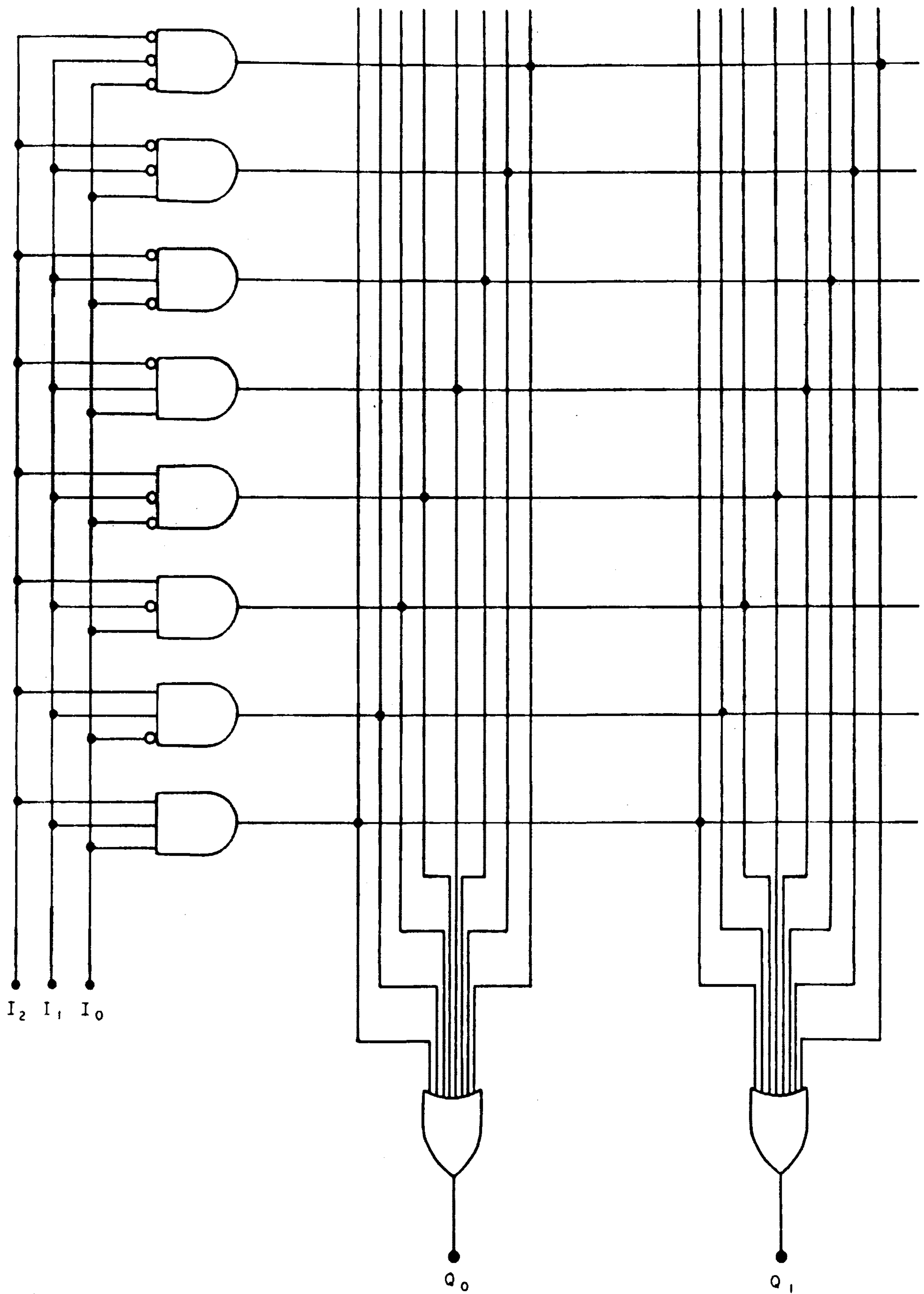

Fig.3.5 A ROM as a combinational circuit

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Fig. 3.6(a) shows a diode-matrix implementation of a 3-input, 4-output ROM. The m-inputs (3) are decoded and used to drive 2^m (8) word lines. Programmable diode connec= tions to the n-bit lines (4) exist at each cross-point. Each bit line forms a diode logic (DL) gate with n_p-inputs, where n_p is the number of connections programmed onto that line (Fig. 3.6(b)).

Programming methods vary, but may be divided into two categories: mask-programming, where the manufacturer uses a special mask to personalize the ROM; and field-programming, where the user programs his own ROM electrically. As a ge= neral rule, the field-programmable ROMs (PROMs) are the cheapest solution for small quantities while the mask-programmable com= ponent is cheaper when considering large quantities. The cost of a ROM may be divided into three components. Firstly there are costs associated with setting-up production of the ROM itself. These consist of a constant overhead, plus a cost associated with the size of the decoder, plus a cost associa= ted with the size of the array. The decoder consists of 2^m- gates, so its cost component may be modelled as being propor= tioned to 2^m. The array cost component is taken as being pro= portional to the number of cross-points, which is $2^m.n$, where n is the number of outputs. Thus the first cost component is

$$\emptyset_1 = A_r + B_r.2^m + C_r\ (2^m.n). \qquad 3.7$$

The second component is related to the programming opera= tion. For both mask- and field-programmable devices this

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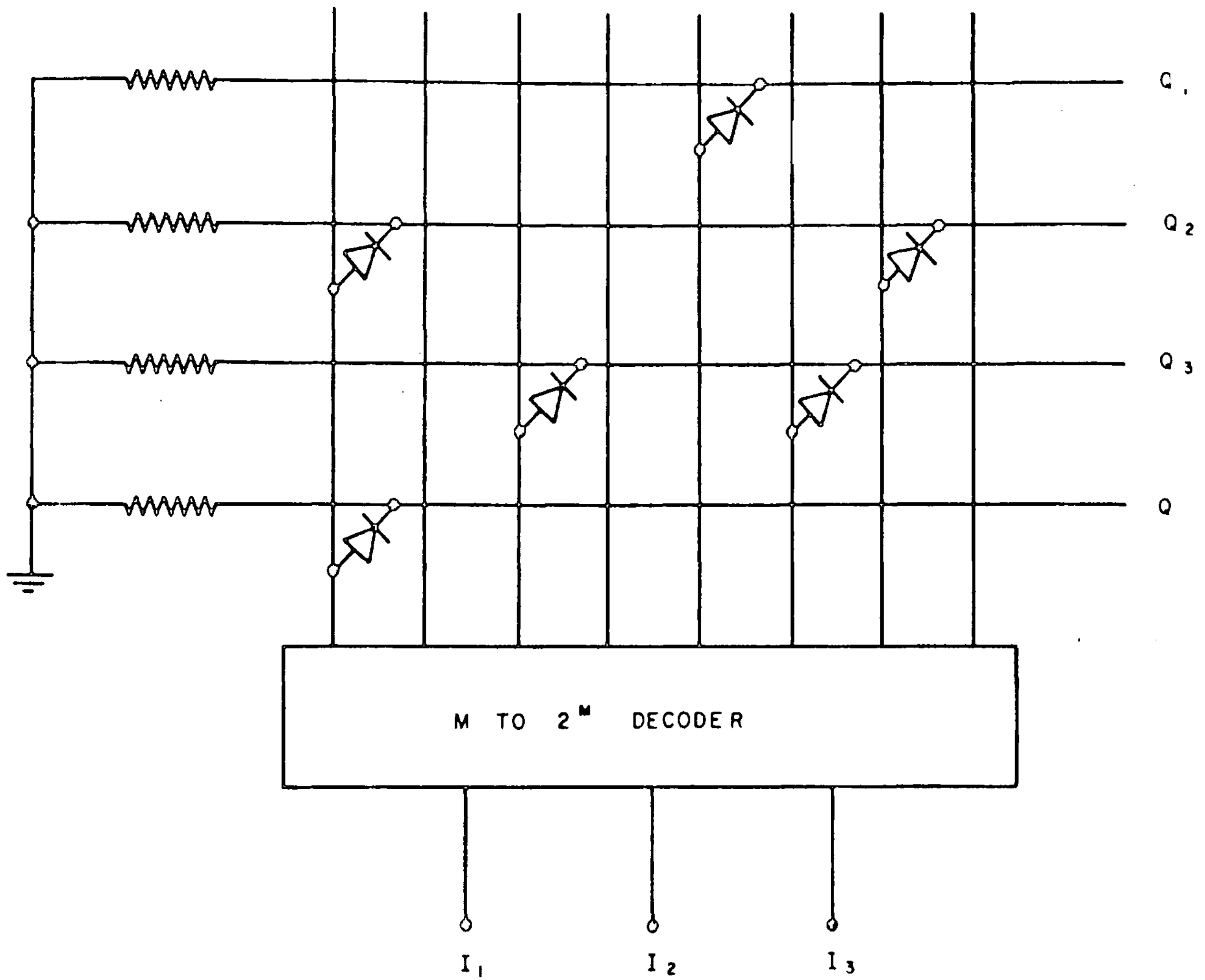
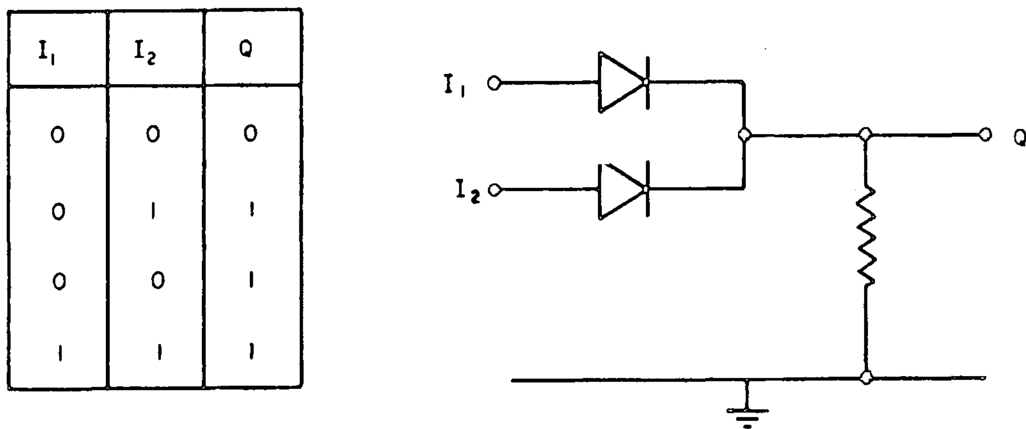


Fig.3.6(a) A diode-matrix ROM



I_1	I_2	Q
0	0	0
0	1	1
0	0	1
1	1	1

Fig.3.6(b) Diode-logic gate

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will consist of a constant overhead plus a component proportional to the number of bits stored, which is $2^m.n$. The total cost is

$$\emptyset_2 = D_r + E_r (2^m.n). \qquad 3.8$$

The third cost is the incremental cost associated with each ROM produced and consists of the bonding and packaging costs. This will depend on the size of the package and the number of bonding operations required. Thus it may be considered proportional to the total number of pins, so that

$$\emptyset_3 = F_r (m + n). \qquad 3.9$$

Combining 3.7, 3.8 and 3.9 gives a total per unit cost of

$$\emptyset_{tr}/p = (D_r + E_r(2^m n))/p + F_r(n + m) + (A_r + B_r 2^m + C_r 2^m n)/i \qquad 3.10$$

where p identical ROMs are required and i is the total production of the standard component. i Will be very large if the ROM is a standard part, so 3.10 reduces to

$$\emptyset_{tr}/p = (D_r + E_r 2^m n)/p + F_r (n + m). \qquad 3.11$$

As in the case of p custom LSI circuits, the per unit cost tends towards a finite value as the volume in= creases. It is not possible to compare the custom IC and ROM solutions for a general case, as the relationship between g, m and n depends on the particular application under consideration. If all parameters are known, equations

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3.3 and 3.11 may be compared to find the cheaper solution. This gives a cost ratio of

$$\emptyset_{tr}/\emptyset_{tc} = \{(D_r + E_r 2^m n)/p + F_r\ (n + m)\}/$$

$$\{(A_c + B_c g)/p + C_c + D_c g\} \qquad 3.12$$

At first glance it would appear that a ROM will generally be cheaper than a custom IC because the constants D_r and E_r are only associated with one mask layer or one programming operation, while A_c and B_c cover all steps in the production process and one likely to be much larger. However, in many applications g is considerably smaller than 2^m.n. This can occur when a large number of the 2^m possible input combinations are 'don't care' conditions.

In a custom IC or random logic solution no gates need to be provided to decode these irrelevant combinations, but in a ROM all 2^m combinations must be decoded, and every cross-point in the matrix must be programmed (in other words, data must be stored at every address). An example of an application where a ROM performs badly is a EBCDIC to ASCII decoder[11]. EBCDIC is a 12-bit code, which means that it has 4 096 possible symbols, while in reality there are only 128 symbols in its character set. A 4 096 x 8-bit ROM could be used, but the usage would be only $\frac{128}{4\ 096}$ x 100 = 3,13%. A custom IC would only require 128 AND gates and 8 OR gates and would

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cost far less (if produced in realistic quantities). It will be shown that this drawback of ROMs is not shared by PLAs.

If one compares the electrical performance of ROMs with that of custom ICs or random logic, one must take care to choose products using comparable technology. Such a comparison shows that ROMs and random logic cir= cuits of a specific logic family have similar speed and power-dissipation performance. For example, the TTL SN74187 1024-bit ROM has a typical propagation delay of 36 ns, and a power dissipation of 15 mW per gate equiva= lent[17]. Implementing the two logic levels with TTL gates would produce a total typical propagation delay of 26 ns and a power consumption of 10 mW per gate. Thus there is no performance advantage to be attained by using ROMs. The increased reliability and improved packing density of the ROM solution are strong incentives, however (e.g. a random logic implementation of the 1024-bit ROM could require as many as 36 packages).

Programmable Logic Arrays (PLAs)

In order to relate the PLA to the preceding discussion of the ROM, it will first be described in terms of the so-called Super ROM model[11]. It has been shown that the major drawbacks of the ROM, when used to replace combinational logic, are its fixed address decoder and the necessity for all addresses to contain data. The PLA may be considered as

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a small ROM with a programmable address decoder (Fig. 3.7). The first matrix enables any q of the 2^m-input addresses to be decoded onto the q address lines. q Is generally smaller than 2^m. Thus the second matrix (which corresponds to the ROM matrix of the previous section) now has dimensions of q x n instead of 2^m.n. The significance of this is obvious if one considers a PLA realization of the EBCDIC to ASCII decoder. Only 128 characters need to be decoded, therefore q = 128. The decoder could be implemented with a PLA consisting of a 12-input, 128-output address decoder and a 128 x 8-bit ROM. The total number of cross-points to be programmed is

$$m.q + q.n = q(m + n)$$
$$= 128(12 + 8)$$
$$= 2\ 560$$, compared to the 32 768 bits for

the ROM solution. The two PLA matrices are together equal to 7,81% of the size of the single ROM matrix, and the usage of the PLA is 100%. The decoder is far less complex, consisting of only 128 AND gates instead of 4 096. Equation 3.10 may be rewritten for the PLA as follows

$$\emptyset_{tp}/p = (D_r + E_r q(m + n))/p + F_r(m + n) +$$

$$(A_r + B_r q + C_r q(m + n))/i \qquad 3.13$$

The following points are observed

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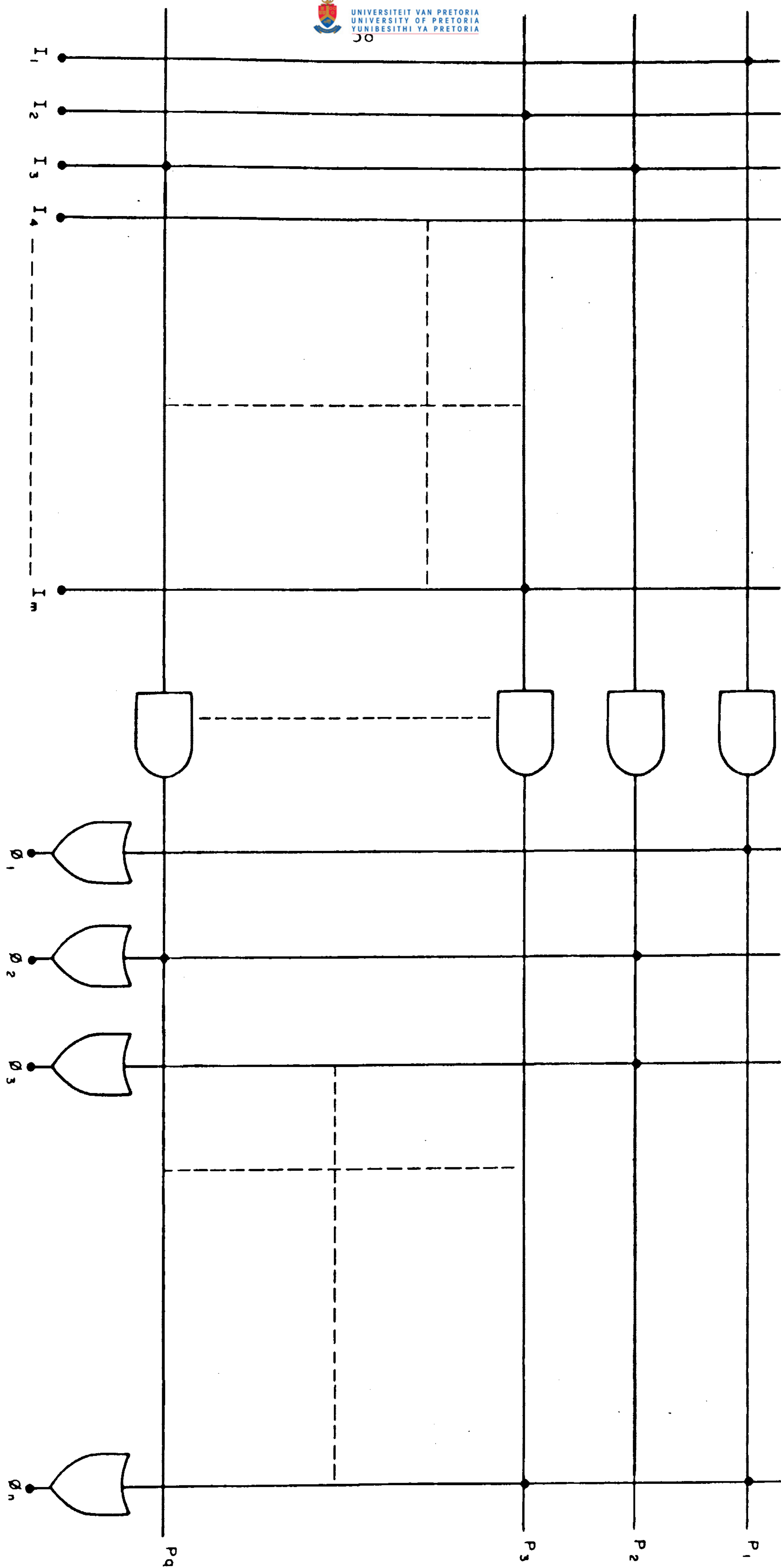

Fig.3.7 The SuperROM model of the PLA

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(i) $\emptyset_{tp}/p \rightarrow F_r\ (m + n)$ as $p \rightarrow \infty$, the same limit as for the ROM. Therefore, for very large quantities the PLA has no cost advantage over the ROM.

(ii) Production overheads are smaller for the PLA. Comparing the last terms in equations 3.10 and 3.13, it is clear that

$$(A_r + B_r q + C_r q\ (m + n))/i \leqslant (A_r + B_r 2^m + C_r 2^m n)/i$$

For the example above:

$$(A_r + 128\ B_r + 2\ 560\ C_r)/i \leqslant (A_r + 4\ 096\ B_r + 32\ 768\ C_r)/i$$

The two terms in the above inequality represent the total production overheads for PLAs and ROMs. Letting p be a constant, the per unit production overheads are:

$$\emptyset_{pp}/p = K_p/i \qquad 3.14$$

and

$$\emptyset_{pr}/p = K_r/i \qquad 3.15$$

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where $K_p < K_r$. These relations are shown in Fig. 3.8. $\emptyset_{pp}/p$ tend to zero much quicker than $\emptyset_{pr}/p$ as production increases. This is a particularly important point for the small-volume producer as it shows that PLA production is economical in smaller volumes than ROMs.

(iii) Letting $i \rightarrow \infty$ with p finite, the overheads may be neglected. From 3.10 and 3.13 the remaining costs are:

$$\emptyset_{rp}/p = (D_r + E_r q\ (m + n)/p + F_r\ (m + n)$$

$$= k_p'/p + F_r\ (m + n)$$

for the PLA and

$$\emptyset_{rr}/p = (D_r + E_r 2^m n)/p + F_r\ (m + n)$$

$$= k_r'/p + F_r\ (m + n)$$

In this case $k_p' \ll k_r'$ (because $q(m + n) \ll 2^m n$). Thus $\emptyset_{rp}/p$ will tend towards the limit of $F_r(m + n)$ much quicker than $\emptyset_{rr}/p$ (Fig. 3.9). The per unit cost of the PLA is therefore lower in the small and medium quantity region.

The PLA has been described in terms of the ROM model and its cost structure compared to that of the ROM. For the user it is perhaps best described directly in terms of logic equa= tions - the so-called AND-OR model[11]. The address-decoding matrix is called the AND array and the ROM matrix the OR array.

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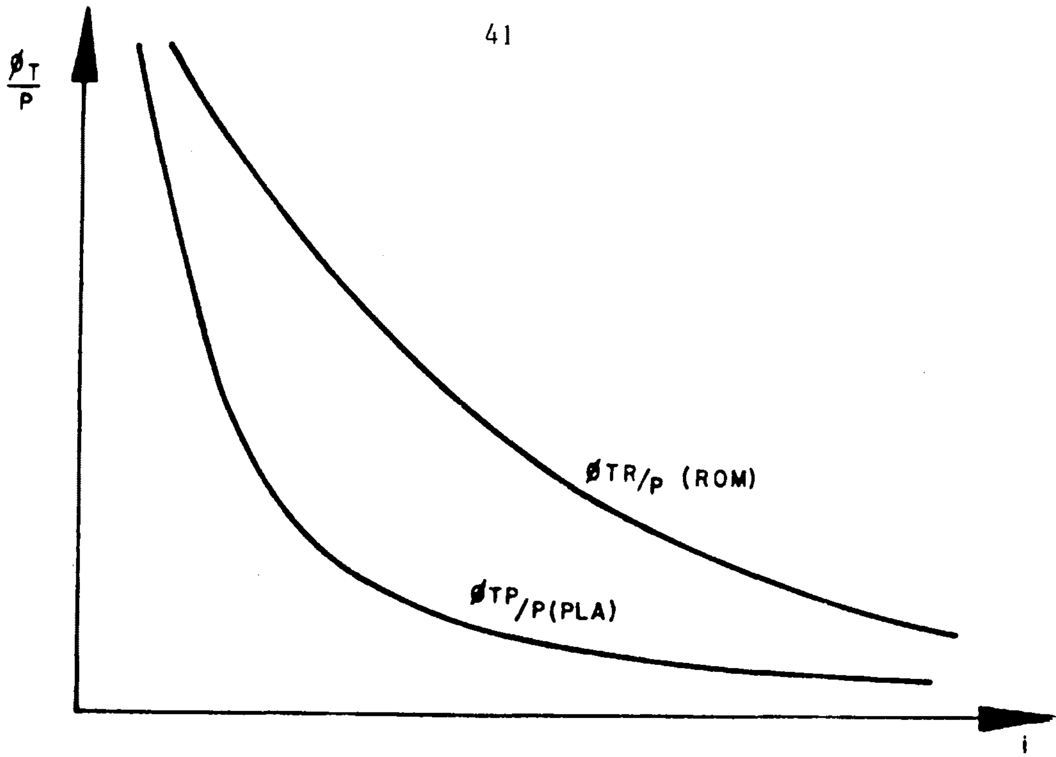

Fig.3.8 $\emptyset_t/p$ vs i

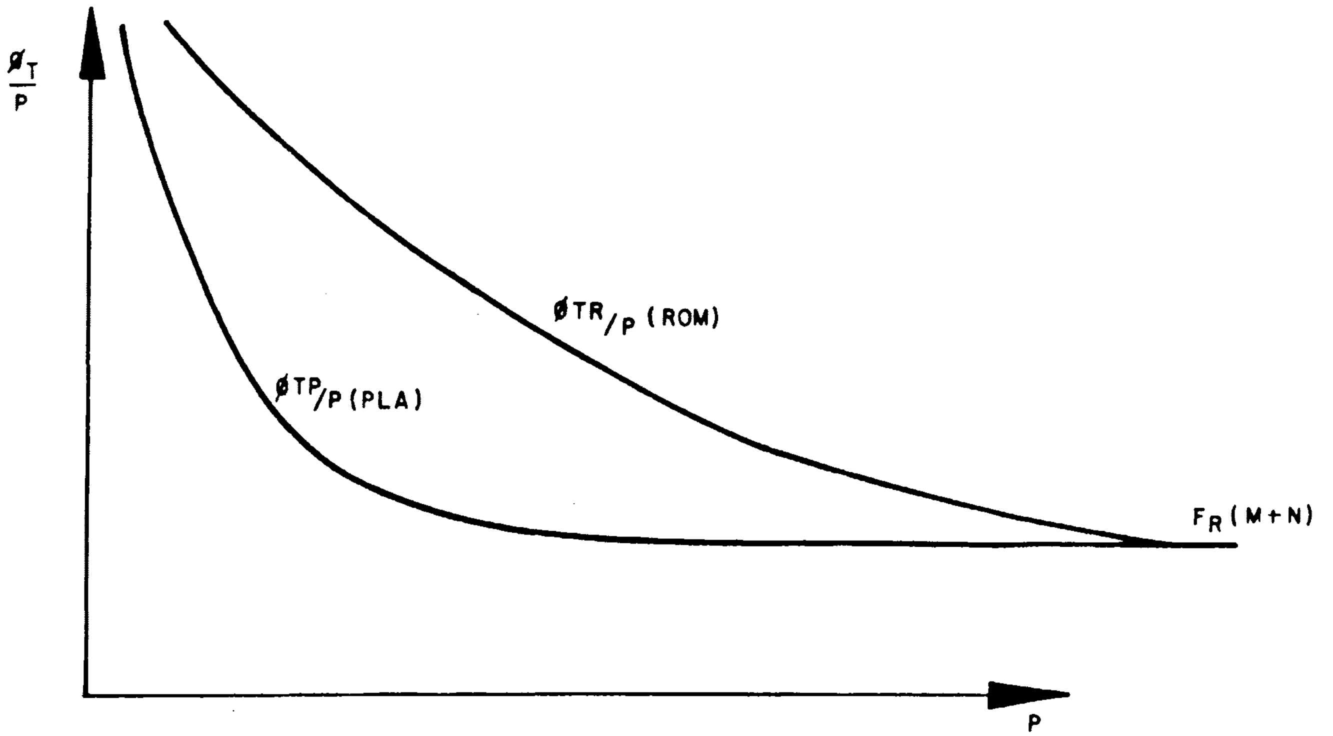

Fig.3.9 $\emptyset_t/p$ vs p

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Input variables I_1 to I_m are formed into various products P_1 to P_q by the AND array. These appear on the address lines (now called product-term lines). Each product-term line represents a term of the form $P_5 = I_1\overline{I}_4 I_7 I_8 \overline{I}_{11}$ (for example). The OR array generates sums of these pro= ducts to form the outputs (e.g. $Q_4 = P_1 + P_4 + P_6 = I_3\overline{I}_7 I_8 + I_1 I_2 \overline{I}_4 + I_9\overline{I}_{11}$). A PLA can represent any n-logic equations in sum-of-products form, with a maximum of m-in= puts and q product terms. The AND-OR terminology will be used in subsequent chapters.

A third method of describing a PLA is by means of a truth-table. This is simply a tabulated version of the lo= gic equation description and will not be discussed.

PLA electrical performance is technology-dependent. However, as the basic element (a decoupled, programmable cross-point) is the same, it follows that PLAs and ROMs implemen= ted in the same technology will have similar electrical cha= racteristics.

PLA applications have been described in several publi= cations in recent years. The following are worthy examples which have appeared in the literature.

(i) A tape-deck controller[11].

A PLA has been used to decode the control signals reaching a tape controller from the com= puter. Seven different commands are required to generate pulses of different widths on 2 outputs to the tape-drive mechanism. The pulses are gene= rated by a 6-stage counter which divides down a

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a clock frequency from the main frame. The PLA combines the control signals with the pulses of various widths emanating from the counter and produces START and STOP signals which are latched and fed to the tape drive (Fig. 3.10). Fourteen inputs, two outputs and 18 product terms are used. A TTL equivalent requires 20 packages.

(ii) A controlled shift register[11].

A PLA has been used together with eight D-type flip-flops to form an 8-bit shift register with various shift patterns: arithmetic shift, logical shift or circular shift, left or right. The PLA uses 4 control signals to define the next-state condition of the flip-flops (Fig. 3.11).

(iii) Decoding microstore addresses in microprogrammed computers[11].

In a single microprogrammed computer the con= tents of the instruction register (i.e. the macro-instruction in machine code) is used to initiate a sequence of micro-instructions in the control store. Usually this is done simply by having the instruction register contain the starting address of the required microroutine. However, as each microroutine occupies several words of microstore, this is wasteful of address bits in the instruction register. For example, if a computer has a set of 100 macro-instructions, each of which initiates a

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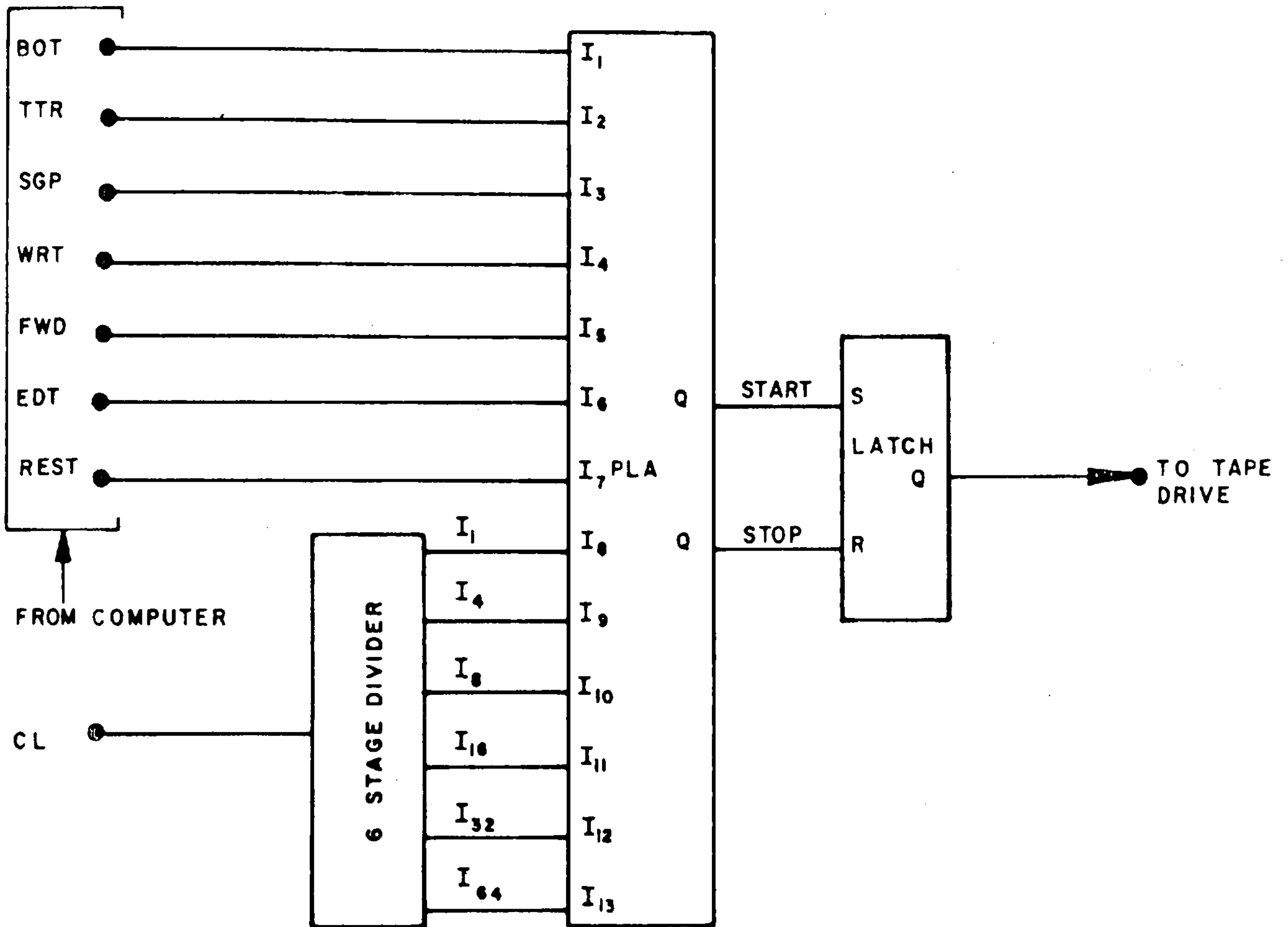

Fig.3.10 Tape deck controller

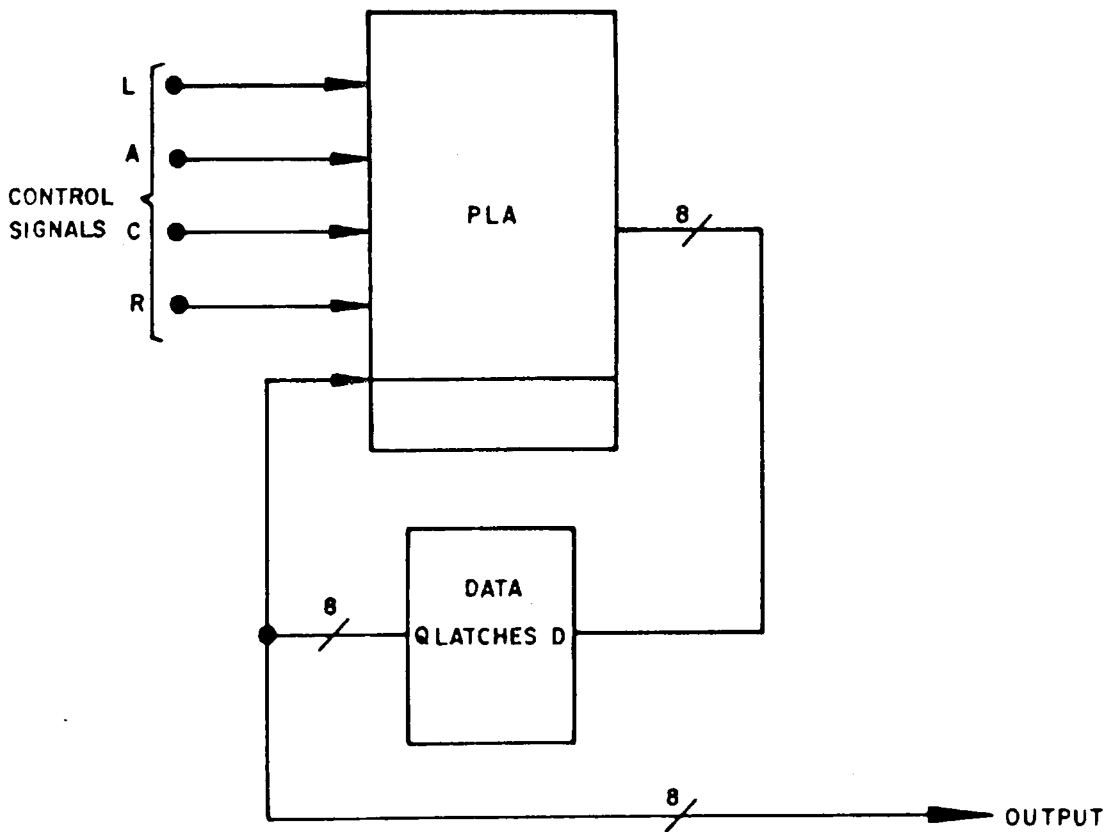

Fig.3.11 A controlled shift register

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sequence of five micro-instructions, then the instruction register must contain enough address bits to address 500 microwords, although only 100 will be addressed. This is because the starting addresses are spaced five words apart. Another problem is the varying width of the address field in the instruction register, depending on the type of instruction being implemented. The micro-store must have as many address bits as the longest address field, even though many locations are not used. Both of these problems can be overcome by the use of a PLA between instruction register and control store (Fig. 3.12). The PLA translates the variable length addresses in the instruction register starting addresses for the microcoder routines, thus enabling the best possible use of the available address bits to be made and enabling the smallest possible ROM to be used for the control store.

(iv) As a microstore in a minicomputer[18].

Special-purpose PLAs have been used as the actual microstore in a minicomputer (Computer Automation Naked Mini/LSI). These PLAs, each with 20 outputs, store all the microcode sequences for the 168 macro-instructions. The machine is designed on a 4-bit slice basis. All the advantages described in example (iii) also accrue in this case. Seven LSI chips are used to implement a complete 16-bit minicomputer.

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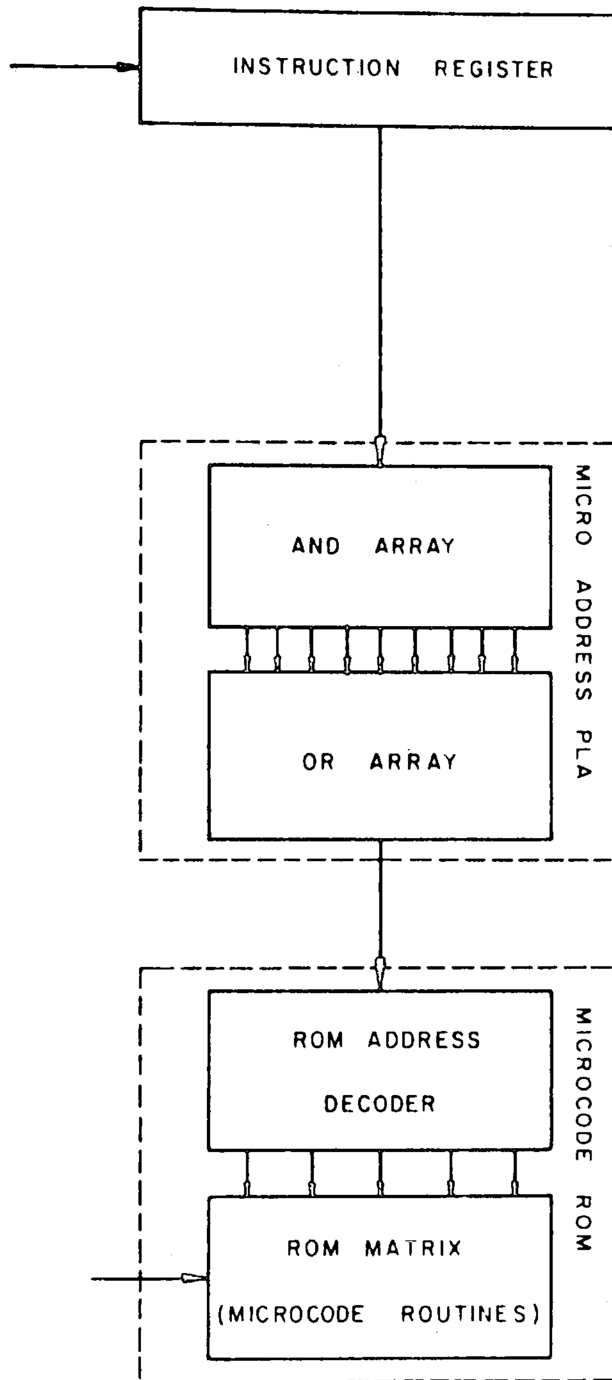

Fig.3.12 Use of a PLA in a microprogrammable mini-computer

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(v) A Core-Memory Patch[19].

A certain number of faults are to be ex= pected in a large core memory. It has been es= timated that a 64k x 8-bit memory could contain as many as 100 defective cores (0,02% fault rate). These can be repaired by a hand restringing routine. Alternatively an auxiliary memory can be used. However, because the faults can occur anywhere in the memory, the addresses of defects will be scat= tered over a wide range. This is a perfect appli= cation for a PLA, which can be used to compress the odd addresses onto product lines, one for each fault. The fault lines are used to generate outputs, which address a small auxiliary RAM, which replaces the damaged cores.

(vi) Fault Monitor Networks in data Multiplexing Systems[20]

PLAs have been used to monitor the selection status of all the inputs to a multiplexer. For cor= rect transmission only one channel of a TDM system must be allowed to transmit at a given moment. Any fault in the multiplexer which allows simultaneous transmission from more than one channel will cause an erroneous transmission. By monitoring the se= lection-status bits, the PLA(s) form an error-de= tection system.

(vii) A vectored priority interrupt system[19]

PLAs have been used to decode an 8-bit priority interrupt vector into memory address of subroutines

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to service the relevant peripheral. This is a similar application to that described under (iii) above.

iii) Generation of characters for a CRT display[20].

Diode-array PLAs have been used for the lo=gical generation of patterns on a CRT display. The information stored in the PLA is used to modulate the Z-axis of the CRT. ROMs have been used for the same function but the cost of the PLA solution is much lower because only the small number of squares on the screen which can produce standard characters needs to be considered when storing data. In the ROM solution the entire sur=face must be stored.

3.4 Summary of Conclusions

On the basis of a study of the various alternatives described in 3.3, it was decided that the PLA is probably the most suitable component for local production. The following factors pointed to this.

1. A demand exists for a component suitable for applica=tions where a microprocessor is too sophisticated or too sequential, while random logic is unacceptably space- or power-consuming.
2. Small volume pre-production overheads are smaller for a PLA than for a ROM and are probably about the same as gate arrays or custom ICs.
3. Per unit costs for small or medium volumes (< 2 000 cir=cuits) are lower for PLAs than for any of the alterna=tives.

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4. Design times are shorter than for custom ICs, gate arrays or ROMs because of the simplified interconnection problem.
5. A PLA implements logic equations in sums-of-products form, which is the most suitable form for minimization by means of existing techniques such as Karnaugh diagrams and Quine-McCluskey algorithms.

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CHAPTER 4

4. CHOOSING A TECHNOLOGY

The original specifications for this design (see Chapter 1) called for an uncommitted digital IC suitable for relatively low-speed ap= plications (below 1 MHz) and featuring a low-power consumption. At the time it was envisaged that I^2L might be used in the design be= cause of its suitable electrical characteristics. However, because of difficulty in adapting the I^2L cell for array use, it was decided to first investigate the more conventional diode and transistor arrays used in commercial PLAs. This chapter compares some process-compatible diode and transistor structures based on commercial designs. It will be shown that these structures are inherently unsuitable for low-speed, low-power applications. This discussion is used as a basis for a descrip= tion of I^2L and its development from conventional direct-coupled tran= sistor logic (DCTL).

4.1 Requirements for PLA structures and technology

Fig. 4.1 is a block diagram of a PLA showing the following sections:

1. Input interfaces.
2. Output interfaces.
3. AND-array.
4. OR-array.

Neglecting initially the form of (1) and (2) (which depend on the type of logic with which the PLA is intended to interface), basic structures and technology must be developed for the AND- and OR-arrays. However, de Morgan's theorem states that

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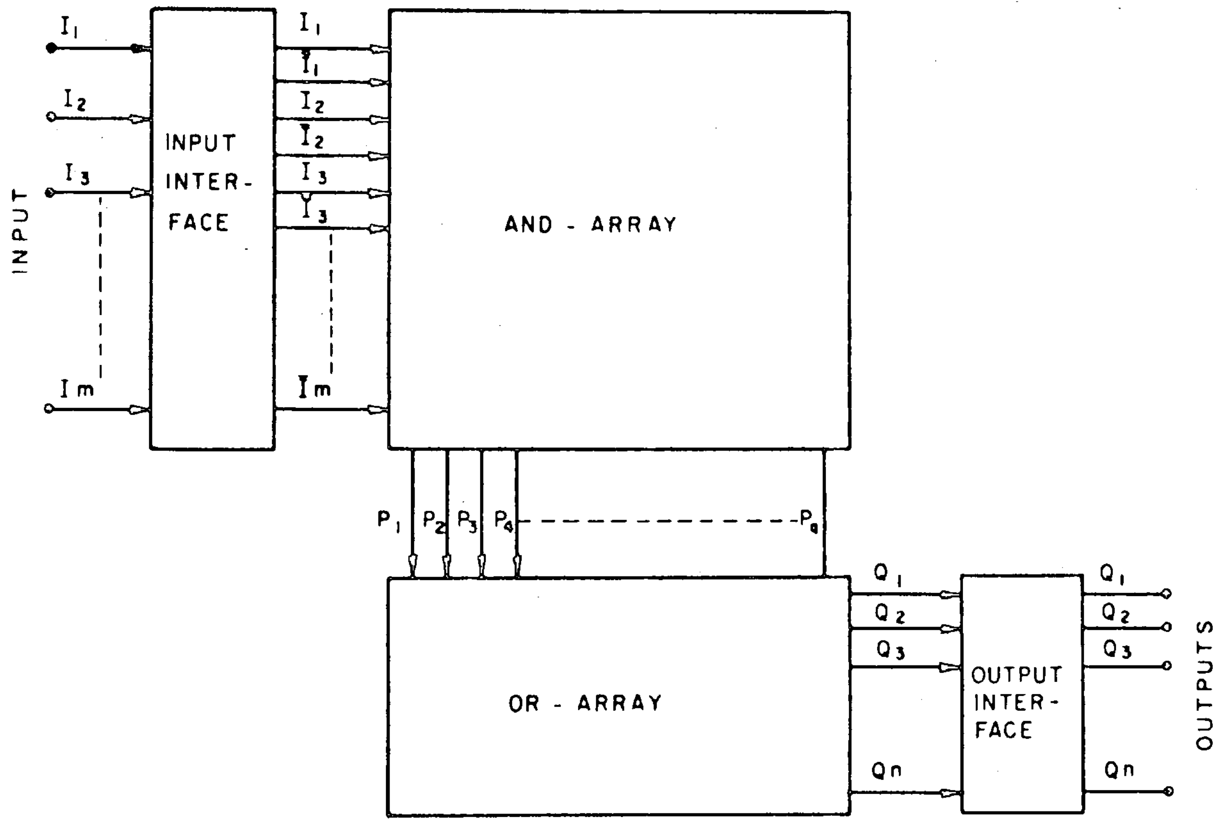

Fig. 4.1: Block Diagram of a PLA

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$$P_1 + P_2 + P_3 \text{ ---------- } + P_n = \overline{\overline{P}_1 . \overline{P}_2 . \overline{P}_3 . \text{ ------ } . \overline{P}_n}$$

or alternatively

$$P_1 . P_2 . P_3 . \text{ ------------ } . P_n = \overline{\overline{P}_1 + \overline{P}_2 + \overline{P}_3 + \text{ --- } + \overline{P}_n}$$

Thus, by pre- and post-inversion the same structure may be used for both arrays. The structure may implement either an AND- or an OR-operation. It will be shown that for certain structures the pre-inversion of signals is implicit.

What are the requirements of the basic cell in such a matrix?

1. It must allow coupling of a signal in one direction only, from input to output. If not, all inputs to the array will be rigidly connected to each other, with an undefined logic state.
2. It must be as compact as possible and have an aspect ratio close to unity, in order to form an array of realistic proportions. For example, consider the following hypothetical PLA (Fig. 4.2):

   Number of inputs (m) = 16

   Number of outputs (n) = 8

   Number of product terms (q) = 96

   Total dimensions of the two arrays: 3 mm x 3 mm.

The AND-array will have 2 m-inputs (the m-inputs to the package plus their complements which are generated in the interface circuitry) and q-outputs. The OR-array has q-inputs and n-outputs. For a basic cell with dimensions Δx and Δy, the overall dimensions of the arrays are

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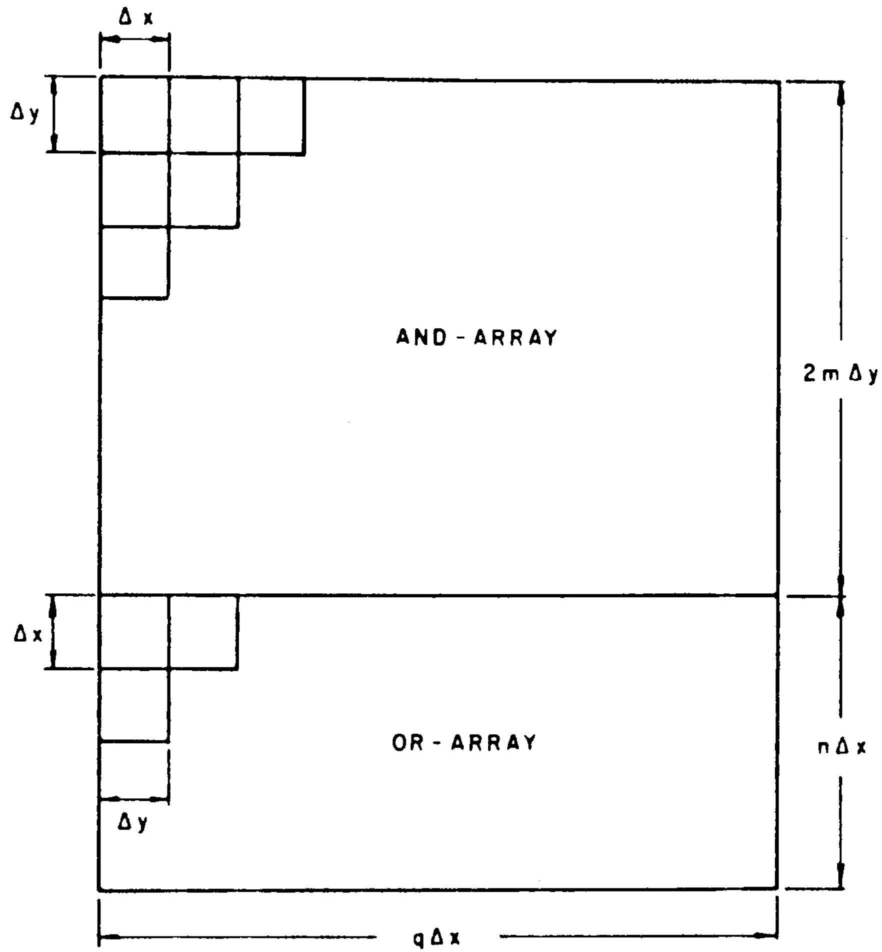

Fig.4.2 Dimensions of a hypothetical PLA

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$X = q\Delta x$

and $Y = (2m + n)\,\Delta y$.

$\therefore\ \Delta x = \frac{X}{q} = \frac{3\ 000}{96} = 31{,}25\ \mu m$

and $\Delta y = \frac{Y}{2m + n} = \frac{3\ 000}{2.16 + 8} = 75\ \mu m$.

The basic cell, therefore, has an area of 31,25 x 75 = 2 344 μm^2, and an aspect ratio of $\frac{75}{31{,}25} = 2{,}4$.

3. Power consumption must be as low as possible. This is a stringent requirement of this particular design.
4. The propagation delay of the cell must be as small as possible.
5. It must be easily programmable.
6. The cells must be easily interconnectable.

In addition, the following constraints apply to this particular design.

7. The cell must be realizable in bipolar process 1A with the minimum of process alteration (preferably none whatsoever).
8. All structures must be designed in accordance with process 1A layout rules (see Appendix A1).

These two constraints place a considerable restriction on the type of cell which may be used. Firstly, any possi= bility of using a MOS-structure must be ruled out completely. This is a pity, as single-channel MOS-technology enables high packing densities to be achieved. Some excellent PLAs have been produced using MOS- structures[21, 22 & 23]. The second restriction is on the maximum packing density at= tainable. This will ultimately be limited by the minimum di= mensions allowed by the layout rules.

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4.2 Methods of personalization

Some bipolar structures will now be examined in terms of the above requirements. However, as the method of programming (or personalization) used has a bearing on structural details, some possible programming methods will first be discussed.

A PLA in the unprogrammed state will either have all cells connected to both rows and columns, or all cells isolated from either a row or a column (Fig. 4.3). In the former case, program= ming consists in disconnecting cells not required from either the row or the column (whichever is easier), and in the latter case in connecting a required cell to a row or a column in order to complete the logic path from input to output. Thus, programming may be achieved either by making or breaking a connecting link at each cell. The following methods have been used to achieve this in com= mercial designs.

4.2.1 Mask programming

A PLA may be personalized for a specific function by designing a suitable contact pattern (metallization) mask. Generally, the contact pattern mask will consist of some compulsory metallization as well as some optional connections which may either be included or omitted[8]. Fig. 4.4(a) shows the con= tact pattern of a programmed diode array. Diodes may be con= nected to the vertical conductors (which are compulsory) by means of small links (which are optional). An alternative method is to run the conductors over the diodes and program the PLA by means of a personalized contact window mask, which

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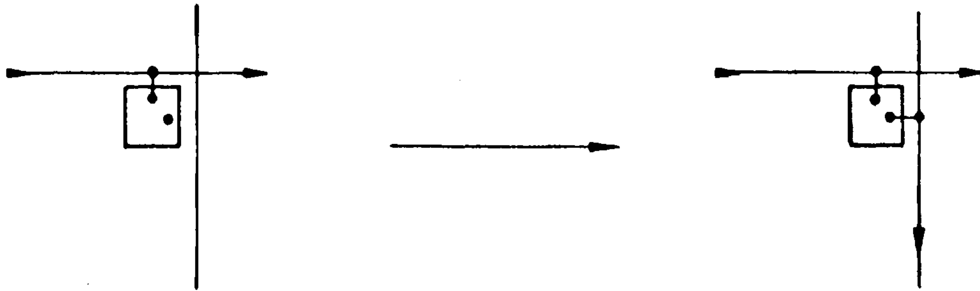

Fig.4.3(a) Programming by forming links

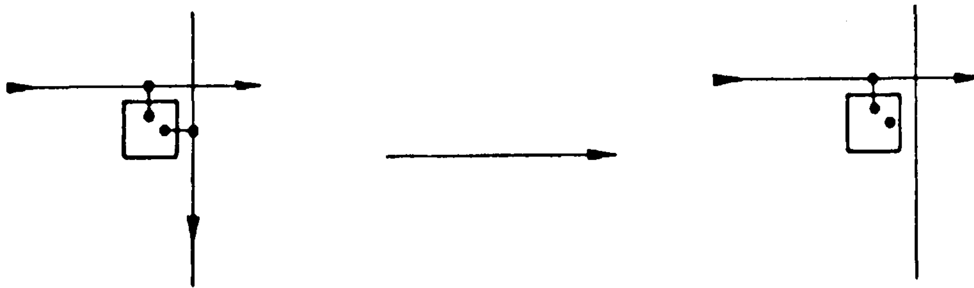

Fig.4.3(b) Programming by breaking links

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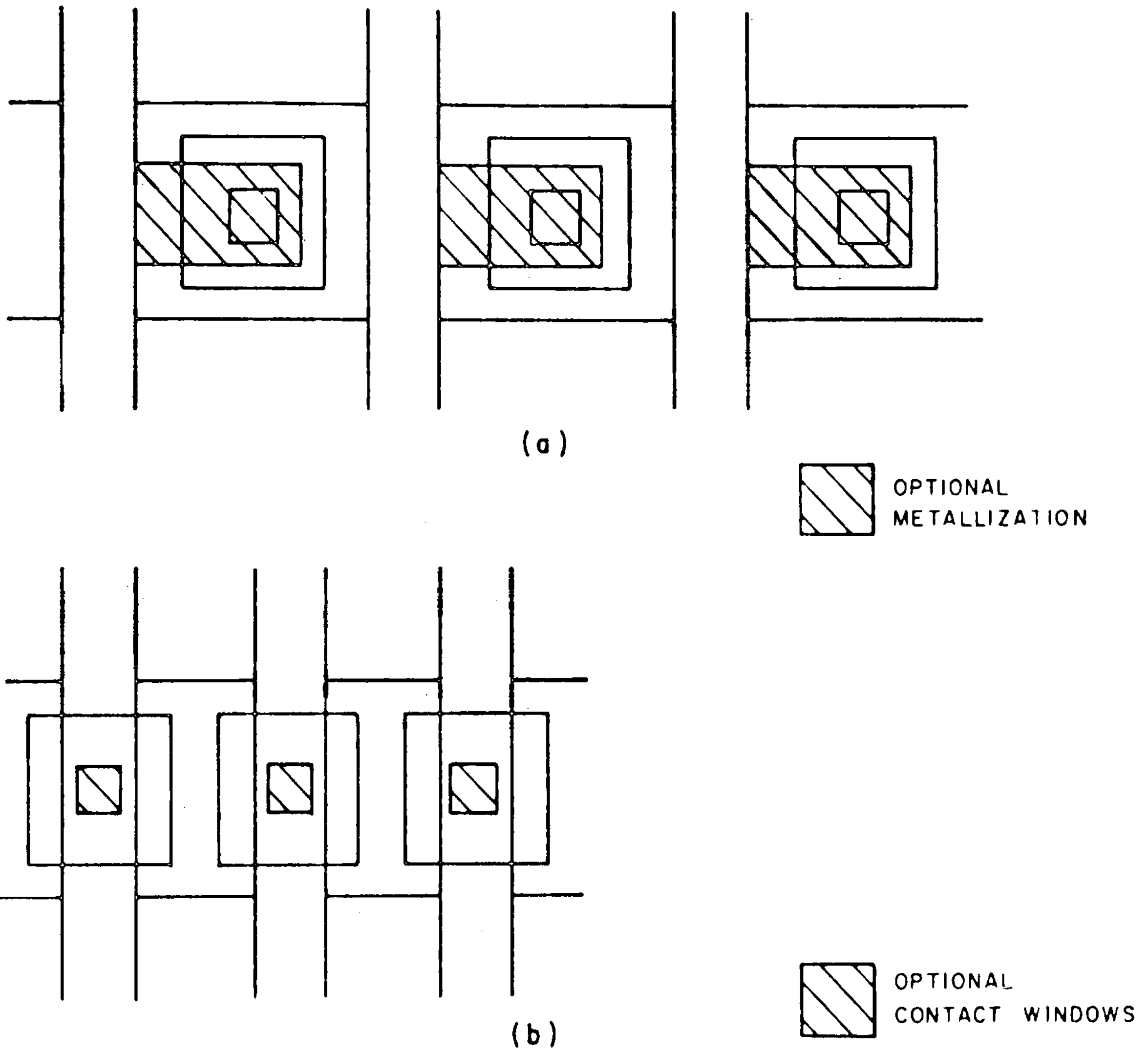

Fig. 4.4: Mask Programming Methods

(a) Programmable Metallization

(b) Programmable Contact Windows

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opens windows in the silicon dioxide layer over the diodes which need to be connected to the conductors[22] (Fig. 4.4(b)). In the case of structures designed according to process 1A layout rules, the latter method enables some saving of space to be achieved and is therefore preferable, as it maximizes packing density. From a production point of view this method is slightly less convenient, as the personalization now takes place one step earlier in the process. The aluminium eva=poration step must now be carried out after personalization, which will tend to increase the turn-around time of a design slightly.

4.2.2 Electrical (field) programming

Field-programmable logic arrays (FLPAs) are becoming in=creasingly popular, as they enable the user to verify his design easily. Mask-programmable logic arrays are cheaper to produce in large quantities though, as the time-consuming elec=trical programming operation of the FPLA is avoided[11]. Per=sonalization may be achieved by means of fusible links, usually made of a nickel-chromium (Ni Cr) alloy. Program=ming is the inverse of the operation used to program a mask-programmable device where connections are made by adding links or opening contact windows. In a virgin FPLA all connections are already made and the unwanted connections are blown by the application of suitable currents. Apart from the Ni Cr-technology, it has been suggested[5] that links consisting of

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suitably doped polysilicon deposited on the silicon sur= face could also be used. However, as none of these fusible link techniques forms part of the standard process it is not considered practical to try and produce an FPLA.

4.2.3 Laser programming

Lasers may be used to program PLAs by burning away unwanted connections. Laser PLAs must be programmed by the producer, but as no special masks are needed, they are cheaper than mask-programmable devices in small quantities. Rockwell use laser encoding when programming their P/N 15900NB PLA in small quantities, while using conventional mask programming for lar= ger quantities[24]. Laser programming may therefore be seen as a secondary programming method which may be used to personalize small quantities of mask-PLAs.

In view of process constraints it would appear that a mask-PLA would be the most suitable for local production. It was decided to produce a PLA using the contact window mask for personalization, in order to maximize packing density. The structures to be described were all designed with mask pro= gramming in mind, but could be modified to suit other methods.

4.3 Silicon PN-diode arrays

Silicon diodes are the most widely used element in PLAs. Several successful commercial designs have been based on this simple struc= ture. They include the following:

1. The Rockwell P/N 15900NB, which uses an array of 128 x 46 silicon-on-sapphire (SOS) diodes[24]. These diodes permit fast switching because of reduced substrate capacitance.

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No interfaces are provided and each diode may be con= nected as part of the AND- or the OR-array.

2. The National Semiconductor DM 7575/76 and DM 8575/76, TTL compatible PLAs with a 14 x 96-gate AND-array and a 96 x 8-gate OR-array[17].
3. The Monolithic Memories 5775A, a pin-compatible replacement for the National product[25].

In a bipolar process such as process 1A, four regions are used to form npn-transistors (see Fig. 4.5).

1. An n-type region consisting of an n^- epitaxial layer and an n^+ diffused buried layer which forms the collector.
2. A diffused p-type region which forms the base.
3. A diffused n^+-region which forms the emitter.
4. A deep p^+ isolation region extending down to the substrate (junction isolation).

A diode may be formed between any two regions of op= posite polarity. As the p^+ isolation region is grounded, it is of no value as an anode. Collector-base or base-emitter junction diodes must therefore be considered. There is a further problem. Process 1A does not make provision for multilayer metallization[26], and so interconnection of cells along one axis of the PLA must take place via a diffused region in the silicon (an 'underpass'). This may be achieved by making one electrode common to all diodes so that it serves as an underpass as well. Two structures based on this principle are shown in Figs. 4.6(a) and 4.6(b). In

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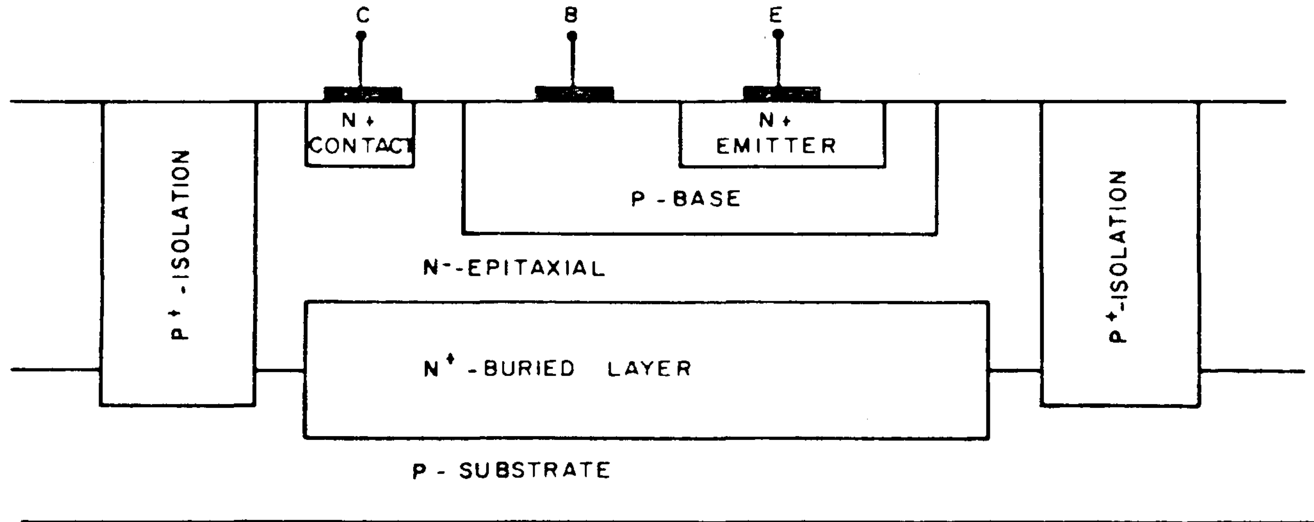

Fig.4.5 Cross-section of an npn transistor

(not to scale)

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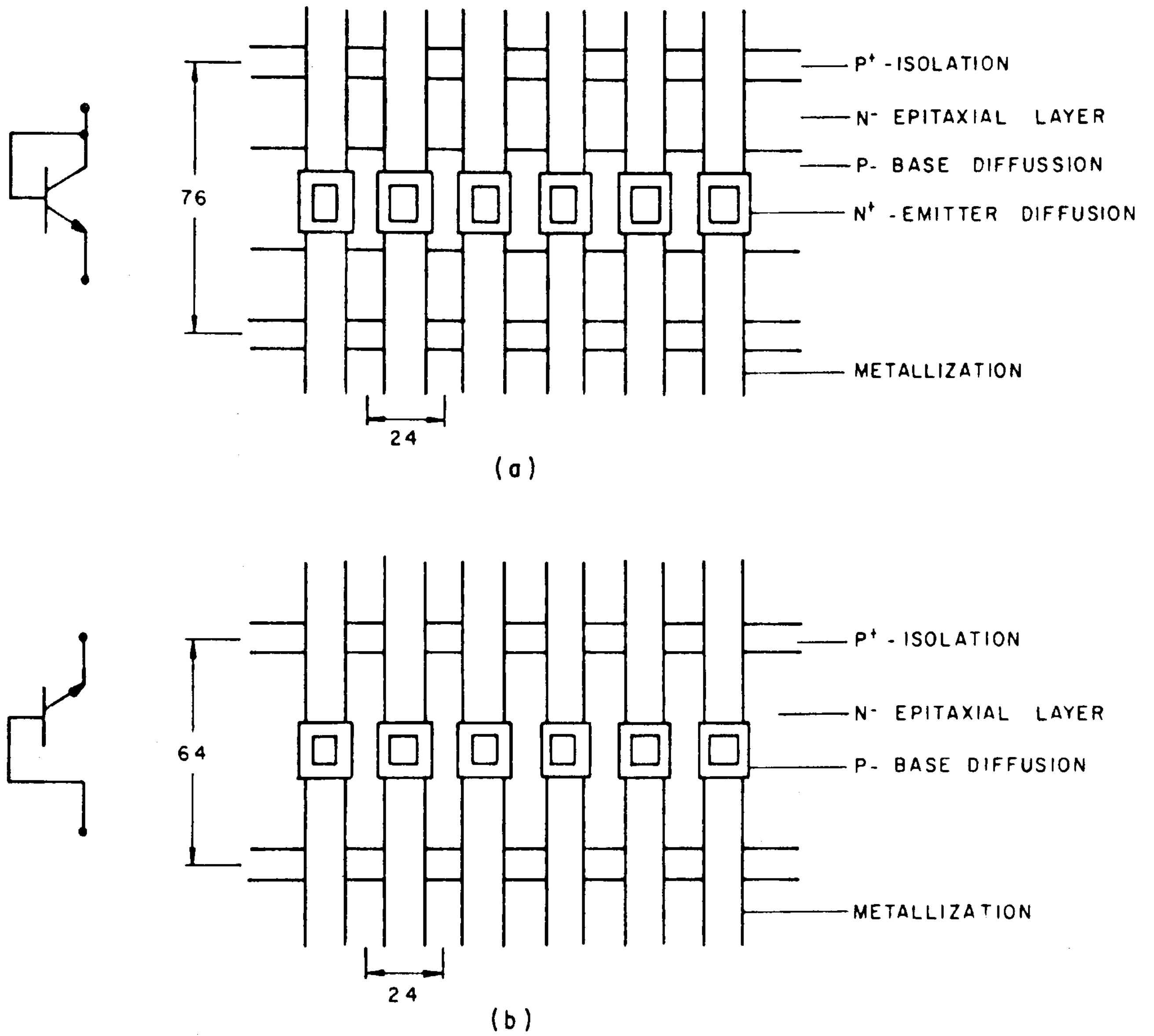

Fig. 4.6: Silicon diode arrays.

(a) Common anode structure.

(b) Common cathode structure.

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the first, a region of p-base diffusion forms a common anode, while a row of cathodes are formed by islands of emitter diffusion. Any array of AND-gates may be formed in this way. As the base-width below the emitters is small, injection will take place into the n-collector region. The latter must therefore be pe= riodically connected to the base region. This is the normal way of connecting transistors to form diodes in integrated circuits[8]. Connecting base to collector also lowers the effective resistance of the anode, as the buried n^+-strip (10 Ω/□) appears in parallel with the p-base diffusion region (100 Ω/□). The second structure uses the collector-base junction and is a little simpler. A common cathode is formed by the n-collector region and islands of p-base diffusion form anodes, thus implementing an OR-structure.

All dimensions in these two structures are the minimum allowed by the process 1A layout rules[26]. Some important physical parameters are summarised in Table I. The common anode structure has a higher packing density and a better aspect ratio. It also has a higher breakdown voltage. How= ever, voltage drops in the anode region limit its use in large arrays.

4.4 Schottky (aluminium-silicon) diodes

Schottky diodes have also been used in a commercial bipolar PLA. Sig= netics use Schottky diodes in the AND-array of their 825100 FPLA,

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thereby achieving a speed advantage over conventional silicon diode PLAs[11 & 19]. A Schottky contact may be formed between an aluminium contact and a lightly doped n-type silicon region. In our conventional bipolar process the n-type epitaxial layer has doping concentration of 8×10^{15} cm^{-3}, which would enable a Schottky contact to be formed. A Schottky diode array could therefore pro= bably be formed as shown in Fig. 4.7, although this structure is not standard for process 1A and has not yet been attempted. The proposed structure is designed according to minimum layout rules and has a similar packing density to the silicon diodes discussed (see Table I).

4.5 Transistor arrays

Intersil use two transistor arrays in their IM 5200 FPLA, which has 14 inputs, 8 outputs and 48 product terms[27]. In the unprogram= med state the transistor bases are open, so that a high resistance exists between collector and emitter. Programming consists in shorting out the base emitter junction by avalanche-induced migration of car= riers. The transistor may now be considered simply as a base-col= lector diode.

Signetics use an extremely compact transistor cell in the OR-array of their 825100 FPLA[19]. Fig. 4.8 shows a section of the array. Each cross-point consists of a common collector (emitter follower) npn-transistor with its base connected to an input line and its emitter driving an output line (via a Ni Cr fusible link). The transistor functions in the same way as a diode, except that

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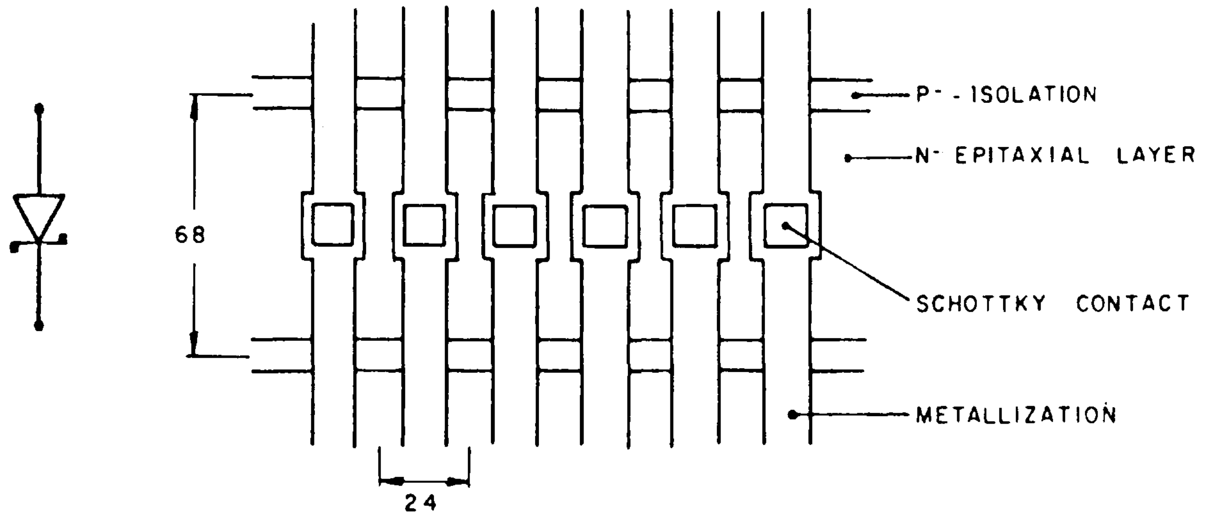

Fig.4.7 A Schottky-diode array

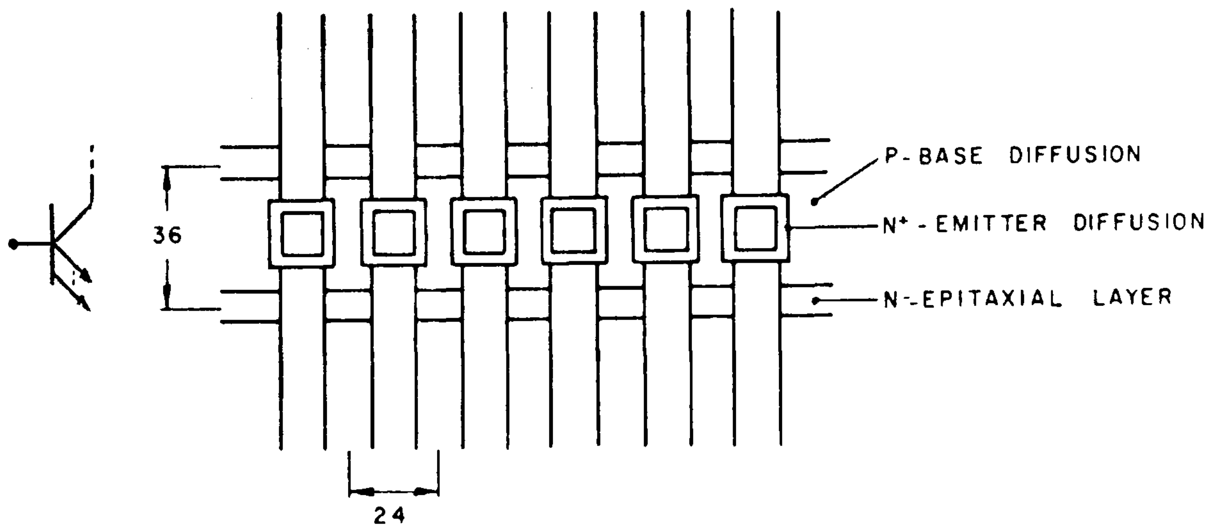

Fig.4.8 An emitter-follower transistor array

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it can deliver a greater current to the output ((β + 1) times the input current). Fig. 4.8 shows why this structure is also very compact: because of the common collector configuration, no p^+-iso= lation is necessary, and the n^- epitaxial layer and n^+ buried layer form a continuous positive supply voltage plane for the whole cir= cuit. The packing density is approximately double that of the diode arrays (see Table I). Because the buried layer is continuous it provides a very low resistance path for current flow to the col= lectors. On the other hand, a voltage drop also occurs in the base region, and as the sheet resistance of this diffusion is fairly high (100 Ω/□), this can be serious. It could be reduced either by wi= dening the base strip or, more effectively, by placing a path of low resistance in parallel with it. The n^+-emitter diffusion has the lowest sheet resistance of all the diffusions in the process (3,7 Ω/□) and is the obvious choice. If the base diffusion strip is widened from 28 μm to 52 μm or 16 μm wide strip of emitter diffusion may be inserted into the region and periodically connected to the base region by means of metallization to ensure a good ohmic contact. The base resistance is now negligible in comparison to that of the n^+-strip. The packing density has been considerably degraded but is still superior to that attainable with diode arrays.

4.6 Comparison of structures

All the structures considered are similar, in that each of them uses a pn-junction (either a diode or the base-emitter junction of a transistor) as a decoupling element. The physical characteristics

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TABLE I

Structure	Cell area (μm^2)	Aspect ratio	Packing density (mm^{-2})	Resistance (Ω)
Common-anode (Base-emitter) diode	1 536	2,67	651	30
Common-cathode (Collector-base) Diode	1 824	3,17	548	12
Schottky diode	1 632	2,83	612	30
Emitter-follower transistor	864	1,5	1 157	86
Emitter-follower transistor with n^+ strip	1 440	2,5	694	5,5

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of these structures are compared in Table I. The resistance per cell has been included here as it is also strongly geometry-dependent. From the point of view of functional density, the com=mon collector transistor array with an n^+-strip would be the best choice, as it has a high packing density and a low resistance, enabling large arrays to be formed.

Table II compares the electrical performance of commercial devices using some of the technologies discussed. The structures are compared on a basis of power consumption, propagation delay and the product of these two, known as the power-delay product. Because the structures are electrically similar, it is understandable that their power-delay products are also very similar. The lower values are achieved by means of special technology such as SOS-diodes (which have very low stray capacitance) and Schottky diodes (which have no excess stored charge). Using conventional silicon diodes suitable for process 1A, a power-delay product of about 7 pJ could be achieved. The power-delay product expresses the amount of energy required to change the logical state of devices. As such it is a useful measure of the 'efficiency' of a digital logic element. If delay time is plotted against power consumption on a double logarithmic scale (Fig. 4.9), a constant power-delay product may be represented by a straight line as shown. While a low power-delay product is desirable for a logic family, the power consumption and propagation delay must also conform individually to certain re=strictions.

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TABLE II

Device	Technology	Delay per element (ns)	Power consumption per element (µm)	Power-delay product (pJ)
National DM 7575	Silicon diodes	45	159	7,1
Rockwell P/N 15900	Silicon-on-sapphire diodes	25	85	2,1
Signetics 825100	Schottky diodes in the AND-array, Emitter-followers in the OR-array	25	148	3,7

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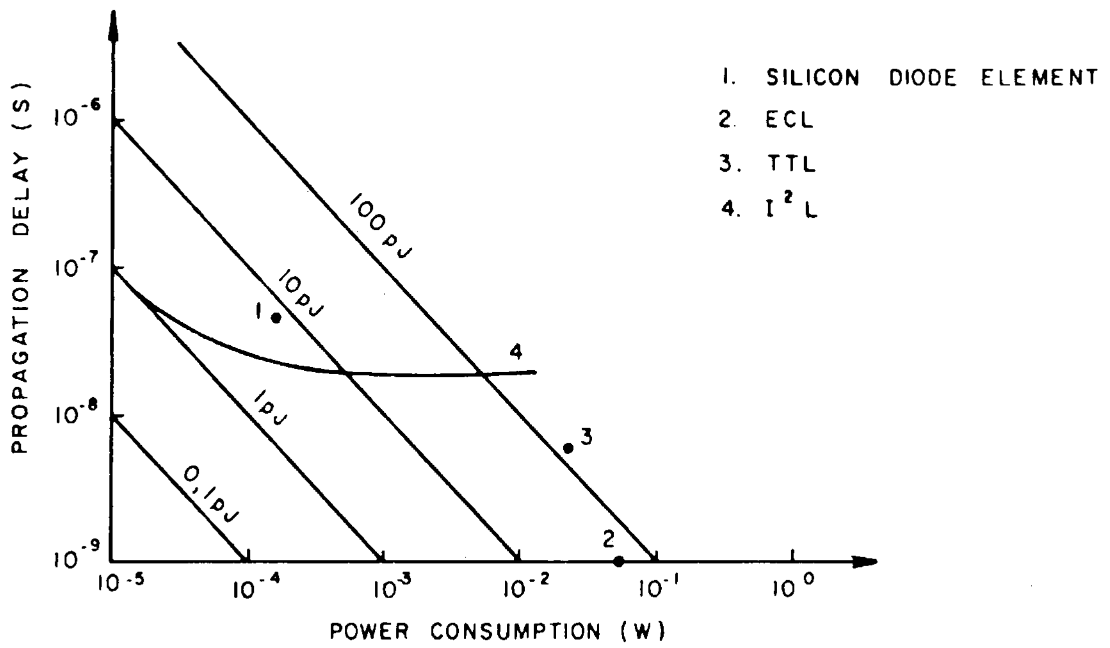

Fig. 4.9: Propagation delay vs power consumption for different logic families

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1. The maximum power consumption is always limited, either by the maximum chip temperature allowable or by power-supply considerations (e.g. portable battery-operated equipment).
2. The maximum delay is limited by the maximum clock fre= quency at which the circuit must operate.

The most suitable logic family for a given application will be one which satisfies the above criteria and which has the lowest power-delay product. Returning to the specifications of Chapter 1 we find that the trade-off between power consumption and maximum frequency of the silicon diode array is not particularly suitable, despite its relatively low power-delay product (7 pJ, compared to 140 pJ for TTL and 55 pJ for ECL)[10]. Assuming negligible delays in the interface circuitry, a maximum clock frequency of 1 MHz im= plies a total propagation delay of less than half a clock period, or 500 ns. Assuming identical elements in both AND- and OR-arrays, this means a delay of 250 ns per cross-point element. The diode-array elements can switch five times faster than this, but at the expense of a high power consumption. It is possible to reduce the power consumption and increase the delay by using high-valued pull-up resistors, but this makes the resistors very large, thus reducing the packing density.

4.7 Integrated injection logic (I^2L)

Integrated injection logic[28], also known as merged transistor logic (MTL)[29] or multi-collector logic (MCL)[30], is a comparatively new

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bipolar logic family. Its most important features are a high functional density, a low power-delay product, and the ability to program the speed-power trade-off to suit a particular appli= cation. It can be produced on a standard bipolar production line with little process alteration.

Fig. 4.10(a) shows direct-coupled transistor logic (DCTL) gates with a resistor load in the collector circuit of each gate. The value of the resistor defines the working point of the gate and hence its power consumption. The transistors are always either off or saturated, and virtually all the power is dissipated in the load resistors. The power consumption per gate is therefore approximately

$$P_g = \frac{Vcc^2}{R_L}$$

If the resistor is made of material of sheet resistance R_s, and the minimum strip-width allowable is W, the resistor requires an area of

$$\begin{aligned} A_R &= \text{number of squares x area of one square.} \\ &= n.W^2 \\ &= \frac{R_L}{R_s} . W^2. \\ &= \frac{Vcc^2 . W^2}{R_s . P_g} \\ &= \frac{k}{P_g} \end{aligned}$$

with $$k = \frac{Vcc^2 . W^2}{R_s}$$

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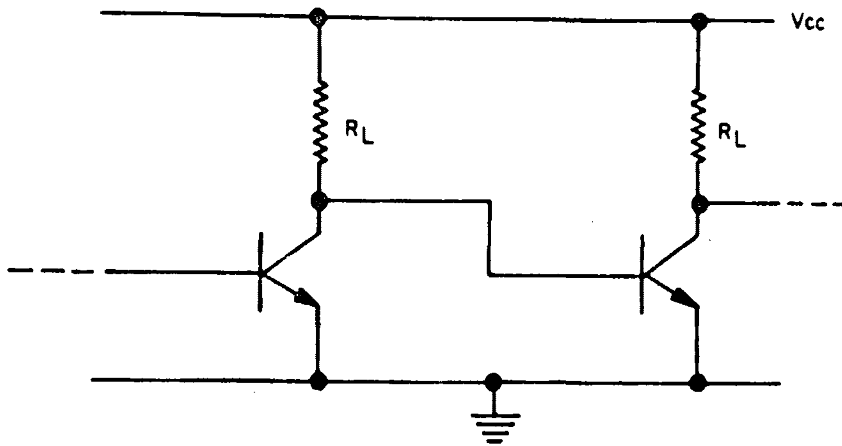

Fig.4.10(a) DCTL gates with resistor loads

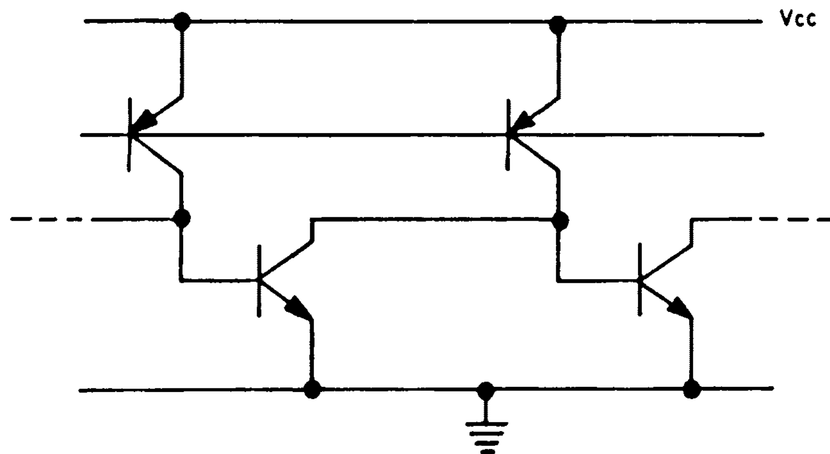

Fig.4.10(b) DCTL gates with pnp-transistor loads

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Thus power consumption can only be reduced by decreasing the packing density. If, on the other hand, the resistor is re=placed by an active load in the form of a pnp-transistor opera=ting as a current source (Fig. 4.10(b)), the area of the load de=vice is independent of the power level, which may be defined by suitably biasing the pnp-transistors. For the same operating current, the power dissipation in the pnp-transistor is the same as in the resistor of the DCTL-gate and is also virtually the total dissipation of the gate. This can be reduced by lowering the supply voltage Vcc. An argument against this is that the voltage noise margin is reduced because the logical '1' voltage level is now closer to the logical '0' level. However, this is not such a serious problem as it may seem, for two reasons:

1. In an LSI circuit, capacitive and inductive coupling is minimized by the small dimensions of all components and interconnections.
2. While the voltage noise margin is low, the power noise margin is still fairly high, because there is always a low impedance path to ground in the circuit.

In I^2L the supply voltage is reduced to the minimum necessary to still switch the npn-transistors on, namely one base-emitter diode voltage drop of about 0,7 V. The bases of the pnp-transistors may now be biased simply by connecting them to ground.

One of the main reasons for the lower packing density of bi=polar circuits is the necessity for isolation between transistors (unlike single channel MOS-technology). Although npn-transistors

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are usually operated in a common emitter-mode, it is in fact the transistor's collector which is formed by the bulk material of the epitaxial layer, and without isolation all the collectors would form a common region. If, however, the transistors are ope= rated in the inverted mode, i.e. the emitter is treated as the collector and vice versa, then the isolation may be dispensed with and the epitaxial layer and buried n^+-layer will form a com= mon emitter region and a ground plane for all the transistors. The advantage of grounding the bases of the pnp-transistors is now evident: the pnp- and npn-transistors may now be merged together as shown in Fig. 4.11(a). The epitaxial layer forms both the base of the pnp- and the emitter of the npn-transistor, while the right-hand p-region forms the base of the npn and the collector of the pnp (hence the name 'merged transistor logic'). Fig. 4.11(b) shows the realization of the same circuit using conventional isolated structures. There is a great saving of area in the I^2L structure because of the omission of the p^+-isolation and the merging of the two transistors.

Fig. 4.12(a) shows the DCTL implementation of logic functions. Each inverter decouples the signal so that the wired AND of any two or more signals may be formed. Obviously the wired-AND principle can be applied to I^2L too. Note, however, that transistors T_1 and T_2 can be replaced by a single transistor with two collectors. Such a structure is not possible using conventional transistors but is easily realized in I^2L. Fig. 4.12(c) shows a 4-collector I^2L

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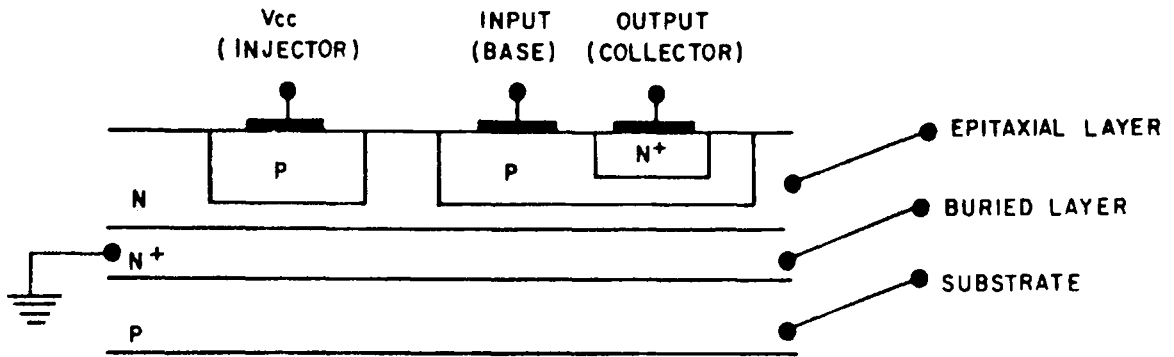

Fig.4.11(a) I^2L cell

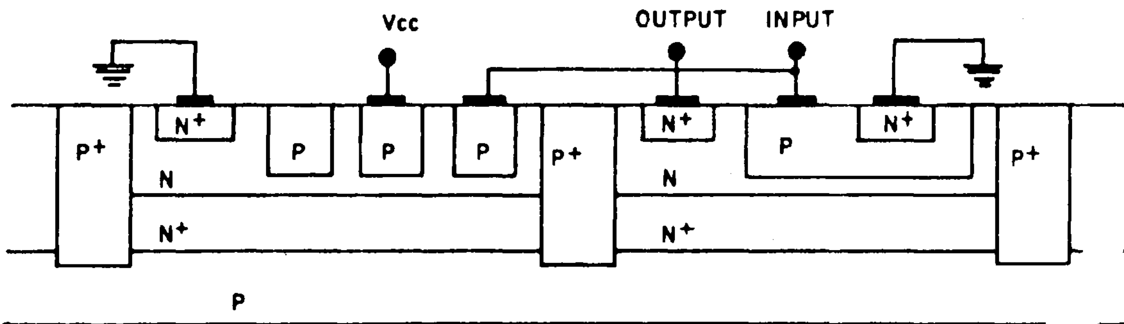

Fig.4.11(b) Same circuit with conventional structures

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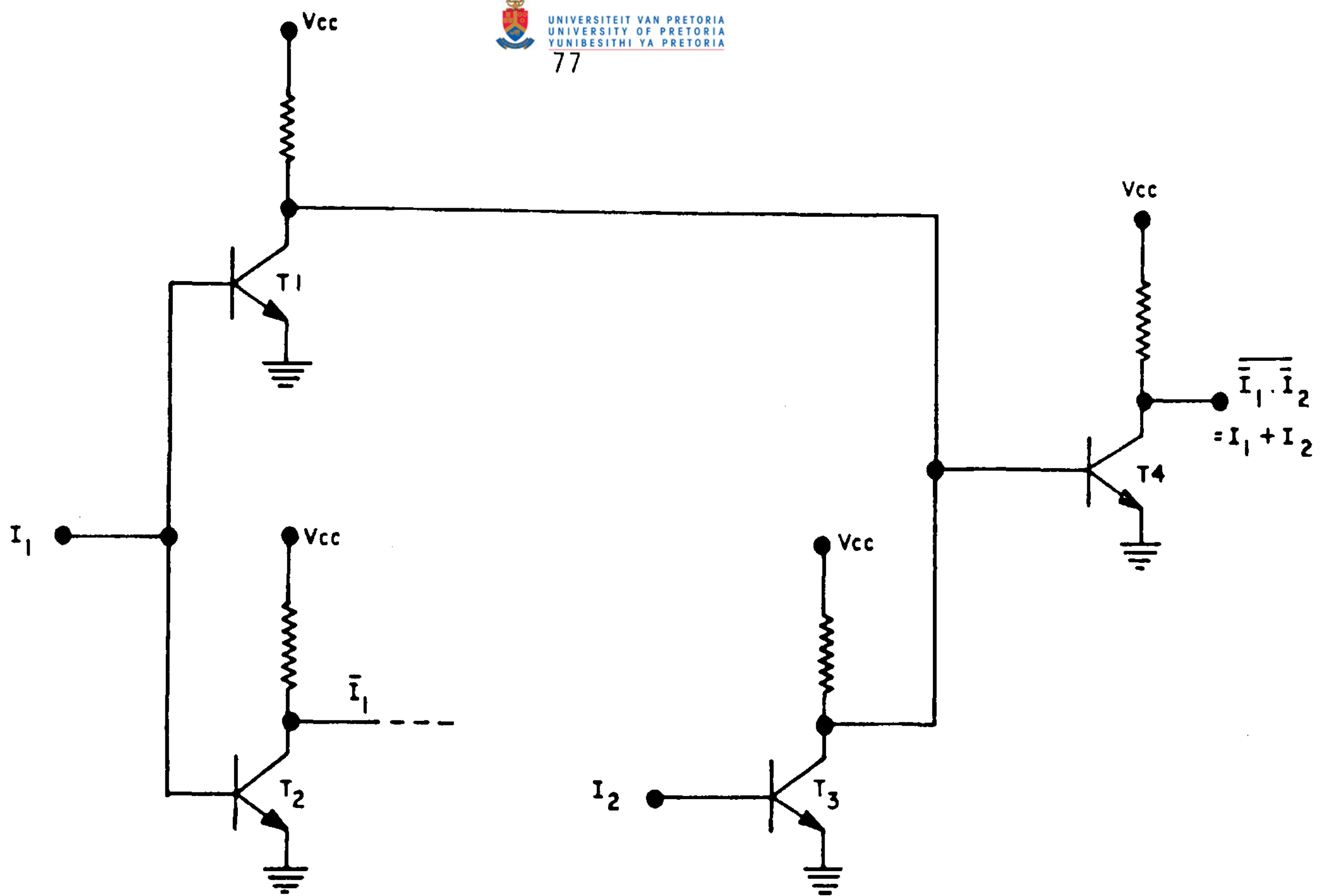

Fig.4.12(a) DCTL OR-gate

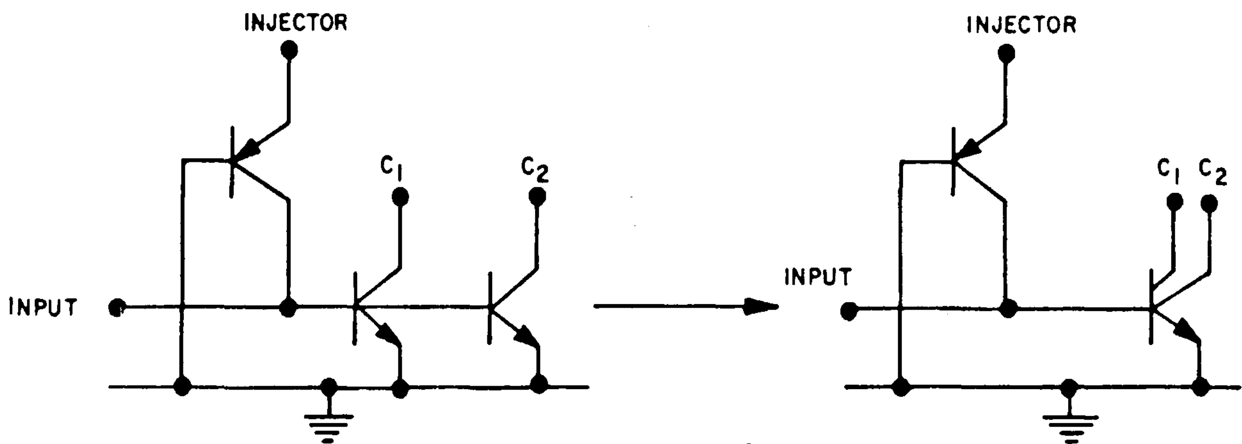

Fig.4.12(b) Merging I^2L npn transistors

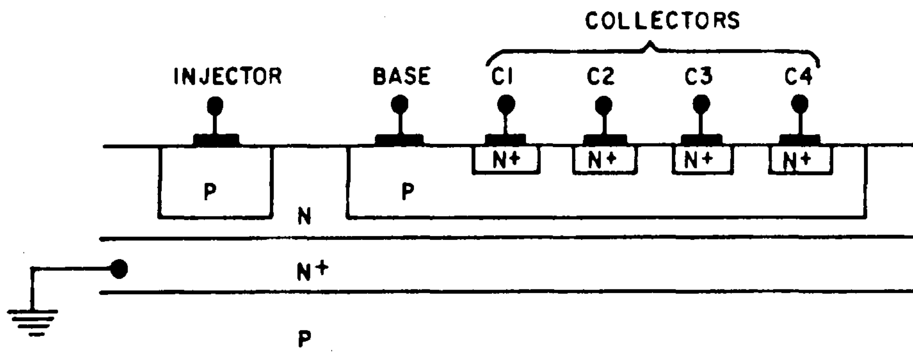

Fig.4.12(c) Four-collector I^2L gate

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gate. An I^2L cell has a fan out equivalent to the number of collectors it possesses.

Because the npn-transistor is operated 'upside down' it is understandable that it will have a low gain in the upward direction, the structure being optimized for downward gain. However, because the pnp-transistors inject identical currents into its base and collector, the requirement for correct opera= tion is only that the effective upward current gain be greater than unity, which is easily obtainable over several decades of current. The current injected into the circuit is defined by the base-emitter voltage of the pnp-transistors, and increases at a tempo of one decade of current per 60 mV of base-emitter voltage. Thus, by a small variation of the supply voltage, it is possible to program the operating point over a wide range (typically from 1 nA to 10 mA per gate). The power-delay product of I^2L is one of the lowest attainable. A figure of 0,12 pJ has been obtained with a structure produced at NEERI, and lower values may be poss= ible, with more optimized technology . The reasons for these low values are:

1. The power dissipation in the load elements has been mi= nimized by reducing the supply voltage to 0,7 V.
2. Because the logic voltage swings are so small (V_{be} - $V_{ce(sat)}$, the junction and stray capacitances in the cir= cuit can be charged and discharged quicker, resulting in smaller delays.

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3. Because of the small dimensions used, junction and stray capacitances are small.

4.8 Conclusions

I^2L is a high-density logic family compatible with standard bipolar processes. Its electrical characteristics may be programmed to suit the requirements of the PLA, unlike the conventional diode and transistor arrays. The development of a PLA-structure based on the I^2L gate is described in detail in the following chapter.

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CHAPTER 5

5. THE DESIGN OF I^2L STRUCTURES SUITABLE FOR USE IN A PLA

5.1 Recombination processes

At low injection levels the characteristics of bipolar devices be= come completely dominated by carrier recombination effects. In a perfect crystal lattice, electrons and holes are unlikely to recombine directly owing to the energy bandgap separating the conduction and valence bands. According to the Schockley-Read-Hall model[33] the recombination rate of carriers is greatly in= creased in practice by the presence of recombination-generation centres, or traps. Physically, these consist of dislocations in the crystal lattice, substitutional or interstitial impuri= ty atoms trapped in the lattice, or surface defects. In terms of the energy-band model, a trap may be considered as having a discrete energy level lying somewhere in the forbidden gap (see Fig. 5.1(a)). Such an energy level is accessible by both holes and electrons. Two recombination and two generation processes are possible[34] (Fig. 5.1(b)):

1. The trap is occupied by an electron. A hole moves from valence band to trap and recombines with the electron (re= combination process).
2. The trap is occupied by an electron which moves into the conduction band (generation process).
3. The trap is occupied by a hole. An electron moves from conduction band to trap and recombines with the hole (re= combination process).

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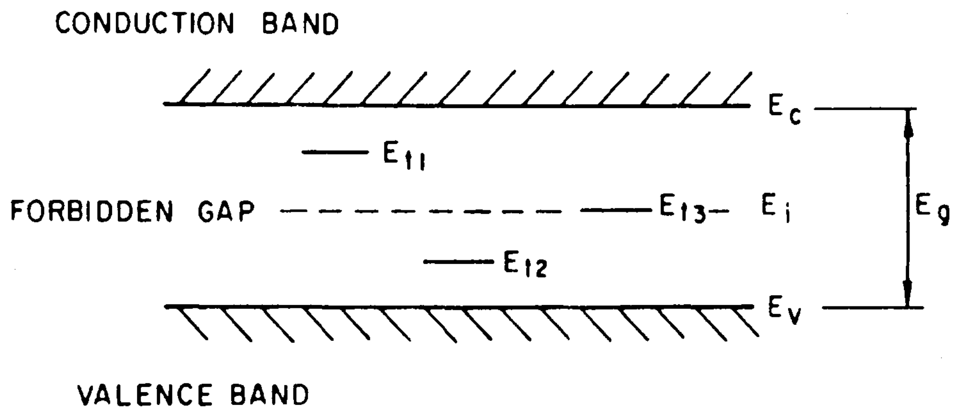

Fig.5.1(a) Energy band model of traps

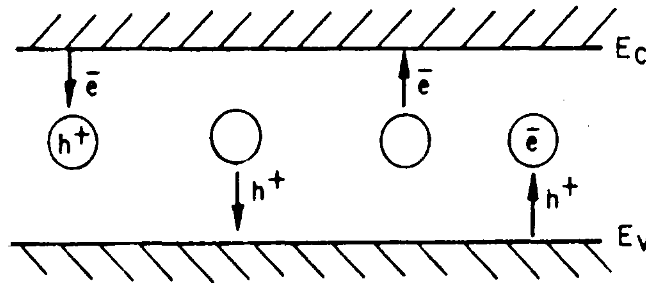

Fig.5.1(b) Generation/recombination processes

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4. The trap is occupied by a hole which moves into the valence band (generation process).

In order to be an efficient recombination centre, a trap must have a roughly equal chance of capturing either a hole or an electron. This implies that the traps having the greatest effect on device performance will be those whose energy levels lie at the intrinsic level, equidistant from conduction and va= lence bands. The density of traps is considered constant through= out the energy bandgap, but the traps near the intrinsic level will be the most effective. Also, as no generation processes oc= cur in forward-biased junctions, only recombination will be re= considered.

Recombination processes will be considered in three regions in the pn-diode in Fig. 5.2(a):

1. In the p-region[35]. At the edge of the space-charge layer $n_p(o) = \bar{n}_p$. For the non-equilibrium condition shown, $\bar{n}_p.\bar{p}_p = n_i^2 e^{\frac{qV}{kT}}$. Assuming total ionization of acceptor inpurities, $\bar{p}_p = N_A$. Therefore

$$n_p(o) = \bar{n}_p = \frac{n_i^2 e^{\frac{qV}{kT}}}{N_A} \qquad (5.1)$$

The electron current density injected into the p-region depends on the gradient of $n_p(o)$ (assuming no drift field exists):

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$$J_n = q\, D_n \frac{dn_p(o)}{dx} \tag{5.2}$$

As a boundary condition we assume that the recom= bination rate is zero at the contact, i.e.

$$U_s = s\,(n_p\,(w_p) - \bar{n}_p) = 0$$

Electrons injected as minority carriers into the p-region will find that many of the traps are filled by holes and some of the electrons will fall into these traps, and recombine with the holes. The rate at which this re= combination process takes place may be characterized by means of a lifetime parameter τ_n, which is the average time before recombination. A diffusion length may also be defined as the average distance that an electron will cover before recombination, and is found to be

$$L_n = \sqrt{D_n\, \tau_n}$$

Using the given boundary condition, the solution of equation 5.2 is

$$J_n = \frac{q\, D_n\, n_i^2\, (e^{\frac{qV}{kT}} - 1)}{N_A\, L_n \tanh (\frac{W_p}{L_n})} \tag{5.3}$$

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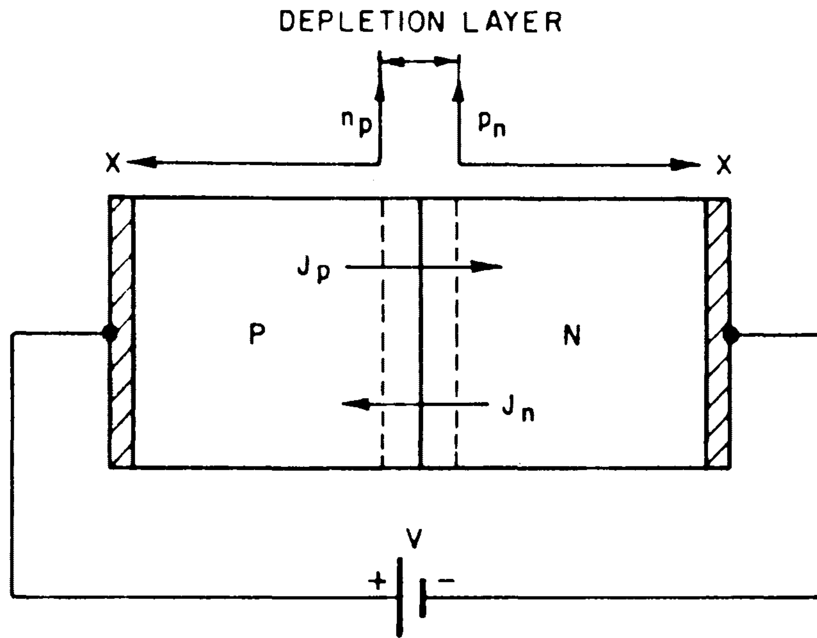

Fig.5.2(a) Bulk recombination in a pn diode

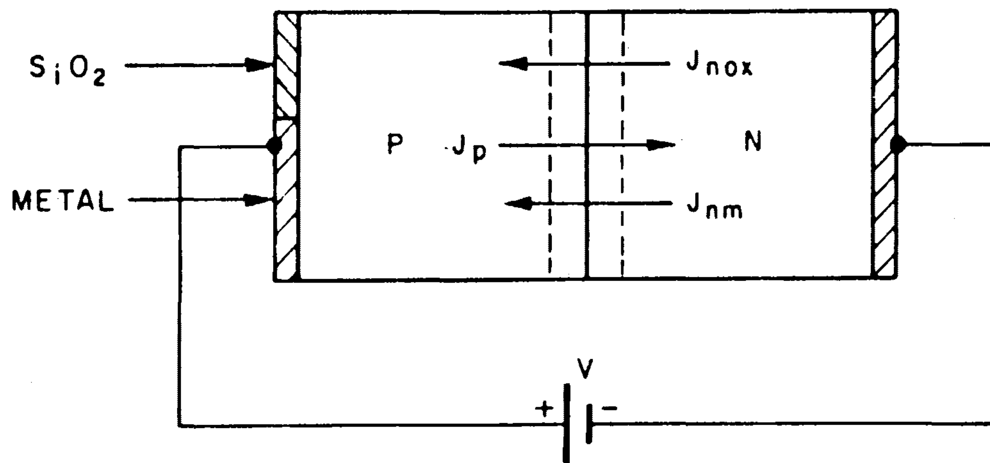

Fig.5.2(b) Surface recombination in a pn diode

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The magnitude of the diffusion current flowing across the junction therefore depends on the recombina= tion rate on the opposite side of the junction. Thus far we have assumed a recombination rate of zero at the termination of the p-region. In the case where the region is terminated by an interface with a finite recombination velocity s (such as an npp^+ diode), equation 5.3 may be written in a different form, i.e.:

$$J_n = \frac{q\, s\, n_i^2 \, (e^{\frac{qV}{kT}} - 1)}{N_A}$$

2. In the n-region. This region may be treated by analogy with the p-region. Let $L_p = \sqrt{D_p \tau_p}$.

$$\bar{n}_n = N_D$$

$$\therefore\ p_n(o) = \frac{n_i^2}{N_D} e^{\frac{qV}{kT}}$$

$$\therefore\ J_p = \frac{q\, D_p\, n_i^2 \, (e^{\frac{qV}{kT}} - 1)}{N_D\, L_p \tanh\left(\frac{W_n}{L_p}\right)} \qquad 5.4$$

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3. In the space-charge region[34]. In an intrinsic semiconductor the concentrations of holes and electrons are equal, i.e. $p = n = \bar{n} = \bar{p}$. But

$$\bar{p} \cdot \bar{n} = n_i^2 \, e^{\frac{qV}{kT}}$$

$$\therefore \bar{p} = \bar{n} = \sqrt{n_i^2 \, e^{\frac{qV}{kT}}}$$

$$= n_i \, e^{\frac{qV}{2kT}} \qquad 5.5$$

The rate at which electrons in the conduction band drop into traps occupied by holes is

$$U_{cp} = \frac{n.f_{tp}}{\tau_{no}}$$

The rate at which holes in the valence band drop into traps occupied by electrons is

$$U_{vn} = \frac{pf_{tn}}{\tau_{po}}$$

Assuming that $f_{tp} = f_{tn} = \frac{1}{2}$ and $\tau_{po} = \tau_{no} = \tau_o$ the recombination rate at the pn-junction is

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$$U_{rp} = U_{rn}$$

$$= U_r$$

$$= n_i^2 \, e^{\frac{qV}{2kT}} \cdot \tfrac{1}{2} \cdot \frac{1}{\tau_o}$$

$$= \frac{n_i \, e^{\frac{qV}{2kT}}}{2 \, \tau_o}$$

It may be shown that the recombination rate declines exponentially with distance on either side of the junction with a characteristic length of $\frac{kT}{qE}$, where $E = \frac{\psi - V}{W}$, the electric field strength. Thus

$$U_r(x) = e^{\frac{-x \, q \, E}{kT}} \cdot \frac{n_i \, e^{\frac{qV}{2kT}}}{2 \, \tau_o}$$

The recombination current density in either the p or the n -half of the space charge layer is therefore

$$J_r = q \int_o^{\frac{W}{2}} U_r(x) dx$$

$$= q \, U_r(o) \int_o^{\frac{W}{2}} e^{\frac{-xqE}{kT}} dx$$

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$$= q\ U_r(o) \int_o^{\infty} e^{\frac{-xqE}{kT}}\ dx$$

$$= q.\ \frac{kT}{qE}\ .\ \frac{n_i\ e^{\frac{qV}{2kT}}}{2\ \tau_o}$$

The total recombination current for both halves of the space charge layer is twice this value:

$$J_{rt} = 2\ J_r$$

$$= \frac{kT\ n_i\ e^{\frac{qV}{2kT}}}{E\ \ \tau_o} \qquad 5.6$$

Another form or recombination which must be taken into account at low current levels is recombination at silicon-silicon dioxide interfaces[36]. We assume that part of the p-region of the diode is terminated by a layer of thermally grown SiO_2. At this surface the regular crystal structure of the silicon is interrupted and the silicon atoms form bonds with atoms of oxygen at high temperatures, to form silicon dioxide. However, the available bonds are not all saturated by oxygen atoms at the silicon-silicon dioxide interface, and the remaining bonds exhibit a strong attraction for impuri= ties. These unsaturated bonds give rise to a number of energy

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levels within the bandgap, known as surface states or Tamm-Schockley states[35]. Apart from these fast surface states, a number of silicon ions also become trapped within the oxide layer as it is grown, resulting in a permanent, positive stored charge. As a result of the principle of charge neutrality, a negative charge develops on the silicon side of the interface, causing a space-charge layer to be formed there. When the diode is forward-biased, recombination takes place at the fast surface states within this space-charge layer. The recombination current density at the surface de= pends on the following factors:

1. The condition of the surface, characterized by the surface recombination velocity s and the surface potential $\emptyset_s$.
2. The carrier densities at the surface (holes and elec= trons). These depend on the deviation from equilibrium caused by the forward-biasing of the pn-junction and are exponentially related to the applied voltage and the surface potential.

The recombination velocity is a measurable constant for a given process. From the device modelling viewpoint we wish to determine the relationship between surface recombination current density and forward bias. This is difficult unless a simplifying assumption is made regarding the surface potential. For a p-type region the carrier densities at the surface are

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$$n_s = n_p e^{\frac{q(V + \phi_s)}{kT}}$$

$$= \frac{n_i^2}{N_A} e^{\frac{q(V + \phi_s)}{kT}}$$

and $$p_s = N_A e^{-\frac{q\phi_s}{kT}},$$

which yields an unwieldly solution for a general value of ϕ_s. If it is assumed that $\phi_s = \phi_{fp} - \frac{1}{2} V$, the carrier den= sities become

$$n_s = p_s = n_i e^{\frac{qV}{2kT}}$$

Fitzgerald and Grove[36] show that the recombination current density is then a maximum and is

$$J_{rs} = \frac{2 q s n_i}{\pi} \cdot \frac{q V}{2kT} \cdot e^{\frac{qV}{2kT}} \qquad 5.7$$

In the case where one carrier density is much higher than the other, the recombination current density would be great= ly reduced (recombination requiring the presence of both car= rier types) and its dependance on applied voltage would be

$$e^{\frac{qV}{nkT}},$$

where n is called the emission coefficient and has a value

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between 1 and 2. In practice the value of n depends on the nature of the surface.

5.2 A static model of the I^2L cell at low and medium injection levels

The static characteristics of the I^2L cell introduced in the pre= vious chapter will now be examined. The approximate model which will be developed is applicable under conditions of low and medium injection - high injection effects such as ohmic voltage drops in the base and 'emitter crowding' have been neglected. The model is based on the injection model of Berger[37], in which lateral current redistribution effects are ignored. Kirschner[38] has shown that this assumption leads to inaccuracy in the calculation of the current gain of the npn transistor and has developed a two-dimensional model of the current components in the base. However, as the purpose of this analysis is to gain insight into the factors influencing I^2L performance at low currents rather than the accurate prediction of this performance, the simpler Berger model is adequate.

Fig. 5.3 shows a section and plan of a typical I^2L cell. The structure may be analysed by partitioning the base region into equally-sized regions surrounding each collector or base contact.[10,37] A cell with a fan out of F will have F + 1 such regions. The fol= lowing current components are shown:

1. The forward hole injection current I_{pf} in the lateral pnp transistor. Neglecting surface and bulk recombination in the pnp base this component is entirely collected by the pnp collector ($\alpha \doteqdot 1$) and supplies the base current for the ver= tical npn transistor.

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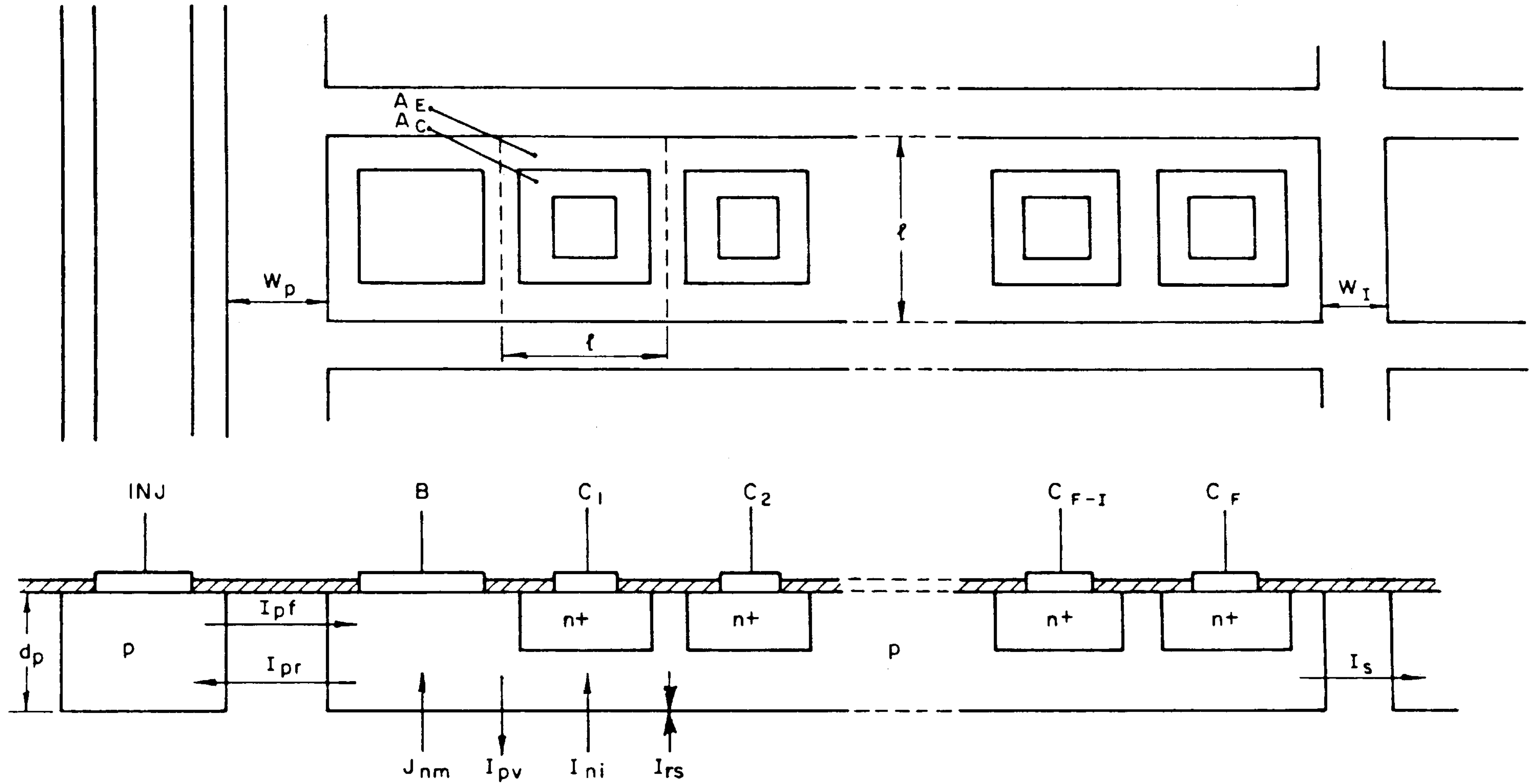

Fig. 5.3: Current components in the I^2L cell

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$$I_{pf} = \frac{q\ A_p\ D_p\ n_i^2\ (e^{\frac{q\ V_{inj}}{kT}} - 1)}{N_D\ L_p\ \tanh\ (\frac{W_p}{L_p})}$$

$$\doteqdot J_{pfs}\ A_p\ e^{\frac{q\ V_{inj}}{kT}} \qquad 5.8$$

2. The reverse hole injection current I_{pr} in the lateral pnp transistor. This component exists because the pnp is saturated when the cell is ON. Analogous to I_{pf},

$$I_{pr} = \frac{q\ A_p\ D_p\ n_i^2\ (e^{\frac{q\ V_{be}}{kT}} - 1)}{N_D\ L_p\ \tanh\ (\frac{W_p}{L_p})}$$

$$\doteqdot J_{prs}\ A_p\ e^{\frac{q\ V_{be}}{kT}} \qquad 5.9$$

3. The vertical electron current in the intrinsic base of the npn transistor. For base widths $W_B << L_n$ we may assume a base transport factor of unity, i.e.

$$I_c = I_{ni} = \frac{q\ A_c\ D_n\ n_i^2\ \ e^{\frac{q\ V_{be}}{kT}}}{\int_o^{W_B} N_A(x)\ dx}$$

for a non-homogeneous base doping $N_A(x)$.

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$$\therefore I_c = J_{nis} A_c e^{\frac{q V_{be}}{kT}} \quad 5.10$$

4. The vertical electron current I_{nm} injected under the metal contact.

$$I_{nm} = \frac{q A_m D_n n_i^2 e^{\frac{q V_{be}}{kT}}}{\int_o^{d_p} N_D(x) \, dx}$$

$$= J_{nms} A_c e^{\frac{q V_{be}}{kT}} \quad 5.11$$

assuming $A_m = A_c$.

5. The vertical electron current I_{no} injected into the oxide covered base region. The exact expression for this current is not known, but as has been shown its maximum possible value is

$$I_{no} = \frac{q^2 (A_E - A_c) (F + 1) s_o n_i V_{be} e^{\frac{q V_{be}}{2kT}}}{\pi kT}$$

Assume a general equation

$$I_{no} = J_{nos} (A_E - A_c) (F + 1) e^{\frac{q V_{be}}{nkT}} \quad 5.12$$

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with $1 \leqslant n \leqslant 2$ and small variation in V_{be}.

6. The vertical hole current I_{pv} injected into the epitaxial layer and buried n^+ layer.

$$I_{pv} = \frac{q\, A_E\, (F + 1)\, s_B\, n_i^2}{N_D'}\, e^{\frac{q V_{be}}{kT}}$$

where $N_D' > N_D$ as a result of the buried layer outdiffusion.

$$\therefore\ I_{pv} = J_{pv}\, A_E\, (F + 1)\, e^{\frac{q V_{be}}{kT}} \qquad 5.13$$

7. The recombination current (holes and electrons) which flows to the space-charge layer of the emitter-base junction.

$$I_{rs} = \frac{kT\, n_i\, A_E\, (F + 1)}{E\, \tau_o}\, e^{\frac{q V_{be}}{2kT}}$$

$$= J_{rss}\, A_E\, (F + 1)\, e^{\frac{q V_{be}}{2kT}} \qquad 5.14$$

for small changes in V_{be}.

8. The lateral hole current I_s which flows out of the side-walls. This current is a particular problem in the case of non-isolated structures.

$$I_s = \frac{q\, A_s\, (2\,(F + 1) + 1)\, D_p\, n_i^2}{N_D\, L_p\, \tanh\left(\frac{W_s}{L_p}\right)}\, e^{\frac{q V_{be}}{kT}}$$

$$= J_{ss} A_s\, (2F + 3)\, e^{\frac{q V_{be}}{kT}} \qquad 5.15$$

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Other currents which have been neglected are recom=bination currents in the space-charge layer of the collector-base junction, bulk and surface recombination in the base of the npn transistor and between cells and hole and electron currents flowing between the injector and the buried layer.

The effective upward current gain per collector is given by the equation

$$\beta_u = \frac{I_c}{\Sigma I_B}$$

$$= \frac{I_c}{I_{pr} + I_{nm} + I_{no} + I_{pv} + I_{rs} + I_s}$$

$$= \frac{J_{nis} A_c e^{\frac{q V_{be}}{kT}}}{J_{prs} A_p e^{\frac{q V_{be}}{kT}} + J_{nms} A_c e^{\frac{q V_{be}}{kT}} + J_{nos} (A_E - A_C)(F+1) e^{\frac{q V_{be}}{nkT}} + J_{pvs} A_E (F+1) e^{\frac{q V_{be}}{kT}} + J_{rss} A_E e^{\frac{q V_{be}}{2kT}} + J_{ss} A_s (2F+3) e^{\frac{q V_{be}}{kT}}} \qquad 5.16$$

in the medium, low and very low injection regions. The common base current gain α_p of the lateral pnp transistor is also of some importance. In the model used only medium injection effects in the pnp transistor are included, and so the model does not predict the fall-off of α_p at low currents. This is not very serious, as the percentage fall-off

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of α_p is much smaller than that of β_u. Assuming that the base transport factor is close to unity, α_p is approxi= mately equal to the emitter injection efficiency, which is

$$\alpha_p = \frac{I_{pf}}{I_{pf} + I_{nr}}$$

$$= \frac{\frac{q A_p D_p \bar{p}_n}{W_p} e^{\frac{q V_{inj}}{kT}}}{\frac{q A_p D_p \bar{P}_n}{W_p} e^{\frac{q V_{inj}}{kT}} + \frac{q A_p D_n \bar{n}_p}{L_n} e^{\frac{q V_{inj}}{kT}}}$$

$$= \frac{1}{1 + \frac{D_n \bar{n}_p W_p}{D_p \bar{p}_n L_n}} \qquad 5.17$$

What are our goals when attempting to optimize I^2L static performance? We wish to develop devices which function correctly over a wide range of current values and with minimal power consumption at all times. The first requirement indicates a minimum value for β_u of somewhat greater than 1 over a wide current range. Although a cell will operate when $\beta_u = 1$, a value of 2 is more practical in view of noise margin conside= rations[39]. With regard to the second requirement, consider

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the power consumption of a cell at a given value of collector current:

$$P_g = V_{inj} I_{inj}$$

$$= \frac{V_{inj} I_c}{\alpha_p \beta_u}$$

Thus for minimum power consumption we must maximize $\alpha_p\beta_u$ while maintaining a value of $\beta_u > 2$. Because of the standard process used, only limited modifications to the pro= cess are permissible. However the following two processes represent little deviation from standard processing and greatly improve performance.

1. Reduction of the epitaxial layer thickness from 10 μm to 6,5 μm. This has the effect of bringing the buried n^+ layer much closer to the p-base region than in the case of a normal transistor. As the buried layer outdiffuses (especially during the long iso= lation drive-in step) it tends to raise the donor con= centration in the emitter near the emitter-base junc= tion. This reduces the vertical injection of holes into the emitter (I_{pv}), thereby improving the emitter injection efficiency. It is then also permissible to reduce iso= lation drive-in time from 16 hours to about 7 hours as a large outdiffusion of the buried layer and a large in- diffusion of the p^+ isolation are not necessary. A

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problem can arise here though, as a result of the $\pm$10% tolerance of the epitaxial layer thickness. If the layer is too thick poor emitter injection effi= ciency is obtained, while if it is too thin break= through to the collectors is possible (see Fig. 5.4(a)). This tolerance did prove to be a source of low yield in production devices. Another disadvantage is that conventional transistors produced on the same wafer will have low breakdown voltages, as the outdiffusion of the buried layer will tend to raise the collector do= ping, just as it raises the emitter doping of inverted transistors. This can create problems when designing interface circuits compatible with high voltages (see 5.6). Using a 6,5 μm epi layer, the breakdown voltage has been found to be in the region of 6 V, compared to 12 V for the standard thickness.

2. A modified sintering process which reduces the surface state density. Process 1A rules specify a 15 minute sinter in dry N_2 at 500 °C after etching of the aluminium. It has been established that an alternative sintering method, consisting of a 30 minute sinter in wet N_2 at 450 °C before etching of the aluminium, greatly im= proves the current gain of both pnp and npn transistors at low currents[40 & 41]. The effect of this sintering process is to reduce the surface state density in the

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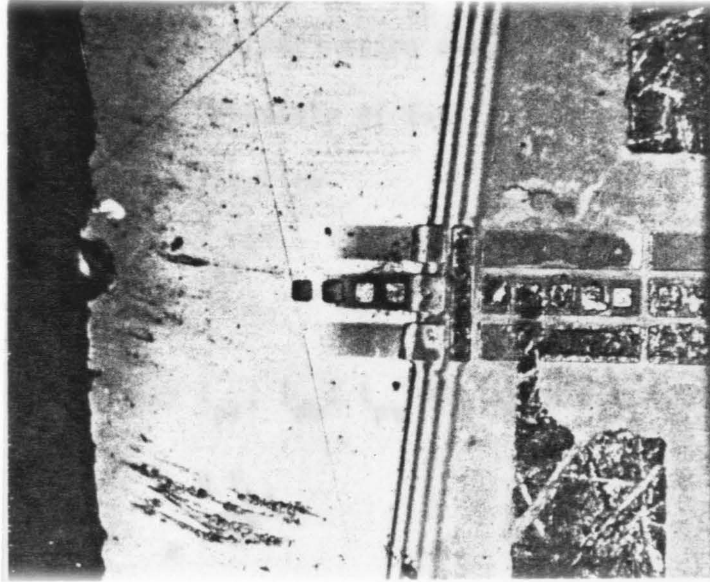

Fig. 5.4(a). Photograph of a Gate (MCL4) Showing Breakthrough of the Buried Layer to the Collectors (1^{0} Bevel and Stain Method)

Fig. 5.4(b). I_c, I_E and I_B as Functions of V_{be}. (MCL2)

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oxide layer covering the base, which reduces the surface recombination current I_{no}. The total base current consists of four current components which are proportional to

$$e^{\frac{q V_{be}}{kT}},$$

namely I_{pr}, I_{nm}, I_{pv} and I_s, a current proportional to

$$e^{\frac{q V_{be}}{2kT}}$$

(I_{rs}) and the surface recombination current I_{no} which is proportional to

$$e^{\frac{q V_{be}}{nkT}},$$

where $1 \leq n \leq 2$. Equation 5.16 may therefore be written in the form

$$\beta_u = \frac{I_{cs}\, e^{\frac{q V_{be}}{kT}}}{(I_{prs} + I_{nms} + I_{pvs} + I_{ss})\, e^{\frac{q V_{be}}{kT}} + I_{rss}\, e^{\frac{q V_{be}}{2kT}} + I_{nos}\, e^{\frac{q V_{be}}{nkT}}}$$

$$= \frac{I_{cs}\, e^{\frac{q V_{be}}{kT}}}{I_{Bs}'\, e^{\frac{q V_{be}}{kT}} + I_{rs}\, e^{\frac{q V_{be}}{2kT}} + I_{nos}\, e^{\frac{q V_{be}}{nkT}}} \qquad 5.18$$

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Fig. 5.4(b) depicts the relationship between V_{be} and I_c, I_E and I_B at low and medium injection levels for an I^2L cell manufactured at the National Electrical Engineering Research Institute (MCL 2; see Appendix A2.2). The value of the emission coefficient may be determined from the slope of these curves, e.g. $n = 1$ corresponds to a slope of 60 mV per decade of current. The collector current which is purely a dif= fusion current has a coefficient of emission very close to unity (1,03), while the n-value of the base current slowly changes from 1,13 at 1 μA to 2 at 100 pA. It has been found empirically that the curvature of I_B can be very accurately approximated by the summation of the three current components shown:

$$I_{B1} = 6,34 \times 10^{-18} \, e^{\frac{q V_{be}}{2kT}}$$

$$I_{B2} = 2,13 \times 10^{-15} \, e^{\frac{q V_{be}}{1,27 \, kT}}$$

$$I_{B3} = 2,53 \times 10^{-12} \, e^{\frac{q V_{be}}{kT}}$$

This is in good agreement with theory, if we as= sume that $I_{rs} = I_{B1}$, $I_{no} = I_{B2}$ and $I'_B = I_{B3}$, and in= dicates an emission coefficient for I_{no} of 1,27. I_B

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and I_c intersect at the point where $\beta_u = 1$, and it is obvious that their intersection is the re=sult of the slow decrease in the magnitude of I_B compared to the I_c at low values of V_{be}, caused by re=combination currents I_{rs} and I_{no}. Reducing the mag=nitude of these components will greatly extend the operating range of the circuit at low currents. Turning now to a structure produced at the production facility (MCL 4, see Fig. 5.5(a)) and Appendix A3.1 with com=pletely standard processing (except for a thinner epi layer) we find an even worse result - the base current is dominated by surface recombination currents with an emission coefficient of 1,6 over many decades of cur=rent and the point at which $\beta_u = 1$ corresponds to $I_c = 0,31$ µA (Fig. 5.5(b)). A second wafer from the same batch was removed from the production line after aluminium evaporation, sintered in wet N_2 and the aluminium etched. The results are shown in Fig. 5.5(b). The component I_{no} of the base current has been reduced by a factor of 130 and the diffusion component is do=minant down to a current of 6 nA below which the emission coefficient begins to increase towards 1,6. I_{rs} has also been greatly reduced by the sinter which improves the condition of the surface where the emitter-base junction intersects it. β_u is still greater than unity

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at 100 pA, the limit for accuracy of the measuring equipment used. The wet-sinter process improves the low current performance by reducing the surface-state density. Hydrogen atoms which are present during the sinter diffuse through the aluminium and combine with the unsaturated bonds at the silicon-silicon dioxide interface.

As these two process modifications cause little dis= ruption of standard processing while greatly enhancing performance they will be incorporated in the production of all I^2L circuits at the National Electrical Engineering Research Institute, including the PLA.

A second approach to device optimization is the development of suitable layout rules. Because of the large number of parasitic currents present, I^2L per= formance is particularly sensitive to changes in layout rules. Our first goal is to try to optimize the $\alpha_p \beta_u$ product. There is some interaction between α_p and β_u as a result of the back-injected hole current I_{pr} which is a significant part of the total npn base current in the medium current regime. Restricting ourselves to current levels where surface and space-charge layer-re= combination is negligible, we may rewrite equation 5.18 a

$$\beta_u = \frac{I_{cs}\, e^{\frac{q V_{be}}{kT}}}{I_{Bs}'\, e^{\frac{q V_{be}}{kT}}}$$

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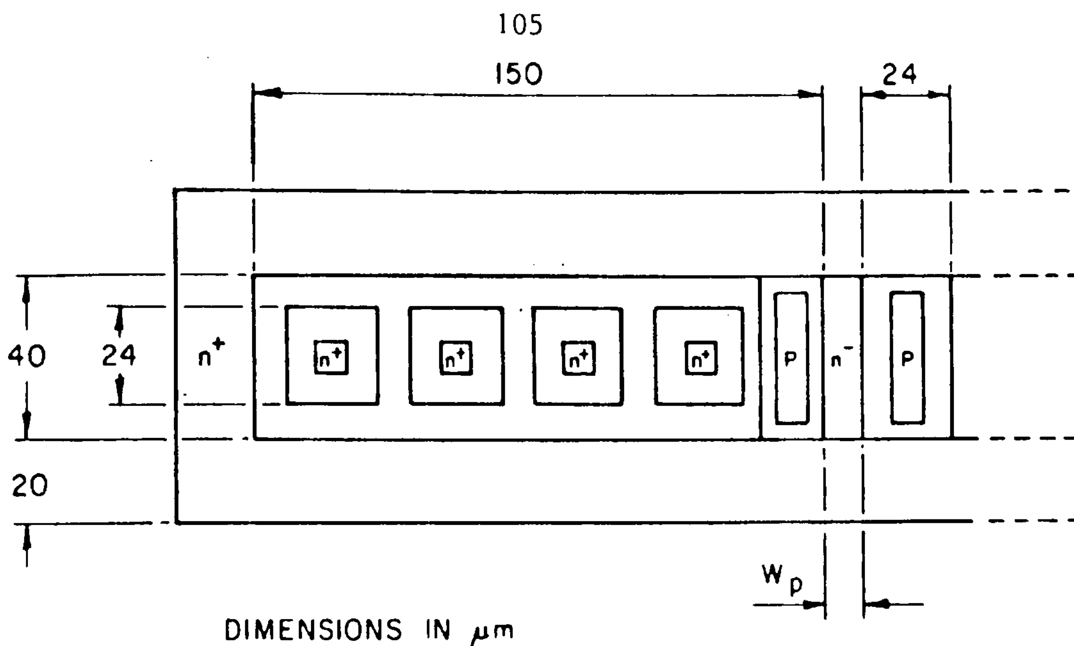

Fig.5.5(a) 4-Collector gate with normal dimensions (MCL4)

Fig.5.5(b) I_c and I_b vs V_{be} (wet and dry sintered devices)

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$$= \frac{I_{cs}}{I_{prs} + I_{nms} + I_{pvs} + I_{ss}}$$

$$\frac{I_{cs}}{\dfrac{q\, A_p\, D_p\, \bar{p}_n}{L_p \tanh\left(\dfrac{W_p}{L_p}\right)} + I_{nms} + I_{pvs} + I_{ss}}$$

$$\div \frac{I_{cs}}{\dfrac{q\, A_p\, D_p\, n_i^2}{N_D\, W_p} + I''_{Bs}}$$

$$\therefore \alpha_p\, \beta_u = \frac{1}{1 + \dfrac{D_n\, N_D\, W_p}{D_p\, N_A\, L_n}} \cdot \frac{1}{\dfrac{q\, A_p\, D_p\, n_i^2}{I_{cs}\, N_D\, W_p} + \dfrac{I''_{Bs}}{I_{cs}}}$$

$$= \frac{1}{(1 + k_1\, W_p)\left(\dfrac{k_2}{W_p}\right) + k_3)}$$

with $k_1 = \dfrac{D_n\, N_D}{D_p\, N_A\, L_n}$, $k_2 = \dfrac{q\, A_p\, D_p\, n_i^2}{N_D\, I_{cs}}$ and $k_3 = \dfrac{I''_{Bs}}{I_{cs}}$.

$$= \frac{W_p}{k_1 k_3 W_p^2 + (k_1 k_2 + k_3)\, W_p + k_2}$$

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which tends to zero when W_p tends to zero or infinity, and has a maximum when

$$\frac{d\alpha_p \beta_n}{d\,W_p} = 0$$

$$\frac{d\alpha_p\,\beta_u}{d\,W_p} = \frac{k_1k_3\,W_p^{\,2} + (k_1k_2+k_3)\,W_p + k_2 - W_p\,(2\,k_1k_3\,W_p + k_1k_2 + k_3)}{(k_1k_3\,W_p^{\,2} + (k_1k_2 + k_3)\,W_p + k_2)^2}$$

and is zero when

$$k_1k_3\,W_p^{\,2} + (k_1k_2 + k_3)\,W_p + k_2 = 2\,k_1k_3\,W_p^{\,2} + (k_1k_2 + k_3)W_p$$

$$\therefore\; k_2 = k_1k_3\,W_p^{\,2}$$

$$\therefore\; W_{p(opt)} = \sqrt{\frac{k_2}{k_1k_3}}$$

$$= \sqrt{\frac{q\,A_p\,D_p^{\,2}\,n_i^2\,N_A\,L_n}{D_n\,N_D^{\,2}\,I''_{Bs}}} \qquad 5.19$$

Although an optimum value of W_p has been shown to exist it is difficult to calculate owing to the large number of process constants in 5.19. If we assume that $I_{nms} << I_{prs} + I_{ss}$ (normally the case), we may write

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$$W_{p(opt)} = k_4 \sqrt{\frac{A_p}{I_{pvs} + I_{ss}}}$$

$$= k_4 \sqrt{\frac{d_p \sqrt{A_E}}{J_{pvs} (F+1) A_E + J_{ss}(2F+3) \sqrt{A_E}}}$$

$$= \frac{k_5}{\sqrt{k_6 \sqrt{A_E} + k_7}}$$

Thus the optimum value of pnp base width is a rather weak function of the size of the npn transistor. This is significant, as it implies that a base width which is found to be optimal for a given structure will also be nearly optimal for larger or smaller structures. An optimal base width for the process used has been established from measurements on six 4-collector I^2L cells having base widths of 6, 8, 10, 12, 14 and 16 μm respectively (see Appendix A3.1). Plotting $\alpha_p\beta_u$ as a function of collector current it was found that a base width of 12 μm gave the best results throughout the medium injection region (see Fig. 5.6). At low currents I_{pr} has little effect on β_u, while at high currents 'emitter crowding' effects dominate.

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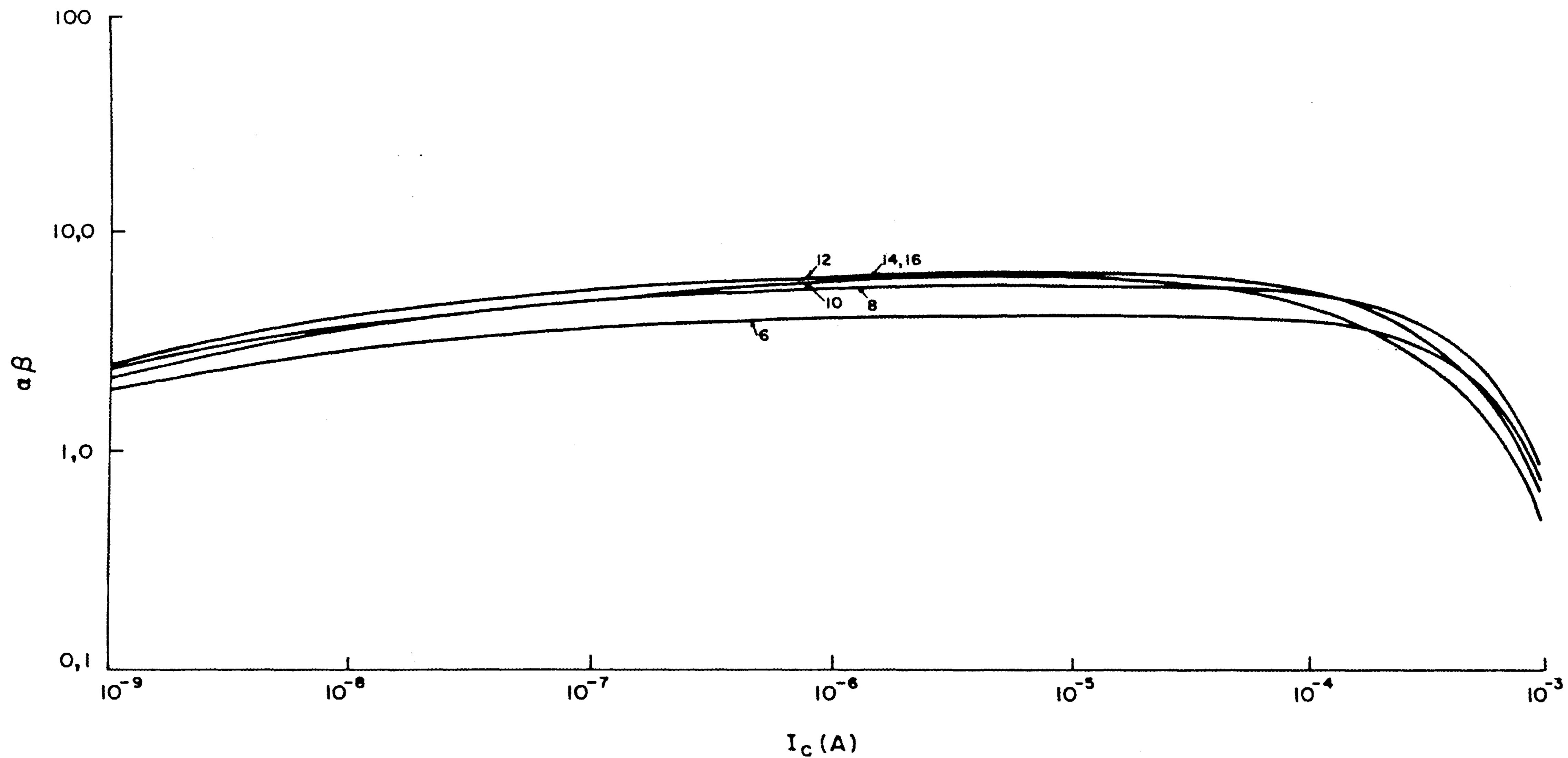

Fig. 5.6: $\alpha_p\beta_u$ vs I_c for a wet-sintered 4-collector cell (MCL 4)

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Having determined the best trade-off possible between α_p and β_u it now remains to maxamize β_u by reducing all other parasitic base current components. Returning once again to equation 5.16 we write it in the following form:

$$\beta_u = \frac{I_c}{\{J_{prs}\, d_p \sqrt{A_E} + J_{nms} A_c + J_{pvs} A_E (F+1) + J_{ss}\, d_p \sqrt{A_E}\}\, e^{\frac{q V_{be}}{kT}} + J_{nos} (A_e - A_c)(F+1)\, e^{\frac{q V_{be}}{1,6\, kT}} + J_{rss} A_E\, e^{\frac{q V_{be}}{2\, kT}}}$$

$$I_c = J_{nis} A_c\, e^{\frac{q V_{be}}{kT}}$$

$$\therefore V_{be} = \frac{kT}{q} \cdot \ln\left\{\frac{I_c}{J_{nis} A_c}\right\}$$

$$\therefore \beta_u = \frac{I_c}{\{J_{prs} d_p \sqrt{A_E} + J_{nms} A_c + J_{pvs} A_E (F+1) + J_{ss} d_p \sqrt{A_E}\}\, \frac{I_c}{J_{nis} A_c} + J_{nos}(A_E - A_c)(F+1)\left\{\frac{I_c}{J_{nis} A_c}\right\}^{\frac{1}{1,6}} + J_{rss} A_E \left\{\frac{I_c}{J_{nis} A_c}\right\}^{\frac{1}{2}}}$$

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$$\therefore \Sigma I_B = J_{prs} \, d_p \frac{\sqrt{A_E}}{A_c} + J_{nms} + J_{pvs} \frac{A_E}{A_c} (F+1) + J_{ss} \, d_p \frac{\sqrt{A_E}}{A_c} \frac{I_c}{J_{ncs} \, A_c}$$

$$+ J_{nos} \frac{(A_E - A_c)}{A_c^{0,66}} (F+1) \left\{ \frac{I_c}{J_{ncs}} \right\}^{0,66}$$

$$+ J_{rss} \frac{A_E}{\sqrt{A_c}} \left\{ \frac{I_c}{J_{nis}} \right\}^{0,5} \qquad 5.20$$

It is obvious that the large emitter/collector area ratio is one of the major causes of the inhe= rently poor upward gain of I^2L transistors. By making the emitter area as close to the collector area as possible we can minimize all the base current components except I_{nm}, which is independent of emitter area.

Another method which is used to improve the low current performance of devices is proportional scaling, whereby all the dimensions of the device are reduced by a constant factor. All area ratios will then remain the same and so the relationship between β_u and V_{be} is un= changed. We are, however, not interested in the value of V_{be} but in the current and because all currents

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are of the form $I = JA\, e^{\frac{q V_{be}}{nkT}}$, decreasing the area A will decrease the value of current cor= responding to a particular value of V_{be}. For example, let $\beta_u = 1$ at $V_{be} = 400$ mV and $I_c = 1$ nA. If we halve the area of all junctions, β_u will still equal 1 at $V_{be} = 400$ mV, but this point will now correspond to a current of 0,5 nA. Expressed differently, by reducing junction areas we can in= crease the current density in the structure, which improves device performance at a given value of current. Unfortunately, it is not possible to apply proportional scaling effectively when one is limited to a standard process, for two reasons:

1. The layout rules specify certain minimum clearances which make it impossible to minimize the emitter/ collector ratio while simultaneously scaling the device to reasonable dimensions.
2. If the areas of horizontal junctions such as the emitter-base junctions are decreased by a factor k, the areas of vertical junctions such as the pnp col= lector base junction are only decreased by a factor $\sqrt{k}$ as the depth of such junctions is fixed by the process.

To investigate the effect of scaling on per= formance, we assume an emitter area which is as close to the area of the collector as the layout

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rules will allow. The following relationship is obtained (see Appendix A.1):

$$A_E = (\sqrt{A_c} + 8)(\sqrt{A_c} + 12)$$

Substituting this value for A_E into equation 5.20 and varying A_c, we can calculate the correspon= ding variations in all of the base current com= ponents. These are shown in Table III and Fig. 5.7(a) with all currents normalized with respect to their values in the minimum geometry structure (A_c = 256 μm^2). Note that with the exception of I_{rs}, all base current components decrease relative to the collector current when the cell size in= creases. This implies an increase in the current gain at medium and low current levels (I_c > 100 pA) and a decrease at very low current levels. It would therefore appear that there is no optimum device - in fact a trade-off exists between current gain at normal operating levels and packing density. This conclusion has been experimentally verified by measurements on a series of inverted npn transistors in a test circuit (MCL 5, see Appendix A3.2). Nine transistors with varying emitter and collector areas were designed and their current gains at 1 μA were

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A_c	A_E	I_{pv}	I_{rp}, I_s	I_{no}	I_{rs}
256	672	1	1	1	1
400	896	0,853	0,732	0,902	1,067
576	1 152	0,762	0,583	0,834	1,143
784	1 440	0,700	0,477	0,783	1,225
1 024	1 760	0,655	0,404	0,744	1,310

TABLE III

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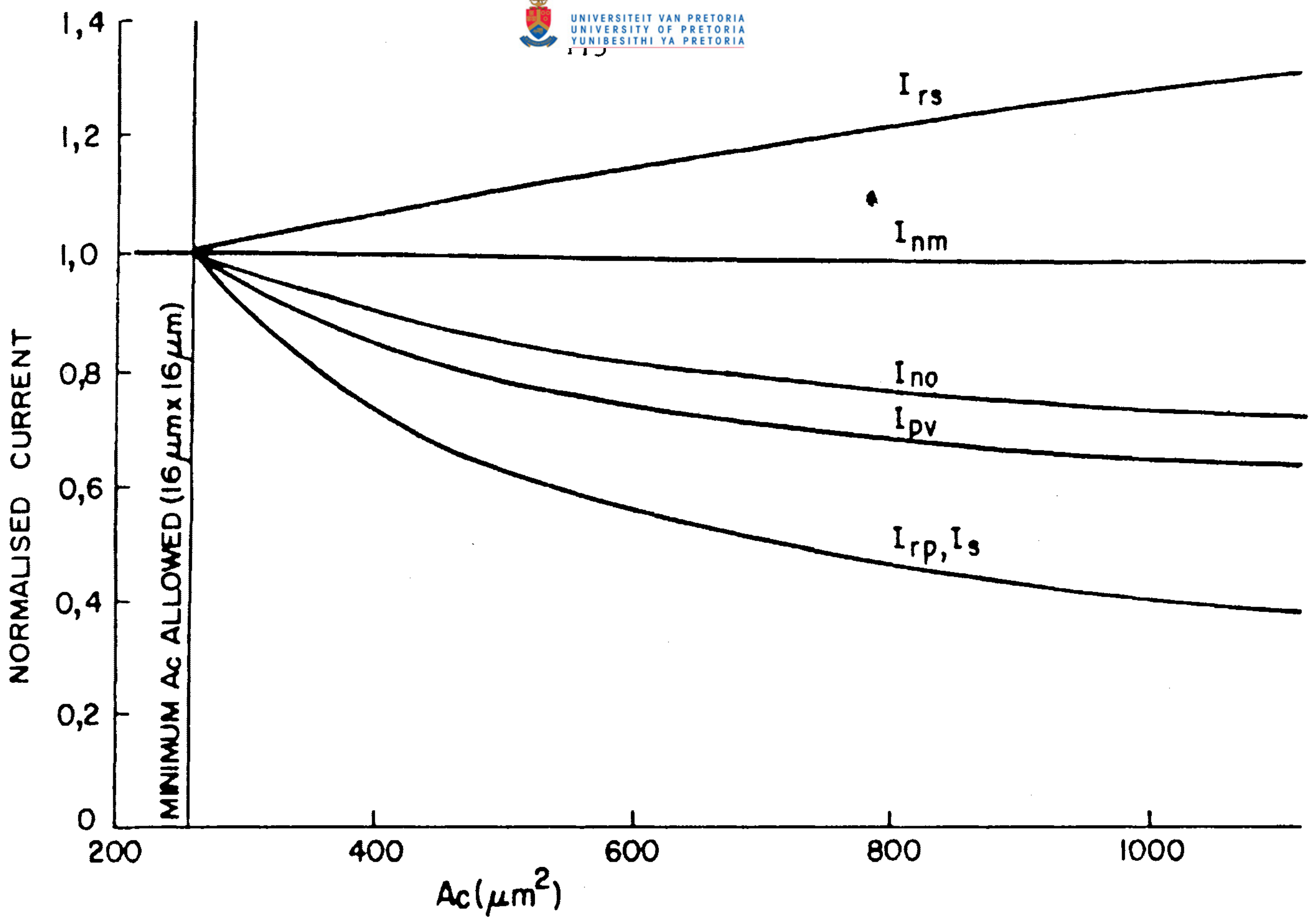

Fig.5.7(a) Normalized base current components as functions of A_c

MINIMUM Ac ALLOWED (16 μm x 16 μm)

MAXIMUM A_c/A_E RATIO ALLOWED

⊙ INDICATES MEASURED POINT

A_E (μm^2): 500, 1000, 1500, 2000, 2500, 3000

A_c (μm^2): 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300

Curves: 6, 8, 10, 12, 14, 16, 18, 20

Fig.5.7(b) A_E vs A_c (β_u as parameter)

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were plotted on a graph of A_E versus A_c (Fig. 5.7(b)). By interpolation and extra= polation a series of curves of constant β_u were plotted. The limitations imposed on di= mensions by the layout rules are also shown. Moving from point A (minimum geometry, A_E = 675 μm^2) to point B (A_E = 1 350 μm^2) along the line of maximum collector/emitter area ratio we find a steady increase in β_u from approximately eight to 20. Because packing density is of ut= most importance it was decided to use the minimum geometry structure, despite its relatively poor performance.

Finally, an analysis of the effect of the isolation between cells on static device perfor= mance must be made. While it was originally stated that I^2L does not require the deep p^+ isolation of a standard bipolar process, it is desirable to pro= vide some form of n^+ isolation in order to minimize the effect of the side-wall current I_s on perfor= mance[28 & 42]. The following possibilities exist (Fig. 5.8):

1. A deep n^+ isolation diffusion extending down to the buried layer(at least 6 μm). There are two disadvantages to this method - firstly, it it is a non-standard process step and secondly, it is space consuming because of the outdif= fusion of about 6 μm to either side.

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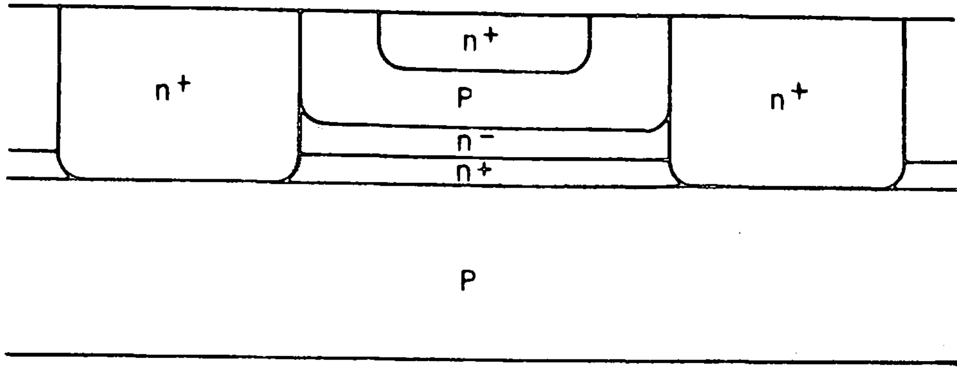

Fig.5.8(a) Deep n^+ isolation

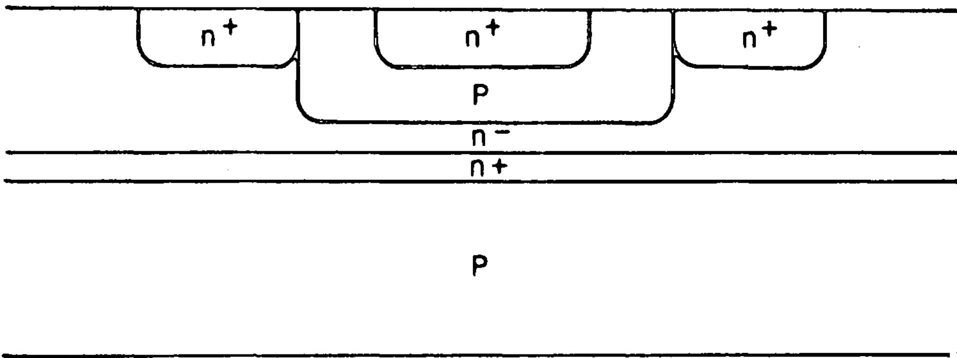

Fig.5.8(b) Shallow n^+ isolation

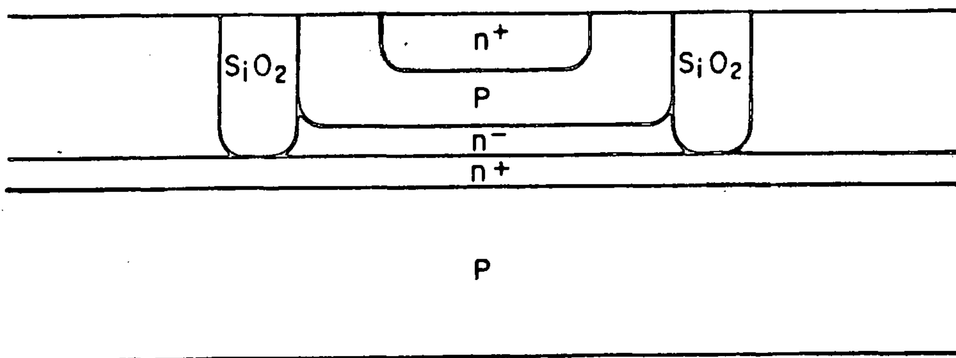

Fig.5.8(c) Isolation by anodic oxidation of silicon

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2. A shallow n^+ isolation diffusion formed during the same process step as the col= lectors (typically 1 → 1,5 μm deep). This method of isolation requires no deviation from the standard process. Furthermore, it requires very little space, as the outdif= fusion to either side is less than 1,5 μm. The edge of the isolation can in fact be made coincident with the edge of the base, so that there is an overlap after outdiffusion. In this case no extra space need be allowed for the isolation compared to a non-isolated device. The isolation is also self-aligning relative to the collectors and the gain will be improved slightly by lateral electron injection from the isolation to the collectors. The reverse hole injection current I_s will not be reduced as much as in the case of a deep n^+ diffusion, as there is still a n^--region below the n^+-collar into which injection may take place. However this fact is somewhat compensated for, firstly by the gettering action of the emitter diffusion step which tends to reduce the number of recom= bination centres in the base, and secondly by the more abrupt n^+ p junction obtained which reduces hole injection more than in the case of the out= diffused deep n^+ diffusion.

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3. A third method which is to be investigated at the National Electrical Engineering Re= search Institute is dielectric isolation by anodization of silicon. This method has im= portant advantages such as high isolation resis= tance, low isolation capacitance and virtually no outdiffusion of the isolation medium. It is however purely in an experimental stage at present.

It was decided to use a shallow n^+ isolation, mainly because of its process simplicity. It remains to determine the width of this isolation necessary for good performance. The effect of I_s on performance will be analyzed in two stages - first the effect of the loss of I_s on cell opera= tion will be modelled and then the effect of the injection of this current into the neighbouring cells will be con= sidered. Equation 5.16 may be written in the following form:

$$\frac{1}{\beta_u} = \frac{I_{no} + I_{nm} + I_{pr} + I_{pv} + I_{rs} + I_s}{I_c}$$

$$= \frac{I_{nos}\, e^{\frac{q V_{be}}{1{,}6kT}} + I_{nms}\, e^{\frac{q V_{be}}{kT}} + I_{prs}\, e^{\frac{q V_{be}}{kT}} + I_{pvr}\, e^{\frac{q V_{be}}{2kT}} + I_{rss}\, e^{\frac{q V_{be}}{2kT}} + I_{ss}\, e^{\frac{q V_{be}}{kT}}}{I_{cs}\, e^{\frac{q V_{be}}{kT}}}$$

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$$= \frac{1}{\beta_I} + \frac{I_{ss}}{I_{cs}}$$

$$\doteq \frac{1}{\beta_I} + \frac{q\, A_s\, D_p\, n_i^2}{I_{cs}\, N_D W_s}$$

$$= \frac{1}{\beta_I} + k_s(W_s) \qquad 5.21$$

β_I is the upward current gain of the intrinsic cell without side-wall currents, and k_s is a factor which describes the effectiveness of the isolation medium and which will be evaluated later. The effective current gain is thus

$$\beta_u = \frac{1}{\frac{1}{\beta_I} + k_s(W_s)} \qquad 5.22$$

Unfortunately the intrinsic current gain is not directly measurable. What is measurable is the current gain of a single cell far removed from any neighbouring cells. This is typical of the situation in a test circuit where each experimental device is separated from its neighbours by a generous margin. What is required is an equation relating the performance of such a test device to the performance of an identical structure in an LSI environment. The current gain of the single device is

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$$\beta_{us} = \frac{1}{\frac{1}{\beta_I} + k_s(\infty)}$$

$$\therefore \frac{1}{\beta_I} + k_s(\infty) = \frac{1}{\beta_{us}}$$

$$\therefore \beta_I = \frac{1}{\frac{1}{\beta_{us}} - k_s(\infty)} \qquad 5.23$$

Substituting 5.23 in 5.22 we obtain

$$\beta_u = \frac{\beta_{us}}{1 + \beta_{us}\,(k_s(W_s) - k_s(\infty))} \qquad 5.24$$

Note that the effect of the lateral injection is to place an upper limit on β_u - if $\beta_{us} \to \infty$, $\beta_u \to \dfrac{1}{k_s(W_s) - k_s(\infty)}$.

The value of $k_s(W_s)$ will be largest when all the adja= cent cells are in a logical '0' state (Fig. 5.9(a)). The pa= rasitic lateral pnp transistor between cells may then be modelled as having a grounded collector. The effect of this hole in= jection on the cell which is ON is to tend to turn it OFF by reducing the base current. As this current is injected into adjacent cells which are OFF, it tends to turn these cells ON by increasing the base current. The worst-case condition here

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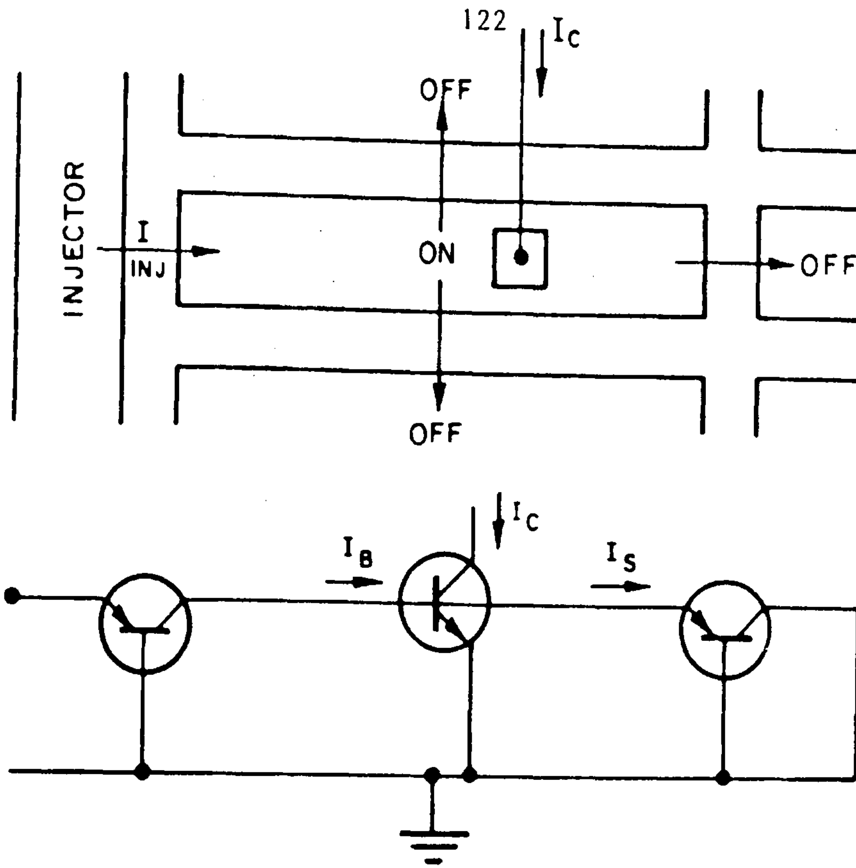

Fig.5.9(a) 'ON' cell surrounded by 'OFF' cells

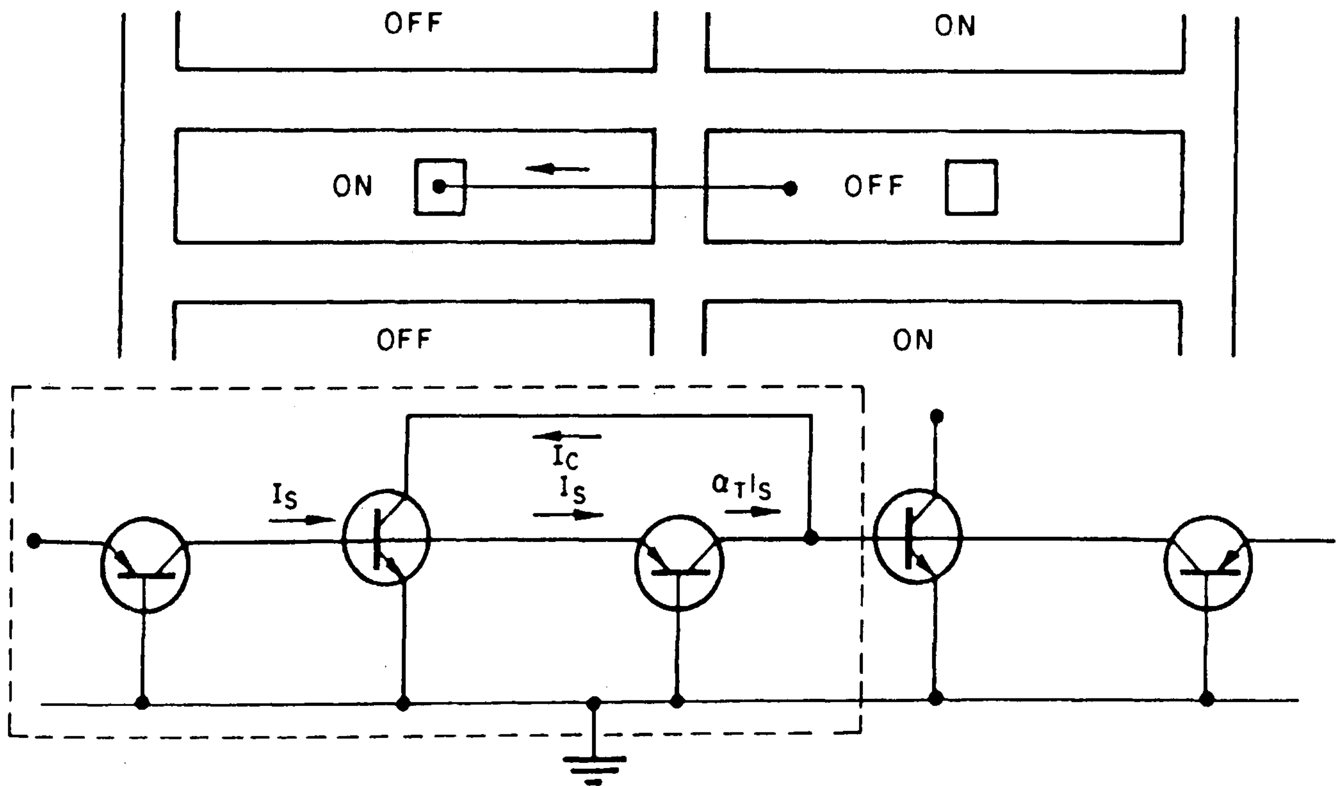

Fig.5.9(b) 'OFF' cells surrounded by 'ON' cells

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is one where a single cell in the OFF state is surrounded by cells which are all ON. The total current injected into this cell is then equal to $\alpha_T I_s$ where α_T is the base transport factor of the parasitic lateral pnp transistor (see Fig. 5.9(b)). Because I^2L cells are inverting an ON cell is always connected to an OFF cell. The devices enclosed by dotted lines in Fig. 5.9(b) may be considered as a single 2-port network with a worst-case current gain of

$$\beta_w = \frac{I_c - \alpha_T(W_s).I_s}{I_B}$$

$$= \frac{I_c}{I_B} - \frac{\alpha_T(W_s)\ I_s}{I_B}$$

$$= \frac{I_c}{I_B} - \frac{\alpha_T(W_s).k_s(W_s)I_c}{I_B}$$

$$= \beta_u\ (1 - \alpha_T(W_s)\ k_s(W_s))$$

$$= \frac{\beta_{us}(1 - \alpha_T(W_s)\ k_s(W_s))}{1 + \beta_{us}\ (k_s(W_s) - k_s(\infty))} \qquad 5.25$$

The maximum possible value of β_u has now been reduced to

$$\frac{1 - \alpha_T(W_s)\ k_s(W_s)}{k_s(W_s) - k_s(\infty)}$$

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when $\beta_{us} \to \infty$. The requirement that $\beta_w \geq 2$ is a far more stringent one than the original requirement that $\beta_u \geq 2$. In order to evaluate the relationship between β_w and β_u we must calculate $k_s(W_s)$ and $\alpha_T(W_s)$.

$$k_s(W_s) = \frac{I_{ss}}{I_{cs}}$$

$$= \frac{q\, A_s\, D_p\, n_i^2}{I_{cs}\, N_D\, L_p\, \tanh\left(\frac{W_s}{L_p}\right)}$$

$$\doteqdot \frac{q\, D_p\, n_i^2}{I_{cs}\, N_D} \cdot \frac{A_s}{W_s} \qquad 5.26$$

In order to determine the constant with accuracy a parabolic approximation of the junction involved may be made. In practice the curvature of the junction is approximately elliptic, but the parabolic assumption greatly simplifies the calculation while introducing little error. $k_s(W_s)$ will be analysed for two different cases:

1. No isolation diffusion (see Fig. 5.10(a)).

$$\Delta A_s = \ell\, \Delta x$$

$$W_s(x) = W_m - 2y$$

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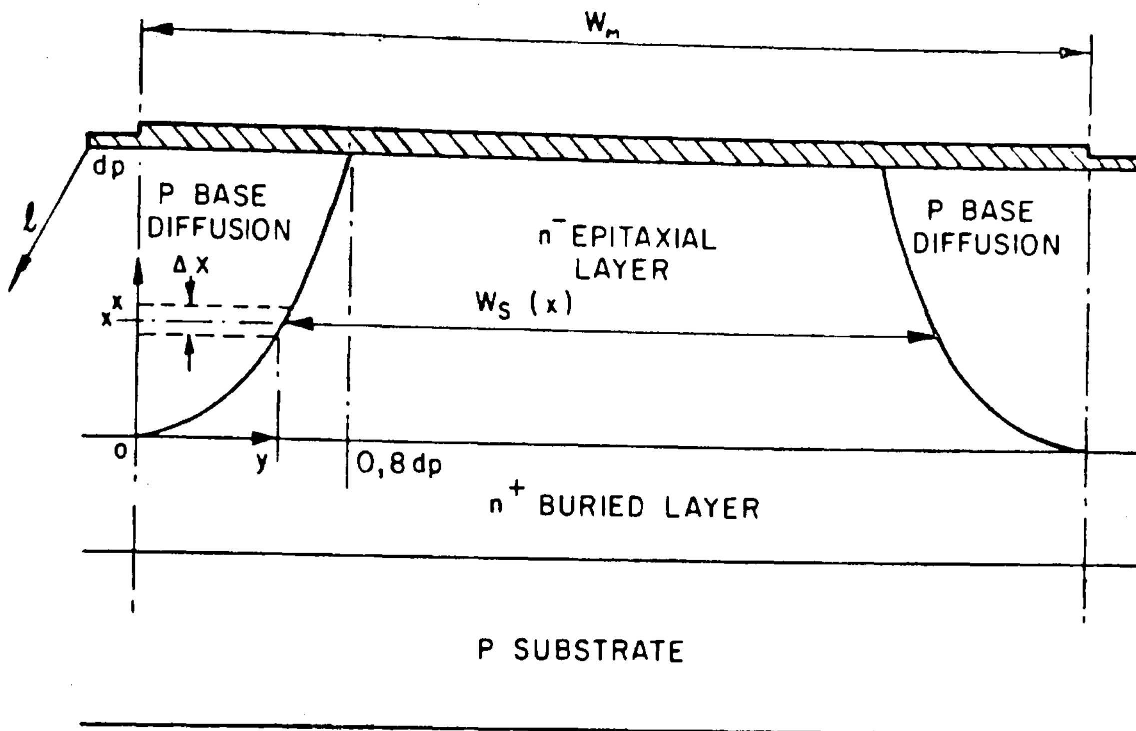

Fig. 5.10(a): Model of out-diffused base regions (no n^+ isolation)

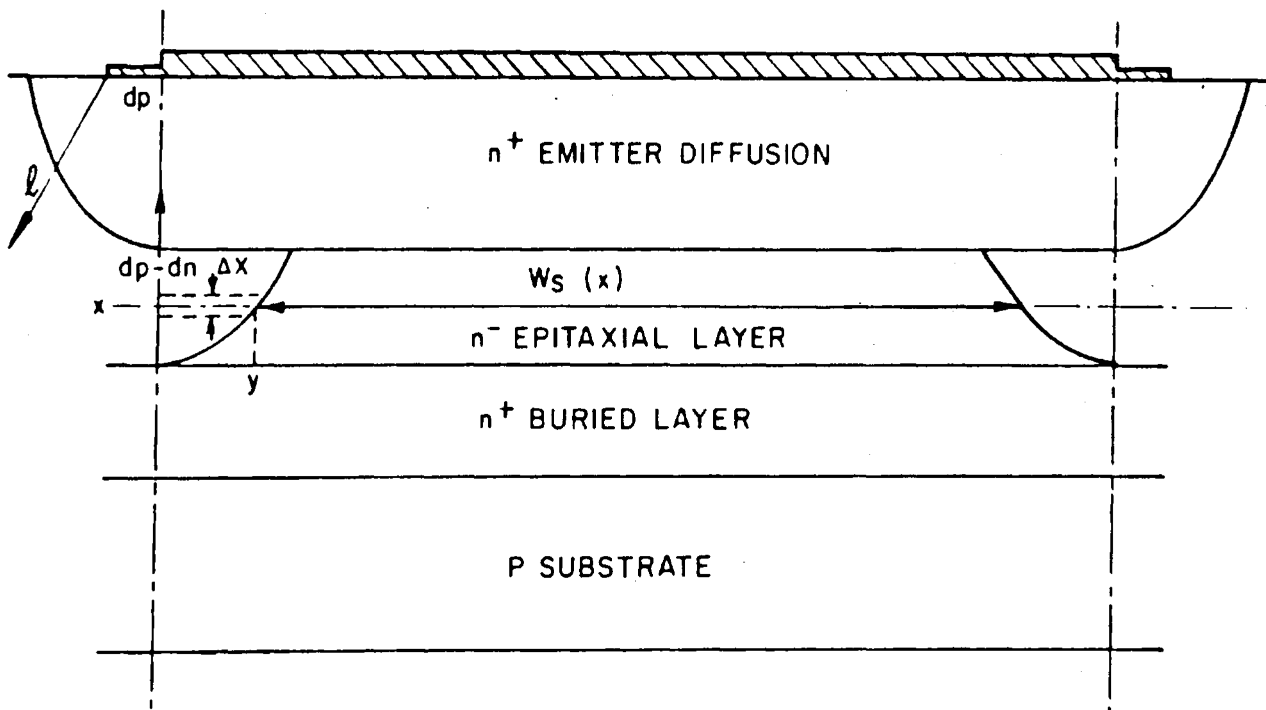

Fig. 5.10(b): Model of out-diffused base regions with n^+ isolation

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We assume a parabolic junction with a lateral diffusion at the surface equal to 80% of the in-diffusion.

$$x = ky^2$$

$$\therefore d_p = k\,(0{,}8\,d_p)^2$$

$$\therefore k = 1/0{,}64\,d_p$$

$$\therefore W_s(x) = W_m - 1{,}6\,\sqrt{d_p}\,.\,\sqrt{x}$$

$$\therefore k_s(W_s) = \frac{q\,D_p\,n_i^2\,\ell}{I_{cs}\,N_D}\int_o^{dp}\frac{dx}{W_m - 1{,}6\,\sqrt{d_p}\,.\,\sqrt{x}}$$

Let $u = w - kx^{\frac{1}{2}}$

$$\therefore x = \frac{(w-u)^2}{k}$$

$$\therefore \frac{du}{dx} = \frac{-k}{2\,x^{\frac{1}{2}}}$$

$$\therefore \frac{dx}{du} = \frac{-2\,x^{\frac{1}{2}}}{k}$$

$$= \frac{-2}{k}\,\frac{(w-u)}{k}$$

$$\frac{dx}{u} = \frac{1}{u}\,.\,\frac{dx}{du}\,.\,du$$

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$$= \frac{-2}{k^2} \frac{(w - u)}{u} du$$

$$\therefore \int_0^{d_p} \frac{dx}{u} = \frac{-2}{k^2} (- u + w \ln u)$$

$$= \frac{-2}{k^2} \left[k x^2 - w + w \ln (w - kx^2) \right]_o^{d_p} \qquad 5.27$$

Assuming that d_p = 1,8 µm, $k_s(W_s)$ may be calculated as

$$k_s(W_s) = \frac{q D_p n_i^2 \ell}{I_{cs} N_D} \cdot (0{,}434 W_m \ln (\frac{W_m}{W_m - 2{,}88}) - 1{,}25) \qquad 5.28$$

and

$$k_s(\infty) = \frac{q D_p n_i^2 \ell}{I_{cs} N_D} \cdot \frac{d_p}{L_p} \qquad 5.29$$

The validity of the model has been tested by means of single-collector gates in MCL 5. The length of the periphery in this case is 124 µm. Using the values of the various con= stants listed, and a measured value for I_{cs}, families of curves, firstly of β_u vs β_{us} and also of β_w vs β_{us} were plotted for dif= ferent values of W_s (see Fig. 5.11). By means of measurements on structures IS08, IS012 and IS016 in MCL 5 it was possible to verify the accuracy of the former to within 15%. The latter set of curves is not directly measurable but gives a useful worst-case value for design purposes.

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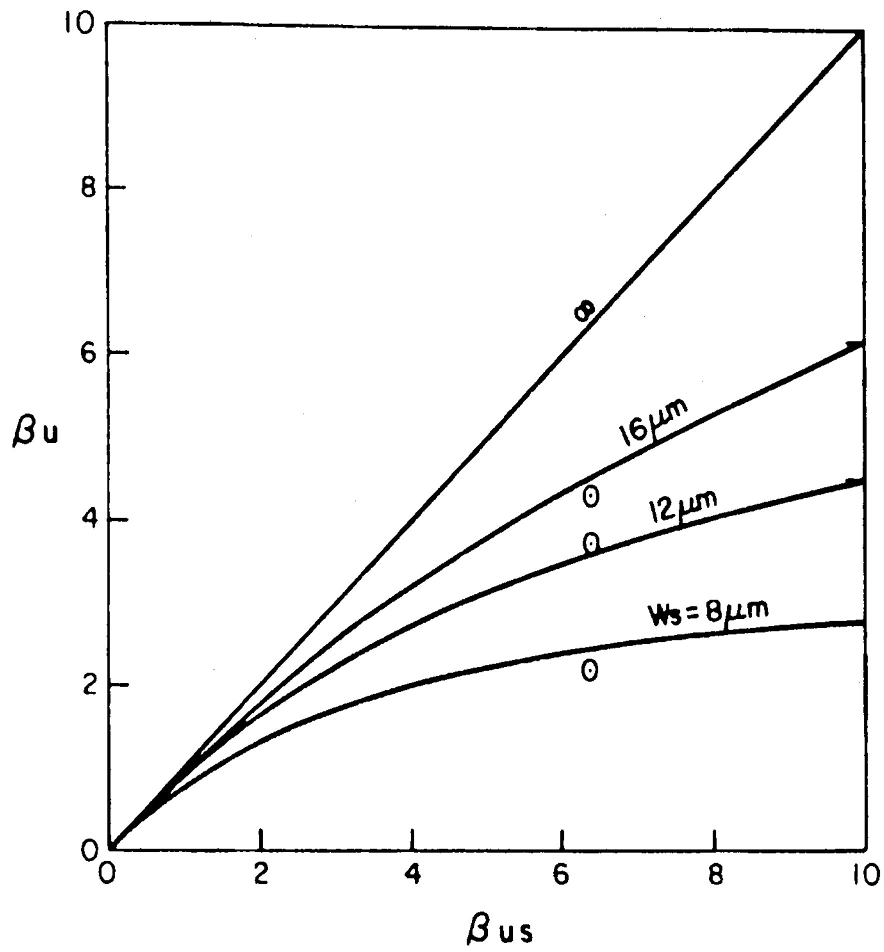

Fig.5.11(a) β_u vs β_{us} (no isolation)

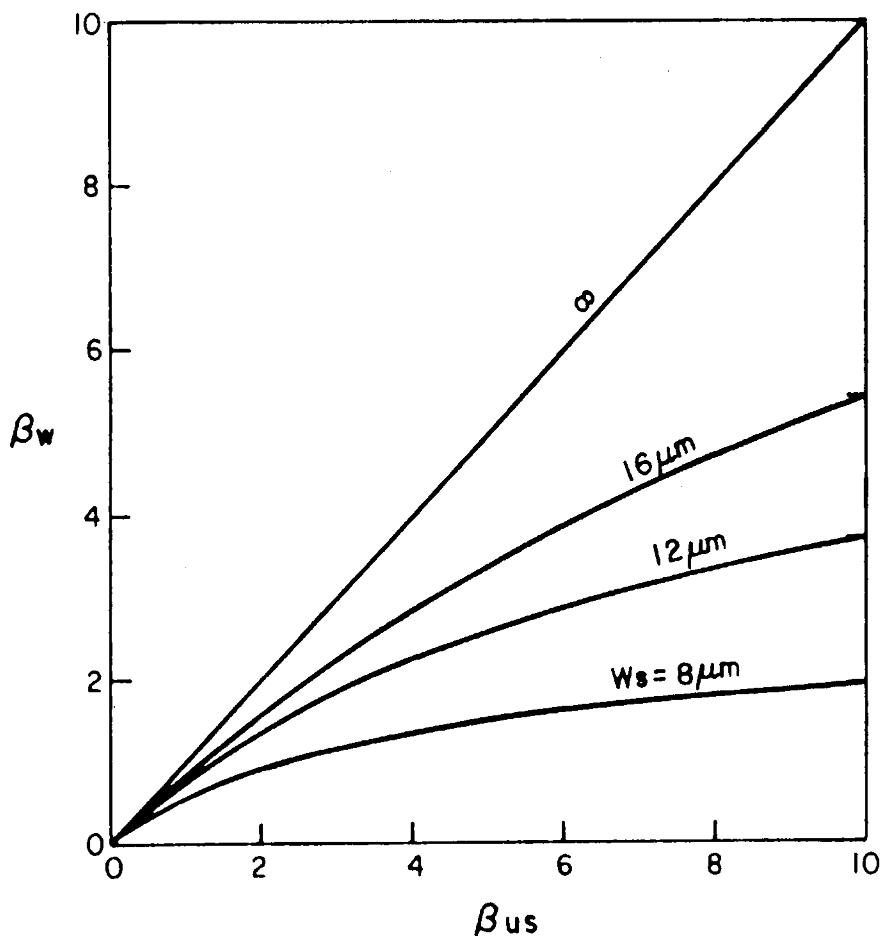

Fig.5.11(b) β_w vs β_{us} (no isolation)

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2. Shallow n^+ isolation (see Fig. 5.12).

The calculations were repeated for the case of a shallow n^+ isolation. It was assumed that lateral injection would only take place in the n^- region below the isolation which ex= tends to a depth d_n. $k_s(w_s)$ may be calculated simply by al= tering the upper limit of integration in 5.27 to $(d_p - d_n)$. With d_n = 1 μm this yields the following results:

$$k_s(W_s) = \frac{q\, D_p\, n_i^2\, 1}{I_{cs}\, N_D} \left(0{,}434\, W_m \ln\left(\frac{W_m}{W_m - 1{,}92}\right) - 0{,}8333\right) \qquad 5.30$$

$$k_s(\infty) = \frac{q\, D_p\, n_i^2\, 1}{I_{cs}\, N_D} \; \frac{(d_p - d_n)}{L_p} \qquad 5.31$$

The results are shown in Fig. 5.12. A considerable reduction in the effect of lateral injection on performance is noticed. This is due to a number of causes. The model describes the effect of a reduction in area and a slight in= crease in spacing after outdiffusion. It was also found that I_{cs} was approximately 45% larger in the case of the isolated devices, and β_{us} increased by a factor of approximately three. The latter two effects result from the gettering action of the n^+ collar described earlier.

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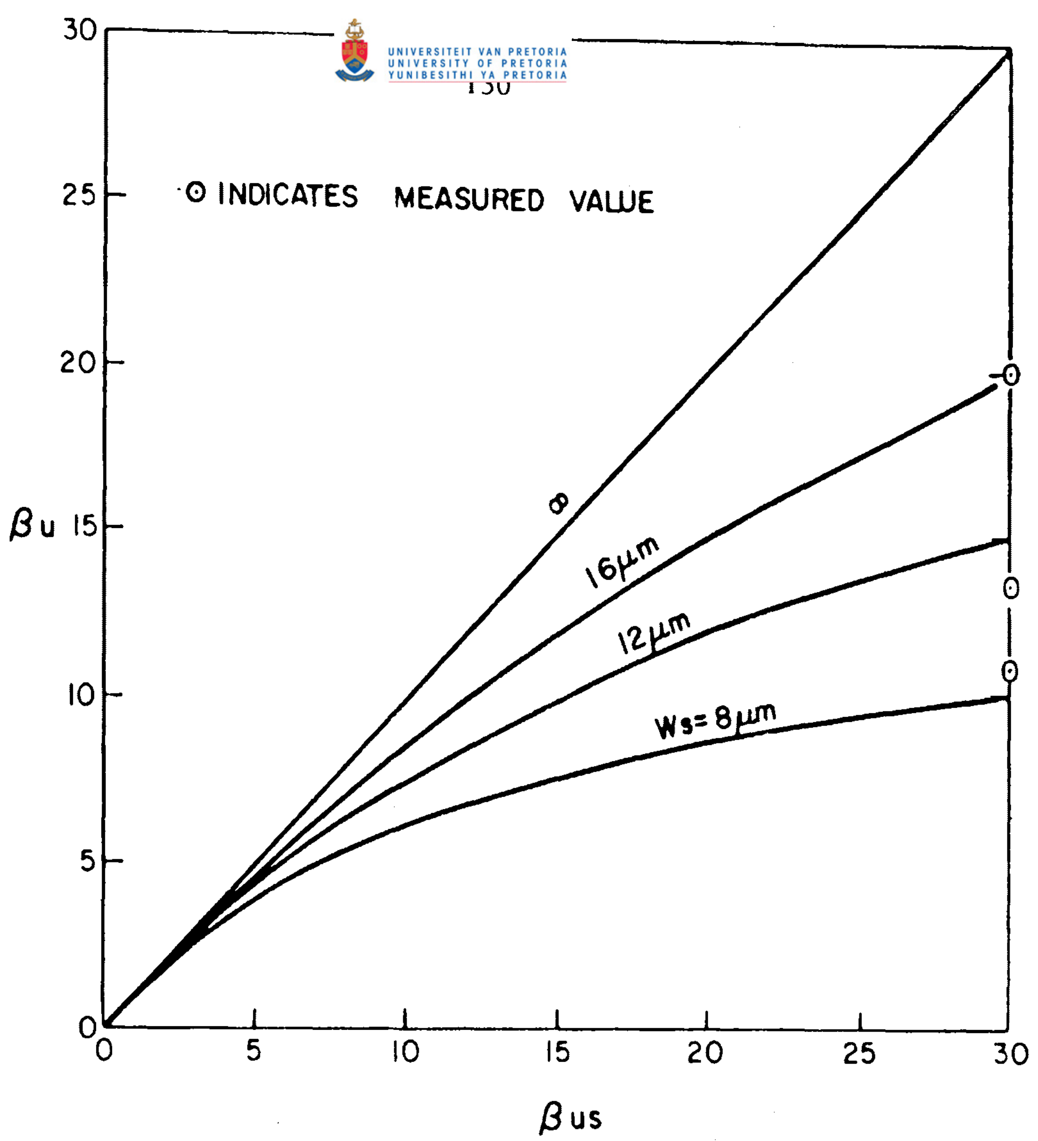

Fig.5.12(a) β_u vs β_{us} (n^+ isolation)

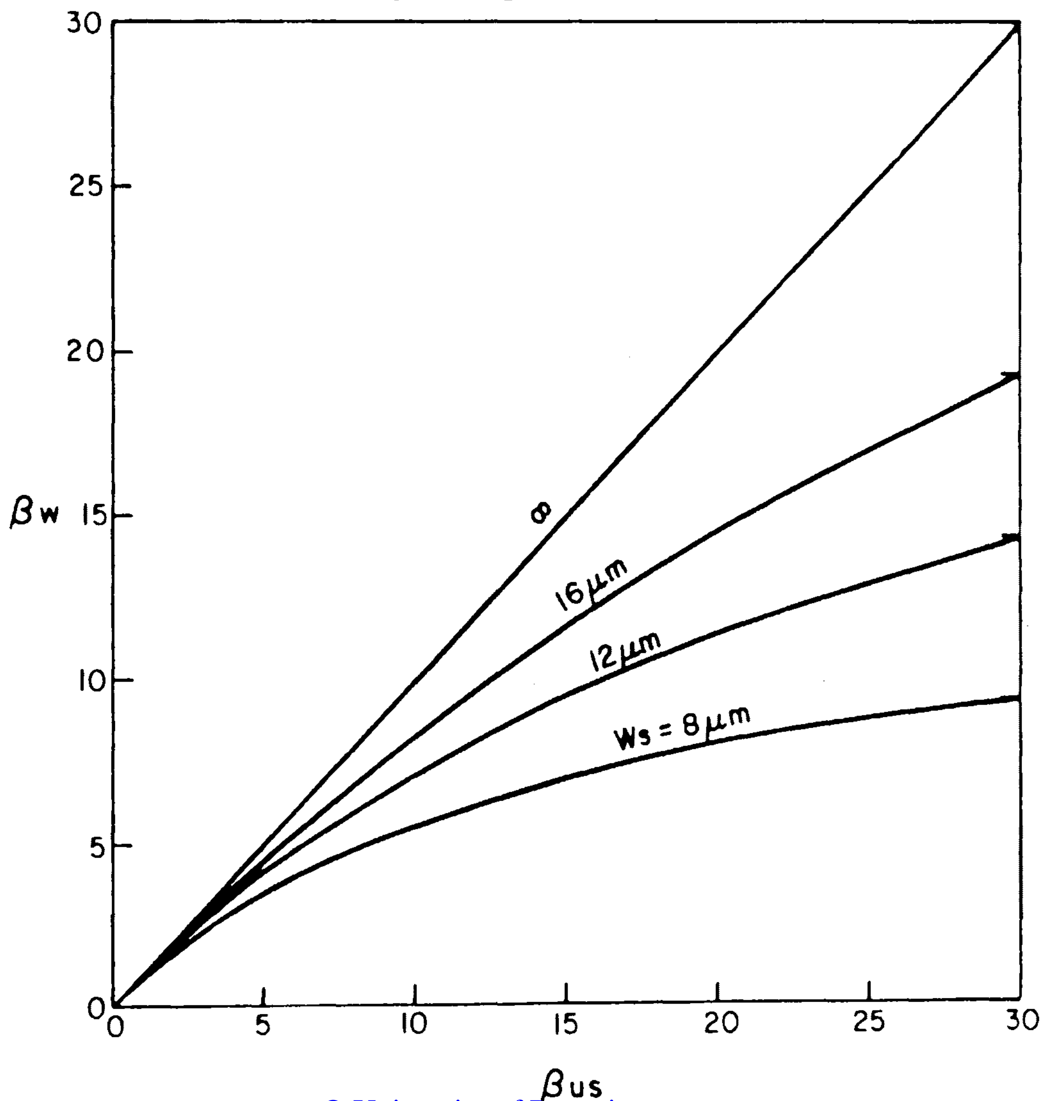

Fig.5.12(b) β_w vs β_{us} (n^+ isolation)

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Before moving on to the question of dynamic perfor= mance, we may briefly recap on the foregoing analysis of static performance. The analysis has shown the following:

(i) There can be no question of an optimum gate size. Decreasing gate size worsens the col= lector/emitter area ratio causing a decrease in βu.

(ii) The use of an n^+ collar improves βu by reducing lateral injection and gettering impurities in the base. Cells may be spaced 8 μm apart if an n^+ collar is used.

(iii) The optimum pnp base width is 12 μm.

(iv) Wet sintering greatly improves the low-current gain by improving the surface condition of the base.

(v) The minimum geometry structure is a usable compo= nent offering a packing density of 180 gates/mm^2 and a βu well in excess of unity (Fig. 5.13). How= ever a large variation in βu is possible because of production tolerances.

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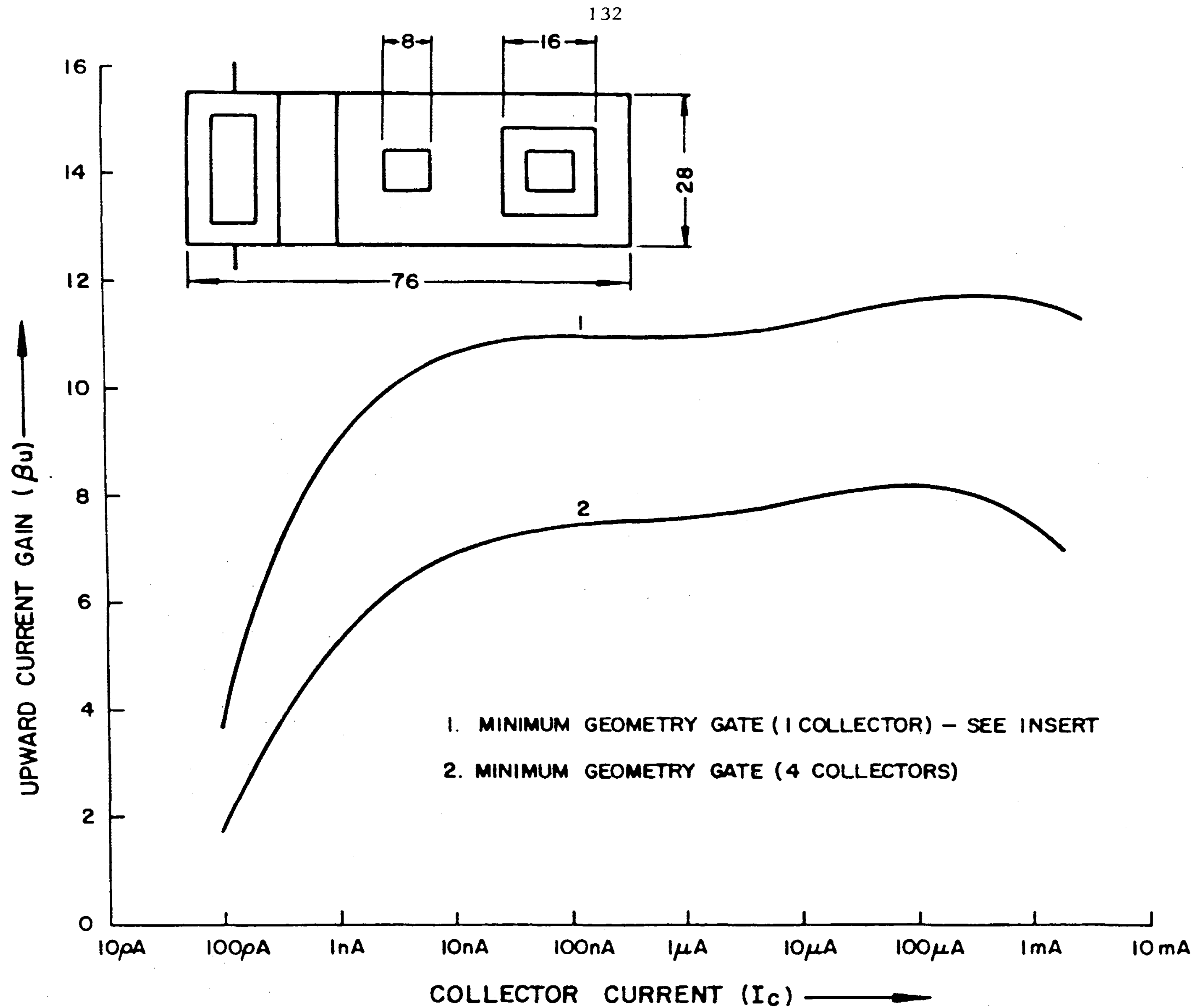

Fig. 5.13: βu vs I_c for 1-collector and 4-collector gates (minimum geometry)

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5.3 Dynamic operation[10 & 35]

Two physical effects normally determine the switching speed of a bipolar device:

1. Active stored charge in the base (and emitter in the case of I^2L).
2. Junction capacitances.

Other high-current effects as a result of internal resis= tances will be ignored. Fig. 5.14 shows the delay vs power curves measured on a series of ring oscillators with different geometries in MCL 5. Two regions of each curve may be distinguished. In the first ($P_g < 10$ µW), delay is inversely proportional to power, i.e. the power-delay product is constant. In this region, delay is determined solely by junction (and stray) capacitances. In the second region ($P_g > 10$ µW) the delay tends towards a con= stant value as a result of the increasing amount of stored charge present. We will consider only the former region in our calculations.

The propagation delay of a gate is defined as the average of the turn-on and turn-off delays:

$$t_d = \frac{t_1 + t_2}{2}$$

Crooke[10] has analyzed the turn-on and turn-off delays in terms of the base-emitter and base-collector junction capacitan= ces. His results will be briefly summarized here. Fig. 5. 15

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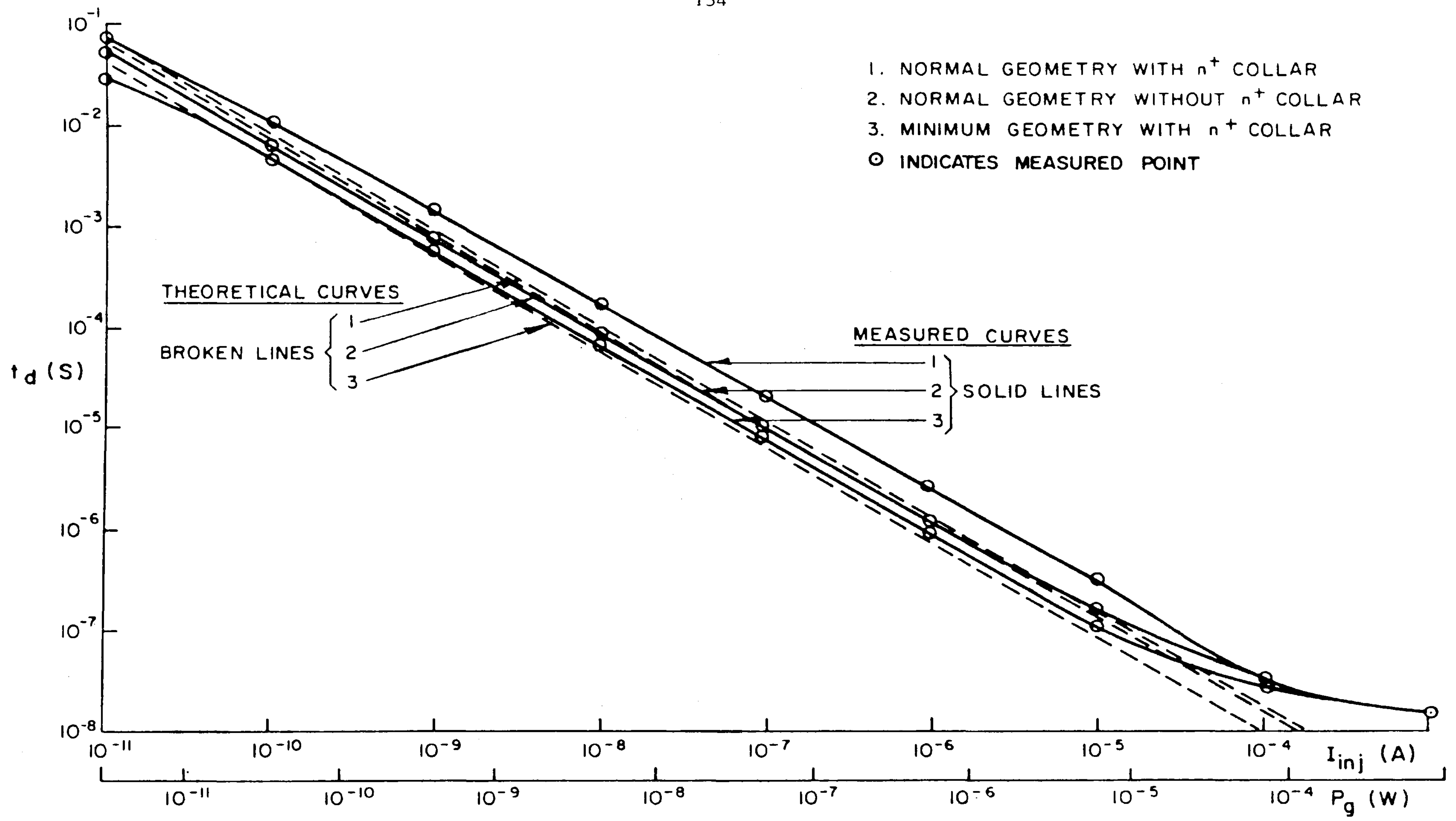

Fig. 5.14: td vs Pg and td vs I_{inj} for various gate geometries

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shows a model of two I^2L cells with junction capacitances included. The input of T1 goes low at t = 0. T2 will only be able to switch on when the voltage V_{be} has risen to a logical '1' value. The current I_{inj} has to charge all the indicated capacitances until this voltage is reached.

$$Q = \int C dV$$

$$\therefore I_{inj} t_1 = \int_{V_{beo}}^{V_{be1}} C_{be} \, d V_{be} + (F + 1) \int_{V_{cb1}}^{V_{cbo}} C_{bc} \, d V_{cb}$$

Let $\Delta V = (V_{be1} - V_{beo}) = (V_{cbo} - V_{cb1})$, the logic voltage swing and assuming that the junction capacitances are constant (they are in fact functions of V_{be} and V_{cb}) the turn-on delay is

$$t_1 = \frac{\Delta V}{I_{inj}} (C_{be} + (F + 1) C_{bc}) \qquad 5.32$$

Similarly the turn-off delay of T3 is determined by the time required to discharge the various capacitances at its base. There is a maximum current of I_{inj} available at the base of T2. to discharge this transistor's base-collector capacitance. At the collector of T2 there is a current $(\beta - 1) I_{inj}$ available to discharge capacitances C_{be} and $F.C_{bc}$ of T3.

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$$\therefore\; t_2 = \Delta V \left(\frac{C_{bc}}{I_{inj}} + \frac{C_{be} + F\, C_{bc}}{(\beta - 1)\, I_{inj}} \right)$$

$$\doteqdot \Delta V \frac{(\beta\, C_{bc} + C_{be} + F\, C_{be})}{\beta\, I_{inj}}$$

$$= \frac{\Delta V}{I_{inj}} \frac{(C_{bc}\,(F + \beta) + C_{be})}{\beta} \qquad 5.33$$

The gate delay is thus

$$t_d = \frac{t_1 + t_2}{2}$$

$$= \frac{\Delta V}{2 I_{inj}} \left(C_{be} + (F+1)\, C_{bc} + \frac{C_{be} + (F + \beta)\, C_{bc}}{\beta} \right)$$

$$= \frac{\Delta V}{2 I_{inj}} \left(C_{be} \left(1 + \frac{1}{\beta}\right) + C_{bc} \left(F + 1 + \frac{F}{\beta} + 1\right) \right)$$

$$\doteqdot \frac{\Delta V}{2 I_{inj}} (C_{be} + (F + 2)\, C_{bc}) \qquad 5.34$$

Predictably the delay is proportional to the logic voltage swing and inversely proportional to the injection current. The logic swing ΔV is equal to the $V_{be} - V_{ce(sat)} \doteqdot V_{be}$, and the

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injector voltage is also $\doteqdot V_{be}$. Therefore the power dissipation is $P_g = V_{inj}\ I_{inj}$

$$\doteqdot V_{be}\ I_{inj}$$

$$\doteqdot \Delta V\ I_{inj}.$$

The power-delay product is

$$PDP = P_g . t_d$$

$$= \Delta V . I_{inj} . \frac{\Delta V}{2 I_{inj}} (C_{be} + (F + 2)\ C_{bc})$$

$$= \frac{\Delta V^2}{2} (C_{be} + (F + 2)\ C_{bc}) \qquad 5.35$$

The logic voltage swing increases slowly with increasing current, and so the power-delay is lowest at low current levels (see Table IV).

It is obviously desirable to minimize C_{bc} and C_{be}. The base-emitter junction is a fairly gradual one and can be approximated as having a linear concentration gradient. The junction capacitance is

$$C_{be} = A_E \left(\frac{q\ (\varepsilon\ \varepsilon_o)^2\ \frac{dN}{dx}}{12\ V_{be}} \right)^{\frac{1}{3}} \qquad 5.36$$

The base-collector junction is closer to an abrupt jnction and its capacitance is therefore approximately

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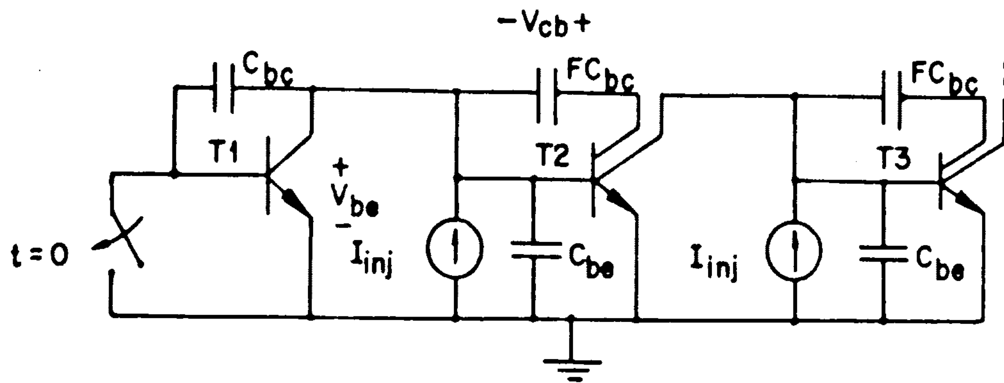

Fig. 5.15: Dynamic model of an I^2L gate

I_{inj} (A)	PDP (pJ) (measured)	PDP (pJ) (calculated)	Error (%)	PDP (pJ) (4 collectors)
10^{-4}	1,8	0,64	-64	1,31
10^{-5}	0,67	0,54	-19	1,1
10^{-6}	0,51	0,45	-12	0,91
10^{-7}	0,38	0,36	-5	0,74
10^{-8}	0,32	0,29	-9	0,59
10^{-9}	0,24	0,22	-8	0,45
10^{-10}	0,17	0,16	-6	0,33
10^{-11}	0,08	0,12	+50	0,23

TABLE IV

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$$C_{bc} = A_c \{\frac{q\ \varepsilon\ \varepsilon_o\ N_D}{2\ V_{bc}}\}^{\frac{1}{2}} \qquad 5.37$$

Values for these capacitances may be obtained from the Plessey technical data file[26], which specifies the following capacitances per unit area and perimeter:

(i) Collector-base junction: 0,17 fF/μm^2 area + 0,94 fF/μm perimeter.

(ii) Base-emitter junction: 1,2 fF/μm^2 area + 3,76 fF/μm perimeter.

Capacitance values were calculated for each of three different structures and the theoretical power-delay curves were compared with measured results (Fig. 5.14). Good agree= ment was obtained at current levels below 100 μA, where stored charges are negligible. Comparing devices with normal geo= metry (cell area = 2 592 μm^2) and minimum geometry (cell area = 1 456 μm^2) both having n^+ collars, the former has a 173% greater delay at the same current, because of greater junction area. Again, comparing normal devices with and without an n^+ collar we find that the latter is typically 107% slower because of the high-capacitance n^+p junction between base and emitter. It is unfortunately not possible to operate the minimum geo= metry device without the n^+ collar, as its current gain is then less than unity. Interestingly, the gate without n^+ collar is the slower of the two at currents above 100 μA, as a result of

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extra stored charge in the n epitaxial region between cells. This indicates a trade-off between low-current and high-current performance. In table IV, measured and calculated values of power-delay product are compared for single-collector minimum geometry devices. Agreement within 20% was obtained from 100 pA to 10 μA (5 decades). Below 100 pA, leakage currents or light give an optimistic result. A theoretical projection was made for a 4-collector structure, which shows a PDP of roughly 1 pJ in the region of interest for the design (10 μA/gate).

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5.4 Voltage-drop problems

A multi-collector I^2L cell is a suitable array element, having several decoupled outputs and an input which also forms a diffused underpass. However, some serious problems arise when one attempts to form a large array in this fashion. In the case of the conventional short-side-injection structure described, the maximum number of collectors is limited by the resistance of the base material (R_s = 100 Ω/□). When the cell is ON a voltage drop exists along the length of the cell which results in the furthest collectors being somewhat starved of base current. Kirschner has analyzed the effect of base re= sistance in the I^2L cell[44]. The various regions of the base are modelled as distributed diode-resistor networks and a 2nd order differential equation is solved to yield the voltage (or current) at any point in the base. In the case of a 4-collector struc= ture with A_E = 40 x 48 μm^2 and A_c = 24 x 24 μm^2 it was found that the current gain of the furthest collector does not deviate from its low-current value by more than 10% for collector cur= rents below 90 μA. Although this result was not obtained in the minimal geometry structures it may be used as a guide, as the structure used had a similar aspect ratio. The result in= dicates that no problem is likely to be experienced with voltage drops in a 4-collector structure at the maximum current level of

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1 → 10 μA per collector necessary for 1 MHz operation (see Fig. 5.13(a)). However, if an injector is required to supply every four collectors, extra metallization or diffused regions are required to connect them all together externally. Similarly all the base regions would need to be connected together.

The need for these extra connections makes the layout com= plex and the attainment of high packing densities problematical. Both connections must have a low resistance, but particularly that to the injectors, where a 18 mV voltage difference can cause a 2:1 current ratio between cells. The base connection serves only to turn the cells OFF and a voltage drop of not greater than $V_{be(on)} - V_{ce(sat)}$, roughly 0,4 V, is permissible. The diffused region with the lowest sheet resistance is the n^+ emitter diffu= sion (used to form the I^2L collectors) which has a sheet resistance of 3,7 Ω/□. Some ways of forming an I^2L array using this diffusion will be considered. Fig. 5.16(a) shows a 96-collector cell in which the injectors and bases are both connected via n^+ underpasses. Each injector supplies current to four collectors on either side - thus there is an injector for every eight collectors. Assuming a strip width equal to the minimum of 16 μm for high packing den= sity and a current of 8 x 10 = 80 μA into the last injector (10 μA/gate), the currents into the other injectors may be cal= culated (see Table V).

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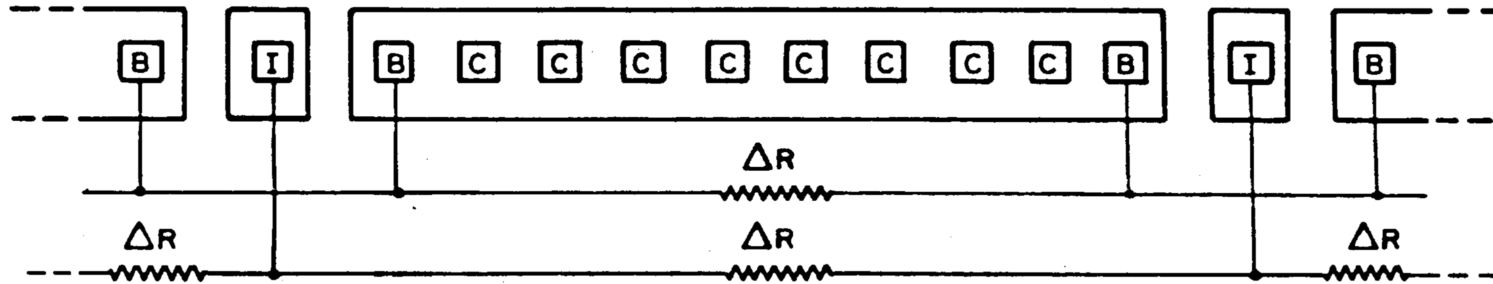

Fig. 5.16(a): Array cell with injector connection via underpass

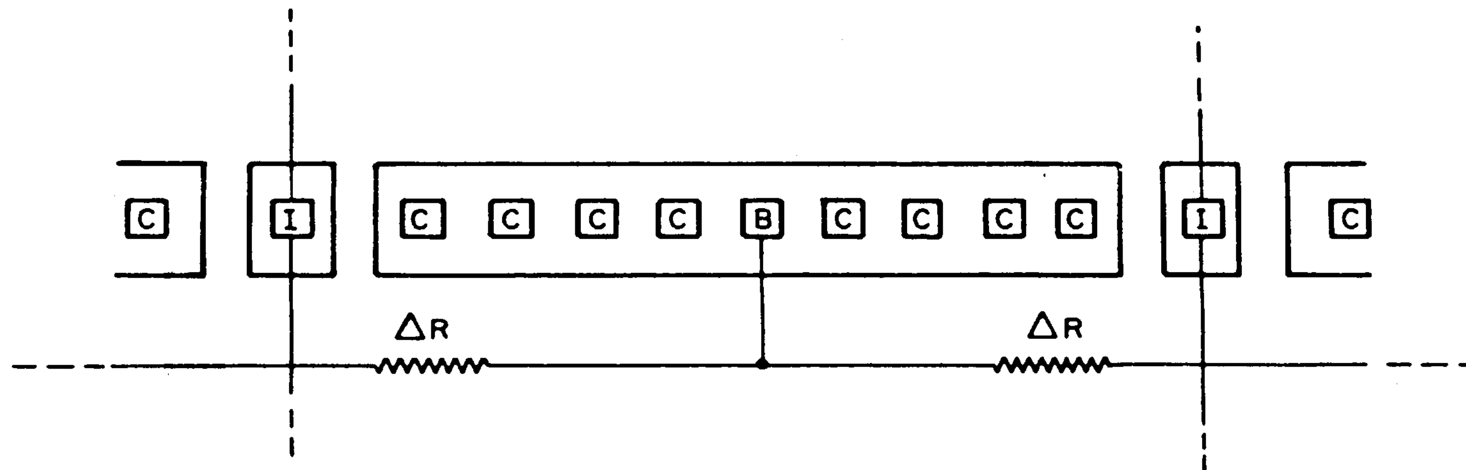

Fig. 5.16(b): Array cell with injector connection via metallization

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Injector Number	Injector Current
12	80 μA
11	83,1 μA
10	89,9 μA
9	101,5 μA
8	120,3 μA
7	151,1 μA
6	204,1 μA
5	304,3 μA
4	524,1 μA
3	1,16 mA
2	4,49 mA
1	150,55 mA

TABLE V

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$$I_n = I_{n+1} \cdot e^{\frac{q}{kT}(V_n - V_{n+1})}$$

$$= I_{n+1} \cdot e^{\frac{q}{kT} \sum_{i=n+1}^{96} I \cdot \Delta R}$$

This is obviously an impractical solution - a current of 80 μA into the last injector requires a current of 150 mA into the first! Fig. 5.16(b) shows an alternative where the connections to the injectors are made via metallization which is interspersed between the collector metallization. This method poses some additional problems at the interface between the AND and the OR arrays but is still feasible. There is now no voltage drop problem when the cell is ON, while the problem of turning the device OFF is now the dominant one. The criterion for correct operation is that when the input terminal at the end of the n^+ underpass is at $V_{ce(sat)}$, the collector which is furthest removed from the input must remain OFF, i.e. it must be incapable of sinking an injector current.

$$\therefore I_{c(off)} << I_{inj}$$

Assuming $I_{inj} = 100\ I_{c(off)}$ gives a safe margin. Thus

$$V_{be} = V_{be(on)} - \frac{kT}{q} \ln (100)$$

$$= V_{be(on)} - 120 \text{ mV}.$$

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The total voltage drop permissible along the n^+ strip is $V_{be(on)} - 120$ mV $- V_{ce(sat)}$. At 10 μA/collector this amounts to about 340 mV.

$$V_R = I_n \Delta R + (I_n + I_{n-1}) \Delta R + (I_n + I_{n-1} + I_{n-2}) \Delta R + \ldots\ldots + \sum_{i=1}^{n} I_i \Delta R.$$

$$= \Delta R \ (I + 2I + 3I + \ldots + nI)$$

(all currents are equal).

$$\therefore V_R = \Delta R \cdot \frac{n}{2} (2 + n - 1) I$$

$$= \frac{I\Delta R.n(n + 1)}{2} \qquad 5.38$$

$$= 78 I\Delta R \text{ (when } n = 12)$$

$$= 78 \times 80 \times 10^{-6} \times 12$$

$$= 74{,}88 \text{ mV.}$$

This allows a safety factor of 4,5 at the maximum current necessary to satisfy the speed requirements.

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This structure is satisfactory except for the fact that the injectors and associated conductors lower the packing den= sity of the AND array by 25%, and also consume space at the edges of the array owing to the large number of underpasses now necessary there. An alternative is to remove the injector transistors from the array entirely, leaving only the inverted npn transistors. The base current then flows into the array via the n^+ underpasses. This is impractical however, for the same reason as is the case for the first structure considered. The problem is a fundamental one stemming from the fact that an I^2L gate requires three connections - input, output and injector, while the traditional diode matrices require only an input and an output. The addition of the injector connection will always cause a reduction in packing density as long as it is made in the same horizontal plane as the other connections. The only way in which the situation may be improved is by using a different layer to make the injector connection.

5.5 Substrate-fed-logic

In 1975, Blatt et al described a novel I^2L structure capable of attaining a higher functional density than the conventional struc= ture considered thus far[43]. While most researchers have attempted to increase packing density by designing smaller structures, the writers pointed out that the maximum packing density attainable is invariably limited by interconnection pattern area rather than device area. In designing their structure they set out to improve this situation in the following ways:

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1. A conventional I^2L gate has one input and several out= puts and can implement a logical operation at each output. A multi-input-multi-output structure capable of performing logic operations at both inputs and outputs would in= crease the functional density of a given structure.
2. The interconnection problem would be greatly simplified if the the injector metallization could be removed from the surface so that only the logical interconnections remained.
3. The fan-out of I^2L gates is limited by the maximum allowable distance between the injector and the furthest collector. A structure in which there is little restriction on the position and number of collectors and base contacts is de= sirable.
4. The area occupied by the injector should be minimized.

These considerations led to the development of the struc= ture shown in Fig. 5.17. It is constructed as follows. An n-type epitaxial layer with a doping level of 10^{17} cm^{-3} is grown on a p-type substrate with a doping level of 5×10^{18} cm^{-3} (both somewhat higher levels than normal). After this a lightly doped (3×10^{15} cm^{-3}) p-type epitaxial layer is grown on the n-type layer, and n-type collectors and isolation diffused into it. The low base doping level enable Schottky-barrier-diode contacts to be formed. These provide multiple decoupled inputs and enable a logical AND operation to be performed at the input as described

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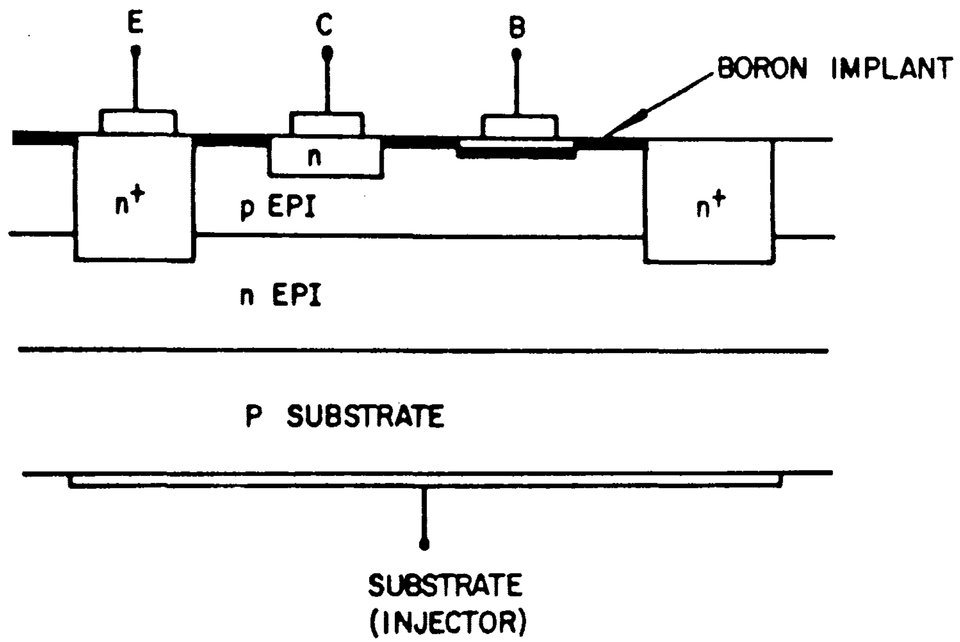

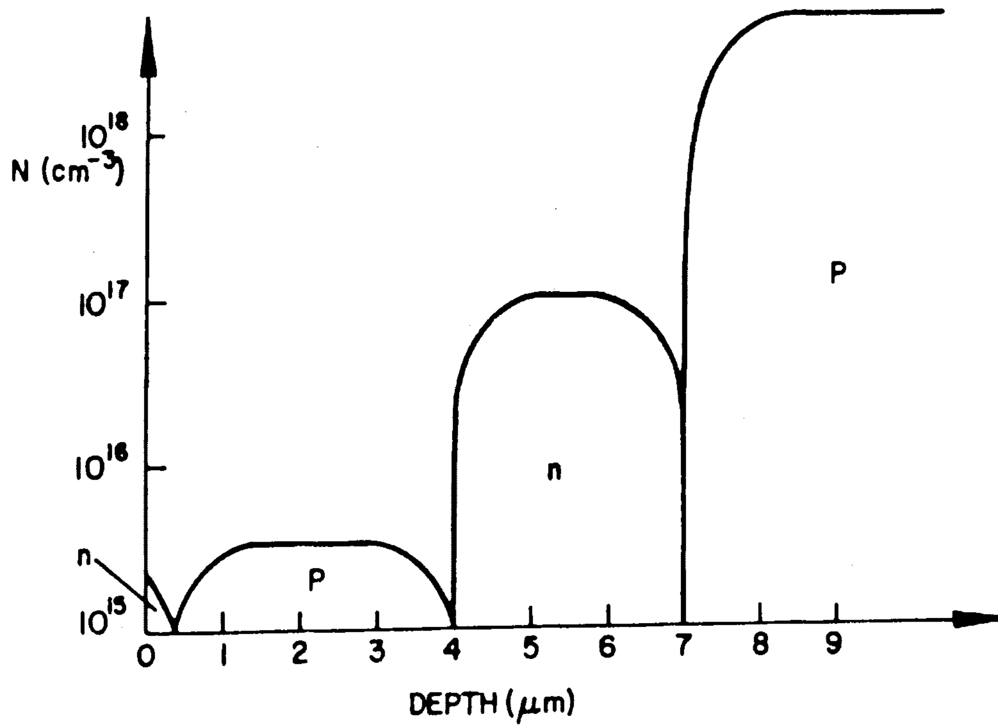

Fig. 5.17: Original SFL gate with doping profile

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above. The low doping also means a high sheet resistance and serious voltage drops between collectors. It is also possible for the surface to invert in the presence of a normal amount of positive charge in the oxide layer. Another problem occurs when a Schottky contact is open circuited. A space-charge layer forms on either side of the Schottky barrier and recombination takes place, lowering the current gain of the npn transistor at low currents. This may be avoided if the base doping below the con= tact is increased. Both these problems are solved by means of a single ion implantation. A silicon dioxide mask which causes the extrinsic base region (but not the base contact) is used for this purpose, implantation taking place through the mask. In the region which is not covered by oxide a Gaussian impurity profile is produced in the base with a maximum below the surface. This ef= fectively reduces the recombination current to Schottky barrier. In the oxide-covered region the implantation is retarded and a high concentration is formed at the surface. This acts as a channel stop, preventing surface inversion from occurring and acts as a low resistance path for the current to the base contact.

However the most interesting feature of the structure is the use of the p-type substrate as the emitter of a vertical pnp transistor which injects current into the base of the npn transistor.

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The conventional lateral pnp transistor has been replaced by the vertical structure which is fully merged with the npn tran= sistor.

Contact to the injector is made via the back of the substrate. Thus no injectors or injector metallization are necessary and the entire surface of the wafer may be devoted to logical inter= connections. The n-epi layer and n^+ isolation grid form a low resistance ground plane as in conventional I^2L. Because the injector contact is made over the entire rear surface the ohmic voltage drop in the injector is uniform throughout the circuit, and all gates will operate at the same current. These properties of substrate-fed-logic (SFL) make it very attractive for use in LSI circuits such as PLAs, ROMs and RAMs. A SFL cross-point element requires only an input and an output on the wafer surface.

Because of the complex process used, SFL is not suitable for direct implementation in process 1. It was decided to develop a simplified version of SFL incorporating only the vertical sub= strate pnp transistor and capable of being produced in the standard process with the minimum of modification. While not exploiting the SFL concept to the full, this approach offers a solution to the voltage drop problem combined with a high packing density.

The doping levels of the original structure were chosen to ensure good emitter efficiencies for both transistors. The sub= strate/n-epi layer doping ratio is 50:1, and the n-epi layer/p-epi

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layer ratio is 33:1. In the case of process 1 with a 6,5 μm epi layer the doping ratio of the npn transistor is reasonable, but a substrate-npn transistor would have extremely poor emitter efficiency. This is because of the presence of the buried n^+ layer which raises the doping level of the base of this transis= tor, and also increases its width to some 12 μm as a result of outdiffusion. If this buried layer were to be omitted, the pro= file would be more favourable for upward pnp action, but the emitter injection efficiency of the npn transistor would be greatly reduced. It was proposed that this undesirable trade-off could be avoided by means of the structure shown in Fig. 5.18(a). An aperture in the buried layer has been introduced at a point in the cell below the base contact and far removed from the ef= fective emitter of the npn transistors. The doping profiles be= low the collectors, and hence the npn upward current gain, re= main unchanged while below the base contact the doping profile favours an upward injection of holes from the substrate into the epi layer, to be collected by the p-type diffused region at the surface. Because injection takes place below the base contact, no extra area is required for the injector.

It was possible to test the feasibility of a substrate-pnp transistor operating in the upward direction by means of a struc= ture in UC1. This structure, shown in Fig. 5.18(b) is a substrate-pnp transistor intended for operation in the downward (Common Collector) mode. Because it has no buried layer, its doping

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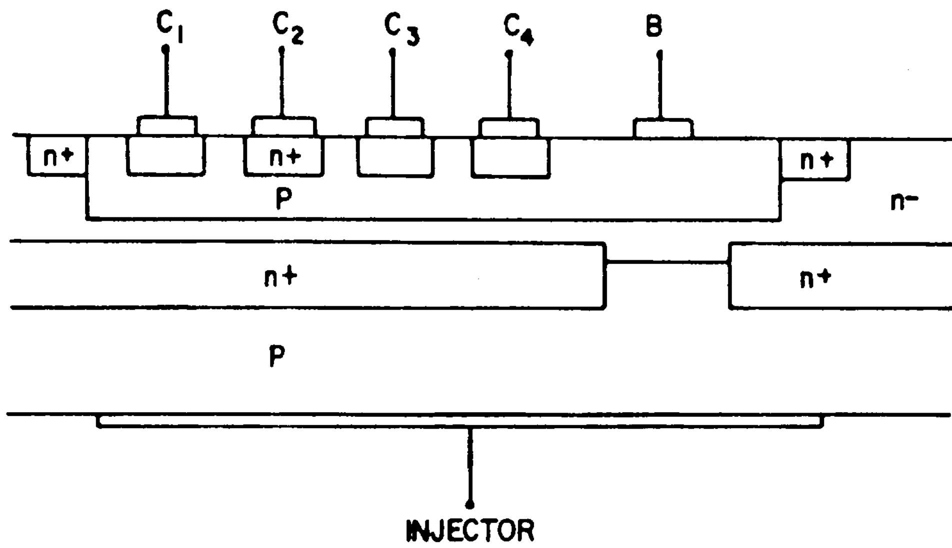

Fig. 5.18(a): Process-compatible substrate-fed I^2L gate

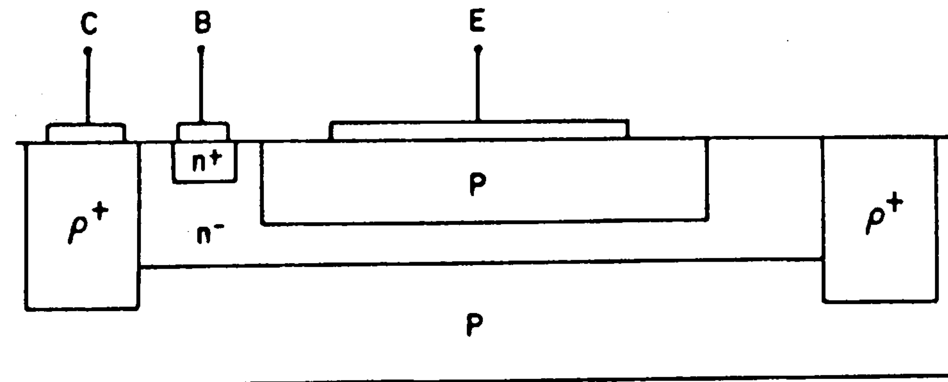

Fig. 5.18(b): UC1 substrate-pnp transistor

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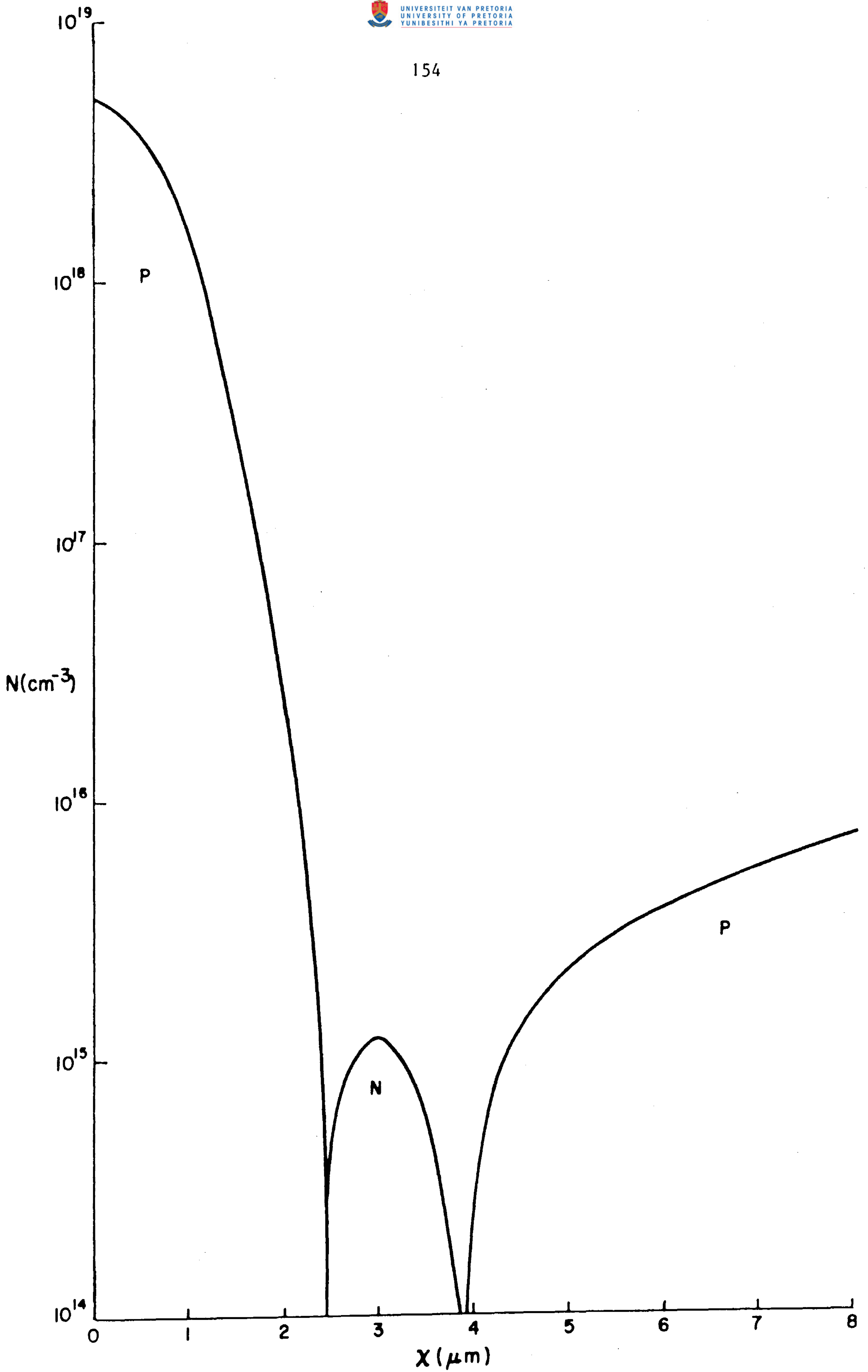

Fig.5.19 Measured doping profile of substrate-pnp transistor

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profile corresponds exactly to that of the operative region in Fig. 5.17. This doping profile has been experimentally de= termined (Fig. 5.19). The current gain of this device when biased in the 'reverse' direction is shown in Fig. 5.20 as a function of emitter current. The common-base current gain has a peak value of 0,68 at I_E = 400 μA and falls rapidly at lower currents. The latter effect is the result of surface re= combination in the large base surface area surrounding the col= lector (the device was dry-sintered). This would not be a se= rious problem in the case of substrate-fed I^2L as the collector would be somewhat larger than the emitter. A problem which is encountered when one forward biases the substrate-epitaxial layer junction is that the p^+ isolation also becomes forward biased with respect to the epitaxial layer and lateral hole injection takes place into the device. As the isolation is only 10 μm away from the collector in the UC1 structure after outdiffusion, it is difficult to determine whether lateral or vertical injec= tion plays a dominant role in the results obtained. In order to acquire more information about the behaviour of a true vertical pnp transistor, special structures were designed and incorporated in the MCL 5 test circuit. These included the following (see Appendix A3):

(i) Substrate pnp transistors, both with and without aper= tures in their buried layers. The isolation around the transistors was placed 100 μm away from the col= lectors to prevent collection of the lateral injection component. However in order to calculate the α of the vertical transistor, the magnitude of the vertical

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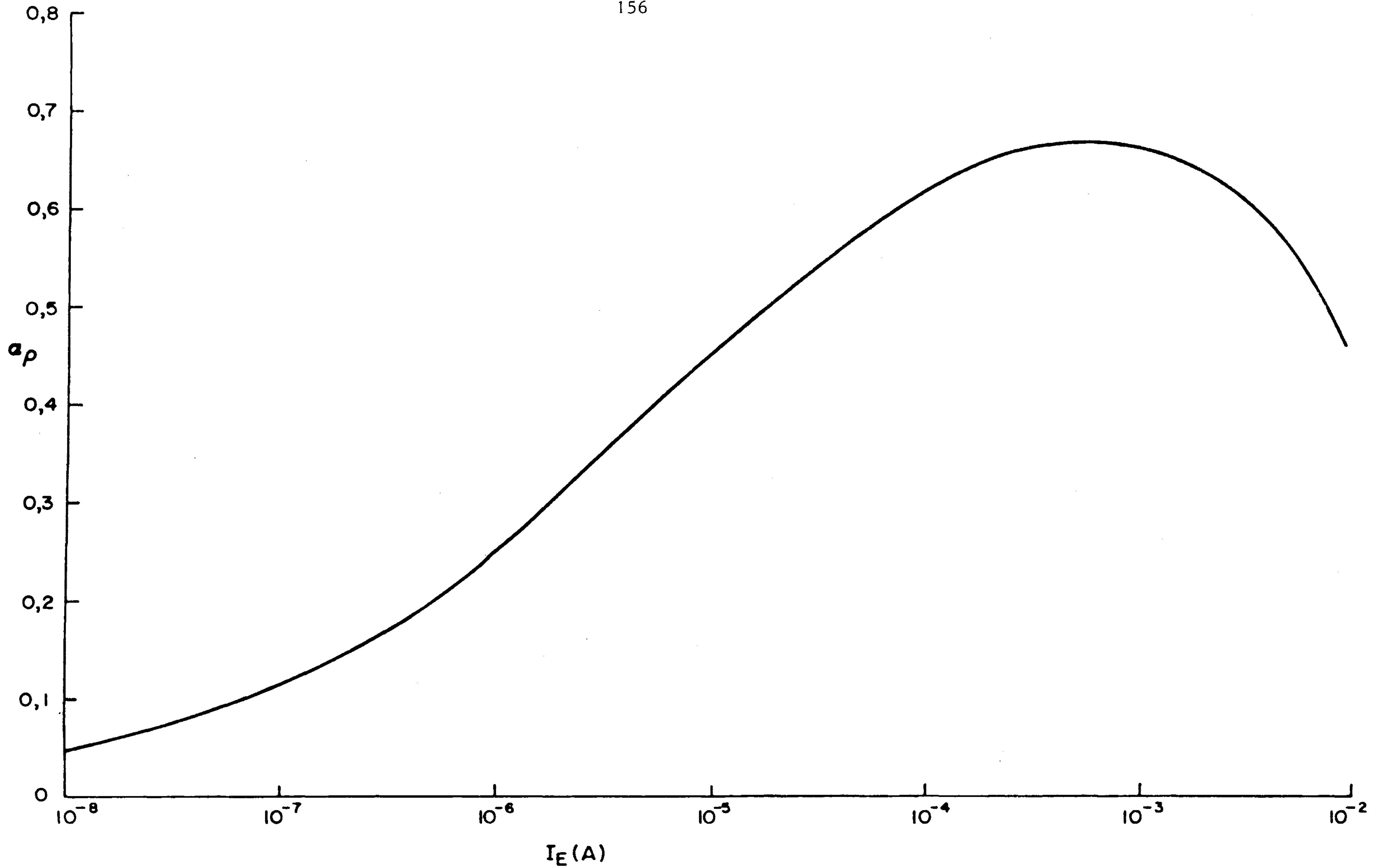

Fig. 5.20: Common-base current gain α_p of substrate-pnp transistor on UC1 (reverse operation)

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and horizontal components of the emitter current must be determined. It was proposed that this be done by means of comparative measurements on two transistors, one with an aperture in the buried layer and the other without. In the latter struc= ture only the horizontal emitter current component is present and it may be measured as function of V_{be}. By subtracting this current from the total emitter current of the former structure at the same value of V_{be} the vertical current component and hence, the current gain, may be determined. In practice it was found that this method is not practicable and no reliable results could be obtained. The reason would appear to be that the vertical current is considerably smaller than the horizontal one, and the calculation is easily upset by other factors such as minor processing variations between circuits. In many cases negative values of α were obtained!

(ii) A ring oscillator with substrate injectors. This device was capable of oscillation, thereby demonstrating in principle the operation of the simplified version of SFL. The frequency of oscillation was however far lower at a given value of current than was the case for an identical oscillator with lateral injectors. This tends to substantiate the aforementioned theory that the ef= fective injector current is far smaller than the total injector current.

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The results obtained with these structures are therefore very inconclusive owing to the impossibility of measuring α_u accurately. From theoretical consi=derations the structure should be capable of achieving a usable value of upward current gain. Assuming an abrupt junction between substrate and epitaxial layer, a theoretical α_u value is given as

$$\alpha_u = \gamma \cdot \alpha_T$$

$$\doteqdot \frac{1}{1 + \frac{D_n N_D W_B}{D_p N_A L_n}} \cdot \frac{1}{1 + \frac{W_B^2}{2L_n^2}}$$

$$= \frac{1}{1 + \frac{22 \cdot 6,5 \times 10^{15} \cdot 1,5}{10 \cdot 1,7 \times 10^{16} \cdot 81,2}} \cdot \frac{1}{1 + \frac{1,5^2}{2 \cdot 81,2^2}}$$

$$= 0,98 \qquad 5.39$$

Furthermore the collector is somewhat larger than the emitter, thus ensuring good collection of minority carriers throughout the base. The current gain would also be maintained at low currents owing to the absence of a $Si\text{-}SiO_2$ interface above the in=trinsic base. It would therefore appear that the structure is worth further investigation. The obvious

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solution to the problem of lateral injection is to replace the diffused isolation with some form of oxide isolation such as the afore-mentioned iso= lation by anodization of silicon. The upward gain α_u could then be measured directly. In an LSI cir= cuit the presence of a p^+ isolation diffusion is of little importance as it would only occur at the pe= riphery of the digital section isolating it from in= terface or analog circuitry. Gates within the array would experience only vertical injection, while those at the periphery would receive both vertical and ho= rizontal injection, resulting in a wastage of current. To ensure a uniform distribution of current throughout the array, the scheme shown in Fig. 5.21 could be used. The apertures in the buried layer below the pe= ripheral cells are omitted and a region of p-base dif= fusion is formed overlapping the isolation and extending to 12 μm from the peripheral cells. This region will act as the emitter of a lateral pnp transistor injecting current into the peripheral cells. By a suitable choice of emitter areas the currents i_h and i_v may be made equal, giving the required uniformity of current dis= tribution. The base width of the lateral pnp transistor is now well controlled as both emitter and collector are formed during the same diffusion.

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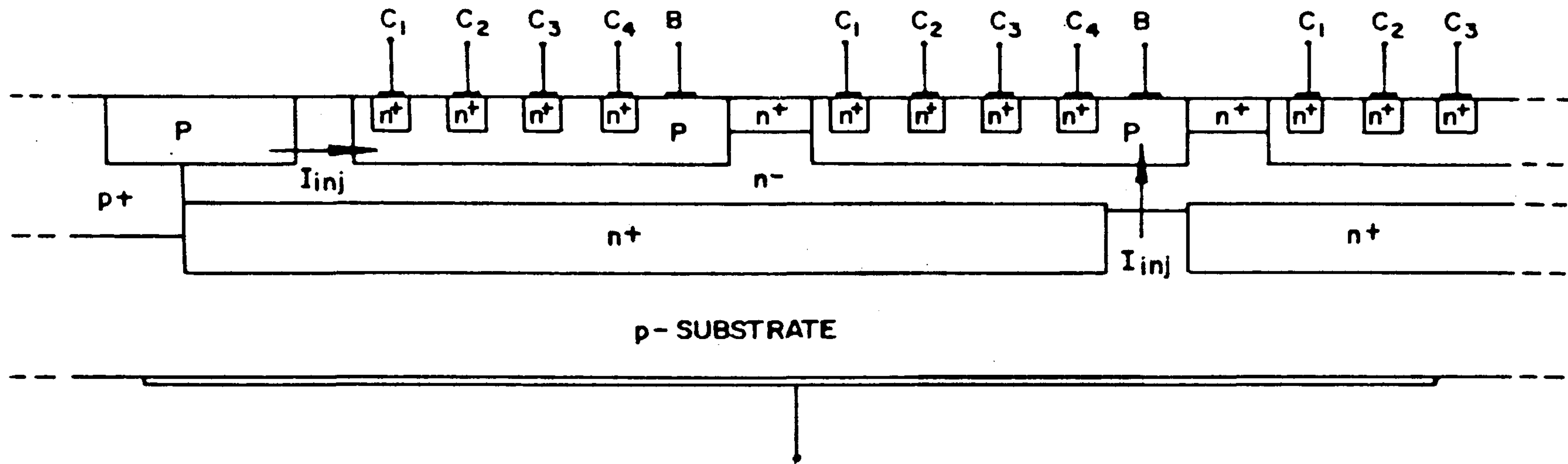

Fig.5.21 A section of the proposed SFL LSI circuit, showing lateral and vertical injectors

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Despite the theoretical feasibility of junction-isolated SFL, it was decided that in view of the urgent need for the PLA a circuit would first be designed using conventional I^2L with lateral injectors, these devices having been fully characterized by measure= ment. This would involve some sacrifice of packing density (the number of product terms was eventually reduced to 80) but would ensure a working prototype in the shortest possible time.

Development of SFL for use in a second version of the PLA as well as other LSI designs would ne= vertheless continue, as the absence of injectors on the surface of any LSI design would both increase packing density and simplify the logical interconnec= tion problem.

5.6 Interface circuits

I^2L is an LSI logic family using small voltage swings and low operating currents. Junction and stray capacitances within the chip are small. This is in strong contrast to the digital 'out= side world' where logic signals are in the form of voltage swings of several volts, currents are in the mA range and capacitance levels are high. Input interfaces capable of generating suitable current-mode signals to drive the I^2L circuitry and output inter= faces capable of producing large voltage swings when driving large capacitive loads are therefore required. The most commonly used

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random logic family today is transistor-transistor logic (TTL), operating from a +5 V power supply. Use of this voltage is so widespread that it has become a de facto stan= dard for LSI circuits. Also widely used is CMOS logic, operating from any voltage between 3 V and 15 V. It was therefore decided that TTL compatibility of inputs and out= puts would be the primary requisite, while CMOS compatibility would also be desirable. On this basis the following speci= fications were compiled:

(i) The input interface should be capable of providing an injector current of suitable magnitude to the input gates of the PLA while being driven by a single TTL or CMOS gate.

(ii) The output interface should be capable of driving a single TTL or CMOS gate at all frequencies of inte= rest (≤ 1 MHz), while consuming a minimum of current when not in use.

5.6.1 Input interface

Table VI compares the limits on voltage levels required for correct operation of TTL and CMOS gates. A suitable threshold voltage must be chosen to satisfy both logic families. This threshold must lie between 0,4 V and 2,4 V. It is also desirable that the whole circuit should operate from a single 0,7 V supply. This mini= mizes chip dissipation and saves an extra pin on the package. An input interface was also required for other

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Parameter	I^2L	TTL	CMOS (10 V)
Logical '0' input voltage	$V_{ce(sat)}$	< 0,8 V	2 V
Logical '1' input voltage	V_{be} (0,7 V)	> 2 V	> 8 V
Logical '0' input current	I_{inj}	< -1,6 mA	-1 μA
Logical '1' input current	0	< 40 μA	< 1 μA
Logical '0' output voltage	$V_{ce(sat)}$	< 0,4 V	< 1 V
Logical '1' output voltage	< BV_{ceo}	> 2,4 V	> 9 V
Logical '0' output current	I_{inj}	16 mA max.	40 mA max.
Logical '1' output current	0	-55 mA max.	-30 mA max.

TABLE VI

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I^2L circuits to be produced and so a general purpose circuit capable of driving one gate load was first designed. This circuit was breadboarded and thoroughly tested using UC1 and MCL5 components (see Fig. 5.22). Using the available injector rail an additional pnp transistor (T6) is formed, generating a current exactly equal to twice the current injected into each cell. This current is fed into a current mirror (T4, T5). The structure has a gain of almost unity.

$$\frac{I_1}{2\ I_{inj}} = \frac{\beta_n}{\beta_n + 1}$$

When the input voltage V_{in} exceeds a value of $V_{be1} + V_{be3} + V_{ce(sat)4}$, or about 1,5 V, transistor T1 turns on causing a current $I_2 = I_1 \cdot \frac{\beta_p}{\beta_p + 1}$ to flow. The value of β_p can vary considerably but a typical value of 10 is reasonable below 200 μA of collector current.

$$\therefore I_2 = 0{,}91\ I_1$$

The I^2L gate is therefore fed with a current virtually equal to twice its collector current, enabling it to function correctly when $\beta_u \geq 0{,}5$. The higher current was provided to help compensate for the larger

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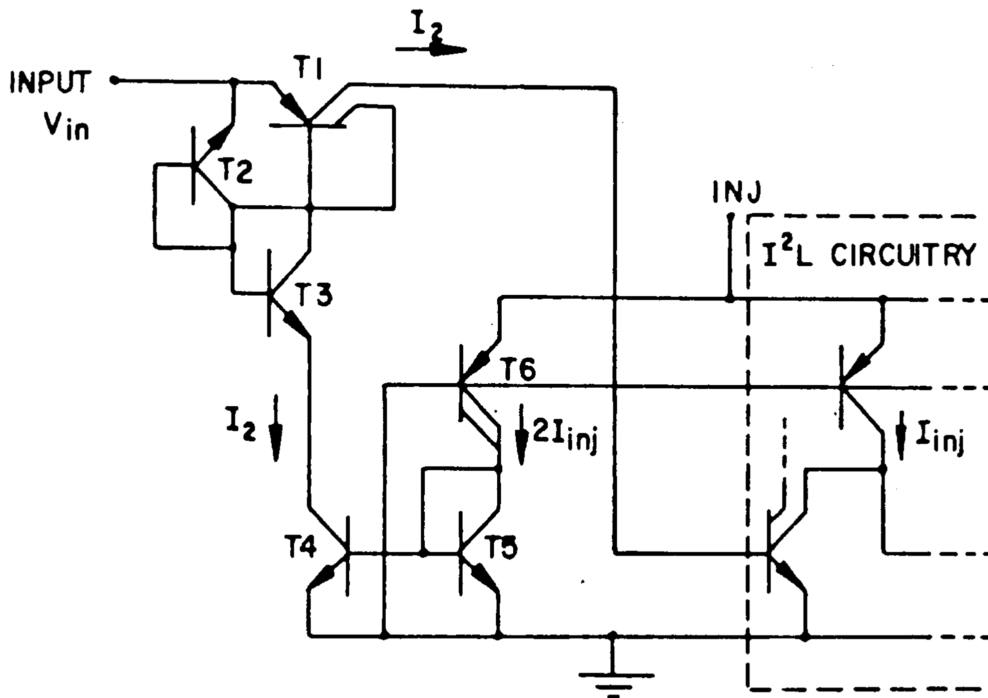

Fig. 5.22: General-purpose input interface

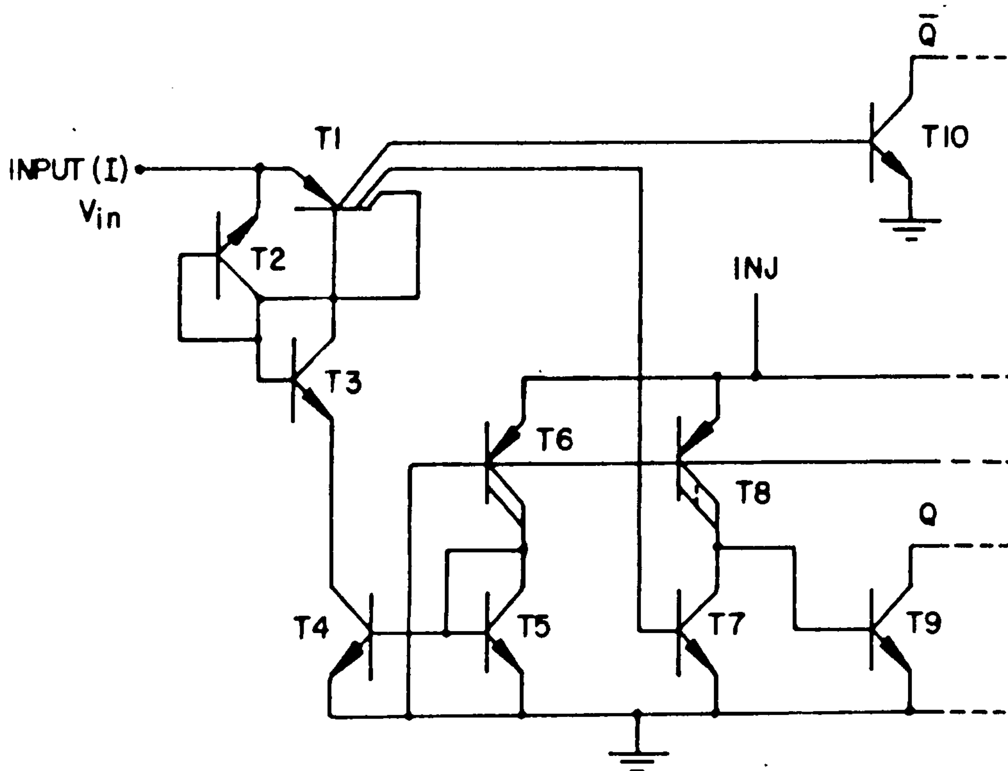

Fig. 5.23: PLA input interface

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capacitances associated with conventional transistors. The input threshold voltage of 1,5 V is suitable for both TTL and CMOS. A big advantage of this circuit is that it is fully supply-voltage independent and any lo= gical '1' voltage greater than 1,5 V is acceptable. The maximum input voltage is ultimately limited by BV_{CEO} of T4. Because of the increased out-diffusion of the buried layer this voltage is much lower than normal and is usually around 5 V. To enable higher voltages to be accommodated, the buried layer of this transistor is omitted, which enables the specified breakdown voltage of > 12 V to be maintained, but at the expense of in= creased series collector resistance. The latter is how= ever not a problem at currents below 100 μA. The break= down voltage of a lateral pnp device is equal to BV_{CES} and is greater than 20 V, even for the I^2L process.

A problem encountered with this circuit was the back-injected current in the saturated transistor T6. This arises because the collector base junction of T6 is forward biased and causes the collector current of T5 to be reduced. It can however be 'designed out' to a large extent by a suitable choice of geometries for T5 and T6. The analysis of this problem is identical to that of the back-injection in the injector pnp transistor, except that the current collected by the substrate must also be taken into account (because $\beta_n >> \beta_u$). We may therefore write directly from equation 5.22 that

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$$\beta = \frac{\beta_n}{1 + k\beta_n}$$

where

$$k = \frac{I_{sp}}{I_{sn}}$$

$$= \frac{I_{sph} + I_{spv}}{I_{sn}}$$

$$= \frac{J_{sph} A_{hp} + J_{spv} A_{vp}}{J_{sn} A_n}$$

Values for the three saturation current densities were determined by measurement as

$$J_{sph} = 1,41 \times 10^{-19} \text{ A}/\mu\text{m}^2$$

$$J_{spv} = 5,78 \times 10^{-21} \text{ A}/\mu\text{m}^2$$

$$J_{sn} = 4,42 \times 10^{-19} \text{ A}/\mu\text{m}^2$$

$$\therefore \beta = \frac{\beta_n}{1 + \dfrac{1,41 \times 10^{-19} A_{hp} + 5,78 \times 10^{21} A_{vp}}{4,42 \times 10^{-19} A_n} \beta_u} \qquad 5.40$$

By connecting various numbers of npn transistors in pa= rallel it was possible to simulate the effect of various values of A_n. The results obtained fully support equation 5.40 and one shown in Table VII.

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n	nA_n	β_n Theoretical	β_n Measured	% Error
1	768	8,7	8,2	+6
2	1 536	15,3	14,5	+5,5
3	2 304	20,5	18,5	+10,8
4	3 072	24,6	21	+17,1
5	3 840	28	24	+16,7

TABLE VII

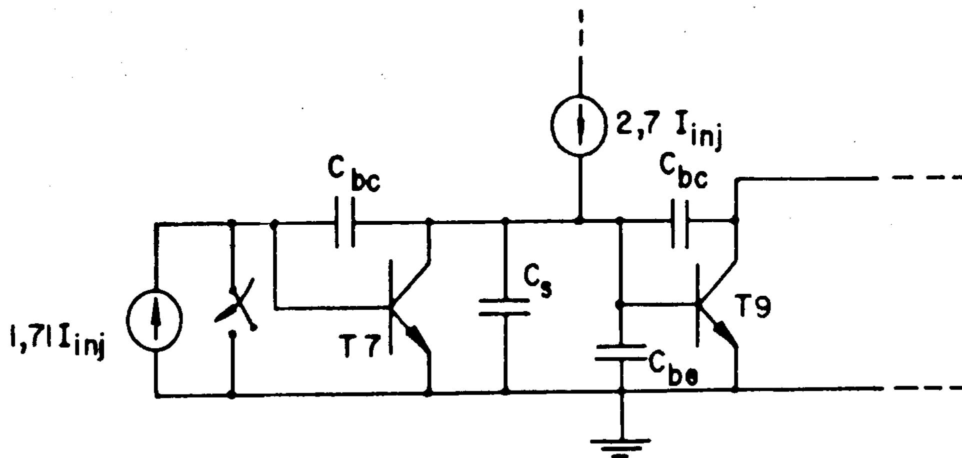

Fig. 5.24: Model of node capacitances in the PLA input interface

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There are certain constraints on the choice of values for the three areas. With a base width of 8 μm, a 28 μm long collector for T6 yields a collector current of $2I_{inj}$, as previously described. The injec= tor of a standard cell is also 28 μm long, but the base width after out-diffusion is 8 μm, whereas T6 will then have a 4 μm base width. This gives the required 2:1 current ratio, as the current injected across a base is proportional to junction area but inversely proportional to base width ($I_{cs} = qAD_{ni}^{2}/N_D W_p$). The areas A_{hp} and A_{vp} are then fixed as 70 μm^2 and 448 μm^2 respectively. Choosing A_n = 660 μm^2 and assuming a worst-case value for β_n of 40 we find from equation 5.40 that β = 14,7; therefore I_1 = 1,88 I_{inj}, and I_2 = 1,71 I_{inj}.

This general-purpose interface was modified to suit the PLA, which requires a fanout of 20 (80 collectors at four collectors per gate), and complementary signals. A collector is added to T1 giving two decoupled outputs, one of which drives the npn transistor T10 which can sink a worst-case current of 80 I_{inj}, giving a safety factor of four. The output of T10 is the complement of the input. The second collector drives the T7/T8/T9 com= bination which yields an in-phase signal, but with greater delay than the output of T10. This delay is almost en= tirely due to the time required to charge and discharge

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the capacitances attached to the base of T9. As T9 needs a large emitter its base emitter capacitance will dominate. Increasing the available current by the collector area of T8 will be of little value, as this will force a corresponding increase in T9's emit= ter size and hence, capacitance. A current of 2,7 I_{inj} was chosen, purely for layout convenience. T8 then has a collector length of 47 μm, and equation 5.40 yields an emitter size for T9 of 2 007 μm^2 (54 μm x 37 μm).

The overall speed of the interface is limited by this node. Using the model in Fig. 5.24, its average de= lay may be found. The rise time is

$$t_1 = \frac{\Delta V}{2,7\ I_{inj}} (C_{be} + C_s + 2\ C_{bc})$$

and the fall time

$$t_2 = \frac{\Delta V}{2,7\ I_{inj}} \frac{(C_{be} + C_s + 2\ C_{bc})}{1,71\ \beta - 1}$$

$$\therefore\ t_d = \frac{t_1 + t_2}{2}$$

$$= \frac{\Delta V}{5,4\ I_{inj}} (C_{be} + C_s + 2\ C_{bc}) \left(1 + \frac{1}{1,71\ \beta - 1}\right)$$

$$\doteq \frac{\Delta V}{5,4\ I_{inj}} (C_{be} + C_s + 2\ C_{bc})$$

$$= \frac{\Delta V}{5,4\ I_{inj}} (6,17\ pF + 1,29\ pF + 1,69\ pF)$$

$$= 1,69 \times 10^{-12} \frac{\Delta V}{I_{inj}} \qquad 5.41$$

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This equation will be used later in a calcula= tion of the overall speed of the complete circuit.

5.6.2 Output interface

It was decided to use open collector output interfaces, for two reasons:

(i) They enable the capacity of the PLA to be in= creased by a wire-AND of several PLAs in parallel;

(ii) no specific supply voltage need be brought onto the chip.

The circuit in Fig. 5.25(a) was eventually used. This is electrically similar to an I^2L gate but uses an npn transistor in the normal mode in order to achieve a high-current sinking capability at the output. For a fan= out of unity into a TTL load the output transistor must be able to sink at least 1,6 mA. Using 2 mA as a design value and assuming $\beta_n \geq 20$, we need a current of $\frac{2\ 000}{20}$ = 100 µA at the base of T2. We now need to decide on a collector area for T1, but this is no easy matter, for the following reasons.

(i) For the PLA to operate at low currents, $I_1 \gg I_{inj}$.

(ii) For the OR array to drive the output interface correctly, $I_1 \leq \beta_u\ I_{inj}$.

Thus making $I_1 \simeq I_{inj}$ will require that the whole circuit be operated at a current of 100 µA/gate thereby greatly increasing power consumption. If, on the other

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hand, we make $I_1 > I_{inj}$ we increase the requirement for β_u, which will probably have a detrimental effect on yield. It was decided to make the length of the collector T1 = 100 μm. This implies that $I_1 = \frac{100}{28} I_{inj} = 3,6\ I_{inj}$. Under worst-case conditions (only one product term selected), β_u must therefore be greater than 3,6. The minimum operating current is now pegged at 28 μA per gate. The geometry of T2 is determined from that of T1 by using equation 5.40 to ensure that $\beta = 20$ when $\beta_n = 40$. This gives a value of $A_n = 5\ 780\ \mu m^2$.

A dynamic analysis of the interface must be made to determine the delay contributed by capacitance at the base of T2. The following capacitances appear at this point:

(i) 80 I^2L device collector-base capacitances amounting to 80 x 0,547 = 43,76 pF.

(ii) Aluminium capacitance to ground, estimated at 24 pF.

(iii) C_{be} of T2, 2,5 pF.

Total capacitance therefore amounts to approximately 70 pF. Assuming $\beta_u \simeq 5$, we may write that

$$t_{do} = \frac{\Delta V}{3,6\ I_{inj}}\ 70 \times 10^{-12}$$

$$= 19,4 \times 10^{-12}\ \frac{\Delta V}{I_{inj}} \qquad 5.42$$

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As T2 has no buried layer for high breakdown voltage and yet carries a current in excess of 1 mA, an analysis of the series collector resistance is called for. Fig. 5.25(b) shows the layout of this de= vice. We may assume a uniform distribution of current throughout the intrinsic transistor area. The lateral current flowing to the collector contact on either side of the emitter can be modelled as flowing from a line equi-distant from the centre line and the edge of the emitter. The resistivity of the epitaxial layer is 0,8 Ω cm. The resistance to each collector contact is therefore

$$R = \frac{0{,}8 \ . \ 14}{1{,}5 \times 16^{-4} . 180} + \frac{0{,}8}{2{,}5 \times 10^{-4}} \cdot \frac{12}{180}$$

$$= 414{,}8 \ \Omega + 213{,}3 \ \Omega$$

$$= 628 \ \Omega.$$

The total series resistance R_c of the device is $\frac{R}{2}$ or 314 Ω. At a current of 2 mA this will add 0,628 V to the saturation voltage of the transistor.

5.7 Overall layout and prediction of performance

Fig. 5.26 is a computer plot of the layout as digitized by means of a CALMA graphic display system. The complete chip has overall dimensions of 3,53 mm by 4,12 mm. The active circuit area ex= cluding scribe channel and bonding pads is approximately 13,4 mm^2.

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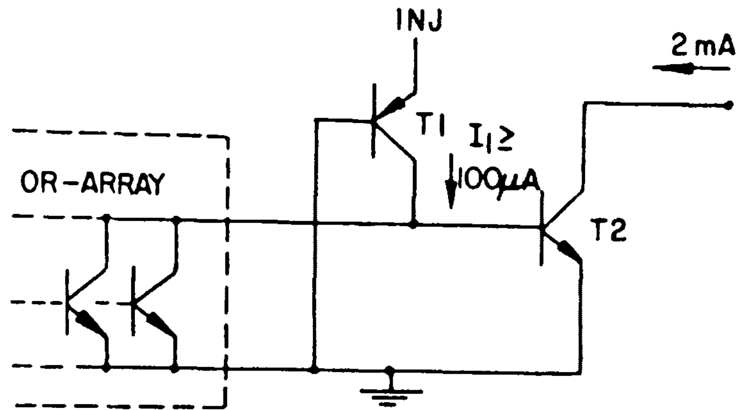

Fig.5.25(a)Circuit diagram of output interface

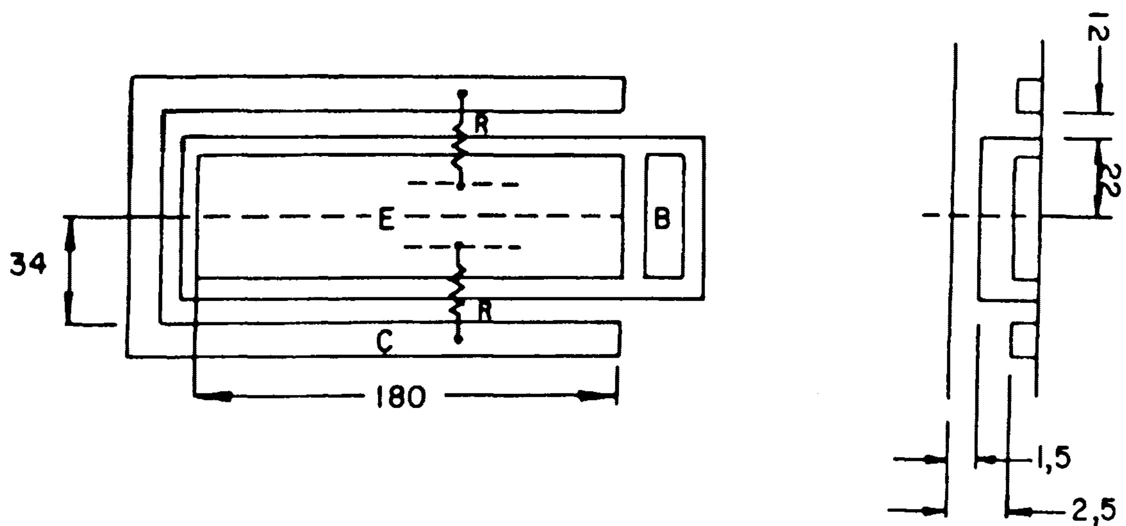

Fig.5.25(b) Calculation of series collector resistance

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The largest portion of the active area (52%) is occupied by the AND-array. The basic structure of this array has been thoroughly described in 5.4. The array contains 640 four col= lector gates giving a gate-packing density of 92 gates/mm^2. The reason for this relatively low value is of course the large percentage of array area occupied by n^+ underpasses (about 50%). The size of this array could be virtually halved if two-layer metallization were available. If the structure is considered as a ROM (One collector = One bit) the density is 367 bits/mm^2. On this basis a 4k ROM could be produced on a chip with an active area of 11,1 mm^2 (3,3 mm x 3,3 mm).

The OR-array is considerably smaller (17% of active area) and has been divided into two halves. This was necessary be= cause of the difference in pitch between the 80 outputs of the AND-array (pitch = 24 μm) and the 80 inputs of the OR-array (pitch = 36 μm). If all the gates had been placed in a single array a considerable amount of space would have been wasted. A disadvantage is that the outputs of the two halves must be joined together. This is done by means of eight aluminium lines running down the left-hand side of the AND-array.

The 16 input interfaces are positioned on either side of the chip in Fig. 5.26, with inputs I_1, I_3, I_5 --- I_{15} on the left and I_2, I_4, I_6 --- I_{16} on the right. They are designed to make use of the space between bonding pads and are laid out

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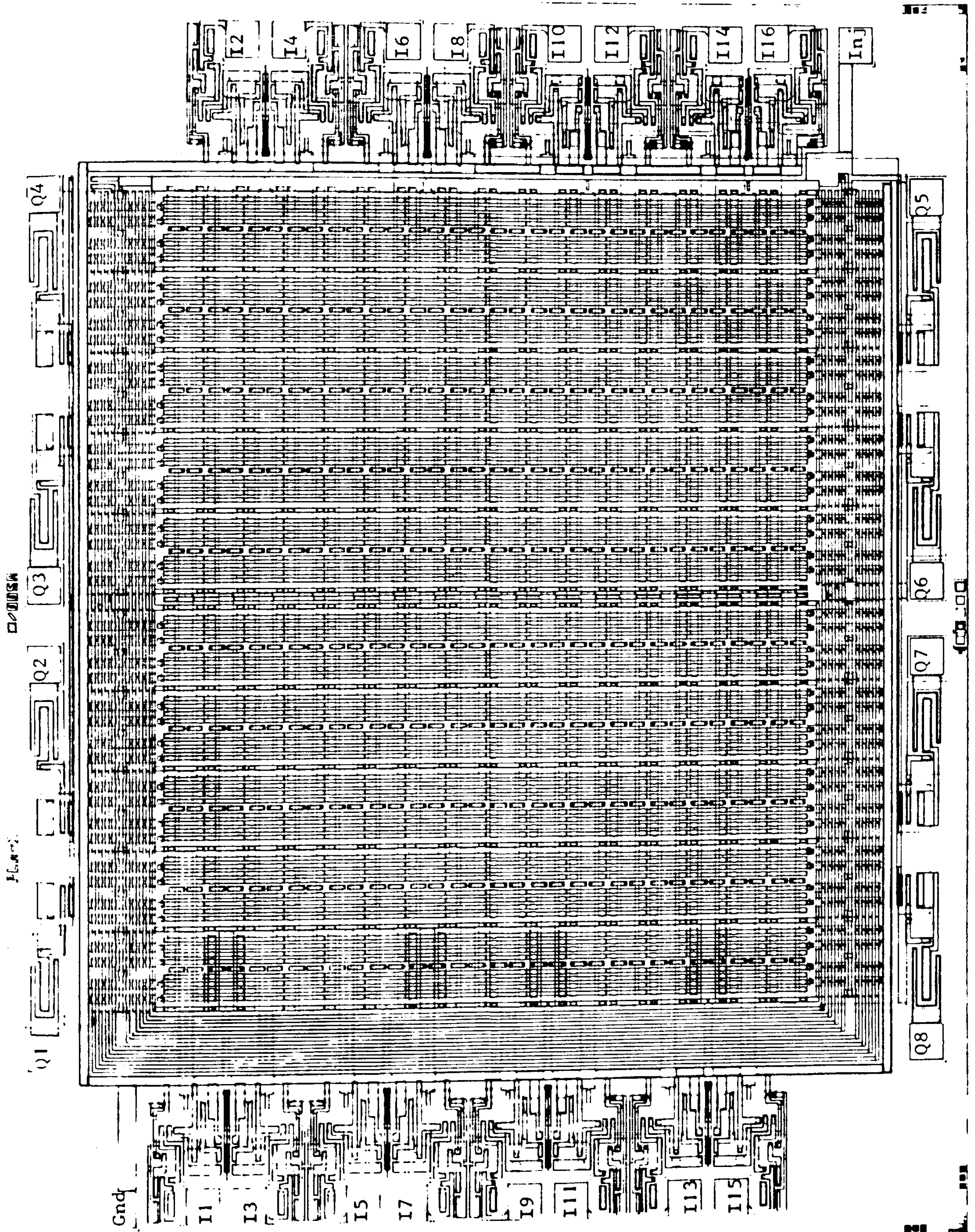

Fig. 5.26: Prototype circuit, code-named PLA-1

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in mirror-imaged pairs. This enables a common injector rail to be used for each pair. Each interface has an area of 0,13 mm^2 and the 16 interfaces occupy 16% of the active area. The eight output interfaces are arranged at the top and bottom of the chip in Fig. 5.26.

Because of the large total current flowing into the chip, all voltage drops in the injector or ground return circuits must be kept to a minimum. For this reason all injector rails are joined to the injector contact at both ends. The maximum voltage drop which can then occur is only one quarter of the voltage drop occurring at the same current with only one end of the rail connected. All injector metallization is made as wide as possible. The ground return circuit is made via the buried n^+ layer and a shallow n^+ contact which completely surrounds the I^2L part of the circuit, thereby minimizing the distance between any point in the circuit and the contact. This effect is carried a stage further by including an n^+ contact strip running verti= cally down the middle of the circuit in Fig. 5.26.

Although a high packing density in the active area was achieved, there are large unused areas in each corner of the chip. It was envisaged that these would be used for adding flip-flops in a later version of the device.

A theoretical prediction of performance will now be made. This will be compared with measured results in the following chapter. The most important performance parameter is the speed-power relationship, which has already been analysed for the basic

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gate and the interface circuits. A basic gate has a delay of

$$t_d = \frac{\Delta V}{2\ I_{inj}} (C_{be} + (F+2)\ C_{bc}) \qquad 5.4$$

For the 4-collector gate, C_{be} = 4,87 pF and C_{bc} = 0,55 pF. In the case of the AND-array the capacitance of the n^+ under=pass appears in parallel with C_{be}. This capacitance amounts to 4,17 pF per gate. The delay of a gate in the AND array is therefore

$$t_{da} = \frac{\Delta V}{2\ I_{inj}} (4,87 + 4,17 + (4+2).0,55) \times 10^{-12}$$

$$= 6,16 \times 10^{-12} \frac{\Delta V}{I_{inj}} \qquad 5.43$$

For the OR array the fanout is eight but a current of 2 I_{inj} per cell is provided, giving an effective fanout of four. The junction capacitances are C_{be} = 10 pF and C_{bc} = 0,55 pF. An additional capacitance of 2,29 pF per gate must be added for the aluminium connections to the gate inputs.

$$\therefore = \frac{\Delta V}{2.2\ I_{inj}} (10 + 2,29 + (8+2)\ 0,55).10^{-12}$$

$$= 31,69 \times 10^{-12} \frac{\Delta V}{I_{inj}} \qquad 5.44$$

The speed-power equations for the input and output interfaces have already been determined as

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$$t_{di} = 1,69 \times 10^{-12} \frac{\Delta V}{I_{inj}} \qquad 5.41$$

and $$t_{do} = 19,4 \times 10^{-12} \frac{\Delta V}{I_{inj}} \qquad 5.42$$

The total propagation delay through the circuit is

$$t_{dt} = t_{di} + t_{da} + t_{dor} + t_{do}$$

$$= \frac{\Delta V}{I_{inj}} (1,69 + 6,16 + 31,69 + 19,4).10^{-12}$$

$$= 31,69 \times 10^{-12} \frac{\Delta V}{I_{inj}} \qquad 5.45$$

The total chip current is

$$I_t = I_i + I_a + I_{or} + I_o$$

$$= 16\ (2+2,7)\ I_{inj} + 640\ I_{inj} + 80.2\ I_{inj} + 8.3,6\ I_{inj}$$

$$= 904\ I_{inj}$$

$$\therefore\ t_{dt} = 31,69 \times 10^{-12} \times 904 \frac{\Delta V}{I_t}$$

$$= 2,86 \times 10^{-8} \frac{\Delta V}{I_t} \qquad 5.46$$

Assuming $\Delta V \doteqdot V_{be}$, equation 5.46 is depicted in Fig. 5.27. 1 MHz operation is possible at a total chip dissipation of 28 mW.

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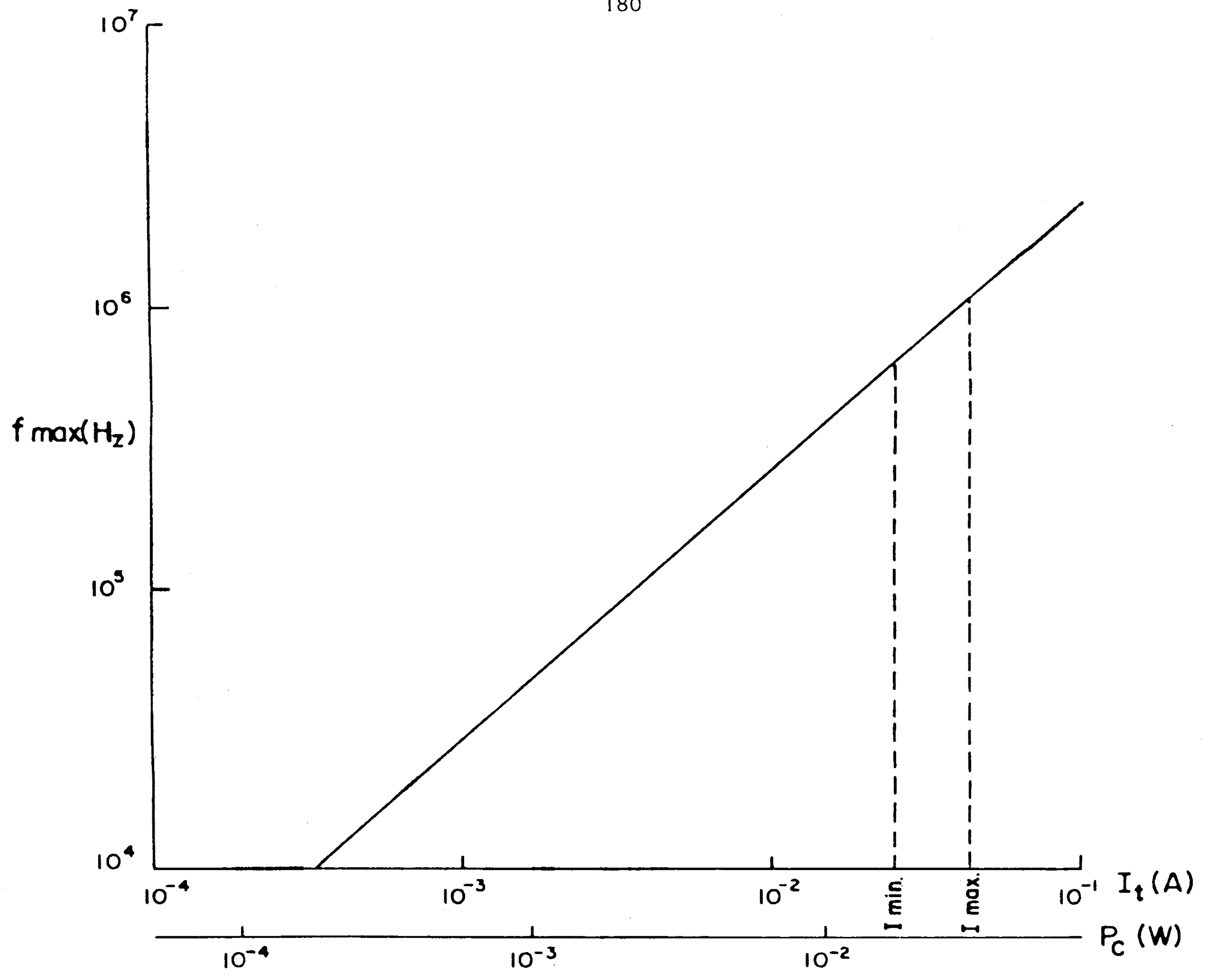

Fig. 5.27: Theoretical curve of f_{max} vs I_t and P_c

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The theoretical operating limits are also indicated. The upper limit is determined by voltage drop considerations (see 5.4) and the lower limit by the requirement of driving a TTL load. If only CMOS circuits were to be driven (or low-power Schottky TTL) this limit could be considerably re=duced.

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CHAPTER 6

6. THE TEST SYSTEM AND THE RESULTS OBTAINED

6.1 The test pattern

The prototype PLA, code-named PLA-1, was programmed with a test pattern designed to enable the full capabilities of the circuit to e evaluated. Programming is achieved by means of a set of optional contact windows in the contact window mask (see Fig. 4.4). To enable the contact window mask to be designed quickly, a coding diagram has been devised (Fig. 6.1). On this form, the position of each input-, output- and product term-line is indi= cated by means of a labelled line. The programming operation lies in placing contact windows at the intersections of those lines. Placing a contact window at the intersection of an input- and a product-term-line includes that input in the product formed on the product-term line. Placing a window at the intersection of a pro= duct-term and an output-line includes the product term in the OR-function formed at that output line. The coding diagram may be used by the designer to specify the program required. The mask is produced by digitizing the coding form using the CALMA system. An additional improvement would be to add the injector contact-windows to the coding form. This would enable the injectors of unused gates to be disconnected, thereby reducing power consumption.

The truth-table of the test pattern was compiled with the following considerations in mind:

1. No yield-versus-area data was available for the I^2L pro= cess. The PLA should therefore be tested in such a way

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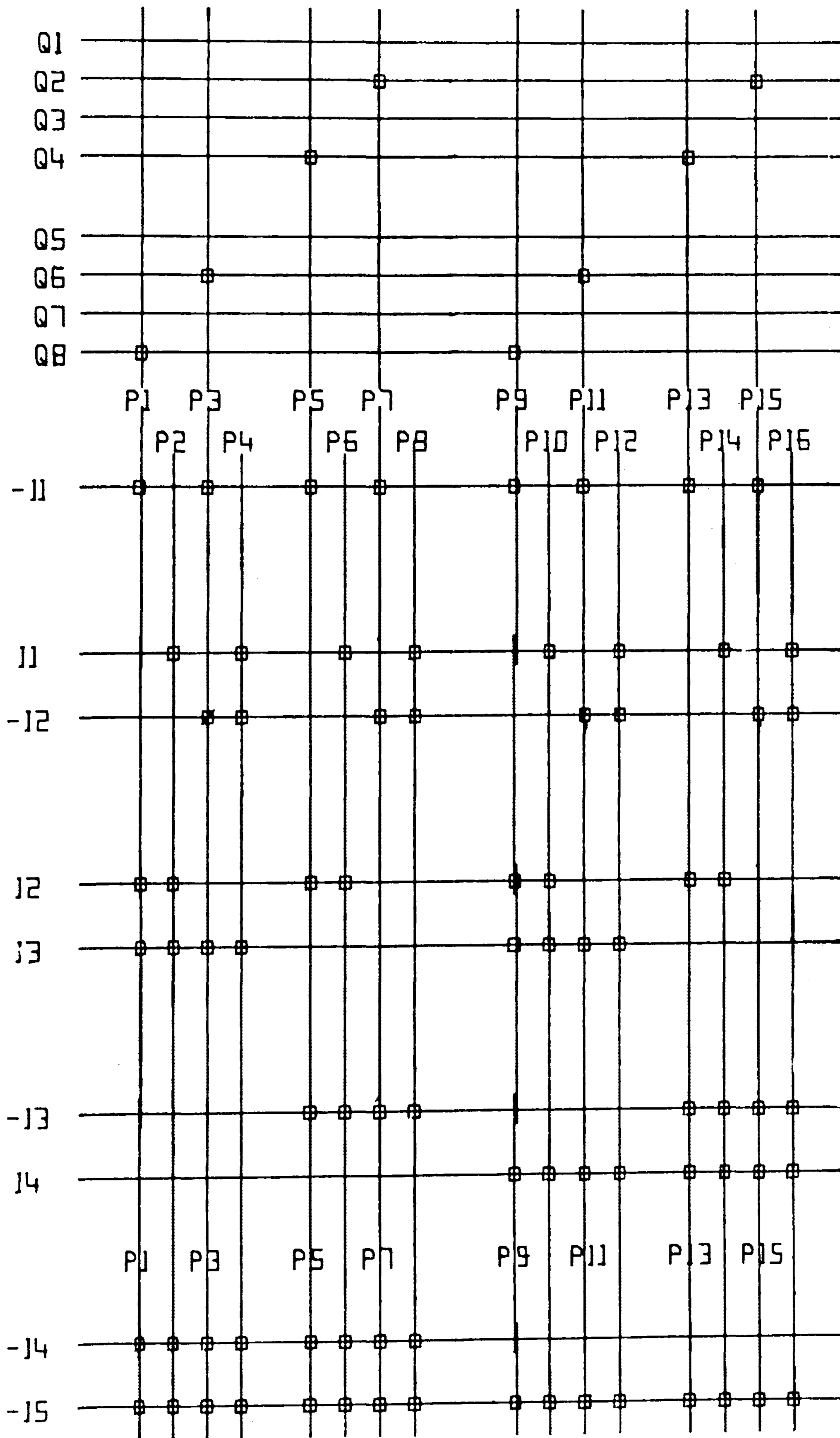

Fig.6.1 Part of the coding form

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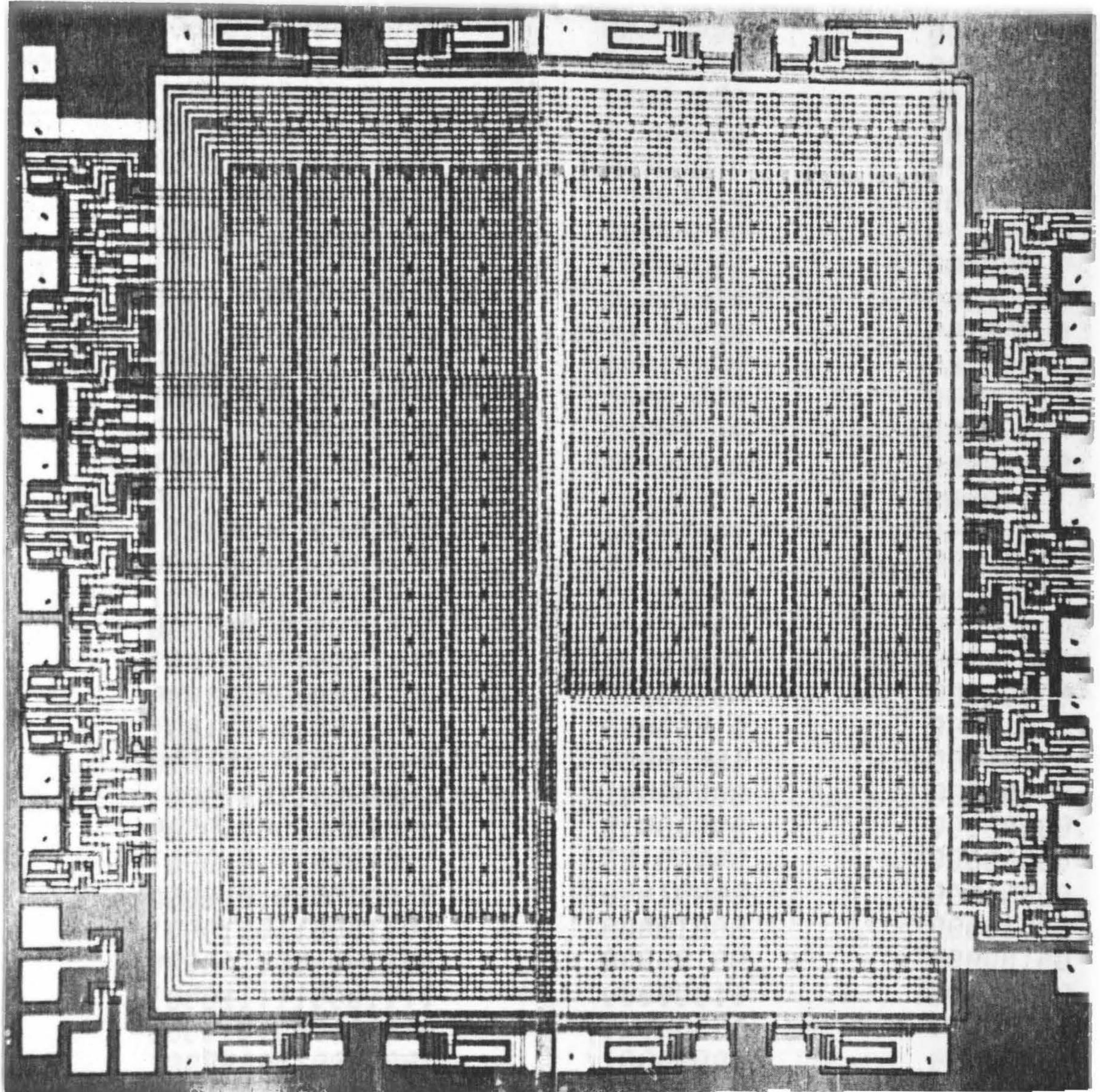

Fig.6.2 PLA-1

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STROOMBAAN NO   PLA000066.RS

NO TERM	INSET-ADRES	VERWAGTE WAARDE	RESULTAAT
1	0000000000000000	00000000	00000000
2	0000000000000000	00000000	00000000
3	0000000000000000	00000000	00000000
4	0000000000000000	00000000	00000000
5	0000000000000000	00000000	00000000
6	0000000000000000	00000000	00000000
7	0000000000000000	00000000	00000000
8	0000000000000000	00000000	00000000
9	0000000000000000	00000000	00000000
10	0000000000000000	00000000	00000000
11	1001100110011001	10000000	00000000
12	0001100000011000	01000000	00000000
13	1001101110011011	00100000	00100000
14	0001101000011010	00010000	00010000
15	1001110110011101	00001000	00001000
16	0001110000011100	00000100	00000100
17	1001111110011111	00000010	00001010
18	0001111000011110	00000001	00000101
19	1001000110010001	10000000	00000000
20	0001000000010000	01000000	00000000
21	1001001110010011	00100000	00100000
22	0001001000010010	00010000	00010000
23	1001010110010101	00001000	00001000
24	0001010000010100	00000100	00000100
25	1001011110010111	00000010	00001010
26	0001011000010110	00000001	00000101
27	1000100110001001	10000000	00000000
28	0000100000001000	01000000	00000000
29	1000101110001011	00100000	00000000
30	0000101000001010	00010000	00010000
31	1000110110001101	00001000	00001000
32	0000110000001100	00000100	00000100
33	1000111110001111	00000010	00001010
34	0000111000001110	00000001	00000101
35	1000000110000001	10000000	00000000
36	0000000000000000	01000000	00000000
37	1000001110000011	00100000	00000000
38	0000001000000010	00010000	00010000
39	1000010110000101	00001000	00001000
40	0000010000000100	00000100	00000100
41	1000011110000111	00000010	00001010
42	0000011000000110	00000001	00000101
43	1011100110111001	10000000	00000000
44	0011100000111000	01000000	00000000
45	1011101110111011	00100000	00000000
46	0011101000111010	00010000	00010000
47	1011110110111101	00001000	00001000
48	0011110000111100	00000100	00000100
49	1011111110111111	00000010	00001010
50	0011111000111110	00000001	00000101

Fig.6.3 Test pattern truth table

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51	1011000110110001	10000000	00000000
52	0011000000110000	01000000	00000000
53	1011001110110011	00100000	00000000
54	0011001000110010	00010000	00010000
55	1011010110110101	00001000	00001000
56	0011010000110100	00000100	00000100
57	1011011110110111	00000010	00001010
58	0011011000110110	00000001	00000101
59	1010100110101001	10000000	00000000
60	0010100000101000	01000000	00000000
61	1010101110101011	00100000	00000000
62	0010101000101010	00010000	00010000
63	1010110110101101	00001000	00001000
64	0010110000101100	00000100	00000100
65	1010111110101111	00000010	00001010
66	0010111000101110	00000001	00000100
67	1010000110100001	10000000	00000000
68	0010000000100000	01000000	00000000
69	1010001110100011	00100000	00000000
70	0010001000100010	00010000	00010000
71	1010010110100101	00001000	00001000
72	0010010000100100	00000100	00000100
73	1010011110100111	00000010	00001010
74	0010011000100110	00000001	00000101
75	1101100111011001	10000000	00000000
76	0101100001011000	01000000	00000000
77	1101101111011011	00100000	00000000
78	0101101001011010	00010000	00010000
79	1101110111011101	00001000	00001000
80	0101110001011100	00000100	00000100
81	1101111111011111	00000010	00001010
82	0101111001011110	00000001	00000101
83	1101000111010001	10000000	00000000
84	0101000001010000	01000000	00000000
85	1101001111010011	00100000	00000000
86	0101001001010010	00010000	00010000
87	1101010111010101	00001000	00001000
88	0101010001010100	00000100	00000100
89	1101011111010111	00000010	00001010
90	0101011001010110	00000001	00000101
91	0000000000000000	00000000	00000000
92	0000000000000000	00000000	00000000
93	0000000000000000	00000000	00000000
94	0000000000000000	00000000	00000000
95	0000000000000000	00000000	00000000
96	0000000000000000	00000000	00000000
97	0000000000000000	00000000	00000000
98	0000000000000000	00000000	00000000
99	0000000000000000	00000000	00000000
100	0000000000000000	00000000	00000000

END AT 1000

*

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that the yield for each functional part may be determined, as well as the overall yield.

2. All inputs, outputs and product terms must be tested.
3. Adjacent inputs, outputs or product terms should pre=ferably not carry identical signals, as a short circuit between them would not be detectable.
4. The input data should be easily generated by means of simple hardware and the output data easily verifiable.

The original truth table satisfied those requirements. It was generated from the outputs of an eight-bit binary counter and the outputs formed an easily recognizable pattern which could be de=tected by means of an ordinary oscilloscope. However, this table was incorrectly programmed into the array owing to some faults in the original coding form. The actual program is shown in Fig. 6.3. It retains certain of the features described above, but is not easily generated from a counter. It was then decided to rather make use of a mini-computer-based automatic test system to generate the necessary input data and analyse the output data.

6.2 The test system

6.2.1 Hardware

A block diagram of the test system is shown in Fig. 6.4. This system was originally developed for testing a sequential cir=cuit at high clock rates. Data is read from the computer memory into the input buffer memory under program control. It is then read into the device under test (DUT) at a rate determined by an external clock generator. The output of

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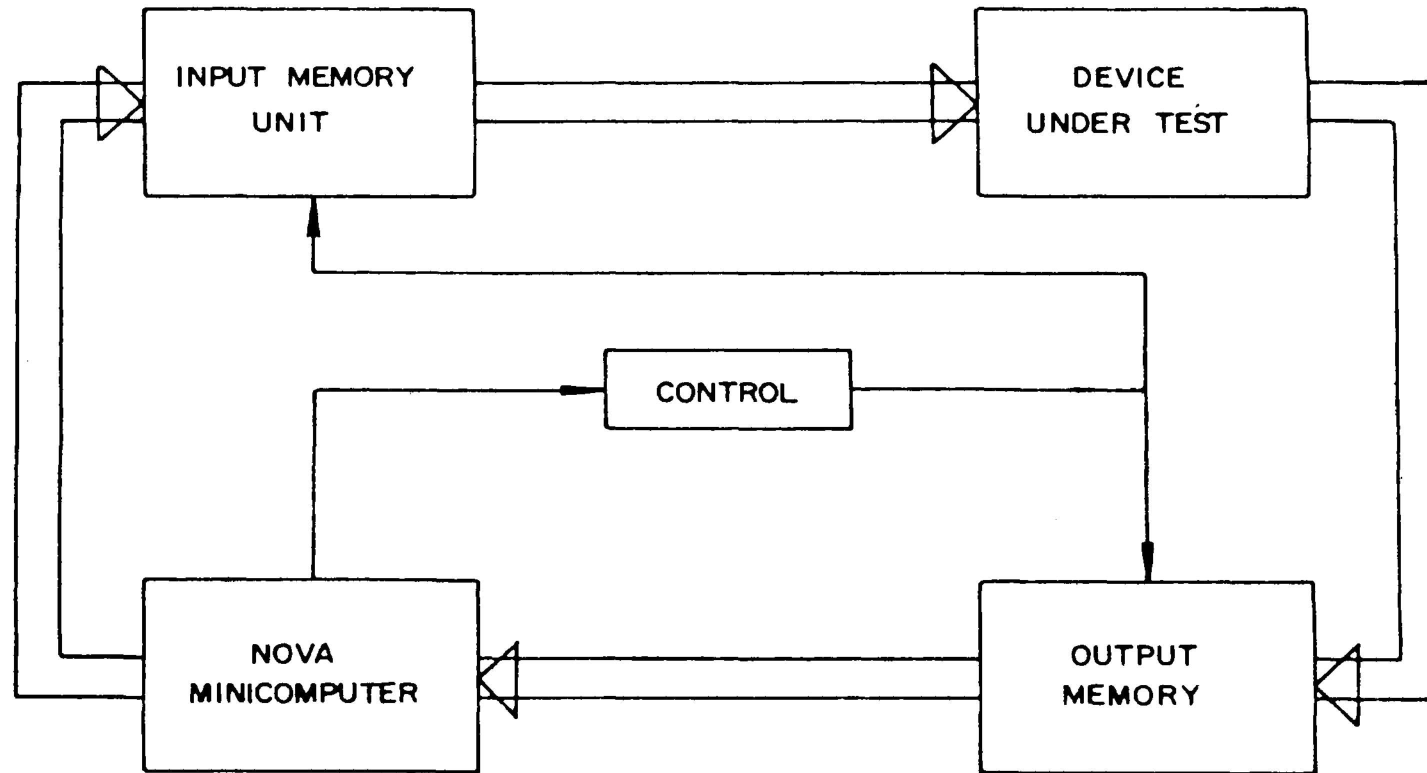

Fig.6.4 Block diagram of test hardware

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the DUT is read into the output buffer memory at the same rate and then back into the computer under program control.

6.2.2 <u>Software</u>

The programs were written in MULTEX BASIC. The first of these was an existing program used to collect data from the devices. This was modified to store the data from a large number of devices on a magnetic disc (PLATEST MB). The second program (PLADATA MB) was written to make a statistical analysis of this data based on the flow chart in Fig. 6.6. This program is designed to detect the fol= lowing.

1. Fully functioning devices. The output data (E) is compared line-for-line with a stored matrix of correct data (D). If all 80 lines are iden= tical, the device is considered to be fully func= tioning. The number of the circuit on the wafer is recorded and used later to relocate working devices for packaging.

2. Defective product terms. Before test 1 is begun a 1 x 80 element matrix H is loaded with zeros. As test 1 is made, defective lines in the output table (corresponding to defective product terms) may be detected. If such a term is found in line x of the output table, the x-th element of matrix H is incremented. After a whole wafer is tested

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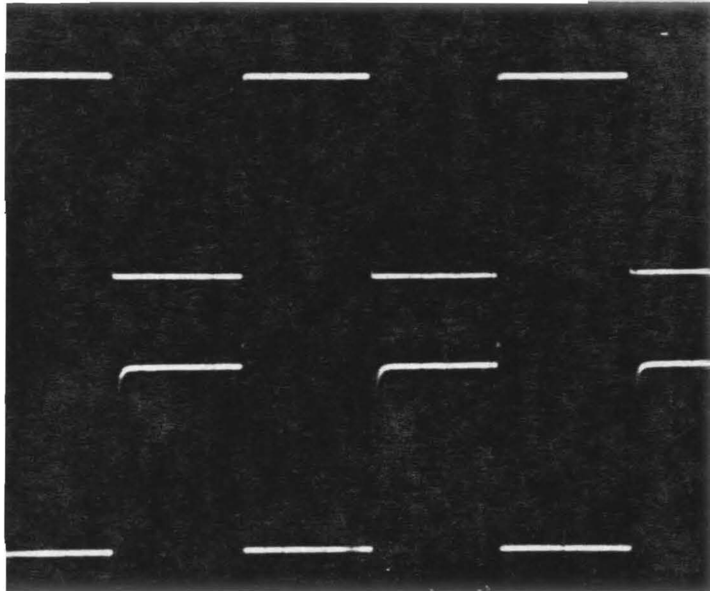

Fig.6.5 Upper trace: I_1-I_{16}

Lower trace: Q_7

Vertical scale: 2V/cm

Horizontal scale: 20μs/cm

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(111 circuits) matrix M =ΣH contains a record of the number of times each product term failed the test out of a possible total of 111.

3. Defective output lines. This part of the pro= gram is designed to detect faulty output lines whose state does not change, i.e. they are stuck either high or low. A 1 x 8 element matrix F is loaded with 11111111. A bit-for-bit compa= rison is then made between the first element of the output data matrix E and each successive ele= ment. As soon as a change ($1 \rightarrow 0$ or $0 \rightarrow 1$) is de= tected in a specific bit position, the corresponding element of F is set to 0.

4. Defective input lines. If a line in the output data table is defective it does not necessarily mean a defective product term - it may be that one or more input bits are defective and so do not address the product term line correctly. An attempt was made in the program to differentiate between defective inputs and defective product terms, by correlating the faulty product term matrix H with each bit of the input-data matrix J. For example, if H [001100---] and J_x = [001100---] it is a reasonable supposition that the fault in h_3 and h_4 is caused by input bit J_x which is

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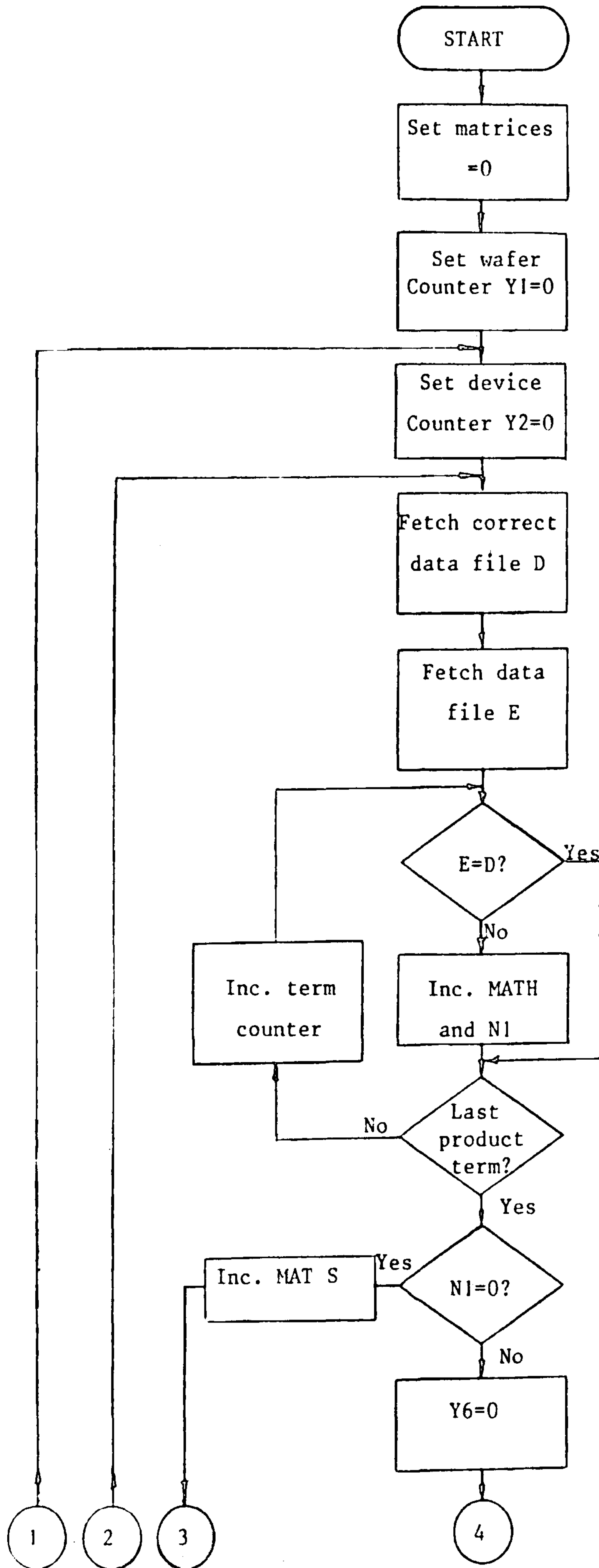

Fig. 6.6: Flow diagram

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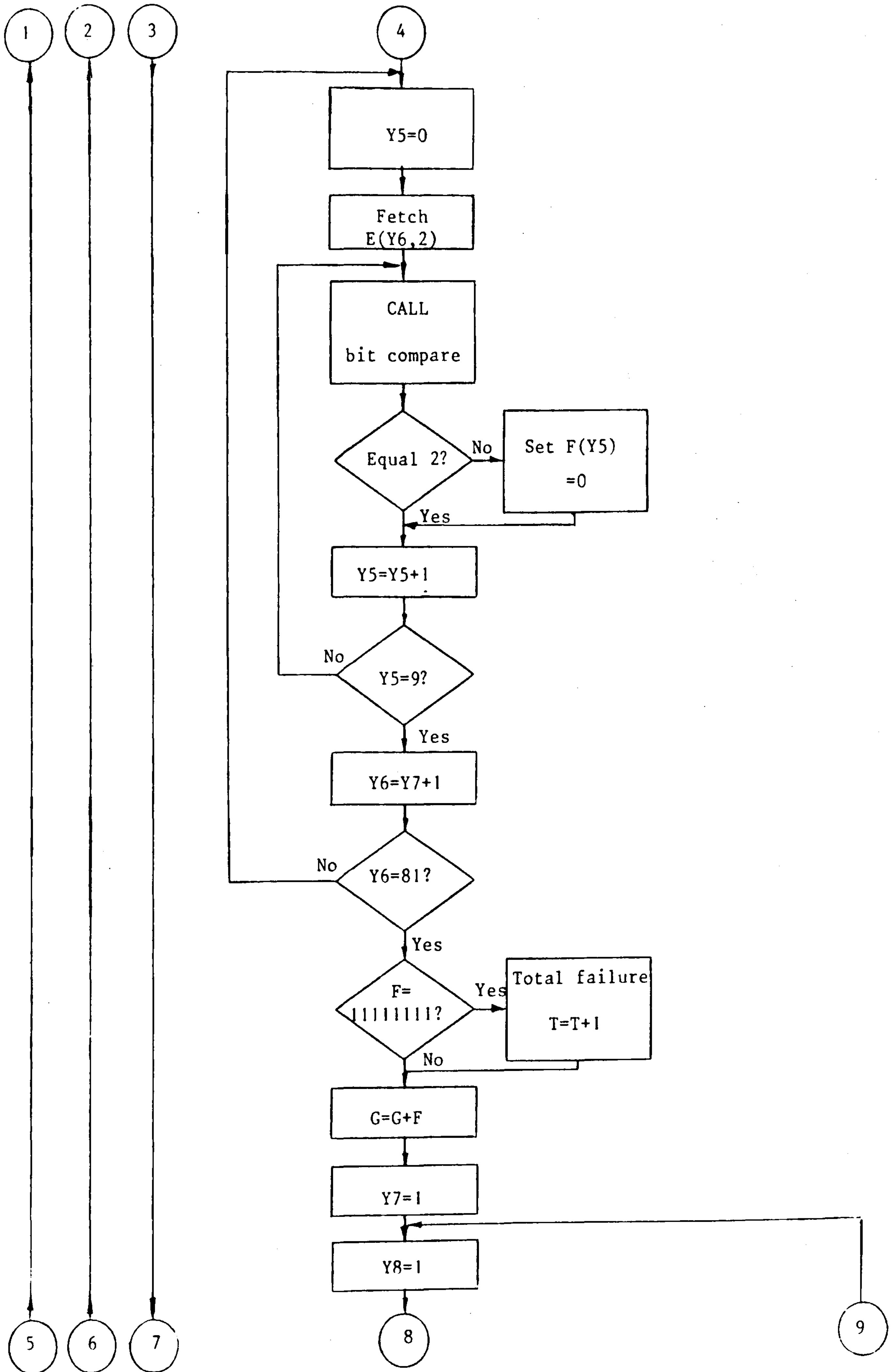

Fig. 6.6: continued

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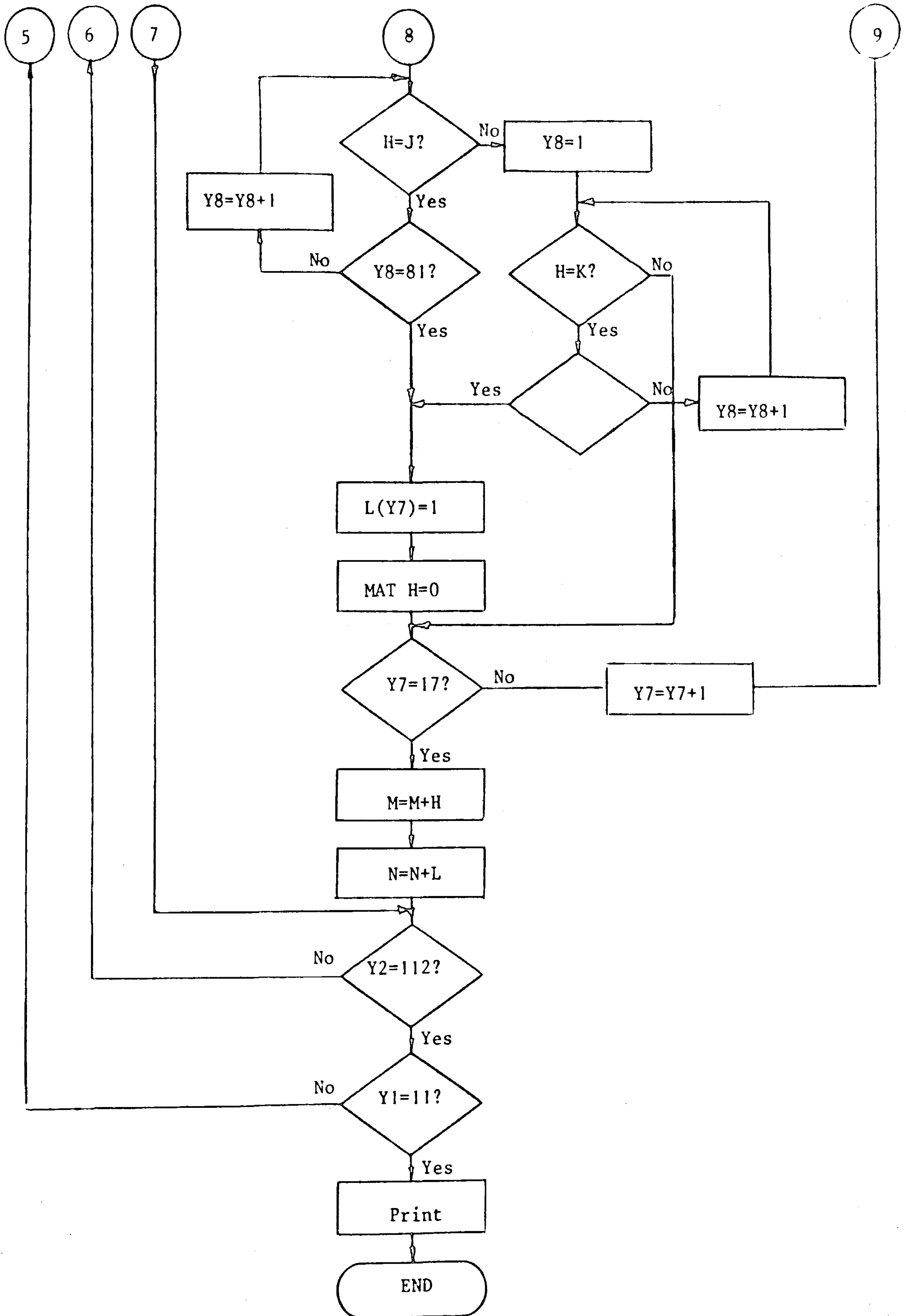

Fig. 6.6: continued

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stuck low. Similarly if J_x = [110011---], the fault is probably caused by J_x being stuck high. To check for these two conditions, the matrix H was compared for equality with each of the 16 x 80 bit columns in J, and also with a matrix K, which consists of the one's complements of each bit of J. If equality is found in either case the product term faults are con= sidered to actually be input faults, the H matrix is reset to zero and bit x of a 16-bit input fault matrix L is incremented.

The information described above has two uses. Firstly, useful information concerning the yield/area relationship may be obtained because each fault is now associated with a spe= cific part of the circuit having a known area. The yield of each part of the circuit as well as the yield of the whole cir= cuit may then be calculated, giving several measured points on the yield/area curve. Further by analysing the fault distribu= tion on several wafers, possible systematic faults (caused by design or layout errors) may be detected.

6.3 Results

6.3.1 Logical tests

A batch of 11 two-inch diameter wafers, each containing 112 circuits, was produced by the IC facility using the process modifications described in Chapter 5. Fig. 6.2 shows a com= pletely processed circuit. These circuits were tested in

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wafer-form at a total current per circuit of 30 mA using 8k2 pull-up resistors at the outputs. This test was in=tended only to detect logical faults and so a low clock rate (1 kHz) was used.

The results of this test were disappointing. A large number of the devices showed evidence of the characteristic 'sliding 1' output data format shown in Fig. 6.3, but in al=most all cases there were several faults present. No single fully working circuit was found. All the faults were iden=tified by the analysis program as product-term faults, i.e. no input fault correlation was obtained. The yield of fully working product-terms was only 0,87%. The program was also not able to detect any output bits stuck high or low. A visual inspection of the output data of several devices was then made. It was observed that often a number of faults were simultaneously present and this would explain the pro=gram's inability to classify the faults correctly. The faults may be roughly categorized as follows:

1. Catastrophic failures. In large areas of certain wafers, all outputs are =1. This is probably due to β_u of these devices being <1 as a result of epi=taxial layer thickness variations (see Chapter 5.2).
2. Random faults. A high occurrence of apparently random faults such as stuck outputs, stuck product-terms and inoperative input bits were also observed. Apart

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from the usual yield-reducing mechanisms in a bipolar circuit such as epitaxial-layer spikes and crystal faults, there is an additional fault-source which may be contributing to the low yield in this case. This is the widespread use of aluminium con= ductors crossing over n^+ emitter diffusion. The oxide layer over the n^+ diffused regions is only 300 nm thick and the possibility of pin holes arising in this oxide layer cannot be ruled out.

3. Systematic failures. It was observed that in many circuits output Q_8 was stuck high. On examining the layout of the circuit on the CALMA system it was found that one of the layout rules, namely the mini= mum clearance of base diffusion surrounding emitter diffusion, had been exceeded on an underpass connecting the Q_8 output interface to the OR-array. It is highly likely that this fault is responsible for the Q_8 out= put being defective.

6.3.2 Electrical tests

Ten chips, each having at least one working output were encap= sulated in 40-pin ceramic packages for the electrical tests. The following measurements were made:

1. Speed power relationship. The relationship between supply current I_t and maximum operating frequency f_{max} was measured on the samples from 300 μA to the point at which the circuits would no longer function. The

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averaged results are listed in Table VIII and are also depicted in Fig. 6.7, together with the theo= retical curve orginally presented in Fig. 5.27. The theoretical results agree with the measured values to within 35%, a good agreement in view of the large number of simplifying assumptions implicit in the calculations.

2. Maximum operating current. This is somewhat better than the calculated worst-case value, and averages at 133 mA. The maximum current which would probably be used in practice is 100 mA, given a maximum operating frequency of 1,75 MHz.

3. Minimum operating current. The minimum supply cur= rent necessary to sink 2 mA is 24,8 mA, agreeing almost exactly with the calculated value of 25 mA.

4. Injector series resistance. This amounts to approxi= mately 10 Ω and will add 16 mW to the total chip con= sumption at 1 MHz (40 mA).

5. Input and output voltage levels. The omission of the buried layer from the input and output transistors proved a successful method of maintaining high break= down voltages. The breakdown voltages were:

$$BV_{IN} = 22 \text{ V and}$$

$$BV_{OUT} = 52 \text{ V.}$$

The output saturation voltage was increased from 170 mV (typical) to 550 mV at 2 mA, implying that the increased collector series resistance is approximately 190 Ω.

Input and output waveforms are depicted in Fig. 6.5.

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I_t (A)	f_{max} (Hz) measured	f_{max} (Hz) calculated	% Error
10^{-1}	$1,75 \times 10^6$	$2,4 \times 10^6$	+37
3×10^{-2}	$7,05 \times 10^5$	$7,6 \times 10^5$	+42
10^{-2}	$2,9 \times 10^5$	$2,6 \times 10^5$	+8
3×10^{-3}	$1,05 \times 10^5$	$8,2 \times 10^4$	-22
10^3	$3,8 \times 10^4$	$2,8 \times 10^4$	-26
3×10^{-4}	$1,05 \times 10^4$	9×10^3	-14

TABLE VIII

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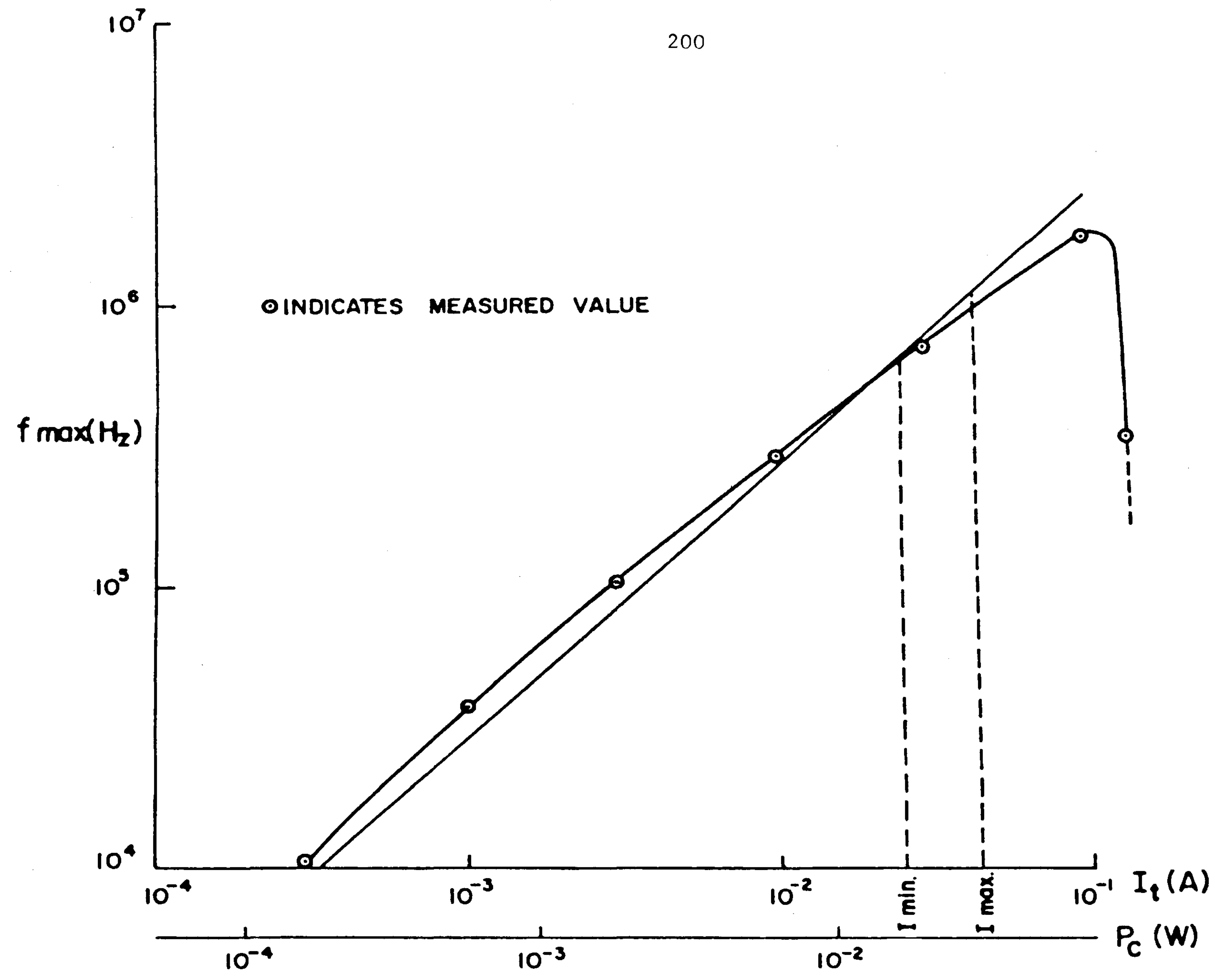

Fig.6.7 f_{max} vs I_t & P_c

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CHAPTER 7

7. CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

A mask-programmable PLA has been designed and manufactured using integrated injection logic produced with a modified standard bi= polar process. Electrical measurements on a small number of samples show that the device meets all the original electrical specifications. Operation at a clock rate of 1 MHz is possible, at a total chip dissipation of 44 mW for a circuit containing 800 equivalent four-collector gates, 16 input interfaces and 8 output interfaces. Good agreement between theoretical and measured speed-power performance has been obtained. Input and output inter= faces function correctly and are TTL and CMOS compatible.

The yield of fully functioning circuits was zero. Apart from a mask layout error and the usual faults common to any bipolar process (e.g. epitaxial layer spikes and crystal defects), a large number of faults were caused by the sensitivity of the upward current gain β_u to variations in epitaxial layer thickness.

7.2 Recommendations

7.2.1 Process changes

It is obvious that drastic changes to the process must be considered to stabilize the current gain of the devices. The large β_u variation is caused by a poorly controlled emitter doping level, which varies between the background concentration (6,5 x 10 cm^{-3}) and a much higher value de= pending on the degree of buried layer out-diffusion. To

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stabilize this concentration at a high value it is pro= posed that the epitaxial layer concentration be increased as much as is practically feasible with the given equip= ment (about 2,6 x 10^{16} cm^{-3}). This will increase the mini= mum current gain by a factor of four. Increasing the no= minal epitaxial thickness will help to prevent punch-through of the emitter to the collector and will ensure a higher breakdown voltage. This has been attempted by other researchers using devices of similar geometry[45], and a good trade-off between β_u and BV_{CEO} was achieved. These modi= fications should have little effect on the performance of the device otherwise, except that α_p of the lateral pnp transistor will be slightly degraded. This will cause a corresponding increase in the power-delay product of the gate. No radical design changes should therefore be neces= sary.

7.2.2 Design changes

The electrical specifications having been met, no design changes are necessary per se. Certain options for changing the capability of the circuit do exist though, and the fol= lowing may be worthy of consideration:

1. If a fixed 5 V supply may be tolerated, the open-collector output interfaces may be replaced by push-pull types. This would save an external com= ponent count. The size of the output transistors could be reduced with a corresponding reduction in junction capacitance. Yield would probably be im= proved, as the present interface requires that $\beta_u \geq 3,6$ for correct operation.

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2. If a breakdown voltage in excess of 7 V could be guaranteed by the process alterations described above, a buried layer could be used in the output transistors, reducing their series collector re= sistance and making a greater fan-out possible.
3. Flip-flops could be added in the unused areas on the chip, enabling a complete sequential system to be realized.
4. Injector contact windows should also be made pro= grammable to enable the power consumption to be kept to a minimum.

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APPENDIX A1

Plessey process 1 layout rules

Clearance	Minimum dimension
Buried n^+ to isolation clearance	24 µm
Isolation diffusion width	12 µm
Base diffusion to base diffusion clearance	8 µm
Base diffusion to isolation diffusion clearance	20 µm
Base to collector contact distance	12 µm
Margin of base diffusion surrounding a contact window	4 µm
Emitter diffusion to emitter diffusion clearance	8 µm
Emitter diffusion to isolation diffusion clearance	20 µm
Margin of emitter diffusion surrounding a contact window	4 µm
Margin of base diffusion surrounding an amitter	6 µm
Size of contact window	8 µm x 8 µm
Aluminium width	10 µm
Aluminium spacing (short runs of < 100 µm)	8 µm
(long runs)	10 µm
Aluminium overlap around contact windows	4 µm
Bonding pad/conductor clearance	32 µm
Bonding pad/bonding pad clearance	48 µm

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APPENDIX A2

Experimental I^2L circuits designed by other researchers in the Solid State Electronics Division

Considerable use has been made in this thesis of results obtained by other researchers at the Solid State Electronics Division. These results were obtained using the following test chips:

A2.1: MCL1 (designed by M. Crooke and R.F. Greyvenstein).

A2.2: MCL2 (designed by M. Crooke and R.F. Greyvenstein).

A2.3: MCL3 (designed by N. Kirschner).

For the sake of completeness these devices are illustrated on the following three pages.

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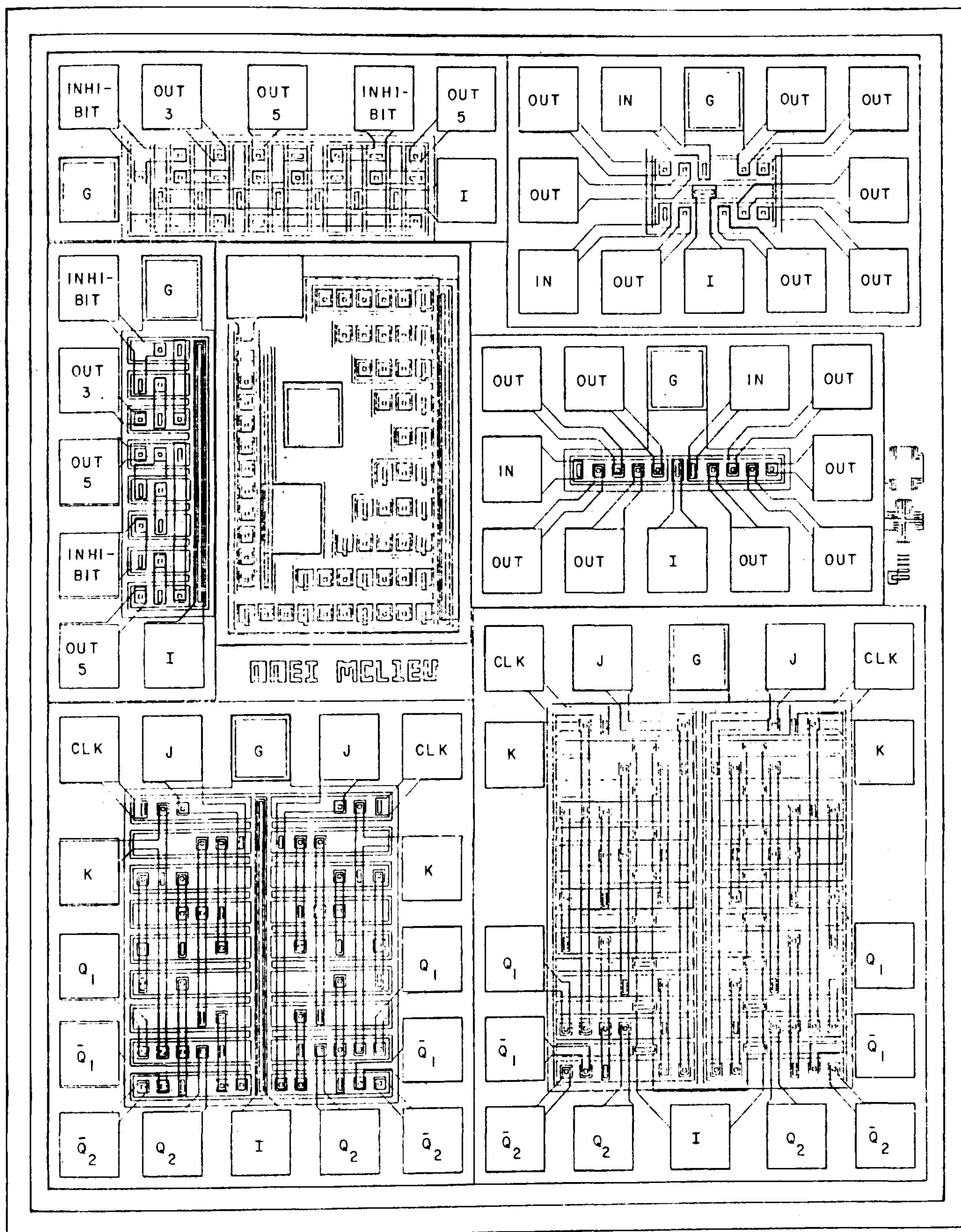

Fig. A.1 : MCL1 test chip

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A2.1

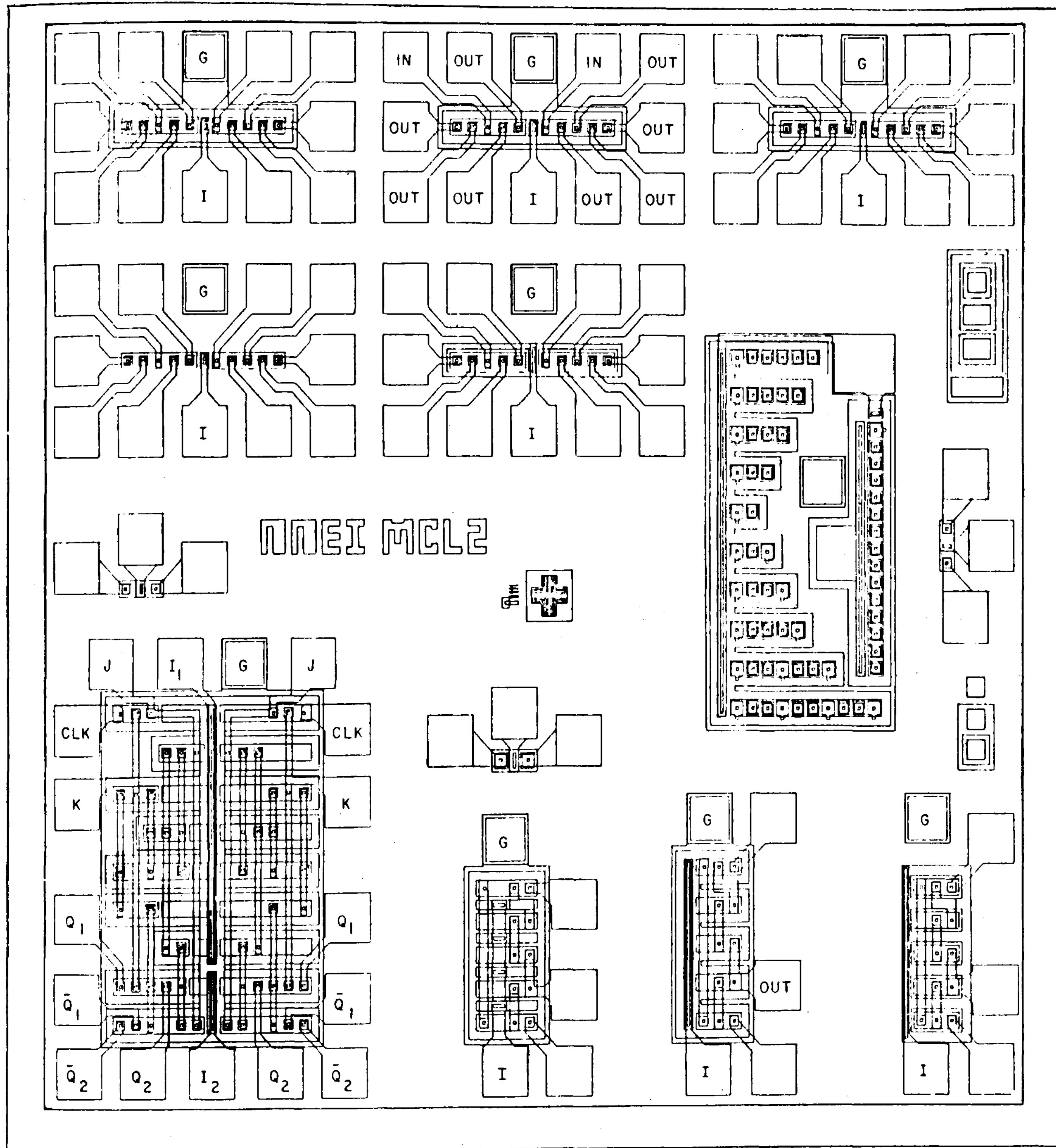

Fig. A.2 : MCL2 test chip

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A2.3

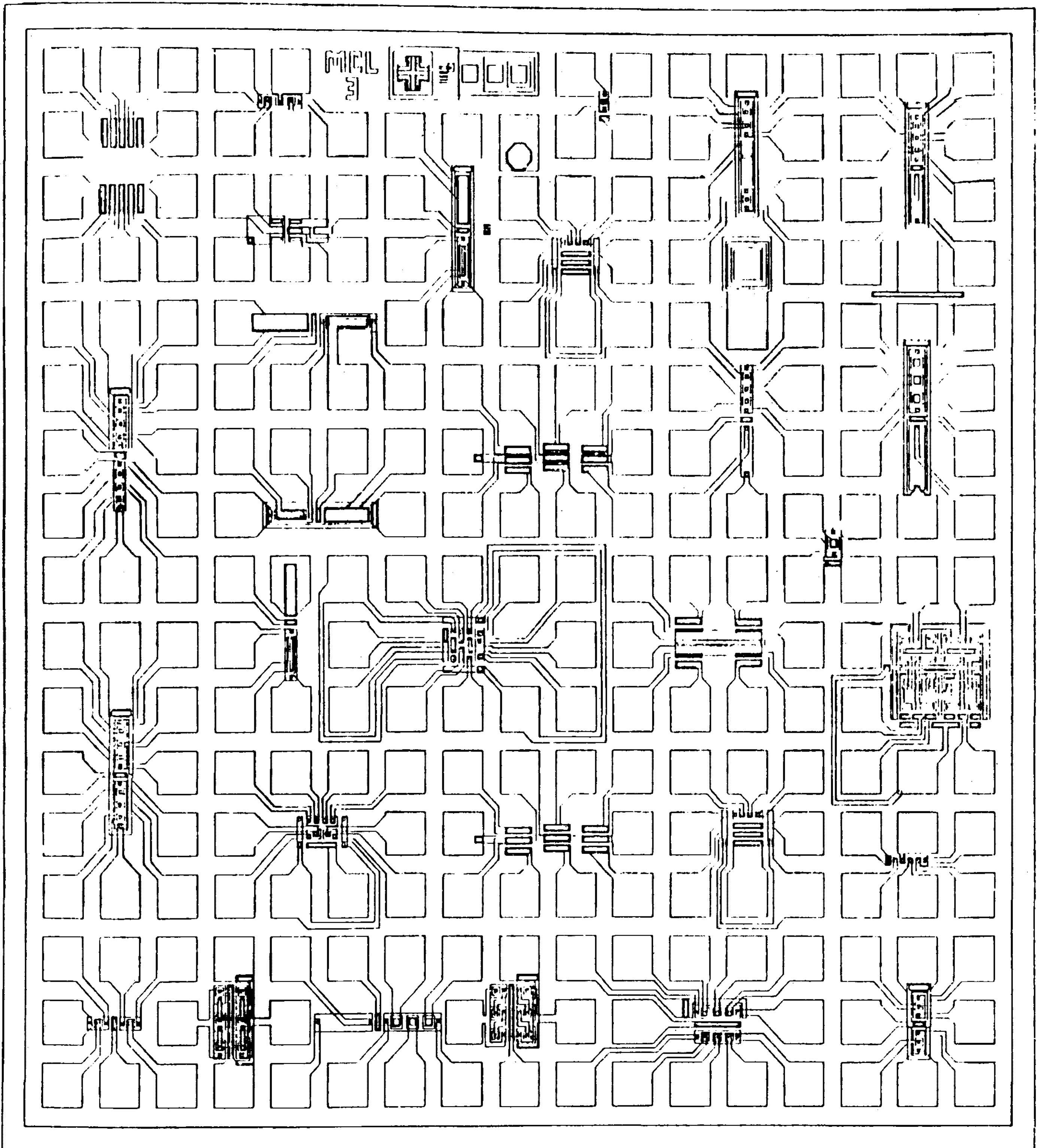

Fig. A.3 : MCL3 test chip

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APPENDIX A3

Experimental I^2L circuits designed by the author as part of this project

Two experimental chips were designed by the author to obtain necessary information about device performance. The results were used to confirm theoretical analyses in Chapter 5. The following structures were incor= porated on these chips:

A3.1: MCL4 (see Fig. A4)

1 : A pinch resistor.

2 → 7 : Normal geometry gates with pnp base widths of 6, 8, 10, 12, 14 and 16 μm.

8 : A MOS-capacitor for measuring surface recombination velocity.

9 → 11 : Minimum geometry gates with isolation widths of 4, 8 and 12 μm.

12 : A test transistor.

A3.2: MCL5 (see Fig. A5)

1 : An input interface.

2 → 4 : Non-isolated gates with isolation widths of 8, 12 and 16 μm.

5 → 7 : Isolated gates with isolation widths of 8, 12 and 16 μm.

8 : Nine transistors with various emitter/collector area ratios.

9 → 11 : Three substrate pnp transistors with different emitter areas.

12 → 17 : Eleven-stage ring oscillators with various geometries and isolation widths.

18 : A D-type flip-flop.

19 : A 96-collector structure with an n^+ underpass.

20 : An output interface.

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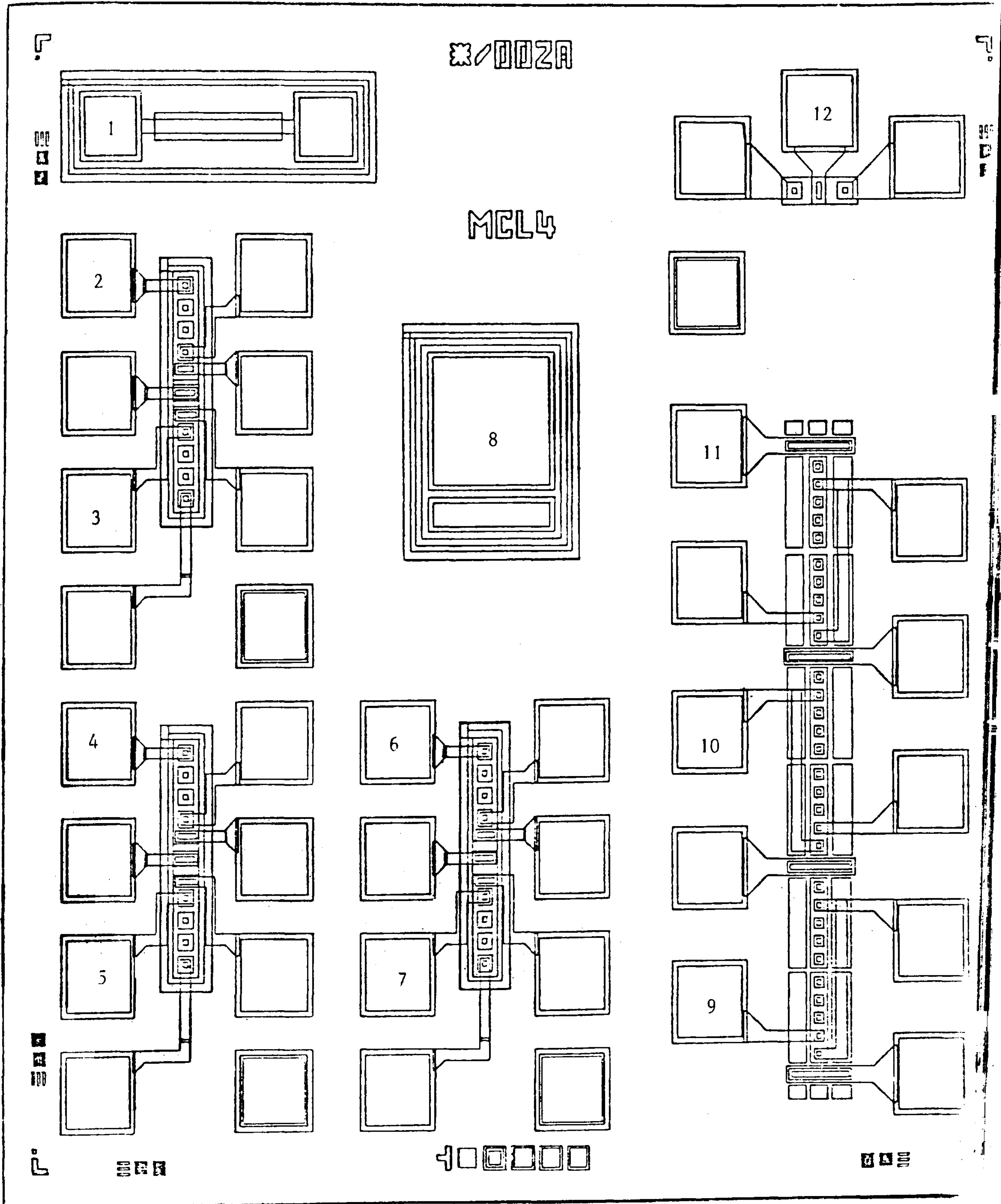

Fig. A.4 : MCL4 test chip

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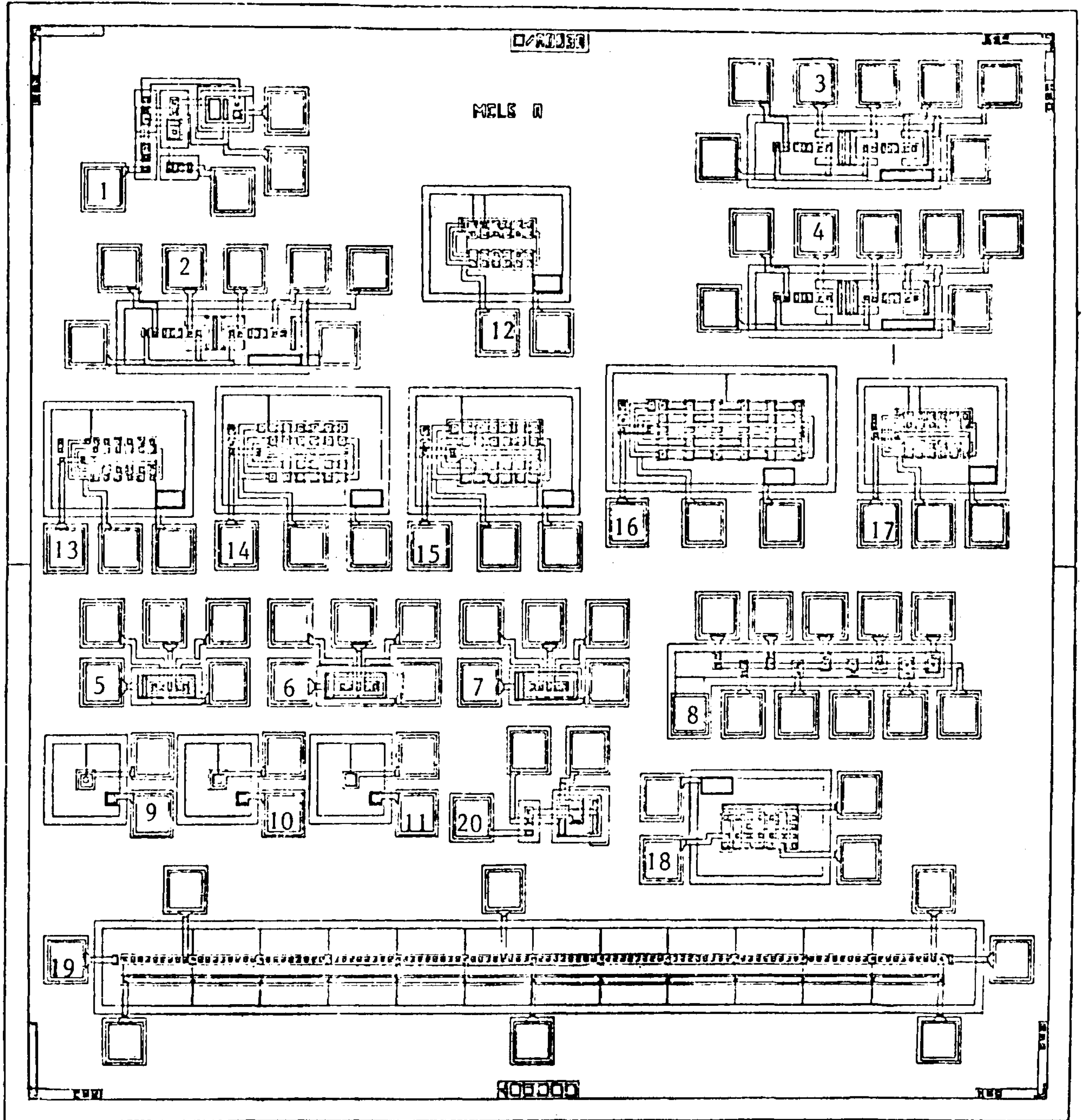

Fig. A.5 : MCL5 test chip

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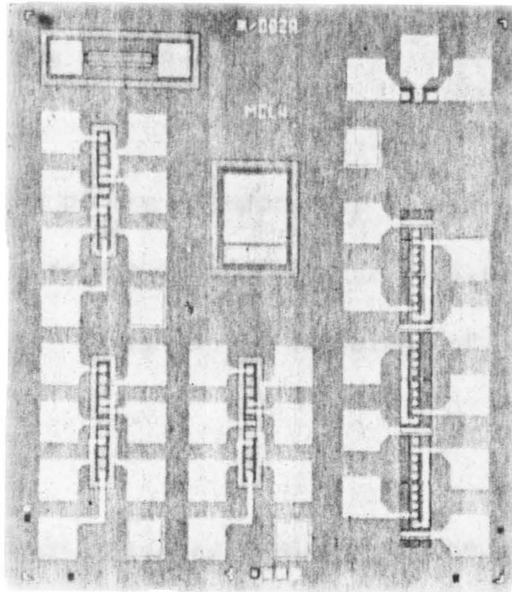

Fig. A6 MCL 4

Fig. A7 MCL 5

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APPENDIX A4

Layout of the AND-arrays and OR-arrays

A4.1 : The AND-array

Fig. A6 shows a section of the AND-array as it was finally laid out. Two eight-collector gates are shown together with two n^+ underpasses connected to the bases. These lie in an island of p-base diffusion between the gates.

A4.2 : The OR-array

Fig. A7 shows four eight-collector gates of the OR-array. The inputs are connected to the bottom of each gate. The injectors are placed between the cells injecting current in both directions. The injectors are designed to inject a current of 2 I_{inj} into each cell.

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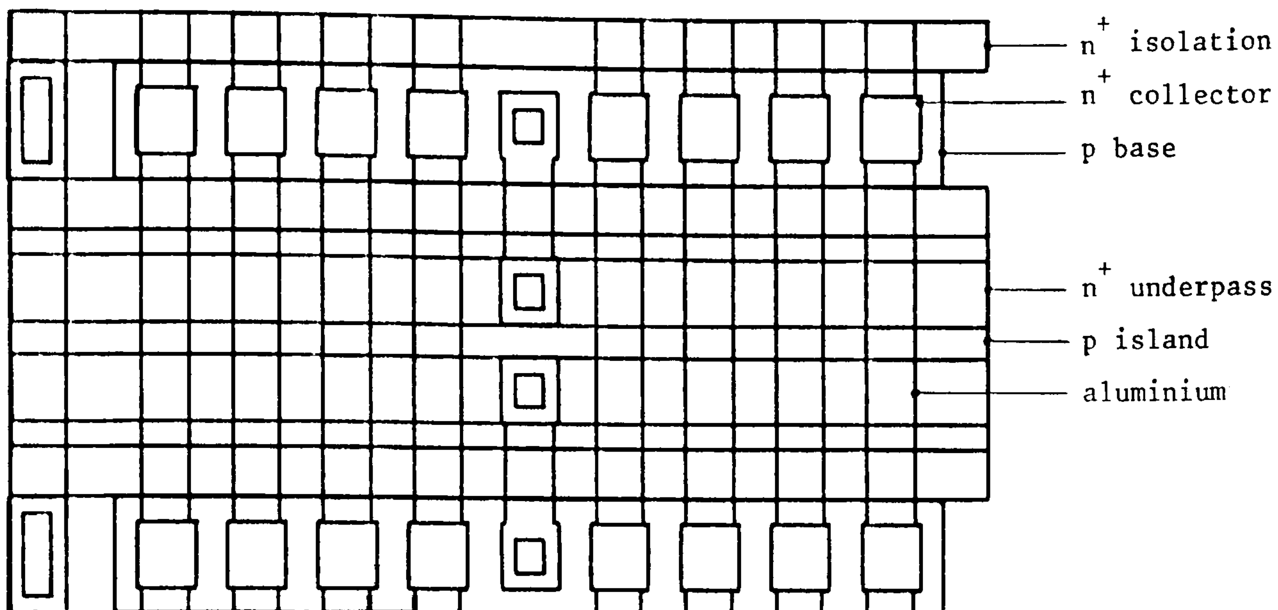

Fig. A6 : A section of the AND-array (1 mm = 2 μm)

n^+ collector
n^+ isolation
aluminium
p base
p injector

Fig. A7 : A section of the OR-array (1 mm = 2 μm)

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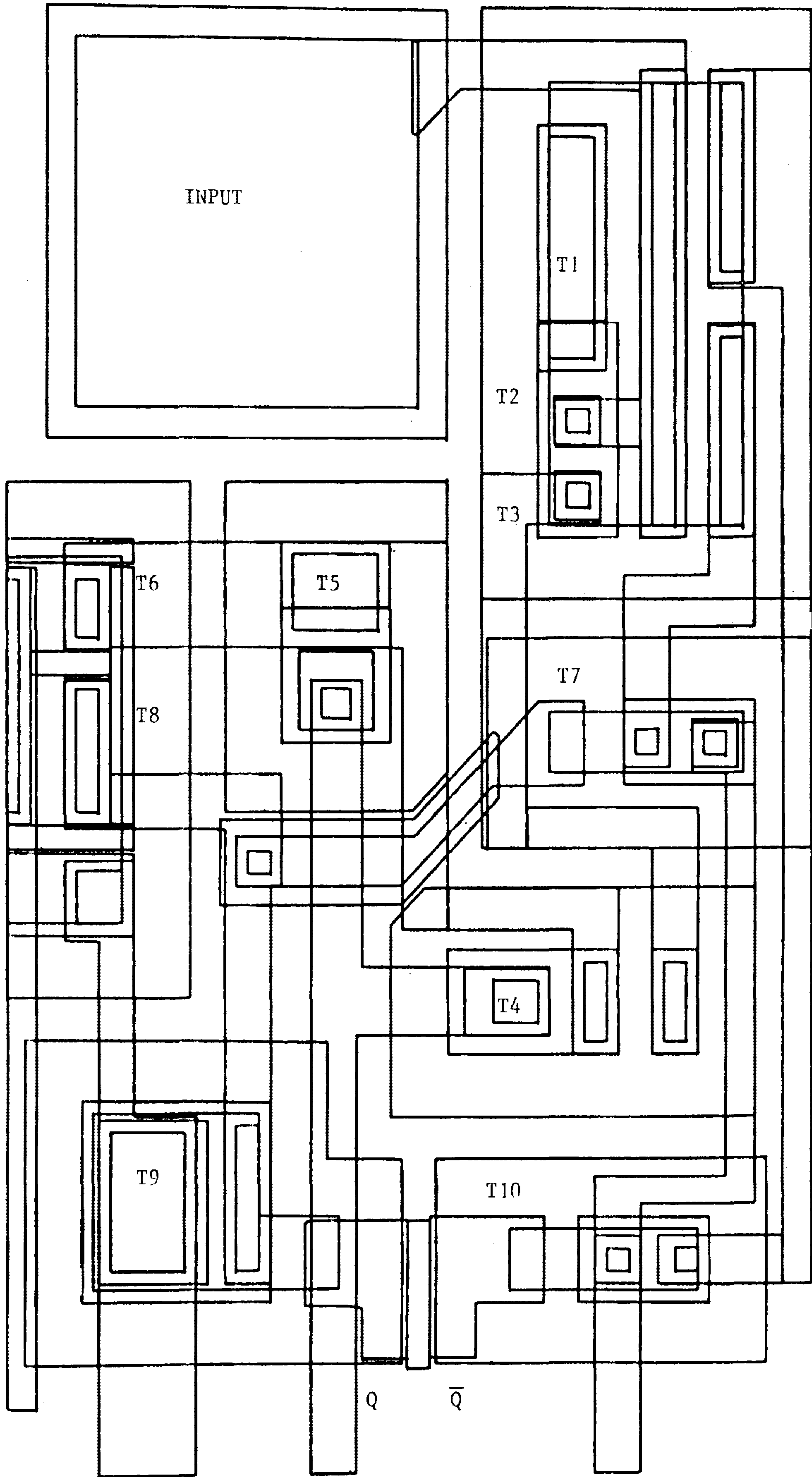

Fig. A8: Input interface (1 mm = 2 µm)

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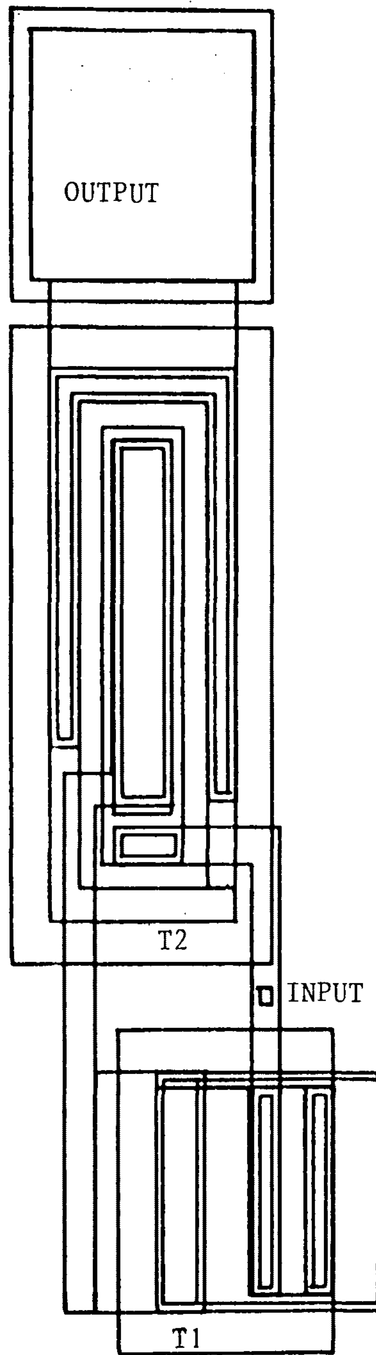

Fig. A9 : Output interface (1 mm = 4 μm)

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APPENDIX A6

Test hardware and software

A6.1 : Hardware used for measuring gate parameters

The equipment used for measuring the static and dynamic parameters of gates has been thoroughly documented elsewhere[45]. Briefly, the measurements were made as follows:

1. Static parameters were measured on a semi-automatic basis. Using an apitaxial current source, two logarithmic current-to-voltage converters and an analog subtraction circuit, a voltage proportional to β_u or α_p may be generated. This is used to make a direct plot of β_u or α_p vs I_c on an X-Y plot=ter, using logarithmic graph paper. Current gain may be plotted over an 8-decade current range from 100 pA to 10 mA.
2. Dynamic parameters such as gate delay were measured using the exponential current source and a high-input impedance active probe. This probe places negligible resistive or capacitive loading on the device under test, which is essen=tial for accurate measurements at low currents. The probe was also used to plot V_{be} vs I_c curves.

A6.2: Software used for functional study

A listing of the test program appears on the following pages.

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```
0010 REM ********************************************************
0020 REM
0030 REM TITEL:  FLADATA.MB
0040 REM
0050 REM BESKRYWING:  ANALISEER TOETSRESULTATE VAN FLA BAAN
0060 REM
0070 REM
0080 REM
0090 REM ********************************************************
0100 PRINT
0110 PRINT
0120 REM
0130 LET B1=SYS(0)
0140 PRINT "TYD PROGRAM BEGIN = ";B1/3600
0150 REM M - MATRIKS VAN FOUTIEWE PRODUKTERME
0160 REM N - MATRIKS VAN FOUTIEWE INSETLYNE
0170 REM S - MATRIKS VAN WERKENDE STROOMBANE
0180 REM G - MATRIKS VAN FOUTIEWE KOLOMME
0190 REM F1$ - NAAM VAN DATA LEER OP SKYF
0200 LET Y1=1
0210 DIM M[1,80],N[1,16]
0220 DIM S[1,112],G[1,8]
0230 DIM F1$[20],F2$[420],F3$[20],F4$[40]
0240 DIM E[100,2],D[100,2]
0250 DIM H[1,80],F[1,6]
0260 MAT M=ZER
0270 MAT N=ZER
0280 MAT S=ZER
0290 MAT G=ZER
0300 LET T=0
0310 REM -----------------------------------------
0320 REM             TOETS PRODUKTERME
0330 REM
0340 REM
0350 REM Y3 = WYSER NA ELEMENTE IN DATA-MATRIKS
0360 REM Y1 = SKYFTELLER     Y2 = STROOMBAANTELLER
0370 REM
0380 REM -----------------------------------------
0390 LET N1=0
0400 REM *** STEL BEGIN TOESTANDE OP
0410 LET Y2=1
0420 REM *** KRY DATA-LEER VAN SKYF
0430 GOSUB 1610
0440 PRINT F1$
0450 REM *** Y3 = 10 IS DIE EERSTE DATA ELEMENT
0460 LET Y3=11
0470 MAT H=ZER
0480 BIAND,E[Y3,2],15,E[Y3,2]
0490 BIAND,D[Y3,2],15,D[Y3,2]
```

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```
0580 REM
0590 IF E[Y3,2]=D[Y3,2] THEN GOTO 0620
0600 LET H[1,Y3-10]=H[1,Y3-10]+1
0610 LET N1=N1+1
0620 LET Y3=Y3+1
0630 IF Y3=91 THEN GOTO 0650
0640 GOTO 0590
0650 IF N1><0 THEN GOTO 0680
0660 LET S[1,(Y2+2)/3]=S[1,(Y2+2)/3]+1
0670 GOTO 1560
0680 GOTO 0690
0690 REM -----------------------------------------------
0700 REM
0710 REM       TOETS VIR FOUTIEWE UITGANGE
0720 REM
0730 REM
0740 REM  Y5 = UITGANGE      Y6 = WYSER NA PRODUKTERME
0750 REM
0760 REM -----------------------------------------------
0770 MAT F=ZER
0780 REM *** STEL BEGIN TOESTANDE OP
0790 LET Y6=11
0800 LET Y5=1
0810 REM *** VERGELYK AL DIE BISSE
0820 LET P4=0
0830 LET P3=8
0840 BITCOMP,E[11,2],E[Y6,2],P3,P4
0850 IF P4=1 THEN GOTO 0870
0860 LET F[1,Y5]=0
0870 LET Y5=Y5+1
0880 IF Y5=9 THEN GOTO 0910
0890 LET P3=P3/2
0900 GOTO 0840
0910 LET Y6=Y6+1
0920 IF Y6=91 THEN GOTO 0940
0930 GOTO 0800
0940 REM *** TOETS OF MATRIKS F =(11111111)
0950 LET I=1
0960 IF F[1,I]><1 THEN GOTO 1000
0970 LET I=I+1
0980 IF I=9 THEN GOTO 1010
0990 GOTO 0960
1000 LET T=T+1
1010 MAT G=G+F
1110 REM ---------------------------------------------------
1120 REM
1130 REM              TOETS VIR FOUTIEWE INSETLYNE
1140 REM
1150 REM ---------------------------------------------------
1160 DIM J[100,2],K[100,2]
1170 DIM F5$[20],F6$[20]
```

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```
1180 DIM L[1,16]
1190 MAT A=ZER[1,80]
1200 LET F5$="PLA3.T"
1210 LET F6$="PLA3C.T"
1220 OPEN FILE[0,3],F5$
1230 MAT READ FILE[0],J
1240 CLOSE FILE[0]
1250 OPEN FILE[1,3],F6$
1260 MAT READ FILE[1],K
1270 CLOSE FILE[1]
1280 MAT A=H
1290 MAT A=(32768)*A
1300 REM *** Y7 = WYSER NA BISSE IN DATA-WOORD
1310 LET Y7=1
1320 REM *** Y8 = INSET DATA-WOORD WYSER
1330 LET Y8=1
1340 LET P3=32768
1350 LET P4=0
1360 BITCOMP,A[1,Y8],J[Y8,2],P3,P4
1370 IF P4=0 THEN GOTO 1410
1380 LET Y8=Y8+1
1390 IF Y8=81 THEN GOTO 1460
1400 GOTO 1360
1410 BITCOMP,A[1,Y8],K[Y8,2],P3,P4
1420 IF P4=0 THEN GOTO 1480
1430 LET Y8=Y8+1
1440 IF Y8=81 THEN GOTO 1460
1450 GOTO 1410
1460 LET L[1,Y7]=1
1470 MAT H=ZER
1480 LET P3=P3/2
1490 LET Y7=Y7+1
1500 IF Y7=17 THEN GOTO 1520
1510 GOTO 1360
1520 REM
1530 MAT M=M+H
1540 REM
1550 MAT N=N+L
1560 LET Y2=Y2+3
1570 IF Y2=334 THEN GOTO 2210
1580 GOTO 0420
1590 PRINT "------------------------------------------------"
1600 REM
1610 REM *** F2$ - STROOMBAAN AANWYSER
1620 REM
1630 PRINT "------------------------------------------------"
1640 FEM
1650 LET F2$[1,30]="000001002003004005006007008009"
1660 LET F2$[31,60]="010011012013014015016017018019"
1670 LET F2$[61,90]="020021022023024025026027028029"
```


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```
1680 LET F2$[91,120]="030031032033034035036037038039"
1690 LET F2$[121,150]="040041042043044045046047048049"
1700 LET F2$[151,180]="050051052053054055056057058059"
1710 LET F2$[181,210]="060061062063064065066067068069"
1720 LET F2$[211,240]="070071072073074075076077078079"
1730 LET F2$[241,270]="080081082083084085086087088089"
1740 LET F2$[271,300]="090091092093094095096097098099"
1750 LET F2$[301,330]="100101102103104105106107108109"
1760 LET F2$[331,360]="110111112113114115116117118119"
1770 LET F2$[361,390]="120121122123124125126127128129"
1780 LET F2$[391,420]="130131132133134135136137138139"
1790 REM
1800 REM F4$ - SKYF AANWYSER
1810 LET F4$[1,20]="00010203040506070809"
1820 LET F4$[21,40]="10111213141516171819"
1830 REM
1840 LET F3$="PLAREG.RS"
1850 OPEN FILE[0,3],F3$
1860 MAT READ FILE[0],D
1870 CLOSE FILE[0]
1880 LET F1$[1,3]="PLA"
1890 LET F1$[4,5]=F4$[Y1,Y1+1]
1900 LET F1$[6,6]="D"
1910 LET F1$[7,9]=F2$[Y2,Y2+2]
1920 LET F1$[10,12]=".RS"
1930 DIM Z[200,2]
1940 OPEN FILE[0,3],F1$
1950 MAT READ FILE[0],Z
1960 CLOSE FILE[0]
1970 MAT E=ZER
1980 FOR I=1 TO 100
1990   LET E[I,2]=Z[2*I,2]
2000 NEXT I
2010 RETURN
2020 RETURN
2030 REM *** DES NA BINER
2040 DIM R$[20]
2050 REM
2060 REM
2070 LET P3=0
2080 LET P2=2048
2090 LET P1=A
2100 FOR N1=1 TO 12
2110   BIAND,P1,P2,P3
2120   IF P3=0 THEN GOTO 2150
2130   LET R$[N1,N1]="1"
2140   GOTO 2160
2150   LET R$[N1,N1]="0"
2160   LET P2=(P2/2)
2170 NEXT N1
2180 RETURN
```

*

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```
2190 REM----------------------------------------
2200 REM
2210 REM *** ROETINE OM RESULTATE UIT TE DRUK
2220 REM
2230 REM----------------------------------------
2240 PRINT
2250 PRINT "POSISIE VAN IC:","#WERKENDE BANE:"
2260 FOR I=1 TO 112
2270   LET S1=S[1,I]
2280   PRINT I; TAB(30);S1
2290 NEXT I
2300 PRINT
2310 PRINT "DEFEKTIEWE BANE:";T
2320 PRINT
2330 PRINT
2340 PRINT "UITGANGE WAT HOOG BLY:"
2350 PRINT "------------------------"
2360 PRINT
2370 PRINT "NOMMER","UITGANG"
2380 FOR I=1 TO 8
2390   LET S2=G[1,I]
2400   PRINT I,S2
2410 NEXT I
2420 PRINT
2430 PRINT
2440 PRINT "FOUTIEWE PRODUKTERME:"
2450 PRINT "-----------------------"
2460 PRINT
2470 PRINT "NOMMER","PRODUKTERM"
2480 FOR I=1 TO 80
2490   LET S3=M[1,I]
2500   PRINT I,S3
2510 NEXT I
2520 PRINT
2530 PRINT
2540 PRINT "FOUTIEWE INSETLYNE:"
2550 PRINT "---------------------"
2560 PRINT
2570 PRINT "NOMMER","INSETLYN"
2580 FOR I=1 TO 16
2590   LET S4=N[1,I]
2600   PRINT I,S4
2610 NEXT I
2620 PRINT
2630 LET Y1=Y1+2
2640 IF Y1=23 THEN GOTO 2660
2650 GOTO 0210
2660 REM *** PROGRAMMERINGSTYD
2670 PRINT
2680 PRINT
2690 LET B2=SYS(0)
2700 PRINT "TYD PROGRAM BEGIN = ";B1/3600
2710 PRINT
2720 PRINT "TYD PROGRAM VOLTOOI = ";B2/3600
2730 PRINT
2740 END
```

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```
0010 REM -------------------------------------------------
0020 REM TITEL: PLATEST.MB
0030 REM
0040 REM      REVISIE              DATUM
0050 REM        01               78/09/19
0060 REM
0070 REM -------------------------------------------------
0080 DIM R1$[16],R2$[16],R3$[16],R4$[16],R5$[16],R6$[16]
0090 DIM Z1$[20],Z2$[20],R$[40]
0100 DIM F1$[20]
0110 DIM F2$[420]
0120 LET F2$[1,30]="000001002003004005006007008009"
0130 LET F2$[31,60]="010011012013014015016017018019"
0140 LET F2$[61,90]="020021022023024025026027028029"
0150 LET F2$[91,120]="030031032033034035036037038039"
0160 LET F2$[121,150]="040041042043044045046047048049"
0170 LET F2$[151,180]="050051052053054055056057058059"
0180 LET F2$[181,210]="060061062063064065066067068069"
0190 LET F2$[211,240]="070071072073074075076077078079"
0200 LET F2$[241,270]="080081082083084085086087088089"
0210 LET F2$[271,300]="090091092093094095096097098099"
0220 LET F2$[301,330]="100101102103104105106107108109"
0230 LET F2$[331,360]="110111112113114115116117118119"
0240 LET F2$[361,390]="120121122123124125126127128129"
0250 LET F2$[391,420]="130131132133134135136137138139"
0260 PRINT
0270 GOTO 0340
0280 PRINT "STROOMBAAN NAAM: ";
0290 INPUT Z2$
0300 PRINT "KLOKFREKWENSIE (IN KHZ): ";
0310 INPUT F1
0320 PRINT "TOEVOERSTROOM (IN MA): ";
0330 INPUT I1
0340 PRINT
0345 GOTO 0365
0350 PRINT "RY DIMENSIE VAN TOETS TABEL";
0360 INPUT M
0365 LET M=60
0370 LET M=M+20
0380 DIM D[M,2],R[2*M,2]
0390 PRINT "BEGIN TOETS (1), RESULTATE (2), NUWE WOORD (-1), NUWE TABEL
(-2)"
0400 INPUT Z1
0410 ON Z1+3 THEN GOTO 0650, 0440, 0390, 0910, 1600
0420 GOTO 0390
0430 PRINT
0440 REM ROETINE OM NUWE WOORD IN TE LEES
0450 PRINT "NAAM VAN TOETS-TABEL";
0460 INPUT Z1$
0470 OPEN FILE[0,3],Z1$
0480 MAT READ FILE[0];D
0490 CLOSE FILE[0]
```

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```
0500 PRINT "NOMMER VAN WOORD (9999,1 OM TE EINDIG)";
0510 INPUT K,L
0520 IF K=9999 THEN GOTO 0610
0530 LET A=D[K+10,L]
0540 GOSUB 2190
0550 PRINT "WOORD",K,L,"=",A2
0560 PRINT "NUWE WOORD";
0570 INPUT A
0580 GOSUB 2290
0590 LET D[K+10,L]=A2
0600 GOTO 0500
0610 OPEN FILE[0,1],Z1$
0620 MAT WRITE FILE[0],D
0630 CLOSE FILE[0]
0640 GOTO 0390
0650 REM ROETINE OM NUWE TOETSTABEL IN TE LEES
0660 PRINT
0670 PRINT "NAAM VAN TOETSTABEL";
0680 INPUT Z1$
0690 MAT D=ZER
0700 PRINT "FORMAAT:  D(I,1),D(I,2)   0<=D<=4096"
0710 PRINT
0720 FOR I=11 TO M-10
0730   PRINT I-10,": ";
0740   INPUT A,X
0750   GOSUB 2290
0760   IF A2>4096 THEN GOTO 0830
0770   LET D[I,1]=A2
0780   LET A=X
0790   GOSUB 2290
0800   IF A2>4096 THEN GOTO 0830
0810   LET D[I,2]=A2
0820   GOTO 0850
0830   PRINT "GETAL GROTER AS 12 BISSE - IDIOOT"
0840   GOTO 0730
0850 NEXT I
0860 PRINT
0870 OPEN FILE[0,1],Z1$
0880 MAT WRITE FILE[0],D
0890 CLOSE FILE[0]
0900 GOTO 0390
0910 REM BEGIN TOETS
0920 PRINT "NAAM VAN TOETSTABEL ";
0930 INPUT Z1$
0940 OPEN FILE[0,3],Z1$
0950 MAT READ FILE[0],D
0960 CLOSE FILE[0]
0970 REM HOOF ROETINE
0980 LET F1$[1,3]="PLA"
0990 PRINT " NOMMER VAN SKYF (TWEE SYFERS --)"
1000 INPUT F1$[4,5]
1010 LET F1$[6,6]="0"
```

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```
1020 FOR Y=1 TO 339 STEP 3
1030   LET F1$[7,9]=F2$[Y,Y+2]
1040   LET F1$[10,12]=".RS"
1050   REM HERSTEL TELLER
1060   PRINT
1070   PRINT "TOETS NOU STROOMBAAN",F1$[7,9]
1080   PRINT
1090   LET A=137
1100   GOSUB 2290
1110   BEHEER,A2
1120   FOR I=1 TO M
1130     REM  1E DEEL VAN INSET BUFFER
1140     BEHEER,7
1150     TOETS,D[I,1]
1160     REM  2E DEEL VAN INSET BUFFER
1170     BEHEER,11
1180     TOETS,D[I,2]
1190     PRINT "L";
1200   NEXT I
1210   PRINT
1220   PRINT "KLAAR GELAAI"
1230   REM HERSTEL TELLER
1240   LET A=117
1250   GOSUB 2290
1260   BEHEER,A2
1270   REM TOETS IC
1280   LET A=240
1290   GOSUB 2290
1300   BEHEER,A2
1310   REM VERTRAGINGSLUS
1320   PRINT
1330   PRINT "VERTRAGINGSLUS"
1340   FOR I=1 TO 1000
1350   NEXT I
1360   REM HERSTEL TELLER
1370   LET A=137
1380   GOSUB 2290
1390   BEHEER,A2
1400   LET A=16
1410   GOSUB 2290
1420   BEHEER,A2
1430   NIOS
1440   FOR I=1 TO 2*M-1
1450     REM 1E DEEL VAN UITSET BUFFER
1460     BEHEER,29
1470     REM LEES RESULTATE IN
1480     RESULT,R[I,1]
1490     REM 2E DEEL VAN UITSET BUFFER
1500     BEHEER,14
1510     RESULT,R[I+1,2]
1520     PRINT "R";
1530   NEXT I
```

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```
1540 PRINT
1550 PRINT "LEES RESULTATE"
1560 PRINT
1570 PRINT " TOETS-RESULTATE JA(-1),NEE(0)";
1580 INPUT I2
1590 ON I2+2 THEN GOTO 1600, 1970
1600 PRINT "TOETS-RESULTATE"
1610 LET Q=M-11
1620 PRINT "EERSTE WOORD (>-10), LAASTE WOORD (<";Q;")";
1630 INPUT N,P
1640 IF P>M-10 THEN GOTO 1620
1650 REM R$(12)= WOORD
1660 LET N=N+10
1670 FOR J=N TO P+10
1680   LET A=D[J,1]
1690   GOSUB 2050
1700   LET R1$=R$
1710   LET A=D[J,2]
1720   GOSUB 2050
1730   LET R2$=R$
1740   LET A=R[2*J,1]
1750   GOSUB 2050
1760   LET R3$=R$
1770   LET A=R[2*J,2]
1780   GOSUB 2050
1790   LET R4$=R$
1800   LET A=R[2*J+1,1]
1810   GOSUB 2050
1820   LET R5$=R$
1830   LET A=R[2*J+1,2]
1840   GOSUB 2050
1850   LET R6$=R$
1860   IF J<11 THEN GOTO 1890
1870   IF J>M-10 THEN GOTO 1890
1880   PRINT J-10;
1890   PRINT  TAB(6);"  ";R1$[9,9];"  ";R1$[10,12];" ";
1900   PRINT R2$[1,3];" ";R2$[4,6];"  ";R2$[7,9];" ";R2$[10,12];
1910   PRINT "         ";R4$[5,12]
1920   PRINT  TAB(6);"  ";R1$[9,9];"  ";R1$[10,12];" ";
1930   PRINT R2$[1,3];" ";R2$[4,6];"  ";R2$[7,9];" ";R2$[10,12];
1940   PRINT "         ";R6$[5,12]
1950 NEXT J
1960 PRINT
1970 OPEN FILE[1,1],F1$
1980 MAT WRITE FILE[1],R
1990 CLOSE FILE[1]
```

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2000 PRINT "HERTOETS (-1), NUWE STROOMBAAN (0)";
2010 INPUT I2
2020 ON I2+2 THEN GOTO 1050, 2030
2030 NEXT Y
2040 GOTO 0970
2050 REM DEC NA BIN ROETINE
2060 REM P1=WOORD,P2=MASKER,P3=RESULTAAT
2070 LET P3=0
2080 LET P2=2048
2090 LET P1=A
2100 FOR N1=1 TO 12
2110   BIAND,P1,P2,P3
2120   IF P3=0 THEN GOTO 2150
2130   LET R$[N1,N1]="1"
2140   GOTO 2160
2150   LET R$[N1,N1]="0"
2160   LET P2=(P2/2)
2170 NEXT N1
2180 RETURN
2190 REM DEC NA OCT ROETINE
2200 IF A>-.5 THEN GOTO 2220
2210 LET A=4096+A-1E-8
2220 LET A=INT(A+.5)
2230 LET A1=0=A2
2240 LET A2=A2+(A-INT(A/8)*8)*10^A1
2250 LET A=INT(A/8)
2260 LET A1=A1+1
2270 IF A><0 THEN GOTO 2240
2280 RETURN
2290 REM OCT NA DEC ROETINE
2300 REM IN =A EN UIT = A2
2310 LET A1=0=A2
2320 LET A2=A2+(A-INT(A/10)*10)*8^A1
2330 LET A=INT(A/10)
2340 LET A1=A1+1
2350 IF A><0 THEN GOTO 2320
2360 RETURN
2370 GOTO 0390
2380 END

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