A HIGH EFFICIENCY HIGH POWER LED DRIVER WITH FAULT TOLERANCE AND MULTIPLE LED LOAD DRIVING USING A COUPLED CUK CONVERTER

by

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Submitted in partial fulfilment of the requirements for the degree
*Master of Engineering (Electrical Engineering)

in the

Department of Electrical, Electronic and Computer Engineering
Faculty of Engineering, Built Environment and Information Technology

UNIVERSITY OF PRETORIA

April 2013

SUMMARY

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Keywords: LED, Cuk, Coupled Inductor, Digital Control, DSP, Multiple LED Load Driver, Fault-tolerant LED Driver.

Lighting consumes approximately 20-25% of the energy produced worldwide. LED based lighting is rapidly becoming the preferred choice over incandescent and fluorescent based lighting. LEDs have advantages such as high efficacy, long operating lifetime and excellent lumen maintenance. Therefore, to gain benefits from LEDs for lighting purposes, they must be driven with efficient drivers which maintain high LED efficacy and long LED lifetime.

A review of existing LED drivers is done, and their advantages and drawbacks are identified. Existing fault-tolerant drivers are also reviewed. Several dimming methods and their effects on the LED efficacy and lifetime are investigated. As a result, a converter with coupled inductors, suitable as an LED driver which has high efficiency and can maintain high LED efficacy, incorporated with a high efficiency dimming method, is chosen.

For the proposed LED driver, a comprehensive analysis on the effects of coupling type and coupling coefficient on converter performance is done. This is carried out to establish the best coupled inductor structure and coupling coefficient, for the proposed LED driver. The coupled inductor obtained is used to achieve high LED efficacy and also used to eliminate the need for an output filtering capacitor. This results in a highly compact, high efficiency and low cost LED driver.

A lossless method of LED string current sensing is proposed, so that driver efficiency is not negatively impacted. The LED driver and a digital control system are designed, with the fault-

tolerant feature incorporated. The LED driver and the control system are simulated and practically implemented. The results obtained show excellent LED driver performance. The fault-tolerant feature can enable the driver to operate under fault conditions, saving repair costs and down time.

Additionally, a novel digitally controlled LED driver, which can drive several independent multiple LED loads, is proposed. This novel driver is simulated and practically implemented; with the results showing excellent driver performance. The novel LED driver can simplify and reduce costs of existing LED lighting systems.

OPSOMMING

'N HOËPRESTASIE- HOËKRAG- LED-DRYWER MET FOUTTOLERANSIE EN VEELVULDIGE LED-LADINGDRYWING WAT GEBRUIK MAAK VAN 'N GEKOPPELDE CUK-OMSETTER

deur

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Sleutelwoorde: LED, CUK, gekoppelde induktor, digitale kontrole, DSP, meervoudige LED-ladingdrywer, fouttolerante LED-drywer

Beligting gebruik ongeveer 20-25% van die energie wat wêreldwyd geproduseer word. LED-gebaseerde beligting is vinnig besig om die voorkeurkeuse te word eerder as gloeilamp- of fluoressensieverligting. LEDs het voordele soos hoë doeltreffendheid, 'n lang operasionele leeftyd en uitstekende lumenhandhawing. Om voordeel te trek uit LEDs vir beligtingdoeleindes, moet hulle deur doeltreffende drywers aangedryf word om hoë LED-doeltreffendheid en 'n lang LED-leeftyd te verseker.

'n Opname van bestaande LED-drywers word gedoen en hulle voor- en nadele word bepaal. Bestaande fouttolerante drywers word oorweeg. Verskeie dempmetodes en hulle uitwerking op die doeltreffendheid en leeftyd van LEDs word ook ondersoek. Op grond daarvan word 'n omsetter met gekoppelde induktors gekies, wat geskik is vir gebruik as 'n hoogs doeltreffende LED-drywer wat ook hoë LED-doeltreffendheid kan handhaaf, tesame met 'n hoogs doeltreffende dempmetode.

'n Uitvoerige analise van die uitwerking van 'n koppeltipe en koppelkoëffisiënt op die omsetterverrigting word vir die voorgestelde LED-drywer gedoen. Dit word gedoen om die beste gekoppelde induktorstruktuur en koppelkoëffisiënt vir die voorgestelde LED-drywer te bepaal. Die gekoppelde induktor wat verkry is, word gebruik om hoë LED-doeltreffendheid te verkry en ook om die behoefte aan 'n uitsetfiltreerkapasitor uit te skakel. Die gevolg is 'n uiters kompakte, baie doeltreffende en goedkoop LED-drywer.

’n Verliesvrye metode vir LED-stringstroombepaling word voorgestel, sodat daar geen negatiewe uitwerking op die doeltreffendheid van die drywer is nie. Die LED-drywer en ’n digitale kontrolesisteem word ontwerp, waarby die fouttoleransiekenmerk ingesluit word. Die LED-drywer en die kontrolesisteem word gesimuleer en prakties geïmplementeer. Die fouttoleransiekenmerk kan die drywer in staat stel om in fouttoestande te werk, wat herstelkoste en staaktyd beperk.

Daarbenewens word ’n nuwe digitaalbeheerde LED-drywer, wat verskeie onafhanklike meervoudige LED-ladings kan aandryf, voorgestel. Die nuwe drywer word gesimuleer en prakties geïmplementeer; die resultate dui op uitstekende drywerwerkverrigting. Die nuwe LED-drywer kan bestaande LED-beligtingsisteme vereenvoudig en die koste daarvan verlaag.

ACKNOWLEDGEMENTS

I would like to express profound gratitude to my supervisor professor Michael Gitau for the useful comments, remarks and engagement through the learning process of this research. I also like to thank my fellow colleague Frederick Mukundi, for fruitful discussions and insights. I am grateful to the Energy Efficiency and Demand Side Management Hub for the financial support that was accorded. Last but not least, I would like to give special thanks to my wife Ahlam and my family, for their encouragement, patience, and unwavering support.

LIST OF ABBREVIATIONS

LED	Light Emitting Diode
PWM	Pulse Width Modulation
AM	Amplitude Mode
EMI	Electro-Magnetic Interference
EMC	Electro-Magnetic Compatibility
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
ZOH	Zero Order Hold
DSP	Digital Signal Processor
RMS	Root Mean Square
PCC	Peak Current Control
HCC	Hysteretic Current Control
ACC	Average Current Control
ADC	Analogue to Digital Converter

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CHAPTER 1 INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Background and Context3

High power LED lighting is rapidly emerging as a preferred technology over incandescent, fluorescent and compact fluorescent based lighting. This is due to the high efficacy that LED's have now achieved [1] [2]. They have advantages such as long operating lifetime, dissipate less heat, excellent lumen maintenance and a high colour rendering index [3] [4]. Therefore, to benefit from the advantages LEDs have to offer, efficient, long lifetime LED drivers are needed.

For high power LED lighting applications such as industrial lighting or street lighting, individual high power LEDs need to be connected in a series-parallel combination [5] [6]. In the case of an open-circuit failure of one or more of the parallel LED strings, the current through the remaining strings will increase, resulting in varied luminous output [7]. This over-current condition may damage the remaining LEDs causing eventual failure of the entire LED lighting system.

Some fault-tolerant LED drivers have been proposed in literature [7]-[11]. A lossy current sensing method, which reduces driver efficiency, was used in [8]. Again, this method is unsuitable if numerous LED strings are to be used, as power dissipation increases drastically. Linear regulators were used in [11], which are unsuitable for high power LED lighting systems due to significant losses. Complex control systems are used in [7] and [10], which may lead to increased costs and reduce the practical implementation viability. To solve the afore-mentioned problems, a lossless method of current sensing using low cost hall-effect switches is proposed. They can be seamlessly integrated with digital controllers, improving control system simplicity, maintaining driver efficiency and reducing cost.

Dimming for high power LED drivers is necessary for energy saving purposes [12]. Basic dimming methods employed for LED drivers are Pulse-width Modulation (PWM) and Amplitude Modulation (AM) [13]-[15]. PWM requires a controlled switch either in parallel or series with the LED load [13] [16] [17]. Use of a controlled switch increases system complexity and cost. PWM dimming introduces current ripple through the LEDs, consequently reducing the LED efficacy and optical output [14] [18]. Furthermore the use of PWM dimming may lead to performance degradation of the optical output and shorten LED lifetime [14] [18]. The rapid switching

introduced by PWM dimming may lead to EMI generation concerns, which needs to be mitigated, thus increasing the complexity and costs of LED drivers [14] [19]. Flicker may become perceivable to the human eye if the PWM dimming frequency is less that 200 Hz [17]. Despite the drawbacks of PWM dimming, it does not introduce LED chromaticity shift, and is suitable for applications such as displays [20].

AM dimming is done by varying the reference value of the current control loop of an LED driver, which effectively controls the LED load current, and in turn determines the optical output [14] [21]. AM does introduce a slight colour shift, as the LED forward current is varied [14] [21] [22]. However, AM is a more efficient dimming method as compared to PWM, as there are no saturation effects, due to the absence of peak currents [14] [42]. AM dimming may also preserve LED life and maintains high LED efficacy [14]. Therefore, the use of AM dimming for a high power LED driver may aid in achieving high LED efficacy and long LED lifetime. Moreover, AM dimming is simple and does not require extra circuitry as compared to PWM, which makes it cost effective.

Dc-dc converters as applied to LED driving applications can be categorized by the nature of input and output currents. The flyback, SEPIC, boost and buck-boost converters can have continuous input currents and pulsating output currents [23]-[25]. The pulsating output current from these converters has the potential to reduce LED efficacy, and even degrade the LED lifetime [27] [26]. Often, a large filtering electrolytic capacitor is needed at the output. This becomes a drawback, as the lifetime of the LED driver is reduced, due to the short lifetime of the electrolytic capacitor [23].

Buck and zeta converters have continuous output currents, and pulsating input currents. This feature leads to EMI generation, which needs additional filtering to comply with EMC standards [27]. On the other hand, a continuous conduction mode cuk converter has both non-pulsating input and output currents [28]. This feature hence reduces EMI filtering requirements [27]. At the same time, the cuk topology efficiently transfers energy capacitively, has a low component count, and the input and output inductors can be coupled on a common magnetic core [28]. Coupling the input and output inductors of the cuk converter can have significant advantages, if this topology is used for LED driving applications.

Coupling can be used to achieve a highly compact, low cost LED driver, and also to minimize the output current ripple significantly, eliminating the need for an output filtering capacitor, and aid in

achieving high LED efficacy. Therefore a coupled cuk converter is proposed to solve the drawbacks associated with other topologies used as LED drivers. These include high EMI generation, use of short lifetime electrolytic capacitors, low LED load efficacy and reduced LED lifetime.

Analogue based control has been popular for controlling dc-dc converters [29]. Due to recent developments in digital signal processors, such as reducing costs and increased processing power, real time digital control of dc-dc converters is gaining popularity [30]. This is due to the numerous advantages that digital control offers over analogue control [30].

Digital controllers have better noise immunity, are less susceptible to parameter variations such as ageing and temperature variations [31]. In addition, because the control algorithm is in software form, digital controllers are suited to implementing complex control algorithms [30]. At the same time, added functionality such as fault detection and remote monitoring can easily be incorporated. Thus digital controllers used in conjunction with LED drivers can add to their functionality, such as fault tolerance, remote dimming capabilities and provide monitoring services. Furthermore, LED drivers with digital control can mitigate problems of analogue controlled drivers such as low reliability, and short driver lifetime.

LEDs require accurate current control due to their small dynamic resistance, to maintain consistent light output [32]. Therefore a suitable high accuracy current control scheme is required. Widely used current control schemes for LED drivers are linear current controllers, peak current controllers (PCC) and hysteretic current controllers (HCC) [12] [33]-[35]. Linear current regulators are highly inefficient and unsuitable for efficient high power LED drivers [33]. PCC achieves inaccurate current control due to the peak-to-average current error [35]. This may impact the LED optical output negatively, and also result in poor current regulation. PCC is also sensitive to noise and is susceptible to sub-harmonic oscillation [35] [36]. HCC achieves better current control accuracy than PCC, but results in higher dissipation in case a resistive sensor is used. However, HCC is also prone to sub-harmonic oscillation [34] [37]. Due to the drawbacks of PCC and HCC, they may be unsuitable for high power LED drivers, as current accuracy is important, and the sub-harmonic oscillation may introduce undesired current ripple through the LEDs.

Average current control (ACC) has high current accuracy, better noise immunity and can avoid sub-harmonic oscillation through selection of proper feedback gain [36]. Therefore, it is worthwhile to consider ACC for use in high power LED drivers to ensure excellent current accuracy thus maintaining consistent light output. Lack of sub-harmonic oscillation and better noise immunity may aid in achieving a high reliability LED driver.

Current ripple through the LEDs affects LED performance. A high peak-peak current ripple with a constant average current leads to increased power dissipation, due to junction heating and thermal derating [38]. This causes depreciation of the LED optical output, efficacy and may result in reduced LED lifetime [26] [38]. Moreover, accurate current control may be a challenge for LED drivers with high current ripple through the load [15]. The high current ripple present at the output of some LED drivers may necessitate the use of an electrolytic capacitor [23] [24] [39]. This in turn may result in short LED driver lifetime [41].

To mitigate problems arising from LED drivers with high output current ripple, such as decreased light output, low LED efficacy and short LED lifetime, a coupled inductor cuk converter is proposed. The coupled inductors are to be used to minimise load current ripple to achieve high LED efficacy, increased optical output and maintain long LED lifetime. The reduced current ripple should also aid in improving current control accuracy. In addition, using the coupled inductors can assist in eliminating the use of an output filtering capacitor. Therefore, using the coupled inductor should contribute to reducing driver component count, and thereby achieve a highly compact and low cost LED driver. It is hypothesized that the coupled inductors will improve the efficiency of the cuk LED driver, as compared to a non-coupled cuk LED driver.

Existing LED lighting systems require a driver for each LED load [23] [40]. This can become costly and result in complicated LED lighting systems as the number of lights increase. A single high power LED driver, using digital control can be designed to drive several independent low power LED loads. These loads can then be separately switched on or off as needed, without affecting operation of the remaining connected loads. This novel concept would simplify installation and reduce costs of existing LED lighting systems.

1.1.2 Research Gap

The effect of coupling type namely, non-symmetric and symmetric coupling and effect of the coupling coefficient on the coupled inductor cuk converter performance for LED driving purposes has not been previously studied. Identifying the best coupling method and coupling coefficient would aid in obtaining a highly efficient, high power LED driver; which also achieves a low output current ripple, consequently resulting in high LED load efficacy. The reduced output ripple would help to eliminate the output filtering capacitor; in turn achieving a low component count and low cost LED driver.

A fault-tolerant LED driver which senses open LED strings, utilising a lossless method of sensing the string current has not been studied in the available literature. Identification of a lossless current sensing technique, integrated with a digital controller should maintain the high LED driver efficiency, while performing the fault-tolerant function, leading to a highly efficient fault-tolerant and high power LED driver.

A single LED driver used for driving multiple low LED loads has not been previously proposed in literature. Using the proposed LED driver with a suitable digital controller to sense which load is connected or disconnected, and automatically control the output current according to load requirements, should lead to the development of a high efficiency multiple load LED driver.

1.2 RESEARCH OBJECTIVE AND QUESTIONS

The following objectives are to be achieved;

(i) To identify the effects of coupling type and coupling coefficient on the isolated cuk converter performance; to aid in identifying the best coupled inductor type and coupling coefficient.

(ii) To develop a high efficiency digitally controlled LED driver with efficient dimming capability that maintains high LED efficacy, long LED lifetime, is compact and has low cost.

(iii) To develop an LED driver that is fault-tolerant and detects string current in a lossless manner.

(iv) To develop an LED driver capable of driving multiple individual LED loads; which can be individually switched on or off, without affecting the operation of the remaining connected loads.

The following are the research questions;

(i) How does the type of coupling, namely non-symmetric coupling and symmetric coupling, and the coupling coefficient, affect the performance of the isolated cuk converter, and which coupling type and coefficient is best for driving LEDs?
(ii) How can high power LEDs be driven with high efficacy and low ripple to maintain long lifetime?
(iii) Can the use of coupled inductors aid in eliminating the need to employ an output capacitor, and to achieve a compact low cost LED driver?
(iv) Is it possible to obtain a fault-tolerant LED driver which detects the LED string currents in a lossless manner?
(v) Is it possible to obtain an LED driver that can drive multiple low power LED loads, whereby each load can be individually switched on and off without affecting operation of the remaining connected loads?

1.3 HYPOTHESES AND APPROACH

The hypotheses are stated as;

(i) An isolated cuk converter with symmetrically coupled inductors and a tight coupling coefficient used as a high power LED driver with amplitude mode dimming, would achieve high driver efficiency, low output current ripple, ensuring a high quality light output, high LED efficacy, may maintain long LED lifetime and can eliminate the need of the output capacitor. This in turn will aid in achieving a compact and low cost driver.
(ii) The use of the proposed LED driver with lossless string current detection and digital control would achieve a highly efficient fault-tolerant high power LED driver.
(iii) Finally, use of a digital control system should enable the proposed single high power LED driver to drive multiple individual low power LED load.

The approach used is given as follows;

(i) Literature review; a study on the different types of converters presently available for LED driving is done. This will aid in choosing a suitable topology for LED driver to be used in light of high LED efficacy, high efficiency and compactness. Presently used dimming methods and fault-tolerant LED drivers will be studied. An overview of digital control techniques as applied to dc-dc converters will be done. A control system will be identified to operate the LED driver in closed-loop to achieve a fault-tolerant driver, and also for a single driver supplying multiple LED loads.

(ii) Analysis, modeling and design; the converter is analyzed and modeled to obtain the necessary transfer-functions for control purposes. The converter components are designed and selected for optimal performance.

(iii) Simulation; the designed converter is simulated with suitable simulation software to validate the design.

(iv) Control system design and simulation; a closed-loop digital control system capable of controlling the LED current is designed. The converter with the control system is simulated again to validate the design.

(v) Practical implementation; the designed converter is implemented in hardware to validate simulation and analytical results.

1.4 RESEARCH GOALS

The research goals are given as follows;

(i) To carry out a comprehensive analysis on the effect of coupling type and coupling coefficient on the performance of the coupled inductor isolated cuk converter; to aid in achieving an LED driver with high efficiency, maintains high LED efficacy, enables output capacitor elimination, and is compact and has low cost.

(ii) To obtain a fault-tolerant high efficiency LED driver with lossless LED string current detection.

(iii) To develop a digitally controlled single LED driver capable of driving multiple LED loads.

1.5 RESEARCH CONTRIBUTION

LEDs need to be driven with high efficiency and low current ripple to obtain high LED efficacy, maintain long lifetime and achieve high quality light output. Therefore, highly efficient LED drivers capable of satisfying the afore-mentioned requirements are needed. Available LED drivers have been studied and have limitations such as low LED efficacy, low dimming efficacy, may not maintain long LED lifetime, are bulky and costly.

An investigation into the effects of coupling type and coupling coefficient of the coupled inductor cuk converter yield results that aid in selecting the best coupling method and coupling coefficient. This will enable the design of a high efficiency LED driver that can maintain high LED efficacy, preserve long LED lifetime and achieve a compact low cost driver.

Fault tolerance of LED drivers is necessary, so that uninterrupted operation can be guaranteed in case of an open-circuit string failure within the high power LED load. This can aid in reducing repair costs and downtime. Presently available fault-tolerant LED drivers have limitations such as complexity and inefficient current sensing techniques. Identification of a lossless method of string current detection can preserve the high LED driver efficiency, and the use of digital control can simplify the controller complexity.

A novel concept of using a digital controller for a single LED driver to drive multiple low power LED loads, which can be individually switched on or off without affecting operation of the connected loads is proposed. This could aid in saving costs and simplify implementation of LED lighting systems.

1.6 OVERVIEW OF STUDY

Chapter 2 deals with an overview of high power LEDs, dimming methods and various converter topologies used as LED drivers; noting their advantages and limitations. Available fault-tolerant LED drivers are also discussed and their limitations pointed out. An overview of current control methods and the effects of current ripple on LED efficacy are also carried out. A study on digital control and design techniques for dc-dc converters is also done. The proposed LED driver to be developed is then finally given.

Chapter 3 deals with the modelling of the isolated coupled inductor cuk converter. A generalised inductor model for non- coupled, non-symmetrically coupled and symmetrically coupled inductors is done. The converter is analysed and state space averaging is used to obtain the necessary control-to-output inductor current transfer-function, necessary for average current control.

Chapter 4 deals with the design and selection of the converter components. The semiconductor devices and capacitors are sized and selected. The isolation transformer is designed. The inductors namely; non-coupled, non-symmetrically-coupled and symmetrically coupled are designed for the practical investigation into the effects of coupling on converter performance, to be done in Chapter 5.

Chapter 5 investigates the effects of different coupling methods, namely non-symmetric and symmetric coupling on the cuk converter performance. Non-coupled inductors are also included for comparison purposes. The comprehensive analysis is done analytically to determine effects of coupling in terms of losses, input and output ripple, impact of coupling on inductance size and LED efficacy. This analysis is carried out to identify the most suitable coupling method and coupling coefficient to be used for the proposed LED driver. The analytical analysis results are then practically validated.

Chapter 6 deals with the design of a digital controller for; (i) a fault-tolerant high power LED driver (ii) an LED driver capable of driving multiple low power LED loads. The designed controller is simulated, and also practically validated. The control is implemented digitally using a suitable DSP.

Chapter 7 deals with the simulated and practical converter results and various converter waveforms are presented. The analytical and practical efficiency of the designed LED driver is also done. Finally, the current regulation of the LED driver is practically done and presented.

Chapter 8 deals with the conclusion of this dissertation, with key findings and observations being pointed out, as well as the scope of future work.

CHAPTER 2 LITERATURE STUDY

In this Chapter, an overview of high power LEDs is briefly discussed regarding the I-V characteristics, series-parallel connections and LED faults. Also, the need for fault-tolerant LED drivers is discussed. Presently available fault-tolerant drivers, found in available literature are also presented.

Dimming methods and their effect on LED efficacy is discussed. LED drivers based on various dc-dc converter topologies found in literature are presented, with their advantages and shortcoming being pointed out. Coupled inductors are briefly discussed, and their use with available LED drivers is presented.

Various current control methods and the effect of current ripple on LED efficacy are briefly discussed. A brief overview of digital control for dc-dc converters is done, and presently available digitally controlled LED drivers are discussed. Finally, the proposed LED driver is presented.

2.1 OVERVIEW OF HIGH POWER LEDS

High power LED based lighting is rapidly emerging as a preferred technology over incandescent and fluorescent based lighting. This is due to the recent developments that have enabled the LED efficacy to exceed that of traditional lighting [2]. LEDs now have significantly longer operating lifetime, dissipate less heat, and have excellent lumen maintenance while sustaining a high colour rendering index [3] [4].

Furthermore, LEDs are compact and robust, have good dimming capability and are mercury free. It is for these reasons that LEDs need to be driven efficiently using reliable and cost effective drivers so as to gain various benefits such as, lower operating costs due to reduced energy consumption, lower maintenance costs, increased luminaire operating lifetime and environmentally safe recycling and disposal at the end of their lifespan [43].

2.1.1 I-V Characteristics of High Power LEDs

LEDs are current devices whose forward current determines the forward voltage and luminous output [32]. The small dynamic resistance of the LED imposes the need for accurate current control

to obtain a precise light level output from the LED [14] [15] [21] [35] [44]. Figure 2.1 shows the typical current-voltage (I-V) characteristic of a high power LED; where I_{fwd} and V_{fwd} are the forward current and voltage respectively at a particular operating point [45].

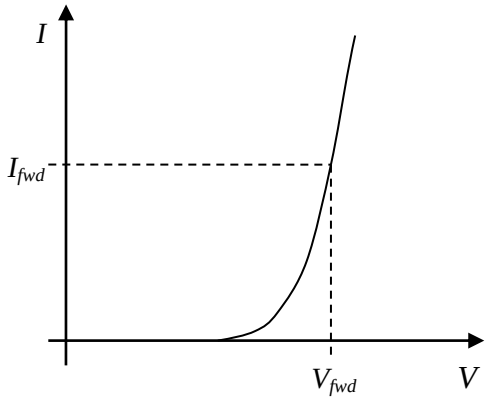


Figure 2.1: The I-V characteristic of a high power LED.

2.1.2 Series-Parallel Connection of LEDs

High power LEDs are commercially available in powers ranging from 1 W to 10W [46]. To obtain a high power LED load suitable for a high light flux application such as street lighting which requires about 100 W to 200 W [5], the individual high brightness LEDs need to be connected in a series-parallel combination [6]. For a given total LED load power, connecting the LEDs only in series yields a high load voltage. This high load voltage may impact the LED driver negatively, as the voltage stress on the active converter switch is increased [27], forcing selection of a switch with a high voltage blocking capability, thereby increasing costs. In addition, an open-circuit failure of one of the LEDs will cause the failure of the whole string, unless a bypass mechanism is in place [10].

On the other hand, connecting the LEDs in only a parallel configuration yields a high total load current. Again, this may impact the LED driver efficiency negatively, as copper and conduction losses in the driver may become significant [27]. The parallel connection has an advantage that open-circuit failures of any of the LEDs results in continued operation of the LED load [8]. Therefore, to achieve an LED load that optimises the LED driver operation, an appropriate series-parallel combination of the LEDs is needed.

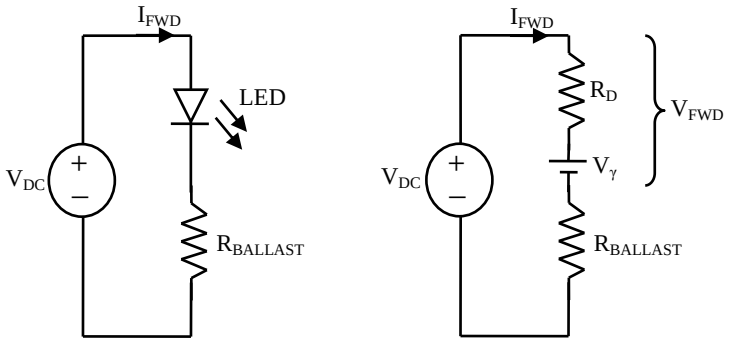
2.1.3 LED Modelling

LED modeling helps to obtain an electrical model as it will be used as a load. A simple model assumes the dynamic resistance of the LED to be static and is considered only at a particular operating point [32]. This results in a straight line diode I-V characteristic. This simple model is suitable if the LED will be operated with only a narrow variation of the forward current.

For LED applications that involve a wide variation of the forward current, as applicable to dimming, then a more accurate model that takes the dynamic resistance and the threshold voltage into account is required. This accurate LED model is as follows [47];

$$V_{FWD}=R_D \cdot I_{FWD}+V\gamma \tag{2.1}$$

Where V_{FWD} is the forward voltage drop, R_D is the dynamic resistance, I_{FWD} is the forward LED current and V_γ is the threshold voltage. Figure 2.2 (a) shows the simple LED model and Figure 2.2 (b) shows the accurate LED model [47].



(a) Simple Model (b) Accurate Model

Figure 2.2: A simple LED model and an accurate LED model.

To obtain an alternative accurate model of the dynamic resistance, the resistance of the LED can be obtained from the I-V curve, and by using a suitable non-linear curve fitting method, a highly accurate dynamic resistance for a particular LED can be obtained at the desired operating current.

2.1.4 LED Faults and Fault-Tolerant LED Drivers

Fault tolerance for an LED load is important as it saves cost and downtime [7]. The most commonly occurring LED fault is an open-circuit fault [8] [10]. For an LED load with several parallel strings, an open-circuit failure of any of the LEDs will lead to the failure of the whole

string. Since the output current of the LED driver is constant, this means that the current through the connected strings would increase, and may cause damage to the remaining LEDs due to over-current conditions, causing eventual failure of the whole LED load [6]. For an LED driver with several LED strings, implementation of a fault-tolerant feature can provide continued operation in case of failure. This can aid in reducing repair costs and downtime.

Fault-tolerant LED drivers have been proposed in [7]-[11]. In [8], a method for identifying which string has open-circuited and consequently adjusting the total load current was implemented. Although the drawback is the lossy current sensing in each string that reduce the overall driver efficiency. In [11], linear regulators are used, which may be unsuitable for high power applications to significant losses. In [10] and [7], complex control systems are used; this may lead to increased costs and reduce the practical implementation viability.

2.2 LED DIMMING METHODS

Dimming provides a good opportunity for high power LED drivers to save energy. Also, dimming is an important LED driver feature, enabling light output control, when the full light output is not required. Several dimming methods are discussed in this Section.

2.2.1 Pulse Width modulation

Pulse Width Modulation (PWM) is implemented by inserting a controlled switch in series or parallel with the load, or even switching on and off the whole converter, resulting in an averaged current which depends on the duty cycle of the dimming PWM current waveform [13] [16] [17] . The PWM method introduces current ripple through the LEDs, and also the peak current present in the PWM waveform does not contribute to light production due to saturation of the LED [21]. Hence a lower efficacy and light output of the LED is seen when using PWM [18]. Since LEDs are highly sensitive to the peak current level, driving them with a pulsating current such as PWM may lead to LED performance degradation in terms of the optical output with time and shortened lifetime [14] [18].

From the LED driver perspective, PWM needs additional switching circuitry adding complexity and cost to the LED driver [12]. Furthermore, the rapid switching of the load current done by PWM dimming introduces EMI concerns and which need to be mitigated adding even further driver complexity [14] [19]. Flicker may become perceivable if the PWM dimming frequency is less than

200Hz [17]. Despite the drawbacks of PWM dimming, it does not introduce chromaticity shift of the optical output, and thereby finds applications where colour shifting is undesirable such as displays [20].

2.2.2 Amplitude Mode Dimming

Amplitude mode dimming is done by changing the reference value of the control loop, consequently varying the current through the LED load, hence controlling the light output [14]. Although a slight colour shift as the forward current is varied is observed [14] [21] [22], AM achieves more efficient dimming as compared to PWM as there is no saturation effect due to the absence of peak currents [14] [42].

In [50], it was found that the colour shift introduced by AM dimming is not significant for white LEDs. In applications such as general high power white LED lighting where the colour shift is not critical and efficiency is of utmost importance, AM dimming is suitable and can be implemented using a suitable current control method. The LED current accuracy when using PWM dimming is not as critical as compared to AM dimming, but PWM imposes a lower efficacy [21]. Therefore this dimming method is simple and does not require any extra circuitry for dimming, making it cost effective.

2.2.3 Bi-level Current Driving

The bi-level current driving method combines AM and PWM methods by introducing an offset in the PWM waveform and reducing the peak value. Thus the bi-level current driving method achieves improved luminous efficacy over the PWM method [14]. Despite the bi-level current waveform having an offset, it is still associated with the peak current magnitude similar to the PWM waveform, and any improvement of luminous efficacy is only slightly incremental. Furthermore, complex current control is required to implement this technique. Other methods of LED current modulation have been proposed in literature, such as pulse-code-modulation and multiphase PWM [45] [48].

2.3 LED DRIVERS

Various dc-dc converters have been used for LED driving. A common driver used is the flyback converter. Other commonly used converters as seen in literature used as LED drivers are SEPIC,

buck-boost, buck (forward converter), with the least common being cuk and zeta. The converters used as LED drivers are briefly described in the following Sections.

2.3.1 Flyback

The flyback converter derived from the buck-boost converter is a commonly used topology for power applications of 50-100W [23]. It uses a low component count and provides a low cost solution. The input current waveform is discontinuous while the output current is of a pulsating nature and a large output capacitor (usually electrolytic) is needed for filtering. There have been numerous proposals of the flyback converter being used as an LED driver [51]. The flyback converter is shown in Figure 2.3.

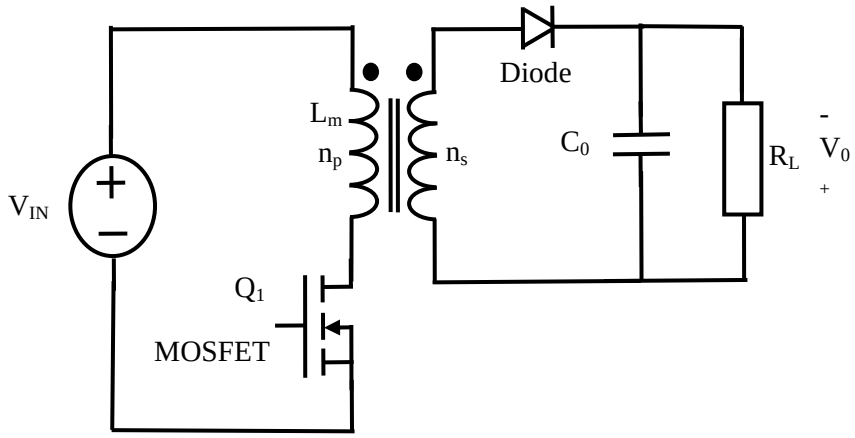


Figure 2.3: A Flyback Converter.

To increase the driver lifetime, it has been suggested in [23] that the output capacitor can be eliminated. The disadvantage of this is that the discontinuous output current that results from this affects the LED as it causes the early degradation and eventual failure [14] [18].

To reduce the core size and to perform PFC, the flyback converter is operated in DCM. However, this results in increased conduction loss and current stress on the switch. DCM also causes generation of excess EMI, which increases the size of the EMI filter [24] [52]. Furthermore, the transformer core in the flyback is not fully utilised due to the uni-polar magnetising current and uni-polar flux swing. In CCM, the generated EMI is less, but a larger core is needed to handle the continuous current. The flyback inductor has to be constructed with a very tight coupling coefficient to minimise the leakage inductance, otherwise this causes excessive voltage spikes across the switch which have to be damped using a snubber [52].

2.3.2 Buck-Boost

There have been a number of proposals of buck-boost converters being used as LED drivers [25] [39] [53]. Buck-boost converters can be either step up or step down, depending on the duty ratio used, while inverting the output. The converter exhibits discontinuous input current like the flyback and SEPIC, but requires a large output capacitance as a filter due to the pulsating output current [54]. In addition, the switch position requires a floating gate drive circuit, increasing the practical implementation complexity [28]. The buck-boost converter is shown in Figure 2.4.

Other variations of the buck-boost topology such as the quadratic buck-boost and the tri-mode buck-boost LED driver have been proposed [55] [56].

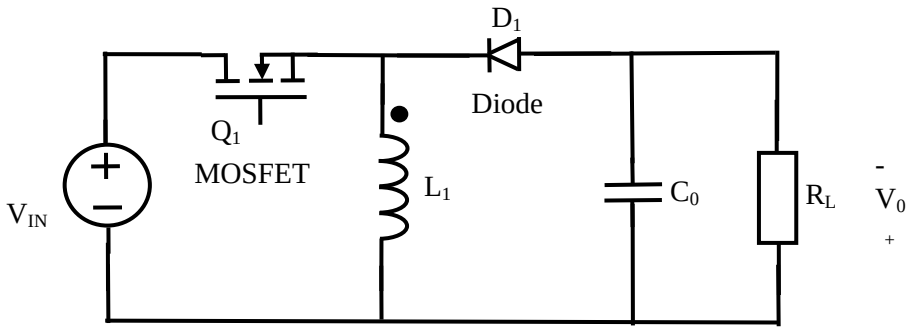


Figure 2.4: A buck-boost converter.

2.3.3 SEPIC

The SEPIC is a 4th order converter and appears numerous times in literature as an LED driver [24], [12]. The SEPIC has a continuous input current and a pulsating output current. Due to the input structure, the SEPIC also finds applications as a power factor correction pre-regulator [57].

A disadvantage of the SEPIC, like the flyback, is the pulsating output current waveform. To filter this current, a large electrolytic capacitor is required to supply the load current when the active switch is turned on. In [24], an interleaved SEPIC converter as an LED driver is proposed to reduce the output filtering requirements. Using interleaving, total ripple cancellation can be achieved at certain duty ratio operating points and the phase shift of the inductor waveforms. The drawback of interleaving is the increased component count and more complex control. Furthermore, the total ripple cancellation only occurs at certain operating points and is unsuitable for operation at different loads. The SEPIC is shown in Figure 2.5.

Since the voltage waveforms of the inductors in the SEPIC are similar, the inductors can be coupled and can benefit from ripple steering [58]. However, only the input ripple current can be minimised while the output ripple remains unchanged. This may have little benefit in regard to the ripple and input harmonics since the input current of the SEPIC is already continuous.

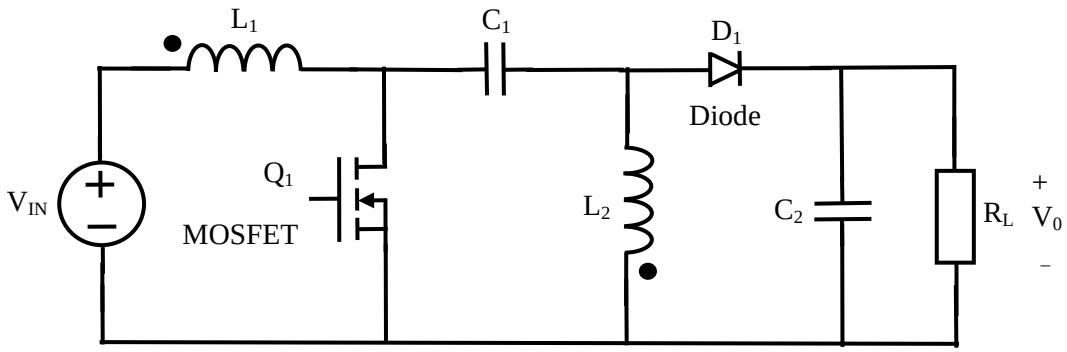


Figure 2.5: A non-isolated SEPIC converter.

2.3.4 Buck Converter

The buck converter is the most basic converter used to step down voltage. A commonly used isolated version derived from the buck topology is the forward converter. The forward converter has been used as an LED driver in [59], whereas a basic single stage buck LED driver has been proposed in [60] and [61]. A variation of the buck converter namely the quadratic buck converter has also been proposed in [62].

2.3.5 Zeta Converter

The zeta converter is a 4^{th} order converter that can be used as a step up or a step down and has a non-inverting polarity. The zeta is also known as the dual of the SEPIC [63]. The input current is of a discontinuous nature, as the switch is connected in series while the output current is continuous. Since the inductor voltage waveforms are similar, the inductors can benefit from coupling. If ripple steering is used to minimise output ripple, then the output capacitor can be made small enough to use a film capacitor which has a long life. In literature, applications of the zeta converter as an LED driver are not many, although it has been proposed in [64]. The zeta topology is shown in Figure 2.6.

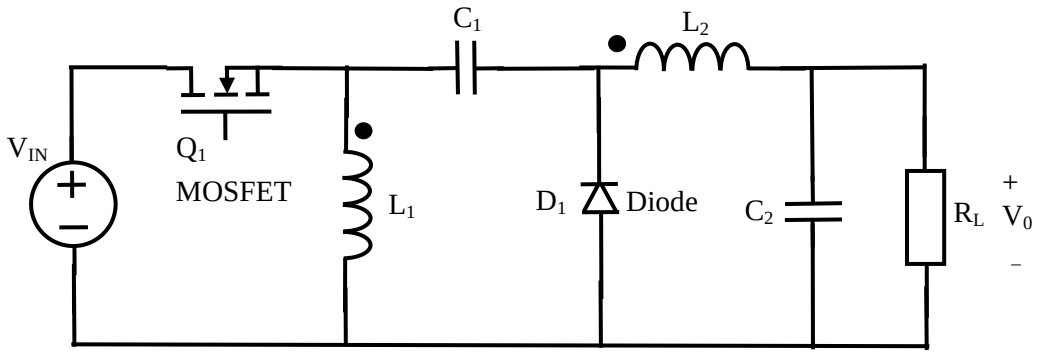


Figure 2.6: A non-isolated zeta converter.

2.3.6 Cuk Converter

The cuk converter is a combination of the basic boost and buck topologies in cascade. Therefore, it has a non-pulsating input and output current. Although it inverts polarity at the output, this however can be corrected by introducing an isolation transformer. The cuk converter performs capacitive energy transfer which is quite efficient [28]. The continuous input and output currents are advantageous because the generation of EMI and harmonics is reduced. This aids in reducing the input switching harmonics filter size and consequently reduces the effect of modifying converter dynamics [27]. The cuk converter switch position is in a favourable position, as no floating gate drive circuitry is needed [28]. Due to the voltage waveforms across the inductors being similar, the inductors can be coupled on a common core. This has benefits such as reducing the inductor size and component count, and can be used in such a way as to minimise ripple at the input or the output-side [28]. Furthermore, the coupling capacitor provides isolation in case of a fault occurring on either the input or output-side.

A non-coupled non-isolated cuk converter has been proposed as an LED driver in [65] and [89]. Although simple, the drawbacks are the extreme duty ratios observed making the control difficult, and use of an output capacitor increases component count. A discontinuous mode non-coupled, non-isolated cuk converter as an LED driver has been proposed in [90]; where it is used to perform automatic power factor correction without using a complex control loop.

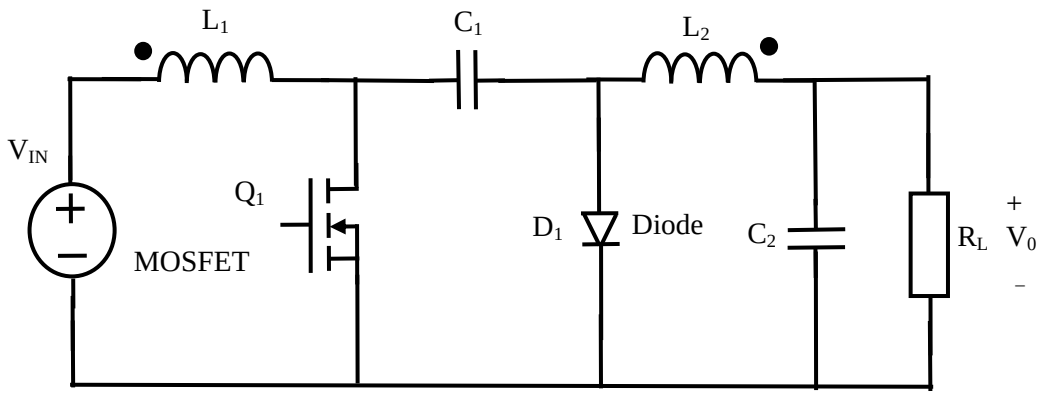


Figure 2.7: A non-isolated cuk converter.

2.3.6.1 Principle of Operation of the Cuk Converter

The basic operation of the cuk converter is explained in this Section [54]. When the active switch is on as shown in Figure 2.9, inductor L_1 charges and current through it ramps up. The diode becomes reverse biased because of the polarity across capacitor C_1. As the voltage across C_1 is greater than V_o, C_1 then discharges through the active switch, and charges inductor L_2 in the process [54].

When the active switch is off, as shown in Figure 2.10, both inductors L_1 and L_2 discharge through the forward biased diode. In this state, C_1 gets charged by the current through the input, L_1 and the diode. As C_1 is charges, the current in L_1 ramps down because V_{C1} has a higher potential than V_{in}. L_2 discharges as it transfers its energy to the output, and the current in L_2 ramps down. Therefore capacitive energy transfer takes place, as the coupling capacitor is charged and discharged periodically, transferring energy from the input to the output [54].

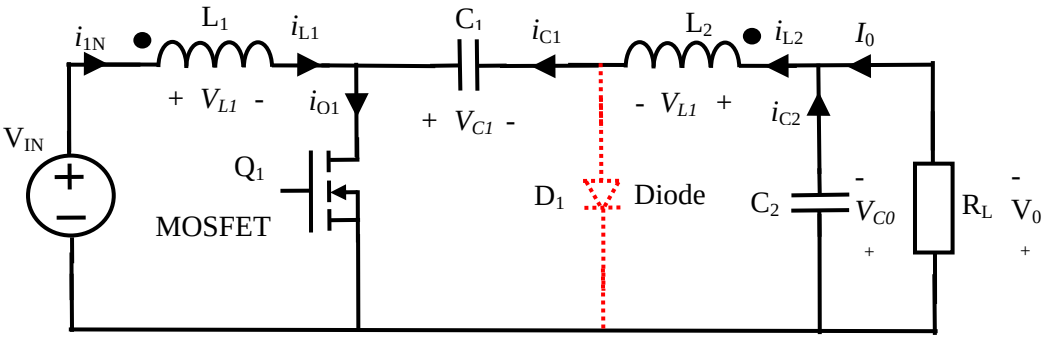


Figure 2.8: The cuk converter when the active switch is on.

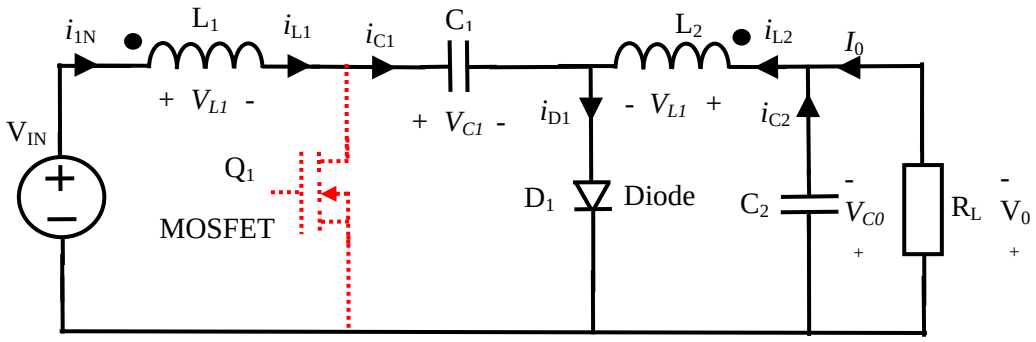
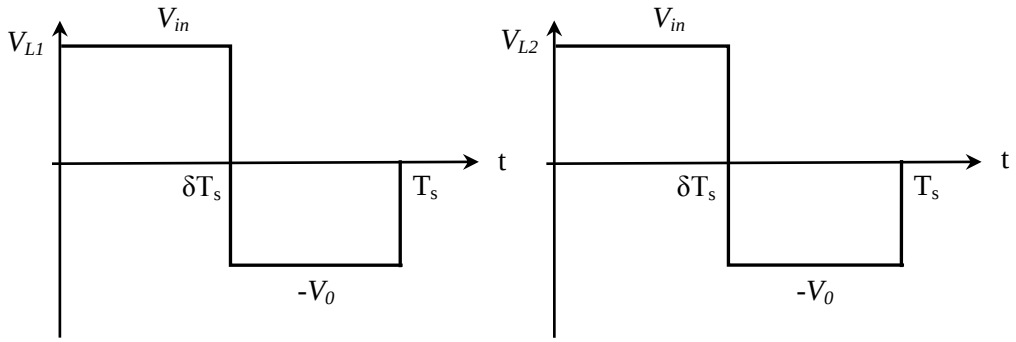


Figure 2.9: The cuk converter when the active switch is off.

2.3.6.2 The Cuk Converter Waveforms

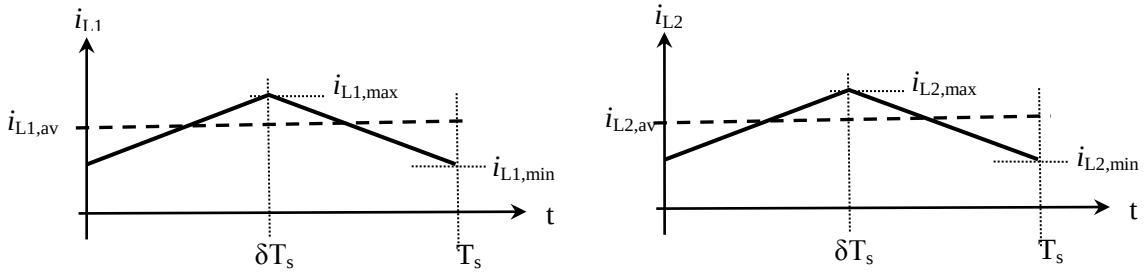
The cuk converter waveforms are briefly discussed in this sub-Section. When the switch is on, then the input voltage is applied across the input inductor L_1, and the potential across C_1, which is equal to V_{in}, is applied to the output inductor L_2. When the switch turns off, the diode then provides a path such that the output capacitor voltage, which is equal to V_o is applied across L_2. The voltage across L_1 is also equal to V_o, as C_1 gets charged from the input [54].

The inductor currents are similar, due to the similar voltage waveforms appearing across them. The inductor voltage waveforms are shown in Figure 2.10. The continuous nature of the output current waveform as seen in Figure 2.11 makes the cuk suitable as a current source to drive an LED load. Due to the similarity of the inductor voltage waveforms, the inductors can be coupled on a common core.



(a) Inductor L_1 voltage waveform (b) Inductor L_2 voltage waveform

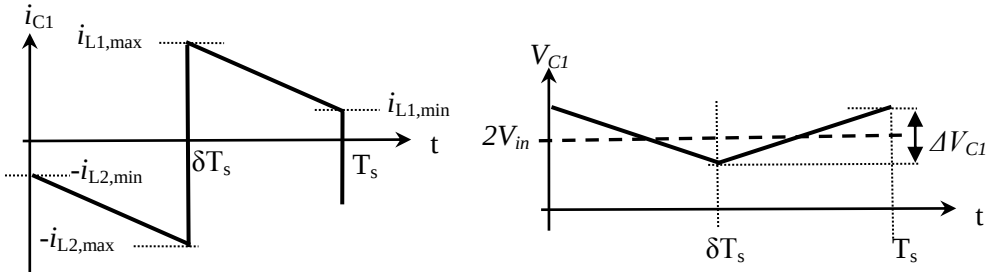
Figure 2.10: The cuk inductor voltage waveforms.



(b) Inductor L_1 current waveform (b) Inductor L_2 current waveform

Figure 2.11: The cuk converter inductor current waveforms.

The net average current through the coupling capacitor is zero, as seen in Figure 2.12. The average voltage potential across C_1 is seen to be twice the input voltage. When operating with a high input voltage, a capacitor that can handle twice this voltage stress is required [54].



(a) Current waveform (b) Voltage waveform

Figure 2.12: Cuk coupling capacitor waveforms.

2.4 COMMERCIAL MULTIPLE LED LOAD DRIVERS

A review of commercially available LED drivers capable of driving multiple LED loads reveals that they are not numerous. Some of these available drivers are seen in [114] and [115]. In [114], a single 600 W LED driver from Metrolight®, that can drive twelve parallel 50 W LED lamps is seen. Although dimming of all lamps is done simultaneously, individual switching off of each lamp is not possible. This can be a disadvantage if this driver is to be used to supply LED lamps in separate rooms, as independent switching on or off is needed.

An LED driver from IST, iDrive®Thor [115] is a 2 kW multichannel LED driver. It has 36 separate channels that can each supply an LED lamp. This driver provides individual dimming for each lamp. This is because each channel consists of a single dc-dc converter, and results in a costly LED driver.

2.5 COUPLED INDUCTORS

Coupled inductors have an advantage that a single magnetic element can replace multiple discrete inductors [66]. This has benefits of increased converter power density and reduced costs. Uses of coupled inductors are widely seen in literature, and have been used in interleaved converters [67], and converters such as the cuk and SEPIC [16] [68]. In [66], it was found that coupled inductors in an interleaved buck converter achieve better transient response as opposed to non-coupled inductors. In [69] it was found that coupled inductors aid in improving efficiency of a multiphase buck converter.

In [28] and [70], it was seen that coupled inductors in a cuk converter coupled be used to perform ripple steering, that is, minimize the input or output current ripple significantly, by configuring the mutual inductance and coupling coefficient in a particular manner. This concept is extended to the SEPIC converter to minimize the input ripple [68]. Recent developments into coupled inductors have seen emergence of twisted core coupled inductors, ultrathin coupled inductors and silicon embedded coreless coupled inductors [71]-[73]. LED drivers employing coupled inductors are widely used [12] [74] [75]. A multi-channel forward converter as an LED driver, using coupled inductors to improve cross-regulation is proposed in [59], while a coupled SEPIC topology is used in [74] and [75].

An LED driver using a coupled inductor cuk topology has not been proposed in literature so far. Extending the idea of using a coupled inductor cuk converter for LED driving purposes can have benefits such as higher efficiency and higher power density, aid in eliminating the output filtering capacitor and thereby achieve a compact low cost driver. Furthermore, the low output current ripple obtainable can aid in achieving high LED efficacy and maintain long LED lifetime. Figure 2.13 shows a coupled inductor; where M is the mutual inductance and k is the coupling coefficient [28].

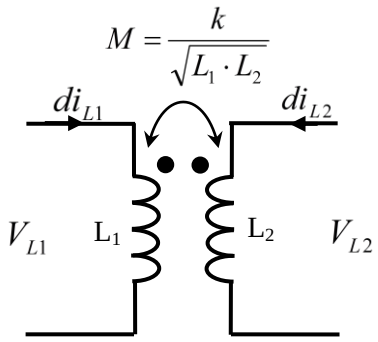


Figure 2.13: A coupled inductor.

A comprehensive study on the effect of coupling type, namely symmetric and non-symmetric coupling, and the effect of coupling coefficient, on the performance of a coupled inductor cuk converter has not been seen in literature yet. Such a study would enable identification of the best coupling type and coupling coefficient suitable for the coupled inductor cuk converter, to be applied as a high power LED driver.

2.6 OVERVIEW OF CURRENT MODE CONTROL METHODS AND CURRENT RIPPLE EFFECT ON LED LOAD EFFICACY AND LIFETIME

As seen in Section 2.1.1, LEDs are current devices whose light output is dependent on the forward current, where the small LED dynamic resistance requires accurate current control, to obtain a precise light level output. Therefore a suitable current control scheme is required. Widely used current control techniques seen in literature for LED drivers are linear current controllers, Peak Current Control (PCC), and Hysteretic Current Control (HCC), for switching converters [12] [33]-[35].

Linear current regulators achieve high regulation accuracy, but have the disadvantage of being highly inefficient, and are unsuitable for high power LED lighting [33]. In PCC, the switch current is sensed only when the switch is on, achieving inaccurate current control due to peak-to-average current error because current feedback information is not available when the switch is off [35] [36]. HCC improves the current control accuracy by sensing the load current both when the switch is on and off, and achieves better accuracy in comparison with PCC without requiring slope compensation [34]. PCC and HCC are simple, inexpensive compensators in the control loop [34] [35] [76]. Despite the advantages, PCC drawbacks are slope compensation requirement for duty cycles beyond 50%, sensitivity to noise and susceptance to sub-harmonic oscillation [36]. Although HCC seems to solve PCC issues such as slope compensation requirement, it results in higher power

dissipation compared to PCC if a resistive sensor is used, and is also prone to sub-harmonic oscillations [34] [37].

Average Current Control (ACC) is not widely used as compared to PCC and HCC for LED drivers, although its application is seen in [6] [64] [77]. In [12] it is found that ACC is complex and is unsuitable for low power low cost LED lighting due to the inclusion of a compensator in the control loop. In comparison to PCC and HCC, ACC has better noise immunity and slope compensation is not needed [36]. In addition, prevention of any sub-harmonic oscillation can be mitigated by proper current amplifier gain [36]. Although ACC requires a compensator in the feedback loop, it is worthwhile to consider it for high power LED applications, as it achieves excellent current accuracy with improved noise immunity. This can aid in achieving consistent light output from the high power LED load, and the improved noise immunity ACC provides can aid driver reliability.

Current ripple through the LEDs affects the LED performance. Increasing the peak-peak current ripple with the average current value maintained constant though the LEDs resulted in increased power dissipation due to thermal derating and junction heating which in turn causes depreciation of both the optical output and efficacy [26] [38]. Junction heat is one of the main factors affecting LED life, and operating the LED at high junction temperatures consequently reduces the LED optical output and lifetime [26]. In addition, accurate current control may also pose a challenge for drivers with high current ripple through the LED load [15]. Therefore, for high current accuracy, good LED efficacy and lifetime, the current ripple in the LEDs must be minimised.

2.7 OVERVIEW OF DIGITAL CONTROL FOR DC-DC CONVERTERS

Analogue based control has been the foremost and obvious choice for controlling high frequency dc-dc converters [29]. Due to developments in digital signal processing such as reducing cost and increased processor power (MIPS), real time digital control of high frequency switched mode power supplies is becoming popular because of numerous advantages they offer over traditional analogue based control [30].

Although analogue control provides low cost and simplicity, it however has disadvantages such as parameter sensitivity to factors such as ageing, drifting due to temperature differences and susceptibility to noise [78]. Furthermore, implementation of complex control schemes may not

always be possible using analogue controllers and are hence limited to simple controllers. Digital controllers on the other hand have various advantages such as better noise immunity, less susceptance to parameter variations (e.g. ageing and temperature variations) [31] [78]. In addition, because the control algorithm is in software form, digital controllers have the flexibility to implement complex control algorithms. During development, the software reprogrammability feature of the digital controllers allows for tuning of the desired controller without undertaking any hardware changes, as opposed to development using analogue controllers [31] [78].

The development environment used for development of the digital controller using a DSP (e.g Code Composer Studio from Texas Instruments [79] [80]) allows for observation of the control variables in real time, a powerful feature which aids in quick control algorithm development and fine tuning. Digital control also offers additional features such as communications and monitoring.

Despite these advantages, digital controllers are not without setbacks. Factors such as finite processor word length and the ADC quantization reduce signal resolution. In addition, despite high DSP MIPS now available, the control algorithm introduces a delay in the control loop. To mitigate this, techniques such as predictive dead beat, Smith Predictor and internal model control have been previously used [29]. Figure 2.14 shows a digitally controlled dc-dc converter [78].

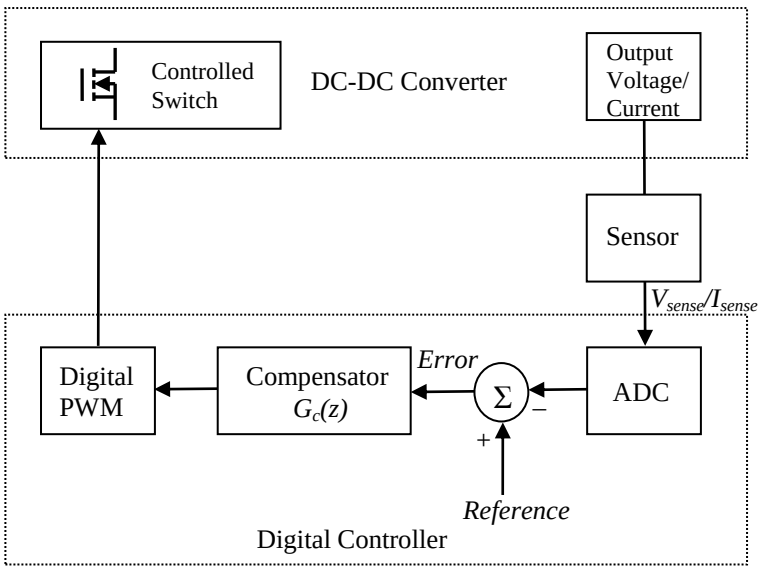


Fig 2.14: A simple representation of a digitally controlled dc-dc converter.

2.7.1 Digital PWM and ADC Resolution Effects

The digital PWM resolution of the digital controller is limited as it outputs the control signal in discrete steps. In addition to this, the ADC also converts the process output (sensed) signal into discrete values. The quantization effects of the digital PWM and the ADC may lead to a phenomenon known as limit cycling [29] [31]. This occurs when the control attempts to regulate the process output to the desired level, but due to the quantization error of the ADC, the ADC output is different from the actual value. Therefore the control algorithm acts to vary the control output (which is the digital PWM signal) to correct the error. Once this is done, the ADC then reads back a different value due to the quantization error, of which the control tries to correct again, and this process eventually leads to steady state oscillations. To prevent this, the digital PWM resolution has to be high enough, so that the smallest step change in the digital PWM output causes an even smaller change in the output quantity being sensed (voltage or current) [31] [81] [82].

2.7.2 Effect of Sampling and Computation Algorithm Time

Finite time delays are introduced into the control loop due to the computation algorithm and the sampling process. This delay is the time period between sampling and control output for one switching period. Consequently, the delay reduces the system phase-margin and the bandwidth, and as a result the transient response is diminished [79].

2.7.3 Digital Design Techniques

Controller design is done to achieve the process control objectives such as desired rise/settling-time, adequate bandwidth for satisfactory transient response and adequate phase-margin for satisfactory overshoot. [78]. Digital design has two common approaches, design by emulation and direct digital design [83]-[85]. These two methods are briefly discussed in the following Sections.

2.7.4 Digital Design by Emulation

In digital design by emulation, the compensation of the control plant is done in continuous time, ignoring any Zero Order Holds (ZOH) and sampler time delays in the control loop. The continuous time compensator is then converted into discrete time compensator using suitable conversion method [78]. Some discretization methods for converting from s-domain into z-domain are; bilinear transform, backward Euler, step invariant and pole-zero match [85].

Bilinear transform converts the entire left hand side s-plane into the unit circle in the z-plane. This has the advantage that it prevents aliasing effects. Furthermore, the controller gain and phase-margin are maintained, but only below $1/10^{th}$ of the sampling frequency. Step invariant transformation preserves step response, but the impulse and frequency response are diminished. The pole-zero method maintains the pole-zero locations, but this may give rise to aliasing errors if the zero frequencies are greater than twice the sampling frequency. The impulse and frequency response of the controller in s-domain are lost when using the backward euler method, despite its conversion simplicity [85].

The resulting discrete time compensator is then implemented as a difference Equation algorithm in the digital controller. The consequence of ignoring the ZOH and sampler time delays is that the resulting closed-loop system has reduced phase-margin. Therefore, the compensator should be designed to give the closed-loop system extra headroom for phase-margin to counter this effect. The main advantage of design by emulation is that the controller design is done in familiar continuous time domain [84].

2.7.5 Direct Digital Design

In the direct digital design method, the effect of ZOH and the sampler delay is included in the continuous time plant to be compensated. The sample and hold transfer-function in continuous time is given as [85];

$$ZOH(s) = \frac{(1 - e^{-sT_s})}{s} \tag{2.2}$$

The sampler time delay is given as [82];

$$T(s) = e^{-sT_d} \tag{2.3}$$

The continuous time uncompensated loop gain including the delays is given as [82];

$$T_{OL}(s) = \left(\frac{1 - e^{-sT_s}}{s} \right) \cdot e^{-sT_d} \cdot G_p(s) \cdot T_m(s) \cdot H(s) \tag{2.4}$$

where T_s is the sampling period, T_d is the sampler time delay, $G_p(s)$ is the continuous time plant, T_m is the PWM modulator gain and H is the feedback sensor and ADC gain. The resulting open loop gain $T_{OL}(s)$ is then transformed into discrete time using a suitable conversion method. Finally,

the discrete time plant is then compensated using the usual continuous time techniques such as the bode-plot or root locus method [84].

The advantage of this method is that the discretization of the plant included with the delays is more accurate and results in a better compensator design. Since the poles and zeros of the compensator are determined with more accuracy, this leads to a system with better bandwidth and phase-margin as compared to the design by emulation [78].

2.7.6 Digitally Controlled LED Drivers

Digitally controlled LED drivers have been previously proposed in [19] [37] [86]-[88]. In [86], a multi-phase buck with dimming via Ethernet communication was implemented. A simple hysteretic digital controller for a buck LED driver was proposed in [37]. Despite the simplicity, the controller introduced ripple through the LEDs due to sub-harmonic oscillations leading to flicker. A boost topology LED driver employing a DSPIC controller was proposed in [88], to demonstrate the viability of digital control. In [65], an offline LED driver using a non-isolated cuk converter was controlled using a HCC, implemented using a microcontroller. Although the control is simple, it is associated with the drawbacks of HCC and extreme duty ratios are observed. Fault-tolerant digitally controlled LED drivers are seen in [10] and [7].

2.8 THE PROPOSED LED DRIVER

A digitally controlled coupled inductor cuk converter with galvanic isolation is proposed. An investigation into the effects of coupling type and coupling coefficient of the coupled inductors, namely; non-symmetric coupling, symmetric coupling and no-coupling, on converter performance is to be done. This will identify the best coupling type and coupling coefficient to be used for the proposed LED driver based on the coupled inductor cuk converter.

A fault-tolerant feature is to be implemented using a suitable digital controller. The current in each string is sensed using a low cost, loss-less hall-effect current sensor. Their outputs are then seamlessly interfaced to the digital controller, and thereby the status of each string is determined by the control algorithm, and used in the computation of the current reference required. The load current required is then determined according to the number of strings connected, ensuring that the correct current flows through each connected load, regardless of whether the other strings are

connected or not. This fault-tolerant feature would maintain high driver efficiency, as the LED string current sensing is done in a lossless manner. The driver is to operate from a dc bus.

A novel concept of driving several low power LED loads using only a single LED driver is also proposed. Again, the use of digital control is used to add to the functionality of existing LED driver systems. Hence, the digital controller is used in conjunction with the lossless current sensors, to determine which LED load is switched on or off. Thus, similar to the fault-tolerant feature, the correct current flow into each load is ensured; regardless of whether the other loads are connected or not. This is achieved because the total load current reference is computed in real time by the control algorithm. The novel LED driver supplying several LED loads would reduce cost and simplify existing LED lighting system installations. For both the fault-tolerant LED driver and the multiple LED load driver, the dimming method chosen is amplitude mode. This is to ensure simplicity, low cost and maintenance of high LED dimming efficacy. Also, the current control method chosen is average current control, as it ensures accuracy and does not introduce sub-harmonic oscillations.

Also, use of the coupled inductors for the proposed LED driver can help in achieving high power density and obtain low cost and a compact LED driver. In addition, the low output current ripple obtainable by the coupled inductors can aid in eliminating the bulky output filtering capacitor, reducing component count and cost, and again aid in increasing the compactness of the driver. For the proposed driver, an output filtering capacitor is not used. Furthermore, the low output ripple obtainable due to the coupled inductors, can maintain high LED efficacy and LED lifetime. Finally, use of digital control can increase the LED driver flexibility such as future control algorithm updating and possibility of linking to a communication system for remote dimming monitoring and control.

Figure 2.15 shows a block diagram of the proposed LED driver, where S_{w1}-S_{wn} are the switches for the low power LED loads, which are also used to simulate and open-circuit fault for the high power LED driver; S_1-S_n are the hall-effect switches used for lossless current sensing and in_1-in_n are the input/output lines of the ports of digital controller. The input voltage to the converter is $V_{in,dc}$, obtained from a dc bus.

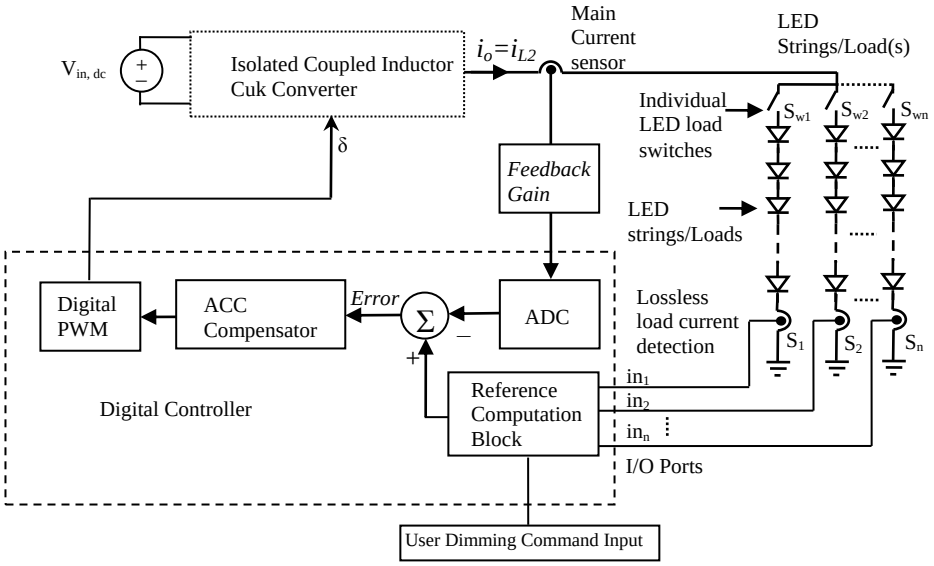


Figure 2.15: The proposed LED driver.

CHAPTER 3 MODELLING THE COUPLED CUK CONVERTER

A generalised coupled inductor model will be derived to aid in modelling the coupled cuk converter. Inductor coupling types namely Symmetric and Non-Symmetric coupling will also be briefly described in this Chapter. The coupled inductor cuk converter differential Equations are then derived and will be used to perform modelling using the state-space approach. The control-to-output inductor current transfer-function will be then derived, for use in designing a suitable current controller.

3.1 COUPLED INDUCTOR MODELLING

The well known transformer model can be extended to model coupled inductors as well [27]. Figure 3.1 shows a coupled inductor model.

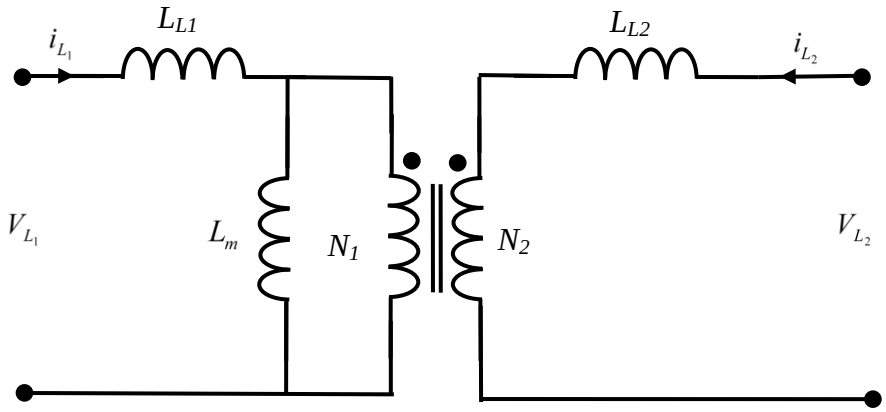


Figure 3.1: Coupled inductor equivalent circuit.

In Figure 3.1, N_1 and N_2 are the primary and secondary turns, L_{L1} and L_{L2} are the primary and secondary leakage inductances and L_m is the magnetizing inductance. Using the model, the coupled inductor voltage Equations can be written as [27];

$$V_{L_1} = L_1 \frac{di_{L_1}}{dt} + M \frac{di_{L_2}}{dt} \tag{3.1}$$

$$V_{L2} = M \frac{di_{L_1}}{dt} + L_2 \frac{di_{L_2}}{dt} \tag{3.2}$$

Where the mutual inductance *M* given as;

$$M = \frac{N_2}{N_1} L_m \tag{3.3}$$

Where the turns ratio *n* is defined as;

$$n = \frac{N_1}{N_2} \tag{3.4}$$

The total input inductance L_1 and output inductance L_2 are given as [27];

$$L_1 = L_{L_1} + n \cdot M \tag{3.5}$$

$$L_2 = L_{L_2} + \frac{1}{n} \cdot M \tag{3.6}$$

3.2 THE COUPLING COEFFICIENTS k_1 AND k_2 OF THE COUPLED INDUCTOR

In the coupled inductor, the flux generated by one winding is not fully coupled by the magnetic core and the other winding. Therefore, a coupling coefficient can be defined for each winding [92]. Figure 3.2 shows the coupled inductor windings and the generated flux [92].

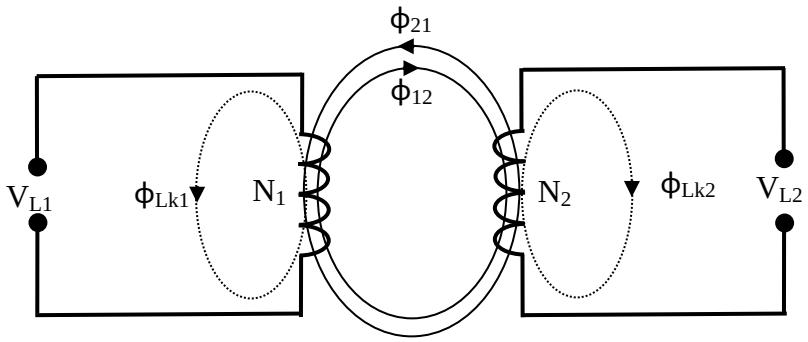


Figure 3.2: The coupled inductor windings and flux generation.

On the primary side, the total flux ϕ_{11} is given as [92];

$$\phi_{11} = \phi_{21} + \phi_{Lk_1} \tag{3.7}$$

Where ϕ_{21} the mutual is flux linkage of the primary winding and ϕ_{Lk_1} is the leakage flux due to the primary winding.On the secondary side, the total flux ϕ_{22} is given as [91];

$$\phi_{22} = \phi_{12} + \phi_{Lk_2} \tag{3.8}$$

Where ϕ_{12} is the mutual flux linkage of the secondary winding and ϕ_{Lk_2} is the leakage flux due to the secondary winding. The coupling coefficient of the primary winding is defined as [92];

$$k_1 = \frac{\phi_{21}}{\phi_{11}} \tag{3.9}$$

The coupling coefficient of the secondary winding can be defined as;

$$k_2 = \frac{\phi_{12}}{\phi_{22}} \tag{3.10}$$

In terms of the turns ratio and inductances, the individual coupling coefficients are defined as [92];

$$k_1 = n \cdot \frac{M}{L_1} \tag{3.11}$$

$$k_2 = \frac{1}{n} \cdot \frac{M}{L_2} \tag{3.12}$$

Finally, the combined coupling coefficient *k*, is given as [92];

$$k = \sqrt{k_1 \cdot k_2} = \frac{M}{\sqrt{L_1 \cdot L_2}} \tag{3.13}$$

3.3 COUPLED INDUCTOR TYPES

The types of coupling considered are namely Symmetrically Coupled (SC) inductors and Non-Symmetrically Coupled (NSC) inductors. As seen in Section 2.3.6.2, the voltage waveforms across the input and output inductors of the cuk converter are identical. This attribute leads to the possibility of using the current ripple steering technique to minimize ripple at the input or the output-side of the converter [91]. This ripple steering phenomenon is achieved using NSC inductors by adjustment of the coupling coefficient and the self inductances in a particular way to achieve the required ripple minimisation [91].

On the other hand, SC inductors achieve ripple reduction on both the input and output-side simultaneously, but do not achieve ripple minimisation to the levels as compared to NSC inductors [91]. Coupling the inductors on a common core reduces the magnetic component size, therefore coupled inductors are beneficial in reducing cost and increasing converter power density. A

detailed converter performance analysis is done in Chapter 5 to identify the best coupling method for the cuk converter as applied for LED driving.

3.3.1 Symmetrically Coupled Inductor

For an inductor to be symmetrically coupled, the leakage inductances on the input-side L_{L1} and the output-side L_{L2} are to be equal. Thus the output inductor L_2 and the mutual inductance M are given as;

$$L_2 = \frac{L_1}{n^2} \tag{3.14}$$

$$M = \frac{k \cdot L_1}{n} \tag{3.15}$$

3.3.2 Non-Symmetrically Coupled Inductor

When the leakage inductances L_{L1} and L_{L2} are not equal, the inductor is non-symmetrically coupled. In addition, the input or output-side current ripple can be minimised by steering the ripple to the output or input-side respectively. This phenomenon of ripple steering was first proposed in [28]. For current ripple minimisation at the output-side, the following conditions must be satisfied;

$$L_2 = \frac{L_1}{k^2 \cdot n^2} \tag{3.16}$$

$$M = \frac{L_1}{n} \tag{3.17}$$

For current ripple minimization at the input-side, the following condition is to be satisfied;

$$M = L_2 \cdot n \tag{3.18}$$

$$L_1 = L_2 \cdot k^2 \cdot n^2 \tag{3.19}$$

3.4 ANALYSIS OF THE ISOLATED COUPLED CUK CONVERTER

3.4.1 Isolated Cuk Converter Transformation to a Non-Isolated Equivalent

For differential Equation derivation and circuit analysis, it is simpler to transform the isolated converter in Figure 3.3 to an equivalent non-isolated circuit as shown in Figure 3.4, by reflecting the components on the secondary side to the primary side using the turns ratio while maintaining

power invariance. The magnetising inductance L_m of the isolation transformer is included in the circuit. The components are assumed to be ideal for simplicity.

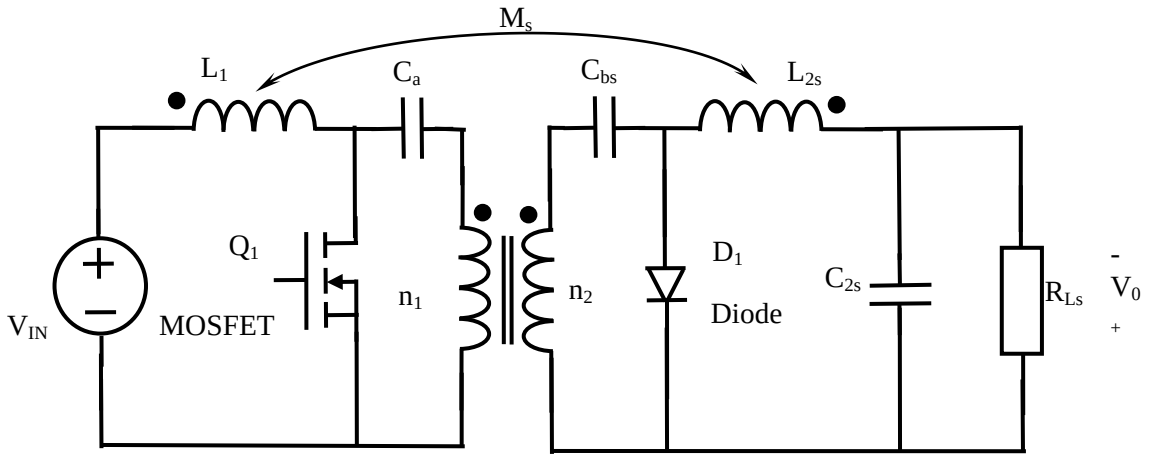


Figure 3.3: The isolated coupled cuk converter.

The secondary side components are reflected to the primary side as follows, where n is the turns ratio and M_s is the mutual inductance of the coupled inductors for the isolated converter;

$$C_2 = \frac{C_{2s}}{n^2} \tag{3.20}$$

$$C_b = \frac{C_{bs}}{n^2} \tag{3.21}$$

$$L_2 = L_{2s} \cdot n^2 \tag{3.22}$$

$$R_L = R_{L_s} \cdot n^2 \tag{3.23}$$

$$M = \frac{M_s}{n} \tag{3.24}$$

$$n = \frac{n_1}{n_2} \tag{3.25}$$

The non-isolated cuk converter differential Equations are derived for the interval when the switch is on, δT_s and when the switch is off, $(1-\delta)T_s$.

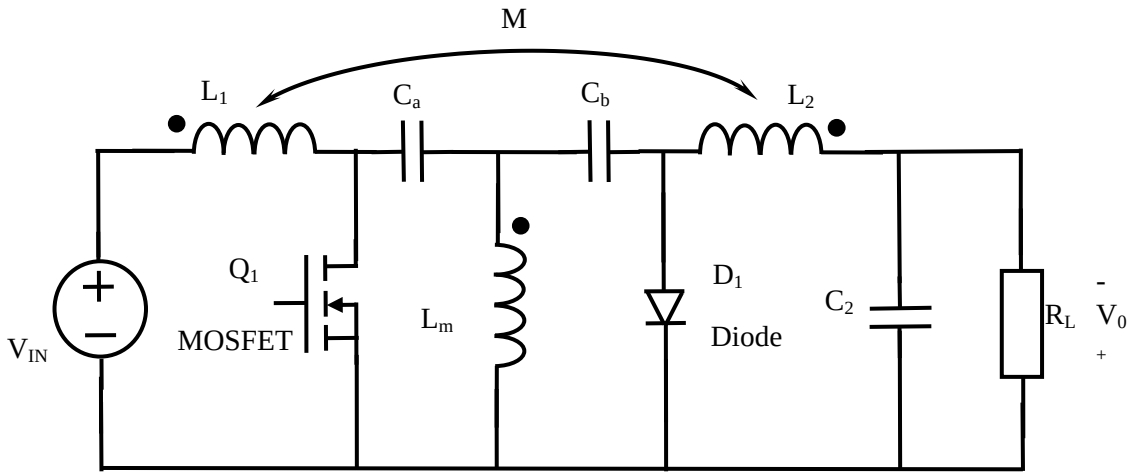


Figure 3.4: The non-isolated cuk converter equivalent with L_m.

3.4.2 When the Switch Q_1 is On

Figure 3.5 circuit shows the node currents and branch voltages of the converter when the switch Q_1, is on.

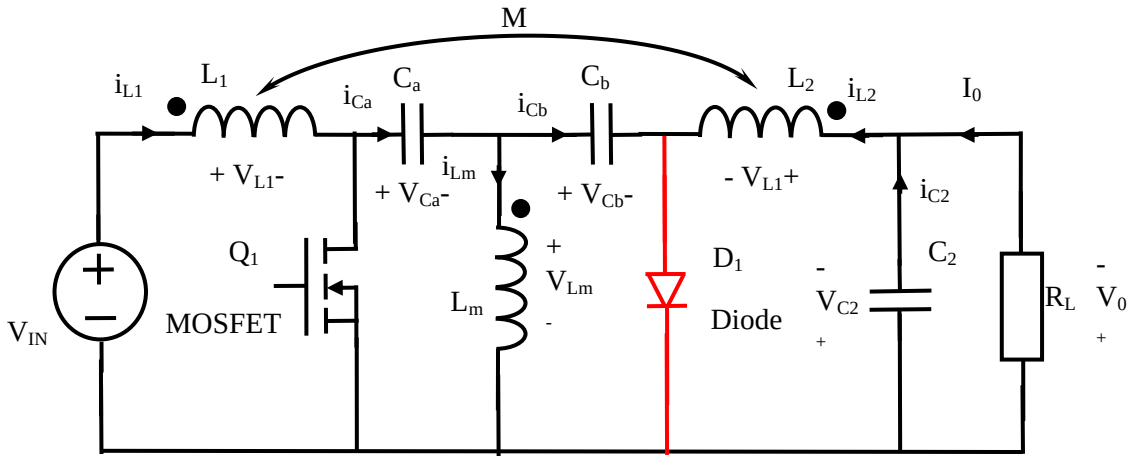


Figure 3.5: Node currents and branch voltages of the converter when the switch Q_1 is on.

The differential Equations are obtained when the switch is on as;

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} \tag{3.26}$$

$$\frac{di_{Lm}}{dt} = \frac{-Vc_a}{L_m} \tag{3.27}$$

$$\frac{di_{L2}}{dt} = \frac{Vc_b}{L_2} + \frac{Vc_a}{L_2} - \frac{Vc_2}{L_2} \tag{3.28}$$

$$\frac{dVc_a}{dt} = \frac{i_{Lm}}{C_a} - \frac{i_{L2}}{C_a} \tag{3.29}$$

$$\frac{dVc_b}{dt} = \frac{-i_{L2}}{C_b} \tag{3.30}$$

$$\frac{dVc_2}{dt} = \frac{i_{L2}}{C_2} - \frac{Vc_2}{RC_2} \tag{3.31}$$

3.4.3 When the Switch Q_1 is Off,

Figure 3.6 shows the node currents and branch voltages when the switch Q_1 is off.

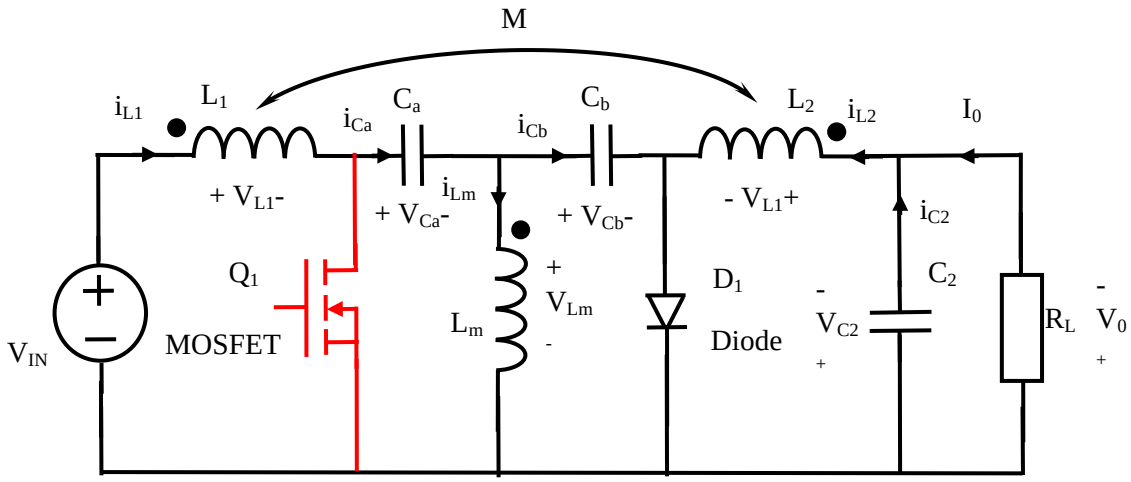


Figure 3.6: Node currents and branch voltages of the converter when the switch Q_1 is off.

The differential Equations are obtained when the switch is off as;

$$\frac{di_{L_1}}{dt} = \frac{V_{in}}{L_1} - \frac{Vc_a}{L_1} - \frac{Vc_b}{L_1} \tag{3.32}$$

$$\frac{di_{Lm}}{dt} = \frac{Vc_b}{L_m} \tag{3.33}$$

$$\frac{di_{L2}}{dt} = -\frac{Vc_2}{L_2} \tag{3.34}$$

$$\frac{dVc_a}{dt} = \frac{i_{L1}}{C_a} \tag{3.35}$$

$$\frac{dVc_b}{dt} = \frac{i_{L1}}{C_b} - \frac{i_{Lm}}{C_b} \tag{3.36}$$

$$\frac{dVc_2}{dt} = \frac{i_{L2}}{C_2} - \frac{Vc_2}{RC_2} \tag{3.37}$$

3.4.4 Solution of the Coupled Inductor Rate of Change of Current

The coupled inductors rate of change of current $\frac{di_{L1}}{dt}$ and $\frac{di_{L2}}{dt}$ are obtained as follows;

$$\frac{di_{L1}}{dt} = \frac{L_2}{\alpha}V_{L1} + \frac{-M}{\alpha}V_{L2} \tag{3.38}$$

$$\frac{di_{L2}}{dt} = \frac{-M}{\alpha}V_{L1} + \frac{L_1}{\alpha}V_{L2} \tag{3.39}$$

Where α is given as $L_1L_2 - M^2$. This solution needs the individual inductor voltages V_{L1} and V_{L2} to be determined for the intervals δT_s and $(1-\delta)T_s$, so that it can be fully solved. For the period δT_s when the switch is on, the inductor voltages are determined as follows;

$$V_{L1} = V_{in} \tag{3.40}$$

$$V_{L2} = V_{Cb} + V_{Ca} - V_{C2} \tag{3.40}$$

For the period $(1-\delta)T_s$ when the switch is off, the inductor voltages are;

$$V_{L1} = V_{in} - V_{Ca} - V_{Cb} \tag{3.42}$$

$$V_{L2} = -V_{C2} \tag{3.43}$$

Using the above found solutions of the coupled inductor voltages, the differential Equations of the coupled inductors are re-written for the intervals δT_s and $(1-\delta)T_s$. For the period δT_s the final coupled inductor rate of change of current solutions are;

$$\frac{di_{L_1}}{dt} = \frac{L_2}{\alpha}V_{in} + \frac{-M}{\alpha}\left(V_{Cb} + V_{Ca} - V_{C2}\right) \tag{3.44}$$

$$\frac{di_{L_2}}{dt} = \frac{-M}{\alpha} V_{in} + \frac{L_1}{\alpha}\left(V_{Cb} + V_{Ca} - V_{C2}\right) \tag{3.45}$$

For the period $(1-\delta)T_s$, the final coupled inductor rate of change of current solutions are;

$$\frac{di_{L1}}{dt} = \frac{L_2}{\alpha}\left(V_{in} - V_{Ca} - V_{Cb}\right) + \frac{-M}{\alpha}\left(-V_{C2}\right) \tag{3.46}$$

$$\frac{di_{L2}}{dt} = \frac{-M}{\alpha}\left(V_{in} - V_{Ca} - V_{Cb}\right) + \frac{L_1}{\alpha}\left(-V_{C2}\right) \tag{3.47}$$

3.4.5 Final Forms of the Converter Differential Equations

The final forms of the differential Equations that fully describe the converter operation are now established for the periods δT_s and $(1-\delta)T_s$. When the switch is on (δT_s), the applicable differential Equations are;

$$\frac{di_{L_1}}{dt} = \frac{L_2}{\alpha} V_{in} + \frac{-M}{\alpha}\left(V_{Ca} + V_{Cb} - V_{C2}\right) \tag{3.48}$$

$$\frac{di_{L_m}}{dt} = \frac{-Vc_a}{L_m} \tag{3.49}$$

$$\frac{di_{L_2}}{dt} = \frac{-M}{\alpha} V_{in} + \frac{L_1}{\alpha}\left(V_{Ca} + V_{Cb} - V_{C2}\right) \tag{3.50}$$

$$\frac{dVc_a}{dt} = \frac{i_{Lm}}{C_a} - \frac{i_{L2}}{C_a} \tag{3.51}$$

$$\frac{dVc_b}{dt} = \frac{-i_{L2}}{C_b} \tag{3.52}$$

$$\frac{dVc_2}{dt} = \frac{i_{L2}}{C_2} - \frac{Vc_2}{RC_2} \tag{3.53}$$

When the switch is off, $(1-\delta)T_s$, the applicable differential Equations are;

$$\frac{di_{L_1}}{dt} = \frac{L_2}{\alpha}\left(V_{in} - V_{Ca} - V_{Cb}\right) + \frac{-M}{\alpha}\left(-V_{C2}\right) \tag{3.54}$$

$$\frac{di_{L_m}}{dt} = \frac{-Vc_b}{L_m} \tag{3.55}$$

$$\frac{di_{L_2}}{dt} = \frac{-M}{\alpha}\left(V_{in} - V_{Ca} - V_{Cb}\right) + \frac{L_1}{\alpha}\left(-V_{C2}\right) \tag{3.56}$$

$$\frac{dVc_a}{dt} = \frac{i_{L1}}{C_a} \tag{3.57}$$

$$\frac{dVc_b}{dt} = \frac{iL_1}{C_b} - \frac{iL_m}{C_b} \tag{3.58}$$

$$\frac{dVc_2}{dt} = \frac{iL_2}{C_2} - \frac{Vc_2}{RC_2} \tag{3.59}$$

3.5 MODELLING OF THE COUPLED INDUCTOR CUK CONVERTER

In this Section, using the converter differential Equations derived in Section 3.4, the coupled cuk converter will be modelled by averaging the differential Equations using the duty ratio as the weight [93]. This will result in the determination of the transfer-functions which will be used to design a suitable controller. The state-space averaging approach is used.

3.5.1 Modelling Using the State-space Approach

To use the state-space approach [27], the differential Equations derived in Section 3.4, are written in matrix form. For the period δT_s, the matrix is;

$$\begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_m}}{dt} \\ \frac{di_{L_2}}{dt} \\ \frac{dVc_a}{dt} \\ \frac{dVc_b}{dt} \\ \frac{dVc_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-M}{\alpha} & \frac{-M}{\alpha} & \frac{M}{\alpha} \\ 0 & 0 & 0 & \frac{-1}{L_m} & 0 & 0 \\ 0 & 0 & 0 & \frac{L_1}{\alpha} & \frac{L_1}{\alpha} & \frac{-L_1}{\alpha} \\ 0 & \frac{1}{C_a} & \frac{-1}{C_a} & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_b} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{Lm} \\ i_{L2} \\ V_{Ca} \\ V_{Cb} \\ V_{C2} \end{bmatrix} + \begin{bmatrix} \frac{L_2}{\alpha} \\ \frac{-M}{\alpha} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_{in} \end{bmatrix} \tag{3.60}$$

In state-space representation, Equation (3.60) is written as [27];

$$\begin{bmatrix} \dot{x} \end{bmatrix} = \begin{bmatrix} A_1 \end{bmatrix} \begin{bmatrix} x \end{bmatrix} + \begin{bmatrix} B_1 \end{bmatrix} \begin{bmatrix} u \end{bmatrix} \tag{3.61}$$

Where $[x]$ is the state variable vector, $[\dot{x}]$ is the first order differential of the state-vector with respect to time, $[A_1]$ and $[B_1]$ are the state matrices, and $[u]$ is the input. The output y is given as [93];

$$y = [C_1][x] + [E_1][u] \tag{3.62}$$

With C_1 and E_1 state matrices given as [93];

$$C_1 = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1] \tag{3.63}$$

$$E_1 = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0] \tag{3.64}$$

The output y is re-written as;

$$y = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1]\begin{bmatrix} i_{L1} \\ i_{Lm} \\ i_{L2} \\ V_{Ca} \\ V_{Cb} \\ V_{C2} \end{bmatrix} + [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0][V_{in}] \tag{3.65}$$

For the period $(1-\delta)T_s$, the differential Equations obtained are given in matrix form as;

$$\begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_m}}{dt} \\ \frac{di_{L_2}}{dt} \\ \frac{dVc_a}{dt} \\ \frac{dVc_b}{dt} \\ \frac{dVc_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-L_2}{\alpha} & \frac{-L_2}{\alpha} & \frac{M}{\alpha} \\ 0 & 0 & 0 & 0 & \frac{1}{L_m} & 0 \\ 0 & 0 & 0 & \frac{M}{\alpha} & \frac{M}{\alpha} & \frac{-L_1}{\alpha} \\ \frac{1}{C_a} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_b} & \frac{-1}{C_b} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{Lm} \\ i_{L2} \\ V_{Ca} \\ V_{Cb} \\ V_{C2} \end{bmatrix} + \begin{bmatrix} \frac{L_2}{\alpha} \\ \frac{-M}{\alpha} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}] \tag{3.66}$$

In state-space representation, Equation (3.66) is written in the form [27];

$$[\dot{x}] = [A_2][x] + [B_2][u] \tag{3.67}$$

The output for the interval $(1-d)T_s$ is represented as [93];

$$y = [C_2][x] + [E_2][u] \tag{3.68}$$

With C_2 and E_2 given as [93];

$$C_2 = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1] \tag{3.69}$$

$$E_2 = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0] \tag{3.70}$$

The output y is re-written as;

$$y = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1]\begin{bmatrix} i_{L1} \\ i_{Lm} \\ i_{L2} \\ V_{Ca} \\ V_{Cb} \\ V_{C2} \end{bmatrix} + [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0][V_{in}] \tag{3.71}$$

Averaging the state matrices using the duty ratio as the weight is done as follows [93];

$$A = A_1 D + A_2(1-D) \tag{3.72}$$

$$B = B_1 D + B_2(1-D) \tag{3.73}$$

$$C = C_1 D + C_2(1-D) \tag{3.74}$$

$$E = E_1 D + E_2(1-D) \tag{3.75}$$

Finally, linearization is performed by perturbing the state-vector and duty ratio, the ac and dc components can be separated, while ignoring the non-linear terms. The linearized state-vector is rewritten as follows [93];

$$\left[X + \tilde{x}\right] = \left[(D + \tilde{\delta})A_1 + (1 - D - \tilde{\delta})A_2\right]\left[X + \tilde{x}\right] + \left[(D + \tilde{\delta})B_1 + (1 - D - \tilde{\delta})B_2\right]\left[U + \tilde{u}\right] \tag{3.76}$$

The linearized output is given as [93];

$$\left[Y + \tilde{y}\right] = \left[(D + \tilde{\delta})C_1 + (1 - D - \tilde{\delta})C_2\right]\left[X + \tilde{x}\right] + \left[(D + \tilde{\delta})E_1 + (1 - D - \tilde{\delta})E_2\right]\left[U + \tilde{u}\right] \tag{3.77}$$

The steady state state-vector is given as;

$$X = -A^{-1}BU \tag{3.78}$$

While the dc terms are given as follows;

$$0 = AX + BU \tag{3.79}$$

$$Y = (-CA^{-1}B + E)U \tag{3.80}$$

The ac components of the state-vector are given as [93];

$$\begin{bmatrix} L_1 \\ L_m \\ L_2 \\ C_a \\ C_b \\ C_2 \end{bmatrix} \begin{bmatrix} \tilde{\cdot} \\ \tilde{x} \end{bmatrix} = A\tilde{x} + B\tilde{u} + \{[A_1 - A_2]X + [B_1 - B_2]U\}\tilde{\delta} \tag{3.81}$$

The ac components of the output vector are given as [93];

$$\begin{bmatrix} \tilde{\cdot} \\ \tilde{y} \end{bmatrix} = C\tilde{x} + E\tilde{u} + \{[C_1 - C_2]X + [E_1 - E_2]U\}\tilde{\delta} \tag{3.82}$$

Where;

$$\tilde{x} = \begin{bmatrix} \tilde{i}_{L1} \\ \tilde{i}_{Lm} \\ \tilde{i}_{L2} \\ \tilde{v}_{ca} \\ \tilde{v}_{cb} \\ \tilde{v}_{c2} \end{bmatrix} \tag{3.83}$$

$$\tilde{u} = \begin{bmatrix} \tilde{v}_{in} \end{bmatrix} \tag{3.84}$$

3.5.2 The Small Signal Transfer-Functions of the Isolated Coupled Cuk Converter

The duty to output and source to output transfer-functions are obtained by taking the Laplace transform of the ac terms obtained in Section 3.5.1 and is given as;

$$\begin{aligned} \tilde{v}_0(s) = &\{C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)u] + [(C_1 - C_2)X + (E_1 - E_2)u]\}\tilde{\delta}(s) \\ &+ \{C[sI - A]^{-1}B + E\}\tilde{u}(s) \end{aligned} \tag{3.85}$$

$$G_{v_o\delta}(s)\big|_{u(s)=0} = C[sI-A]^{-1}[(A_1-A_2)X+(B_1-B_2)u]+[(C_1-C_2)X+(E_1-E_2)u] \quad (3.86)$$

$$G_{v_o v_{in}}(s)\big|_{\delta(s)=0} = C[sI-A]^{-1}B+E \quad (3.87)$$

The ac duty to state and source to state transfer-functions are also obtained by taking the Laplace transform of the small signal components and are written as;

$$\begin{aligned}\tilde{x}(s) = &\left\{[sI-A]^{-1}[(A_1-A_2)X+(B_1-B_2)u]+[(C_1-C_2)X+(E_1-E_2)u]\right\}\tilde{\delta}(s)\\ &+\left\{[sI-A]^{-1}B+E\right\}\tilde{u}(s)\end{aligned} \quad (3.88)$$

$$G_{x\delta}(s)\big|_{u(s)=0} = [sI-A]^{-1}[(A_1-A_2)X+(B_1-B_2)u]+[(C_1-C_2)X+(E_1-E_2)u] \quad (3.89)$$

$$G_{xv_{in}}(s)\big|_{\delta(s)=0} = [sI-A]^{-1}B+E \quad (3.90)$$

Where $[I]$ is given as an identity matrix. The derived control-to-output transfer-functions are given in appendix A.

3.6 CHAPTER CONCLUSION

A generalised coupled inductor model, applicable for both SC and NSC inductors was derived. Analysis of the coupled inductor cuk converter was then done, and the various differential Equations required for modelling were obtained. The coupled inductor cuk converter was then modelled using the classical state-space approach. The control-to-output transfer functions were derived. The effects of coupling coefficient and coupling type for SC and NSC inductors are compared with Non-Coupled inductors later in Section 6.1.

CHAPTER 4 CONVERTER DESIGN AND COMPONENTS SIZING

LED load design is undertaken and a single high power LED load and several low power LED loads are simultaneously designed, by selecting the appropriate series-parallel string combination. Effect of temperature on the LED current and voltage characteristics is investigated, and forced cooling is adopted to keep the LED junction temperature in an acceptable range. Accurate dynamic resistance modelling for the LED loads is derived from the practically measured I-V curves. The required dimming levels are then selected. The operating parameters of the LED driver are chosen; based on an isolated cuk converter whose input dc voltage is 280-380 V. The switching frequency and the isolation transformer turns ratio are selected.

NC, NSC and SC inductors are also designed in this Chapter, for an investigation of coupling type on converter performance. The isolation transformer is then designed and the coupling capacitors are sized and selected. Also, the MOSFET switch and diode are sized and selected. Finally, a snubber circuit is designed to clamp voltage spikes across the switch, due to the isolation transformer primary side leakage inductance.

4.1 LED LOAD DESIGN

A single high power LED load with several strings, and one with several low power LED loads are designed simultaneously in this Section. This design is undertaken for a driver, which can; (i) detect the number of open strings in the high power load (ii) detect which low power load is connected/disconnected, and recalculate the control current reference in real time so that an accurate current is fed to the remaining connected strings/loads. The selected high power LED is the LCW W5AM [94]. It has a maximum forward current I_{fmax} of 1000 mA at a forward voltage V_f of 3.6 V at 25°C.

4.1.1 Single High Power LED load

The total LED load wattage P_{TOT} is selected as 90W at 25°C, although this Figure will reduce with increase in temperature as will be seen in the following Section. The forward current I_f for an individual LED is to be operated at 85% of I_{fmax} which is 850 mA, where the forward voltage V_f is

obtained as 3.53 V at 25°C from the LED datasheet. The power consumption of a single LED is then obtained as;

$$P_{LED} = I_f \cdot V_f = 850\,\text{mA} \times 3.53\,\text{V} = 3\,\text{W} \tag{4.1}$$

The total number of LEDs q_{TOT}, is determined as;

$$q_{TOT} = \frac{P_{TOT}}{P_{LED}} = \frac{90\,\text{W}}{3\,\text{W}} = 30\,\text{LEDs} \tag{4.2}$$

4.1.2 Selection of the LED Series-Parallel String Combination

Choosing a single high power string would result in a high LED string voltage, requiring the driver to meet this high output voltage requirement [8]. This has the impact of increasing the voltage stress across the driver switch, forcing the selection of a switch with high blocking voltage. In addition, in case of an open-circuit failure of any of the LEDs, the whole string would fail [10], unless a means to bypass the faulty LED is provided. On the other hand, several parallel LED strings would result in a low total load voltage and a significantly high total string current [6]. In regard to the driver, very low output voltage would result in an extremely small duty ratio if a high input voltage is used, which is difficult to achieve in practice. For an isolated driver, a large number of turns on the secondary side of the isolation transformer are needed. This increases the copper losses in the isolation transformer [27], which impacts driver efficiency negatively. An advantage of using several parallel strings is that if one string were to have an open-circuit failure, the other connected strings provide continued operation. Considerations of the afore-mentioned factors lead to an appropriate series-parallel string combination, that guide the selection of an appropriate LED load string voltage and current that matches and optimises the driver operation. Table 4.1 illustrates different series-parallel configurations and the effect on the string currents and voltages at 25°C for the selected LED. The total rated power is 90 W, while the total number of LEDs is 30.

Table 4.1: Various series-parallel combinations and the LED string currents and voltages at 25°C.

No. of Parallel Strings	1	2	3	5	6
No. of LEDs per String	30	15	10	6	5
Current per String (*A*)	0.85	0.85	0.85	0.85	0.85
Total LED Load Current (*A*)	0.85	1.70	2.550	4.25	5.1
LED String Voltage (*V*)	105.9	52.95	35.3	21.18	17.65

For the design, an LED load with three parallel strings is selected which has a total load voltage and current of 35.3 V and 2.55 A respectively. In case of an open-circuit failure of one string, the other two connected loads would still be usable. For continued operation, the driver controller detects the open string and reduces the output power to match the power of the remaining connected loads. Therefore the power for one string is 30 W, for 2 strings it is 60 W and for 3 strings it is 90 W. The output voltage and current specifications of the isolated driver/converter can be chosen as per the selected LED load specification.

4.1.3 Several Low Power LED Loads

To test the concept of a single high power LED driver supplying several, low power LED loads which can be individually switched on or off, are needed. From the design of the high power LED load seen in Section 4.1.1, the three parallel strings designed will be implemented as three individual LED loads, with each load having a power of 30 W. Hence the driver control system senses connected/disconnected loads, and adjusts the output current accordingly so that the operation of the connected loads is not interrupted and negatively affected.

4.1.4 Effect of Temperature Rise on the High Power LED Load Voltage and Current

The designed LED load was practically implemented and tested to demonstrate the effect of temperature rise on the string voltage and current. The LEDs were mounted on a heatsink, and two scenarios were tested; with forced cooling (which the LED load was designed for) and without forced cooling at an ambient temperature of 26°C. Initially, the LED load current was driven at a current of 2.6 A, and the heatsink temperature for both scenarios was monitored until steady state value. Forced cooling maintained the heatsink temperature at 38°C while the non-forced cooling maintained a heatsink temperature of 70°C. The voltage and current measurements were then taken as the current was gradually reduced. The current and voltage characteristics of the two heatsink temperatures are plotted in Figure 4.2. The 25°C curve is obtained from the datasheet [94].

From Figure 4.2, as the temperature increases, it is seen that the LED load voltage drops at the particular desired operating current of 2.55 A. At the constant total load current of 2.55 A, the following observations are made; at a heatsink temperature of 25°C, the high power LED load voltage, power and dynamic resistance are 35.3 V, 90 W, and 13.84 Ω respectively; at a heatsink temperature of 38°C, the high power LED load voltage, power and dynamic resistance are 34.71 V, 88.5 W, and 13.61 Ω respectively; at a heatsink temperature of 70°C, the high power LED load

voltage, power and dynamic resistance are 33.9 V, 86.45 W, and 13.29 Ω respectively. Although the LED driver is to be designed to drive a load of 90 W at 25°C, the practical constraint of temperature rise reduces this value by 1.51 W at 38°C and 3.55 W at 70°C.

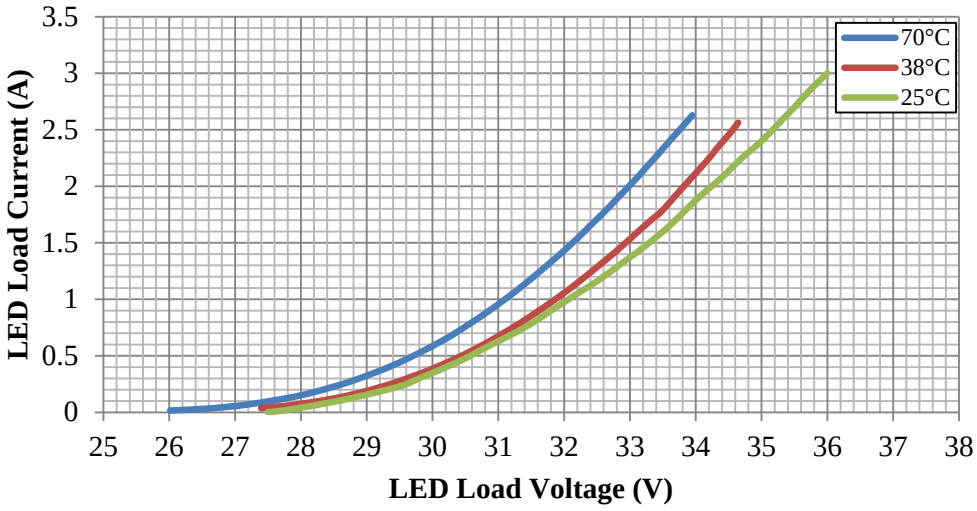


Figure 4.2: The LED load voltage and current characteristics for various temperatures.

4.1.5 The LED Junction Temperature T_j

The operating junction temperature T_j of the LEDs must be determined so as not to exceed the maximum junction temperature $T_{j,max}$ of 125°C. To determine T_j, the LED array thermal model in Figure 4.3 is used, similar to [95], where $R_{\theta j\text{-}case}$ is the thermal resistance from the junction to the LED casing, $R_{\theta case\text{-}pcb}$ is the thermal resistance from the case to the thermal PCB, $R_{\theta pcb\text{-}sink}$ is the thermal resistance from thermal PCB to the heatsink, $R_{\theta pcb\text{-}sink}$ is the thermal resistance from thermal PCB to the heatsink and $R_{\theta sink\text{-}amb}$ is the thermal resistance from heatsink to ambient air. The thermal resistance from the junction to the heatsink ($R_{\theta j\text{-}sink}$) is given by [95];

$$R_{\theta j-sink} = R_{\theta j-case} + R_{\theta case-pcb} + R_{\theta pcb-sink} \tag{4.3}$$

Since all the LEDs are mounted on a single heatsink, the total thermal resistance from the junction to the heatsink $R_{\theta j\text{-}sink,\,TOT}$ is found by the parallel combination of the individual $R_{\theta j\text{-}sink}$ contributed by each LED. Therefore $R_{\theta j\text{-}sink,\,TOT}$ is given by [95];

$$R_{\theta j-sink,TOT} = \frac{R_{\theta j-sink}}{q_{TOT}} \tag{4.4}$$

The junction to ambient thermal resistance $R_{\theta j-amb}$, is given as [54];

$$R_{\theta j-amb} = R_{\theta j-sink,TOT} + R_{\theta sink-amb} \tag{4.5}$$

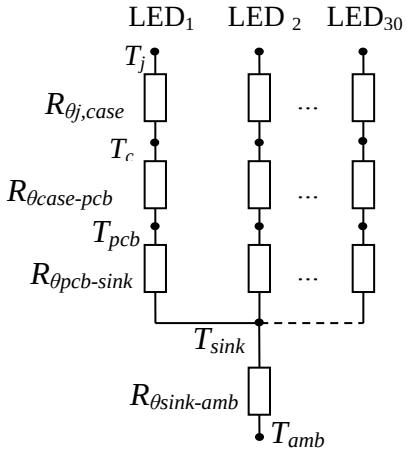


Figure 4.3: The LED array thermal model.

Finally, the LED junction temperature T_j, is found as [54];

$$T_j = T_{amb} + P_{diss} \cdot R_{\theta j-amb} \tag{4.6}$$

From the LED datasheet [94], the thermal PCB datasheet [96] and the heatsink datasheet [97], the various thermal impedances are given as; $R_{\theta j-case}$ = 6.5°C/W, $R_{\theta case-pcb}$ = 0.4°C/W, $R_{\theta pcb-sink}$ = 0.769°C/W, $R_{\theta sink-amb,CONV.}$ = 1.2°C/W, $R_{\theta sink-amb,FORCED}$ = 0.67°C/W. From Table 4.2, the power dissipation (P_{diss}) at heatsink temperatures 38°C and at 70°C is given as 88.49 W and 86.45W respectively. At the heatsink temperature 70°C, using the $R_{\theta sink-amb,CONV.}$, $R_{\theta j-amb}$ is obtained using Equations (4.3), (4.4) and (4.5);

$$R_{\theta j-amb} = 0.2556\,°C/W + 1.39\,°C/W = 1.6456\,°C/W \tag{4.7}$$

T_j for convectional cooling is obtained from (4.6) for T_{amb} of 26 °C as;

$$T_j = 26\,°C + (86.45\,W \times 1.6456\,°C/W) = 168.26\,°C \tag{4.8}$$

At the heatsink temperature of 38°C, using $R_{\theta sink-amb,FORCED}$, $R_{\theta j-amb}$ is obtained as;

$$R_{\theta j-amb} = 0.2556\,°C/W + 0.67\ °C/W = 0.9256\,°C/W \tag{4.9}$$

T_j for forced cooling is found as;

$$T_j = 26\,°C + (88.49\,W \times 0.9256\,°C/W) = 107.9\,°C \tag{4.10}$$

For convectional cooling, T_j is seen to be above $T_{j,max}$ by 43.25°C. Operating the LEDs with a higher T_j than recommended by the manufacturer will result in degradation of performance such as colour shifting and short operating lifetime, and therefore convectional cooling in this case is not recommended. When forced cooling is used, T_j is below $T_{j,max}$ by a good safety margin of 17.1°C. This ensures long LED lifetime and good lumen maintenance and allows a maximum T_{amb} of 43°C.

Although forced cooling adds extra power requirements, the heatsink which was used was the only one available at hand (which for forced cooling has a thermal impedance of 1.2°C/W), forced cooling will be adopted for the LED load so as to maintain the heatsink temperature at 38°C at an ambient temperature of 26°C. Therefore the LED driver current controller must regulate the load current constantly at 2.55 A from start up, when the heatsink temperature rises from 25°C to the steady state temperature of 38°C. This implies that the load power will reduce from 90 W to 88.49 W.

4.1.6 The Accurate LED Load Dynamic Resistance Model

An accurate model for the dynamic resistance can be derived from the I-V curves in Figure 4.2. The dynamic resistance varies in a manner that follows the inverse power law. Only the heatsink temperature of 38°C is considered, as this is the operating condition chosen. The dynamic resistance of the high power LED load R_D can be described using a power law curve fitting method. MS Excel was used to obtain Equation (4.11) and (4.12), of which the regression factor is 0.9999.

$$R_D = 32.144 \cdot I_{LOAD}^{-0.918}\ \Omega \tag{4.11}$$

For a single low power LED load, the dynamic resistance $R_{D,L}$, is given as;

$$R_{D,L} = 96.432 \cdot I_{LOAD}^{-0.918}\ \Omega \tag{4.12}$$

4.2 DIMMING LEVELS OF THE LED LOAD

Dimming is necessary for energy saving purposes. Since the optical output varies almost linearly [94] when performing dimming using AM, the load current will be reduced in the same proportion to achieve the dimming effect. In [98], the lighting level required for industrial lighting is 300 Lux. Considering an area of 8m^2, the minimum lumen output requirement is ~2500 Lm for the high power LED load. Similarly, for domestic use, the minimum light level required is 300 Lux [98].

Thereby a single low power LED load can light an area of 2.7m^2 at the minimum 300 Lux requirement.

For 0% dimming, the total light output is 4135.8 Lm and 1378.6 Lm for the high power LED load and the low power LED load (1 string) respectively. The minimum lumen output required is ~2500 Lm and ~833 Lm for the high power LED and low power LED loads respectively. This corresponds to a dimming level of 50%, and hence this is the lowest dimming level that is adopted. Table 4.2 shows the load power and lumen output of a single high power LED load, and the low power LED load. The temperature is 38°C. The Lumen output is obtained from the datasheet [94].

Table 4.2: Dimming levels and lumen output at casing temperature 38°C

Load Type	**Single High Power LED load**			**Single Low Power LED load**		
Dimming Level %	I_{LOAD} (A)	Lumen (Lm)	P_{LOAD} (W)	I_{LOAD} (A)	Lumen output (Lm)	P_{LOAD} (W)
50	1.275	2558.7	41.57	0.425	852.9	13.86
25	1.9125	3440.9	63.86	0.6375	1146.96	21.29
0	2.55	4135.8	88.5	0.85	1378.6	29.5

4.3 OPERATING PARAMETER SELECTION OF THE ISOLATED CUK CONVERTER

The cuk converter operating parameters are selected in this sub-Section. The converter is to be operated from a dc bus with a voltage variation of 280-380 V. The large input voltage necessitates the use of a high frequency isolation transformer to avoid extreme small duty ratios, and to achieve the desired step down ratio to match the designed LED load current and voltage requirements. From Table 4.2, the load voltage would vary from 34.71–32.60 V, for heatsink temperature of 38°C, for a 3-string 0% dimming and 1-string-50% dimming respectively. The isolated cuk converter preliminary specifications are given in Table 4.3.

4.3.1 Effect of the Isolation Transformer Turns Ratio on the Switch Voltage

The isolation transformer turns ratio has an impact on the voltage stress experienced across the switch. Equation (4.11) shows this relationship, (where V_{SW} is the switch voltage stress, V_{IN} is the input voltage, n is the turns ratio and V_o is the output voltage) [27]. Accordingly, an acceptable turns ratio has to be selected to obtain a suitable switch voltage. In addition, the turns ratio affects

the capacitor size on the secondary side. The implication of a large turns ratio results in large capacitor requirements on the secondary side.

$$V_{SW} = V_{IN} + nV_O \tag{4.13}$$

Table 4.3: The converter specifications

Dc Input Voltage ($V_{in\ min}$)	280 - 380 V
Nominal dc Input Voltage ($V_{in\ nom}$)	340 V
Output Voltage (V_o)	35.25 – 34.7 V
Output Power (P_o)	88.5 – 13.86 W
Output Current (I_o)	2.55 – 0.425A
Load (R_{Load})	13.61 – 76.71 Ω

4.3.2 Selection of the Isolation Transformer Turns Ratio

The optimum switch utilization for an isolated cuk converter occurs at the duty ratio (δ_{OPT}) of 0.3333 [27]. Therefore, the converter will be designed with a duty ratio as close as possible to this value. For a non-ideal isolated cuk converter, the duty ratio δ is derived as follows;

$$\delta = \frac{(V_{fwd} + I_{L2}r_{L2} + V_O)}{\frac{(V_{IN,NOM} - I_{L1}r_{L1} - V_{sw,sat})}{n} + (V_O + V_{fwd} + I_{L2}r_{L2})} \tag{4.14}$$

Where; V_O is the output voltage, V_{fwd} is the diode forward voltage drop, $I_{L1}r_{L1}$ and $I_{L2}r_{L2}$ are the voltage drops across inductor L_1 and L_2 respectively, $V_{IN,NOM}$ is the nominal input voltage, $V_{sw,sat}$ is the voltage drop across the switch and n is the turns ratio of the isolation transformer (n_{pri} /n_{sec}). Using δ_{OPT} = 0.3333, and preliminary worst case values $V_{fwd} = 2\,\text{V}$, $I_{L1}r_{L1} = 2\,\text{V}$, $I_{L2}r_{L2} = 2\,\text{V}$ and $V_{sw,sat} = 2.5\,\text{V}$, the turns ratio *n* is found as follows;

$$\begin{aligned} n &= \frac{(V_{IN,NOM} - I_{L1}r_{L1} - V_{sw,sat})}{\frac{(V_O + V_{fwd} + I_{L2}r_{L2})}{\delta_{OPT}} - (V_O + V_{fwd} + I_{L2}r_{L2})} \\ &= \frac{(340 - 2 - 2.5)}{\frac{(34.71 + 2 + 2)}{0.3333} - (34.71 + 2 + 2)} = 4.33 \approx 4 \end{aligned} \tag{4.15}$$

Although a fractional turns ratio is practically possible, the calculated turns ratio is rounded off lower to an integral number for simplicity. The voltage stress across the switch is given as;

$$V_{SW} = V_{IN,NOM} + nV_O = 340 + (4 \times 34.71) = 479 \text{ V} \tag{4.16}$$

This is an acceptable voltage and a suitable switch can be selected with this voltage blocking capability. The actual duty ratio can then be calculated from (4.13) as;

$$\delta = \frac{(2+2+34.71)}{\frac{(340-2-2.5)}{4} + (34.71+2+2)} = 0.3158 \tag{4.17}$$

With n = 4, the actual duty ratio is close to the optimum duty ratio δ_{OPT} .

4.4 DESIGN OF THE COUPLED CUK CONVERTER

The switching frequency of the converter will be selected in this Section. The dc NC, NSC and SC inductors are sized and designed. The isolation transformer is also designed, and the coupling capacitors are sized. The active switch and output diode is selected. Finally, a snubber to clamp excessive voltage spikes on the active switch is designed.

4.4.1 Switching Frequency Selection

The switching frequency selection is important as it affects the passive component sizes and the switching losses in the semiconductor devices. Ideally, the magnetic components and capacitors used are desired to be compact to yield a high power density converter, with a high dynamic response. This is attained by using a high switching frequency, but has the drawback of reducing converter efficiency due to semiconductor switching losses and core losses in the transformer core [27]. As a compromise between the losses and component size, a switching frequency of 200 kHz is chosen.

4.4.2 Inductor Design and Input Current for Input Inductance Sizing

The input current is obtained as 0.26 A from Table 4.3 for an assumed converter efficiency of 100%; with input power of 88.5 W and nominal input voltage of 340 V. This efficiency is assumed for sizing purposes only and an accurate efficiency analysis will be carried out in Chapter 7. Using this input current value, the NC, NSC and SC inductors are sized as per a given input current ripple value.

4.4.2.1 Input Inductance Sizing

A comparative analysis is to be done in Chapter 5 for the three coupled inductor structures namely; NC, NSC and SC, and the practical inductor designs are undertaken in this Section. For comparison purposes, the same shape, size and core material are maintained. Initially, input inductance is designed for a NC inductance and the output inductance is simply determined by using the isolation transformer turns ratio. This same input and inductance values for the NC inductor are thus used to design the NSC and SC inductors. The input inductance for a NC inductor is calculated as;

$$L_1 = \frac{V_{IN,NOM} \cdot \delta}{\Delta I_{L_1,pk-pk} \cdot f_{sw}} \tag{4.18}$$

Where $\Delta I_{L_1,av,pk-pk}$ is the peak to peak ripple across L_1, the ripple is chosen as 100% of the maximum average input current I_{in} of 0.26A. This value of ripple ensures continuous input current conduction while maintaining a small inductance value. Hence L_1 is given as;

$$L_1 = \frac{340\,\text{V} \times 0.3158}{100\% \times 0.26\,\text{A} \times 200 \times 10^3\,\text{Hz}} = 2.064 \times 10^{-3}\,\text{H} \approx 2 \times 10^{-3}\,\text{H} \tag{4.19}$$

Output Inductance L_2 values for NC, NSC, and SC are given in Section 4.4.2.8, 4.4.2.9 and 4.4.2.10 respectively.

4.4.2.2 Selection of Maximum Operating Flux Density B_{SAT}

For a dc inductor, the high frequency ripple is small, and has negligible effect on the core losses, and core losses can be neglected [54]. On the other hand, it becomes pertinent to avoid saturation of the core by operating below the saturation flux density limit. The material chosen for the dc inductor design is N87 from EPCOS [99], as it has acceptable performance for a dc inductor application. The saturation flux density for N87 at 25°C ($B_{SAT(25°C)}$) is 0.463 T, while at 100°C $B_{SAT(100°C)}$ it is 0.380 T, at the magnetic field intensity of 400 A/m [99]. For the dc inductor design, B_{SAT} is chosen as 0.3 T so as to keep within the linear flux density region.

4.4.2.3 Selection of the Core Size

To select the core, the following area-product (*AP*) formula is used [58].

$$AP = A_w \cdot A_e = \left[\frac{L \cdot I_{PK,MAX} \cdot I_{RMS,MAX}}{B_{SAT} \cdot k_{cu} \cdot J_{RMS}} \right]^{1.31} \tag{4.20}$$

Where; A_w =Winding window area [m^2], A_e =Magnetic cross-section [m^2], L =Input inductance [H], $I_{PK,MAX}$ =The maximum peak input current [A], $I_{RMS,MAX}$ =The maximum RMS Input Current [A], k_{cu} =Copper utilization factor , J_{RMS} =Current density [A/m^2]. $I_{PK,MAX}$ and $I_{RMS,MAX}$ for the worst case input power using a safety factor S_{factor} of 160% ,are obtained as follows;

$$I_{RMS,MAX} = I_{in} \cdot S_{factor} = 0.26 \times 160\% = 0.416\ \text{A} \tag{4.21}$$

$$I_{PK,MAX} = I_{RMS,MAX} + (I_{RMS,MAX} \times 25\%) = 0.416\ \text{A} + (0.416\ \text{A} \times 25\%) = 0.52\ \text{A} \tag{4.22}$$

For a worst case power dissipation $P_{W,SP}$ of 155×10^3 W/m^3, copper utilization factor k_{cu} of 0.4, and copper resistivity of $2.2 \times 10^{-8}\ \Omega$-m at 100°C, the current density J_{RMS} is determined as follows [54];

$$J_{RMS} = \sqrt{\frac{P_{W,SP}}{\rho_{cu} \cdot k_{cu}}}\ [\text{A/m}^2] = \sqrt{\frac{155 \times 10^3\ \text{W/m}^3}{2.2 \times 10^{-8}\ \Omega\text{-m} \times 0.4}} = 4.20 \times 10^6\ \text{A/m}^2 \tag{4.23}$$

$I_{PK,MAX}$ and $I_{RMS,MAX}$ are multiplied by a safety factor of 2, so that the coupled inductor core chosen can withstand any unforeseen current transients, as current transients are foreseen due to step changes in load and input voltage. The required area product *AP* is evaluated as follows [58];

$$AP = A_w \cdot A_e = \left[\frac{2 \times 10^{-3}\ \text{H} \times 0.416\ \text{A} \times 2 \times 0.52\ \text{A} \times 2}{0.3\ \text{T} \times 0.4 \times 4.20 \times 10^6\ \text{A/m}^2}\right]^{1.31} = 8.16 \times 10^{-12}\ \text{m}^4 \tag{4.24}$$

Because the same core size and shape is to be used for NC, NSC and SC inductors, a larger core than required for the NC inductor is chosen. This is to accommodate the spacers between the windings for the NSC and SC inductors as will be seen in Sections 4.4.2.9 and 4.4.2.10 respectively. A PQ 32/20 core with an *AP* of $1.5548 \times 10^{-8}\ \text{m}^4$ is selected. Also, due to its cylindrical centre leg shape and a square window area which accommodates a cylindrical spacer to be used for the desired leakage inductance for the NSC and SC inductors. Furthermore, it is compact and has good shielding. The following summarises the PQ 32/20 parameters; A_e (Winding Window Area) $= 0.169 \times 10^{-3}\ \text{m}^2$, A_w (Magnetic cross-section) = $0.092 \times 10^{-3}\ \text{m}^2$, W_W (Window Width) = $11.5 \times 10^{-3}\ \text{m}$, b_W (Bobbin Width)= $8.9 \times 10^{-3}\ \text{m}$, H_{TOT} (Total Winding Height)=

6.425×10^{-3} m, MLT (Mean Length Turn)= 66.7×10^{-3} m, AP (Area product)= 1.5548×10^{-8} m^4, and $R_{\theta,CORE}$ (Core Thermal Resistance)= 8°C/W.

4.4.2.4 Calculation of Input and Output Inductor Turns

The minimum number of turns of the NC, NSC and SC inductors is calculated as [58];

$$N_{MIN} = \frac{L \cdot I_{PK,MAX}}{A_e \cdot B_{MAX}} = \frac{2\times10^{-3}\ \text{H}\times0.416\ \text{A}}{0.169\times10^{-3}\ \text{m}^2\times0.3\ \text{T}} = 16.41\ \text{Turns} \tag{4.25}$$

The number of turns N_{MIN} cannot be lower than 16.41, otherwise the flux density in the core will exceed B_{SAT}. Also, N_{MIN} has to be integrally divisible by 4, which is the turns ratio of the isolation transformer. Hence, N_{MIN} is rounded higher to an integral value divisible by 4, and depends on a suitable air-gap length l_g. The energy stored in the magnetic material is insignificant and an air-gap is required to produce the required inductance. For the SC and NSC inductors, the air-gap must be placed in the centre leg [58], to achieve the correct location of desired leakage inductance on the output inductor, and to have a simple mechanically stable core. The PQ32/20 core selected was already gapped at 0.7 mm by the manufacturer. Hence the actual number of turns of the input inductor N_{L_1} is calculated as follows (neglecting fringing flux);

$$N_{L_1} = \sqrt{\frac{L \cdot l_g}{\mu_0 \cdot \mu_r \cdot Ae}} = \sqrt{\frac{2\times10^{-3}\ \text{H}\times0.7\times10^{-3}\ \text{m}}{4\pi\cdot10^{-7}\times0.169\times10^{-3}\ \text{m}}} = 81.19 \approx 84\ \text{Turns} \tag{4.26}$$

Since the isolation transformer has a step down ratio of 4, then the output inductor number of turns N_{L_2} is divided by this ratio, thus N_{L_2} = 21 turns.

4.4.2.5 Calculation of Inductor Wire Gauges

The wire gauge to be used by NC, NSC and SC inductors is calculated in this Section. Copper losses in the inductor windings cause a temperature rise within the windings, and should be minimised for good efficiency. The area and diameter of the input inductor wire is given as [27];

$$A_{cu,L_1} = \frac{I_{L_1,RMS}}{J_{RMS}} = \frac{0.416\ \text{A}}{4.20\times10^{6}\ \text{A/m}^2} = 0.099\times10^{-6}\ \text{m}^2 \tag{4.27}$$

$$d_{w,L_1} = \sqrt{\frac{4 \cdot A_{cu,L_1}}{\pi}} = \sqrt{\frac{4 \times 0.0979 \times 10^{-6}\,\text{m}^2}{\pi}} = 0.355 \times 10^{-3}\,\text{m} \quad (4.28)$$

From the wire gauge Table [27], $0.355 \times 10^{-3}\,\text{m}$ corresponds to AWG 28 which has a diameter of $0.366 \times 10^{-3}\,\text{m}$ and has a resistance $R_{AWG,28}$ of 0.21427 Ω/m. The area and diameter of the output inductor wire are given as;

$$A_{cu,L_2} = \frac{I_{L_2,RMS}}{J_{RMS}} = \frac{2.55\,\text{A}}{4.20 \times 10^{6}\,\text{A/m}^2} = 0.6071 \times 10^{-6}\,\text{m}^2 \quad (4.29)$$

$$d_{w,L_2} = \sqrt{\frac{4 \cdot A_{cu,L_2}}{\pi}} = \sqrt{\frac{4 \times 0.6071 \times 10^{-6}\,\text{m}^2}{\pi}} = 0.8792 \times 10^{-3}\,\text{m} \quad (4.30)$$

From the wire gauge Table, $0.8792 \times 10^{-3}\,\text{m}$ corresponds to AWG 19 which has a diameter of $0.948 \times 10^{-3}\,\text{m}$ and has a resistance $R_{AWG,19}$ of 0.02636 Ω/m.

4.4.2.6 Calculation of Winding Resistances Temperature Rise

The resistance of the input winding is given as [27];

$$r_{L_1} = MLT \cdot N_{L_1} \cdot R_{AWG,28} = 6.67 \times 10^{-2}\,\text{m} \times 84 \times 0.21427\,\Omega/\text{m} = 1.2\,\Omega \quad (4.31)$$

The temperature rise in the input winding is [27];

$$\Delta T_{WIND,L_1} = R_{WIND,L_1} \cdot R_{\theta,CORE} \cdot \left(I_{L_1,RMS}\right)^2 = 1.2\,\Omega \times 8\,°\text{C/W} \times \left(0.416\,\text{A}\right)^2 = 1.66\,°\text{C} \quad (4.32)$$

The resistance of the output winding is given as [27];

$$r_{L_2} = MLT \cdot N_{L_2} \cdot R_{AWG,19} = 6.67 \times 10^{-2}\,\text{m} \times 21 \times 0.02636\,\Omega/\text{m} = 37 \times 10^{-3}\,\Omega \quad (4.33)$$

The temperature rise in the winding is [27];

$$\Delta T_{WIND,L_2} = R_{WIND,L_2} \cdot R_{\theta,CORE} \cdot I_{L_2,RMS}^{\ 2} = 37 \times 10^{-3}\,\Omega \times 8\,°\text{C/W} \times \left(2.55\text{A}\right)^2 = 1.92°\text{C} \quad (4.34)$$

Temperature rise values of $\Delta T_{WIND,L_1}$ and $\Delta T_{WIND,L_2}$ are acceptable.

4.4.2.7 Calculation Winding Height

The bobbin width b_W of the PQ 32/20 core is given as 8.9mm. The winding height is given as the number of wire layers multiplied by the diameter of the wire used. The number of layers for the input inductor is given as [58];

$$Layers_{L_1} = \frac{N_{L_1} \cdot d_{W,L_1}}{b_W} = \frac{84 \times 0.366 \times 10^{-3}\,\text{m}}{8.9 \times 10^{-3}\,\text{m}} \approx 4 \tag{4.35}$$

The winding height for the input inductor is;

$$H_{WIND,L_1} = d_{W,L_1} \cdot Layers_{L_1} = 0.366 \times 10^{-3}\,\text{m} \times 4 \approx 1.5 \times 10^{-3}\,\text{m} \tag{4.36}$$

The number of layers for the output inductor is given as;

$$Layers_{L_2} = \frac{N_{L_2} \cdot d_{W,L_2}}{b_W} = \frac{21 \times 0.948 \times 10^{-3}\,\text{m}}{8.9 \times 10^{-3}\,\text{m}} \approx 3 \tag{4.37}$$

The winding height for the output inductor is given as;

$$H_{WIND,L_2} = d_{W,L_2} \cdot Layers_{L_2} = 0.948 \times 10^{-3}\,\text{m} \times 3 \approx 2.844 \times 10^{-3}\,\text{m} \tag{4.38}$$

4.4.2.8 NC Inductors Winding Arrangement

For the NC inductors, the input and output inductors are wound on two separate PQ32/20 cores. Since the isolation transformer has a turns ratio n = 4, the output inductance L_2 is thus;

$$L_2 = \frac{L_1}{n^2} = \frac{2 \times 10^{-3}\,\text{H}}{4^2} = 0.125 \times 10^{-3}\,\text{H} \tag{4.39}$$

4.4.2.9 NSC Inductor Leakage Inductance L_{L2} and Required Spacer Height

To achieve a NSC inductor, the two windings are wound on the same PQ32/20 core with a space gap introduced to achieve the desired leakage inductance in the correct location [58]. The leakage inductance L_{L2}, for the NSC inductors is computed and used to determine the spacer gap size required to achieve this leakage inductance. The mutual inductance M, is found using (3.17), using L_1 = 2 mH and turns ratio n = 4 as;

$$M = \frac{2 \times 10^{-3}\,\text{H}}{4} = 0.5 \times 10^{-3}\,\text{H} \tag{4.40}$$

The output inductance L_2 is calculated using (3.16), with k = 0.98 as;

$$L_2 = \frac{2\times10^{-3}\ \text{H}}{0.98^2\times4^2} = 130.154\times10^{-6}\ \text{H} \tag{4.41}$$

The leakage inductance L_{L2} is determined using (3.6) as;

$$L_{L2} = L_2 - n\cdot M = 130.154\times10^{-6}\ \text{H} - 4\times0.5\times10^{-3}\ \text{H} = 5.154\times10^{-6}\ \text{H} \tag{4.42}$$

The leakage inductance L_{L2} is defined using the spacer height S_1 as [58];

$$L_{L_2} = \frac{\mu_0\cdot N_{L_2}{}^2\cdot MLT\cdot S_1}{W_W} = \frac{\mu_0\times21^2\times66.7\times10^{-3}\times\text{S}_1}{1.15\times10^{-2}\,\text{m}} = (3.2142\times10^{-3}\times S_1) \tag{4.43}$$

Using $L_{L2} = 5.154\times10^{-6}$ H, S_1 is found as;

$$S_1 = \frac{5.154\times10^{-6}\ \text{H}}{3.2142\times10^{-3}} = 1.603\times10^{-3}\ \text{m} \tag{4.44}$$

The gap is introduced in between the windings as shown in Figure 4.4 (a).

4.4.2.10 SC Inductor Leakage Inductance L_{L1} and L_{L2} and Required Spacer Heights

The spacer gaps required for the SC inductor are computed after determining the leakage inductances L_{L1} and L_{L2}. The mutual inductance is found using (3.15), with coupling coefficient k = 0.98 and turns ratio n = 4, as;

$$M = \frac{0.98\times2\times10^{-3}\ \text{H}}{4} = 0.49\times10^{-3}\ \text{H} \tag{4.45}$$

Inductance L_2 is determined using (3.14) as;

$$L_2 = \frac{2\times10^{-3}\ \text{H}}{\times4^2} = 125\times10^{-6}\ \text{H} \tag{4.46}$$

The leakage inductances L_{L1} and L_{L2} are calculated using (3.5) and (3.6) as;

$$L_{L1} = L_2 - n\cdot M = 2\times10^{-3}\ \text{H} - 4\times0.49\times10^{-3}\ \text{H} = 40\times10^{-6}\ \text{H} \tag{4.47}$$

$$L_{L2} = L_2 - n\cdot M = 125\times10^{-6}\ \text{H} - 4\times0.49\times10^{-3}\ \text{H} = 2.5\times10^{-6}\ \text{H} \tag{4.48}$$

The gap S_2 is the spacer that produces the leakage inductance L_{L1}, and is defined as [58];

$$L_{L_1}\cdot = \frac{\mu_0\cdot N_{L_1}{}^2\cdot MLT\cdot S_2}{W_W} = \frac{\mu_0\times84^2\times66.7\times10^{-3}\times\text{S}_1}{1.15\times10^{-2}\,\text{m}} = (51.42\times10^{-3}\times S_2) \tag{4.49}$$

Using $L_{L1} = 40\times10^{-6}$ H, S_2 is found as;

$$S_2 = \frac{40\times10^{-6}\ \text{H}}{51.42\times10^{-3}} = 0.777\times10^{-3}\ \text{m} \tag{4.50}$$

Similarly, the spacer gap S_2 that produces the leakage inductance L_{L_2} is defined as [58];

$$L_{L_2} = \frac{\mu_0 \cdot N_{L_2}{}^2 \cdot MLT \cdot S_3}{W_W} = \frac{\mu_0 \times 21^2 \times 66.7\times10^{-3} \times S_3}{1.15\times10^{-2}\,\text{m}} = (3.214\times10^{-3} \times S_3) \tag{4.51}$$

Using $L_{L_2} = 2.5\times10^{-6}$ H, S_3 is found as;

$$S_3 = \frac{2.5\times10^{-6}\ \text{H}}{3.214\times10^{-3}} = 0.777\times10^{-3}\ \text{m} \tag{4.52}$$

The spacers are introduced in between the windings as shown in Figure 4.4 (b).

(a) Non-Symmetrically Coupled Inductor (b) Symmetrically Coupled Inductor

Figure 4.4: Coupled inductor construction profiles.

4.4.3 Isolation Transformer Design

The isolation transformer is designed in this Section. The ferrite material chosen is N87 by EPCOS [99], as it has acceptable performance at the switching frequency of 200 kHz. From the N87 Material Datasheet, the power loss at 100°C for 200 kHz switching frequency is given as;

$$P_{v,sp,100°C,200kHz} = 175kW/m^3 \tag{4.53}$$

This will be the maximum allowed power loss in the transformer core. For an optimal transformer design the ratio of ac resistance to dc resistance to obtain optimum conductor size and minimum winding loss is given by [100];

$$\frac{R_{ac}}{R_{dc}} = 1.5 \tag{4.54}$$

The transformer design inputs are given as follows; $V_{PRI,RMS} = 232.5\,\text{V}$, $I_{PRI,RMS} = 0.431\,\text{A}$, $V_{SEC,RMS} = 58.13\,\text{V}$, $I_{SEC,RMS} = 1.725\,\text{A}$, $\delta = 0.3158$, $B_{C,\max} = 0.1\,\text{T}$, $V_{PRI,PK} = 173\,\text{V}$, $V_{SEC,PK} = 43.1\,\text{V}$, $\mu_{r,N87} = 2{,}200$, $k_{cu} = 0.3$ and $\rho_{cu,100°C} = 2.2\times10^{-8}\,\Omega\,\text{m}$. For the design, the allowable current density is [54];

$$J_{RMS} = \sqrt{\frac{P_{v,sp}}{k_{cu}\cdot\rho_{cu}\cdot\frac{R_{ac}}{R_{dc}}}} = \sqrt{\frac{175\times10^{3}\ \text{W/m}^3}{0.3\times2.2\times10^{-8}\,\Omega\text{m}\times1.5}} = 4.2044\times10^{6}\ \text{A/m}^2 \tag{4.55}$$

The total apparent power of the transformer is determined as [100];

$$S_{Total} = V_{PRI}\cdot I_{PRI} + V_{SEC,RMS}\cdot I_{SEC,RMS} \tag{4.56}$$

$$S_{Total} = 232.5\,\text{V}\times0.431\,\text{A} + 58.13\,\text{V}\times1.725\,\text{A} = 200.48\ \text{VA} \tag{4.57}$$

The area product *AP*, is used to determine the core size as [100];

$$AP = \frac{\sqrt{\delta}\cdot S_{Total}}{4\cdot B_{c,\max}\cdot f_{sw}\cdot J_{RMS}\cdot k_{cu}} \tag{4.58}$$

$$AP = \frac{\sqrt{0.3158}\times200.48}{4\times0.1\,\text{T}\times200\times10^{3}\ \text{Hz}\times4.2044\times10^{6}\ \text{A/m}^2\times0.3} = 1.11\times10^{-9}\ \text{m}^4 \tag{4.59}$$

The chosen core is the E19/8/5, with an *AP* of $1.247616\times10^{-9}\ \text{m}^4$. The chosen core parameters are as follows; A_c (Magnetic Cross Section) $= 23.04\times10^{-6}\,\text{m}^2$, W_W (Window Width) $= 11.4\times10^{-3}\,\text{m}$, W_H (Window Height) $= 4.5\times10^{-3}\,\text{m}$, MLT (Mean Length Turn) $= 38.2\times10^{-3}\,\text{m}$, AP (Area product) $= 1.247616\times10^{-9}\ \text{m}^4$ and ℓm (Magnetic Mean length) $= 46.7\times10^{-3}\,\text{m}$. The minimum number of primary turns is given as [100];

$$N_{PRI} = \frac{\delta\cdot V_{PRI,PK}}{4B_{c,\max}\cdot f_{sw}\cdot A_C} = \frac{0.3132\times173\text{V}}{4\times0.1\,\text{T}\times200\times10^{3}\ \text{Hz}\times23.04\times10^{-6}\,\text{m}^2} = 29.6\approx32 \tag{4.60}$$

The number of secondary turns is given as [100];

$$N_{SEC} = \frac{V_{SEC,PK}}{V_{PRI,PK}}\cdot N_{PRI} = \frac{43.1V}{173V}\times32 = 7.5\approx8 \tag{4.61}$$

The Area $A_{cu,PRI}$ of the wire used for the primary winding is then determined as [100];

$$A_{cu,PRI} = \frac{I_{PRI,RMS}}{J_{RMS}} = \frac{0.431}{4.2044\times10^{6}\ \text{A/m}^2} = 102.5\times10^{-9}\ \text{m}^2 \tag{4.62}$$

The diameter of the primary wire to be used is [27];

$$d_{WIRE,PRI} = \sqrt{\frac{4A_{cu,PRI}}{\pi}} = \sqrt{\frac{4\times102.5\times10^{-9}\ \text{m}^2}{\pi}} = 0.36128\times10^{-3}\ \text{m} \tag{4.63}$$

The Area $A_{cu,SEC}$ of the wire used for the secondary winding is determined similarly as [100];

$$A_{cu,SEC} = \frac{I_{SEC,RMS}}{J_{RMS}} = \frac{1.725\ \text{A}}{4.2044\times10^{6}\ \text{A/m}^2} = 410.28\times10^{-9}\ \text{m}^2 \tag{4.64}$$

The diameter of the secondary wire to be used is [27];

$$d_{WIRE,SEC} = \sqrt{\frac{4A_{cu,SEC}}{\pi}} = \sqrt{\frac{4\times410.28\times10^{-9}\ \text{m}^2}{\pi}} = 0.7227\times10^{-3}\ \text{m} \tag{4.65}$$

The skin depth of the copper at 100°C and at a frequency of 200 kHz is given as [54];

$$\delta_{Skin} = \sqrt{\frac{\rho_{cu,100°C}}{\pi\cdot f_{sw}\cdot\mu_O}}\ [\text{m}] = \sqrt{\frac{2.2\times10^{-8}\ \Omega\text{m}}{\pi\times200\times10^{3}\,\text{Hz}\times\mu_O}} = 0.16692\times10^{-3}\,\text{m} \tag{4.66}$$

$$2\delta_{Skin} = 0.33384\times10^{-3}\,\text{m} \tag{4.67}$$

Due to the skin effect and to minimize ac resistance of the wire used, if $2\delta_{Skin}$ is less than the wire diameter calculated in (4.63) and (4.65) above, then stranded wires are needed. The number of strands for the primary is given as [100];

$$Strands_{PRI} = \frac{A_{cu,PRI}}{\pi\delta^2_{SKIN}} = \frac{102.5\times10^{-9}\ \text{m}^2}{\pi(0.16692\times10^{-3}\text{m})^2} = 1.17 \approx 2 \tag{4.68}$$

$$Strands_{SEC} = \frac{A_{cu,SEC}}{\pi\delta^2_{SKIN}} = \frac{410.28\times10^{-9}\ \text{m}^2}{\pi(0.16692\times10^{-3}\text{m})^2} = 4.68 \approx 6 \tag{4.69}$$

For simplicity, the wire diameters are selected as close as possible to $2\delta_{Skin}$. This is done to ensure compactness and avoid unnecessary over-sizing. Therefore, for the primary winding, AWG 28 with a diameter of 0.366×10^{-3} m is selected. For the secondary winding, AWG 26 with a diameter of 0.452×10^{-3} m is selected. The primary winding resistance can now be calculated as (where r_{AWG28} and r_{AWG26} are the resistances of the wires obtained from the wire gauge Table) [100];

$$r_{pri} = \frac{MLT \cdot N_{PRI} . r_{AWG28}}{Strands_{PRI}} = \frac{38.2\times10^{-3}\,\text{m}\times31\times214\times10^{-3}\,\Omega/\text{m}}{2} = 0.127\Omega \quad (4.70)$$

$$r_{sec} = \frac{MLT \cdot N_{SEC} . r_{AWG26}}{Strands_{SEC}} = \frac{38.2\times10^{-3}\,m\times8\times134.5\times10^{-3}\,\Omega/m}{6} = 6.85\times10^{-3}\ \Omega \quad (4.71)$$

The magnetising inductance is given as [54];

$$L_m = \frac{A_c . \mu_{rN87} \cdot \mu_o \cdot N^2{}_{PRI}}{\ell m} = \frac{23.04\times10^{-6}\,m^2\times2200\times\mu_o\times31^2}{46.7\times10^{-3}\ \text{m}} = 1.312\times10^{-3}\ \text{H} \quad (4.72)$$

To minimise voltage and current spikes which cause EMI generation and stress the active switch, the leakage inductance can be minimised by interleaving the windings. The number of interfaces is chosen as 4 and the primary leakage inductance is calculated as follows [54];

$$\begin{aligned} L_{LK,PRI} &= \frac{\mu_0 \cdot N_{PRI}{}^2 \cdot MLT \cdot W_W}{3 \cdot p^2 \cdot W_H} \\ &= \frac{\mu_0 \times 31^2 \times 38.2\times10^{-3}\,\text{m}\times11.4\times10^{-3}\,\text{m}}{3\times4^2\times4.5\times10^{-3}\,\text{m}} = 2.43\times10^{-6}\ \text{H} \end{aligned} \quad (4.73)$$

The construction profile showing the interleaved windings and interfaces is shown in Figure 4.5.

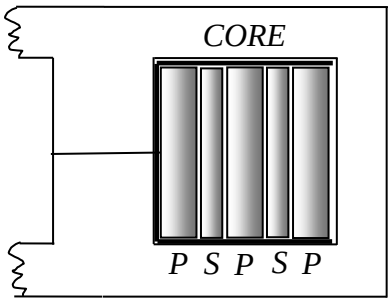


Figure 4.5: Construction profile of the isolation transformer.

4.4.4 Coupling Capacitors Sizing and Selection

The coupling capacitors C_a and C_{bs} are sized in this Section. $V_{Ca,av}$ and $V_{Cbs,av}$ are average voltages across C_a and C_{bs} respectively. The capacitors are sized by recognising that $V_{Ca,av} = V_{in}$ and $V_{Cbs,av} = V_o$, and the ripple $\Delta V_{Ca,pk-pk}$ and $\Delta V_{Cb,pk-pk}$ are to be equal. Using duty ratio δ =

0.3158, switching period T_{sw} = 5µs, output current I_o = 2.55 A and $\Delta V_{Ca,pk-pk}$ = $\Delta V_{Cb,pk-pk}$ = 0.8%, C_a and C_{bs} are sized as follows;

$$C_a = \frac{I_o \cdot \delta \cdot T_{sw}}{\Delta V_{c_a\ pk-pk} \cdot n} = \frac{2.55\,\text{A} \times 0.3158 \times 5\,\mu\text{s}}{0.8\% \times 340 \times 4} = 370\,\text{nF} \approx 470\,\text{nF} \tag{4.74}$$

$$C_{bs} = \frac{I_o \cdot \delta \cdot T_{sw}}{\Delta V_{c_b\ pk-pk}} = \frac{2.55\text{A} \times 0.3158 \times 5\,\mu\text{s}}{0.8\% \times 34.71} = 14.5\,\mu\text{F} \approx 15\,\mu\text{F} \tag{4.75}$$

The capacitance values obtained are rounded off to the nearest available standard values. Polypropylene and polyester capacitors have been chosen due to the low ESR and long life that they exhibit. The coupling capacitor C_a selected is Epcos-B32686-A474, polypropylene, 0.47 µF, V_{dc} =1000 V and the equivalent series resistance (ESR) is 0.2 Ω. The coupling capacitor C_{bs} selected is Epcos-B32524-Q1156, polyester, 15 µF, V_{dc} =100 V and ESR= 0.2 Ω.

4.4.5 MOSFET Selection

It was seen in Section 4.2 that the maximum voltage stress V_{SW} experienced by the switch is 519 V. For the MOSFET selection, a safety factor of 2 for V_{SW} is desired so that the switch can handle any voltage transients and switching spikes due to the leakage inductance of the isolation transformer. Therefore a MOSFET with a voltage blocking capability of at least 1 kV and have acceptable switching losses at the switching frequency of 200 kHz is required. To obtain the switching loss, the peak switch current $i_{sw,pk}$ is obtained as;

$$i_{sw,pk} = I_{L_1,av} + \frac{\Delta i_{L_1 p-p}}{2} + \frac{\Delta i_{L_m p-p}}{2} + \frac{I_{L_2,av}}{n} + \frac{\Delta i_{L_2 p-p}}{2n} \tag{4.76}$$

Where; n is the turns ratio of the isolation transformer, $\Delta i_{L_m p-p}$ is the p-p ripple across the magnetizing inductance of the isolation transformer L_m, $I_{L_1,av}$ and $I_{L_2,av}$ are the average currents for input and output-side inductances respectively, $\Delta i_{L_1 p-p}$ and $\Delta i_{L_2 p-p}$ are the p-p currents for the input and output inductors respectively. The peak-peak ripples are given as follows;

$$\Delta i_{L_1 p-p} = \frac{V_{in} \cdot \delta}{L_1 \cdot f_{sw}} = \frac{340\,\text{V} \times 0.3158}{2 \times 10^{-3}\,\text{H} \times 200 \times 10^{-3}\,\text{Hz}} = 268.43 \times 10^{-3}\,\text{A} \tag{4.77}$$

$$\Delta i_{L_m p-p} = \frac{V_{in} \cdot \delta}{L_m \cdot f_{sw}} = \frac{340\,\text{V} \times 0.3158}{1.312 \times 10^{-3}\,\text{H} \times 200 \times 10^{-3}\,\text{Hz}} = 409.19 \times 10^{-3}\,\text{A} \quad (4.78)$$

$$\Delta i_{L_2 p-p} = \frac{V_o \cdot \delta}{L_2 \cdot f_{sw}} = \frac{34.71\,\text{V} \times 0.3158}{0.125 \times 10^{-3}\,\text{H} \times 200 \times 10^{-3}\,\text{Hz}} = 438.456 \times 10^{-3}\,\text{A} \quad (4.79)$$

Thus $i_{sw,pk}$ is found using Equation (4.76) where; $I_{L_1,av} = 260 \times 10^{-3}$ A, $I_{L_2,av} = 2.55$ A and $n = 4$ as 1.29 A. The RMS current $I_{sw,RMS}$, through the switch is given as;

$$I_{sw,RMS} = \sqrt{\delta \cdot \frac{1}{3} \cdot \left({I_{sw,H}}^2 + I_{sw,H} I_{sw,L} + {I_{sw,L}}^2 \right)} \quad (4.80)$$

Where;

$$I_{sw,H} = \left(I_{L_1,av} - \frac{\Delta i_{L_1 p-p}}{2} \right) + \left(\frac{I_{L_2,av}}{n} - \frac{\Delta i_{L_2 p-p}}{2n} \right) - \left(\frac{\Delta i_{L_m p-p}}{2} \right) \quad (4.81)$$

$$I_{sw,L} = \left(I_{L_1,av} + \frac{\Delta i_{L_1 p-p}}{2} \right) + \left(\frac{I_{L_2,av}}{n} + \frac{\Delta i_{L_2 p-p}}{2n} \right) + \left(\frac{\Delta i_{L_m p-p}}{2} \right) \quad (4.82)$$

Again, using values obtained by Equations (4.77), (4.78) and (4.79) and substituting in Equation (4.80), $I_{sw,RMS}$ is found as 520.27×10^{-3} A. Using a safety factor of 2, a MOSFET which can carry an RMS current of at least 1.04 A and a peak current of 2.58 A is required. The selected MOSFET is STW13NK100Z [101]. Its specifications are $R_{ds,on}$ =0.7 Ω, $I_{d\ max\ (100°C)}$ =13 A, V_{dmax} =1000 V, rise-time t_{ri}=t_{rv} =35ns and fall time t_{fi} =t_{fv} =45ns. The switching loss $P_{sw,sw}$, of this MOSFET is calculated as follows [54];

$$P_{sw,sw} = \frac{1}{2} V_{sw} \cdot i_{sw,pk} \cdot f_{sw} \left(t_{ri} + t_{fv} + t_{rv} + t_{fi} \right) \quad (4.83)$$

Using $V_{sw} = 519$ V, $i_{sw,pk}$ = 1.29 A, $\left(t_{ri} + t_{fv} + t_{rv} + t_{fi} \right) = 160 \times 10^{-9}$ s and $f_{sw} = 200$ kHz, $P_{sw,sw}$ is found as 10.712 W. The conduction loss $P_{sw,cond}$ in the active switch is given follows where $R_{DS,on}$ is the MOSFET on resistance;

$$P_{sw,cond} = {I^2}_{sw,RMS} \cdot R_{DS,on} \quad (4.84)$$

Using $I_{sw,RMS} = 520.27 \times 10^{-3}$ A, and $R_{DS,on} = 0.7\,\Omega$, $P_{sw,cond}$ is found as 189.28×10^{-3} W.

The total power dissipation $P_{DISS,sw}$ is given as;

$$P_{DISS,sw} = P_{sw,sw} + P_{sw,cond} = 10.9\,\text{W} \tag{4.85}$$

Given the maximum junction temperature $T_{j,MAX}$ is 150°C, and the ambient temperature T_{amb} is 40°C. The heatsink thermal requirement is given as [54];

$$R_{\theta j-a} = \frac{T_{j,MAX} - T_{amb}}{P_{DISS,sw}} = \frac{150°\text{C} - 40°\text{C}}{10.9\,\text{W}} = 10.09\,°\text{C/W} \tag{4.86}$$

4.4.6 Diode Selection

The diode on the secondary side of the converter must block a voltage $V_{d,Block}$ given as;

$$V_{d,block} = \frac{V_{in,MAX}}{n} + V_o = \frac{380\,\text{V}}{4} + 34.71\,\text{V} = 129.71\,\text{V} \tag{4.87}$$

As stated previously, a safety factor of 2 is used, so that the diode selected may withstand any unexpected voltage spikes or load transients. Hence the diode selected must block a voltage of at least 260 V. The RMS current $I_{D,RMS}$, through the diode is given as;

$$I_{D,RMS} = \sqrt{(1-\delta)\cdot\frac{1}{3}\cdot\left(I_{D,H}{}^2 + I_{D,H}I_{D,L} + I_{D,L}{}^2\right)} \tag{4.88}$$

Where;

$$I_{D,H} = I_{L_1,av}\cdot n + I_{L_2,av} + \frac{1}{2}\left(\Delta i_{L_1 p-p}\cdot n + \Delta i_{L_m p-p}\cdot n + \Delta i_{L_2 p-p}\right) \tag{4.89}$$

$$I_{D,L} = I_{L_1,av}\cdot n + I_{L_2,av} - \frac{1}{2}\left(\Delta i_{L_1 p-p}\cdot n + \Delta i_{L_m p-p}\cdot n + \Delta i_{L_2 p-p}\right) \tag{4.90}$$

Using the values obtained by Equations (4.77), (4.78) and (4.79), using $n = 4$, $\delta = 0.3158$ and substituting in Equation (4.88), $I_{D,RMS}$ is found as 3.063 A. To withstand any load transients, again a safety factor of 2 is used. Therefore a diode that can handle at least 6.13 A is to be selected. A silicon carbide shottky diode C3D08060A is selected, which has zero recovery losses [102]. It has the following specifications, $V_{d,block}$ = 600 V, $I_{d,av}$ = 8A, V_{fwd} at 3.12 A is 1.2 V and R_{fwd} = 0.03 Ω. The losses considered in the diode are due to the dynamic resistance, R_{fwd}, and the forward voltage drop V_{fwd}. The loss $P_{D,cond}$ due to diode resistance R_{fwd} is given as;

$$P_{D,cond} = I^2{}_{D,RMS} \cdot R_{fwd} = 3.063\,\text{A}^2 \times 0.03\,\Omega = 0.281\,\text{W} \tag{4.91}$$

The loss in diode $P_{D,thresh}$ due to the forward voltage drop is given as follows, where;

$$I_{D,av} = \frac{1}{2}\left(I_{D,H} + I_{D,L}\right)\left(1-\delta\right) \tag{4.92}$$

$$P_{D,thresh} = V_{fwd} \cdot I_{D,av} \tag{4.93}$$

Using Equations (4.89) and (4.90), $P_{D,thresh}$ is found as 2.947 W. The total diode loss $P_{DISS,D}$ is given by;

$$P_{DISS,D} = P_{D,cond} + P_{D,thresh} = 0.281\,\text{W} + 2.947\,\text{W} = 3.228\,\text{W} \tag{4.94}$$

The maximum junction temperature $T_{j,MAX}$ is 110°C, and the ambient temperature T_a is 40°C. The heatsink °C /W requirement is given as;

$$R_{\theta j-a} = \frac{T_{j,MAX} - T_a}{P_{DISS,D}} = \frac{110°\text{C} - 40°\text{C}}{3.74\,\text{W}} = 21.69°\text{C/W} \tag{4.95}$$

4.4.7 Gate Drive Circuit Design

The ACPL H342 chip is chosen due to its capability driving the selected MOSFET at 200 kHz [103]. Furthermore, it provides optical isolation making it safe and suitable to use with digital system such as a microprocessor. The circuit diagram can be found in [103]. The power dissipation due to charging and discharging of the MOSFET gate capacitor is given as;

$$P_C = Q_G \cdot V_{GS} \cdot f_{sw} = 190 \times 10^{-9}\ \text{C} \times 10\,\text{V} \times 200 \times 10^3\,\text{Hz} = 0.38\,\text{W} \tag{4.96}$$

Where V_{GS} = 10V (Supply Voltage of the MOSFET driver), Q_G = 190 nC (MOSFET gate charge) [101]. The gate resistance R_G is calculated as follows;

$$R_G \geq \frac{V_{CC} - V_{EE} - V_{OL}}{I_{oLPEAK}} = \frac{10 - 0 - 0}{2.5\,\text{A}} = 4\,\Omega \tag{4.97}$$

Due to the high switching frequency of 200 kHz, the gate drive circuit has to be located close to the MOSFET gate. In addition, the drain and source pins and their PCB tracks are to be located far away as possible to avoid injecting any switching noise into the gate drive circuit. The gate drive printed circuit board design is given in the Appendix B.

4.4.8 Snubber Design

The leakage inductance of the isolation transformer causes a voltage spike to appear across the switch as it turns off [54]. This voltage spike leads to generation of EMI, increased switching losses, and may damage the switch if the voltage limit is exceeded [27] [54] [104]. Snubbers that have no loss and recycle the leakage energy can lead to higher efficiency [105], but at the expense of increased complexity and component count. To achieve a low cost snubber, an RCD overvoltage snubber is used [54]. The actual measured leakage inductance $L_{LK,PRI}$ was found to be 4.4 µH. The maximum V_{SW} = 519 V occurs when V_{in} = 380V, and V_o=34.71V; obtained from Equation (4.13). Figure 4.7 (a) shows a peak voltage spike of 860 V occurring as the switch turns off. This is a large spike and needs to be clamped to an acceptable level. To achieve this, an RCD snubber is designed using a procedure similar to [104]. The average power to be dissipated in the snubber, P_{sn}, when the switch is on is given as [104];

$$\begin{aligned} P_{sn} &= 0.5 \cdot L_{LK,PRI} \cdot {i_{LK,av}}^2 \cdot f_{sw} \\ &= 0.5 \times 4.4 \times 10^{-6}\,\text{H} \times 0.68\,\text{A}^2 \times 200 \times 10^3\,\text{Hz} = 0.203\,\text{W} \end{aligned} \tag{4.98}$$

Where $i_{LK,av}$ is the average current through the leakage inductance, which is equal to the current through the coupling capacitor C_a. P_{sn} is seen to be quite small, and would not drastically impact the efficiency of the driver. An acceptable voltage V_T, is chosen as 540 V as the maximum spike voltage to appear across the switch. Therefore the snubber voltage V_{sn} is found as [104];

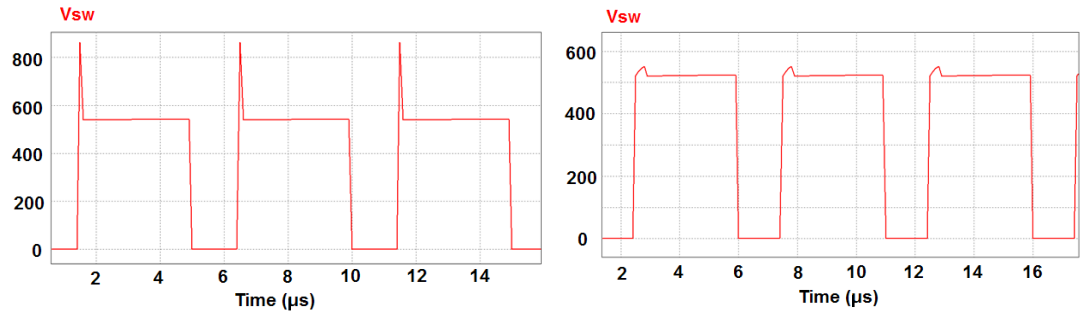
$$V_{sn} = V_T - V_{SW} = 540 - 519 = 21\,\text{V} \tag{4.99}$$

The snubber resistance R_{sn}, and snubber capacitance C_{sn} are found as [104];

$$R_{sn} = \frac{{V_{sn}}^2}{P_{sn}} = \frac{21\,\text{V}^2}{0.203\,\text{W}} = 2.17\,\text{k}\Omega \approx 2.2\,\text{k}\Omega \tag{4.100}$$

$$C_{sn} = \frac{T_{sw}}{R_{sn}} = \frac{5 \times 10^{-6}\,\text{s}}{2.2\,\text{k}\Omega} = 2.27\,\text{nF} \approx 2.2\,\text{nF} \tag{4.101}$$

The wattage of R_{sn} is chosen as 1 W, and for C_{sn}, a 2.2 nF, 1000 V capacitor ECKA3A222K is selected. The ultra-fast diode chosen is STTH310, which has ratings of 1000 V and 3A. Figure 4.6 shows the implemented snubber, which clamps the excessive voltage to an acceptable level as shown by the simulated result in Figure 4.7 (b).



(a) Without snubber (b) With designed snubber

Figure 4.7: Simulated switch voltage.

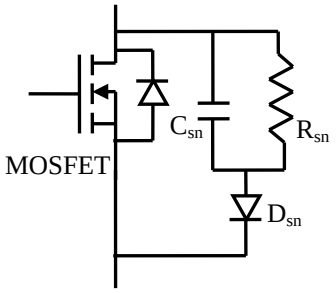


Figure 4.6: The implemented RCD snubber.

4.5 CHAPTER CONCLUSION

A single high power LED load of 88.5 W and three low power LED loads each of 29.5 W were designed. Effect of temperature on LEDs was practically done and forced cooling was adopted to keep the LED junction temperature in an acceptable range. The dynamic resistance model for the LED load was derived from the practical I-V curves at 38°C. The dimming levels were selected, given the minimum light output required. Following the LED load design, the operating parameters of the LED driver, an isolated cuk were chosen.

The isolation transformer was designed. The converter components such the coupling capacitors, MOSFET switch and diodes were sized and selected. Three inductor structures, NC, NSC and SC inductors were designed to enable practical investigation into the effects of inductor coupling types on driver performance to be done in Chapter 5. Finally, a snubber network to clamp the voltage spikes appearing across the active switch was designed to minimise EMI and switching losses.

CHAPTER 5 EFFECTS OF COUPLING ON THE CUK CONVERTER PERFORMANCE

A comprehensive analysis on performance of a cuk converter using three different inductor structures namely; Non-Coupled (NC), Symmetrically Coupled (SC) and Non-Symmetric Coupled (NSC) inductors has not been seen in available literature. Furthermore, for the SC and NSC inductors, the effect of coupling coefficient on performance is investigated; that is loose and tight coupling. This comprehensive analysis is key to identifying the inductor structure that offers the best converter performance to achieve high driver efficiency, high LED efficacy and optical output, possibility of maintaining long LED life and also achieve acceptable inductance size. Practical experimental evaluation using NC, tightly coupled SC and NSC is then finally done to validate the theoretical analysis. Finally, the SC (k = 0.98) is inductor structure chosen to implement the proposed LED driver, as it meets the high performance requirements needed.

5.1 CONVERTER PARAMETERS USED

For the purpose of this analysis, a cuk converter with the following specifications is used; input dc voltage V_{in} = 340 V; output voltage, V_o = 34.71 V; average input current, $I_{L_1,av}$ = 0.26 A; average output current, $I_{L_2,av}$ = 2.55 A; isolation transformer turns ratio, n =4; duty ratio, δ = 0.3; isolation transformer magnetising inductance, L_m = 1.312 mH; switch stress voltage, $V_{sw} = V_{in} + nV_o$ = 478.9 V; switch delay times, $t_{ri} + t_{fv} + t_{rv} + t_{fi}$ = 100 ns; active switch on resistance, $R_{DS,on}$ = 0.7 Ω; diode dynamic resistance, R_{fwd} = 0.03 Ω; diode forward voltage drop, V_{fwd} =1.2 V; coupling capacitor C_a ESR, r_{C_a} = 0.2 Ω; coupling capacitor C_b ESR, r_{C_b} = 0.2 Ω; isolation transformer primary winding resistance, r_{pri} = 0.127 Ω; and isolation transformer secondary winding resistance, $r_{\sec}$ = $6.85\times10^{-3}\Omega$. The input inductance resistance, r_{L_1} and output inductance resistance, r_{L_2} are calculated according the required inductances.

5.2 IMPACT OF COUPLING TYPE ON INPUT AND OUTPUT RIPPLE

The type of coupling used affects the input and output current ripple magnitudes. The coupling types considered are; Non-Coupled (NC), Symmetrically Coupled (SC) and Non-Symmetrically Coupled (NSC). For SC and NSC inductors, the coupling coefficient *k* considered is 0.5 and 0.98; to determine the effects of coupling on converter performance. The output inductance, L_2, is dependent on the input inductance L_1, for the coupled inductors case SC and NSC. For SC inductors, the output inductance L_2 is determined using (3.14), while for NSC inductors, the output inductance L_2 is determined using (3.16). The expression used to obtain the peak-peak current ripple percentage for L_1 NC and NSC inductors is given by;

$$i_{L_1}\ \%\,\text{current ripple}_{\text{pk-pk}} = \frac{V_{in}\cdot\delta\cdot 100}{f_{sw}\cdot i_{L_1,ave}\cdot L_1} \tag{5.3}$$

The expression used to obtain the peak-peak current ripple percentage for L_2 NC inductors is given by;

$$i_{L_2}\ \%\,\text{current ripple}_{\text{pk-pk}} = \frac{V_{in}\cdot\delta\cdot 100}{f_{sw}\cdot i_{L_2,ave}\cdot L_2} \tag{5.4}$$

The expression used to obtain the peak-peak current ripple percentage for L_1 and L_2 SC inductors and L_2 for NSC inductors is given by use of the control-to-output inductor transfer function $G_{iL_2\delta}(s)$ derived in Chapter 3 [106];

$$i_{L_1}\ \%\,\text{current ripple}_{\text{pk-pk}} = \left|Gi_{L_1\delta}(j2\pi f_{sw})\right|\frac{Sin(\pi\delta)\cdot 100}{\pi\cdot\delta\cdot i_{L_1,ave}} \tag{5.5}$$

$$i_{L_2}\ \%\,\text{current ripple}_{\text{pk-pk}} = \left|Gi_{L_2\delta}(j2\pi f_{sw})\right|\frac{Sin(\pi\delta)\cdot 100}{\pi\cdot\delta\cdot i_{L_2,ave}} \tag{5.6}$$

5.2.1 Symmetrically Coupled Inductors

Figures 5.1 and 5.2 show the effects of symmetric coupling of the input and output inductors on the input and output peak-peak current ripple respectively. NC inductor ripple is also plotted for comparison purposes. Equations (5.3) and (5.5) are used to plot the characteristics in Figure 5.1, while Equations (5.4) and (5.6) are used to plot the characteristics in Figure 5.2.

As seen in Figure 5.1, for a given inductance L_1 value, NC inductors yield higher current ripple than the SC inductors. SC (k = 0.98) inductors achieve a slightly lower ripple as compared with NC

inductors, but also have a higher ripple as compared with SC(k = 0.5) inductors between the range of 0.946mH and 5mH. For L_1 = 2mH, NC inductors yield a current ripple of 105%, SC (k = 0.98) and SC (k = 0.5) inductors yield 75% and 61% current ripple respectively. For this inductance value, there is a significant ripple reduction of 30% and 44% for SC (k = 0.98) and SC (k = 0.5) inductors respectively as compared to NC inductors.

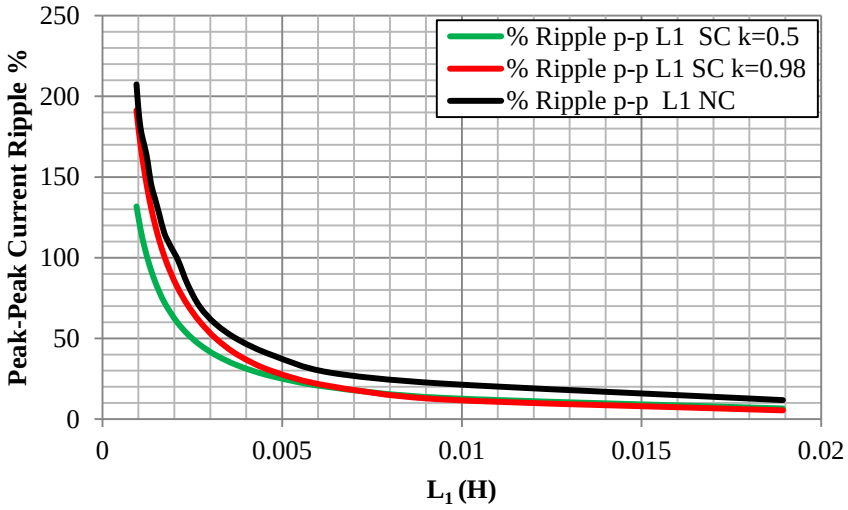


Figure 5.1: Peak-peak (p-p) current ripple plotted against inductance L_1 for SC and NC inductors

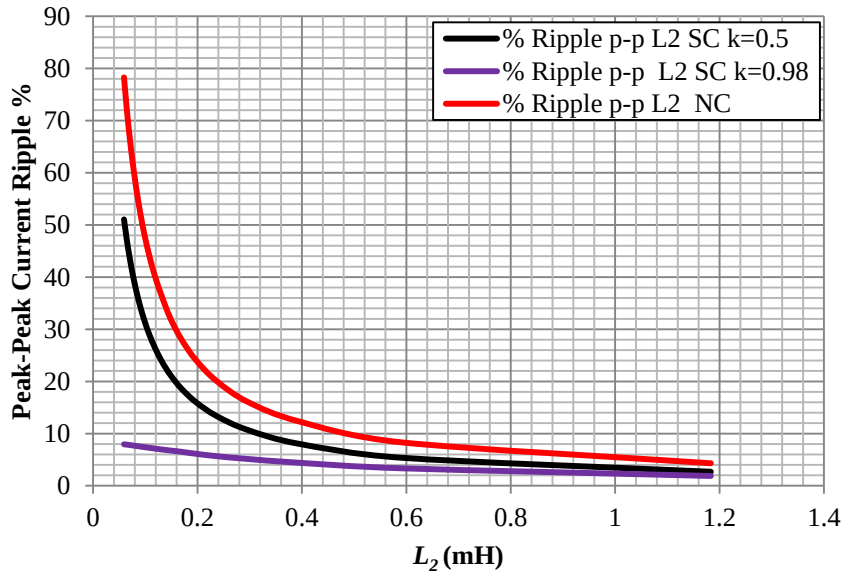


Figure 5.2: Peak-peak (p-p) current ripple plotted against inductance L_2 for SC and NC inductors.

As seen in Figure 5.2, for a given inductance value, NC inductors give rise to the highest peak-peak ripple magnitude, in comparison with SC inductors. SC (k = 0.5) exhibits a higher peak-peak ripple than SC (k = 0.98). For L_2 = 120 µH, NC inductors yield a current ripple of 40%, SC (k = 0.5) and SC (k = 0.98) inductors yield 26% and 6.5% current ripple respectively. For this inductance value, there is a significant ripple reduction. The values are 14% and 33.5% for SC (k = 0.5) and SC (k = 0.98) inductors respectively, as compared to NC inductors.

5.2.2 Non-Symmetrically Coupled Inductors

The input and output current ripple with respect to the NSC inductors sizes are plotted in Figures 5.3 and 5.4. The ripple due to NC inductors is plotted as a reference. Equation (5.3) is used to plot the characteristics in Figure 5.1, while Equations (5.4) and (5.6) are used to plot the characteristics in Figure 5.2.

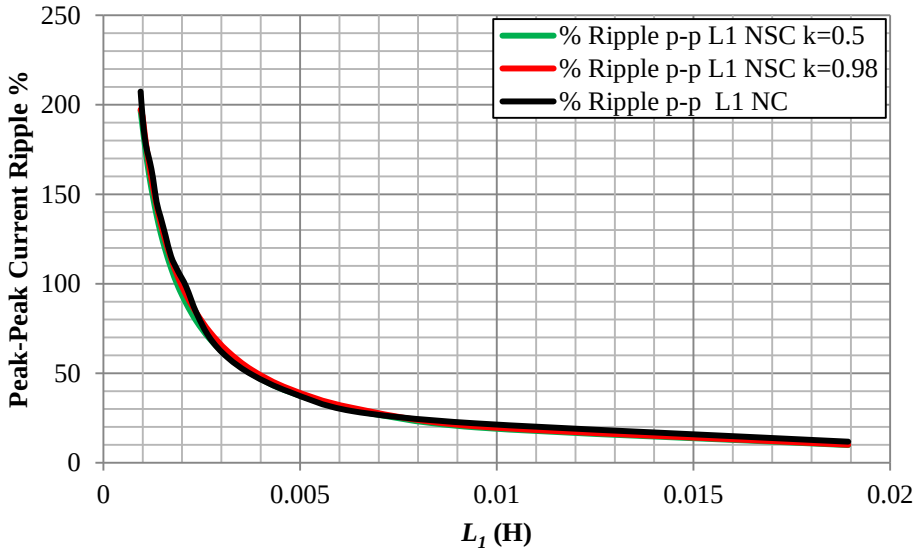


Figure 5.3: Peak-peak current ripple plotted against inductance L_1 for NSC and NC inductors.

From Figure 5.3, it is seen that the current ripple magnitudes are the same for both NC and NSC inductors. This is due to the ripple steering effect, where the output inductor ripple is steered to the input-side. From Figure 5.4, the NC inductors give rise to the highest ripple magnitude for all values of inductance, as compared to NSC inductors. Successful ripple steering is observed for the NSC inductors as the output current ripple is observed to be <2.2% and <0.02% for NSC (k = 0.98) and NSC (k = 0.5) respectively for all values of inductance. For a given inductance L_2 = 120 µH, the ripple for NC inductors is 40% and 2.1% and 0.02% for NSC (k = 0.98) and NSC (k = 0.5)

respectively. Thus NSC inductors (both k = 0.5 and k = 0.98) achieve a significant peak-peak ripple reduction of <37.9% as compared to NC inductors.

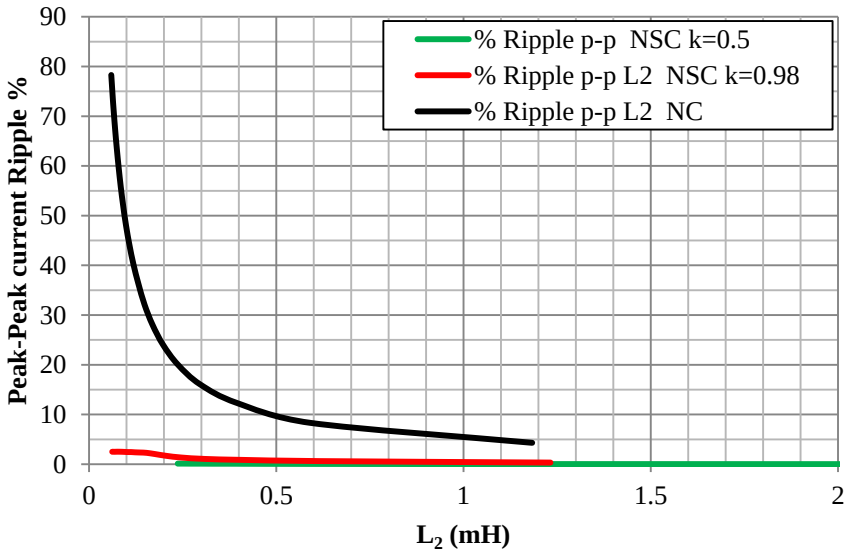


Figure 5.4: Peak-peak current ripple plotted against inductance L_2 for NSC and NC inductors

5.2.3 Comparison of Non-Coupled, Symmetrically Coupled and Non-Symmetrically Coupled Inductors

Table 5.1 shows the peak-peak current ripple percentage for various types of coupling and input inductance L_1 values;

Table 5.1: Peak-peak (p-p) current ripple percentage for L_1 and various types of coupling

L_1 (mH)	0.946	2	3	4	5	9
Ripple $_{p-p}$ NC	200%	105%	62%	46%	37%	22%
Ripple $_{p-p}$ SC (k=0.5)	130%	61%	40%	30%	15%	12%
Ripple $_{p-p}$ SC (k=0.98)	190%	75%	52%	35%	18%	12%
Ripple $_{p-p}$ NSC (k=0.5)	200%	105%	62%	46%	37%	22%
Ripple $_{p-p}$ NSC (k=0.98)	200%	105%	62%	46%	37%	22%

It is seen from Table 5.1 that for any given inductance value, that the input current ripple due to NC and NSC inductors is the same. SC (k = 0.5) inductors achieve the lowest peak-peak ripple for any given inductance value as compared to NC, NSC and SC (k = 0.98). For SC (k = 0.98) inductors, the peak-peak ripple is seen to be higher for a given inductance range of 0.946mH to 5mH as

compared to SC (k = 0.5) inductors, but this ripple is still lower than for NC and NSC inductors. At 3mH for SC (k = 0.98), the ripple percentage is 12% higher than SC (k = 0.5), but is 10% lower than NC and NSC inductors. The output inductance L_2 and the peak-peak ripple percentages for various coupling methods are given in Table 5.2.

Table 5.2: Peak-peak (p-p) current ripple percentage for L_2 and various types of coupling

L_2 (µH)	80	120	200	320	400	600	800
Ripple $_{p-p}$ NC	60%	40%	23.8%	15%	11%	10%	6.5%
Ripple $_{p-p}$ SC (k=0.5)	38.2%	26%	14.9%	10%	8%	5.5%	4.1%
Ripple $_{p-p}$ SC (k=0.98)	6.8%	6.5%	6.1%	4.5%	4.2%	3.6%	2.9%
Ripple $_{p-p}$ NSC (k=0.5)	<0.02%	<0.02%	<0.02%	<0.02%	<0.02%	<0.02%	<0.02%
Ripple $_{p-p}$ NSC(k=0.98)	2.2%	2.1%	1.9%	1.1%	0.9%	0.5%	0.4%

From Table 5.2, NC inductors achieve the highest ripple for any given inductance. SC (k = 0.5) achieves a lower ripple than that of NC inductors. For SC (k = 0.98) inductors, the ripple is significantly reduced as compared to NC and SC (k = 0.5) inductors.

NSC inductors give rise to the lowest output ripple as compared to NC and SC inductors. It is observed that NSC (k = 0.5) achieves the lowest ripple of <0.02% for the inductance range of 80-800 µH, whereas NSC (k = 0.98) achieves a ripple of <2.2% for the same range. Comparing NSC (k = 0.98) and SC (k = 0.98), there is no significant difference in terms of ripple magnitude for the entire range of inductance. At 120 µH, SC (k = 0.98) achieves a higher ripple of only 4.4% than NSC (k = 0.98), while at 400µH, SC (k = 0.98) achieves a higher ripple magnitude of 3.3% as compared to NSC (k = 0.98).

Despite the NSC achieving the lowest output ripple; it may not be the best choice if efficiency is an important consideration as seen in Section 5.3. It can be concluded that the performance of SC and NSC for k = 0.98 is fairly similar with respect to the output-side current ripple. As seen previously, the highest efficiency of the driver is noted when using SC (k = 0.98) inductors, and this may be the best choice so as to achieve the combination of highest efficiency and maintenance of low output ripple. In regard to the inductance sizes required as per a desired input or output current ripple, they are discussed in Section 5.5.

5.3 IMPACT OF COUPLING ON DRIVER EFFICIENCY

The driver efficiency is dependent on various types of losses occurring in the converter. The losses considered are semiconductor losses, copper losses, coupling capacitor losses and core losses in the magnetic components. Any other losses are neglected.

5.3.1 Semiconductor Losses

Semiconductor losses comprise switching losses in the active switch and conduction losses in both the diode and the active switch. Losses that may arise due to any switch voltage spikes are neglected. Switching loss in the controlled semiconductor switch is a function of the peak switch current $i_{sw,pk}$, and the switching loss $P_{sw,sw}$, is given by (4.83); and the conduction loss in the active switch $P_{sw,cond}$, is given by (4.84). The loss due to diode resistance $P_{D,cond}$, is given by (4.91). The loss in the diode due to the forward voltage drop $P_{D,thresh}$, is given by (4.93). Total semiconductor loss is finally obtained as;

$$P_{sem} = P_{D,cond} + P_{D,thresh} + P_{sw,cond} + P_{sw,sw} \tag{5.19}$$

5.3.2 Comparison of Semiconductor Loss for Different Coupling Types

Using the converter parameters given in Section 3.1, the effects of non-coupled (NC), symmetrically coupled (SC) and non-symmetrically coupled (NSC) inductors on the semiconductor losses are investigated. For SC and NSC inductors, the coupling coefficient *k* considered is 0.5 and 0.98.

As seen from Figure 5.5, for all types of coupling, the semiconductor loss P_{sem} reduces with increase in inductance size. This is due to the reduction of the peak-peak inductor currents, consequently reducing the switch peak and RMS current, and in turn resulting in semiconductor loss reduction. In comparison to SC and NSC inductors, NC inductors exhibit the highest P_{sem} of 13.76W for L_1 = 0.9646 mH and gradually drops to 11.27 W for L_1=18.93 mH. NC inductors have the highest P_{sem} as it has the highest peak-peak inductor currents both on the input and the output.

The loss P_{sem} for SC inductors is very similar for both coupling coefficients *k* of 0.5 and 0.98. The coupling coefficient has little or no effect on P_{sem}. It is observed that SC inductors for both *k* = 0.5

and 0.98 achieve a lower dissipation P_{sem} for a given inductance L_1 value. For L_1 = 0.946 mH, P_{sem} = 12.8 W, and for L_1 = 18.93 mH, P_{sem} = 11.218 W. In comparison to NC inductors, SC inductors reduce power dissipation by 0.96 W and 0.052 W for L_1 values of 0.946 mH and 18.93 mH respectively.

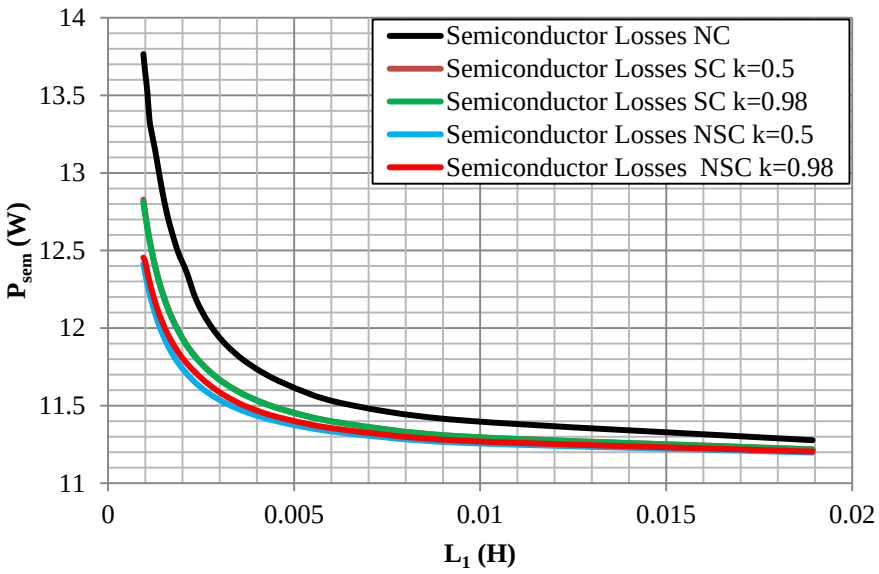


Figure 5.5: Semiconductor losses for various types of inductor coupling

NSC inductors exhibit the lowest dissipation P_{sem} in comparison to NC and SC inductors. For NSC inductors, the losses are seen to be slightly lower when k = 0.5 as compared to when k = 0.98 for a given value of inductance. When k = 0.98, P_{sem} is 12.45 W and 11.2 W for inductance size L_1 of 0.946 mH and 18.93 mH respectively. For k = 0.5, P_{sem} is 12.41 W and 11.19 W for inductance size L_1 of 0.946 mH and 18.93 mH respectively.

Table 5.3: Semiconductor power loss P_{sem} for various types of coupling

L_1		0.946 mH	18.93 mH
P_{sem} **(NC)**	k = 0	13.76 W	11.27 W
P_{sem} **(SC)**	k = 0.5	12.8 W	11.218 W
	k = 0.98	12.8 W	11.218 W
P_{sem} **(NSC)**	k = 0.5	12.41 W	11.19 W
	k = 0.98	12.45 W	11.2 W

In comparison to NC inductors, the loss P_{sem} for NC inductors (k = 0.98) is lower by 1.31 W at L_1 = 0.946 mH and 0.08 W at L_1 = 18.93 mH. In comparison to SC inductors, the loss P_{sem} for NC inductors (k = 0.98) is lower by 0.39 W at L_1 = 0.946 mH and 0.018 W at L_1 = 18.93 mH. A summary of the losses at particular inductance values is given in Table 5.3.

5.3.3 Coupling Capacitor Losses

The losses considered in the coupling capacitors C_a and C_b are due to the ESR r_{C_a} and r_{C_b} respectively. The output capacitor is not used in this analysis and its ESR is neglected. The power loss in the coupling capacitor C_a is given by;

$$P_{C_a} = I_{Ca,RMS}{}^2 \cdot r_{C_a} \tag{5.20}$$

Where;

$$I_{Ca,RMS} = \sqrt{\delta \cdot \frac{1}{3} \cdot \left(I_{Ca,H_1}{}^2 + I_{Ca,H_1} I_{Ca,L_1} + I_{Ca,L_1}{}^2\right) + (1-\delta) \cdot \frac{1}{3} \cdot \left(I_{Ca,H_2}{}^2 + I_{Ca,H_1} I_{Ca,L_2} + I_{Ca,L_2}{}^2\right)} \tag{5.14}$$

$$I_{Ca,H_1} = \frac{\Delta i_{L_m p-p}}{2} - \left(\frac{I_{L_2,av}}{2} - \frac{\Delta i_{L_2 p-p}}{2 \cdot n}\right) \tag{5.21}$$

$$I_{Ca,L_1} = \frac{-\Delta i_{L_m p-p}}{2} - \left(\frac{I_{L_2,av}}{2} + \frac{\Delta i_{L_2 p-p}}{2 \cdot n}\right) \tag{5.22}$$

$$I_{Ca,H_2} = I_{L_1,av} + \frac{\Delta i_{L_1 p-p}}{2} \tag{5.23}$$

$$I_{Ca,L_2} = I_{L_1,av} - \frac{\Delta i_{L_1 p-p}}{2} \tag{5.24}$$

The power loss in the coupling capacitor C_b is given by;

$$P_{C_b} = I_{Cb,RMS}{}^2 \cdot r_{C_b} \tag{5.25}$$

Where;

$$I_{Cb,RMS} = \sqrt{\delta \cdot \frac{1}{3} \cdot \left(I_{Cb,H_1}{}^2 + I_{Cb,H_1} I_{Cb,L_1} + I_{Cb,L_1}{}^2\right) + (1-\delta) \cdot \frac{1}{3} \cdot \left(I_{Cb,H_2}{}^2 + I_{Cb,H_1} I_{Cb,L_2} + I_{Cb,L_2}{}^2\right)} \tag{5.20}$$

$$I_{Cb,H_1} = -I_{L_2,av} + \frac{\Delta i_{L_2 p-p}}{2} \tag{5.26}$$

$$I_{Cb,L_1} = -I_{L_2,av} - \frac{\Delta i_{L_2 p-p}}{2} \tag{5.27}$$

$$I_{Cb,H_2} = \left(\frac{I_{L_1,av}}{2} + \frac{\Delta i_{L_1 p-p}}{2} + \frac{\Delta i_{L_m p-p}}{2} \right) \cdot n \tag{5.28}$$

$$I_{Cb,L_2} = \left(\frac{I_{L_1,av}}{2} - \frac{\Delta i_{L_1 p-p}}{2} - \frac{\Delta i_{L_m p-p}}{2} \right) \cdot n \tag{5.29}$$

The total capacitor losses P_c is given by;

$$P_C = P_{C_a} + P_{C_b} \tag{5.30}$$

5.3.4 Comparison of Power Loss in Coupling Capacitors for Various Inductor Coupling Types

As seen from Figure 5.6, it is the NC inductors that yield the highest power dissipation, P_c. For L_1 = 0.946 mH and 18.93 mH, P_C is 0.77 W and 0.6 W respectively. NC inductors give rise to the highest power dissipation as compared to SC and NSC inductors due to the higher ripple current on both the input and output inductors, and result in a higher RMS current through the coupling capacitors C_a and C_b.

In the case of NSC inductors the loss is very similar regardless of the coupling coefficient used. It can be concluded that for NSC inductors, the coupling coefficient used has little effect on the capacitor losses. NSC inductors achieve slightly lower capacitor loss P_c as compared to the NC inductors. For L_1 = 0.946 mH and 18.93 mH, P_c is 0.736 W and 0.6 W respectively. For SC inductors, there is a significant difference in P_c when the coupling coefficient k = 0.5 and when 0.98. For a coupling coefficient k = 0.5, the highest loss is 0.69 W dropping to 0.6 W for inductance value L_1 for 0.946mH and 18.93mH respectively.

When k = 0.98, P_C does not vary significantly as the inductance is increased. P_C for k = 0.98 is observed to be 0.068 W, and this value is lower by 0.7 W as compared with NC inductors at 0.946 mH. SC inductors (k = 0.98) achieve the lowest RMS current through the coupling capacitors and results in the lowest loss P_C of 0.068W as compared to NC, SC (k = 0.5) and NSC.

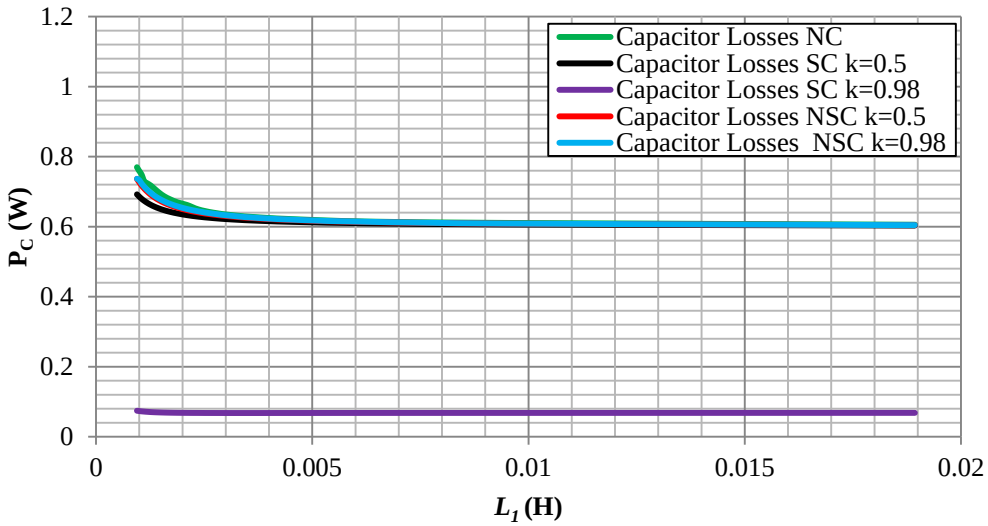


Figure 5.6: Capacitor losses for various types of inductor coupling

Table 5.4: Capacitor power loss P_C for various types of coupling

L_1		0.946 mH	18.93 mH
P_C **(NC)**	k=0	0.77 W	0.6 W
P_C **(SC)**	k=0.5	0.69 W	0.6 W
	k=0.98	0.068 W	0.068 W
P_C **(NSC)**	k=0.5	0.736 W	0.6 W
	k=0.98	0.736 W	0.6 W

5.3.5 Copper Losses

The copper losses considered are due to the resistive elements of the inductors and isolation transformer windings. Change in the winding resistances with increase in inductance is considered. The current density in the conductors is taken to be constant for all inductance values. To obtain the resistance of the inductor windings, the conductor number of turns N_{L_1} and N_{L_2} are given by;

$$N_{L_1} = \sqrt{\frac{L_1 \cdot l_g}{\mu_o \cdot \mu_r \cdot A_e}} \tag{5.31}$$

$$N_{L_2} = \frac{N_{L_1}}{n} \tag{5.32}$$

Where l_g is the air-gap length taken as 0.1 mm, μ_o is $4\pi \times 10^{-7}$ H/m, μ_r is taken as 1, and A_e is the winding window area (taken as 0.169×10^{-3} m for a PQ32/20 Core). For inductors L_1 and L_2, AWG 28 and AWG 19 are used respectively. The resistances of AWG 28 (r_{AWG28}) and AWG 19 (r_{AWG19}) are 0.21424 Ω/m and 0.02636 Ω/m at 100°C respectively. The actual resistances r_{L_1} and r_{L_2} are determined by Equation (4.31) and (4.33) respectively, where MLT is taken as 6.67×10^{-2} m for a PQ32/20 core. The copper loss in inductor L_1 is given by;

$$P_{L_1} = I_{L_1,RMS}{}^2 \cdot r_{L_1} \tag{5.35}$$

Where;

$$I_{L_1,RMS} = I_{L_1,av}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L_1 p-p}}{2 \cdot I_{L_1,av}}\right)^2} \tag{5.36}$$

Similarly, the copper loss in inductor L_2 is given by;

$$P_{L_2} = I_{L_2,RMS}{}^2 \cdot r_{L_2} \tag{5.37}$$

Where;

$$I_{L_2,RMS} = I_{L_2,av}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L_2 p-p}}{2 \cdot I_{L_2,av}}\right)^2} \tag{5.38}$$

The current flowing through the primary transformer winding is the same as the current though capacitor C_a. Copper loss in primary transformer winding is obtained as;

$$P_{pri} = I_{Ca,RMS}{}^2 \cdot r_{pri} \tag{5.39}$$

Similarly, the current flowing through the secondary transformer winding is the same as the current though capacitor C_b. The copper loss power loss in secondary winding is;

$$P_{\text{sec}} = I_{Cb,RMS}{}^2 \cdot r_{\text{sec}} \tag{5.40}$$

Finally, the total copper loss is obtained as;

$$P_{copper} = P_{L_1} + P_{L_2} + P_{pri} + P_{\text{sec}} \tag{5.41}$$

5.3.6 Comparison of Copper Loss for Various Inductor Coupling Types

As shown in Figure 5.7, NC inductors have the highest copper loss. This is due to the larger inductor current ripple on both the input and output-side, resulting in a higher RMS current.
The highest copper loss is observed for NC inductors as 2.03 W at L_1 = 0.946 mH, and drops to a minimum of 1.8 W at 3.5 mH. The loss then increases linearly to 1.9 W at inductance value L_1 of 18.93 mH.

The copper loss for NSC inductors is similar for both coupling coefficients of 0.5 and 0.98. The highest power loss for NSC is noted as 1.94 W at L_1 = 0.946 mH, and drops to a minimum of 1.8 W at 3.5 mH. The loss increases linearly again to 1.9 W at L_1=18.93 mH. The reason for the similarity is that regardless of the coupling coefficient, NSC inductors minimize the output current ripple of which the magnitude is comparable when k = 0.5 and k = 0.98. On the input-side, the current ripple magnitude is the same regardless of the coupling coefficient. This results in very similar copper losses despite the difference in coupling coefficient. This increase of loss is attributed to the increase of winding resistance with increase in inductance.

After inductance L_1 is increased beyond 3.5 mH, the losses are seen to be fairly similar for both NC and NSC inductors. SC (k = 0.5) achieves a slightly lower copper loss than compared to NC and NSC inductors, but only up to inductance L_1 value of approximately 5 mH. After this, the losses for SC (k = 0.5) is closely similar to NC and NSC inductors. The highest copper loss exhibited by SC (k = 0.5) is 1.81 W at L_1 = 0.946 mH and the minimum loss of 1.71 W is observed at L_1=2.5 mH.
SC (k = 0.98) exhibits the lowest loss as compared to NC, NSC and SC (k = 0.5) inductors. This is due to the lowest RMS currents that SC (k = 0.98) inductors achieve.

As seen with NC, NSC and SC (k = 0.5) inductors, the highest power loss occurs with the lowest value of inductance (L_1 = 0.946 mH). For SC (k = 0.98), the lowest power loss occurs at the lowest inductance value. It is also noted that there is no minimum loss point for SC (k = 0.98) as seen with the other inductor coupling types. Instead, the power loss increases fairly linearly with increase in inductance size. Therefore, this characteristic of SC (k = 0.98) inductors can allow the choice of a small sized inductor, while minimizing the loss; contrary to the characteristics of NC, NSC and SC (k = 0.5).

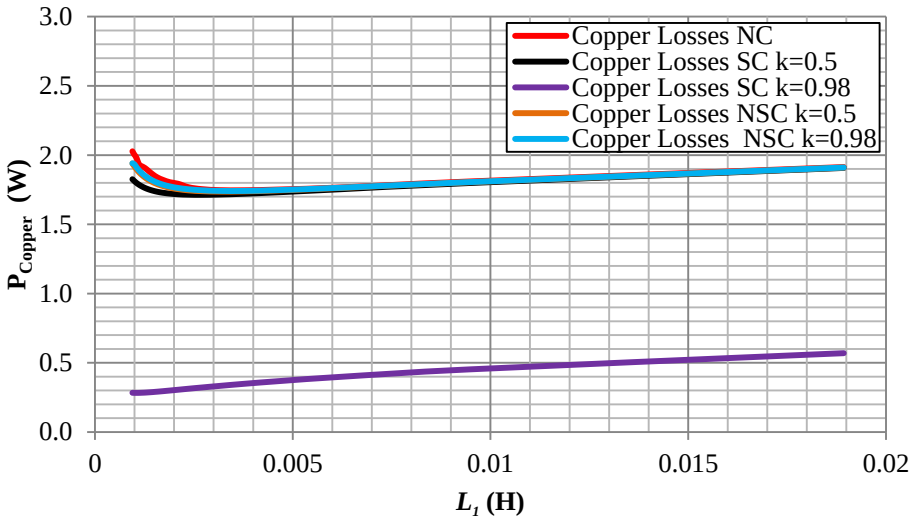


Figure 5.7: Copper losses for various types of inductor coupling

The lowest and highest copper loss for SC (k = 0.98) is 0.29 W and 0.58 W for inductance L_1 values of 0.946 mH and 18.93 mH respectively. Considering power loss at L_1 = 2 mH, SC (k = 0.98) reduces power loss significantly by 1.5 W as compared to NC inductors. A tabular comparison of the copper losses is done in Table 5.5.

Table 5.5: Copper loss P_{copper} for various types of coupling

L_1		0.946 mH	18.93 mH	Inductance at minimum loss
P_C (NC)	k = 0	2.03 W	1.9 W	1.8 W at 3.5 mH
P_C (SC)	k = 0.5	1.81 W	1.9 W	1.71 W at 2.5 mH
	k = 0.98	0.29 W	0.58 W	No minimum loss
P_C (NSC)	k = 0.5	1.94 W	1.9 W	1.8 W at 3.5 mH
	k = 0.98	1.94 W	1.9 W	1.8 W at 3.5 mH

5.3.7 Magnetic Core Losses

The core losses in the inductors and the isolation transformer are considered. Losses due to harmonics are neglected for simplicity.

5.3.7.1 Inductor Core Losses

The peak flux density in the ferrite core is required to determine the core loss, and is given by follows for the first inductor L_1;

$$\Delta B_{L_1} = \frac{L_1 \cdot \Delta i_{L_{1p-p}}}{2 \cdot N_{L_1} \cdot A_e} \tag{5.42}$$

Similarly for the second inductor L_2, the peak flux density is given by;

$$\Delta B_{L_2} = \frac{L_2 \cdot \Delta i_{L_{2p-p}}}{2 \cdot N_{L_2} \cdot A_e} \tag{5.43}$$

Using Equations (5.38) and (5.39), the core loss of the selected ferrite material is determined from the manufacturers' data [99] and is used to determine the ferrite material core loss. The total core losses in the selected core are a function of the peak flux density and are determined by;

$$P_{C,L} = A_e \cdot l_m \left(P_{vL_1,core} + P_{vL_2,core} \right) \tag{5.44}$$

Where $P_{vL_1,core}$ and $P_{vL_2,core}$ are the power dissipation of the ferrite material at the calculated peak flux density ΔB_{L_1} and ΔB_{L_3} respectively, at the given switching frequency. l_m is the mean magnetic length of the selected core (l_m is 55.5×10^{-3} m for a PQ32/20 core) and A_e is the core cross sectional area (A_e is 0.169×10^{-3} m for a PQ32/20 core). The ferrite material chosen is N87 from EPCOS [99] and the switching frequency is 200 kHz.

5.3.7.2 Isolation Transformer Core Losses

Core loss in the isolation transformer is obtained by [27];

$$P_{C,Tx} = k_{fe} \cdot (\Delta B)^{\beta} \cdot A_c \cdot l_m \tag{5.45}$$

Where k_{fe} and β are the core loss coefficient and core loss exponent, dependent on the selected material properties. A_c is the core magnetic cross-section (for the E19/8/5 core it is 22.5×10^{-6} m) and l_m is the magnetic mean length (for the E19/8/5 core it is 46.7×10^{-3} m). The peak flux density is further given by [27];

$$\Delta B = \left[\frac{\rho \cdot \left(\delta \cdot T_{sw} \cdot V_{in}\right)^2 \cdot {I_{TOT}}^2}{2 \cdot k_{cu}} \cdot \frac{MLT}{W_A \cdot {A_c}^3 \cdot l_m} \cdot \frac{1}{\beta \cdot k_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \tag{5.46}$$

Where ρ is the conductor resistivity (for copper it is 17.24×10^{-9} Ω-m at 100°C), k_{cu} is the copper fill factor (taken as 0.3), MLT is the mean length of one turn (for the E19/8/5 core it is 32.8×10^{-3} m) and W_A is the winding area (for the E19/8/5 it is 28.4×10^{-6} m^2). Furthermore, the total current I_{TOT} passing through the windings is given as follows where *n* is the turns ratio;

$$I_{TOT} = I_{pri,_{RMS}} + \frac{I_{\sec,_{RMS}}}{n} \tag{5.47}$$

The selected core is E19/8/5 and the ferrite material is N87 [99]. For operation at 200 kHz switching frequency, k_{fe} and β are obtained as 32.9×10^{-6} W/T$^{\beta}$m^3 and 2.54 respectively [99].

5.3.8 Comparison of Inductor Core Loss for Various Coupling Types

From Figure 5.8, the highest core loss is exhibited by NC inductors. The power loss is 1.23×10^{-3} W for inductance L_1 = 0.946 mH, and reduces inversely with increase in inductance to 0.05×10^{-3} W for inductance value L_1 = 18.93 mH. Inductor core losses for NSC inductors (both k = 0.5 and k = 0.98) are very similar. Although NSC (k = 0.5) exhibits a slightly lower loss than NSC (k = 0.98). The inductor core losses for NSC (k = 0.98) and NSC (k = 0.5) inductors are 0.66×10^{-3} W and 0.6×10^{-3} W for L_1 at 0.946 mH respectively.

SC inductors achieve the lowest inductor core losses as compared to NC and NSC inductors. This is due to the lower peak-peak current ripple in the inductors which lead to a smaller hysteresis loop; which consequently leads to lower core loss. SC (k = 0.98) exhibits a slightly higher core loss as compared to SC (k = 0.5). For inductance L_1 of 0.946 mH, SC (k = 0.98) and SC (k = 0.5) have inductor core losses of 0.6×10^{-3} W and 0.45×10^{-3} W respectively. However, after inductance L_1 of about 5 mH, the core losses are similar for both coupling coefficients. For inductance L_1 = 2 mH, SC (k = 0.98) inductors have a lower loss difference of 0.31×10^{-3} W than NC inductors.

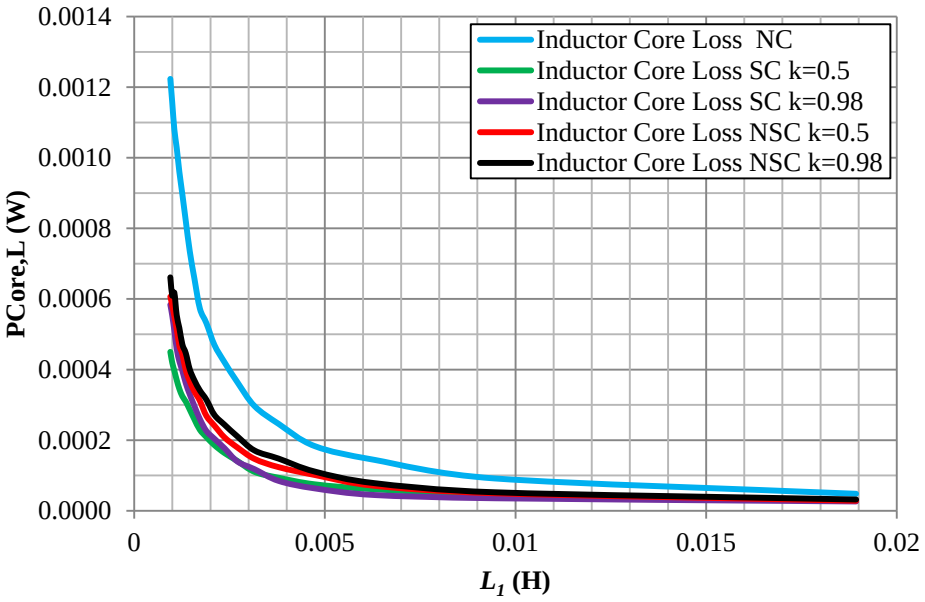


Figure 5.8: Inductor core losses for different coupling types.

SC inductors achieve the smallest inductor core losses as compared to NC and NSC inductors. However, SC (k = 0.5) inductors achieve the lowest loss as compared to SC (k = 0.98). Considering the benefits of SC (k = 0.98) on copper losses, choosing a coupling coefficient of 0.98 may not have a significant impact on the core loss. This is because the core losses exhibited by both SC (k = 0.5) and SC (k = 0.98) are fairly small relative to the losses of NC inductors.

5.3.9 Comparison of Isolation Transformer Core Loss for Various Coupling Types

From Figure 5.9, NC inductors have the highest transformer core losses. This is due to the higher RMS currents flowing through the isolation transformer primary and secondary windings as compared to NSC and SC inductors.

The peak core loss for NC inductors is seen to be 0.251 W for inductance L_1 of 0.946 mH. However, after inductance L_1 is increased beyond 5 mH, the loss remains fairly constant at 0.225 W. NSC (k = 0.5), NSC (k = 0.98) and SC (k = 0.5) inductors have closely similar core losses. For inductance L_1 of 0.946 mH and 18.93 mH, the losses are 0.245 W and 0.225 W respectively.

SC (k = 0.98) shows the lowest core loss, and is fairly constant at 0.13 W for inductance L_1 values in the range of 1.5 mH to 18.93 mH. The peak loss for SC (k = 0.98) inductors is seen to be 0.139

W at inductance L_1 = 0.946 mH. For L_1 = 2 mH, SC (k = 0.98) inductors achieve a lower loss difference of 0.105 W as compared to NC inductors. Therefore, SC (k=0.98) inductors are the best choice so as to minimize the transformer core losses.

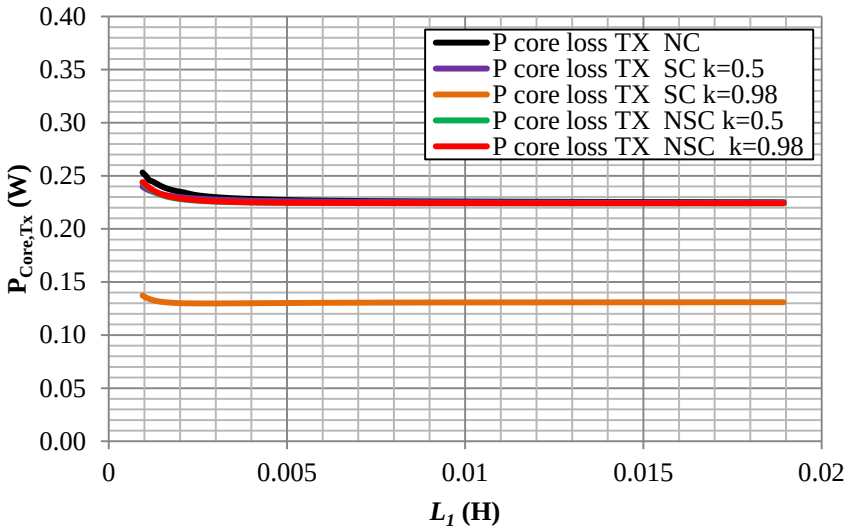


Figure 5.9: Transformer core losses for different coupling types.

5.3.10 Comparison of Total Power Loss for Various Inductor Coupling Types

The total power loss P_{total} in the driver is compared for various types of coupling. P_{total} is obtained by summing the considered losses; Semiconductor losses P_{sem}, capacitor losses P_C , copper losses P_{copper}, inductor core losses $P_{Core,L}$ and transformer core losses $P_{Core,Tx}$. The NC inductors, exhibit the highest total loss, P_{total}, as compared to SC and NSC inductors as seen in Figure 5.10. The loss is noted as 16.8 W and 14.05 W for inductance values L_1 of 0.946 mH and 18.93 mH respectively.

NSC and SC (k = 0.5) inductors show close similarity in power loss given an inductance value. Despite this, SC (k = 0.5) inductors show a slightly higher power dissipation than NSC inductors. The peak loss for SC (k = 0.5) inductors is 15.6 W and 13.9 W for inductance values L_1 of 0.946 mH and 18.93mH respectively. Thus SC (k = 0.5) reduces P_{total} by 1.2 W and 0.15 W for inductance values L_1 of 0.946 mH and 18.93 mH respectively.

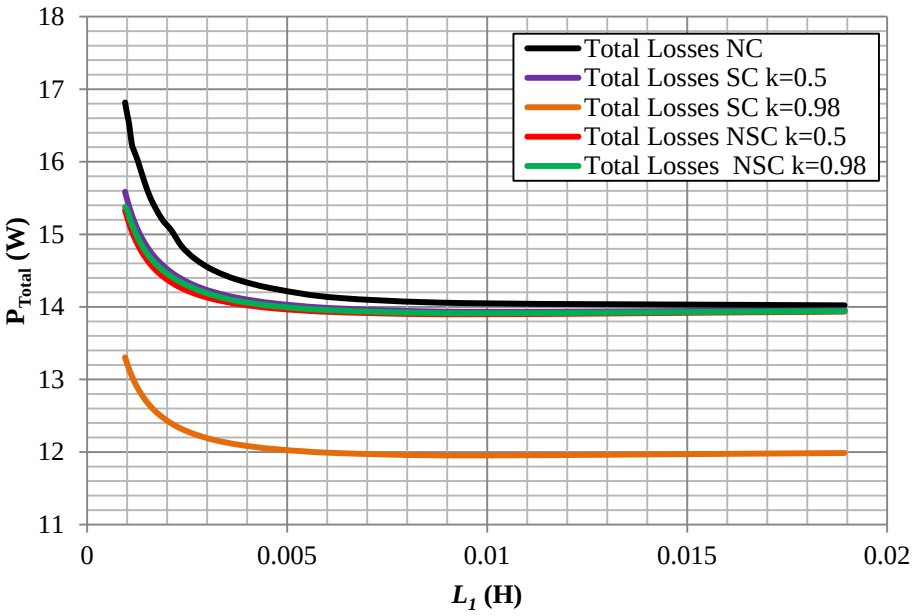


Figure 5.10: Total driver losses for various types of inductor coupling.

For NSC inductors, the total losses do not differ significantly despite the difference in coupling coefficient used. NSC inductors achieve similar P_{total} reduction as SC (k = 0.5).

The lowest loss is exhibited by SC (k = 0.98) inductors. The peak loss for this case is 13.25 W and 12 W for inductance values L_1 of 0.946 mH and 18.93 mH respectively. Compared to NC inductors, SC (k = 0.98) inductors achieve a reduction in total power loss of 3.55 W and 2.05 W for inductance L_1 values of 0.946 mH and 18.93 mH respectively. Hence SC (k = 0.98) is expected to achieve the highest efficiency as compared to all the other coupling types presented.

5.4 IMPACT OF COUPLING ON THE LED LOAD EFFICACY

LED efficacy is impacted upon by the ripple magnitude [38]. Furthermore, the LED efficacy and light output are affected by the current ripple shape; for the same magnitude, triangular ripple results in higher efficacy and light output as compared to sinusoidal ripple [38]. Table 5.6 shows the efficacy and light output of an LED for various ripple magnitudes, both sinusoidal and triangular. From Table 5.6, the triangular shaped ripple of up to 50% peak-peak, can maintain high efficacy and light output >99%.

Table 5.6: Effect of Ripple on LED efficacy and light output [38]

Peak-Peak Ripple	Current Ripple Shape	Efficacy	Light Output
25%	*Triangular*	>99%	>99%
	Sinusoidal	97.5%	98%
50%	*Triangular*	>99%	>99%
	Sinusoidal	96%	97.5%
100%	*Triangular*	96%	98%
	Sinusoidal	89.5%	95%

5.4.1 Non-Coupled Inductors

When no output capacitor is used for the NC inductor cuk converter, the output current ripple waveform is triangular in shape. To maintain LED efficacy >99% the minimum inductance L_2 required on the output-side to maintain a peak-peak current ripple of 50% is 100 µH. The input and output inductors L_1 and L_2 respectively of the NC inductor cuk converter can be sized independently. However, using separate inductors is more costly and bulky as compared to using coupled inductors.

5.4.2 Non-Symmetrically Coupled Inductors

Using NSC inductors achieves a very low output ripple that maintains the LED efficacy and light output >99%. As seen previously, k = 0.5 and k = 0.98 achieve a peak-peak ripple percentage of <0.02% and <2.2% for the inductance in the range of 80-800 µH. Thus NSC inductors are the best choice to maintain high LED efficacy and light output. However, they may not be the optimum choice with regard to driver efficiency, as NSC inductors achieve a lower efficiency as compared to SC inductors.

5.4.3 Symmetrically Coupled Inductors

The output current ripple shape is triangular when no output capacitance is used. SC (k=0.5) inductors would maintain an LED efficacy and light output of >99% as the highest ripple observed from Figure 5.2 at the minimum inductance of 60µH is 50%. The ripple value drops to 38.2% and 14.9% for 80µH and 200µH respectively.

SC (k = 0.98) inductors achieve a low ripple of < 6.8% for all inductance L_2 values, and would maintain a high LED efficacy and light output of >99%. However, inductance L_2 cannot be so small as it would impact the sizing of L_1; where the input current ripple has to be in an acceptable range. As seen in Section 3.3, SC (k = 0.98) achieves the lowest driver losses as compared to SC (k = 0.5). Since both coupling coefficients of 0.5 and 0.98 maintain an LED efficacy and light output of >99%, the best choice would be to select SC (k = 0.98). This would ensure the highest driver efficiency and the highest LED efficacy and light output. Furthermore, the low output current ripple of <6.8% that SC (k = 0.98) inductors achieve would eliminate the use of any output filtering capacitor, reducing component count and cost.

5.5 IMPACT OF COUPLING ON INDUCTANCE SIZE

The type of coupling used has an impact on the size of input and output inductance for a given peak-peak ripple percentage value. A comparison between NC, SC and NSC inductors is done in this sub-Section.

From Figure 5.11, the inductance values of NC and NSC inductors are the same given a ripple magnitude. The SC (k = 0.5) inductors achieve lowest inductance given a particular ripple magnitude. When the coupling coefficient k is increased to 0.98, the required inductance for the same given ripple magnitude is larger. When coupling coefficient k is 0.5 and 0.98, the required inductance to keep input peak-peak current ripple at 50% is 2.5 mH and 3.3 mH respectively. For the same ripple, NC and NSC inductance L_1 is 3.9 mH.

Since SC (k = 0.98) achieves the lowest driver losses as compared to NC, NSC and SC (k = 0.5) inductors, a tradeoff between inductance size and efficiency is needed. If an input peak-peak ripple of 50% and SC were to be selected due to the lower inductance value it achieves, SC (k = 0.98) would require 0.8 mH additionally as compared to SC (k = 0.5). This is not a significant inductance increase, and SC (k = 0.98) would achieve the lowest driver losses as seen in Section 3.3. NC and NSC are not considered as they require larger inductance and result in higher driver losses. Furthermore, NC inductors result in separate inductances, increasing volume and cost as compared to the coupled counterparts.

From Figure 5.12, for a given inductance value, NC inductors achieve the highest ripple as compared to SC and NSC inductors. For NSC inductors, the output ripple is independent of output

L_2 inductance value. Therefore, any selection of inductance size will result in < 2.2% output peak-peak current ripple. SC (k = 0.5) shows a non-linear progression of inductance size L_2 against output peak-peak ripple, similar to NC inductors. For a ripple of 50%, L_2 is 62.5 µH and 98.6 µH for SC (k = 0.5) and NC inductors respectively. SC (k = 0.98) achieves a significantly lower ripple for the same inductance size as compared to NC and SC (k = 0.5). SC (k = 0.98) inductors achieve a ripple of <6.8% for the same inductance values of SC (k = 0.5) and NC inductors. When the inductance is varied from 68.75 µH to 337.5µH, the corresponding change in ripple for SC (k=0.98) is 3.5%. This is not a significant variation, and this feature allows for selection of any output inductance size.

SC (k = 0.98) inductors exhibit the lowest driver losses, and can maintain LED efficacy and light output >99%. Furthermore, the insignificant variation of 3.5% aids in making the output inductance value independent of the input ripple and inductance size. In other words, a selection of the input inductance as per a given input-side ripple has little effect on the output ripple magnitude.

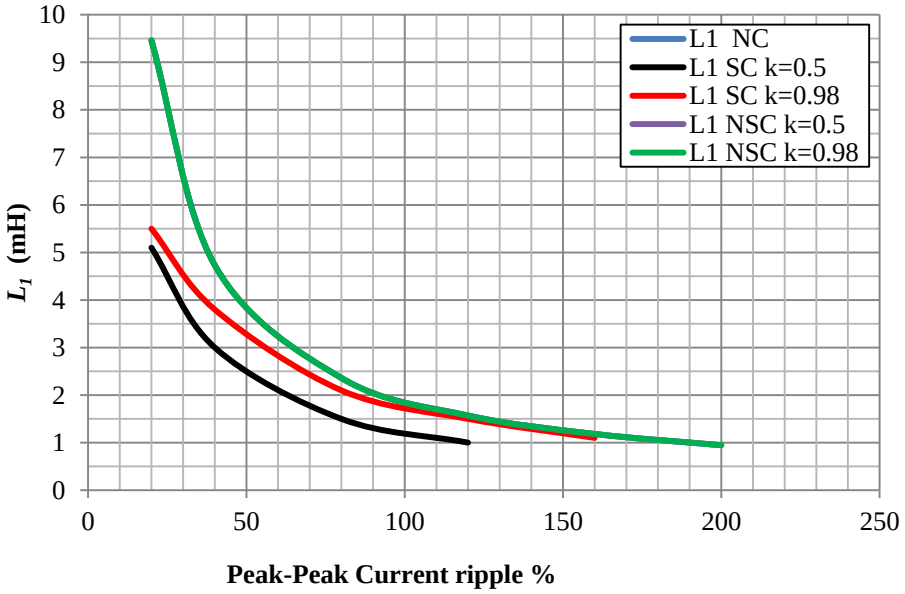


Figure 5.11: L_1 plotted against peak-peak current ripple for NC, SC and NSC inductors.

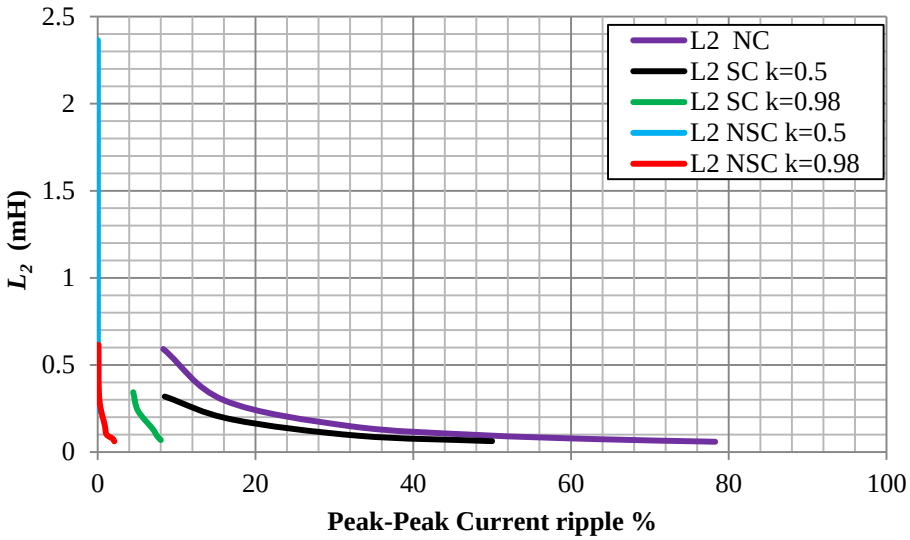


Figure 5.12: L_2 plotted against peak-peak current ripple for NC, SC and NSC inductors.

5.6 PRACTICAL VALIDATION OF DRIVER PERFORMANCE FOR VARIOUS INDUCTOR TYPES

To validate the theoretical analysis, a practical experiment is performed by operating the cuk converter with each of the inductor structures; NC, SC and NSC inductors. The design of the inductors used was shown in Chapter 4. The coupling coefficient of the coupled inductors is selected as 0.98, therefore only tight coupling is considered practically.

5.6.1 Inductor Selection

The three structures NC, SC and NSC inductors used are designed so that the input inductance L_1 is 2 mH for all of them. This value of inductance is chosen as it results in acceptable inductance size and acceptable input current ripple percentage for continuous conduction mode. Referring to Figures 3.1 and 3.3, for L_1 = 2 mH, the input peak-peak current ripple is 100%, 85%, and 100% for NC, SC and NSC inductors respectively.

The corresponding output inductances for SC and NSC inductors is found using Equations (3.1) and (3.2). For NC inductors, the output inductance used is equal to the SC inductor. Thus L_2 is found as 125 µH, 125 µH and 130.15 µH for NC, SC and NSC inductors. Referring to Figures 3.2 and 3.4, the output peak-peak current ripple percentage is 38%, 6.5% and 2.1% for NC, SC and

NSC inductors respectively. The mutual inductance M for SC and NSC is 490 µH and 500 µH respectively.

5.6.2 Practical Inductance Measurements

The designed three inductor structures are practically implemented and the same core size is used for all of them. Table 5.6 shows the practical values for the NC, SC and NSC inductors.

Table 5.6: Practical inductor measurements

Inductor Type	SC	NSC	NC
L_1 (mH)	2.032	2.037	2.034
L_2 (µH)	124.7	129.1	126.2
M (µH)	488.5	496.2	0
k	0.97	0.97	0

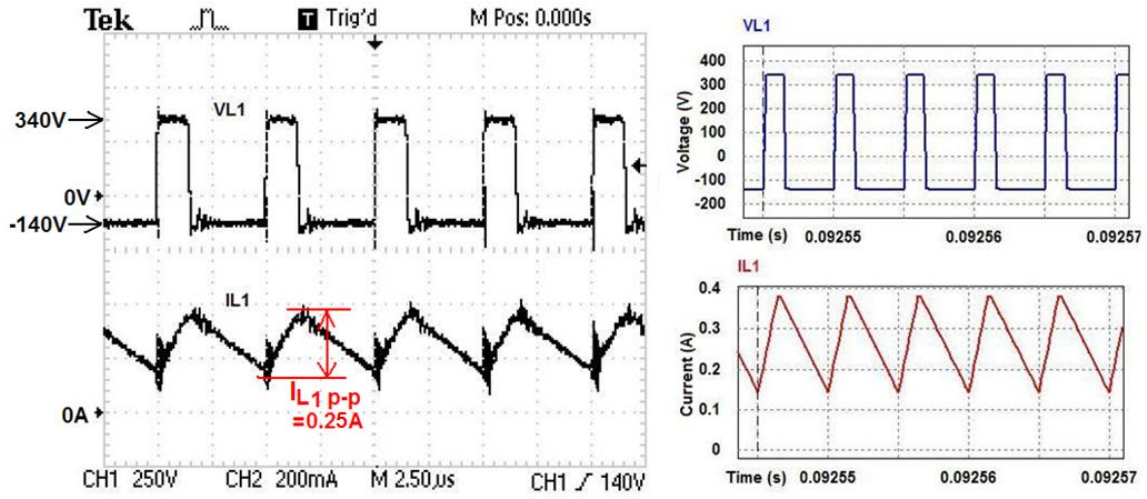
The practical coupling coefficient k of 0.97 for both SC and NSC inductors was achieved. Although a k of 0.98 was desired, the slightly lower practical coupling coefficient obtained may be attributed to practical considerations such as non-ideal flux linkages. The series resistances of inductors L_1 and L_2, were measured to be 0.8 Ω and 0.05 Ω respectively for all the inductor types considered.

5.6.3 Practical and Simulated Inductor Waveforms

The practical and simulated waveforms are presented. For the simulated waveforms, the converter parameters given in Section 3.1 and inductor values in Section 3.6.1 are used. For the practical waveforms, the input voltage is 340 V and duty ratio used is 0.3, similar to the converter parameters in Section 3.1. A summary of the practical peak-peak, RMS, and average currents are given in Table 5.7.

5.6.3.1 NC Inductor Waveforms

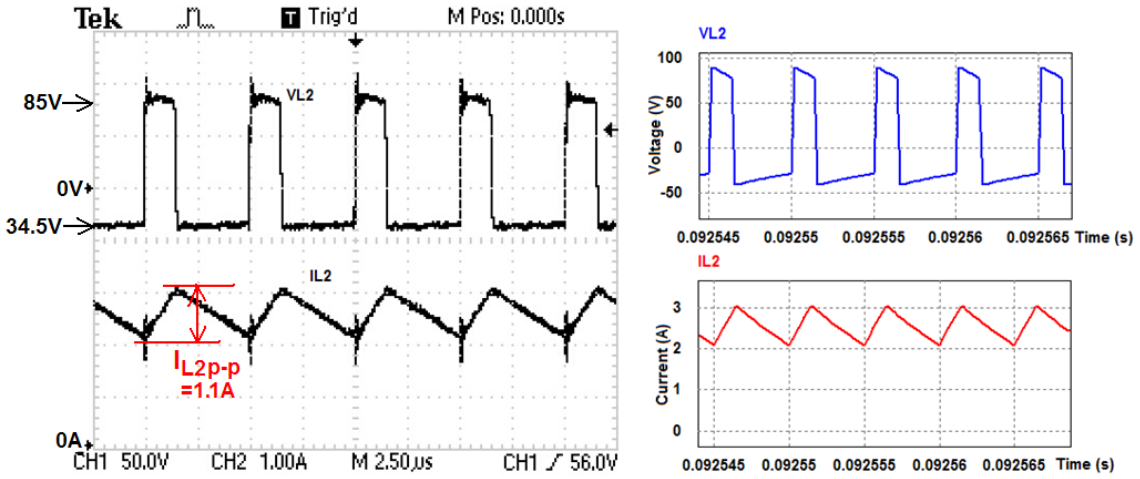
As seen from Figure 5.13, the practical and simulated waveforms are fairly similar. From inductor L_1 voltage waveforms, the positive voltage is 340 V and the negative voltage as 140 V for both the practical and simulated waveforms. The peak-peak current of inductor L_1 is 0.25 A for both the practical and simulated waveforms.



(a) Practical waveforms (b) Simulated waveforms

Figure 5.13: NC inductor L_1 waveforms.

The output inductor L_2 practical and simulated current waveforms are seen to be quite similar from Figure 5.14. The peak-peak current is 1.1 A and 0.95 A for the practical and simulated waveforms respectively. The practical and simulated inductor voltage waveforms are seen to be fairly similar, with a positive magnitude of 85V and a negative magnitude of 34.5 V.

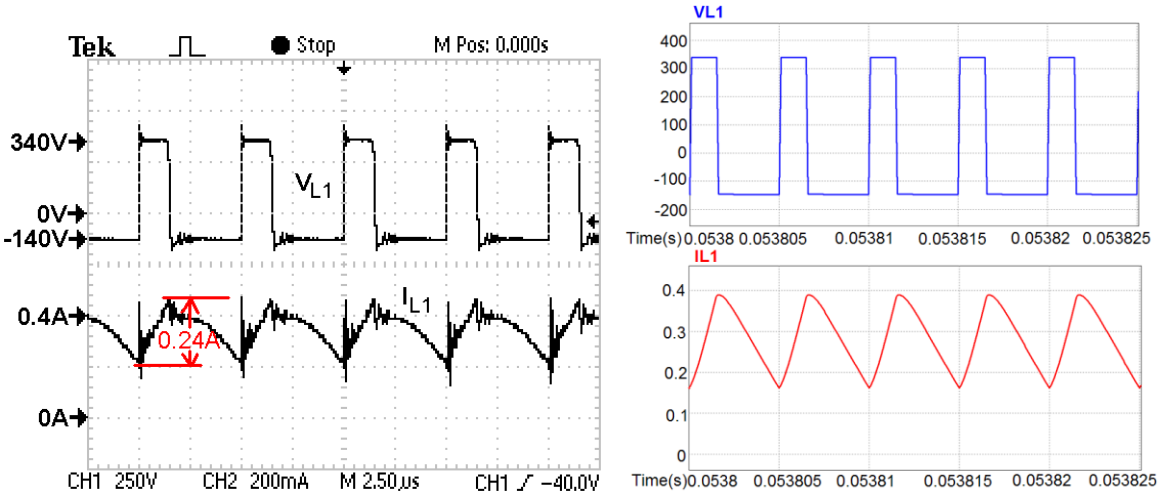


(a) Practical waveforms (b) Simulated waveforms

Figure 5.14: NC practical and simulated inductor L_2 waveforms.

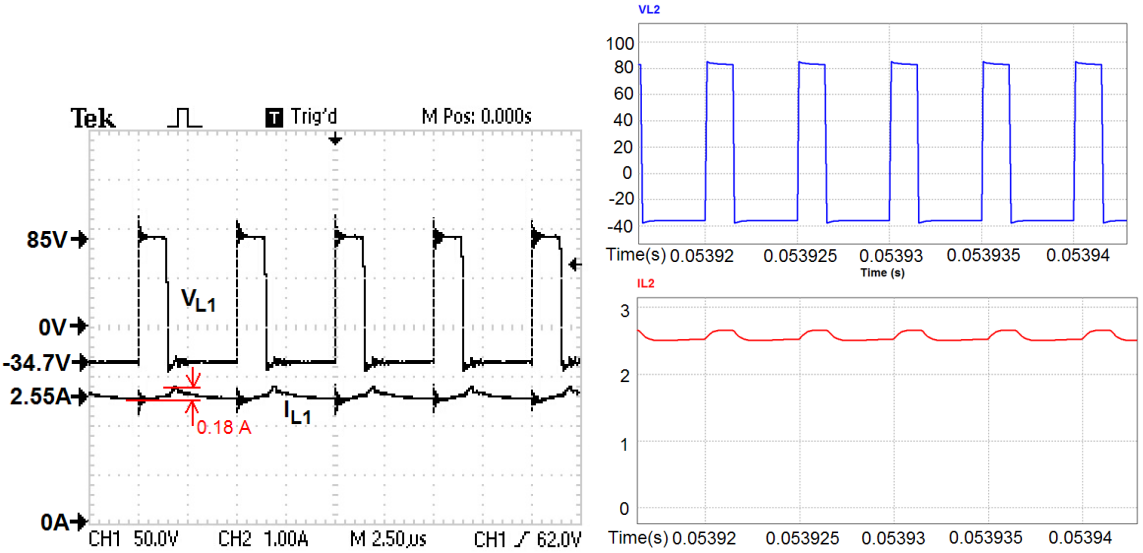
5.6.3.2 SC Inductor Waveforms

For SC inductors, the practical and simulated waveforms are fairly similar. As seen in Figure 5.15, the peak-peak current ripple for L_1 is 0.24 A and 0.226 A for the practical and simulated waveforms. The voltage waveforms are once again quite similar with the positive voltage seen as 340 V and the negative voltage being 140 V for both the practical and simulated waveforms.



(b) Practical waveforms (b) Simulated waveforms

Figure 5.15: SC practical and simulated inductor L_1 waveforms.



(a) Practical waveforms (b) Simulated waveforms

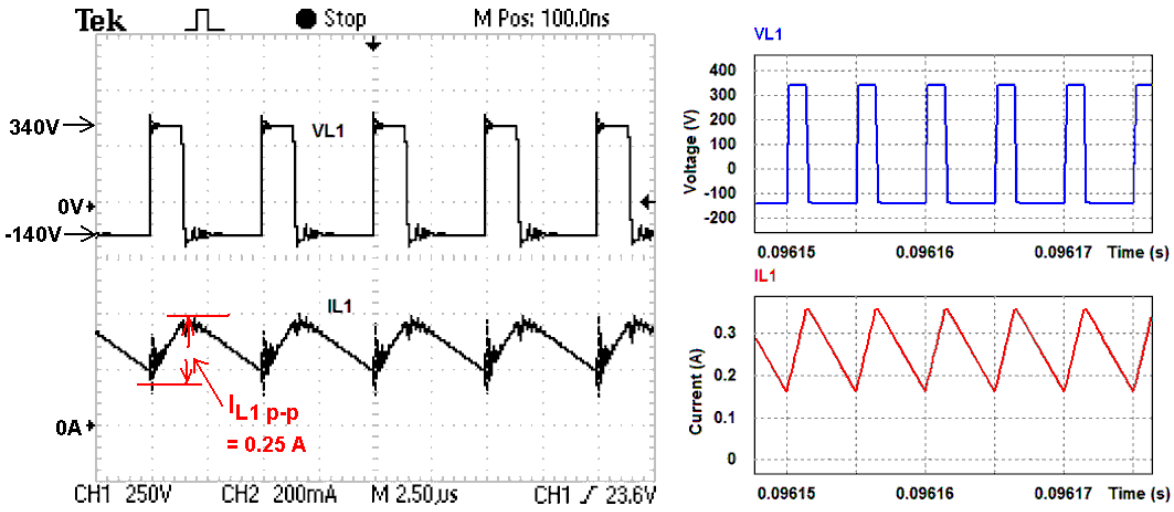
Figure 5.16: SC inductor L_2 waveforms.

The output inductor L_2 practical and simulated waveforms are observed in Figure 5.16. The inductor currents for both the practical and simulated waveforms are quite similar. The peak-peak current is 0.18 A and 0.158 A for the practical and simulated waveforms respectively. The voltage waveforms are seen to have a positive magnitude of 85 V and negative magnitude of 34.5 V for both the practical and simulated waveforms in Figure 5.16.

5.6.3.3 NSC Inductor Waveforms

The NSC input inductor L_1 practical and simulated waveforms are seen in Figure 5.17. Once again there is fairly close similarity of the practical and simulated waveforms. The peak-peak current magnitudes for the practical and simulated waveforms are 0.25 A and 0.243 A respectively. Again the practical inductor L_1 voltage is in good agreement with the simulated waveform, with the positive voltage noted as 340 V and the negative voltage as 140 V.

The practical and simulated waveforms for the output inductor L_2 are shown in Figure 5.18. Successful ripple reduction is seen on the output current waveform for both the practical and simulated waveforms. The peak-peak ripple is 0.1 A and 0.04 A for the practical and simulated waveforms.



(a) Practical waveforms (b) Simulated waveforms

Figure 5.17: NSC inductor L_1 waveforms.

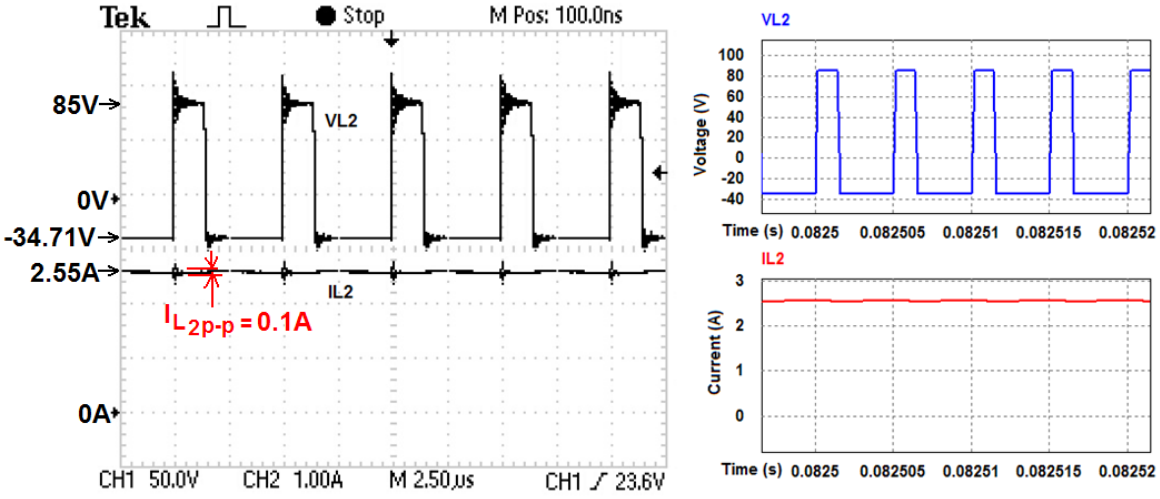


Figure 5.18: NSC practical and simulated inductor L_2 waveforms.

5.6.4 Measured and Simulated Peak-Peak, RMS and Average Inductor Currents

A summary of the practically measured peak-peak, RMS and average currents for the three inductor structures is shown in Table 5.7. As seen from Table 5.7, for the $i_{L1\ p\text{-}p}$ currents for NC, SC and NSC inductors, the practical values bear close resemblance to the simulated values. The slight difference between the practical and simulated values could be attributed to measurement errors and variation in component values. It is seen that SC inductors achieve the lowest peak-peak ripple, whose practical and simulated magnitudes are 0.24A and 0.226 A respectively.

Table 5.7: Practical and simulated peak-peak (p-p), RMS and average inductor currents

Inductor Type	**NC**		**SC**		**NSC**	
	Practical	*Simulated*	*Practical*	*Simulated*	*Practical*	*Simulated*
$i_{L1\ p\text{-}p}$ (A)	0.25	0.25	0.24	0.226	0.25	0.243
$i_{L1\ RMS}$ (A)	0.315	0.33	0.306	0.32	0.310	0.33
$i_{L1\ ave}$ (A)	0.308	0.32	0.3	0.29	0.305	0.31
$i_{L1\ p\text{-}p}$ ripple %	81.16	78.13	80	77.93	81.96	78.39
$i_{L2\ p\text{-}p}$ (A)	1.1	0.95	0.18	0.158	0.1	0.04
$i_{L2\ RMS}$ (A)	2.552	2.554	2.551	2.551	2.552	2.55
$i_{L2\ ave}$ (A)	2.55	2.55	2.55	2.55	2.551	2.55
$i_{L2\ p\text{-}p}$ ripple %	43.13	37.25	7.058	6.196	3.92	1.57

The NC and NSC inductors achieve the same practical peak-peak ripple of 0.25 A. It is therefore practically validated that SC inductors achieve a lower input inductor peak-peak current ripple than NS and NSC inductors. For the $i_{L2\ p\text{-}p}$ currents, again the practical and simulated values are in close agreement. It is seen that NSC achieves the lowest practical and simulated peak-peak ripples of 0.1 A and 0.04 A respectively. For the practical result, NSC inductors achieve a 90.9% ripple magnitude reduction as compared to the NC inductor L_2 peak-peak ripple, which is 1.1 A in magnitude.

The SC inductor L_2 achieves a peak-peak ripple of 0.18 A, which is a ripple percentage of 7.058%. As compared to the NC output inductor L_2, the SC inductor achieves a ripple magnitude reduction of 83.63%. It is therefore practically validated that using a SC inductor can achieve significant output ripple reduction. This low output peak-peak ripple of 7.058% eliminates the need of an output filtering capacitor, and will ensure that the LED load achieves efficacy and light output of greater than 99%. Therefore, the SC inductors are selected in the implementation of the LED driver.

5.7 ANALYTICAL AND PRACTICAL CONVERTER LOSSES FOR NC, SC AND NSC INDUCTORS

The analytical losses for NC, SC and NSC inductors are obtained from Figure 5.10 at L_1= 2 mH and are summarized in Table 5.8. The practical losses were measured and are tabulated in Table 5.8 as well. The converter input voltage is 340 V, and the LED load power is 88.5 W.

Table 5.8: Analytical and practical converter losses

Inductor Type	NC	SC	NSC
Analytical Losses (W)	15.303	12.603	14.254
Practical Power Loss (W)	16.15	13.42	15.08

From Table 5.8, the analytical losses and practical losses are in close agreement. The slight difference between the analytical and practical values is an average of approximately 0.83 W. This slight difference could be attributed to measurement errors and variation in component values.

From Table 5.8, it is seen that NC inductors achieve the highest practical losses of 16.15 W, followed by NSC inductors which achieve practical losses of 15.08 W. On the other hand, SC

inductors achieve a practical loss of 13.42 W, which is 20.34 % and 12.37% less than losses for NC and NSC inductors respectively. It is therefore inferred that efficiency improvement is possible by using SC inductors for the coupled cuk converter, as compared to using NC and NSC inductors.

Since SC inductors achieve the lowest driver losses, the SC inductor structure is chosen for the implementation of the proposed LED driver.

5.8 CHAPTER CONCLUSION

A comprehensive analysis of three inductor structures namely; NC, NSC and SC inductors, was carried out to determine their effects on performance of the cuk converter. The coupling coefficients considered for the NSC and SC inductors were 0.5 and 0.98. Such a comprehensive analysis has not been seen previously in available literature.

The impact of the three inductor structures and the coupling coefficients on driver efficiency, LED load efficacy and inductance size was comprehensively determined analytically, and the results obtained were compared. It was found that SC (k=0.98) inductors achieve the best performance in terms of driver efficiency, and achieve acceptable performance in terms of LED efficacy and light output, and the inductance size. Therefore, the SC (k=0.98) inductors meet the high performance parameters needed for proposed LED driver.

Practical validation was carried out to confirm the analytical analysis in terms of the peak-peak current ripples and total converter losses, and there was fairly good agreement. Hence by using SC (k=0.98) inductors, LEDs could be driven with high efficacy and light output of greater than 99%. This should aid in maintaining long LED lifetime. As the efficiency of the cuk converter is higher by using SC (k=0.98) inductors, it is this inductor structure that was chosen to implement the proposed LED driver. Due to the low output ripple obtained by the SC (k=0.98) inductors, the need for an output filter capacitor is eliminated. The SC inductor thus achieves a compact LED driver with low component count and cost.

CHAPTER 6 LED DRIVER CONTROLLER DESIGN

A control system applicable for two concepts proposed in Section 2.7, is developed in this Chapter. The first concept is the control of a fault-tolerant dimmable high power LED driver powering a single LED load. The controller detects an open-circuited string within the LED load using lossless current sensing, and accordingly adjusts the driver output current to drive the remaining connected strings at the correct current, given a certain dimming level. The lossless LED string current sensing will not impact driver efficiency negatively

The second concept is novel, and is the control of a single high power LED driver supplying several, dimmable, low power LED loads. Each load can be individually switched on or off if needed, without affecting operation of the other connected loads. Digital control is used to implement the two concepts. The novel LED driver would simplify and reduce costs of existing LED lighting systems

Therefore, a controller suitable for the afore-mentioned two concepts is designed and implemented practically. A compensator which maintains stability for all input voltage ranges, dimming levels and connected loads/strings, thus satisfying the control objectives is designed. Since digital control is to be used, the compensator is designed in the familiar s-domain, and discretized using the bilinear transform; and the control algorithm to be implemented digitally using a DSP is derived. The criteria for selecting a suitable DSP to prevent limit cycling problems for an average current controlled isolated cuk is also presented. The current sensors to be used are selected, and the practical signal conditioning circuit is designed. Also, the hardware needed to interface the DSP and the LED driver is designed. Controller design is finally verified through simulation and is also practically validated with excellent performance.

6.1 EFFECTS OF COUPLED INDUCTORS ON THE $G_{iL_2\delta}(s)$ TRANSFER FUNCTION

The effect of coupling and coupling types on the $G_{iL_2\delta}(s)$ transfer function are considered and compared. It is seen in [66] [69], that coupled inductors can aid in improving system transient response and speed response. Therefore, a similar comparison of the effect of coupling type and

coupling coefficient on the $G_{iL_2\delta}(s)$ transfer function, for a coupled cuk converter has not been seen in literature; the objective is to determine these effects using a quantitative example. The $G_{iL_2\delta}(s)$ transfer function is considered, as is used to design the output current controller for the designed LED driver. The parameters used are; quality factor (Q), resonant frequency (f_0) and open loop bandwidth. The types of coupling considered are SC and NSC; for both cases the coupling coefficient k, considered is 0.5 and 0.98. NC inductors are considered for comparison purposes.

The operating conditions are; input dc voltage, V_{in} = 340 V, duty ratio δ = 0.3030, component values for the non-isolated equivalent are: C_a=15 uF, C_b = 0.9375 uF, R_L=217.76 Ω, isolation transformer magnetising inductance, L_m=1.312 mH.

For the NC inductors, L_1= 2 mH, L_2 = 2 mH, M = 0. For the SC inductors; L_1 = 2mH and L_2 = 2 mH, for k = 0.5, M = 500 µH and for k=0.98 M= 1.96 µH. For the NSC inductors; L_1 = 2 mH, M = 2 mH, for k = 0.5, L_2= 8 mH, and for k = 0.98, M = 2.0825 mH.

6.1.1 Effect of Coupling Type and Coupling Coefficient on $G_{iL_2\delta}(s)$ Transfer Function

The $G_{iL_2\delta}(s)$ transfer function for SC and NSC inductors for both coupling coefficients k, of 0.5 and 0.98 are plotted in Figure 6.1. From Figures 6.1 and 6.2, the glitch that occurs at 1.4 kHz is due to the capacitor sizes C_a and C_b for the isolated cuk converter, which is dealt with extensively in [111]. For all the plots, the dc gain is seen to be 10.2 dB.

For the NC inductor as seen in Figure 6.1, the natural frequency f_0, occurs at 4.31 kHz, with a peak gain magnitude of 26.5 dB and the quality factor is seen to be 16.3 dB. This value of f_0 is attributed to the dominant complex Left Hand Plane (LHP) zeros that exist at this frequency, which introduce a phase drop of 180°. The notch seen on the gain at 5.13 kHz is caused by complex Right Hand Plane (RHP) zeros in the vicinity of f_0, which again introduce a further phase drop of 180°. Due to these two pairs of complex zeros being so close, the bandwidth of the NC inductor transfer-function is seen as 4.91 kHz. The combined phase drop of 360° makes compensator design a difficult task.

From Figure 6.1, for NSC (k=0.5), f_0 occurs at 4.912 kHz, which is slightly higher by 0.6 kHz as compared to the NC inductors f_0. The peak gain magnitude is seen as 20.9 dB, while the Q-factor is 8.2 dB, which is lower by about 50% than the Q-factor for NC inductors.

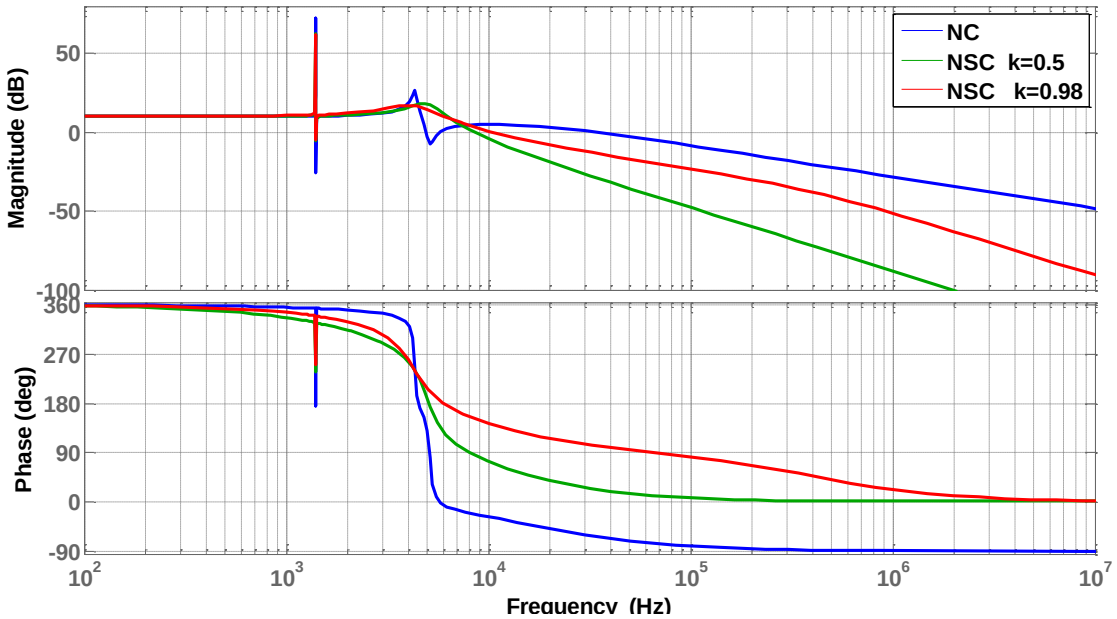


Figure 6.1: Bode-plot for $G_{iL_2\delta}(s)$ for k=0.5 and 0.98 for NSC inductor and NC inductor.

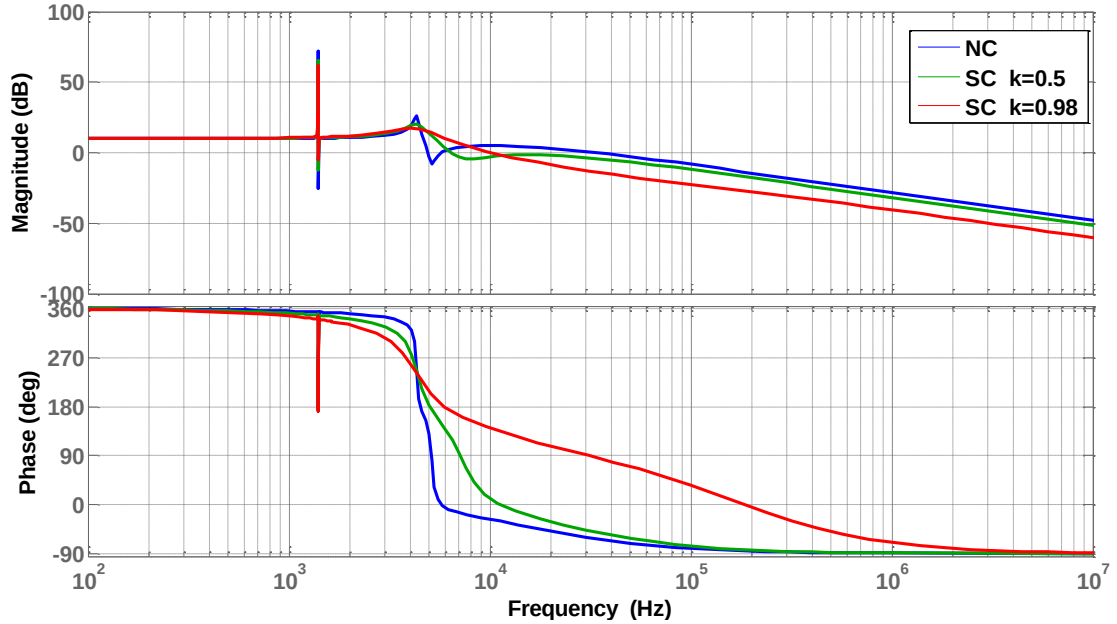


Figure 6.2: Bode-plot for $G_{iL_2\delta}(s)$ for k=0.5 and 0.98 for SC inductors and NC inductor.

This means that NSC (k=0.5) inductors achieve better system damping than the discrete NC inductors. This implies that by coupling the inductors, a better transient response is achieved in comparison with the NC inductors. The slightly higher f_0 is attributed to the lack of complex RHP zeros; instead there exist a single RHP zero at 8.389 kHz. The implication is that a smaller phase drop of 90° is seen at this frequency. Despite the existence of this single real RHP zero, compensation is easier as the phase drop is not as drastic as compared to the NC inductors transfer-function. A roll off of approximately 37 dB is seen after 5 kHz. The open-loop bandwidth is 8.63 kHz, almost twice the NC inductors transfer-function bandwidth. This implies that the system response speed for NSC (k=0.5) is faster than the system response speed of the NC inductors. It can be concluded so far that coupling improves system performance by better transient response and system response speed.

From Figure 6.1, for the NSC (k=0.98) inductors, f_0 is seen to occur at 4.156 kHz caused by the dominant complex LHP zeros existing at this frequency, at which the gain magnitude is 17 dB. The Q-factor is seen to be 6.8 dB, and this value is smaller by 9.5 dB and 1.3 dB as compared to the Q-factors of the NC and NSC (k=0.5) inductors respectively. Again this indicates that as the coupling coefficient k, is increased to 0.98, the system damping improves, consequently improving transient response.

Again, the lack of complex RHP zeros is noted, instead a single real RHP zero exists at 8.389 kHz, which introduces a 90° phase drop at this frequency. The position of this real single RHP zero seems to be not affected by the coupling coefficient value, as it also occurs at the same frequency of 8.389 kHz for the NSC (k=0.5) inductors as well. Similar to the NSC (k=0.5) inductors, the drastic phase drops associated with the NC inductors are not seen with the NSC (k=0.98) inductors; this makes compensation easier. The bandwidth is noted as 10.5 kHz, which is 1.87 kHz and 5.59 kHz more than the NSC (k=0.5) and NC inductors respectively. Thus as the coupling coefficient k, is increased to 0.98, it results in a higher system bandwidth.

The SC inductor transfer functions are plotted in Figure 6.2, while the NC inductor transfer function is included for comparison. From Figure 6.2, for the SC (k=0.5) inductors, f_0 is seen to occur at 4.35 kHz due to the dominant LHP zeros existing at this frequency; causing a 180° drop in the phase. The gain magnitude at f_0 is 20.1 dB; The Q-factor is noted as 9.9 dB; higher by 1.8 dB as compared to NSC (k=0.5) inductors and lower by 6.4 dB as compared to the NC inductors. Again,

the SC (k=0.5) inductors achieve better damping than the NC inductors, and exhibit improved transient response. The notch seen at 7.13 kHz is due to a pair of complex RHP zeros, which cause another drastic drop of 180° in the phase. The existence of this pair of complex RHP zeros so close to f_0, cause the bandwidth of the system to be limited at 6.44 kHz. This also makes compensation challenging due to the large phase drops.

From Figure 6.2, for SC (k=0.98) inductors, f_0 is seen to occur at 4.174 kHz due to the dominant pair of complex LHP zeros. The gain magnitude at f_0 is 17.2 dB. The Q-factor seen is 7 dB, which is 2.9 dB lower than when the coupling coefficient k, is 0.5. Again, this implies that tighter coupling achieves better system damping and better transient response.

For the SC (k=0.98) inductors, there are no complex RHP zeros as in the case when the coupling coefficient k, is 0.5; instead there are two real RHP zeros, one occurring at 9.182 kHz and the other at 143.15 kHz. They each contribute to a phase drop of 90°, which is spread out rather than the drastic phase drop of 180° as the case of when the coupling coefficient k, is 0.5. In terms of system compensation, a higher coupling coefficient k, of 0.98 may be better as the phase drops are gradual. The open loop bandwidth of SC (k=0.98) inductors is noted as 10.2 kHz, this is higher by 3.76 kHz than when the coupling coefficient k, is 0.5; this can imply that tighter coupling achieves higher system bandwidth, hence faster system response.

The overall conclusions that can be made are that the higher the coupling coefficient for both NSC and SC achieve higher system bandwidth which results as better system response speed, as well as better damping, which translates to better dynamic response of the system. Also, it becomes easier to compensate tightly coupled inductors (k=0.98) than it is for loosely coupled inductors (k=0.5) and NC inductors (k=0).

Due to the complex nature of the $G_{iL_2\delta}(s)$ transfer function, which is of 5^{th} order, it is difficult to qualitatively identify how exactly the coupling coefficient and coupling type affects the dominant poles and zeros in the transfer function. It is for this reason that a practical quantitative example was used to explain the effect of coupling and coupling type on the natural frequency, Q-factor and bandwidth. Therefore, the qualitative analysis exercise is left as part of future work. Table 6.1 shows the summary of the NC, NSC and SC inductor transfer functions for various coupling coefficients.

Table 6.1: Summary of the NC, NSC and SC inductor transfer functions

Coupling Type	Bandwidth (kHz)	Quality Factor *Q* (dB)	Natural Frequency f_0 (kHz)	RHP zeros
NC	4.91	16.3	4.31	Complex pair at 5.13 kHz
NSC (k=0.5)	8.63	8.1	4.912	Single Real at 8.389 kHz
NSC (k=0.98)	10.5	6.8	4.156	Single Real at 8.389 kHz
SC (k=0.5)	6.44	9.9	4.35	Complex pair at 7.13 kHz
SC (k=0.98)	10.2	7	4.174	Two Real at 9.182 kHz and 143.15 KHz

6.2 CONTROL OBJECTIVES

The LED driver will be designed using the SC (k=0.98) Inductors. An output filtering capacitor is not used. The input variables affecting the open-loop LED driver are;

(i) Variation of input dc voltage from 280 V to 380 V

(ii) Dimming levels from 0% to 50%

(iii) The number of connected strings/loads

A suitable controller that takes into account the above variables and ensures the correct load current is to be designed. The control objective is stated as; the controller must sense the number of connected strings/loads, and adjust the driver current through each string/load, given a particular dimming level input, over the entire range of input dc voltage. The light output of a connected string/load is to remain unaffected regardless of whether the other loads are connected or not. To accomplish the stated objective, digital control is chosen, due to its numerous advantages over analogue control as seen in Section 2.6. Also, since amplitude mode dimming is the most efficient, it is this method that will be used to perform dimming.

Determining how many LED strings/loads are connected will be done by use of hall-effect switches, which are a non-invasive, low cost and lossless method of current detection. The LED driver is based on the isolated coupled cuk, is a 5th order converter, since an output capacitor is not used. Due to its non-minimum phase characteristics, it is difficult to design a controller that will ensure stability and good response over a wide range of operation [107]. For the purpose of controlling the LED current, a simple, single loop controller is desired, and this means that the

speed and transient response have to be compromised to a level where satisfactory performance is achieved. Figure 6.3 shows the block diagram of the proposed control system using a DSP, for controlling a high power LED driver with multiple LED strings/loads;

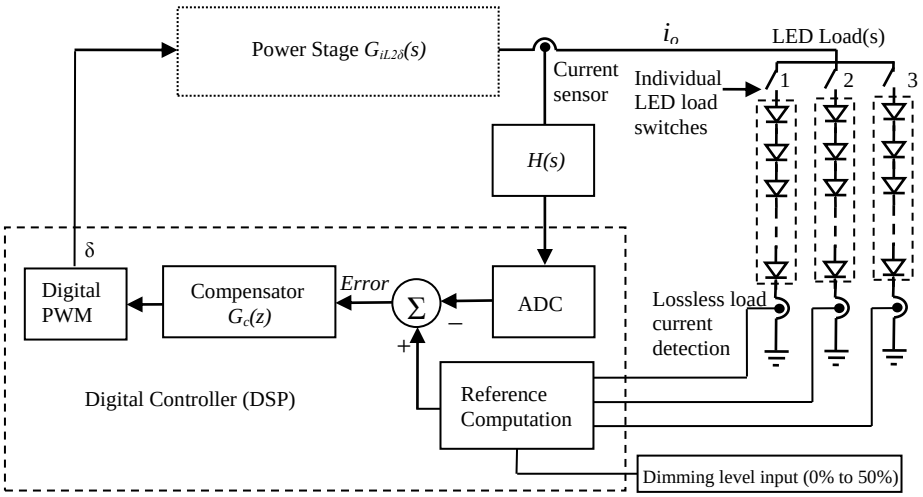


Figure 6.3: The proposed control system for and LED driver with multiple strings/loads.

6.3 DUTY RATIO COMPUTATION

For energy saving purposes, dimming is necessary. The duty ratio required is computed for various dimming levels, connected strings/loads and input voltage range. Load temperature variation is also taken into account; to and is used to investigate effects of temperature variation on the $G_{iL_2\delta}(s)$ transfer-function. The dimming levels, with the corresponding load current I_{LOAD}, dynamic load resistance R_D, load voltage V_{LOAD}, and actual duty ratios δ_{Vin} for different input voltages and load temperatures for some operating points are given in Table 6.2. The dimming levels of 0%, 25% and 50% are taken from Table 4.2.

The dynamic resistances for the different load temperatures are calculated using Equations (4.11) and (4.12) for 38°C and 25°C respectively. The actual duty ratio is computed using (4.13). For simplicity, V_{sat}, $I_{L1}r_{L1}$ and $I_{L2}r_{L2}$ are calculated as follows;

$$V_{sat} = r_{DS,ON} \cdot I_{sw,RMS} = 0.7\,\Omega \times 0.54\,\text{A} = 0.378\,\text{V} \tag{6.1}$$

$$I_{L1,RMS}r_{L1} = 0.306\,\text{A} \times 1.2\,\Omega = 0.367\,\text{V} \tag{6.2}$$

$$I_{L2,RMS}r_{L2} = I_{o,av} \cdot r_{L2} = 2.551\,\text{A} \times 0.037\,\Omega = 0.094\,\text{V} \tag{6.3}$$

Where $I_{sw,RMS}$, $I_{L1,RMS}$ and $I_{L2,RMS}$ are obtained experimentally from Section 5.6.

Table 6.2: Dimming levels and corresponding load current, load dynamic resistance and various duty ratios for different input voltages, load temperatures and connected strings/loads

Load Temp	Dim-ming	Loads/ Strings	R_D (Ω)	I_{LOAD} (A)	V_{LOAD} (V)	P_{LOAD} (W)	$\delta_{Vin-280V}$	$\delta_{Vin-340V}$	$\delta_{Vin-380V}$
25°C	0%	3	13.84	2.550	35.30	90.01	0.3489	0.3061	0.2830
38°C	0%	3	13.61	2.550	34.71	88.50	0.3453	0.3027	0.2797
	25%	2	26.18	1.275	33.38	42.57	0.3371	0.2950	0.2545
	50%	1	76.71	0.425	32.60	13.86	0.3321	0.2904	0.2680

6.4 EFFECT OF DIMMING, INPUT VOLTAGE AND LOAD TEMPERATURE VARIATION ON $G_{iL_2\delta}(s)$

Due to dimming and input voltage variation, the converter duty ratio must change to keep the output current at the desired level. The dynamic resistance R_D of the LED load varies due to dimming and load temperature variation. Therefore, the designed controller should be capable of ensuring system stability despite these variations. The effect of the changing input voltage, dimming levels and load temperature on the control-to-output inductor current transfer-function $G_{iL_2\delta}(s)$ is plotted in Figure 6.4 using the values from Table 6.2. The extreme cases considered are listed as;

(i) P_{LOAD} = 90 W, V_{in} = 280V, δ = 0.3493, Load$_T$ = 25°C, R_D=13.84Ω (0% dimming)

(ii) P_{LOAD} = 88.485 W, V_{in} =280V, δ=0.3456, Load$_T$ = 38°C, R_D=13.61Ω (0% dimming)

(iii) P_{LOAD} = 42.05 W, V_{in} = 380V, δ = 0.2697, Load$_T$ = 25°C, R_D=25.66 Ω (50% dimming)

(iv) P_{LOAD} = 41.73 W, V_{in} = 380V, δ = 0.2683, Load$_T$ = 38°C, R_D=25.57 Ω (50% dimming)

From Figure 6.4, for a given dimming level and input dc voltage, the effect of load temperature variation from 25°C to 38°C has no significant impact on the $G_{iL_2\delta}(s)$ transfer-function. Therefore, sensing the load temperature is not necessary, and simplifies controller design. As the dimming level is reduced from 50% to 0%, and input voltage is reduced from 380-280V respectively, the low frequency gain up to 1.43 kHz is seen to reduce as well.

The respective gains for 380 V - 50% dimming and 280 V – 0% dimming are 29 dB and 34 dB. The phase from low frequency up to 1.43 kHz is fairly constant at 360° for all dimming levels for

input voltages of 280 V and 380 V. The glitch seen on the gain and phase at 1.43 kHz is seen for both input voltages of 280V and 380V and both dimming levels of 0% and 50%. This is due to the dominant left hand complex poles and zeros that exist at this frequency.

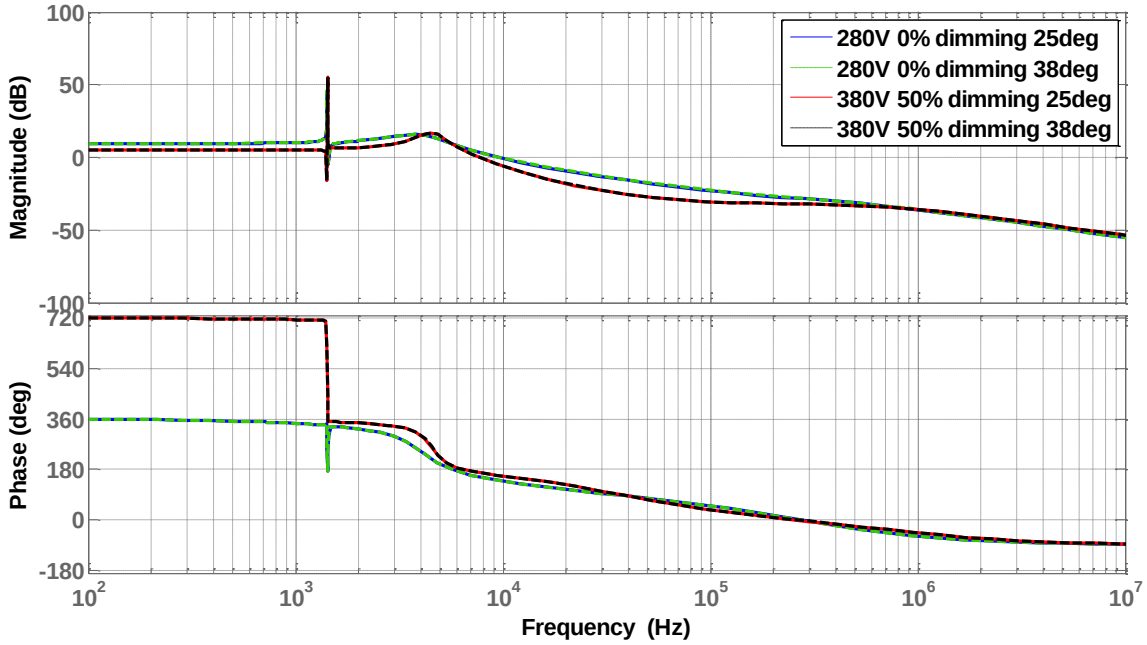


Figure 6.4: Bode-plot of $G_{iL_2\delta}(s)$ for extreme input voltages, dimming levels and load temperatures

For an input voltage of 280V and 0% dimming, resonance is observed at 4.02 kHz, which introduces a phase-lag of 180°. Similarly, for an input voltage of 380V and 50% dimming, resonance is seen to occur at 4.47 kHz, which also introduces a phase-lag of 180°. This large phase drop in the vicinity of 3 kHz to 100 kHz means achieving a crossover frequency larger than 3 kHz may be challenging. Thus the crossover frequency may have to be reduced below 3 kHz to achieve stability for all input voltage and dimming level variations.

The reducing gain with increase in dimming levels results in increase of phase-margin; this is because the phase of $G_{iL_2\delta}(s)$ is seen to be gradually reducing from 360° at dc to 0° at 100 kHz. Hence it is expected that increased damping will be observed with increased dimming. This may be an advantage as stability is improved with reducing load power.

6.5 CONTROLLER SPECIFICATIONS

The controller specifications for worst case step changes in input voltage, load step changes and dimming level step changes are given in Table 6.3. The LED load does not need very fast response, and controller specifications can be relaxed to achieve a controller that achieves stability for operating converter parameters such as input voltage and dimming level variation. A single-loop current controller is used, and the transfer-function $G_{iL_2\delta}(s)$ is needed. With the given controller specifications in Table 6.3, the relation between the bandwidth, rise-times and settling-times are satisfied theoretically.

Table 6.3: Controller specifications

Transient Step Change in Input Voltage		**Stability Margins**	
Rise-time	<1 ms	*Gain-margin*	At least 10dB
Settling-time	<30 ms	*Phase-margin*	At least 45°
% Overshoot	<100%	*Crossover-Frequency*	At least 15 Hz
Steady-State Error	Eliminated within 40ms after a transient	*Output Current Regulation*	<1% of the output current
Transient Behaviour for Step Change in Load			
Rise-time	<0.1 ms		
Settling-time	<5 ms		

6.6 COMPUTATION OF REFERENCE MAGNITUDE AND CURRENT SENSOR GAIN

The reference value is required within the control loop to determine the output current from the converter, and hence obtain the correct load current. The reference magnitude I_{ref}, given the number of connected strings/loads and dimming levels is given as;

$$I_{ref} = \frac{\left(1 - \frac{\%\,\text{dimming}}{100}\right) \cdot I_{string,NOM} \cdot S_{CONN}}{I_{T,LOAD,MAX}} \tag{6.4}$$

Where $I_{string,NOM}$ = 0.85 A, which is the nominal current per string/load, $I_{T,LOAD,MAX}$ = 3 A, which is the maximum connected load current limit, $\%\,\text{dimming}$ is the dimming level and S_{CONN} is the number of connected strings/loads. Using (6.4), some reference values for the respective dimming levels and connected loads are given in Table 6.4.

The PWM modulating saw-tooth wave amplitude V_m is chosen as 1 V. The feedback sensor gain H is determined using the nominal value of I_{ref}, when the total connected load current $I_{T,LOAD,NOM}$ is 2.55 A, as follows;

$$H = \frac{I_{ref,NOM}}{I_{T,LOAD,NOM}} = \frac{0.85\,\text{V}}{2.55\,\text{A}} = \frac{1}{3} \tag{6.5}$$

Table 6.4: Values of I_{ref} for various dimming levels and connected strings/loads

Dimming %	S_{CONN}	I_{ref} (V)	$I_{T,LOAD}$ (A)
0	3	0.85	2.55
25	2	0.425	1.275
50	1	0.14166	0.425

6.7 CONTROLLER DESIGN IN $s-$DOMAIN

A controller which maintains stability for all input voltages, dimming levels and connected loads/stings is desired. To achieve this, the controller is designed for the mid-point operating condition, which from Table 6.2, occurs when V_{in} = 340 V at a dimming level of 25% and with two strings connected (P_{LOAD} = 42.57 W). The closed-loop gain response using the designed compensator will be tested to evaluate performance such as overshoot, settling-time, and load current regulation for step changes in input voltage and dimming levels.

6.7.1 The Uncompensated Loop-Gain of the Output Inductor $T_{uncomp}(s)$

The loop-gain of the uncompensated system is given as follows;

$$T_{uncomp}(s) = T_m(s) \cdot H(s) \cdot G_{iL_2\delta}(s) \tag{6.6}$$

Where $T_m(s)$ is the PWM modulator gain given as $1/V_m$ = 1, $H(s)$ = 1/3 and $G_{iL_2\delta}(s)$ is the control-to-output inductor current transfer-function. $T_{uncomp}(s)$ is plotted in Figure 6.6 for V_{in} = 340V, δ = 0.2950, S_{CONN} = 2, Load_T = 38°C (to achieve a dimming level of 25%, resulting in R_D = 26.175 Ω). The pole-zero map of transfer-function $T_{uncomp}(s)$ is plotted in Figure 6.5 to aid in discussion of the bode-plot transfer-function $T_{uncomp}(s)$ in Figure 6.6.

From Figure 6.6, the dc gain up to 1.42 kHz is seen as -5.27 dB, while the phase remains fairly close to 0° up to 1.42 kHz. The glitch seen on the gain plot at 1.42 kHz is caused by complex conjugate LHP zeros and poles existing at this frequency which cause the resonance glitch and phase glitch. Resonance is seen on the gain plot at 4.33 kHz is due to a pair of dominant complex conjugate LHP poles, which introduce a drastic phase-lag of 180° at 4.33 kHz, making the phase plot cross the 180° line at 6.25 kHz. It is this large phase drop that makes compensation difficult and reduces the achievable system gain crossover frequency.

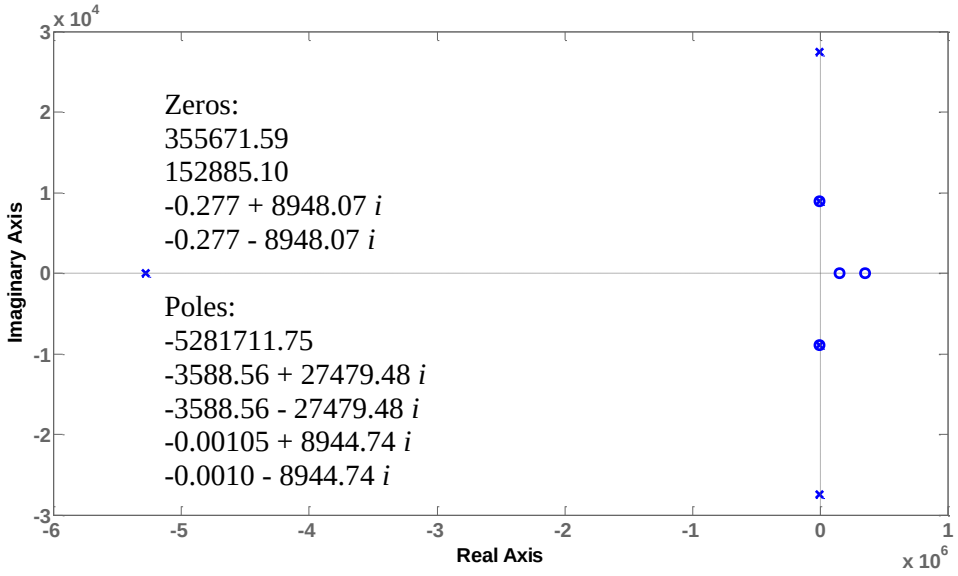


Figure 6.5: The Pole zero map of $T_{uncomp}(s)$ for V_{in} = 340 V for 25% dimming level and S_{CONN} = 2

There are two real RHP zeros which exist at 24.33 kHz and 56.6 kHz, and each introduces a 90° phase drop at their respective frequencies; making this system have non-minimum phase characteristics [108]. Despite the existence of these RHP zeros, they occur far away beyond 24 kHz, and do not have much influence on the phase in the vicinity of the resonant frequency of 4.33 kHz; therefore, compensation is made easier.

There is a real pole at 840 kHz, which causes the gain to roll off at 6 dB/decade after this frequency. To achieve a compensated system, it becomes necessary to reduce the crossover frequency below 3 kHz, so that a sufficient phase margin is attained. Although reduction of the crossover frequency reduces the system response speed, it will be shown that it is not detrimental, as the LED light output or load step change does not need very fast response. In fact this provides a

smooth transition between one dimming level and a load step to another, which makes it comfortable to the human eye.

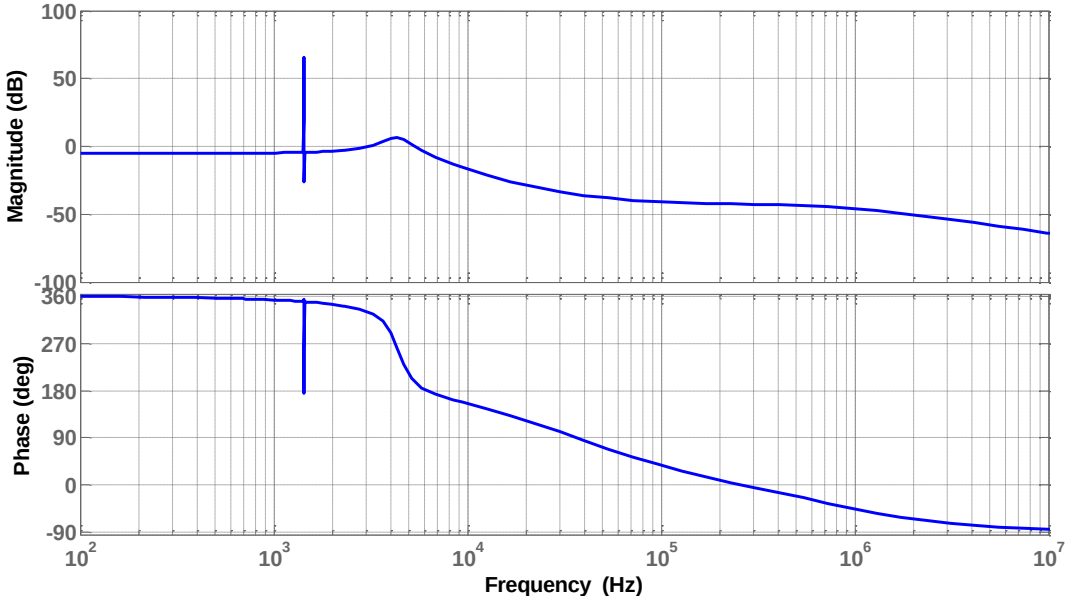


Figure 6.6: Bode-plot of $T_{uncomp}(s)$ for V_{in} = 340V, dimming level of 25%, and S_{CONN} = 2.

6.7.2 Compensator Design in $s-$Domain

A simple 3-pole 1-zero compensator is chosen as it allows a large phase decrease of $T_{uncomp}(s)$, just before 1.42 kHz. A low frequency pole is placed near the origin at 0.723 Hz to eliminate the steady-state error, and a zero is placed at frequency at least 1/5th of the switching frequency of 200 kHz, at 28.4 kHz to attenuate switching noise. At this point, the gain and phase at the achievable crossover frequency of 68 Hz is -44.7 dB and 270° respectively. Two real poles are placed at 277 Hz, to obtain a gain of -45.6 dB and a phase of 237° at 68 Hz. The gain of the compensator was increased to 188.55, resulting in the compensated gain-margin of 16.7 dB, phase-margin of 58.1° and a crossover frequency of 68 Hz. Despite the crossover frequency being so low, the compensator is tested for stability for the worst case conditions of $T_{uncomp}(s)$ for all ranges of input voltages, dimming levels and connected strings/loads. The compensator transfer-function $G_c(s)$ is given by (6.7).

$$G_c(s) = k \cdot \frac{1-\frac{s}{f_{z_1}}}{\left(1+\frac{s}{f_{p_1}}\right)\cdot\left(1+\frac{s}{f_{p_2}}\right)\cdot\left(1+\frac{s}{f_{p_3}}\right)} \tag{6.7}$$

Where; gain k = 188.55, zero frequency f_{z_1} =28.42 kHz , pole frequencies f_{p_1} =0.723 Hz, f_{p_2} = f_{p_3} = 227.36 Hz The actual compensator transfer-function is given as;

$$G_c(s) = 188.55 \frac{\left(1 - 5.6 \times 10^{-6} s\right)}{(1 + 0.22s)(1 + 0.0007s)(1 + 0.0007s)} \tag{6.8}$$

The compensator $G_c(s)$ bode-plot is given in Figure 6.7, as well as $T_{uncomp}(s)$ and $T_{comp}(s)$.

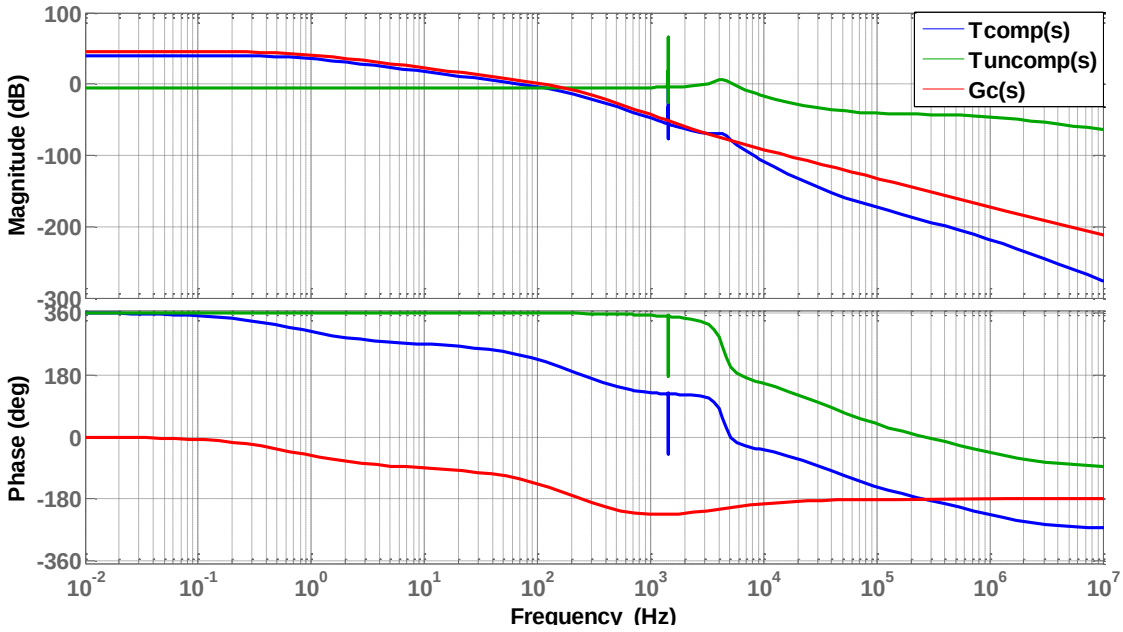


Figure 6.7: Bode-plot of the designed compensator $G_c(s)$, $T_{comp}(s)$ and $T_{uncomp}(s)$.

6.7.3 The Compensated Loop Gain $T_{comp}(s)$

The compensated loop gain $T_{comp}(s)$ is plotted in Figure 6.7. It can be seen that the compensator achieves a stable loop gain with a gain-margin of 16.7 dB and a phase-margin of 58.1°. The achieved crossover frequency is 68 Hz. The roll-off achieved is approximately 20 dB/Decade, and aids in attenuating high frequency switching noise effectively. To investigate whether the designed controller is suitable for all operating conditions, the compensated loop gains for the extreme operating conditions given in Section 6.5 are plotted in Figure 6.8.

At an input voltage of 280 V, dimming level of 0% and 3 connected strings/loads, the controller achieves a gain-margin of 10.8 dB, and a phase-margin of 39.1°. The crossover-frequency at this operating point is 111 Hz. When the input voltage is increased to 380 V, at a dimming level of 50%

and 1 connected load/string, the gain-margin achieved is 25.8 dB, while the phase-margin is seen to be 79°, although the crossover frequency reduces to 25.9 Hz. For both operating conditions, the roll off is maintained at approximately 20 dB/Decade. From Figures 6.7 and 6.8, it is observed that the designed compensator achieves a stable loop-gain over the entire operating range of input voltages and dimming levels. The stability margins are summarized in Table 6.5. The associated rise and settling-times will be shown in the control simulation results Section in 6.11.

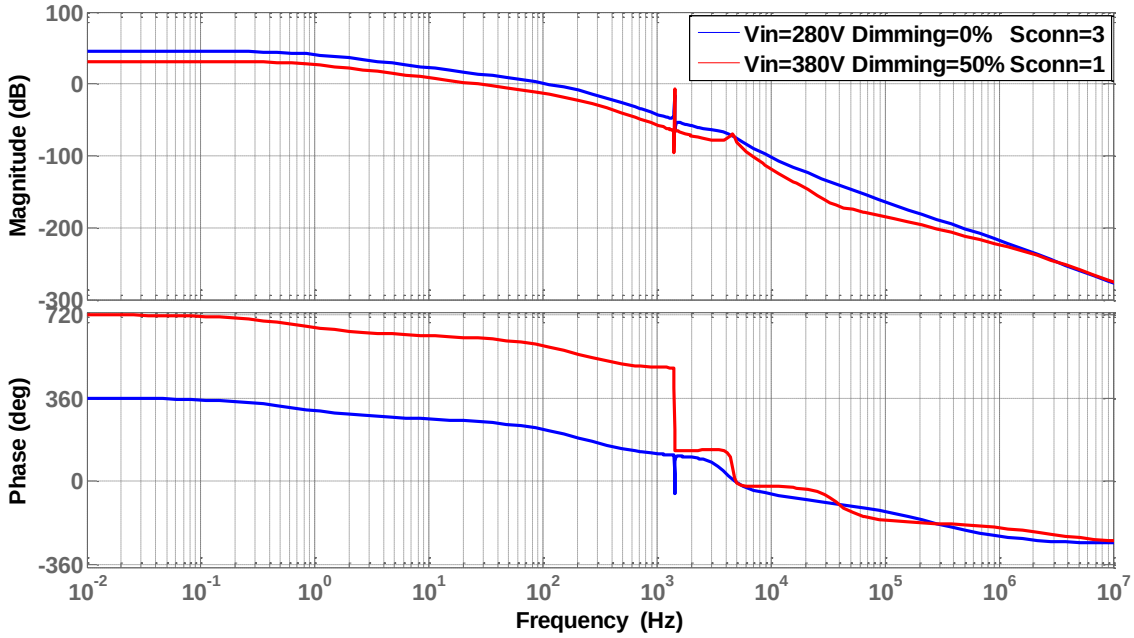


Figure 6.8: The compensated bode-plot $T_{comp}(s)$ for the extreme operating points.

Table 6.5: Summary of stability margins of the compensated loop gain $T_{comp}(s)$

Input Voltage	Dimming Level % and Number of Connected Strings/Loads	Phase-margin	Gain-margin	Crossover Frequency
280 V	0% , 3 strings	39.1°	10.8 dB	111 Hz
340 V	25% , 2 strings	58.1°	16.7 dB	68 Hz
380 V	50% dimming, 1 string	79°	25.8 dB	25.9 Hz

6.8 CONTROLLER TRANSFORMATION TO *z*-DOMAIN

For digital control, the continuous time compensator is transformed into a discrete time compensator using a suitable transformation technique. For this particular controller, the bilinear transform method is considered as it preserves the controller gain and phase-margin and has no aliasing effects [85]. Since digital design by emulation is used, the ZOH delays are ignored. This results in a smaller actual phase-margin than was designed for. The best achievable phase-margin of the compensated loop gain for the extreme operating conditions was found to be between 48.1° and 81.3°. The continuous time compensator in Equation (6.8) is transformed to discrete time using the bilinear transform method with a sampling frequency of 200 kHz and is found as;

$$G_{ci}(z) = \frac{6.3495368\times10^{-7}z^3 + 6.8922323\times10^{-7}z^2 - 5.2641459\times10^{-7}z - 5.8068414\times10^{-7}}{z^3 - 2.9857419z^2 + 2.9715349z - 0.98579292} \quad (6.9)$$

Equation (6.9) can be rewritten in terms of the error E and the output y as;

$$G_{ci}(z) = \frac{y}{E} = \frac{b_0 + b_1z^{-1} + b_2z^{-2} + b_3z^{-3}}{1 + a_1z^{-1} + a_2z^{-2} + a_3z^{-3}} \quad (6.10)$$

Where the controller coefficients are given as; $b_0 = 6.3495368\times10^{-7}$, $b_1 = 6.8922323\times10^{-7}$, $b_2 = -5.2641459\times10^{-7}$, $b_3 = -5.8068414\times10^{-7}$, $a_1 = 2.9857419$, $a_2 = 2.9715349$ and $a_3 = -0.98579292$.

6.9 REQUIRED ADC AND DPWM RESOLUTION TO AVOID LIMIT CYCLING

Limit cycling in digital control is a problem that affects stability of a closed-loop system. Therefore, careful selection of DPWM and ADC resolution of the digital controller is needed for successful stable closed-loop operation [78]. Limit cycling occurs when a single step change of the DPWM causes an error larger than the resolution of the ADC. Since DPWM has only discrete values of duty ratio, this implies that the LED driver output current will also have discrete values in steady state.

The controller makes the output current track the reference to achieve the desired output current, which is sensed and converted to a discrete value by the ADC. If a single discrete step change of the DPWM generates an error larger than the ADC resolution, then the controller output will toggle the DPWM between two discrete duty ratio values to attempt to attain the desired output, leading to oscillations [78]. Therefore, the ADC and DPWM resolution need to be carefully selected [31]. The

required ADC and DPWM resolution for various voltage controlled converters was presented in [31]. Similarly, for the current controlled isolated cuk, the required ADC and DPWM resolution, depending on the desired current regulation level is derived in the proceeding Section.

6.9.1 ADC Resolution Requirement

For the current controlled cuk, The ADC resolution required depends on the output percentage current regulation value. For this computation, it is assumed $I_{L_{2s,av}} \approx I_o$. Thus the required ADC resolution n_{adc} is derived as;

$$n_{adc} \geq \log_2\left(\frac{V_{adc,\max}}{V_{ref}} \cdot \frac{I_o}{\Delta I_o}\right) \tag{6.11}$$

where $V_{adc,max}$ is the maximum allowable input voltage to the ADC , V_{ref} is the reference voltage for the control feedback loop, I_o is the output load current, and ΔI_o = % current regulation $\cdot I_o$.

6.9.2 DPWM Resolution Requirement

Another criterion is needed to fulfil the DPWM resolution requirement to prevent limit cycling. The current transformation transfer-function for the isolated cuk is given as [27];

$$U(D) = \frac{I_o}{I_{in}} = \frac{n(1-D)}{D} \tag{6.12}$$

Where n is the isolation transformer turns ratio. Due to the discrete nature of the DPWM, the smallest change in duty ratio $\Delta U(D)$ is derived as;

$$\Delta U(D) = \frac{n(1-2D)}{D(D2^{n_{pwm}}+1)} \tag{6.13}$$

where n_{pwm} is the DPWM bit resolution. To avoid limit cycling, the following derived condition must be satisfied;

$$\frac{V_{adc,\max} I_o}{2^{n_{adc}} V_{ref}} \geq \Delta I_o \tag{6.14}$$

where the smallest change due to the discrete nature of DPWM in output current is $\Delta I_o = I_{in}\Delta U(D)$. Therefore (6.14) can be re-written as;

$$\frac{V_{adc,\max} I_o}{2^{n_{adc}} V_{ref}} \geq I_{in} \Delta U(D) \tag{6.15}$$

Making n_{pwm} the subject and obtaining an expression for the required DPWM resolution;

$$n_{pwm} \geq \log_2 \left[\frac{1}{D} \left(\frac{(1-2D)2^{n_{adc}} V_{ref}}{(1-D)V_{adc,\max}} - 1 \right) \right] \tag{6.16}$$

Equation (6.16) gives the required DPWM resolution for a current controlled isolated cuk, given the ADC bit resolution.

6.10 PRACTICAL DIGITAL CONTROLLER IMPLEMENTATION

6.10.1 Selection of the Digital Signal Processor

Careful selection of the digital controller needs to be done to achieve successful digital control. The appropriate ADC bit resolution is determined using (6.11). By using a current regulation value of 1% of I_o (where $I_{L_{2s,av}} \approx I_o$), $V_{adc,max}$ of 3.3V, and V_{ref} as 0.85V, the minimum ADC bit resolution is found as;

$$n_{adc} \geq \log_2 \left(\frac{3.3\,\text{V}}{0.85\,\text{V}} \times \frac{2.55\,\text{A}}{25.5 \times 10^{-3}\,\text{A}} \right) = 8.6 \text{ Bits} \tag{6.17}$$

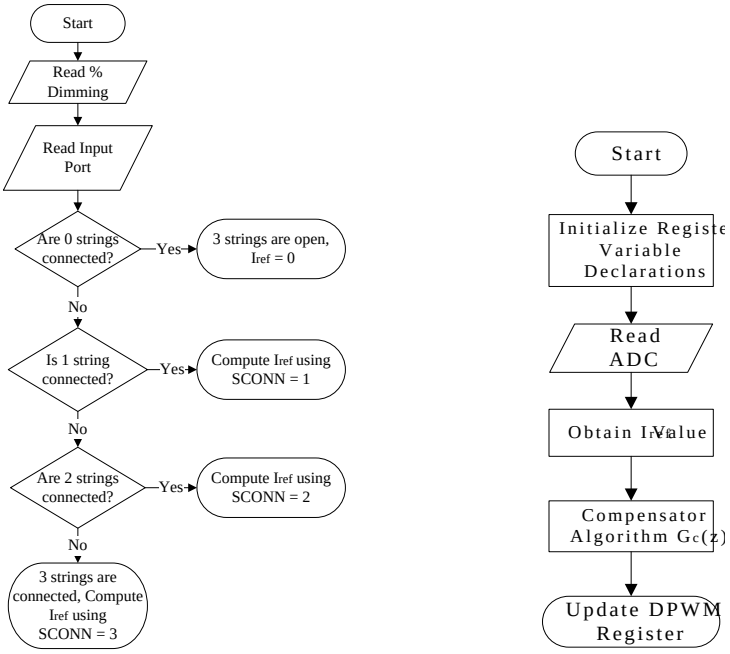
A DSP with greater than 8.6 ADC bit resolution is required. DSP's with 12-Bit ADC's are common, and will be used as the next criteria for determining the required DPWM resolution. To identify the required DPWM resolution, by using D = 0.3027 (for nominal voltage V_{in} = 340 at 0% dimming) the minimum DPWM resolution is found using Equation (6.17) as;

$$n_{pwm} \geq \log_2 \left[\frac{1}{0.3027} \left(\frac{(1-(2 \times 0.3027)) \times 2^{12} \times 0.85}{(1-0.3027) \times 3.3} - 1 \right) \right] = 10.95 \text{ Bits} \tag{6.18}$$

Therefore a DPWM resolution of greater than 10.95 Bits is required to avoid the limit cycling problem. The DSP selected which satisfies the required minimum ADC and DPWM resolution is the TMS320F28027 [109]. It has features such as a 32 Bit CPU, a maximum Clock of 60MHz (resulting in 60 MIPS), a 12 Bit ADC with 4.6 MSPS, and a high resolution PWM (HRPWM) of 14.8 bits at 200 kHz switching frequency. Although it also features a standard PWM, its resolution is only 8.22 bits at a 200 kHz switching frequency.

6.10.2 Algorithm for Sensing Connected Strings/Loads

The flowchart of the digital control algorithm for determining the current reference value, depending on the number of connected loads/strings, given the desired dimming level is shown in Figure 6.9. This algorithm is implemented in the DSP, and the resulting reference value obtained is used by the main control algorithm to generate an error value for further processing.



(a) Algorithm for sensing connected strings/loads (b) the main control algorithm and I_{ref} computation

Figure 6.9: Flow chart of the digital control algorithm for sensing open strings/loads.

6.10.3 Operation of the DSP and Main Control Algorithm Implementation

For the selected DSP, to generate a 200 kHz PWM signal, Timer 1 is configured in up-count mode and loaded with a value of 300, corresponding to the PWM period time of 5µs. The Timer 1 counter is then compared with a value in the compare register CMPAHR to generate the required duty cycle value. An interrupt is generated at the mid-point of the PWM waveform to begin a start of conversion by the ADC. The ADC samples the output inductor current at this mid-point instant to avoid switching noise. After the ADC conversion is complete, the ADC generates an interrupt signalling an end of conversion.

The reference value obtained by the algorithm to determine which loads/strings are connected (given a dimming value by the user) is then subtracted from the ADC result to generate an error.

This error is then processed by the main control algorithm written by the user to perform the lag compensation. The algorithm result is updated into CMPAHR for the next PWM cycle, and the latest duty cycle value takes effect at the start of a new switching cycle. Due to the high computation speed of the DSP and ADC conversion speed, sampling of the output inductor current, control algorithm computation and duty cycle updating occurs well before the next ADC start of conversion interrupt. The actual control algorithm obtained from Equations (6.9) and (6.10) with the given coefficients; to be implemented on the DSP is given as;

$$y(n) = b_0\ E(n) + b_1 E(n-1) + b_2 E(n-2) + b_3 E(n-3) - a_1 y(n-1) - a_2 y(n-2) - a_3 y(n-3) \quad (6.19)$$

Where the controller coefficients b_0, b_1, b_2, b_3, a_1, a_2 and a_3 are given in Section 6.8.

6.10.4 Hardware Interfacing

The DSP needs a feedback signal from the sensed inductor current so that it can generate the control action. The current sensor's output which is a voltage, has to be signal conditioned so that it may match the ADC input voltage range. Furthermore, an anti-aliasing filter is needed to attenuate any switching noise riding on the current feedback signal, before being inputted to the ADC. Current detection in each load/string is required to provide feedback to the controller, so that appropriate control action is taken depending on the number of connected strings/loads.

6.10.5 Open String or Load Disconnection Detection Circuit

A non-lossy method is used to detect current flow through each string/load. Resistive sensing is not considered primarily due to insertion loss which negatively impacts driver efficiency. The current detector selected is the CSDA1BA hall-effect switch. It is able to detect current flow between 0.25 - 1 A, and gives a digital low output when there is current flow. Furthermore, isolation is inherent, and provides a safe interface to the DSP. A circuit showing the implementation of the hall-effect switch is shown in Figure 6.10. A buffer 74LV04 is used to translate the voltage output of the current detector to correspond with the voltage input range of the DSP.

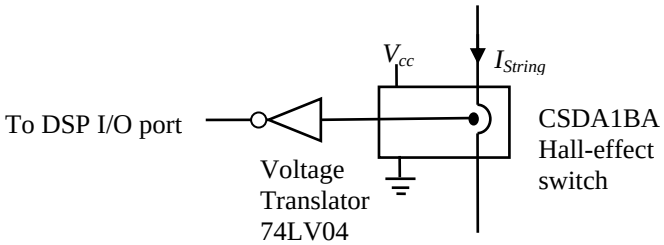


Figure 6.10: Current detection using a hall-effect switch and DSP interface.

6.10.6 Current Sensor Selection and Signal Conditioning

A current sensor based on resistive sensing is not considered as it does not provide isolation between the converter and the DSP, and dissipates power thus reducing system efficiency [110]. Therefore a non-dissipative current sensor that provides magnetic isolation is selected. Despite a resistive sensor having a greater bandwidth than a hall-effect current sensor, the sensor selected is the LEM CAS-6NP. It is a closed-loop flux gate sensor which has a bandwidth of 300kHz, and a current measuring range of +/- 6 A. The practical sensor output voltage V_s with respect to current flow I is given by;

$$V_s = 0.2064 \cdot I + 2.5 \tag{6.20}$$

Since the ADC input voltage range from 0 - 3.3V, the output voltage range of the sensor has to be signal conditioned to match the ADC input voltage range, as shown in Table 6.6.

Table 6.6: The current sensor output and required signal conditioning circuit output voltage

I (Current Flow)	$\boldsymbol{V_s}$ (Sensor Output Voltage)	$\boldsymbol{V_{sc}}$ (Signal Conditioning Circuit Output Voltage)
0 A	2.5 V	0 V
3 A	3.1192 V	3.3 V

A signal conditioning circuit with an output voltage V_{sc}, can be described as;

$$V_{sc} = m \cdot V_s - b \tag{6.21}$$

Thus substitution of Equation (6.20) into (6.21), and using the values for V_s and V_{sc} when I = 0 A and I = 3 A from Table 6.4, a set of simultaneous Equations are obtained. The values m and b are found as 5.3294 and 13.3236 respectively. Implementation of Equation (6.21) is done using an operational amplifier circuit given in Figure 6.11(a), where;

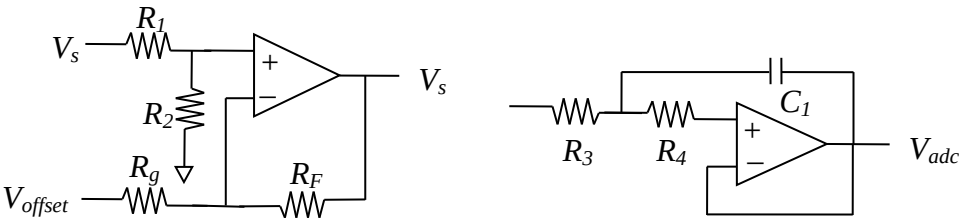
$$m = \left(\frac{R_2}{R_1 + R_2} \right) \cdot \left(1 + \frac{R_F}{R_g} \right) \tag{6.22}$$

$$b = \left(V_{offset} \cdot \frac{R_F}{R_g} \right) \tag{6.23}$$

Using V_{offset}=2.5 V, the required resistance values are obtained as; R_1=6.2 kΩ, R_2=33 kΩ, R_F=16 kΩ and R_g=3 kΩ. The selected op-amp is TL974, which features a gain-bandwidth of 12 MHz.

6.10.7 The Anti-aliasing Filter and Buffer Selection

The anti-aliasing filter is necessary to prevent switching noise from being sampled by the ADC. A low pass filter with a cut off frequency of 80 kHz is selected, which is low enough to avoid aliasing errors, as it is below half the switching frequency of 200 kHz. A second-order low-pass sallen-key topology is used for simplicity. The filter is shown in Figure 6.11(b), with R_3=1.2 kΩ , R_4=2.4 kΩ and C_1=1 nF. The selected op-amp is TL974. The DSP PWM output port has amplitude of 3.3 V, whereas the gate driver input requires a signal with a 5 V amplitude, therefore a buffer with a voltage level translation from 3.3 V to 5 V is required. The selected buffer is 74LV244.



(a) The signal conditioning circuit (b) The anti-aliasing filter

Figure 6.11: The interface circuits.

6.10.8 Practical Set-up

The full practical set up circuit diagram is given in Figure 6.12.

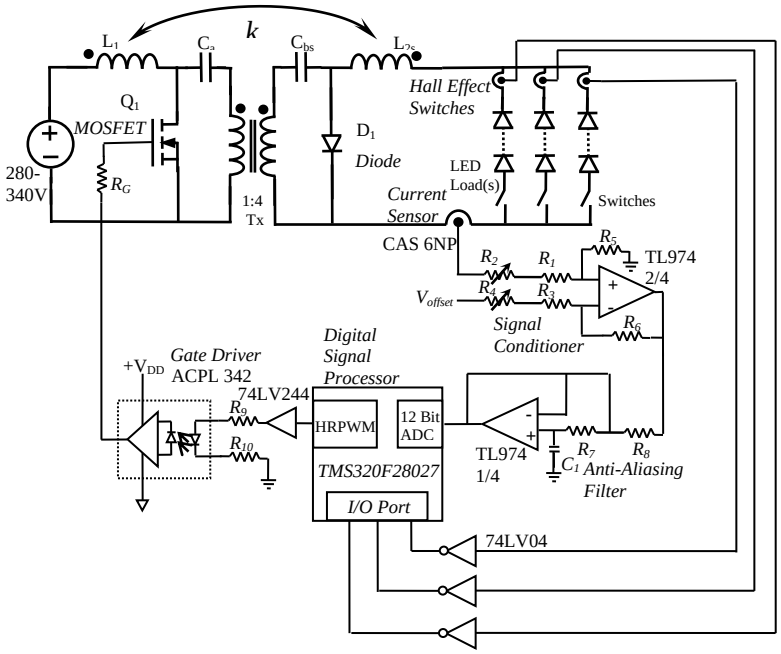


Figure 6.12: Practical setup circuit diagram.

6.11 SIMULATED AND PRACTICAL CLOSED-LOOP CONVERTER RESPONSE WITH DIGITAL CONTROL

To verify controller operation, the output inductor current response is observed for;

(i) Step change in input voltage

(ii) Step change in dimming reference

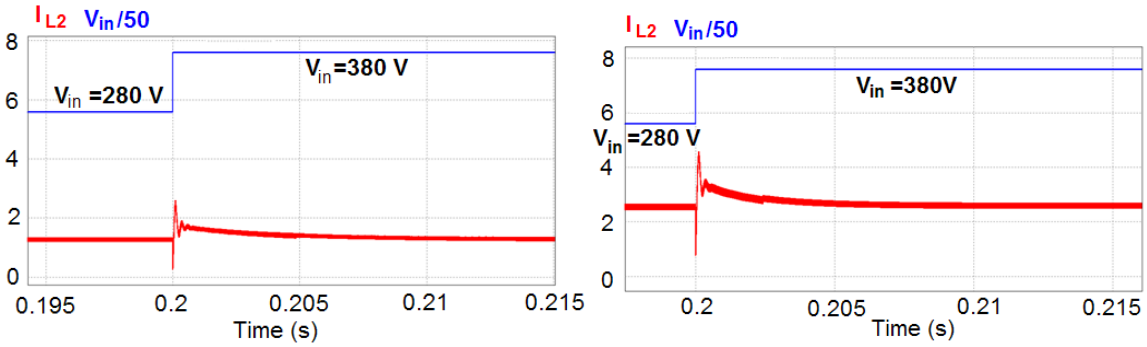
(iii) Step change in increasing load/strings

(iv) Step change in reducing load/strings

6.11.1 Simulated Driver Current Response for a Step Input Voltage

Figure 6.13 (a) shows the load current response as the dc input voltage is stepped from 280 V to 380 V. The load current is seen to settle smoothly within 12 ms after the step change. Figure 6.13 (b) shows the load current response as the dc input voltage is stepped from 280 V to 380 V for a dimming level of 0%. The rise-time, settling-time, overshoot are summarised in Table 6.7.

The simulated current regulation is seen to be 0.994% and 0.548% for a dimming level of 50% and 0% respectively. This satisfies the control objective of the desired current regulation of <1%. The overshoot for 50% and 0% dimming is seen to be 98.93% and 79.46% respectively and meets the desired controller objective of <100% overshoot.



(a) Step change for 50% dimming (b) Step change for 0% dimming

Figure 6.13: The driver output current response for a step input voltage from 280-380 V

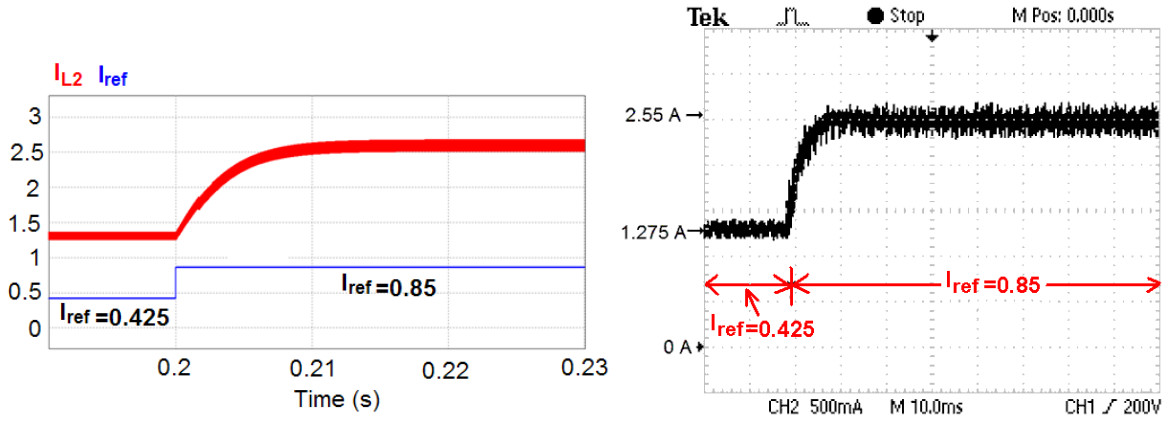
The settling-time when the dimming level is 50% and 0% is 12 ms and 6 ms respectively. This again satisfies the controller objective of settling-time <30 ms.

Table 6.7: The load current settling-time, % overshoot and current regulation for 0% and 50% dimming levels

Dimming Level %	$I_{L2av280V}$	$I_{L2av380V}$	**Settling-Time (ms)**	**Maximum I_o(A)**	**Overshoot %**	**Current Regulation %**
50	1.2641	1.2768	12	2.54	98.93	0.994
0	2.538	2.552	6	4.58	79.46	0.548

6.11.2 Practical Simulated and Load Current Response for a Current Reference Step Change

The driver output load current is observed when a step change in the current reference is done from a 50% to 0% dimming level. The input voltage is 340V and 3-strings are connected. From the simulated step response seen in Figure 6.14(a), it is observed that the rise-time is 5.21 ms and the settling-time is 9.36 ms. For the practical step response seen in Figure 6.14(b), it is seen that the rise-time is 6 ms and the settling-time is 10 ms. The simulated and practical step responses are fairly similar, and this shows successful practical controller design. The obtained simulated and practical rise and settling-times ensure a smooth transition between one dimming level and another for the LED load; making it comfortable for the human eye.



(a) Simulated driver output current response (b) Practical driver output current response

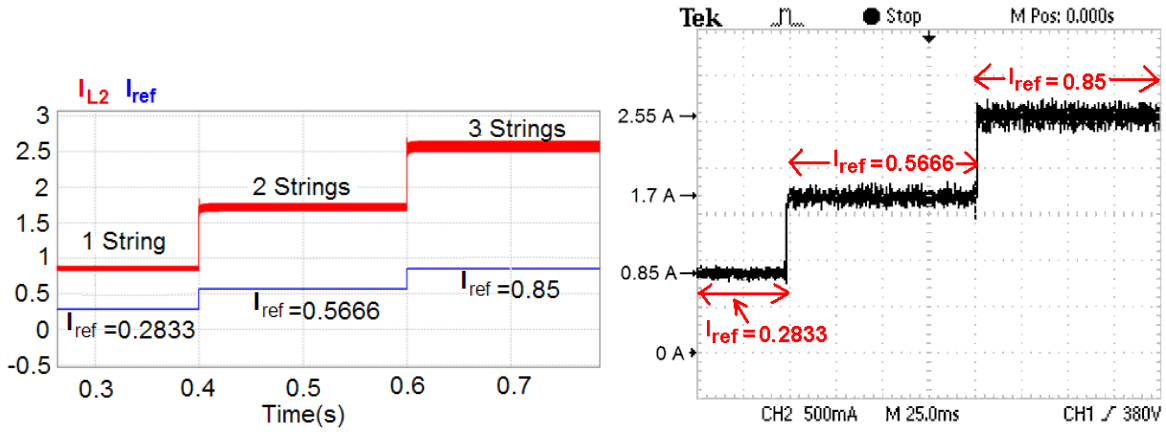
Figure 6.14: Driver output current response for a step input current reference from 0.4266 to 0.85

6.11.3 Simulated and Practical Current Response for Step Changes in Increasing Load

Sequential loading of an LED driver driving multiple loads is simulated in this Section. The total LED driver load is stepped up by sequentially connecting lower LED loads/strings connected in parallel to the driver. The load is then stepped up by connecting 1, 2 and 3 LED strings. The input voltage considered is 340 V. Two dimming levels are also considered, 0% and 50%. Simulated and practical responses are shown and discussed for the considered dimming levels and load step changes.

Figure 6.15(a) shows the simulated response while Figure 6.15(b) shows the practical response, when the dimming command is 0%. The simulated and practical rise-time and settling-times are summarized in Table 6.7. From Figure 6.15, as the load is stepped from 1 string to 2 strings, the simulated current rise-time is 0.056 ms, while the settling-time is 1.5 ms. The practical rise-time is 0.07 ms and the settling-time is 2 ms. Similarly, when the load is stepped from 2 strings to 3 strings, simulated rise-time is 0.044 ms and the settling-time is 1.3 ms. The practical rise-time is 0.05 ms and the settling-time is 1.5 ms. The practical rise and settling-times are fairly similar to the simulation, and therefore validate the theoretical controller design.

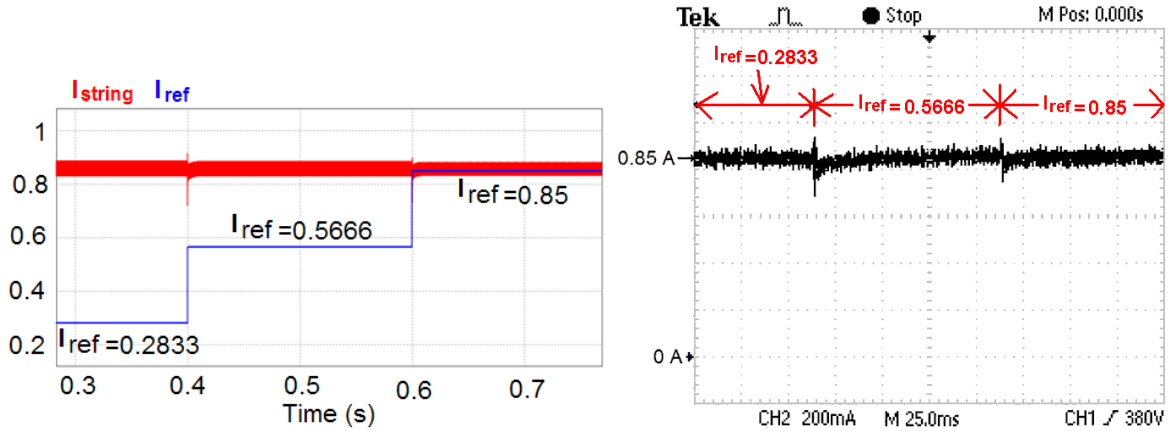
These responses as the load is stepped are quite fast, and ensure that the desired light output from each string/load is quickly reached as soon as it is connected and is in agreement with the corresponding bandwidth of the system.



(a) Simulated total driver output current (b) Practical total driver output current

Figure 6.15: Driver output current response for a step changes in load for a 0% dimming level

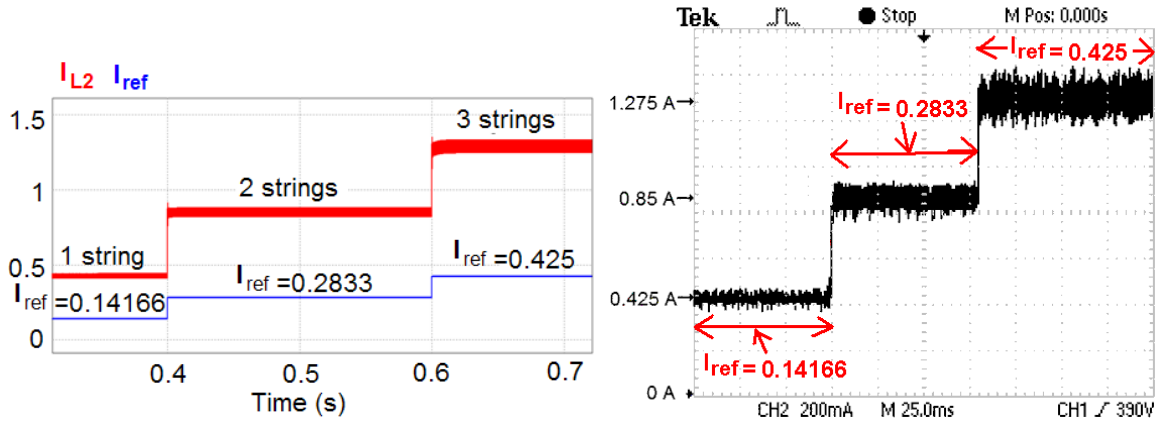
Moreover, the simulated and practical rise and settling-times satisfy the load step change objectives; where the rise and settling-times are <0.1 ms and <5 ms respectively. The average driver output current when 1, 2, and 3 strings are connected is noted as 0.85 A, 1.7A and 2.55 A respectively for both the simulation and the practical results.



(a) Simulated single string current (b) Practical single string current

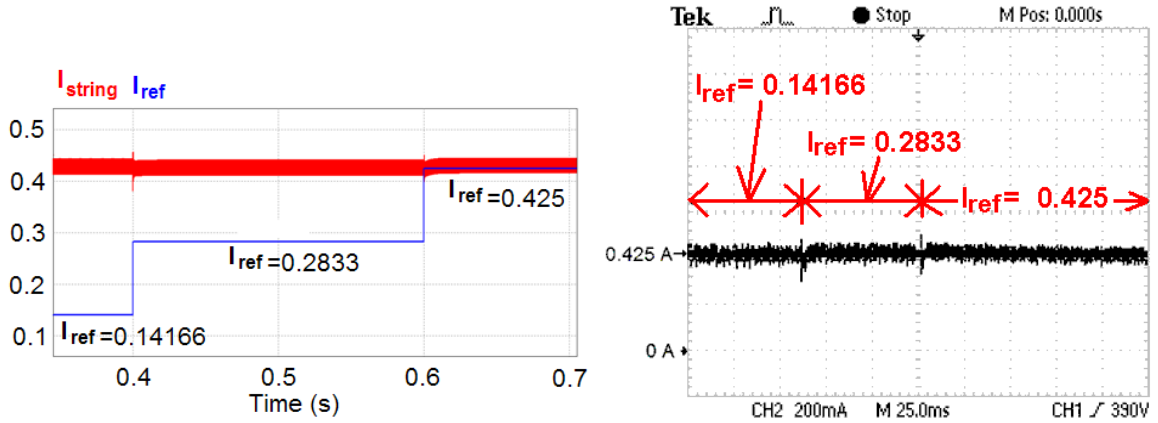
Figure 6.16: The current through the first string, as other loads/strings are sequentially connected, for a 0% dimming level.

Figure 6.17 shows the driver output current response to step changes in load. The dimming level is 50%. From Figure 6.17(a), when the load is stepped from 1 to 2-strings, the simulated rise and settling-time is 0.054 ms and 2.79 ms respectively. Similarly, from Figure 6.17(b), the practical rise-time and settling-time is 0.07 ms and 3 ms respectively.



(a) Simulated total driver output current (b) Practical total driver output current

Figure 6.17: The driver output current response for a step changes in load for a 50% dimming level



(a) Simulated single string current (b) Practical single string current

Figure 6.18: The current through the first string, as other loads/strings are sequentially connected, for a 50% dimming level.

From Figure 6.17(a), when the load is stepped from 2 to 3-strings, the observed simulated rise and settling-time is 0.043 ms and 2.1 ms respectively. Similarly, from Figure 6.17(b), the practical rise and settling-time is 0.05 ms and 2.5 ms respectively.

Once again, the simulated and practical responses show strong correlation, and therefore the simulated results are practically validated. In addition, the simulated and practical responses obtained indicates fairly quick controller response which satisfies the controller load step change objectives of rise and settling-times of <0.1 ms and <5 ms respectively. The average driver output

current when 1, 2, and 3 strings are connected is noted as 0.425 A, 0.85 A and 1.275 A respectively for both the simulated and practical results.

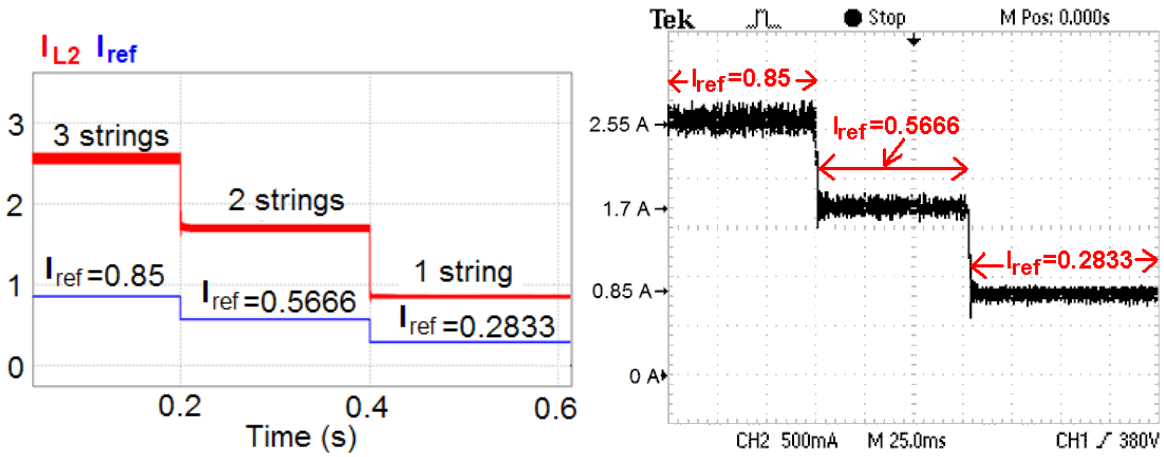
Figures 6.16 and 6.18 show the current in the first connected string/load for dimming levels of 0% and 50% respectively, as the other strings/loads are sequentially connected. From Figure 6.16 and 6.18, as other strings/loads are connected, it is observed that the average current in the string remains at 0.85 A and 0.425 A for 0% and 50% dimming levels respectively; for both the simulated and practical waveforms. This means that the optical output from the first connected string/load remains at the desired consistent level, even as the other loads/strings are sequentially connected to the driver. This satisfies one of the control objectives that the operation of the connected string/load is to remain unaffected regardless of whether the other loads are connected or not. The rise-times and settling-times from Figures 6.15 to 6.18 are summarised in Table 6.8.

Table 6.8: Rise and settling-times for driver output current for load transitions

Dimming Level	**Rise/Settling-Time**	**String Connection Transition**	**1-2**	**2-3**
0%	Rise-time (ms)	*Simulated*	0.056	0.044
		Practical	0.07	0.05
	Settling-time (ms)	*Simulated*	1.5	1.3
		Practical	2	1.5
50%	Rise-time (ms)	*Simulated*	0.054	0.043
		Practical	0.07	0.05
	Settling-time (ms)	*Simulated*	2.79	2.1
		Practical	3	2.5

6.11.4 Simulated and Practical Current Response for Step Changes in Reducing Load

Open-circuit failure or switching off loads/strings is simulated for a high power LED driver, driving three LED loads/strings. The total load is stepped from 3, 2, 1, and 0 connected strings. The input dc voltage considered is 340 V and the dimming level is 0%. Figure 6.19 shows the simulated and practical driver output current for step change reduction in connected strings. This is done to simulate an open-circuit fault or switching off each string, hence each connected string is sequentially disconnected.

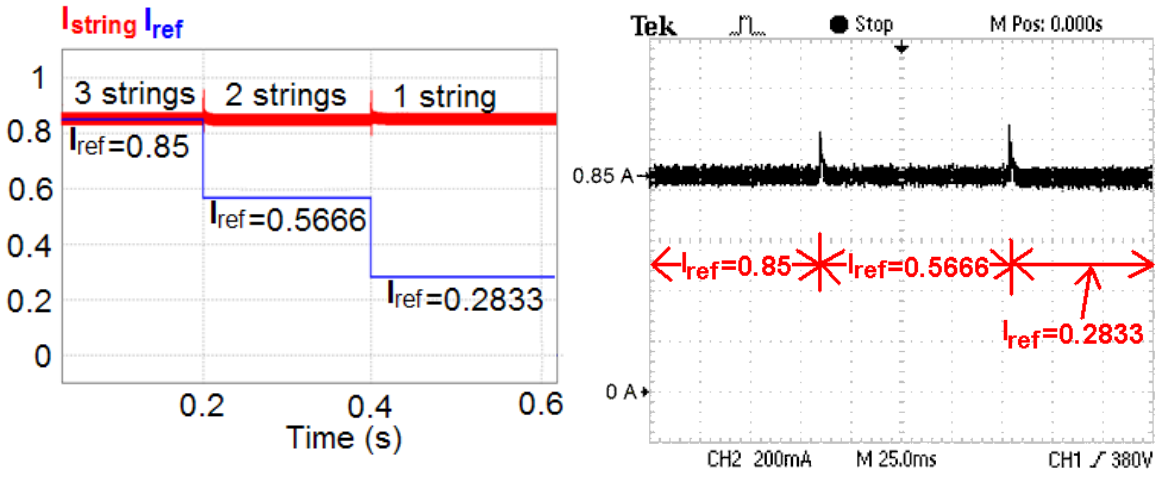


(a) Simulated driver output current (b) Practical driver output current

Figure 6.19: The driver output current response for a step changes in reducing load for a 0% dimming level.

From Figure 6.19(a), as the load is stepped from 3 to 2 connected strings, the simulated driver current fall-time is observed to be 0.0725 ms, while the settling-time is 1.4 ms. Likewise, from Figure 6.19 (b), the practical driver current fall-time is observed as 0.08 ms, while the settling-time is 1.6 ms. As the load is again stepped from 2 to1 string, the simulated driver current fall-time is 0.083 ms and the settling-time is 1.6 ms. The practical driver current fall-time is observed as 0.1 ms, while the settling-time is 1.8 ms. Again, similar to the step changes in increasing load, this response is quite fast, and shows that the controller reacts in a short time to changes in load. Thus the controller performs an excellent fault-tolerant function.

Figure 6.20 shows the simulated and practical current in the third connected string. For the given dimming level of 0%, the string current is seen to be constant at an average of 0.85 A for both the simulated and practical waveforms. Once again, this shows that the optical output of this string is not affected by the open-circuit failure or intentional switching off of the other strings. This shows the successful implementation of a controller which allows the fault-tolerant function.



(a) Simulated single string current (b) Practical single string current

Figure 6.20: The current through the third string, as other loads/strings are sequentially disconnected, for a 0% dimming level

Figure 6.21 shows the various LED loads/strings as they are practically driven, for a 0% dimming level, where each connected string has a forward current of 0.85 A.

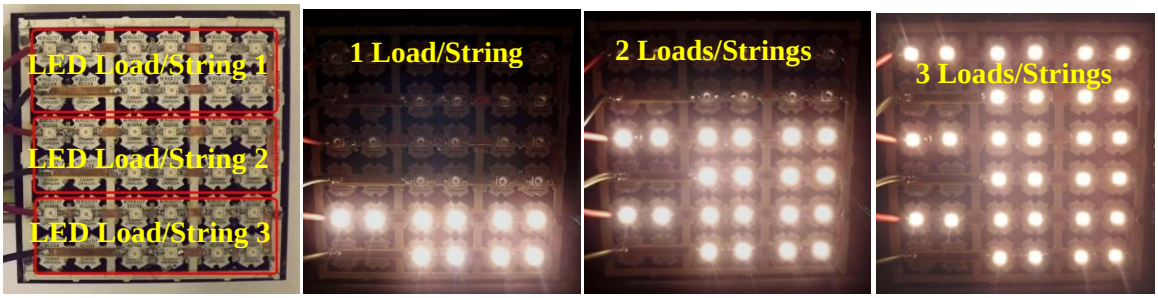


Figure 6.21: Connected LED/Strings Loads for 0% dimming, where each load /string has a forward current of 0.85 A.

6.12 CHAPTER CONCLUSION

It was found out that the tighter the coupling coefficient (k=0.98), for both NSC and SC, the higher the system bandwidth, transient response and system damping, as compared against loosely coupled (k=0.5) and NC inductors (k=0); for the coupled cuk converter. Also, it becomes easier to compensate tightly coupled inductors (k=0.98) than it is for loosely coupled inductors (k=0.5) or NC inductors (k=0). Thus it is concluded that tight coupling can achieve better system performance for the coupled cuk converter.

A digital controller was designed and implemented for two concepts namely; control of a single high power LED driver with independent multiple LED loads, and the control of a fault-tolerant high power LED driver with open-circuit string failure detection. In both cases, lossless current detection is done using hall-effect switches which interface seamlessly with the DSP. The controller specifications were given for the current-loop, and the compensator was designed via the emulation method. The compensator was designed to ensure stability for; input voltage range 280 - 380 V, dimming levels of 0%, 25% and 50%, and connected strings/loads 1, 2 and 3.

Despite the low bandwidth achieved, it was shown that the designed controller meets application requirements and has excellent performance. The required ADC and DPWM resolution requirements to avoid limit cycling for a current controlled isolated cuk converter were determined and used to select the appropriate DSP, given the current regulation value needed. An algorithm for sensing disconnected loads/strings was devised for implementation into the DSP. Hardware interfacing design of the selected hall-effect switches, current sensor signal conditioning and the required anti-aliasing filter to the DSP was done and practically implemented.

To test the controller, step changes in input voltage from 280 – 380 V was simulated for dimming levels of 50% and 0%, with 3 strings connected. The settling-time, overshoot and current regulation obtained were within the controller specifications and show successful controller design. Step changes in increasing loads/strings was simulated and practically done to emulate a converter supplying multiple loads. The simulation and practical results show excellent output driver current performance. Step changes in reducing loads was also simulated and done practically, to simulate an LED driver supplying multiple loads, or to replicate string failure; with excellent driver output current response from both simulated and practical results.

In conclusion, successful lossless current sensing in each LED string was achieved by using hall-effect switches, for the purposes of lossless LED string fault detection. This method does not impact the driver efficiency negatively. Finally, a novel LED driver was devised, that can drive multiple low power LED loads, which can be individually switched on or off; without affecting the operation of the connected loads was developed. This novel driver can simplify and reduce the costs of presently available LED lighting systems.

CHAPTER 7 DRIVER EFFICIENCY AND CURRENT REGULATION RESULTS

The SC inductor for the isolated cuk converter that was designed is employed as an LED driver. The fault-tolerant LED driver and the novel multiple LED load driver efficiencies and current regulation results are determined in this Chapter. The practical results are obtained with the digital closed-loop control system in place.

The analytical, simulated and practical current and voltage results for the various converter components are determined and compared. Various component waveforms, both simulated and practical are presented to validate the driver operation. The simulated results are obtained using PSIM software. The analytical efficiency and load current regulation are determined and compared with practical results. This is done for the LED driver supplying 3 strings/loads and also for 1 string/load. For both analytical and practical results, the dimming levels considered are 0%, 25% and 50%, for an input dc voltage range of 280 V to 380 V.

7.1 ANALYTICAL RESULTS EQUATIONS

The various currents and voltages for various components used in the converter are determined analytically, so that a comparison can be made with the simulation results. The inductor L_1 and L_2 peak-to-peak (p-p) and RMS currents are obtained using Equations (5.5) and (5.6) respectively. Inductor voltages V_{L1} and V_{L2} are given as;

When switch is on;

$$V_{L_1} = V_{in} \tag{7.1}$$

$$V_{L_2} = \frac{V_{in}}{n} \tag{7.2}$$

When switch is off;

$$V_{L_1} = -V_o \cdot n \tag{7.3}$$

$$V_{L_2} = -V_o \tag{7.4}$$

The coupling capacitor C_a and C_{bs} RMS currents are obtained using Equations (5.21) and (5.27) respectively. The voltage pk-pk ripple across the capacitors C_a and C_{bs} is given by;

$$\Delta V_{C_a,pk-pk} = \frac{I_{L_2,av} \cdot \delta \cdot T_{sw}}{C_a \cdot n} \tag{7.5}$$

$$\Delta V_{C_a,pk-pk} = \frac{I_{L_2,av} \cdot \delta \cdot T_{sw}}{C_{bs} \cdot n} \tag{7.6}$$

The MOSFET switch and diode RMS current are given by Equations (5.10) and (5.14) respectively. The blocking voltage of the MOSFET switch $V_{sw,Block}$, and diode $V_{d,Block}$, are given as;

$$V_{sw,Block} = V_{in} + n \cdot V_o \tag{7.7}$$

$$V_{d,Block} = \frac{V_{in}}{n} + V_o \tag{7.8}$$

The load current is the same as inductor L_2 current. The peak-peak load voltage $V_{LOAD,pk-pk}$ is given as;

$$V_{LOAD,pk-pk} = \Delta i_{L_2,pk-pk} \cdot R_D \tag{7.9}$$

Using the value of δ computed by Equation (4.13), using the value of R_D as 13.61 Ω (for 0% dimming) and using a dc input voltage V_{in} as 340 V, the analytical , simulated and practical results are compared in the proceeding Section.

7.2 SIMULATION AND PRACTICAL RESULTS

The simulated results are obtained using the circuit given in Figure 7.1, which is simulated using PSIM software [112]. The practical results are obtained from the constructed circuit shown in Figure 7.2.

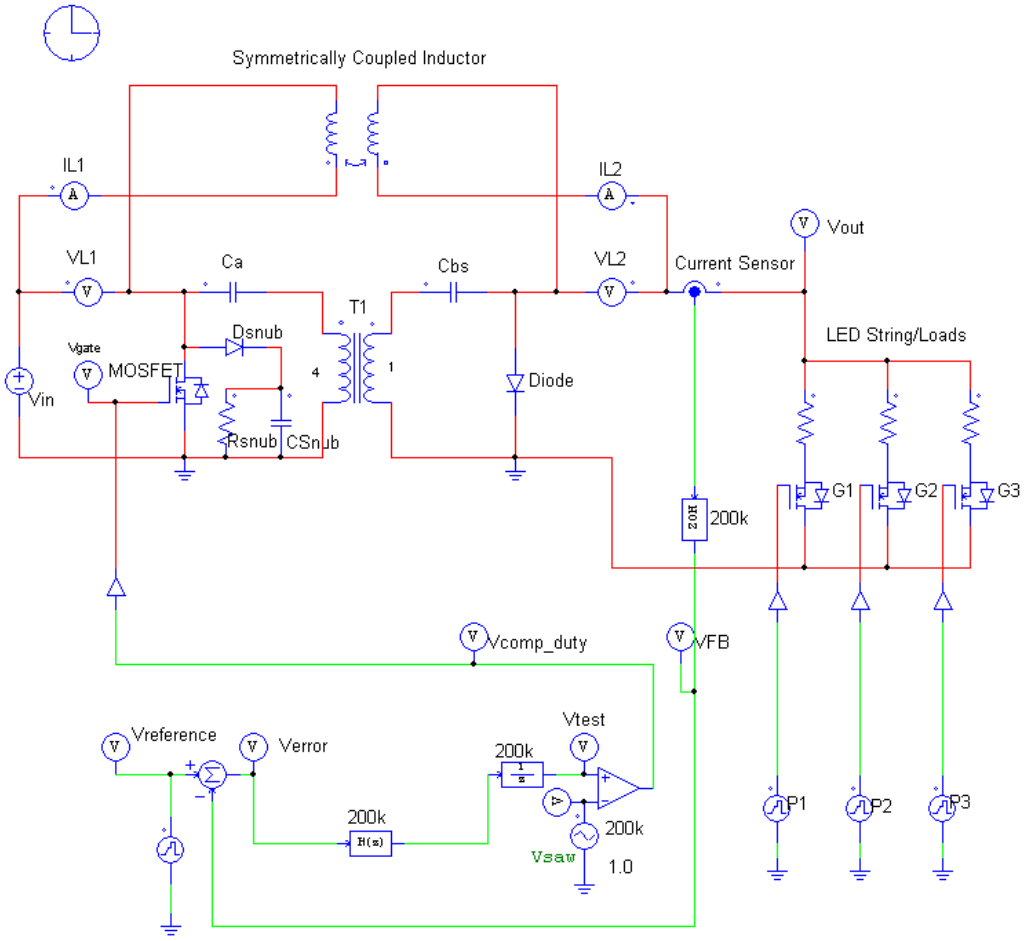
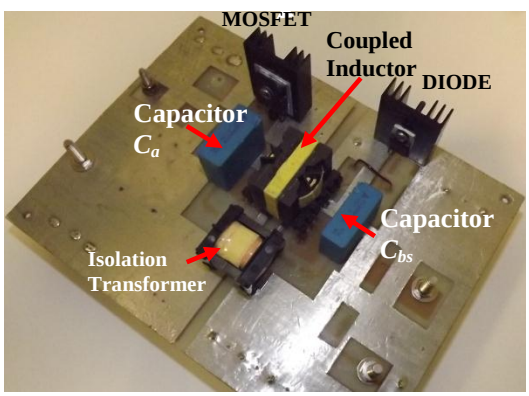
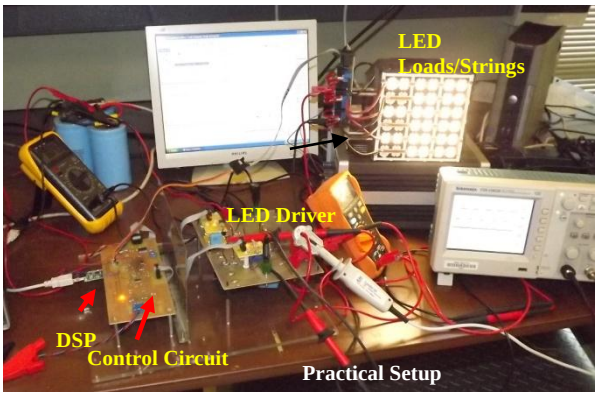


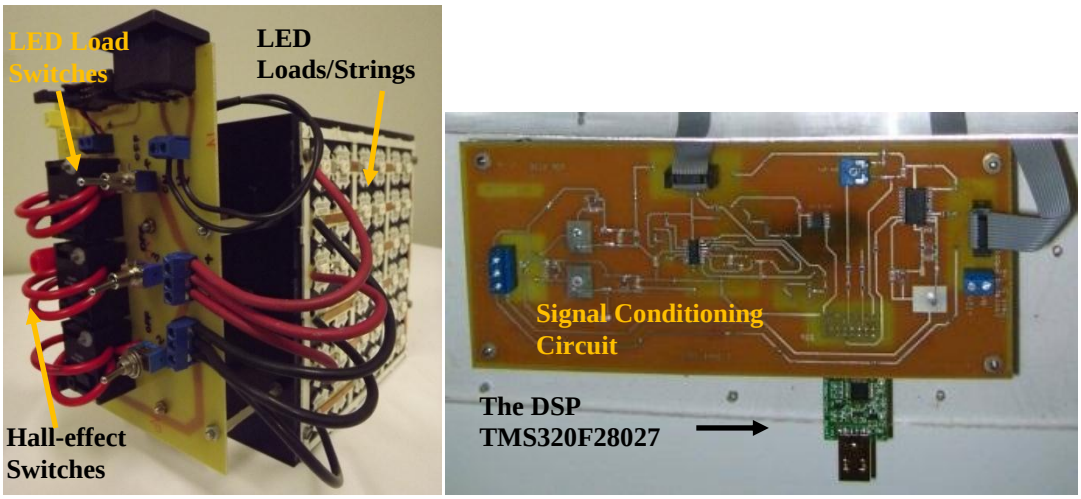
Figure 7.1: Simulation circuit.



(a) The designed LED driver



(b) The practical Setup



(c) The LED loads/strings (d) The DSP and signal conditioning circuit

Figure 7.2: The designed practical LED driver system.

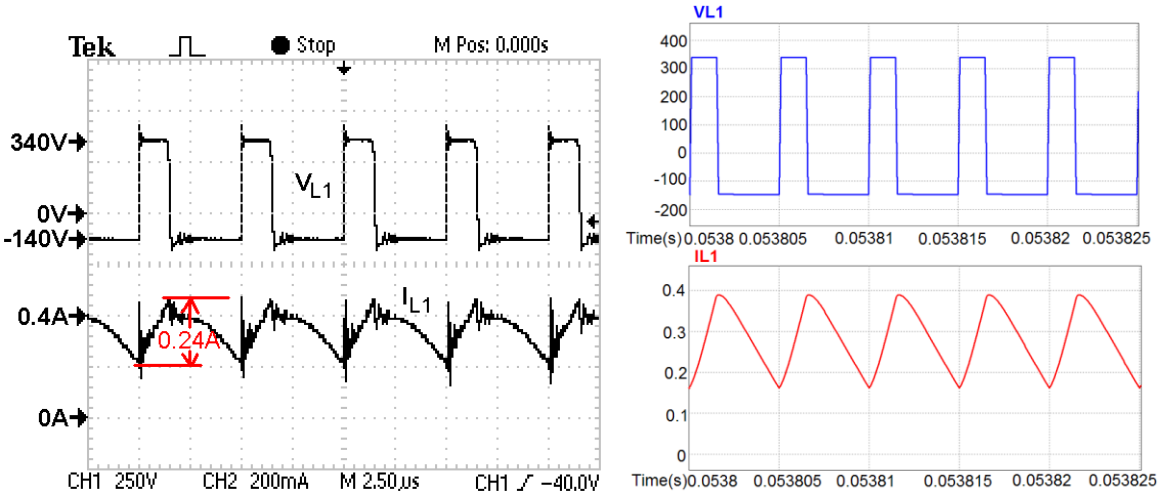
7.2.1 Results for Inductor L_1

The inductor L_1 current results are given by Table 7.1. For the analytical, simulated and practical inductor voltages V_{L1} and V_{L2} are; when the active switch is on, V_{L1} = 340V, V_{L2} = 85V; when the active switch is off, V_{L1} = -138.8 V and V_{L2} = -34.7 V.

Table 7.1: Inductor L_1 current results

Parameter	Analytical	Simulated	Practical
$\Delta i_{L_1,pk-pk}$ (A)	0.225	0.226	0.24
$i_{L_1,RMS}$ (A)	0.268	0.287	0.313
$i_{L_1,av}$ (A)	0.260	0.278	0.302

The simulated and practical peak-peak current ripples agree reasonably well within an 8.6% error margin. This could be attributed to measurement and component value errors. For the practical, the peak-peak ripple is 79.5%. The practical and simulated inductor L_1 waveforms are shown in Figure 7.3. It is observed that the practical and simulated waveforms agree well.



(b) Practical waveforms (b) Simulated waveforms

Figure 7.3: Inductor L_1 waveforms

7.2.2 Results for Inductor L_2

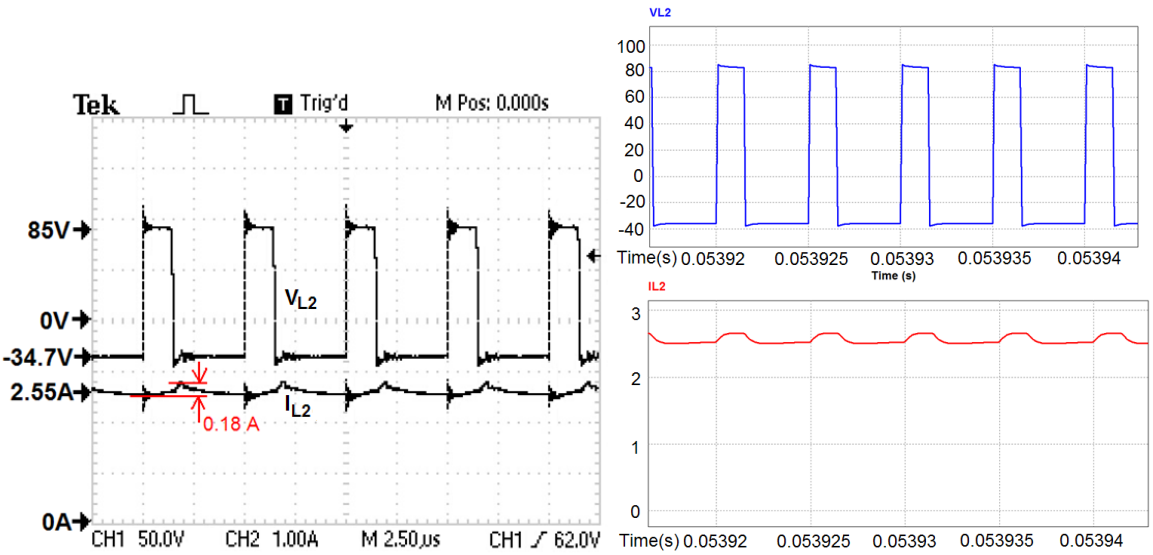
The inductor L_2 current results are given by Table 7.2. The load current is the same as inductor L_2 current, as no output filtering capacitor is used in the isolated cuk converter. The analytical and simulated inductor L_2 current results are similar. However, it is noted that the practical current $i_{L_2,pk-pk}$, is higher by 13.9% as compared to the simulated result. This could be attributed to the practical current probe measurement error and errors in component values.

Table 7.2: Inductor L_2 current results

Parameter	Analytical	Simulated	Practical
$\Delta i_{L_2,pk-pk}$ (A)	0.156	0.158	0.18
$i_{L_2,RMS}$ (A)	2.550	2.550	2.552
$i_{L_2,av}$ (A)	2.55	2.55	2.552

The practical peak-peak current ripple obtained by the SC inductor is 7.05%. This low ripple magnitude ensures that the LED load efficacy is maintained above 99% [38]. The advantage of using a SC inductor which achieves this low ripple eliminates the need for an output filtering capacitor; reducing driver component count and cost. Therefore, the objective of obtaining an LED driver that yields high LED efficacy, as well as lower component count and cost is achieved.

Figure 7.4 shows the practical and simulated inductor L_2 current and voltage waveforms. It is clearly evident that the practical and simulate waveforms bear close similarity.



(c) Practical waveforms (b) Simulated waveforms

Figure 7.4: Inductor L_2 waveforms.

7.2.3 Results for Coupling Capacitors C_a and C_{bs}

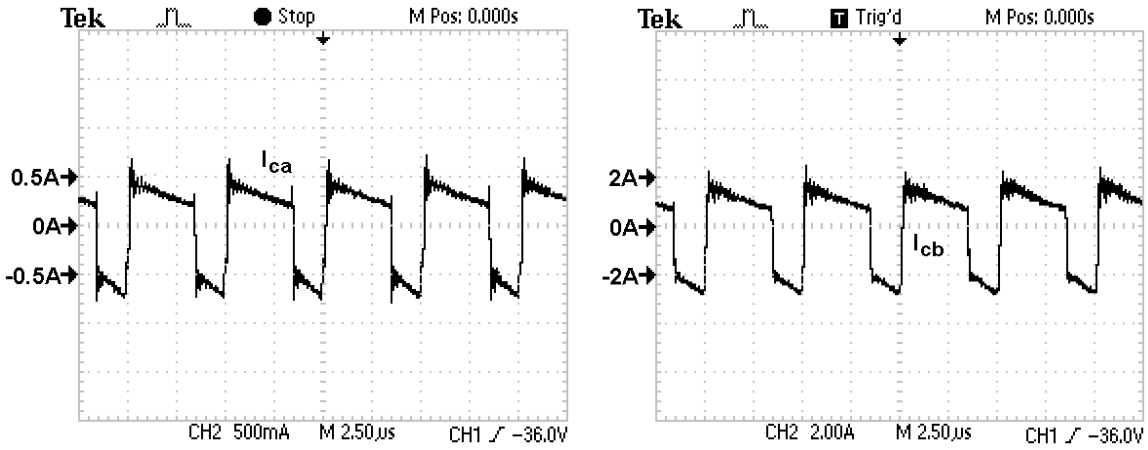
Table 7.3 shows the coupling capacitor current and voltage analytical, simulated and practical results.

Table 7.3: The Coupling capacitor results

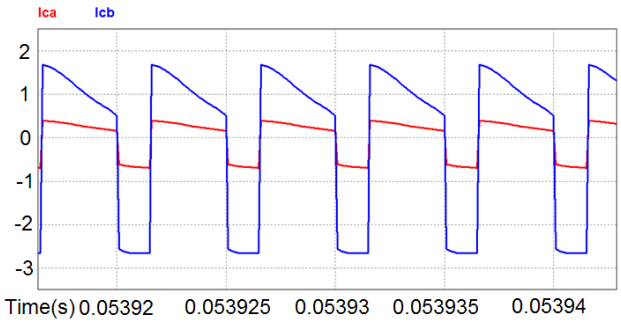
Parameter	Analytical	Simulated	Practical
$i_{C_a,RMS}$ (A)	0.419	0.421	0.43
$i_{C_{bs},RMS}$ (A)	1.745	1.742	1.76
$\Delta V_{C_a,pk-pk}$ (V)	2.02	2.131	2.2
$\Delta V_{C_{bs},pk-pk}$ (V)	0.253	0.261	0.28

From Table 7.3 analytical, simulated and practical results are all seen to be in excellent agreement. The analytical, simulated and practical average voltage across the coupling capacitors was obtained as; $V_{C_a,av}$ = 340 V and $V_{C_{bs},av}$=34.7 V. The practical $V_{C_a,pk-pk}$ and $V_{C_{bs},pk-pk}$ magnitudes obtained compare well with the simulated and analytical values. It can be concluded that the capacitor sizing was successfully done. Figure 7.5 shows the coupling capacitor practical and simulated current

waveforms. The practical and simulated coupling capacitor voltage waveforms are shown in Figure 7.6.

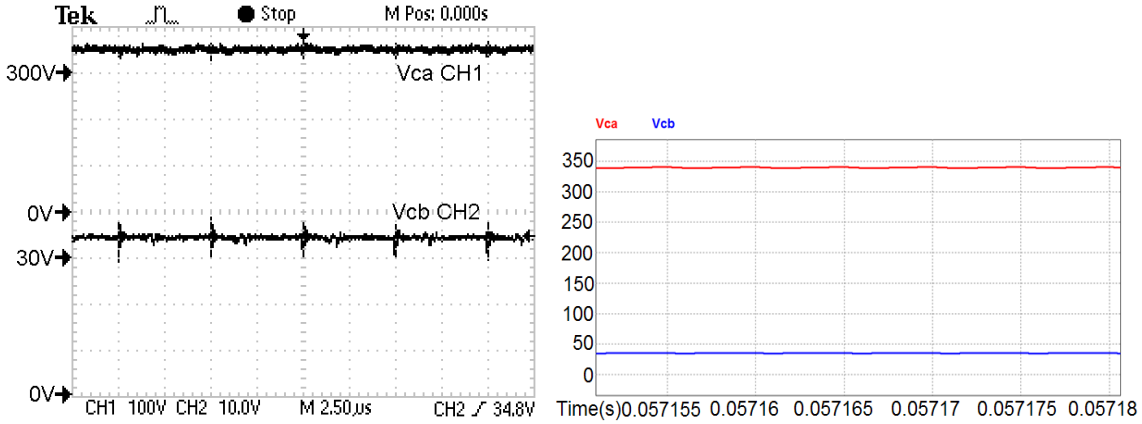


(a) Capacitor C_a practical waveform (b) Capacitor C_{bs} practical waveform



(d) Capacitor C_a and C_{bs} simulated waveforms

Figure 7.5: Practical and simulated coupling capacitor current waveforms



(a) Practical waveforms (b) Simulated waveforms

Figure 7.6: Coupling capacitors C_a and C_{bs} voltage waveforms.

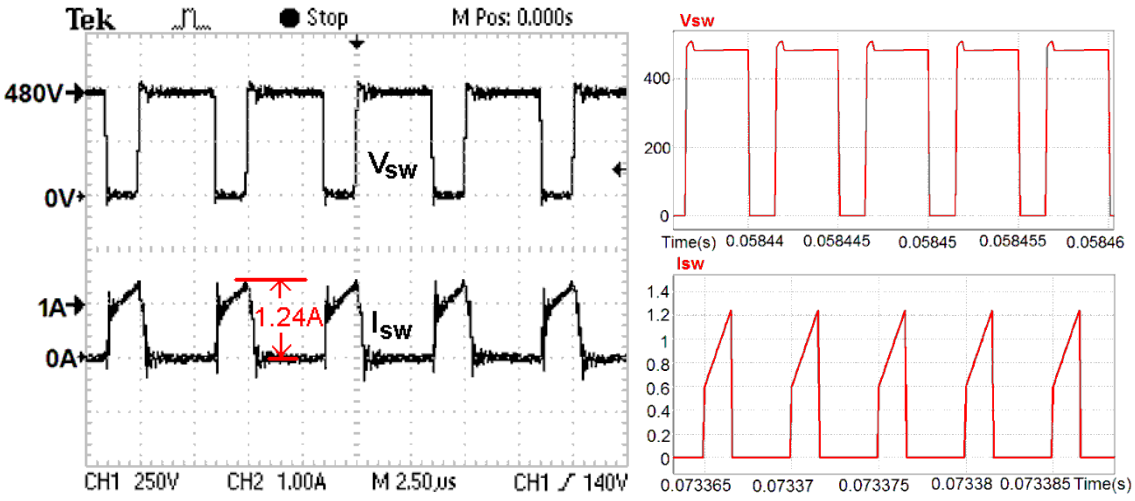
7.2.4 Results for the Switch and Diode

The switch and diode results are given in Table 7.4.

Table 7.4: The active switch and diode results

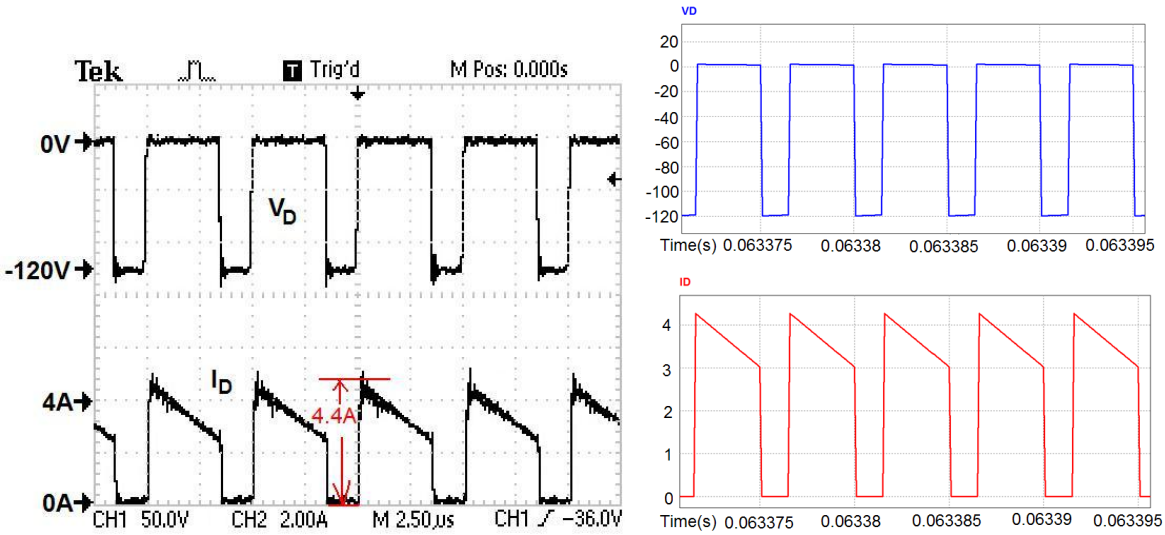
Parameter	Analytical	Simulated	Practical
$V_{sw,Block}$ (V)	478.74	478.68	479
$i_{sw,RMS}$ (A)	0.5	0.508	0.54
$i_{sw,pk}$ (A)	1.226	1.23	1.24
$V_{d,Block}$ (V)	119.71	119.62	120
$i_{d,RMS}$ (A)	3.073	3.047	3.16

From Table 7.4, the analytical, simulated and practical voltage and current results are in good agreement. Figure 7.7 shows the practical and simulated active switch waveforms, while Figure 7.8 shows the diode practical and simulated waveforms. From these Figures, it is observed once again that the practical and simulated waveforms bear close similarity.



(a) The switch practical waveforms (b) The switch simulated waveforms

Figure 7.7: The active switch waveforms.



(a) The diode practical waveforms (b) The diode simulated waveforms

Figure 7.8: The diode voltage and current waveforms.

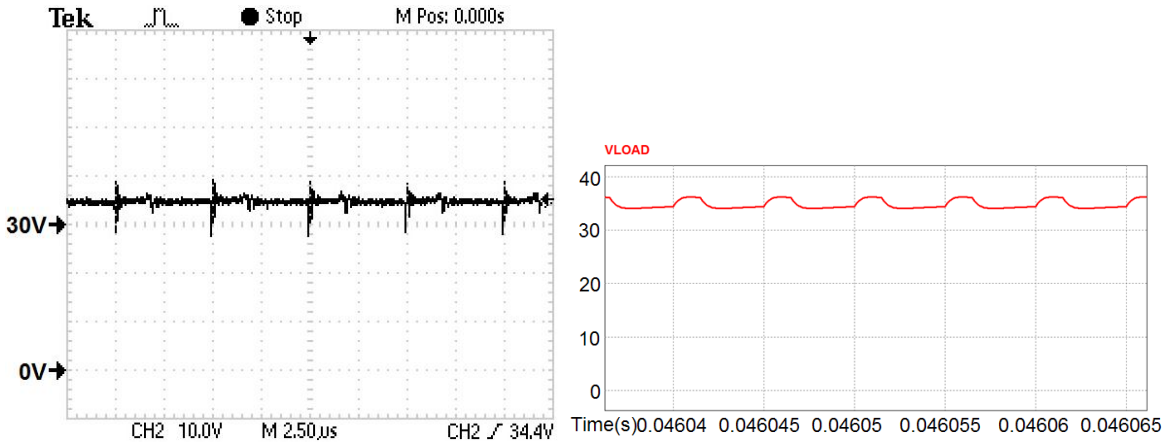
7.2.5 Results for the LED Load Voltage

The LED load voltage results are given in Table 7.5.

Table 7.5: The LED load voltage results

Parameter	Analytical	Simulated	Practical
$V_{Load,av}$ (V)	34.71	34.71	34.7
$\Delta V_{Load,pk-pk}$ (V)	2.123	2.127	2.46

From Table 7.5, the analytical, simulated and practical average voltage $V_{Load,av}$ and peak-peak voltage, $\Delta V_{Load,pk-pk}$ results are in close agreement with each other. Figure 7.9 shows the practical and simulated LED load voltage waveform. The LED load consists of 3 strings whose dynamic resistance, R_D is 13.6 Ω.



(a) The practical waveform (b) the simulated waveform

Figure 7.9: The LED load voltage waveform.

7.2.6 Results for L_2 Current for 0% and 50% Dimming Levels and Various Connected Strings/Loads

The analytical, simulated and practical peak-peak current ripple, RMS and average current for the total connected load is tabulated in this Section. The dimming levels considered are 0% and 50%, and the number of connected strings/loads are 3, 2 and 1. The analytical values of duty ratio δ, load dynamic resistance R_D used for the analytical computation are found using (4.13) and (4.11) respectively. The input voltage is 340 V and Table 7.6 shows these results.

From Table 7.6, the analytical, simulated and practical results agree fairly well. As the dimming level is increased from 0% to 50%, the RMS $i_{L_2,RMS}$, peak-peak $\Delta i_{L_2,pk-pk}$ and average $i_{L_2,av}$ currents through inductor L_2, reduce proportionally by approximately 50% . The highest practical peak-peak ripple across L_2 is noted as 0.18 A when dimming is 0% and for 3 connected strings/loads. This is a 7.06% peak-peak current ripple across the 3 connected loads, which implies that the LED load efficacy is >99% [38].

The lowest practical peak-peak ripple across L_2 is noted as 0.04 A when dimming is 50% and 1 connected string/load. This is a 0.94% peak-peak current ripple across the 1 connected load, and results in an LED load efficacy of >99% [38]. It can be concluded that for the extreme dimming levels of 0% and 50%, and the connected strings/loads 1 and 3, the LED efficacy is maintained >99%. The designed LED driver satisfies one of the objectives that the LED load ripple should be

low enough to maintain a high LED efficacy of >99% for all dimming levels and connected strings/loads.

Table 7.6: The RMS, pk-pk and average current through L_2 for various dimming levels and connected LED strings/loads

Number of Connected Strings/Loads		**3**			**2**			**1**		
Dimming		$i_{L_2,RMS}$ (A)	$\Delta i_{L_2,pk-pk}$ (A)	$i_{L_2,av}$ (A)	$i_{L_2,RMS}$ (A)	$\Delta i_{L_2,pk-pk}$ (A)	$i_{L_2,av}$ (A)	$i_{L_2,RMS}$ (A)	$\Delta i_{L_2,pk-pk}$ (A)	$i_{L_2,av}$ (A)
Analytical	0%	2.550	0.156	2.55	1.7	0.10	1.7	0.85	0.057	0.85
	50%	1.275	0.084	1.275	0.85	0.06	0.85	0.425	0.03	0.42
Simulated	0%	2.550	0.158	2.55	1.71	0.11	1.7	0.850	0.058	0.85
	50%	1.275	0.089	1.275	0.85	0.06	0.85	0.425	0.031	0.42
Practical	0%	2.552	0.18	2.552	1.71	0.14	1.71	0.85	0.08	0.85
	50%	1.276	0.10	1.276	0.85	0.08	0.85	0.424	0.04	0.42

This is accomplished by the use of a SC inductor. Furthermore, it can be concluded that the low practical ripples obtained for the extreme dimming levels of 0% and 50% for 3 and 1 connected strings/loads, (7.06% and 0.94%), could aid in maintaining long LED life [38].

7.3 EFFICIENCY ANALYSIS

Efficiency analysis is carried out for the designed LED driver based on a SC inductor isolated cuk converter with the following parameters;

(i) V_{in} from 280 - 380V, 3 strings/loads, dimming levels of 0%, 25% and 50%

(ii) V_{in} from 280 - 380V, 1 string/load, dimming levels of 0% , 25% and 50%

The efficiency for afore-mentioned parameters is determined analytically and practically, and the results are compared in the proceeding Sections.

7.3.1 Analytical Efficiency Computation

The analytical losses occurring in the designed LED driver are determined using the following Equations are used; for the active switch loss, summation of Equation (5.7) and (5.9) ; Diode loss, summation of Equations (5.13) and (5.17); copper loss, Equation (5.41); capacitor loss, Equation (5.30); inductor core loss, Equation (5.44) and snubber loss, Equation (4.98). The core loss in the

isolation transformer is negligible as seen in Section 3.3.7.2 and is neglected in the loss computation. The duty ratio δ is computed using Equation (4.13), and the dynamic resistance R_D is obtained using Equation (4.11). The converter parameters given in Section 5.1 are used for the analytical loss computation. The efficiency η, is determined as [113];

$$\eta\,\% = 100 \cdot \frac{1}{1 + \frac{P_{Loss,Total}}{P_o}} \tag{7.10}$$

Where $P_{Loss,Total}$ is the total analytical loss, and P_o is the LED load output power. Figure 7.10 shows the analytical losses occurring in the LED driver, for an operating point of V_{in} = 340 V, 0% dimming and 3 strings/loads connected. It is observed that the major loss mechanisms are the switch loss and diode loss, which are 46% and 31% respectively, of the total analytical loss of 12.58 W at the given operating point. This means that if the switching and diode loss were to be reduced, this driver would have significant improvement in efficiency.

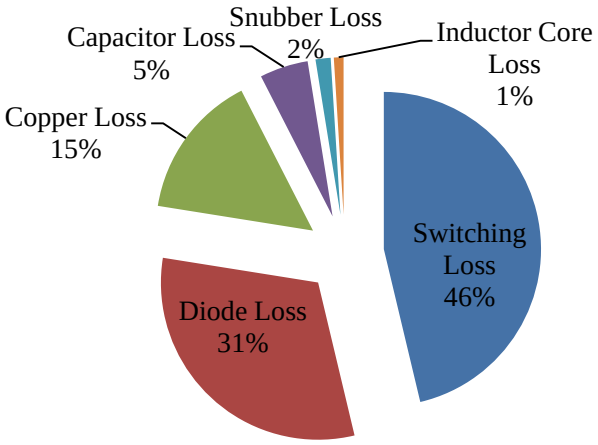


Figure 7.10: Analytical losses at V_{in} = 340V, at 0% dimming for 3 connected strings/loads.

7.3.2 Driver Efficiency for 3 Connected Strings/Loads

The analytical and practical driver efficiency is plotted in Figure 7.11, for 3 connected strings/loads for various input voltages and dimming levels. The practical efficiency measurements are done using average input and output voltages and currents. The practical efficiency is measured with the closed-loop digital average current control system in place. It is observed that the highest analytical and practical efficiencies are 87.6% and 87.2% respectively, for a 0% dimming level at 280 V. The lowest analytical and practical efficiencies are observed as 85.9% and 84% for a dimming level of

50% at 380 V. The differences in the analytical and practical efficiencies could be attributed to measurement errors. The analytical and practical efficiencies compare well, as the practical measurement is within a 2% acceptable tolerance margin, as compared to the analytical result. The difference between the analytical and practical efficiency measurements could be attributed to measurement and component value errors.

Also, as the input voltage is increased from 280 V to 380 V, the efficiency is seen to reduce, given a dimming level. As the input voltage increases, the RMS currents through the components reduces, which results in lower copper loss, capacitor loss and diode loss. On the other hand, since the switching loss is the dominant loss mechanism, and it increases with increasing input voltage. This results in an overall efficiency reduction as the input voltage is increased.

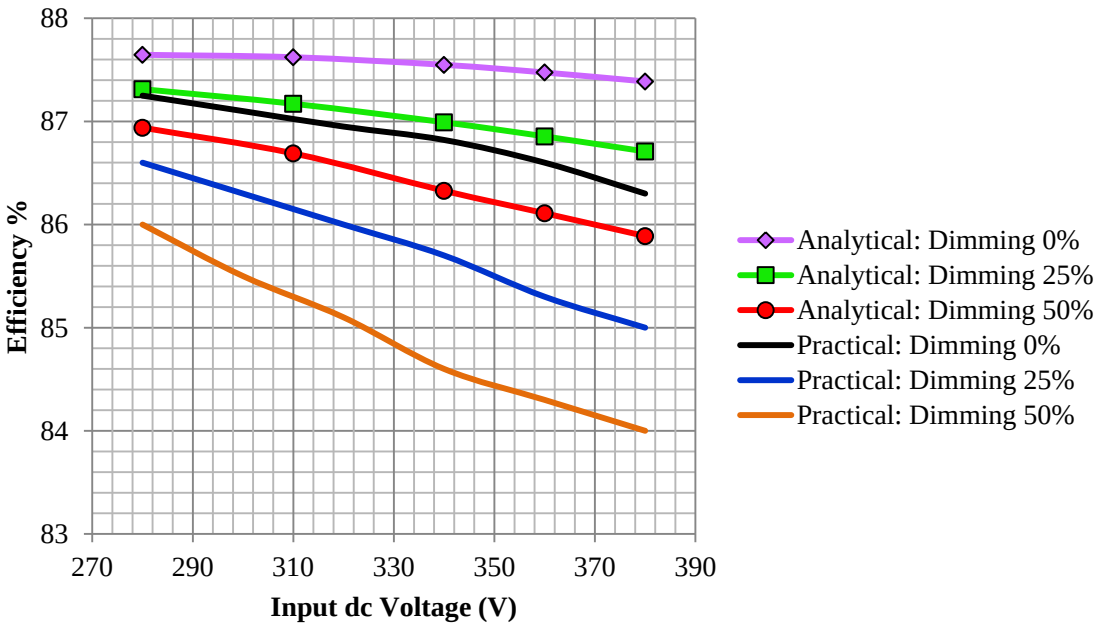


Figure 7.11: Analytical and practical efficiency with 3 connected strings/loads for various dimming levels.

For an LED driver driving 3 strings/loads, the practical peak efficiency achieved was 87.2% and is reasonably high. This satisfies the objective of achieving a high efficiency fault-tolerant LED driver supplying 3 LED strings, or an LED driver supplying 3 low power LED loads.

7.3.3 Driver Efficiency for 1 Connected String/Load

The analytical and practical driver efficiency is plotted in Figure 7.12, for 1 connected string/load, for various input voltages and dimming levels. The highest analytical and practical efficiencies are noted as 85% and 84.1% respectively, for a 0% dimming level at 280 V. The lowest analytical and practical efficiencies are observed as 78.1% and 75.3% for a dimming level of 50% at 380 V. The analytical and practical efficiencies compare well, as the practical measurement is within an acceptable 3.6% tolerance margin, as compared to the analytical result. The difference between the analytical and practical efficiency measurements could be attributed to measurement and component value errors.

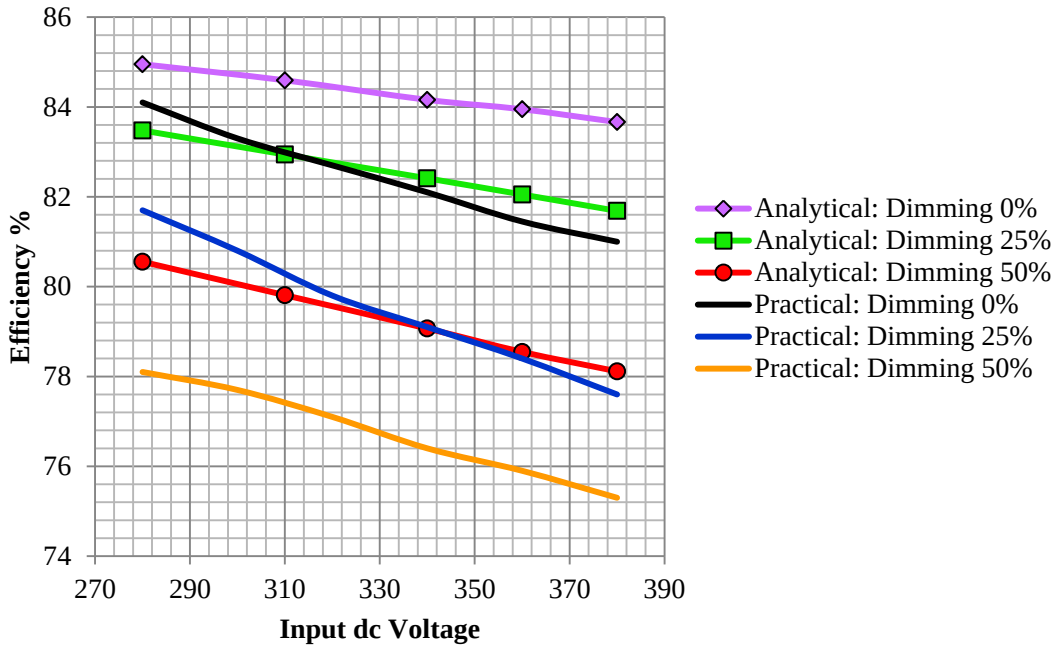


Figure 7.12: Analytical and practical efficiency with 1 connected string/load for various dimming levels.

The trend of reducing efficiency as the input voltage is increased, given a dimming level, is similar to the reducing efficiency trend noted in Section 7.3.2. This is again attributed to the increasing switching loss with increasing input voltage, which is the dominant loss mechanism. For a fault-tolerant LED driver supplying 1 string, or an LED driver supplying 1 low power LED load, the practical efficiency achieved of 84.1% is fairly high. This satisfies the objective of achieving a high efficiency fault-tolerant LED driver or a high efficiency LED driver supplying several low power LED loads.

7.3.4 Driver Efficiency at Various Power Levels

Table 7.7 shows the driver efficiencies at various power and load levels, at the nominal input dc voltage of 340 V. It is seen that for a given dimming level, when the load is reduced from 3 strings to 1 string, the efficiency is seen to reduce. For a 0% dimming level, when the load is reduced from 13.61 Ω to 40.83 Ω (corresponding to a power reduction from 88.5 W to 29.5 W), the efficiency reduces by 4.72%. Similarly, for a 50% dimming level, when the load is reduced from 25.57 Ω to 76.71 Ω, corresponding to a power reduction from 41.57 W to 13.86 W) the efficiency reduces by 8.2%.

Table 7.7: Efficiency at various power levels for V_{in} = 340 V

Dimming	Load	Power (W)	Efficiency
0%	3 Strings, 13.61Ω	88.5	86.82%
0%	1 String, 40.83 Ω	29.5	82.1%
50%	3 Strings, 25.57 Ω	41.57	84.6%
50%	1 String, 76.71 Ω	13.86	76.4%

Efficiency is normally a function of load, and it is expected that the efficiency will decrease as the load (or power) is reduced. It can be seen from Table 7.7, that the designed LED driver does have this characteristic.

7.4 PRACTICAL LOAD CURRENT REGULATION

The practical load regulation results as the input dc voltage is varied from 280 V to 380 V, are obtained by measuring the actual driver load current i_{LOAD}, and computing the difference from the desired current. The load regulation results are obtained for 0%, 25% and 50% dimming levels for 3 connected strings/loads and 1 connected string/load. The results are obtained with the closed-loop controller in place. The theoretical current regulation objective from Section 6.5 is given as <1%. The desired load current magnitudes are given in Table 7.8.

Table 7.8: The desired load current (i_{LOAD}) for various loads and dimming levels

Desired i_{LOAD}	0% Dimming	25% Dimming	50% Dimming
3 Strings/Loads (A)	2.55	1.9125	1.275
1 String/Load (A)	0.85	0.6375	0.425

7.4.1 Practical Load Current Regulation for 3 Connected Strings/Loads

Figure 7.13 shows the load current regulation for 3 connected strings/loads, as the input voltage is varied from 280 V to 380 V, given a dimming level of 0%, 25% and 50%.

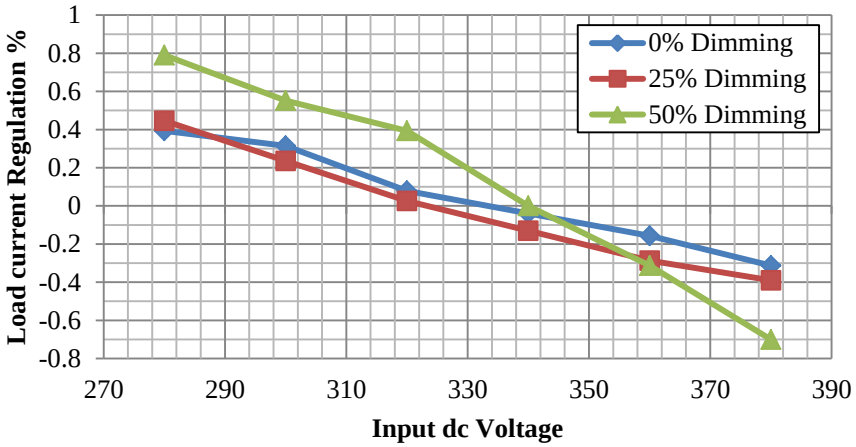


Figure 7.13: Load current regulation of various dimming levels for 3 connected strings/loads.

As seen in Figure 7.13, for all dimming levels, the best current regulation occurs when the input dc voltage is between 330 V and 340 V. For 0% dimming at the nominal voltage of 340 V, the regulation is noted as -0.04%. This shows excellent performance of the digital Average Current Control (ACC) system which maintains tight current regulation.

The poorest current regulation is observed for 50% dimming at 280 V as 0.79%, although this is still less than the theoretical 1% current regulation objective. It can be concluded that for the LED driver supplying 3 connected LED strings/loads, the digital ACC system achieves tight current regulation within 0.79%, for any given dimming level and input voltage.

This means that consistent light output is achieved from the LED load for different dimming levels and input voltage conditions. Thus the theoretical current regulation value of <1% is successfully achieved practically.

7.4.2 Practical Load Current Regulation for 1 Connected String/Load

Figure 7.14 shows the load current regulation for 1 connected string/load, as the input voltage is varied from 280 V to 380 V, given a dimming level of 0%, 25% and 50%. From Figure 7.14, the

best current regulation is observed when the input dc voltage varies from 320 V to 340 V. The current regulation value for 0% dimming at the nominal voltage of 340 V is noted as -0.12%. Again, this shows excellent current regulation performance from the digital ACC system.

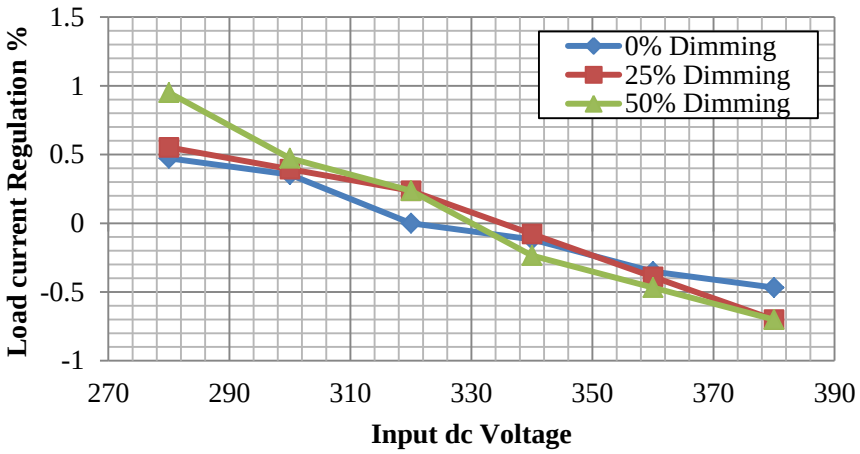


Figure 7.14: Load current regulation of various dimming levels for 1 connected string/load.

The worst current regulation of 0.95% is seen when the input voltage is 280 V, for 50% dimming. Despite this, this value is still within the theoretical current regulation objective of <1%. For the 1 connected string/load, the digital ACC system exhibits excellent performance, as the current regulation is maintained within 0.95% for any given dimming level or input voltage. This in turn ensures consistent light output from the LED string/load for all dimming levels and input voltages.

Finally, the excellent current regulation for 1 connected string/load shows that the LED driver together with the digital ACC system successfully achieves objectives of tight current regulation of <1%.

7.5 CHAPTER CONCLUSION

The SC inductor, isolated cuk converter is applied as an LED driver. The analytical, simulated and practical current and voltage results for various converter components are presented and discussed. The simulated and practical waveforms presented are in good agreement, and show successful converter design. The results are obtained to validate operation of the proposed fault-tolerant LED driver, and also for the novel multiple LED load driver.

The output current ripple obtained when the LED driver is supplying 3 LED strings/loads at 0% dimming and 1 LED string/load at 50% dimming is found practically as 7.05% and 0.94%. These low output current ripple results are attributed to the use of a SC inductor. This suggests the LED load efficacy and optical output is >99% for the entire dimming range; from 0% to 50% and also for connected strings/loads of 1, 2 and 3. Again, the low output current ripple may ensure LED lifetime longevity. Furthermore, the low output ripple value obtained eliminated the need for an output filtering capacitor, and it was not used. This reduces converter component count and reduces cost. Therefore, the high LED efficacy and bulky output capacitor elimination is attributed to the use of the tightly coupled SC inductor.

The analytical and practical efficiencies obtained are found to be in close agreement within a 3.6% margin of error. The practical peak efficiency of 87.2% is obtained when the input voltage is 280 V, for a 0% dimming level and 3 connected strings/loads. Similarly, the practical peak efficiency of 84.1% is obtained for at an input voltage of 280 V, for 1 connected LED string/load at 0% dimming. These efficiencies are reasonably high, and yield a high efficiency LED driver. The dominant loss mechanism noted is the switch loss. If this were to be reduced, the efficiency of the proposed driver can be significantly improved, and this can be part of the future work. Nevertheless, the proposed LED driver using a coupled inductor cuk converter has been seen to achieve a reasonably high efficiency, which is attributed to the use of a SC inductor.

The worst practical load current regulation of 0.95% was obtained when the LED driver was supplying 1 string at 50% dimming level at 280 V input voltage. Despite this, it is still within the <1% load current regulation objective. The load current regulation obtained for 3 connected strings/loads; at 0% dimming at the nominal input voltage of 340 V was found as -0.04%. This value shows excellent performance of the practical digital ACC implemented. It can be concluded that the digital ACC ensures tight current regulation within 0.95%, regardless of the dimming level, input voltage, and the connected strings/loads; this ensures consistent light output from the LED load.

It is finally concluded that the objective of obtaining a highly efficient, compact and low cost LED driver, with dimming capability and has high LED efficacy which may maintain long LED lifetime, has been successfully achieved. This is applicable to both the fault-tolerant driver, and the novel multiple LED load driver.

CHAPTER 8 CONCLUSION AND FUTURE WORK

8.1 CONCLUSION

LED lighting systems are rapidly gaining dominance. High driver efficiency, high LED efficacy and long LED lifetime are important factors that need to be considered. To achieve these requirements, the driver must operate with a current that has a low peak-peak current ripple at all times. This ensures high LED efficacy capability and can possibly contribute to long LED lifetime.

The proposed LED driver employed a coupled inductor cuk converter with AM dimming. This was chosen to satisfy requirements of high driver efficiency, and high LED efficacy. A comprehensive analysis was done to investigate the effects of coupling type and also the coupling coefficient, on the performance of the cuk converter employed as an LED driver. Types of inductor coupling investigated were; symmetrically coupled, non-symmetrically coupled and non-coupled inductors. This was done to identify the best coupling type and coupling coefficient for LED driver applications. Such a comprehensive analysis has not been reported in available literature.

Fault-tolerant LED drivers are needed to ensure continued operation of the lighting system in case of an LED fault. Digital control was used to enhance operation of the LED driver, by detecting an open-circuit LED string; ensuring continued operation of the LED driver under fault conditions. The current sensing of the LED string was done in a lossless manner, so as not to impact the driver efficiency negatively.

A novel LED driver capable of driving several independent LED loads, which can be individually switched on or off without affecting operation of the connected loads was proposed and successfully implemented. Such an LED driver would simplify and drastically reduce costs of existing LED lighting systems

The conclusions of this dissertation are summarised in light of the research questions;

(i) How does the type of coupling, namely non-symmetric coupling and symmetric coupling, and the coupling coefficient, affect the performance of the isolated cuk converter, and which coupling type and coefficient is best for driving LEDs?

A comprehensive analysis of three inductor structures namely; NC, NSC and SC inductors, was done to determine their effects on performance of the cuk converter. The coupling coefficients considered were 0.5 and 0.98 for both the NSC and SC inductors.

The impact of the three inductor structures and the coupling coefficients on driver efficiency, LED load efficacy and inductance size were investigated in detail analytically, and the obtained results were compared. It was found that tightly coupled SC inductors (k=0.98), achieves the best performance in terms of driver efficiency, achieves acceptable performance in terms of LED efficacy and light output, and inductance size.

Practical validation for the three inductor structures was also done, and the experimental results agreed reasonably well with the analytical results. By using SC (k=0.98) inductors, LEDs will then be driven with high efficacy and light output of greater than 99%. This should help guarantee long LED lifetime. The efficiency of the cuk converter is higher by using SC (k=0.98) inductors as compared to the NC and NSC inductors. It is this inductor structure that was therefore chosen to implement the proposed LED driver.

Due to the low output ripple obtained using the SC (k=0.98) inductors, the need for a bulky output filter capacitor is eliminated. The SC inductor thus achieves a compact LED driver with low component count and cost. The objective of identifying the best coupling type and coupling coefficient for the cuk converter applied as an LED driver was therefore achieved successfully.

(ii) How can high power LEDs be driven with low ripple to maintain high efficacy and possibility of long lifetime?

Coupling the input and output inductors of a cuk converter topology used as an LED driver, achieved significant peak-peak current ripple reduction. This ensures that the LEDs were driven with a high efficacy of greater than 99%. The low output peak-peak ripple obtained should help to maintain long LED lifetime. Furthermore, since AM dimming does not introduce any current ripple in the LED load, it helps to maintain high LED efficacy and also possibly prolong LED lifetime.

Therefore, the objective of developing a high efficiency driver that maintains high LED efficacy and possibly help prolong LED lifetime was successfully achieved.

(iii) Can the use of coupled inductors aid in eliminating the use of an output capacitor, and to achieve a compact low cost LED driver?

Using symmetrically coupled inductors for the proposed LED driver achieved a low output peak-peak current ripple that maintained a high LED efficacy. The need for a bulky output capacitor was eliminated, as additional filtering would not improve LED efficacy any further. Therefore, using coupled inductors achieved compact inductance size, reduced LED driver component count, resulting in a highly compact and low cost LED driver. The objective of obtaining a compact LED driver with minimum component count and low cost was thus successfully achieved.

(iv) Is it possible to obtain a fault-tolerant LED driver which detects the LED string currents in a lossless manner?

Lossless LED string current sensing was achieved by using low cost hall-effect switches. They did not affect the efficiency of the LED driver, and were seamlessly integrated with the digital controller. For an LED driver with numerous LED strings, using a lossy current sensing method could drastically reduce the driver efficiency. Therefore, using the low cost hall-effect current sensing for a fault-tolerant driver can aid to ensure high LED driver efficiency, and can also be a cost effective solution.

Using digital control enabled the enhancement of an LED driver by allowing a fault-tolerant feature in a simple and cost effective manner. An open-circuit failure in any of the LED strings was detected by the digital controller, and the current in the remaining connected loads was maintained at the desired level. Therefore, the fault-tolerant feature achieved should help to maintain continued LED driver operation under fault conditions, improving reliability and also reducing running costs and downtime. It is concluded that the objective of obtaining a fault-tolerant LED driver with lossless LED string current detection was successfully achieved.

(v) Is it possible to obtain an LED driver that can drive multiple low power LED loads, of which each load can be individually switched on and off without affecting operation of the connected loads?

A single novel LED driver capable of driving several independent LED loads was implemented successfully using digital control. Current in each LED load was sensed in a lossless manner, and a digital controller was used to maintain the desired current in the connected loads, regardless of whether some loads were turned off and then on again. This novel concept can simplify and reduce costs of already existing LED lighting systems, where a driver is required for each LED load. Finally, the objective of obtaining a multiple load LED driver was achieved with success.

8.2 FUTURE WORK

The future work to develop the proposed LED driver further is summarised as follows;

(i) Incorporation of remote dimming and monitoring capabilities

For the LED driver used for applications such as street lighting, the remote dimming feature from a central control unit would enable energy saving when the full light output is not required. Monitoring capabilities can enable detection of fault location in the grid system, and could be effectively used for smart grid applications.

(ii) Qualitative analysis of the Non-symmetric and Symmetric coupling types on the converter transfer functions

A qualitative analysis to investigate the effect of the coupling coefficient and the type of coupling on the coupling coefficient, for the proposed LED driver, needs to be done. This would give insight into control performance parameters such as transient response and converter bandwidth depending on coupling type and coupling coefficient.

(iii) LED driver with power factor correction and soft switching

The proposed LED driver can be incorporated with a suitable power factor correcting control scheme so that it may operate with a high input power factor, directly from the mains. This is to satisfy the lighting equipment standards requirements. Soft switching can be implemented to improve efficiency of the proposed LED driver, as the switching loss is the dominant loss mechanism.

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APPENDIX A COUPLED INDUCTOR CUK CONVERTER TRANSFER FUNCTIONS

A.1 THE CONTROL-TO-OUTPUT VOLTAGE TRANSFER-FUNCTION

By applying the state space approach described in Section 3.5, the control-to-output voltage transfer-function is given by Equation (A.1), with the coefficients given by Equations (A.2-A.13);

$$G_{v_o\delta}(s) = \frac{V_{IN}\left(a_1 s^4 + a_2 s^3 + a_3 s^2 + a_4 s + a_5\right)}{b_1 s^6 + b_2 s^5 + b_3 s^4 + b_4 s^3 + b_5 s^2 + b_6 s + b_7} \tag{A.1}$$

$$a_1 = \left(L_1{}^2 L_m RC_a C_b + L_1 L_m MRC_a C_b\right)(1-D) \tag{A.2}$$

$$\begin{aligned} a_2 = {} & L_m M^2 C_a + L_m M^2 C_b (-1-D)^2 - L_1{}^2 L_m C_a + L_1{}^2 L_m C_b D^2 \\ & - \left(L_1 L_m MC_a + L_1 L_m MC_b\right)\left(2D(1-D)\right) \end{aligned} \tag{A.3}$$

$$a_3 = \left(L_1{}^2 RC_a + L_1 L_m RC_a + L_1 L_m RC_b\right)(1-D)^2 - L_1 MRC_b\left(D(1-D)\right) \tag{A.4}$$

$$a_4 = -L_1{}^2 D^2 - \left(M^2 + L_1 M\right)(1-D)^2 \tag{A.5}$$

$$a_5 = L_1 R(1-D)^2 \tag{A.6}$$

$$b_1 = \left(L_2 L_m RC_2 C_a C_b L_1{}^2 - L_m RC_2 C_a C_b L_1 M^2\right)(1-D)^2 \tag{A.7}$$

$$b_2 = \left(L_2 L_m C_a C_b L_1{}^2 - L_m C_a C_b L_1 M^2\right)(1-D)^2 \tag{A.8}$$

$$\begin{aligned} b_3 = {} & L_1{}^2 L_2 RC_2 C_a - L_1 M^2 RC_2 C_a (1-D)^4 + L_1{}^2 L_m RC_a C_b (1-D)^2 \\ & + \left(L_1{}^2 L_2 RC_2 C_b + L_1{}^2 L_m RC_2 C_a + L_1{}^2 L_m RC_2 C_b - L_1 M^2 RC_2 C_b\right)\left(D^2 (1\text{-}D)^2\right) \\ & + \left(L_1 L_2 L_m RC_2 C_a + L_1 L_2 L_m RC_2 C_b\right)(1-D)^2 \\ & + \left(L_1 L_m MRC_2 C_a + L_1 L_m MRC_2 C_b\right)\left(2D(1-D)^3\right) \end{aligned} \tag{A.9}$$

$$\begin{aligned} b_4 = {} & \left(L_1{}^2 L_2 C_a - L_1 M^2 C_a + L_1 L_2 L_m C_b + L_1 L_2 L_m C_a\right)(1-D)^4 \\ & + \left(L_1{}^2 L_2 C_b + L_1{}^2 L_m C_a + L_1{}^2 L_m C_b - L_1 M^2 C_b\right)\left(D^2 (1-D)^2\right) \\ & + \left(L_1 L_m MC_a + L_1 L_m MC_b\right)\left(2D(1-D)^3\right) \end{aligned} \tag{A.10}$$

$$\begin{aligned} b_5 = {} & \left(L_1{}^2 RC_a + L_1 L_2 RC_2 + L_1 L_m RC_a + L_1 L_m RC_b\right)(1-D)^4 \\ & + \left(L_1{}^2 RC_2 + L_1{}^2 RC_b\right)\left(D^2 (1-D)^2\right) + L_1 MRC_2\left(2D(1-D)^3\right) \end{aligned} \tag{A.11}$$

$$b_6 = L_1{}^2 D^2 (1-D)^2 + L_1 L_2 (1-D)^4 + L_1 M 2D(1-D)^3 \tag{A.12}$$

$$b_7 = L_1 R(1-D)^4 \tag{A.13}$$

A.2 THE CONTROL-TO-OUTPUT INDUCTOR CURRENT TRANSFER-FUNCTION

The control-to-output inductor current transfer-function is given by Equation (A.14), with the coefficients given by Equations (A.15-A.27);

$$G_{iL_2\delta}(s) = \frac{V_{IN}\left(g_1 s^5 + g_2 s^4 + g_3 s^3 + g_4 s^2 + g_5 s + g_6\right)}{h_1 s^6 + h_2 s^5 + h_3 s^4 + h_4 s^3 + h_5 s^2 + h_6 s + h_7} \tag{A.14}$$

$$g_1 = \left(L_1^{\,2} L_m R^2 C_2 C_a C_b - L_1 L_m M R^2 C_2 C_a C_b\right)(1-D) \tag{A.15}$$

$$\begin{aligned} g_2 = {} & \left(L_1^{\,2} L_m R C_a C_b - L_1 L_m M R C_a C_b\right)(1-D) - \left(L_m M^2 R C_2 C_a + L_m M^2 R C_2 C_b\right)(1-D)^2 \\ & - \left(L_1^{\,2} L_m R C_2 C_b - L_1^{\,2} L_m R C_2 C_a\right) D^2 - \left(L_1 L_m M R C_2 C_b + L_1 L_m M R C_2 C_a\right)(2D(1\text{-}D)) \end{aligned} \tag{A.16}$$

$$\begin{aligned} g_3 = {} & \left(L_1 L_m R^2 C_2 C_b + L_1^{\,2} R^2 C_2 C_a + L_1 L_m R^2 C_2 C_a - L_m M^2 C_a - L_m M^2 C_b\right)(1-D)^2 \\ & - \left(L_1^{\,2} L_m C_a + L_1^{\,2} L_m C_b\right) D^2 - \left(L_1 L_m M C_a + L_1 L_m M C_b\right)(2D(1-D)) \\ & - L_1 M R^2 C_2 C_b D(1-D) \end{aligned} \tag{A.17}$$

$$\begin{aligned} g_4 = {} & \left(L_1^{\,2} R C_a - M^2 R C_2 + L_1 L_m R C_a + L_1 L_m R C_b\right)(1-D)^2 \\ & - \left(L_1^{\,2} R C_2\, D^2 + L_1 M R C_2\right)(2D(1-D)) - L_1 M R C_b D(1-D) \end{aligned} \tag{A.18}$$

$$g_5 = \left(C_2\, L_1 R^2 - M^2\right)(1-D)^2 - L_1^{\,2} D^2 - L_1 M\, 2D(1\text{-}D) \tag{A.19}$$

$$g_6 = L_1 R (1-D)^2 \tag{A.20}$$

$$h_1 = \left(L_2 L_m C_2 C_a C_b L_1^{\,2} R^2 - L_m C_2 C_a C_b L_1 M^2 R^2\right)(1-D)^2 \tag{A.21}$$

$$h_2 = \left(L_2 L_m R C_a C_b L_1^{\,2} - L_m R C_a C_b L_1 M^2\right)(1-D)^2 \tag{A.22}$$

$$\begin{aligned} h_3 = {} & \left(L_1^{\,2} L_2 R^2 C_2 C_a + L_1 L_2 L_m R^2 C_2 C_a - L_1 M^2 R_2 C_2 C_a + L_1 L_2 L_m R^2 C_2 C_b\right)(1-D)^4 \\ & + L_1^{\,2} L_m R^2 C_a C_b (1-D)^2 + \begin{pmatrix} L_1^{\,2} L_2 R^2 C_2 C_b + L_1^{\,2} L_m R^2 C_2 C_a \\ - L_1 M^2 R^2 C_2 C_b + L_1^{\,2} L_m R^2 C_2 C_b \end{pmatrix}\left(D^2 (1-D)^2\right) \\ & + \left(L_1 L_m M R^2 C_2 C_a + L_1 L_m M R^2 C_2 C_b\right)\left(2D(1-D)^3\right) \end{aligned} \tag{A.23}$$

$$\begin{aligned} h_4 = {} & \left(L_1^{\,2} L_2 R C_a - L_1 M^2 R C_a + L_1 L_2 L_m R C_b + L_1 L_2 L_m R C_a\right)(1-D)^4 \\ & + \left(L_1^{\,2} L_2 R C_b + L_1^{\,2} L_m R C_a + L_1^{\,2} L_m R C_b - L_1 M^2 R C_b\right)\left(D^2 (1-D)^2\right) \\ & + \left(L_1 L_m M R C_a + L_1 L_m M R C_b\right)\left(2D(1-D)^3\right) \end{aligned} \tag{A.24}$$

$$\begin{aligned} h_5 = {} & \left(L_1^{\,2} R^2 C_a + L_1 L_2 R^2 C_2 + L_1 L_m R^2 C_a + L_1 L_m R^2 C_b\right)(1-D)^4 \\ & + \left(L_1^{\,2} R^2 C_2 + L_1^{\,2} R^2 C_b\right)\left(D^2 (1-D)^2\right) + L_1 M R^2 C_2\, 2D(1-D)^3 \end{aligned} \tag{A.25}$$

$$h_6 = + L_1 L_2 R (1-D)^4 + L_1^{\,2} R \left(D^2 (1-D)^2\right) + L_1 M R 2D(1-D)^3 \tag{A.26}$$

$$h_7 = + L_1 R^2 (1-D)^4 \tag{A.27}$$

APPENDIX B PRACTICAL LED DRIVER PCB DESIGNS

B.1 THE GATE DRIVE PCB

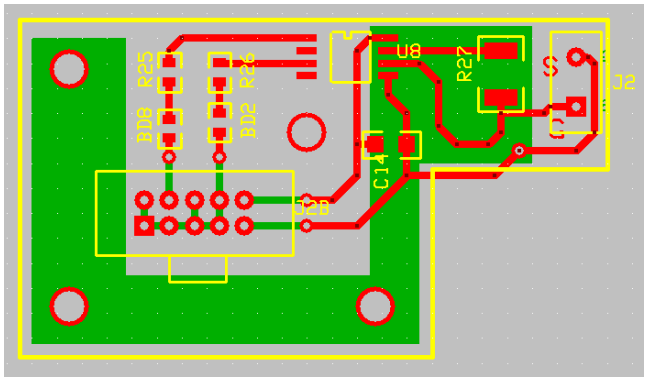
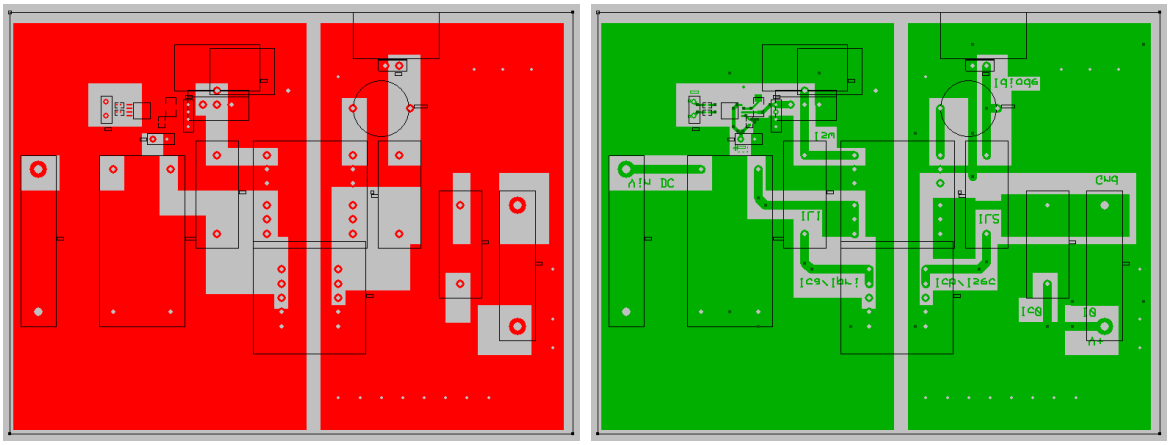


Figure B.1: The gate drive PCB design

B.2 THE MAIN LED DRIVER PCB



(a) Top PCB layer (b) Bottom PCB layer

Figure B.2: The main LED driver PCB design

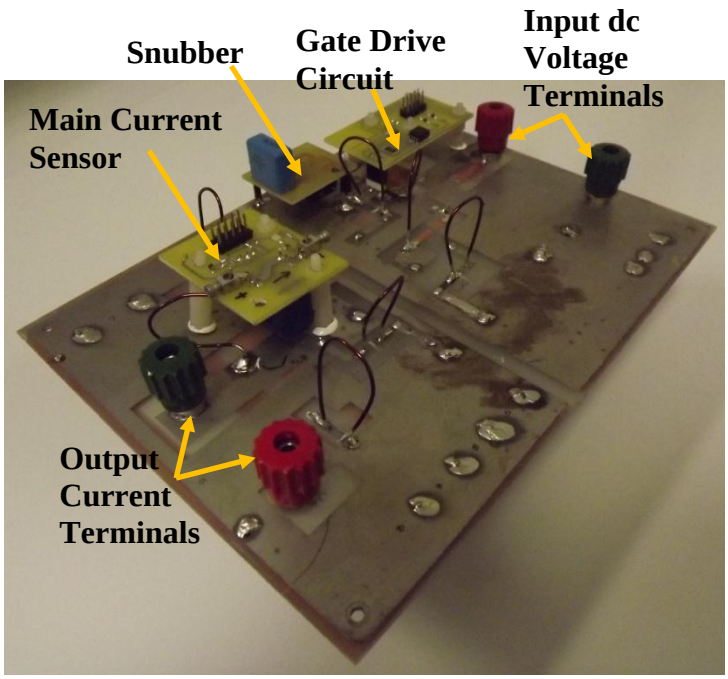


Figure B.3: The LED driver and associated circuitry

B.3 THE DSP TO LED DRIVER SIGNAL CONDITIONING PCB

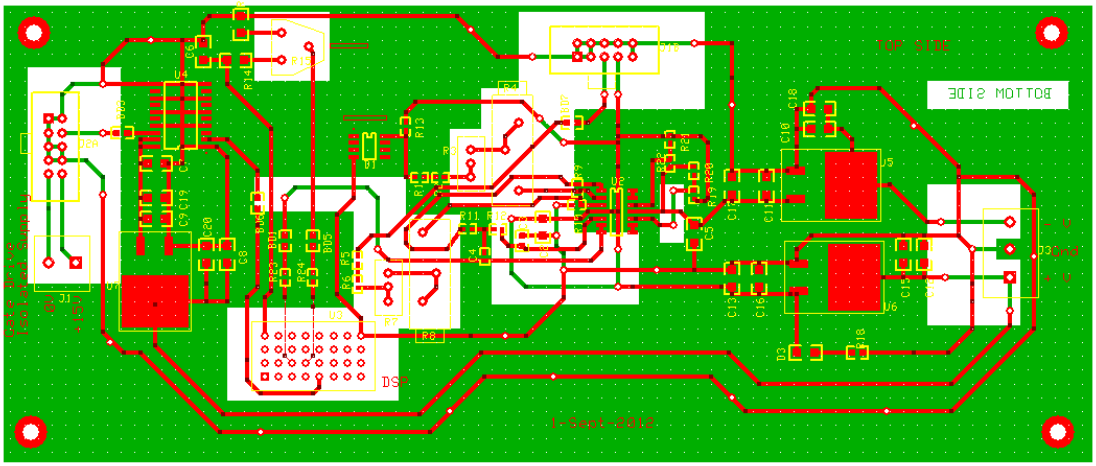


Figure B.4: The main signal conditioning PCB design

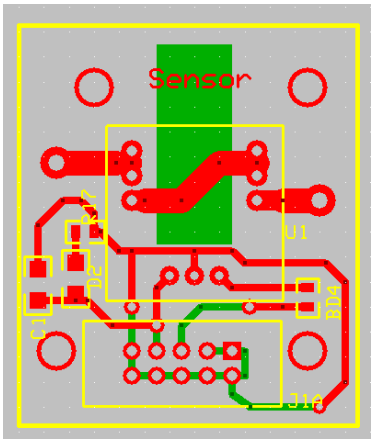


Figure B.5: The main current sensor PCB design

B.4 THE LED LOAD PCB TO SIGNAL CONDITIONING PCB

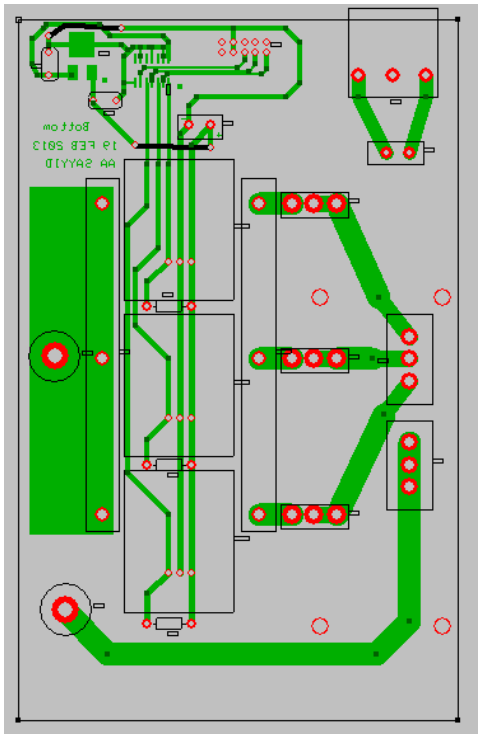


Figure B.6: The LED lossless sensor PCB design

APPENDIX C THE DSP CONTROL CODE

C.1 THE DSP CONTROL C-CODE

The control code in C for the DSP is given in this Section.

```
//         FILE:   Cuk LED driver Control-Main.C
//         Description:     This is the Main C-Code for the Control
//                          of a fault-tolerant LED driver and a
//                          Multiple LED Load driver. The target is
//                          the TMS320F28027 DSP

#include "ProjectName-Settings.h"
#include "PeripheralHeaderIncludes.h"
#include "DSP2802x_EPWM_defines.h"
#include "DPlib.h"
#include "IQmathLib.h"

// Declare Constants
//Dimming Level Required
_iq24 FACT=4753545;//0% DIMMING= 4753545 ; 25% DIMMING =3565158;    50% DIMMING=2376772;
_iq24 SCONN;
// Function Prototypes used
void DeviceInit(void);
#ifdef FLASH
        void InitFlash();
#endif
void MemCopy();

// Digital Power Library Modules
void ADC_SOC_CNF(int ChSel[], int Trigsel[], int ACQPS[], int IntChSel, int mode);
void PWM_1ch_CNF(int16 n, int16 period, int16 mode, int16 phase);
// ConFigure the ADC
int     ChSel[16] =   {0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0};
```

```
int             TrigSel[16] = {0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0};
int    ACQPS[16] =   {7,7,7,7,7,7,7,7,7,7,7,7,7,7,7,7};
// ------ Digital Power Library Net Pointers ------------------------
// The net pointers used for the digital power Library are declared here
//ADC 1 channel
extern volatile long *ADCDRV_1ch_Rlt0;   //instance #0, ADC
// 3P3Z Controller
extern volatile long *CNTL_3P3Z_Ref1;    //instance #1,3P3Z Controller
extern volatile long *CNTL_3P3Z_Out1;
extern volatile long *CNTL_3P3Z_Fdbk1;
extern volatile long *CNTL_3P3Z_Coef1;
// PWM Driver 1 channel
extern volatile long *PWMDRV_1ch_Duty1;          // instance #1, EPWM1
// The digital power Library Variables are declared here
volatile long Filter_Out , Adc_Out, Ref_Value;
#pragma DATA_SECTION(CNTL_3P3Z_CoefStruct1, "CNTL_3P3Z_Coef");
struct CNTL_3P3Z_CoefStruct CNTL_3P3Z_CoefStruct1;

//%%%%%%%%%% Main Control Code %%%%%%%%%%%%%%%%%%
void main(void)
{ DeviceInit();  // Intitialize Device
#ifdef FLASH
        MemCopy(&RamfuncsLoadStart, &RamfuncsLoadEnd, &RamfuncsRunStart);
        InitFlash();       // Initialize Flash
#endif
        // ConFigure PWM Module
        PWM_1ch_CNF(1, 300, 1, 0); // 200 kHz
        //  ADC  trigger from EPWM1 Period event Configuration
        ChSel[0]=14;              //Map channel 0 to pin ADC-B6
        //  Trigger Event Selection for ADC
        TrigSel[0]= ADCTRIG_EPWM1_SOCA;
        //  ADC conFigured with auto interrupt clear mode
        // ADC interrupt after End of Conversion of channel 0
        ADC_SOC_CNF(ChSel,TrigSel,ACQPS,0,2);
```

```
        // ConFigure the EPWM1 to start the Start of Conversion
        EPwm1Regs.ETSEL.bit.SOCAEN        = 1;
        EPwm1Regs.ETSEL.bit.SOCASEL = ET_CTR_PRD;
        // PRD event trigger for ADC SOC
   EPwm1Regs.ETPS.bit.SOCAPRD     = ET_1ST;
   // pulse Generation on every event
        // Initialise Digital Power library
        DPL_Init();
        // Library Module connection to NETS
        //---------------------------------------
        // ADC Output Connection to the Net Variable
        ADCDRV_1ch_Rlt0  = &Adc_Out;
        // Connect the CNTL_3P3Z block to the variables
        CNTL_3P2Z_Fdbk1 = &Adc_Out;
        CNTL_3P2Z_Out1 = &Filter_Out;
        CNTL_3P2Z_Ref1 = &Ref_Value;
        CNTL_3P2Z_Coef1 = &CNTL_3P3Z_CoefStruct1.b2;
        // Connect the PWM Driver input to the output of the 3P3Z controller
        PWMDRV_1ch_Duty1 = &Filter_Out;
        // Initialize the Controller Coefficients
        CNTL_3P2Z_CoefStruct1.b3 = _IQ26(0.000000580684140);
        CNTL_3P2Z_CoefStruct1.b2 = _IQ26(0.000000526441459);
        CNTL_3P2Z_CoefStruct1.b1 = _IQ26(0.000000689223230);
        CNTL_3P2Z_CoefStruct1.b0 = _IQ26(0.000000634953680);
        CNTL_3P2Z_CoefStruct1.a3 = _IQ26(-0.98579292);
        CNTL_3P2Z_CoefStruct1.a2 = _IQ26(2.9715349);
        CNTL_3P2Z_CoefStruct1.a1 = _IQ26(2.9857419);
        CNTL_3P2Z_CoefStruct1.max =_IQ24(0.5);
        CNTL_3P2Z_CoefStruct1.min =_IQ24(0.0);
// ConFigure the Interrupts
        EALLOW;
   PieVectTable.EPWM1_INT = &DPL_ISR;              // Map Interrupt
        PieCtrlRegs.PIEIER3.bit.INTx1 = 1;      // PIE level enable, Grp3 / Int1
        EPwm1Regs.ETSEL.bit.INTSEL = ET_CTR_PRD;       // INT on PRD event
```

```
        EPwm1Regs.ETSEL.bit.INTEN = 1;            // Enable INT
   EPwm1Regs.ETPS.bit.INTPRD = ET_1ST;       // Generate INT at every event

   IER |= M_INT3;                        // CPU INT3 connected to EPWM1-6 INTs:
   EINT;                          // Enable interrupt
   ERTM;                          // Enable interrupt
        EDIS;
        for(;;)  //infinite loop
        {  // Identify Open or Closed LED Strings/Loads
        //Compute the Number of connected Strings/Loads
SCONN=_IQ24(1+GpioDataRegs.GPADAT.bit.GPIO3+GpioDataRegs.GPADAT.bit.GPIO2);
                //Compute the Reference value
                Ref_Value = _IQmpy(FACT,SCONN); }
} //End of Main Control Code
```