Linearity Improvement Analysis for PAs at mm-Wave Frequencies

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***Abstract*—This article presents an adaptive predistortion (APD) linearization technique to improve the linearity of mm-wave power amplifiers (PAs) specifically at 60 GHz. The PA and the APD were designed using the 0.13 μm SiGe BiCMOS process. The predistortion is applied to the PA by varying the gain of the PA through its variable gain amplifier. The PA achieves a P_{SAT} of 11.97 dBm and $IP_{1\,dB}$ of -10 dBm. After linearization the PA has an improved $IP_{1\,dB}$ of -6 dBm. This linearization technique results in an optimum IMD3 reduction of 10 dB.**

Key words — Linearization, predistortion, 60 GHz, SiGe HBT power amplifier, intermodulation distortion 3rd component (IMD3).

1. INTRODUCTION

The 3 GHz unlicensed bandwidth allocation at 60 GHz has made this mm-wave spectrum lucrative for fast gigabit applications. Therefore high bandwidth and spectral efficient modulation schemes such as orthogonal frequency division multiplexing (OFDM) have been considered as the modulation scheme for communication systems in the mm-wave frequency band [1]. OFDM is sensitive especially to non-linearities in the transmitter. The power amplifier (PA) is located in the transmitter and must amplify the input signal and deliver high output linear power while being efficient, but its performance is severely affected by the scaled semiconductor technology and the operating frequency. For this reason the PA is one of the most challenging functional blocks in the transmitter at 60 GHz [2]. Therefore, in order to achieve good linearity with sufficient efficiency, some type of linearization technique has to be implemented [3]. Among the various linearization techniques that are available, predistortion is the most attractive and promising one in mm-wave frequencies because of the advantages of small size, low

complexity and low cost. The predistortion technique generates the inverse characteristic function of the PA to extend the linear output power region [4]. Existing predistortion linearizers mostly consist of diode linearizers [5-6] to minimise the IMD3 components. Another predistortion method that has been implemented at 60 GHz to realise the predistortion characteristic is using the cold metal-oxide-semiconductor field effect transistor as the linearizer [4].

2. INTERMODULATION DISTORTION ANALYSIS

To understand the behaviour of the non-linear components, Volterra series analysis is performed on the small-signal common emitter (CE) heterojunction bipolar transistor (HBT) model shown in Figure 1. The main contributors of non-linearity, as shown in Figure 1, are the diffusion capacitance C_{diff}, the collector current I_C and the base current I_B [7]. I_C and I_B are both functions of the non-linear v_π. C_{diff} is assumed to be linear with I_C. It is assumed that the base-collector capacitance C_{BC} and the base-emitter depletion capacitance C_j are linear.

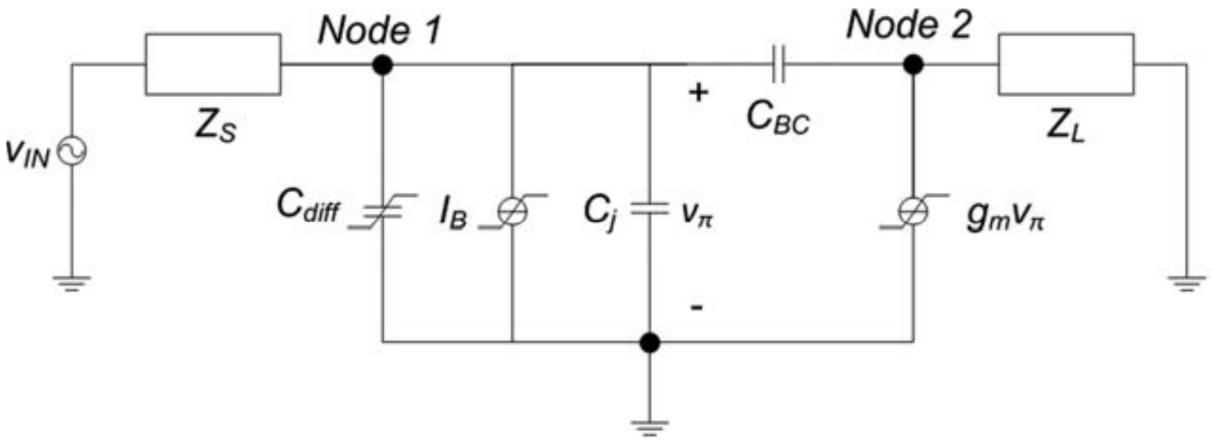

Figure 1 Small-signal HBT model with non-linear components

The collector current is given by (1):

$$I_C = I_Q e^{\frac{v_\pi}{V_T}} \tag{1}$$

Using the Taylor series expansion, (1) can be represented in (2):

$$I_C = I_Q[\frac{v_\pi}{V_T} + \frac{1}{2}\left(\frac{v_\pi}{V_T}\right)^2 + \frac{1}{6}\left(\frac{v_\pi}{V_T}\right)^3 + \cdots]. \tag{2}$$

The Taylor coefficients are defined in (3) to (5):

$$g_{m1} = \frac{I_C}{V_T} \tag{3}$$

$$g_{\pi 1} = \frac{g_{m1}}{\beta_f} \tag{4}$$

$$C_{diff1} = \tau_F g_{m1} \tag{5}$$

where $\beta_f = \frac{I_C}{I_B}, \tau_F = \frac{Q_{diff}}{I_C}$ and Q_{diff} is the diffusion charge.

The non-linearity components can therefore be written in (6) to (8):

$$i_c(t) = g_{m1} v_\pi(t) + g_{m2} {v_\pi}^2(t) + g_{m3} {v_\pi}^3(t) \tag{6}$$

$$i_b(t) = g_{\pi 1} v_\pi(t) + g_{\pi 2} {v_\pi}^2(t) + g_{\pi 3} {v_\pi}^3(t) \tag{7}$$

$$q_{diff}(t) = C_{diff1} v_\pi(t) + C_{diff2} {v_\pi}^2(t) + C_{diff3} {v_\pi}^3(t). \tag{8}$$

Following Kirchhoff's current law in Figure 1 and converting the impedances to admittances produce the following matrix (9) [8]:

$$\begin{bmatrix} Y_S(s) + g_{\pi 1} + s(C_{diff1} + C_j + C_{BC}) & -sC_{BC} \\ g_{m1} - sC_{BC} & Y_L(s) + sC_{BC} \end{bmatrix} \begin{bmatrix} V_{11}(s) \\ V_{12}(s) \end{bmatrix} = \begin{bmatrix} Y_S(s) V_{IN}(s) \\ 0 \end{bmatrix} \tag{9}$$

where $V_{11}(s)$ and $V_{12}(s)$ refer to the first order Volterra kernel voltages at nodes 1 and 2 respectively. With $V_{IN}(s) = 1$, and using Cramer's rule to solve the above matrix, $V_{12}(s)$ can be obtained in (10):

$$V_{12}(s) = \frac{-Y_S(s)[g_{m1} - sC_{BC}]}{\det(Y(s))} \tag{10}$$

where $\det(Y(s)) = (Y_L(s) + sC_{BC})[Y_S(s) + g_{\pi 1} + s(C_{diff1} + C_j + C_{BC})] + sC_{BC}(g_{m1} - sC_{BC})$ and $s = j\omega$.

The second and third order Volterra kernels are obtained by placing the second and third order non-linear current and capacitors in parallel to the linear current sources and capacitor respectively and the input voltage is shorted. The second order non-linear components are defined in (11) to (13):

$$i_{c2} = g_{m2}V_{11}(s_1)V_{11}(s_2) \tag{11}$$

$$i_{b2} = g_{\pi 2}V_{11}(s_1)V_{11}(s_2) \tag{12}$$

$$i_{diff2} = C_{diff2}V_{11}(s_1)V_{11}(s_2)(s_1 + s_2). \tag{13}$$

The second order Volterra kernels are then obtained using Cramer's rule and are shown in (14) to (15):

$$V_{21}(s_1, s_2) = \frac{-(Y_L(s_1 + s_2) + (s_1 + s_2)C_{BC})(i_{b2} + i_{diff2}) - (s_1 + s_2)C_{BC}i_{c2}}{\det(Y(s_1 + s_2))} \tag{14}$$

$$V_{22}(s_1, s_2) = \frac{-(Y_S(s_1 + s_2) + g_{\pi 1} + (s_1 + s_2)(C_{diff1} + C_j + C_{BC}))i_{c2} + (g_{m1} - (s_1 + s_2)C_{BC})(i_{b2} + i_{diff2})}{\det(Y(s_1 + s_2))}. \tag{15}$$

The third order non-linear components are shown in (16) to (18):

$$i_{c3} = g_{m3}V_{11}(s_1)V_{11}(s_2)V_{11}(s_3) + 2g_{m2}\overline{V_{11}V_{21}} \tag{16}$$

$$i_{b3} = g_{\pi 3}V_{11}(s_1)V_{11}(s_2)V_{11}(s_3) + 2g_{\pi 2}\overline{V_{11}V_{21}} \tag{17}$$

$$i_{diff3} = (C_{diff3}V_{11}(s_1)V_{11}(s_2)V_{11}(s_3) + 2C_{diff2}\overline{V_{11}V_{21}})(s_1 + s_2 + s_3) \tag{18}$$

where $\overline{V_{11}V_{21}} = \frac{V_{11}(s_1)V_{21}(s_2,s_3)+V_{11}(s_2)V_{21}(s_1,s_3)+V_{11}(s_3)V_{21}(s_1,s_2)}{3}$.

The third order Volterra kernel is shown in (19):

$$V_{32}(s_1,s_2,s_3) = \frac{-(Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j+C_{BC}))i_{c3}+(1-\frac{(s_1+s_2+s_3)C_{BC}}{g_{m1}})(i_{b3}+i_{diff3})(g_{m1})}{\det(Y(s_1+s_2+s_3))} \tag{19}$$

where $\det\big(Y(s_1 + s_2 + s_3)\big) = [Y_S(s_1 + s_2 + s_3) + g_{\pi 1} + (s_1 + s_2 + s_3)\big(C_{diff1} + C_j + C_{BC}\big)](Y_L(s_1 + s_2 + s_3) + (s_1 + s_2 + s_3)C_{BC}) + (s_1 + s_2 + s_3)C_{BC}(g_{m1} - (s_1 + s_2 + s_3)C_{BC})$.

The intermodulation distortion ratio is given by (20):

$$IMD3 = \frac{3}{4}{V_{IN}}^2\left|\frac{V_{32}(s_1,s_2,s_3)}{V_{12}(s_1)}\right| \tag{20}$$

$$= \frac{3}{4}{V_{IN}}^2\left|\frac{-(Y_S(s_1 + s_2 + s_3) + g_{\pi 1} + (s_1 + s_2 + s_3)(C_{diff1} + C_j + C_{BC}))i_{c3} + (1 - \frac{(s_1+s_2+s_3)C_{BC}}{g_{m1}})(i_{b3} + i_{diff3})(g_{m1})}{[Y_S(s_1 + s_2 + s_3) + g_{\pi 1} + (s_1 + s_2 + s_3)(C_{diff1} + C_j + C_{BC})](Y_L(s_1 + s_2 + s_3) + (s_1 + s_2 + s_3)C_{BC}) + (s_1 + s_2 + s_3)C_{BC}(g_{m1} - (s_1 + s_2 + s_3)C_{BC})}\right.$$

$$\left.\times\frac{(Y_L(s_1) + s_1C_{BC})[Y_S(s_1) + g_{\pi 1} + s_1(C_{diff1} + C_j + C_{BC})] + s_1C_{BC}(g_{m1} - s_1C_{BC})}{-Y_S(s_1)[g_{m1} - s_1C_{BC}]}\right|$$

where $s_1 = s_2 = j\omega_1$ and $s_3 = -j\omega_2$.

By letting $C_{BC} = 0$ [8-9], (20) can be simplified to (21):

$$IMD3 = \frac{3}{4}{V_{IN}}^2 \left| \frac{\left(\frac{(Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j))i_{c3}}{g_{m1}} - (i_{b3}+i_{diff3})\right)}{[Y_S(s_1+s_2+s_3)+g_{\pi 1}+(s_1+s_2+s_3)(C_{diff1}+C_j)](Y_L(s_1+s_2+s_3))} \times \frac{Y_L(s_1)[Y_S(s_1)+g_{\pi 1}+s_1(C_{diff1}+C_j)]}{Y_S(s_1)} \right|. \quad (21)$$

As shown in (3) and (21), increasing the biasing current and the gain will reduce the IMD3 component and improve linearity [7, 9]. The point at which the IMD3 component equals the fundamental component known as the input third order intercept point IIP_3 is shown in Figure 2. A transistor size of 0.12 μm × 16 μm was used to simulate the IIP_3. As shown in Figure 2, the linearity increases sharply for small biasing currents and is then followed by a gradual increase in the linearity as the biasing current increases. The IIP_3 begins to taper off for biasing currents > 23 mA.

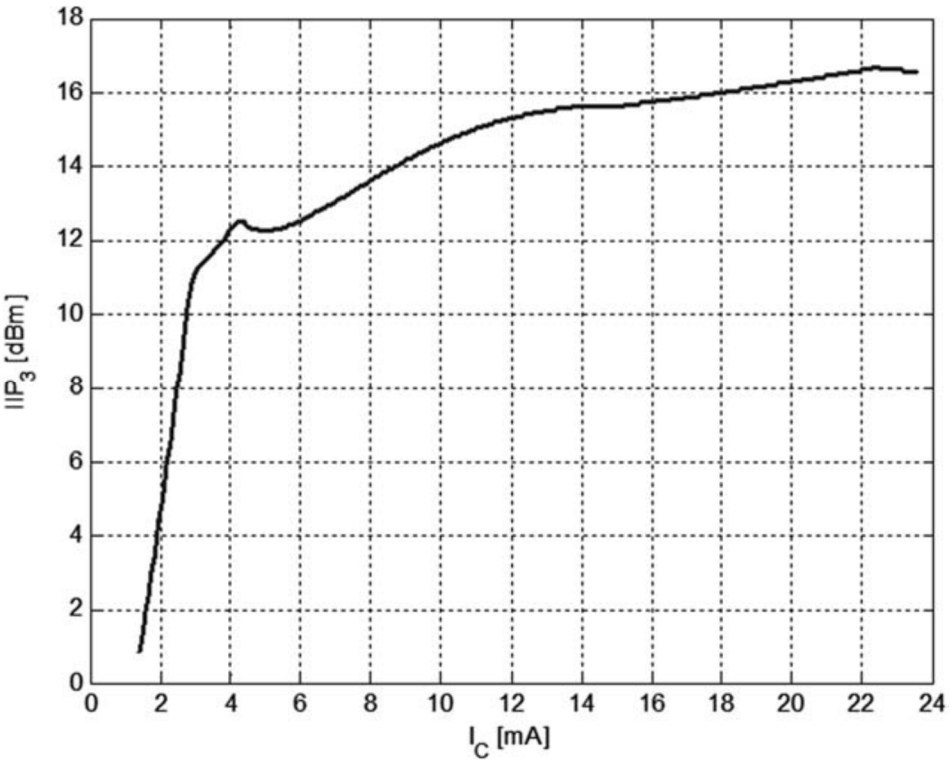

Figure 2 IIP_3 for a CE SiGe HBT

In terms of the large signal analysis the output power of the PA is defined using (22):

$$P_{OUT}[dBm] = G[dB] + P_{IN}[dBm]. \quad (22)$$

However, all PAs suffer from the non-linear effect of saturation where the gain begins to decrease with increasing input power. The variable gain amplifier (VGA) is therefore used to realise the predistortion function by providing an increasing gain at certain measured power output levels and therefore ensuring a constant overall gain such that the output power remains linear until the saturation limit has been reached, at which point no further linearity improvement can be achieved.

3. CIRCUIT DESIGN

The circuit designed to improve the linearity of the PA at 60 GHz is shown in Figure 3. To achieve this, the following subsystems were required: VGA, PA, power detector, analog-to-digital converter (ADC), decision-making circuitry, digital-to-analog converter (DAC). A feedback path from the DAC to the VGA made this predistortion design adaptable.

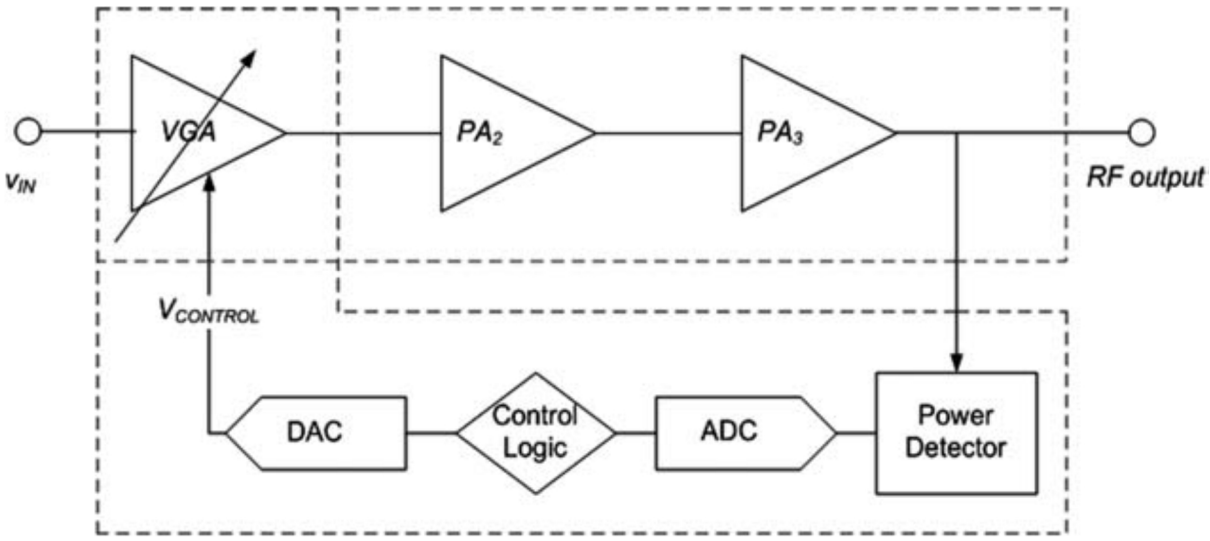

Figure 3 Adaptive predistortion and PA circuit

The PA and the adaptive predistortion circuits were designed using the IBM process design kit (PDK). Both CMOS and SiGe HBT were used in the design of the complete system. This was

made possible because of the BiCMOS technology that is supported by the IBM PDK, therefore allowing the integration of CMOS and SiGe. A photograph of the chip is shown in Figure 4.

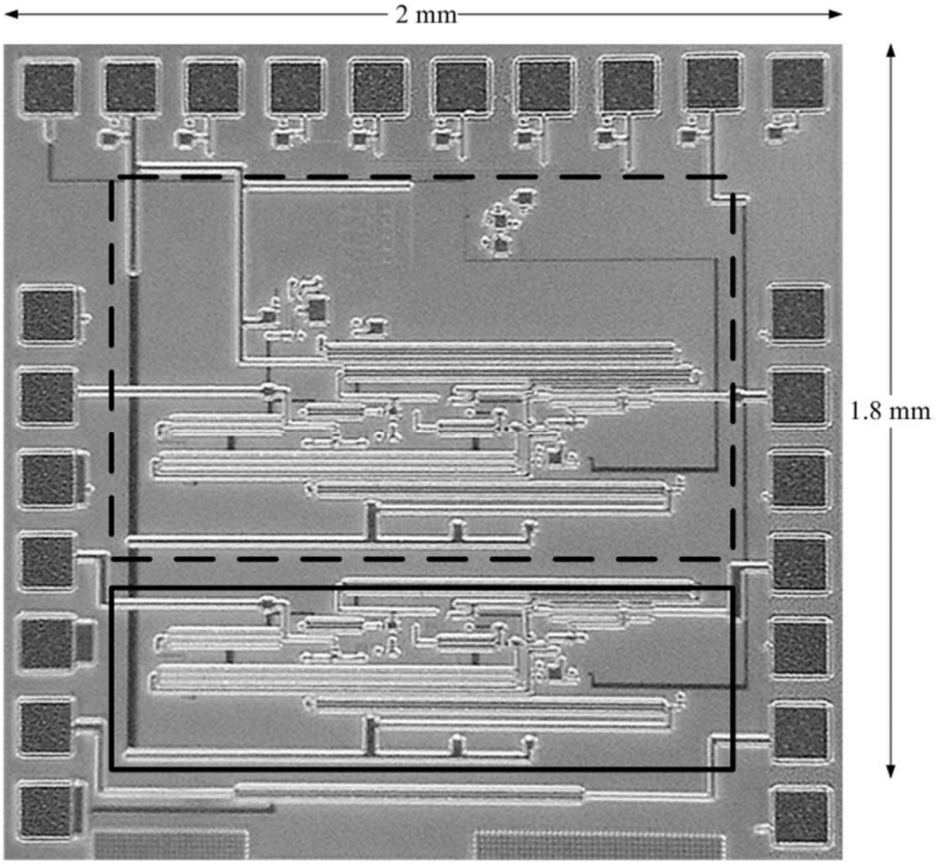

Figure 4 Photograph of the complete chip

The complete chip in Figure 4 consists of the non-linearized PA in the black rectangle and linearised PA with its subsystems in the patterned rectangle. The entire chip occupies an area of 2 mm × 1.8 mm.

A three-stage, single-ended CE configuration was used for the PA. The PA is designed to operate within the Class AB region. Therefore high performance SiGe HBTs with f_T > 200 GHz and an emitter width of 0.12 μm were used as power transistors. A major drawback due to the

scaling of the SiGe HBT is the reduced breakdown voltage, which is caused by impact ionization. However, this breakdown voltage can be overcome by using a 300 Ω at the base of the transistor, resulting in the breakdown voltage shifting from 1.7V to 4 V [10]. The last stage of the PA was designed for maximum output power and the first stage was designed to operate as a VGA. The VGA is controlled by the bias voltage supplied by the DAC, as shown in Figure 5.

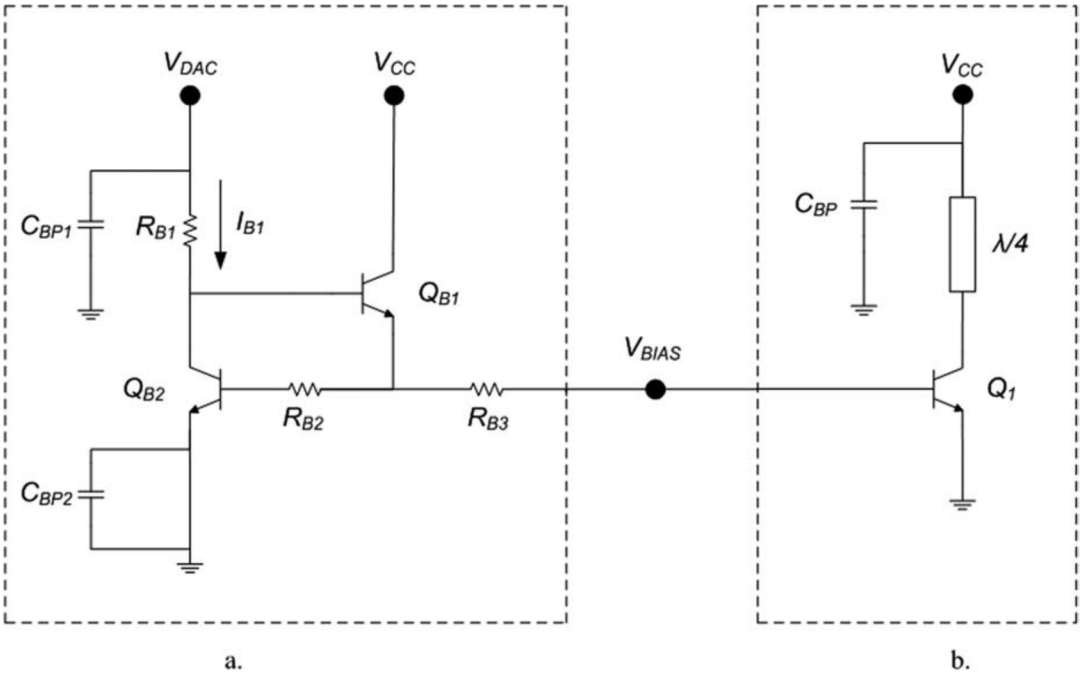

Figure 5 (a) Biasing circuit for the VGA and (b) VGA schematic

The minimum and maximum bias current for the VGA is 16 mA and 22 mA respectively to provide sufficient gain variation to realize the predistortion function and to ensure that the PA operates within the Class AB mode. By-pass capacitors are used extensively in the bias circuits to provide AC grounding. The complete three-stage PA is unconditionally stable.

As shown in Figure 3, the power detector measures the output power and filters it through a low pass filter. The detected power, V_{PDET}, is then applied to the control logic circuit using the

on-chip ADC. The control logic as defined in Table 1 then outputs a control command and the desired voltage is outputted by the DAC.

Table 1 Operation of the Control Logic and Output Voltages of the DAC

P_{OUT} (dBm)	Condition	Comparator Output	XOR Output	$V_{CONTROL}$ (V)
<-7.8	$V_{PDET} < V_{REF1}$	00000	100000	1.52
>-7.5	$V_{PDET} > V_{REF1}$	10000	010000	1.55
>-2.75	$V_{REF2} < V_{PDET} < V_{REF3}$	11000	001000	1.57
>5	$V_{REF3} < V_{PDET} < V_{REF4}$	11100	000100	1.59
>7.5	$V_{REF4} < V_{PDET} < V_{REF5}$	11110	000010	1.62
>9.5	$V_{PDET} > V_{REF5}$	11111	000001	1.7

As shown in Table 1, there are five comparator reference voltages, V_{REFx}, where x = 1 to 5. A corresponding digital signal is generated (XOR output) when the detected output power of the PA satisfies the condition set out in Table 1. This digital signal then commands the DAC to output the desired control voltage, which then drives the VGA.

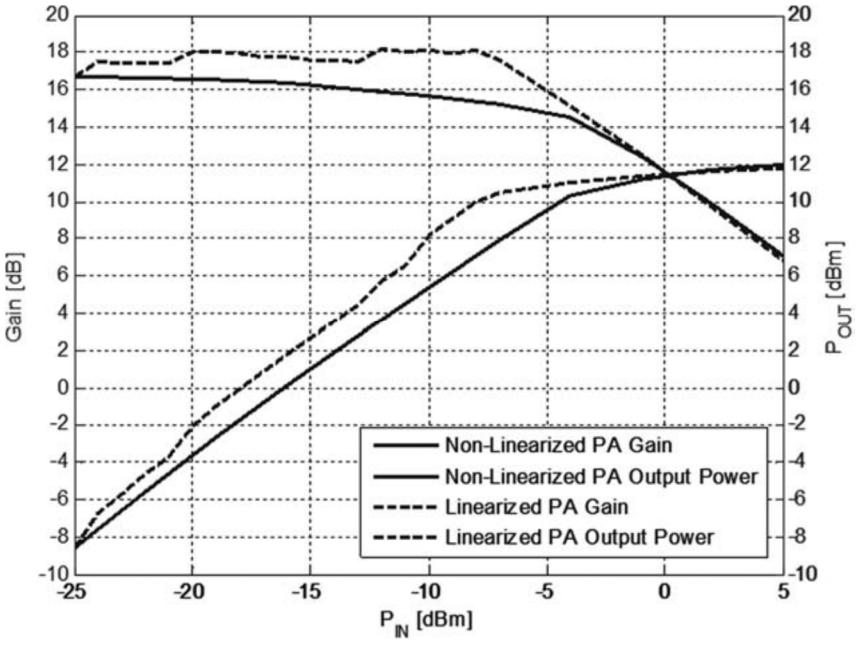

Figure 6 Gain and output power for non-linearized and linearized PAs

4. RESULTS

Figure 6 plots the non-linearized and linearized gain and output power of the PAs. The input power 1 dB compression point ($IP_{1\,dB}$) of the non-linearized PA occurs at -10 dBm. With the linearized PA, the gain is fixed around 18 dB, resulting in an increased $IP_{1\,dB}$ of -6 dBm and linearized output power. The linearized PA shows an improvement of 2.5 dBm, at which point no further linearization can be applied and the linearised PA begins to saturate. The power added efficiency (PAE) of both the non-linearized and linearized PAs is shown in Figure 7. The peak

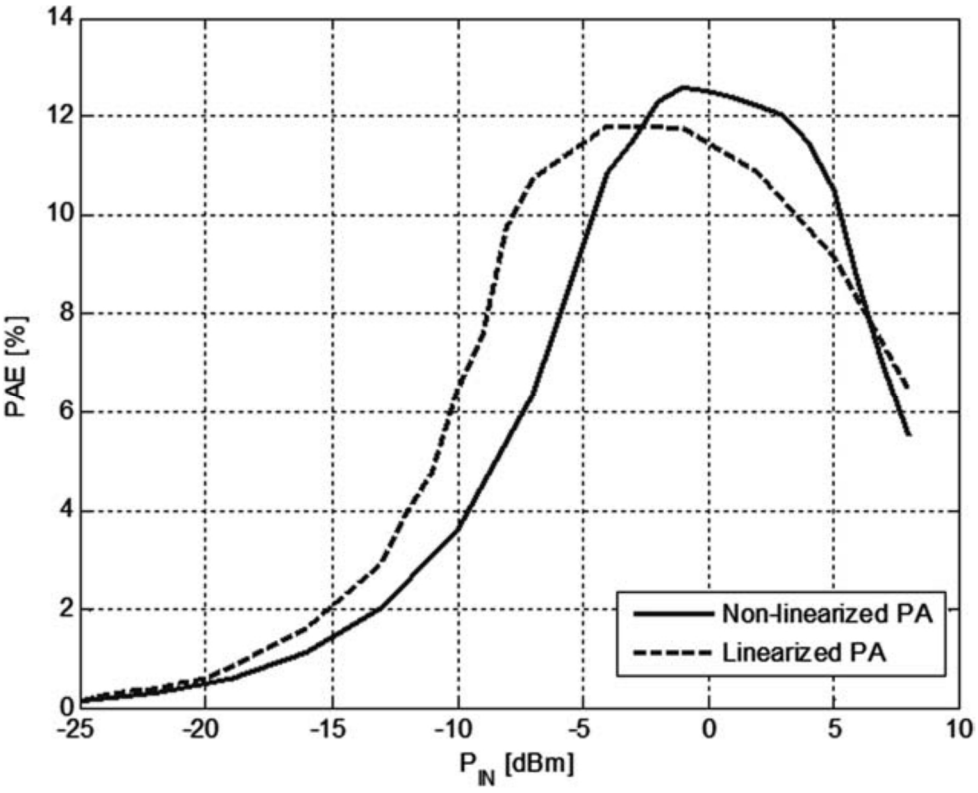

Figure 7 PAE for non-linearized and linearized Pas

PAE of the non-linearized PA is 12.6%; however, at the $IP_{1\,dB}$ the PAE is 3.63% while the peak PAE of the linearized PA is 11.8% and 11% at the $IP_{1\,dB}$. The reduced PAE (as defined in (23)) is expected because of the increased P_{DC} due to the dynamic bias mechanism.

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \quad (23)$$

The IMD3 components are shown in Figure 8. A 100 MHz tone spacing was used in the two-tone test to analyse the IMD3 components. The use of the predistortion linearization technique results in a reduction of the IMD3 component. Optimum reduction is achieved for output power between -7 and 3 dBm with a maximum IMD3 improvement of 10 dB being achieved.

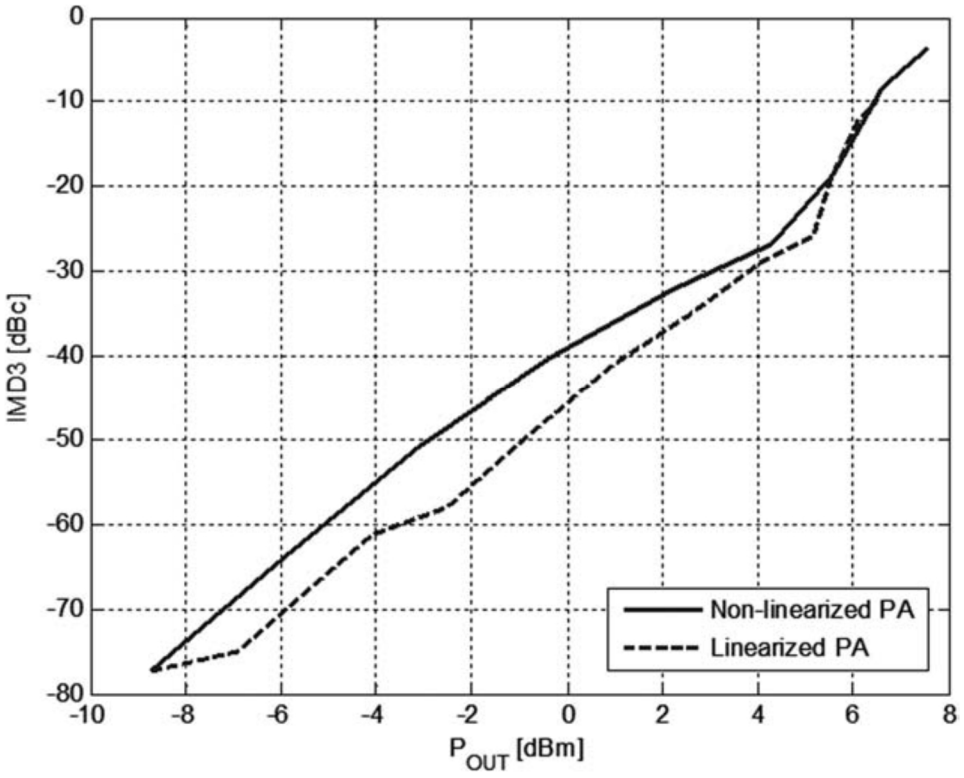

Figure 8 IMD3 components for non-linearized and linearized Pas

5. CONCLUSION

A 60 GHz PA with adaptive predistortion using the IBM BiCMOS process was presented.The PA saturates at 11.97 dBm. The predistortion circuit improves the linearity of the PA with an optimum IMD3 improvement of 10 dB. The linearization technique also improves the linear

output power to $IP_{1\ dB}$ from -10 dBm to -6 dBm, resulting in an improved linear output power of 2.5 dBm.

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