A TEMPERATURE STABILISED CMOS VCO BASED ON AMPLITUDE CONTROL

by

Johny Sebastian

Submitted in partial fulfilment of the requirements for the degree
Master of Engineering (Microelectronic Engineering)

in the

Department of Electrical, Electronic and Computer Engineering
Faculty of Engineering, Built Environment and Information Technology

UNIVERSITY OF PRETORIA

November 2013

SUMMARY

A TEMPERATURE STABILISED CMOS VCO BASED ON AMPLITUDE CONTROL

by

Johny Sebastian

Supervisor: Prof. S. Sinha

Department: Electrical, Electronic and Computer Engineering

University: University of Pretoria

Degree: Master of Engineering (Microelectronic Engineering)

Keywords: Analogue integrated circuits, automatic amplitude control, CMOS integrated circuits, CMOS technology, frequency drift, radio frequency integrated circuits, temperature dependence, thermal instability, threshold voltage, voltage-controlled oscillator.

Speed, power and reliability of analogue integrated circuits (IC) exhibit temperature dependency through the modulation of one or several of the following variables: band gap energy of the semiconductor, mobility, carrier diffusion, current density, threshold voltage, interconnect resistance, and variability in passive components. Some of the adverse effects of temperature variations are observed in current and voltage reference circuits, and frequency drift in oscillators. Thermal instability of a voltage-controlled oscillator (VCO) is a critical design factor for radio frequency ICs, such as transceiver circuits in communication networks, data link protocols, medical wireless sensor networks and microelectromechanical resonators. For example, frequency drift in a transceiver system results in severe inter-symbol interference in a digital communications system. Minimum transconductance required to sustain oscillation is specified by Barkhausen's stability criterion. However it is common practice to design oscillators with much more transconductance enabling self-startup. As temperature is increased, several of the variables mentioned induce additional transconductance to the oscillator. This in turn translates to a negative frequency drift.

Conventional approaches in temperature compensation involve temperature-insensitive biasing proportional-to-absolute temperature, modifying the control voltage terminal of the

VCO using an appropriately generated voltage. Improved frequency stability is reported when compensation voltage closely follows the frequency drift profile of the VCO. However, several published articles link the close association between oscillation amplitude and oscillation frequency. To the knowledge of this author, few published journal articles have focused on amplitude control techniques to reduce frequency drift. This dissertation focuses on reducing the frequency drift resulting from temperature variations based on amplitude control. A corresponding hypothesis is formulated, where the research outcome proposes improved frequency stability in response to temperature variations.

In order to validate this principle, a temperature compensated VCO is designed in schematic and in layout, verified using a simulation program with integrated circuit emphasis tool using the corresponding process design kit provided by the foundry, and prototyped using standard complementary metal oxide semiconductor technology. Periodic steady state (PSS) analysis is performed using the open loop VCO with temperature as the parametric variable in five equal intervals from 0 – 125 °C. A consistent negative frequency shift is observed in every temperature interval (≈ 11 MHz), with an overall frequency drift of 57 MHz. However similar PSS analysis performed using a VCO in the temperature stabilised loop demonstrates a reduced negative frequency drift of 3.8 MHz in the first temperature interval. During the remaining temperature intervals the closed loop action of the amplitude control loop overcompensates for the negative frequency drift, resulting in an overall frequency spread of 4.8 MHz. The negative frequency drift in the first temperature interval of 0 to 25 °C is due to the fact that amplitude control is not fully effective, as the oscillation amplitude is still building up. Using the temperature stabilised loop, the overall frequency stability has improved to 16 parts per million (ppm)/°C from an uncompensated value of 189 ppm/°C.

The results obtained are critically evaluated and conclusions are drawn. Temperature stabilised VCOs are applicable in applications or technologies such as high speed-universal serial bus, serial advanced technology attachment where frequency stability requirements are less stringent. The implications of this study for the existing body of knowledge are that better temperature compensation can be obtained if any of the conventional compensation schemes is preceded by amplitude control.

OPSOMMING

'N TEMPERATUURGESTABILISEERDE CMOS-SBO GEBASEER OP AMPLITUDEBEHEER

deur

Johny Sebastian

Studieleier: Prof. S. Sinha

Departement: Elektriese, Elektroniese en Rekenaaringenieurswese

Universiteit: Universiteit van Pretoria

Graad: Meester in Ingenieurswese (Mikroelektroniese Ingenieurswese)

Sleutelwoorde: Analoog-geïntegreerde stroombane, outomatiese amplitudebeheer, CMOS geïntegreerde stroombane, komplementêre metaal-oksied-halfgeleiertegnologie (CMOS-tegnologie), frekwensiedwaling, radiofrekwensie-geïntegreerde stroombane, temperatuurafhanklikheid, termiese onstabiliteit, drempelspanning, spanningsbeheerde ossilator.

Die spoed, krag en betroubaarheid van analoog-geïntegreerde stroombane toon temperatuurafhanklikheid deur die modulasie van een of verskeie van die volgende veranderlikes: bandgapingsenergie van die halfgeleier, mobiliteit, draerdiffusie, stroomdigtheid, drumpelspanning en tussenskakelweerstand, asook toleransies in passiewe komponente. Van die nadelige effekte van temperatuurwisseling kan waargeneem word in stroom- en spanningverwysingsbane en frekwensiedwaling in ossilators. Die termiese onstabiliteit van 'n spanningsbeheerde ossilator (SBO) is 'n kritiese ontwerpsfaktor vir radiofrekwensie-stroombane, soos gevind in sender-ontvangerstroombane, dataskakelprotokolle, mediese draadlose sensornetwerke en mikroelektromeganiese resoneerders. Frekwensiedwaling in 'n sender-ontvangerstelsel kan byvoorbeeld ernstige intersimboolversteuring in 'n digitale kommunikasiestelsel tot gevolg hê. Die minimum transkonduktansie wat vereis word om 'n ossilasie te handhaaf, word deur Barkhausen se stabiliteitkriteria gespesifiseer, maar dit is algemene gebruik om ossilators met heelwat meer transkonduktansie te ontwerp, wat self-aanskakeling moontlik maak. Soos die temperatuur verhoog word, veroorsaak verskeie van die veranderlikes wat genoem is

aanvullende transkonduktansie in die ossilator. Dit het ’n negatiewe frekwensiedwaling tot gevolg.

Konvensionele benaderings tot temperatuurkompensasie behels temperatuur-onsensitiewe voorspanning- proporsioneel-tot-absolute temperature, wat die beheerterminaal van die SBO verander deur die gebruik van ’n toepaslik opgewekte spanning. Verbeterde frekwensiestabiliteit word waargeneem wanneer die kompensasiespanning sterk ooreenstem met die freksensiedwalingprofiel van die SBO. Nogtans trek verskeie gepubliseerde artikels ’n verband tussen ossilasie-amplitude en ossilasiefrekwensie. Na die beste wete van hierdie outeur het baie min artikels tot dusver klem geplaas op amplitudebeheertegnieke om frekwensiedwaling te beperk. Hierdie verhandeling fokus daarop om die frekwensiedwaling wat ontstaan uit temperatuurwisselings gebaseer op amplitudebeheer te verminder. ’n Ooreenstemmende hipotese is geformuleer, waar die navorsingsresultaat verbeterde frekwensiestabiliteit in reaksie op temperatuurwisselings in die vooruitsig stel.

Om hierdie beginsel te bevestig, word ’n temperatuurgekompenseerde SBO in skematiese en uitlegformaat ontwerp, geverifieer deur die gebruik van ’n simulasieprogram met geïntegreerde stroombaanbeklemtoning wat gebruik maak van die ooreenstemmende proses-ontwerpstel wat deur die produksiefasiliteit voorsien is, en as prototipe ontwikkel deur die gebruik van standaard- CMOS-tegnologie. Periodieke bestendigetoestand-analise word uitgevoer deur die ooplus-SBO met temperatuur as die parametriese veranderlike, in ses gelyke intervalle van 0 – 125 °C. Konsekwente negatiewe frekwensieverskuiwing word waargeneem in elke temperatuurinterval (≈ 11 MHz), met ’n algehele frekwensieverskuiwing van 57 MHz. Soortgelyke periodieke bestendige toestand-analise, wat uitgevoer word deur ’n SBO in die temperatuurgestabiliseerde lus te gebruik, demonstreer egter verminderde negatiewe frekwensiedryf van 3.8 MHz in die eerste temperatuurinterval. Gedurende die oorblywende temperatuurintervalle oorkompenseer die geslotelus-aksie van die amplitude-beheerlus vir die negatiewe frekwensiedryf, wat ’n algehele frekwensieverspreiding van 4.8 MHz tot gevolg het. Die negatiewe frekwensiedryf in die eerste temperatuurinterval van 0 tot 25 °C kan toegeskryf word aan die feit dat amplitudebeheer nie ten volle doeltreffend is nie, omdat die ossilasie-amplitude nog besig is om op te bou. Deur die gebruik van die temperatuurgestabiliseerde lus het die algehele frekwensiestabiliteit verbeter vanaf ’n ongekompenseerde waarde van 189 ppm/°C tot 16 ppm/°C.

Die resultate wat verkry is, word krities geëvalueer en gevolgtrekkings word gemaak. Temperatuurgestabiliseerde SBOs kan aangewend word in toepassings of tegnologie soos ’n hoëspoed- universele geleistam en reeks-gevorderde tegnologiese hegstuk waar frekwensiestabiliteitvereistes nie so streng is nie. Die implikasie van hierdie studie vir die bestaande kennisveld is dat beter temperatuurkompensasie behaal kan word indien enige van die konvensionele kompensasieskemas voorafgegaan word deur amplitudebeheer.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my loving wife, Rina, daughters, Shweta and Priyanka, for their support and patience during the study. Thanks to my parents, Rosamma and Scaria Sebastian, who taught me the importance of 'consistent hard work' from an early age, which has motivated me in this journey.

Very special thanks to my academic supervisor, and good friend, Prof. Saurabh Sinha, for his interminable belief in me and incredible amounts of support and timely guidance. Many thanks to Mrs Tilla Nel for administrative support, Dr Jannes Venter for Cadence Virtuoso related assistance, Adriaan de Kamper and Johan Schoeman for verifying the summary in Afrikaans, and Marius Goosen and Antonie Alberts for their assistance at the laboratory, Carl & Emily Fuchs Institute for Microelectronics (CEFIM), Dept.: Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa.

I would like to acknowledge fellow student Johan Venter for his assistance in improving this dissertation and wise suggestions. A special mention to Dr Deepa George for her help with Linux operating system related issues and also for intelligent discussions regarding the research topic and Dr Wynand Lambrechts for the final proofreading for consistency.

Finally I would like to thank my employer, Tshwane University of Technology, South Africa, for providing the opportunity to undertake this study and for partially funding this research.

LIST OF ABBREVIATIONS

AAC	Automatic amplitude control
ABB	Adaptive body bias
AC	Alternating current
BiCMOS	Bipolar complementary meta-oxide semiconductor
BJT	Bipolar junction transistor
BSIM	Berkeley short-channel insulated gate-FET model
BSN	Body sensor network
CAD	Computer aided design
CMOS	Complementary metal oxide semiconductor
DC	Direct current
DRC	Design rule check
FBAR	Film bulk acoustic-wave resonator
FOM	Figure of merit
HBT	Hetero-junction bipolar transistor
HQ	High quality-factor
IC	Integrated circuit
LQ	Low quality-factor
LVS	Layout versus schematic-check
MEMS	Microelectromechanical systems
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
MPW	Multi project wafer
NDA	Non-disclosure agreement
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PDK	Process design kit

PLL	Phase locked loop
PLS	Post layout simulation
ppm	Parts per million
PSS	Periodic steady state
PTAT	Proportional to absolute temperature
PVT	Process-voltage-temperature
Q	Quality-factor
RF	Radio frequency
SiGe	Silicon germanium
SIW	Substrate integrated waveguide
SPICE	Simulation program with integrated circuit emphasis
TC	Temperature coefficient
TM	Typical mean
VBIC	Vertical bipolar integrated company
VCO	Voltage-controlled oscillator
WP	Worst-case power
WS	Worst-case speed
ZTC	Zero temperature coefficient

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Context of the problem

Current and voltage references are essential circuits in many analogue and mixed-circuit designs to establish the quiescent points in circuits such as oscillators, amplifiers and phase-locked loops (PLL). Any variability in voltage and current reference as a result of temperature variation is a critical design problem [1], [2], especially for radio frequency (RF) applications. Furthermore, frequency drift in oscillators as a result of temperature variation is a profound consideration in modern electronic systems, such as transceiver circuits in mobile and communication networks, medical sensor networks and micromechanical resonators used in the silicon die [3].

Several temperature compensation methods are described in literature. In voltage and current references temperature insensitive bias is generated using proportional to absolute temperature (PTAT) sources [4]. In voltage-controlled oscillators (VCOs), a suitable compensation voltage is created and used to modify the control voltage (V_{CNTRL}) terminal relating to the oscillator frequency [5], [6], [7]. The frequency of the inductor-capacitor-based (LC) VCO may be represented by equation (1.1).

$$\omega(T) = \sqrt{\frac{1}{L\left(C_f + C_v(V_{CNTRL})\right)}\left[1 - \frac{C_f R_L^2(T) + C_v(V_{CNTRL})R_L^2}{L}\right]} \tag{1.1}$$

where L *is* the inductor, C_f, the fixed capacitance in the tank circuit, C_v, the variable capacitance of a varactor controlled by a voltage V_{CNTRL}, and the R_L the losses in the inductor [8]. As the temperature is increased, $V_{CNTRL}(T)$ is increased in a corresponding manner such that the resulting change in C_v compensates for the frequency drift.

Superior frequency accuracy and low drift with temperature and low noise have allowed quartz crystal tuned oscillators to become the industry standard over many years to provide a clock reference in several systems [9]. As the density of electronics has grown exponentially, the size of the crystal has remained the same. Many authors are exploring

the possibility of using film bulk acoustic wave resonator (FBAR) based oscillators [9]. In comparison with complementary metal oxide semiconductor (CMOS) LC oscillators, FBAR based oscillators have successfully demonstrated a superior power and phase noise performance, but still suffer from a negative temperature coefficient (TC) and needs to be compensated electronically [9]. An on-chip PTAT sensor reads the temperature and the digitised output removes an appropriate capacitor from the VCO tank circuit, in effect reducing the frequency drift [9], [10]. Furthermore to maintain optimum phase noise, it is essential to limit the drive amplitude. An automatic level control circuit to minimise the phase noise and a generated compensation voltage for frequency compensation is described in [11].

A combination of material compensation and electronic compensation is applied in [3], where material compensation makes use of silicon dioxide (SiO_2) with positive TC in the resonator stack to neutralise the effect of the negative TC of silicon. To compensate accurately further for the oscillator drift, a compensating voltage is obtained by differencing a PTAT reference and band gap reference. This error voltage is then converted to a corresponding error current. The square root of the error current generates a compensation voltage identical to the ‘S’-shaped frequency response of a varactor used in frequency compensation [3], [8].

Another effective method of temperature compensation reported by [12] is applicable for millimetre-wave oscillators using substrate integrated waveguide (SIW) oscillators. The dimensions and permittivity of the substrate of the intra-chip cavity affects the resonant frequency. In the proposed method [12] the dimensions are carefully selected as the coefficient of expansion of the cavity compensates for frequency drift.

Various physiological sensors in implantable body sensor networks (BSN) provide wireless connectivity to a nearby base station for medical applications. The BSN essentially operates in power-saving mode, but needs to be calibrated for frequency regularly for effective operation under temperature variations. In implantable devices, an

injection-locked frequency divider architecture is proposed in [13]. For such implantable devices, the base station is locked to a crystal oscillator frequency using a PLL. The base station sends the reference signal periodically to the BSN, which in turn performs the frequency recalibration.

For VCOs, oscillation amplitude is associated with the oscillating frequency [14]. Therefore amplitude control techniques become necessary to keep the oscillation frequency steady. An amplitude control mechanism to reduce the phase noise and to improve immunity against process, supply voltage and temperature (PVT) variations is suggested [15], [16], [17], [18].

This section summarises the effect of temperature change on current, voltage references, and resulting frequency instability in oscillators. Therefore frequency drift compensation is necessary for RF applications, and various methods implemented in the current body of knowledge are described. In VCOs frequency drift is also linked to the oscillation amplitude instability.

1.1.2 Research gap

To the knowledge of this author, the current body of knowledge concentrates on generated error voltage as a means to compensate for frequency drift and the use of amplitude control techniques for improving immunity against PVT variations. This research focuses on an amplitude control mechanism for frequency drift compensation resulting from temperature variation.

1.2 RESEARCH OBJECTIVE AND QUESTIONS

The research objective in this study is to reduce the temperature dependency of the LC VCO. This research objective raises the following research questions:

- How is it possible to compensate for *frequency drift* in LC VCO as a result of temperature variations?

- What are the different factors affecting frequency drift of an LC oscillator as a result of temperature variations?
- How are the individual variables contributing to the dynamics of frequency drift and are any of these variable noncumulative?
- How is it possible to reduce the influence of these variables on frequency drift?

The hypothesis for this study is formulated as follows.

> *If factors that contribute to frequency drift as a result of temperature variations in an LC VCO are identified, it is possible to reduce the influence of temperature by controlling the frequency drift dynamics.*

1.3 JUSTIFICATION FOR THE RESEARCH

Table 1.1 compares this work with recent and relevant journal articles in the field of temperature compensation in oscillators. References [3], [9], [11] in the table have used bulk acoustic wave resonators and the remaining references are either *LC* or *RC* oscillators. Reference [12] describes the implementation of temperature compensation by making use of the thermal coefficient of expansion of silicon cavity in SIW oscillator, while authors [3], [4], [7], [8], [11] have used the control voltage terminal of the VCO by supplying a suitable compensating voltage generated within the substrate. Reference [10] has adaptively modified the fractional-*N* frequency synthesiser according to a temperature reference implemented in the substrate to implement frequency compensation.

A PTAT source is used in the generation of compensation voltage in [4], where a voltage divider formed using polysilicon resistance with a positive TC and a diffusion resistance with a negative TC is utilised in [7]. A non-linear compensation voltage generated is used for frequency compensation in [3], [8], [11].

Table 1.1 Comparison of this work with relevant published work in the current body of knowledge

	[3] 2012	**[9] 2010**	**[11] 2007**	**[12] 2012**	**[4] 2012**	**[7] 2010**	**[8] 2009**	**[10] 2010**	**This work**
Technology node	0.18 µm	0.35 µm	0.6 µm	-	90 nm	0.18 µm	0.25 µm	0.18 µm	0.35 µm
Frequency (MHz)	427	1500	5.5	9921	1400	14	800	20	2400
Temperature range (°C)	-10 – 70	0 – 100	25 – 125	-40 – 80	30 – 100	-40 – 125	-10 – 80	-40 – 85	0 – 125
$\Delta_f = \frac{\partial_f \times 10^6}{\Delta T \times f_r}$ (ppm/°C)	±0.4375	±10	0.39	2.11	51.43	11.52	1.689	±0.24	15.89
Type of compensation	2nd order parabolic compensation using negative capacitance	Mechanical coarse tuning, fine tuning using digital removal of capacitor bank	Amplitude control, a temperature compensating bias circuit proportional to a square root of a reference current	Using coefficient of expansion of SIW cavity	V_{CNTRL} modified using a voltage compensation	V_{CNTRL} modified using a voltage compensation	V_{CNTRL} modified using a voltage compensation	Fractional-*N* synthesiser adaptively programmed	Amplitude control
Oscillator architecture	LBAR resonator	FBAR resonator	FBAR resonator	SIW resonator	Ring VCO	*RC*	*LC*	*LC*	*LC*

1.4 METHODOLOGY

This research starts with a literature study to identify the causes of frequency drift in an LC VCO. In order to implement the selected compensation method, the technology provided by ams AG (formerly known as austriamicrosystems AG) is reviewed. A suitable block diagram is presented and developed into a circuit schematic. The schematic design is simulated using Cadence Virtuoso to verify the expected compensation. The layout of the schematic is then prepared. The complete design is then prototyped and mounted on a printed circuit board (PCB). In order to answer the research questions and to verify the hypothesis, the prototyped temperature stabilised VCO is subjected to different temperatures and the corresponding oscillation frequencies are recorded and analysed.

1.5 OUTLINE OF THIS REPORT

This study is documented as follows:

- Chapter 1: Introduction

  This chapter describes the context of the research problem, research questions and hypothesis, and gives a brief description of the methodology followed.
- Chapter 2: Literature study

  The literature study that revealed the origins of frequency drift in LC VCOs is described in this chapter. Contributions by various authors are reviewed. The selected method of frequency drift compensation using amplitude control is reviewed, and compared to current methods.
- Chapter 3: Research methodology

  The methodology followed is further elaborated in this chapter by considering different possible independent variables and dependent variables. In the case of multiple independent variables, various options are considered for keeping it constant during testing. Chapter 3 concludes with the measurement setup.
- Chapter 4: Circuit design

  The schematic and layout design of the temperature stabilised VCO is described in Chapter 4. RF design using the transconductance efficiency (g_m/I_D) method is

followed for the design of two relevant blocks: the oscillator and the operational amplifier for best compromise between power consumption and speed. Chapter 4 provides the complete layout prototyped in silicon and mounted on a PCB to be verified.

- Chapter 5: Simulation results and experimental verification

  The experimental verification is described in Chapter 5. Simulation results are provided together with measured results to verify the hypothesis. Post-layout simulation (PLS) results are provided where necessary. All the research questions are addressed and the verification of the hypothesis is concluded in this chapter.

- Chapter 6: Conclusion

  Chapter 6 concludes this study by critically evaluating the frequency compensation using automatic amplitude control (AAC). Possible methods for improving the frequency compensation beyond what has been achieved so far are discussed and possible future research areas as a result of this study are documented.

1.6 DELIMITATIONS OF THE SCOPE OF THIS STUDY

The objective of this research is to reduce the frequency drift as a result of temperature variations. Some methods used are applicable in general to PVT variations. While phase noise is important in VCOs, optimisation of phase noise is outside the scope of this work and not presented in this dissertation.

1.7 CONCLUSION

This chapter contextualises this research by presenting various frequency stabilisation methods. Research questions and a research hypothesis are formulated. Descriptions of the methodology followed in this study are mentioned, followed by an overview of this dissertation.

CHAPTER 2 LITERATURE STUDY

2.1 INTRODUCTION

Chapter 1 presented that the output frequency of an oscillator varied as the ambient temperature was changed. As the dissertation progresses to Chapter 2, the effect of variation of temperature on each component and building block of a VCO needs to be identified. The cause of temperature dependency on semiconductors and on on-chip passive components such as diffused resistors, capacitors and inductors are investigated in sections 2.2 – 2.3. Sections 2.4 – 2.5 examined the current sources and in section 2.6 – 2.7 discuss the VCO core, topology and various parameters of interest and identified the mechanism of frequency drift.

In order to validate the hypotheses, the methods of temperature compensation techniques will be explored in section 2.8 to identify possible compensation strategies at RF.

2.2 TEMPERATURE DEPENDENCY IN SEMICONDUCTORS

2.2.1 Metal-oxide semiconductor (MOS) devices

The threshold voltage V_t of a semiconductor junction is

$$V_t = \frac{\sqrt{2qN_A\varepsilon(2\emptyset f)}}{C_{ox}} + 2\emptyset_f + \emptyset_{ms} - \frac{Q_{ss}}{C_{ox}} \tag{2.1}$$

where,

$$\emptyset_f = \frac{kT}{q}\ln\left[\frac{N_A \exp\left(\frac{Eg}{2kT}\right)}{\sqrt{N_c N_v}}\right] \tag{2.2}$$

and

$$\gamma = \frac{1}{C_{ox}}\sqrt{2q\epsilon N_A}\ \mathrm{V}^{½} \tag{2.3}$$

where,

q is the electron charge (1.6×10^{-19} C), N_D, N_A are the doping densities of donor atoms and acceptor atoms respectively, ε is the permittivity of silicon (1.04×10^{-10} F/m), Φ_f is the Fermi level potential (usually 0.3 V) of silicon, C_{ox} is the gate oxide capacitance per unit area, $\emptyset_{ms}$ is the work function difference between gate metal and silicon, Q_{ss}/C_{ox} is the negative gate-source voltage that is required to overcome positive potential that exists at

the gate oxide-silicon interface, E_g is the band-gap energy of silicon at absolute zero (0 K), k = 1.38 × 10 $^{-23}$ J/K is the Boltzmann's constant, T is the temperature in Kelvin scale, N_v and N_c are the densities of allowed states at the edges of valance band and conduction band respectively [19].

By substituting (2.2) into (2.1) and differentiating with respect to temperature yields

$$\frac{dV_t}{dT} = -\frac{1}{T}\left[\frac{E_g}{2q} - \emptyset_f\right]\left[2 + \frac{\gamma}{\sqrt{2\emptyset_f}}\right] \tag{2.4}$$

If $E_g /2q > \Phi_f$ according to (2.4) the threshold voltage, V_t decreases with increment in temperature [19].

The expression for drain current in an *n*-channel metal-oxide semiconductor field effect transistor (MOSFET), derived for long channel operation is

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2 \tag{2.5}$$

Equation (2.5) has the mobility term μ_n and the threshold voltage V_t, both depends on temperature and both the variables have negative TC [20]. Therefore it is possible to have a zero temperature coefficient (ZTC) bias point, where any variation in temperature should not affect the bias point.

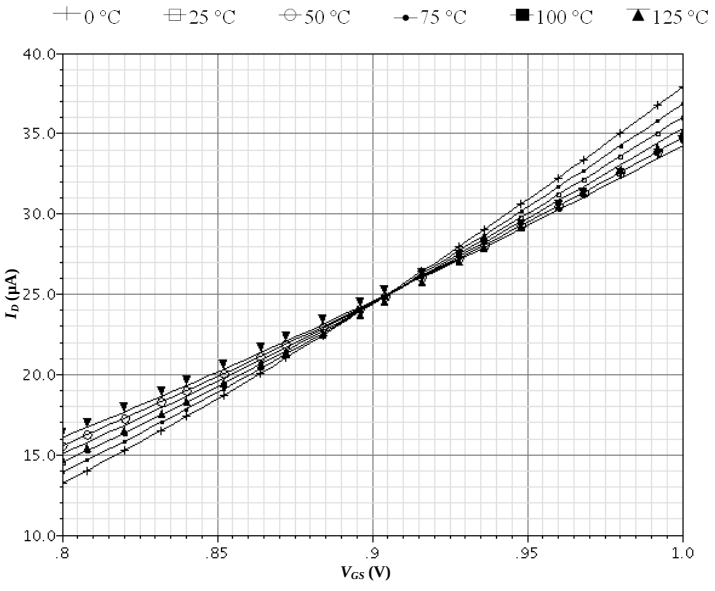


Figure 2.1 ZTC bias point for an *n*-channel enhancement MOSFET with *W*=10 µm and *L* = 0.35 µm, simulated in Cadence Virtuoso

Fig. 2.1 depicts the variation of drain current (I_D) for different V_{GS}, for a MOSFET simulated in Cadence Virtuoso using process models supplied by the foundry ams AG. Mutual cancellation of mobility and threshold voltage temperature variations utilised in making temperature independent voltage source is demonstrated in [20]. P channel enhancement MOS devices also demonstrate a ZTC bias point.

2.2.2 Heterojunction bipolar transistors (HBT)

All the derivations in this section are presented for NPN devices operating in the forward active region. PNP devices will show similar trends but with polarity reversed. An HBT differs from a bipolar junction transistor (BJT) in fabrication and semiconductor materials used. HBTs demonstrate similar direct current (DC) characteristics compared to conventional BJT, but its performance in alternating current (AC) is far superior. The use of silicon-germanium (SiGe) alloy in base region reduces the base transit time considerably by accelerating the electrons to its near saturation velocity [21]. Considering the fact that base transit time actually limits the high frequency response in Si BJT, one could understand why an HBT could provide very high values of unity gain frequency (f_t). HBTs also show low phase noise profile and high immunity against radiation. These enhanced properties make it suitable for RF and microwave applications. 1/f noise performance of an HBT is at least two orders of magnitude compared to a BJT of similar size and bias current. However HBT behaves similar to BJT as far as temperature variations are concerned [21].

For Bipolar devices the base emitter voltage is

$$V_{BE} = V_T \ln \frac{Ic}{Is} \tag{2.6}$$

From equation (2.6) it can be shown that as the temperature increases V_{BE} reduces [19], [21].

2.3 EFFECT OF TEMPERATURE ON PASSIVE COMPONENTS

Integrated resistors are manufactured using ion implanted layers or diffused layers. These substrate resistance shows positive TC [22]. Monolithic capacitors are implemented by

making use of depletion capacitance of a *PN*-junction under reverse bias condition. This type of capacitance also varies with the amount of reverse bias applied [19]. MOS capacitors are manufactured by making use of emitter diffusion area and aluminium metal layer sandwich a thin layer of S_iO_2 insulation. This form of capacitance shows much higher capacitance per area and better linearity and lower TC [19]. Typical value of TC of a poly-poly capacitor is 20 ppm/ºC [22].

Another passive component that is affected by variation of temperature is on-chip *LC* resonators. In Fig. 2.2 an *LC* resonator is modelled by an ideal inductance *L* in parallel with inter-wire capacitance *C*. The series resistances R_L and R_C are representing the corresponding ohmic losses in the coil [23].

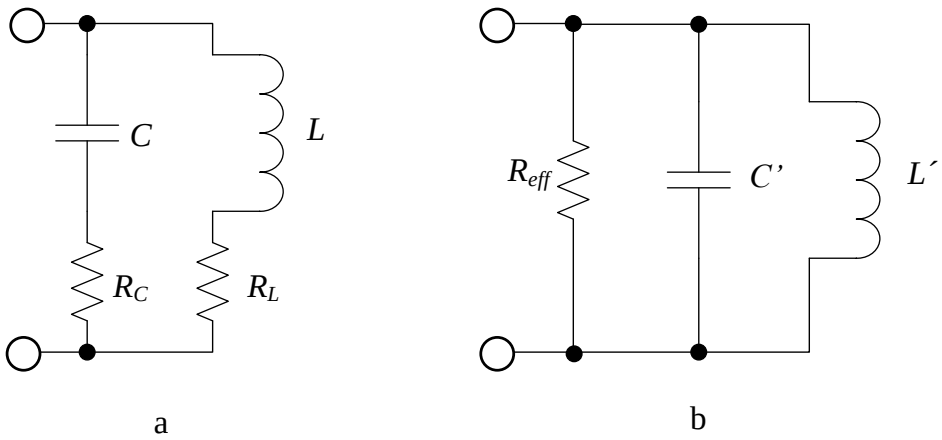


Figure 2.2 a. A simplified *LC* resonator schematic, b. parallel equivalent diagram [23]

Using series to parallel conversion it is well-known that

$$R_{eff} \cong \left(Q_L{}^2 + 1\right)\frac{R_L}{R_L+R_C} \tag{2.7}$$

$$Q_L \cong \frac{\omega_o L}{R_L} \tag{2. 8}$$

Increase in R_L caused by increased temperature results in negligible change in R_{eff} from (2.7). But from (2.8) it is obvious that the quality factor (Q_L) of the inductor is reduced.

2.4 SOURCES WITH POSITIVE TEMPERATURE COEFFICIENT

From (2.7) the thermal voltage is directly proportional to absolute temperature. An implementation of thermal voltage referenced current source using bipolar CMOS (BiCMOS) is given in Fig. 2.3 [19].

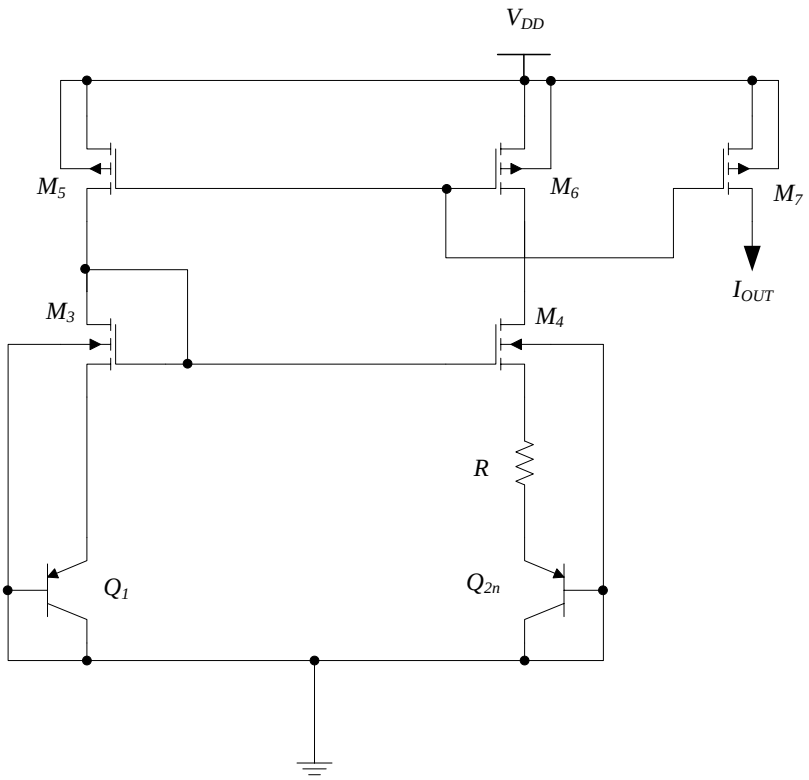


Figure 2.3 V_T referenced current source using BiCMOS process [19] (© [2010], with permission from John Wiley & Sons, Inc.)

From Fig. 2.3, it can be shown that the difference between two emitter voltages appear across R and if Q_2 has the emitter base area n times that of Q_1, then

$$I_{OUT} = V_T \frac{\ln n}{R} \tag{2.9}$$

By finding the derivative with respect to temperature and simplifying yields to

$$\frac{\partial I_{OUT}}{\partial_T} = \ln n \left[R \frac{\partial VT}{dT} V_T \frac{\partial R}{\partial T} \right] \tag{2.10}$$

Rearranging yields

$$TC = \frac{1}{I_{OUT}} \frac{\partial I_{OUT}}{\partial T} = \left[\frac{1}{V_T} \frac{\partial VT}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \right] \tag{2.11}$$

The first term in the parenthesis has positive TC and the second term, the diffused resistor also shows positive TC and they both tend to cancel each other at a certain temperature producing a lower TC. A V_T source shows variation of about 85 µV/ºC [19].

2.5 SOURCES WITH NEGATIVE TEMPERATURE COEFFICIENT

The threshold voltage reduces with increase in temperature (section 2.2.1). Therefore a current source that makes use of V_t shows a negative temperature coefficient. An implementation of a V_t referenced current source is in Fig. 2.4 [19].

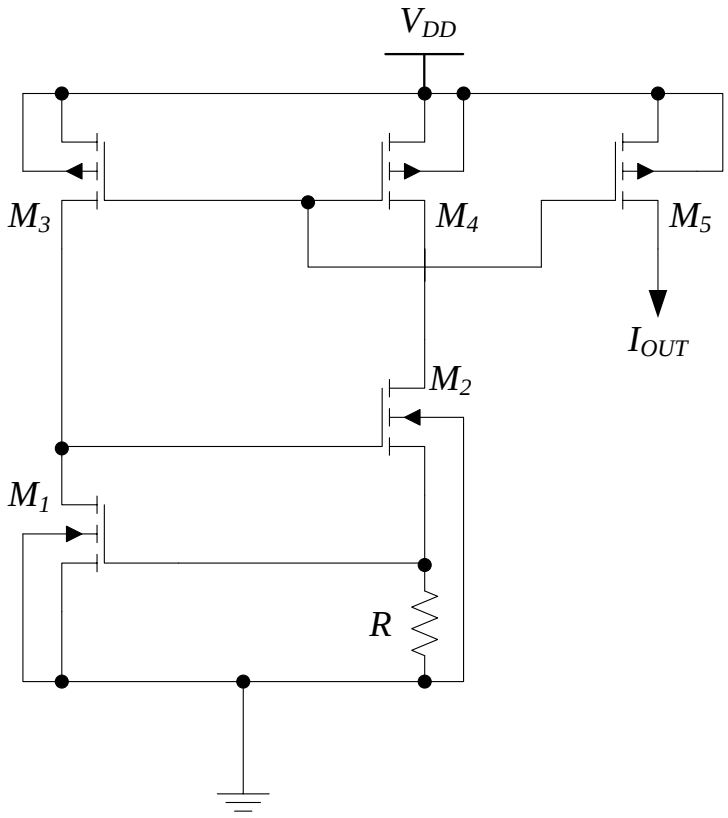


Figure 2.4 A threshold voltage referenced current source [19] (© [2010], with permission from John Wiley & Sons, Inc.)

From Fig. 2.4, the voltage across R is $V_t + V_{ov1}$. Hence

$$I_{OUT} = \frac{V_t + V_{OV1}}{R} \tag{2.12}$$

for devices with large geometry V_{ov1} could be very low compared to V_t. Therefore this circuit is known as V_t referenced bias circuit.

Sections 2.2 – 2.3 compiled the effect of temperature on semiconductors, passives such as integrated resistors, MOS capacitors. Effects of temperature variation on current sources are captured in sections 2.4 – 2.5.

2.6 VOLTAGE CONTROLLED OSCILLATORS

In order to associate the effects of temperature on semiconductors, passives, and current sources to frequency translation in an oscillator, it is imperative that one needs to re-visit the basic oscillator theory. Once the mechanisms that cause the frequency drift in an oscillator are identified an appropriate compensation strategy could be derived. This section starts with an investigation into theory of oscillations, various topologies of oscillators and adaptation of an oscillator as a VCO. Different parameters of interest of a VCO are to be explored. This section will conclude with an overview of an accepted figure of merit (FOM) of a VCO.

2.6.1 Theory of oscillations

Barkhausen's criteria of oscillation stipulates that the minimum condition for sustained oscillation is a close loop gain of unity. However to self-start the oscillation a more stringent requirement to be satisfied; closed loop gain > 1. It also specifies the frequency of oscillation will be determined by the feedback loop that provides the required phase shift. A block diagram depicting positive feedback adopted from [23] is given in Fig. 2.5.

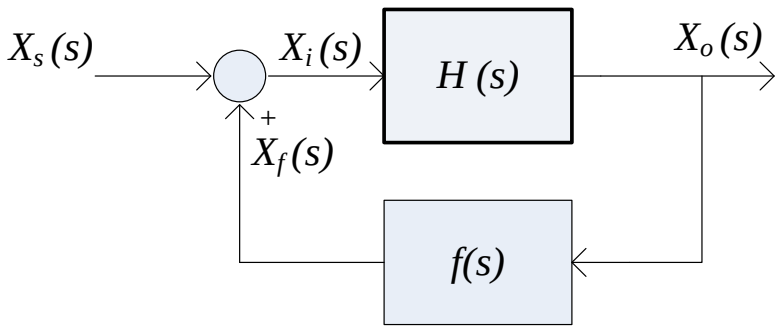


Figure 2.5 Block representation of positive feedback [23] (© [2009], with permission from Cambridge University Press)

From Fig. 2.5 closed loop expression yields to

$$\frac{Xo(s)}{Xi(s)} = \frac{H(s)}{1-H(s)f(s)} \tag{2.13}$$

When *H(s) f(s)* = 1 the gain of this closed loop system grows towards infinity and any noise that may present at the input will be amplified. When the magnitude of *H(s) f(s)* $= unity$, (loop gain) a self-sustained oscillation mechanism exists. However this condition does not ensure self-starting of oscillations. For a unity loop gain the circuit may latch rather than oscillate [23]. Therefore the loop gain should be greater than what is required to sustain the oscillations. For loop gain more than unity, the amplitude of oscillations grows in every cycle in the loop. In practical oscillators the nonlinearity of transistors forces the oscillation amplitude at its saturation levels. Fig. 2.6 illustrates a direct implementation of the block diagram in Fig. 2.5 using a tank circuit and positive feedback [23].

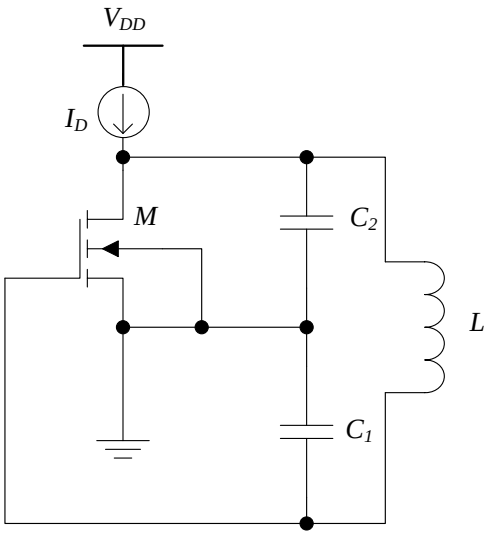


Figure 2.6 Colpitts oscillator [23] (© [2009], with permission from Cambridge University Press)

Using passive impedance transformation the impedance seen by the tank (Fig. 2.6) will be;

$$\frac{\left(1+\frac{C_1}{C_2}\right)^2}{g_m} \tag{2.14}$$

for Colpitts oscillator, and

$$\frac{\left(1+\frac{L1}{L2}\right)^2}{g_m} \tag{2.15}$$

for Hartley configuration

Proper selection of capacitance (inductance in case of Hartley) ratio the low input impedance of a common base (common gate) amplifier is effectively buffered, keeping the quality factor (Q) of the tank unaffected.

This section summarises the significance of gain of the sustaining amplifier and the Q factor of the inductor in an oscillator. Any variability in the gain of the amplifier as a result of temperature variation may affect the oscillator stability (sections 2.2 – 2.5).

2.6.2 Alternate view of an oscillator

If the transistor in Fig. 2.7a [24] is biased in linear region, the impedance seen between drain and gate of M_1 could be calculated by connecting a test voltage v_{test} and calculating the current produced by the test source (i_{test}).

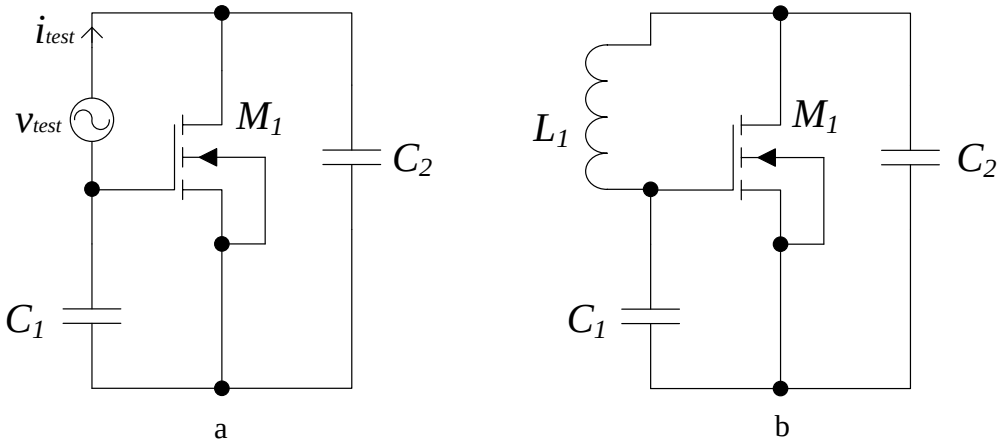


Figure 2.7 a. one port active circuit to find the input impedance, b. an inductor connected at the input port [24] (© [2001], with permission from McGraw-Hill)

From Fig. 2.7a it can be derived

$$Z_i = \frac{v_{test}}{i_{test}} = \frac{g_m}{s^2 C_1 C_2} + \frac{1}{sC_1} + \frac{1}{sC_2} \tag{2.16}$$

for $s = j\omega$, the input impedance term contains the real term ($-g_m/\omega^2 C_1 C_2$). Alternatively this circuit could be considered as 'active capacitance' that is capable of replacing the energy "converted" in an inductor if incorporated as a resonator together with an inductor. This circuit could generate and sustain oscillations if the inductor value is less than $L = g_m/\omega^2 C_1 C_2$. A common gate configuration will result if the gate terminal is connected as common ground. Similarly a common source and common drain configurations could be achieved by using source or drain terminal as common ground respectively. All the three possible configurations are given in Fig. 2.8.

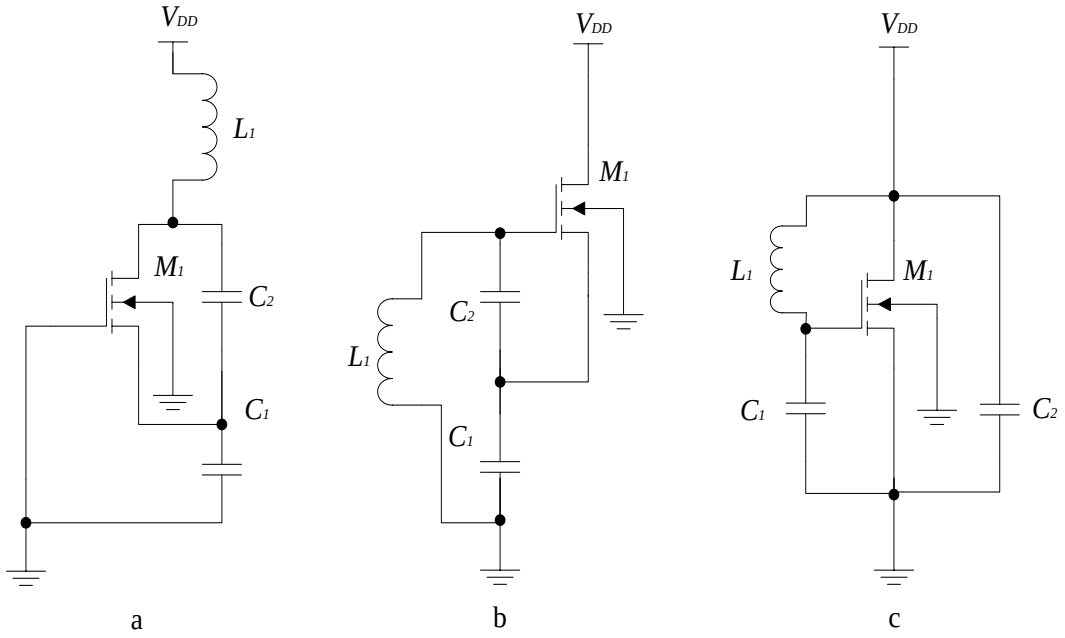


Figure 2.8 Three different configurations of oscillators [24], a. common gate, b. common drain, c. common source (© [2001], with permission from McGraw-Hill)

Due to inherent high frequency properties, a common gate topology is preferred over the other two configurations. To vary the frequency of an oscillator the capacitance or inductance associated with the tank needs to be varied. The capacitance associated with a varactor could be varied by controlling the amount of reverse bias across. Therefore in VCO implementations the most widely used method to vary the frequency is by connecting a reverse biased varactor in parallel with the tank [25], [26].

2.6.3 Oscillator quality factor

The Q of a tank is defined as "energy stored divided by energy dissipated", and is mainly limited by the winding resistance of the inductor [23]. Using this concept the

$$Q = \frac{\omega L}{R_L} \tag{2.17a}$$

where ωL is the inductive reactance of the coil and R_L is the series resistance of the inductor. Q of the oscillator will be less than Q of the tank due to various loading effects. Q of the oscillator

$$Q_{osc} = \frac{\omega_o}{2}\frac{d\Phi}{d\omega}$$

but

$$\frac{d\Phi}{d\omega} = -2C_{eq}R_{eff}$$

therefore

$$Q_{osc} = \omega_o R_{eff} C_{eq} \tag{2.17b}$$

where

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

Here R_{eff} is the equivalent parallel impedance considering all loading effects including input impedance of the active device and any resistive component of the inductance and any substrate contributions.

2.6.4 VCO topologies

Three configurations of oscillator are discussed before modified to a VCO. As per discussion in section 2.6.2 a common gate oscillator as in Fig. 2.8 was selected. The very low input impedance of the common gate amplifier makes it difficult to design a VCO for high frequency applications. An easier solution is to include a buffer between the tank and the input node as shown in Fig. 2.9. The buffer prevents the low input impedance of the transistor loading the tank. An equal amount of bias is provided for both gates of the transistors.

From Fig. 2.9 the impedance looking at any of the drain terminals is $-1/g_m$. Therefore the total impedance seen by the tank $R_{in} = 2/g_m$. This means that if the equivalent parallel resistance (R_{eff}) is less than the absolute value of R_{in} then this circuit will oscillate [23], [24]. This form of an oscillator is popularly known as negative transconductance oscillator as the name is self-explanatory.

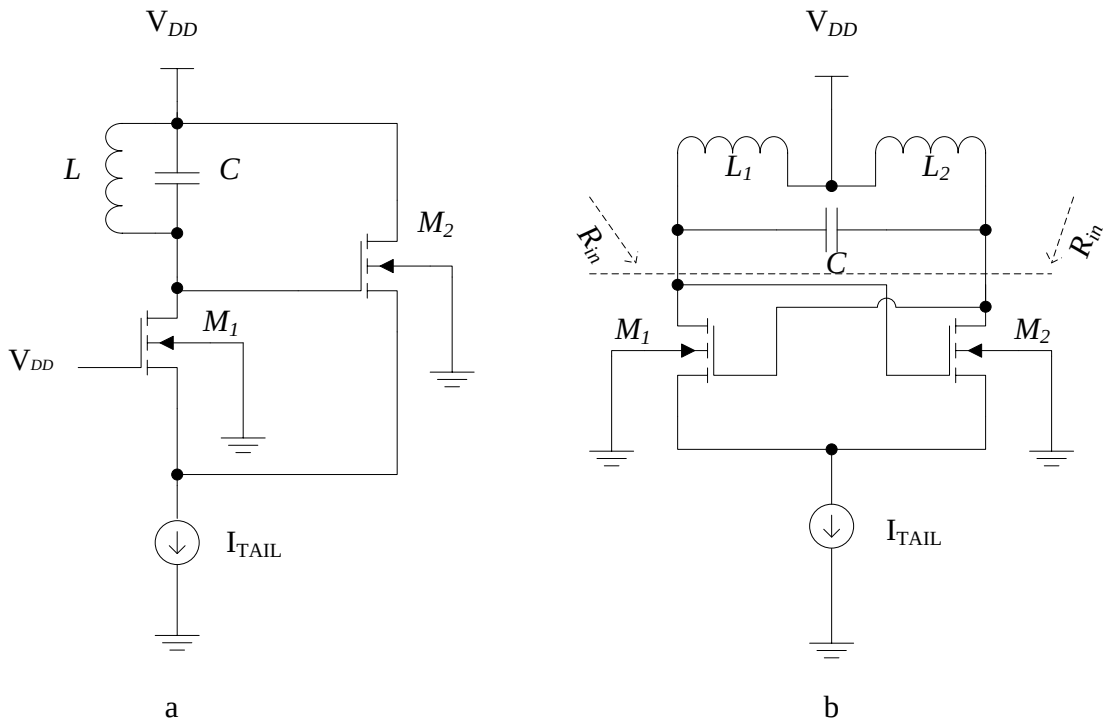


Figure 2.9 a. Common source buffer is added in the feedback loop of a Colpitts oscillator, b. Differential mode oscillator by addition of an inductor [23] (© [2009], with permission from Cambridge University Press)

The oscillator topology in Fig. 2.9b is termed differential and has certain benefits compared with previous topologies discussed. The voltage swing at the drain of M_2 will switch off M_1 and vice versa. Since both transistors are conceptually identical this will ensures that 50 % duty cycle is achieved.

2.6.5 VCO theory

The output of the VCO without any controlling voltage is known as “free running” frequency f_o. In presence of a control voltage (V_C), VCO output will be modified.

$$\omega(t) = \omega_o + K_{vco}V_C(t) \tag{2.18}$$

where, $K_{VCO} = d\omega/dt$ rad/s/V. K_{VCO} is also known as gain of the VCO in radians per second per voltage.

For a sinusoidal with an amplitude *A* and argument *Φ(t)*

it can be shown that

$$\omega(t) = A\sin[\omega_o t + K_{vco}\int V_C(t)\,dt] \tag{2.19}$$

This is the basic expression of a VCO in time domain [23], [25]. Assuming $V_C = 0$ V will still produce an output frequency same as VCO free running frequency. Narrow band frequency modulation will result if V_C is a sinusoidal with a small value argument.

2.6.6 VCO parameters

The two most predominant parameters of VCOs, phase noise and the tuning range are explained below.

2.6.6.1 Phase noise

Phase noise in a VCO influences the selectivity and signal to noise ratio of transmitters and receivers [27], [28]. Factors that determine the phase noise of an oscillator are silicon lattice photon scattering, MOS flicker noise and corner frequency, the resonator *Q*, and the final output signal to noise ratio [29]. Mathematical representation of a periodic sinusoidal

$$\omega(t) = [A\cos\omega_c t + \Phi_n(t)]$$

where $\Phi_n(t)$ is a small random excess phase representing variations in time period and is known as phase noise.

When

$$\Phi_n(t) \ll 1$$

then

$$\omega(t) \approx [A\cos\omega_c t - \Phi_n(t)\sin\omega_c t] \tag{2.20}$$

Equation (2.20) shows that the spectrum of phase noise is translated onto the carrier frequency [23], [24]. An expression that quantifies the transfer function of a phase noise is Leeson's equation.

$$\left|\frac{Y(j\omega)}{X(j\omega)}\right|^2 = \frac{1}{4Q^2}\left(\frac{\omega_o}{\Delta\omega_o}\right)^2 \quad (2.21)$$

Leeson's equation specifies that phase noise is inversely related to Q^2 of the tank and frequency deviation $\Delta\omega_o$. Phase noise is quantified as the noise power in unit bandwidth at an offset frequency (typically 100 kHz or 1 MHz depending on the carrier frequency) from the carrier divided by the carrier frequency expressed in dBc/Hz.

2.6.6.2 Tuning range

Tuning range of a VCO is the range of VCO's output frequency that can capture a carrier frequency. Tuning range is directly related to VCO's gain K_{VCO}. With higher values of K_{VCO} larger tuning range could be achieved. There are several authors who have studied the relationship between K_{VCO} and phase noise [30], [31], [32]. From (2.18 and 2.19) it is evident that large K_{VCO} tends to up convert the tail current noise into amplitude modulation (AM) at the output of the oscillator. The presence of a varactor converts this change in amplitude into frequency and results in phase noise [23]. Many authors recommend 20 % of carrier frequency as tuning range as a good compromise with phase noise. However the low values of tuning range needs to be compensated for wide bandwidth applications. A digitally switched capacitor or inductor bank is used for this purpose [33].

2.6.7 FOM

To make realistic comparison between different designs various authors use a common FOM [25].

$$FOM = L\{\Delta f\} - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) \quad (2.22)$$

where $L\{\Delta f\}$ is the measured phase noise at the frequency offset from the carrier f_o. FOM ranging from -170 dB to -194 dB are reported by various authors [34], [35].

2.7 EFFECT OF TEMPERATURE VARIATION ON VCO'S PERFORMANCE

A generalised schematic of a negative g_m oscillator is given in Fig. 2.10. The parasitic are represented by R_L and R_C of inductor and capacitors respectively. The natural resonant frequency of the resonator is

$$\omega_o = \sqrt{1/LC} \tag{2.23a}$$

the self-oscillation frequency of an LC oscillator varies in a predictable manner due to variations in temperature and bias conditions [12] and [36]. A schematic of generalised LC oscillator is depicted in Fig. 2.10 [36].

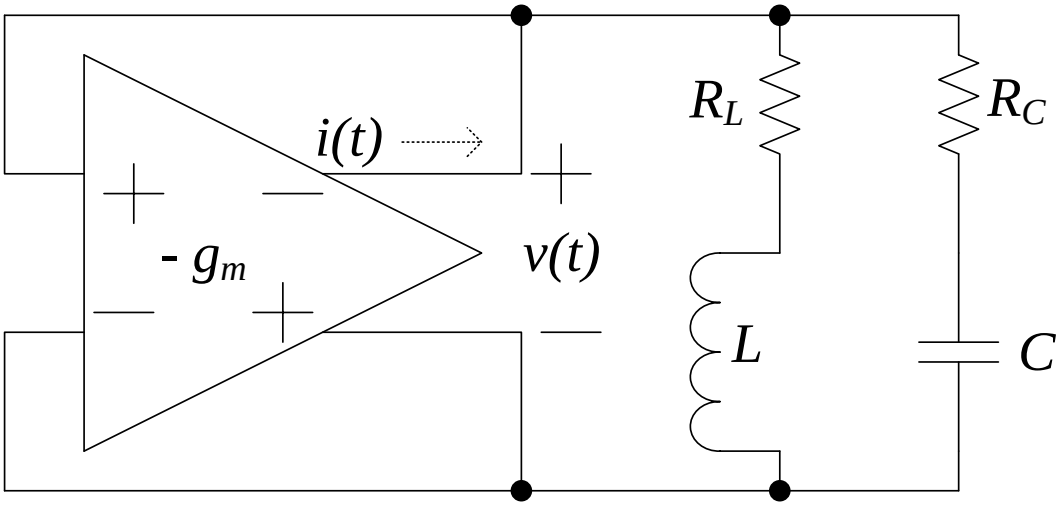


Figure 2.10 A generalised schematic of a *negative* g_m LC oscillator [36] (© [2007], IEEE)

By considering Fig. 2.10 the actual oscillation frequency depends on the sustaining transconductance amplifier which is required to overcome the loss in the tank. Therefore the oscillation frequency is modified as in (2.23b).

$$\omega_1 = \omega_0 \sqrt{\frac{L - CR_L^2}{L - CR_C^2}} \tag{2.23b}$$

assuming loss in the integrated capacitor is negligible compared to that of integrated inductor, the oscillation frequency could be modified as

$$\omega_1 \approx \omega_o \sqrt{1 - \frac{CR_L^2}{L}} \tag{2.24}$$

As per the discussion in section 2.3 where R_L demonstrates a positive TC, it is evident that an *LC* oscillator demonstrates a linear negative TC.

Furthermore in a VCO an increment in tail current, a power supply spike, or change in temperature leads to an injection of a current *i(t)* with high harmonic content into the tank. The capacitor absorbs most of this current as an inductor cannot respond instantaneously.

These consequently create a harmonic work imbalance in the *LC* network and reconciled by reducing the frequency of oscillation. Equation (2.25) enables the prediction of self-oscillation frequency as a function of bias conditions [12], [36].

$$\omega = \omega_1 \left(1 - \frac{1}{2Q^2} \sum_{n=2}^{\infty} \frac{n^2}{n^2-1} h_{i(n)}^2\right) \tag{2.25}$$

where,

$$Q = \omega_o L/(R_L + R_C),$$

and

$$h_{i(n)} = I_n/I_1$$

where I_n is the n^{th} Fourier coefficient of *i(t)*.

Change in oscillation amplitude causes additional harmonic distortion in the tank as higher harmonics easily pass through the lower impedance of the tank capacitance causing an imbalance in reactive power in the tank [37], [38]. The tank circuit responds to this by altering the phase, any change in phase is compensated by changing the frequency and cause a frequency drift in the VCO output. The approximate equations (2.24), and (2.25) confirm the argument that any positive increment in tail current results in reduction of the oscillation frequency.

From (2.23a) the effective inductance and the capacitance of the tank primarily determine the oscillation frequency. The current that passes through the inductor causes an image current in the substrate. This image current in the substrate reduces the effective inductance. As the temperature increased, the substrate resistance increases. This increment in resistance reduces the image current and increases the effective inductance. In a spiral inductor, conductors are placed in close proximity to one another. Currents each segment could induce eddy currents in other segments and cause series resistance to increase [39]. This phenomenon causes further reduction in frequency according to equation (2.24). Another effect of increasing temperature is reduction in the *Q* of the circuit as mentioned in section 2.3. But the effective capacitance constitutes of the capacitance of the resonator as well as parasitic contributions from all reverse biased

junctions shunting the inductor. The capacitance of the resonator displays a lower temperature dependency.

From this discussion it can be concluded that in an *LC* oscillator frequency drift originate through modulation of:

a) net tank inductance *L*, or capacitance *C* from (2.23a)

b) net loss in tank inductance R_L or capacitance R_C from (2.24)

c) the harmonic content of bias current *i(t)* from (2.24, 2.25).

2.8 TEMPERATURE COMPENSATION

A low voltage VCO is extremely sensitive to PVT due to small overdrive voltages utilised [40]. As the mechanisms of frequency drift in an oscillator are clearly identified in section 2.7, various temperature compensation strategies that are successfully implemented by various authors are explored and critically evaluated in this section.

2.8.1 Temperature insensitive biasing

Temperature insensitive biasing may be achieved by finding a weighted sum of two sources, one that has a positive TC and the other with a negative TC [22], [41]. A conceptual implementation of a voltage source with reduced TC shown in Fig. 2.11 [19].

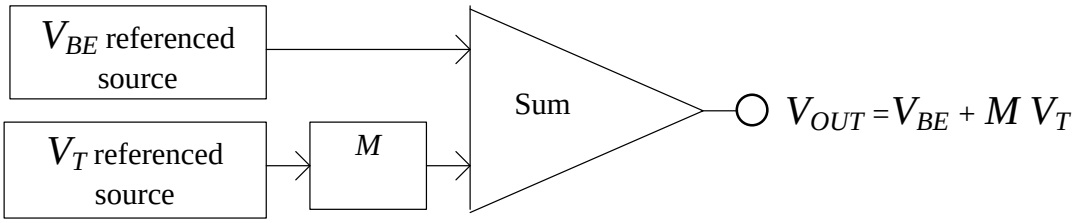


Figure 2.11 Block diagram representation of temperature insensitive biasing circuit using V_{BE} and V_T sources [19] (© [2010], with permission from John Wiley & Sons, Inc.)

V_{BE} referenced source demonstrated about -2 mV/ºC variation with temperature while V_T source with 85 µV/ºC [19]. A temperature insensitive voltage source with a zero temperature coefficient could be built by adjusting the value of *M*.

Scaling current of a BJT is given by

$$I_s = \frac{qAD_n}{W_B N_A} e^{\frac{E_g}{kT}} \tag{2.26}$$

re-arranging (2.26) with the use of Einstein's relation yields:

$$\mu_n = \left(kq/_T\right) D_n,$$

$$\overline{\mu_n} = CT^{-n}$$

and

$$e^{\frac{E_g}{kT}} = DT^3 e^{\left(-\frac{E_g}{V_T}\right)}$$

therefore

$$V_{BE} = V_T \ln(I_1 T^{-\gamma} E e^{\frac{E_g}{V_T}}) \tag{2.27}$$

γ=4-n

where

$$I_1 = GT^{\alpha} \tag{2.28}$$

therefore

$$V_{BEon} = E_g - V_T[\gamma - \alpha] \ln(T) - \ln EG \tag{2.29}$$

and from Fig. 2.12

$$V_o = V_{BE} + MV_T \tag{2.30}$$

substituting (2.29) in to (2.30) gives

$$V_o = E_g - V_T[\gamma - \alpha] \ln(T) + V_T[M + \ln(EG)] \tag{2.31}$$

finding the derivative of (2.31) and equating to zero yields

$$[M + \ln(EG)] = (\gamma - \alpha) \ln(T_0) + (\gamma - \alpha) \tag{2.32}$$

by substituting (2.32) into (2.31) yields

$$V_o = E_g + V_T(\gamma - \alpha)\left(1 + \ln\frac{T0}{T}\right) \tag{2.33}$$

differentiating (2.37) with reference to temperature yields

$$\frac{dVo}{dT} = (\gamma - \alpha)\frac{V_T}{T}\left(\ln\frac{T0}{T}\right) \tag{2.34}$$

equation (2.34) shows the temperature coefficient becomes zero when $T_0 = T$. Most often a VCO is operated over a range of temperatures. Therefore it would be useful to have a broader effective temperature coefficient term.

$$TC_{eff} = \frac{1}{Vo}\left(\frac{V_{max} - V_{min}}{T_{max} - T_{min}}\right)$$

There are several low TC voltage and current reference circuits implemented successfully [1], [2], [41], [42].

2.8.2 Adaptive body bias (ABB)

The negative resistance required to maintain oscillations varies a lot over the frequency range, causing the eventual frequency drift [25]. Another form of on-chip variability arises from changes in process parameters [43]. This occurs due to proximity effects in photolithography, non-uniform conditions during deposition and random dopant concentrations. This change in process parameters alters channel length, width, oxide thickness and dopant concentrations [44].

From (2.13) and subsequent discussion it is evident that designers are frequently drawn towards designing the oscillator to function under the worst case condition and providing the transistors with higher transconductance than minimum required to sustain oscillations. This leads to higher power consumption than desired, but offers effective immunity against PVT variations.

In order to provide robustness against PVT variations and also to reduce power consumption many authors propose ABB technique [40], [45], [46]. The following explanations and Fig. 2.12 are from [40], [44], [47].

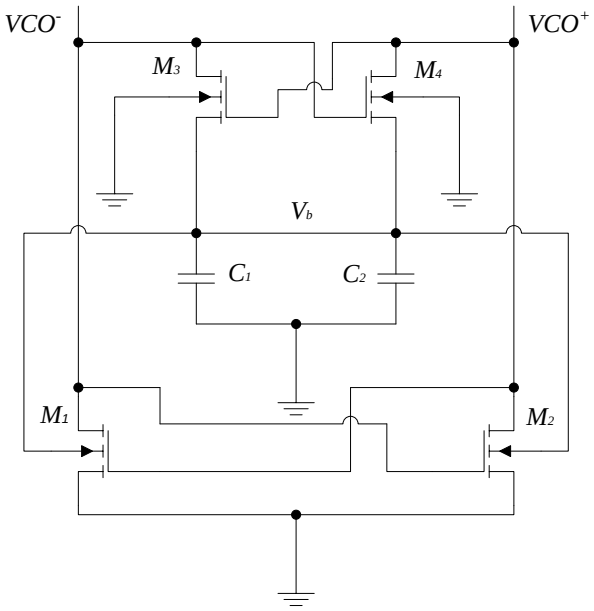


Figure 2.12 Block diagram representation of ABB [40] (© [2009], IEEE)

In Fig. 2.12, the two peak detectors identify negative peak of the sinusoidal waveforms across C_1 and C_2. There are no oscillations at start up and very low voltage is applied to the body of cross coupled transistors. This keeps the V_t of M_1 and M_2 low and thereby producing high values of transconductance. As the oscillations begin and increase in amplitude, V_b becomes more negative; this body bias will increase the V_t of M_1 and M_2 and the transconductance is reduced. In this way the sensitivity of transconductance of the cross-coupled pair to PVT variation is reduced, and also reduces power consumption.

Slightly modified version of ABB is reported in [48], where a negative peak detector output is smoothened using a low pass filter before using as body bias for transistors for improved performance in class C VCOs.

2.8.3 Automatic amplitude control (AAC)

To keep the phase noise minimum it is required to keep the oscillation amplitude high. However; once the oscillation amplitude exceeds V_t of M_1 and M_2 in Fig. 2.12, each transistor enters into the triode region and effectively reduces the Q of the tank drastically. The degradation of tank Q generates higher order harmonics and up-converts flicker noise

of the current source and compromises the phase noise performance [37], [38]. Fig. 2.13 illustrates the voltage swing at the drain of M_1 and M_2 [40].

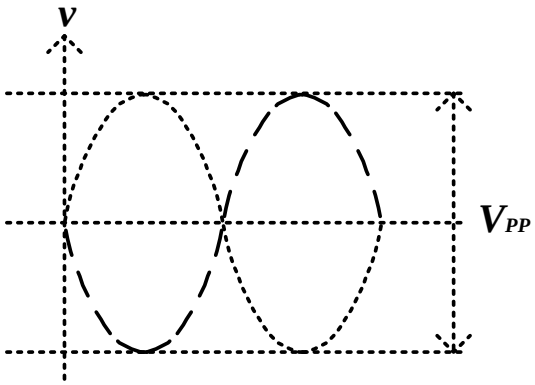


Figure 2.13 VCO voltage swing at the drains of M_1 and M_2 [40] (© [2009], IEEE)

The condition for saturation for M_1 can be deduced using figures 2.12 and 2.13

$$V_{GS(M1)} - V_{DS(M1)} \leq V_t \tag{2.35}$$

therefore the optimum oscillation amplitude for best phase noise performance is

$$V_{PP} \leq V_t \tag{2.36}$$

In order to maintain the oscillation amplitude at the optimal level, an AAC circuit may be used [8], [11], [16]. A block diagram of AAC is provided in Fig. 2.14.

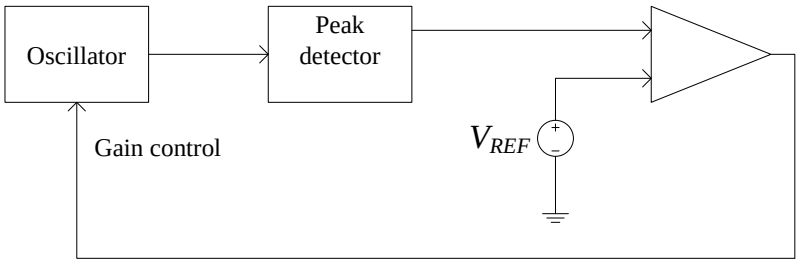


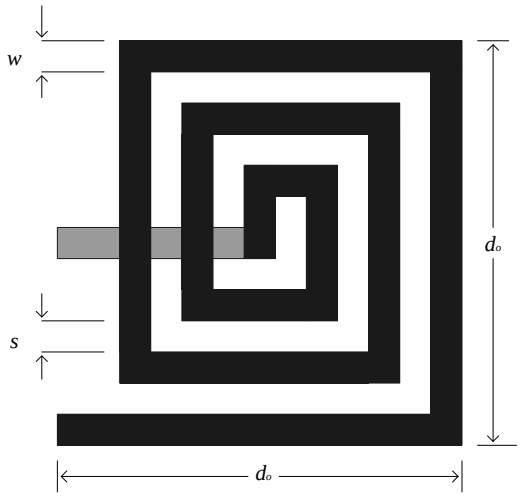
Figure 2.14 Block diagram of an AAC [11] (© [2007], IEEE)

In Fig. 2.14, at start-up there are no oscillations; the peak detector output level will be small and gain control will not be activated. As the oscillator picks up its amplitude, peak detector output exceeds a pre-determined level V_{REF}, the gain of the amplifier will be reduced, keeping the oscillator output at a constant level.

2.9 MONOLITHIC INDUCTORS

With growing demand for completely integrated radio communication systems, the CMOS technology has evolved to allow the fabrication of integrated inductors on the same substrate as the rest of the RF circuit. This will preclude the need for external connections and thus reduce electrical and magnetic coupling and parasitic inductance and capacitance due to connection wires [40]. Apart from the self-resonant frequency the important parameters of interest are its *Q* factor and the area consumed by the inductor on silicon substrate [23]. The *Q* factor of an inductor is limited by several factors such as resistive losses in the spiral coil and substrate losses [39]. Inductances could be implemented in different methods; multi-layer spiral inductors known as microelectromechanical (MEMS) inductors, bond wire or using microstrip lines. Very high *Q* values could be achieved using MEMS and microstrip inductors and are expensive to manufacture. Given that the primary intention of this dissertation does not demand very high *Q* values, only spiral inductors are considered.

Multi-layer silicon technology allows fabrication of a spiral inductor. The physical structure of a spiral inductor is defined by number of turns (*n*), the width of the wire (*w*), the space (*s*) and the total area (d_o^2) as shown in Fig. 2.15 [39]. At RF modelling a spiral inductor is complex due to the presence of Eddy currents in the interconnect and substrate loss in the silicon [8] and [39].



a

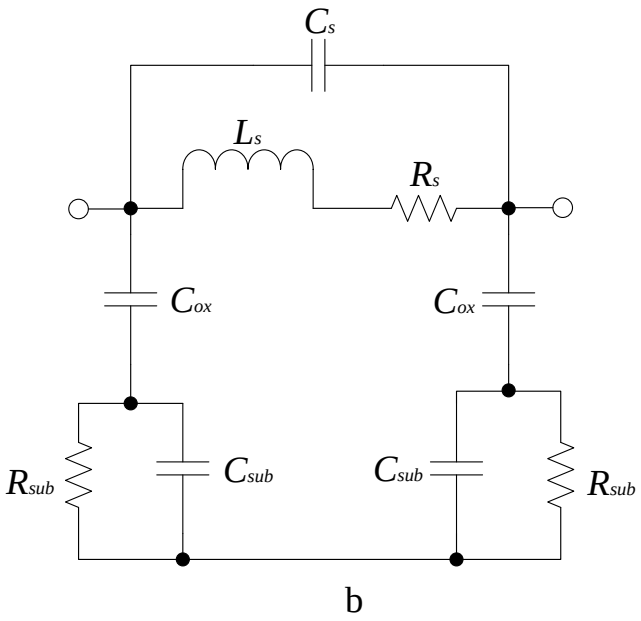


Figure 2.15 a. A three turn spiral inductor structure, b. Lumped physical model of a spiral inductor on silicon [49] (© [1998], IEEE)

2.9.1 Series inductance L_s

From Fig. 2.15b the series inductance L_s represents the inductance of the spiral and the underpass. This term is constituted by self-inductance and mutual inductance between two adjacent wires. The self-inductance (L) and mutual inductance (M) are related as

$$M = k\sqrt{L_1 L_2} \tag{2.37}$$

where k is the coefficient of coupling.

Self-inductance could be calculated as follows;

$$L_{self} = 2l\left[\ln\left(\frac{2l}{w+t}\right) + 0.5 + \frac{(w+t)}{3l}\right] \tag{2.38}$$

where L_{self} is the self-inductance in nH, l is the wire length in cm, w is the width in cm, t is the thickness in cm.

The mutual inductance between two parallel wires could be calculated as follows

$$M = 2lM' \tag{2.39}$$

where M is in nH and M' is the mutual inductance parameter that can be found by

$$M' = \ln\left[\frac{l}{GMD} + \sqrt{1 + \left(\frac{l}{GMD}\right)^2}\right] - \left[\sqrt{1 + \left(\frac{GMD}{l}\right)^2} + \frac{GMD}{l}\right] \quad (2.40)$$

Here *GMD* denotes the geometrical mean distance between wires in cm.

2.9.2 Series resistance R_s

At DC, the current density is uniform across the cross section of a wire. At RF eddy currents are generated within the conductor by the time varying magnetic field around the wire. This eddy current opposes the flow of the current that caused the magnetic field according to Lenz's Law and cause non uniform current density in its cross-section. This non uniform current density known as skin effect will increase the AC resistance.

To quantify the total effect of eddy currents in a conductor a critical parameter called skin depth (δ) is introduced. Skin depth describes the degree of penetration by the electric current and magnetic flux into the surface of the conductor at high frequencies [39].

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}$$

where ρ, μ and f represents resistivity in Ω-m, permeability in H/m and frequency in Hz respectively. In Fig. 2.15b, the series resistance R_s denotes the energy losses due to skin effect and proximity effects at RF in the spiral structure [39].

$$R_s = \frac{\rho l}{w t_{eff}} \quad (2.41)$$

$$t_{eff} = \delta\left(1 - e^{-t/\delta}\right)$$

where, δ is the skin depth due to skin effect, t is the physical thickness of the wire and both measured in meters.

2.9.3 Series capacitance C_s

The capacitance between two adjacent turns is negligible due to very little potential difference between them [32], [39]. However there is larger potential difference between spiral and the underpass. Capacitance C_s symbolises the parasitic capacitance between outer and inner terminals of the spiral inductor and is due to overlap between spiral and the

centre-tap underpass [32]. Presence of this capacitance permits signal current flow directly from one end of the terminal to the other bypassing the spiral.

$$C_s = nw^2 \frac{\epsilon_{ox}}{t_{oxM1-M2}} \tag{2.42}$$

2.9.4 Substrate parasitic

The capacitance between spiral and the substrate is modelled by C_{ox} the oxide capacitance, C_{sub} the substrate capacitance where R_{sub} models resistance of the substrate originate from the majority carrier concentration. Due to the physical size of the inductor on the silicon die, the lateral dimensions are much larger than oxide thickness. Therefore substrate capacitances and resistances are directly proportional to area of the inductor [39]. Hence the following estimations are made:

$$C_{ox} = \frac{1}{2} lw \frac{\epsilon_{ox}}{t_{ox}} \tag{2.43}$$

$$C_{sub} = \frac{1}{2} lwC'_{sub} \tag{2.44}$$

$$R_{sub} = \frac{2}{lwG'_{sub}} \tag{2.45}$$

where, C'_{sub} and G'_{sub} are the capacitance and conductance per unit area of the silicon substrate.

2.10 CONCLUSION

Effect of temperature variation on semiconductor devices were investigated. It was re-capped that the threshold voltage of a MOS device and V_{BE} of bipolar devices reduces with temperature while the thermal voltage V_T of a bipolar device displayed positive increment with temperature. A negative increment in V_t causes increased transconductance in the VCO core that results in higher oscillation amplitude. It was also established that any increment in oscillation amplitude translated into negative shift in frequency.

The frequency drift mechanism in an LC oscillator was investigated and identified three major causes. These are modulation of the net tank inductance or the net tank capacitance, net losses in the inductor and capacitor and the harmonic current *i(t)* that is generated in the

tank due to change in supply voltage or temperature. Therefore in order to mitigate the frequency shift of a VCO the following techniques were proposed:

1. All active devices were to be biased at ZTC point to reduce the temperature dependency.
2. A current source with a negative TC is chosen for tail current supply as the negative TC of the source tend to reduce the increment in tranconductance available to the VCO core as the temperature is increased.
3. An ABB circuit to reduce the sensitivity to PVT variation by modulating the threshold voltage of the transistor.
4. An AAC circuit to keep the oscillation amplitude at an optimal level.

The tail current source with negative TC could effectively compensate for the increased transconductance in the VCO core as the temperature is increased. As MOS devices exhibit a ZTC bias point, reduced temperature sensitivity could be achieved if all active devices were biased at ZTC point. The ABB circuit effectively modulates the V_t of the -g_m stages to compensate for PVT variations. The AAC loop maintains an optimal amplitude thereby preventing amplitude to frequency conversion and also provides negative feedback that stabilises the ZTC bias point.

As the temperature compensation strategies are identified here the dissertation continues to research methodology in Chapter 3.

CHAPTER 3 RESEARCH METHODOLOGY

3.1 INTRODUCTION

The causes of frequency divergence of a VCO when temperature is varied were identified in Chapter 2. Different compensation strategies were discussed and a number of reparation procedures were also identified in section 2.8. Chapter 2 concluded with a set of four procedures to achieve temperature compensation in a VCO.

Chapter 3 describes the research methodology used to collect the data to substantiate the hypothesis that was defined in Chapter 1. This chapter is intended to build on the introductory methodology mentioned in section 1.4 and to provide an assurance that appropriate procedures were followed. The rest of the chapter is organised as follows: research methodology framework, justification for chosen design methodology, the limitations of the said methodology, computer aided design (CAD) tools used, integrated circuit (IC) manufacturing and measurement setup as well as the conclusion.

3.2 RESEARCH METHODOLOGY FRAMEWORK

Two important methodology phases were followed in this dissertation. During the first phase, a literature survey was performed to reveal the causes of temperature dependency in an integrated VCO. A number of compensation techniques were chosen and were discussed in Chapter 2. To validate the hypothesis an appropriate design was created and simulated utilising Cadence Virtuoso [50] that use simulation program for integrated circuit emphasis (SPICE) as the backend. Simulation results are presented in Chapters 5. The sequence of events that constitutes the research methodology used in this dissertation is provided as a block diagram in Fig. 3.1.

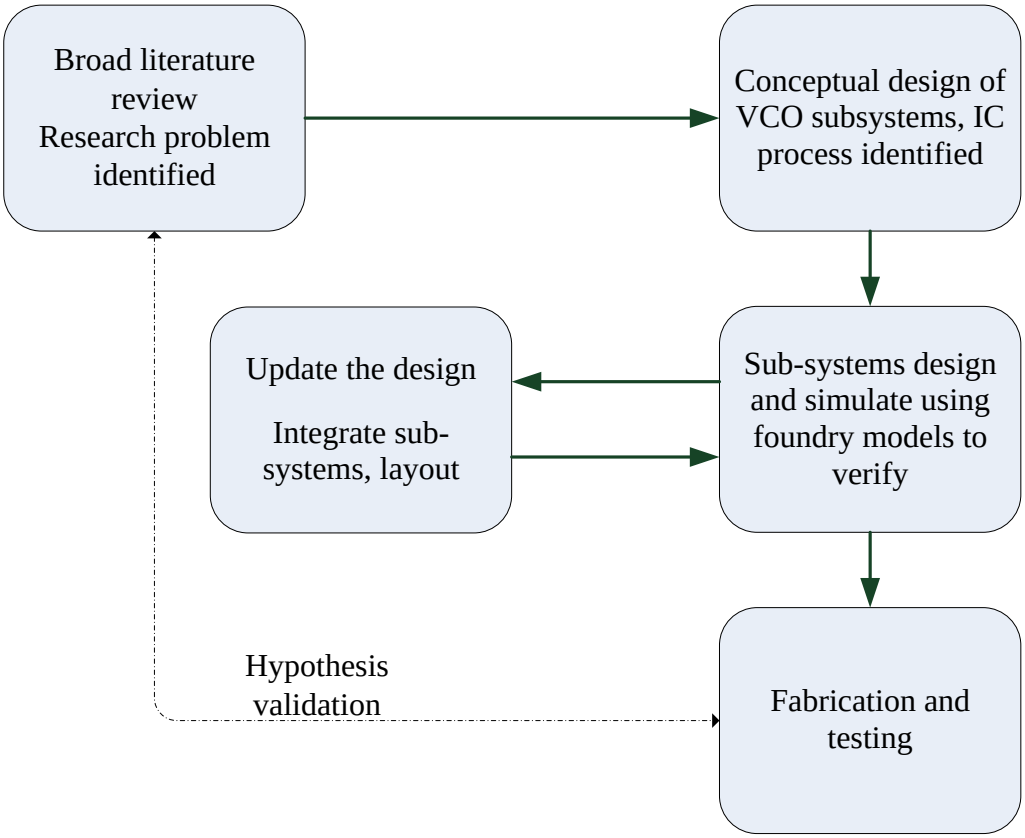


Figure 3.1 Block diagram of research methodology pursued

As shown in Fig. 3.1, in the second phase of the methodology an appropriate layout was created from the design and a design rule check (DRC), and layout versus schematic (LVS) check were performed to prevent violations of rules set by the foundry. This temperature compensated VCO was realised using a 0.35 µm CMOS technology from ams AG. The prototyped IC was then mounted on a PCB and subjected to different temperature and the frequency drift is measured to further verify the hypothesis.

3.3 JUSTIFICATION FOR THE METHODOLOGY

Chapter 2 described the research problem of frequency drift in the VCO as a result of temperature variation as well as diverse possible reparation methods. The independent variable in this research is temperature, the dependent variables being the threshold voltage of semiconductors, non-zero TC of passive components, tail DC drift and their combined contribution to VCO output frequency deviation.

A feasible way of verifying the hypothesis is to realise the system in the corresponding technology node and to carry out practical measurements using accurately calibrated equipment. In this dissertation 0.35 µm BiCMOS process technology and models provided by the foundry were made use of [51]. As a verification tool all the designs are simulated in Cadence Virtuoso, using the models supplied by the foundry. Spectrum analyser (Rohde & Schwarz, FSP3) at the University of Pretoria and associated labs were used for subsequent RF measurements.

3.4 LIMITATIONS OF METHODOLOGY

The methodology adopted was based on the assumption that the only independent variable was temperature. Process variations, caused mainly by changes in gate oxide thickness (t_{ox}) and doping concentration, could alter the threshold voltage and mobility of the MOS transistor [11]. Therefore the VCO oscillation frequency may shift with the process even if the system is compensated for temperature. Another possible cause for frequency drift is supply voltage variation.

3.4.1 Process variations

Process variations could cause inter-die variations that produce a dispersion of values of transistor parameters and passives from expected values [44], [47]. However, all the devices in the same chip suffer from similar variations. The intra-die variations are usually solved by careful layout techniques and proper sizing of the paired devices [47]. Therefore it could be concluded that the process variation was actually an independent variable, but nonetheless well-controlled for this research, as chips from the same die were used for final measurements.

3.4.2 Supply voltage variations

Discussions in section 2.7 revealed that a voltage supply fluctuation could cause frequency dispersion in a VCO. In order to mitigate this possible cause of frequency shift, an appropriately regulated voltage supply (Escort EPS-3250) was used during the measurement phase of this dissertation.

3.5 CAD TOOLS

As the first phase of verifying the hypothesis, the design was simulated in Cadence Virtuoso. This software package was used for drawing schematic layout as well as for simulations. It makes use of the power of hierarchical design, by making use of component reuse. The individual packages that are used in the Cadence Virtuoso platform are now explained briefly.

3.5.1 Virtuoso schematic editor

The Virtuoso schematic editor allows the user an interface with SPICE. Any design that is drawn in this editor is converted into a text file that describes the interconnection of all the ports in the design. It is also supplied with a well-defined component library and permits hierarchical design.

3.5.2 Virtuoso Analog Design Environment

The Virtuoso Analog Design Environment family of products features a simulator-independent environment for graphical user interface, distribution of multiple simulations, integrated waveform display and interface with popular third party SPICE simulators by creating netlists from the schematics [50].

3.5.3 Virtuoso Multi-Mode Simulation

Virtuoso Multi-Mode Simulation combines three powerful simulation engines, namely Ultrasim, Spectre and Virtuoso Accelerated Parallel Simulator.

The Virtuoso Spectre Circuit simulator is capable of accurate SPICE-level simulation for analogue, mixed signal and RF circuits. Virtuoso Accelerated Parallel Simulator is a scalable RF and mixed signal simulator that can accommodate millions of transistors, passive components and parasitic elements. The Virtuoso Ultrasim Full-Chip simulator is FastSPICE based for pre-layout and post-layout verification of blocks to full-chip. These simulators permit several different analyses, with different degrees of power and convenience. For example, Spectre L permits the following analysis:

DC, AC and time-domain analysis, noise, transfer function and sensitivity analysis, transient noise analysis, Monte Carlo and parametric statistical support and parameter sweep.

3.5.4 Virtuoso layout suite

In order to prototype the design the foundry requires a layout of the verified schematic. The Virtuoso layout suite permits the designer to create an accurate layout of analogue or mixed signal design. It also provides a real-time design rule check that enforces the design rule set by the foundry.

3.6 IC PROTOTYPING

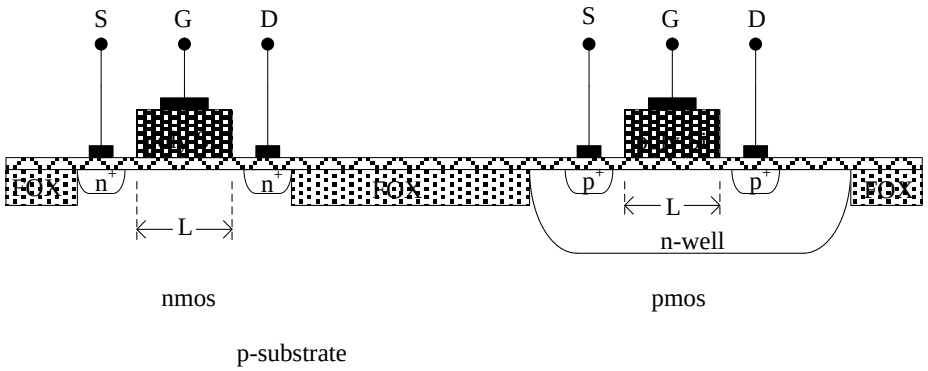
After the design was tested by the CAD tools, it was prototyped from the foundry ams AG and measurements were performed to validate the hypothesis. Hence the validity of the various components and sub-circuits needs to be characterised at RF for a rational result. Geometrical and electrical parameters that control the fabrication process are provided by the foundry ams AG. These information are bound by the non-disclosure agreement signed by the author and university with the foundry.

3.6.1 Technology

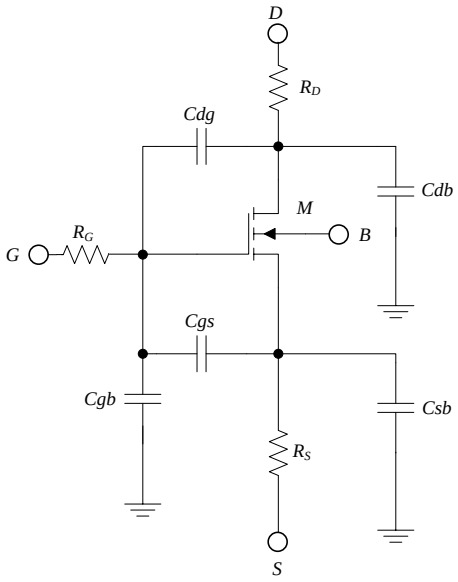
To verify the hypothesis the designed VCO at 2.4 GHz needs to operated at a range of temperatures from 0 °C to 125 °C. Therefore the technology selected for this study is S35M4D5 from ams AG, for the following reasons: BiCMOS technology that allows HBTs as well as CMOS devices, all devices are characterised from a few kHz up to several GHz, and are valid in the required temperature ranges [51]. Due to a non-disclosure agreement (NDA) between the author and the foundry through the University of Pretoria, certain process parameters have been excluded from this dissertation.

3.6.2 NMOS/PMOS models (`modnrf/modprf`)

Berkely short-channel IGFET model (BSIM3v3) model is used to characterise the MOS devices. A cross sectional view of the NMOS and PMOS transistors are depicted in Fig. 3.2.



a



b

Figure 3.2 a. Cross-sectional view of NMOS and PMOS transistors (bulk connection not shown) [22] (© [2005], with permission from Wiley-Interscience), b. Sub-circuit model of an NMOS at RF [23] (© [2009], with permission from Cambridge University Press)

In Fig. 3.2 the following legend is used.

R_G is the gate resistance, R_D is the drain resistance, R_S is the source resistance,

NMOS is the intrinsic NMOS transistor modelled by BSIM3v3.1,

C_{gd}, C_{gs} are the gate drain, and gate source capacitances respectively,

C_{gb}, C_{db}, C_{sb} are the junction capacitances between gate, drain, source respectively with bulk.

3.6.3 MOS worst case models

In addition to typical mean (TM) models, four worst case parameters sets are made available by ams AG.

WP – worst case power – fast NMOS fast PMOS

WS – worst case speed – slow NMOS slow PMOS

WO – worst case one – fast NMOS slow PMOS

WZ – worst case zero – slow NMOS fast PMOS

3.6.4 Bipolar transistor model

There are three different types of bipolar transistors available: a parasitic vertical bipolar transistor , a lateral bipolar transistor model and HBT.

A cross-sectional view of an HBT is furnished in Fig 3.3. HBTs make use of an *n*+ poly-Si as emitter, a SiGe base layer and a buried *n*+ region as collector. A vertical bipolar inter-company (VBIC) model is supplied by ams AG. A cross sectional view is furnished in Fig. 3.3 [21].

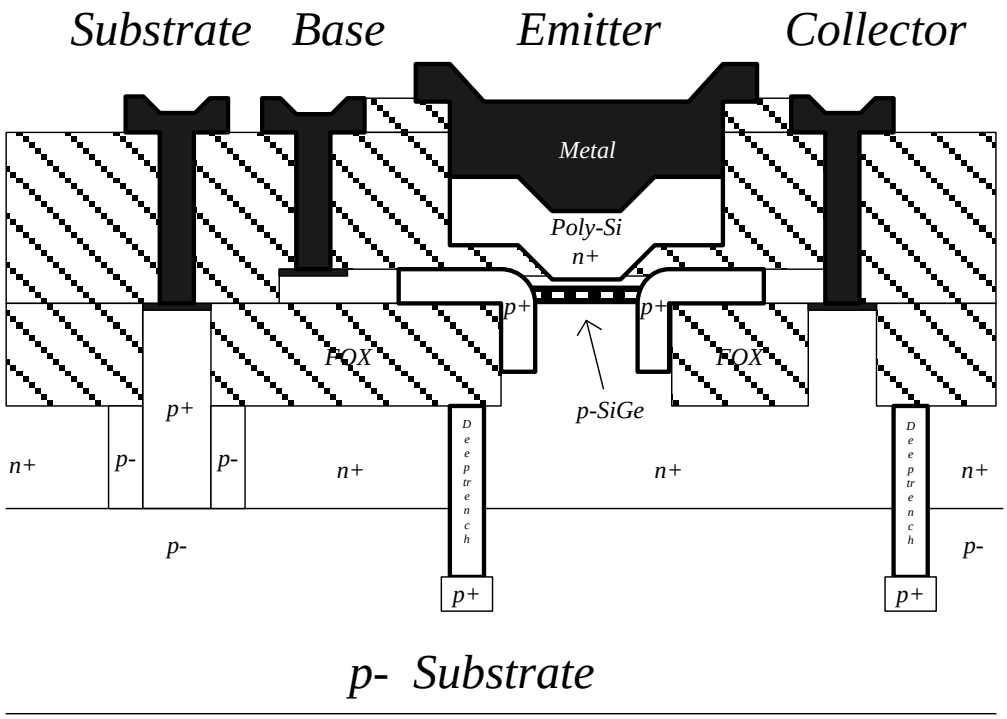


Figure 3.3 Cross-sectional view of an npn single collector single base (`npn111`) HBT [21] (© [2002], Artech House Inc.)

The nomenclature used in Fig. 3.3 displays the number of collector, base and emitter terminals; therefore `npn121` has a single collector, two bases and single emitter terminals. Worst case tolerances with respect to the main parameters are supplied by the foundry for the following pre-defined worst cases.

HS – high speed and high beta

LB – low speed and low beta

HB – low speed and high beta

3.6.5 MOS varactor (`cvar`)

A varactor is implemented using an accumulation mode PMOS capacitor. BSIM3v3.2 model includes the gate-bulk capacitance voltage. As shown in Fig. 3.4, these MOS capacitors are laid out in a series of rows and columns which are connected in parallel to achieve the required amount of capacitance. This layout also increases the *Q* factor. This

model scales proportionally with device width. Hence capacitance could be adjusted by setting the number of columns and rows in the layout.

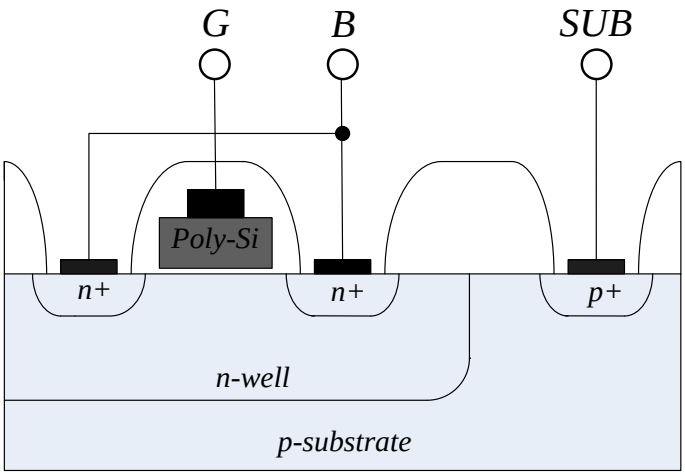


Figure 3.4 Accumulation mode PMOS varactor cross-section [23] (© [2009], with permission from Cambridge University Press)

As in Fig. 3.4, MOS varactors are used in reverse bias conditions: the models are validated for wide temperature ranges (see the NDA note – Section 3.6.1).

3.6.6 On-chip capacitors

There are two forms parallel plate capacitors possible within a chip namely `poly1-poly2` capacitor and the metal-insulator-metal capacitors. `CMIM` capacitors make use of two different metal layers. A cross-sectional view of `poly1-poly2` capacitor and a general equivalent model displaying the parasitics are illustrated in Fig. 3.5. High values of *Q* are possible with this type of implementation.

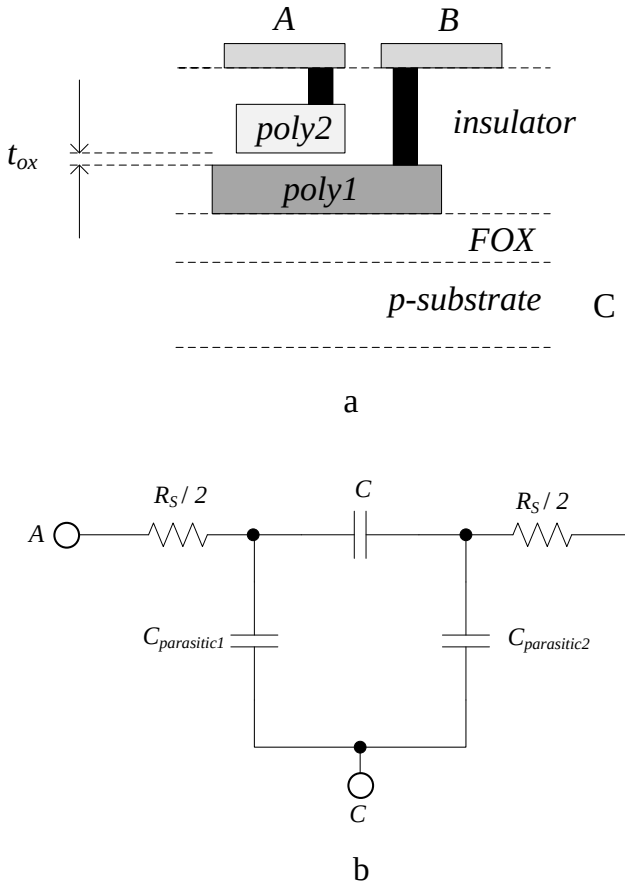


Figure 3.5 `Poly-poly` capacitor, a. cross-sectional view [22], b. equivalent model at RF (© [2005], with permission from Wiley-Interscience)

where C is the series capacitance,

R_s is the series resistance,

$C_{parasitic}$ are the substrate parasitic capacitance from plate 1 and 2.

3.7 SYSTEM DESIGN

Section 2.10 concluded with a combination of four schemes to make the VCO less sensitive to temperature. The use of ABB together with AAC is reconsidered as the operation of the former and latter are not mutually exclusive. ABB circuit modulates the V_t of the transistor as a function of oscillation amplitude. Once the oscillation amplitude picked up, ABB circuit is still responds to change in amplitude. With AAC present in the

system, such that change in oscillation amplitude is compensated in transconductance and an equilibrium state is established. Any further modification of V_t by the ABB circuit will alter the equilibrium state and reduce the effectiveness of the compensation circuitry. Therefore it was decided not to use ABB circuit.

The second change in approach was in the implementation of a current source with a negative TC to supply the VCO. The error voltage produced by the error amplifier must be used to control the current supply. This would in effect lead to modifying the current source, and would lose out on voltage headroom. As a design trade-off it was decided to replace the current source with a series control transistor whose conductivity was made proportional to the error voltage generated. An NMOS transistor is used as the series control element M_{CNTRL}, and to prevent the latch up situation when switched on, the AAC output V^+ is kept higher than V^-. From Fig. 3.6 it is also evident that the differential input to OTA, V_{ID} = (V^+-V^-) directly affect the amount of amplitude control possible. Accordingly, a higher-level block diagram is presented in Fig. 3.6.

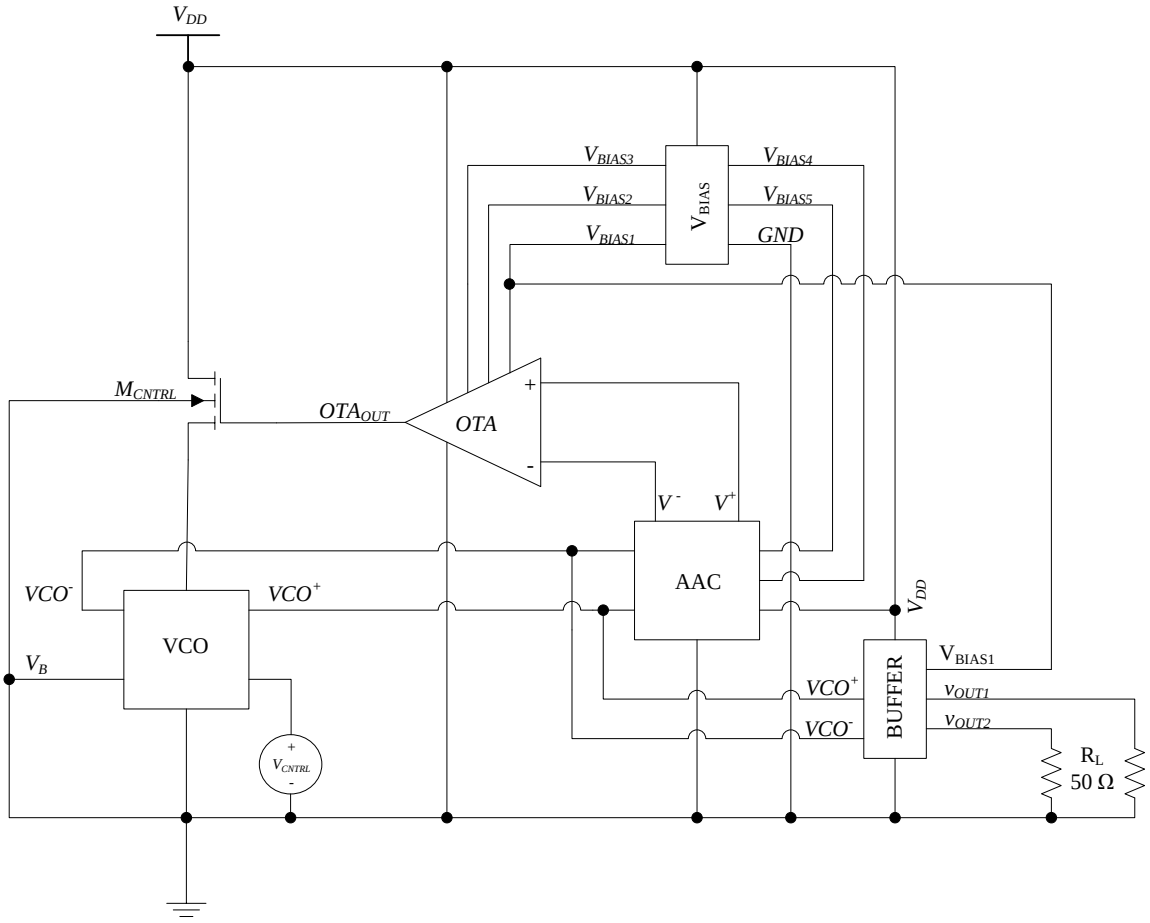


Figure 3.6 Block diagram of the Temperature Compensated VCO

In Fig. 3.6 V_{CNTRL} is the external DC input, while v_{OUT1} and v_{OUT2} are the two outputs. The buffer permits the transfer of RF energy to the external 50 Ω impedance.

3.8 MEASUREMENT SETUP

The prototyped IC received back from the foundry was mounted on a PCB to facilitate various measurements. The output frequency as a function of V_{CNTRL} and as a function of temperature are two significant parameters to be measured. Hence the device under test was kept in a temperature controlled chamber while measurements were performed. Measurement setup is illustrated in Fig. 3.7.

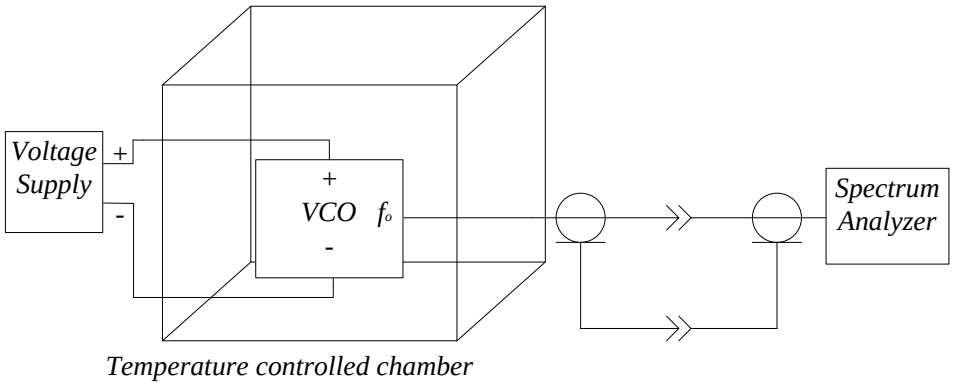


Figure 3.7 Measurement setup

As shown in Fig. 3.7, an external regulated supply is used to power the VCO. This ensured that supply voltage variation did not influence the device under test (VCO).

3.9 CONCLUSION

Chapter 3 described the procedures followed in this study to verify the hypothesis. The CAD tools used in the dissertation were briefly discussed – an assessment of their key capabilities as applicable to this study was presented. The RF SPICE model and process control parameters supplied by the foundry were examined, various process control parameters observed and the range of their validity checked. A distinction was made between process control parameters vs. information parameters supplied by the foundry. Measurement setup and various measurements and relevant units were identified.

Process and supply voltage variations were postulated as two independent variables that can be effectively controlled during the measurement phase of the research. The only dependent variable that could thus affect the result is the variation in the resistance (`rpoly`) with temperature. Fortunately, this variable is incorporated into the model supplied by the foundry, and hence considered as a controlled variable.

The next chapter presents the relevant design, simulation and layout pertaining to the hypothesis under evaluation.

CHAPTER 4 CIRCUIT DESIGN

4.1 INTRODUCTION

In order to substantiate the hypothesis defined in Chapter 1 of this dissertation, a temperature compensated VCO needs to be designed, fabricated in silicon wafer and tested. The process that followed in schematic design, layout design, various verification procedures that followed in preparation for fabrication are described in this chapter. There are five main subsystems to be devised, namely the oscillator, the AAC, the op-amp, bias voltages and finally the buffer.

The most important design considerations are explained, although exact calculation of each individual component is excluded because well-established expressions and principles are followed. Each of the designs generated were simulated thereafter at the typical mean parameters provided by the foundry ams AG using Cadence Virtuoso. Further worst case simulations were performed since the fabrication process offers non-ideal process variations. There are three process corners identified in the form of TM, WP, WS for transistors and capacitors. Further corners are identified for inductors in the form of ‘high *Q* factor’ (HQ), and ‘low *Q* factor’ (LQ). The complete list of process corners is found in Table 4.1.

Table 4.1 Process corners identified

Corner Name	CMOS	C	L
0	TM	TM	TM
1	WP	WP	HQ
2	WS	WP	HQ
3	WP	WS	HQ
4	WS	WS	HQ
5	WP	WP	LQ
6	WS	WP	LQ
7	WP	WS	LQ
8	WS	WS	LQ

The last four corners in Table 4.1 are expected to perform much worse in any RF design due to the low *Q* factor of the inductors. Suitable design adjustments are made to accommodate for worst case corners and are mentioned in Table 4.5.

The layout of the verified schematic is prepared and further layout versus schematic error checking was performed.

In analogue design, use of large overdrive voltage for transistors ensures faster circuits at the expense of power consumption. A transistor operated in weak inversion provides slower but power efficient circuit. However in micro powered circuits the best compromise between power consumption and speed is obtained when transistors operate in moderate inversion [52]. The ratio of transconductance to the drain current (transconductance efficiency) to ratio of drain current to transistor width, I_D/W (current density) is used as the main design parameter. A design procedure proposed by [53] is followed in this design of the oscillator and the operational transconductance amplifier (OTA).

4.2 THE OSCILLATOR

A differential cross coupled topology was adopted for the oscillator. The selection of the topology was defended in section 2.6.4. The ZTC bias point is selected for the design of the oscillator. A plot of this point against transistor current density, I_D/W is depicted in Fig. 4.1.

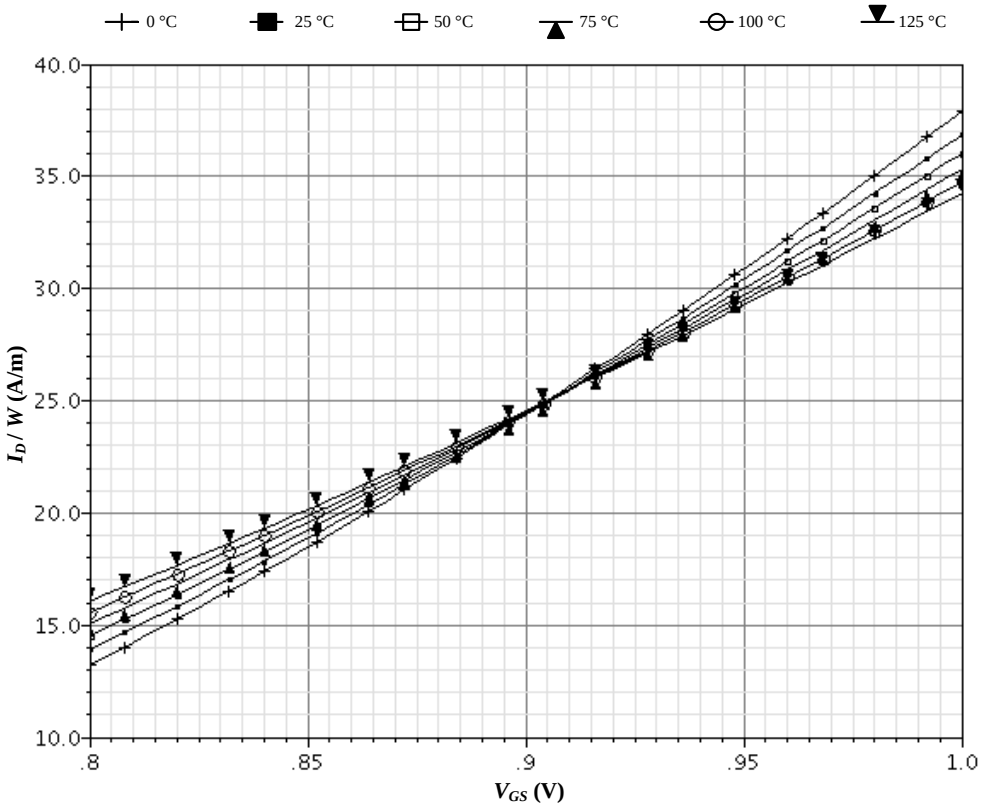


Figure 4.1 ZTC bias point plotted against transistor current density

In Fig. 4.1, the ZTC bias for NMOS transistors is observed when I_D/W = 25 and is chosen for this design of the oscillator.

4.2.1 The tank circuit

The inductors were chosen from the process design kit (PDK) provided by ams AG. A thick metal spiral inductor with L_s = 1.49 nH and a Q factor of 9.6 at 2.4 GHz were selected. The required value of capacitance is calculated. A `CMIM` capacitance with a Q > 100 is the obvious choice compared to `CPOLY` with a Q value close to 58.

Using 2.17a, 2.17b

$$R_{eff} = 9.6 \times 2\pi \times 2.4 \times 10^{9} \times 2 \times 1.49 \times 10^{-9} = 431.4\ \Omega$$

$$g_m \geq \frac{2}{431.4} = 4.636\ \text{mS}$$

g_m = 6 mS is selected to make the oscillations self-starting.

In order to assist in further design g_m/I_D vs. I_D/W plots are derived using Cadence Virtuoso employing Spectre Simulator. Transistors of minimum channel length are selected as they deliver better unity gain frequency (f_t). This argument is verified further in Fig. 4.9. All the simulations are performed using transistors of W = 10 µm and L = 0.35 µm. Transistors with different widths and lengths are found to be overlapping as reported in [52]. The derived plots are depicted in Fig. 4.2. They are also repeated for PMOS transistors.

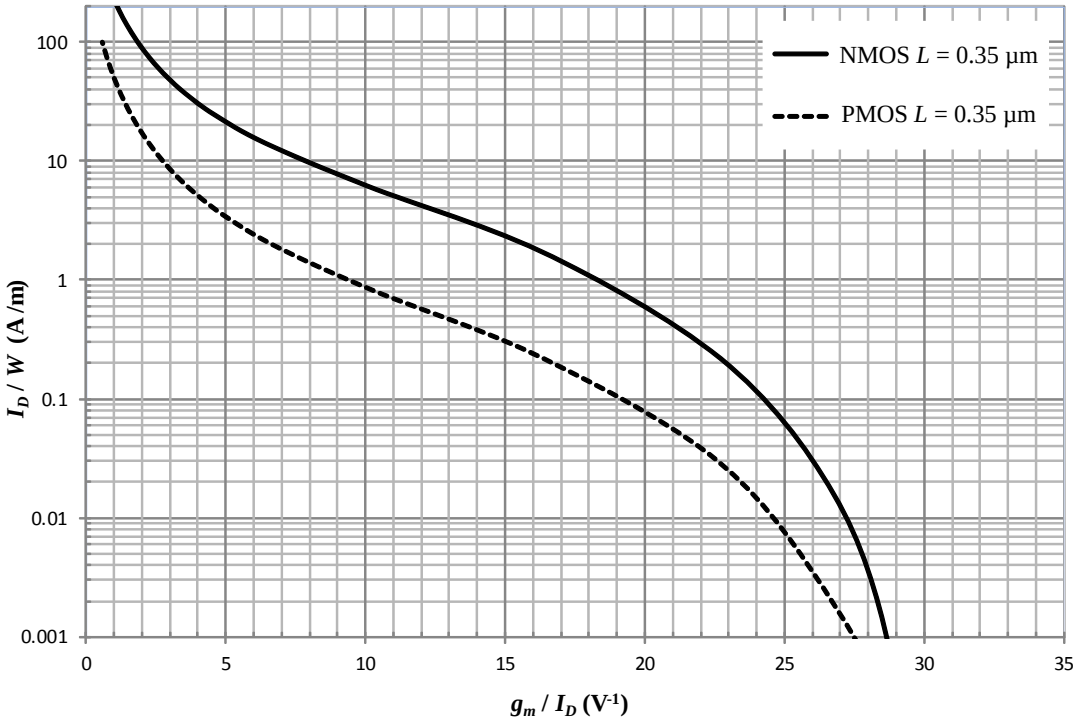


Figure 4.2 A plot of transconductance efficiency (g_m/I_D) versus current density (I_D/W) for NMOS and PMOS transistors

It is evident from Fig. 4.2 that a higher transconductance efficiency offers lower current density so that a suitable trade off must be made to achieve the required design objectives.

Transistor current density I_D/W = 25 A/m is selected, and from Fig. 4.2 the corresponding transconductance efficiency g_m/I_D = 4.5 (V^{-1})

$$\therefore I_D = \frac{g_m}{g_m/I_D} = \frac{6\text{ mS}}{4.5} = 1.33\text{ mA}$$

and

$$W = \frac{I_D}{I_D/W} = \frac{1.33\ mA}{25} = 53.33\ \mu m$$

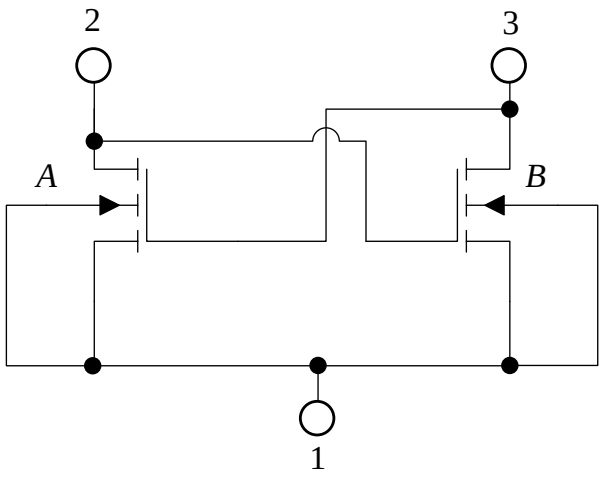
The following modifications are made to accommodate for all process corners after worst case simulations.

g_m = 20 mS

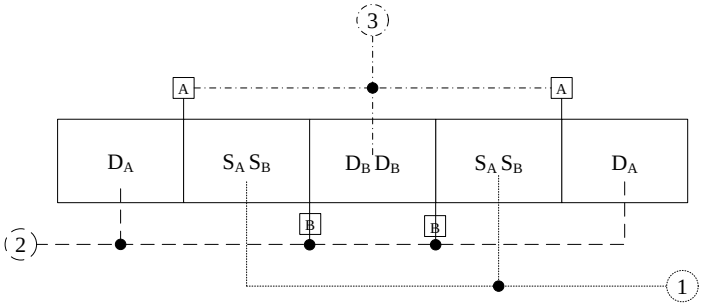
I_D = 4.4 mA

W = 120 µm

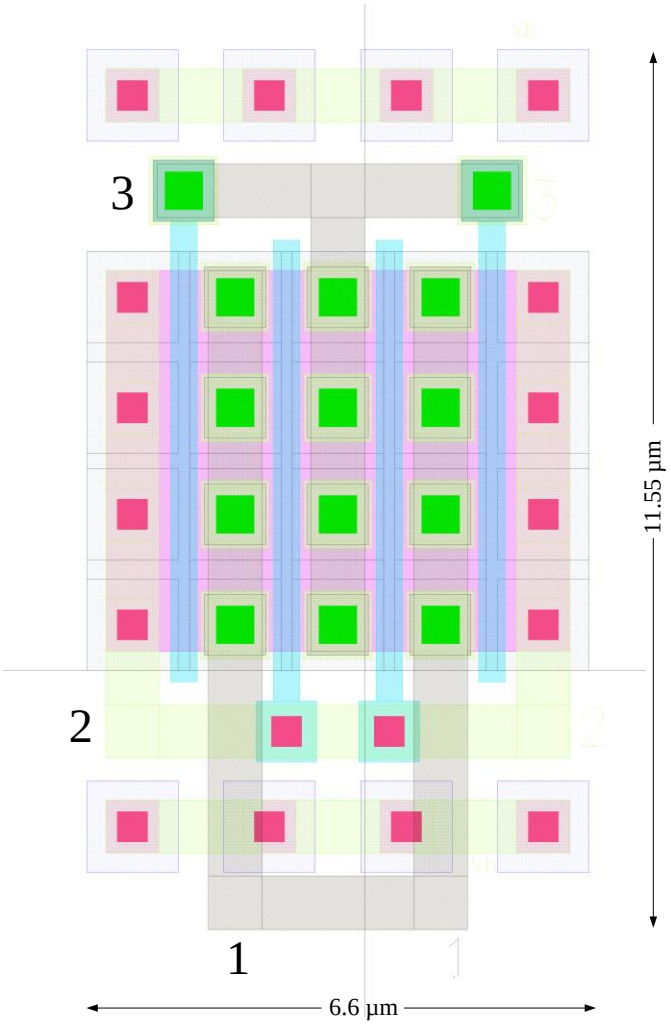
In order to improve the matching between drain and source regions of a large transistor, a multi-fingered interlaced layout method is adopted. For the oscillator differential cross-coupled transistors of size W/L = 120/0.35 are used. A standard cell of size (5 µm/0.35 µm) is constructed, with 24 fingers being used. Their interlacing is illustrated in Fig. 4.3.



a



b



c

Figure 4.3 Illustration of interlacing of transistors A and B: a. the schematic, b. the stick diagram, and c. the layout

The rectangular blocks in Fig. 4.3 b. indicate an *n*-type diffusion, where points 1, 2, 3 are the common points identified from the basic schematic of the transistors A and B. D_A, D_B, S_A, S_B indicate the drain and source regions of transistors A and B. In order to achieve the total width of 120 µm, 24 fingers each of 5 µm width are used. To further improve the matching between transistor fingers, dummy transistors of size (5/0.35) are inserted at both ends of the diffusion.

4.2.2 The varactor

In order to vary the frequency of the oscillator, a varactor is to be included. The two different types of varactors available in the process are junction varactors, and the MOS varactors operated in the accumulation mode. Tuning range, the *Q* factor, power consumption, and phase noise at large offset frequency from the carrier are considered as the variables in the selection of varactor. It was observed that the accumulation mode MOS varactor offers a performance much superior to junction varactors in terms of power consumption, phase noise and tuning range [23], [54]. In addition improved low frequency noise performance and a much better matched capacitance pair in an n^+ NWELL MOS varactor were reported [55]. An accumulation mode MOS varactor known as `CVAR` in the ams AG process is utilised in this work. There are four rows, and twelve columns are used to provide a C_{max} of 934.877 fF. The circuit diagram of the oscillator is depicted in Fig. 4.4.

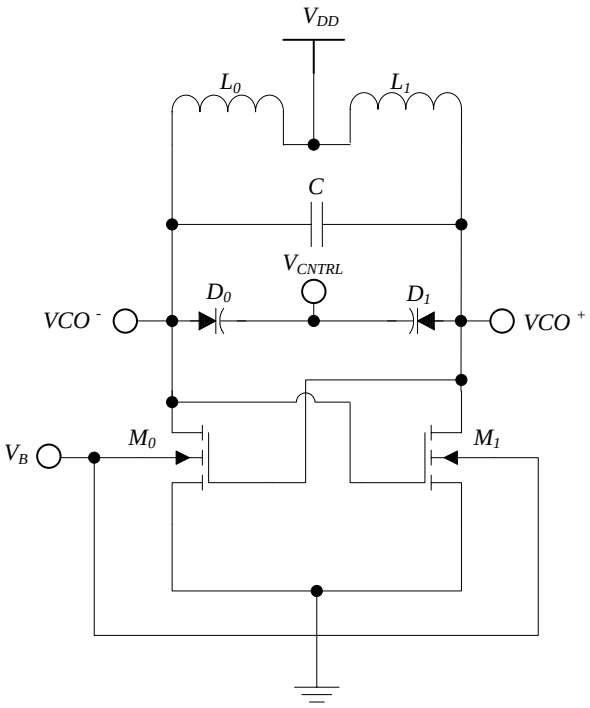
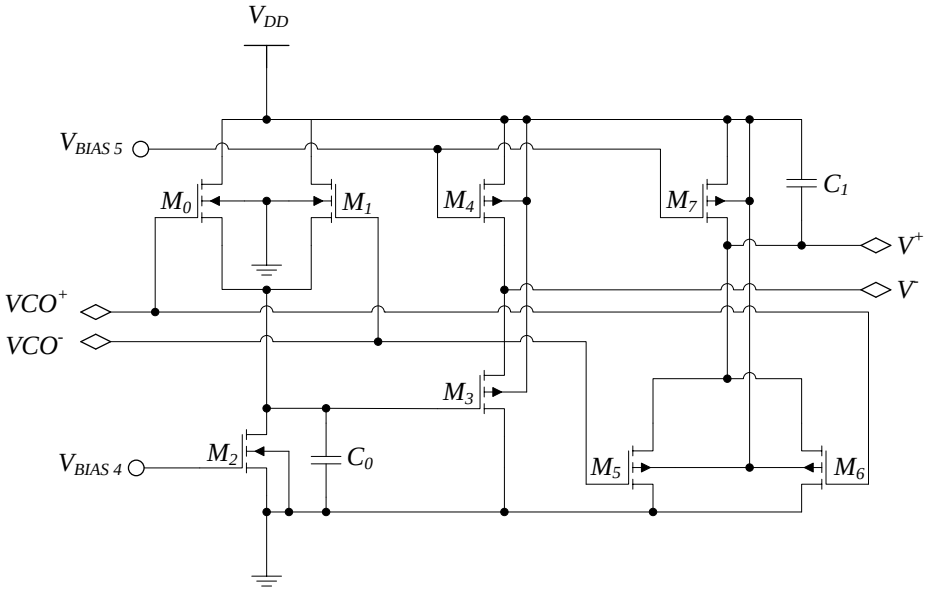


Figure 4.4 Illustration of topology used for the oscillator [23] (© [2009], with permission from Cambridge University Press)

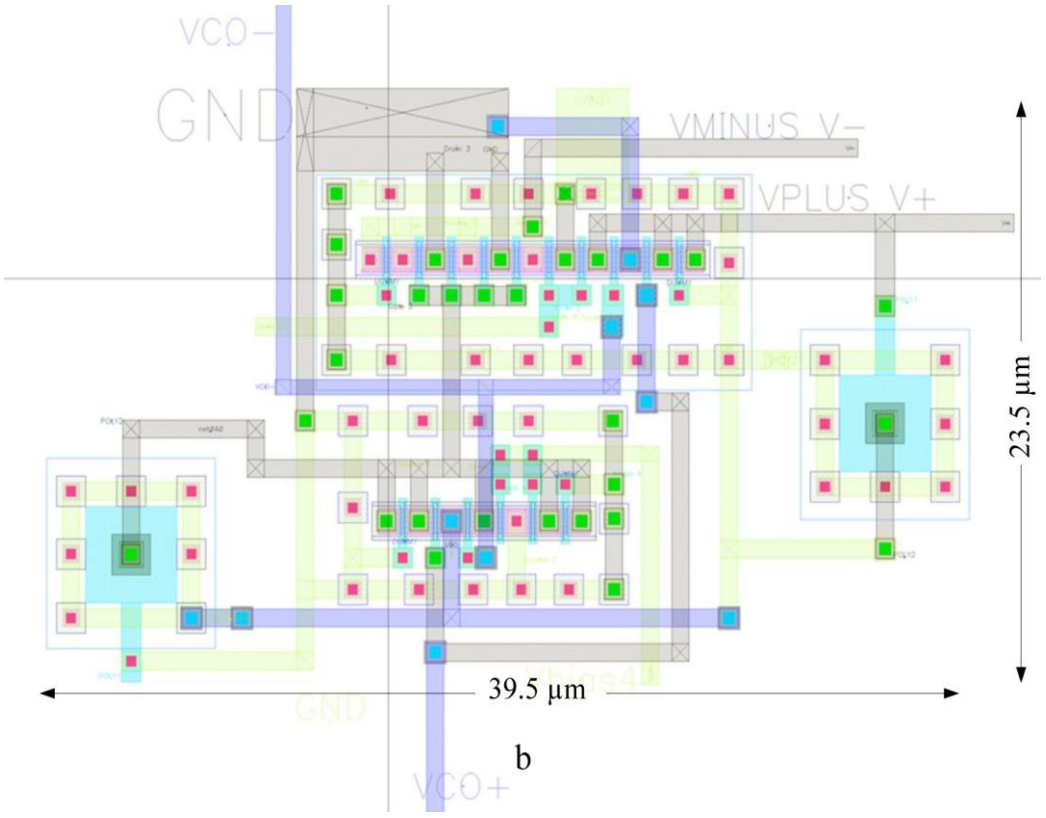
In Fig 4.4 the bulk connection of the differential cross coupled transistors M_0, and M_1 are provided as terminal V_B. This terminal was intended to be used with the ABB circuit mentioned in section 2.8.2. It was eventually decided to not utilize the ABB as explained in section 3.7. Therefore this terminal needs to be connected to the ground terminal.

4.3 THE AAC

From the sinusoidal generated by the oscillator, two voltages that represent the average positive peak (V^+) and the average negative peak (V^-) are formed by the AAC. Fig. 4.5 shows the complete circuit diagram of the AAC. Transistors M_0 and M_1 conduct alternately at the corresponding positive peak of the sinusoidal, and charge the capacitor C_0. M_2 acts as the current source. Similarly a negative peak detector is implemented using PMOS devices M_5, M_6, M_7 and a capacitor C_1. Transistor M_3 acts as a DC level shifter while M_4 is the current source.



a



b

Figure 4.5 a. AAC circuit schematic [56] (© [2005] IEEE), b. layout

In Fig. 4.5, the primary design consideration was to keep the power consumption as low as possible. Therefore devices with small widths are used. The voltage developed across C_0 is then level shifted using a DC level shifter which is implemented utilising M_3 and the current source M_4. With respect to Fig. 3.6 and the discussion of AAC provided in section 3.7, it is evident that tighter amplitude control may be achieved if the difference between V^+ and V^- ($V_{ID} = V^+ - V^-$) is set at a smaller value. Therefore it is imperative that AAC needs to be characterised for different values of V_{ID}. Tighter amplitude control is expected to provide with better temperature compensation but the effect of process variations needs to be accounted for. For a given oscillation amplitude ($VCO^+ - VCO^- = Vp\text{-}p$ = 1 V), the aspect ratio of level shifter M_3 is varied such that V_{ID} = 0.7 V, 0.8 V and 0.9 V. The resulting periodic steady state analysis (PSS) performed at temperatures 0 °C to 125 °C in five steps. This simulation is again repeated at nine process corners. Frequency drift in ppm/°C versus process corners are plotted in Fig. 4.6.

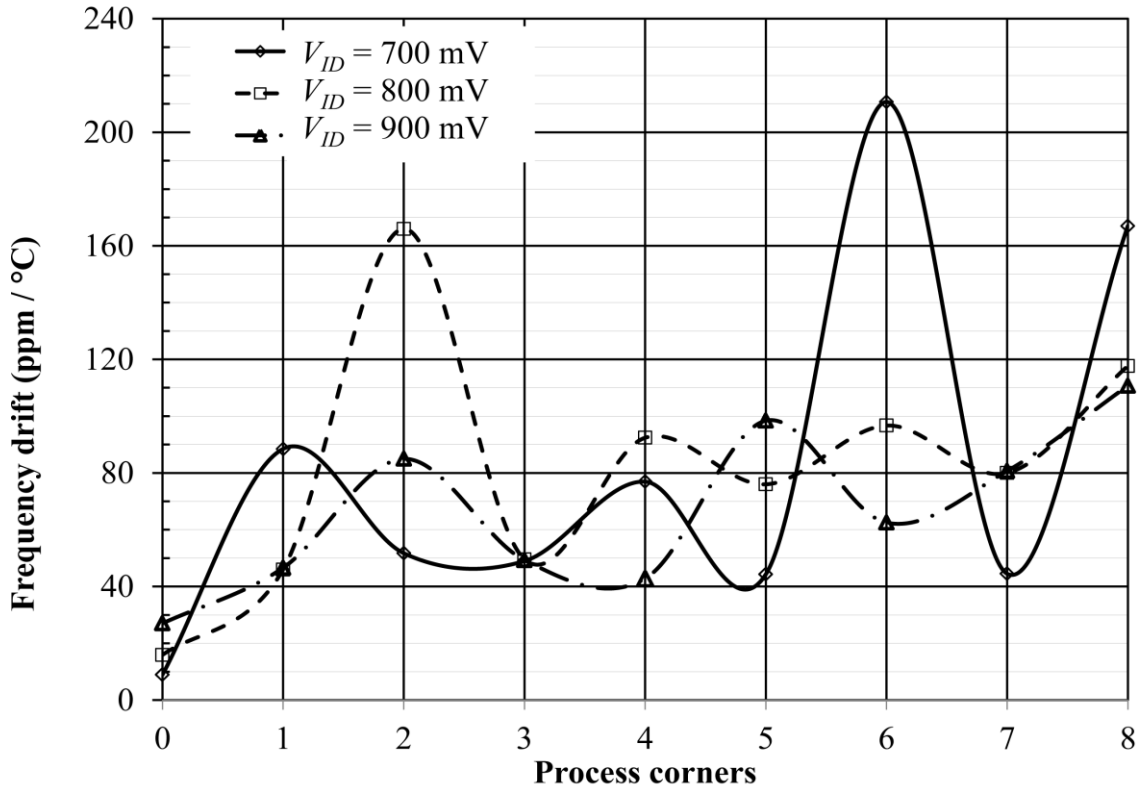


Figure 4.6 Frequency drift versus process corners for different V_{ID}

From Fig. 4.6 it is evident that best frequency compensation is observed for V_{ID} = 0.7 V, at process corner 0 (all TM with 9 ppm/°C), but provide very high frequency drift at corners 6 (WS, WP, LQ) and 8 (WS, WS, LQ). For V_{ID} = 0.8 V, corner 2 (WS, WP, HQ) performs the worst. The worst result at typical mean corner (38 ppm/°C) is observed for V_{ID} = 0.9 V, but for provide minimum deviation from the mean at other process corners. The best performance in typical mean corner is always the best choice for any design, but as a design trade-off V_{ID} = 0.8 V is selected for this design. The voltage distributions in the design for each node in the AAC circuit are listed in Table 4.2.

Table 4.2 The DC node voltages designed in AAC

Nodes	**Voltage (V)**
VCO^+	1 V
VCO^-	1 V
V_{C0}	0.2 V
V^-	1.4 V
V^+	2.2
V_{BIAS4}	0.9 V
V_{BIAS5}	2.2 V

As shown in Table 4.2, the level shifted voltage V^- is kept smaller than V^+, as explained in section 3.7. C_0 and C_1 are implemented using `CPOLY` available in the ams AG process. The components, designed transistor aspect ratios and drain currents, as well as the values of capacitance are listed in Table 4.3.

Table 4.3 Component values designed for AAC

List of Components / Type	Component Value	Drain Current
C_0 (CPOLY)	2.752 fF	N/A
C_1 (CPOLY)	2.752 fF	N/A
M_0 / NMOS	1 µ / 0.35 µ	10 µA
M_1 / NMOS	1 µ / 0.35 µ	10 µA
M_2 / NMOS	2 µ / 0.35 µ	20 µA
M_3 / PMOS	10 µ / 0.35 µ	15 µA
M_4 / PMOS	1 µ / 0.35 µ	15 µA
M_5 / PMOS	1 µ / 0.35 µ	5 µA
M_6 / PMOS	1 µ / 0.35 µ	5 µA
M_7 / PMOS	1 µ / 0.35 µ	10 µA

It can be observed from Table 4.3 that smaller device widths and smaller drain currents are selected. The total power consumed by the AAC circuit is 89 µW.

4.4 THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

An OTA is used as the error amplifier due to its high gain, reasonably large output signal swing and input dynamic range [57], [58]. The output of this operational amplifier is utilised to drive the input capacitance of the transistor M_{CNTRL} illustrated in Fig. 3.10. For this purpose M_{CNTRL} needs to be designed first.

The drain current of transistor M_{CNTRL} needs to be effectively restrained by the OTA output that is controlled by the AAC output voltage. During normal operation this must be the ZTC bias defined in Chapter 2. The overdrive voltage of this transistor needs to be selected in such a way that resulting transistor size is economical while preventing triode operation in large signal swing. In order to achieve effective control of current over a wider range, V_{ov} = 0.7 V is chosen.

$$(W/L)_{MCNTRL} = \frac{2I_D}{k_n' V_{ov}^2} = \frac{2 \times 4.4\text{ mA}}{170\text{ µ} \times 0.7^2} = 105.6 \cong \frac{40}{0.35}$$

The input capacitance of this transistor is yielded by

$$C_{gs_{MCNTRL}} = \frac{2}{3} WLC_{0x} = \frac{2}{3} 40\text{ µ} \times 0.35\text{ µ} \times 4.54 \frac{\text{fF}}{\mu\text{m}^2} = 127.1\text{ fF}$$

which is the loading capacitance of the OTA.

One of the factors that could affect the gain of an op-amp is the short channel effect. This effect in turn modifies the square law transfer characteristics in the saturation region to a more linear response [19]. Therefore it is necessary to exemplify MOS transistor's transfer characteristics. A plot of drain current vs. gate-source voltage is simulated for this purpose and illustrated in Fig. 4.7.

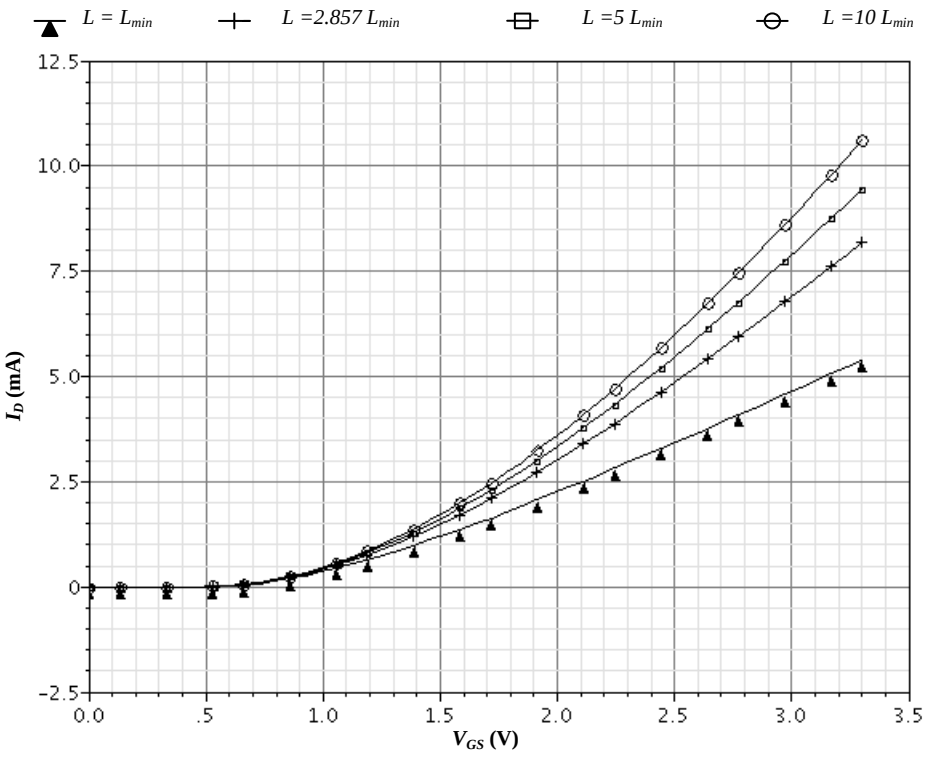


Figure 4.7 A plot of drain current versus gate-source voltage for different channel lengths of an NMOS transistor

The deviance from the ideal square law behaviour is more conspicuous at shorter channel lengths where $L = L_{min}$. It can also be noted that the short channel effect on drain current is gradually reduced as the channel length increases from the minimum value.

The output impedance of the op-amp directly contributes towards the gain; therefore a longer channel length must be utilised. However, larger channel lengths consume valuable space on the silicon wafer. As a design compromise, channel length of 1 µm (2.857 L_{min}) is chosen in this design. Moreover it was reported in [59] in analogue circuits, choosing a longer channel length would provide higher performance than minimum channel length that the particular process technology provides.

The large output impedance provided by the cascode current loading stage delivers positive voltage gain even if short channel effects reduce the output impedance considerably. The topology used for the OTA is depicted in Fig. 4.8.

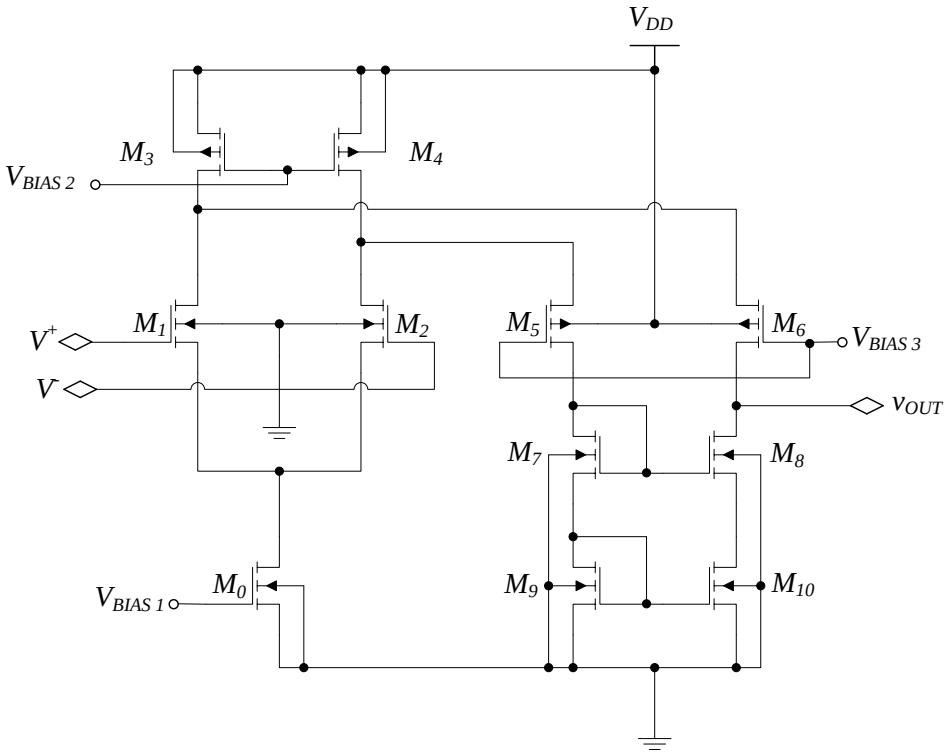


Figure 4.8 Folded Cascode OTA topology used [19] (© [2010], IEEE)

In Fig. 4.8, transistors M_0, M_3, M_4, M_5, and M_6 act as current sources. The differential input gain stage is constituted by M_1 and M_2 while $M_7 - M_{10}$ act as the cascode loading stage.

The input common mode range and the output swing are as follows.

$$(V_{tn} + 2V_{ovn}) < V_{iCM} < (V_{DD} - V_{ovp} - V_{tn}) \quad (4.1)$$

$$(V_{tn} + 2V_{ovn}) < V_O < (V_{DD} - 2V_{ovp}) \quad (4.2)$$

The design variables and procedures adopted from [52], [53] are listed in Table 4.4.

Table 4.4 List of design variables and design constraints

Design Variable	**Remarks**	**Design Constraints**
$A_v \approx 500$	High gain required to provide effective compensation by suppressing the amplitude.	Bandwidth (B)
R_s = 1 MΩ	Assumed to estimate input pole	
C_L = 127 fF	C_L = Input capacitance of the loading stage = $(WLC_{ox})_{MCNTRL}$	Output pole (p_{out}) << Input pole (p_{in}) $p_{out} = \frac{1}{2\pi R_L C_L}$ (4.3)
C_{gs} = 90 fF	WLC_{ox} of a sample transistor ($WL \approx 20$ µm^2)	Input pole $p_{in} = \frac{1}{2\pi R_s C_{gs}}$ (4.4)
Bandwidth B = 300 kHz	Gain bandwidth product is kept small	$B \geq \frac{1}{2\pi\, p_{in}}$ (4.5) $B \geq \frac{1}{2\pi\, p_{out}}$ (4.6)
$f_{t\,min}$	Unity gain frequency of the transistor	$f_t = \frac{g_{m\,min}}{2\pi C_{gs\,max}}$ (4.7)

In order to assist in further design the transconductance efficiency is again plotted against f_t for NMOS and PMOS transistors of different channel lengths of L = 0.35 µm and L = 1 µm. The plots are shown in Fig. 4.9.

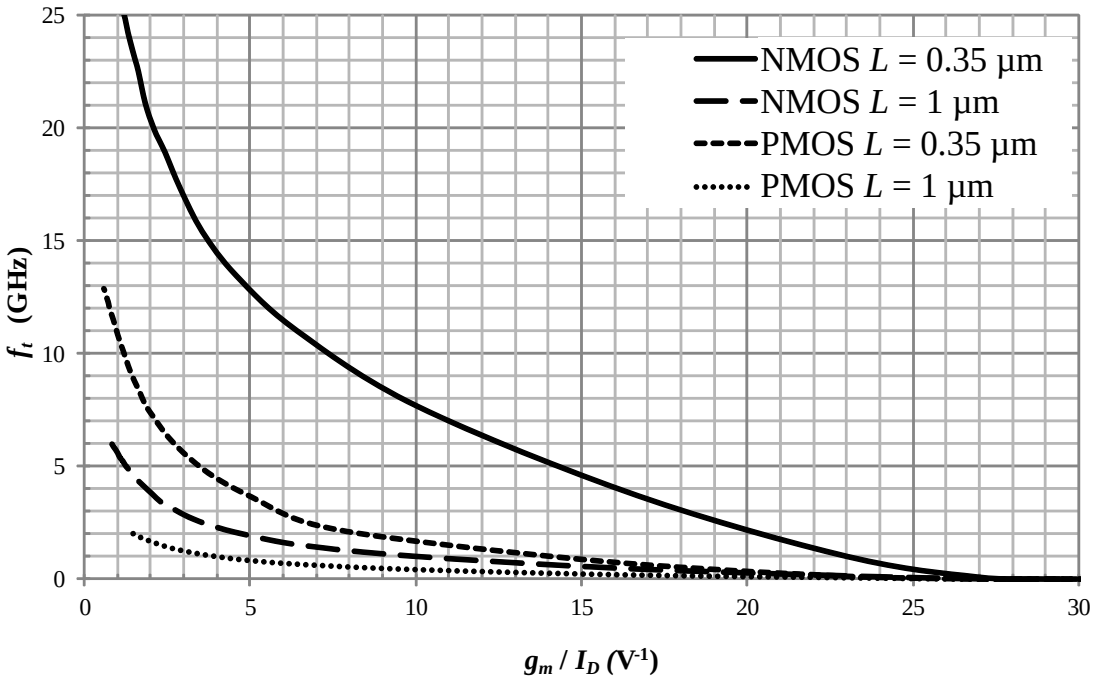


Figure 4.9 Unity gain frequency f_t versus g_m/I_D for NMOS and PMOS transistors

From Fig 4.9 it is evident that the NMOS and the PMOS behave identically with clear distinction between them. As expected, due to relevant doping – the NMOS offers a much better unity gain frequency compared to PMOS transistors. It can also be noted that the unity gain frequency of longer channel length (L = 1 µm) devices is much inferior to that of a short channel transistor with L = 0.35 µm.

Interesting observations were made by plotting transconductance efficiency versus Early voltage (V_A) for the MOS transistors using DC operating point simulation in Cadence Virtuoso, and are depicted in Fig. 4.10.

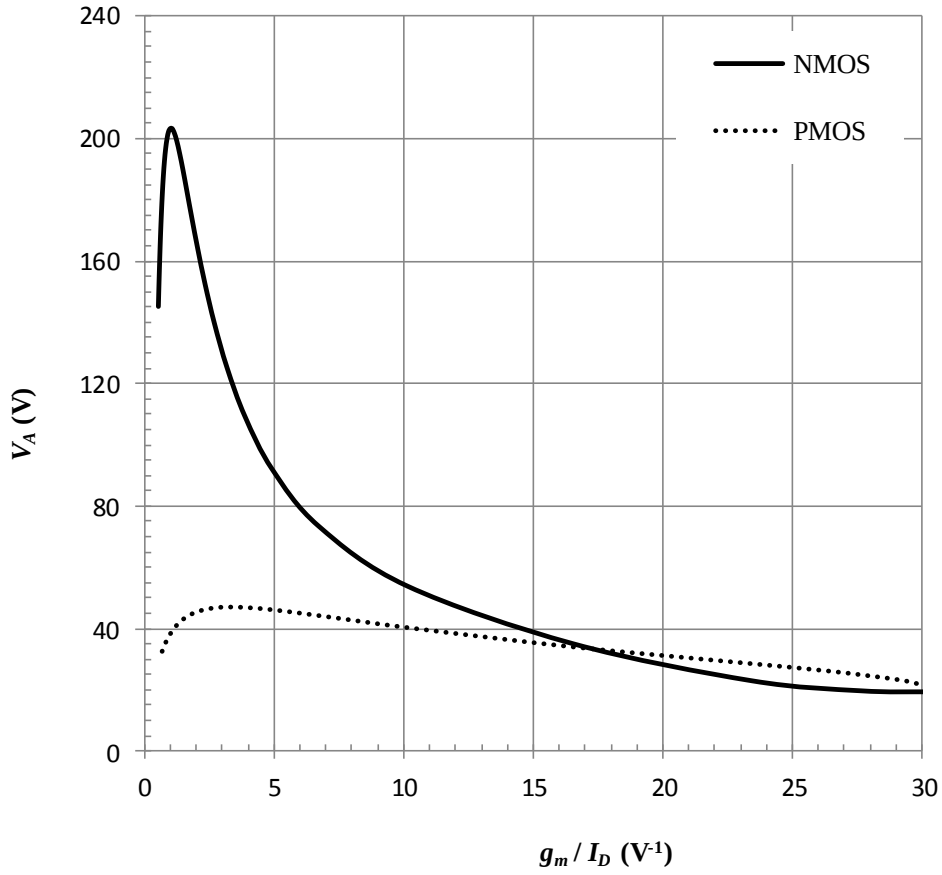


Figure 4.10 Early voltage of a MOSFET versus transconductance efficiency

The plot in Fig 4.10 reveals that the V_A of both NMOS and PMOS are identical when they are in strong inversion. As the degree of inversion reduces NMOS demonstrates higher values of V_A compared to PMOS transistors. This also confirms the argument in section 4.1 that weak inversion generates higher gains as the gains are inversely proportional to channel length modulation parameter λ.

Assuming $p_{out} \gg p_{in}$, using (4.7)

$$g_{m\,min} = 2\pi B C_L = 239.4 \text{ nS}$$

to ensure the input pole does not exceed the bandwidth, using (4.4)

$$C_{gs} = \frac{1}{2\pi B R_s} = 530 \text{ fF}$$

The assumed value of C_{gs} is less than the calculated value and the output pole remains to be dominant.

$g_{m1} = g_{m2} = 500$ µS is selected for high voltage gain. The corresponding unity gain frequency is found using (4.7)

$$f_t = \frac{500\ \mu S}{2\pi \times 90\ fF} = 882\ MHz$$

using the plot in Fig. 4.9 for NMOS with $L = 1$ µm, and $f_t \approx 1$ GHz results in

$$g_m/I_D \approx 10$$

$$\therefore I_{D1} = I_{D2} = \frac{g_m}{g_m/I_D} = 50\ \mu A$$

from Fig. 4.2 the current density for NMOS is found to be

$$I_D/W \approx 6$$

$$\therefore W_1 = W_2 = \frac{I_{D1}}{I_D/W} = \frac{50\ \mu A}{6\ A/m} = 8.33\ \mu m$$

$$I_{D0} = I_{D1} + I_{D2} = 100\ \mu A$$

$$\therefore W_0 = \frac{I_{D0}}{I_D/W} = \frac{100\ \mu A}{6\ A/m} = 16.7\ \mu m$$

$I_{D3} = I_{D4} = 1.4\ I_{D1} = 70$ µA is chosen so that there is current flowing through the loading stage at all times.

$g_m/I_D = 10\ V^{-1}$ is selected to be same as NMOS. The corresponding current density from Fig. 4.2 (for PMOS) is 0.85 A/m.

$$\therefore W_3 = W_4 = \frac{I_{D3}}{I_D/W} = 83.5\ \mu m$$

the bias current flowing through PMOSs M_5, M_6:

$$I_{D5} = I_{D6} = 20\ \mu A$$

$$\therefore W_5 = W_6 = \frac{I_{D5}}{I_D/W} = 24\ \mu m$$

The currents flowing through the NMOS loading stages $M_7 = M_8 = M_9 = M_{10}$:

$$I_{D7} = 20\ \mu A$$

$$\therefore W_7 = W_8 = W_9 = W_{10} = \frac{I_{D7}}{I_D/W} = 9\ \mu\text{m}$$

The designed OTA is simulated at typical mean and eight worst case corners identified in Table 4.1. Some of the transistor aspect ratios are readjusted to accommodate for changes required, to accommodate for especially corners 5 (WP, WP, LQ) and 8 (WS, WS, LQ). All transistor sizes are listed in Table 4.5.

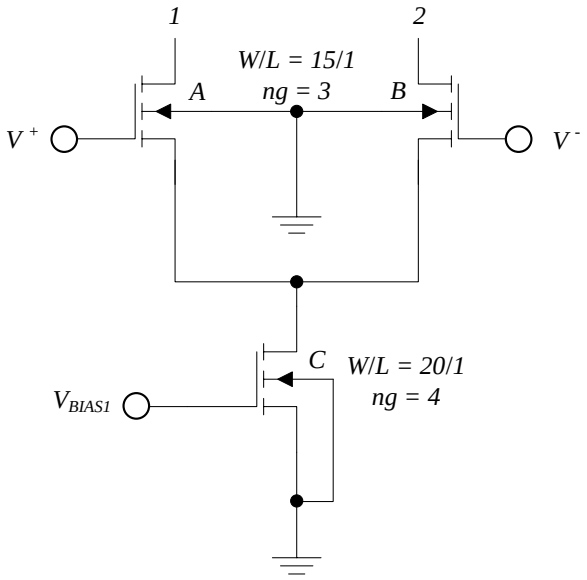
Table 4.5 List of transistors designed for the folded cascode OTA in Fig. 4.8

Transistor Name	NMOS / PMOS	W/L	Reason for Modification
M_0	NMOS	20/1	To accommodate for change in V_{BIAS1}
M_1	NMOS	15/1	To accommodate for change in V_{BIAS1}
M_2	NMOS	15/1	To accommodate for change in V_{BIAS1}
M_3	PMOS	80/1	*N/A*
M_4	PMOS	80/1	*N/A*
M_5	PMOS	80/1	To accommodate for corners 5, and 8
M_6	PMOS	80/1	To accommodate for corners 5, and 8
M_7	NMOS	20/1	To accommodate for corners 5, and 8
M_8	NMOS	20/1	To accommodate for corners 5, and 8
M_9	NMOS	20/1	To accommodate for corners 5, and 8
M_{10}	NMOS	20/1	To accommodate for corners 5, and 8

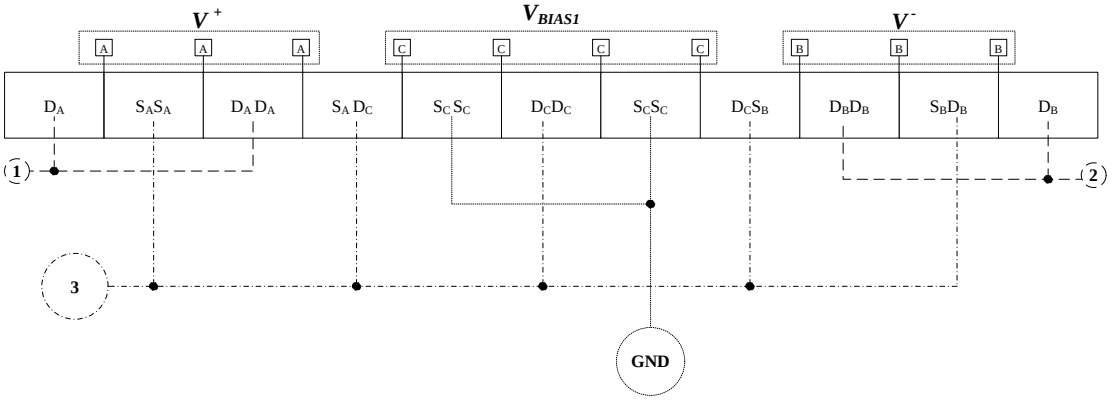
The aspect ratios of M_0, M_1 and M_2 are modified so that a reduction of voltage in V_{BIAS1} is compensated. Aspect ratios of transistors M_5 – M_{10} are also modified as mentioned in Table 4.5.

A multi-fingered interlaced layout format is used to improve the matching and to reduce the parasitic capacitance. Fig. 4.11 illustrates the layout followed in designing M_0, M_1 and

M_2. A similar interlaced sequence is followed in designing the layout of the rest of the circuit.



a



b

Figure 4.11 Illustration of layout design of M_0,M_1 and M_2, a. the schematic, b. using stick diagram

In Fig. 4.11a, transistors M_1, M_2, M_0 are labelled as A, B and C respectively. Common terminals identified are marked as V^+, V^-, V_{BIAS1}, 1, 2 and the ground. A standard cell with an aspect ratio, W/L = (5/1) is selected to design the circuit. M_1 and M_2 utilise three

standard cells and M_0 four cells to satisfy the design requirements. The stick diagram is made use of to generate the optimum layout.

4.5 BIAS VOLTAGE GENERATION

A folded cascode such as that in Fig. 4.8 made use of three voltage references. In addition to this the AAC also required two reference voltages. Since resistive networks demonstrate strong temperature dependency, it was decided to generate these voltages using MOS devices only. This has led to lower power consumption as well. The drain source connections endorse saturation operation for all devices. The required bias voltages are listed in Table 4.6.

Table 4.6 Reference voltage required for the OTA and AAC

Parameter	Voltage (V)
V_{BIAS1} (OTA)	0.76 V
V_{BIAS2} (OTA)	2.47 V
V_{BIAS3} (OTA)	2.30 V
V_{BIAS4} (AAC)	0.90 V
V_{BIAS5} (AAC)	2.05 V

In Table 4.6 $V_{BIAS1,}$ and V_{BIAS2} are calculated to deliver the required amount of bias currents for M_0 and M_3, M_4 respectively. V_{BIAS3} is calculated in such a way that transistor M_3 and M_4 are biased at the edge of saturation region so that maximum positive output swing (4.2) is obtained. The bias circuit used is illustrated in Fig. 4.12. The total power consumed in this circuit is 120.7 µW.

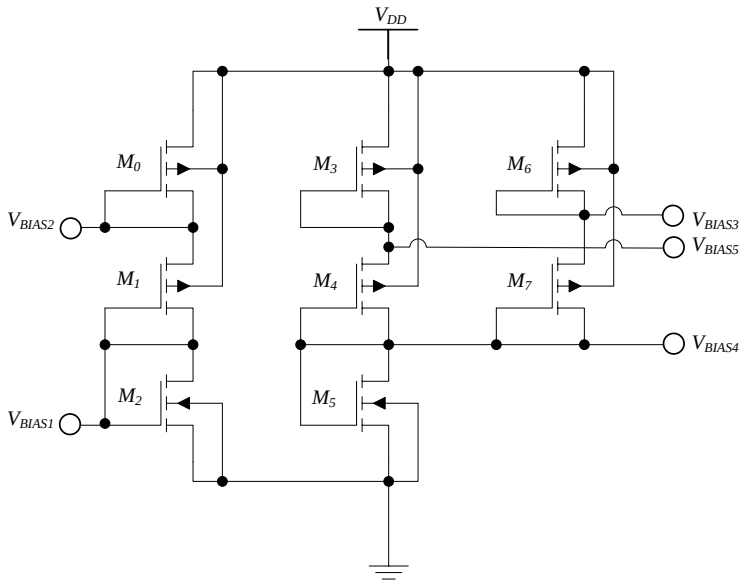


Figure 4.12 Circuit used to generate five reference voltages

In Fig. 4.12, the closed loop connection of M_6, M_7 to the drain of M_5 stabilises the bias voltages against minor variations in supply voltages. The transistor sizes and the drain currents are listed in Table 4.7.

Table 4.7 Transistor sizes and the drain currents used in design of reference voltage generation

Transistor / Type	I_D **(µA)**	W/L **(µm/µm)**	**Number of Gates**
M_0 / PMOS	20	16.8 / 0.35	42
M_1 / PMOS	20	0.8 / 0.35	2
M_2 / NMOS	20	2 / 0.35	5
M_3 / PMOS	30	1.2 / 0.35	3
M_4 / PMOS	30	2.8 / 0.35	7
M_5 / NMOS	45	0.8 / 0.35	2
M_6 / PMOS	15	2.4 / 0.35	6
M_7 / PMOS	15	1.2 / 0.35	3

It is evident from Table 4.7 that in the layout design of the reference voltage generator, the smaller transistor widths were used. This is to precisely adjust the bias voltage closer to the required values.

4.6 THE OUTPUT BUFFER

The generated sinusoidal needs to be connected to 50 Ω load impedance through a buffer. The design constraint here is to reduce the power consumption while delivering sufficient signal amplitude to the load. In order to reduce the power consumption an emitter follower is biased at a very low current. The circuit diagram is illustrated in Fig. 4.13.

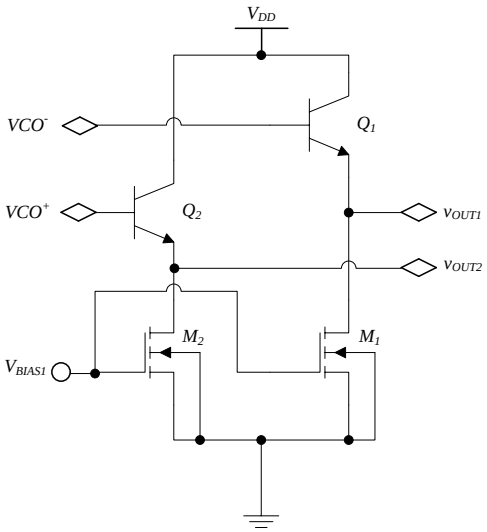


Figure 4.13 Emitter follower circuit

In Fig. 4.13 an HBT is chosen as the emitter follower as it provides much higher transconductance compared to a MOSFET. The current source is implemented using NMOS transistors.

The g_m of the transistor was selected such that it delivers maximum power output to the 50 Ω external load.

$$1/g_m = 50$$

$$g_m = 20 \text{ mS}$$

$$I_C = 500 \text{ µA}$$

The complete layout is depicted in Fig. 4.14.

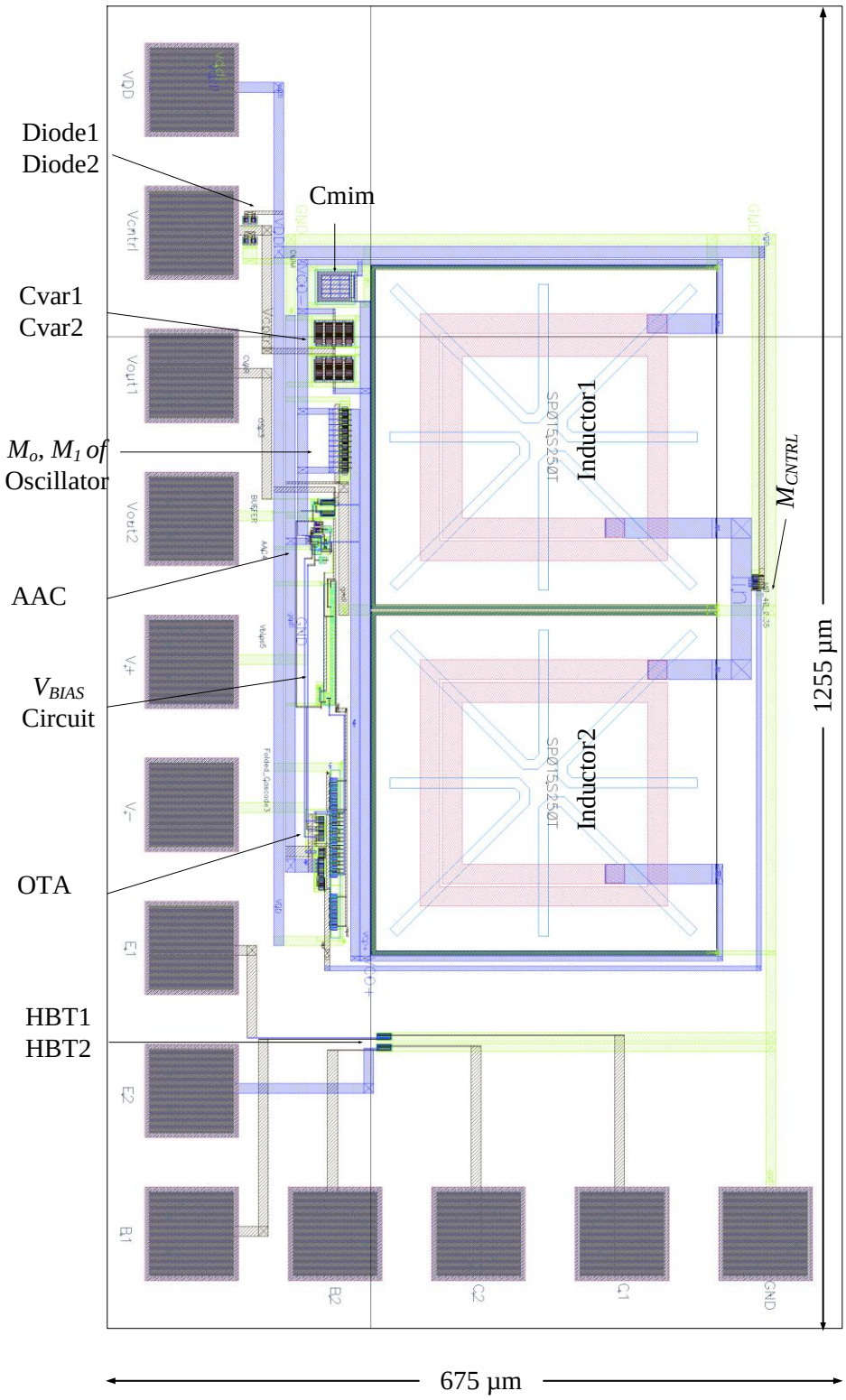


Figure 4.14 The complete layout

In Fig. 4.14 Diode1, Diode2 are connected to V_{CNTRL} terminal to prevent electrostatic discharge. The two spiral inductors are 1.49 nH each, having physical dimention of 345 µm × 350 µm.

This is a multi project wafer (MPW) and the floor plan of the four designs that are incorporated in the IC are as depicted in Fig. 4.15.

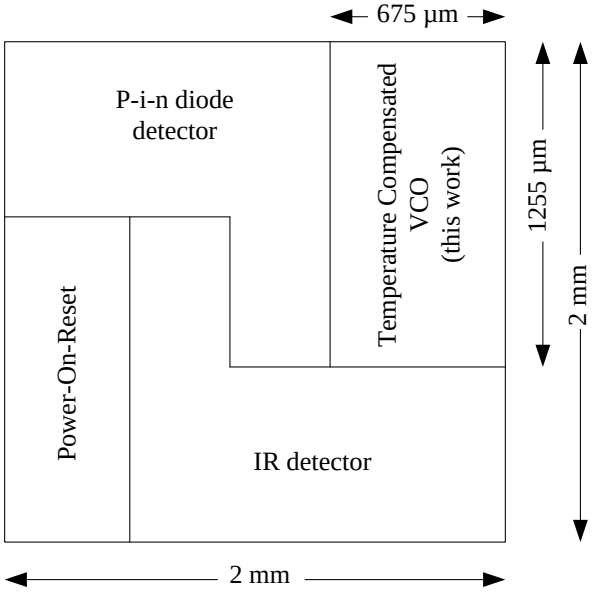


Figure 4.15 The chip floor plan

As illustrated in Fig. 4.15, the centre part of the wafer is reserved for the pixels of the photo-detector project to capture maximum light in this MPW. The remaining two projects including this work shared the rest of the wafer space.

4.7 PACKAGING

Considering the frequency of operation, the packaging used for the fabricated IC should offer low inductance and capacitance. Moreover the IC needs to be heated up to 125 °C in several steps to verify the frequency deviation as a function of temperature. Therefore it is important that the packaging offers good thermal conductivity, thereby offering a minimum gradient of temperature between packaging and the inner die.

Since the QFN 56 package, with its exposed thermal die pad at the board level, offers minimum inductance and capacitance it is selected for this MPW. Moreover the thermal die pad offers a direct heat transfer from the die to the board [60]. The design related to this dissertation makes use of pins 35 to 47. The physical dimensions and the bonding diagram of the IC inside the package are depicted in Fig. 4.16.

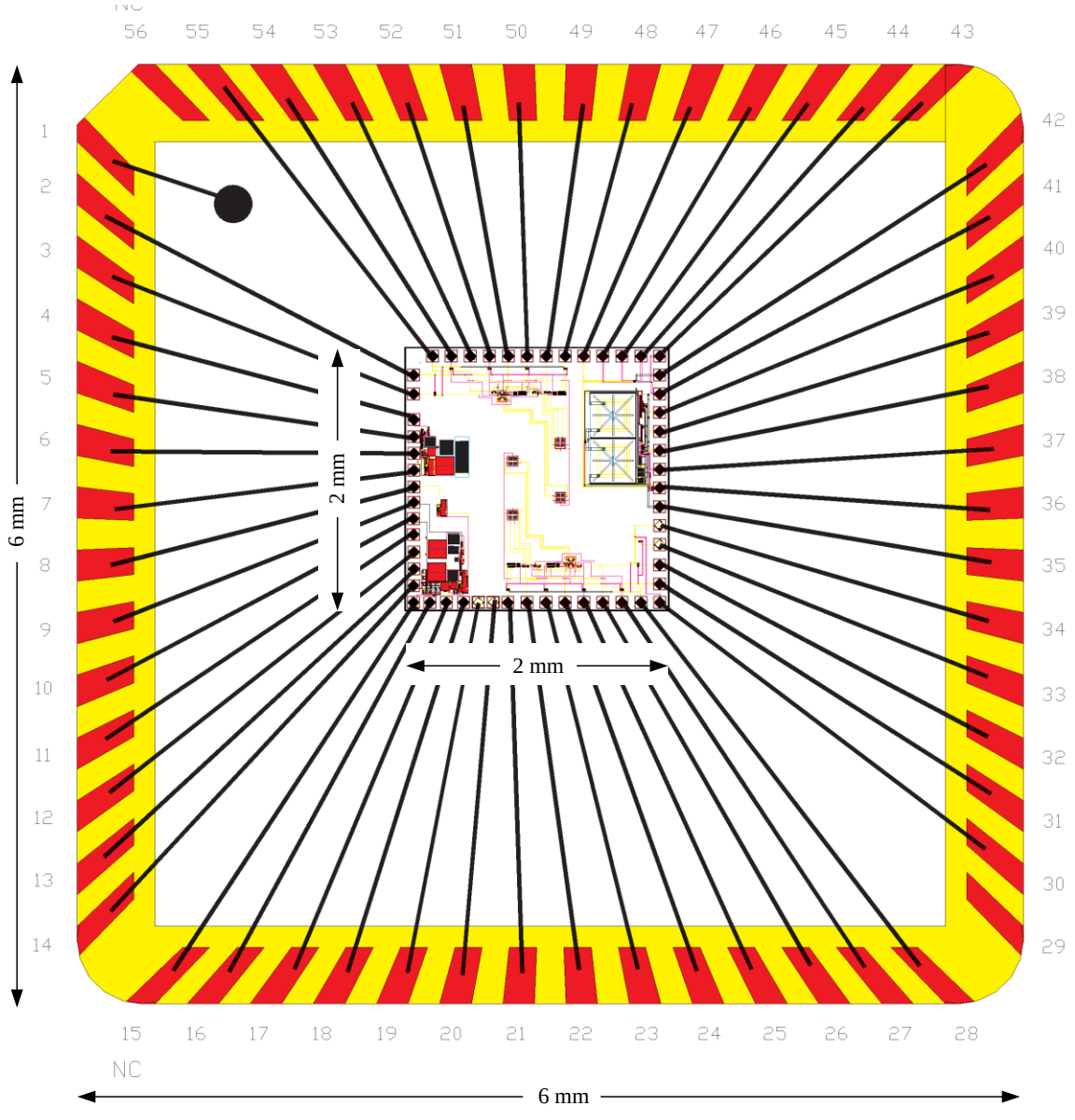


Figure 4.16 The bonding diagram of the QFN 56 package

In Fig. 4.16, bonding wires are used to interconnect the terminal of the IC to the package. The shortest bonding wire has a length of 2 mm with the longest being 3.606 mm. The

wavelength of operation of the circuit is 125 mm, so that bonding wire of the required length could cause distortion at the output. In order to characterise the effect of bonding wires on the signal strength, two pins (19, 20) are interconnected in the IC using available metal layers.

4.8 PCB

A microwave laminate - allows for the transmission of signals exhibiting the minute wavelengths of RF with minimal loss and stable, consistent performance [61]. Relative permittivity (ε_r) of the dielectric constant, the dissipation factor, and the dielectric constant tolerance are the most important parameters of interest at microwave frequencies. Additionally, the thermal coefficient of relative permittivity is also important for this study as variations in temperature are imminent.

Distributed models are thus used to account for the magnitude and phase shift of the signal over the transmission line. In order to minimise reflection, all transmission lines must be terminated in characteristic impedance of the terminating load. In addition electromagnetic radiation and capacitive coupling among the elements causes unintentional losses that may also significantly alter the performance of the circuit.

Therefore a four layer PCB with power lines sandwiched between two ground planes is chosen. Furthermore this four layer PCB allows microstrip transmission lines to be designed to match the characteristic impedance of the measuring equipment. The thickness of the PCB material needs to be selected in such a way that the resulting width of the transmission line is close to 1 mm [62].

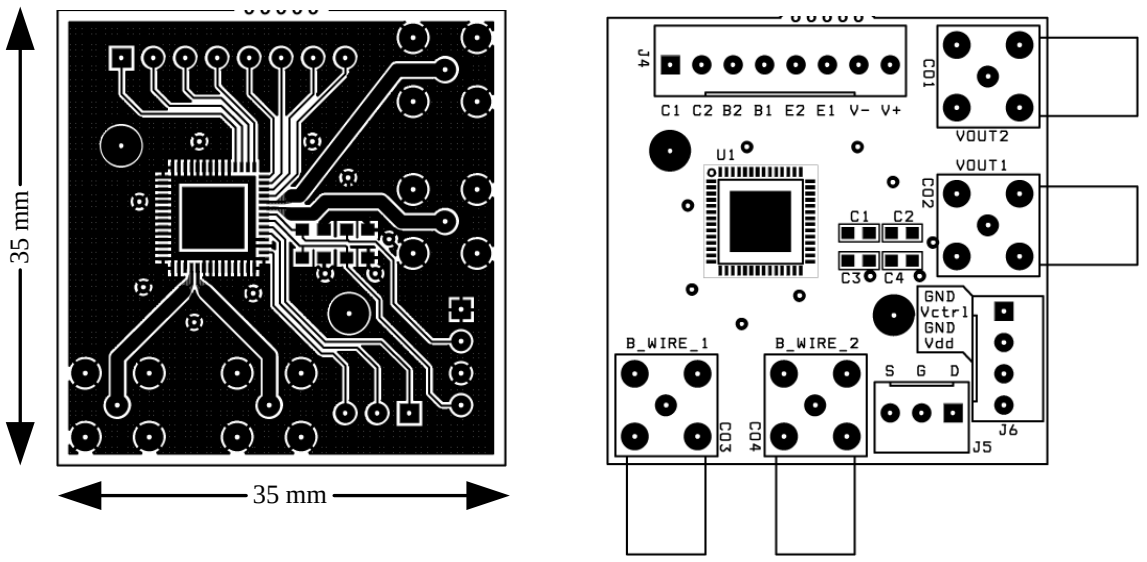
The characteristic impedance of the microstrip lines designed must not change as it would result in inconsistent readings during the frequency stability measurements. It is thus necessary to have a low ε_r for the board material. The most common PCB materials that are widely used at RF are listed in Table 4.8 [62], [63].

Table 4.8 Typical values of relative permittivity in various laminates versus tolerance and thermal coefficient of ε_r /°C

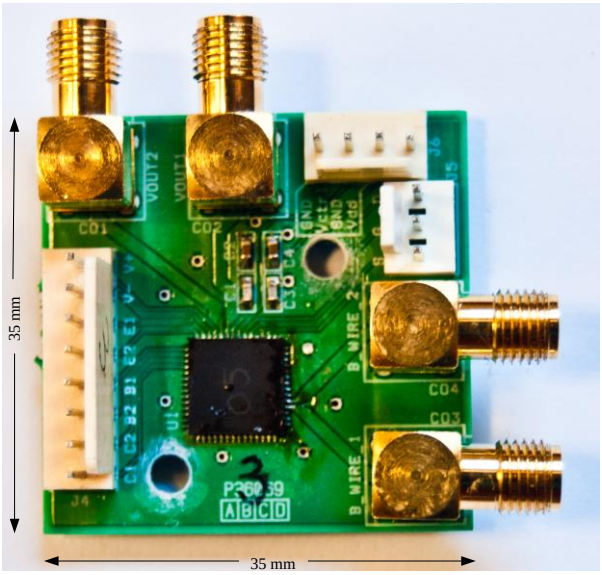
Board Material	Relative Permittivity (ε_r)	Dielectric constant tolerance	Thermal Coefficient of ε_r
FR4	4	± 5 – ± 25 %	+ 200 ppm/°C
RO4003	3.55	± 0.05	+ 40 ppm/°C
Rogers/RT Duroid	2.94	± 0.04	+ 12 ppm/°C

From Table 4.8, it is clear that, the least costly choice, the FR4 material has a large tolerance on the relative permittivity and could result in inconsistent characteristic impedance for a transmission line. RO4003 and RT Duroid have a lower tolerance and lower thermal coefficient of ε_r. Considering the lower ε_r, lower thermal coefficient, and taking cost into account, RO4003 with a thickness of 0.8 mm is chosen.

The PCB is fabricated and populated using an external vendor: its design, layout and a photograph are provided in Fig. 4.17.



a b



c

Figure 4.17 a. PCB design, b. the layout, c. populated with IC and the components

In Fig. 4.17, all RF lines v_{OUT1},v_{OUT2}, pins 19 and 20 are connected to female SMA connectors using microstrip transmission lines matched to 50 Ω impedance of the RF measuring equipment. The rest of the pins are provided using 2.54 mm headers.

4.9 CONCLUSION

The hypothesis formulated in Chapter 1 proclaims that the temperature dependency of an LC oscillator could be reduced by controlling the oscillation amplitude. Hence the sub-systems that constitute a temperature compensated VCO are an oscillator operated at ZTC, an AAC that generates two voltages which represent the positive and negative peaks of the oscillation sinusoidal, an OTA that acts as an error amplifier which regulates the bias current to the oscillator, a bias voltage reference using MOS transistors, and an output buffer which were designed in schematic and layout. The completed design is thereafter integrated in a single IC and subsequently fabricated in silicon-germanium. A suitable PCB was designed and populated with the IC and other components so that various measurements are performed efficiently.

CHAPTER 5 SIMULATION RESULTS AND EXPERIMENTAL VERIFICATION

5.1 INTRODUCTION

This chapter experimentally addresses research questions associated to study. Simulation results are also provided, together with measured results to enable comparisons and discussions. PLS are provided where necessary to explicate the mismatches between the simulations and experimental results. Two important measurements are provided, namely frequency versus V_{CNTRL} and frequency versus temperature.

5.2 FREQUENCY VERSUS V_{CNTRL}

Fig. 5.1 depicts the output frequency of the system as a function of control voltage. Simulation results, as well as measured results, are plotted by sweeping V_{CNTRL} from 0.6 V to 1.8 V. The temperature stabilised VCO was supplied by Escort 3 EPS-3250 power supply. Frequency and power measurements were performed using Rohde & Schwarz spectrum analyzer FSP3 (1164.4391.03) with a noise floor of -145 dBm using 0 dB RF attenuation, at resolution bandwidth of 10 Hz, and a video bandwidth of 1 Hz for 1 – 3 GHz frequency range.

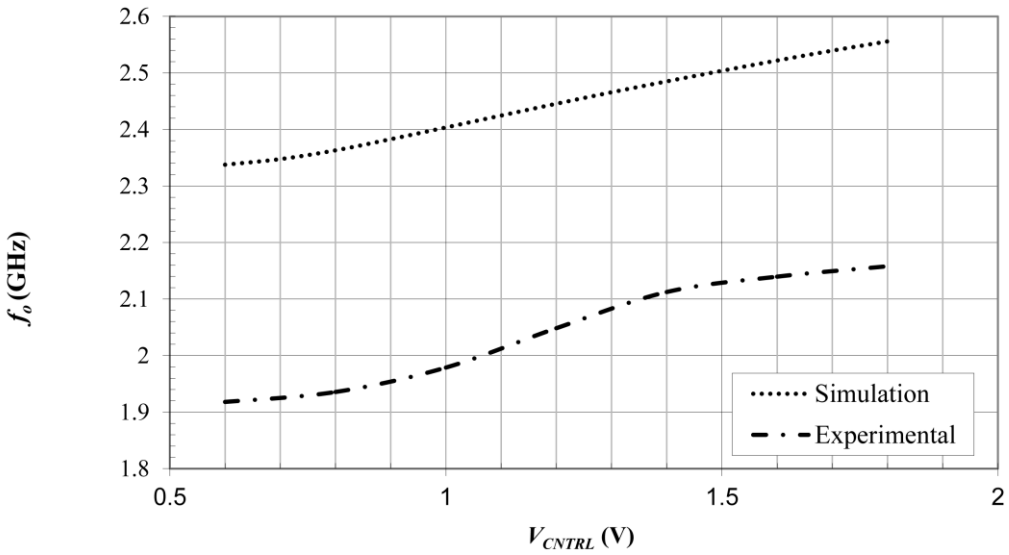


Figure 5.1 f_o vs. V_{CNTRL} for simulation and experimental results

As illustrated in Fig 5.1 the experimental result follows that of the simulation result as far as frequency deviation. However the experimental frequency is about 400 MHz lower than that of the simulation results. This is due to parasitic capacitances due to metallic interconnects that are not accounted for in simulation.

$$\Delta_f / \Delta V_{CNTRL} = 180 \text{ MHz/V for simulation}$$

$$\Delta_f / \Delta V_{CNTRL} = 200 \text{ MHz/V for experimental results.}$$

The simulated power outputs, together with measured output power in the real time experimentation, are listed in Table 5.1.

Table 5.1 Power output: Simulation versus experimental reading

V_{CNTRL} (V)	p_{out} (dBm) (Simulation)	p_{out} (dBm) (experimental)
0.6	3.60	- 37.9
0.8	3.34	- 34.3
1	3.30	- 33.5
1.2	3.42	- 35.7
1.4	3.68	- 27.4
1.6	3.97	- 30.6
1.8	4.16	- 29.7

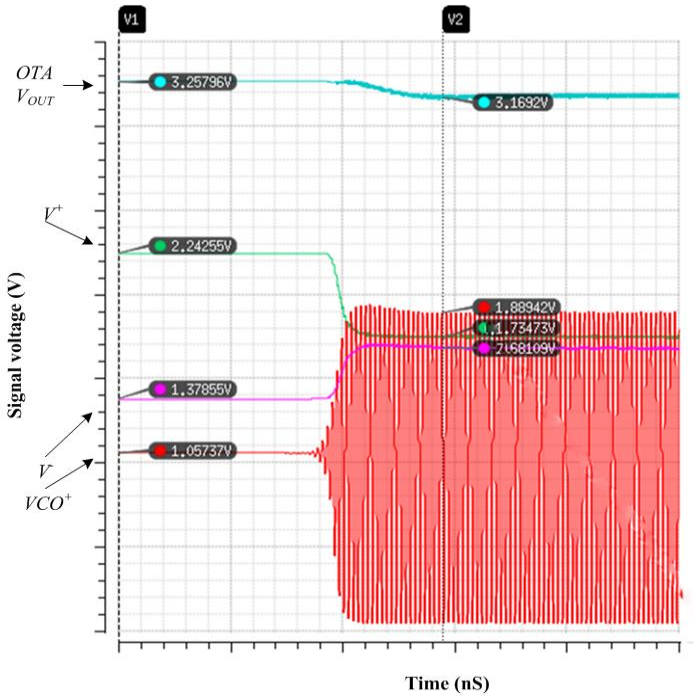
The power output readings recorded in Table 5.1 indicate that the experimental reading is on average 38 dB less than the simulation result. Lower than expected output power is explained in section 5.4.

5.3 FREQUENCY VERSUS TEMPERATURE

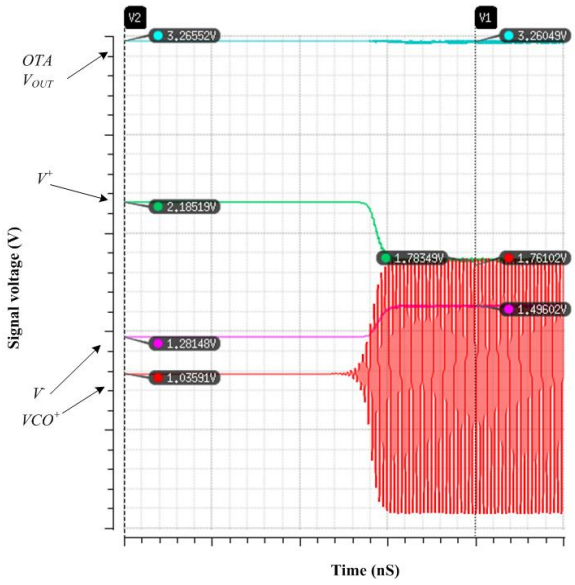
Frequency drift as a result of temperature variations needs to be recorded to verify the hypothesis. Transient simulation results are presented first, followed by PSS analysis to determine the frequency shift.

5.3.1 Simulation results

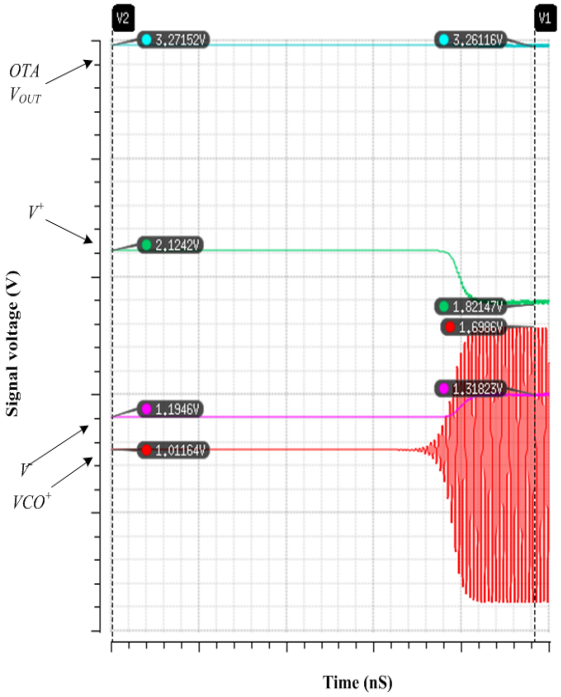
A parametric simulation of the complete circuit over a temperature range of 0 to 125 °C in three steps generated the plot of Fig. 5.2. This plot includes *OTA* V_{OUT}, V^+, V^-, VCO^+ at three different temperatures of 0, 62.5 and 125 °C.



a



b



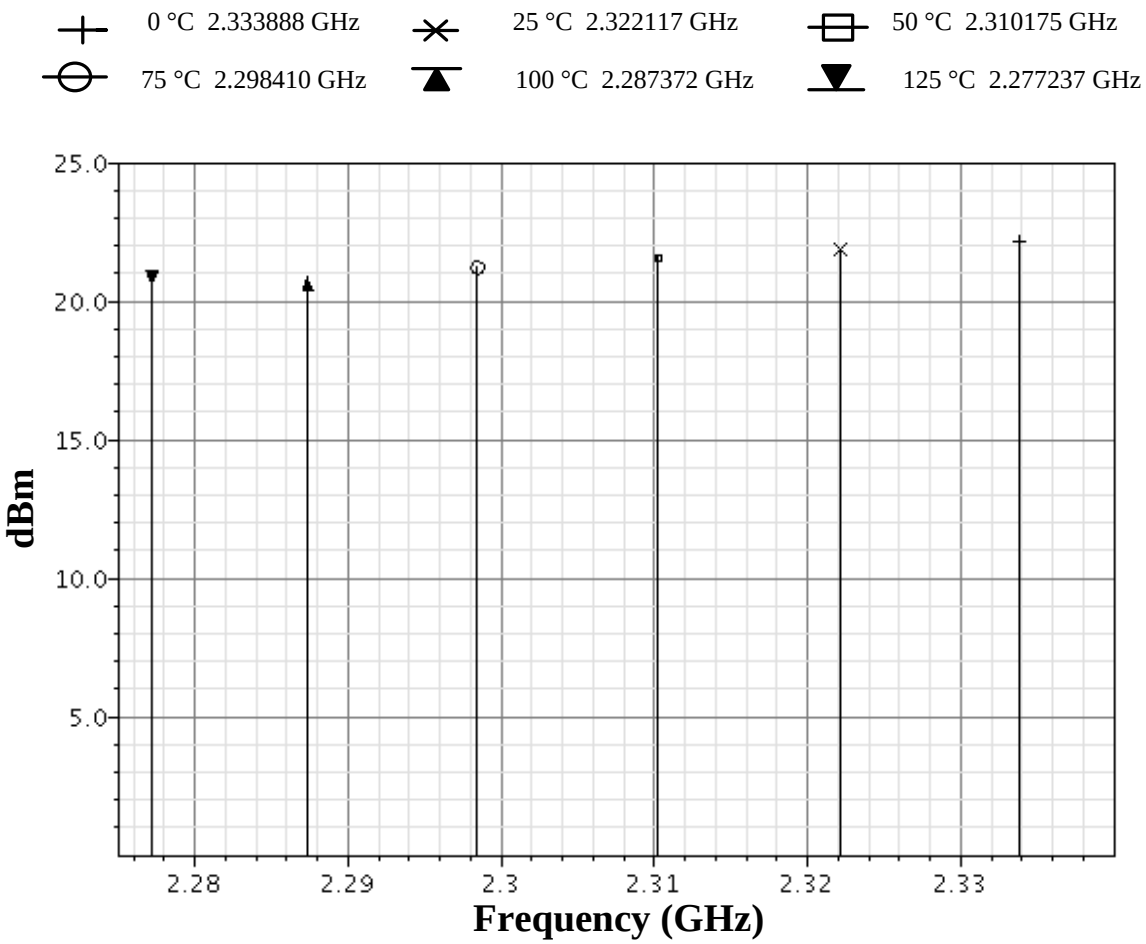
c

Figure 5.2 Waveforms observed at different points of block diagram in Fig. 3.10 using Spectre Simulator in Cadence a. at temperature 0 °C, b. at temperature 62.5 °C, c. at temperature 125 °C

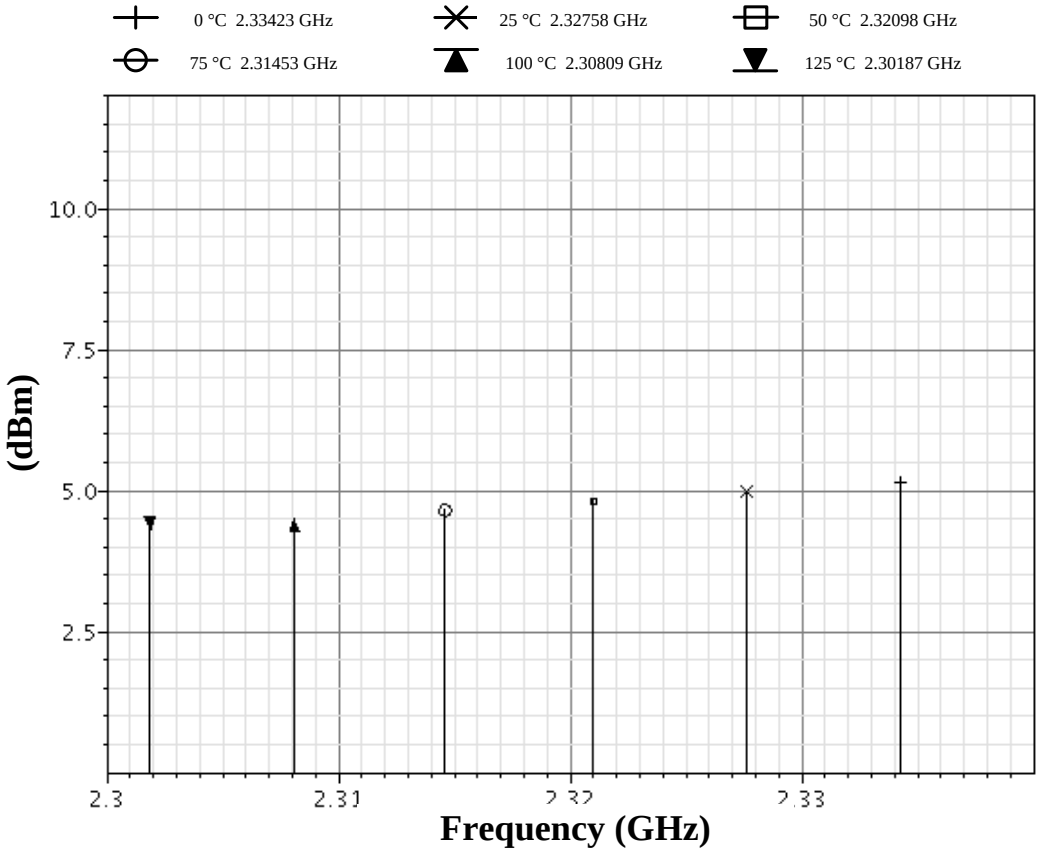
From Fig. 5.2 it is evident that as the temperature is varied, the closed loop action of the temperature compensated VCO forces V^+ and V^- to be closer so that the oscillation amplitude is stabilised. The OTA output illustrating the change in potential as a result of modified transconductance is described in section 2.7. This in turn confirms that the available transconductance is dynamically controlled by this compensation scheme.

Sections 2.4, 2.5, and 2.10 relate the frequency drift to the TC of the bias source. In order to verify the influence of the bias source on the performance of an open loop VCO, PSS simulations were performed on an oscillator directly supplied by a 3.3 V power supply first, and then connected to a current source with a negative TC such as in Fig. 2.4.

The results of the PSS analysis with temperature as parametric sweep variable at an interval of every 25 °C are presented in Fig. 5.3.



a



b

Figure 5.3 Frequency spread in an open loop VCO as a function of temperature, a. supplied directly from power supply, b. supplied using a current source with negative TC

In Fig. 5.3a the frequency spread is 56.65 MHz for a temperature sweep of 0 °C to 125 °C in five steps. Frequency spread for the VCO supplied using a current source with a negative TC demonstrates lower frequency drift of 32.36 MHz. It can also be noticed from this figure that the frequency drift in both cases are in a negative direction. This fact closes the argument made in section 2.7 that in an LC VCO the frequency drift is in a negative direction as the temperature is increased, and if supplied using a current source with a suitable amount of negative TC the frequency drift could be lower. It can be argued that the observed reduction in frequency drift is insufficient because the amount of negative TC of the current source is not designed specifically to compensate for the frequency drift.

The temperature compensated VCO is subjected to PSS analysis, over a temperature spread from 0 °C to 125 °C in five equal steps. The results of this simulation are provided in Fig. 5.4.

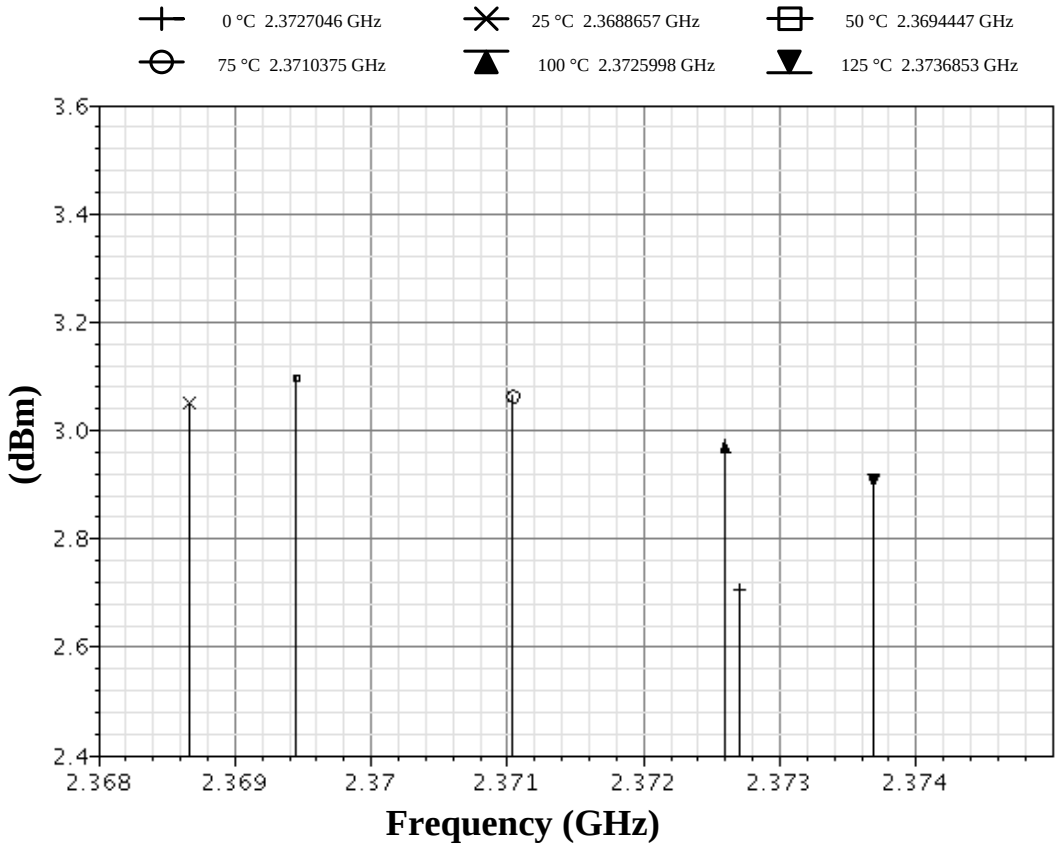


Figure 5.4 Illustration of frequency spread in the temperature compensated VCO

From Fig. 5.4 it can be observed that the total frequency spread has reduced to 4.82 MHz. It is worthwhile noticing that the frequency drift is in a negative direction between the temperatures of 0 and 25 °C. Between temperatures of 25 and 125 °C, the compensatory action of the amplitude loop limits the transconductance available to the VCO core, thereby reducing the frequency drift, as described in section 2.7. Table 5.2 compiles the results presented in Fig. 5.3 a, b, and 5.4 in five temperature intervals of 25 °C.

Table 5.2 Frequency compensation observed in five temperature intervals of 25 °C

Temperature interval (°C)	**Case 1 Δf (MHz)**	**Case 2 Δf (MHz)**	**Case 3 Δf (MHz)**
0 – 25	-11.76	-9.84	-3.787
25 – 50	-11.94	-9.31	0.5274
50 – 75	-11.77	-8.45	1.593
75 – 100	-11.04	-7.48	1.562
100 – 125	-10.14	-6.5	1.086

In Table 5.2, an open loop VCO is used for case 1 and case 2. The former is supplied directly from a power supply and the latter uses a current source with negative TC, as explained at the beginning of this section. Case 3 readings are taken using a temperature-compensated VCO. In case 1, in every temperature interval there is a consistent frequency shift in a negative direction. Case 2 is similar to case 1, but with a reduced amount of frequency shift, as expected. In case 3, in the first interval 0 to 25 °C there is reduced frequency shift of 3.787 MHz. This confirms that the closed loop action is effective in reducing the frequency drift. In the next four intervals of temperatures, the negative frequency shift is completely compensated for by this system; in fact it over-compensated for, resulting in a slight positive shift in frequency. It can also be concluded from Table 5.2 that the amplitude control action is not fully effective in the temperature range of 0 to 25 °C. This is due to the fact that at startup the amount of transconductance available to the VCO core is just sufficient to establish the Barkhausen criterion for self-starting oscillations, as mentioned in section 2.6.1. As the oscillation amplitude is much smaller than V_{GS} of transistors in AAC circuit, the amplitude control was not active. For the rest of the temperature intervals the AAC is active and explains the improved temperature compensation.

Three causes of the frequency drift mechanism in an *LC* oscillator are described in section 2.7. These are, in summary, net losses in the inductor, net losses in the capacitor and the change in harmonic content of the bias current *i(t)*. Of the three variables, the first two remained as constants, as the same VCO is used in the simulation. Therefore it can be concluded that if frequency spread is diminished, there is less injection of harmonic content *i(t)* into the tank. A well-regulated oscillation amplitude in this design must have kept the bias current near constant value, which results in a minimum shift in oscillation frequency.

In order to account for the effects of process variation on frequency spread, PSS simulation is repeated over nine process corners; the summary of the results is provided in Table 5.3.

Table 5.3 depicts the frequency compensation obtained at nine process corners in simulation

Corners	***Δf* (MHz)**	**Frequency drift (ppm/°C)**
0	4.768	15.89
1	13.80	46
2	49.94	166.5
3	14.90	49.67
4	27.74	92.47
5	22.80	76
6	29.02	96.73
7	24	80
8	35.31	117.7

In table 5.3 the frequency drift is calculated as

$$\boldsymbol{Frequency\ drift} = \frac{\Delta \boldsymbol{f} \times \mathbf{10^6}}{\Delta \boldsymbol{T} \times \boldsymbol{f_o}}$$

where, ΔT is the temperature sweep, and f_o is the centre frequency of the VCO.

Table 5.3 confirms that the typical mean corner yields the best frequency compensation, while corner 2 performs worst. The values provided in Table 5.3 correspond to V_{ID} = 800 mV in Fig. 4.6.

5.3.2 Experimental measurements

The result presented in section 5.3.1 describes how amplitude control is effective in reducing frequency drift. It also illustrates why amplitude control is not fully active in the first temperature interval. However the fabricated IC did not respond to the variation in temperature as expected. In order to establish why frequency compensation has not been achieved, and to explain why the power output from the IC is very low compared to the expected results as provided in Table 5.1 under case 3, one needs to isolate the individual subsystems that constitute the IC. The oscillator and the buffer stage are ruled out as sinusoidal output is present from the IC. PLS is performed on subsystems AAC, OTA, and the voltage reference circuits.

5.4 PLS

PLS provides an effective platform to compare schematic design results with those of an extracted netlist generated from the layout design. Usually parasitic effects associated with the layout design affects the response of the design in comparison to that of the schematic. In this study, PLS is used as a diagnostic tool to verify the causes of unexpected circuit operation.

In order to facilitate PLS a new schematic view is created; with two instances of the same circuit. One of the instances is assigned to a schematic netlist while the second one is assigned to the extracted netlist using '`Config View`' in Cadence Virtuoso.

5.4.1 AAC

The schematic view of the AAC is prepared for the PLS. Supply voltage V_{DD} and the two bias voltages required are supplied using sources V_0, V_1, and V_2. The schematic used is depicted in Fig. 5.5.

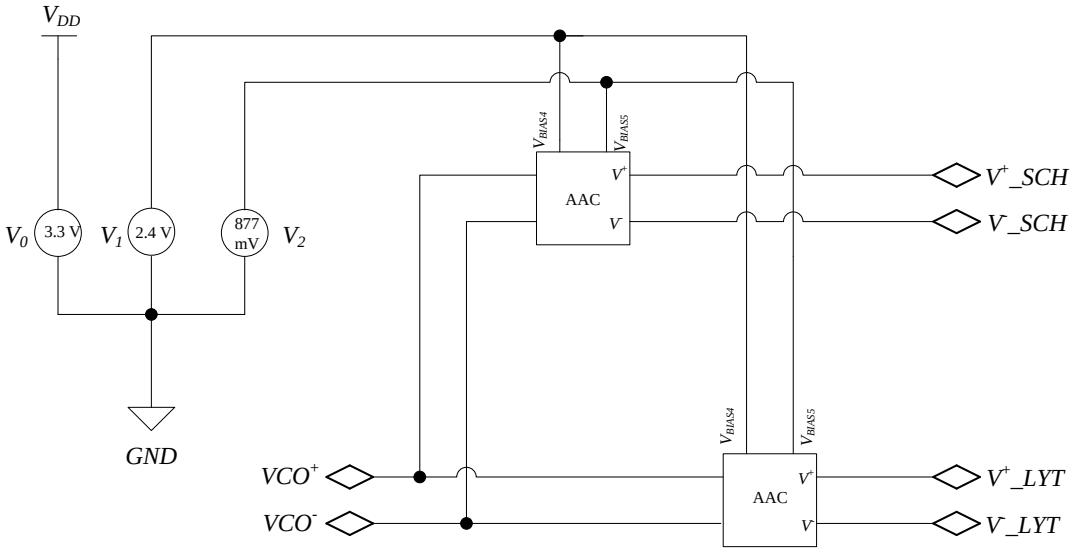


Figure 5.5 Schematic view of the AAC prepared for PLS

In Fig 5.5, the two terminals labelled V^+_SCH and V^-_SCH represent schematic outputs. The remaining two terminals labelled V^+_LYT and V^-_LYT represent outputs generated by simulating the extracted netlist from the layout. The stimulus provided at the input is sinusoidal of 2.4 GHz frequency with a peak of 1 V, 180° out of phase with each other. The four output waveforms observed are provided together with the two input waveforms in Fig. 5.6.

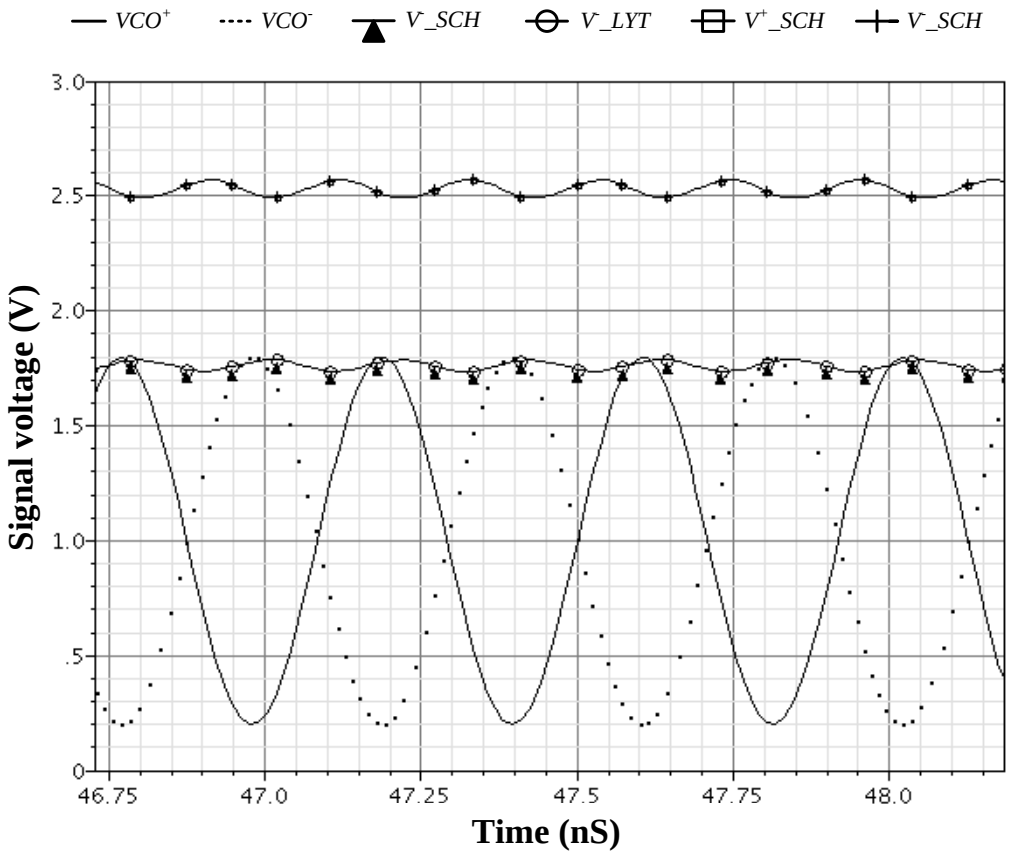


Figure 5.6 The input and output waveforms observed in PLS of AAC

From Fig. 5.6, it is evident that the output from the schematic (V^+_SCH) is overlapping the output from the layout (V^+_LYT). It can also be noted that the voltage V^+ is higher than that of V^-, as expected. This PLS confirms that the AAC is working in exactly the manner it was designed for.

5.4.2 OTA

PLSs are subsequently performed on OTA to verify its operation. The result of the AC analysis is depicted in Fig. 5.7.

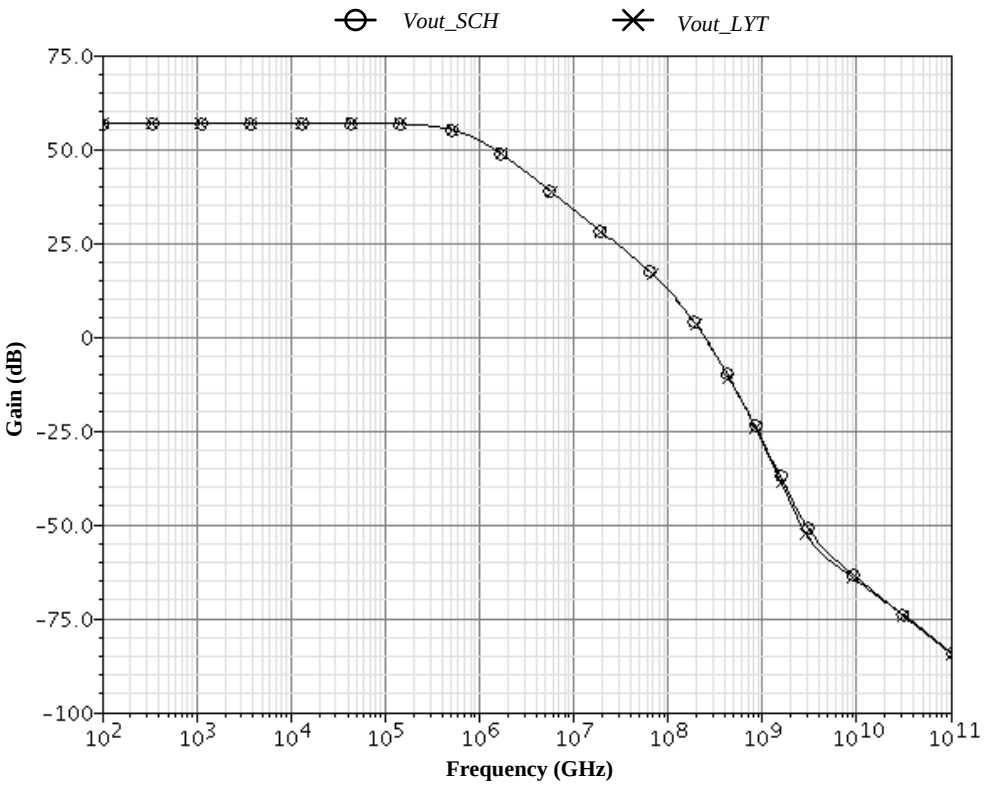


Figure 5.7 Results of AC analysis in PLS of OTA

In Fig 5.7, the layout output follows that of the schematic, yielding a gain of 56 dB as expected. There is a minute dissociation between the two outputs between 1 GHz and 10 GHz. In comparison, between the outputs of schematic versus layout, it could be concluded that the OTA is working perfectly.

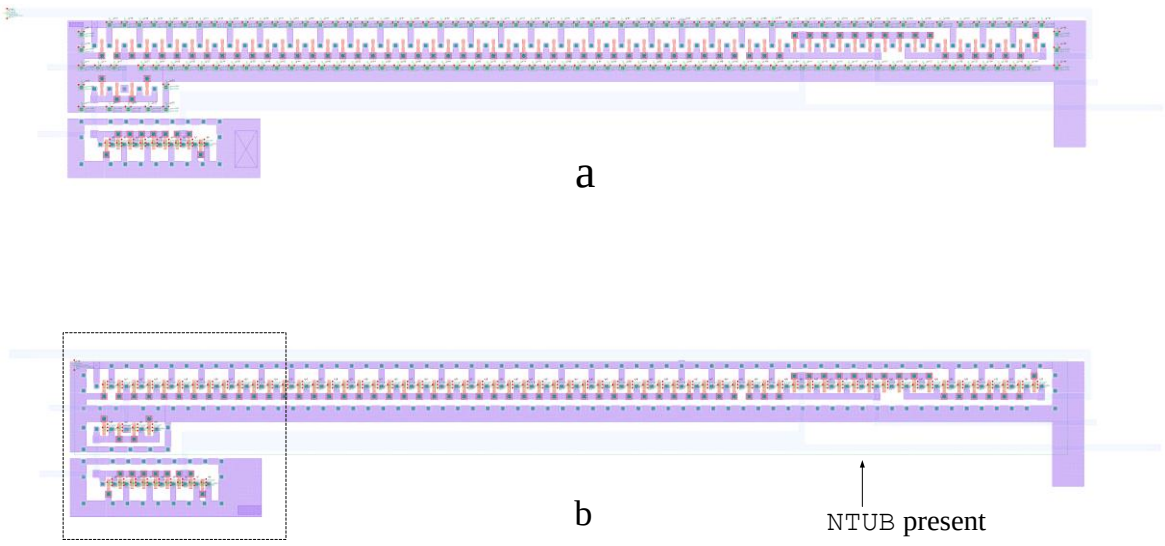
5.4.3 Bias voltage generation

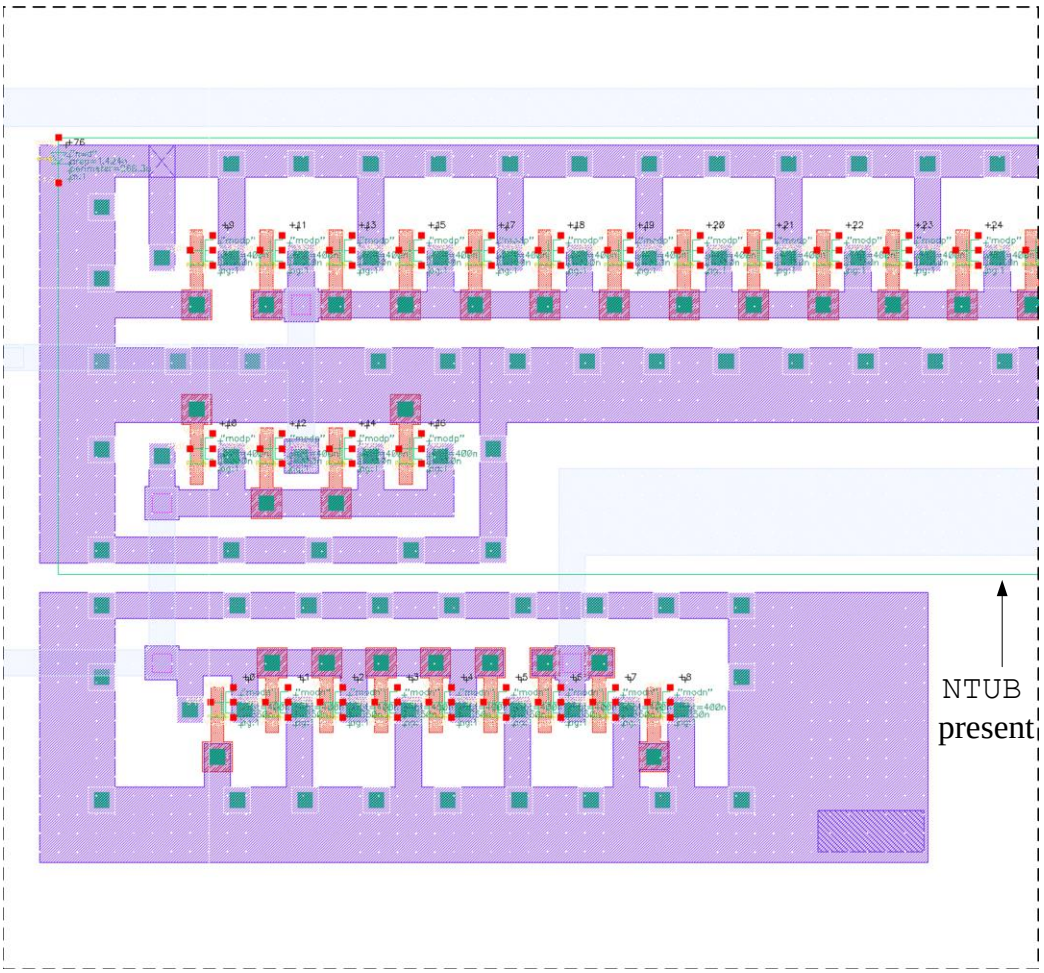
The next block to be verified is the reference voltage generator circuit. DC operating point analysis is performed using the schematic and extracted view using '`Config View`' in Cadence. The results are listed in Table 5.4

Table 5.4 List of bias voltages generated by schematic versus layout

Bias Voltage	Schematic (V)	Layout (V)
V_{BIAS1}	0.727	2.488
V_{BIAS2}	2.375	0
V_{BIAS3}	2.240	0
V_{BIAS4}	0.877	2.477
V_{BIAS5}	2.119	0

PLS on AAC, and OTA was found acceptable, but next on voltage reference circuit clarifies that the voltages generated are incorrect as presented in Table 5.4. An initial examination of the bias voltage generation circuit illustrated in Fig. 4.12 discloses that all voltages generated by PMOS devices are shorted to ground. This information has led to further investigation of the circuit. An LVS performed exposed that the NTUB layer, where PMOS transistors are drawn, was missing. This is not noticeable from the layout itself, as the NTUB layer is always concealed by the FIMP layer in the ams AG process. However, the extracted layout exposes the NTUB in a green rectangle. The absence of the green rectangle around the PMOS confirms the missing NTUB in Fig. 5.8a.





c

Figure 5.8 Layout of voltage reference circuit drawn in Cadence Layout Editor; a. no NTUB present, b. NTUB present, taken from original drawing to indicate the absence of NTUB in a, c. enlarged view of the selected area in rectangle in b

Fig. 5.8 confirms that NTUB is missing in the layout of the voltage reference circuit and all the PMOS transistors are not active. Furthermore there are vias connecting the expected NTUB to $V_{DD,}$ cause short circuit to ground, and explains the higher power consumption, and low output power.

The impact of failure to generate correct bias voltages is multifold. Transistor M_0 of OTA will be biased several times more than the required value. The current sources of the OTA are implemented using PMOS transistors are in triode region, and the NMOS loading stage remains in triode, little gain possible, explains lack of frequency drift compensation.

V_{BIAS4}, and V_{BIAS5} are used to bias the transistors in AAC. However, the presence of a voltage bias (V_{BIAS4}) on the NMOS transistors results in generating a voltage V^+ higher than V^- and the OTA still generates a positive voltage at its output. A positive voltage at the gate of M_{CNTRL} switches on VCO as in Fig. 3.6 and oscillations are present at the output. However, no temperature compensation was possible, as OTA could not generate sufficient voltage gain.

5.5 CONCLUSION

The set of research questions mentioned in Chapter 1 are answered in Chapter 2, as various factors contributing to the frequency drift are listed in section 2.7. It was also identified in Chapter 2 that mobility and the threshold of the MOS devices are contributing to frequency shift are not cumulative. Therefore a ZTC bias point was positively identified. In order to compensate for the frequency drift, an amplitude control method was proposed in this study.

The hypothesis mentioned in Chapter 1 claims, “If selected factors that contribute to frequency drift in an LC VCO as a result of temperature variations are identified, it is possible to reduce the influence of temperature by controlling the frequency drift dynamics”.

In this study the frequency drift of the LC VCO is reduced to 15.89 ppm/°C from an uncompensated value of 189 ppm/°C using ZTC bias and an AAC circuit that reduces the amplitude-to-frequency conversion.

CHAPTER 6 CONCLUSION

6.1 INTRODUCTION

In Chapter 1 of this dissertation, which describes the context of the research problem, research questions are raised and the hypothesis is articulated and justified in comparison with recently published works relating to temperature compensation. A broad literature survey is reported in Chapter 2 of this work, identifying possible variables and the way in which these contribute to the problem of frequency drift. A number of possible answers to the research questions are identified and a unique combination of solutions is suggested for validating the hypothesis.

The methodology followed in verifying the hypothesis is described in Chapter 3, which concludes with a system design representing the conceived ideas. Chapter 3 also describes the selection of a technology node for the implementation of the idea into silicon IC. In Chapter 4, each section of the block diagram is translated into a corresponding schematic and simulated using the models available for the corresponding technology node. A layout of the schematic is then prepared and verified further using DRC and LVS features available with Cadence Virtuoso.

Measured data using the prototyped IC is verified in Chapter 5, together with the simulation results. Close correspondence between simulations versus experimental results is observed. Further PLS is also performed to explain the unexpected results. Chapter 6 verifies whether the research questions have been completely substantiated, checks the validity of the hypothesis and closes this dissertation.

6.2 CONCLUSIONS ABOUT RESEARCH QUESTIONS AND HYPOTHESIS

The primary and secondary research questions are repeated here for convenient reference. Primary research question:

> How is it possible to compensate for *frequency drift* in LC VCO as a result of temperature variations?

Secondary research questions:

- What are the different factors affecting frequency drift of an LC oscillator as a result of temperature variations?
- How are the individual variables contributing to the dynamics of frequency drift? Are any two variables noncumulative?
- How is it possible to reduce the influence of these variables on frequency drift?

6.2.1 WHAT ARE THE DIFFERENT FACTORS AFFECTING FREQUENCY DRIFT?

The variables affecting frequency drift as a result of temperature variance are mobility of charge carriers in the semiconductor (μ), the threshold voltage of transistors (V_t), the net losses in the inductor (R_L), net losses in the capacitor (R_C), and the injection of harmonic content of the bias current *i(t)* into the tank. In Chapter 5 it was verified that frequency drift reduces when amplitude control is used, and it could be concluded that the variables identified are in fact causing the frequency drift.

6.2.2 ARE ANY TWO VARIABLES CONTRIBUTING TO FREQUENCY DRIFT NONCUMULATIVE

Negative TC is associated with μ, and V_t, are non-cumulative. A ZTC bias point of current was positively identified and was used in the design of an LC oscillator.

6.2.3 HOW IS IT POSSIBLE TO REDUCE THE INFLUENCE OF THESE VARIABLES ON FREQUENCY DRIFT?

A ZTC bias current is used to reduce influence of μ, and V_t. However R_L, R_C, and *i(t)* still contribute to the negative TC. Measured results display much better frequency stability, reconfirming that AAC limits the injection of harmonic current into the tank. Therefore it can be concluded that by holding the oscillation amplitude to a near constant value, injection of harmonic component of bias current had in fact been suppressed.

This also means that the first two variables, R_L and R_C, are still contributing to frequency drift, but at a much lower levels. Therefore it can also be concluded that the contribution of losses in the tank to frequency drift is made indirectly through perturbation in oscillation amplitude, which is held fairly constant.

6.3 CONCLUSIONS ABOUT RESEARCH PROBLEM

The hypothesis is repeated again for convenient reference.

> "If selected factors that contribute to the frequency drift as a result of temperature variations in an LC VCO are identified, it is possible to reduce the influence of temperature by controlling the frequency drift dynamics".

The selected factors that contribute to the frequency drift are negative TC of mobility and threshold voltage, and the harmonic component of the bias current that is injected into the tank circuit of the *LC* oscillator. As selected in Chapter 2, AAC is used to hold the amplitude constant and prevent the effect of harmonic injection. By taking into account the amount of frequency compensation reported in Chapter 5 (16 ppm/°C) over a temperature range of 0 to 125 °C, it could also be concluded that even the contribution of net losses in the tank to frequency drift are reduced. This in turn means that even losses in the tank contributing to frequency drift are indirectly converted into perturbations in the oscillation amplitude.

6.4 IMPLICATIONS FOR THEORY

At the end of Chapter 2, the existing body of knowledge suggests that the origins of frequency drift in LC VCO are net losses in the inductor, net losses in the capacitor, and the injection of harmonic content of bias current into the tank. Furthermore, the drain current expression of a MOS transistor has two components, namely mobility of the carriers and the threshold voltage, which demonstrate a negative TC. However, a ZTC bias point is available.

The accepted method of temperature compensation in the present body of knowledge is well illustrated in Table 1.1 in section 1.3. In LC oscillators one needs to generate a current or voltage that accurately represents the frequency deviation, and use it to generate V_{CNTRL} to be used as a compensating voltage to reduce the frequency drift. Improved compensation is obtained when the compensation voltage is identical to the non-linear frequency profile of the varactors. Several authors suggest amplitude control as a means of reducing phase noise. Some authors use amplitude control in improving the immunity of the oscillator against PVT in general. However, this study suggests that amplitude control is effective in reducing the frequency drift by limiting the amplitude to frequency conversion.

In this work the use of ZTC bias current has improved the frequency stability better than 50 ppm/°C. Further stability improvement is obtained using amplitude control. It could be concluded that better temperature compensation could be obtained if any compensation scheme should be preceded by amplitude control.

6.5 LIMITATIONS AND FURTHER RESEARCH

6.5.1 Limitations

The amount of frequency stability achieved is in comparison with recently published work referred to in Table 1.1. However, the results obtained in this work are limited to very narrow temperature ranges in applications such as Ethernet, where the required amount of stability is within ±100 ppm. Modern applications, such as Bluetooth, demand much better accuracy and combination of amplitude control and electronic tuning may be required.

6.5.2 Further research

A few suggestions for future work emanate from this dissertation:

- Several authors state that PMOS transistors offer better immunity against phase noise, 1/f noise etc. A PMOS device used as the M_{CNTRL} could improve the phase noise performance.

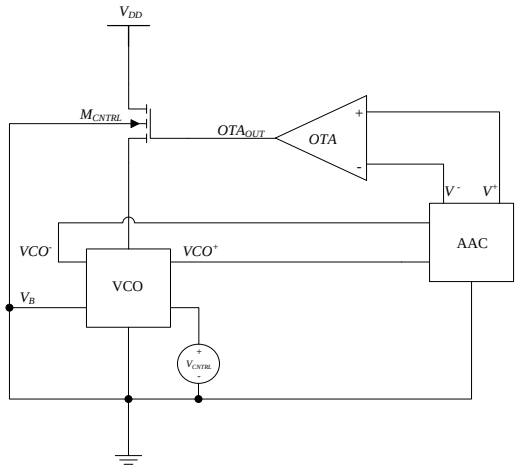


Figure 6.1 A simplified block diagram of the temperature compensated VCO

- The OTA input stage could be designed using PMOS transistors, as PMOS input stages offer better phase noise performance.
- OTA makes use of three bias reference voltages. This dissertation made use of a MOS transistor network to generate them. It could be better if all voltage references should be more immune to temperature variations such as PTAT sources.

REFERENCES

[1] G. De Vita and G. Innaccone, "A Sub-1-V, 10 ppm/°C, Nanopower Voltage Reference Generator," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 7, pp. 1536-1542, Jul. 2007.

[2] G. Serrano and P. Hassler, "A Presicion Low-TC wide-Range CMOS Current Reference," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 558-565, Feb. 2008.

[3] H. M. Lavasani, W. Pan, B. P. Harrington, R. Abdolvand and F. Ayazi, "Electronic Temperature Compensation of Lateral Bulk Accoustic Resonator Reference Oscillator Using Enhanced Series Tuning Technique," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 6, pp. 1381-1393, Jun. 2012.

[4] I-C. Hwang, "A 0.236 mm^2, 3.99 mW Fully Integrated 90 nm CMOS L1/L5 GPS Frequency Synthesizer Using a Regulated Ring VCO," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 6, pp. 324-326, Jun. 2012.

[5] W-H Chen, W-F. Loke, and B. Jung, "A 0.5 V, 440-µW Frequency Synthesizer for Implantable Medical Devices," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 8, pp. 1896-1907, Aug. 2012.

[6] P-W. Chen, T-Y. Lin, L-W. Ke, R. Yu, M-D. Tsai, S. Yeh, Y-B. Lee, B. Tzeng, Y-H. Chen, S-J. Huang, Y. -H. Lin, and G. -K. Dehng, "A 0.13 *µm* CMOS Quad-Band GSM/GPRS/EDGE RF Transceiver Using a Low-Noise Fractional-N Frequency Synthesizer and Direct-Conversion Architecture," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1454-1463, May 2009.

[7] Y. Tokunaga, S. Sakiyama, A. Matsumoto, and S. Dosho, "An On-Chip CMOS Relaxation Oscillator With Voltage Averaging Feedback," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1150-1158, Jun. 2010.

[8] M. S. McCorquodale, G. A. Carichner, J. D. O' Day, S. M. Pernia, S. Kubba, E. D. Marsman, J. J. Kuhn, and R. B. Brown, "A 25-MHz Self-Referenced Solid-State

Frequency Source Suitable for XO-Replacement," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 5, pp. 943-956, May 2009.

[9] S. Rai, Y. Su, W. Pang, R. Rubi, and B. Otis, "A Digitally Compensated 1.5 GHz CMOS/FBAR Frequency Reference," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 57, no. 3, pp. 552-561, Mar. 2010.

[10] M. H. Perrot, S. Pamarti, E. G. Hoffman, F. S. Lee, S. Mukherjee, C. Lee, V. Tsinker, S. Perumal, B. T. Soto, N. Arumugham, and B. W. Garlepp," A Low Area, Switched-Resistor Based Fractional -N Synthesizer Applied to a MEMS-Based Programmable Oscillator, "*IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2566-2581, Dec. 2010.

[11] K. Sundaresan, G. K. Ho, S. Pourkamali, and F. Ayazi, "Electronically Temperature Compensated Silicon Bulk Accoustic Resonator Reference Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1425-1433, Jun. 2007.

[12] T. Djerafi, K. Wu and D. Deslandes, "Temperature Drift Compensation Technique for Substrate Integrated Waveguide Oscillator," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 9, pp. 489-491, Sept. 2012.

[13] J. Bae, L. Yan, and H-J. Yoo, "A Low Energy Injection-Locked FSK Transceiver With Frequency-to-Amplitude Conversion for Body Sensor Applications," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 928-937, Apr. 2011.

[14] C. A. Marquart, T. Zourntos, S. Magierowski, and N. J. Mathai, "Sliding-Mode Amplitude Control Techniques for Harmonic Oscillators," *IEEE Transactions on Circuits and Systems –II: Express Briefs*, vol. 54, no. 11, pp. 1014-1018, Nov. 2007.

[15] T-H. Lin, R-L. Hsu, C-L. Li and Y-C. Tseng, "A 5 GHz, 192.6 dBc/Hz/mW FOM, LC – VCO System with Amplitude Control Loop and LDO Voltage Regulator in 0.18 μm CMOS," *IEEE Microwave and Wireless Components letters*, vol. 17, no. 10, pp. 730-732, Oct. 2007.

[16] L. He, Y. P. Xu, and M. Palaniapan, "A CMOS Readout Circuit for SOI Resonant Accelerometer with 4-μg Bias Stability and 20-$\mu g/\sqrt{Hz}$ Resolution," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1480-1490, Jun. 2008.

[17] J. Chen, F. Jonsson, M. Carlsson, C. Hedenäs, and L-R. Zheng, "A Low Power, Startup Ensured and Constant Amplitude Class-C VCO in 0.18 *μm* CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 8, pp. 427-429, Aug. 2011.

[18] K. M. Hussein and E. Hegazi, "An All-Analog Method to Enhance Amplitude Stability in Pierce Crystal Oscillators," *IEEE Transactions on Circuits and Systems – Regular Papers*, vol. 59, no. 3, pp. 463-470, Mar. 2012.

[19] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed. New York: John Wiley & Sons, Inc., 2010.

[20] I. M. Filanovsky and A. Allam, "Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits," *IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications*, vol. 48, no. 7, pp. 876-884, Jul. 2001.

[21] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Boston, MA: Artech House Inc., 2002.

[22] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 2nd ed., New York: IEEE Press/Wiley-Interscience, 2005.

[23] Y. Leblebici and D. Leblebici, *High-Frequency CMOS Analog Intergrated Circuits*. New York: Cambridge University Press, 2009.

[24] B. Razzavi, *Design of Analog CMOS Integrated Circuits*, New York: McGraw-Hill, 2001.

[25] D. Hauspie, E-C. Park, and J. Craninckx, "Wideband VCO with Simultaneous Switching of Frequency Band, Active Core, and Varactor Size," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 7, pp. 1472-1480, Jul. 2007.

[26] S-L. Jang, Y-K. Wu, C-C. Liu and J-F. Huang, "A Dual-Band CMOS Voltage-Controlled Oscillator Implemented with Dual-Resonant LC Tank," *IEEE Microwave and Wireless Components letters*, vol. 19, no. 12, pp. 816-818, Dec. 2009.

[27] Q. Zou, K. Ma, K. S. Yeo, and W. M. Lim, "Design of a Ku-Band Low-Phase-Noise VCO Using the Dual *LC* Tanks," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 59, no. 5, pp. 262-266, May 2012.

[28] G. Li and E. Afshari "A Distributed Dual-Band LC Oscillator Based on Mode Switching," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 1, pp. 99-107, Jan. 2011.

[29] J. Li and S. M. R. Hasan, "Pulse-Biased Low-Power Low-Phase-Noise UHF LC-QVCO for 866 MHz RFID Front-End," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 10, pp. 3120-3125, Oct. 2012.

[30] P. Ruippo, T. A. Lehtonen, and N. T. Tchamov, "An UMTS and GSM Low Phase Noise Inductively Tuned LC VCO," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 3, pp. 163-165, Mar. 2010.

[31] K-W. Cheng and M. Je, "A Current-Switching and g_m-Enhanced Colpitts Quadrature VCO," *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 3, pp. 143-145, Mar. 2013.

[32] Y. -J. Moon, Y. -S. Roh, C. -Y. Jeong, and C. Yoo, "A 4.39 - 5.26 GHz LC-Tank CMOS Voltage-Controlled Oscillator with Small VCO-Gain Variation," *IEEE Microwave and Wireless Components letters*, vol. 19, no. 8, pp. 524-526, Aug. 2009.

[33] A. Italia, C. M. Ippolito, and G. Palmisano, "A 1-mW 1.13 – 1.9 GHz CMOS LC VCO Using Shunt-Connected Switched-Coupled Inductors," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 6, pp. 1145-1155, Jun. 2012.

[34] H-H. Hsieh and L-H. Lu, "A High-Performance CMOS Voltage-Controlled Oscillator for Ultra-Low Voltage Operations," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 3, pp. 467-473, Mar. 2007.

[35] B. Soltanin, H. Ainspan, W. Rhee, D. Friedman and P. R. Kinget, "An Ultra-Compact Differentially Tuned 6-GHz CMOS LC-VCO with Dynamic Common-Mode Feedback," *IEEE Journal of Solid-State Cicruits*, vol. 42, no. 8, pp. 1635-1641, Aug. 2007.

[36] M. S. McCorquodale, J. D. O' Day, S. M. Pernia, G. A. Carichner, S. Kubba, and R. B. Brown, "A Monolithic and Self-Referenced RF *LC* Clock Generator Compliant with USB 2.0," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 385-399, Feb. 2007.

[37] P. Ward and A. Duwel, "Oscillator Phase Noise: Systematic Construction of an

Analytical Model Encompassing Nonlinearity," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 58, no. 1, pp. 195-205, Jan. 2011.

[38] A. Tasić, W. A. Serdijn, and J. R. Long, "Spectral Analysis of Phase Noise in Bipolar LC-Oscillators – Theory, Verification, and Design," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 57, no. 4, pp. 737-751, Apr. 2010.

[39] C. P. Yue and S. S. Wong, "Physical Modelling of Spiral Inductors on Silicon," *IEEE Transactions on Electron Devices*, vol. 47, no. 3, pp. 560-568, Mar. 2000.

[40] D. Park and S. Cho, "Design Techniques for Low-Voltage VCO with Wide Tuning Range and Low Sensitivity to Environmental Variations," *IEEE Transactions on Microwave Theory andd Techniques*, vol. 57, no. 4, pp. 767-774, Apr. 2009.

[41] K. Uneo, T. Hirose, T. Asai, and Y. Amemiya, "A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Rreference Circuits Consisting of Subthreshold MOSFETs," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 2047-2053, Jul. 2009.

[42] H. Kayahan, Ö. Ceylan, M. Yazici, S. Zihir, and Y. Gurbuz, "Wide Range, Process and Temperature Compensated Voltage Controlled Current Source," *IEEE Transactions on Circuits and Systems –I: Regular Papers*, vol. 60, no. 5, pp. 1345-1353, May 2013.

[43] K. Sundaresan, P. E. Allen and F. Ayazi, "Process and Temperature Compensation in a 7-MHz CMOS Clock Oscillator," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 433-442, Feb. 2006.

[44] S. V. Kumar, C. H. Kim, S. S. Sapatnekar, "Body Bias Voltage Computations for Process and Temperature Compensation," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 16, no. 3, pp. 249-262, Mar. 2008.

[45] J-S. Yuan and S. Chen, "A Simulation Study of Colpitts Oscillator Reliability and Variability," *IEEE Transactions on Device and Materials Reliability*, vol. 12, no. 3, pp. 576-581, Sept. 2012.

[46] H. Mostafa, M. Anis, and M. Elmasry, "A Novel Low Area Overhead Direct Adaptive Body Bias (D-ABB) Circuit for Die-to-Die and Within-Die Variations Compensation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 10, pp. 1848-1859, Oct. 2011.

[47] D. Gomes, M. Sroka, and J. L. G. Jimenéz, "Process and Temperature Compensation for RF Low-Noise Amplifiers and Mixers," *IEEE Transactions on Circuits and Systems – I: Regular Paperes*, vol. 57, no. 6, pp. 1204-1211, Jun. 2010.

[48] W. Deng, K. Okada and A. Matsuzawa, "Class-C VCO with Amplitude Feedback Loop for Robust Start-Up and Enhanced Oscillation Swing," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 429-440, Feb. 2013.

[49] J. Burghartz, D. C. Edelstein, M. Soyuer, H. A. Ainspan and K. A. Jenkins, "RF Circuit Design Aspects of Spiral Inductors on Silicon," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2028-2034, Dec. 1998.

[50] Cadence Design Systems. (2009, May) [Online]. www.cadence.com

[51] ams AG. (2009) [Online]. http//:www.ams.com

[52] F. Silveira, D. Flandre, P. Jespers, "A g_m/I_D Methodology for Design of Analog Circuits and Its Application to the Synthesis of a Silicon-on Insulator Micropower OTA," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314-1319, Sept. 1996.

[53] B. Boser. (2011, Dec.) Analog Design Using g_m/I_D and f_t Metrics. [Online]. http://www.eecs.berkeley.edu

[54] D. Yang, Y. Ding, and S. Huang, "A 65-nm High-Frequency Low-Noise CMOS Based RF SoC Technology," *IEEE Transactions on Electron Devices* , vol. 57, no. 1, pp. 328-335, Jan. 2010.

[55] Y-J. Chan C-F. Huang, C-C. Wu, C-H. Chen and C-P. Chao, "Perfomance Consideration of MOS and Junction Diodes for Varactor Application," *IEEE Transactions on Electron Devices*, vol. 54, no. 9, pp. 2570-2573, Sept. 2007.

[56] D. Miyashita, H. Ishikuro, S. Kousai, H. Kobayashi, H. Majima, K. Agawa and M. Hamada, "A Phase Noise Minimisation of CMOS VCOs over Wide Tuning Range and Large PVT Variations," in Proceedings of the *IEEE Custom Integrated Circuits Conference*, San Jose, CA, 18 – 21 Sept. 2005, pp. 583-586.

[57] R. S. Assaad, J. S. -Martinez, "The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2535-2542, Sept. 2009.

[58] S. V. Thyagarajan, S. Pavan, and P. Sankar, "Active-RC Filters Using the Gm Assisted OTA-RC Technique," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1522-1533, Jul. 2011.

[59] S. Y. Kim, S. Baytok, and K. Roy, "Thin-Box Poly Si Thin-Film Transistors for CMOS-Compatible Analog Operations," *IEEE Transactions on Electron Devices*, vol. 58, no. 6, pp. 1687-1695, Jun. 2011.

[60] F. Mortan and L. Wright, "56-Pin Quad Flatpack No-Lead Logic Package," Texas Instruments, Dallas, Application Report SCEA032, 2003. [Online]. http://www.ti.com

[61] T. S. Laverghetta, "Microwave Materials," in *Practical Microwaves*. Indianapolis, Indiana, USA: Prentice Hall, Inc., Feb. 1996, ch. 1.

[62] B. B. Steer T. C. Edwards, *Foundations of Interconnects and Microstrip Design*, 3rd ed. New York: John Wiley & Sons, Ltd, 2000.

[63] Rogers Corporation. (Apr. 2000) Home Page [Online]. http://www.rogerscorp.com